


# LCFC Confidential

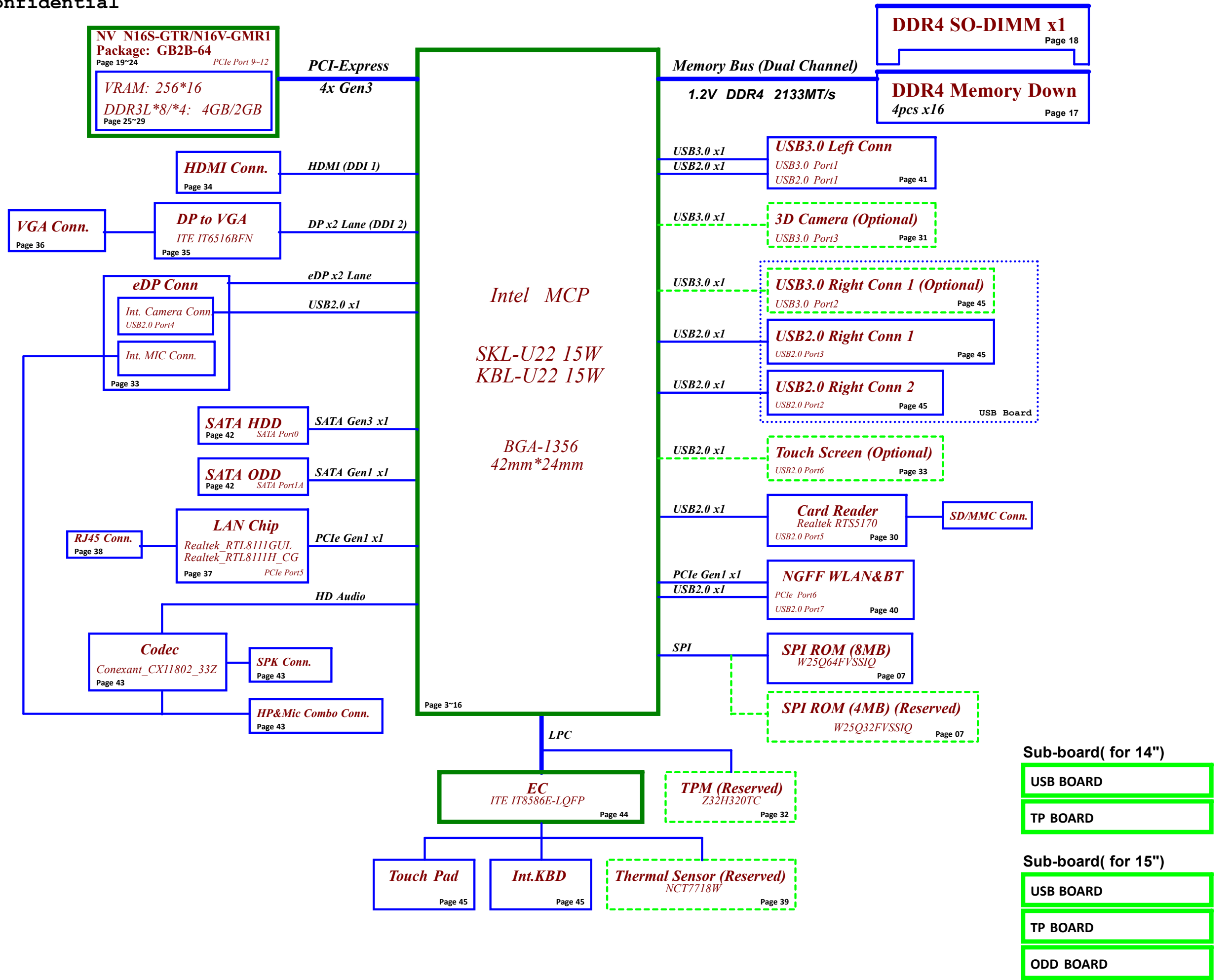
## CG411/CG511 MB Schematics Document

Intel Skylake-U22/Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2016-01-09

REV: 1.0

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- Sub-board( for 14")**
- USB BOARD
  - TP BOARD
- Sub-board( for 15")**
- USB BOARD
  - TP BOARD
  - ODD BOARD

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**Voltage Rails ( O --> Means ON , X --> Means OFF )**

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function	BOM Structure	BTO Item
USB3.0	1	USB3.0 Conn Left	@
	2	USB3.0 Conn Right(optional)	14@
	3	3D Camera(optional)	15@
	4	NC	14or15@
	5	NC	14or17@
	6	NC	
USB2.0	1	USB3.0 Conn Left	
	2	USB2.0 Conn1 Right	Cannonlake@
	3	USB2.0 Conn2 Right	CD@
	4	Camera	DUALMIC@
	5	Cardreader	EMC@
	6	Touch Panel	EMC_15@
	7	Bluetooth	EMC_NS@
	8	NC	EMC_PX@
	9	NC	EMC_PXNS@
	10	NC	ES@
PCIE	1	NC	EXO@
	2	NC	
	3	NC	ME@
	4	NC	NTS@
	5	LAN	
	6	WLAN	
	7	used as SATA	
	8	used as SATA	
	9~12	DGPU	PX@
	X4 PCIE		RANKA@
			RANKB@
			Realtek_SD@
SATA	0	HDD	SINGLEMIC@
	1A	ODD	SINGLERANK@
	1B	used as PCIE	DUALRANK@
	2	used as PCIE	TS@
			TPM@
		UMA@	

**SMBUS Control Table**

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

**EC SMBus1 address**

**EC SMBus2 address**

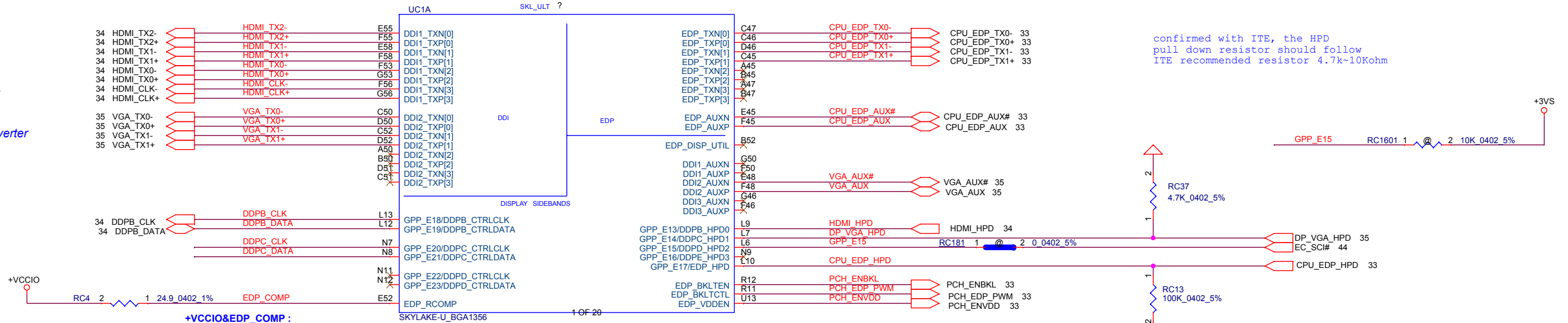
**EC SMBus3 address**

**PCH SM Bus address**

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update	Wlan	Reserved		
		DGPU	need to update				

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HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK  
  
DP TO VGA Converter



confirmed with ITE, the HPD pull down resistor should follow ITE recommended resistor 4.7k-10kOhm

+VCCIO&EDP\_COMP :  
Trace Width: 20mil  
Isolation Spacing: 25mil  
Max length: 100mil

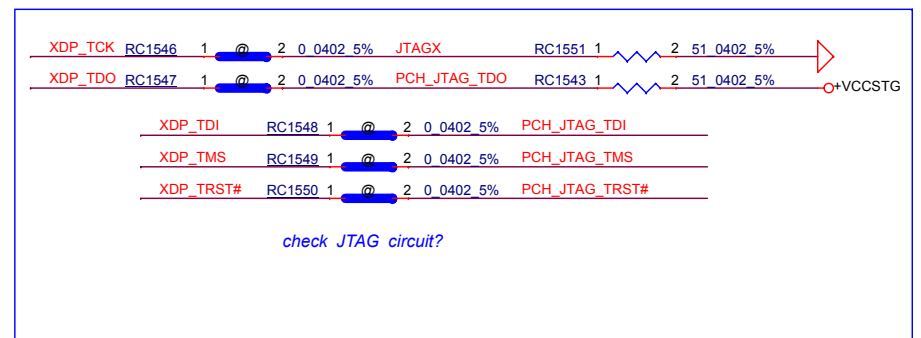
check PROCHOT# circuit with PWR

check H\_THRMTRIP# if need to connector to EC

check DDPC\_CLK pull high or not?

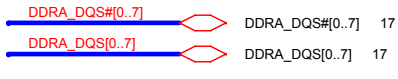
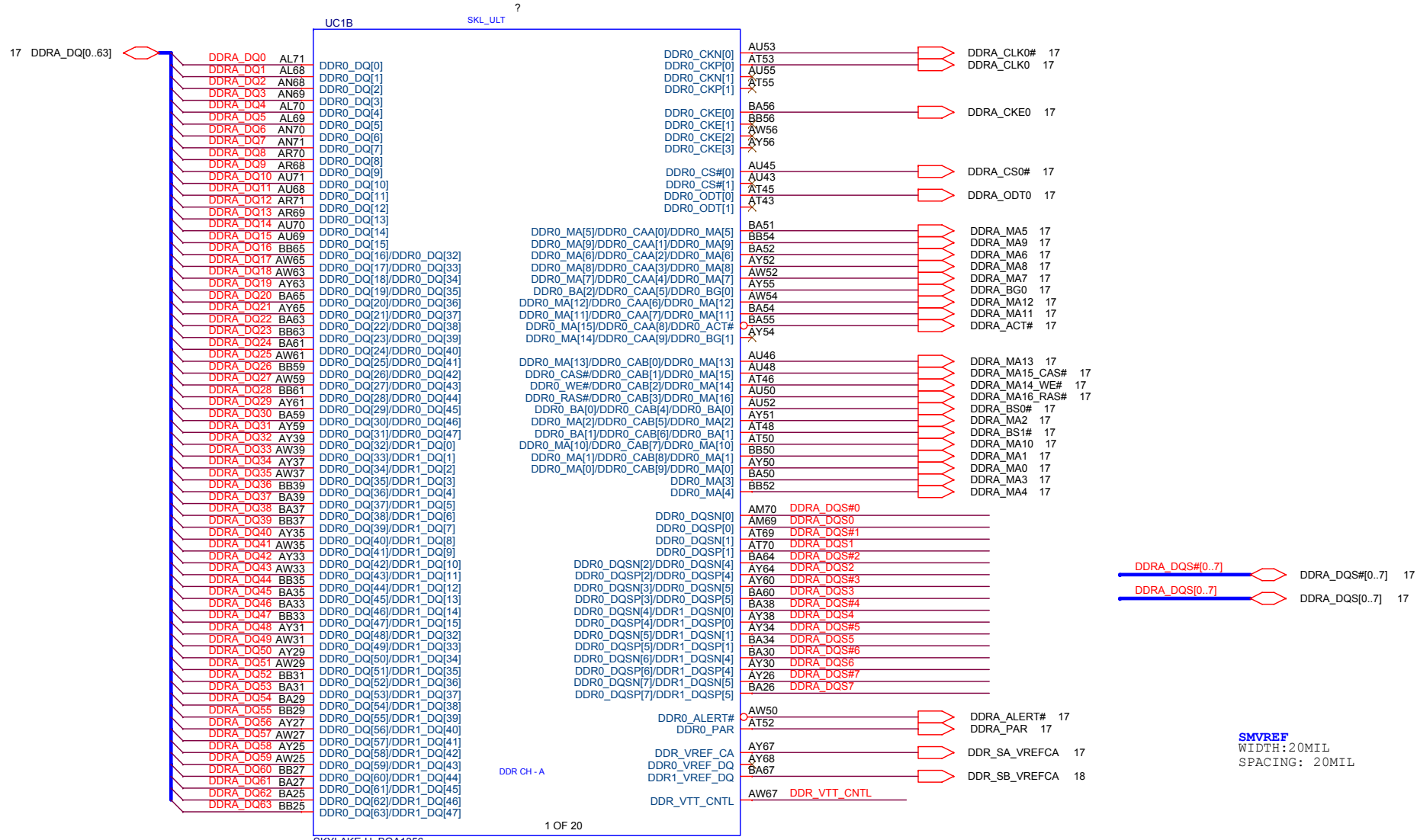
DDP\*\_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC

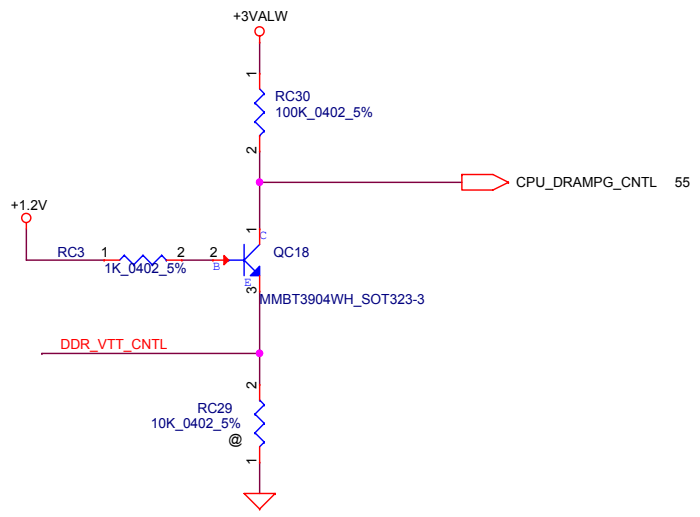


check JTAG circuit?

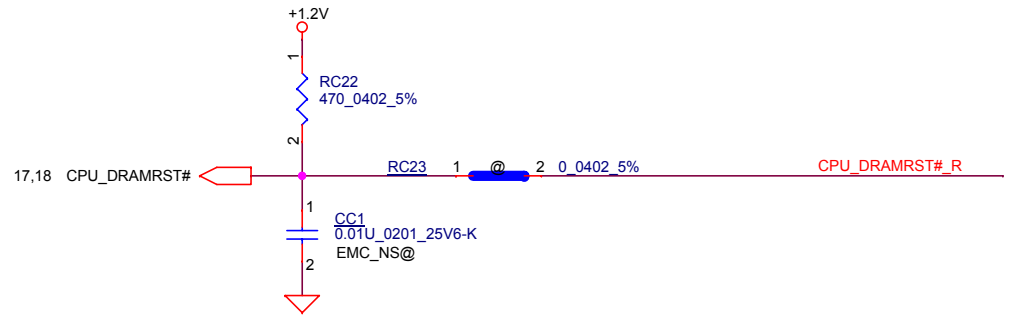
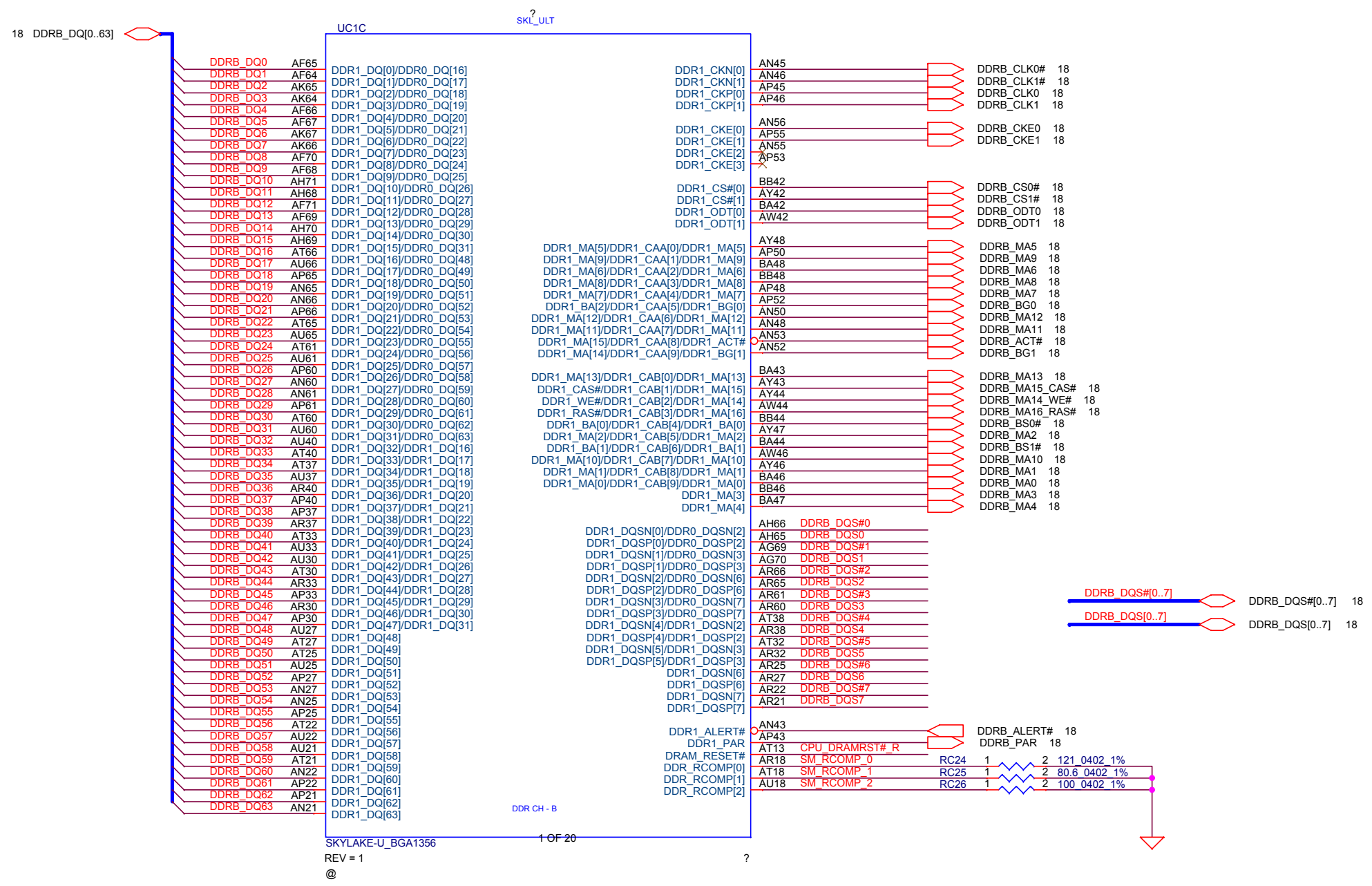
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SMVREF  
WIDTH: 20MIL  
SPACING: 20MIL

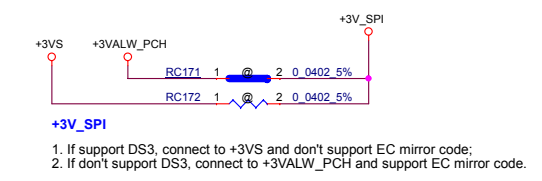
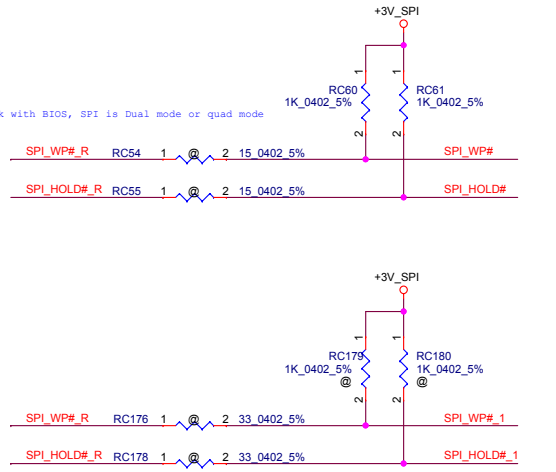
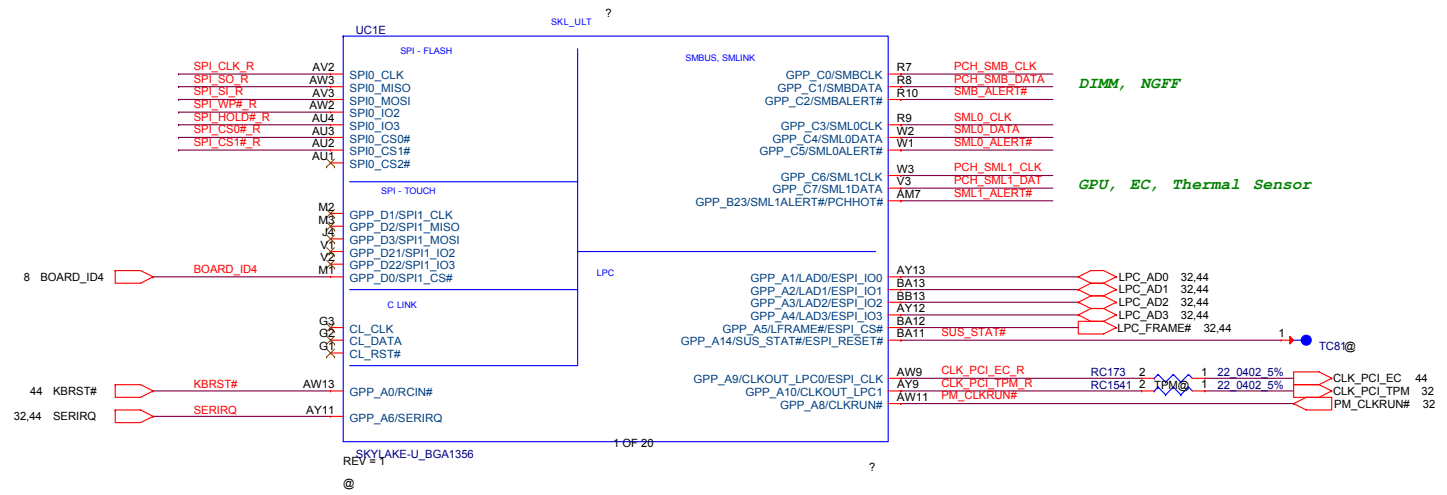
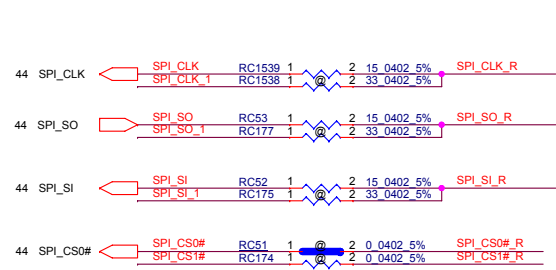


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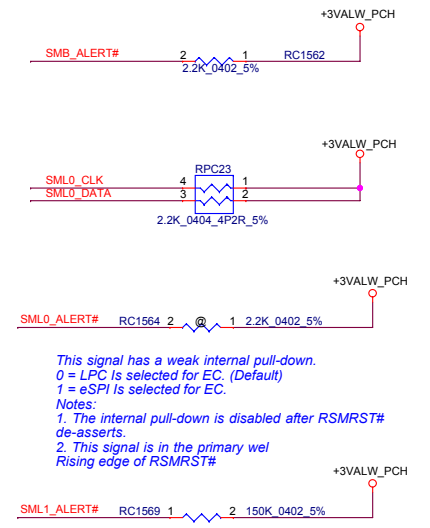
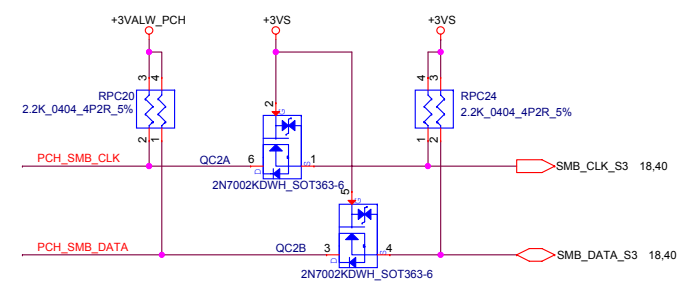
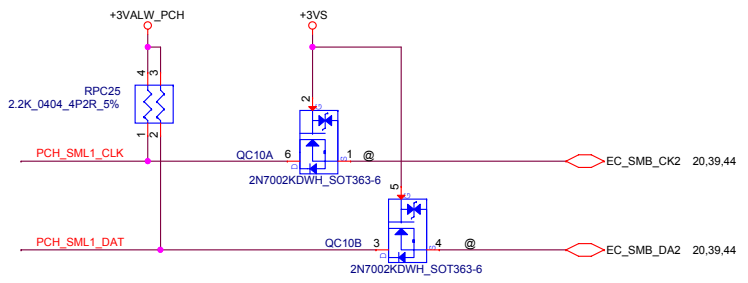
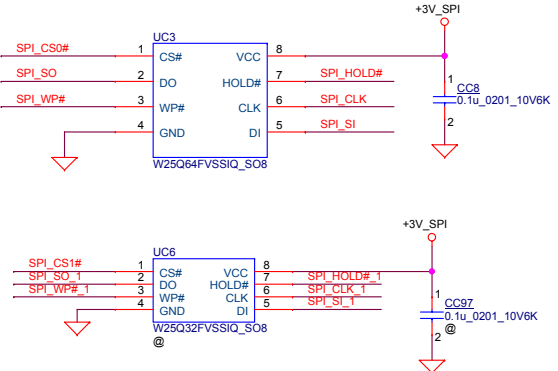
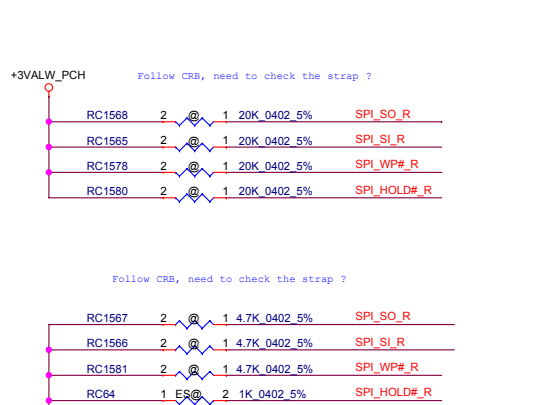
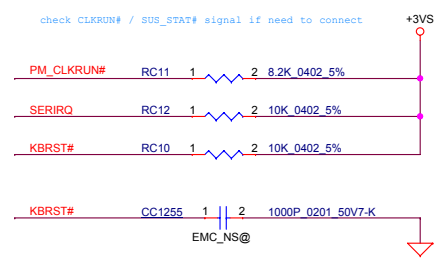


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- +3V\_SPI**
1. If support DS3, connect to +3VS and don't support EC mirror code;
  2. If don't support DS3, connect to +3VALW\_PCH and support EC mirror code.

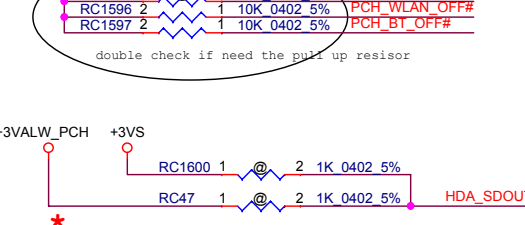
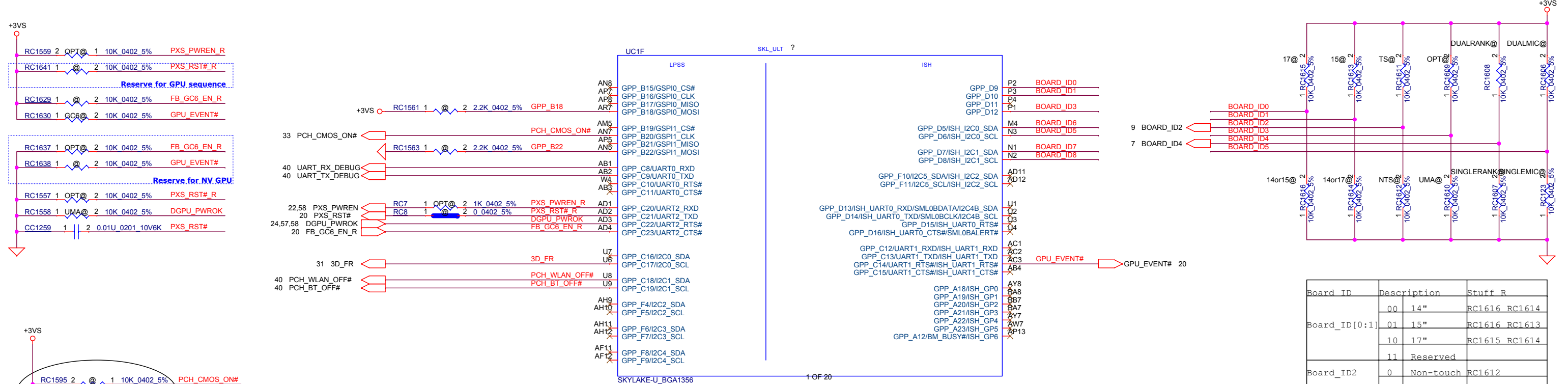


This signal has a weak internal pull-down.  
 0 = LPC is selected for EC. (Default)  
 1 = eSPI is selected for EC.  
 Notes:  
 1. The internal pull-down is disabled after RSMRST# de-asserts.  
 2. This signal is in the primary well  
 Rising edge of RSMRST#

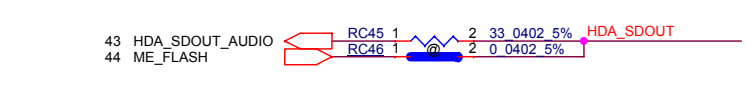
To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST# (Refer to WWS2\_MOW)

Based on WW36 SKL U&Y WOM, RC64 populated, and RC61 de-populated for SKL U ES sample. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

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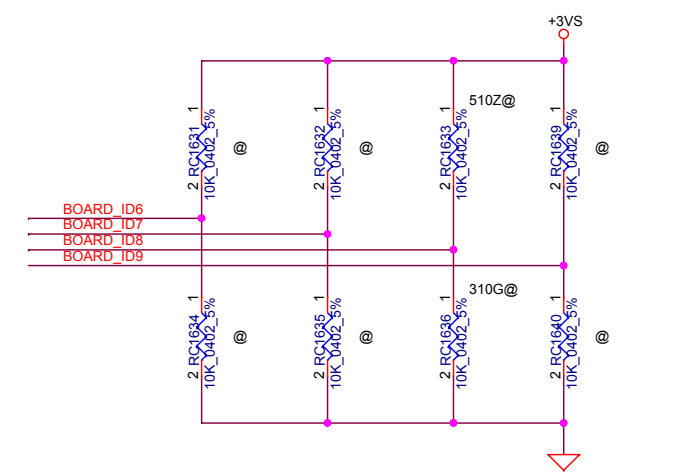


**HDA\_SDO** This signal has a weak internal pull-down.  
 0 = Enable security measures defined in the Flash Descriptor.  
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) * 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPi0 MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) * 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPi1 MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) * 1 = LPC	0	Rising edge of PCH_PWROK

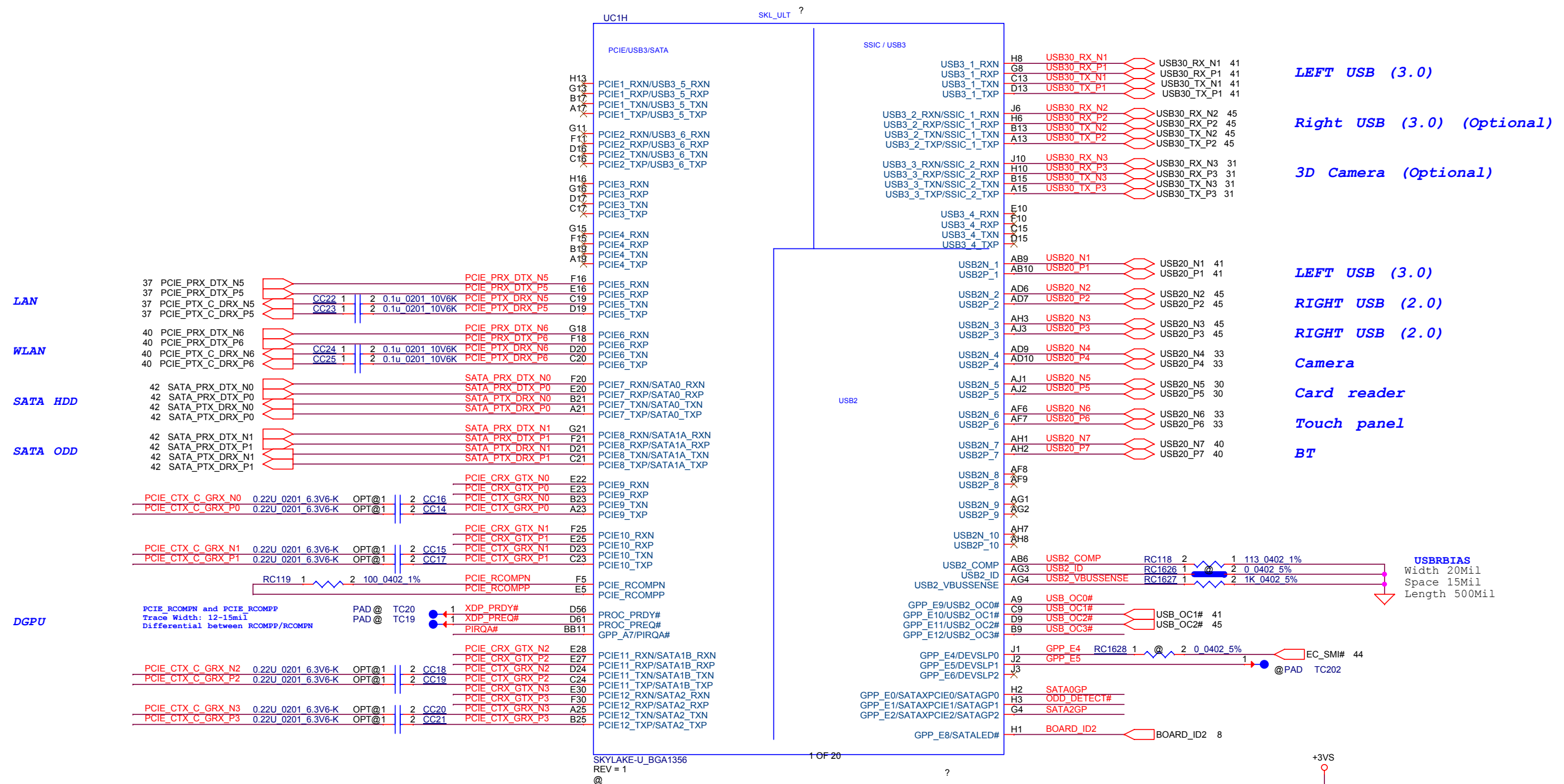
Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11 Reserved	
Board_ID2	0 Non-touch	RC1612
	1 Touch	RC1611
Board_ID3	0 UMA	RC1610
	1 DTS	RC1609
Board_ID4	0 SingleRank	RC1607
	1 DualRank	RC1608
Board_ID5	0 SingleMIC	RC123
	1 DualMIC	RC1606



Board ID	Description	Stuff R
Board_ID[6:7]	00 Samsung 8Gb	RC1634 RC1635
	01 Hynix 8Gb	RC1634 RC1632
	10 Micron 8Gb	RC1631 RC1635
	11 Reserved	RC1631 RC1632
Board_ID8	0 310G	RC1636
	1 510Z	RC1633
BOARD_ID9	0 Reserved	
	1 Reserved	

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LEFT USB (3.0)

Right USB (3.0) (Optional)

3D Camera (Optional)

LEFT USB (3.0)

RIGHT USB (2.0)

RIGHT USB (2.0)

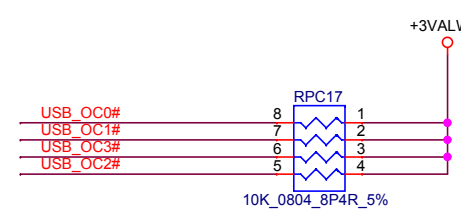
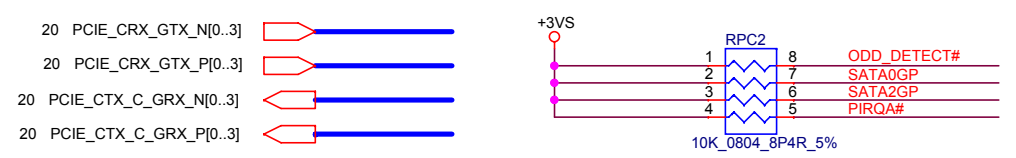
Camera

Card reader

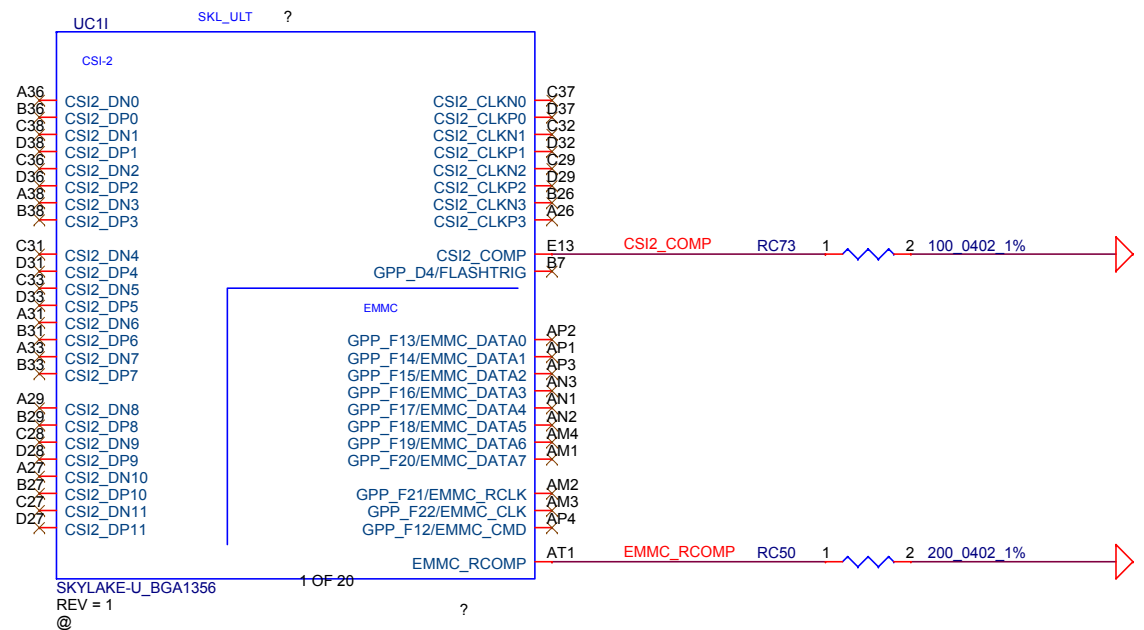
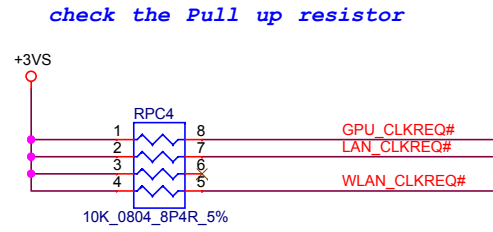
Touch panel

BT

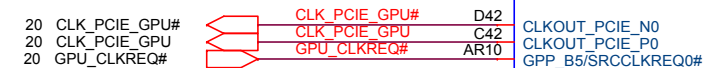
USBRBIAS  
Width 20Mil  
Space 15Mil  
Length 500Mil



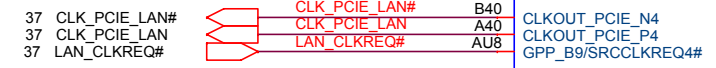
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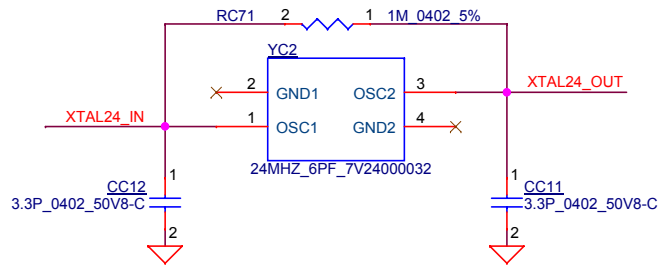
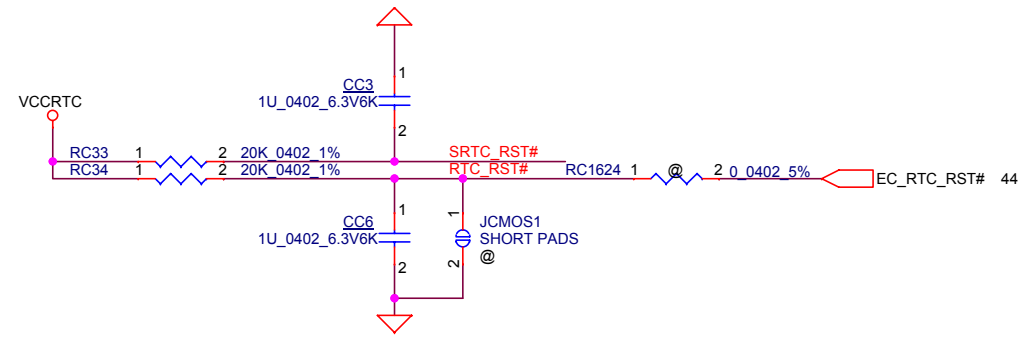
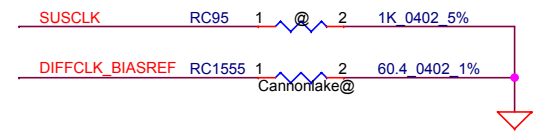
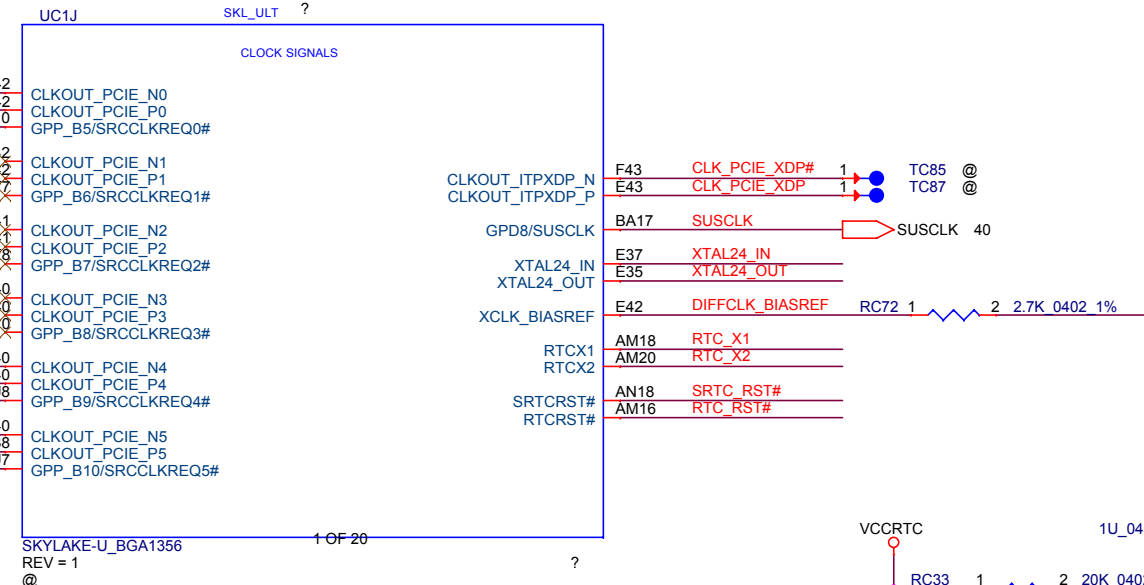
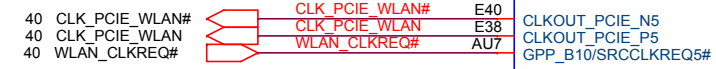
PCIE CLK0 DGPU



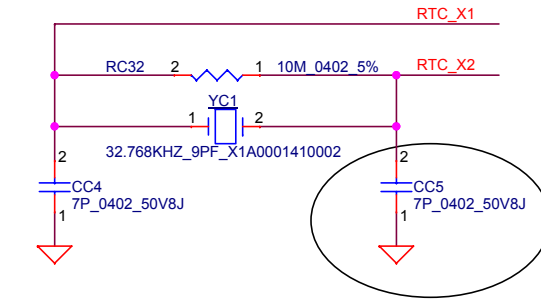
PCIE CLK4 LAN



PCIE CLK5 WLAN

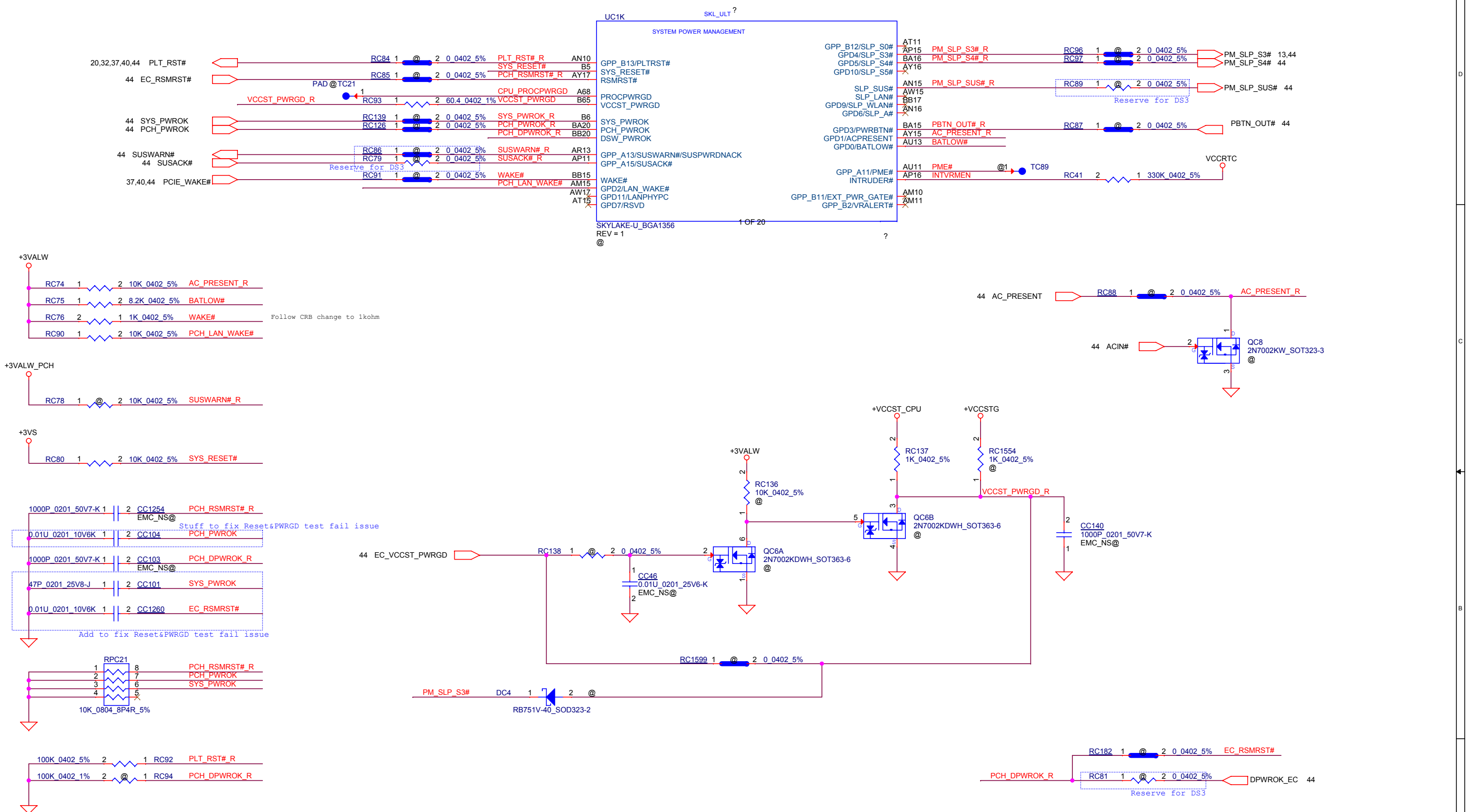


need to use 38.4MHz (30ohm) for Cannonlake-u

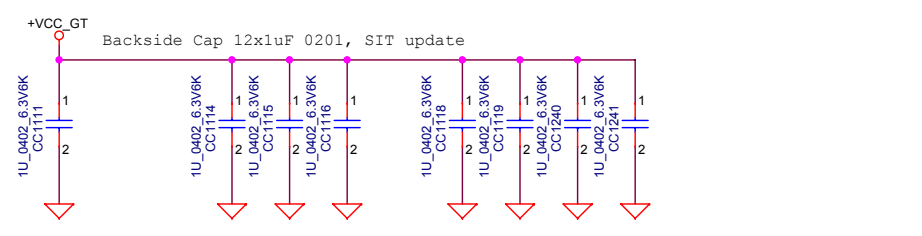
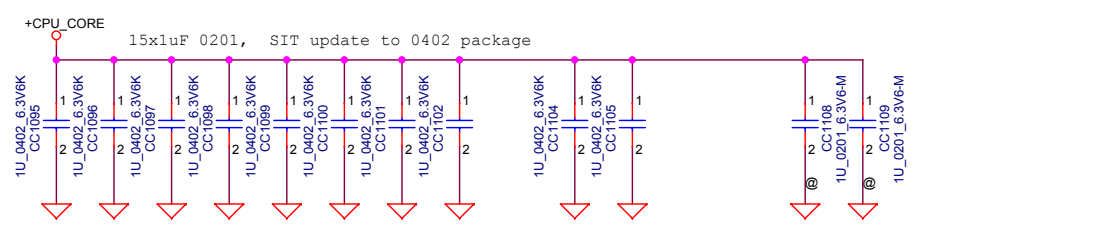
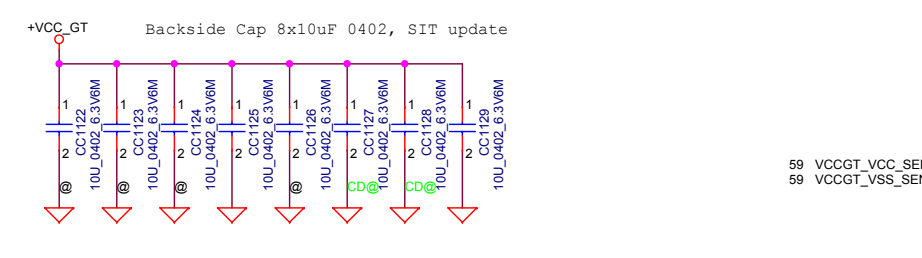
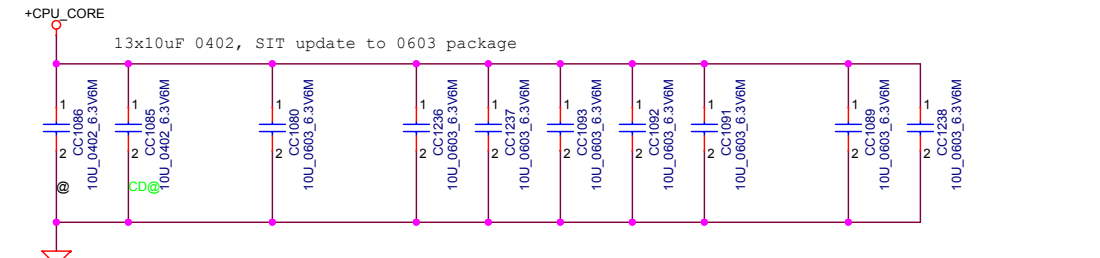
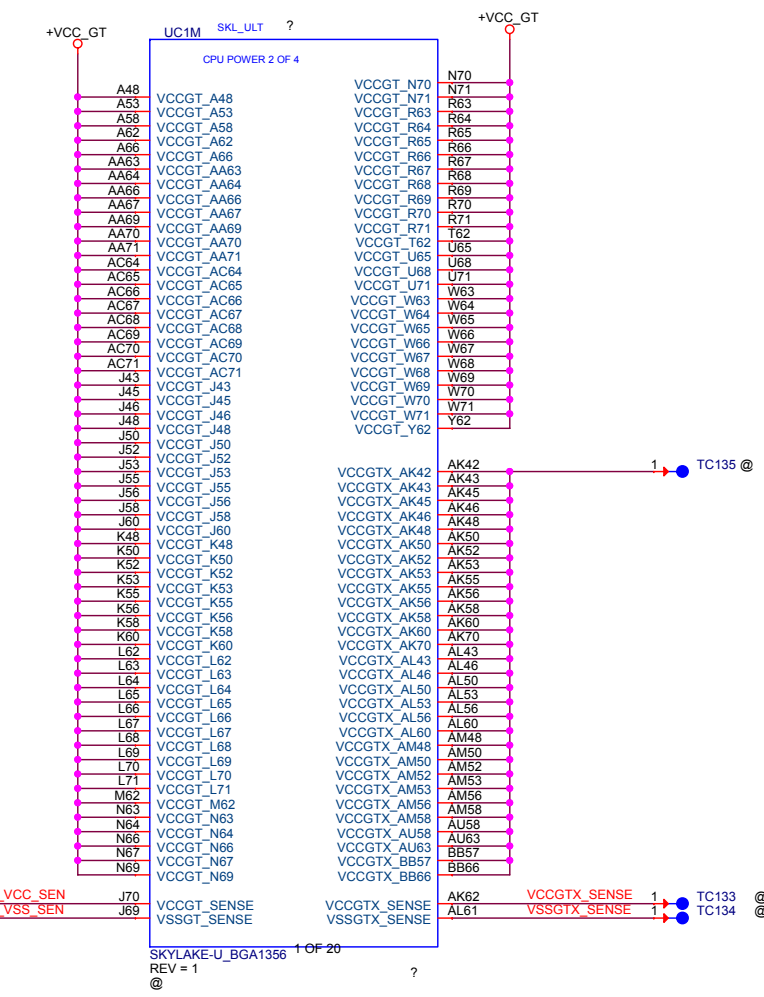
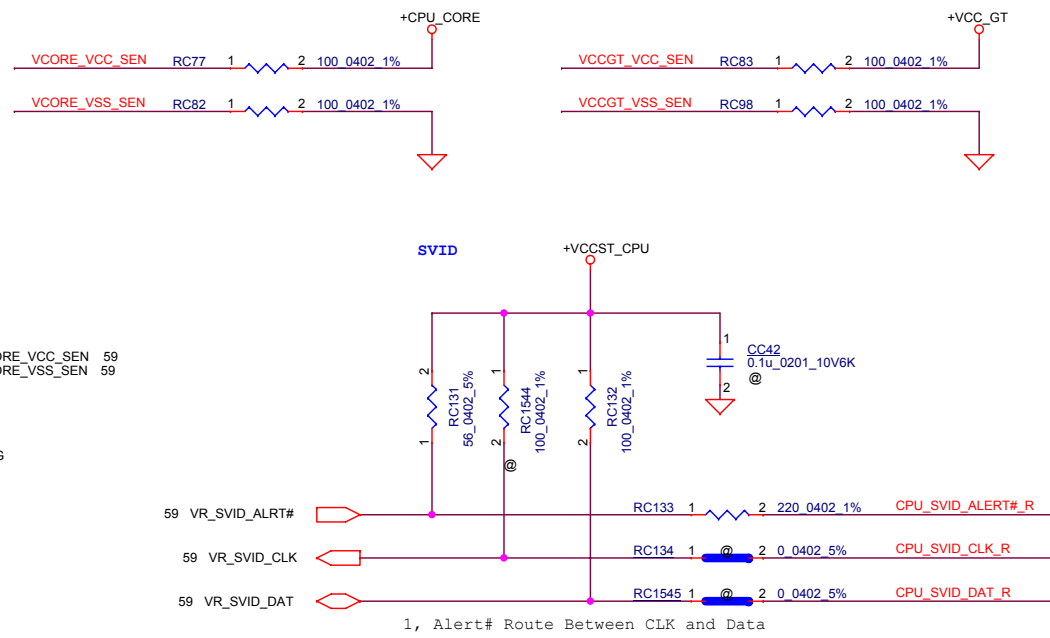
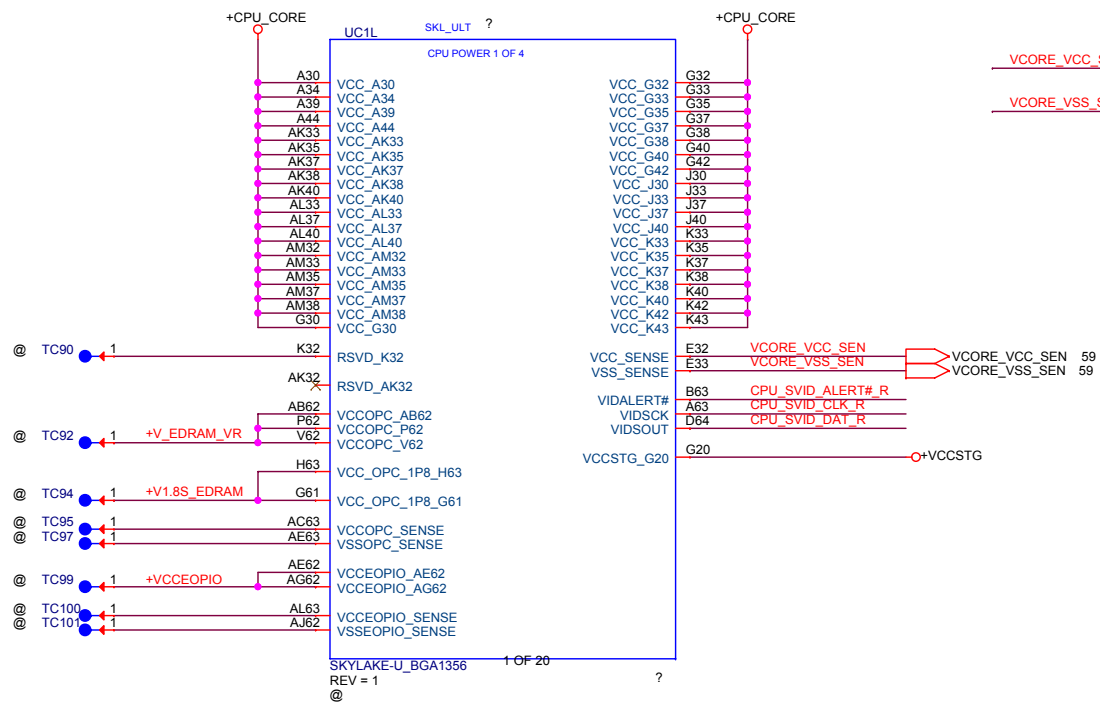


when single end external clock generator used, this pin should be grounded

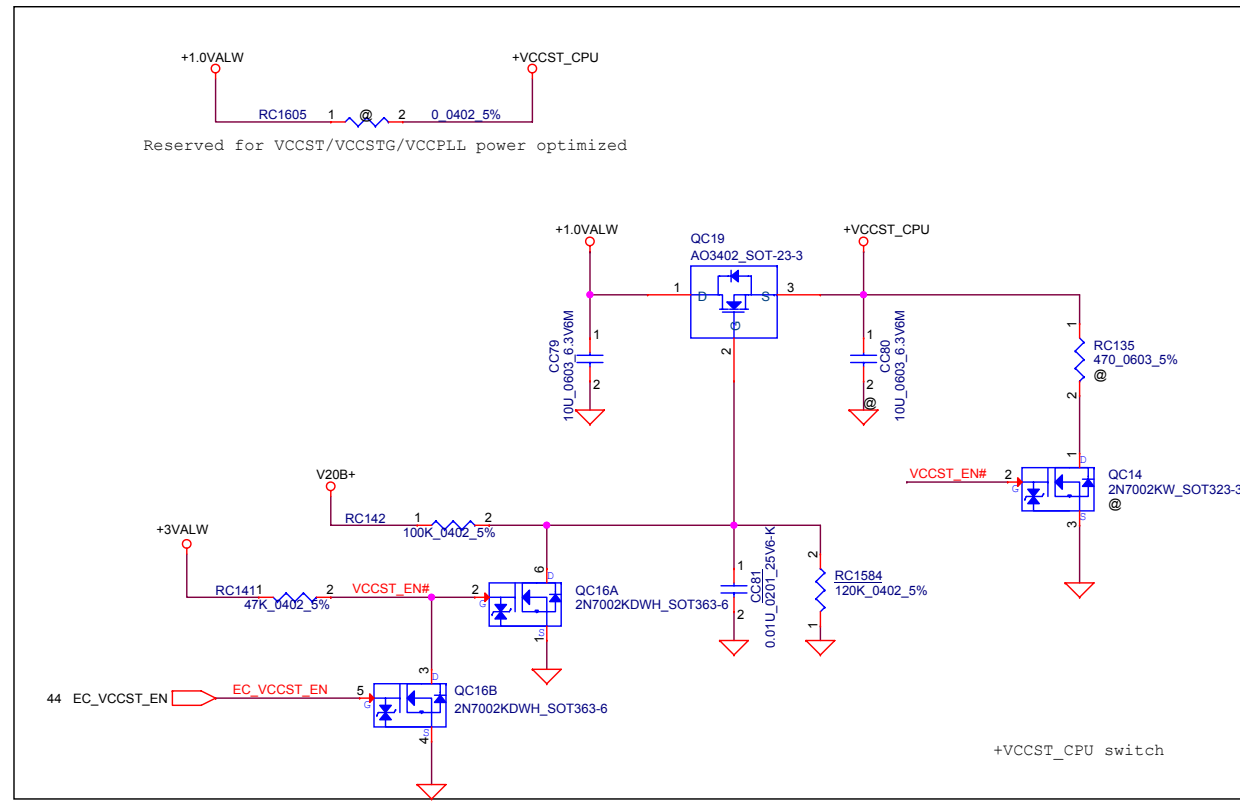
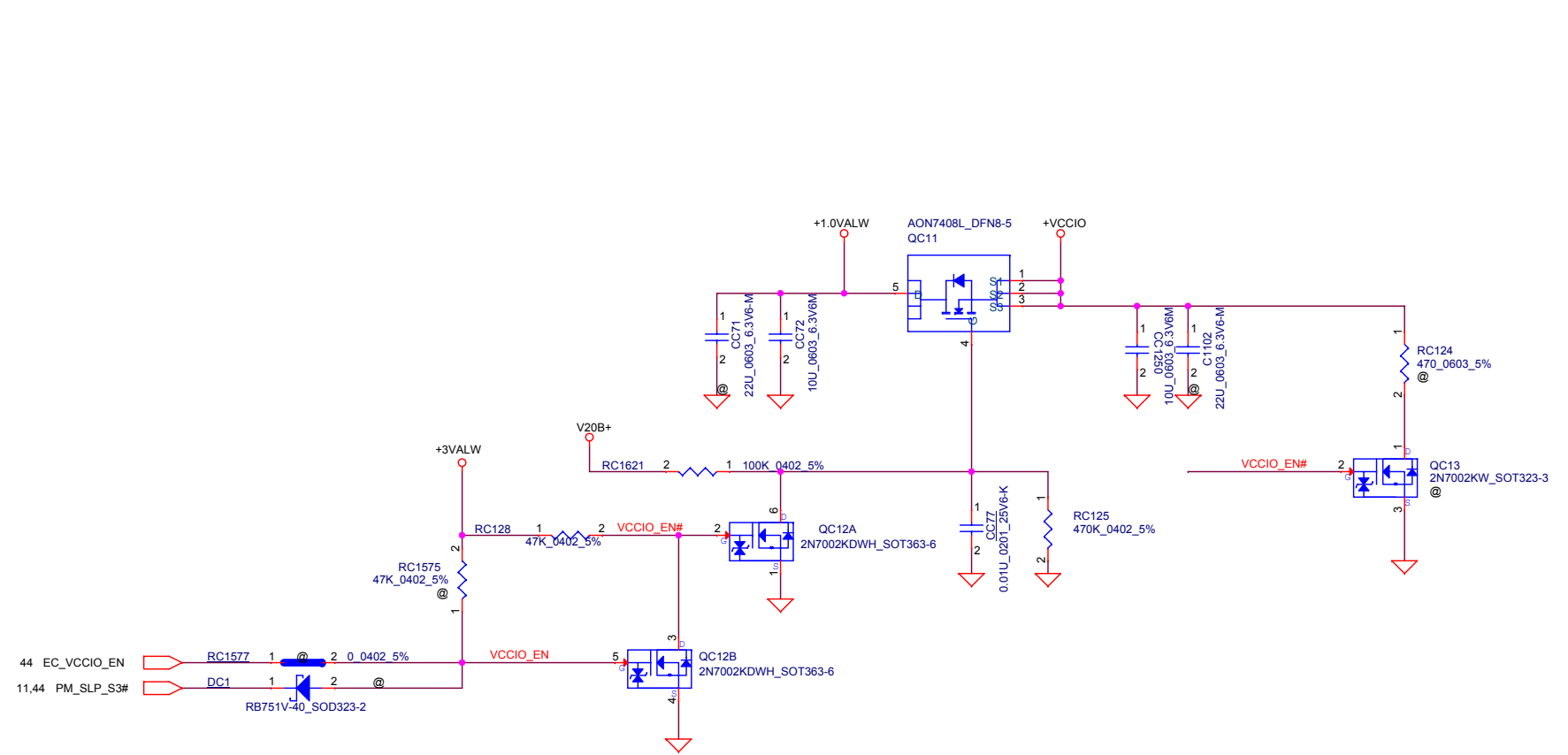
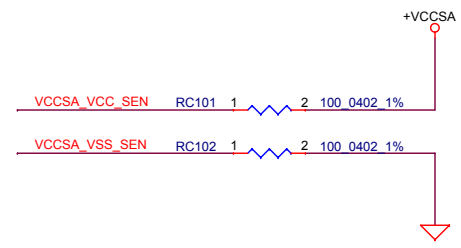
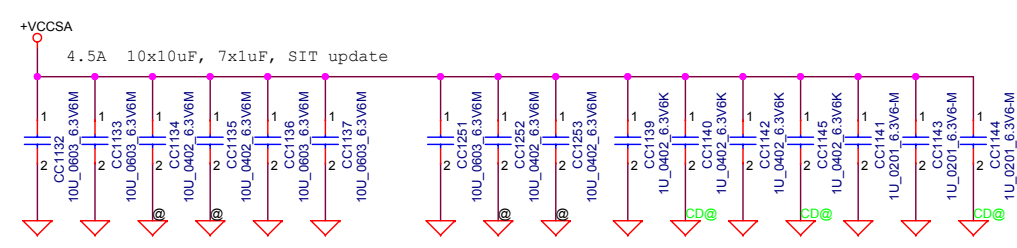
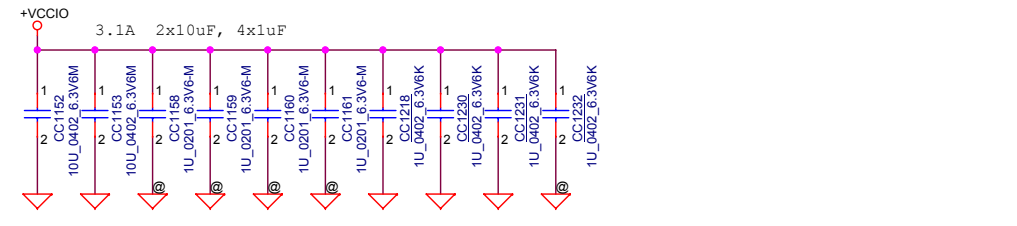
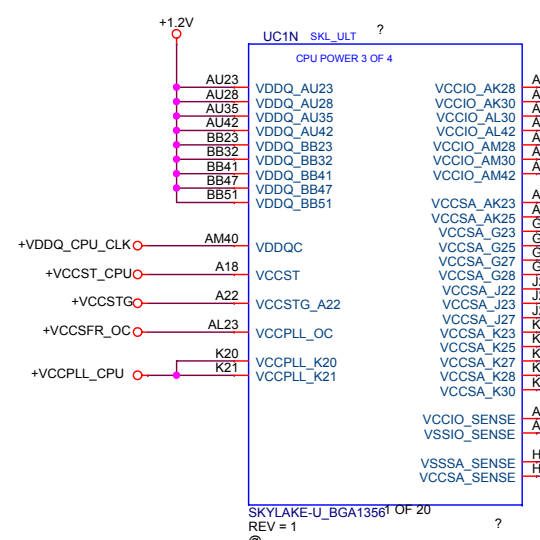
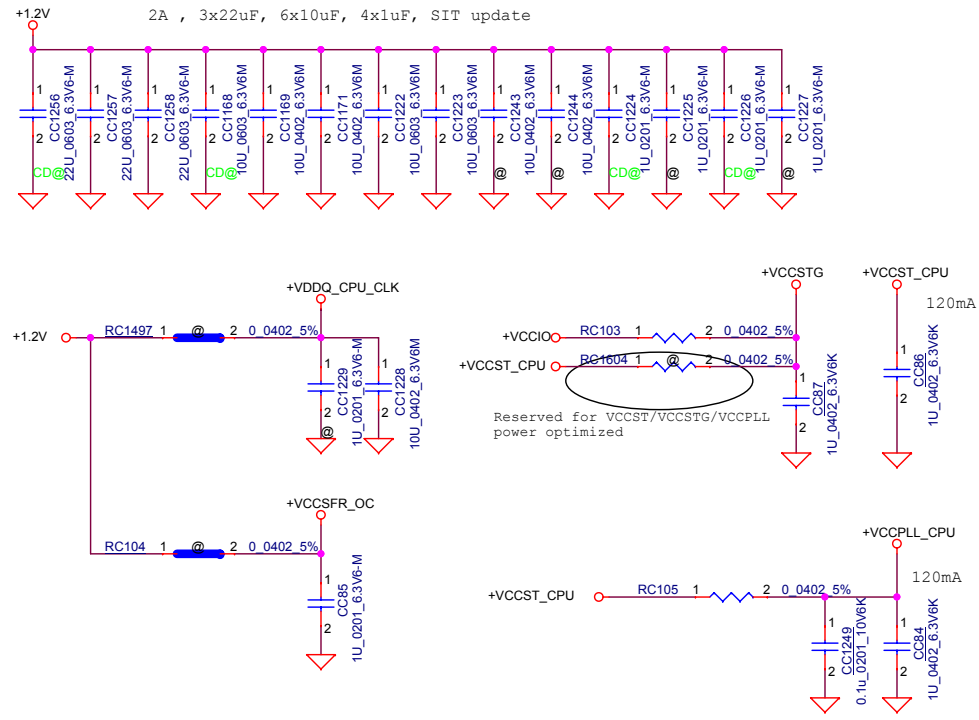
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	
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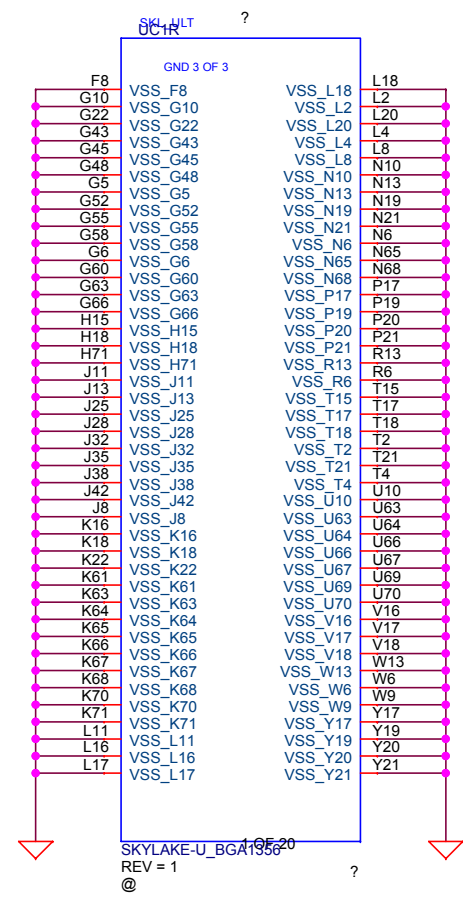
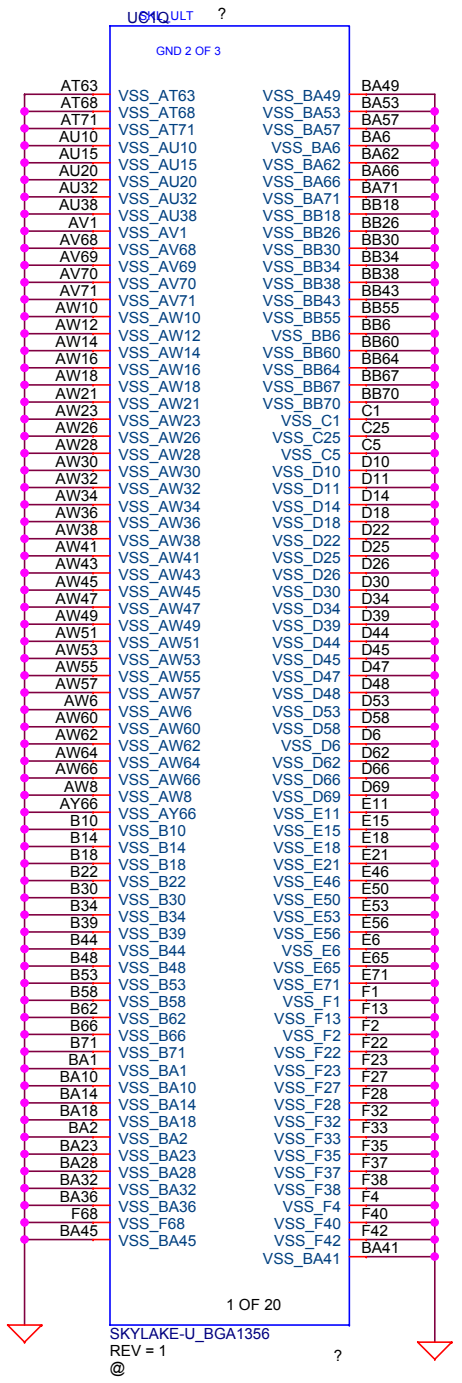
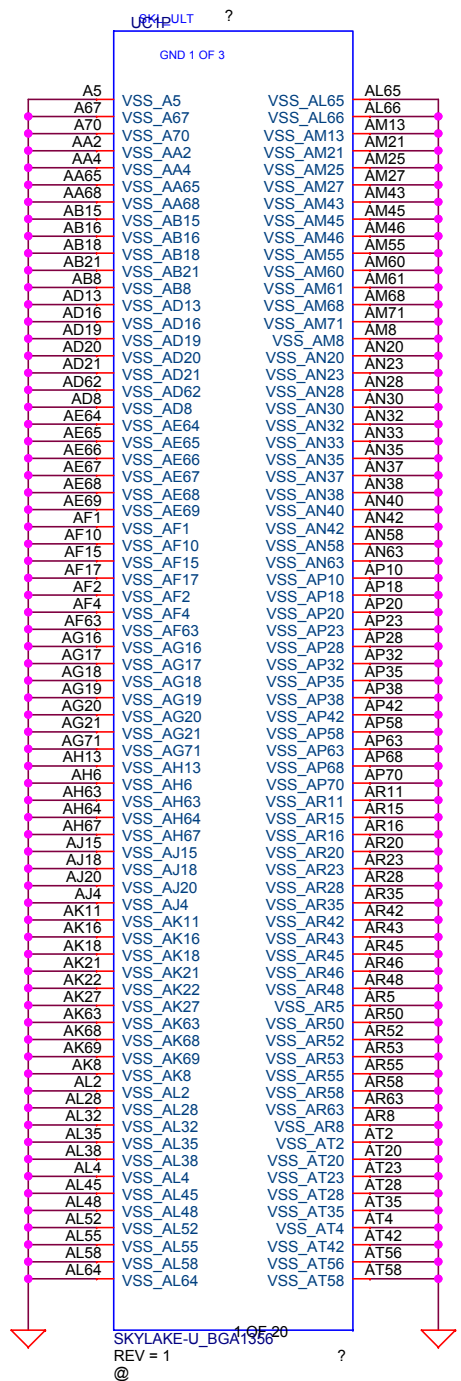
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	MCP (CPU PWR1)	
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Date:	Thursday, January 14, 2016	Sheet	12	of	60




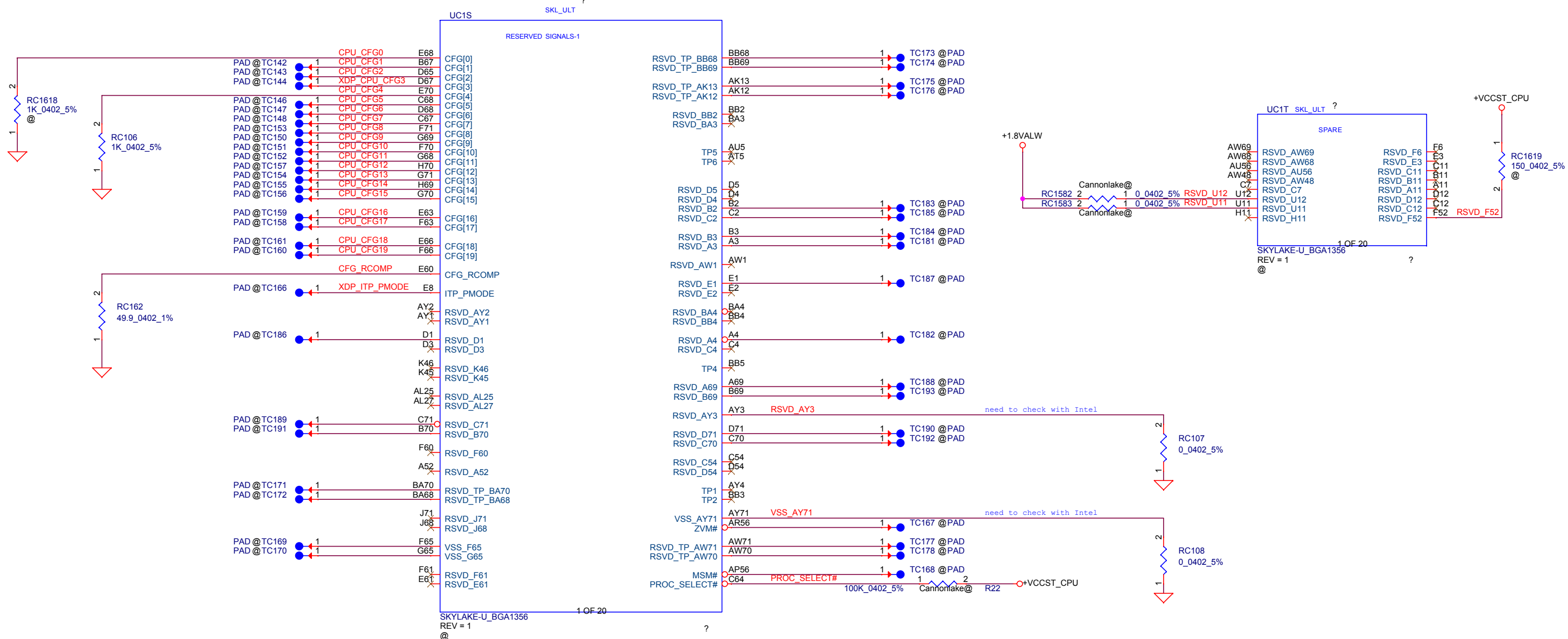
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	
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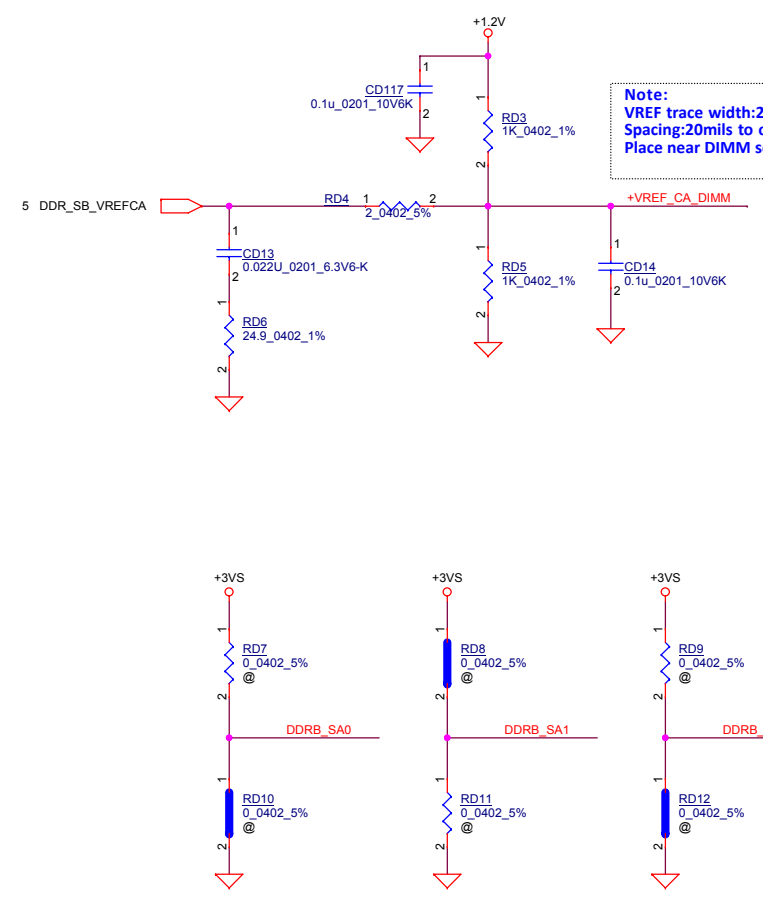
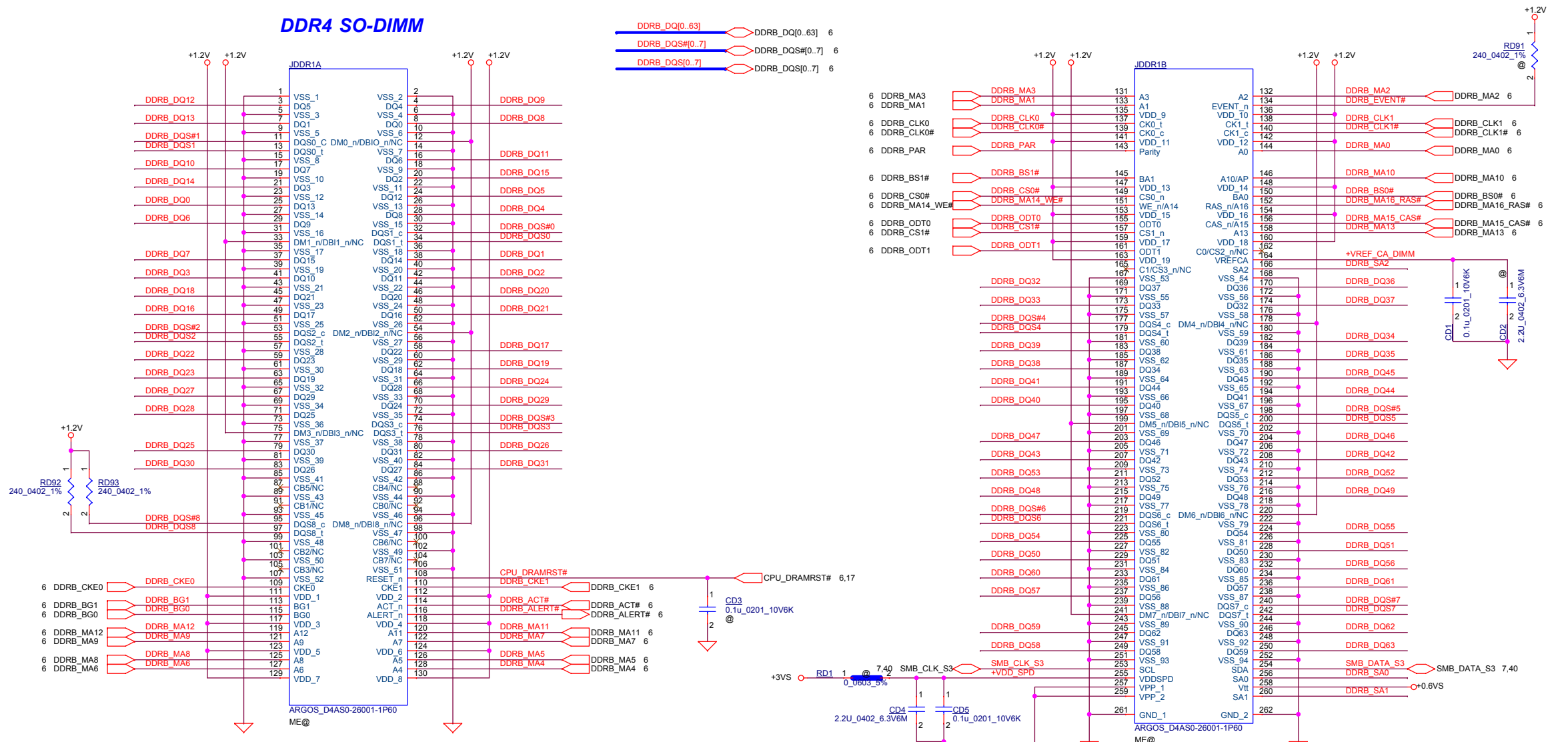
Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	- 1 = eDP Disabled - 0 = eDP Enabled*	1

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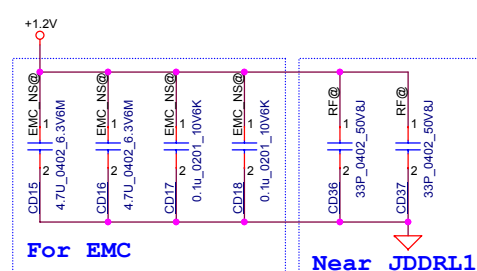
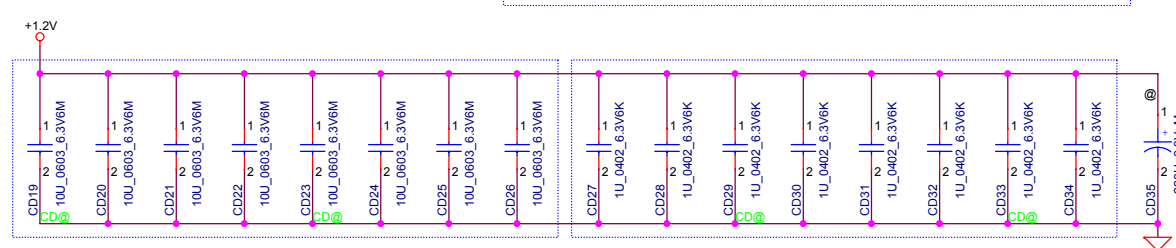
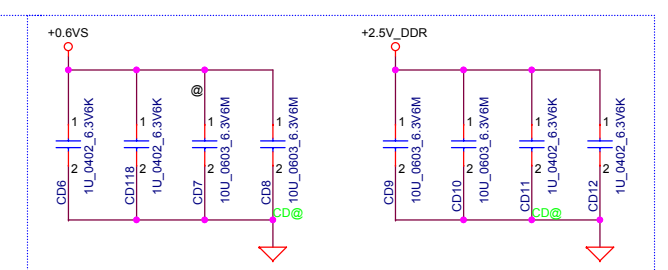
Title		
MCP (CFG,RESERVED)		
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# DDR4 SO-DIMM



**Layout Note:**  
Place near DIMM



SPD Address = 2H

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## N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

## Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

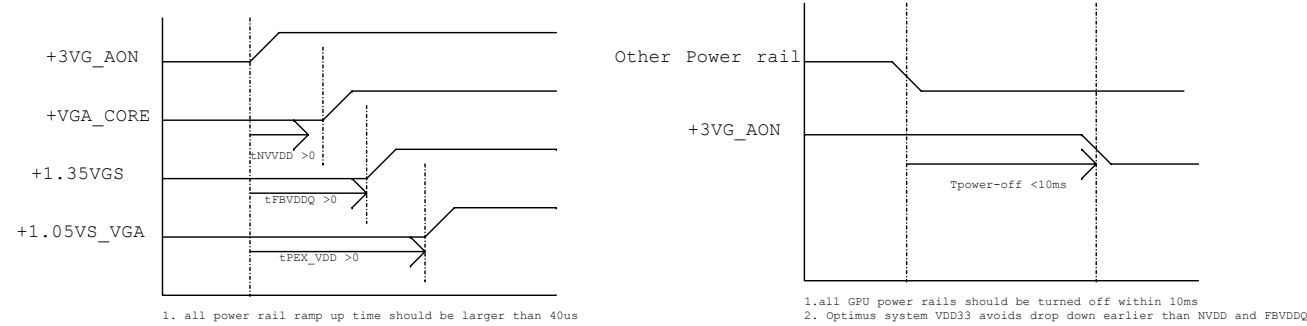
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)	FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.05V)		Other (3.3V)		
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

## N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

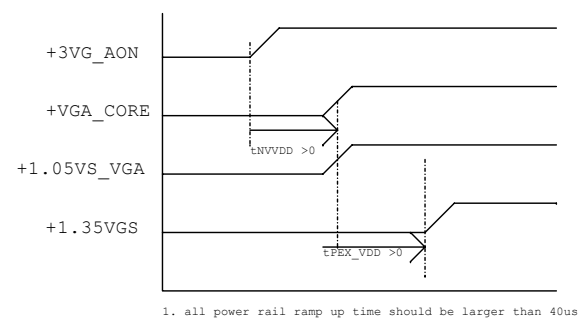
## N15V-GM Power Sequence



## N15x Binary Straps

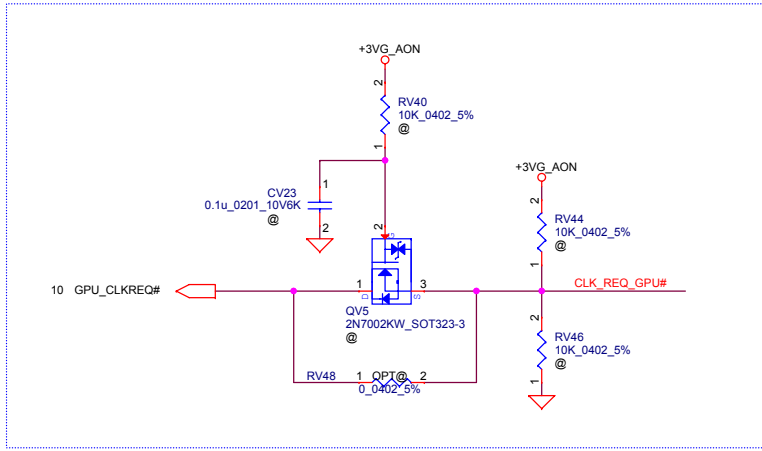
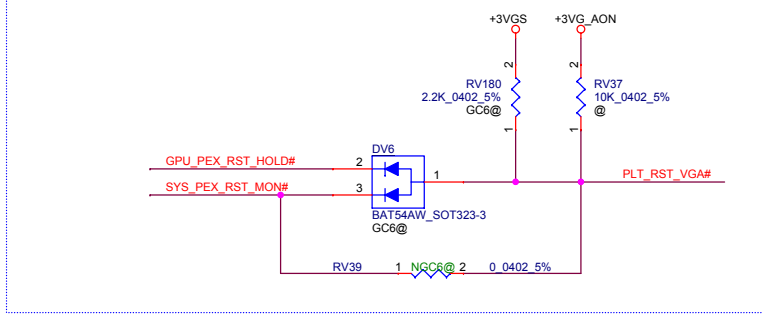
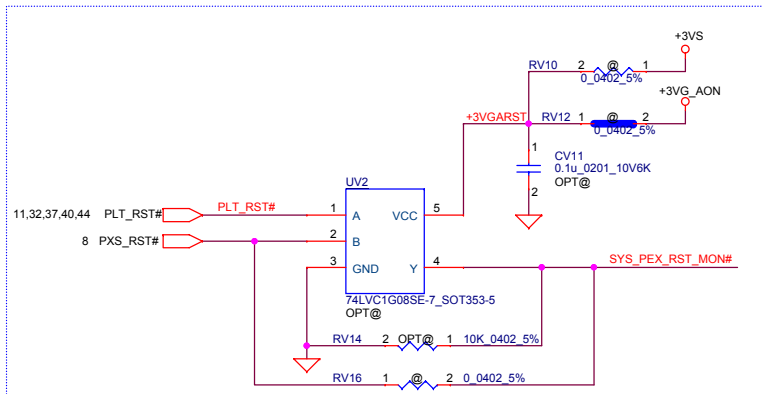
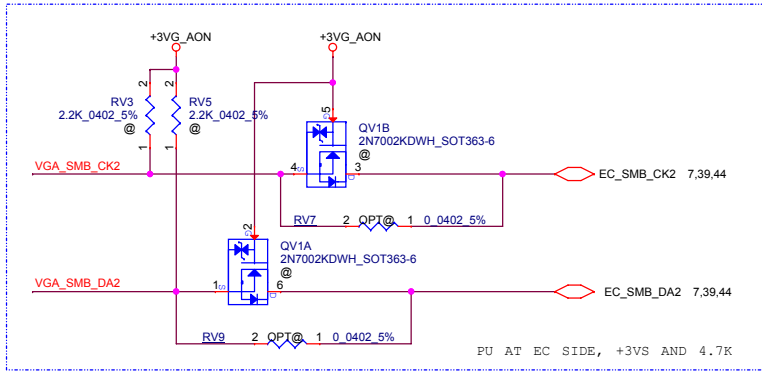
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

## N15S-GT Power Sequence

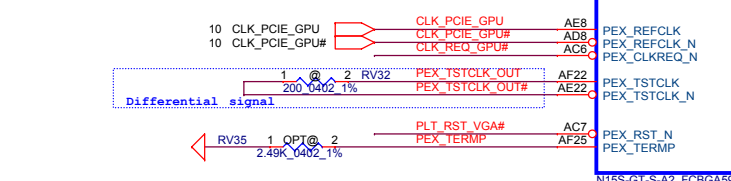


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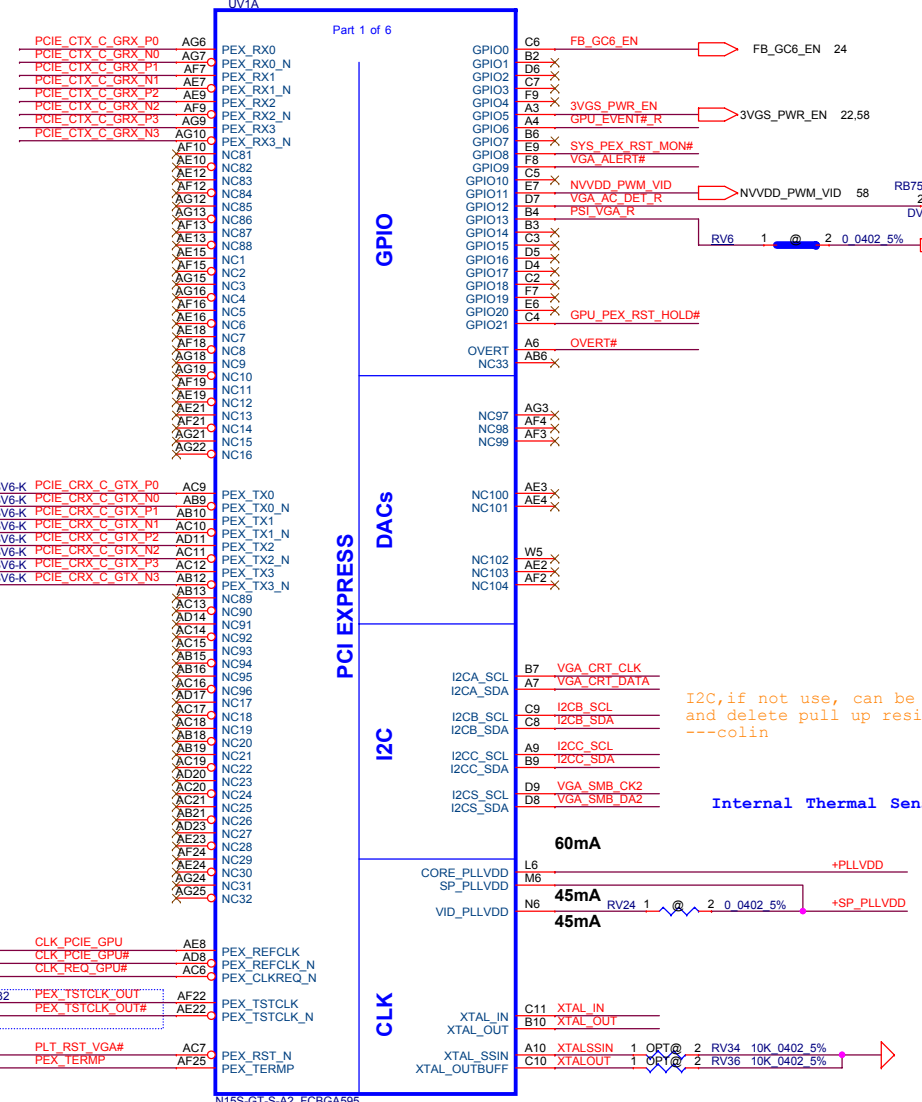
- 9 PCIE\_CRX\_GTX\_N[0..3]
- 9 PCIE\_CRX\_GTX\_P[0..3]
- 9 PCIE\_CTX\_C\_GRX\_N[0..3]
- 9 PCIE\_CTX\_C\_GRX\_P[0..3]



PCIE_CRX_GTX_P0	OPT@	CV10	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_P0	AC9	PEX_TX0
PCIE_CRX_GTX_N0	OPT@	CV13	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_N0	AB9	PEX_TX0_N
PCIE_CRX_GTX_P1	OPT@	CV8	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_P1	AB10	PEX_TX1
PCIE_CRX_GTX_N1	OPT@	CV9	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_N1	AB10	PEX_TX1_N
PCIE_CRX_GTX_P2	OPT@	CV6	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_P2	AD11	PEX_TX2
PCIE_CRX_GTX_N2	OPT@	CV7	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_N2	AC11	PEX_TX2_N
PCIE_CRX_GTX_P3	OPT@	CV4	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_P3	AC12	PEX_TX3
PCIE_CRX_GTX_N3	OPT@	CV5	1	2	0.22U	0.201	6.3V6-K	PCIE_CRX_C_GTX_N3	AB12	PEX_TX3_N

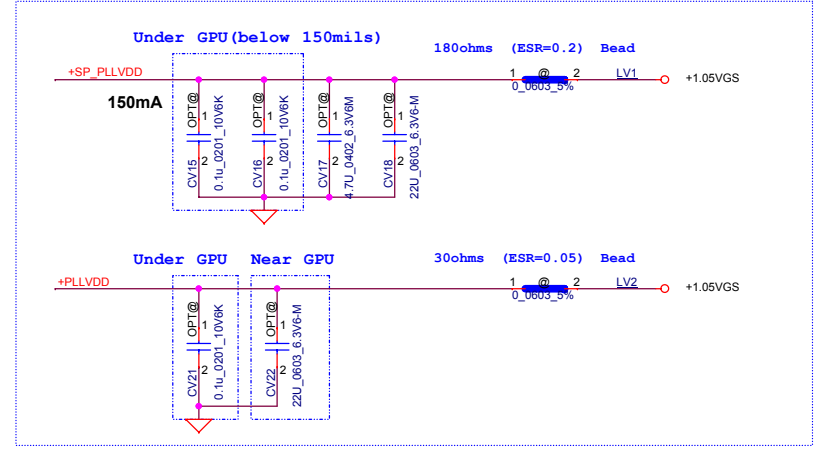
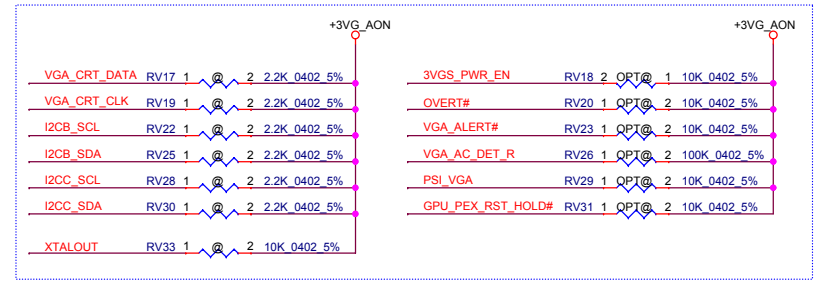
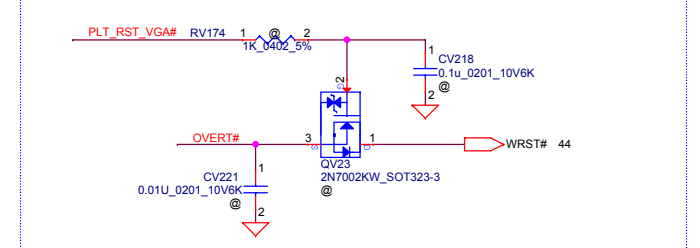
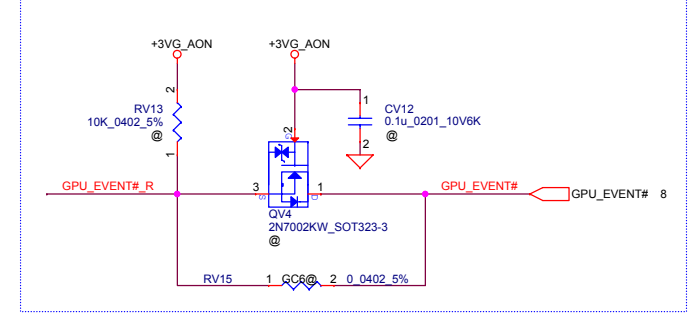
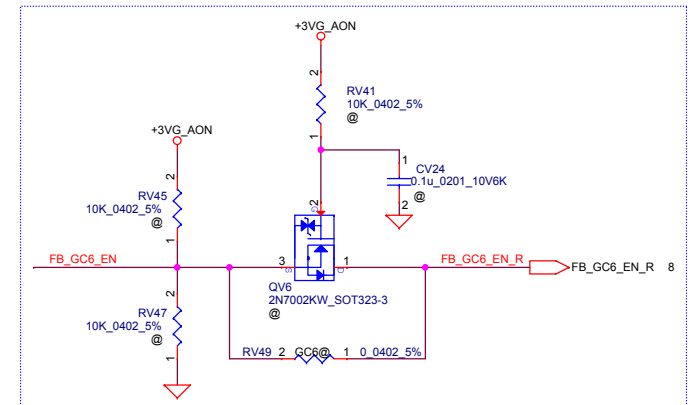
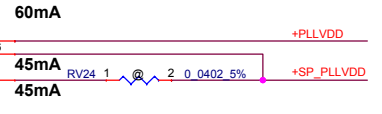


N15S-G1-S-A2-FCBGA595

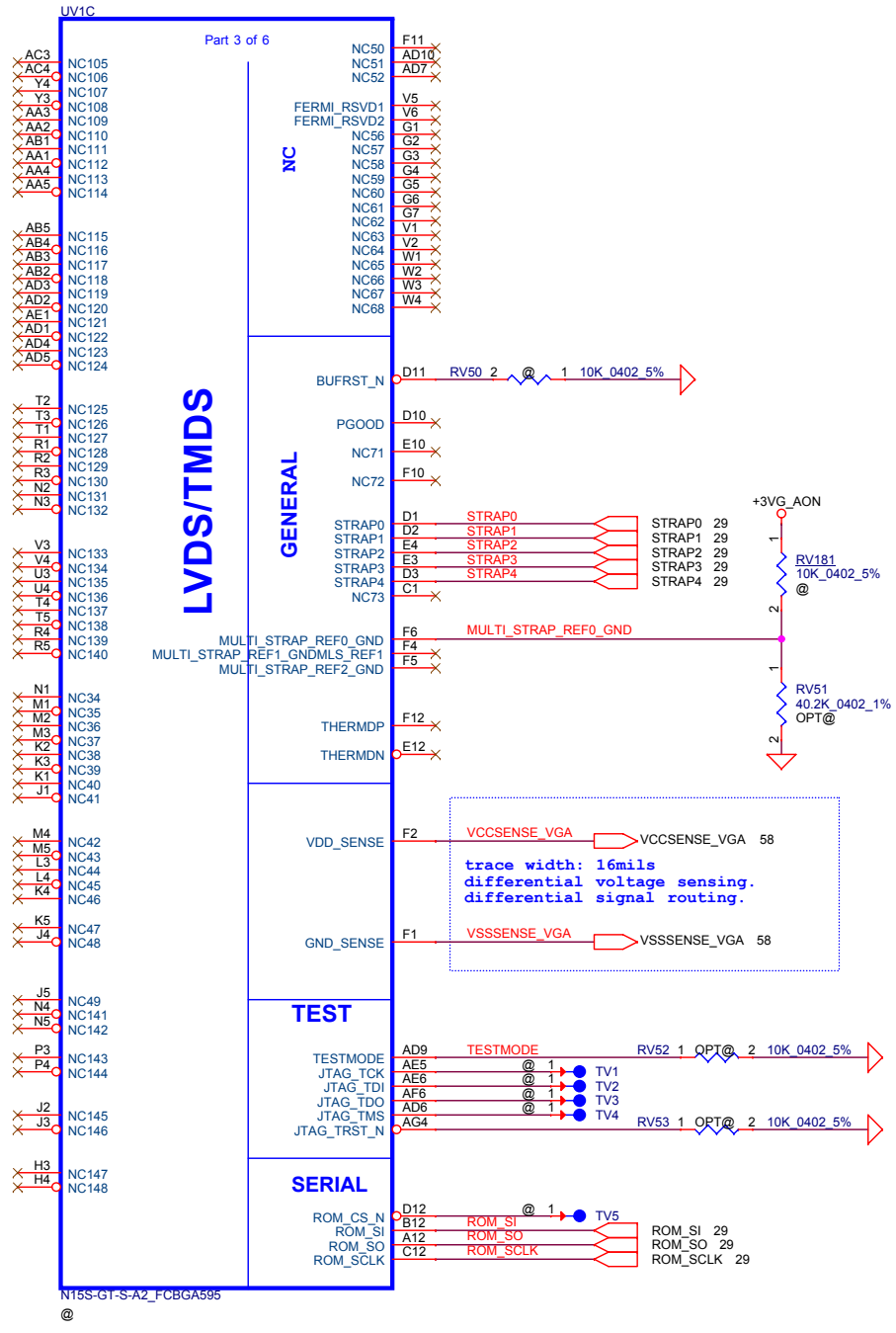


I2C, if not use, can be soft grounded and delete pull up resistor  
---colin

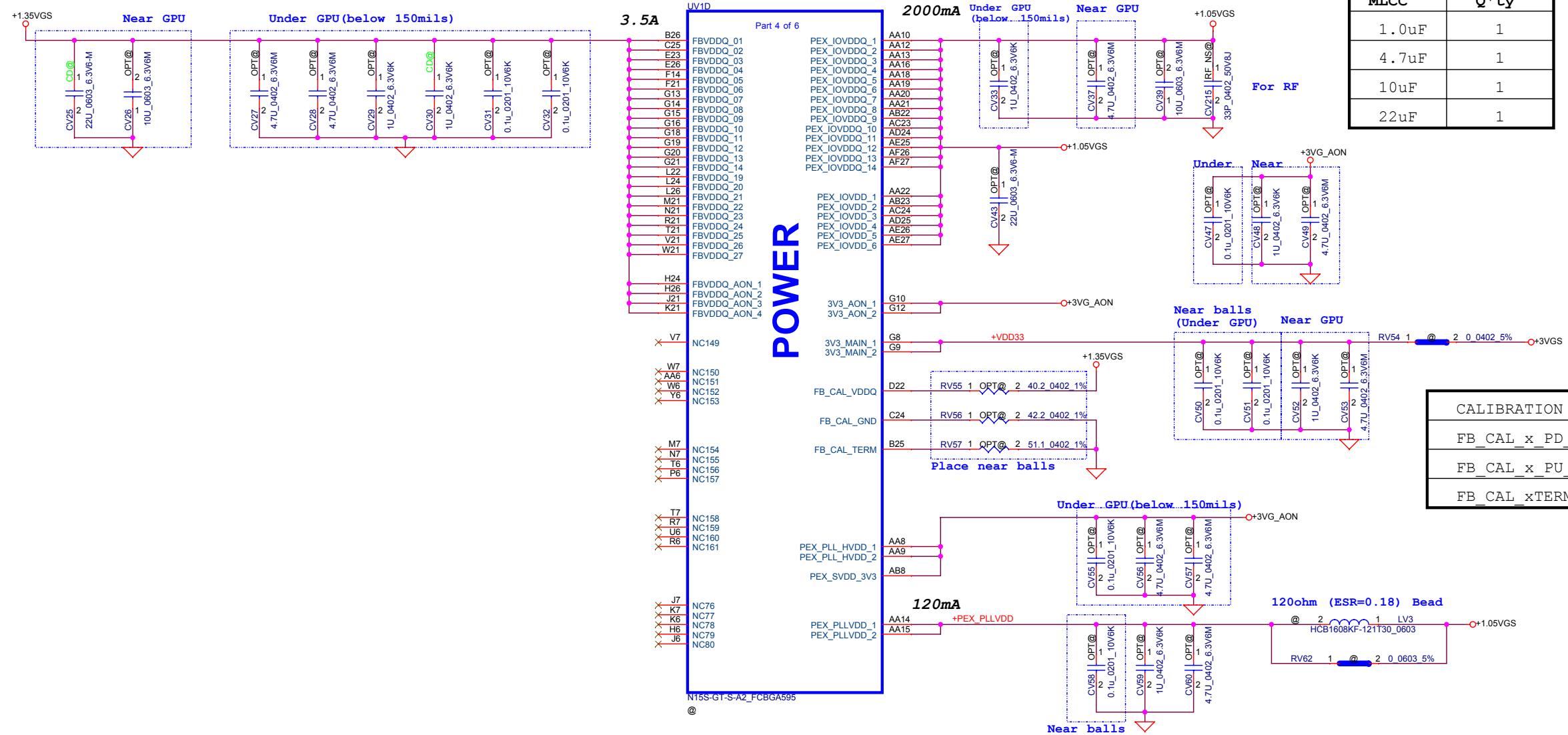
Internal Thermal Sensor



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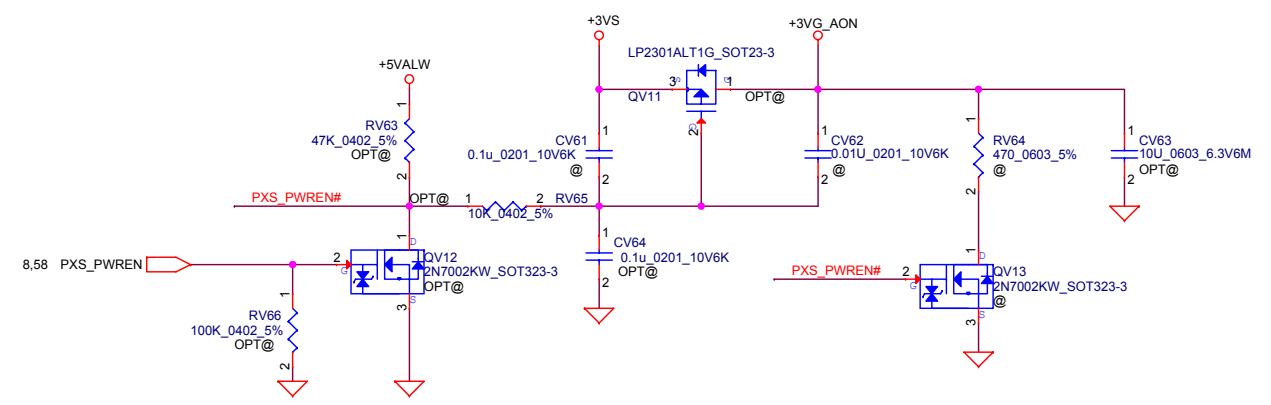


PEX\_IOVDD/Q Decoupling

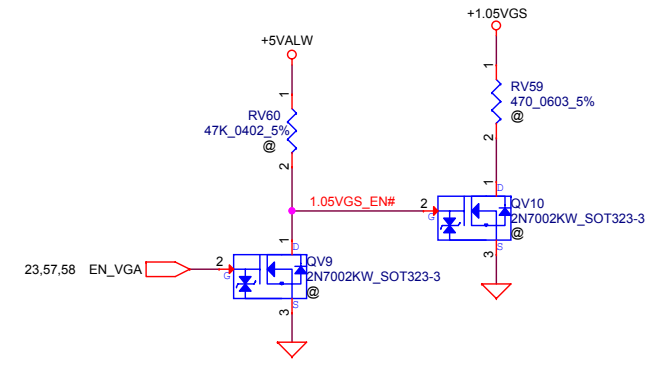
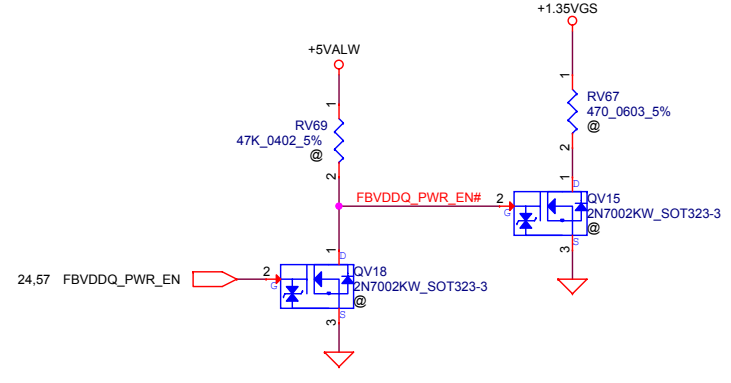
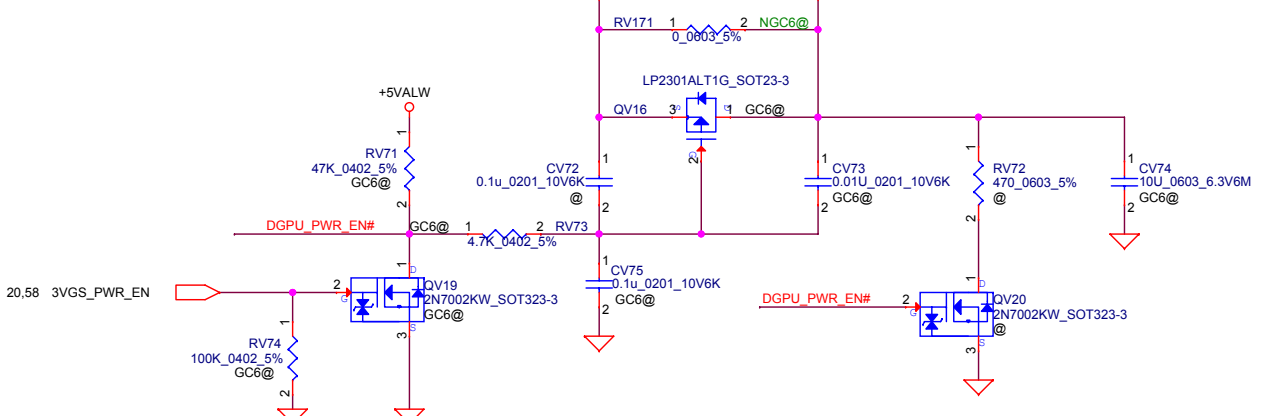
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4.7uF	1
10uF	1
22uF	1

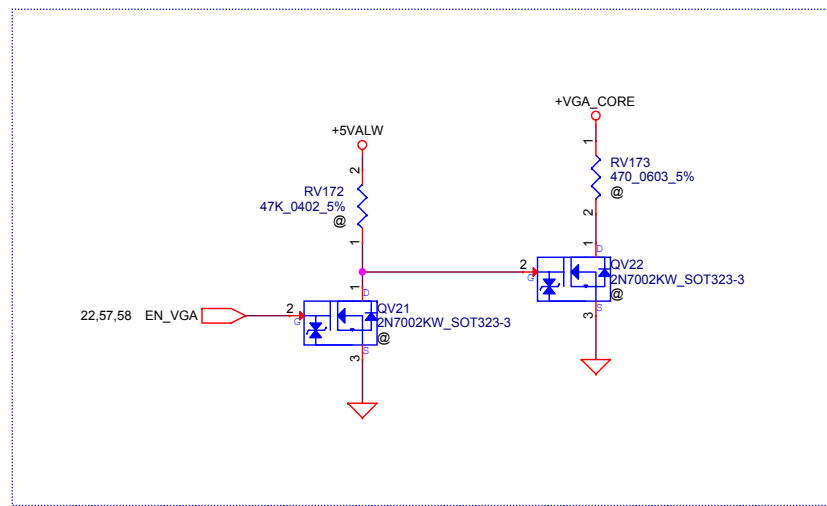
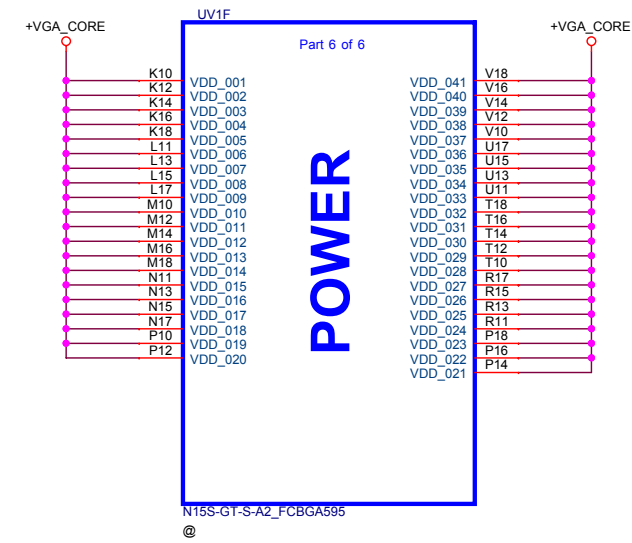
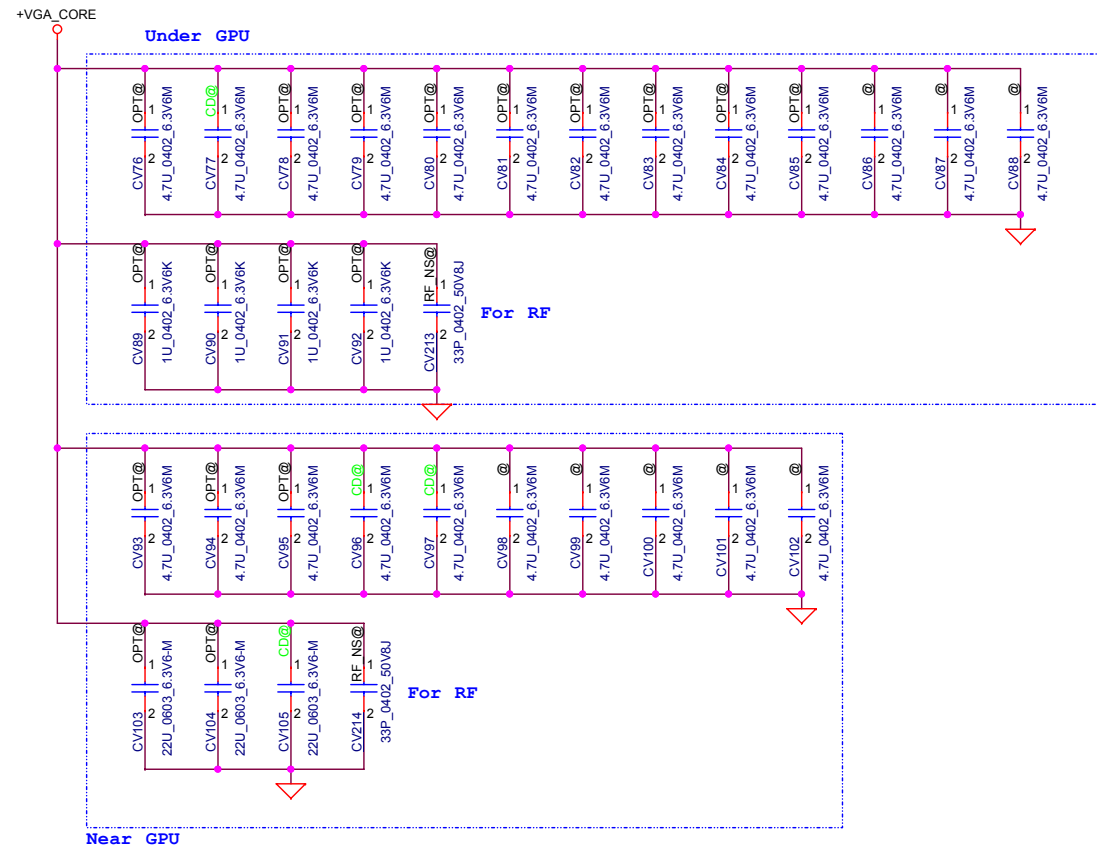
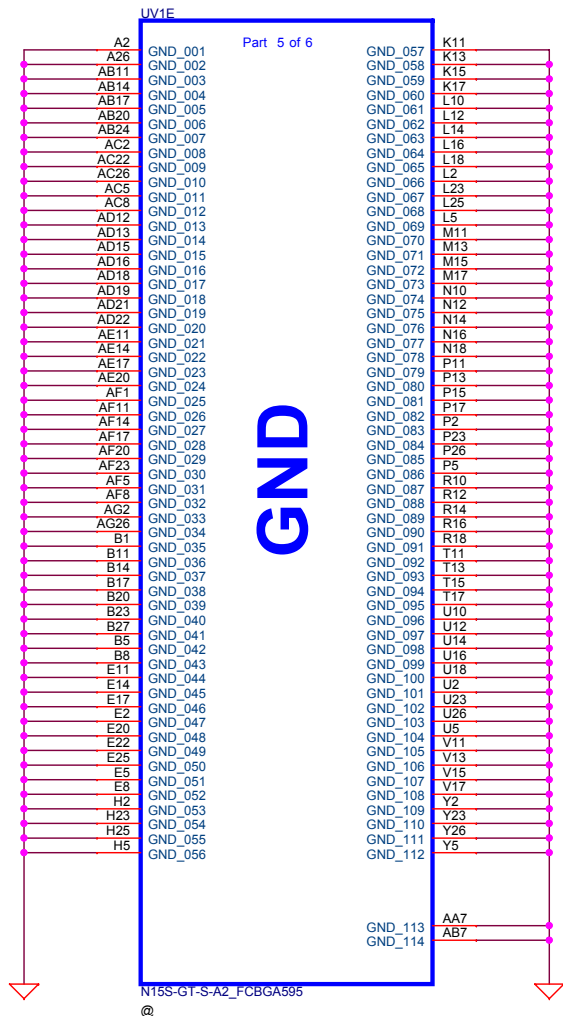
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

+3.3VS TO +3VG\_AON



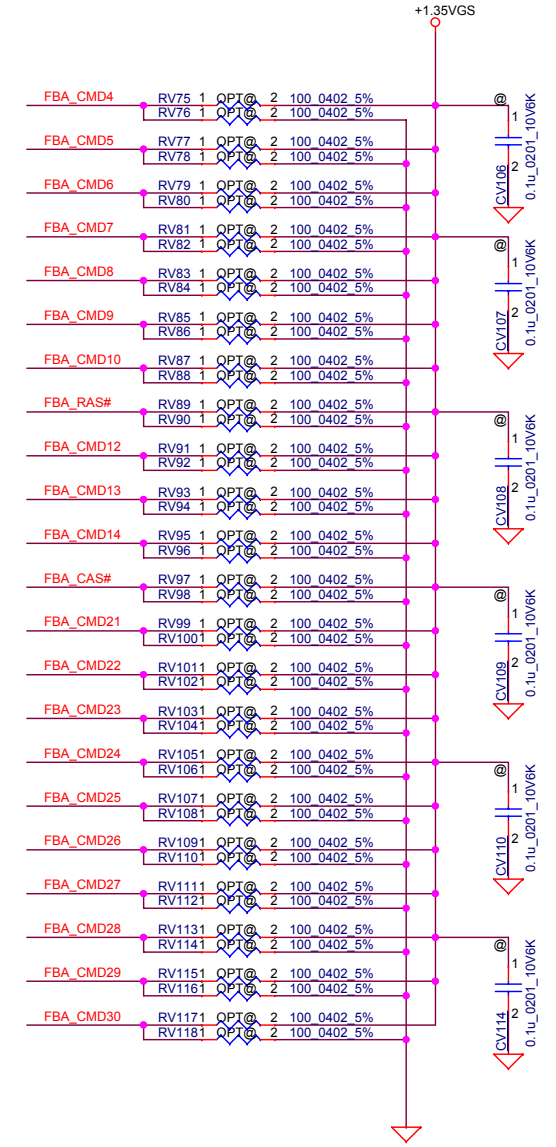
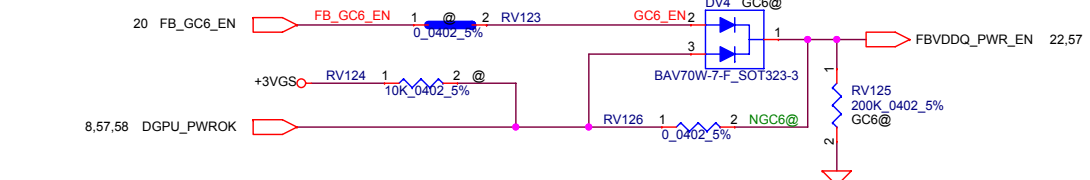
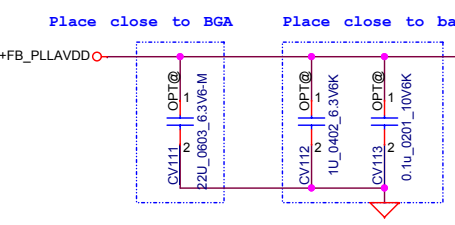
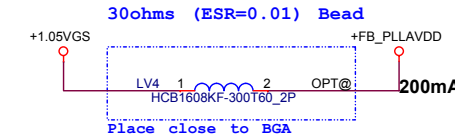
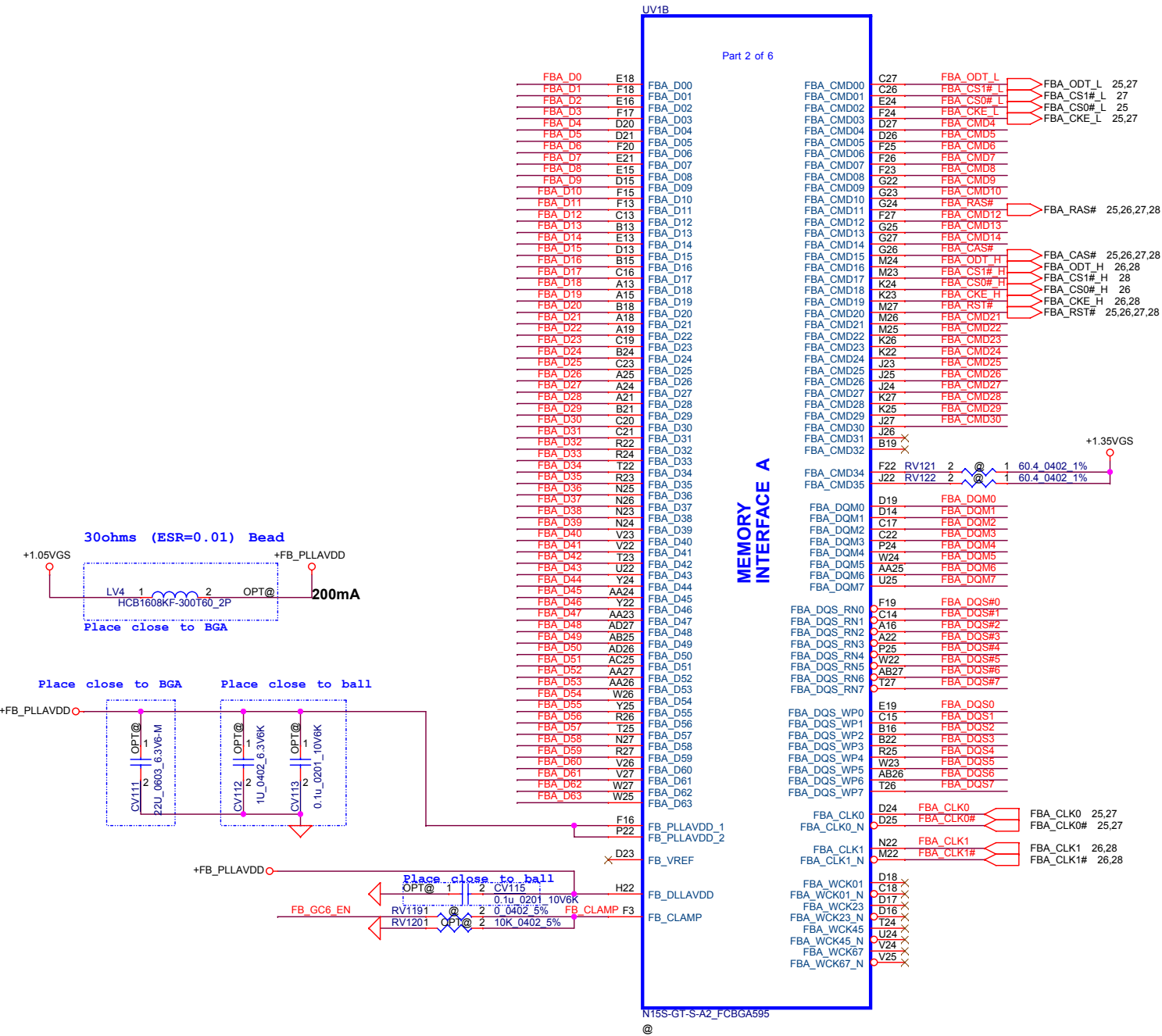
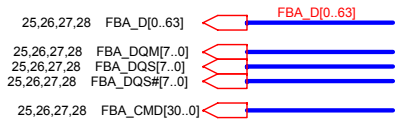
+3.3VS TO +3VGS





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Size	Document Number	Rev	1.0
C	CG411	Date:	Thursday, January 14, 2016   Sheet 23 of 60



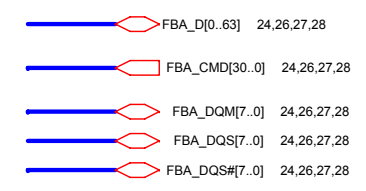
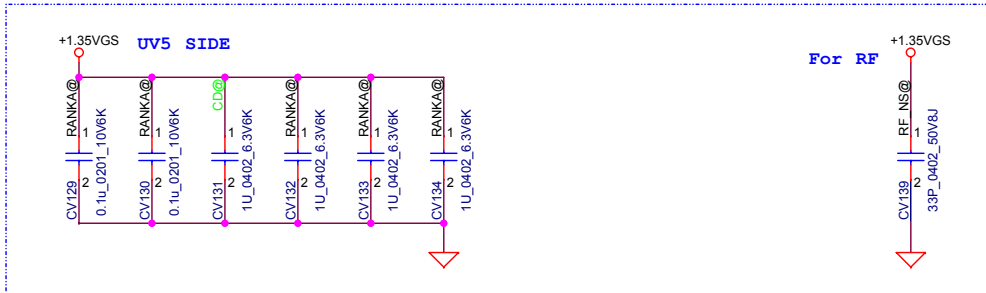
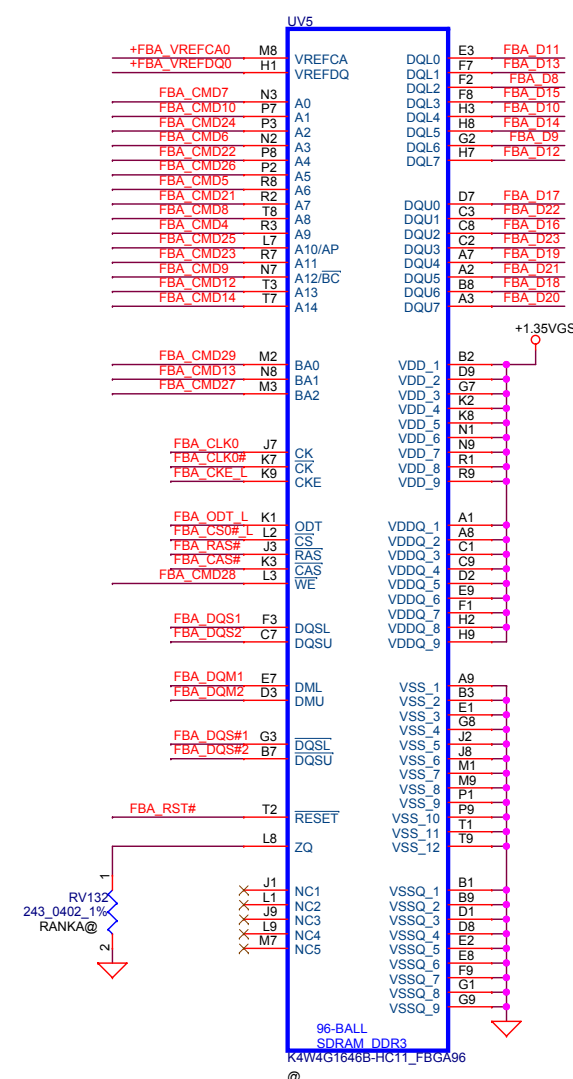
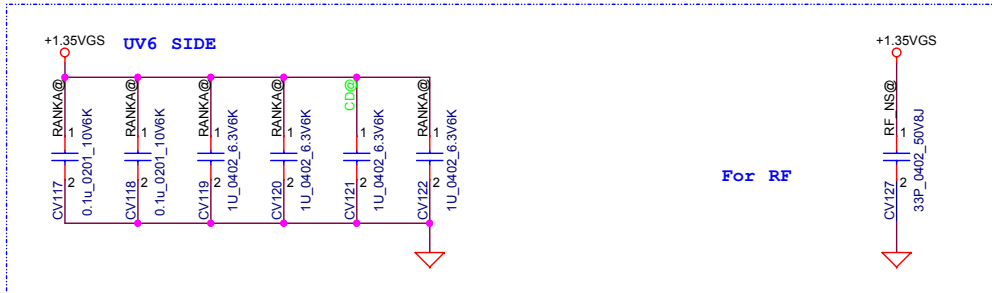
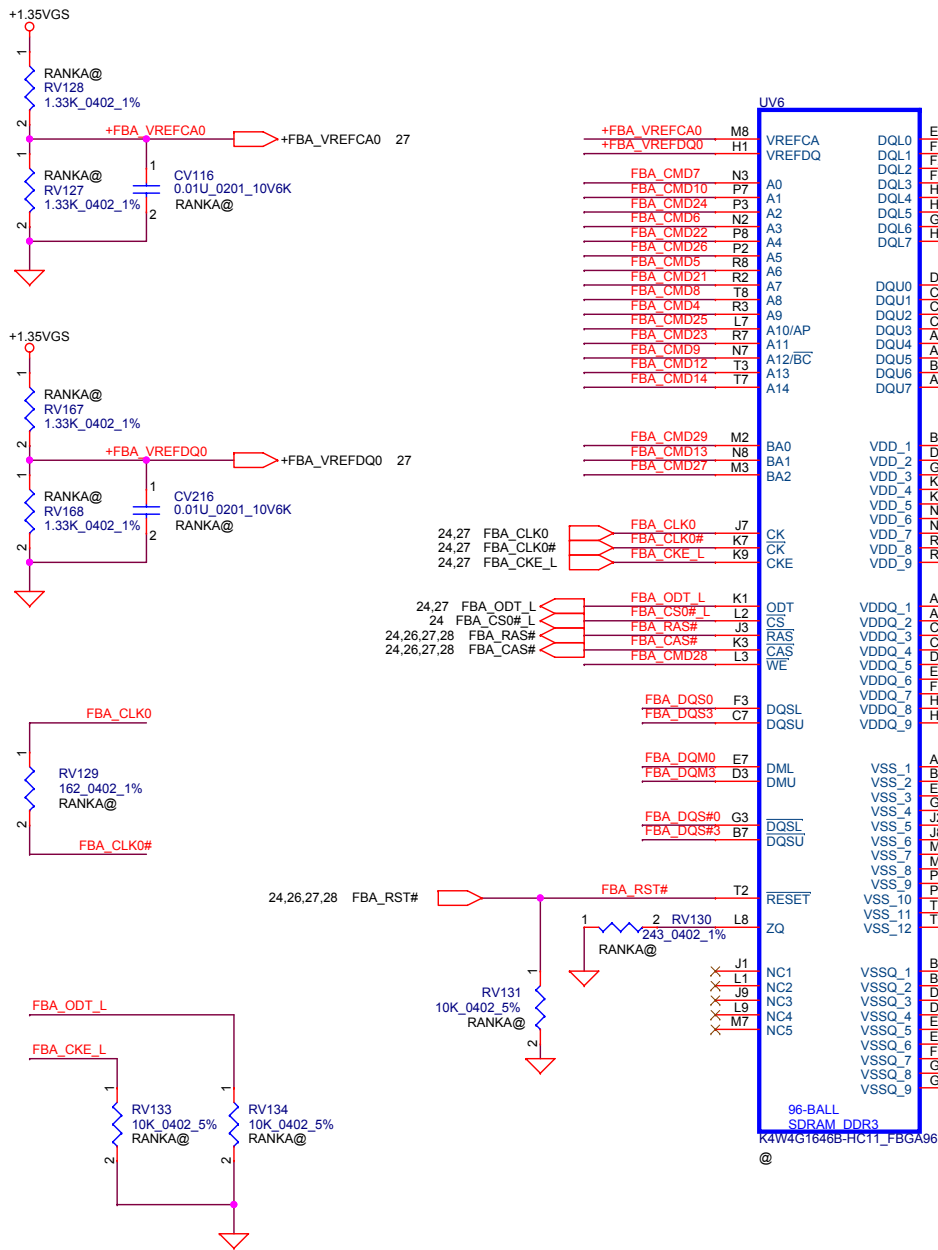


CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16	ODT_H		ODT_H	
FBx_CMD17			CS1#_H	
FBx_CMD18			CS0#_H	
FBx_CMD19			CKE_H	CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

Vinafix

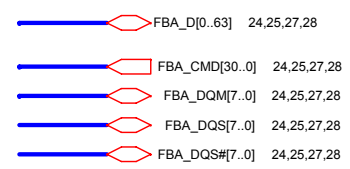
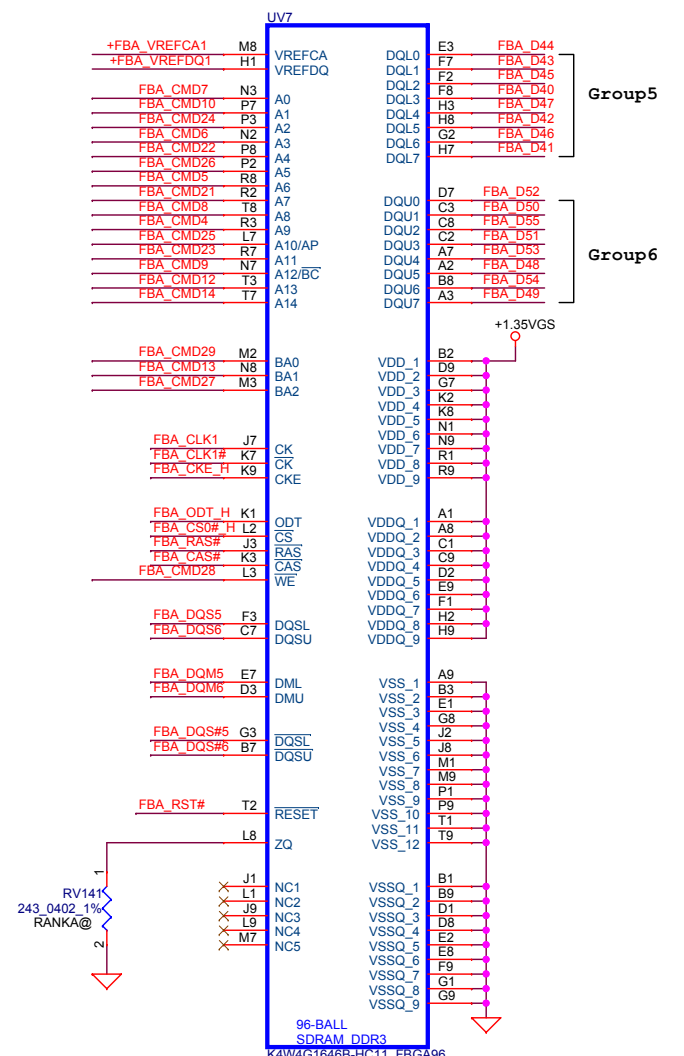
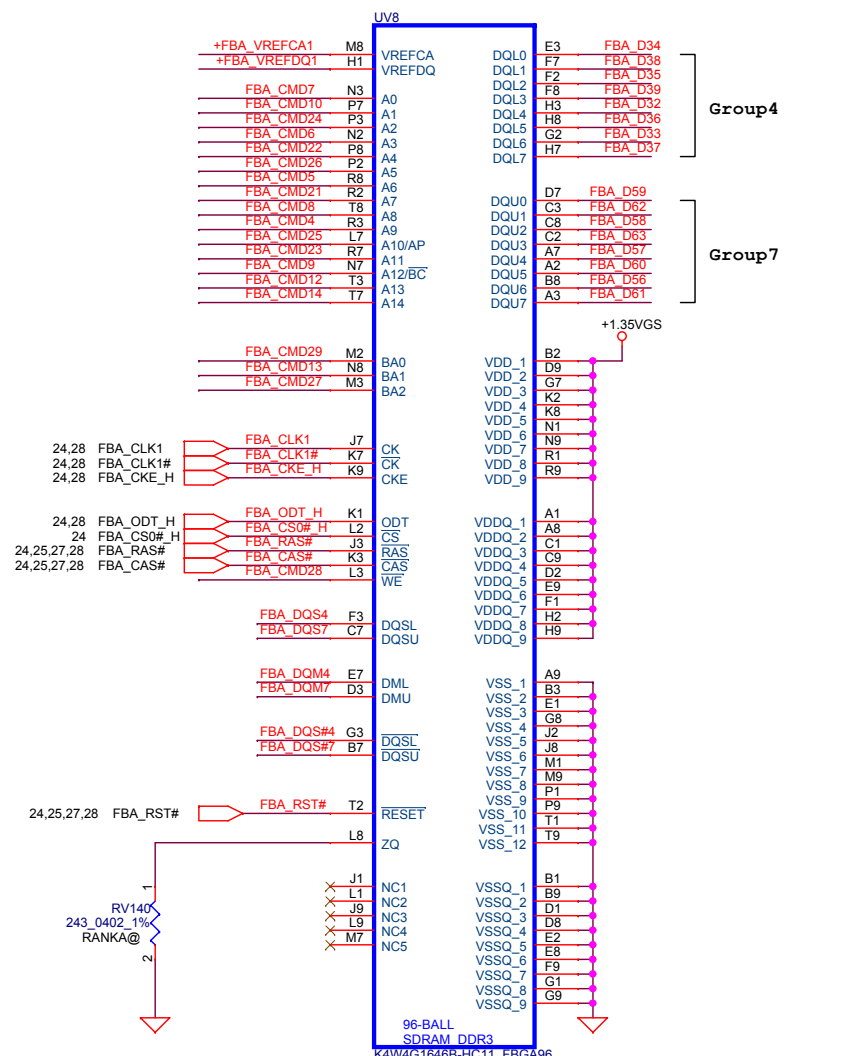
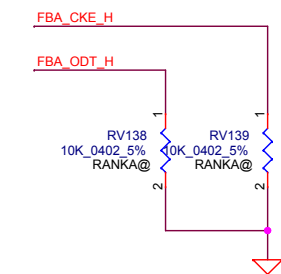
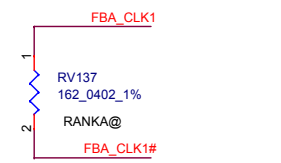
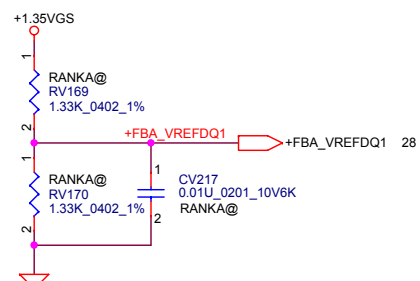
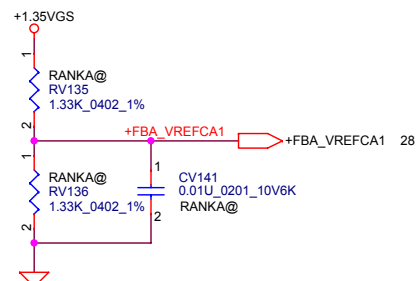
at least 16 mils width(optimal)  
20 mils spacing to other signals /planes



**CMD mapping mod Mode E**

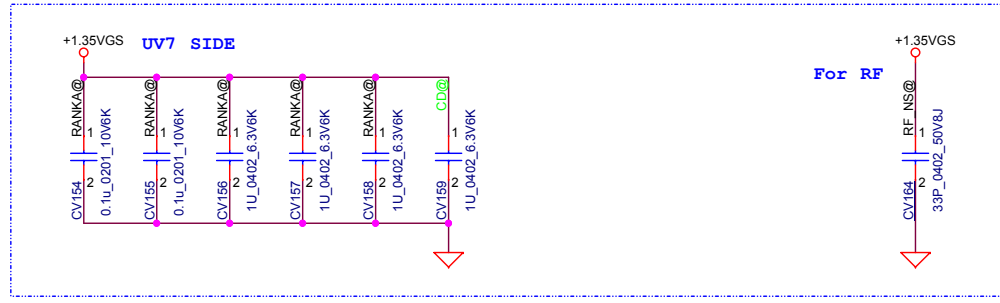
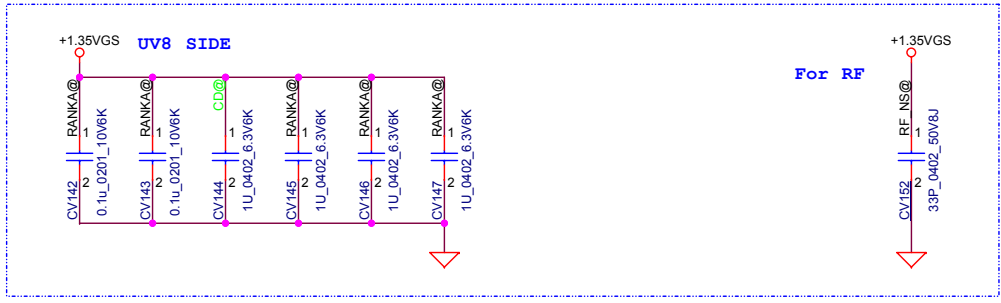
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30		BA2	BA2	BA2

at least 16 mils width(optimal)  
20 mils spacing to other signals /planes

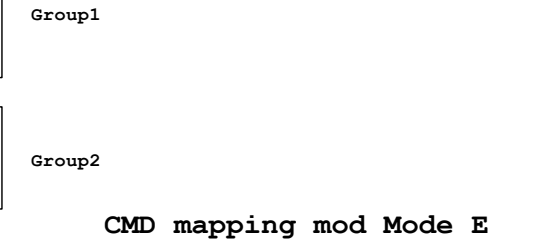
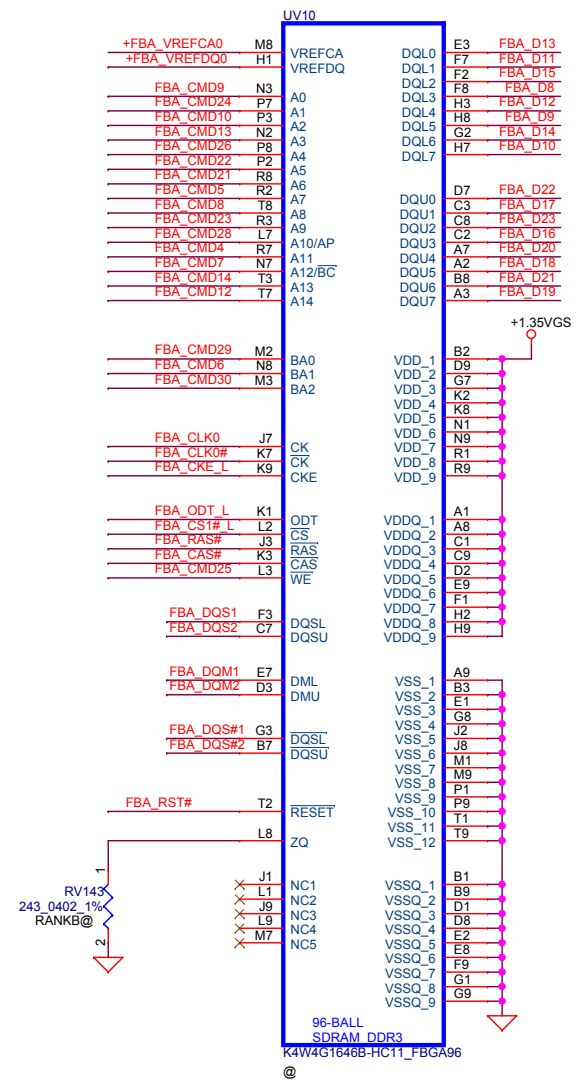
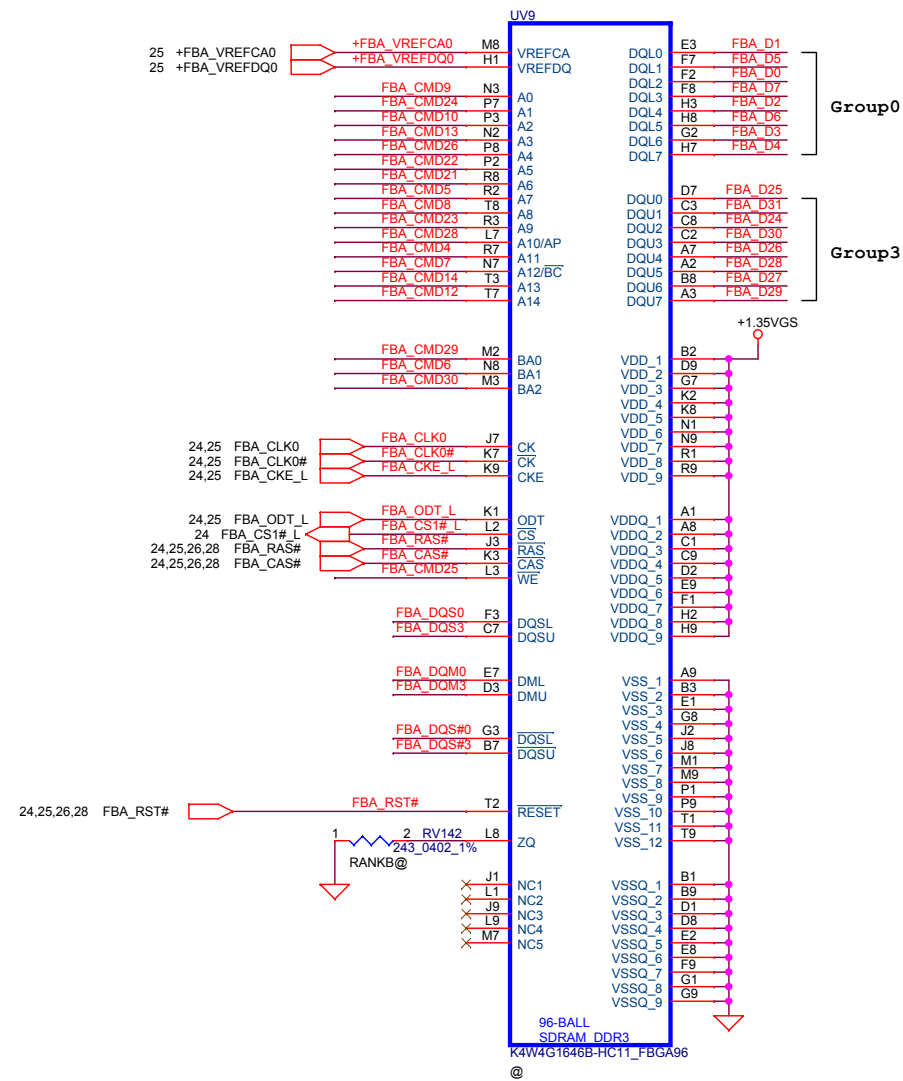
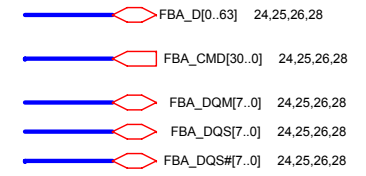


**CMD mapping mod Mode E**

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30		BA2	BA2	

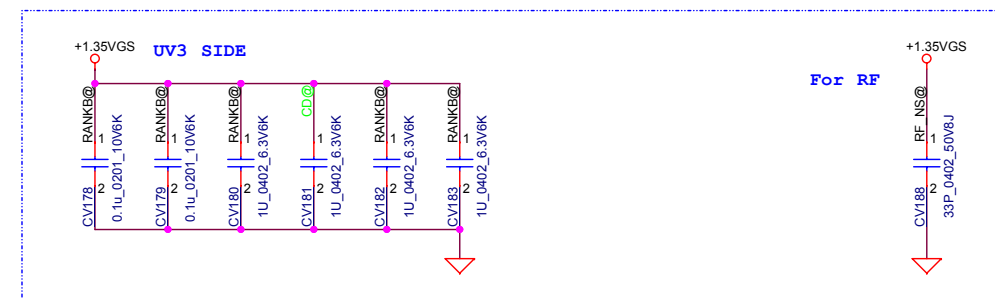
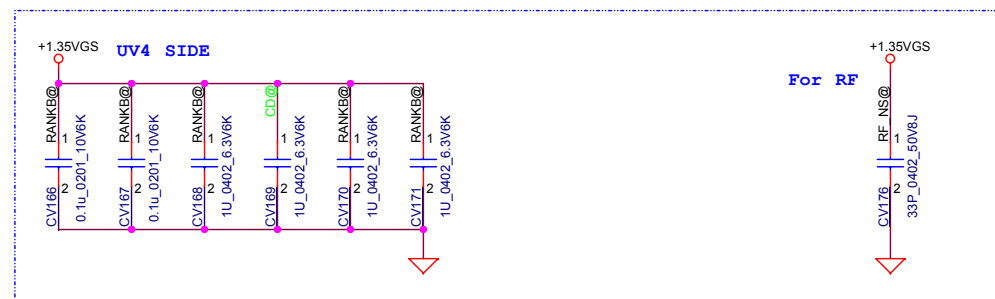


at least 16 mils width(optimal)  
20 mils spacing to other signals /planes

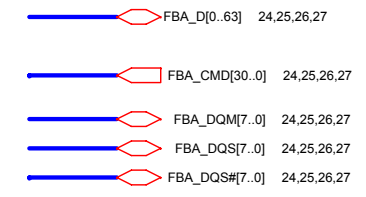


CMD mapping mod Mode E

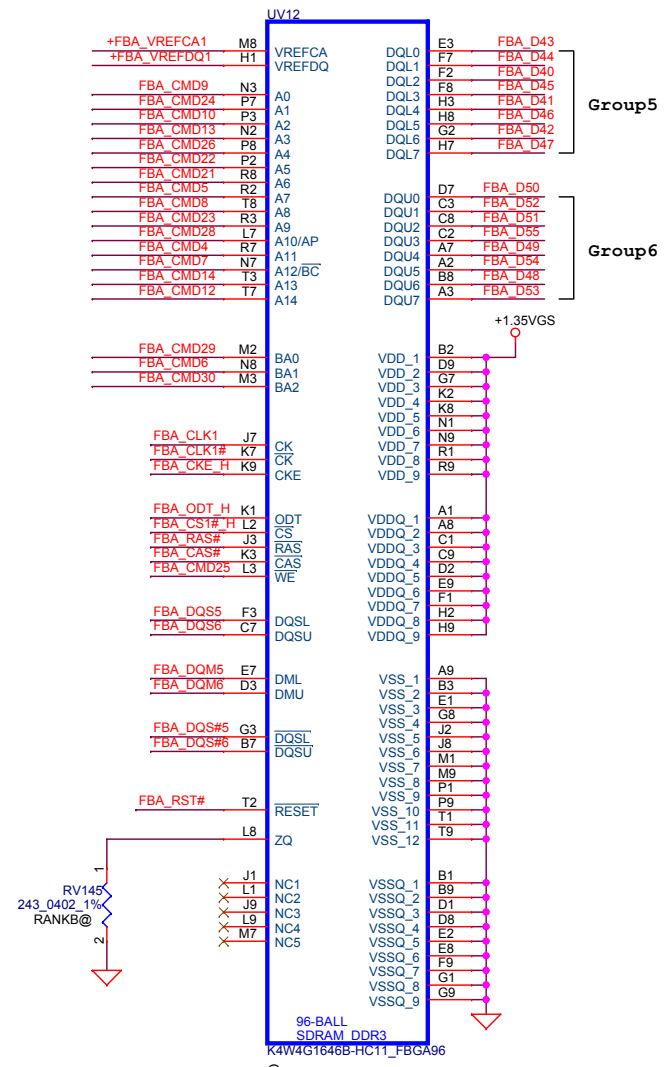
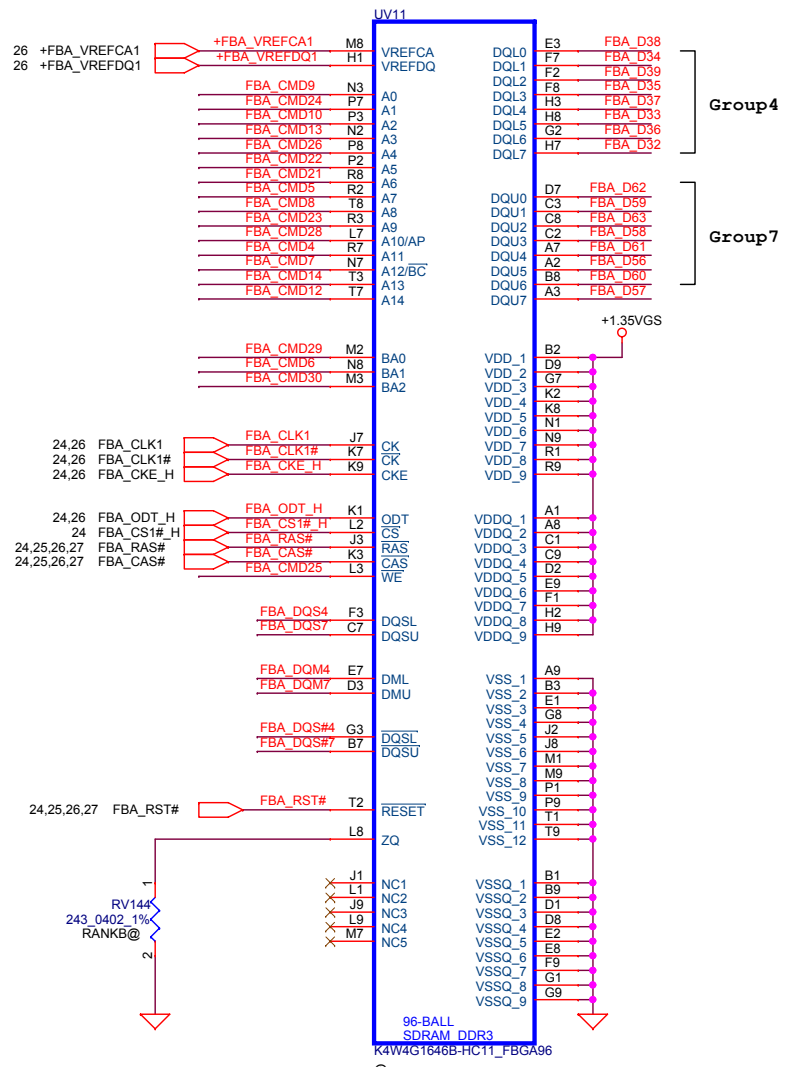
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3			CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16			ODT_H	
FBx_CMD17			CS1#_H	
FBx_CMD18			CS0#_H	
FBx_CMD19			CKE_H	
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





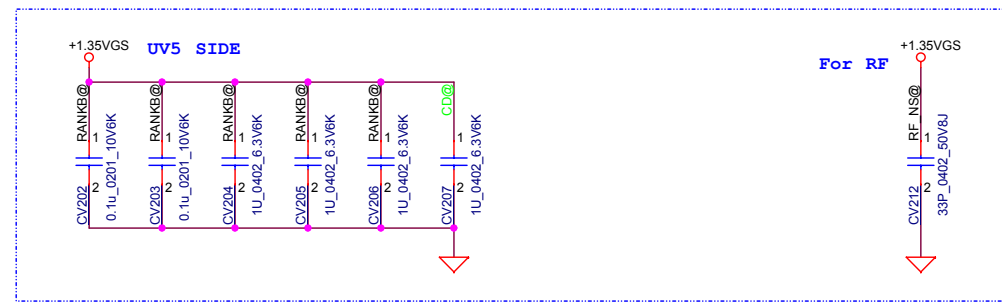
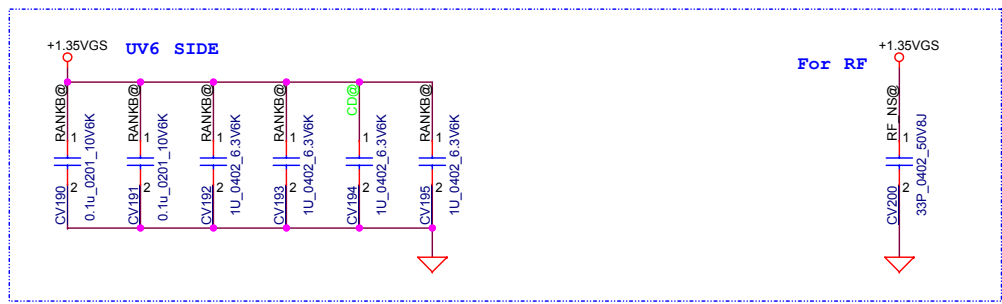


at least 16 mils width(optimal)  
20 mils spacing to other signals /planes

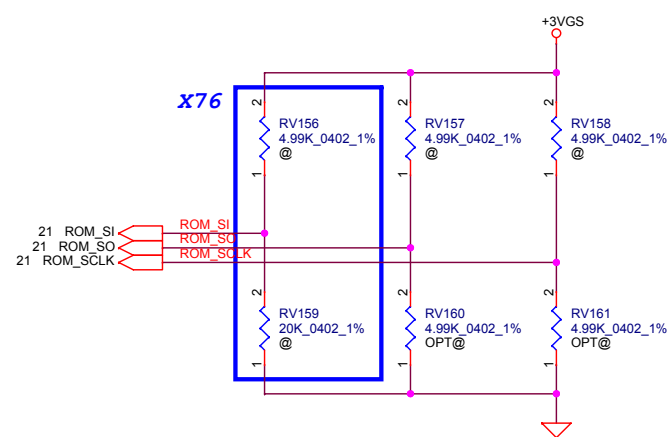
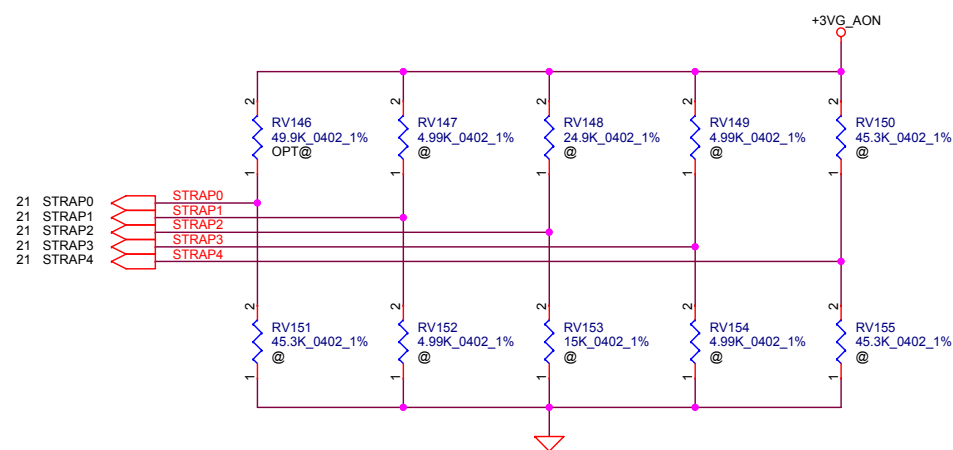


CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H	ODT_H	
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H	CKE_H	
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2







Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

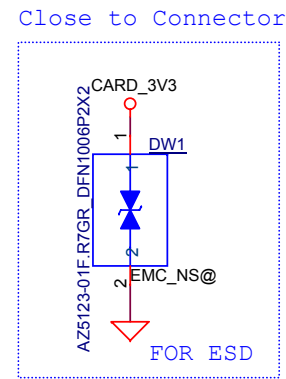
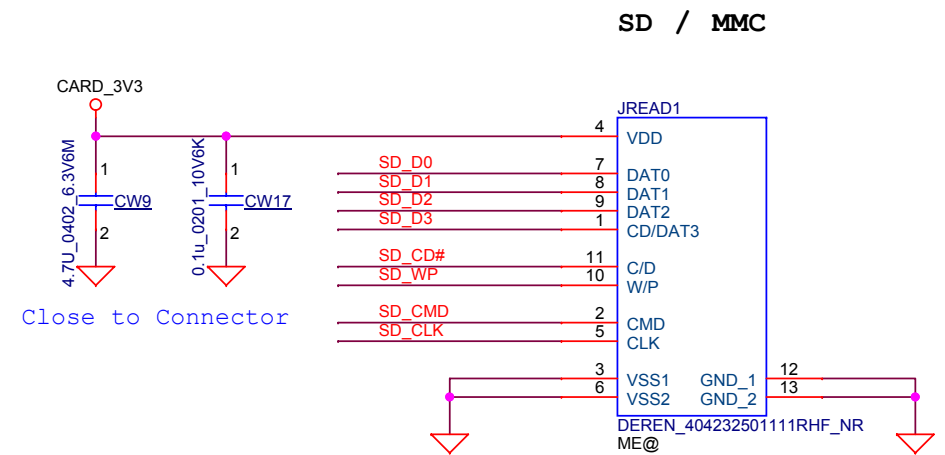
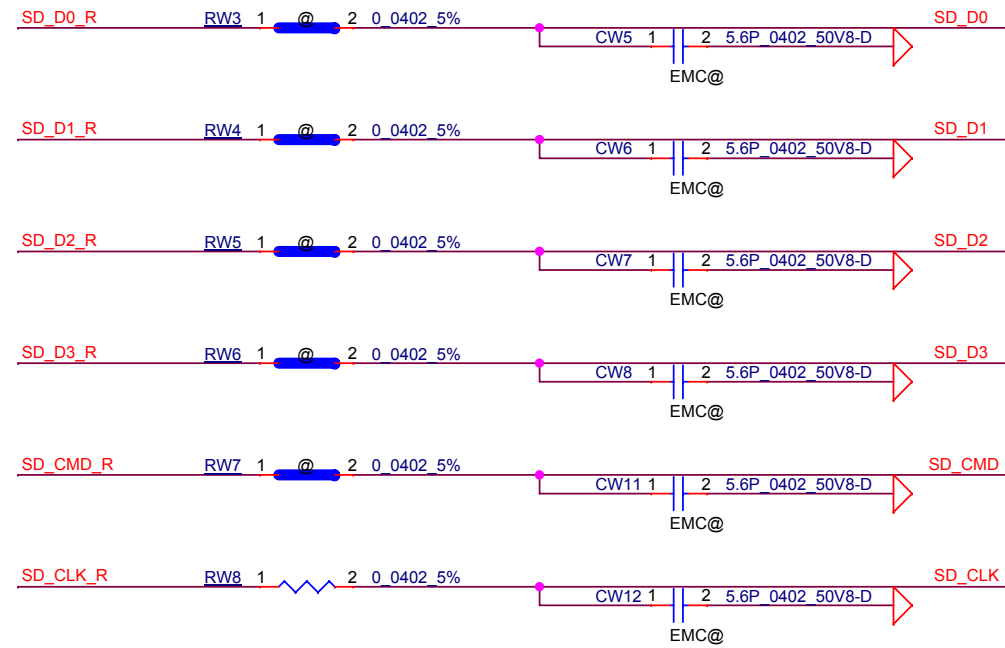
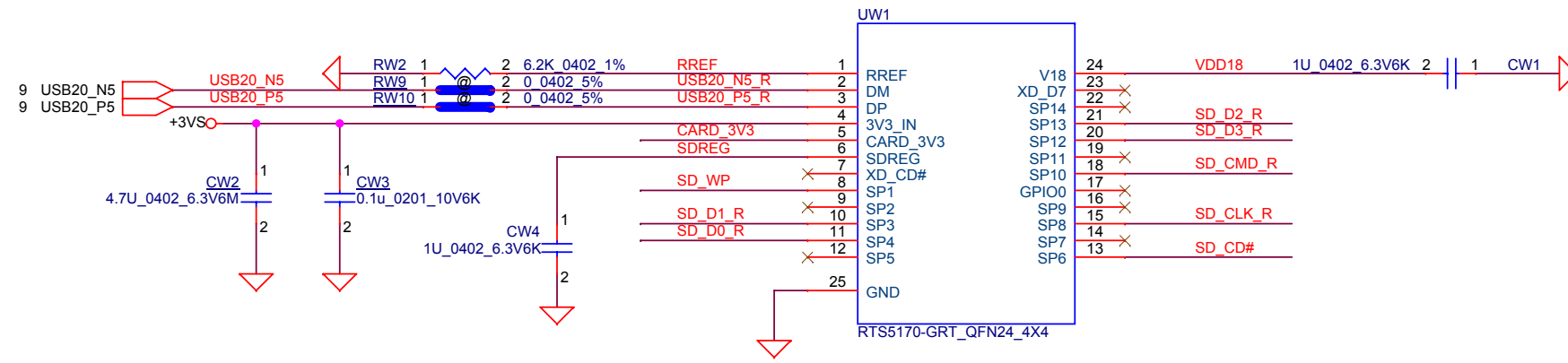
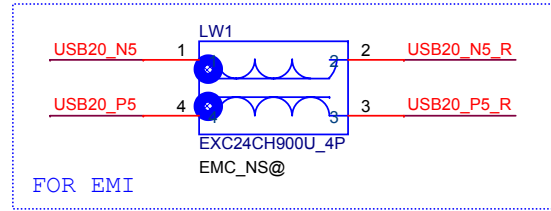
PCIE_CFG	
0	(Default)
1	


SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

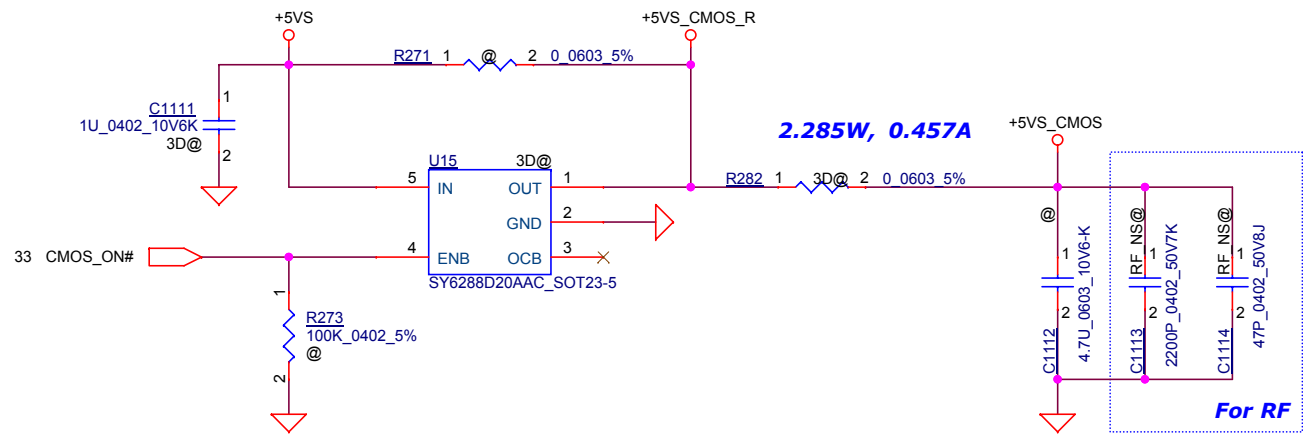
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	Configuration	FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	Single-Rank	Samsung 900MHz K4W4G1646E-BC1A 256M x 16	0x1 PD 10K	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		Hynix 900MHz H5TC4G63CFR-NOC 256M x 16	0x2 PD 15K							
		Micron 900MHz MT41J256M16LY-091G:N 256M x 16	0x6 PD 34.8K							
	Dual-Rank	Samsung 900MHz K4W4G1646E-BC1A 256M x 16	0xF PU 45.3K							
		Hynix 900MHz H5TC4G63CFR-NOC 256M x 16	0xE PU 34.8K							
		Micron 900MHz MT41J256M16LY-091G:N 256M x 16	0xA PU 15K							

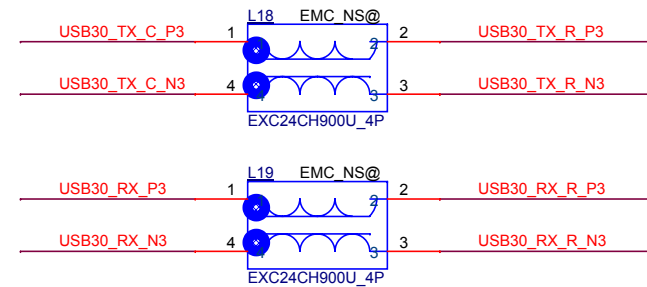
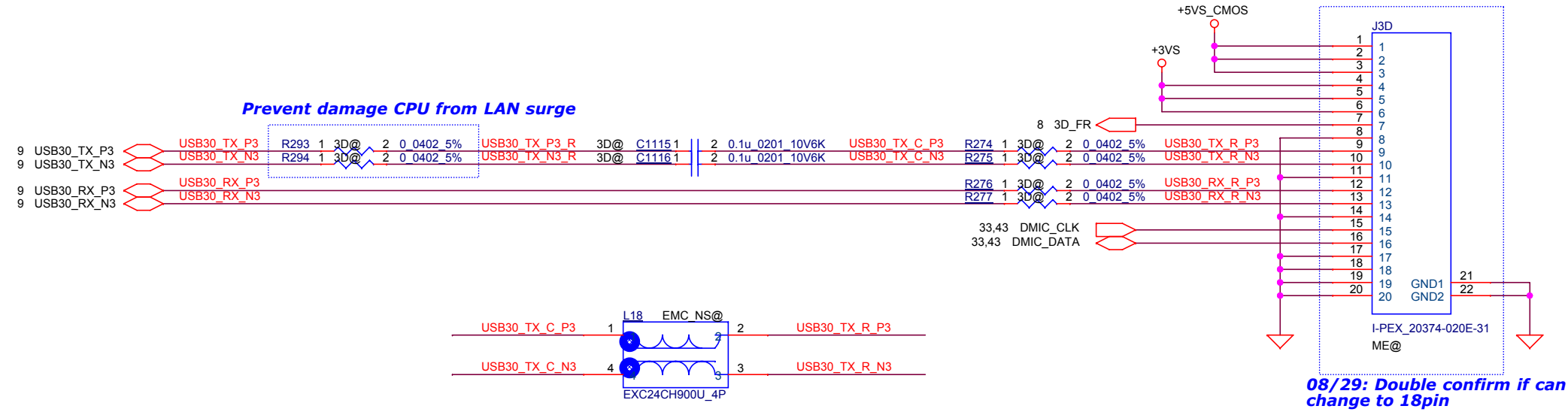
VRAM	X76 P/N	VRAM Q'ty	VRAM P/N
Samsung	X7610212201	4	SA000063F20
	X7610212001	8	
Hynix	X7610212202	4	SA00007DU10
	X7610212101	8	
Micron	X7610212203	4	SA00007QJ00
	N/A	8	



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Issued Date	2015/08/20	Deciphered Date		
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Size Custom	Document Number <b>CG411</b>		Rev 1.0	
Date:	Thursday, January 14, 2016		Sheet 30 of 60	

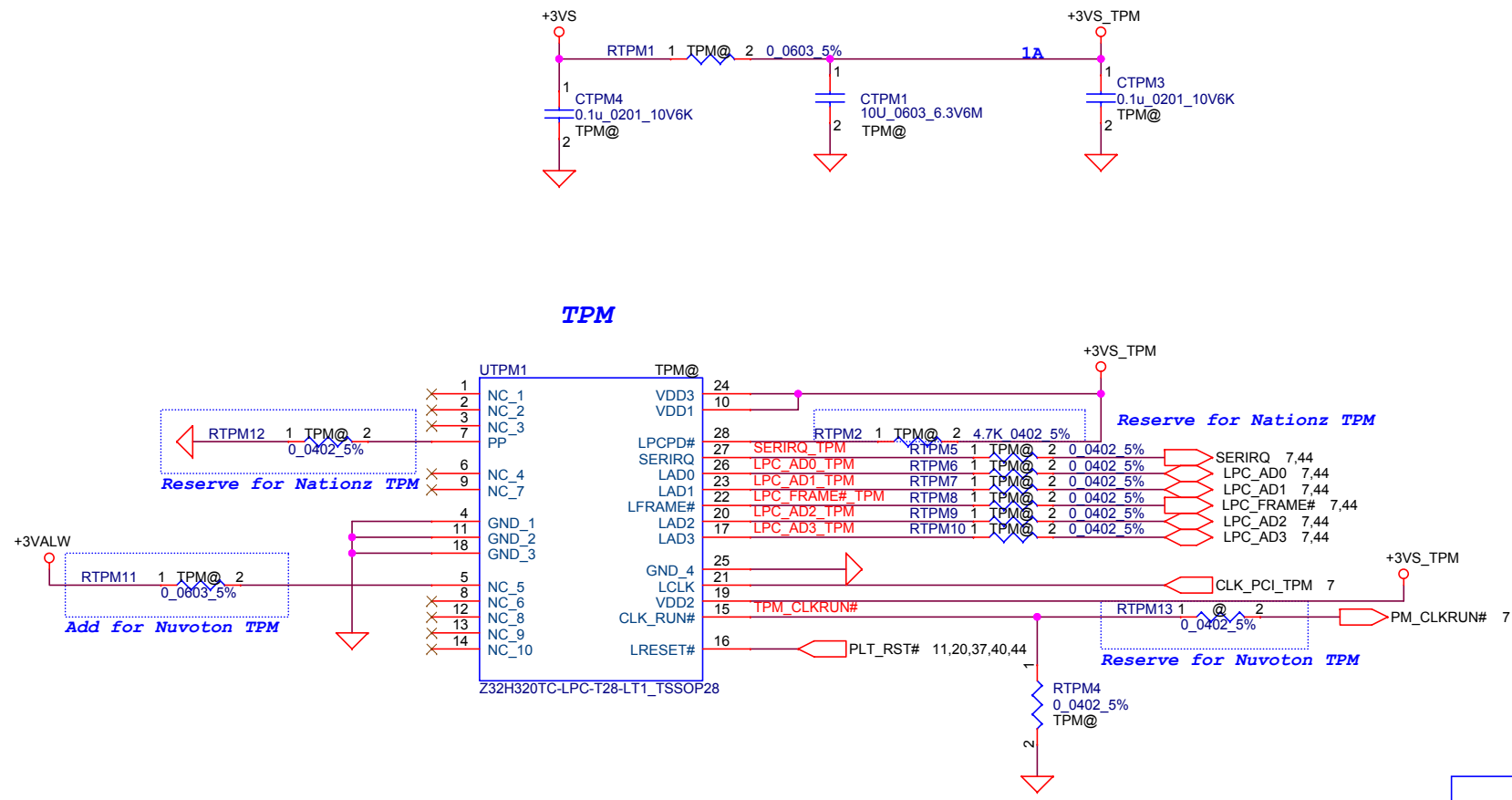


### 3D Camera DB Connector




Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/08/20	Deciphered Date	2016/08/20
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			Document Number <b>CG411</b>
			Rev 1.0
			Date: Thursday, January 14, 2016
			Sheet 31 of 60

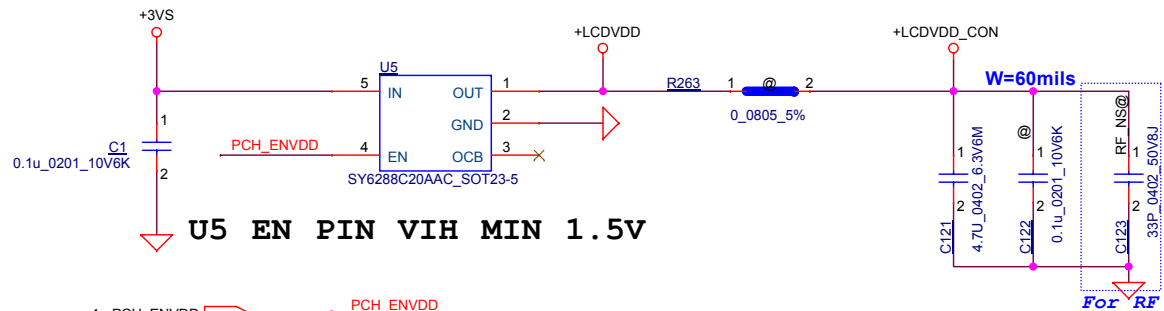




	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

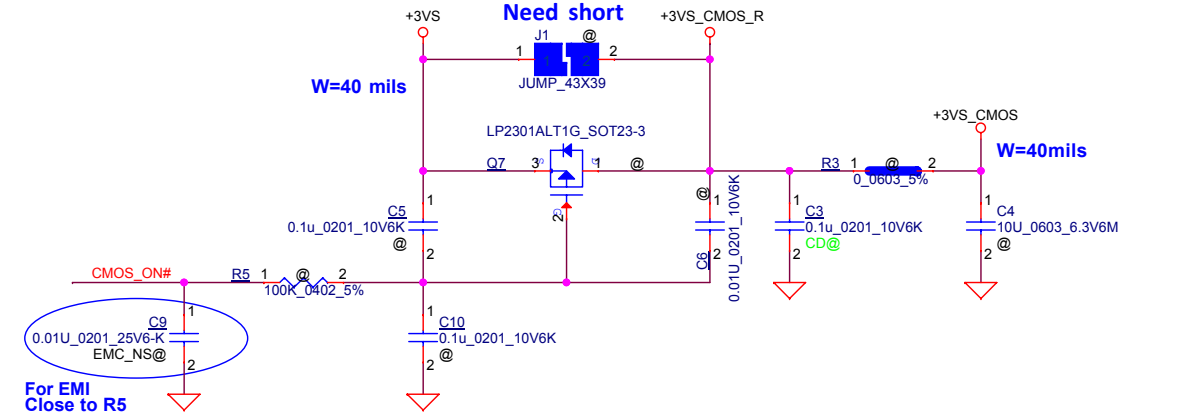
Security Classification	LC Future Center Secret Data		Title			
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Title		TPM
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# LCD POWER CIRCUIT

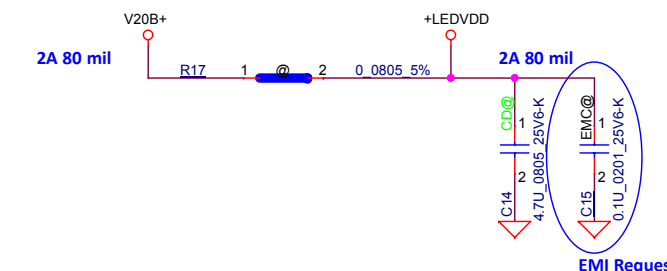
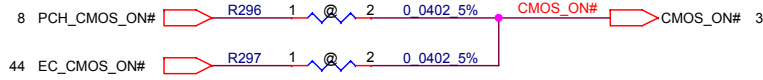


U5 EN PIN VIH MIN 1.5V

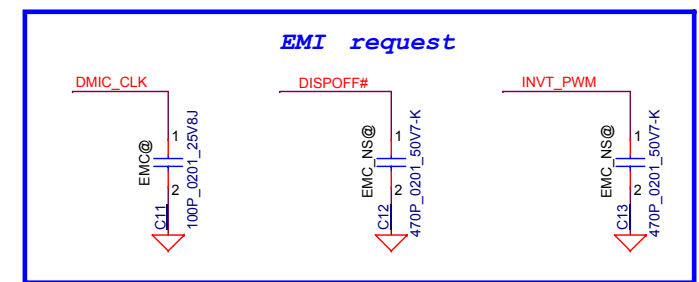
# CMOS Camera



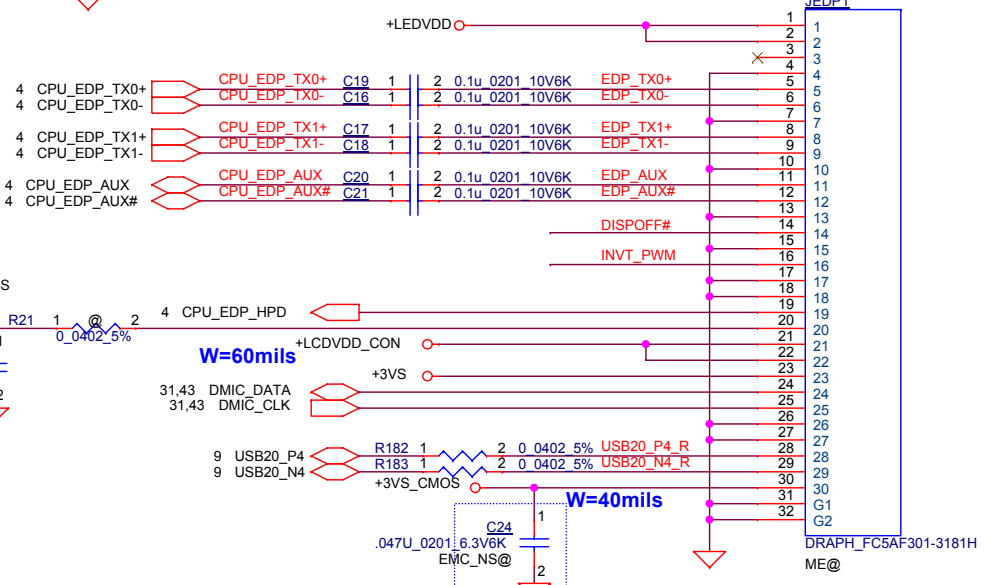
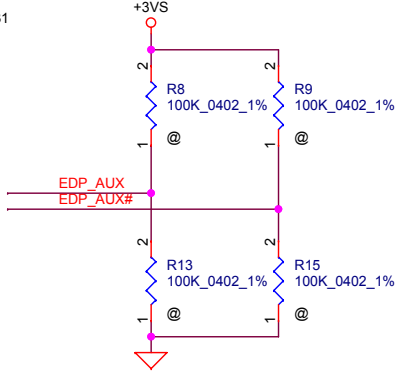
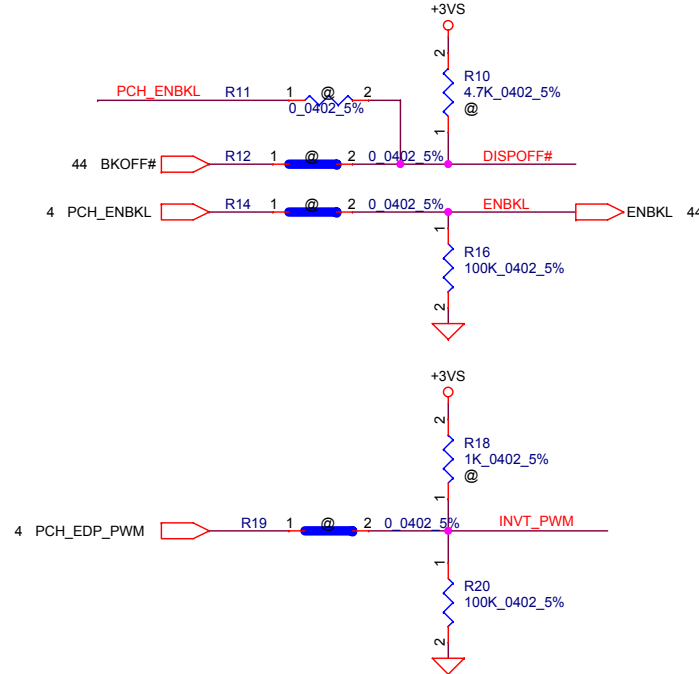
For EMI Close to R5



EMI Request

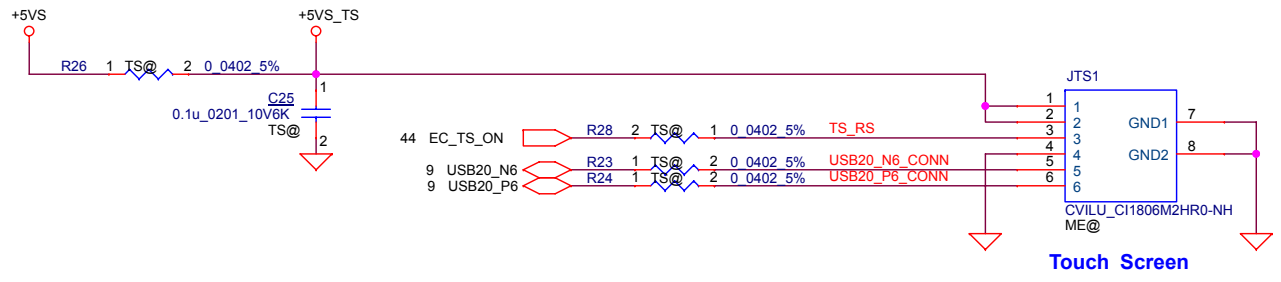


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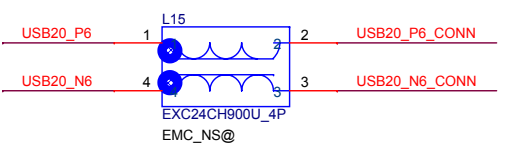


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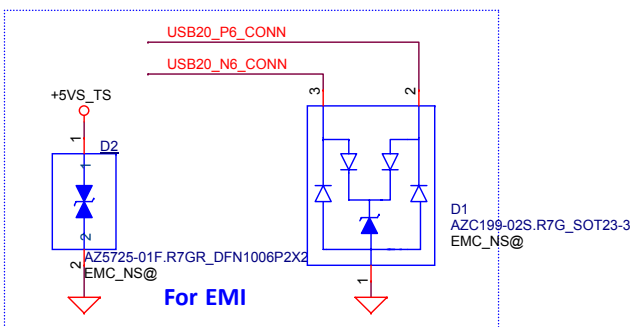
# Touch Screen



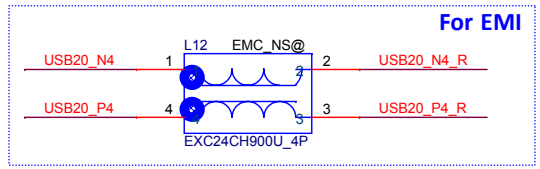
Touch Screen



For EMI



For EMI

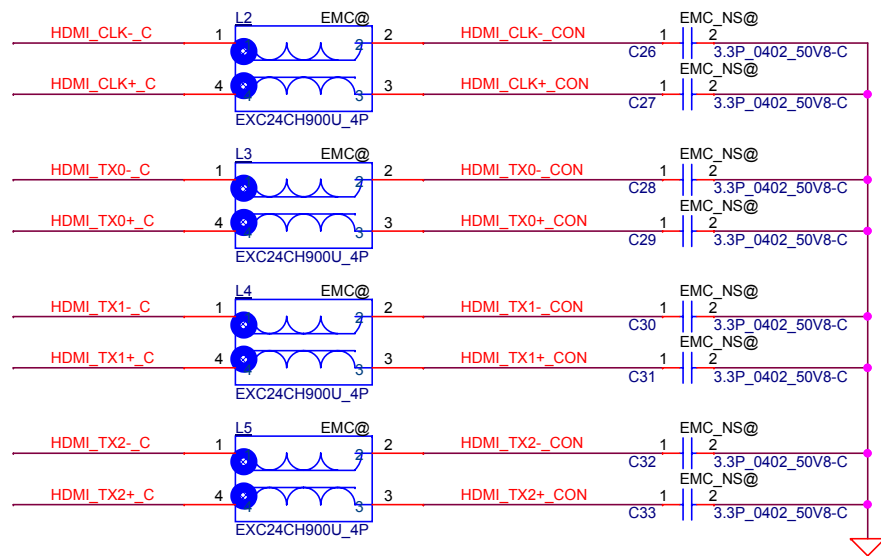


For EMI

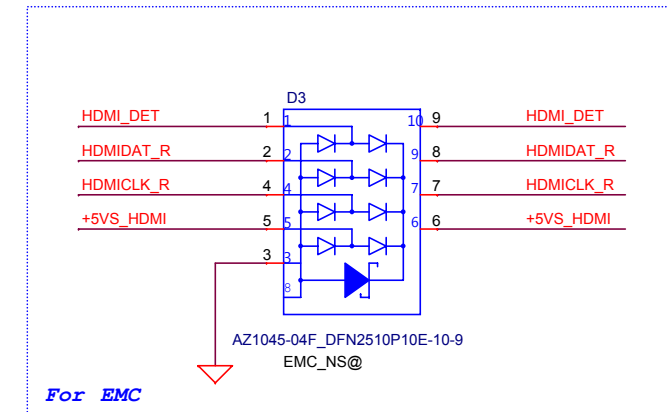
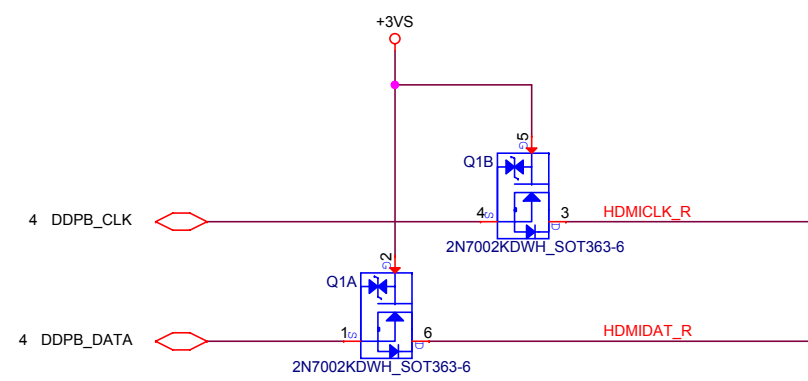
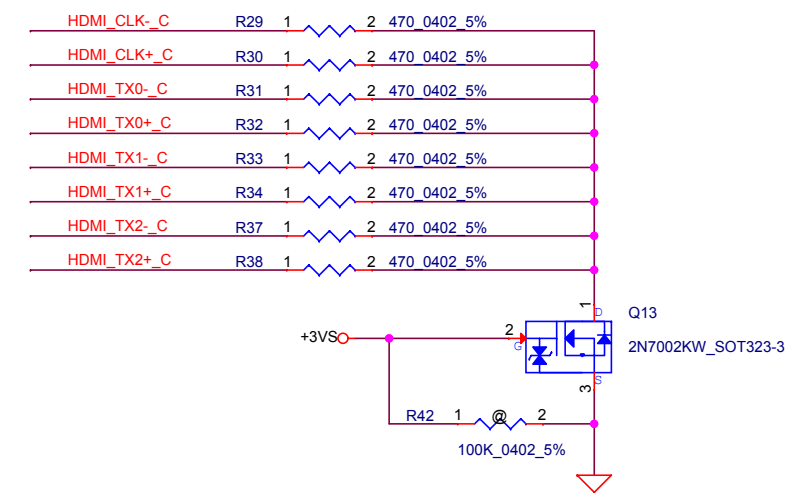
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Issued Date	2015/08/20	Deciphered Date
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Title		LCFC
eDP/CMOS/Touch screen		
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Custom	CG411	1.0
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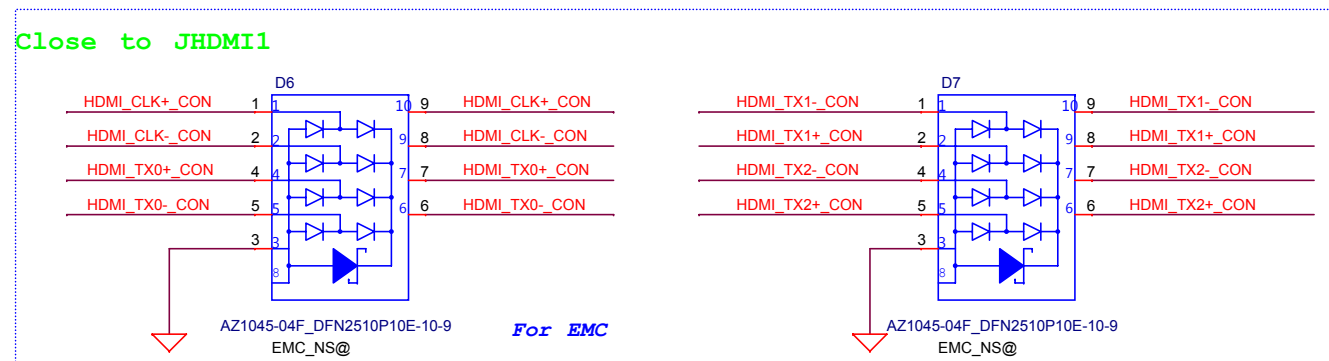
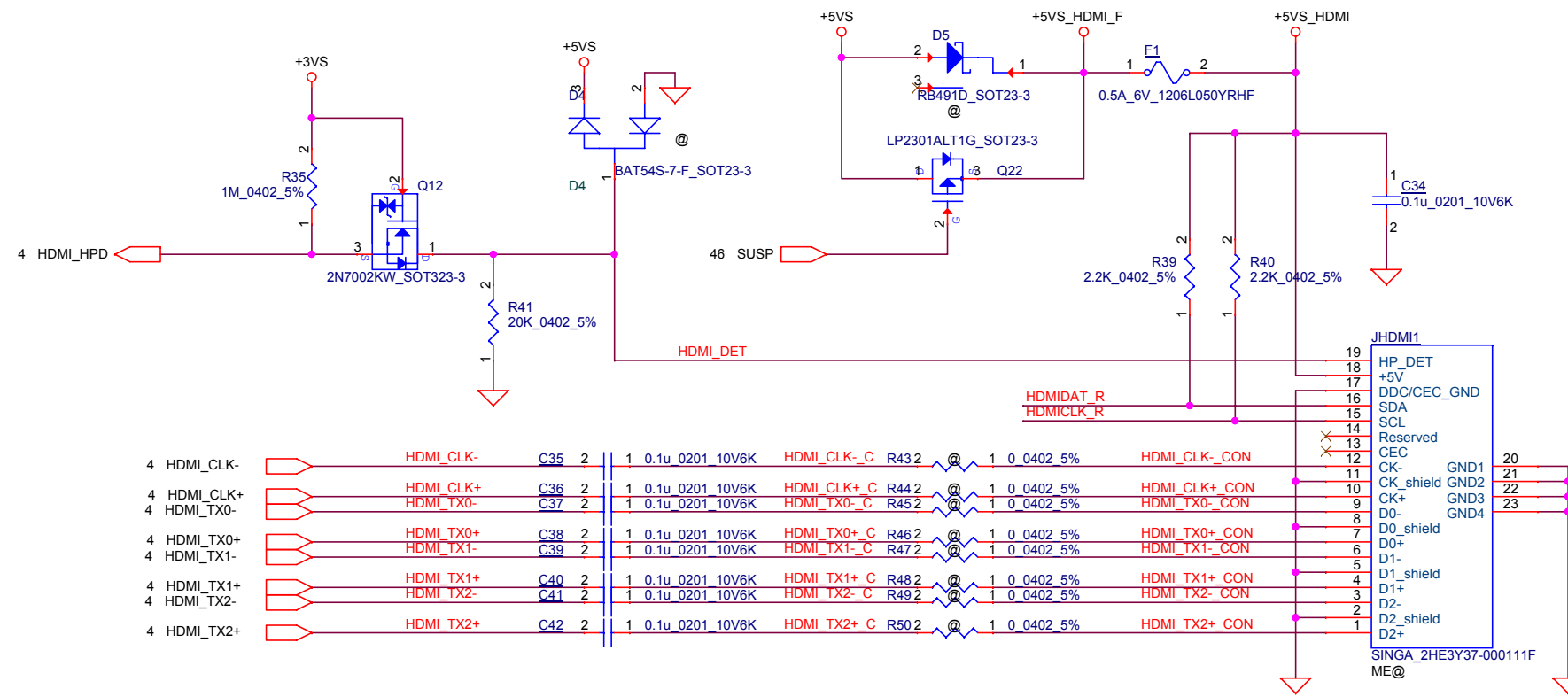




For EMC



For EMC

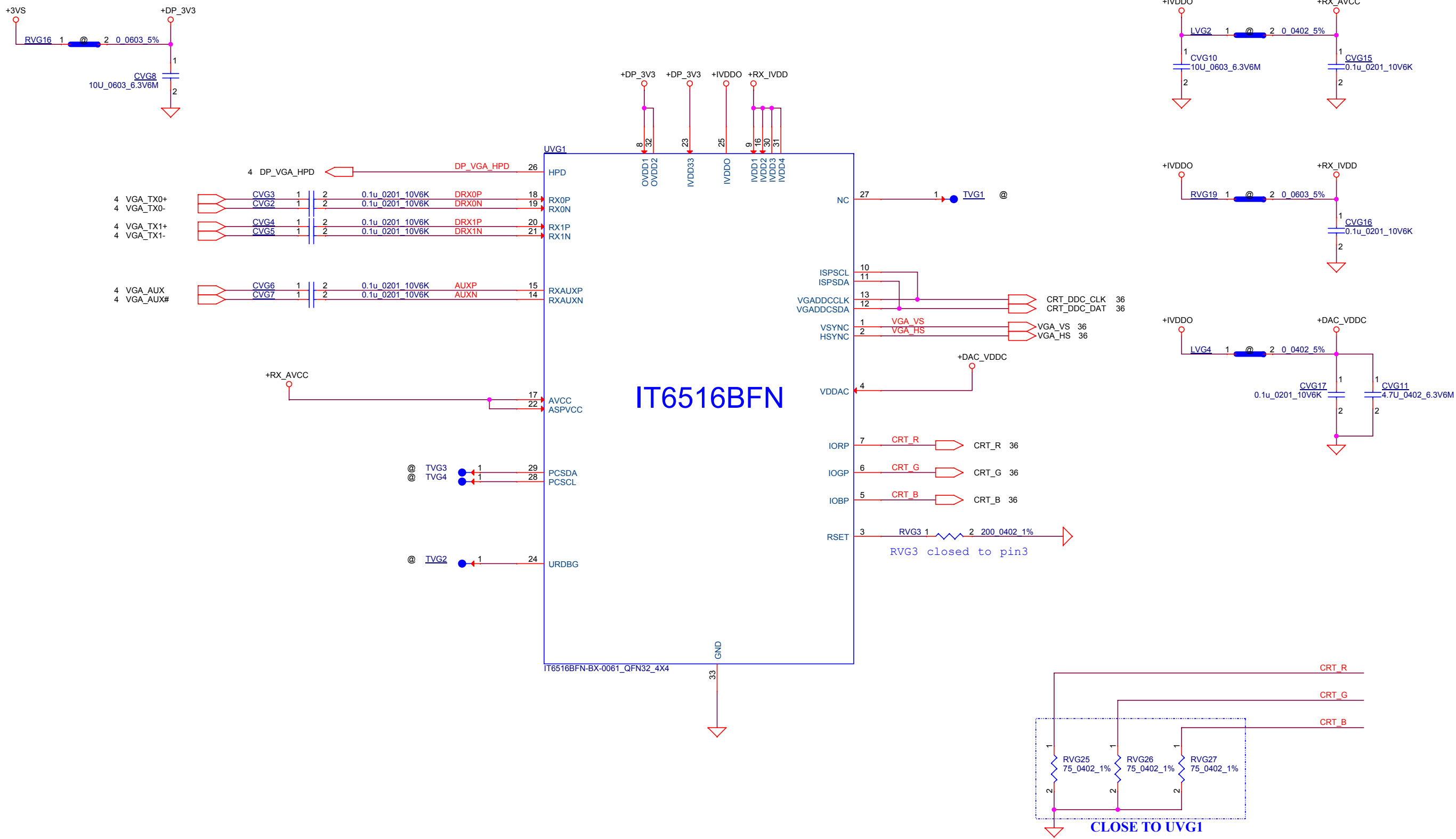


For EMC

For EMC

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Size	Custom	Document Number	<b>CG411</b>		Rev
Date:	Thursday, January 14, 2016	Sheet	34	of	60

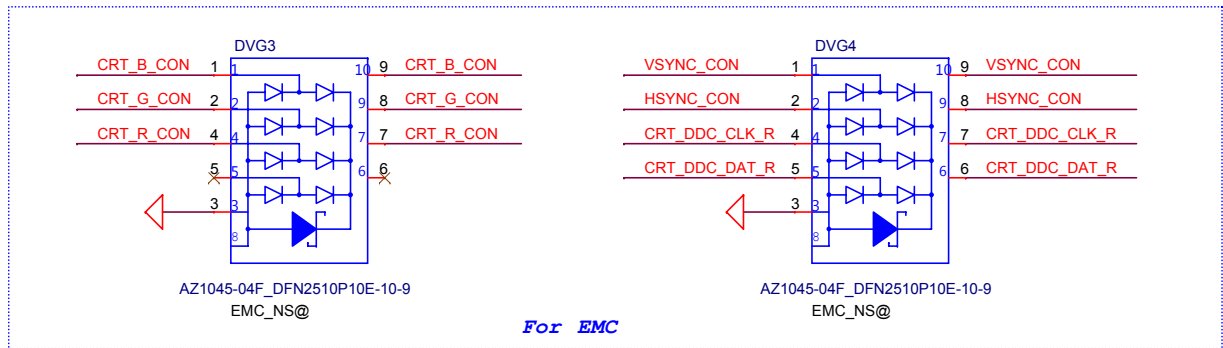
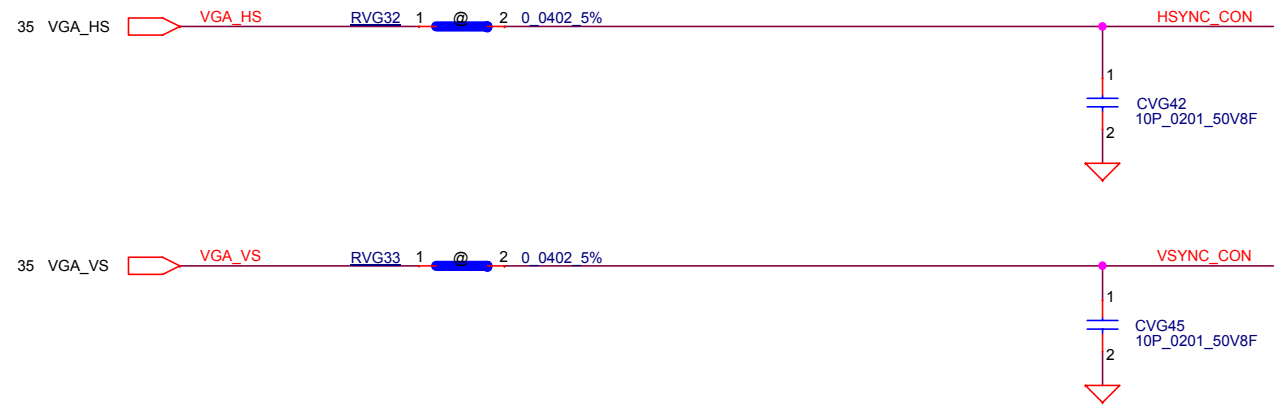
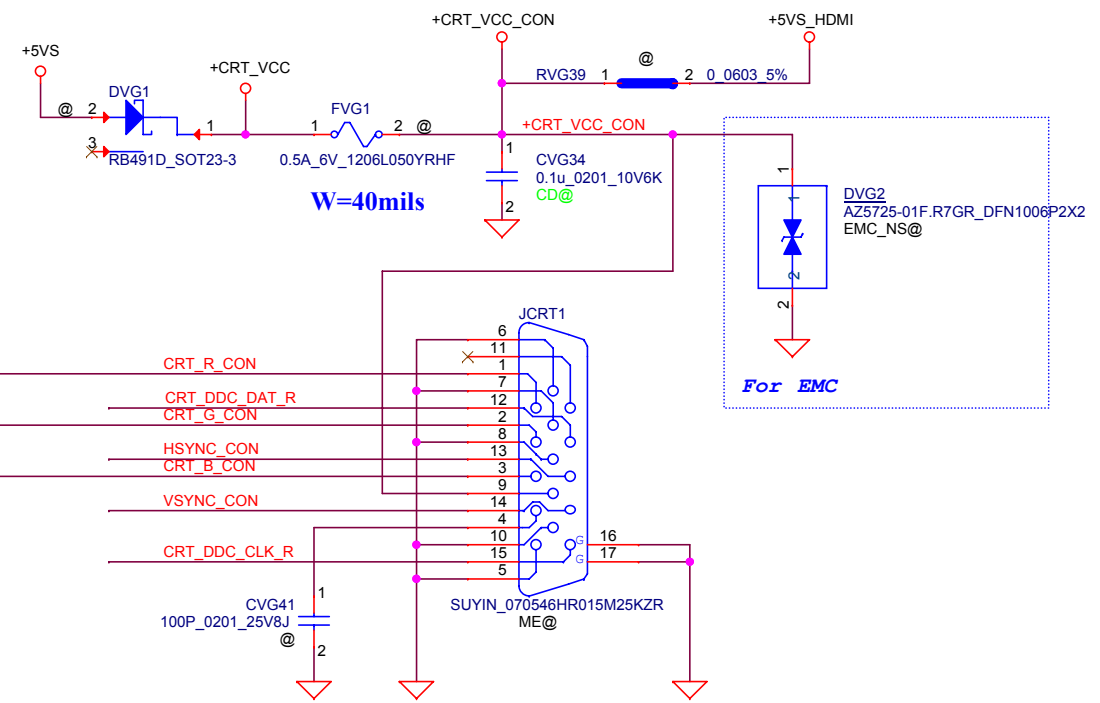
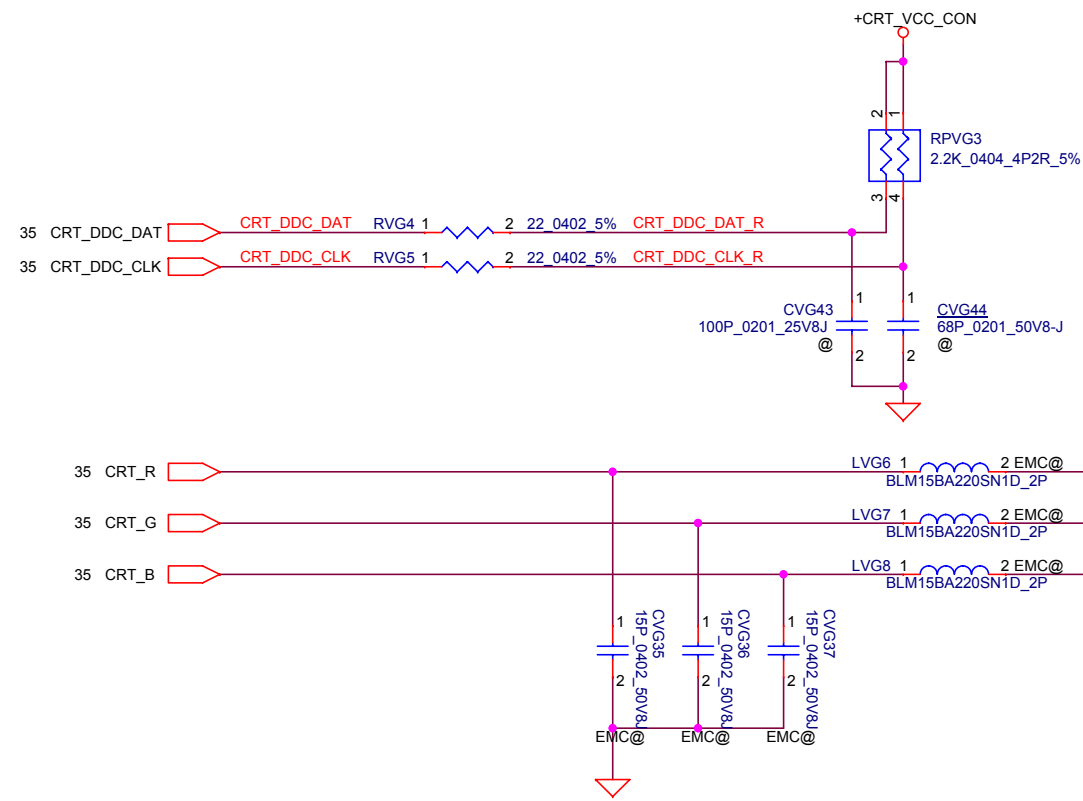




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Title			
DP to VGA (IT6516BFN)			
Size	Document Number	Rev	1.0
Custom	CG411		
Date:	Thursday, January 14, 2016	Sheet	35 of 60

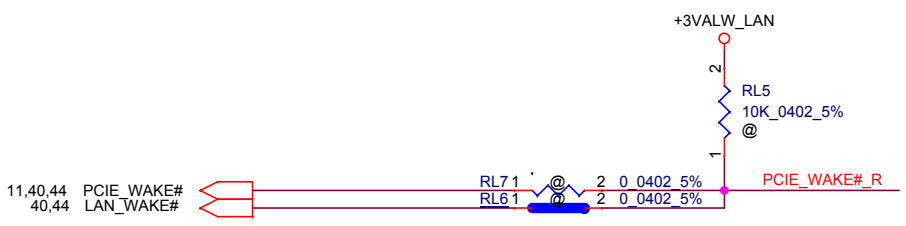
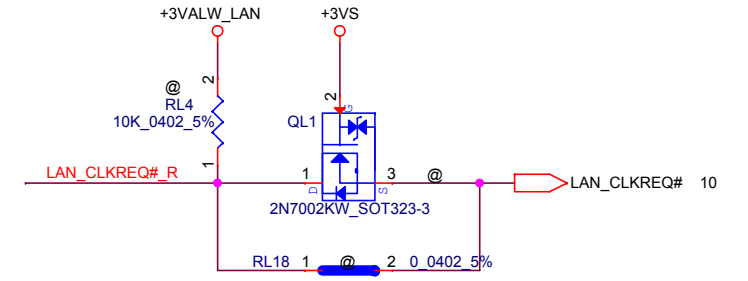
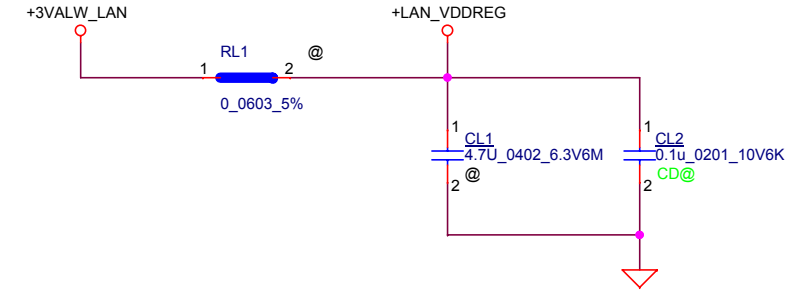
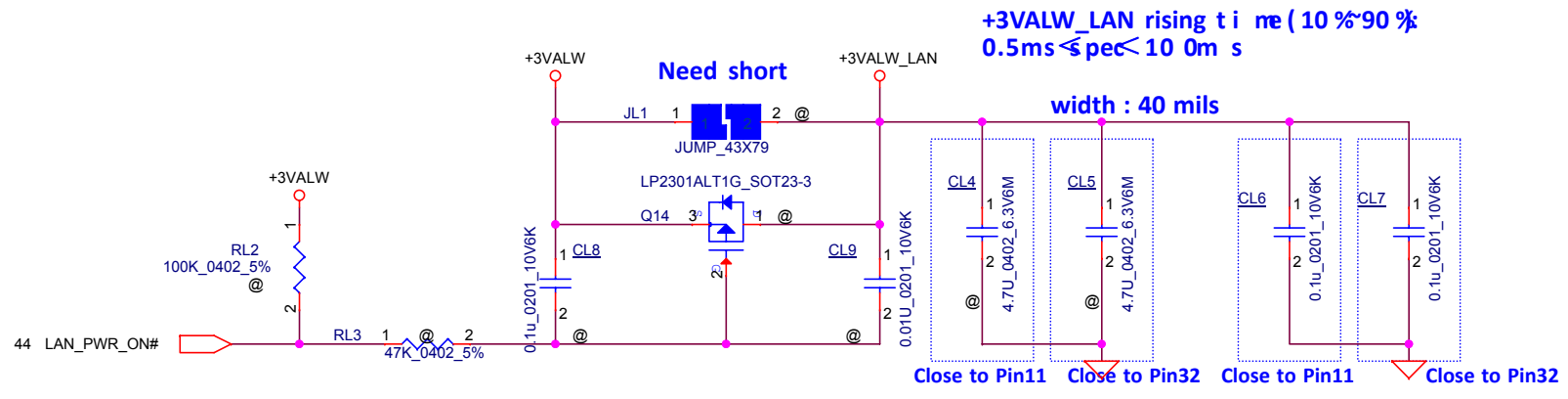
# CRT Connector



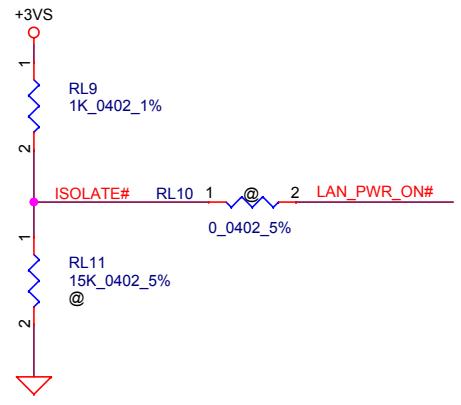
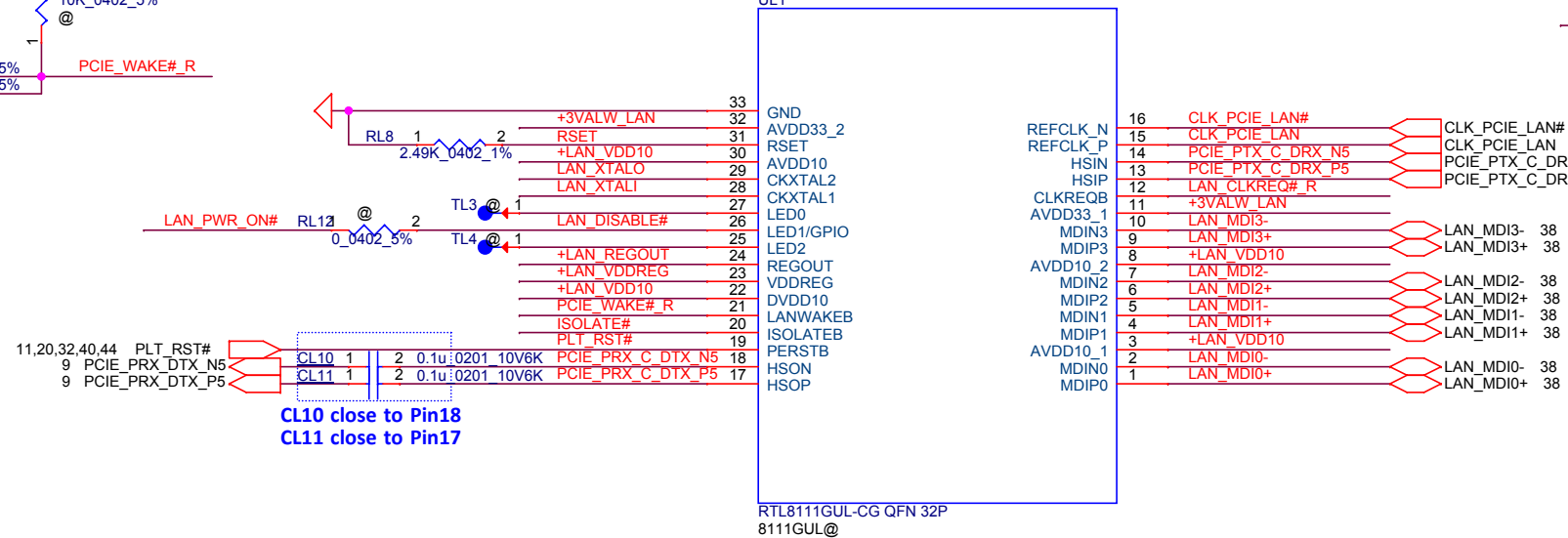
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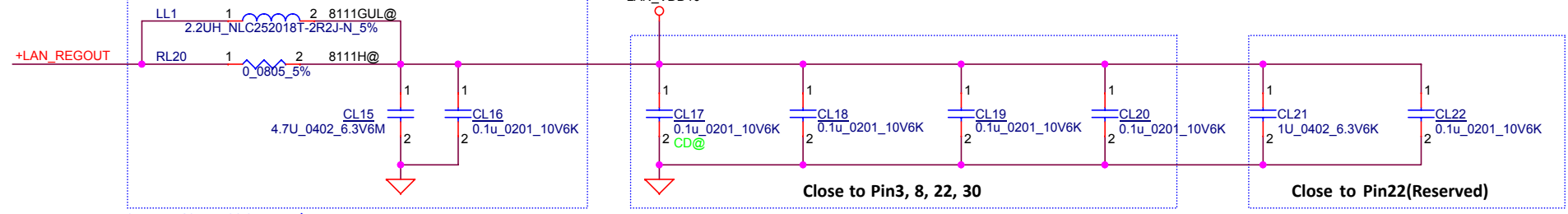
**+3VALW TO +3VALW\_LAN**



**manual change the Codec PN to RTL8111GUL-CG**



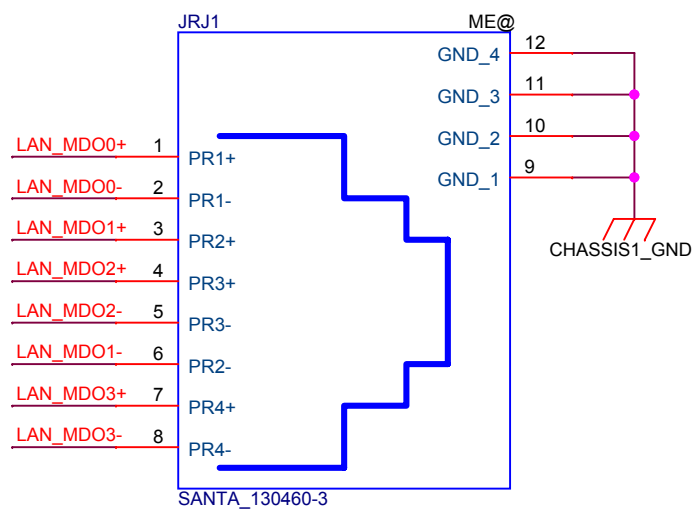
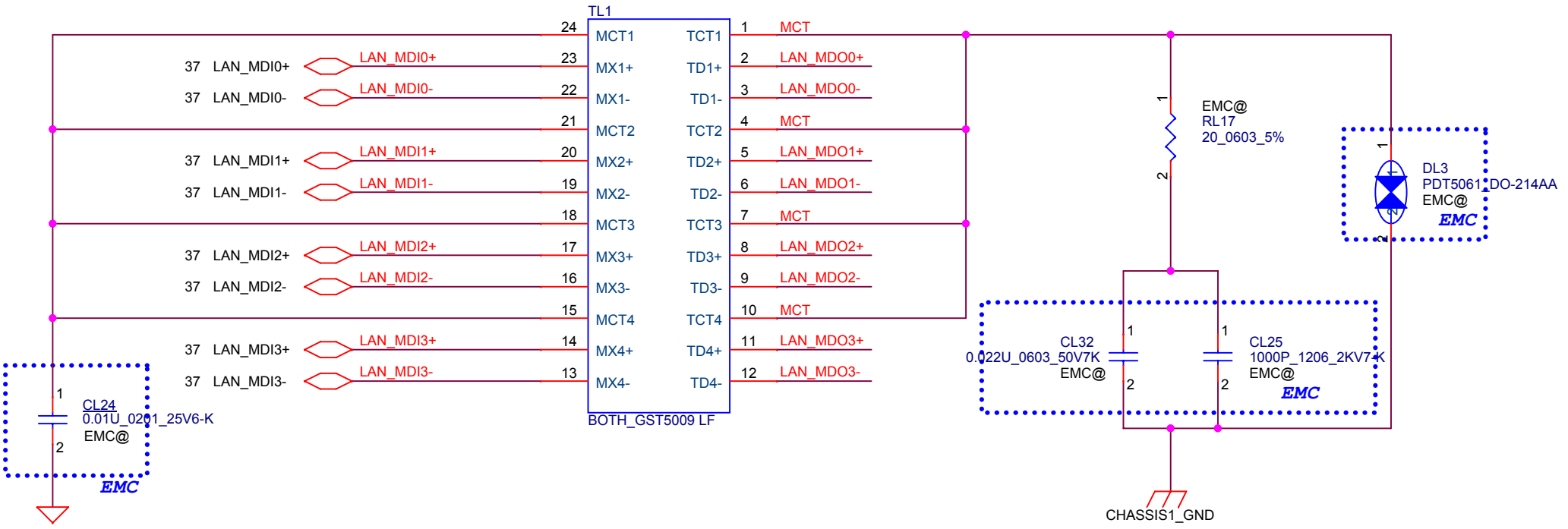
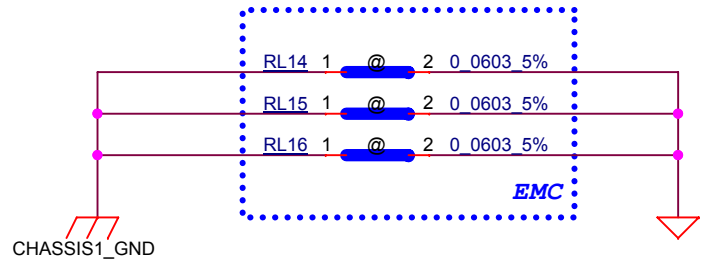
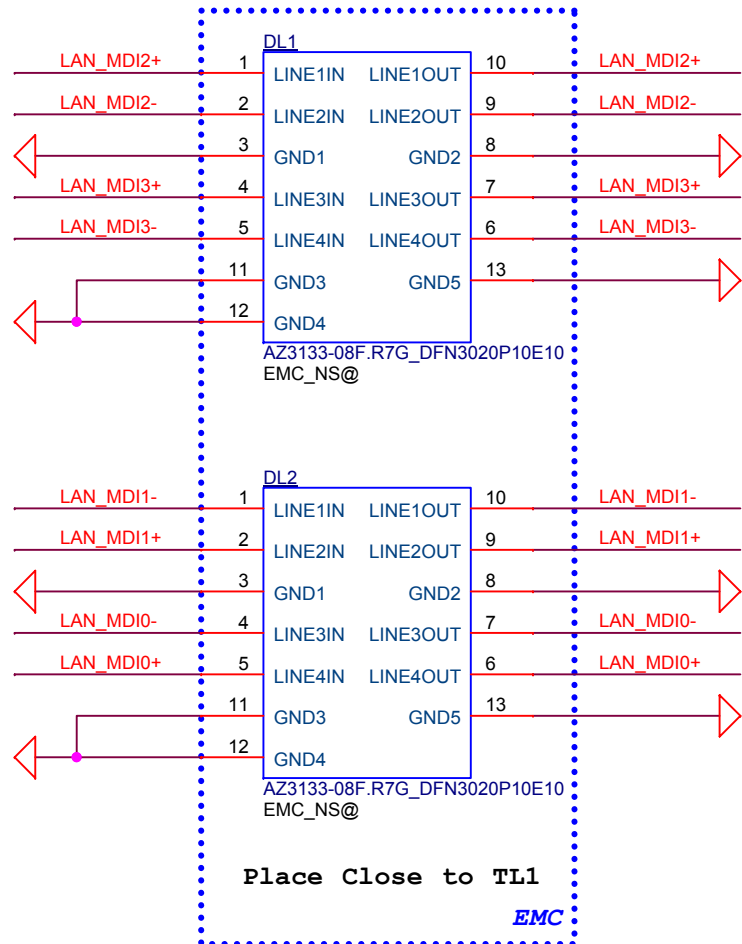
**For RTL8111GUL(SWR mode, reserved)**  
**For RTL8111H (LDO mode)**




Layout Note: LL1 must be within 200mil to Pin24,  
 CL15,CL16 must be within 200mil to LL1  
 +LAN\_REGOUT: Width =60mil

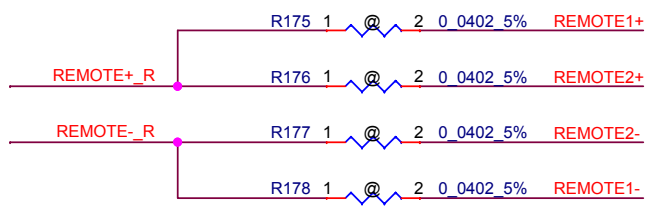
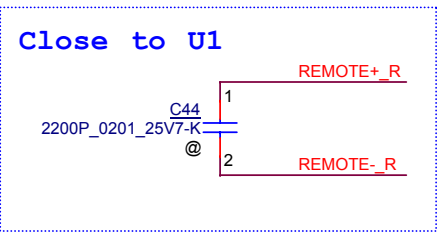
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	
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				Rev 1.0
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DL1/DL2  
1'S PN:SC300003M00

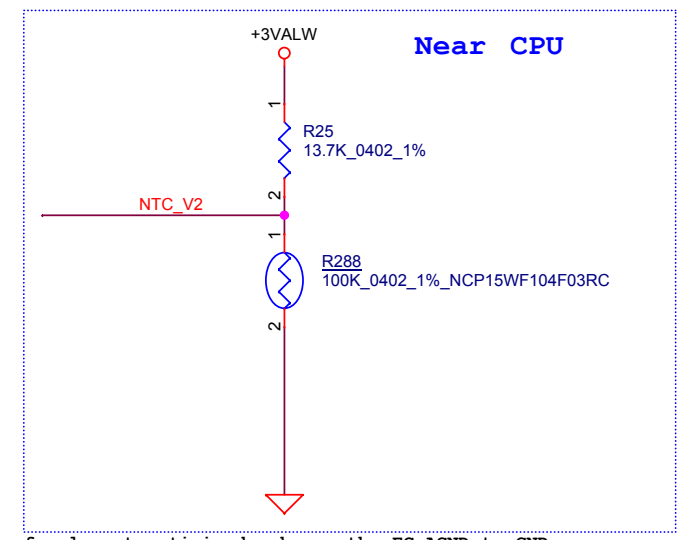
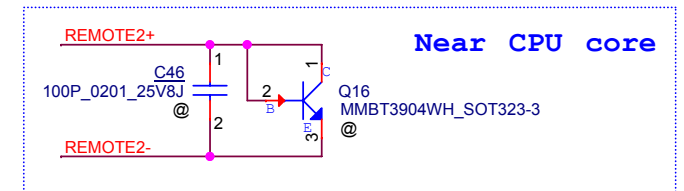
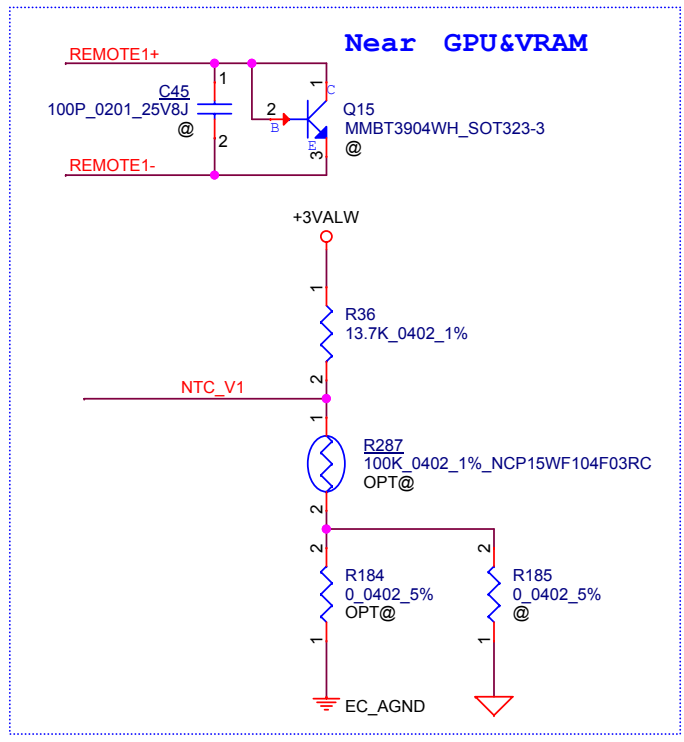


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Size	Document Number		Rev	
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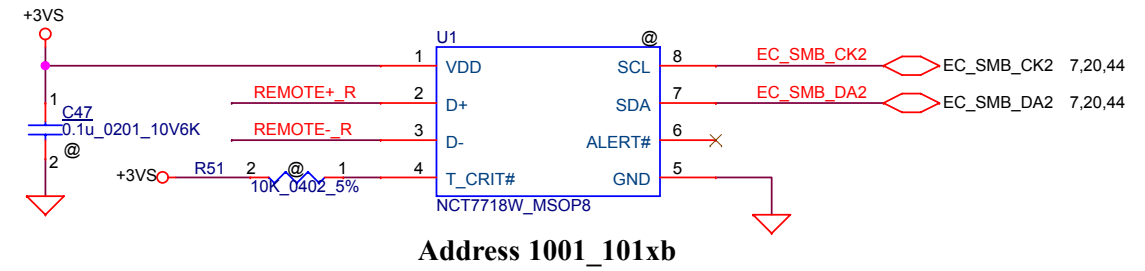




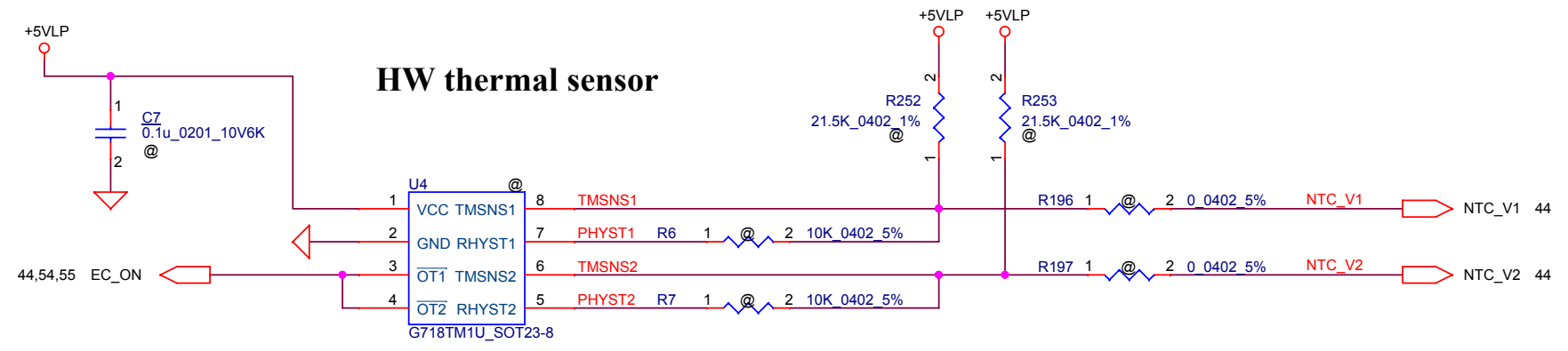
REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



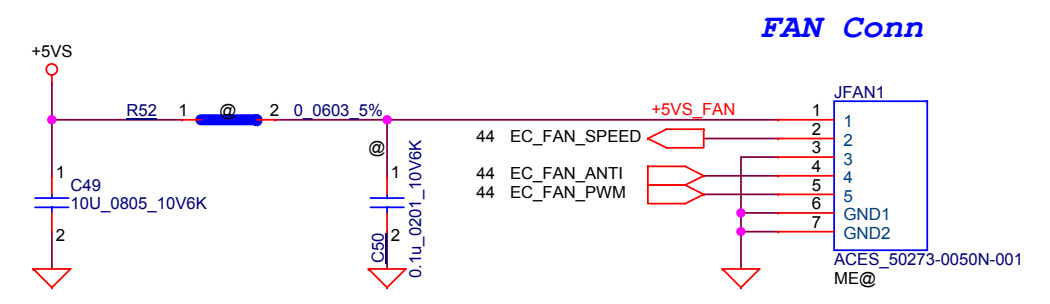
**SMSC thermal sensor placed near DIMM**



**HW thermal sensor**

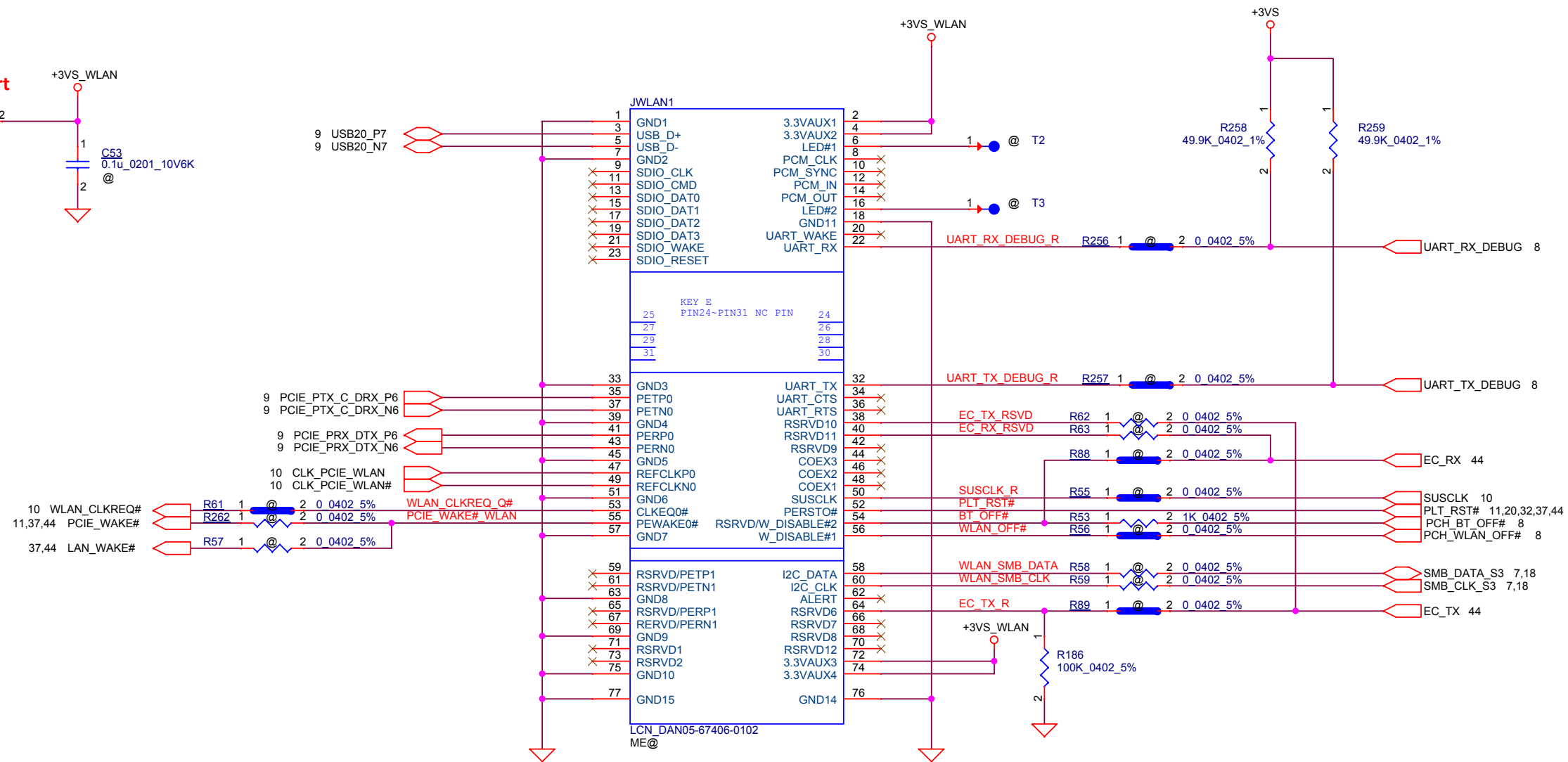



over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C



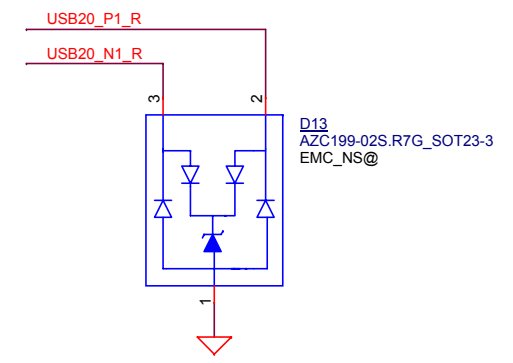
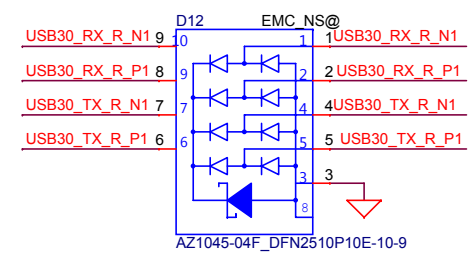
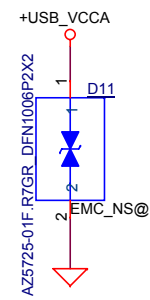
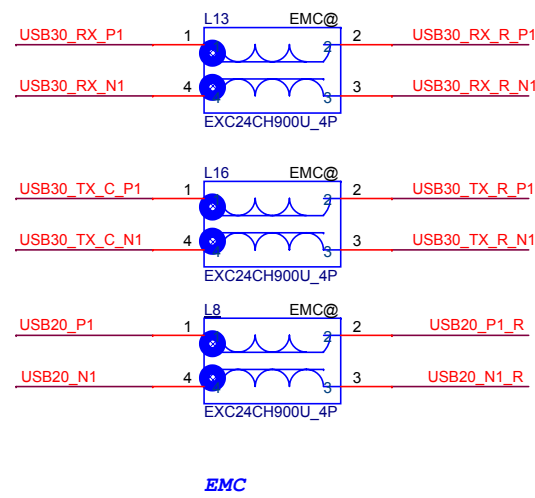
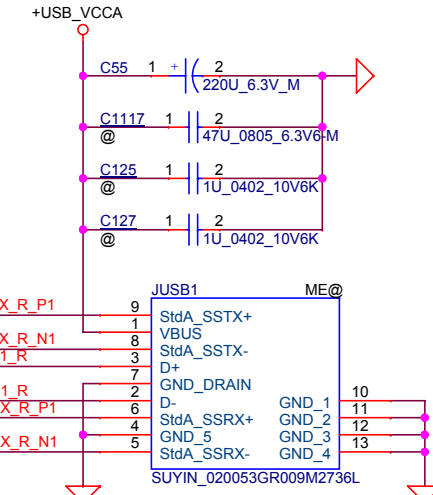
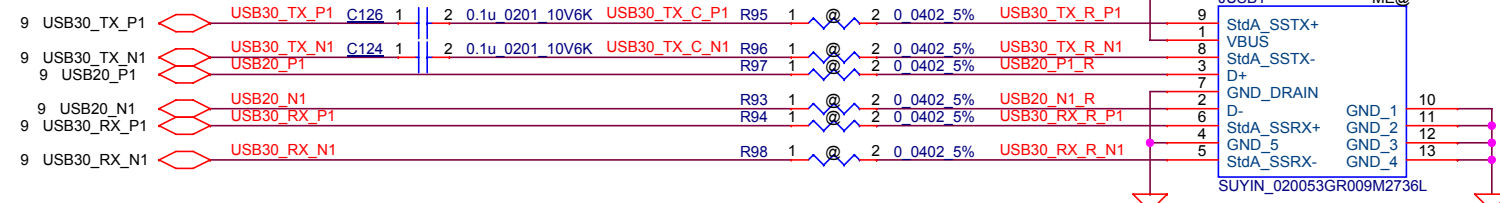
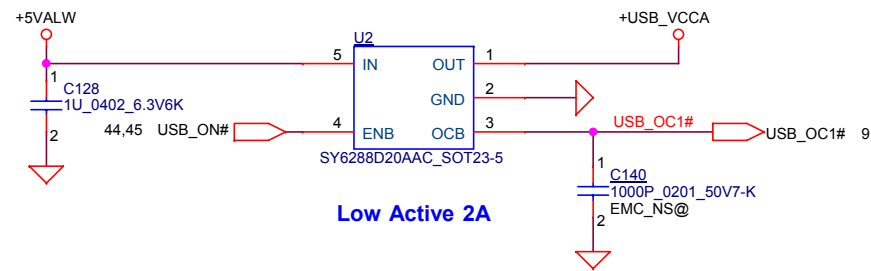
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	<b>Thermal sensor/FAN CONN</b>	
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# Mini-Express Card(WLAN/WiMAX)



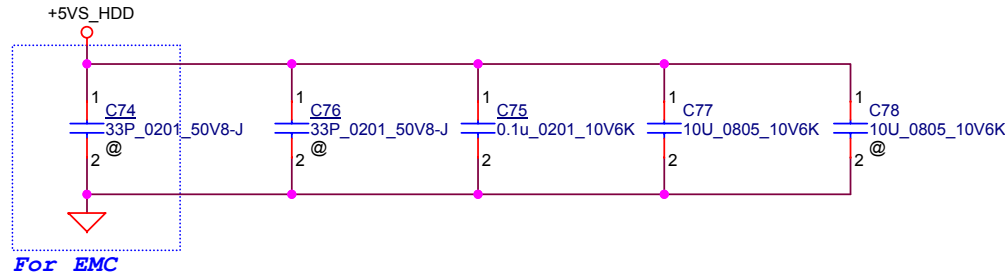
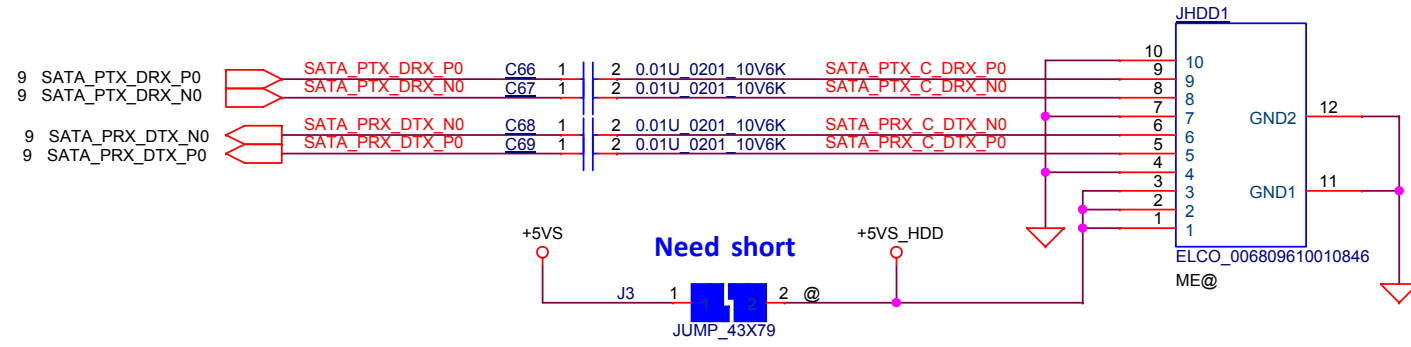
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# LEFT SIDE USB3.0 PORT x1

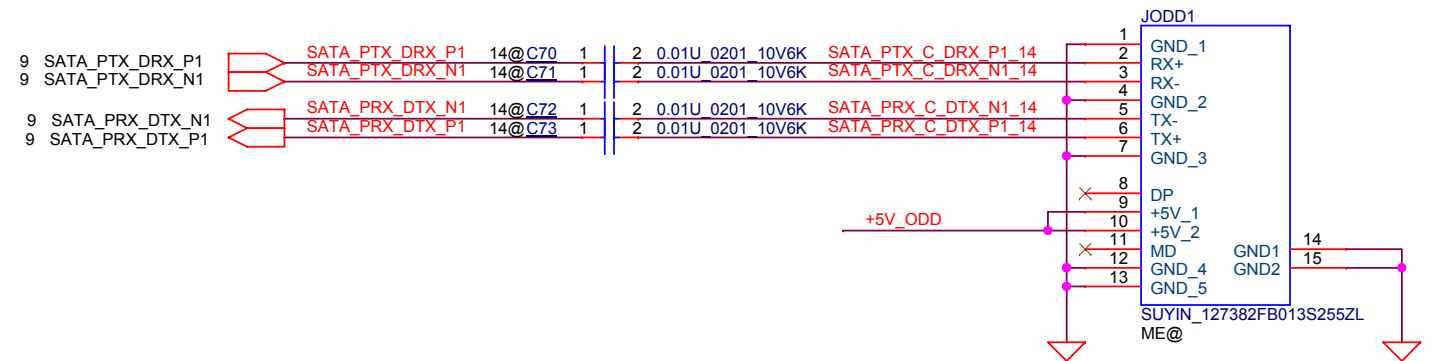


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Issued Date	2015/08/20	Deciphered Date	2016/08/20	USB3.0 PORT (LEFT)	
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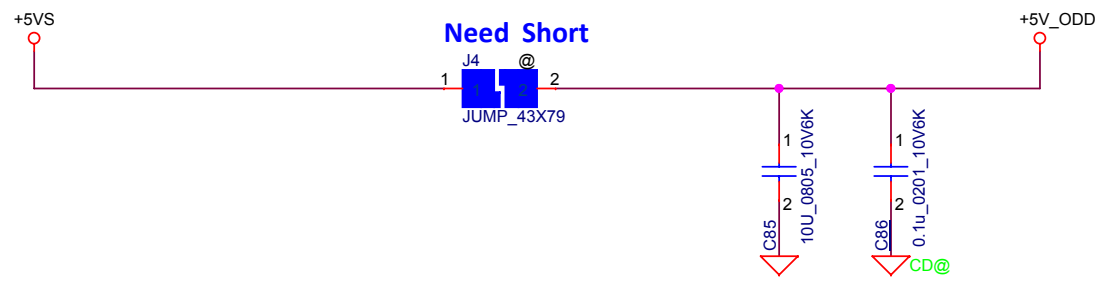
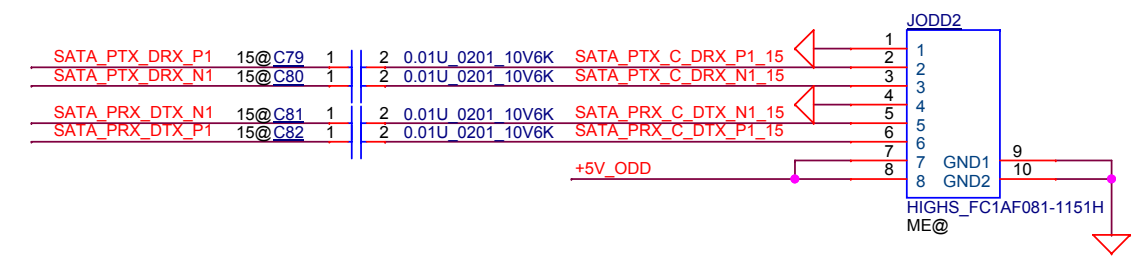
### SATA HDD Conn.




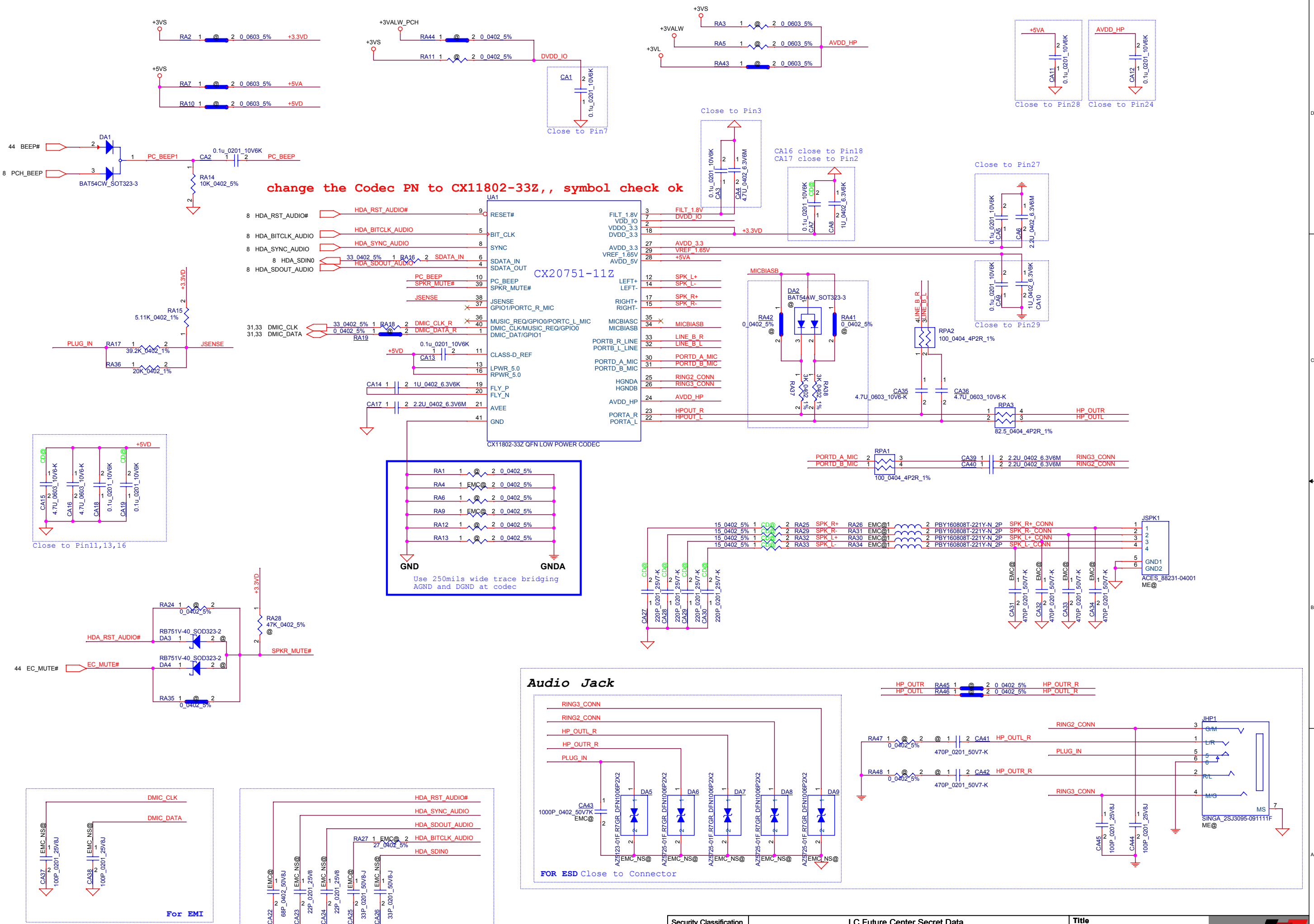
### FOR 14" SATA ODD Conn.



### FOR 15" SATA ODD FFC Conn



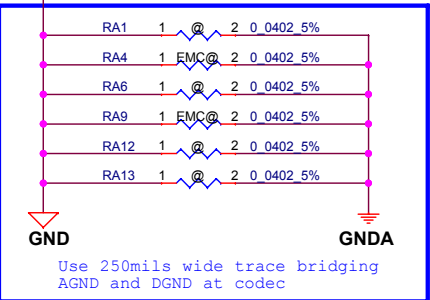
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change the Codec PN to CX11802-33Z,, symbol check ok

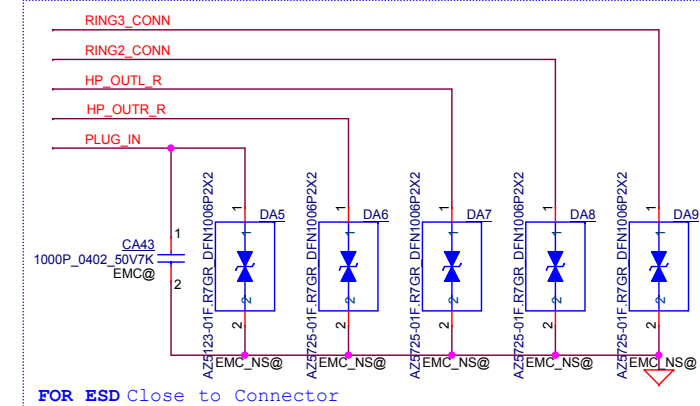
CX20751-11Z

CX11802-33Z QFN LOW POWER CODEC



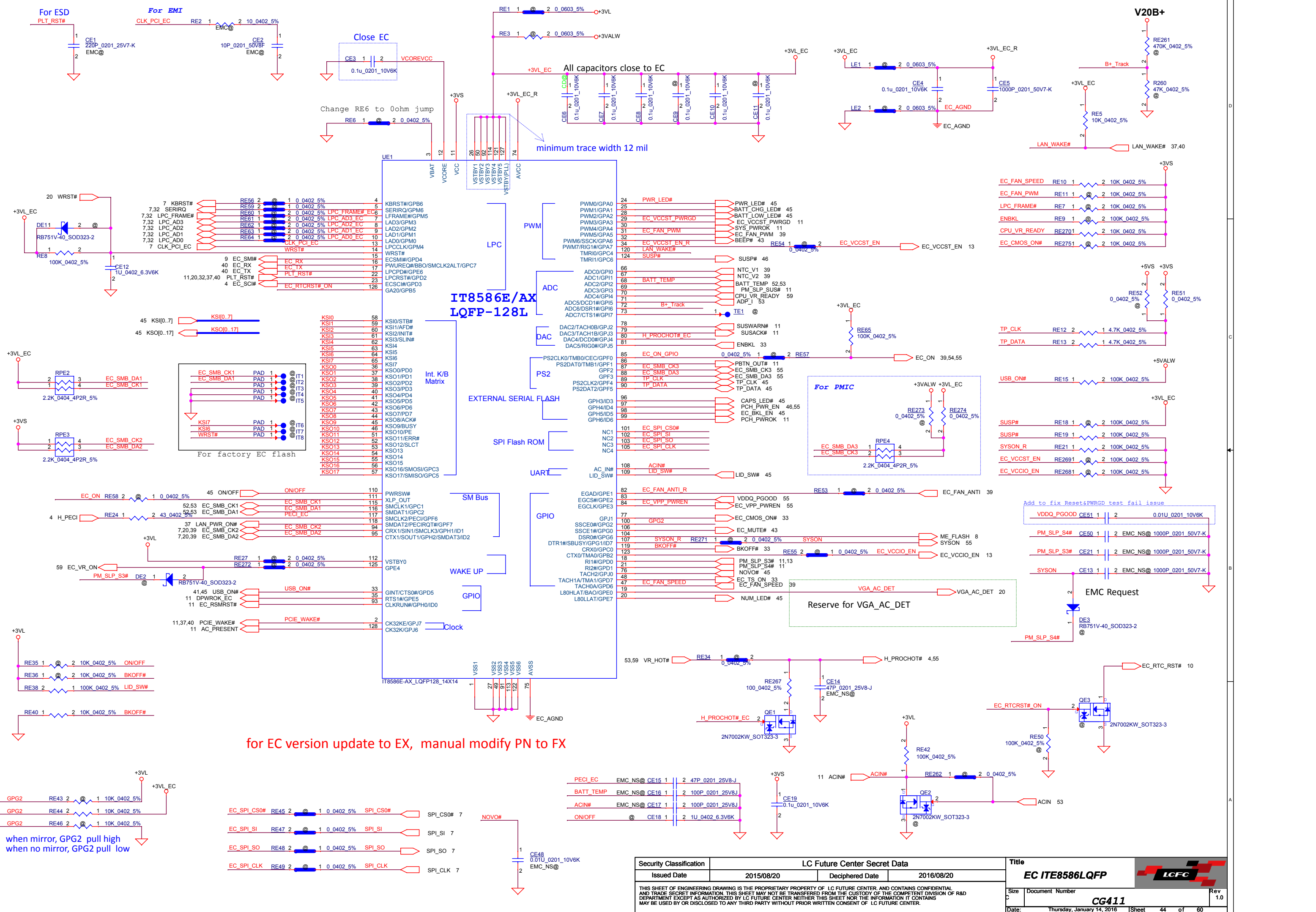
Use 250mils wide trace bridging AGND and DGND at codec

Audio Jack



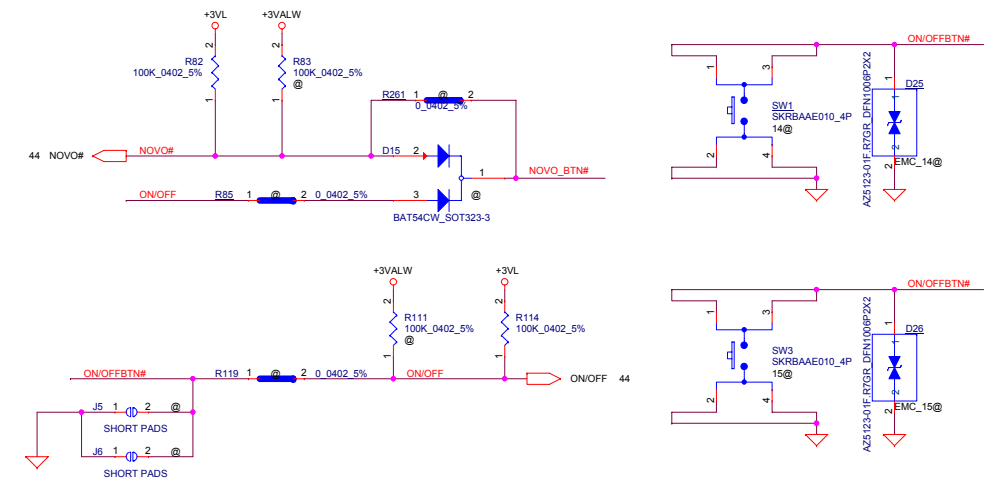
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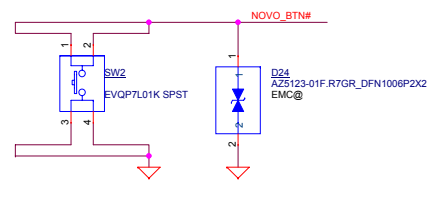


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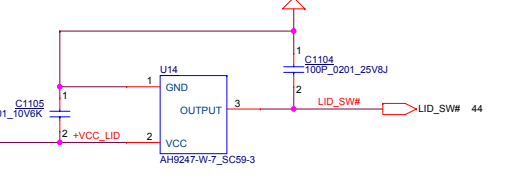
**ON/OFF switch**



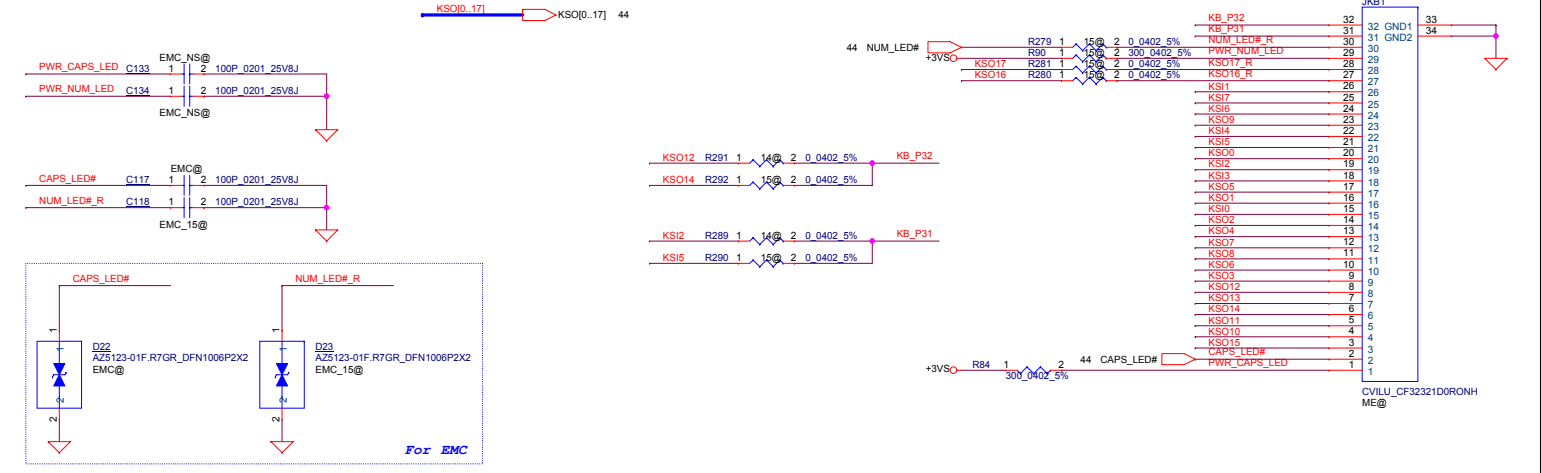
**Novo button**



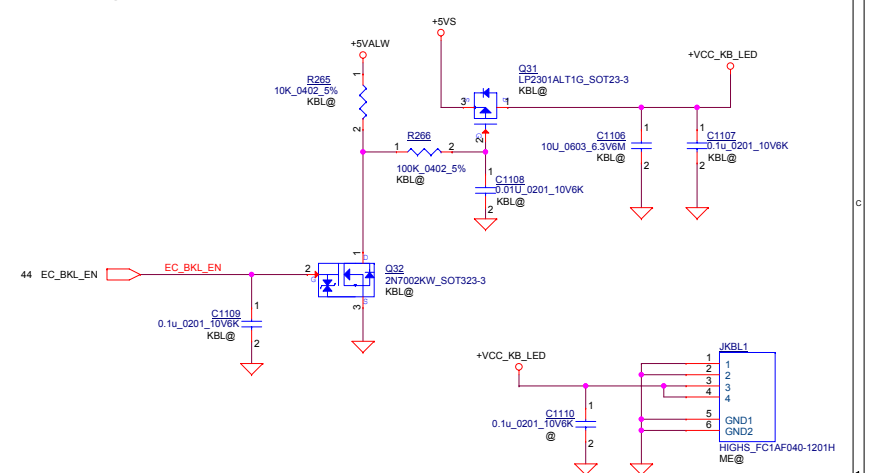
**LID switch**



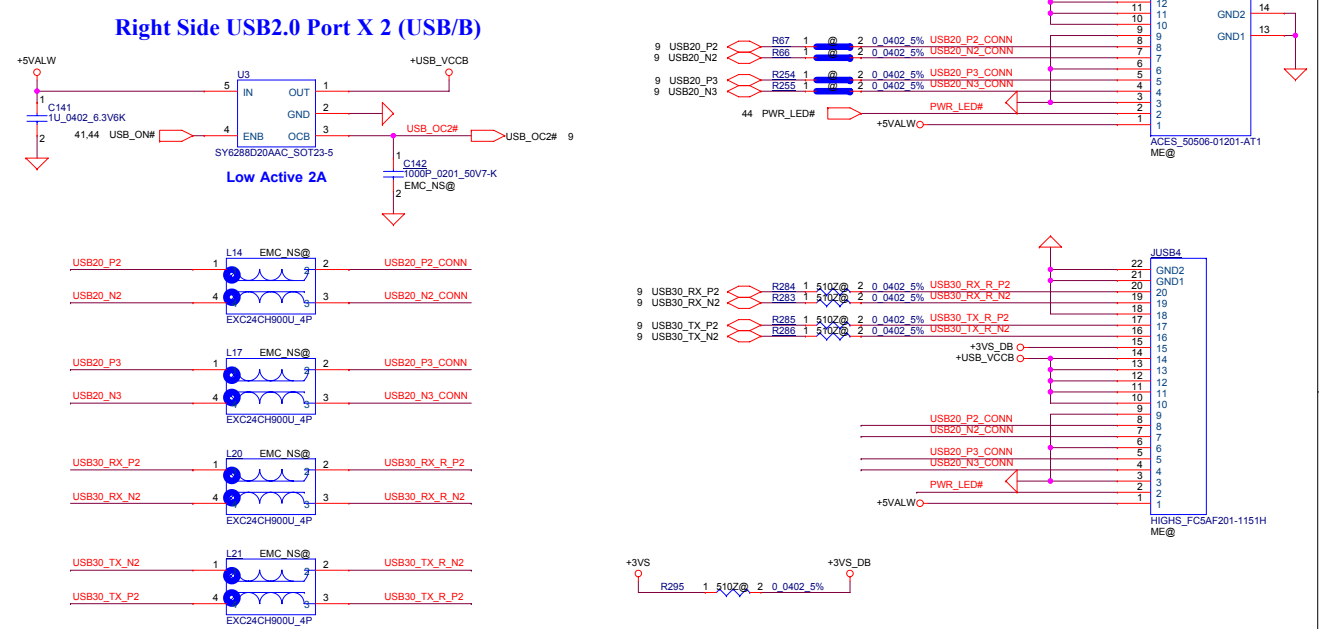
**K/B Connector**



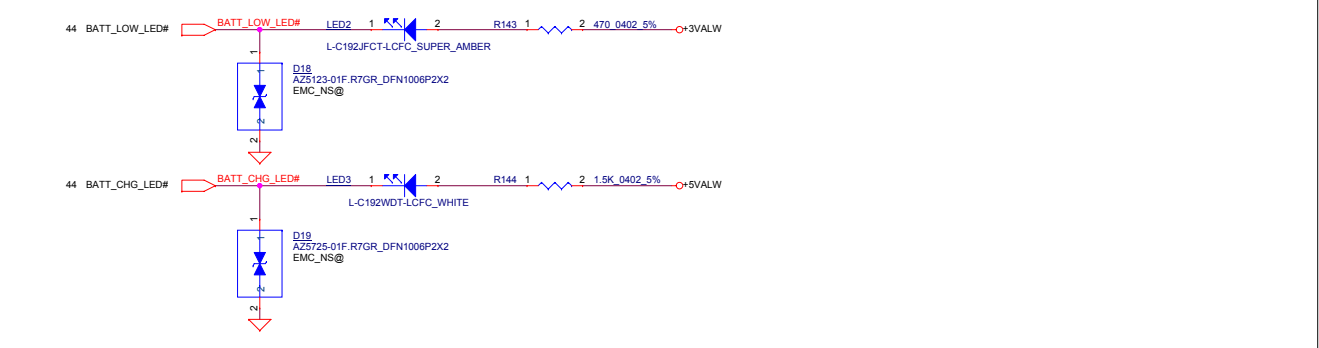
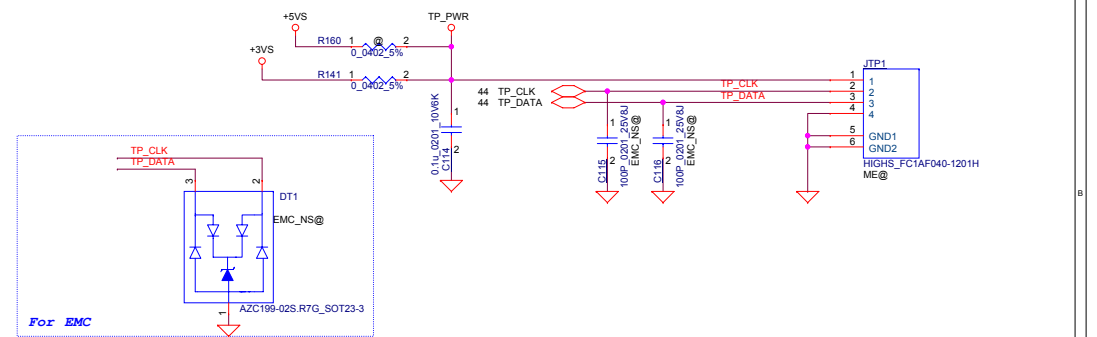
**KB Backlight Connector**



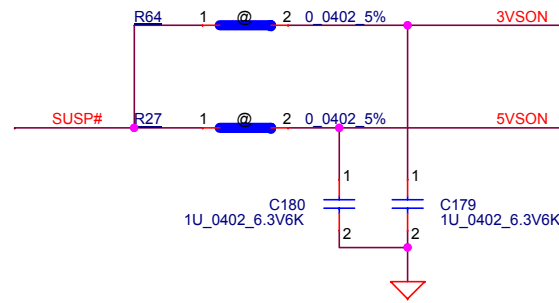
**USB DB Connector**



**TP/B Connector**

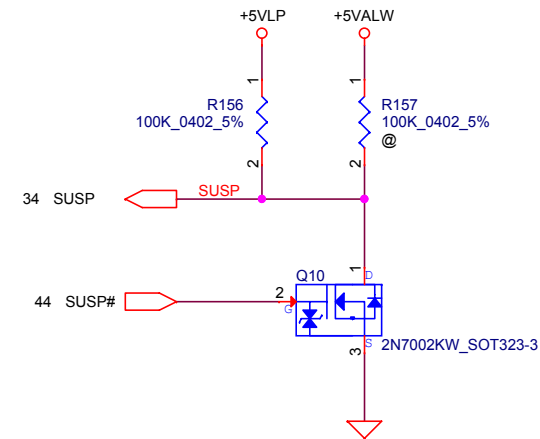
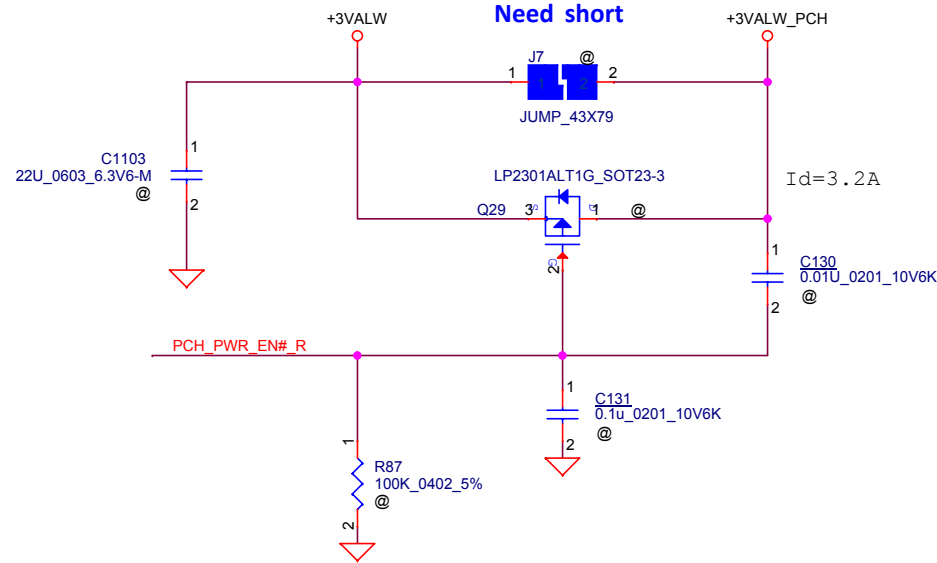
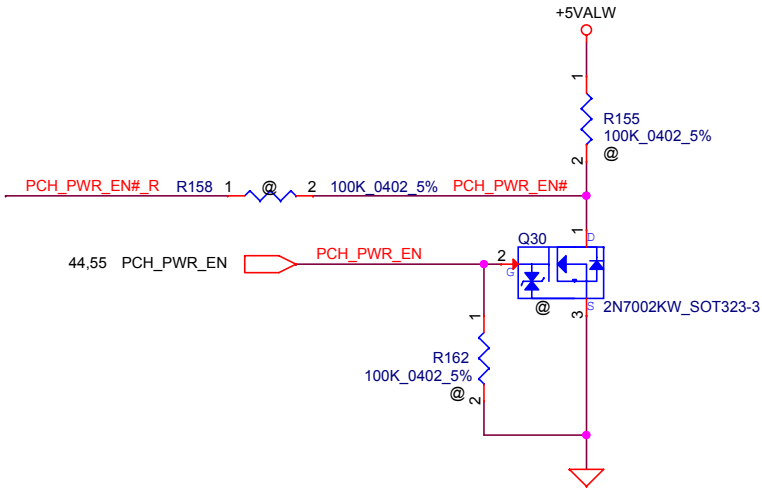
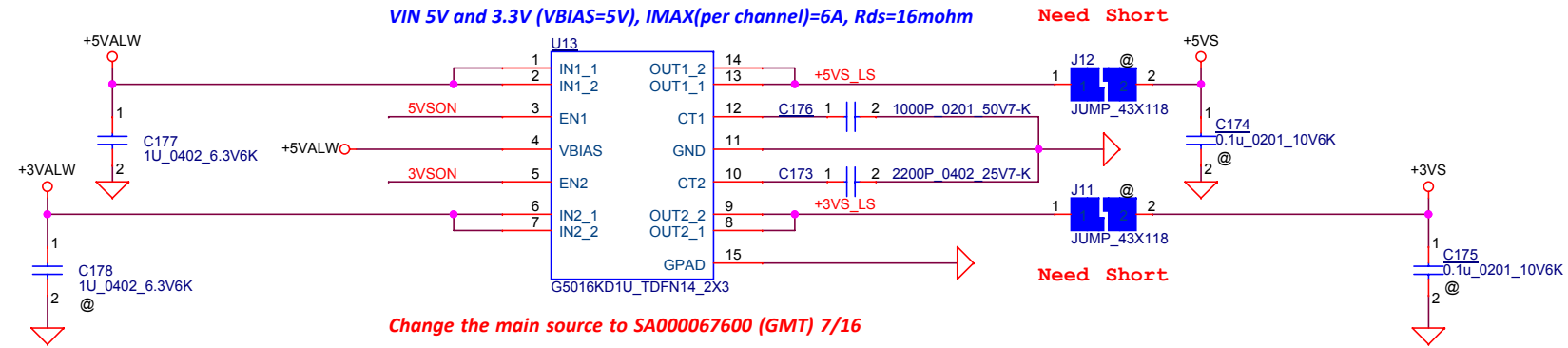


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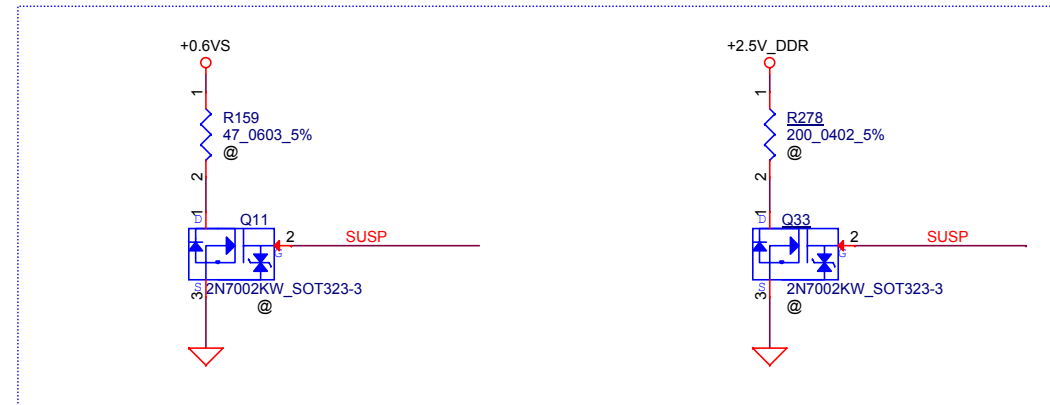


**Load Switch**  
**+5VALW To +5VS**  
**+3VALW To +3VS**

**+3VS, C173 --> 2.74ms**  
**+5VS, C176 --> 2.03ms**

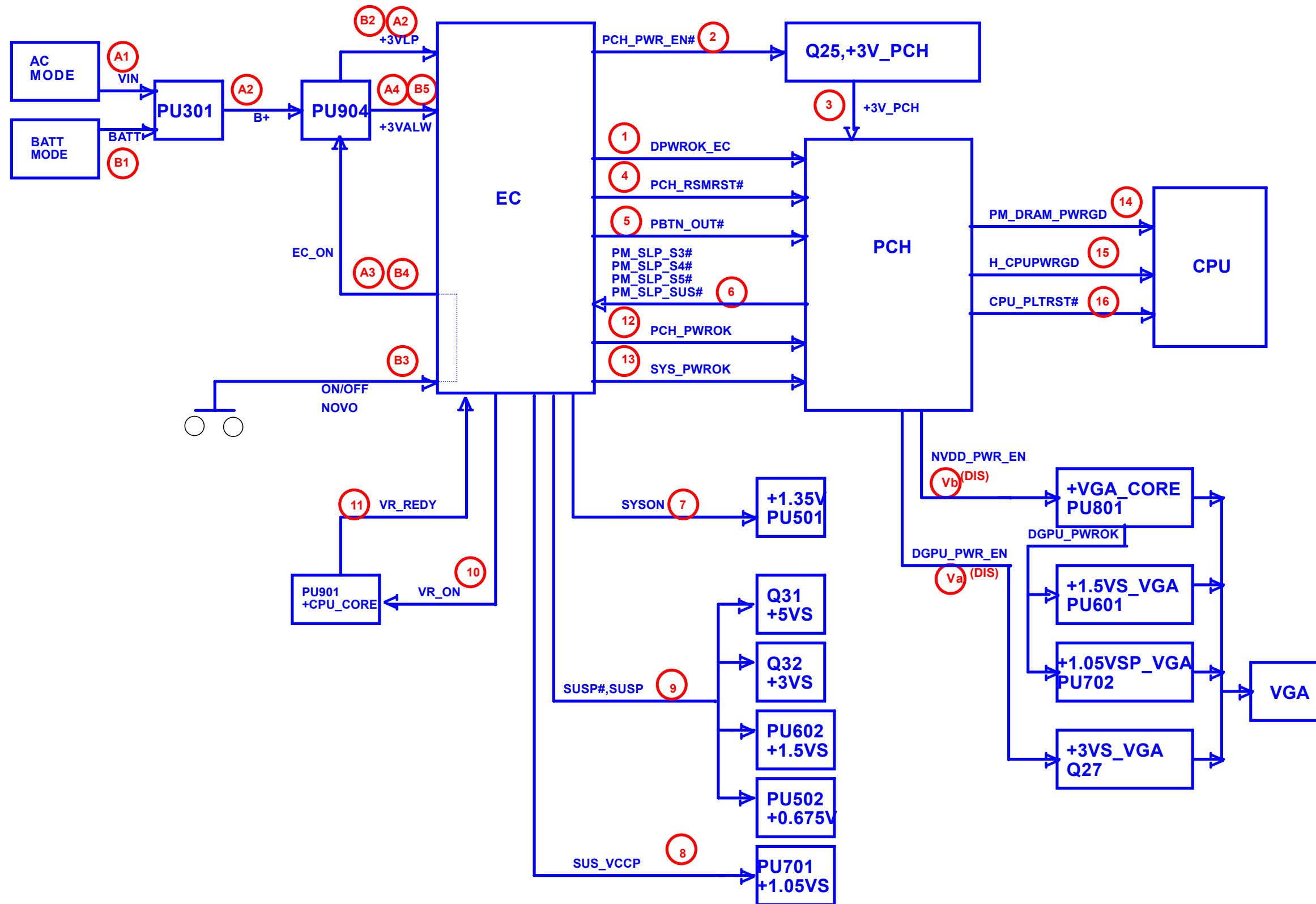



**For DisCharge**




08/29: Need double check enable signal and the resistance

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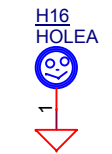
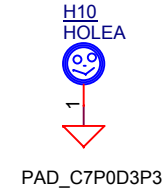
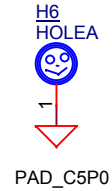
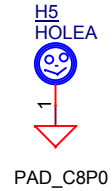
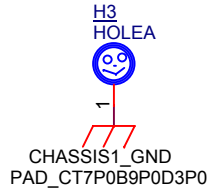
2

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**PCB Fedcal Mark PAD**



PAD\_O2P6X2P5D2P6X2P5N PAD\_O2P5X3P0D2P5X3P0N PAD\_O2P5X2P9D2P5X2P9N



PAD\_CT7P0B9P0D3P0 pad\_ct6p0b7p0d4p0 pad\_ct6p0b7p0d4p0 pad\_ct6p0b7p0d4p0 pad\_ct6p0b7p0d4p0 PAD\_ShapeT9P0X8P0CB9P0D3P0 PAD\_ShapeT7P5X8P0D3P4 PAD\_CT7P0B6P0D3P3 PAD\_C3P0D3P0N PAD\_C6P0D2P5

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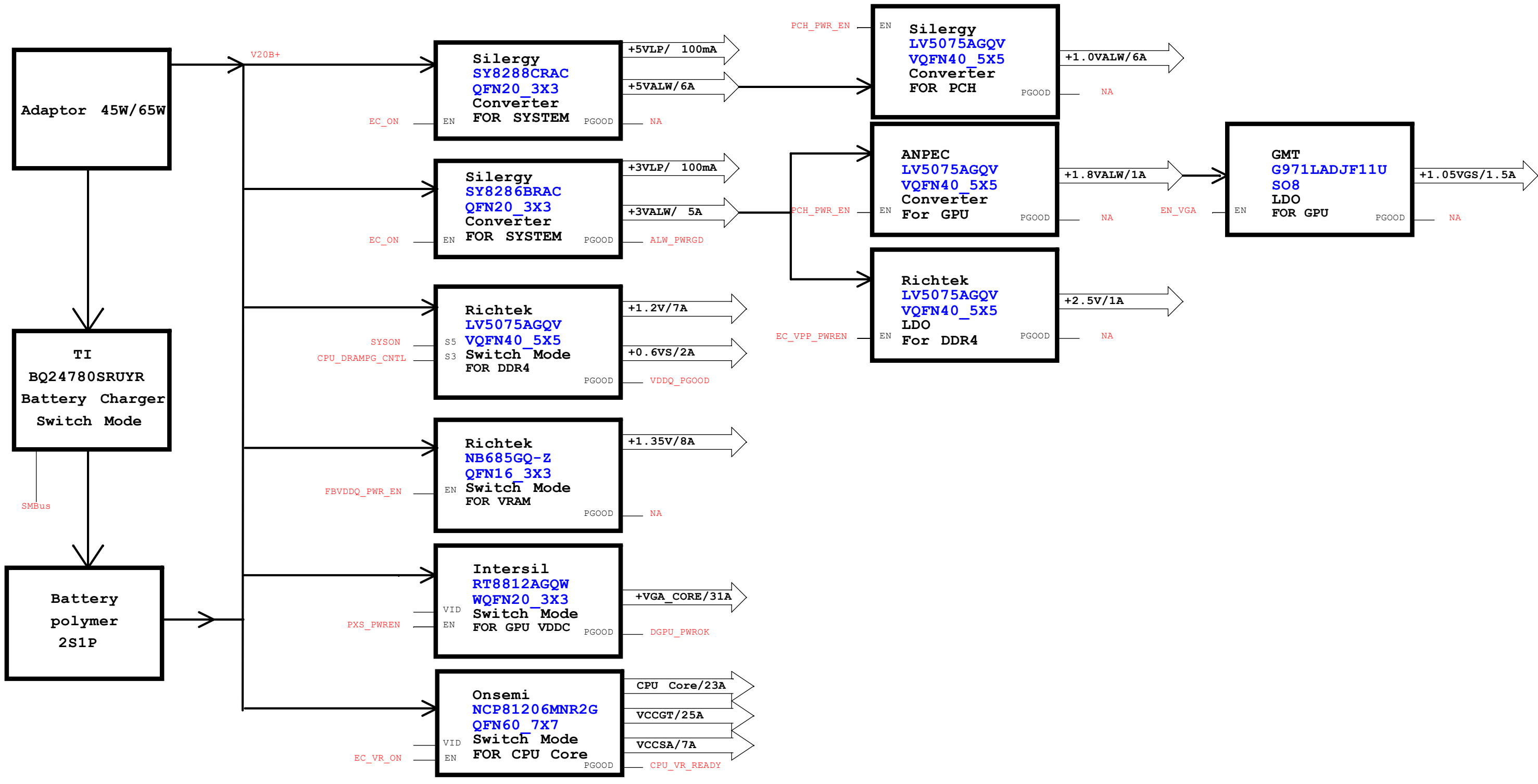
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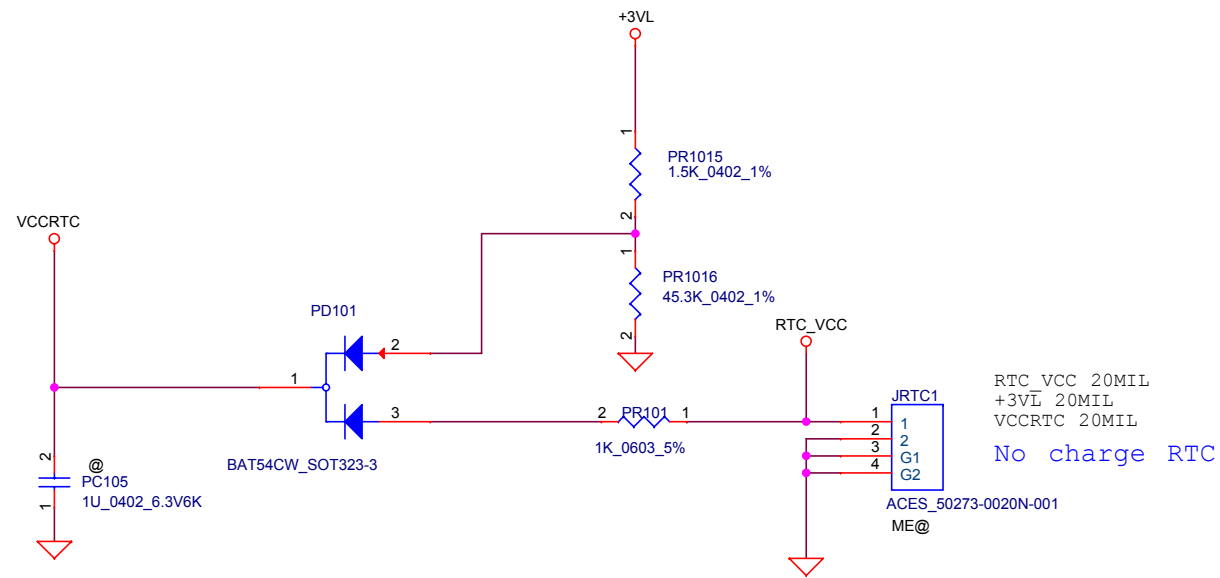
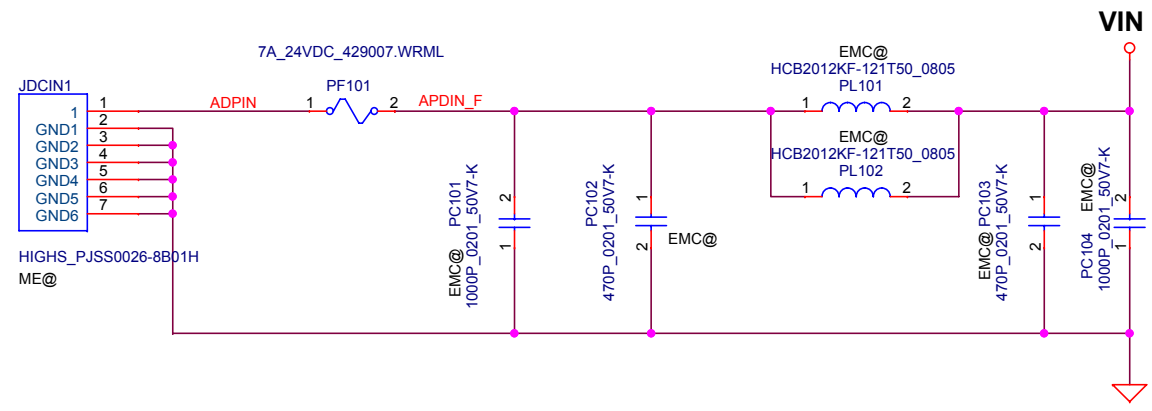





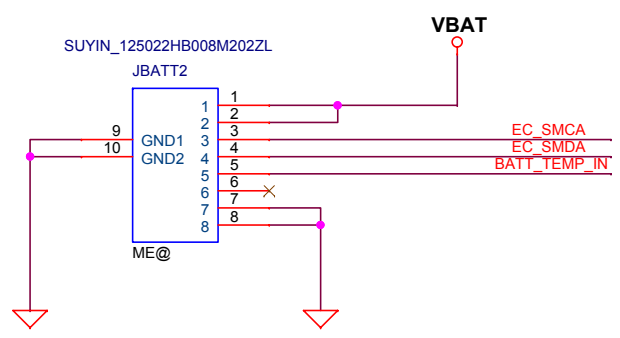
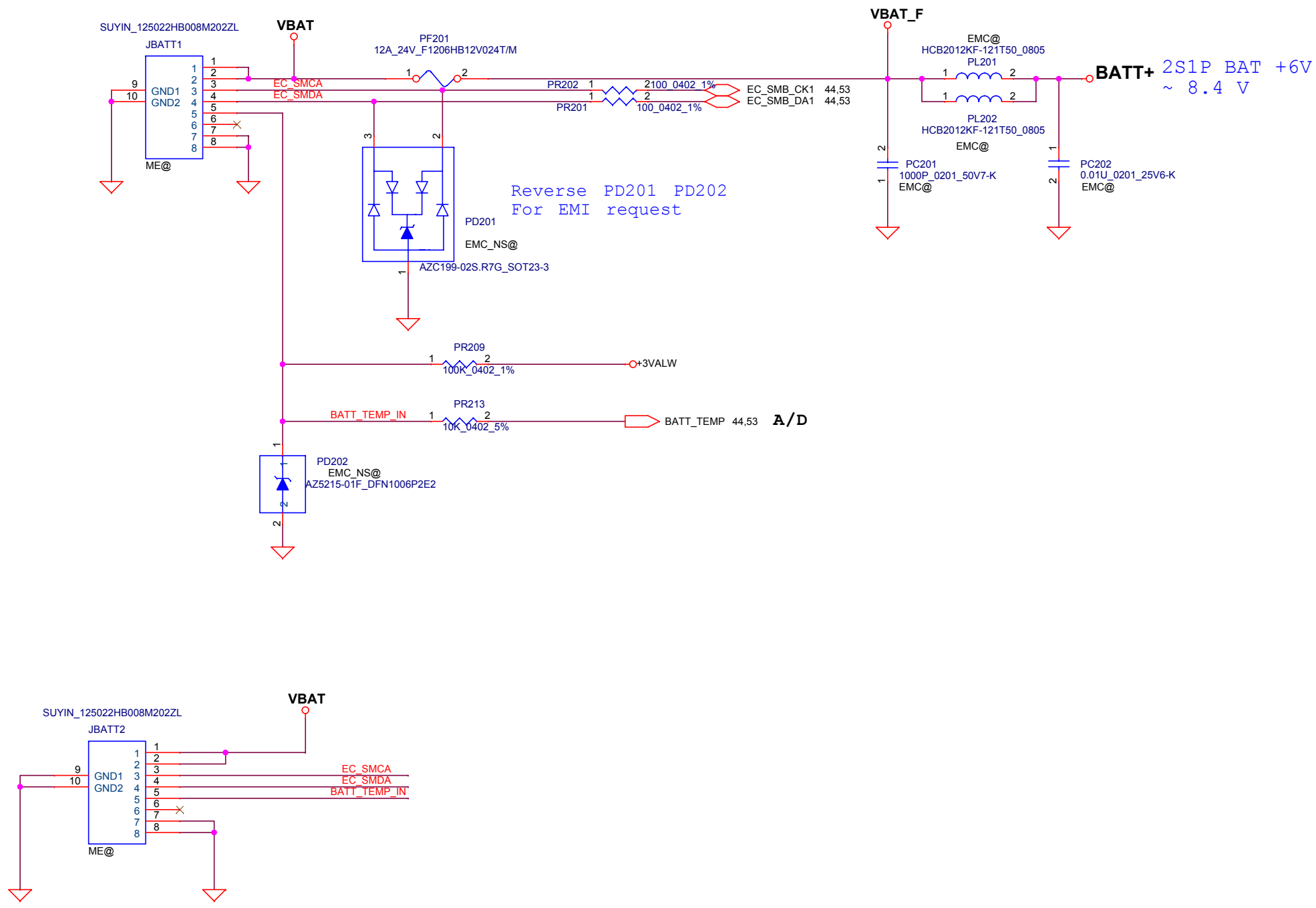
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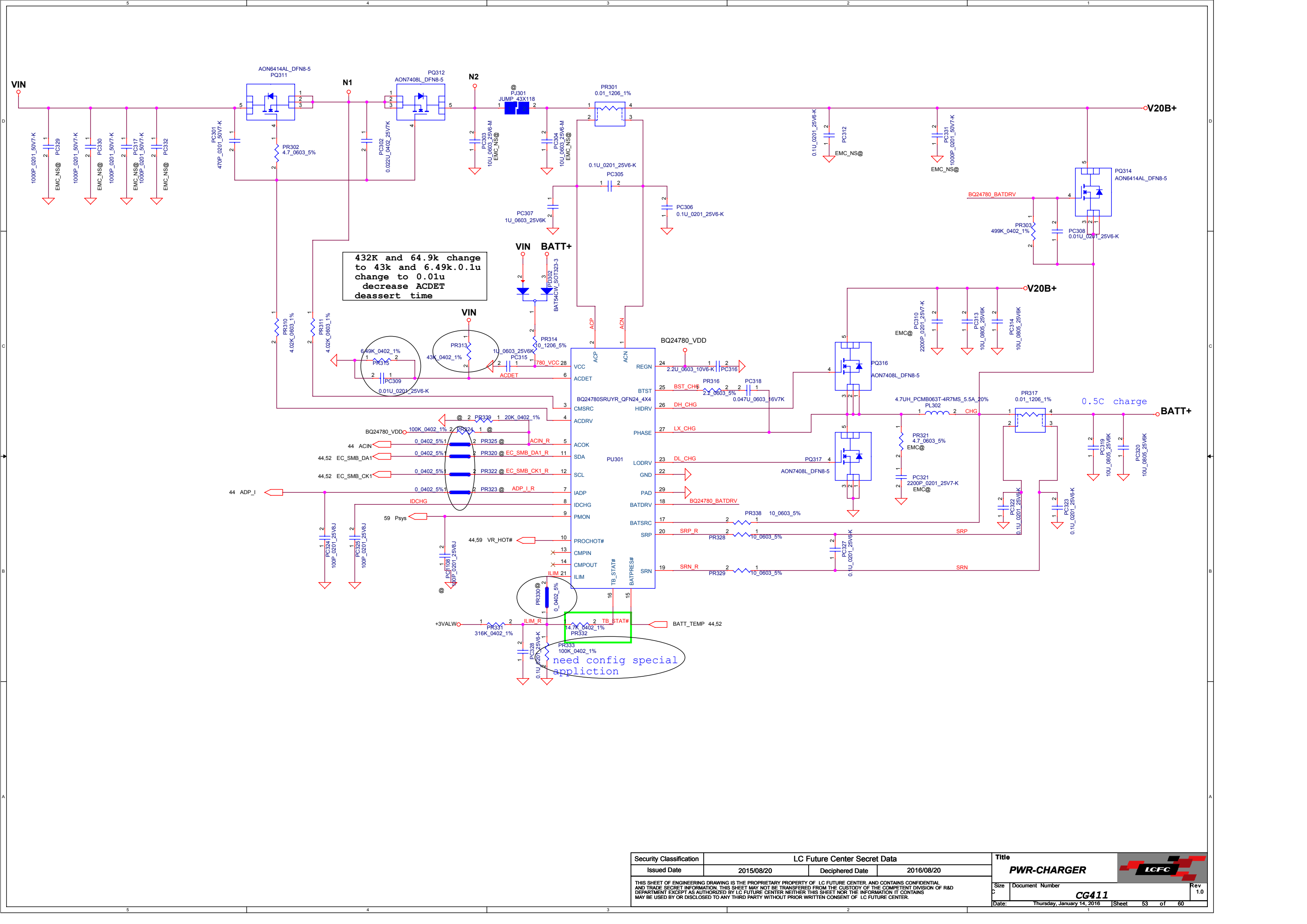
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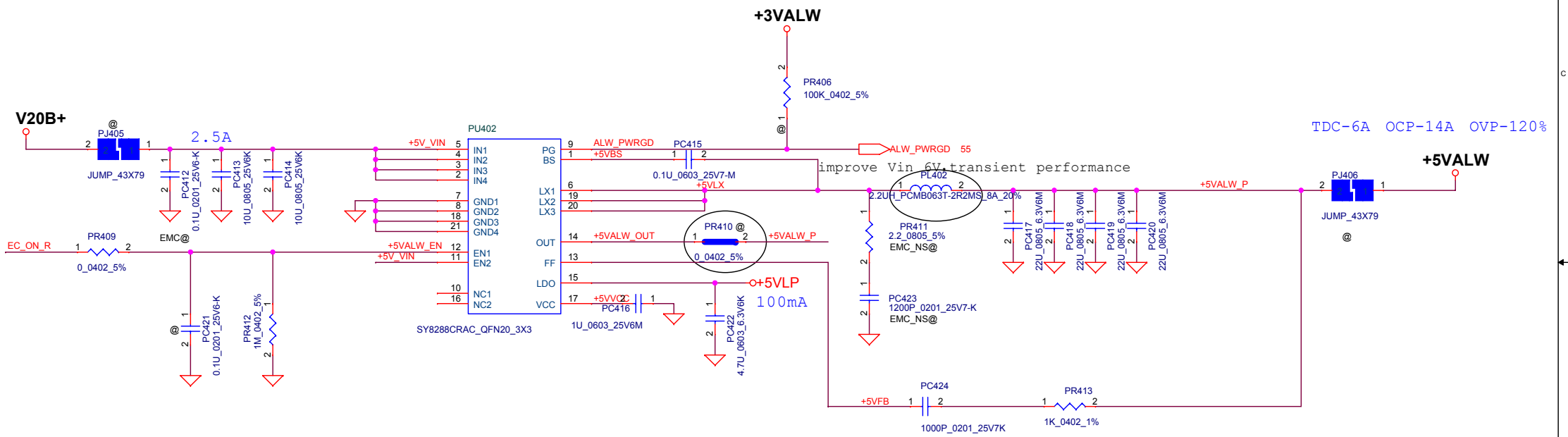
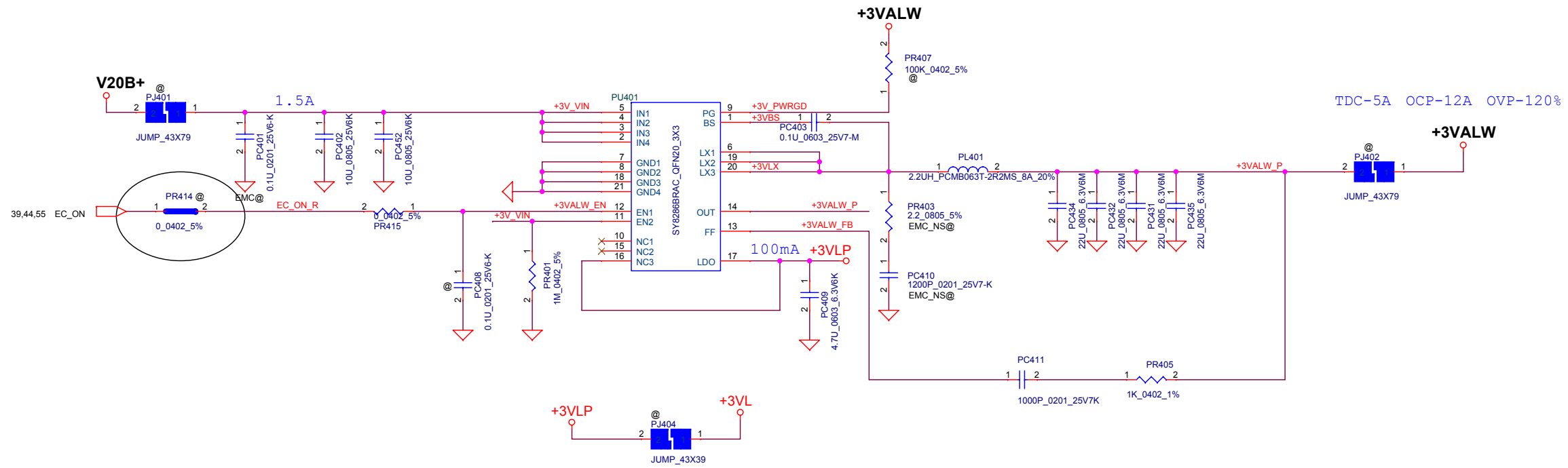
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432K and 64.9k change to 43k and 6.49k. 0.1u change to 0.01u decrease ACDET deassert time

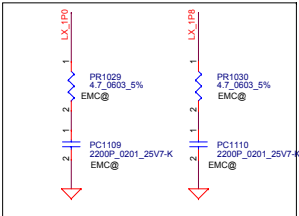
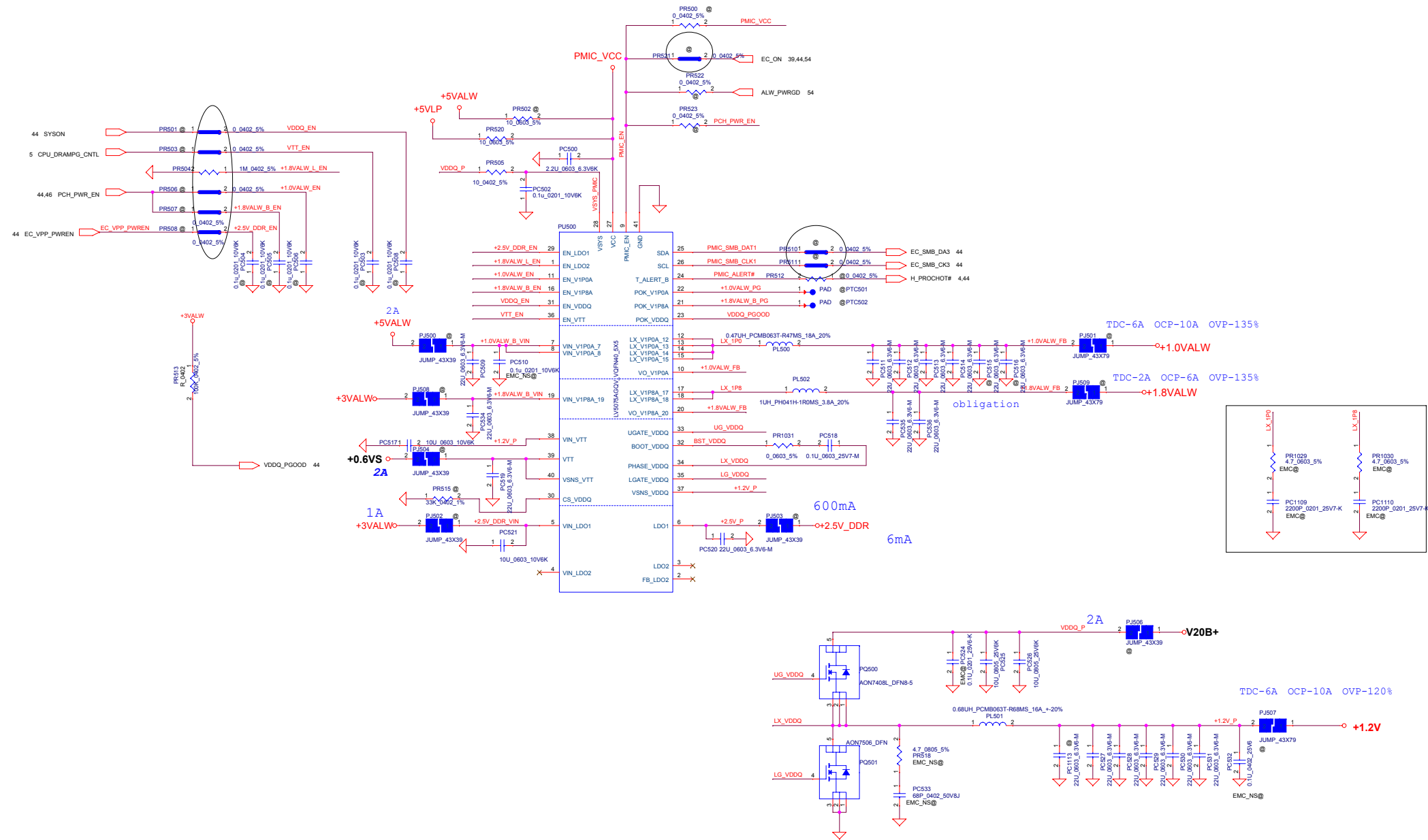
need config special application

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6800pf soft start 2ms  
47nf soft start 7ms

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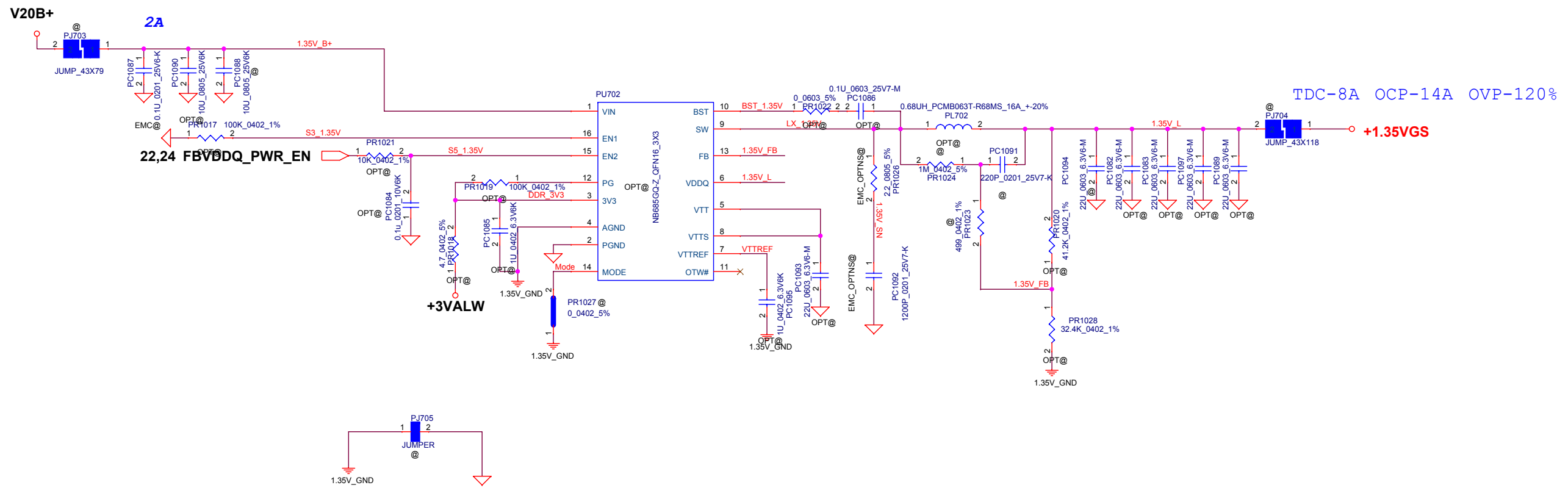
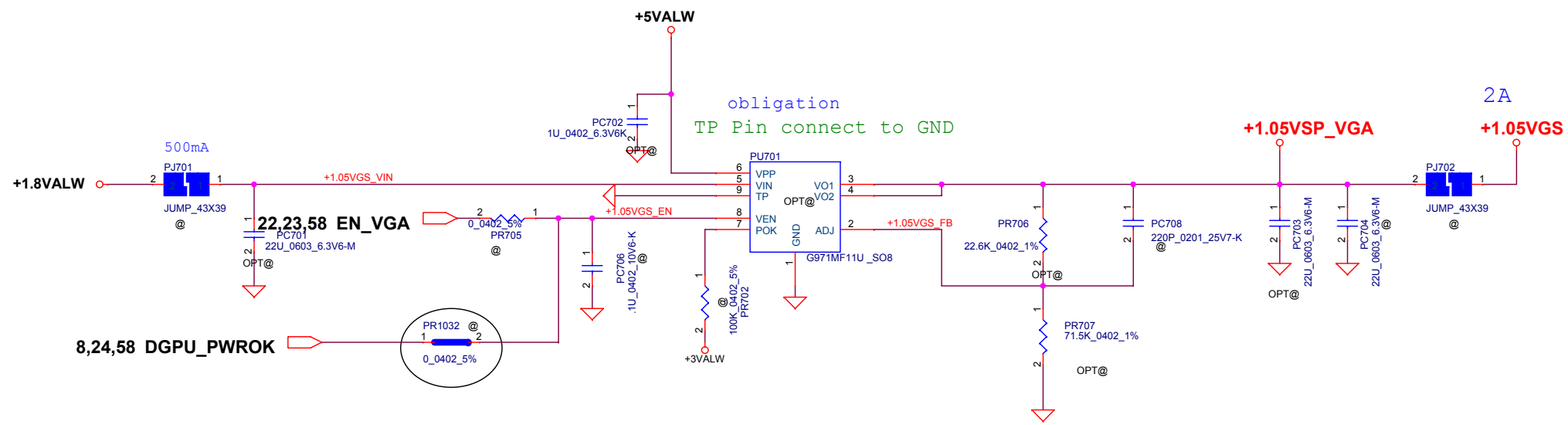
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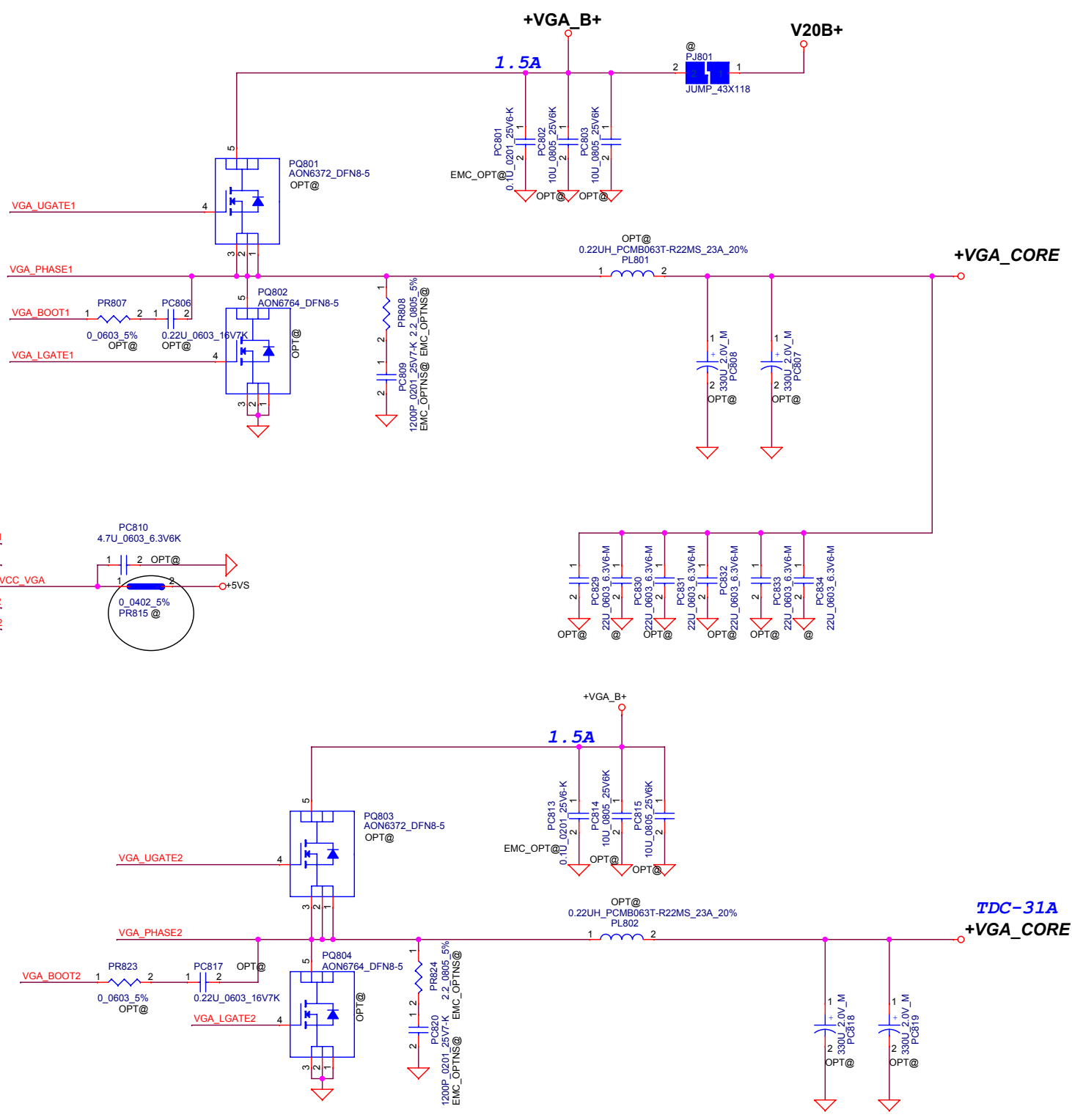
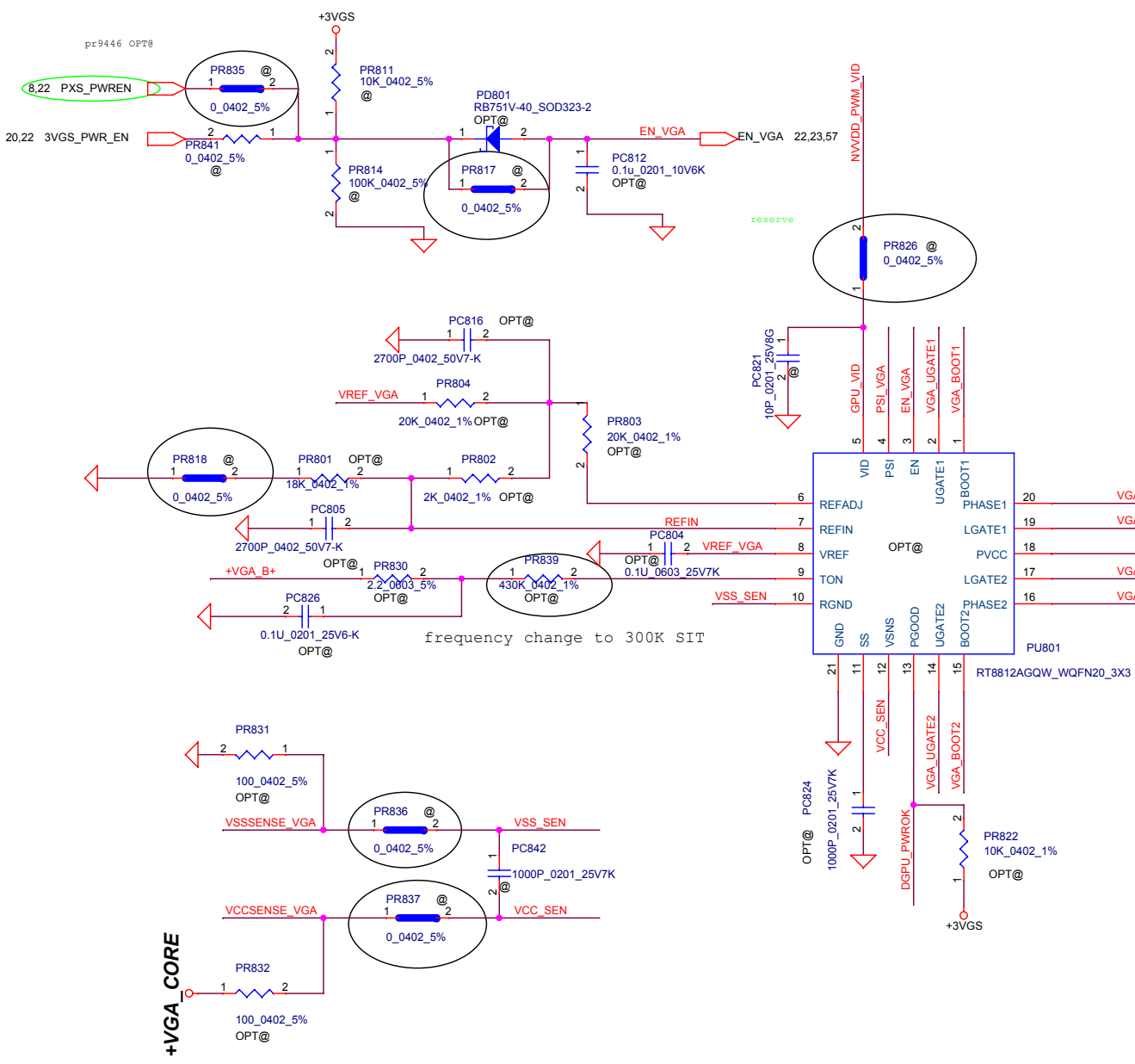
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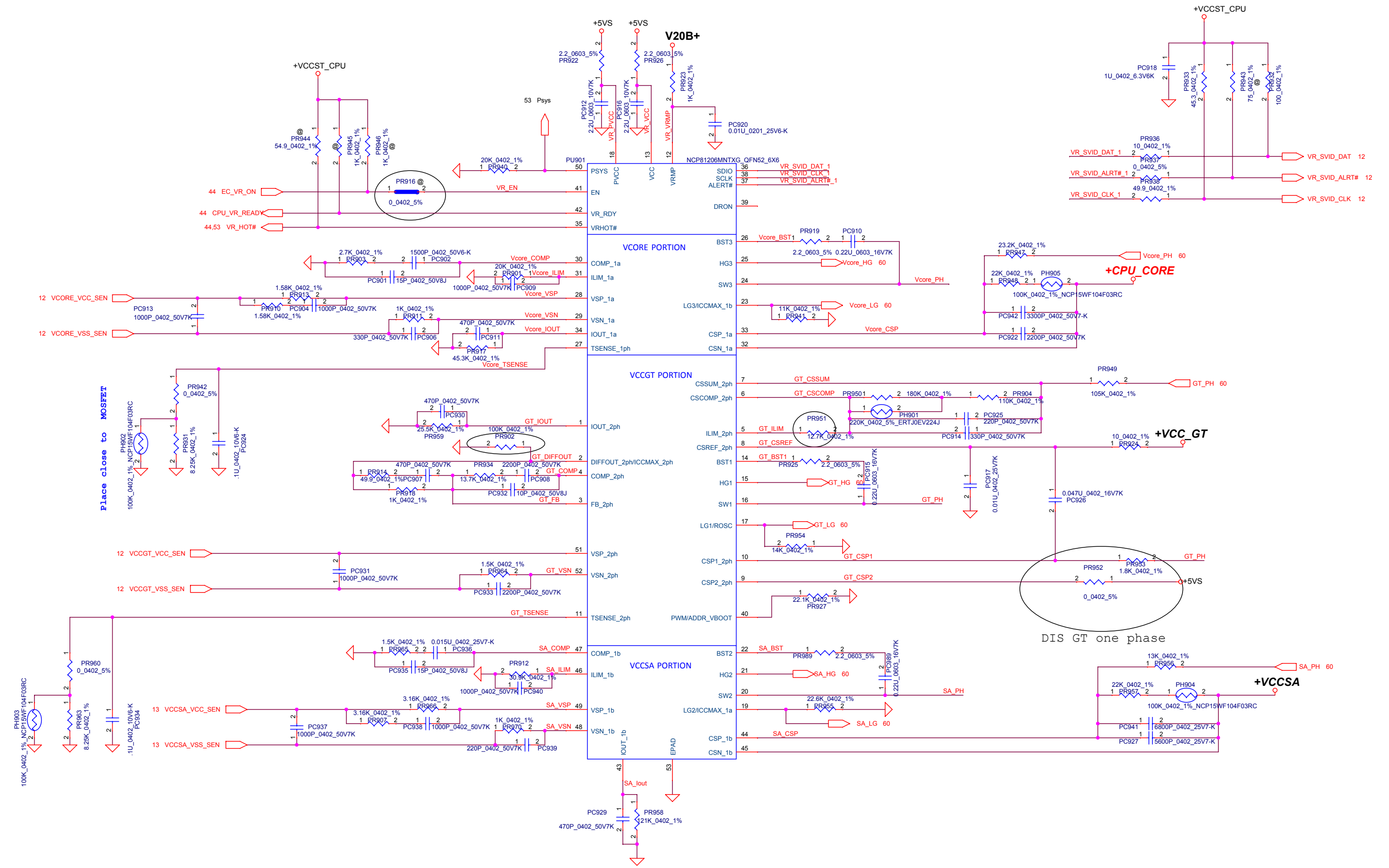


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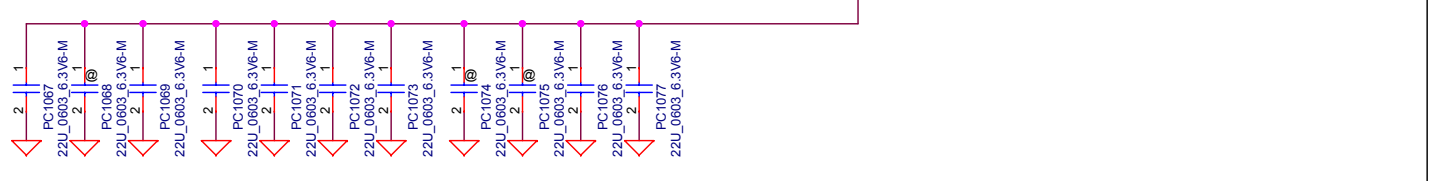
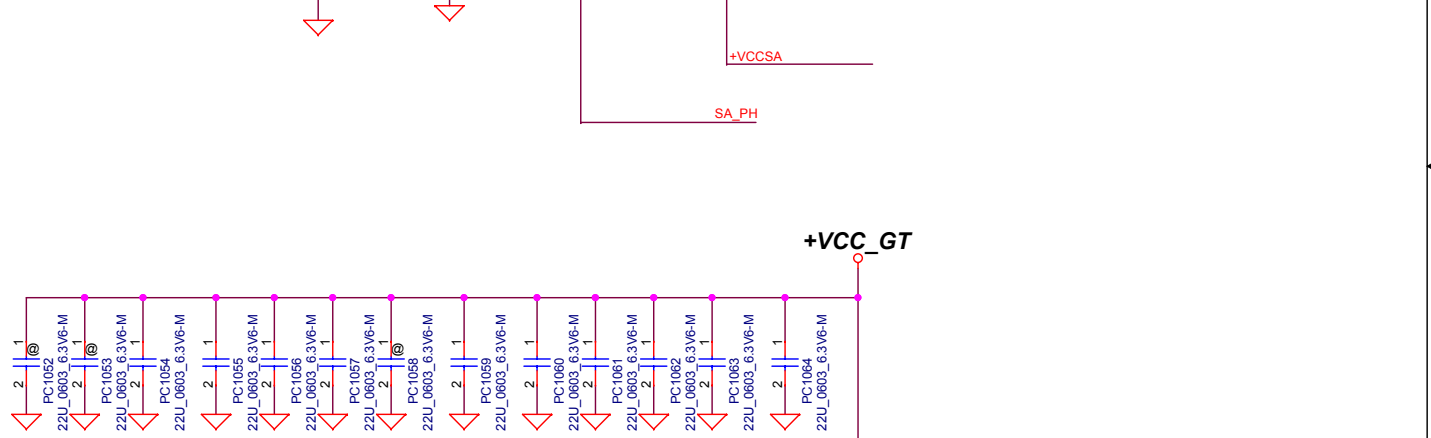
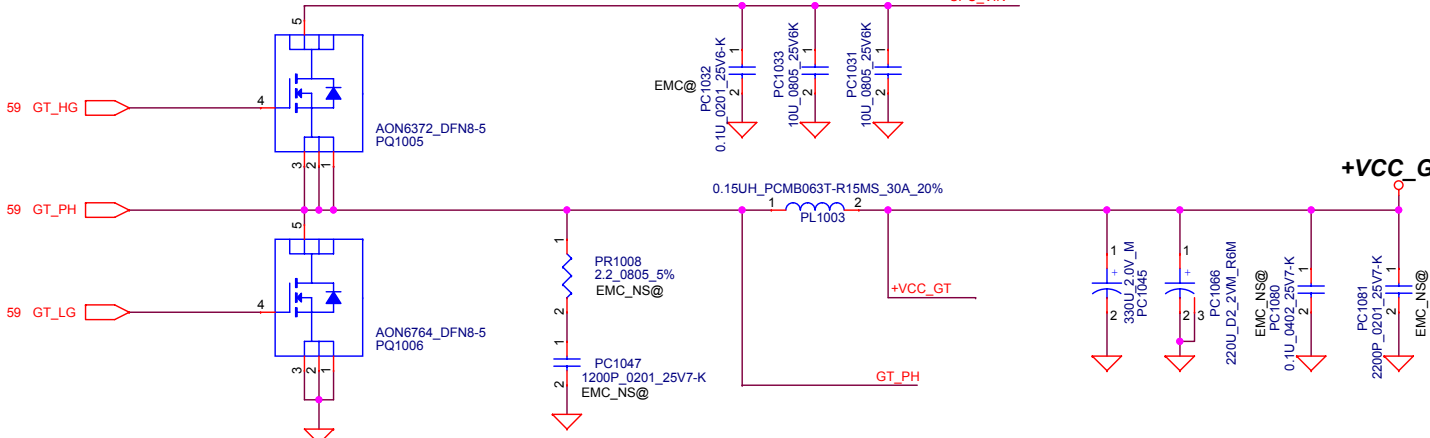
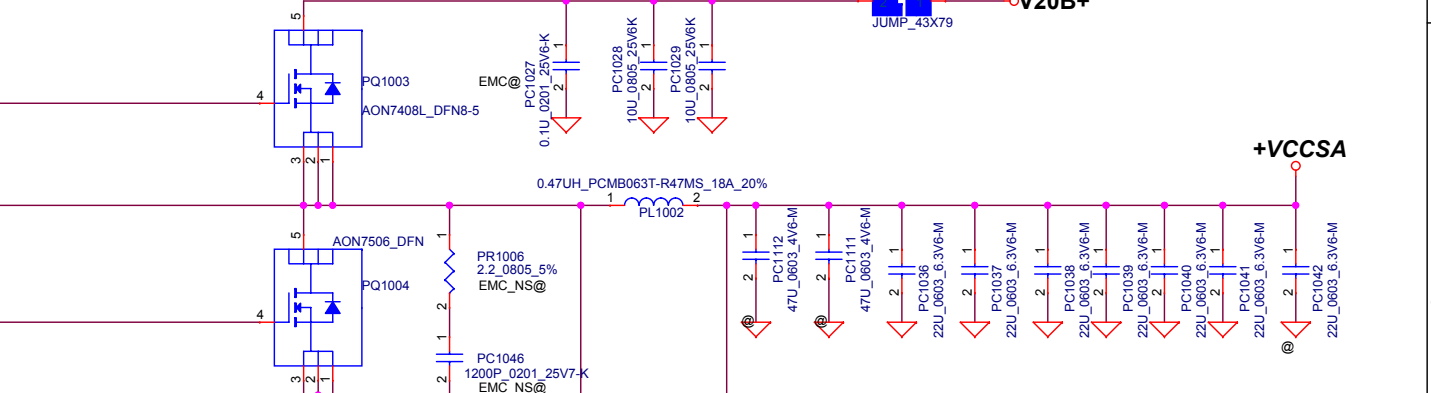
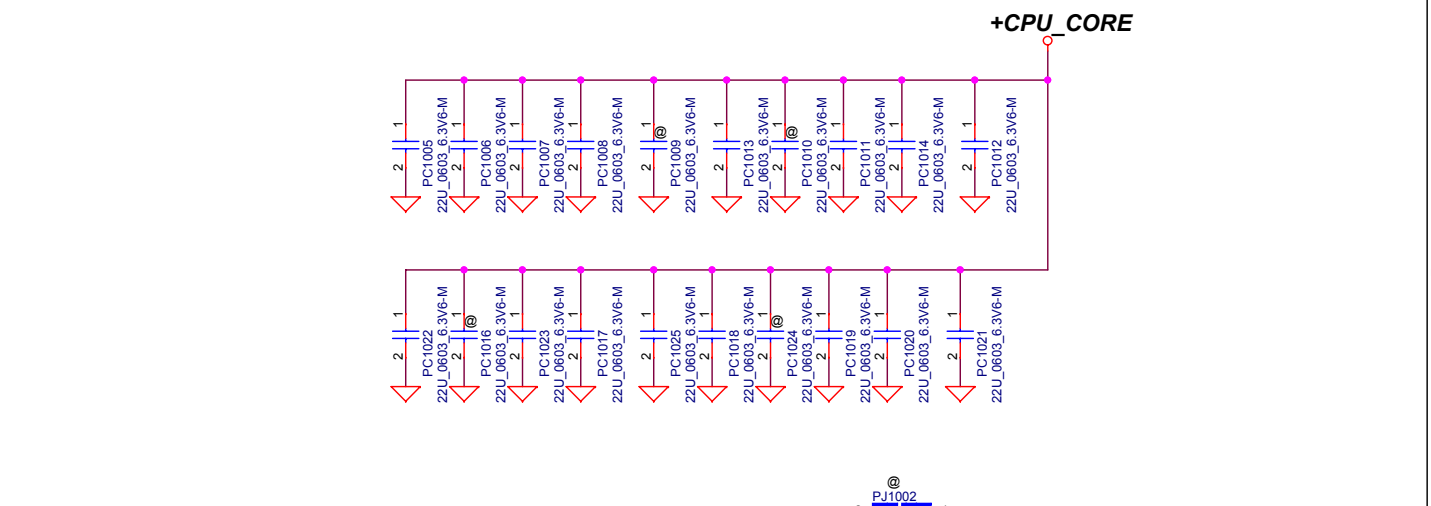
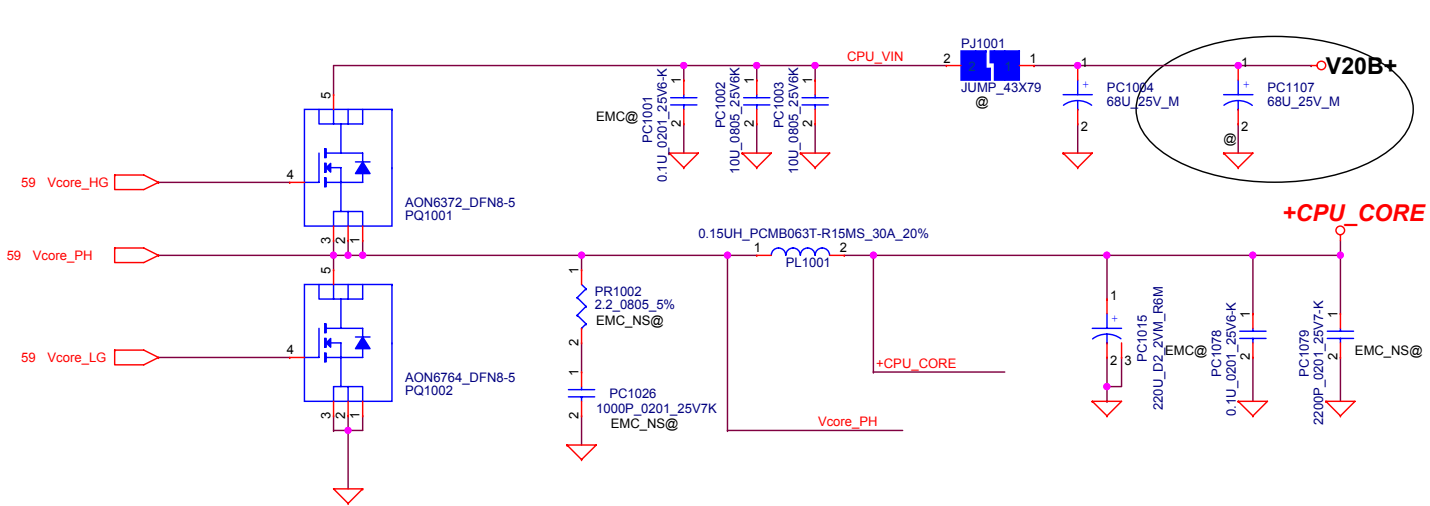
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- 20 PSI\_VGA PSI\_VGA
- 21 VSSSENSE\_VGA VSSSENSE\_VGA
- 21 VCCSENSE\_VGA VCCSENSE\_VGA
- 8.24.57 DGPU\_PWROK DGPU\_PWROK



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