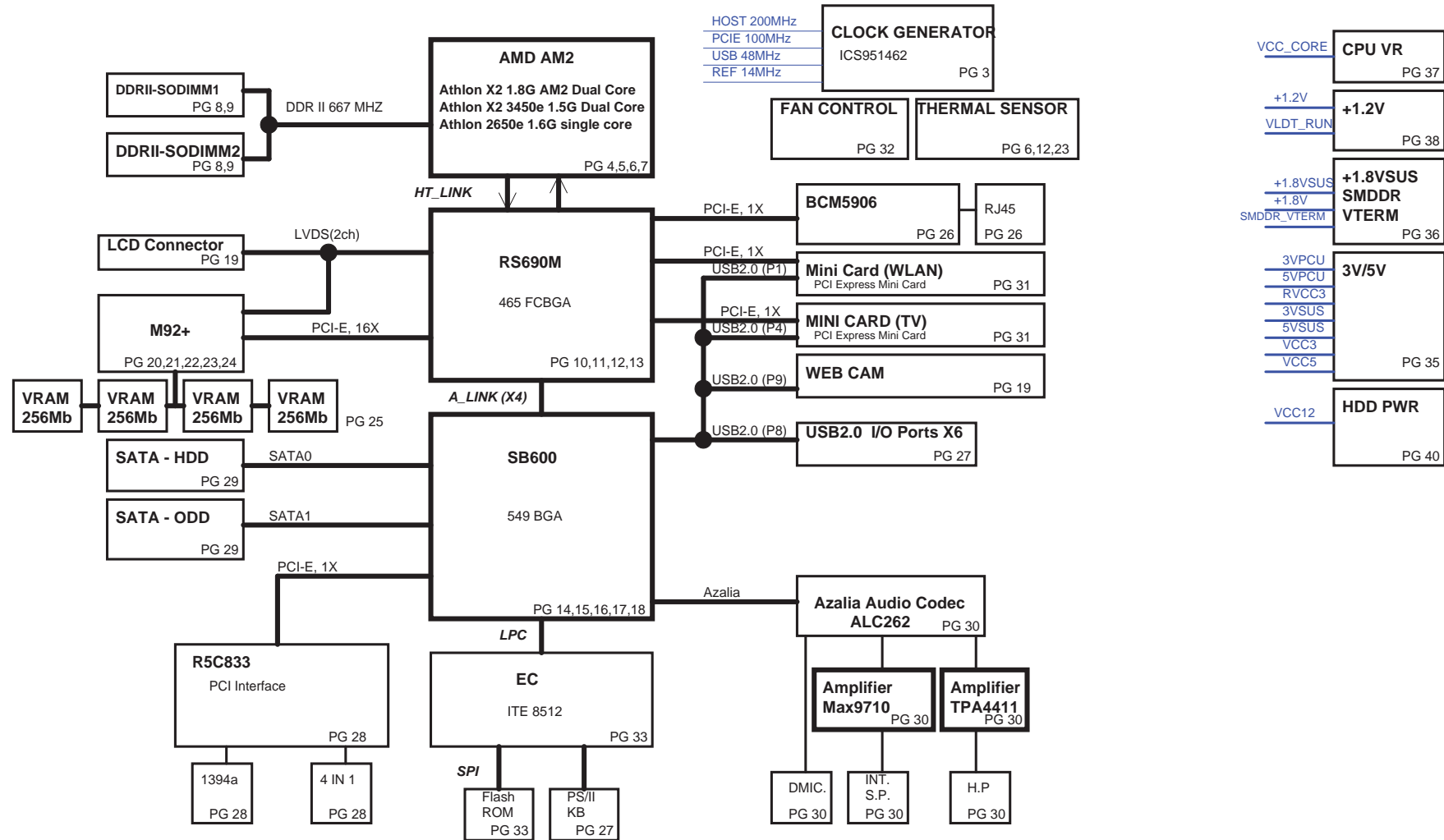


SYSTEM BLOCK DIAGRAM



Voltage Rails

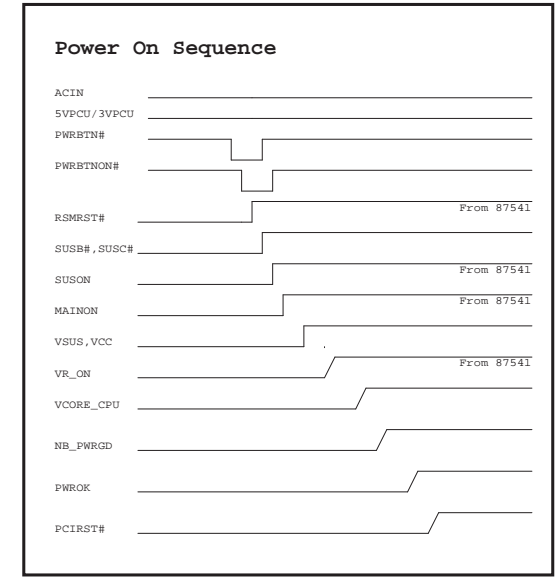
Power	Voltage	S0-S2	S3	S4	S5	Ctl Signal
VIN	19V	V	V	V	V	
5VPCU	5V	V	V	V	V	3V5V_EN
3VPCU	3V	V	V	V	V	3V5V_EN
15VPCU	15V	V	V	V	V	3V5V_EN
+3.3VALW	3V	V	V	V	V	STB_ON
+1.2VALW	1.2V	V	V	V	V	STB_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC2.5	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC_NB	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VCC1.1	1.1V	V				MAINON

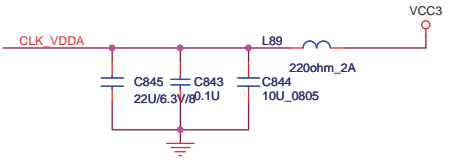
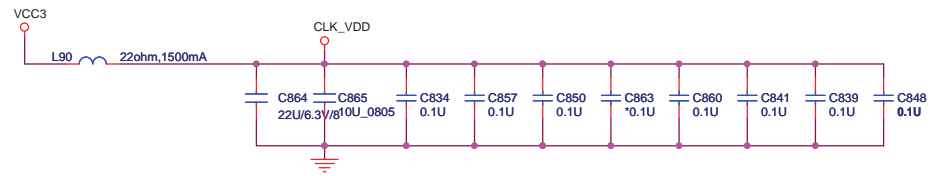
- Page 01: Block diagram
- Page 02: System information
- Page 03: Clock generator ICS951462
- Page 04: AMD M2+ HT I/F
- Page 05: AMD M2+ DDRII MEMORY I/F
- Page 06: AMD M2+ CTRL & DEBUG
- Page 07: AMD M2+ PWR & GND
- Page 08: DDR2 SODIMM X 2
- Page 09: DDR2 Termination
- Page 10: RS690MC HT interface
- Page 11: RS690MC PCIE interface
- Page 12: RS690MC PLL & VEDIO I/F
- Page 13: RS690MC Power
- Page 14: SB600 PCIE/PCI/RTC/LPC/CPU Interface
- Page 15: SB600 ACPI/GPIO/USB/AC97
- Page 16: SB600 SATA/PATA Interface
- Page 17: SB600 POWER & Decoupling
- Page 18: SB600 Straps
- Page 19: LCD PANEL/WEBCAM
- Page 20: M82-M(PCIE I/F)
- Page 21: M82M(LVDS/RGB/HDMI/TV)
- Page 22: M82-M(MEM I/F)
- Page 23: M82-M(Thermal/STRAP/EEPROM)
- Page 24: M82-M(POWER/GND)
- Page 25: VRAM1*4(GDDR2-BGA84)
- Page 26: LAN BCM5906
- Page 27: USB
- Page 28: R5C843 PCI/1394
- Page 29: SATA HDD/ODD
- Page 30: HD_ALC262
- Page 31: MINI CARD
- Page 32: FAN/ Daughter board
- Page 33: EC ITE8512
- Page 34: ACIN
- Page 35: 5V / 3V (MAX10720)
- Page 36: DDR 1.8V(TPS51116)
- Page 37: CPU CORE (MAX8774)
- Page 38: NB 1.2V(RT8202)
- Page 39: VDD_CORE (OZ8118)
- Page 40: 12V/ HDD(MAX15026)
- Page 41: NB CORE(OZ8116)
- Page 42: POWER MANGER DIAGRAM
- Page 43: SCREW HOLE & EMI
- Page 44: History

PCB STACK UP

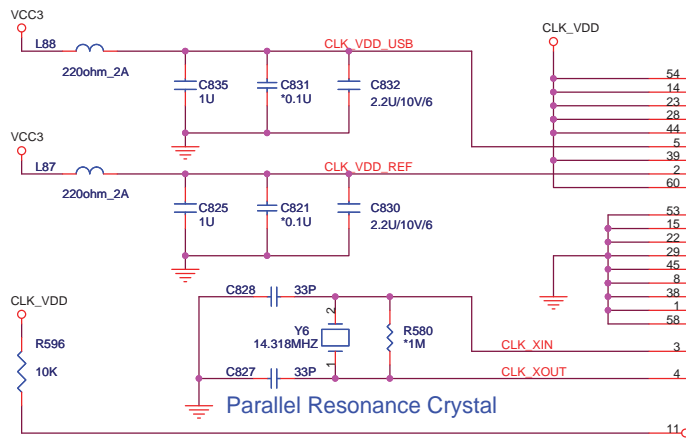
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : VCC
- LAYER 6 : IN2
- LAYER 7 : GND
- LAYER 8 : BOT

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLK
NB VGA	NA	A		
SB	AD31(INT)	NA	NA	
AC87/AZALIA	AD31	NA	B	INT
USB	AD30	NA	D	INT
R5C843	AD16	0	E/F/G	PCLK0



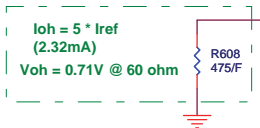


Put Decoupling Caps close to Clock Fen. power pin



Parallel Resonance Crystal

8,15,23 SCLK0
8,15,23 SDATA0



$$I_{oh} = 5 * I_{ref} \quad (2.32mA)$$

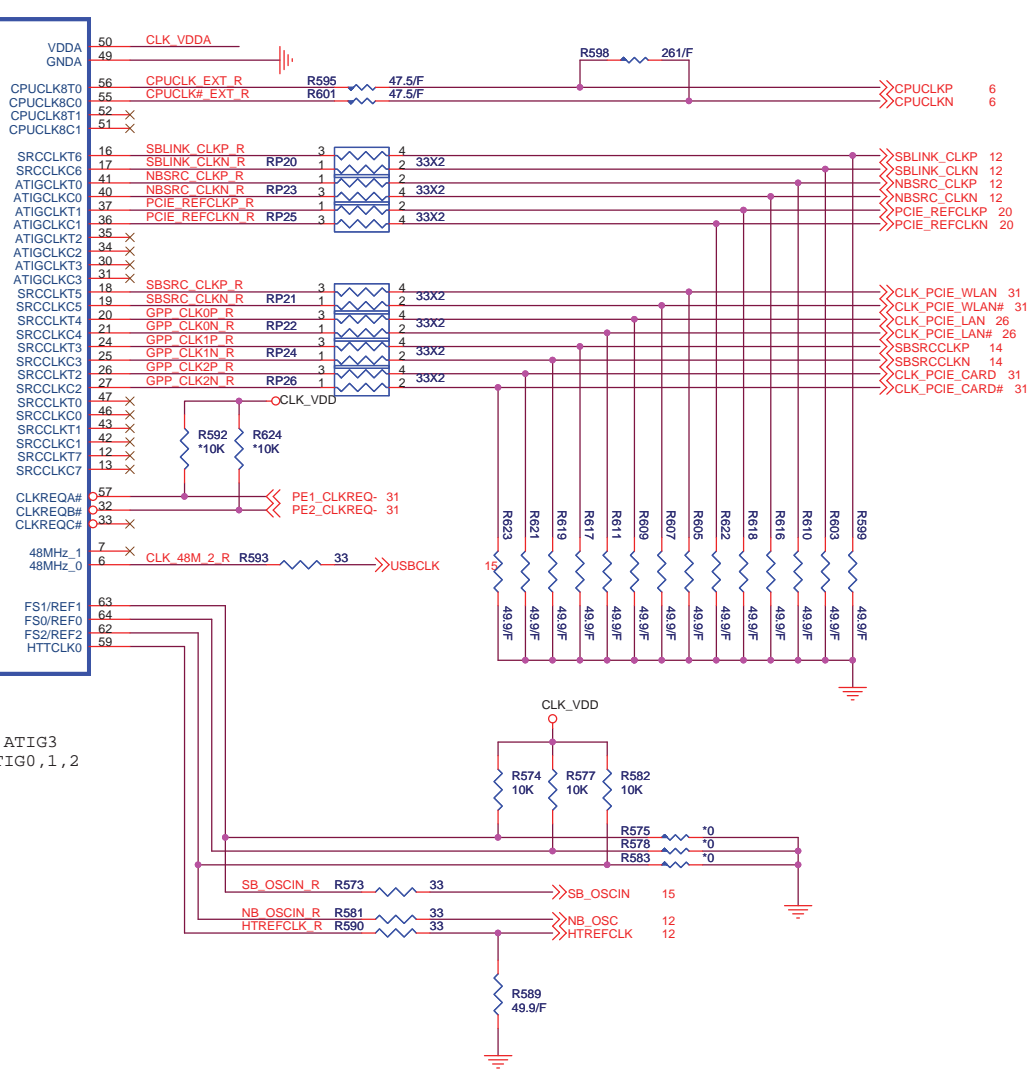
$$V_{oh} = 0.71V @ 60 \text{ ohm}$$


CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock



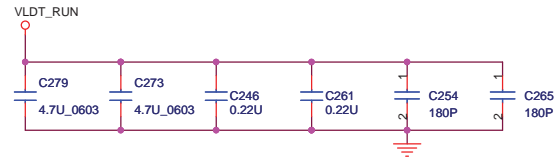
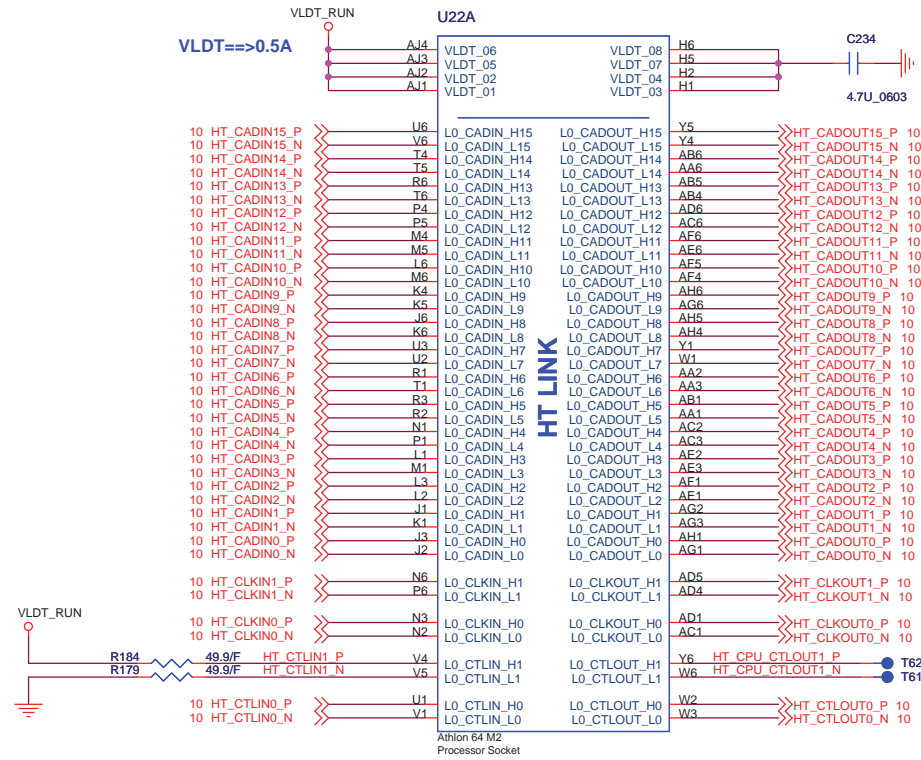


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PROJECT : QUI

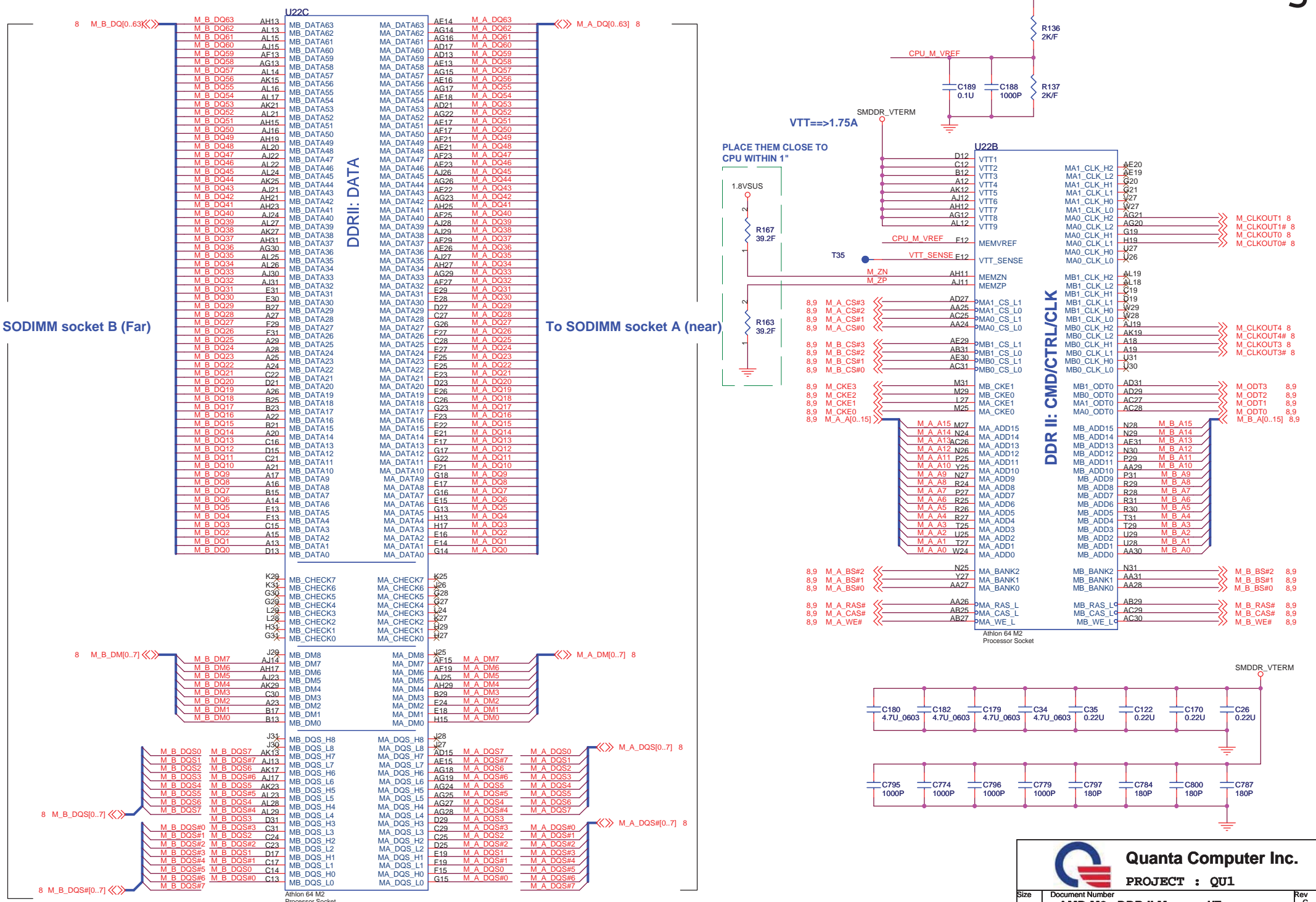
Size	Document Number	Rev
Clock Generator		C
Date:	Saturday, February 21, 2009	Sheet 3 of 44

CPU HyperTransport Interface

VDDLDRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



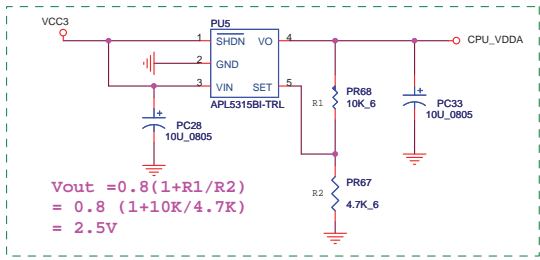
Processor DDR2 Memory Interface



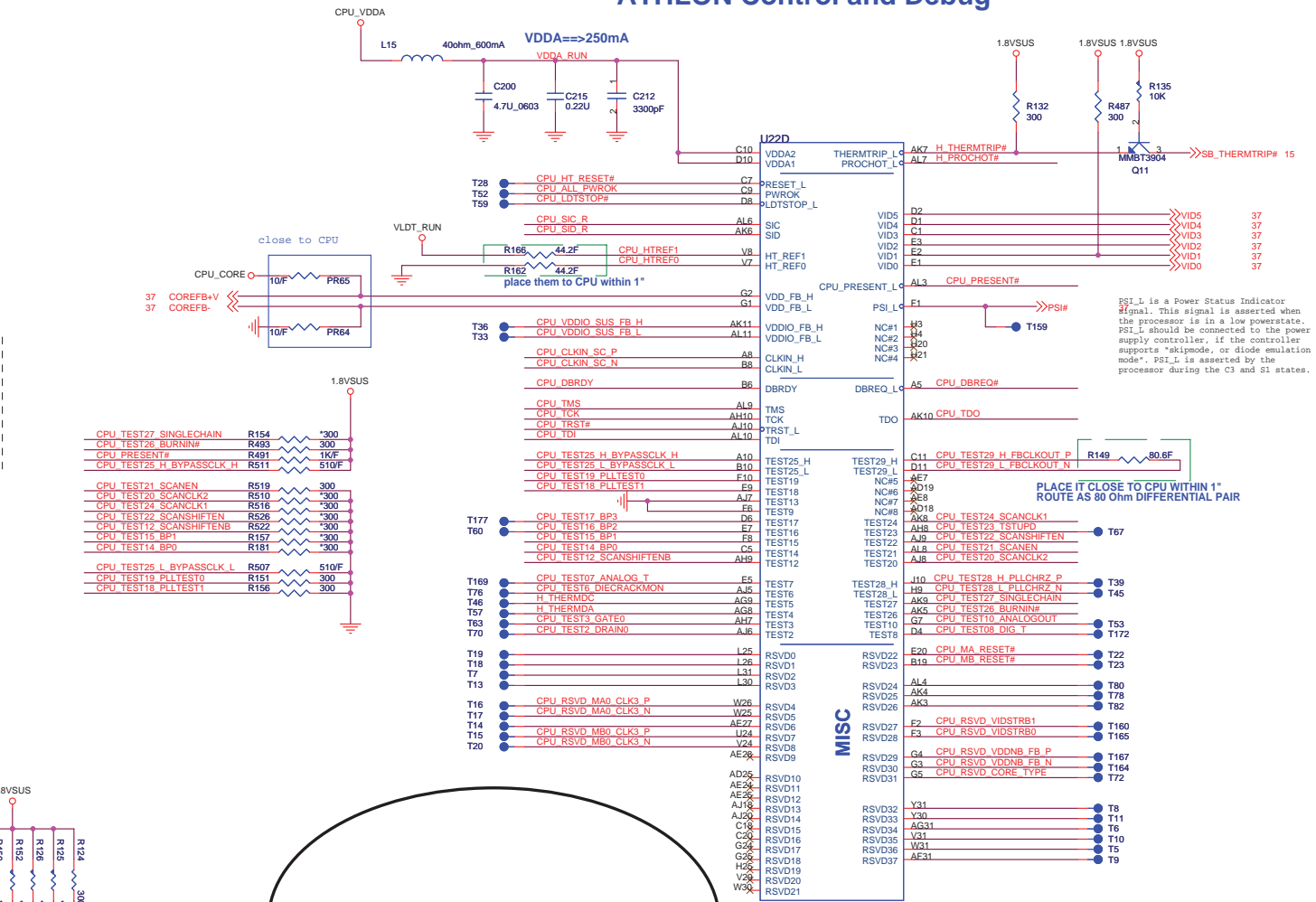
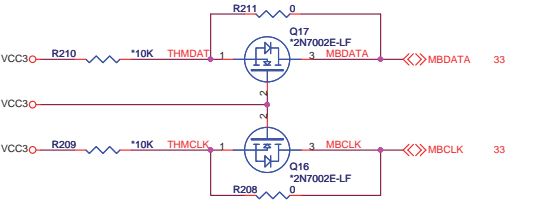
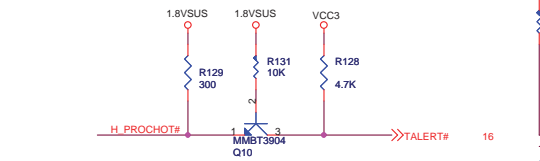
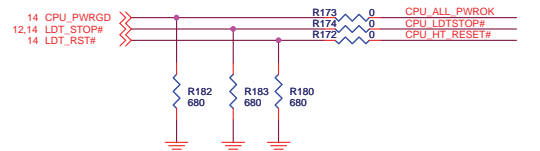
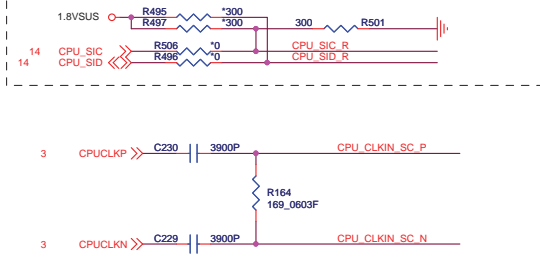
Quanta Computer Inc.
PROJECT : QUI

Size	Document Number	Rev
	AMD M2+ DDR II Memory I/F	C
Date:	Saturday, February 21, 2009	Sheet 5 of 44

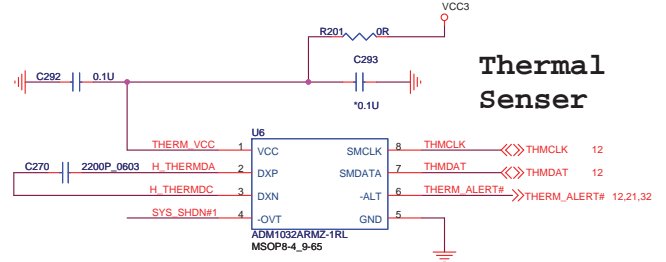
ATHLON Control and Debug



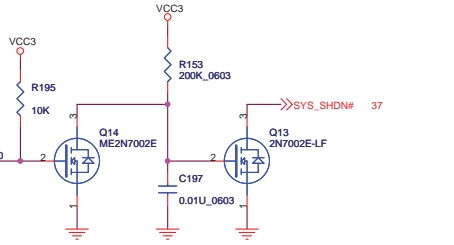
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pullup to VSS.



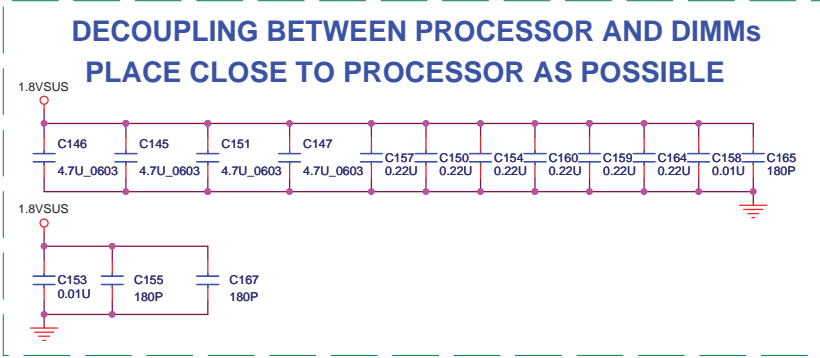
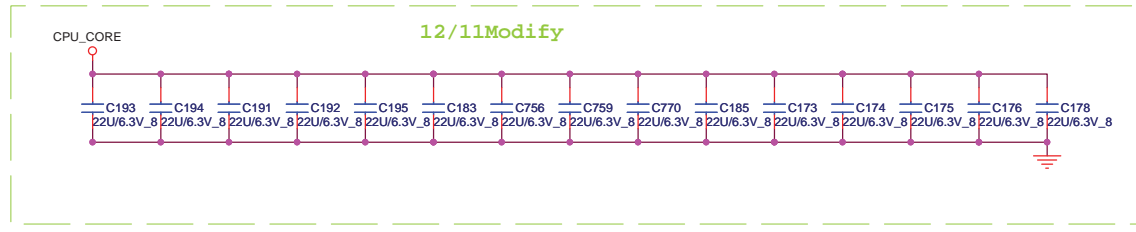
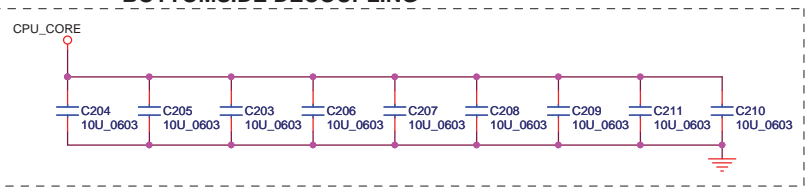
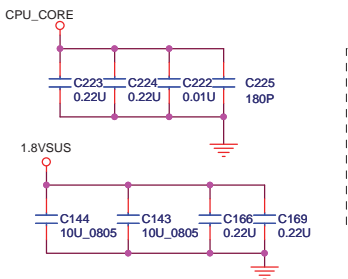
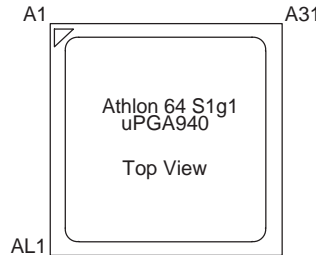
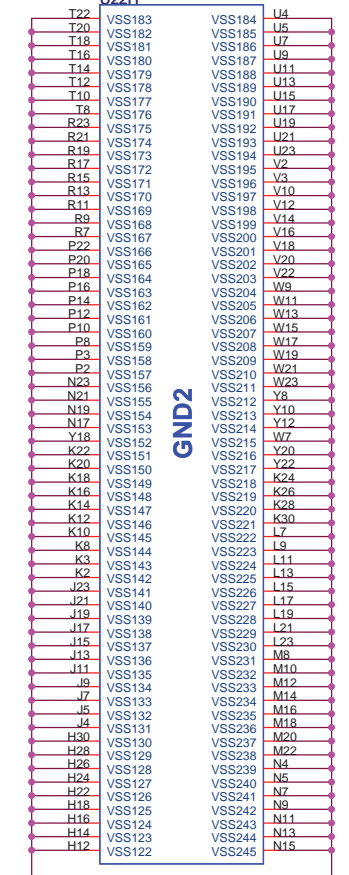
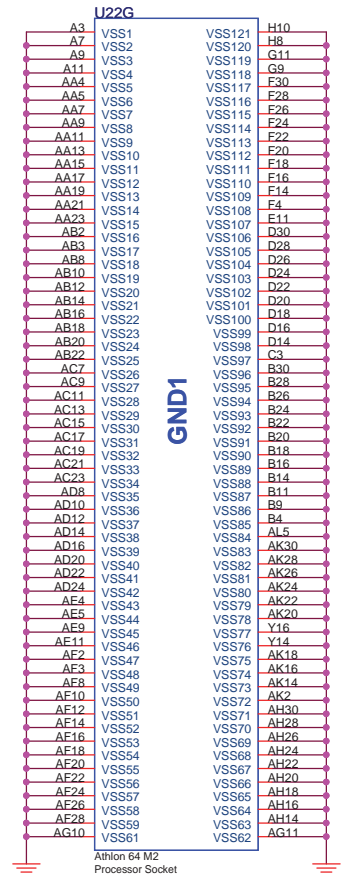
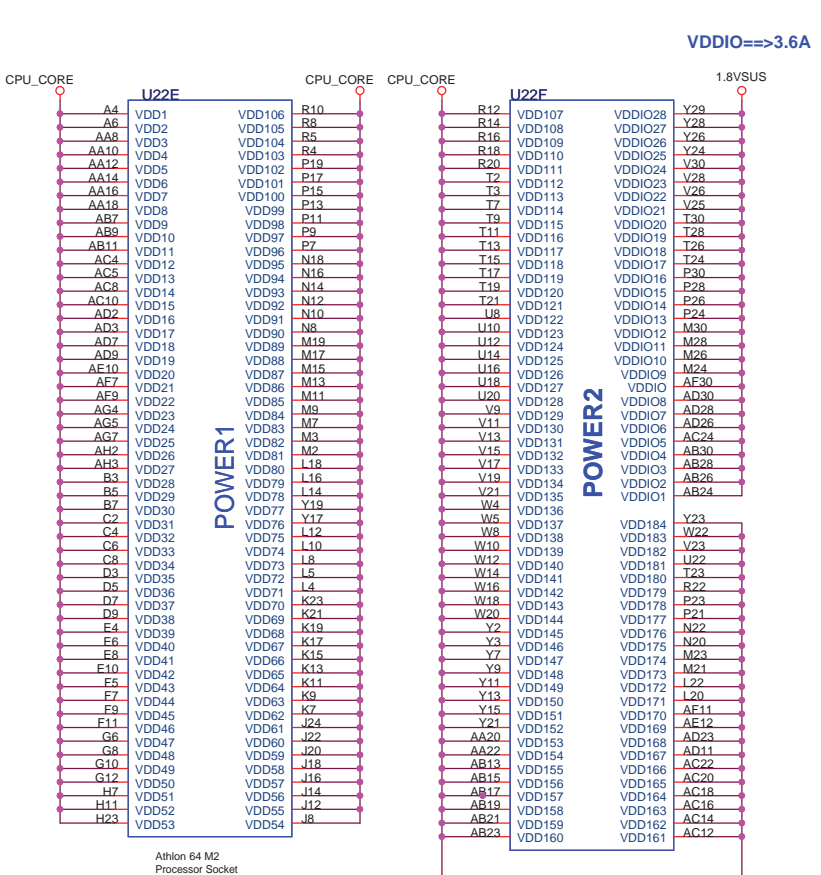
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

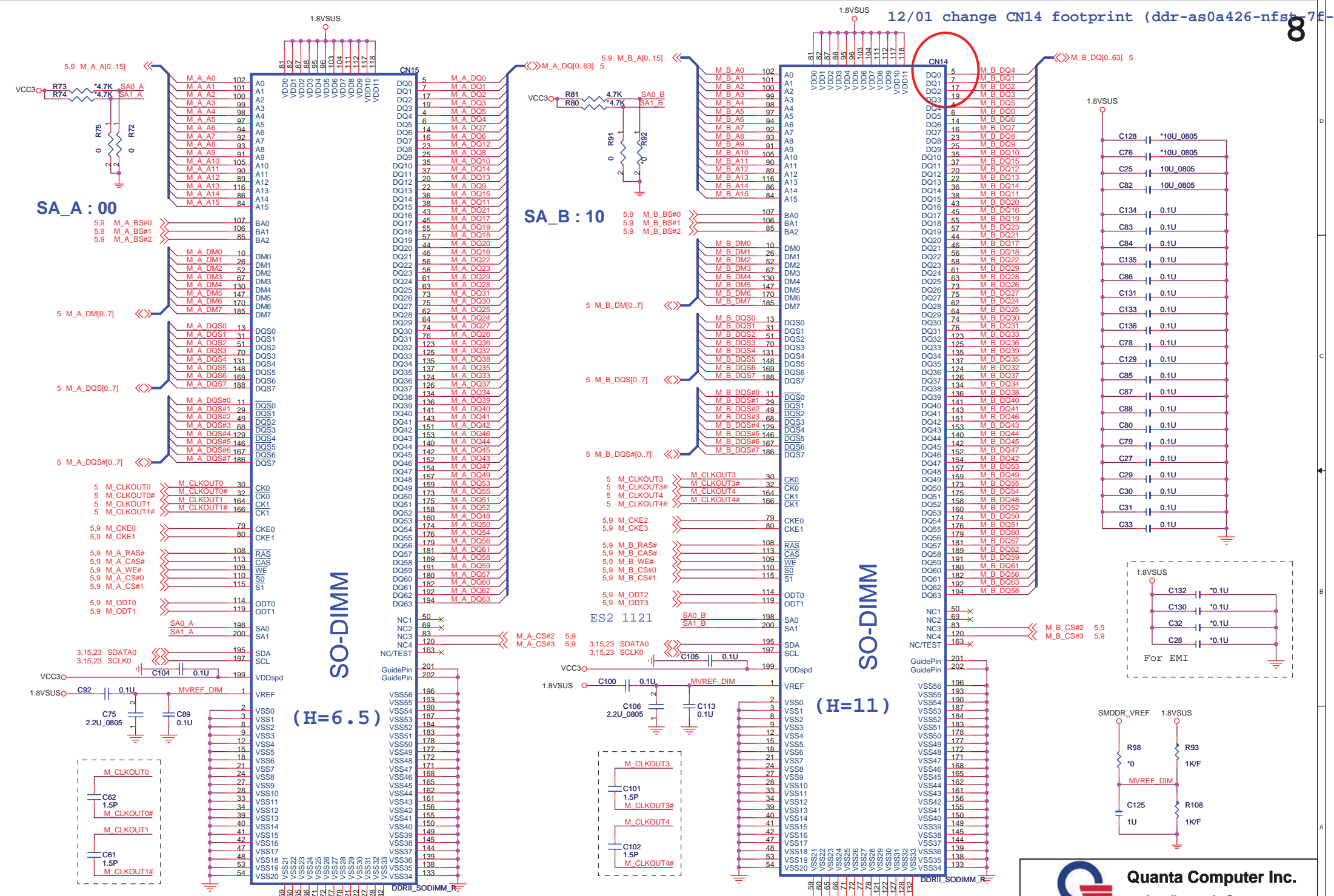


SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

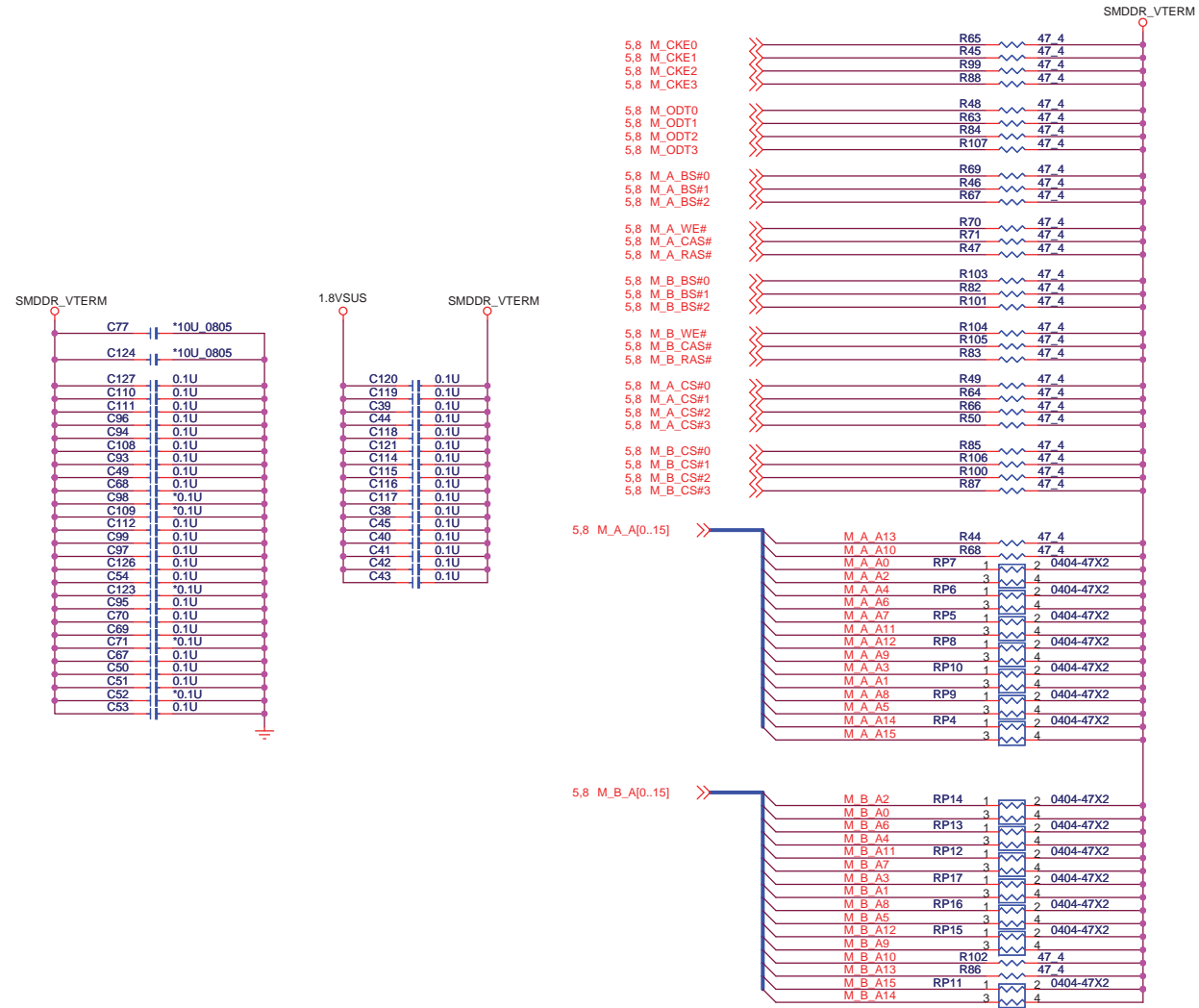


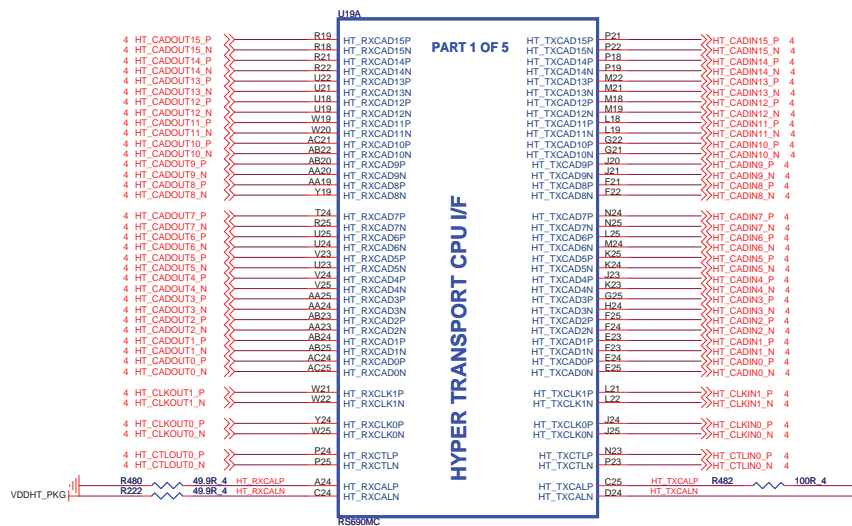
PROCESSOR POWER AND GROUND



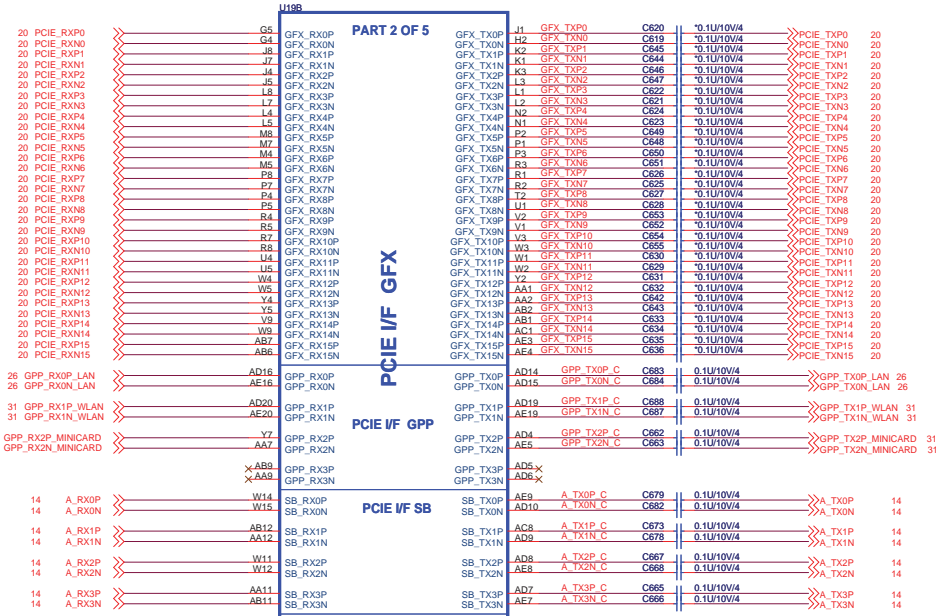


1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resin only from the business partners that Sony approves as Green Partners.



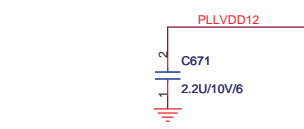
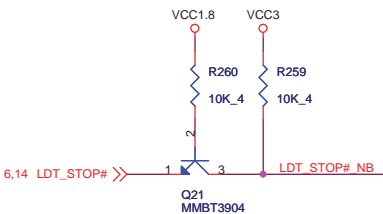
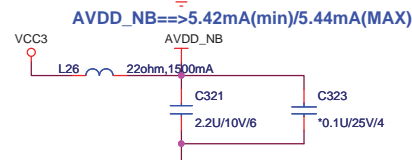
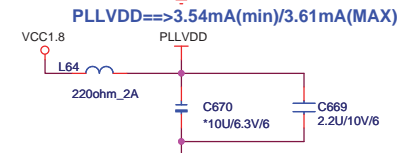
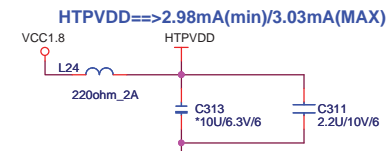


20 PCIE_RXP[15..0] >> PCIE_RXP[15..0]
 20 PCIE_RXN[15..0] >> PCIE_RXN[15..0]
 20 PCIE_TXP[15..0] >> PCIE_TXP[15..0]
 20 PCIE_TXN[15..0] <<< PCIE_TXN[15..0]

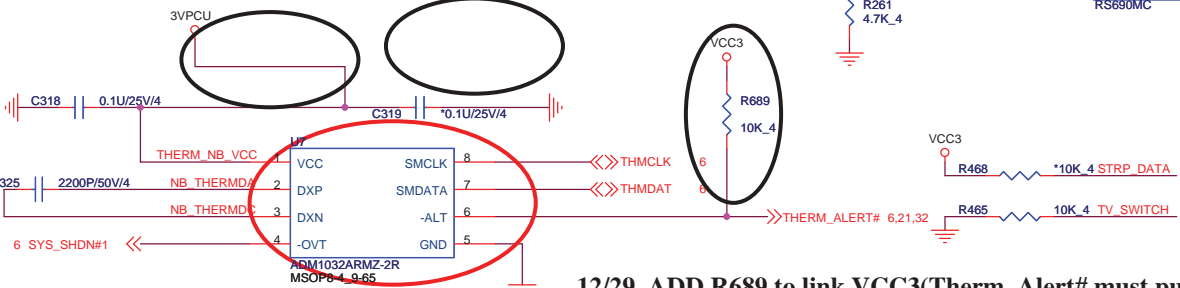


Place these caps close to connector



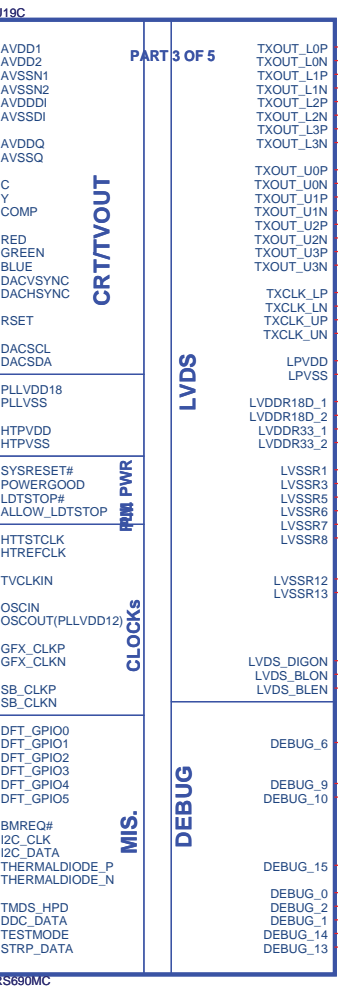
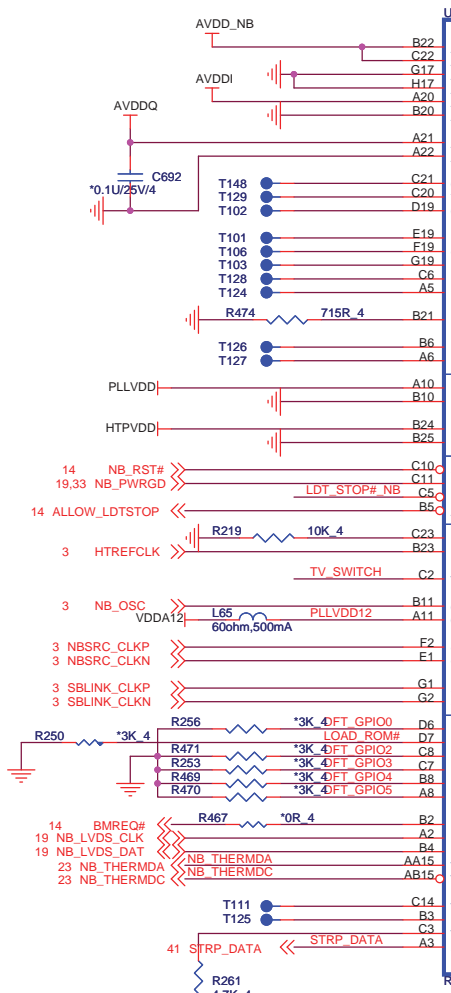


NB Thermal Sensor



12/29 ADD R689 to link VCC3(Therm_Alert# must push Hi)

12/02 change U7 P/N:AL001032002



PART 3 OF 5

CRT/VIDEO

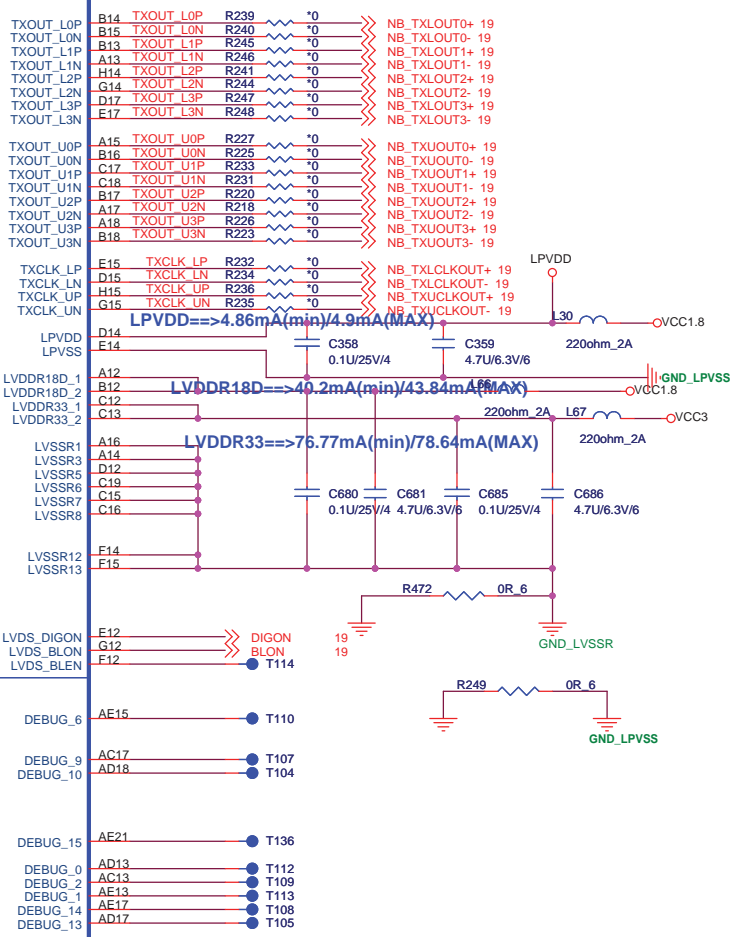
LVDS

PWR

CLOCKS

DEBUG

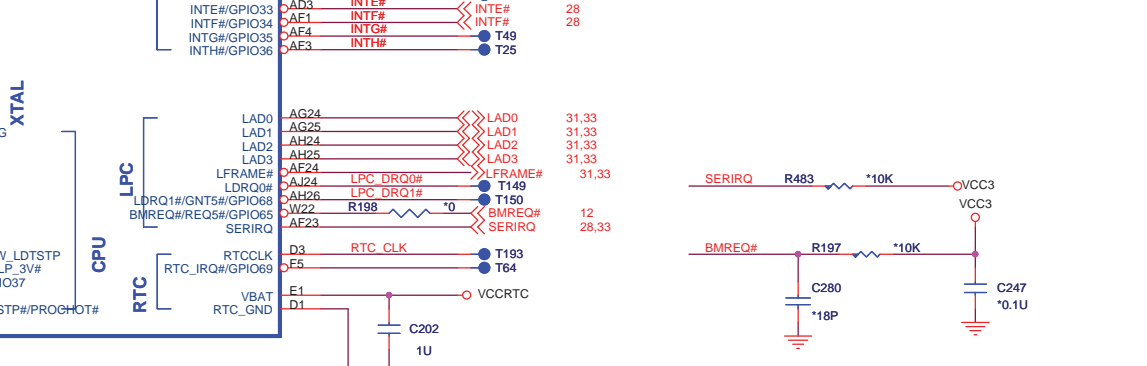
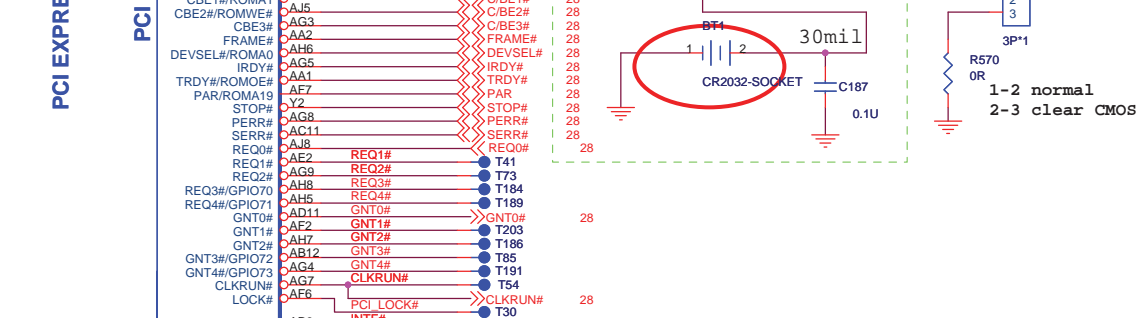
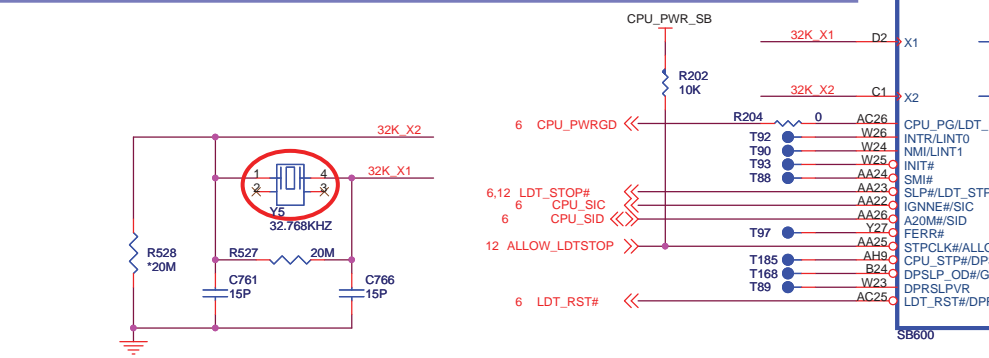
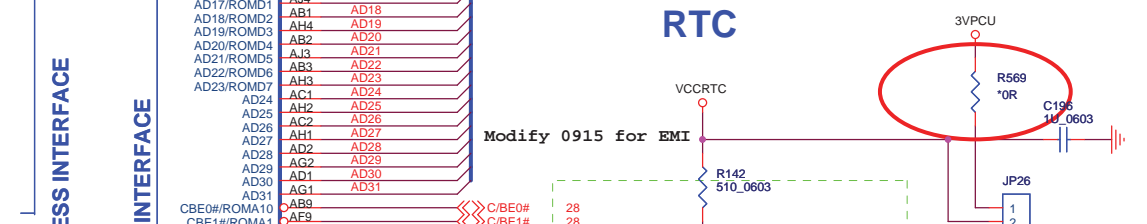
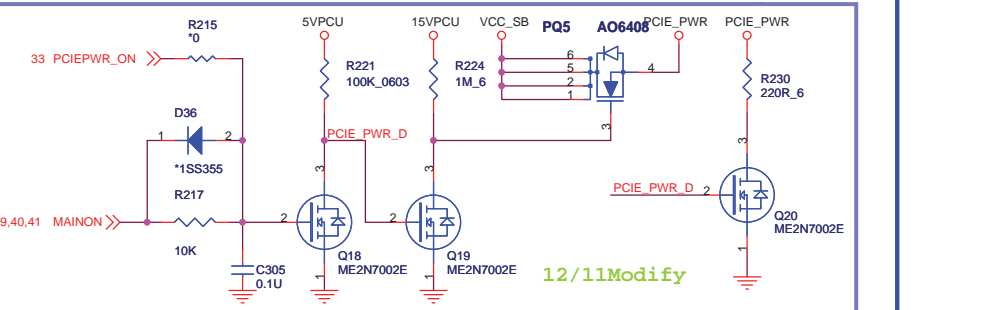
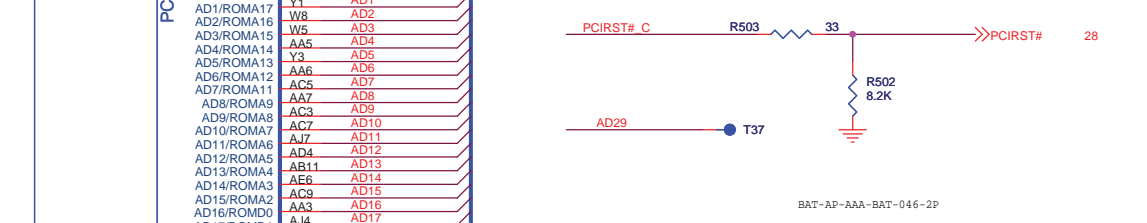
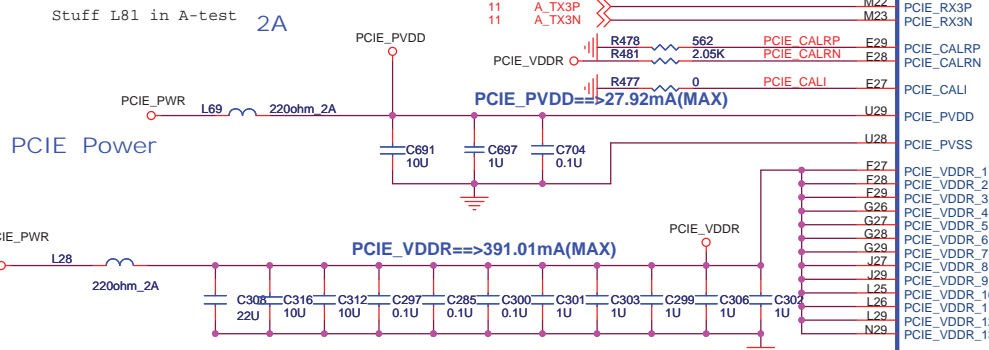
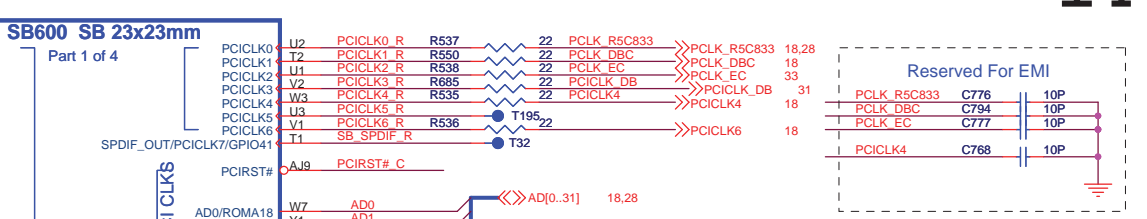
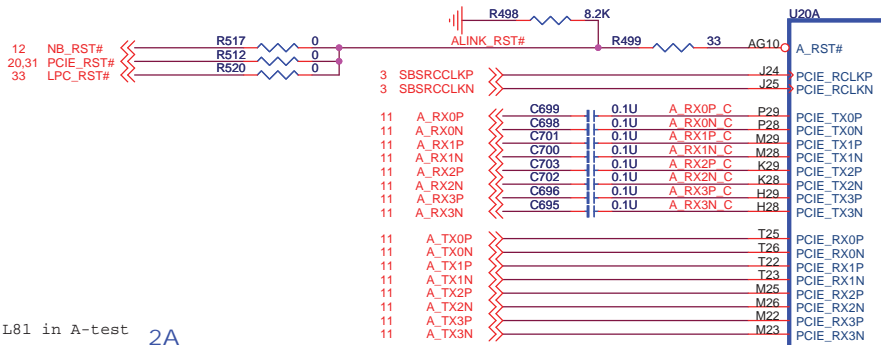
MIS.



LOAD_ROM#: LOAD ROM STRAP ENABLE
 High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

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PROJECT : QU1

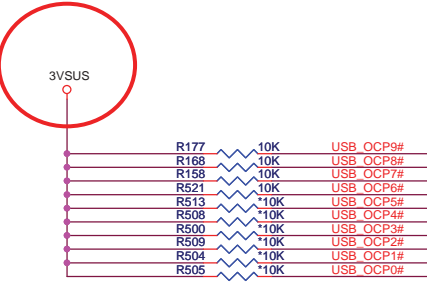
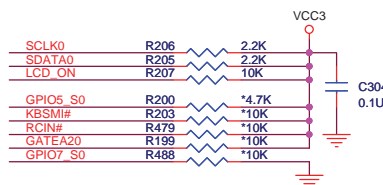
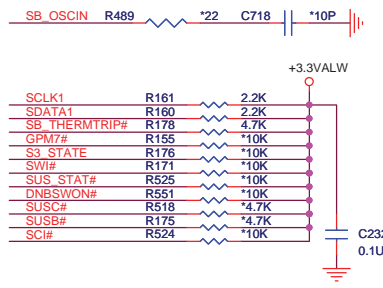
Size	Document Number	Rev
	RS690MC PLL & VEDIO I/F	A
Date:	Saturday, February 21, 2009	Sheet 12 of 44



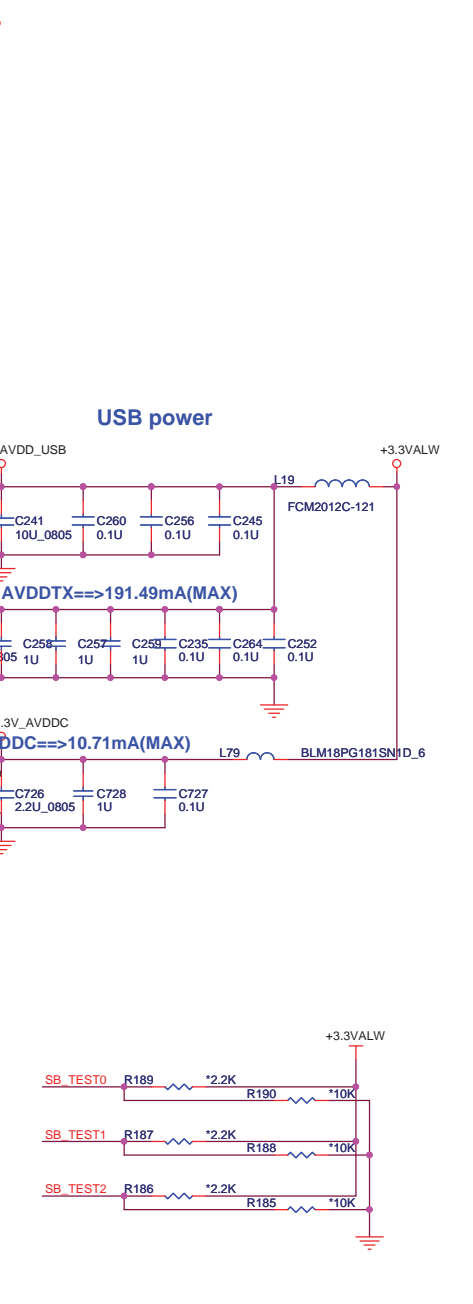
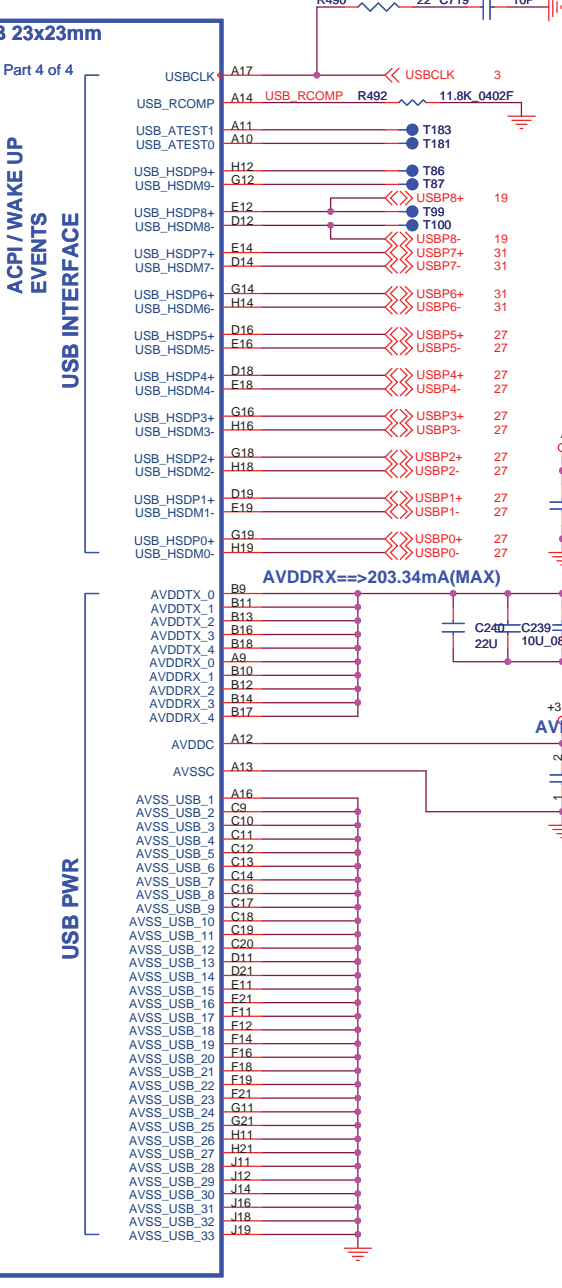
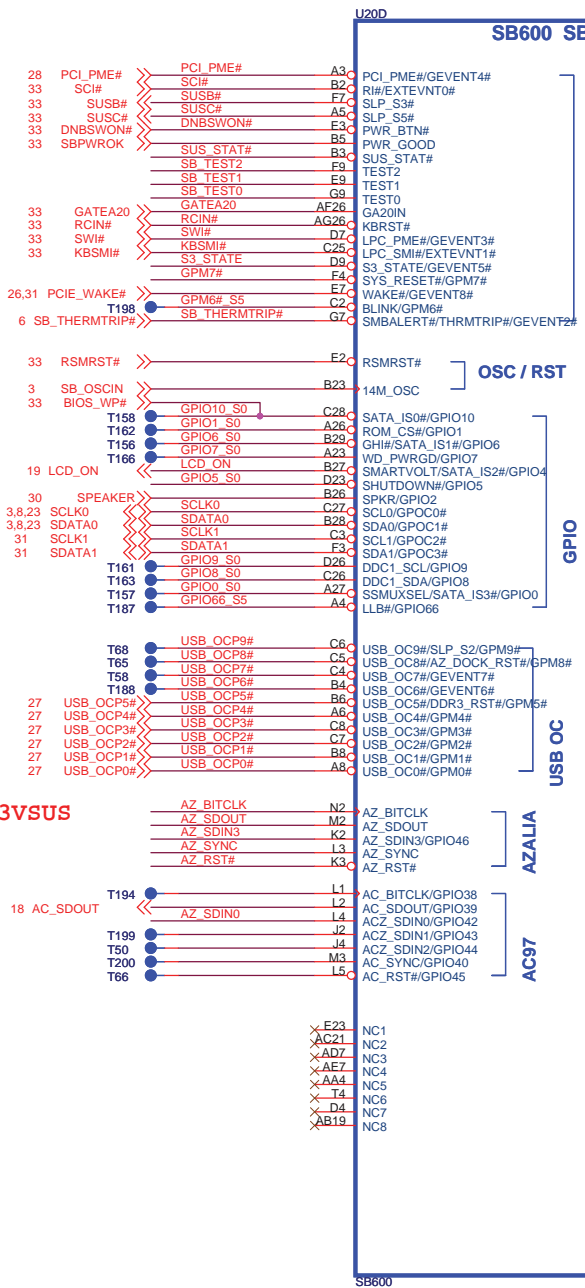
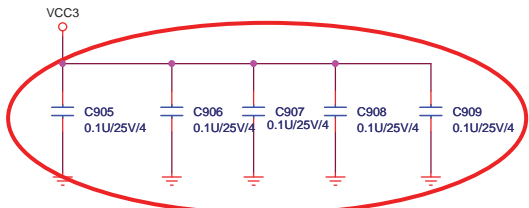
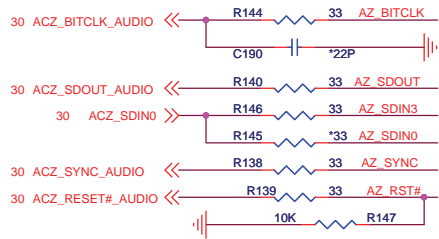
12/01 Change Y5 footprint like Y1 (XTAL-8_4X3_7-5_5X2_8)

Quanta Computer Inc.
PROJECT :QU1

Size	Document Number	Rev
	SB600 PCIE/PCI/CPU/LPC	C
Date:	Saturday, February 21, 2009	Sheet 14 of 44



12/05 change USB Power from Vcc3 to 3VSUS



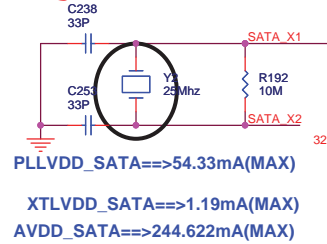
12/10 add xxxxxxxx

Quanta Computer Inc.
PROJECT :QU1

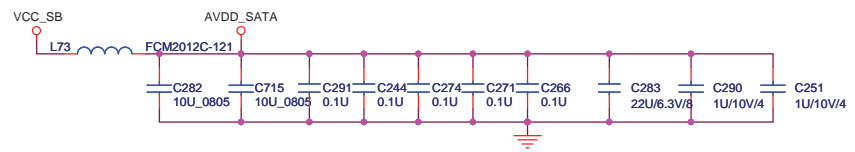
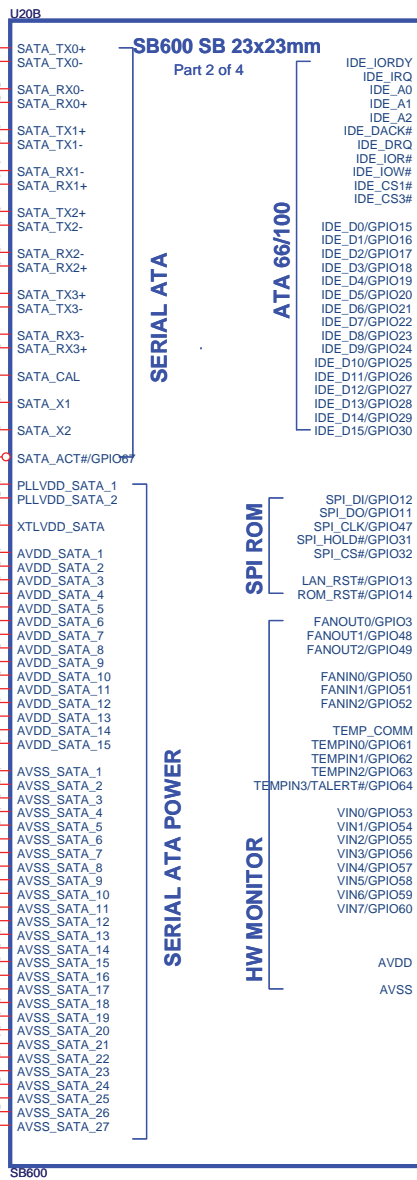
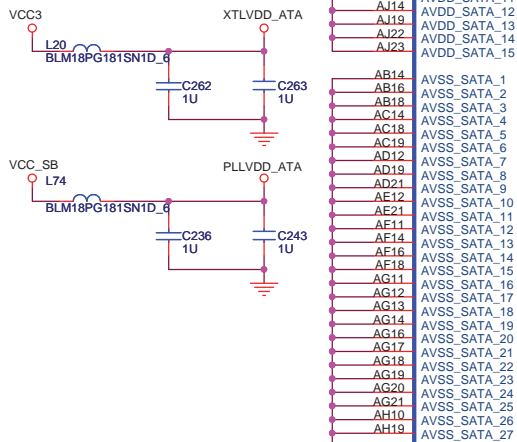
Size	Document Number	Rev	C
	SB600 ACPI/GPIO/USB/AC97		
Date:	Saturday, February 21, 2009	Sheet	15 of 44

12/26 change Y2 P/N to meet ACL.(BG625000737)

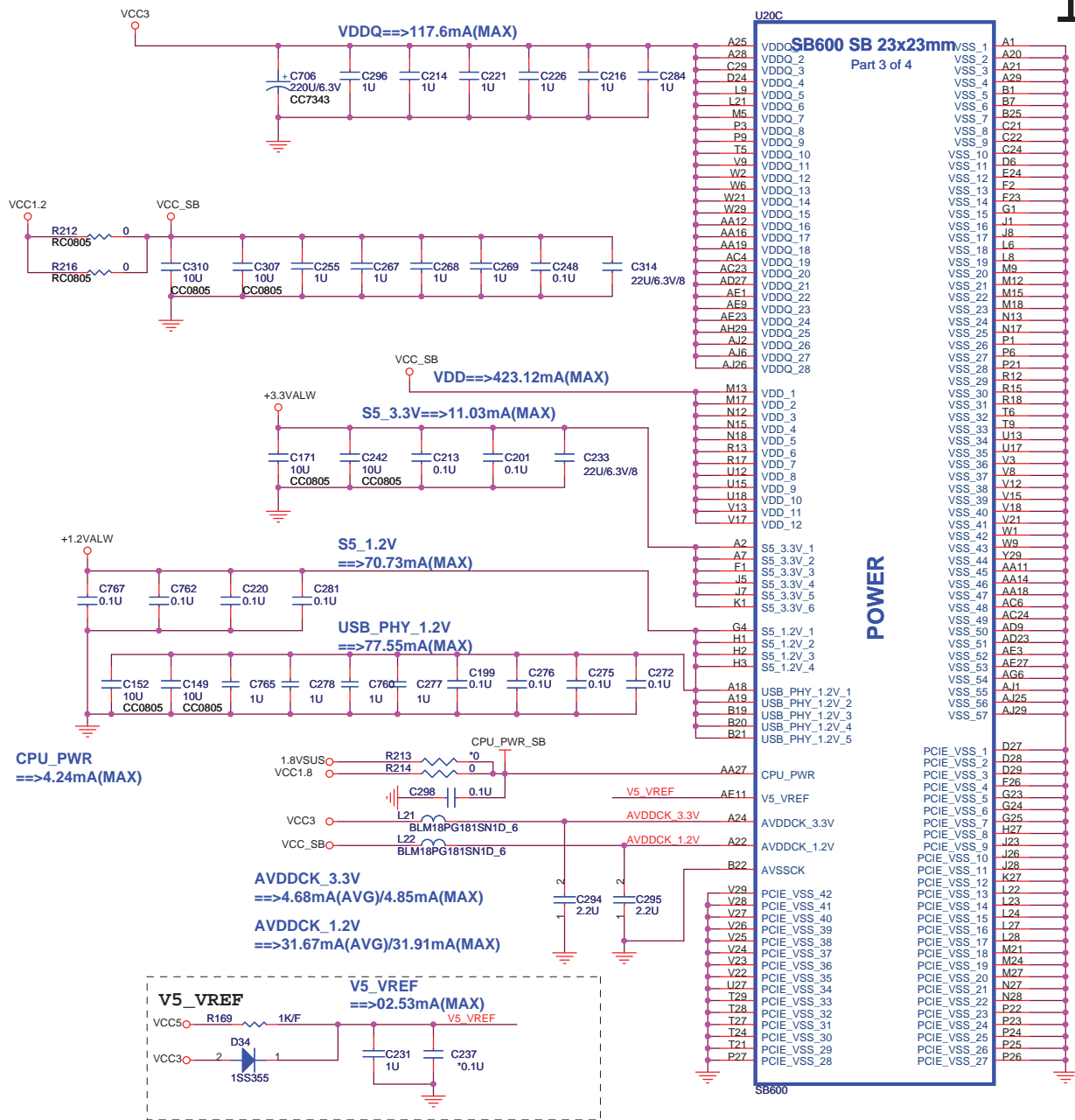
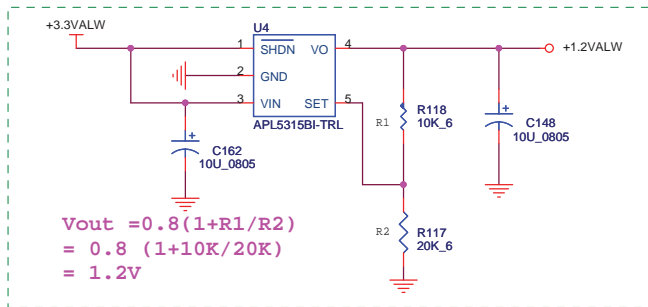
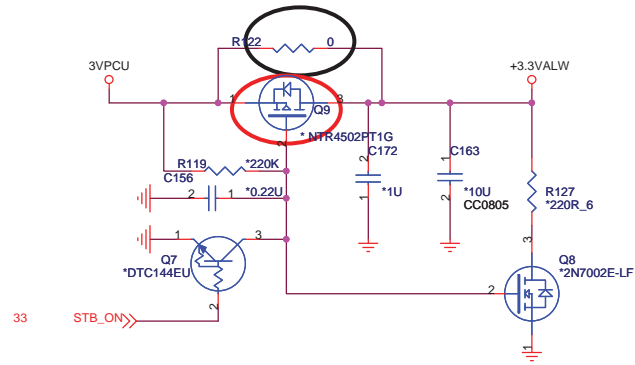
12/02 change Y2 P/N:BG625000885



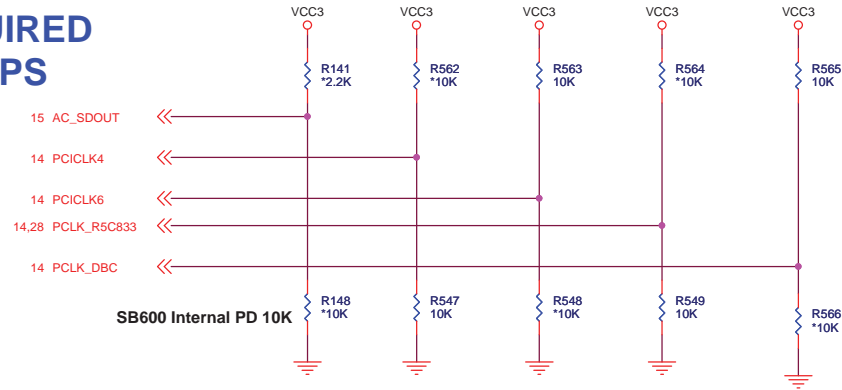
SATA Power



12/21 ADD R122 for HW Lose

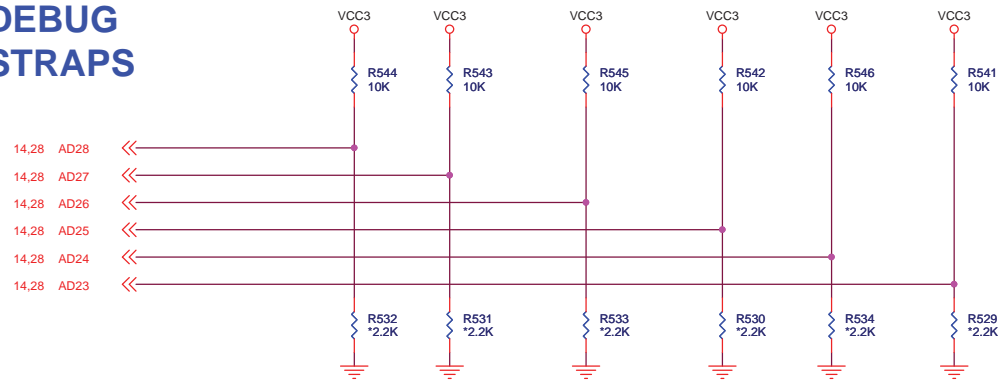


REQUIRED STRAPS



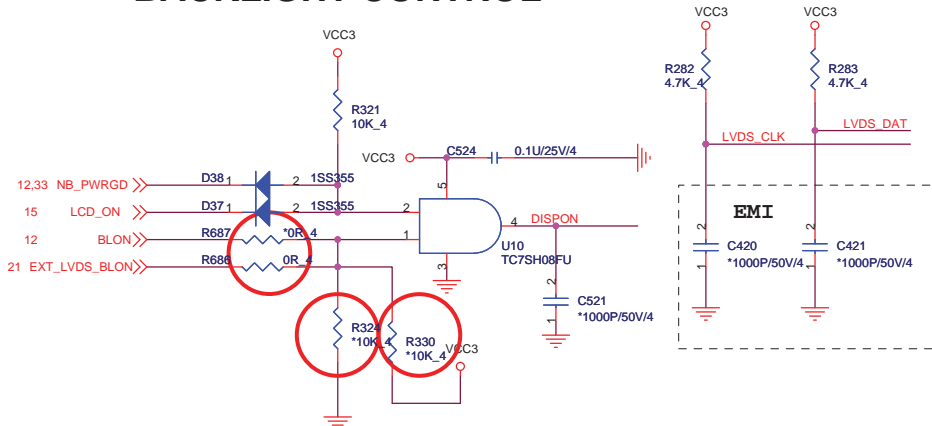
	AC_SDOUT	PCICLK4	PCICLK6	PCLK_R5C843	PCLK_DBC
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	PCI_CLK0	PCI_CLK1
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

BACKLIGHT CONTROL

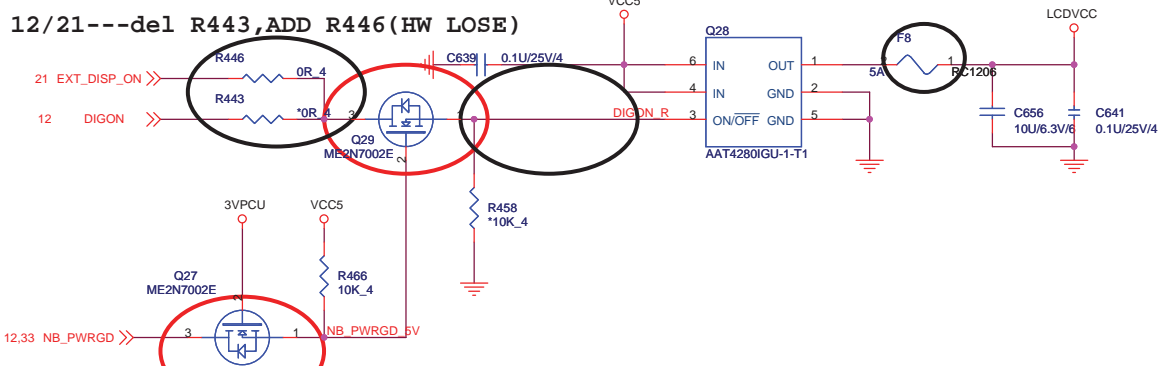


12/05---del R330,R324(white screen issue)
 12/05---exchange D35,D36 to R686,R687(white screen issue)

PANEL VCC CONTROL

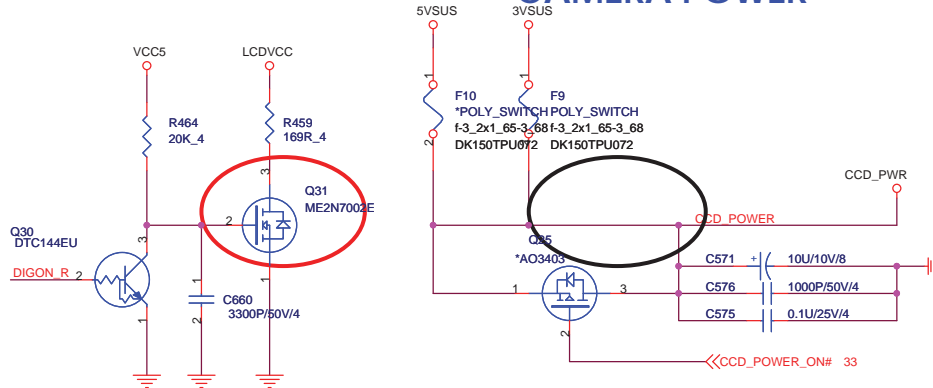
Change F8=7A fuse (P/N:DK700WFO06)(LCD INRUSH CURRENT=3A)

12/21---del R443,ADD R446(HW LOSE)



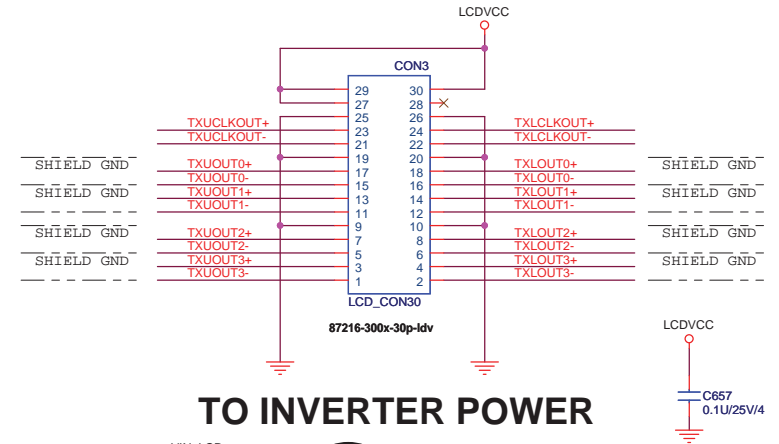
12/01 change the footprint to SOT23_213-3_3-2

CAMERA POWER

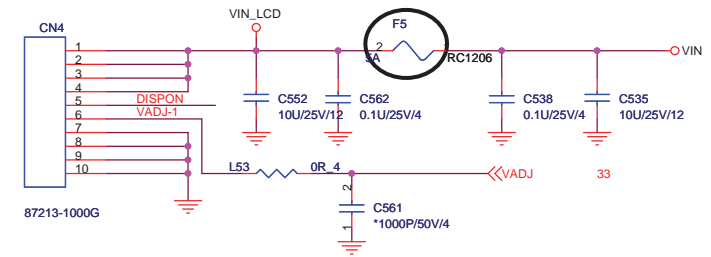


12/01 change the footprint to SOT23_213-3_3-2

LCD CONNECTOR

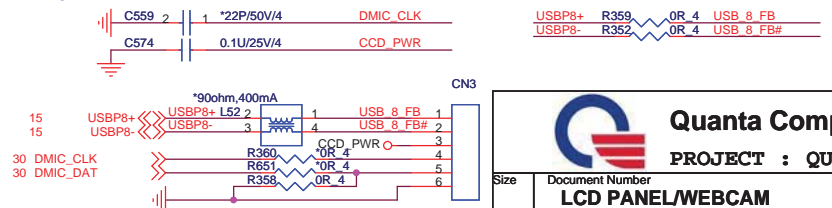


TO INVERTER POWER



21 GPU_LVDS_DAT	R289	0	LVDS_DAT	R285	*0	NB_LVDS_DAT	12
21 GPU_LVDS_CLK	R288	0	LVDS_CLK	R284	*0	NB_LVDS_CLK	12
21 GPU_TXLOUT0-	R454	0	TXLOUT0-	R262	*0	NB_TXLOUT0-	12
21 GPU_TXLOUT0+	R456	0	TXLOUT0+	R257	*0	NB_TXLOUT0+	12
21 GPU_TXLOUT1-	R450	0	TXLOUT1-	R266	*0	NB_TXLOUT1-	12
21 GPU_TXLOUT1+	R452	0	TXLOUT1+	R264	*0	NB_TXLOUT1+	12
21 GPU_TXLOUT2-	R445	0	TXLOUT2-	R270	*0	NB_TXLOUT2-	12
21 GPU_TXLOUT2+	R448	0	TXLOUT2+	R268	*0	NB_TXLOUT2+	12
21 GPU_TXUOUT0-	R453	0	TXUOUT0-	R263	*0	NB_TXUOUT0-	12
21 GPU_TXUOUT0+	R455	0	TXUOUT0+	R258	*0	NB_TXUOUT0+	12
21 GPU_TXUOUT1-	R449	0	TXUOUT1-	R267	*0	NB_TXUOUT1-	12
21 GPU_TXUOUT1+	R451	0	TXUOUT1+	R265	*0	NB_TXUOUT1+	12
21 GPU_TXUOUT2-	R444	0	TXUOUT2-	R271	*0	NB_TXUOUT2-	12
21 GPU_TXUOUT2+	R447	0	TXUOUT2+	R269	*0	NB_TXUOUT2+	12
21 GPU_TXLCLKOUT-	R461	0	TXLCLKOUT-	R254	*0	NB_TXLCLKOUT-	12
21 GPU_TXLCLKOUT+	R463	0	TXLCLKOUT+	R251	*0	NB_TXLCLKOUT+	12
21 GPU_TXUCLKOUT-	R460	0	TXUCLKOUT-	R255	*0	NB_TXUCLKOUT-	12
21 GPU_TXUCLKOUT+	R462	0	TXUCLKOUT+	R252	*0	NB_TXUCLKOUT+	12
21 GPU_TXLOUT3-	R439	0	TXLOUT3-	R276	*0	NB_TXLOUT3-	12
21 GPU_TXLOUT3+	R441	0	TXLOUT3+	R272	*0	NB_TXLOUT3+	12
21 GPU_TXUOUT3-	R440	0	TXUOUT3-	R277	*0	NB_TXUOUT3-	12
21 GPU_TXUOUT3+	R442	0	TXUOUT3+	R273	*0	NB_TXUOUT3+	12

FOR EMI WEB CAM MODULE



Quanta Computer Inc.
 PROJECT : QUI

Size	Document Number	Rev
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11 PCIE_TXP[15..0] << PCIE_TXP[15..0]
 11 PCIE_TXN[15..0] << PCIE_TXN[15..0]

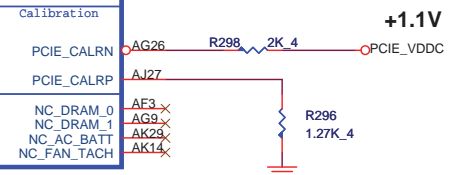
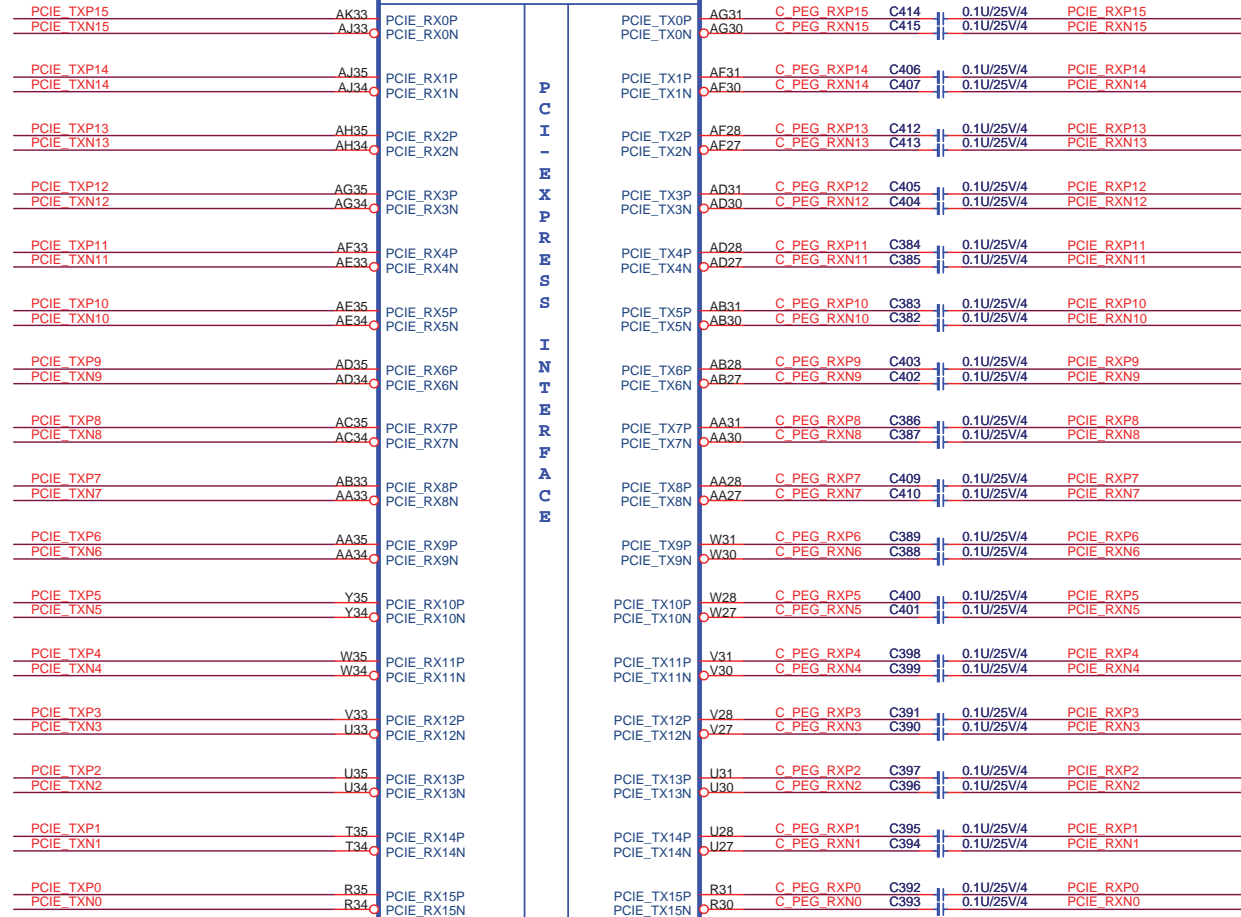
11 PCIE_RXP[15..0] >> PCIE_RXP[15..0]
 11 PCIE_RXN[15..0] >> PCIE_RXN[15..0]

U17A

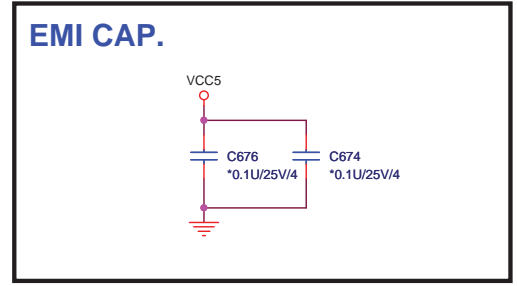
PART 1 OF 7

P
C
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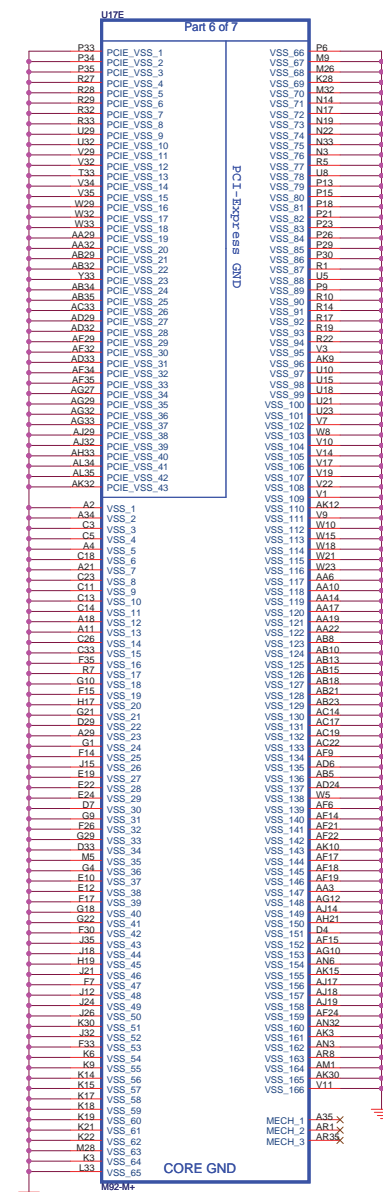
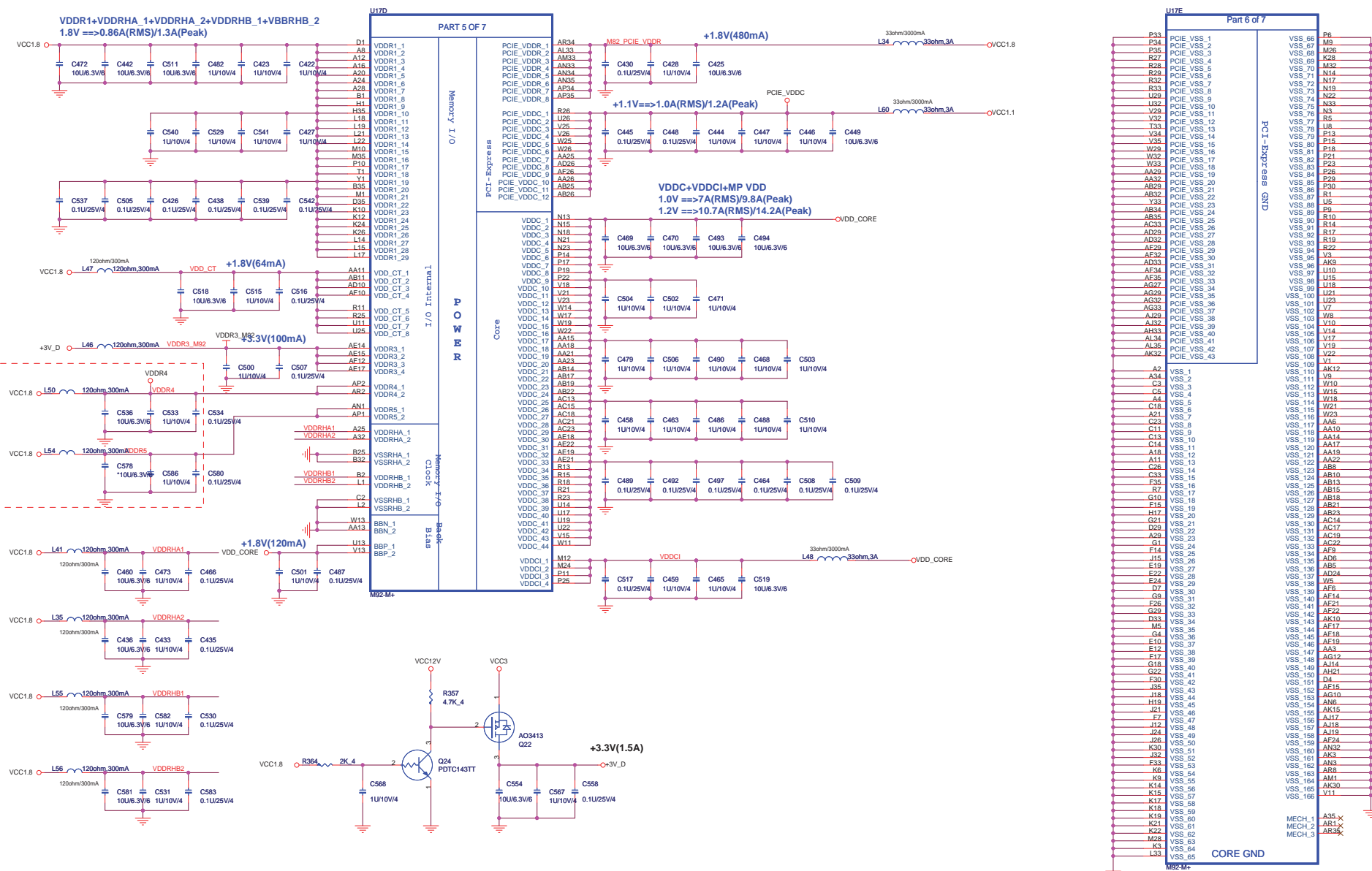


M92-M+ Quantat Lenovo
 M82-M AJ072800T16 AJ072800T17
 AJ070700T13 AJ070700T12



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 PROJECT : QJ1

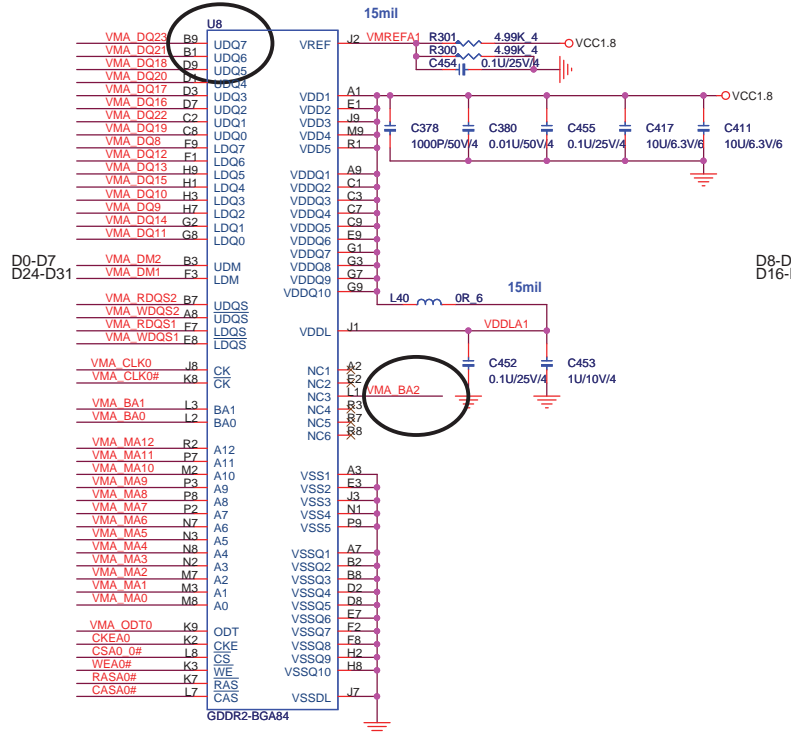
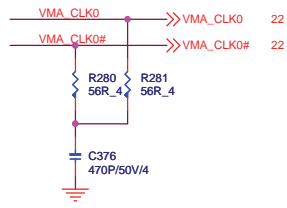
Size	Document Number	Rev
	M82-M PCI-E	A
Date:	Saturday, February 21, 2009	Sheet 20 of 44



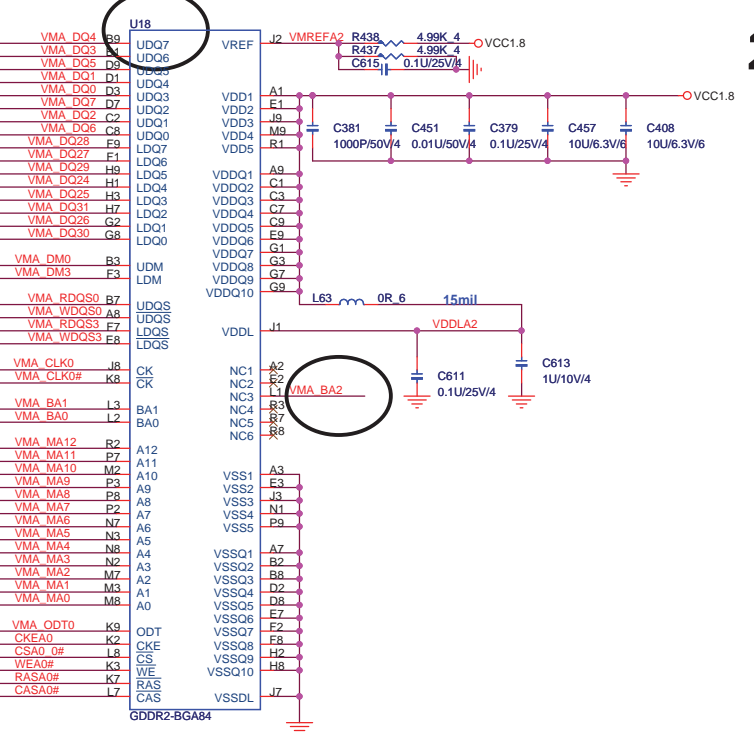
Channel A-1

- 22 VMA_DQ[63..0] >> VMA_DQ[63..0]
- 22 VMA_DM[7..0] >> VMA_DM[7..0]
- 22 VMA_RDQS[7..0] >> VMA_RDQS[7..0]
- 22 VMA_WDQS[7..0] >> VMA_WDQS[7..0]
- 22 VMA_MA[12..0] >> VMA_MA[12..0]

- VMA_ODT0 >> VMA_ODT0 22
- CKEA0 >> CKEA0 22
- CSA0_0# >> CSA0_0# 22
- WEA0# >> WEA0# 22
- RASA0# >> RASA0# 22
- CASA0# >> CASA0# 22



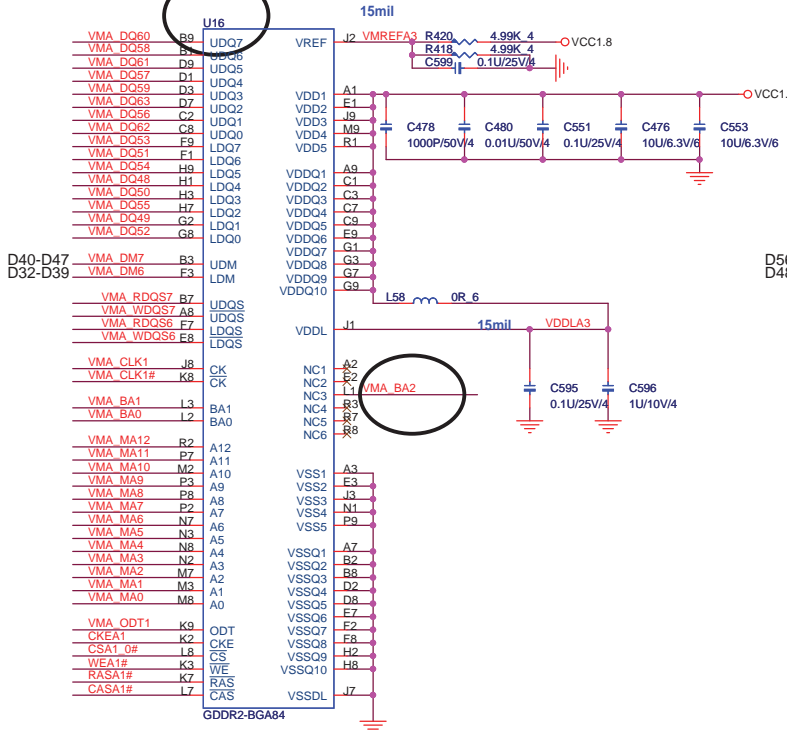
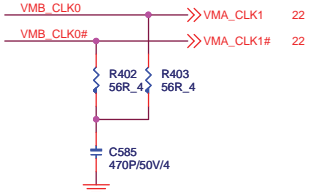
D8-D15
D16-D23



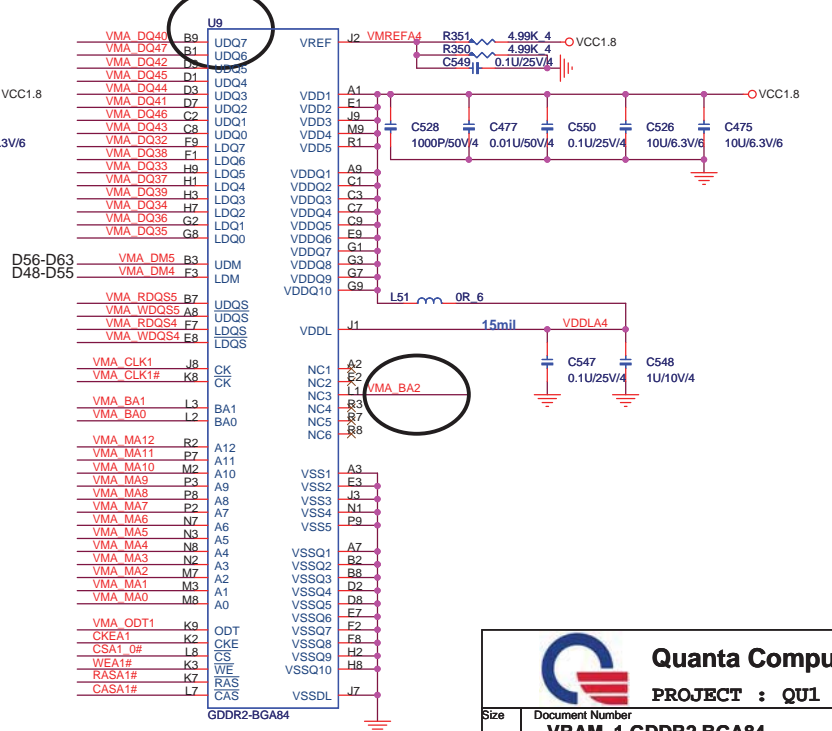
12/17 change U8,U9,U16,U18 (P/N:AKD5FG-TW03) (VRAM change to 400MHZ)

Channel B-1

- 22 VMA_ODT1 >> VMA_ODT1 22
- 22 CKEA1 >> CKEA1 22
- 22 CSA1_0# >> CSA1_0# 22
- 22 WEA1# >> WEA1# 22
- 22 RASA1# >> RASA1# 22
- 22 CASA1# >> CASA1# 22



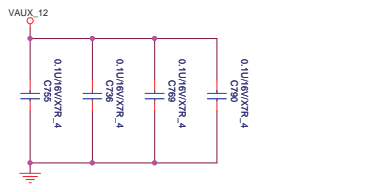
D40-D47
D32-D39



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PROJECT : QUL

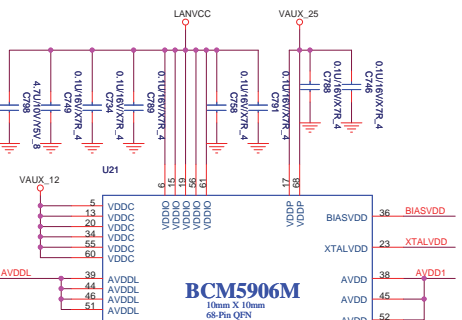
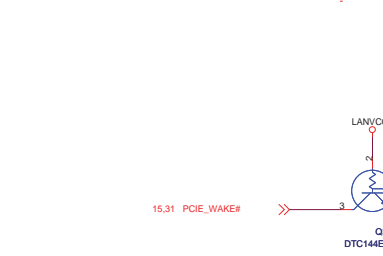
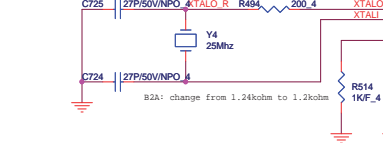
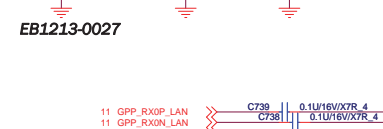
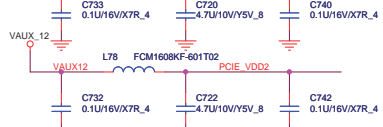
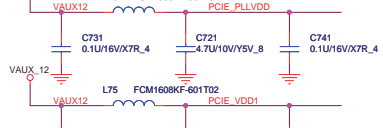
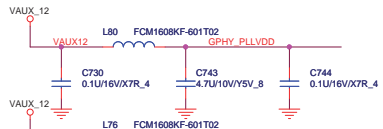
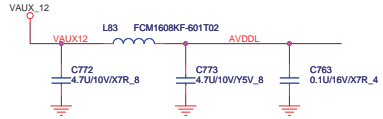
Size Document Number
VRAM_1 GDDR2 BGA84 Rev A

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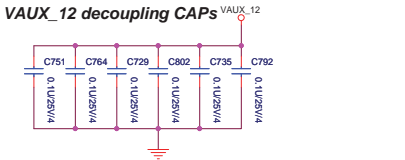
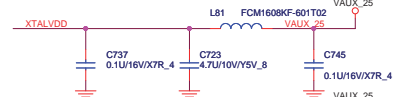


VDDC+AVDLL+GPHY_PLLVDD+PCIE_VDD+PCIE_PLLVDD==>375mA

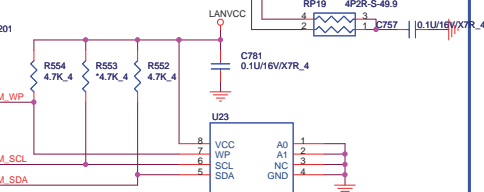
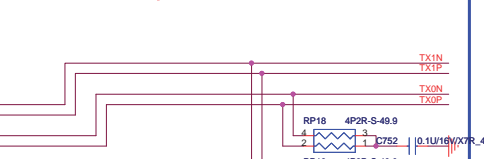
AVDD+VDDP+XTALVDD+BIASVDD==>90mA



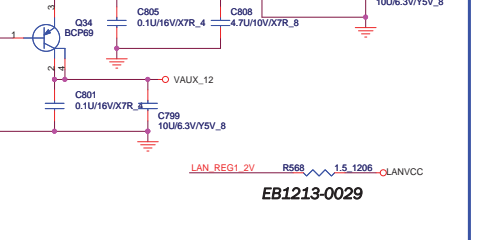
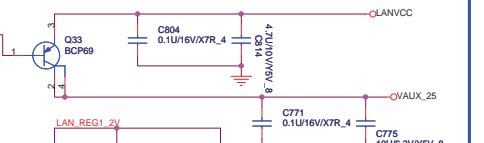
BCM5906M
10mm X 10mm
68-Pin QFN



VAUX_12 decoupling CAPS



Broadcom recommended cost down solution



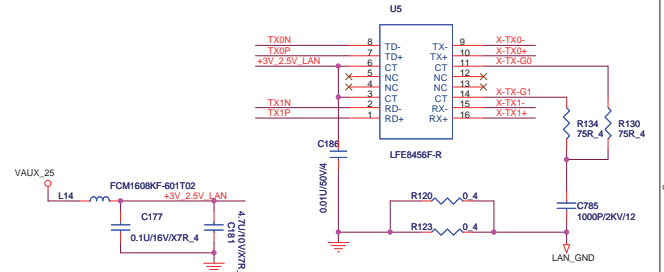
LANVCC



LAN Power 15mils(331mA)

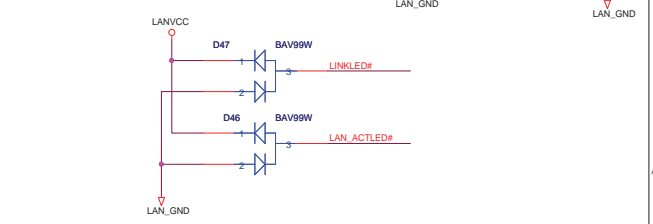
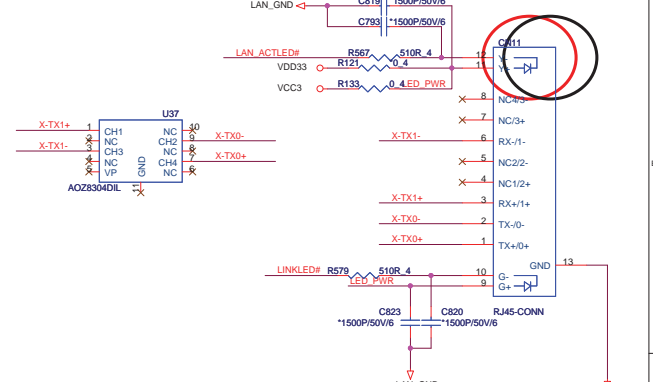
WIDE TRACE

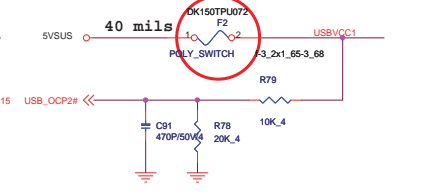
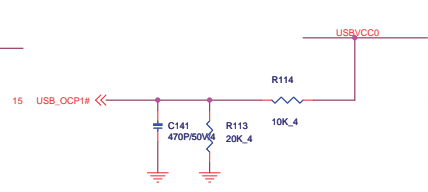
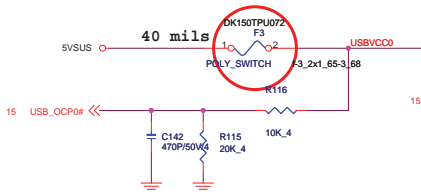
10/100 Transformer



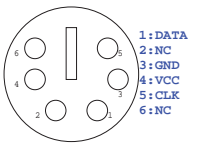
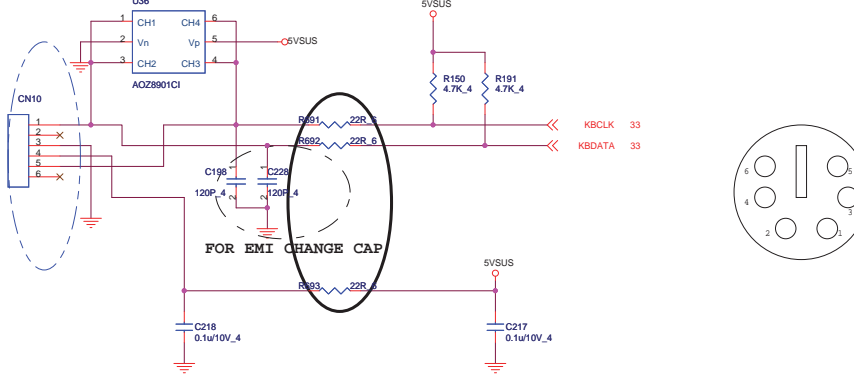
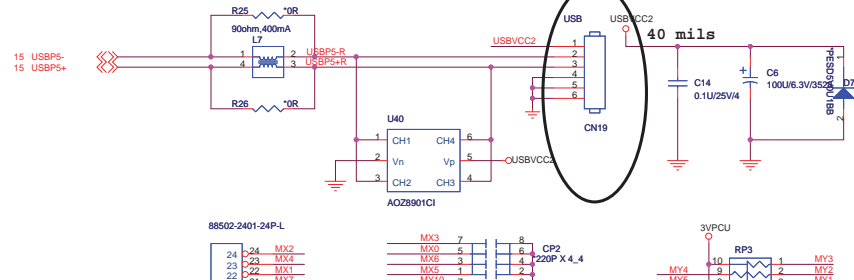
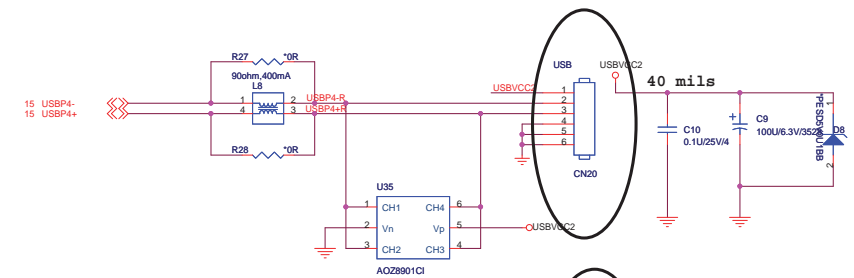
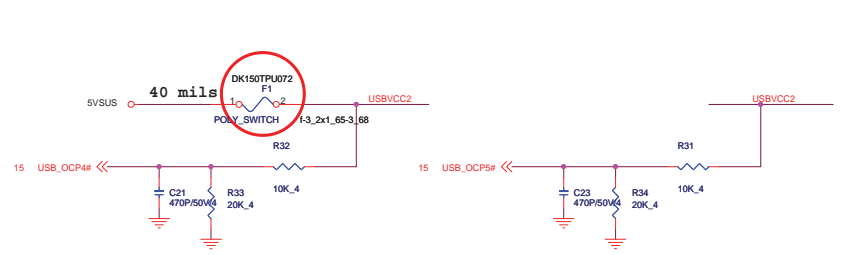
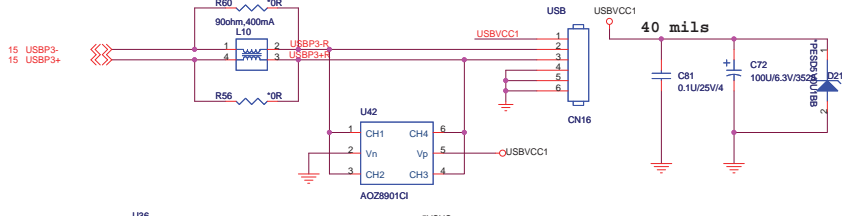
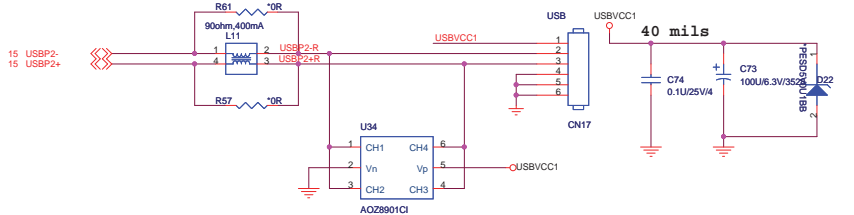
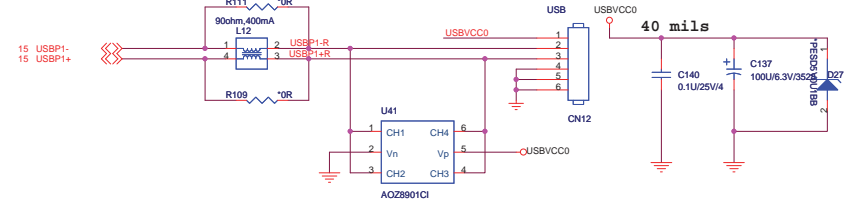
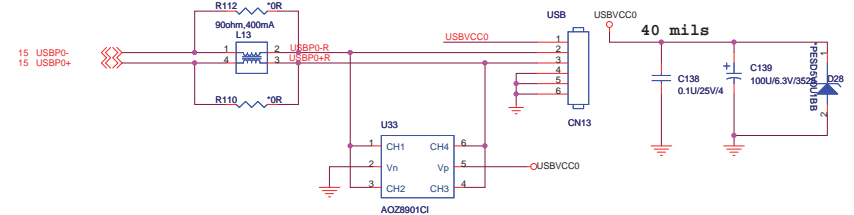
RJ45

12/23 del R587(LAN link issue)
EB1213-0030
12/05 Layout update the CN11 Footprint
12/29 R26 change CN11 (P/N:DFTJ12FS001)(Change LED color)





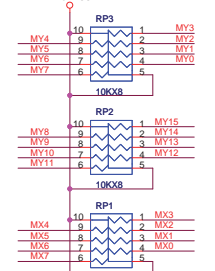
12/01 change F1,F2,F3 P/N (DK150TPU072) and footprint (f-3_2x1_65-3_68)

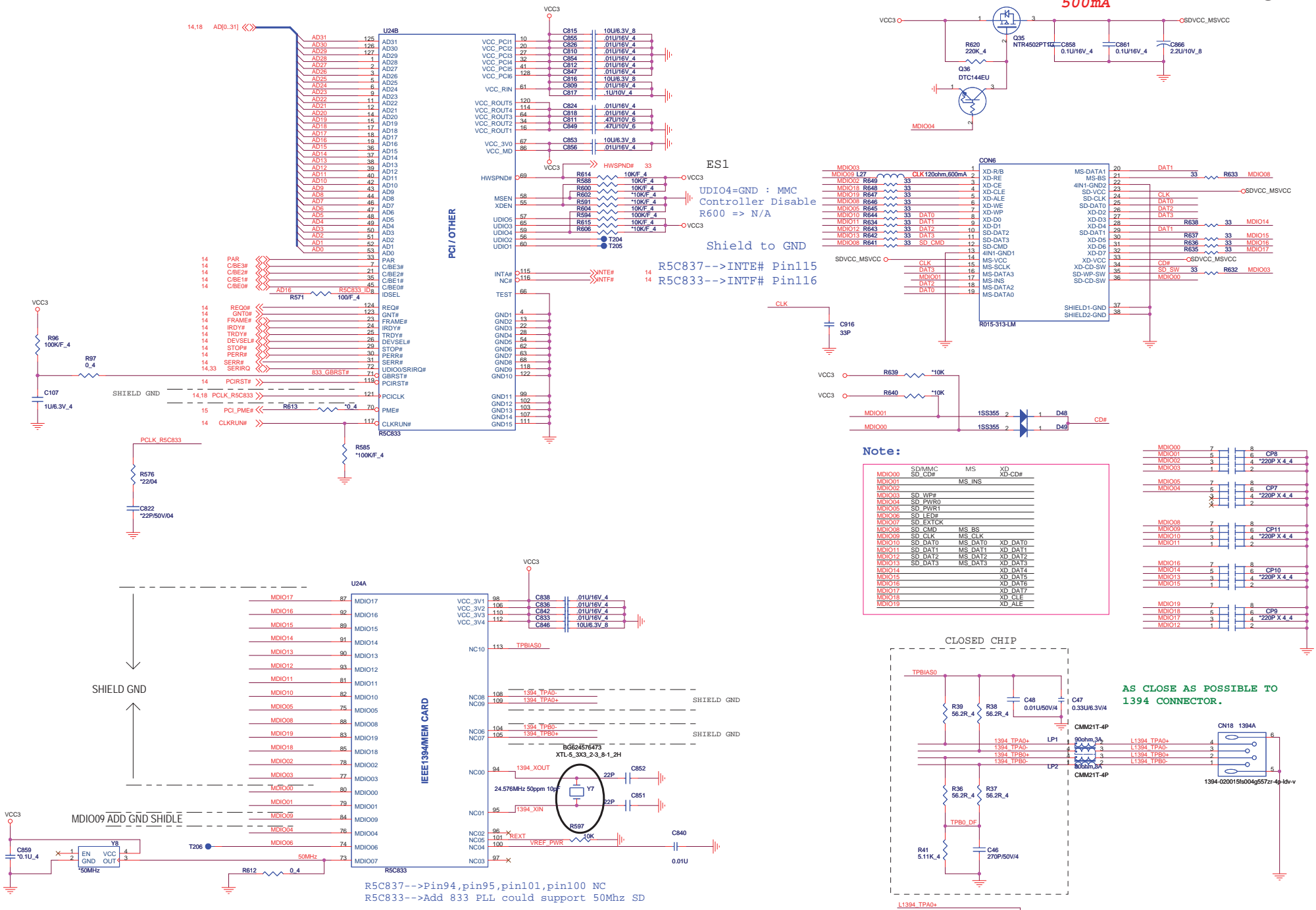


88502-2401-24P-L

24	MX2	8
23	MX4	8
22	MX1	8
21	MX7	8
20	MX3	8
19	MX0	8
18	MX6	8
17	MX5	8
16	MX4	8
15	MY1	8
14	MY3	8
13	MY6	8
12	MY5	8
11	MY7	8
10	MY8	8
9	MY9	8
8	MY10	8
7	MY13	8
6	MY12	8
5	MY11	8
4	MY14	8
3	MY15	8
2	MY13	8
1	MY15	8

MX3	7	8
MX0	6	8
MX6	3	8
MX5	1	8
MX7	7	8
MX4	5	8
MX1	3	8
MX0	1	8
MX6	7	8
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MX4	5	8
MX1	3	8
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MX0	1	8





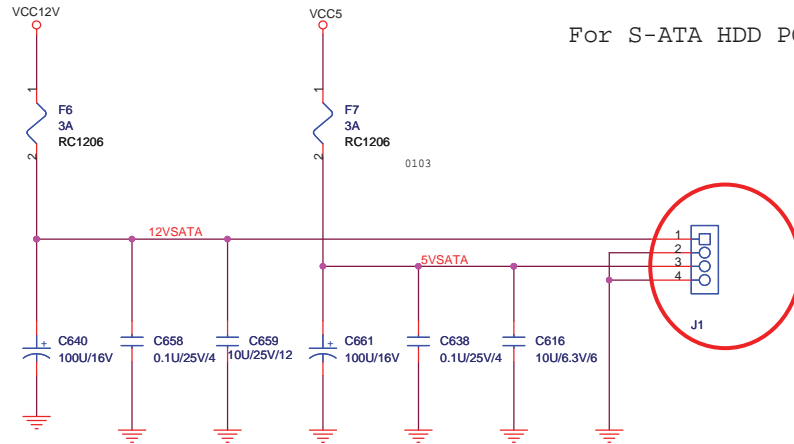
Quanta Computer Inc.
PROJECT : Q01

Size Document Number
R5C833 / 1394

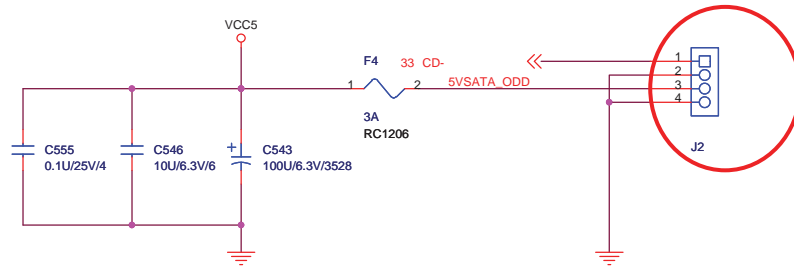
Date: Saturday, February 21, 2009 Sheet 28 of 44

60 mils

For S-ATA HDD POWER

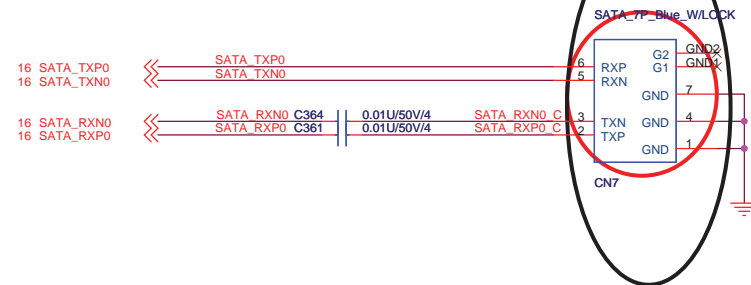


12/02 change J1,J2 PN:DFHS04FR207

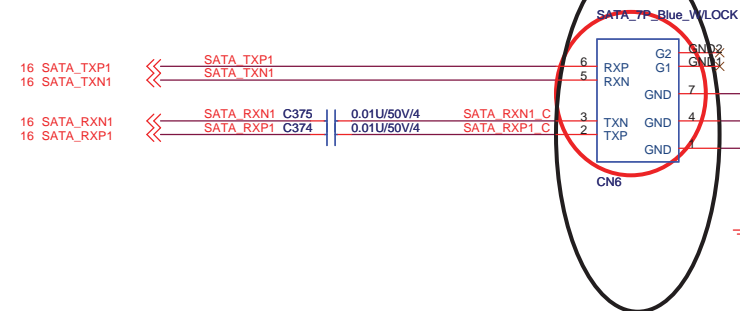


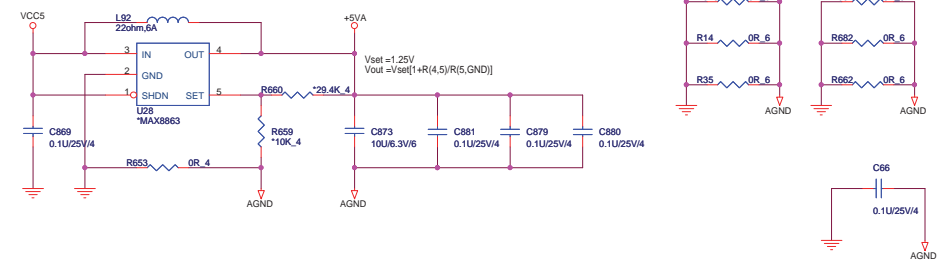
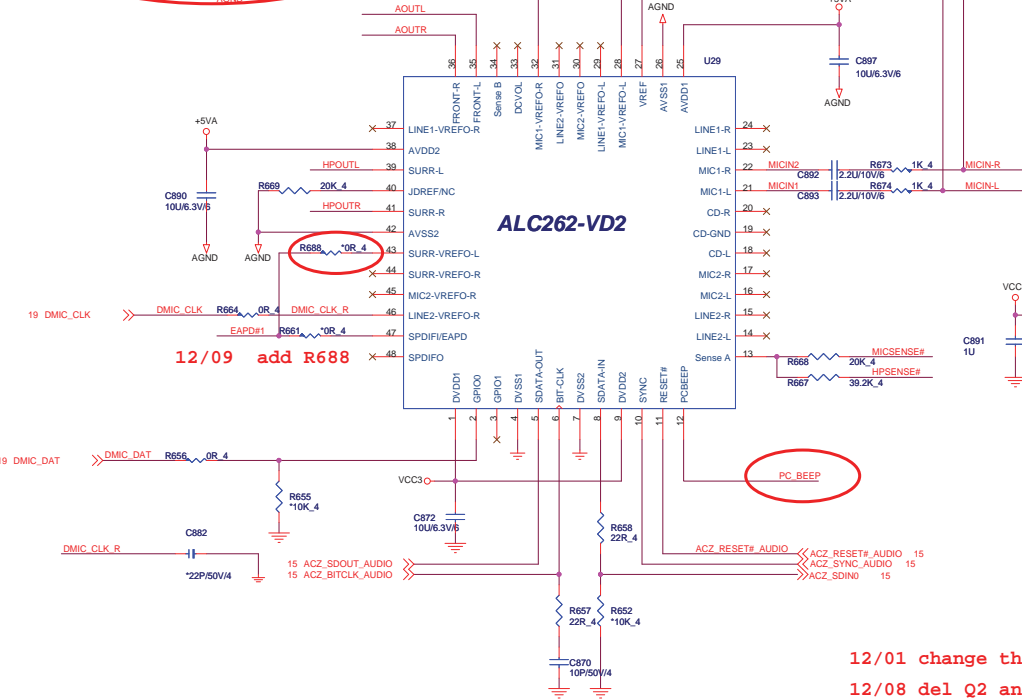
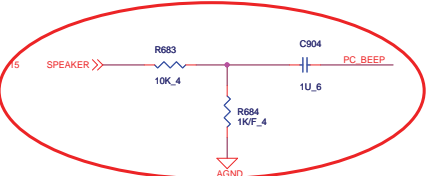
12/05 change CN6,CN7 Footprint sata-aba-sat-010-k07-7p-r

SATA HDD CONNECTOR

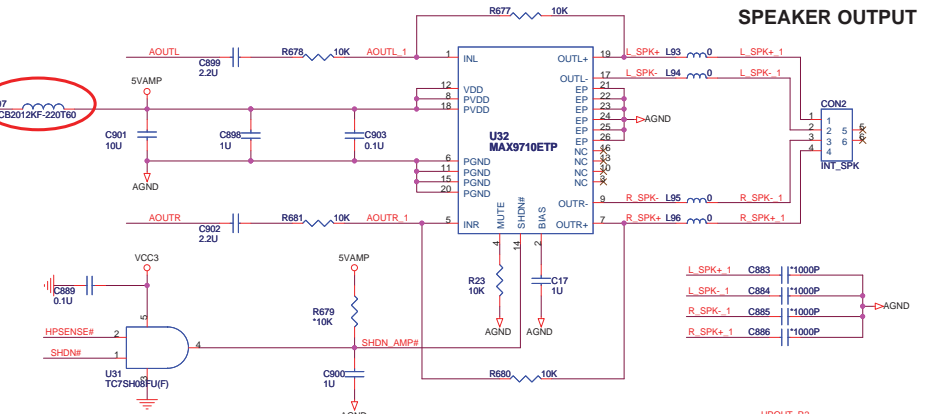


SATA ODD CONNECTOR

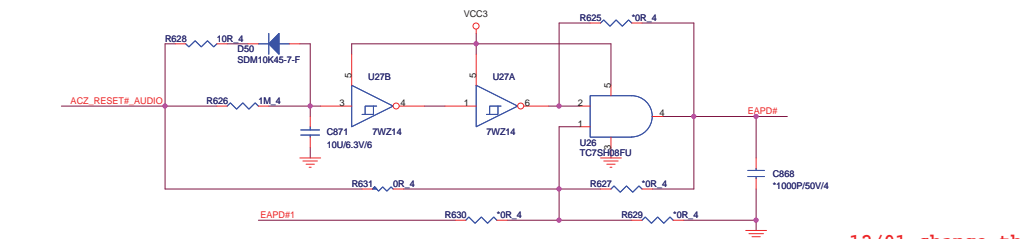
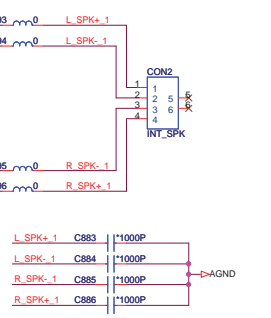




AUDIO AMPLIFIER

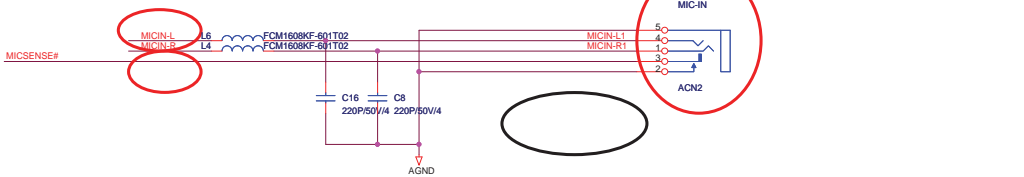


SPEAKER OUTPUT



12/01 change the footprint to SOT23_213-3_3-2
 12/08 del Q2 and R16

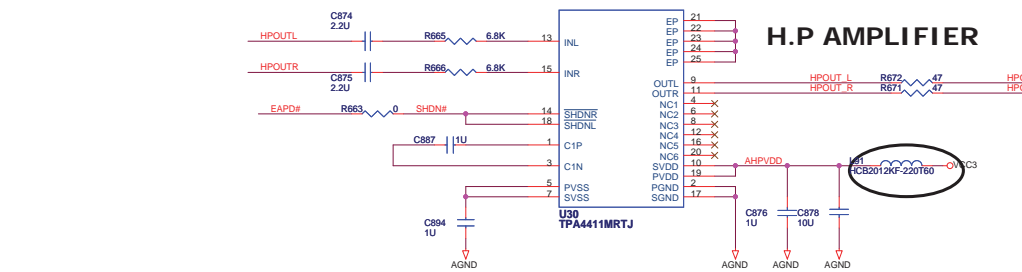
MIC-IN



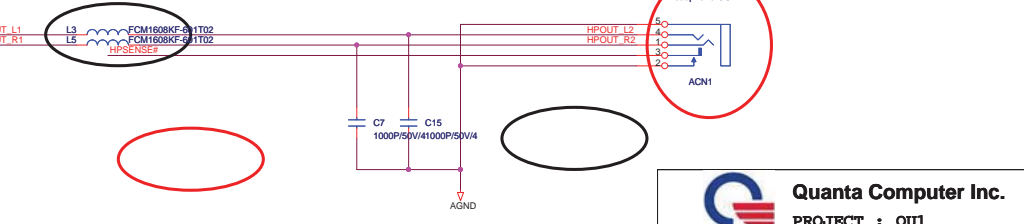
12/01 change the footprint to SOT23_213-3_3-2

12/08 Change ACN1, ACN2 P/N and Footprint

H.P AMPLIFIER



Headphone-OUT

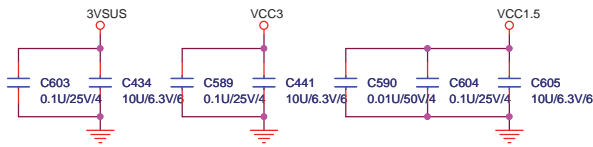
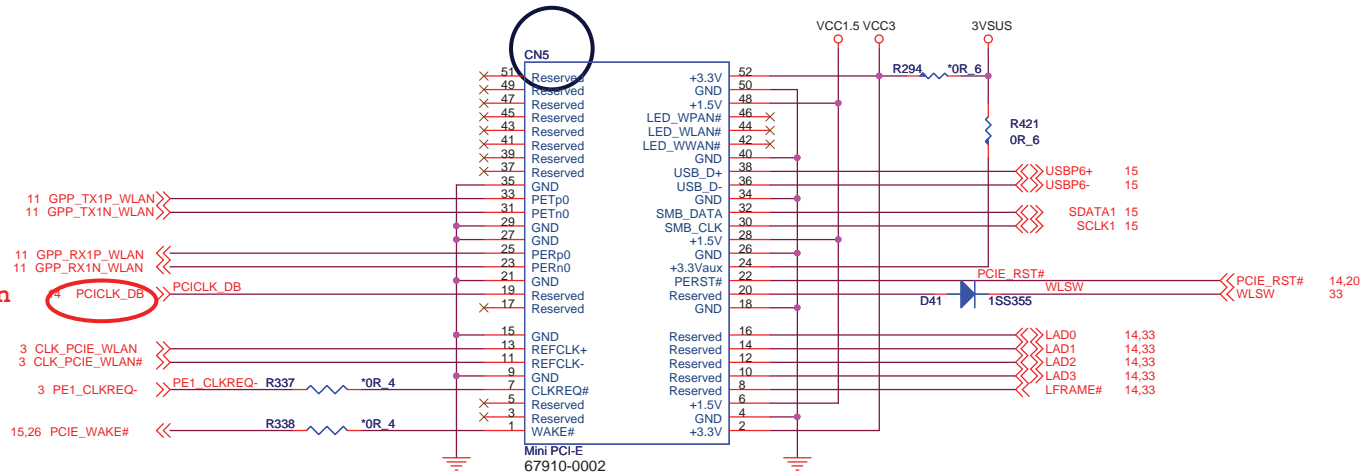


12/08 del Q3 and R18

Mini Card (WLAN)

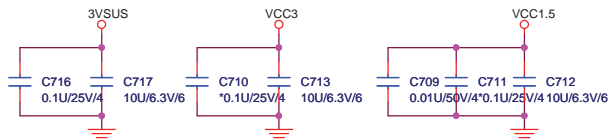
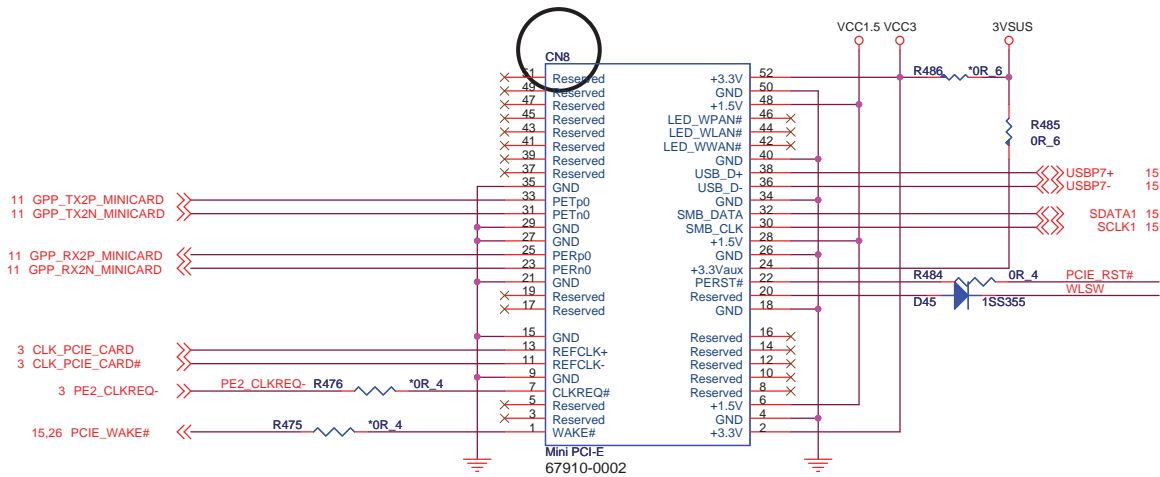
12/26 change CN5,CN8 P/N to meet ACL.(DFHD52MS057)

12/04 ADD debug port function

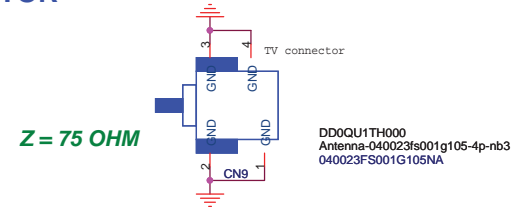


Mini Card (TV Card)

12/26 change CN5,CN8 P/N to meet ACL.(DFHD52MS057)

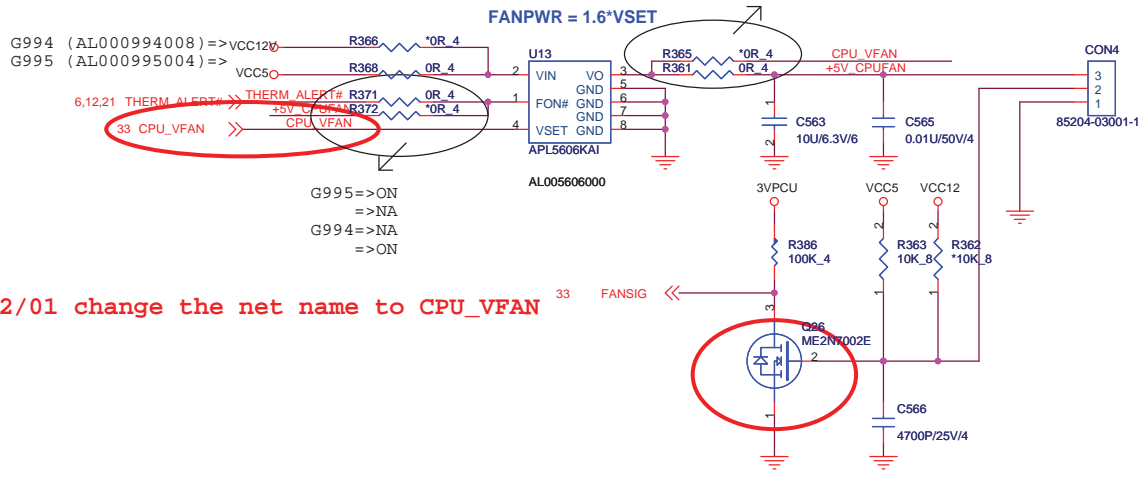


TV ANTENNA CONNECTOR
ANT. CONNECTOR



FAN CONN

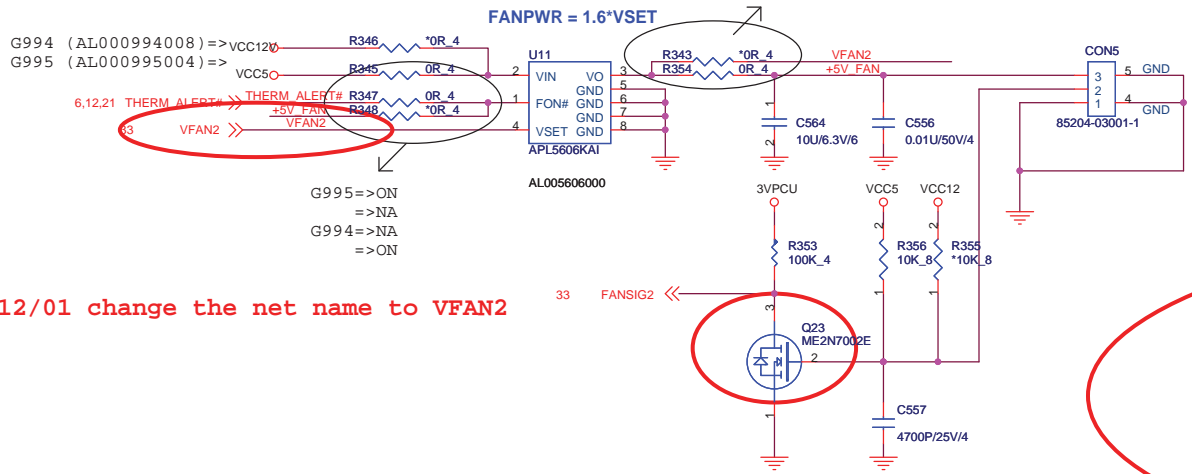
G994=> ON
=> NA
G995=> NA
=> ON



12/01 change the net name to CPU_VFAN

12/01 change the footprint to SOT23_213-3_3-2

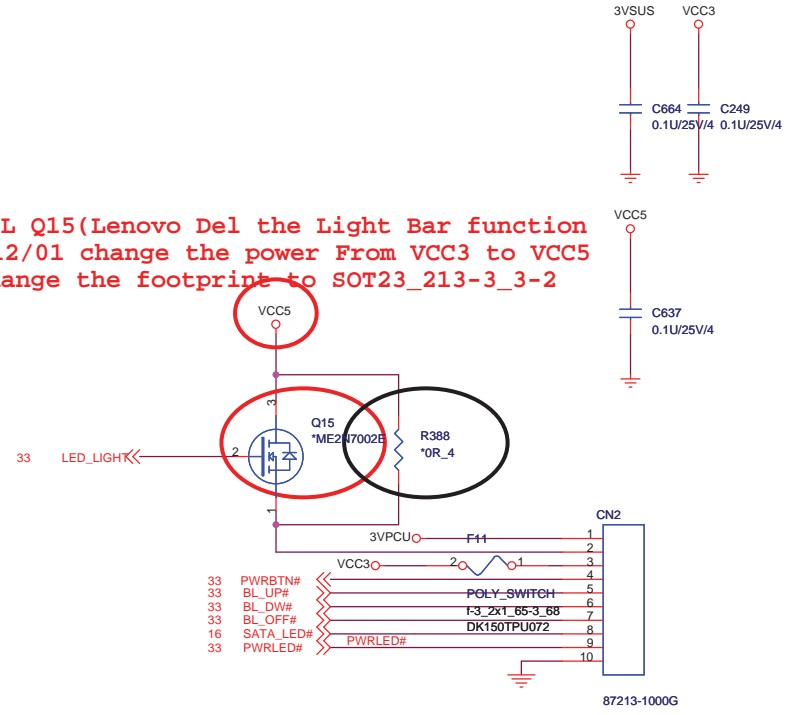
G994=> ON
=> NA
G995=> NA
=> ON



12/01 change the net name to VFAN2

12/01 change the footprint to SOT23_213-3_3-2

12/01 DEL Q15(Lenovo Del the Light Bar function)
12/01 change the power From VCC3 to VCC5
12/01 change the footprint to SOT23_213-3_3-2



12/01 del U1,Q1,Q3,R13,C11,R21,R11,R29

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

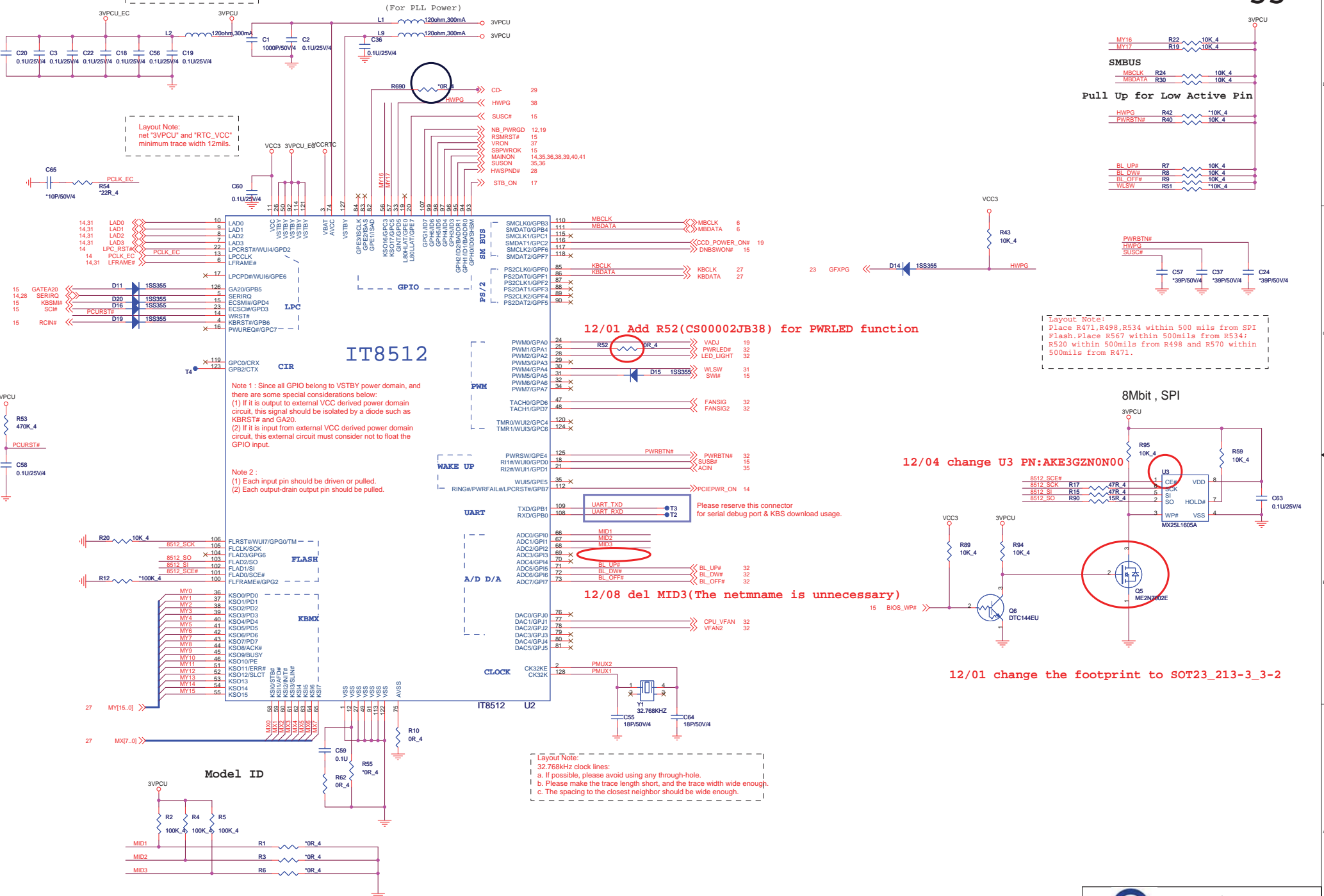
Layout Note:
Place R471,R498,R534 within 500mils from SPI
Flash. Place R557 within 500mils from R534;
R520 within 500mils from R498 and R570 within
500mils from R471.

12/01 Add R52(C500002JB38) for PWLED function

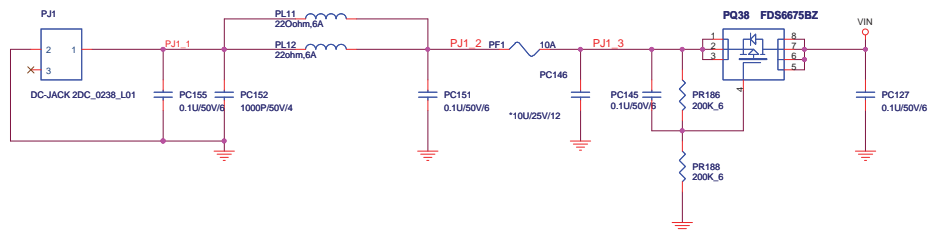
12/04 change U3 PN:AKE3GZNN00

12/08 del MID3(The netname is unnecessary)

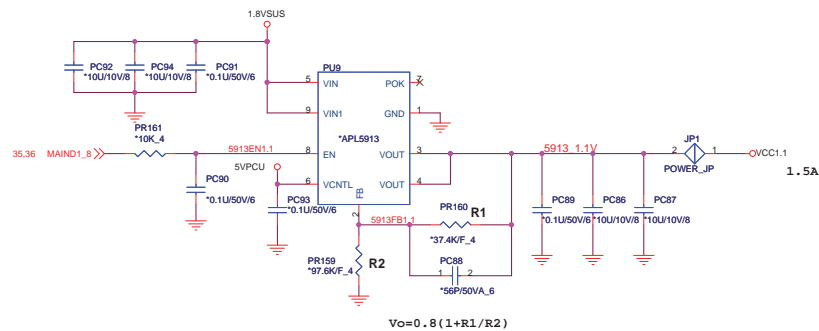
12/01 change the footprint to SOT23_213-3-3-2

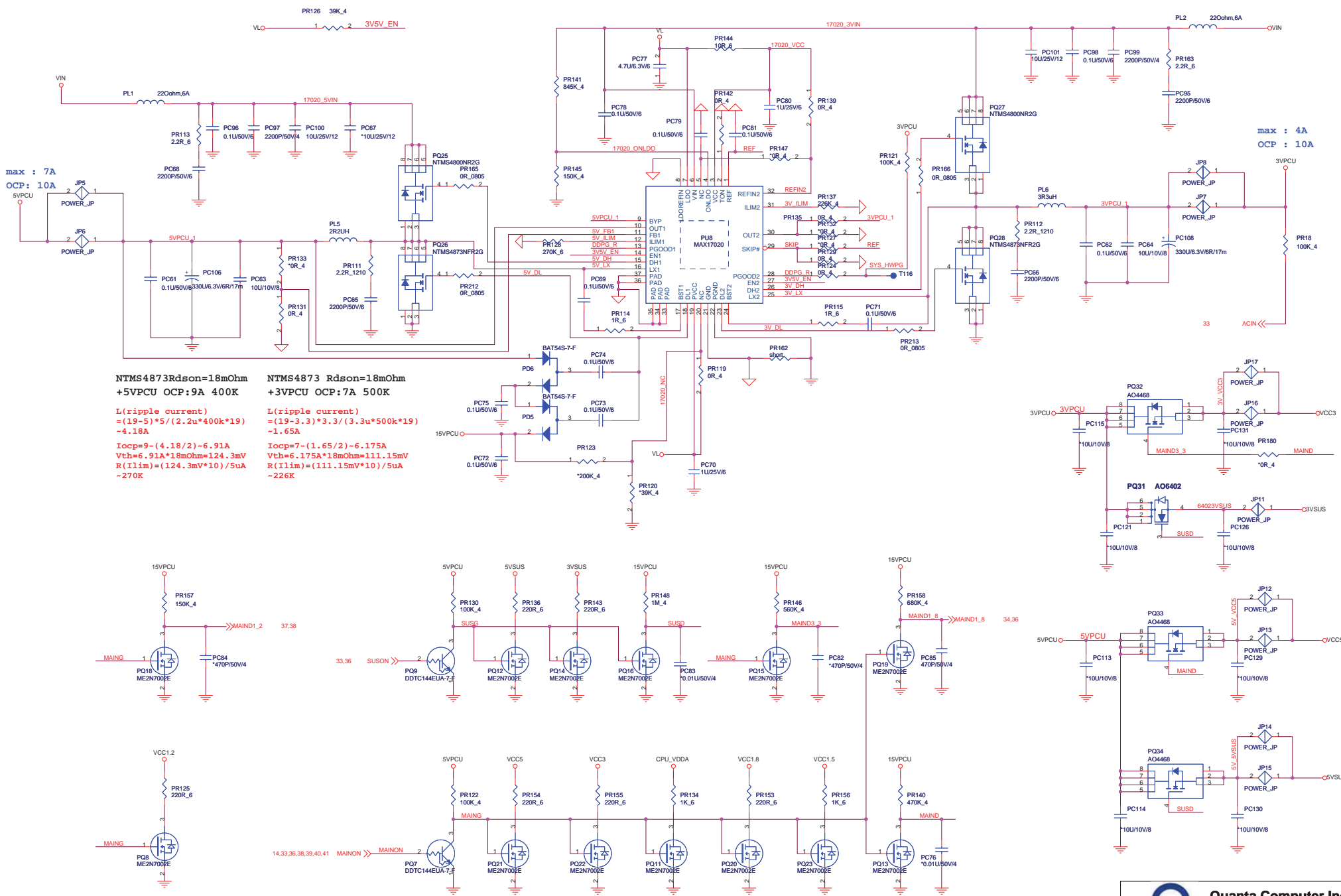


ACIN



+1.1V

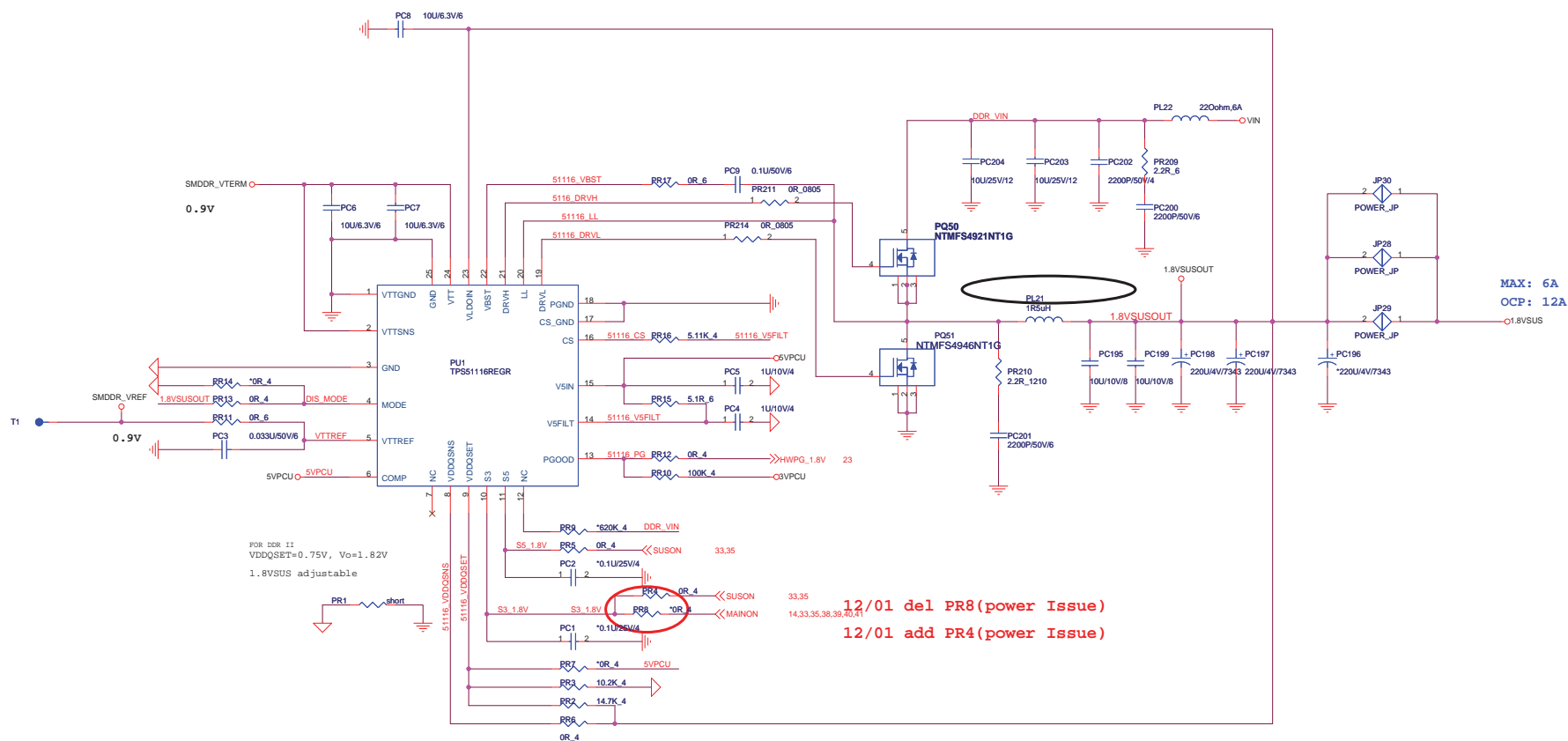




max : 4A
OCP : 10A

NTMS4873Rdson=18mOhm
+5VPCU OCP:9A 400K
L(ripple current)
=(19-5)*5/(2.2u*400k*19)
~4.18A
Iocp=9-(4.18/2)~6.91A
Vth=6.91A*18mOhm=124.3mV
R(ILim)=(124.3mV*10)/5uA
~220K

NTMS4873 Rdson=18mOhm
+3VPCU OCP:7A 500K
L(ripple current)
=(19-3.3)*3.3/(3.3u*500k*19)
~1.65A
Iocp=7-(1.65/2)~6.175A
Vth=6.175A*18mOhm=111.15mV
R(ILim)=(111.15mV*10)/5uA
~226K

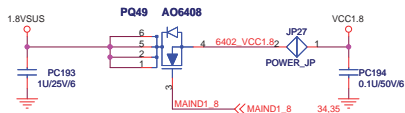


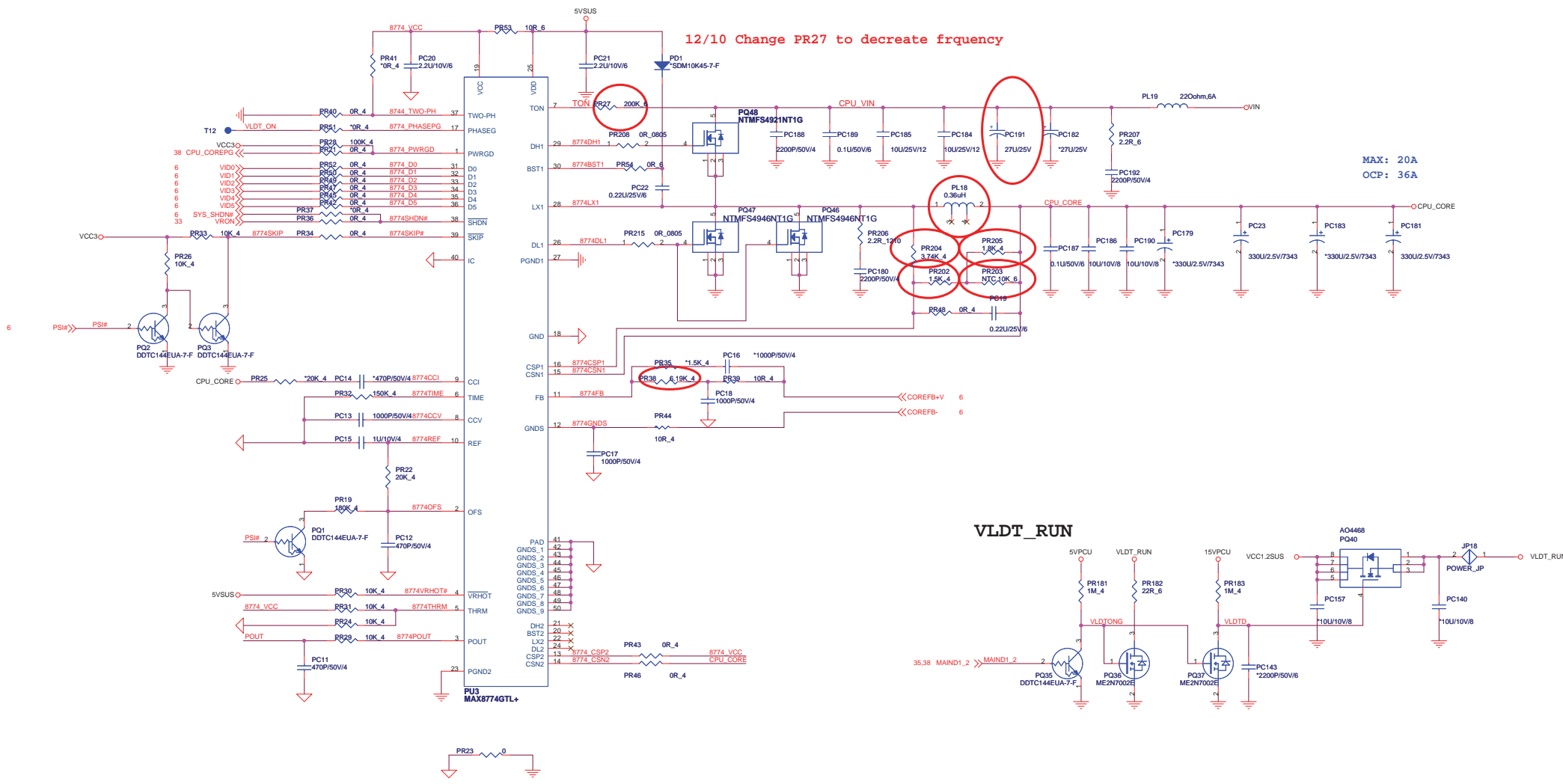
FOR DDR II
 VDDQSET=0.75V, Vo=1.82V
 1.8VSUS adjustable

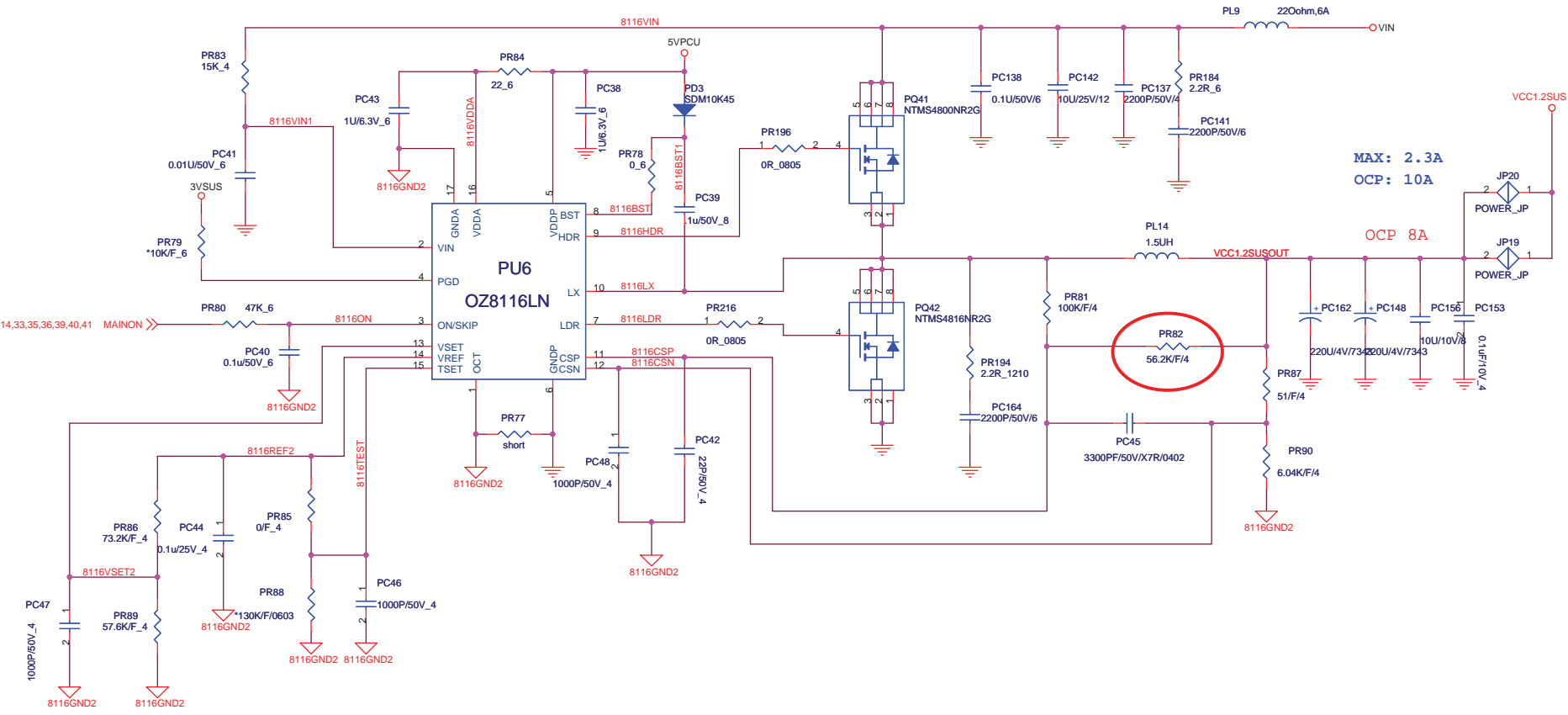
12/01 del PR8(power Issue)
 12/01 add PR4(power Issue)

NTMFS4946Rdson=3.8~4.6mOhm

L(ripple current)
 $= (19-1.8) * 1.8 / (1.5u * 400k * 19)$
 $\sim 2.72A$
 $4.6m * (12 - (2.72/2)) = RILIM * 10uA$
RILIM=5.11K
 $((10u * PR67) / Rdson) + (\Delta I / 2) = Iocp$



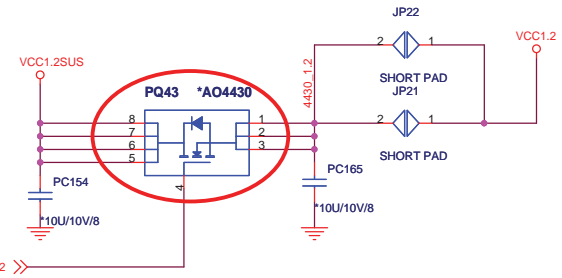




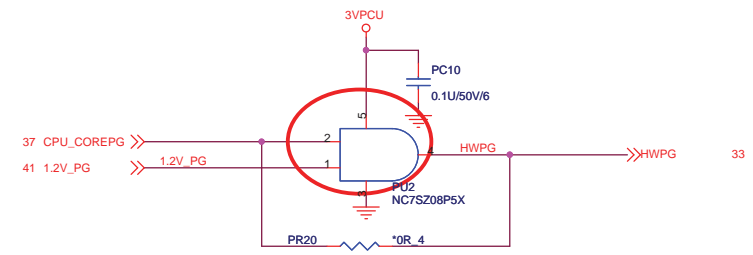
MAX: 2.3A
OCP: 10A

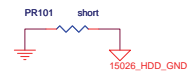
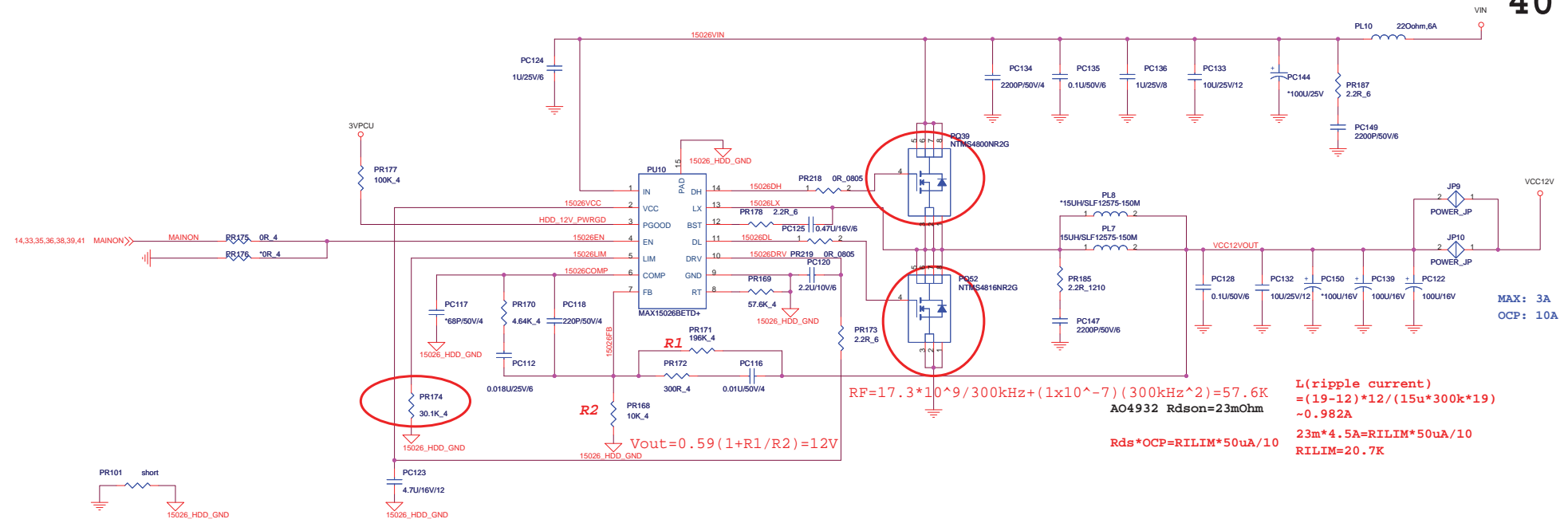
OCP 8A

12/01 del PQ43(Power Issue)

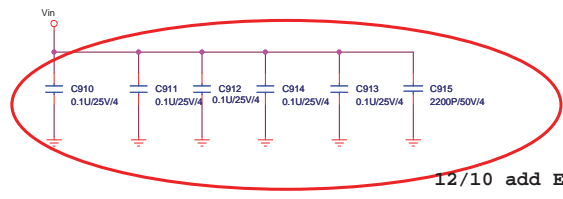
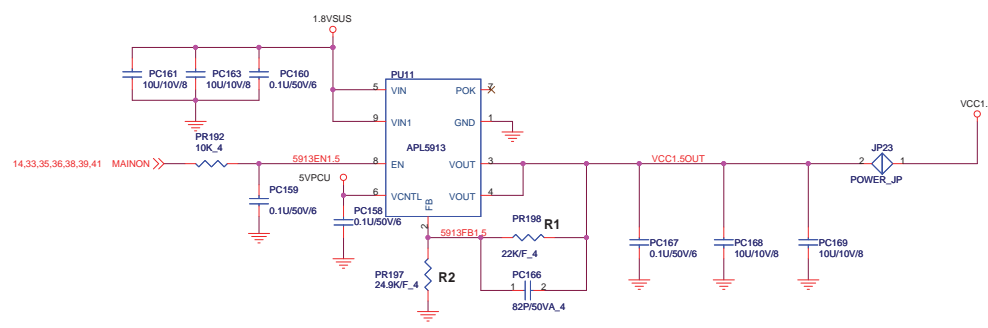


12/01 change PU2 p/n to AL17SZ08006(Buyer request)




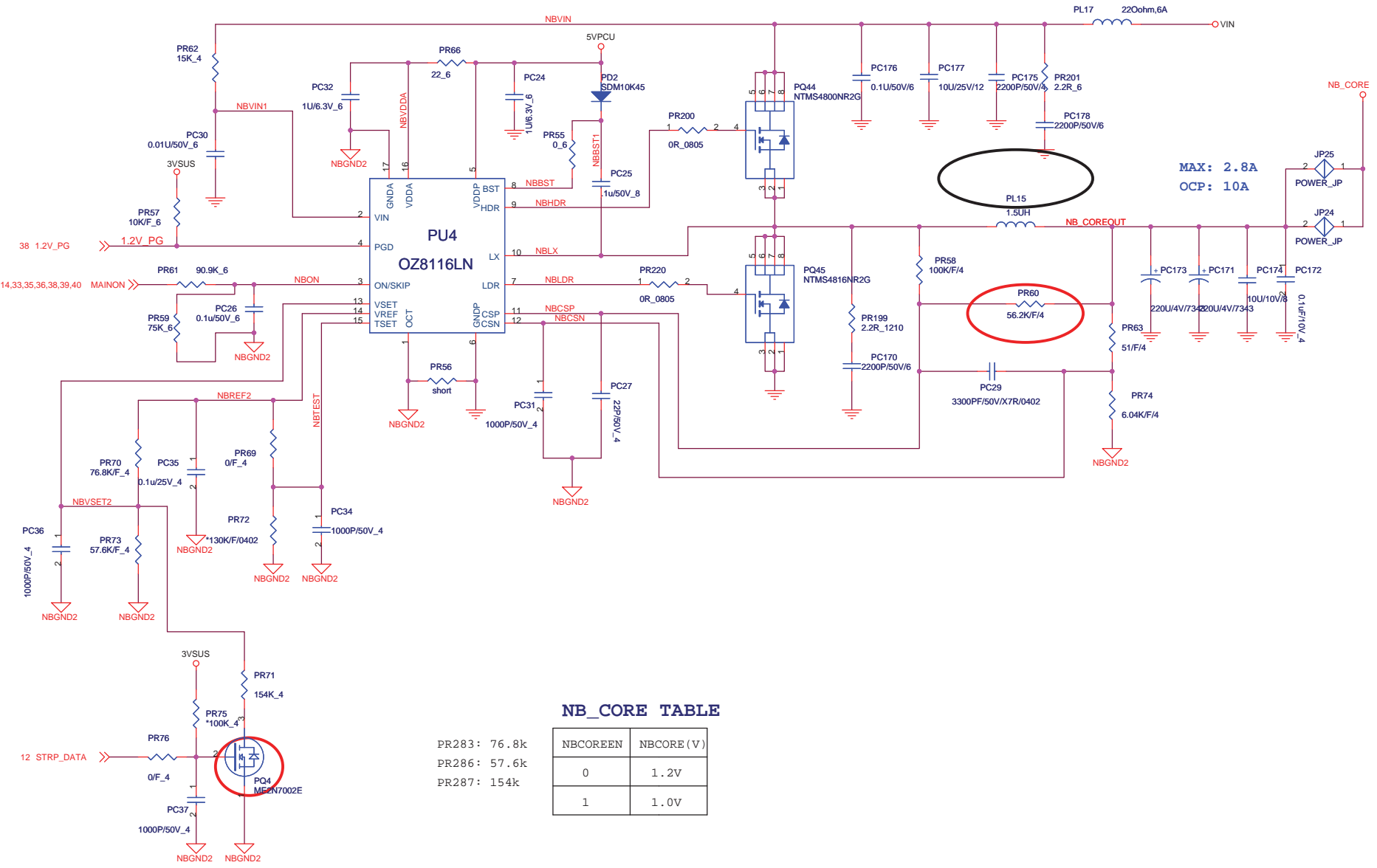


MINI CARD POWER



12/10 add EMI solution


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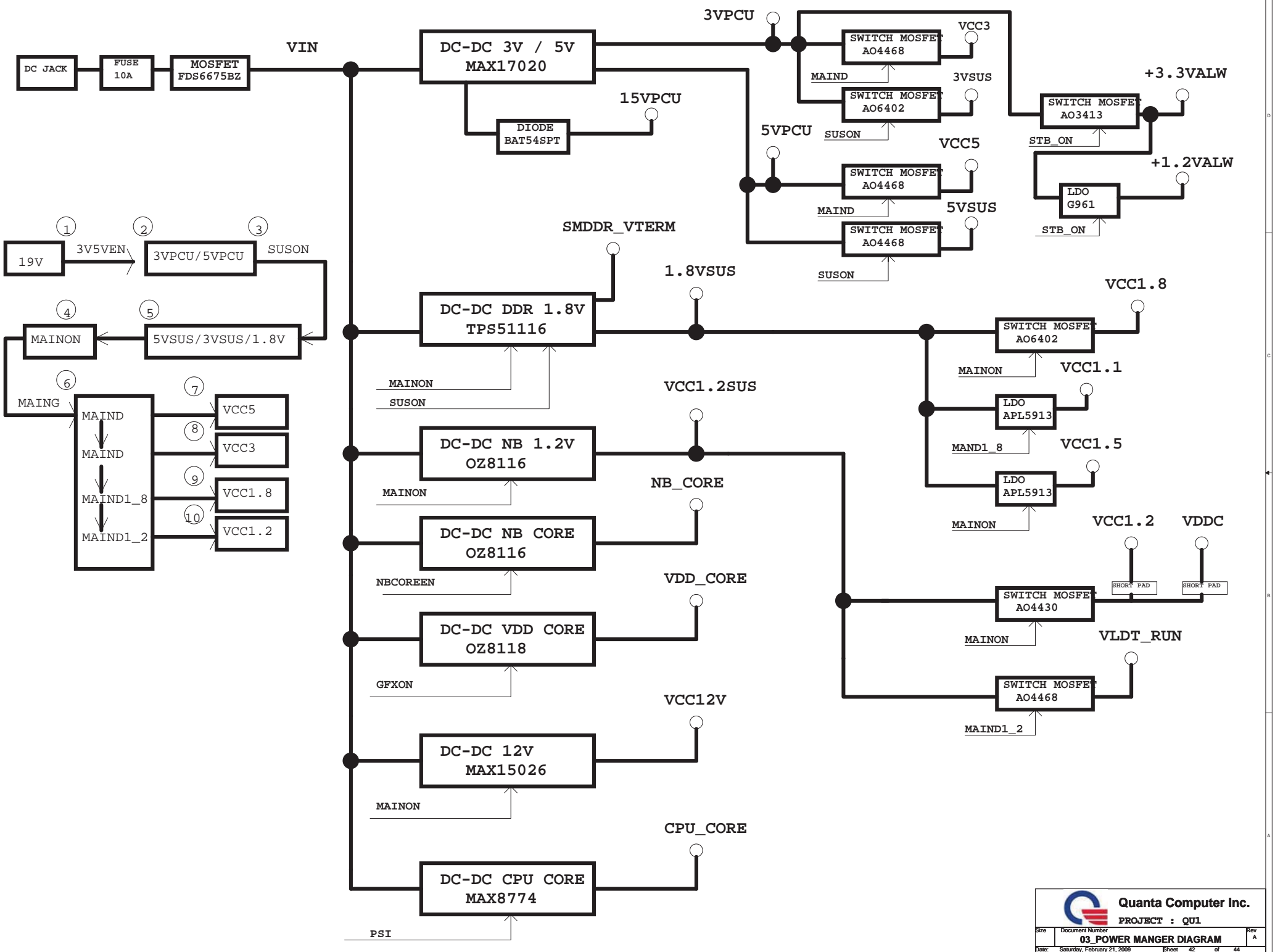
MAX: 2.8A
OCP: 10A

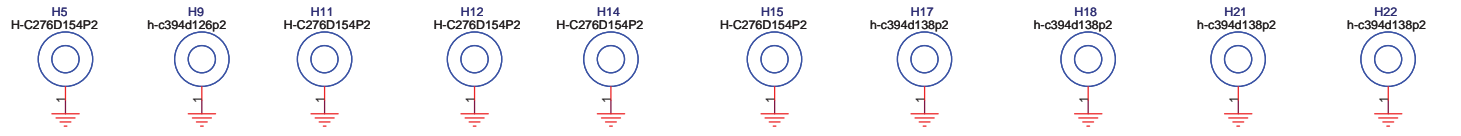
NB_CORE TABLE

NBCOREEN	NBCORE (V)
0	1.2V
1	1.0V

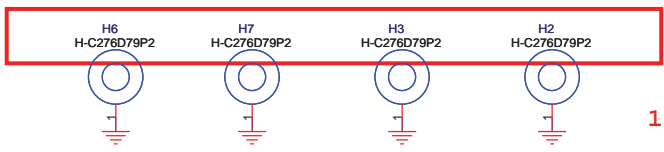
PR283: 76.8k
PR286: 57.6k
PR287: 154k

12/01 change the footprint to SOT23_213-3_2



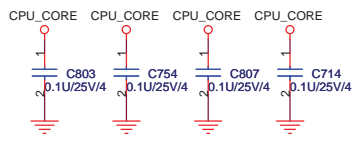
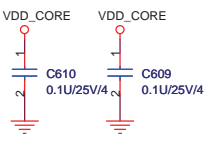
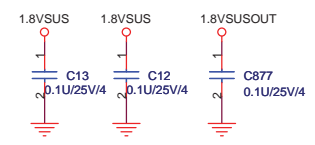
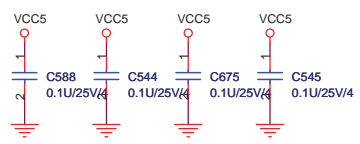
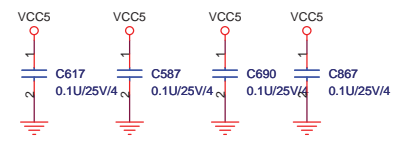
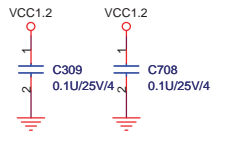
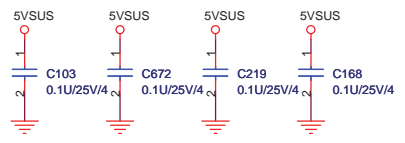
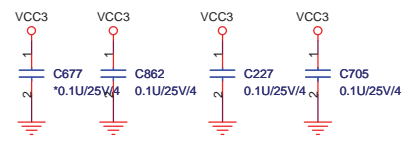
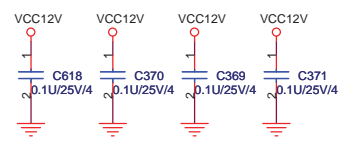
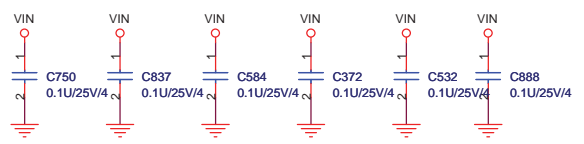
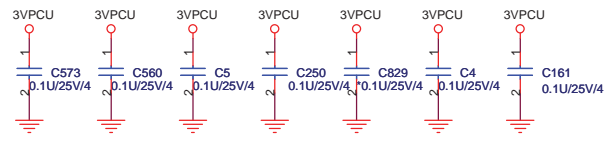



12/02 ME DEL H10 Location



12/02 change H2,H3,H6,H7 footprint to ????(waitting Layout team confirm)

12/02 change H5,H11,H12,H14,H15 footprint to ???(waitting Layout team confirm)



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