Compal Confidential

QIWG7 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13P-GL

2011-12-28

LA-7983P

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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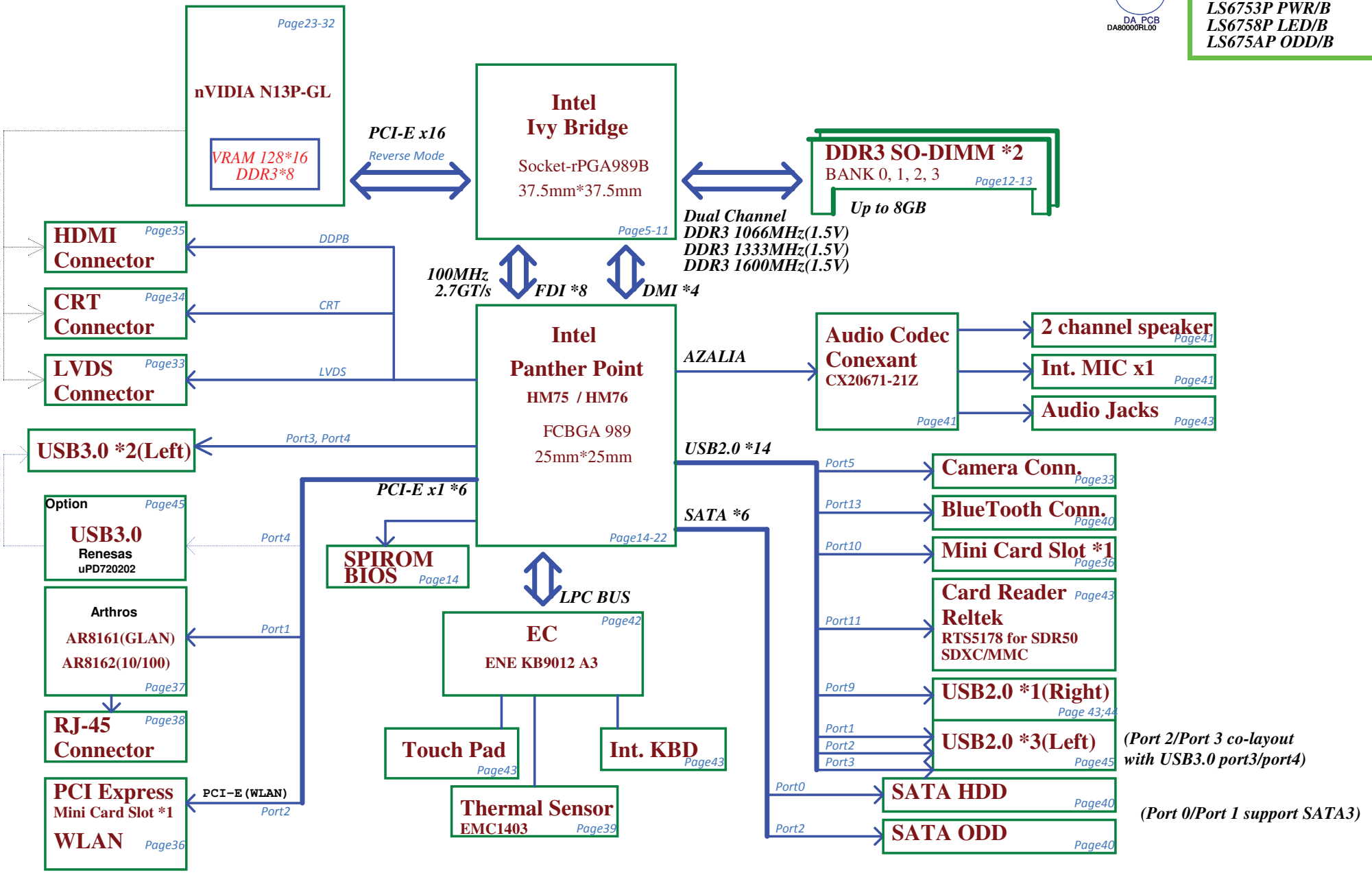
Title: Cover Page		
Size: Custom	Document Number: LA-7983P	Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 1 of 60	

ZZZ
LA7983
DA_PCB
DA80000RL00

LS7988P CR_AUDIO/B
LS7987P USB/B
LS6753P PWR/B
LS6758P LED/B
LS675AP ODD/B



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Title: Block Diagram

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 2 of 60

Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Left Side) USB2.0
	UHCI1	2	USB Port (Left Side) USB3.0
		3	USB Port (Left Side) USB3.0
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
UMA only	UMA@
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
Camera	CMOS@
Green Clock	GCLK@
	GCLK244@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

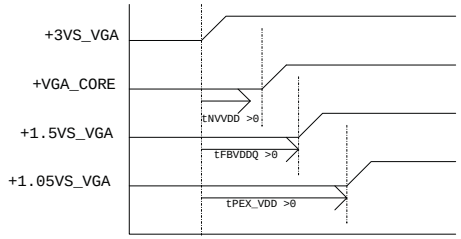
Size: B | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 3 of 60

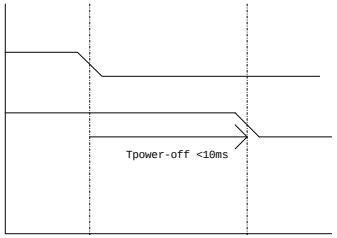
Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13P GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (MHz)	NVCLK /MCLK	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GL (28nm)	???

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL	Samsung 900MHz							
		64Mx16	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 900MHz							
		64Mx16	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 900MHz							
		128Mx16	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 900MHz							
		128Mx16	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

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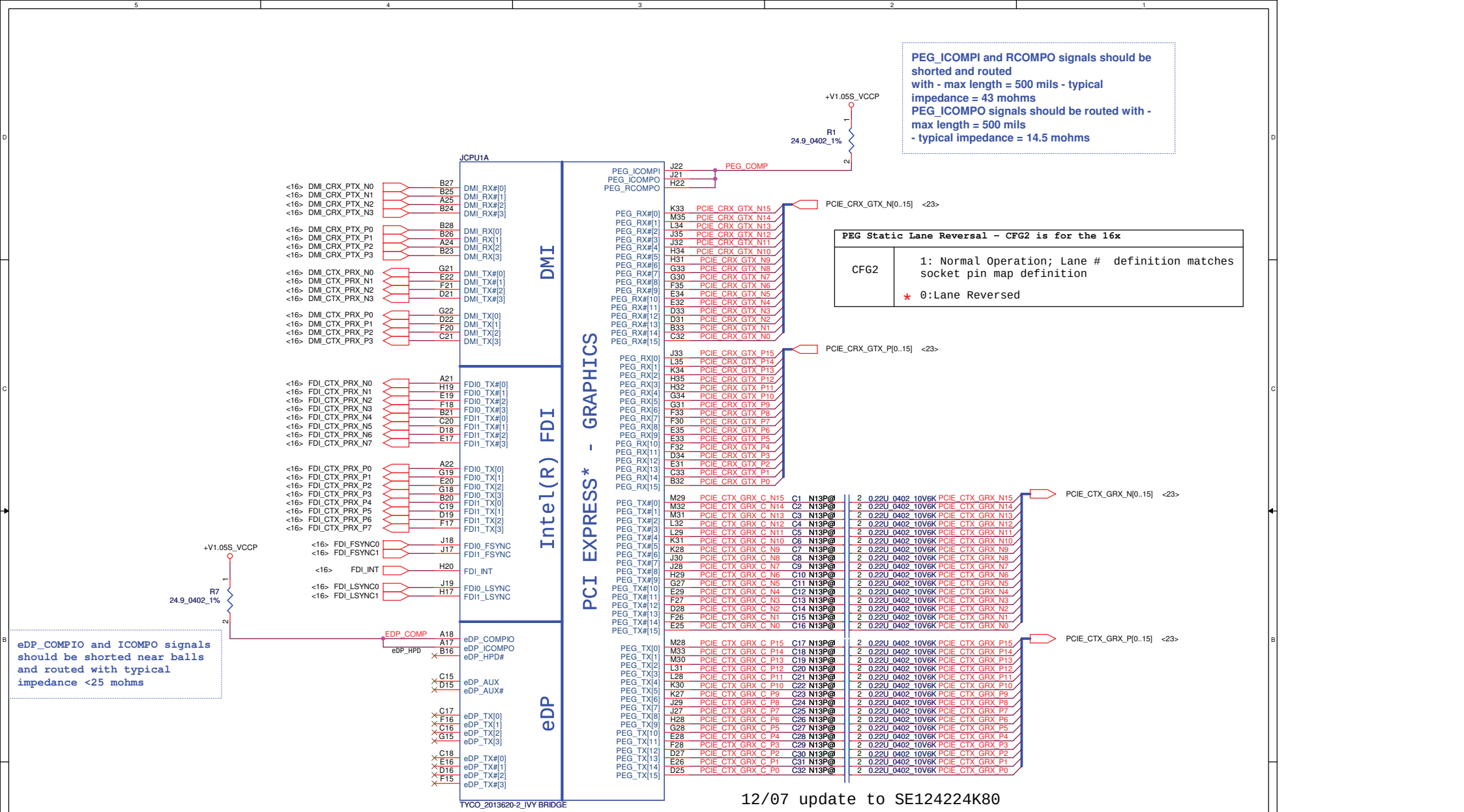
Title: VGA Notes List		
Size: Custom	Document Number: LA-7983P	Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 4 of 60	



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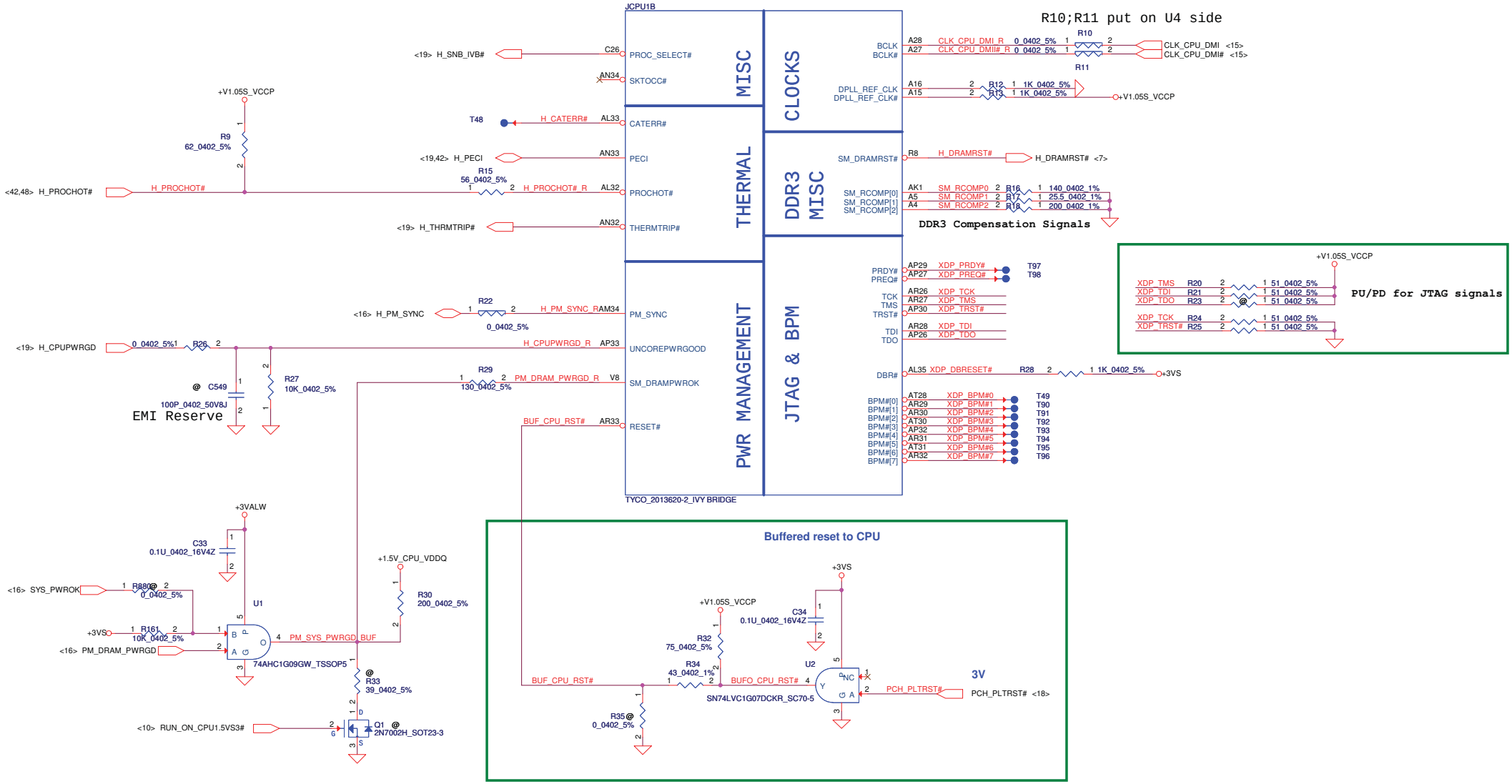
Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

Size	Document Number	Rev
Custom	*LA-7983P*	0.3

Date: Thursday, January 05, 2012 Sheet 5 of 60



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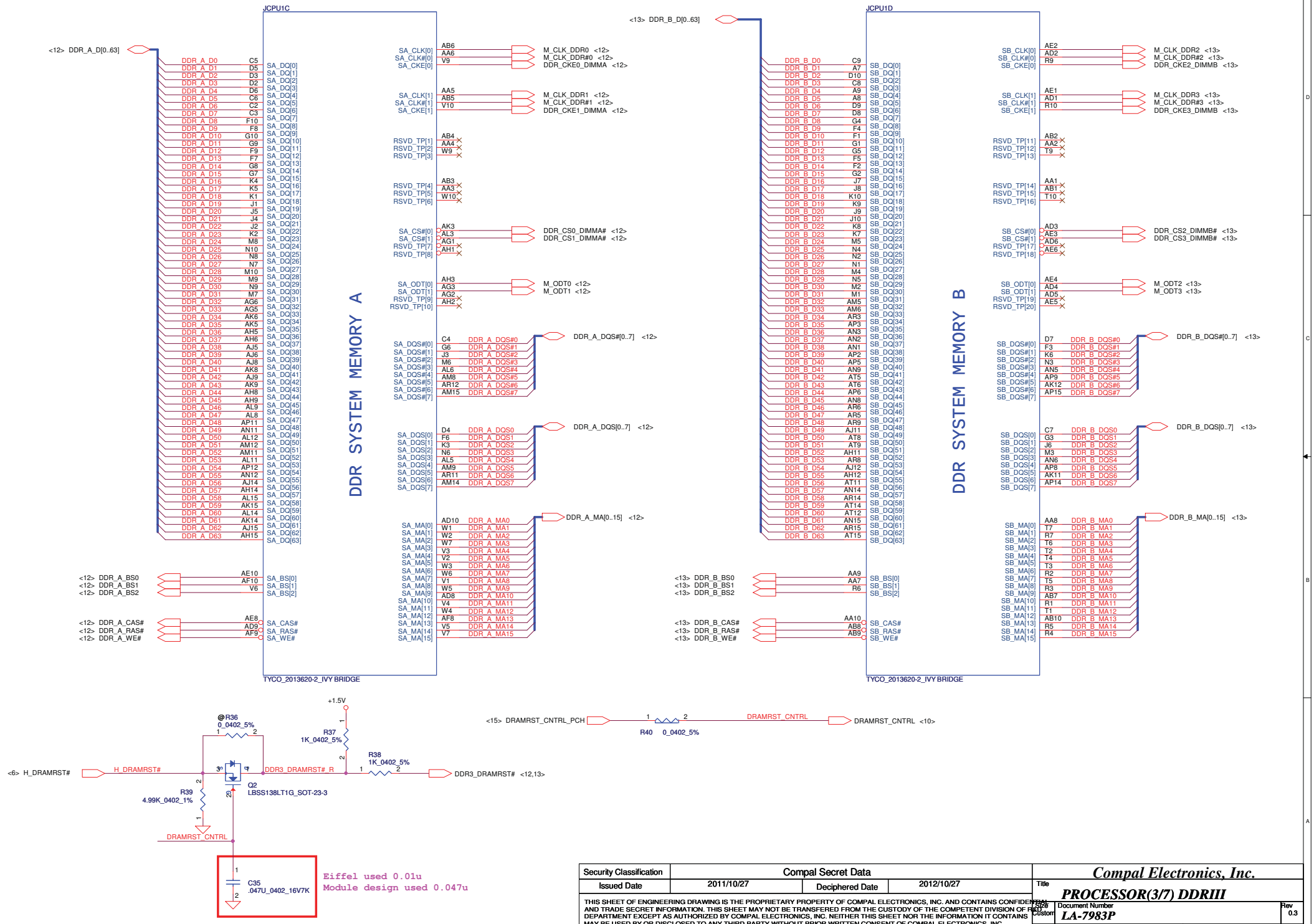
Title	Compal Electronics, Inc.		
	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 6 of 60		



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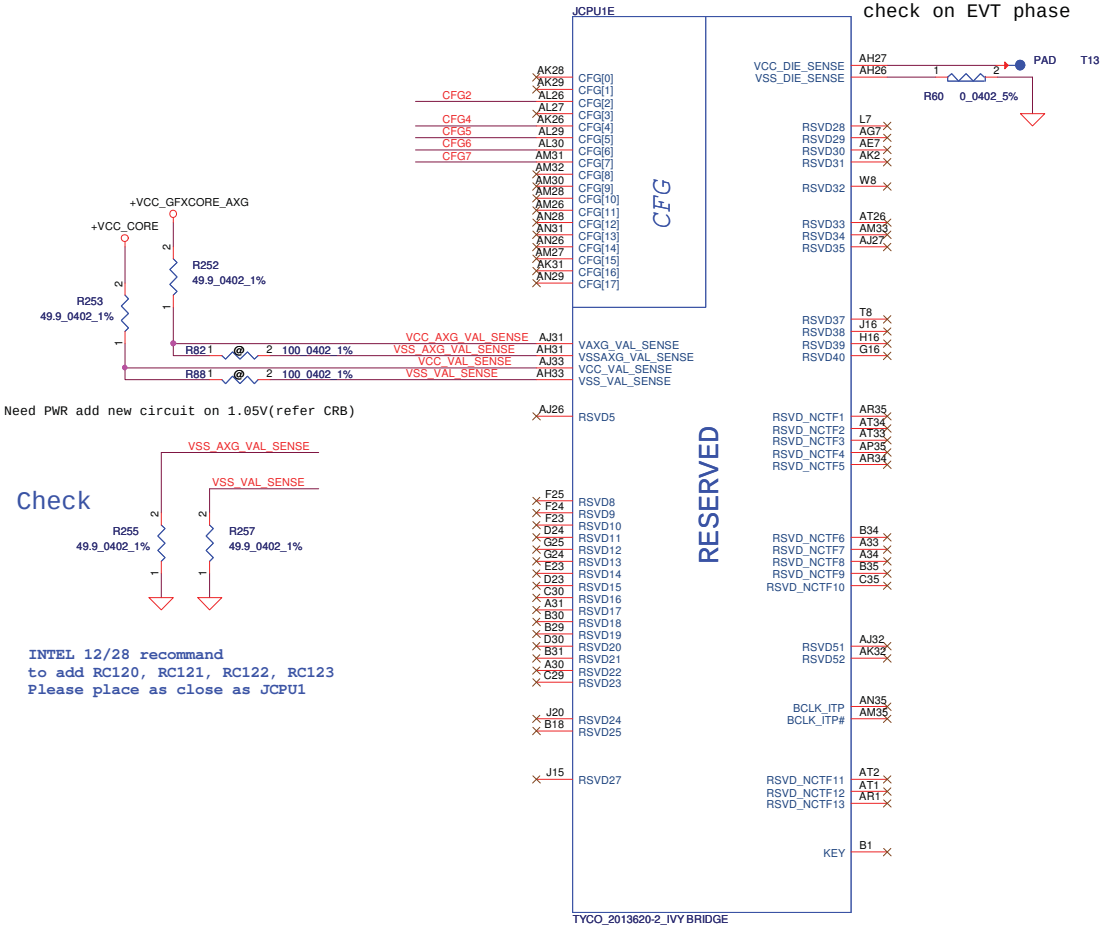
Title	PROCESSOR(3/7) DDRIII		
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 7 of 60		

CFG Straps for Processor

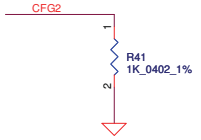


Interl request AH26 short GND
check on EVT phase

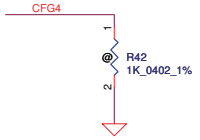
Need PWR add new circuit on 1.05V(refer CRB)

Check

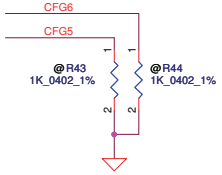
INTEL 12/28 recommand
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1



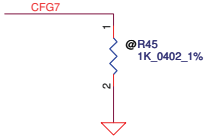
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 8 of 60

POWER

JCPU1F

+VCC_CORE

EDS v1.5 QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

AG35	VCC1	VCCIO1	AH13
AG34	VCC2	VCCIO2	AH10
AG33	VCC3	VCCIO3	AG10
AG32	VCC4	VCCIO4	AC10
AG31	VCC5	VCCIO5	Y10
AG30	VCC6	VCCIO6	U10
AG29	VCC7	VCCIO7	P10
AG28	VCC8	VCCIO8	L10
AG27	VCC9	VCCIO9	J14
AG26	VCC10	VCCIO10	J13
AF35	VCC11	VCCIO11	J12
AF34	VCC12	VCCIO12	J11
AF33	VCC13	VCCIO13	H14
AF32	VCC14	VCCIO14	H12
AF31	VCC15	VCCIO15	H11
AF30	VCC16	VCCIO16	G14
AF29	VCC17	VCCIO17	G13
AF28	VCC18	VCCIO18	G12
AF27	VCC19	VCCIO19	F14
AF26	VCC20	VCCIO20	F13
AD35	VCC21	VCCIO21	F12
AD34	VCC22	VCCIO22	F11
AD33	VCC23	VCCIO23	E14
AD32	VCC24	VCCIO24	E12
AD31	VCC25		
AD30	VCC26	VCCIO25	E11
AD29	VCC27	VCCIO26	D14
AD28	VCC28	VCCIO27	D13
AD27	VCC29	VCCIO28	D12
AD26	VCC30	VCCIO29	D11
AC35	VCC31	VCCIO30	C14
AC34	VCC32	VCCIO31	C13
AC33	VCC33	VCCIO32	C12
AC32	VCC34	VCCIO33	C11
AC31	VCC35	VCCIO34	B14
AC30	VCC36	VCCIO35	B12
AC29	VCC37	VCCIO36	A14
AC28	VCC38	VCCIO37	A13
AC27	VCC39	VCCIO38	A12
AC26	VCC40	VCCIO39	A11
AA35	VCC41		
AA34	VCC42	J23	
AA33	VCC43	VCCIO40	
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
V28	VCC68		
V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

TYCO_2013620-2_IVY BRIDGE

+V1.05S_VCCP

C99
.1U_0402_16V7K

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT#
VIDSCLK
VIDSOUT

AJ29 H_CPU_SVIDALRT# — R47 43_0402_1% — VR_SVID_ALRT# <55>
AJ30 H_CPU_SVIDCLK — 0_0402_5% — R48 — VR_SVID_CLK <55>
AJ28 H_CPU_SVIDDAT — 0_0402_5% — R49 — VR_SVID_DAT <55>

R50 130_0402_5% +V1.05S_VCCP

0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51
100_0402_1%

VCC_SENSE
VSS_SENSE

AJ35 VCCSENSE_R — R52 0_0402_5%
AJ34 VSSSENSE_R — R53 0_0402_5%

VCCSENSE <55>
VSSSENSE <55>

10/19 Update to @ for PWR modification.

VCCIO_SENSE
VSS_SENSE_VCCIO

B10
A10 VSSIO_SENSE_L — R74 10_0402_1% @ — VSSIO_SENSE

VCCIO_SENSE <52,53>

R66 @ 100_0402_1%

R54
100_0402_1%

R74 & R79 put together

+V1.05S_VCCP

R79
10_0402_1%

VSSIO_SENSE_L <53>

10/19 Add off page to PWR side.

VSS_SENCE 100ohm +-1% pull-down to GND near processor

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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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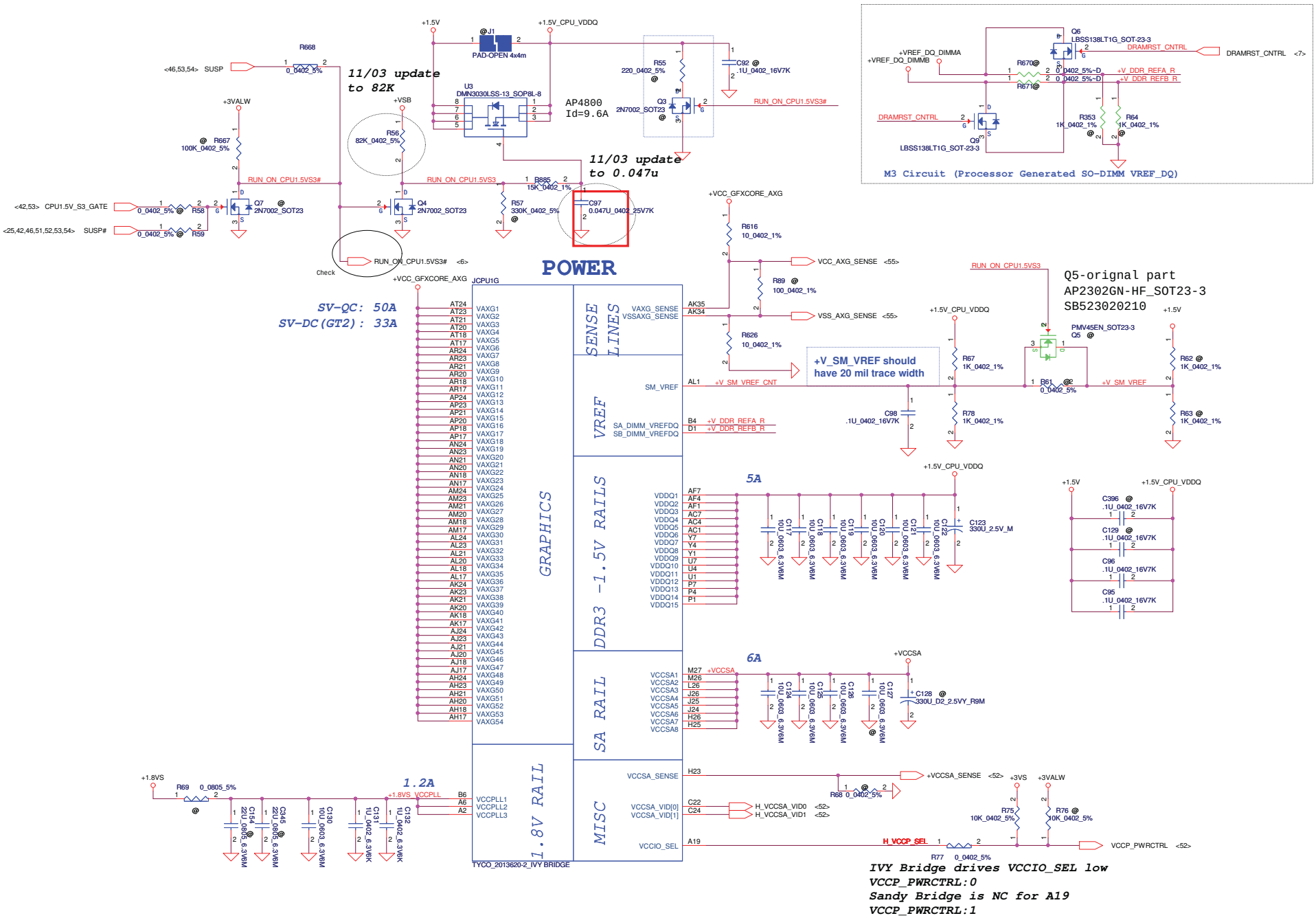
Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 9 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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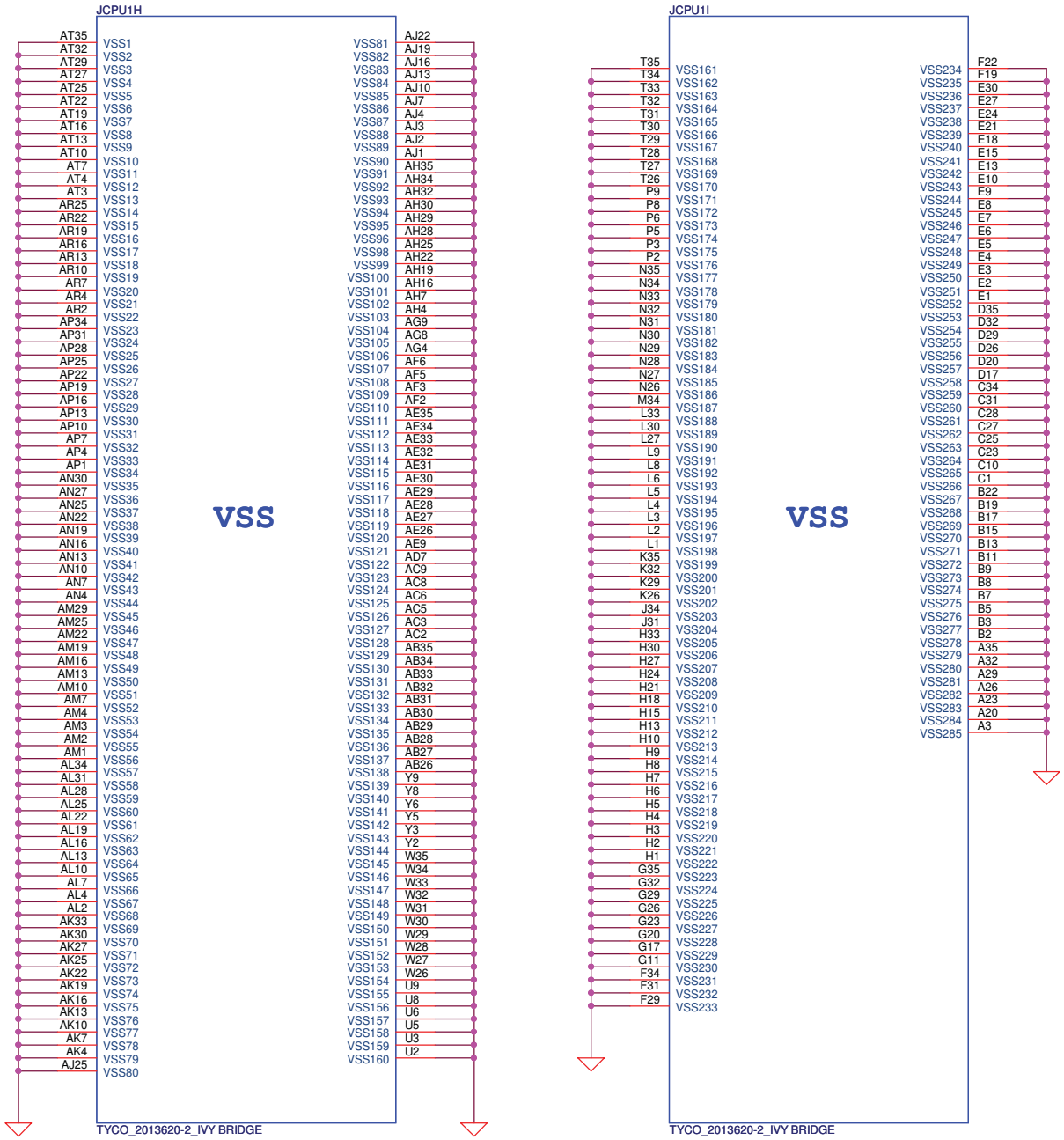
Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 10 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-7983P	0.3

Date: Thursday, January 05, 2012 Sheet 11 of 60

DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

DDR3_DRAMRST# <7,13>

SMB_DATA_S3 <13,15,36>
SMB_CLK_S3 <13,15,36>

+0.75VS

0.65@0.75V

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

EVT Check

C149 @ 220U_6.3V_M

Layout Note:
Place near DIMM

7/28 Update connect GND directly

Layout Note:
Place near DIMM

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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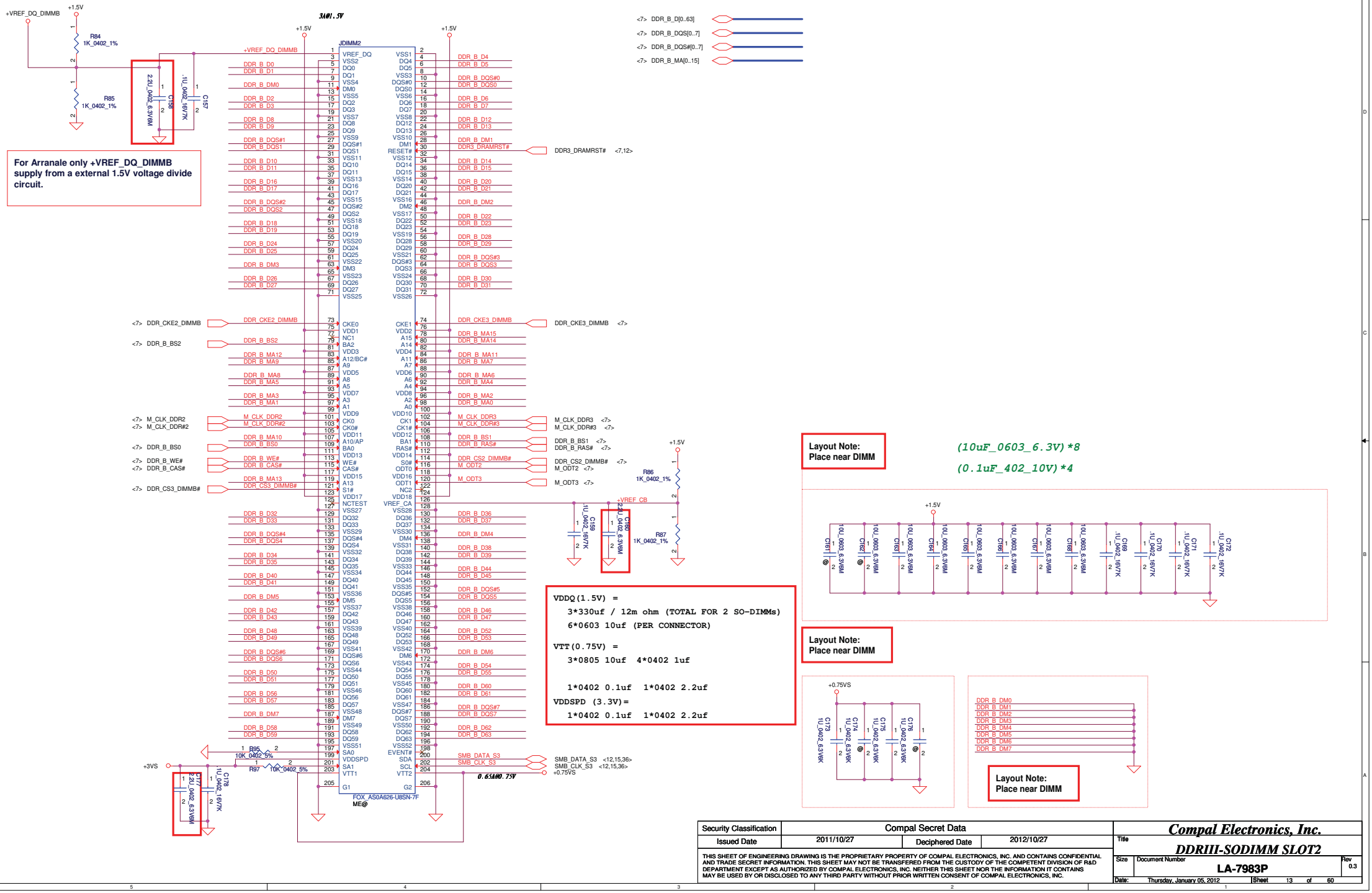
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **LA-7983P** | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 12 of 60



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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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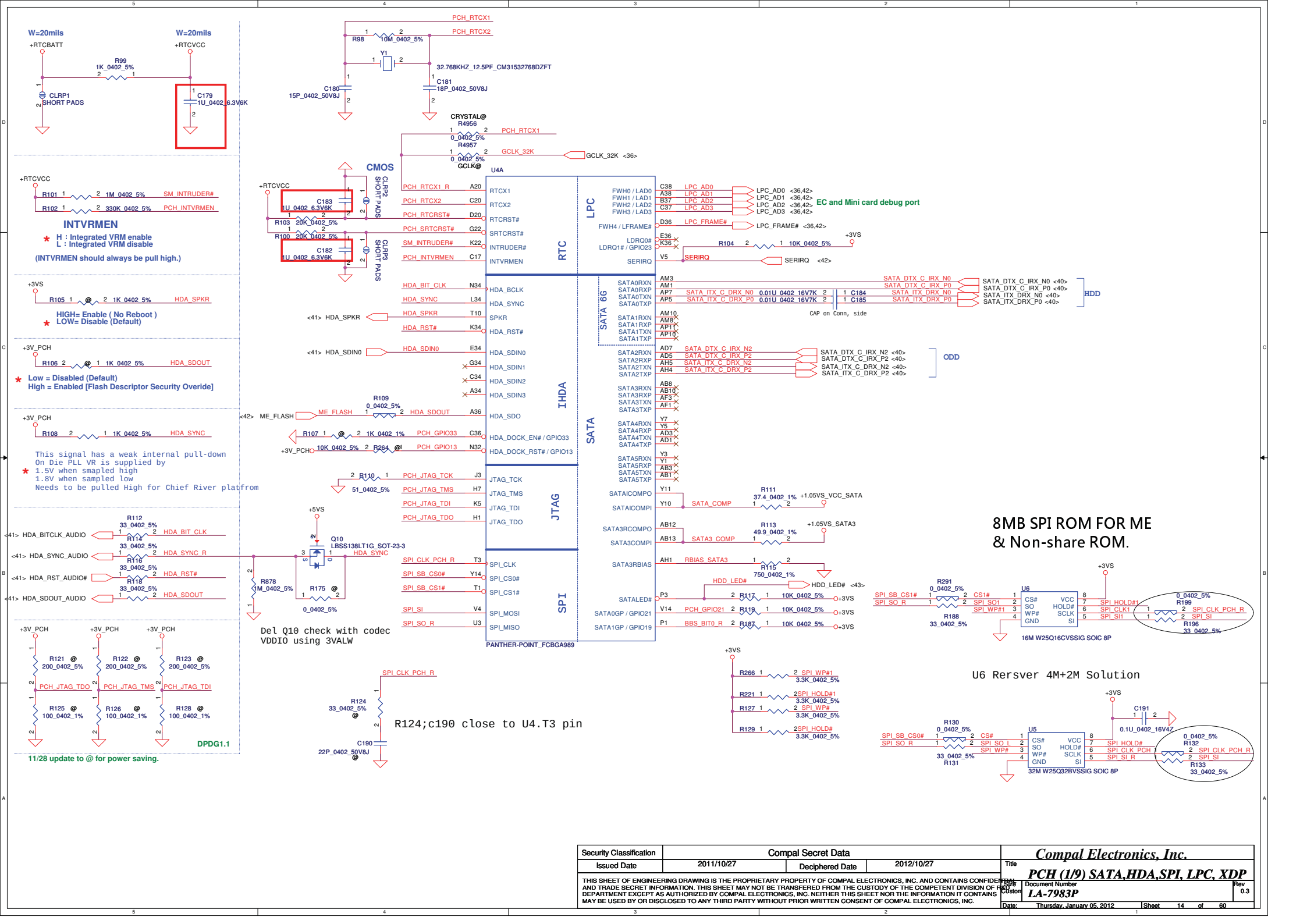
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-7983P	0.3

Date: Thursday, January 05, 2012 Sheet 13 of 60



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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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Compal Electronics, Inc.	
Title	PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom	Document Number: LA-7983P
Rev	0.3
Date: Thursday, January 05, 2012	Sheet 14 of 60

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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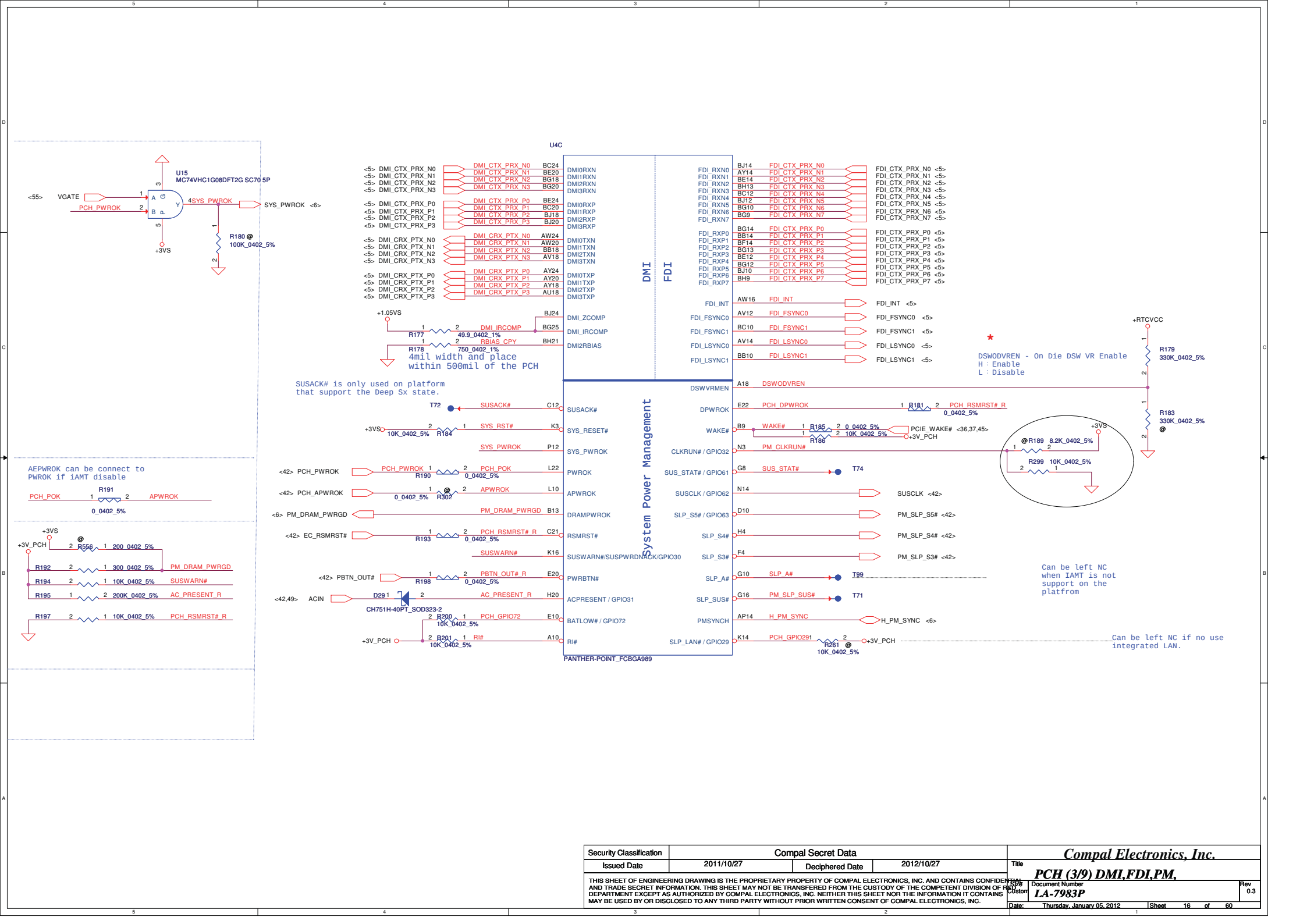
Compal Electronics, Inc.			
Title: PCH (2/9) PCIE, SMBUS, CLK			
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 15 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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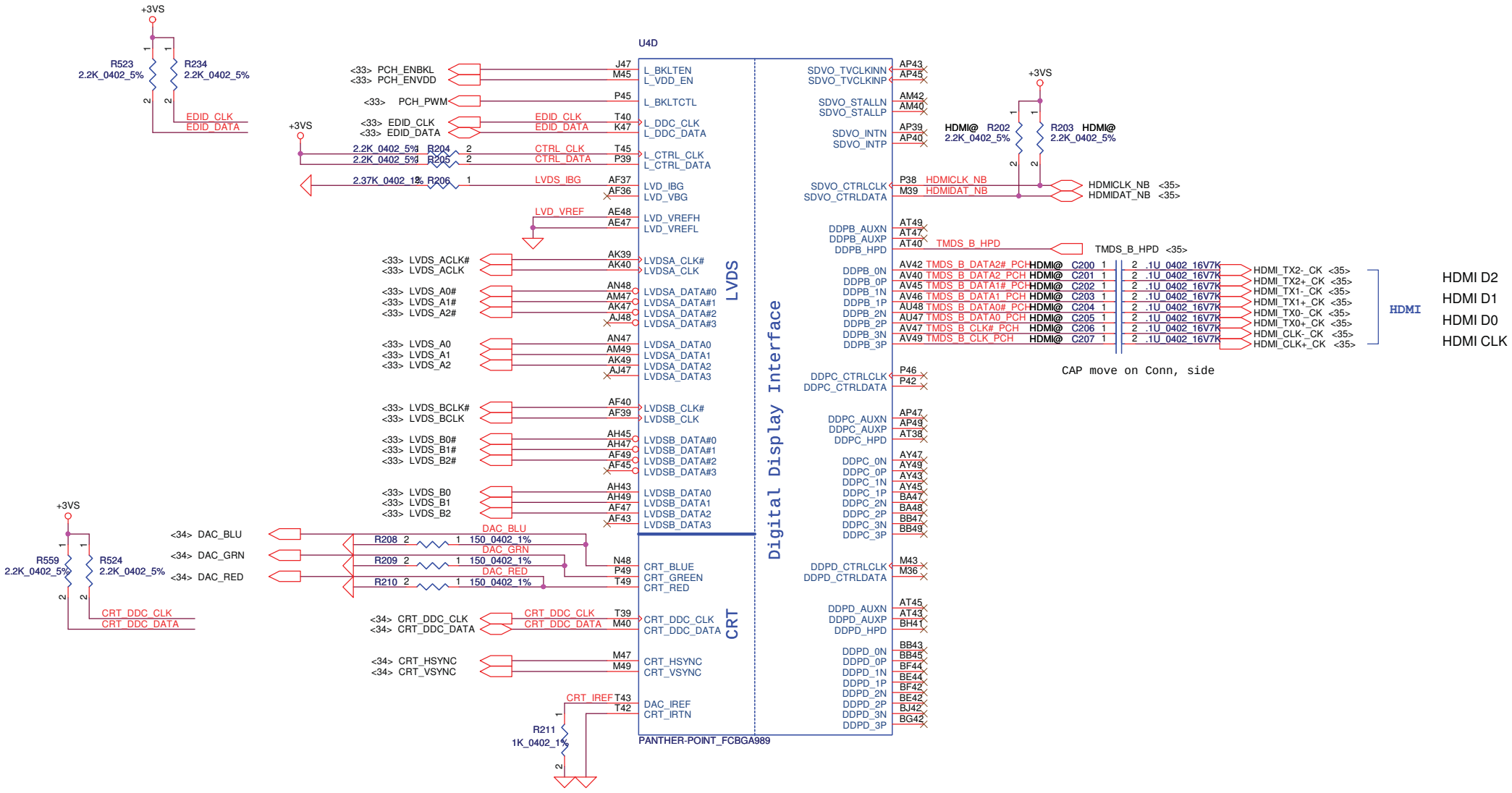
Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom	Document Number: LA-7983P	Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 16 of 60	



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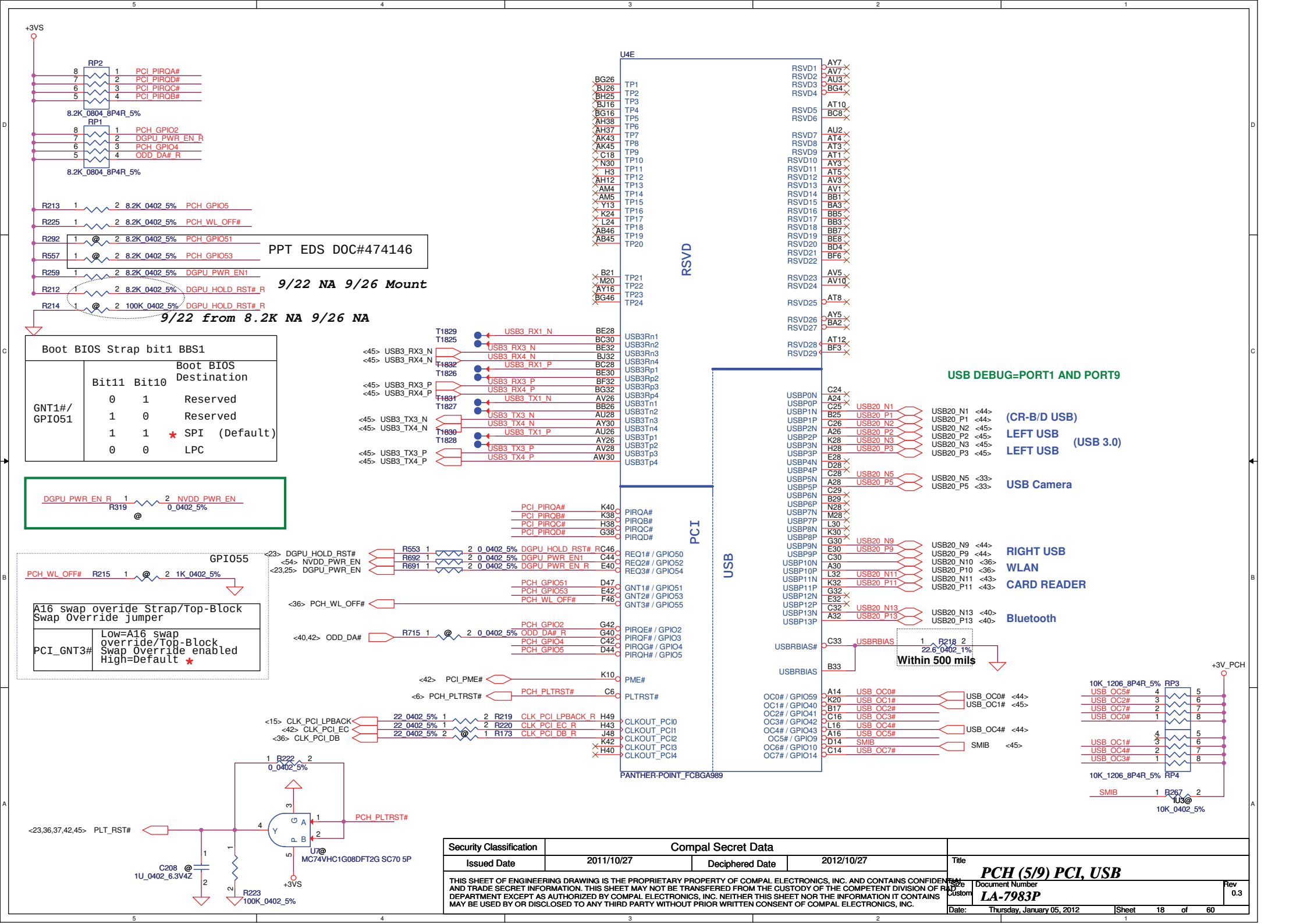
Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
B	LA-7983P	0.3

Date: Thursday, January 05, 2012 Sheet 17 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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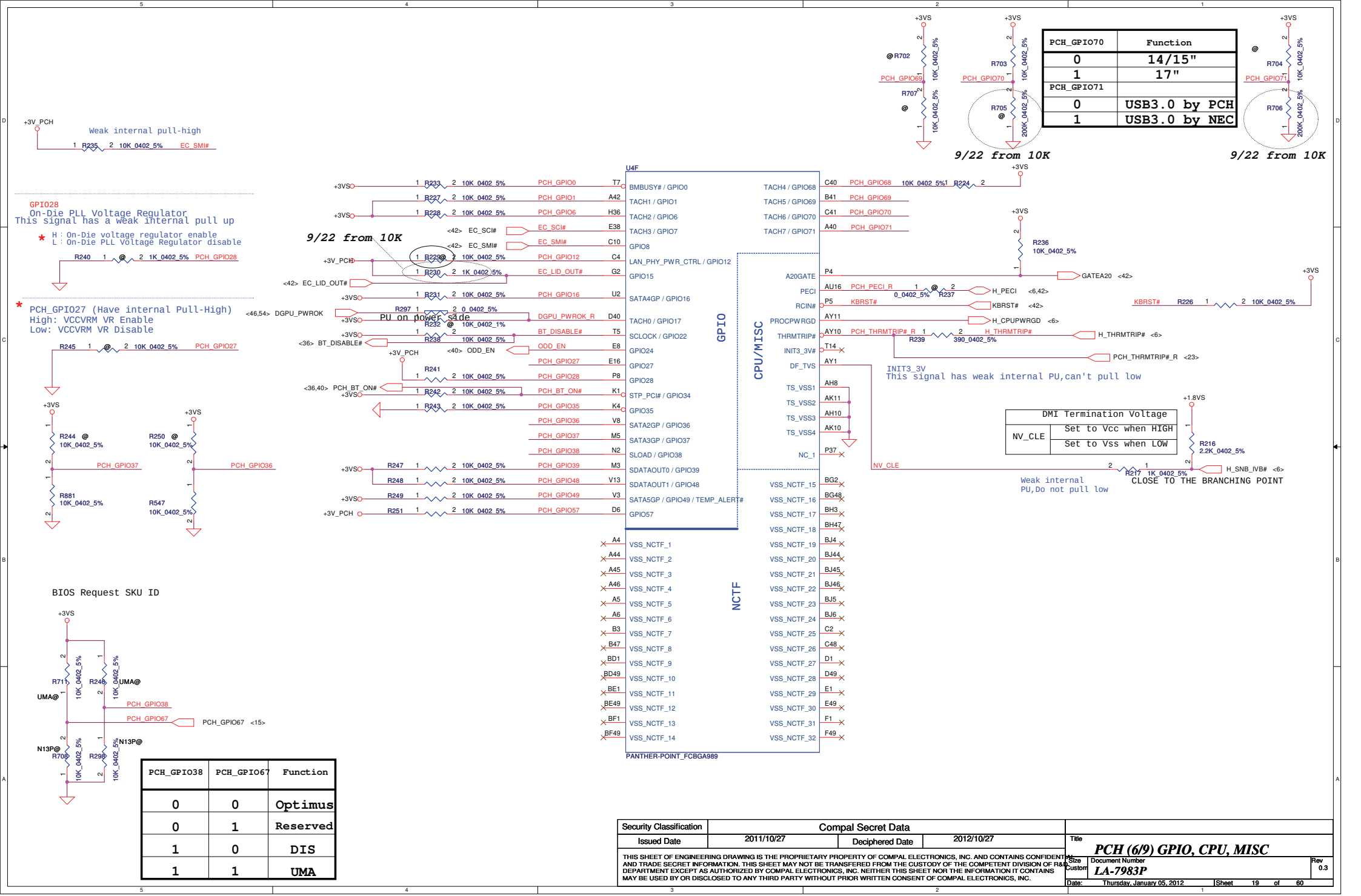
Title	PCH (5/9) PCI, USB		
Size	Custom	Document Number	LA-7983P
Rev	0.3		
Date:	Thursday, January 05, 2012	Sheet	18 of 60



Security Classification	Compal Secret Data	
Issued Date	2011/10/27	Deciphered Date 2012/10/27

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Title	PCH (6/9) GPIO, CPU, MISC		
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 19 of 60		

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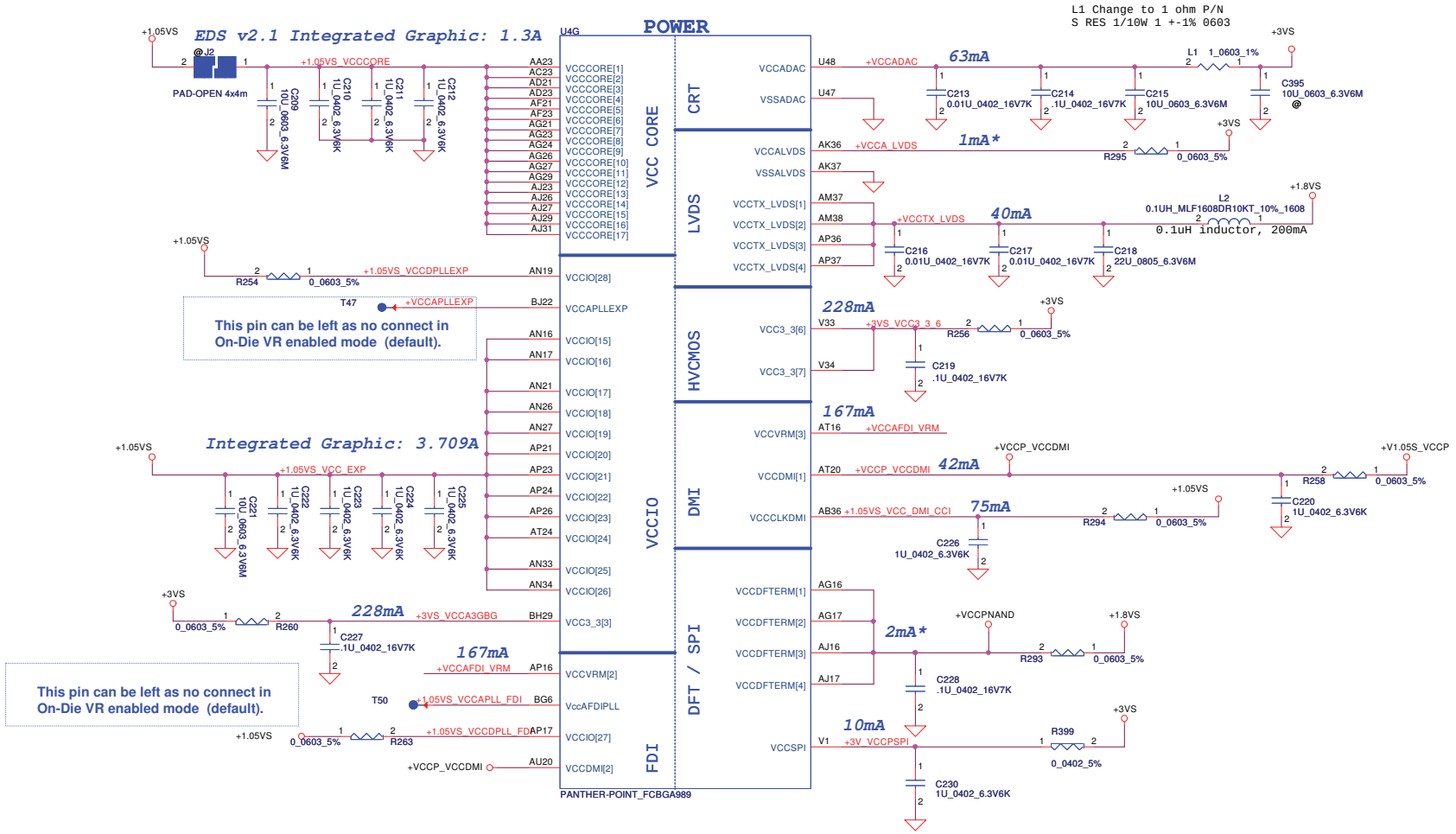

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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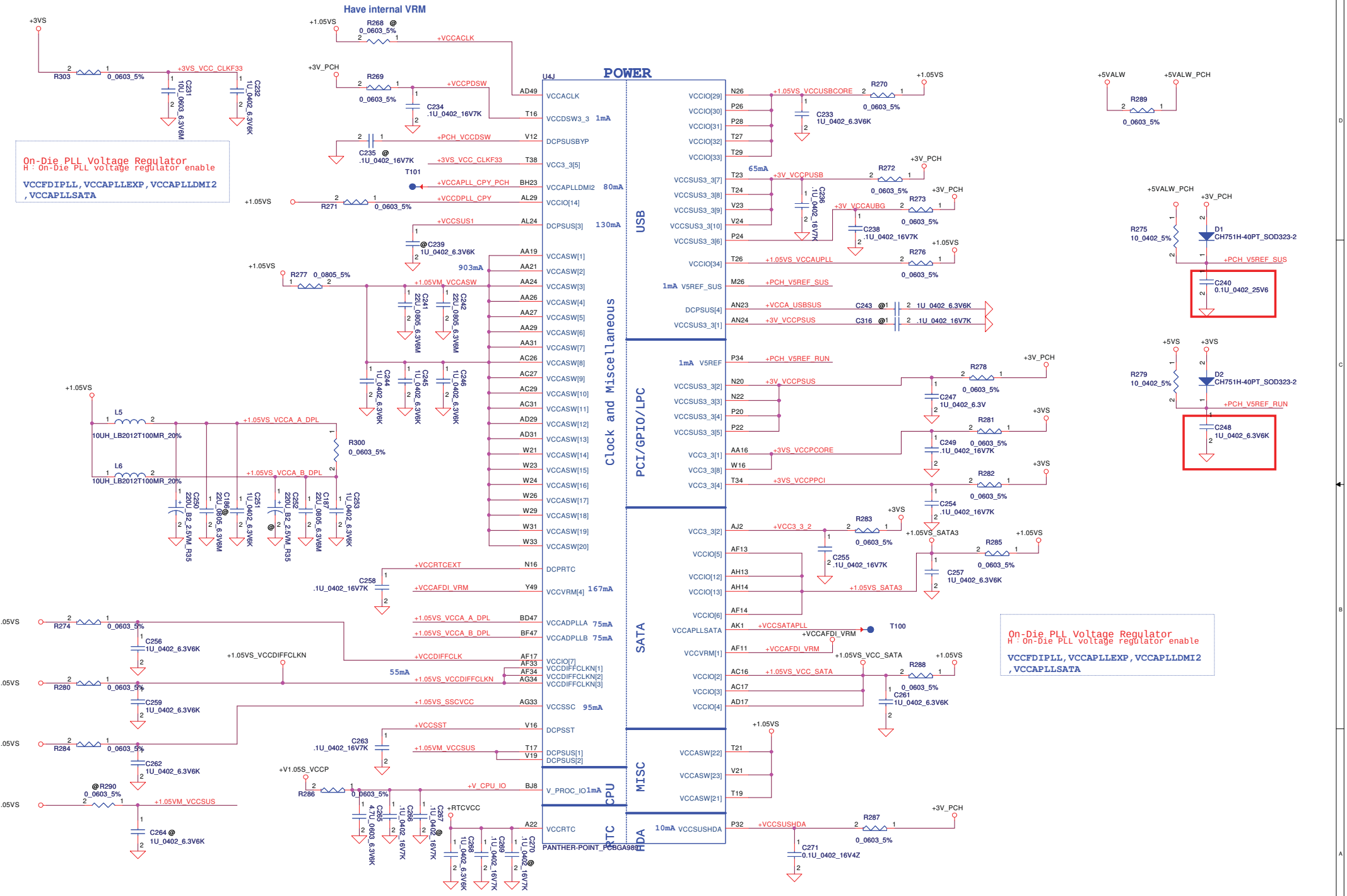
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 20 of 60



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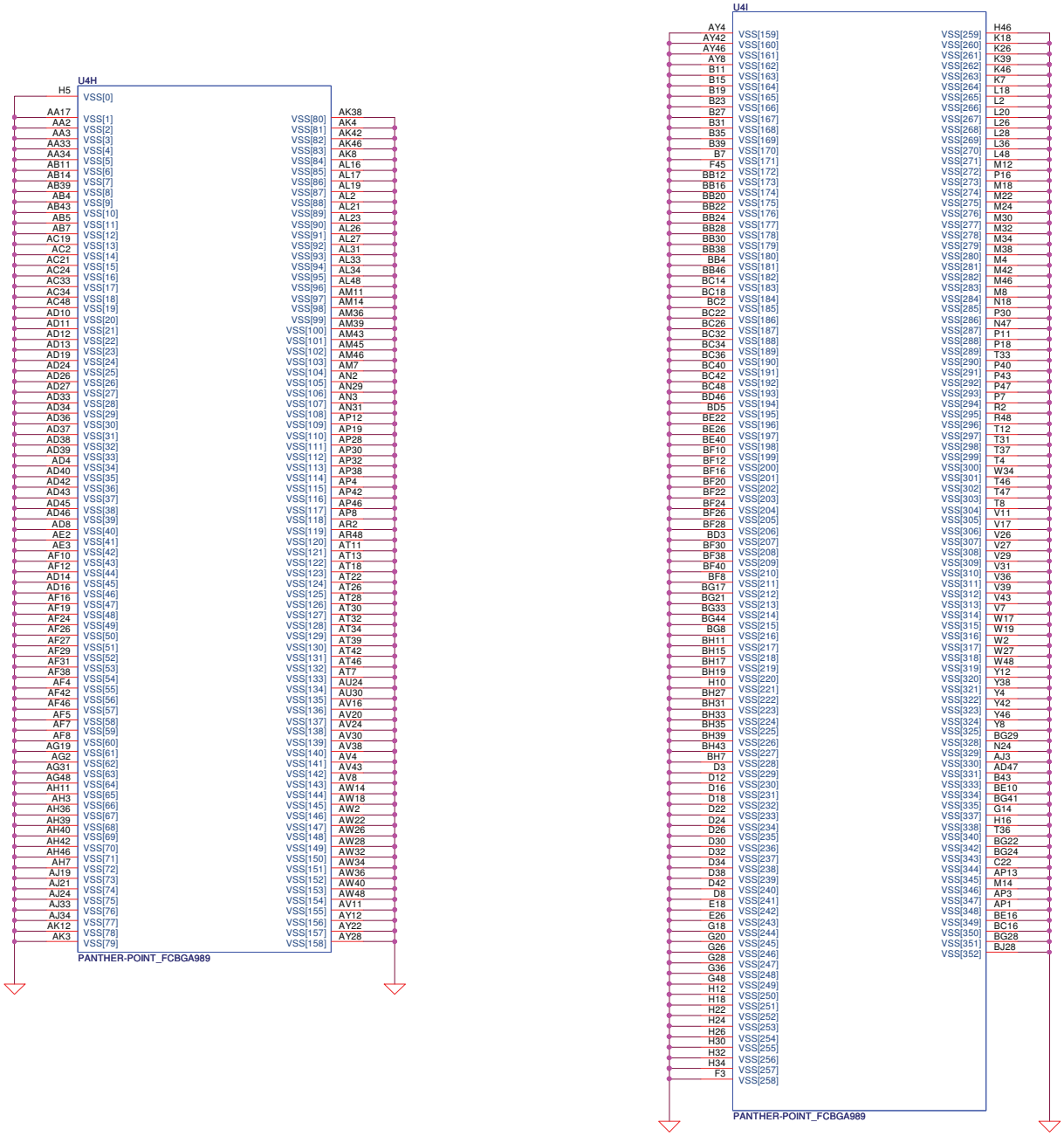
Title	Compal Electronics, Inc. PCH (8/9) PWR		
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 21 of 60		



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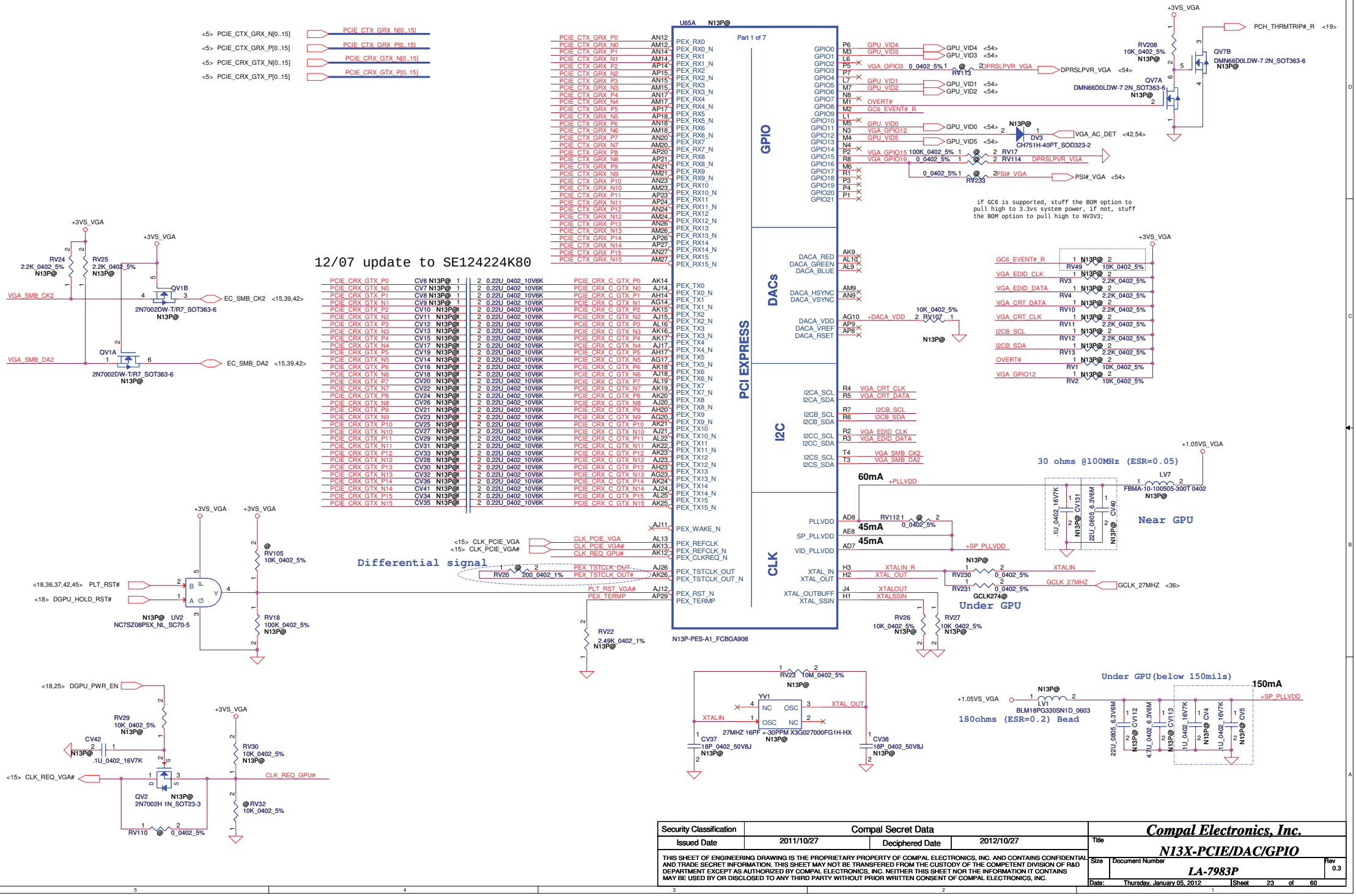
Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 22 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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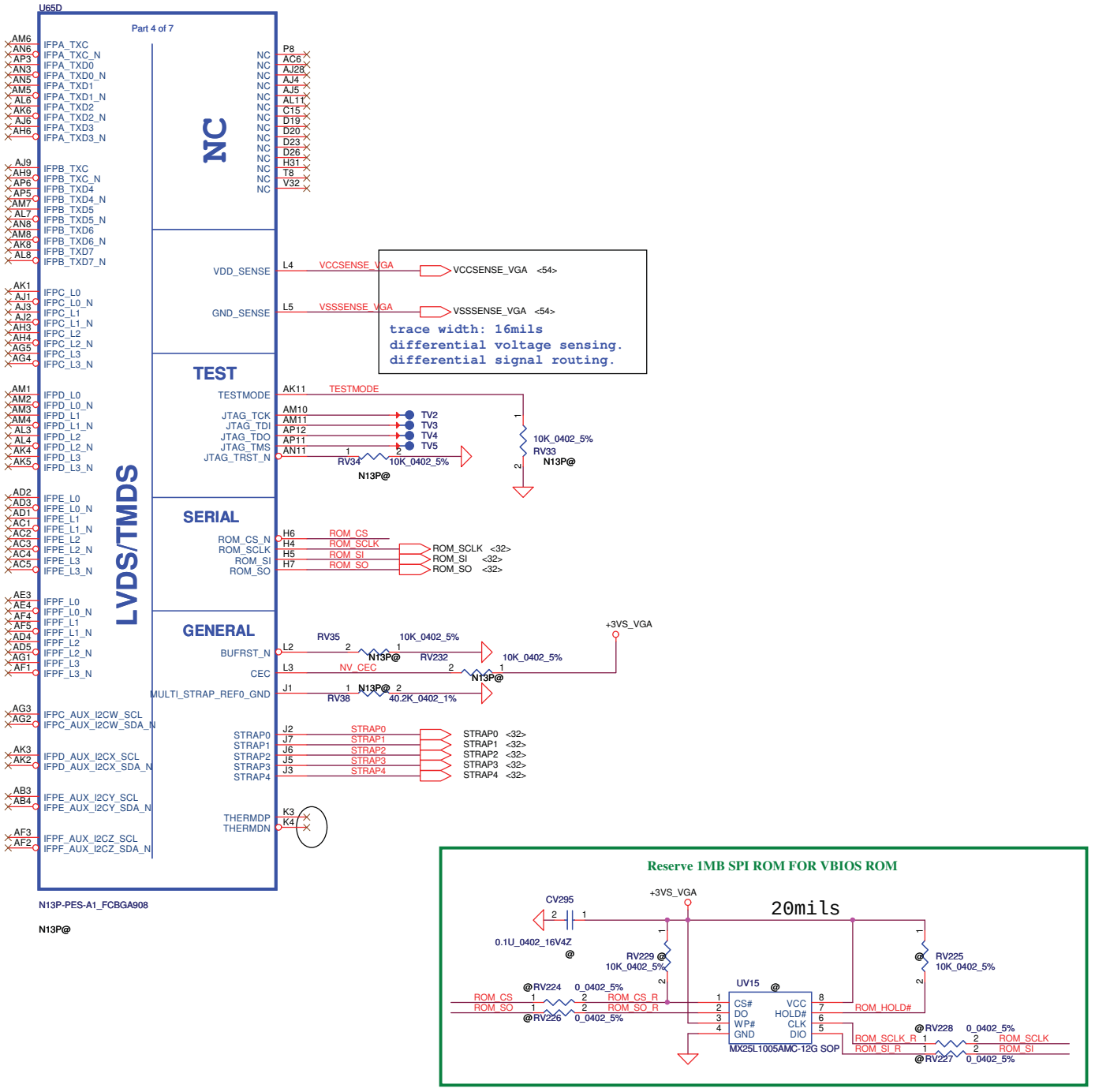
Compal Electronics, Inc.

Title: **N13X-PCIE/DAC/GPIO**

Size	Document Number	Rev
	LA-7983P	0.3

Date: Thursday, January 05, 2012 | Sheet 23 of 60



Security Classification	Compal Secret Data		
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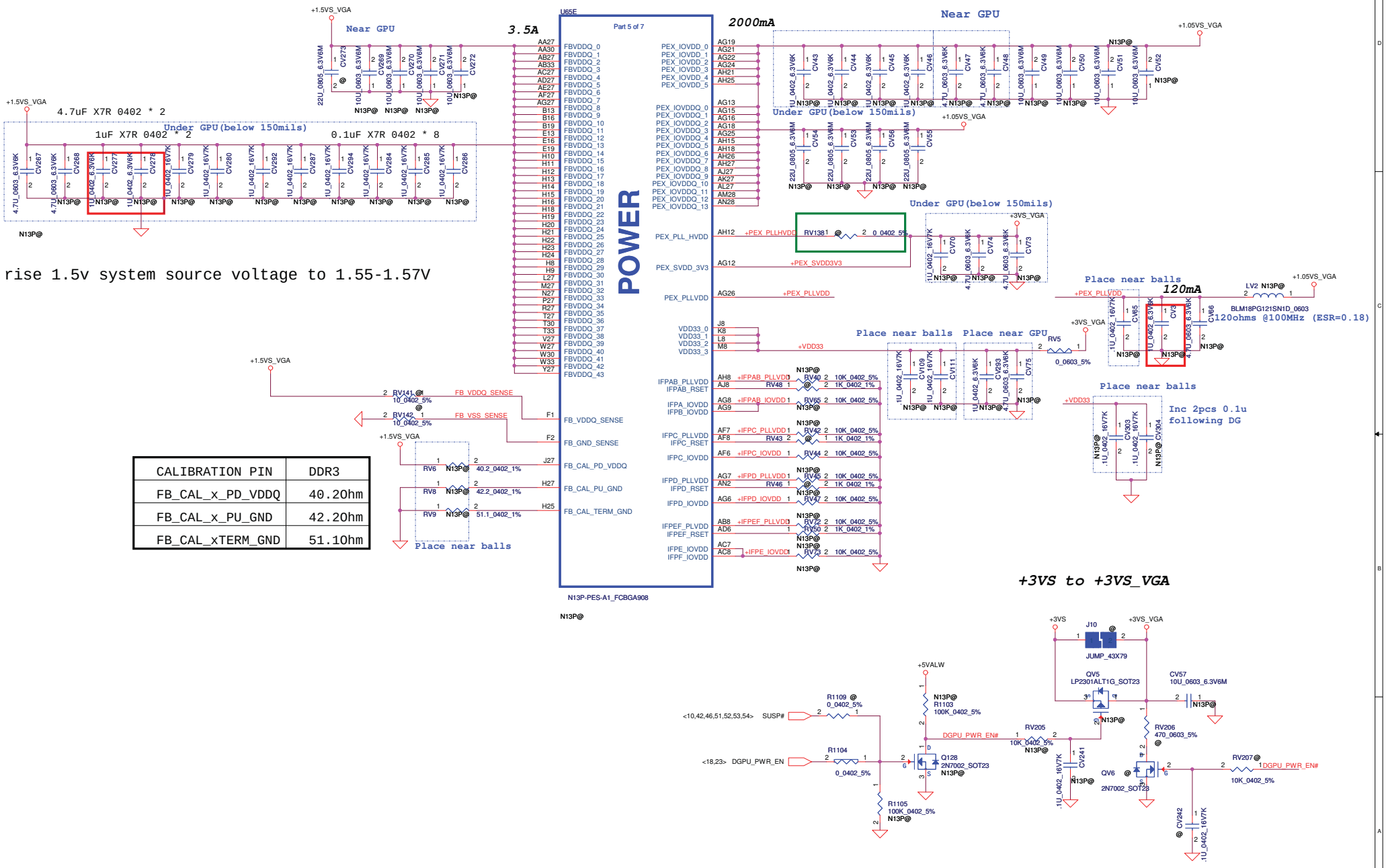
Compal Electronics, Inc.

Title: N13X-LVDS/HDMI/DP/THM

Size | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 24 of 60



CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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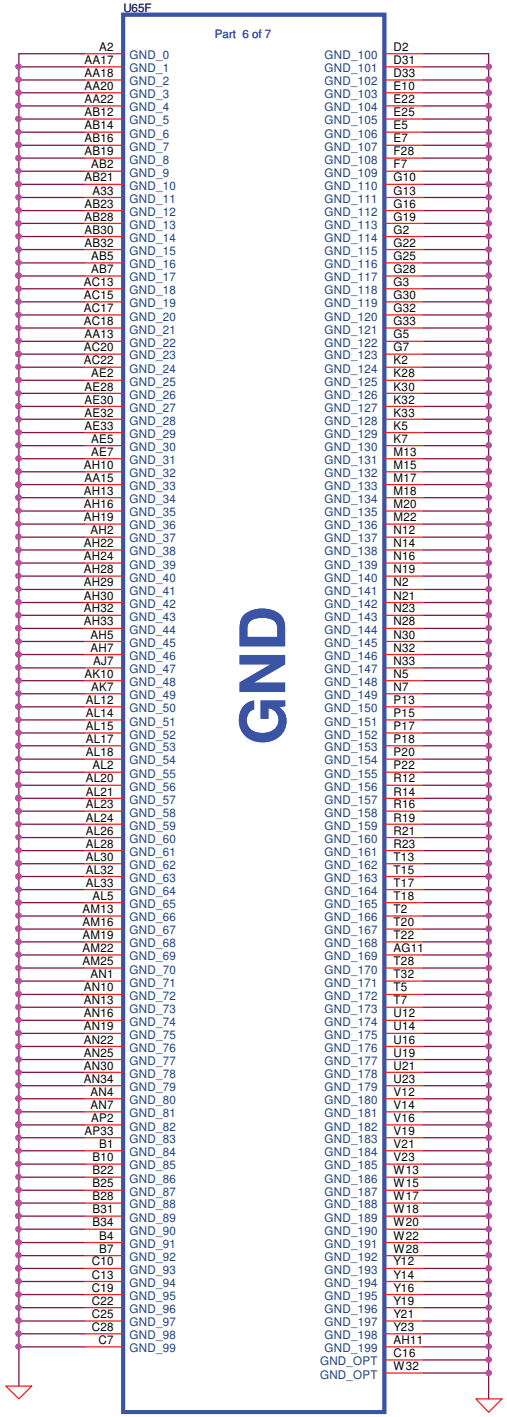
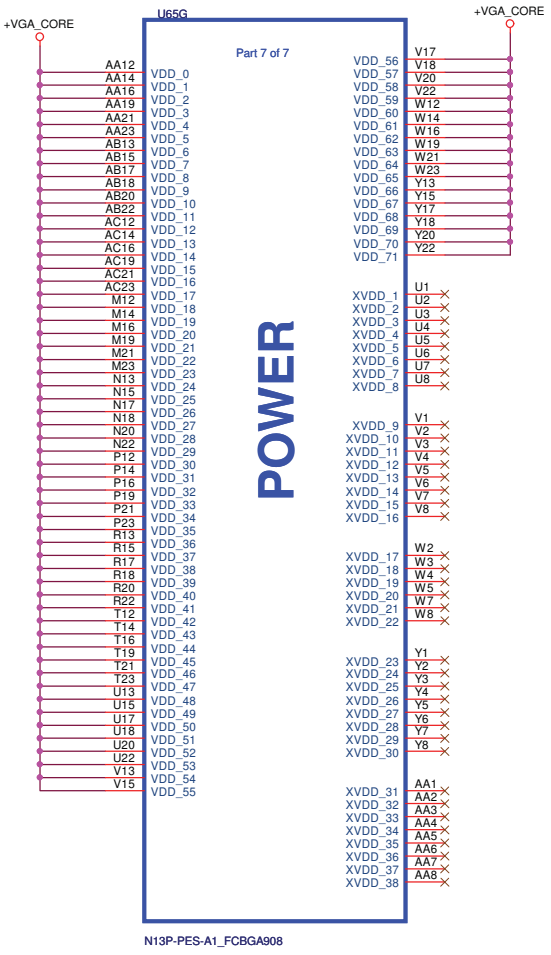
Compal Electronics, Inc.

Title: **N13X-POWER**

Size | Document Number: **LA-7983P** | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 25 of 60





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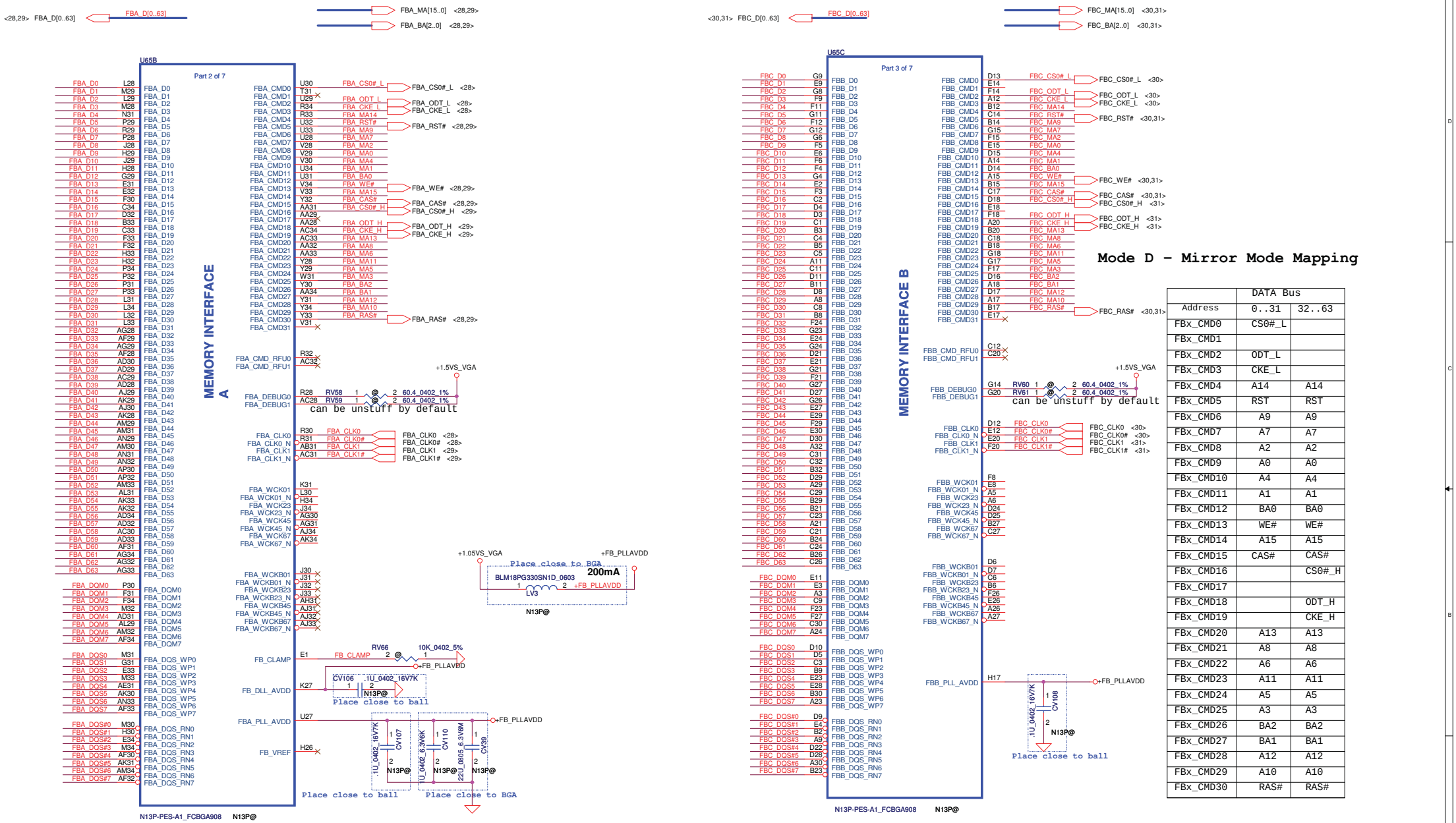
Compal Electronics, Inc.

Title: N13-VGA CORE, GND

Size | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 26 of 60



Mode D – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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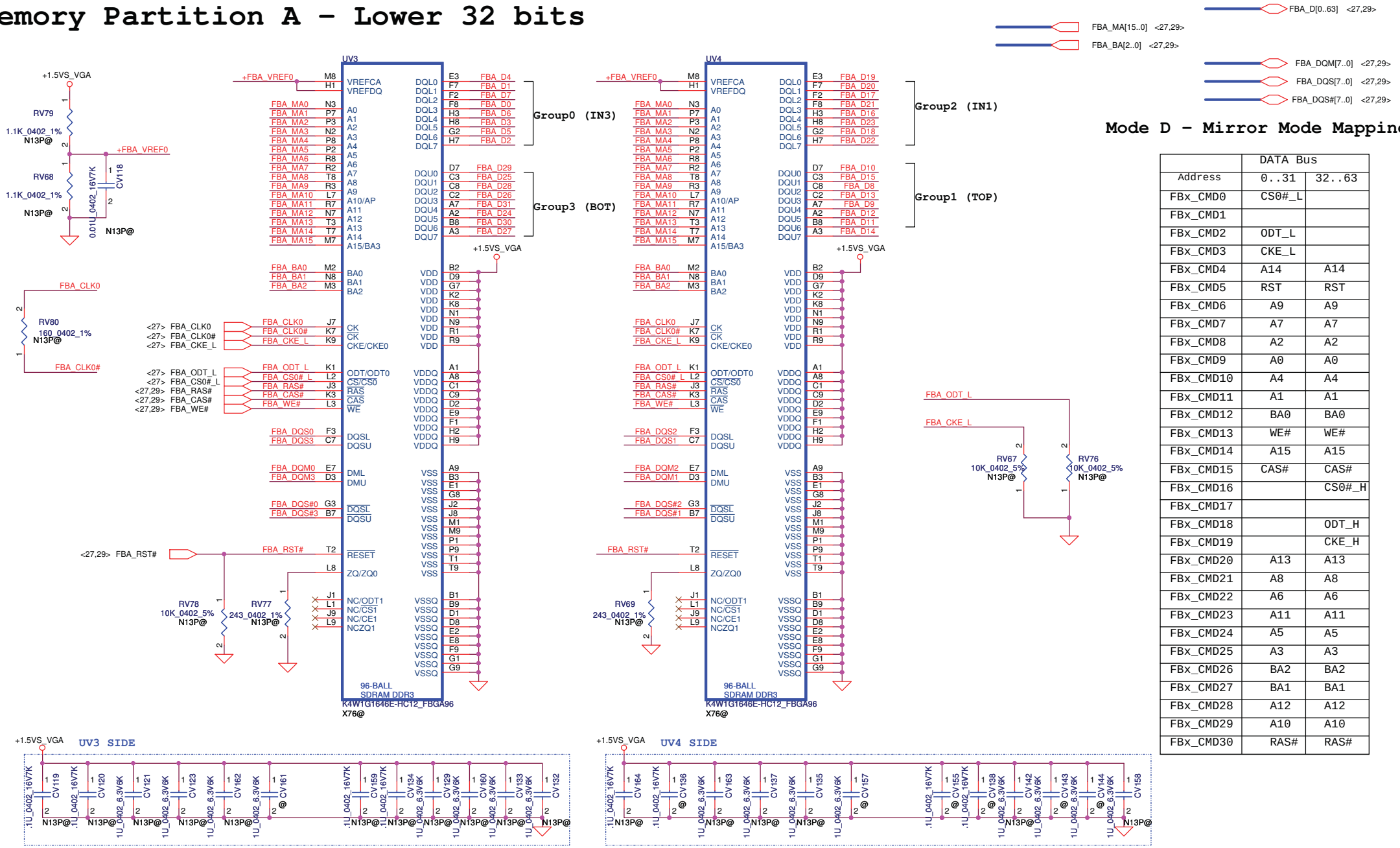
Compal Electronics, Inc.

Title: **N13X-MEM Interface**

Size	Document Number	Rev
	LA-7983P	0.3

Date: Thursday, January 05, 2012 Sheet 27 of 60

Memory Partition A - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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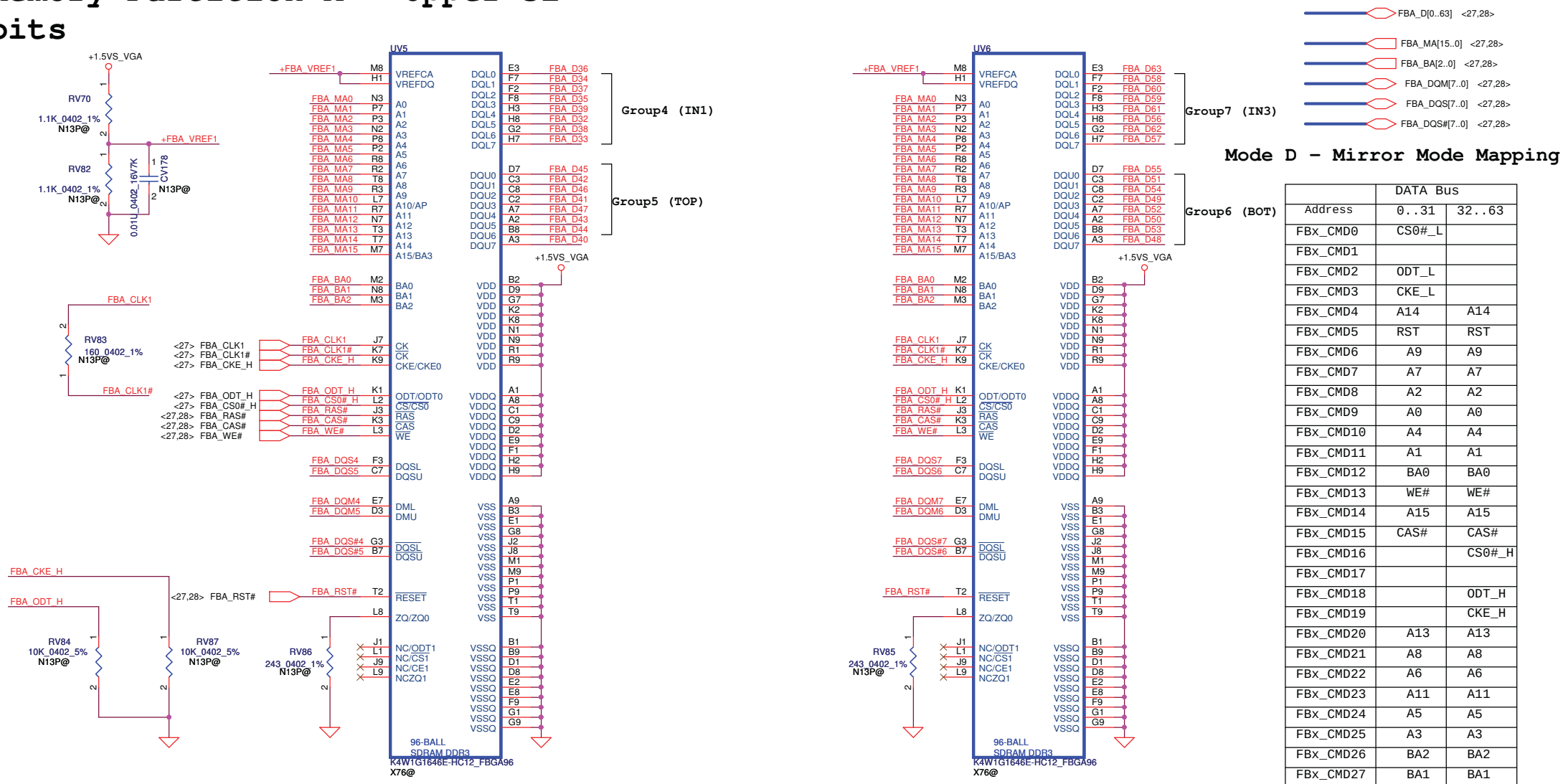
Compal Electronics, Inc.			
Title	N13X-VRAM A Lower		
Size	Document Number	LA-7983P	Rev 0.3
Date: Thursday, January 05, 2012	Sheet 28 of 60		

Memory Partition A – Upper 32 bits



Mode D – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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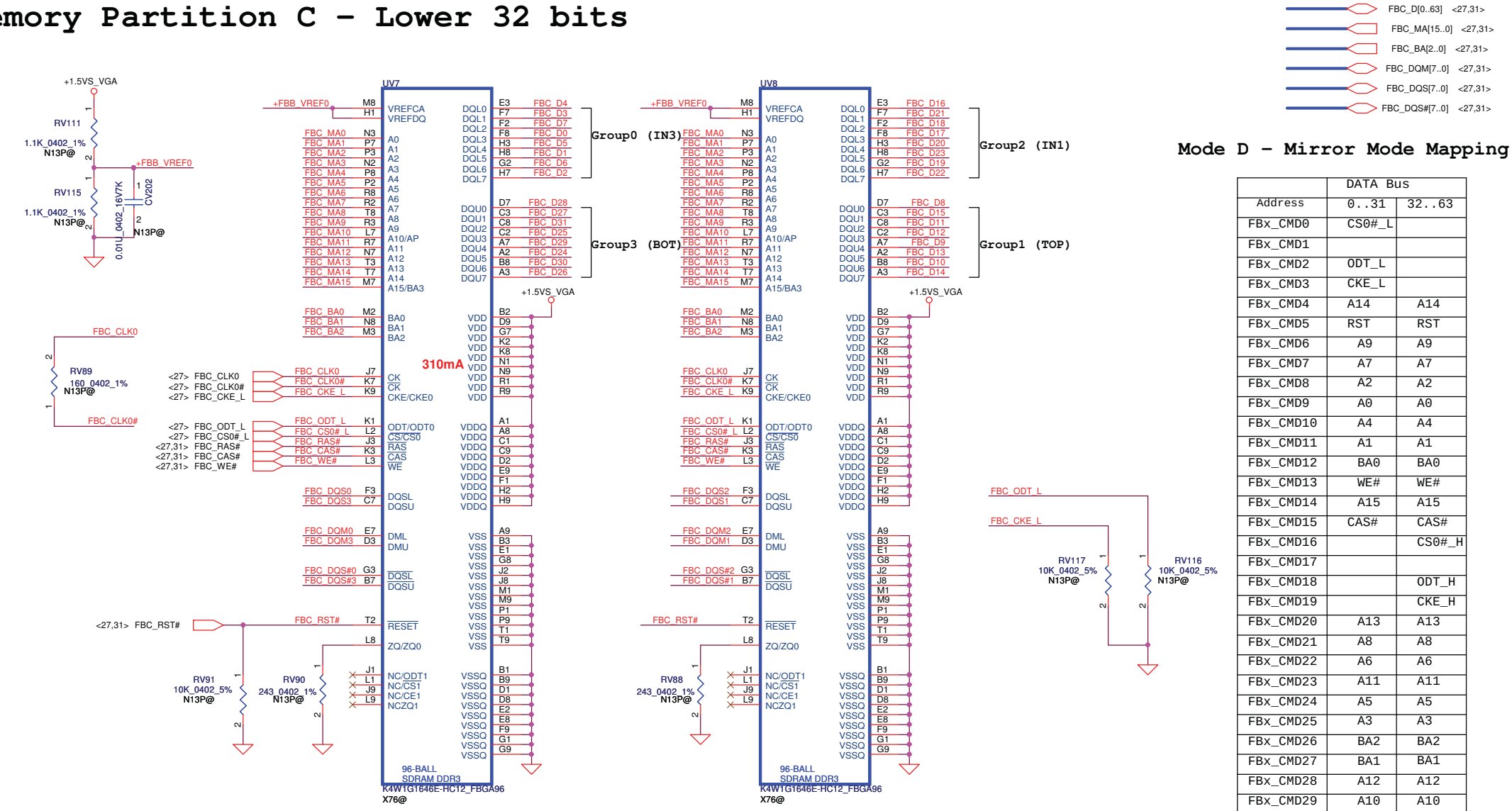
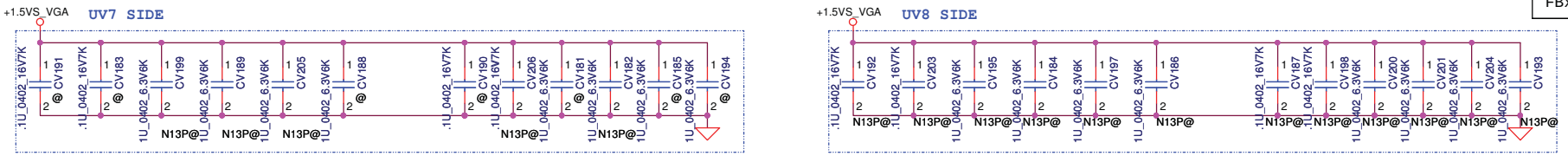
Compal Electronics, Inc.			
Title	N13X-VRAM A Upper		
Size	Document Number		Rev
	LA-7983P		0.3
Date:	Thursday, January 05, 2012	Sheet	29 of 60

Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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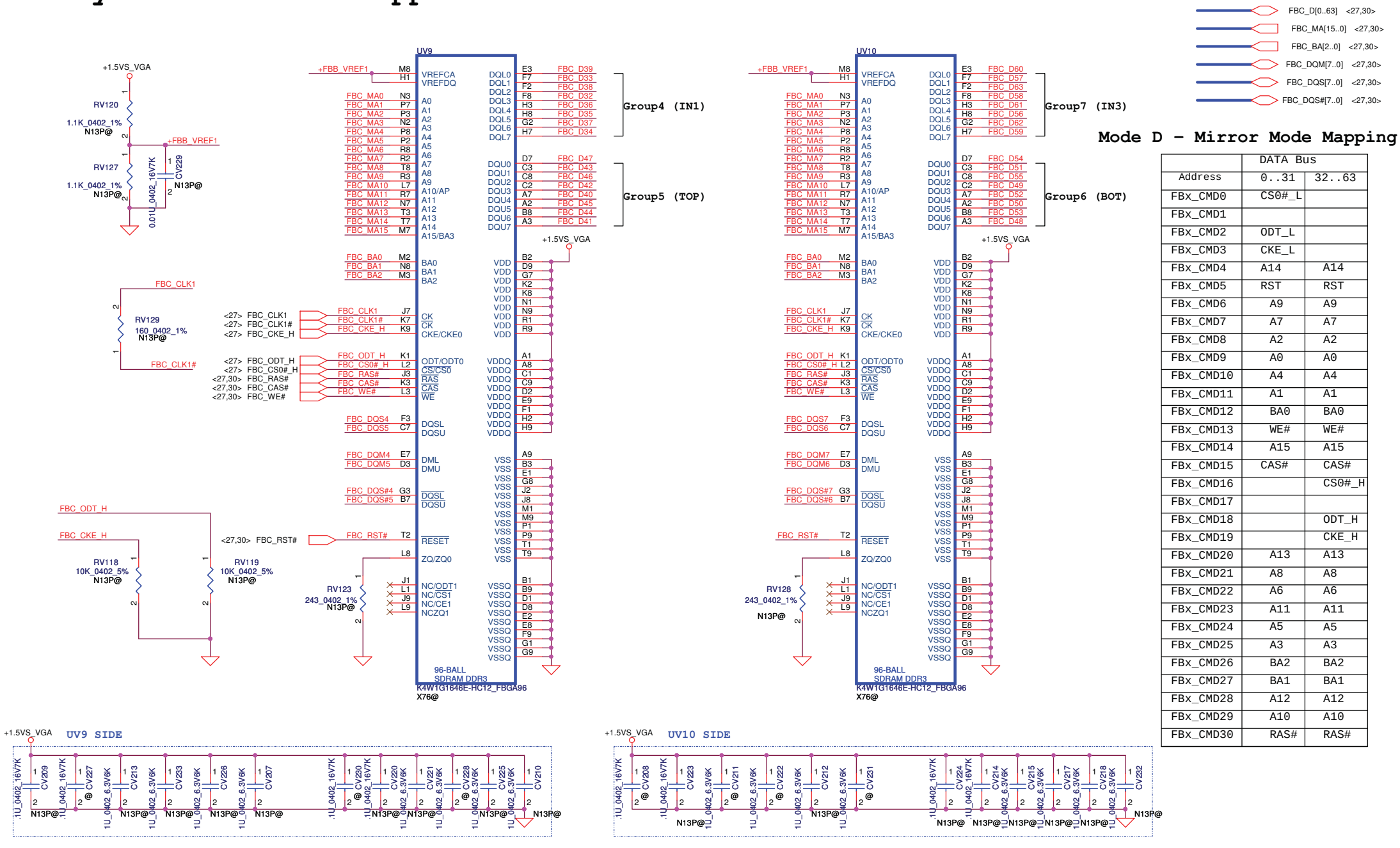
Compal Electronics, Inc.

Title: N13X-VRAM C Lower

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 30 of 60

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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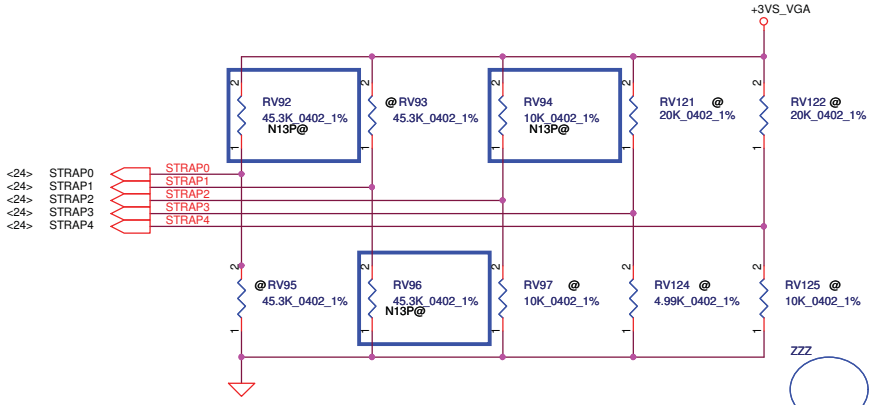
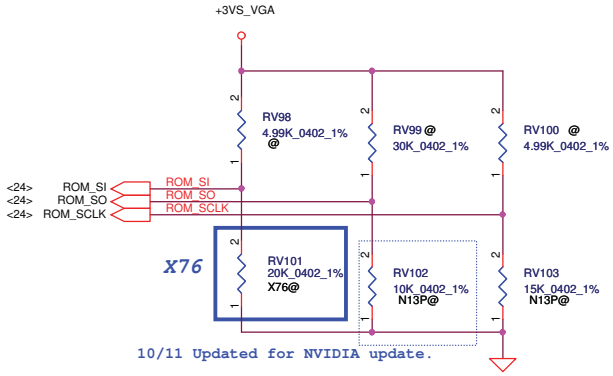
Compal Electronics, Inc.

Title: N13X-VRAM C Upper

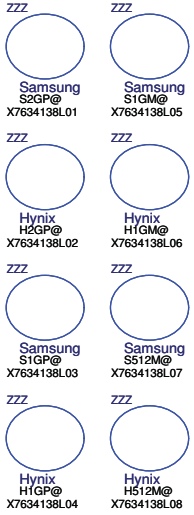
Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 31 of 60





10/11 Updated for NVIDIA update.



For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	X76 ROM_SI	X76 ROM_SO	X76 ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

10/11 Updated for NVIDIA update.

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

USER Straps

User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

PCIE_MAX_SPEED

0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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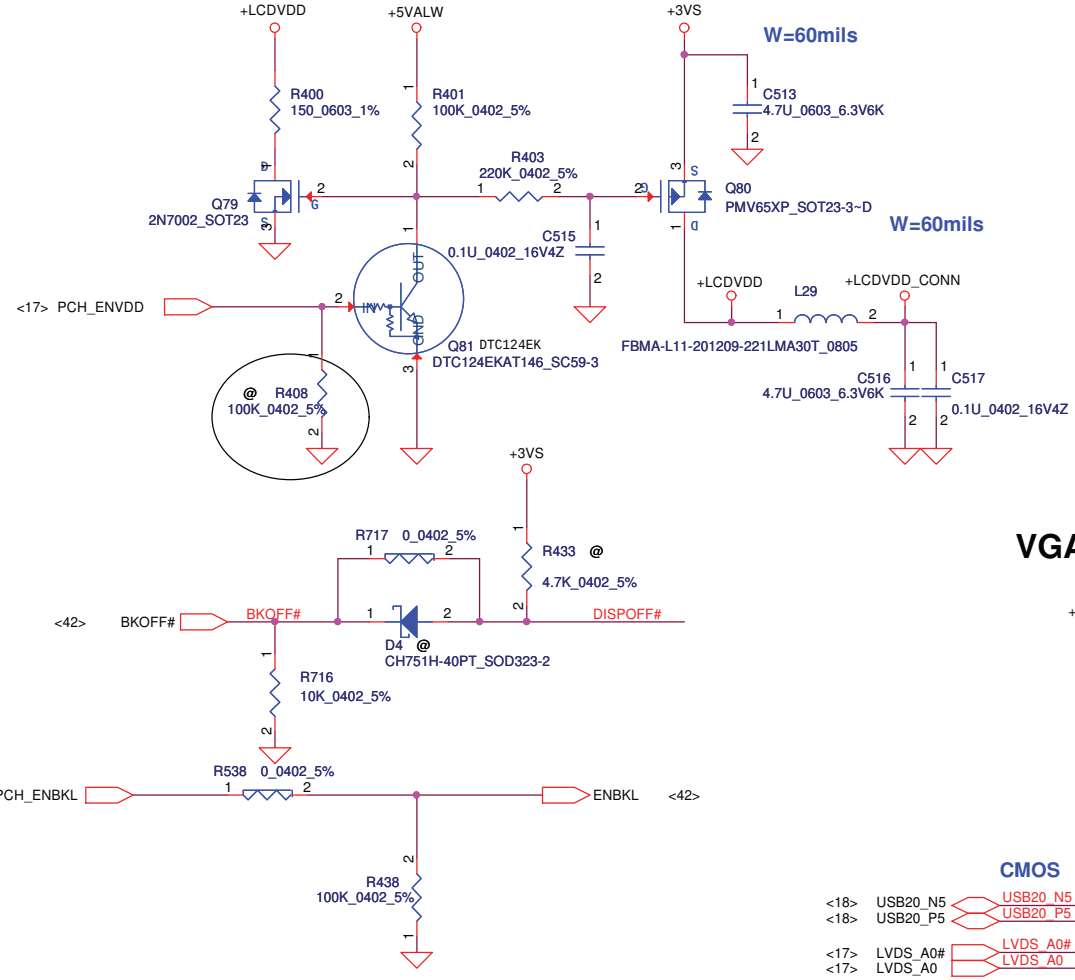
Compal Electronics, Inc.

Title: N13X_MISC

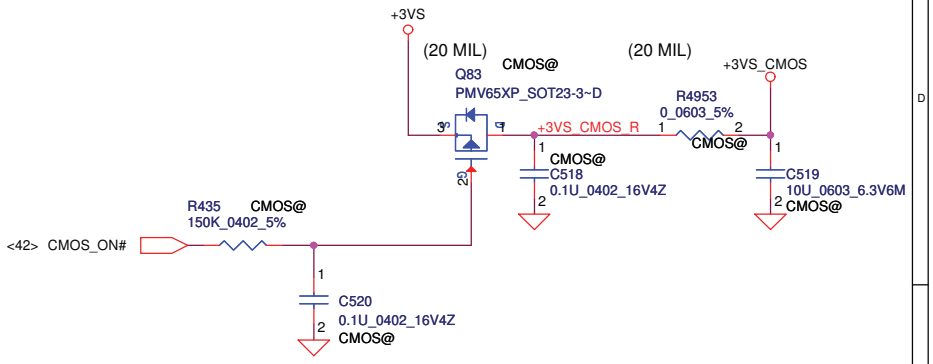
Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 32 of 60

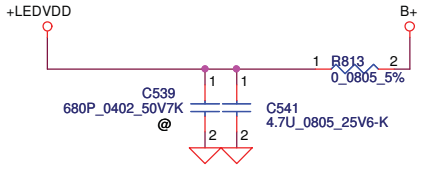
LCD POWER CIRCUIT

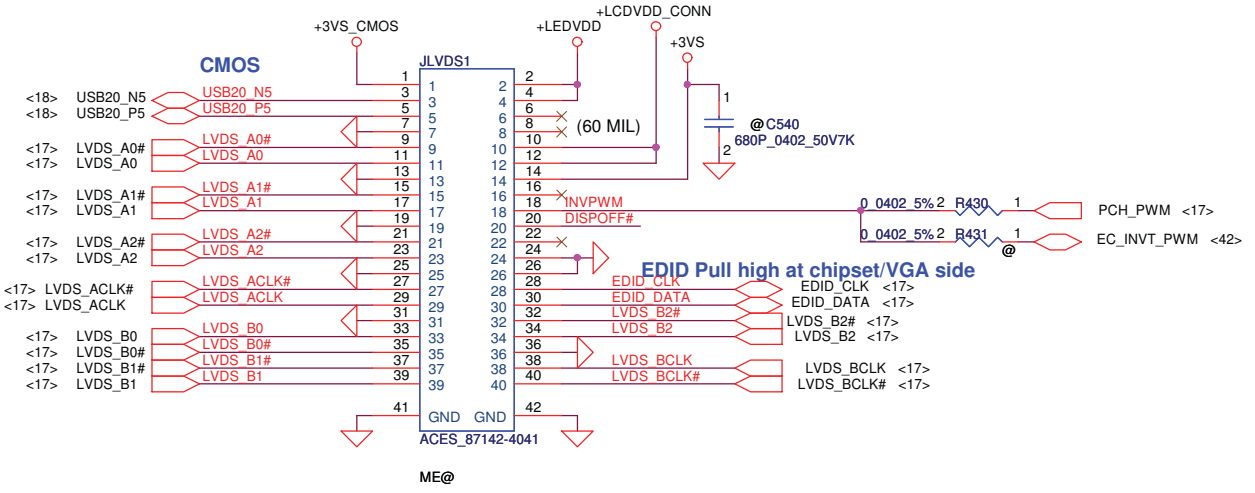


CMOS Camera



VGA LCD/PANEL BD. Conn.





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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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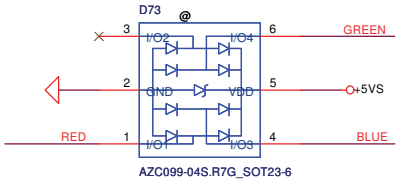
Compal Electronics, Inc.

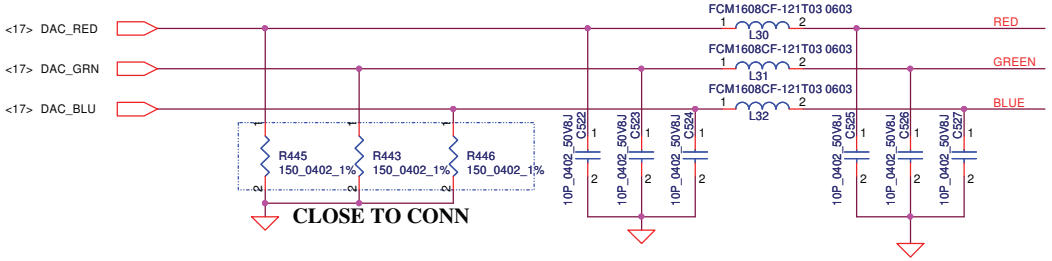
Title: LVDS/CAMERA

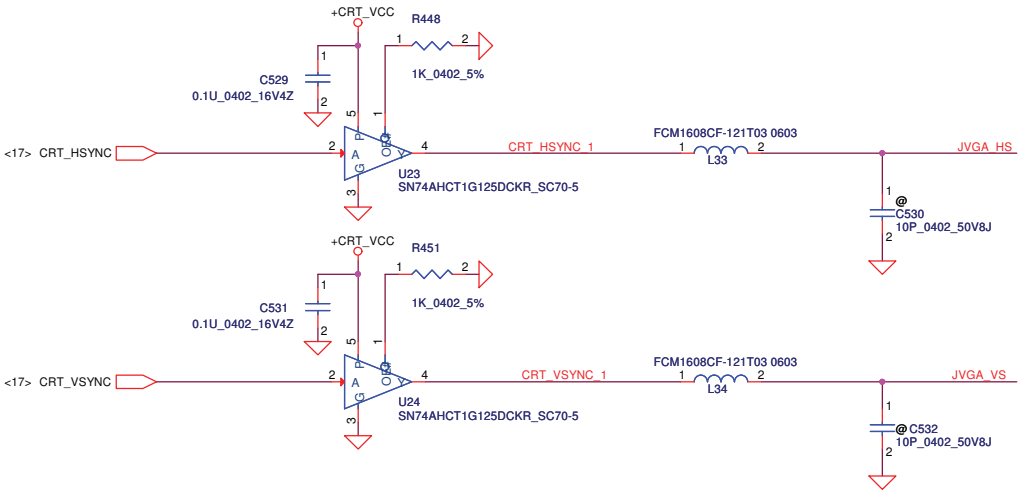
Size	Document Number	Rev
Custom	LA-7983P	0.3

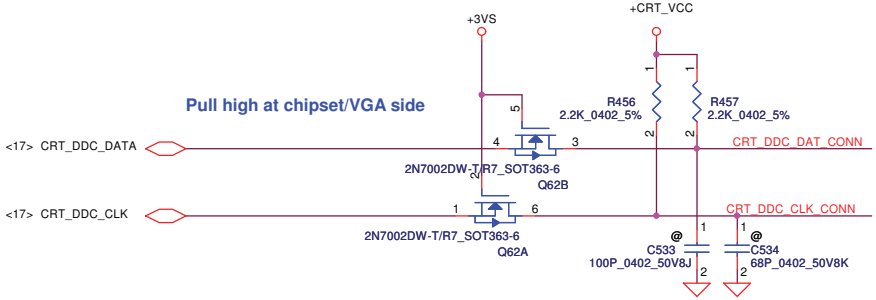
Date: Thursday, January 05, 2012 Sheet 33 of 60

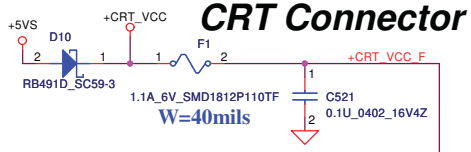
CRT Connector

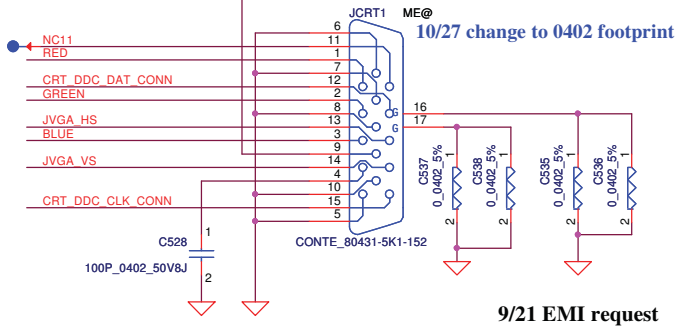




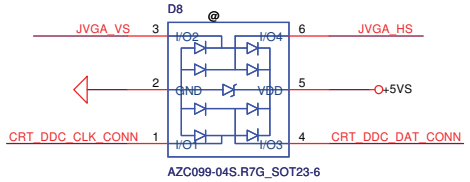








9/21 EMI request
0ohm and mount



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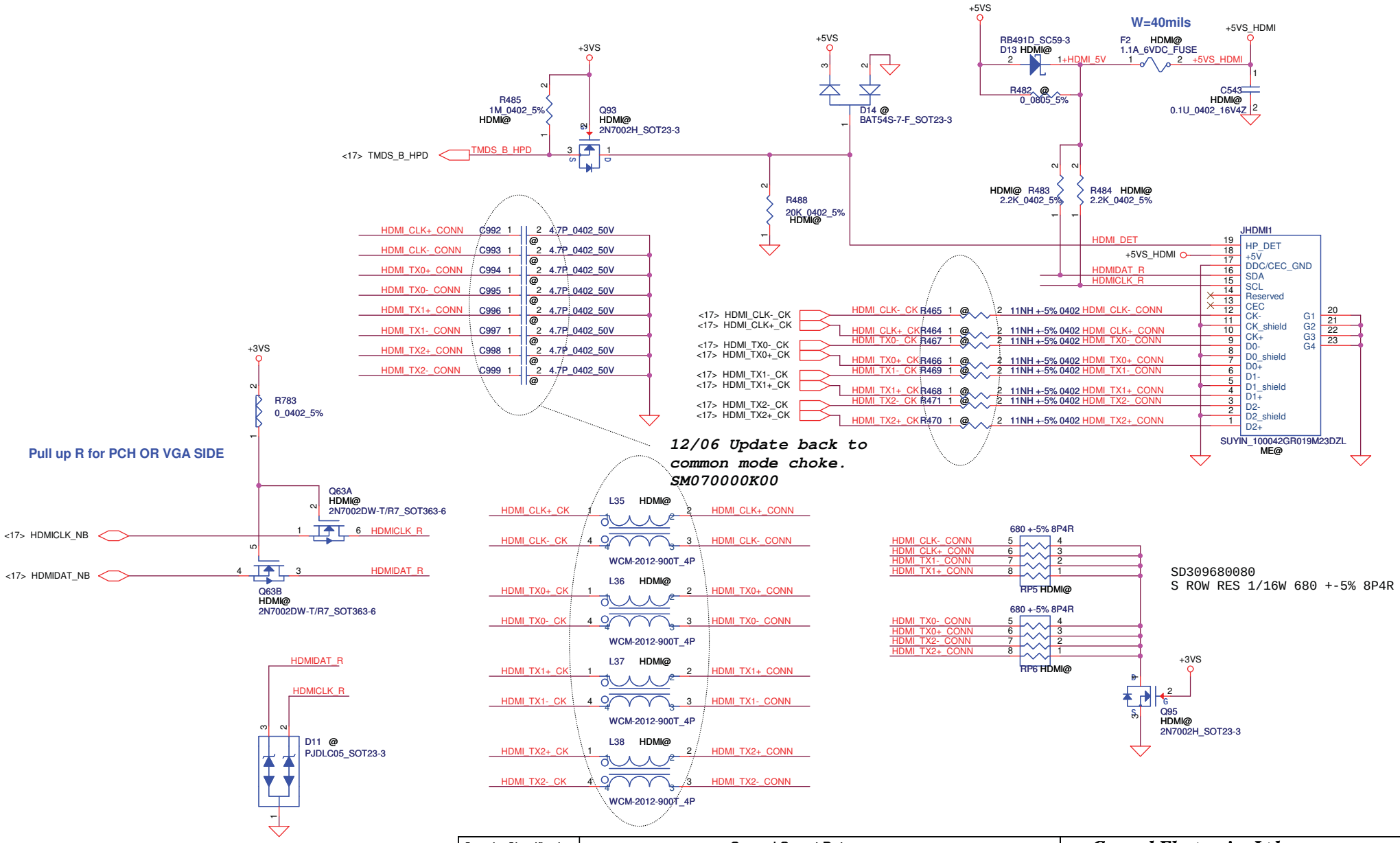
Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 34 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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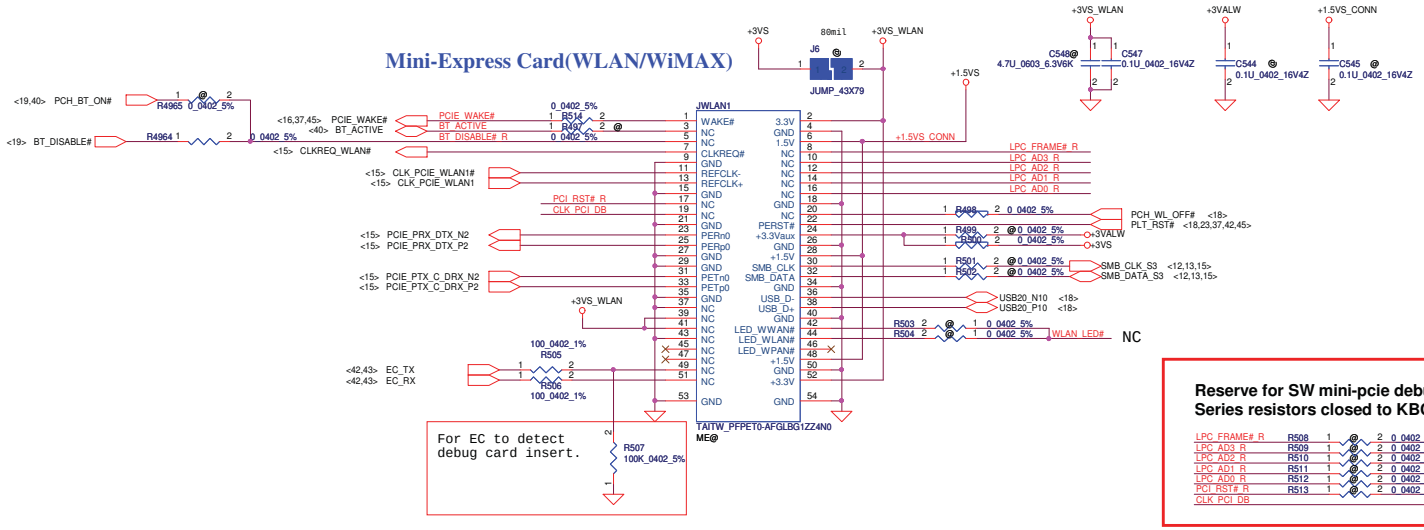
Compal Electronics,Ltd.

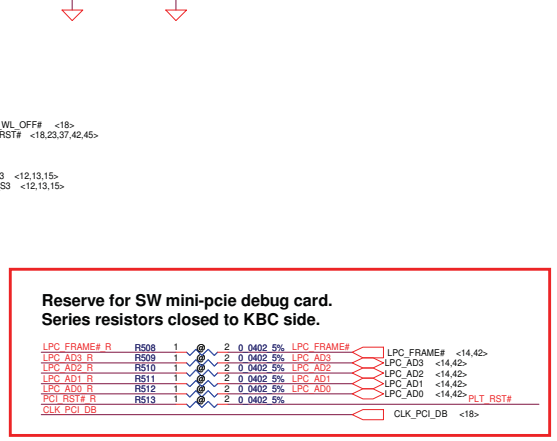
Title: HDMI CONN

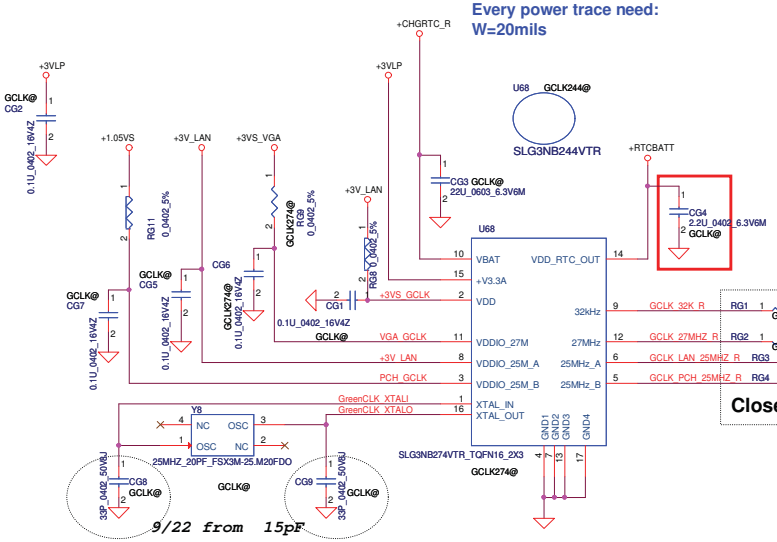
Size: B | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 35 of 60

Mini-Express Card for WLAN/WiMAX(Half)



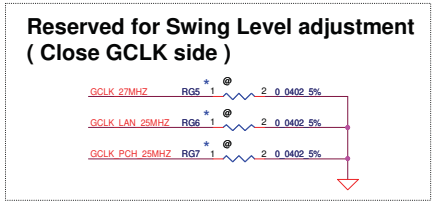




For GreenCLK generate CLK:
Mount: All parts in this page except
Swing Level RES (Marked "*")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969

PCH_32.768K
NV_GPU
LAN
PCH_25M

Close to GCLK



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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Compal Electronics, Inc.			
Title: Mini-Card/Green CLK			
Size	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 36 of 60		

Atheros request can't disable LAN power

+3VALW +3V_LAN

J18 JUMP_43X79

Q130 LP2301ALT1G_SOT23

<42> LAN_PWR_ON# — LAN_PWR_ON# — R4977 10K_0402_5%

C1001 .1U_0402_16V7K

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN — R525 4.7K_0402_5% @ — <18,23,36,42,45> PLT_RST# — PLT_RST#

Layout Notice : Place as close chip as possible.

Close together

+LX

+1.1_DVDDL — R1357 0_0402_5% — +LX_R

L74 SWR@ 4.7UH_SIA4012-4R7M_20% — +LX

C935 @ 1000P_0402_50V7K

C936 0.1U_0402_16V4Z

C937 10U_0603_6.3V6M

Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

L77 FBMA-L11160808601LMA10T_2P — +1.1_AVDDL_L

L78 SWR@ FBMA-L11160808601LMA10T_2P — +1.1_AVDDL — +1.1_DVDDL

C967 0.1U_0402_16V4Z

C980 1U_0402_6.3V4Z

C317 4.7U_0603_6.3V6K

Place close to Pin34

U41 8162@ AR8162-AL3A-R

SA000050E00_S IC AR8161-AL3A-R QFN 40P E-LAN CTRL
SA000052J10_S IC AR8162-AL3A-R QFN 40P E-LAN CTRL

H --> Overclocking mode
L --> Not overclocking mode

+3V_LAN — R1367 0_0402_5% — +AVDDH_AVDD3.3

C948 0.1U_0402_16V4Z

C949 1U_0402_6.3V4Z

Place close to Pin16

Place Close to Chip

U41 GIGA@ Atheros AR8151/AR8161

<15> PCIE_PRX_DTX_N1 — C946 .1U_0402_16V7K — PCIE_PRX_C_DTX_N1 — 29 TX_N

<15> PCIE_PRX_DTX_P1 — C947 .1U_0402_16V7K — PCIE_PRX_C_DTX_P1 — 30 TX_P

<15> PCIE_PTX_C_DRX_N1 — 36 RX_N

<15> PCIE_PTX_C_DRX_P1 — 35 RX_P

<15> CLK_PCIE_LAN# — 32 REFCLK_N

<15> CLK_PCIE_LAN — 33 REFCLK_P

PLT_RST# — 2 PERST#

<16,36,45> PCIE_WAKE# — R1369 @ 0_0402_5%

<42> LAN_WAKE# — R1370 @ 0_0402_5% — PCIE_WAKE#_R — 3 WAKE#

+3V_LAN — R521 4.7K_0402_5% @

Vendor recommand reseve the PU resistor close LAN chip

25 SMCLK

26 SMDATA

28 NC

27 TESTMODE

+3V_LAN — R520 4.7K_0402_5% @ — LAN_XTALO — 7 XTLO

LAN_XTALI_R — 8 XTLI

<15> CLKREQ_LAN# — 4 CLKREQ#

+1.1_AVDDL — 13 AVDDL

+1.1_AVDDL — 19 AVDDL

+1.1_AVDDL — 31 AVDDL

+1.1_AVDDL_L — 34 AVDDL

+1.1_AVDDL — 6 AVDDL_REG/AVDDL

41 GND

AR8161-AL3A-R_QFN40_5X5

38 LED_0 — ACTIVITY — ACTIVITY <38>

39 LED_1 — LAN_LINK# — LAN_LINK# <38>

23 LED_2 — LAN_CLK_SEL — R4958 @10K_0402_5%

TRXN0 12 MDI0- — MDI0- <38>

TRXP0 11 MDI0+ — MDI0+ <38>

TRXN1 15 MDI1- — MDI1- <38>

TRXP1 14 MDI1+ — MDI1+ <38>

TRXN2 18 MDI2- — MDI2- <38>

TRXP2 17 MDI2+ — MDI2+ <38>

TRXN3 21 MDI3- — MDI3- <38>

TRXP3 20 MDI3+ — MDI3+ <38>

10 RBIAS — LAN_RBIAS — R1371 2.37K_0402_1%

Place Close to PIN1

1 VDD33 — +3V_LAN

40 LX — +LX

5 VDDCT/ISOLAN — +1.7_VDDCT — R1372 30K_0402_1% — +3VS

24 DVDDL/PPS 37 DVDDL_REG/DVDDL — +1.1_DVDDL

16 AVDDH/AVDD33 — +AVDDH_AVDD3.3

22 AVDDH — +2.7_AVDDH

9 AVDDH_REG — +2.7_AVDDH

LDO Mode

LAN_LINK# — R4959 10K_0402_5% — LDO@

Place Close to PIN1

+3V_LAN

1000P_0402_50V7K

C950 0.1U_0402_16V4Z

C951 1U_0402_6.3V4Z

C952 10U_0603_6.3V6M

C953 10U_0603_6.3V6M

C954

C956 0.1U_0402_16V4Z — Near Pin13

C957 0.1U_0402_16V4Z — Near Pin19

C958 0.1U_0402_16V4Z — Near Pin31

C959 1U_0402_6.3V4Z

C960 0.1U_0402_16V4Z — Near Pin6

C961 0.1U_0402_16V4Z

C962 1U_0402_6.3V4Z — Near Pin9

C963 0.1U_0402_16V4Z — Near Pin22

C964 0.1U_0402_16V4Z

C965 1U_0402_6.3V4Z — Near Pin37

<15> PCH_LAN_48M — C981 @ 5P_0402_50V8 — LAN_XTALI

Place Close to C968

Y6 25MHZ_20PF_FSX3M-25.M20FDO — NC OSC OSC NC — LAN_XTALO

C968 15P_0402_50V8J

C969 15P_0402_50V8J

<36> GCLK_LAN_25MHZ — GCLK_LAN_25MHZ — C988 5P_0402_50V8 — LAN_XTALI — R1373 0_0402_5% — LAN_XTALI_R

CRYSTAL@ GCLK@

3.3V : Enable switching regulator
0V : Disable switching regulator

12/29, Y6 changes to SJ10000E800
S CRYSTAL 25MHZ 10PF +-20PPM 7V25000014

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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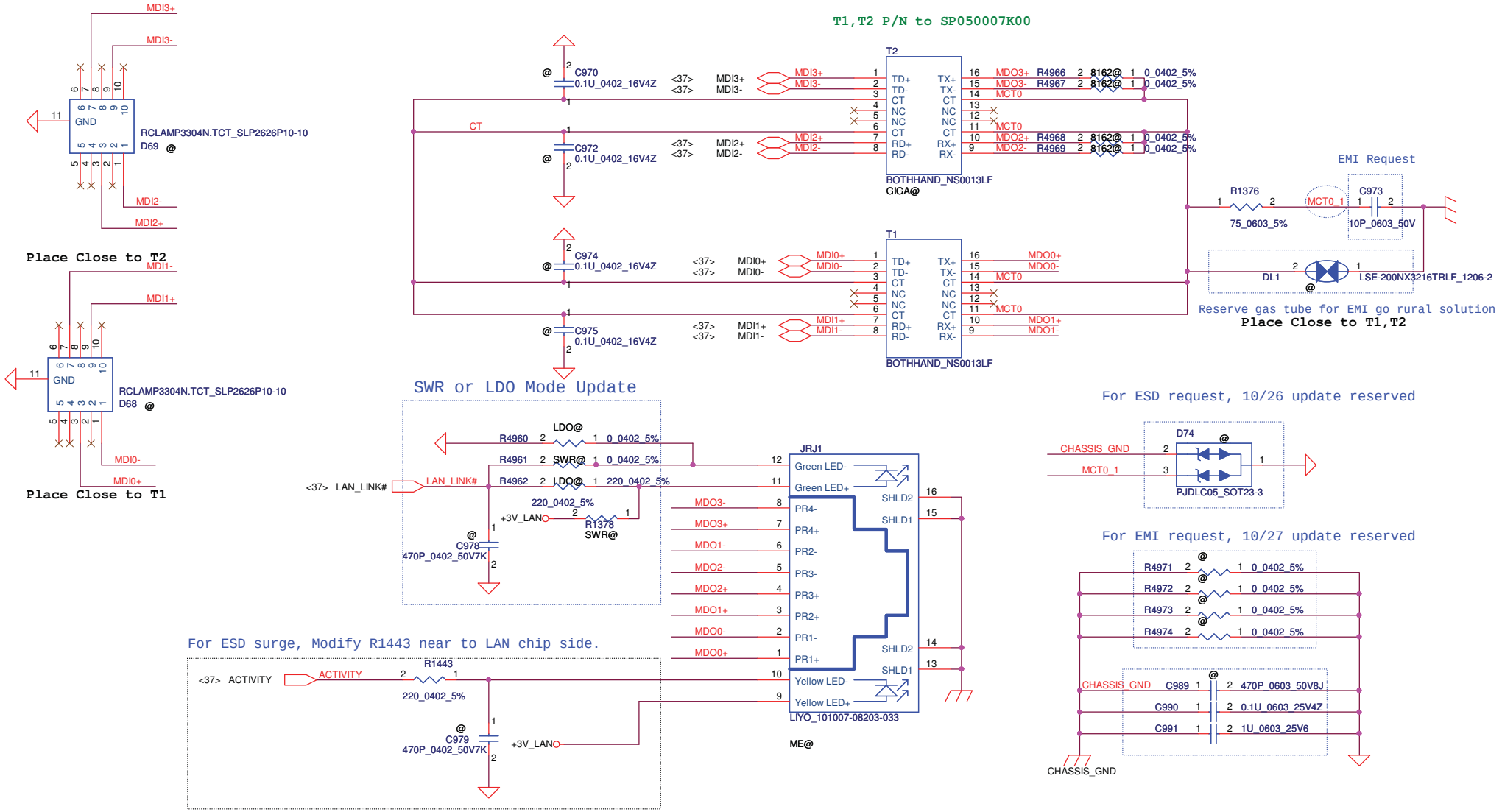
Compal Electronics, Inc.

Title: LAN-AR8151/8161

Size: Custom | Document Number: LA-7983P | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 37 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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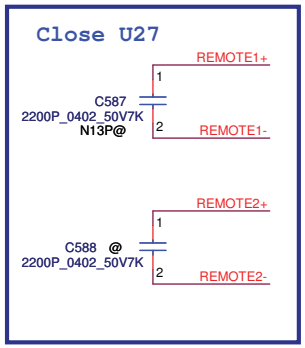
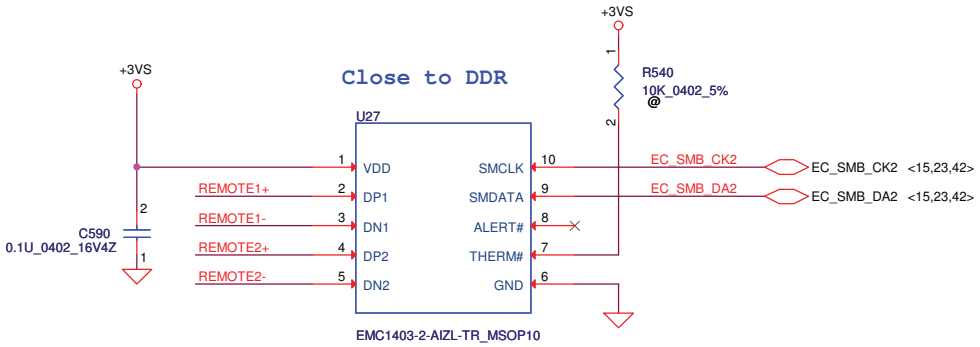
Compal Electronics, Inc.

Title: LAN_Transformer

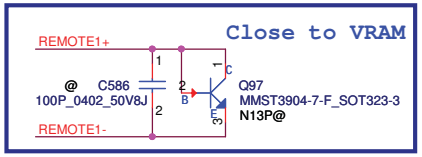
Size: B | Document Number: LA-7983P | Rev: 0.3

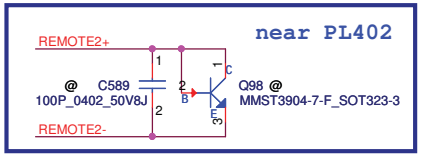
Date: Thursday, January 05, 2012 | Sheet 38 of 60



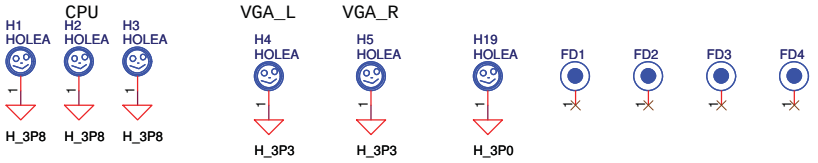


Address 1001_101xb

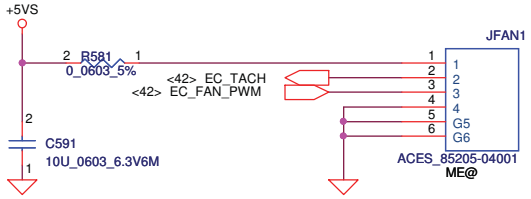


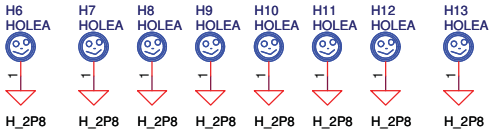


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

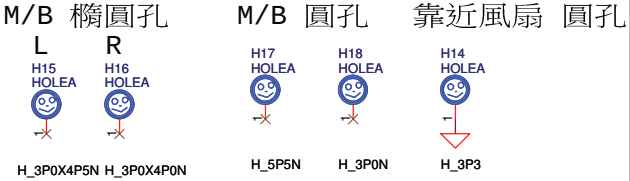


FAN1 Conn





2P8 * 8pcs



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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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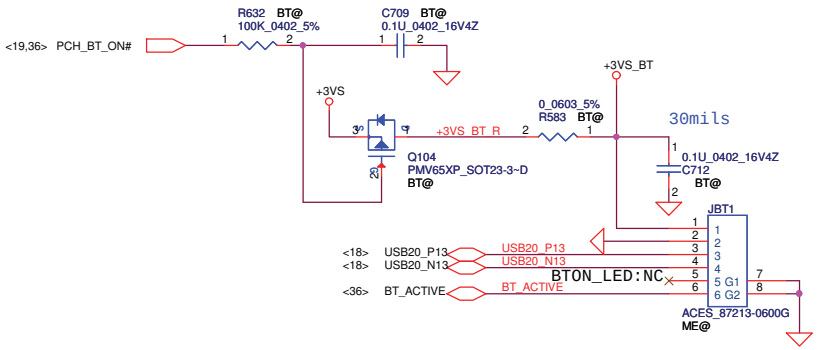
Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

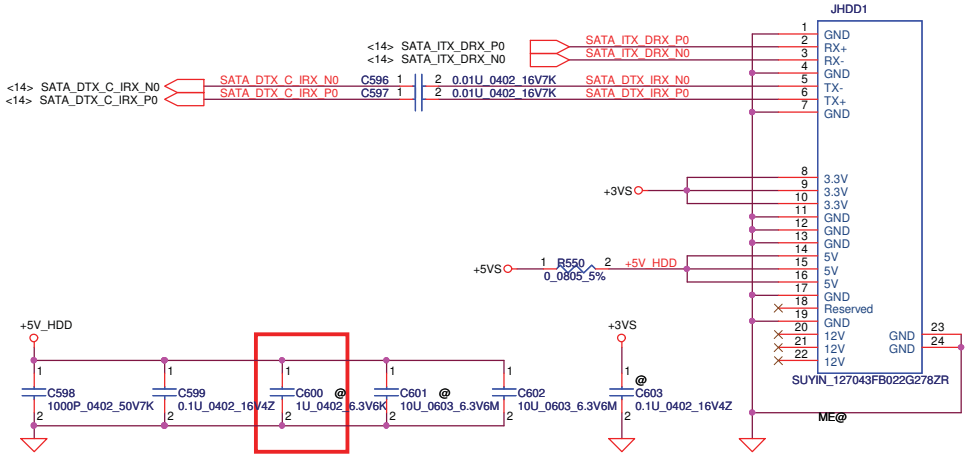
Size: B | Document Number: **LA-7983P** | Rev: 0.3

Date: Thursday, January 05, 2012 | Sheet 39 of 60

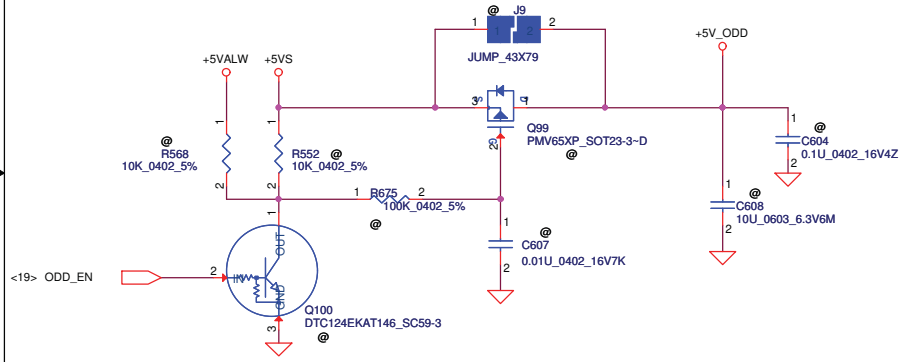
BT MODULE CONN



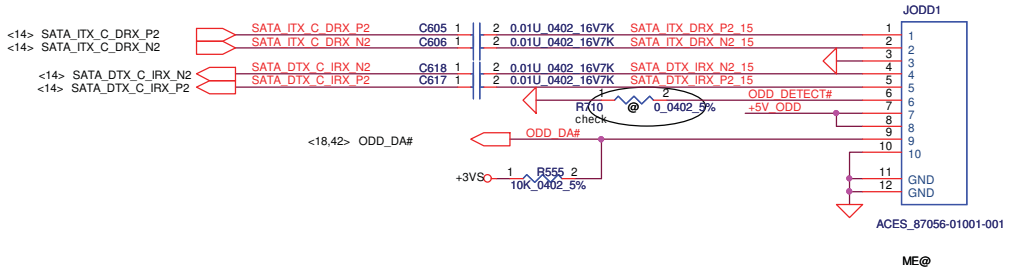
SATA HDD Conn.



ODD Power Control



SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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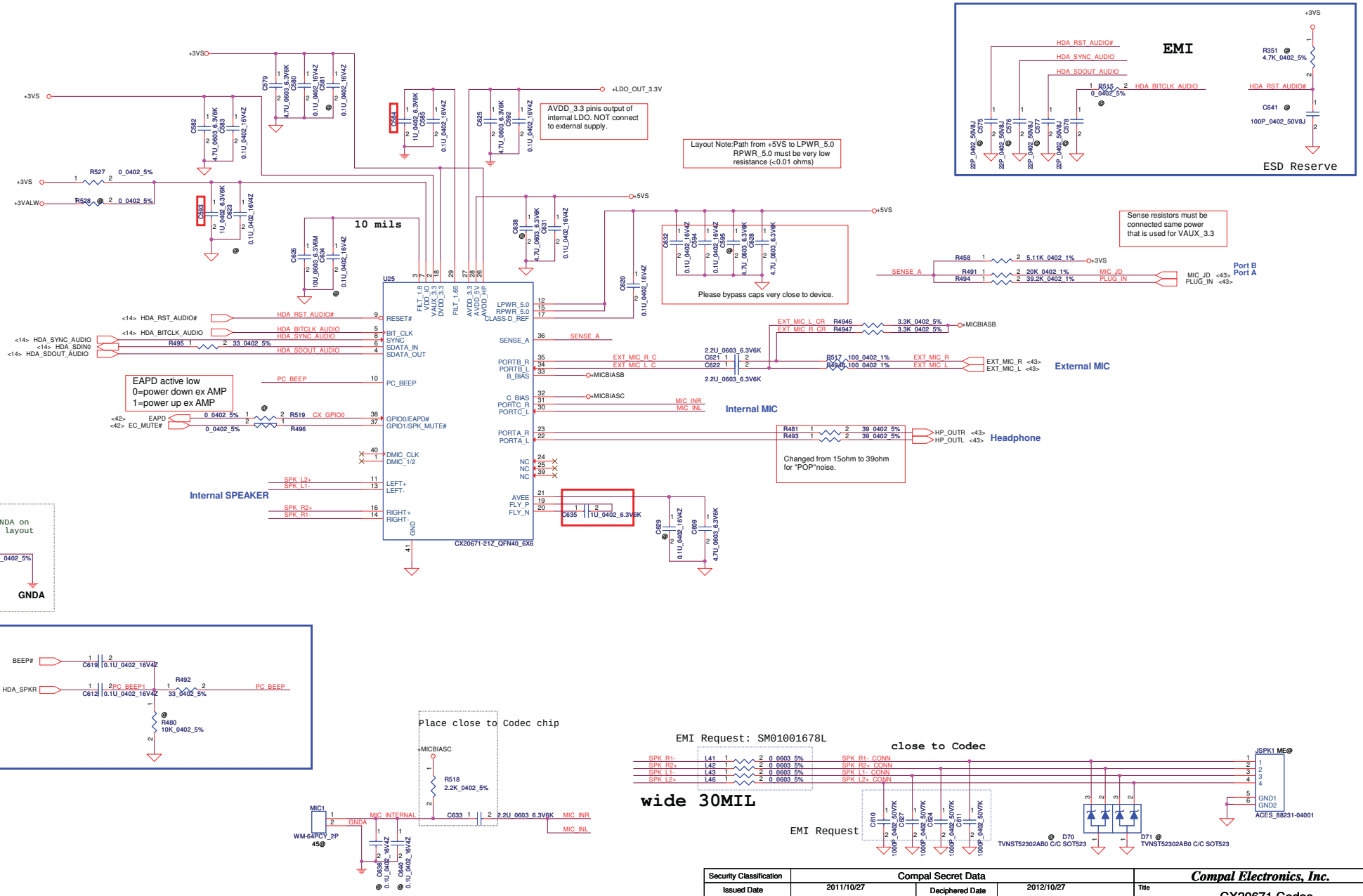
Compal Electronics, Inc.

Title: HDD/ODD/BT Connector

Size	Document Number	Rev
Custom	LA-7983P	0.3

Date: Thursday, January 05, 2012 Sheet 40 of 60

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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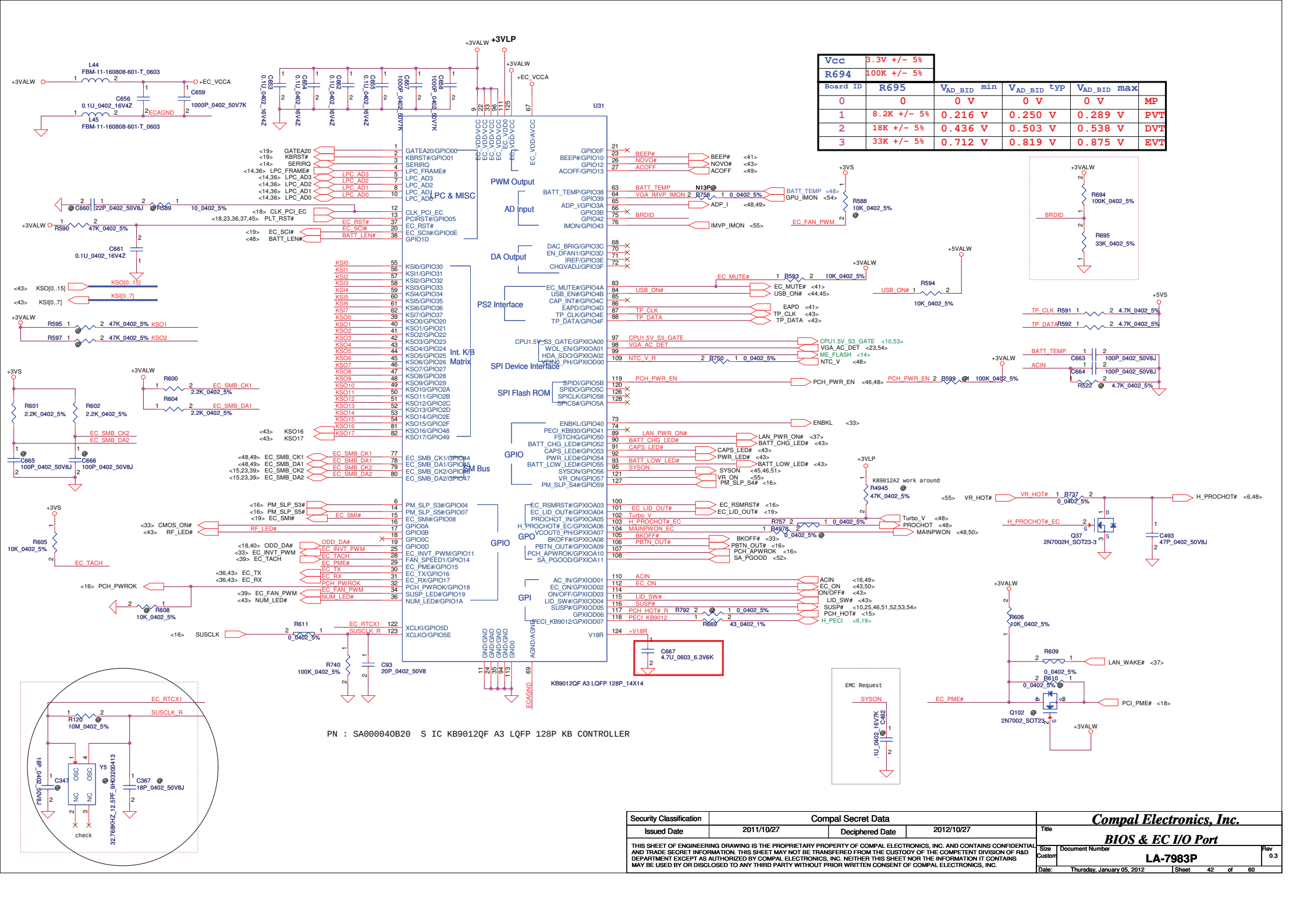
Compal Electronics, Inc.			
Title	CX20671 Codec		
Size	Document Number		Rev
Custom	LA-7983P		0.3
Date: Thursday, January 05, 2012	Sheet	41	of 60


Vcc 3.3V +/- 5%
R694 100K +/- 5%
Board ID | R695 | VAD_BID min | VAD_BID typ | VAD_BID max
0 | 0 | 0 V | 0 V | 0 V | MP
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | PVT
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | DVT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | EVT
U31
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
KB9012QF A3 LQFP 128P_14X14
PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER
EMC Request
Security Classification | Compal Secret Data
Issued Date | 2011/10/27 | Deciphered Date | 2012/10/27
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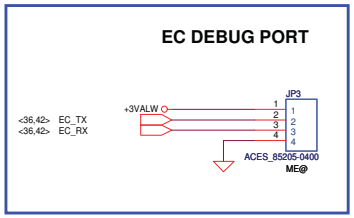
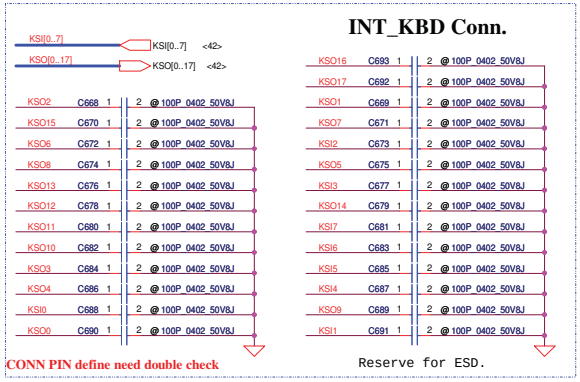
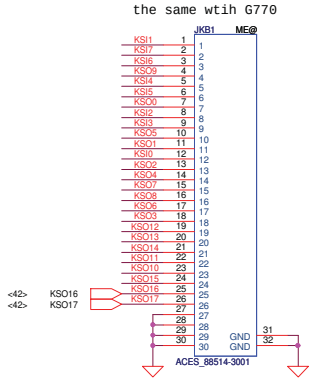
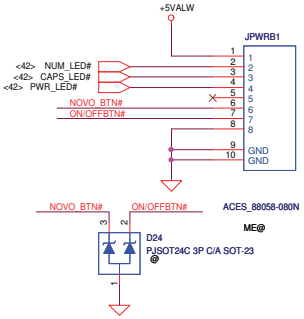
Compal Electronics, Inc.
Title: BIOS & EC I/O Port
Size: Custom | Document Number: LA-7983P | Rev: 0.3
Date: Thursday, January 05, 2012 | Sheet 42 of 60



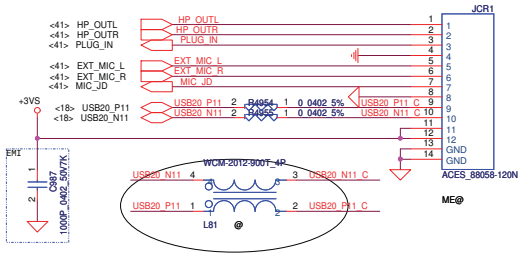




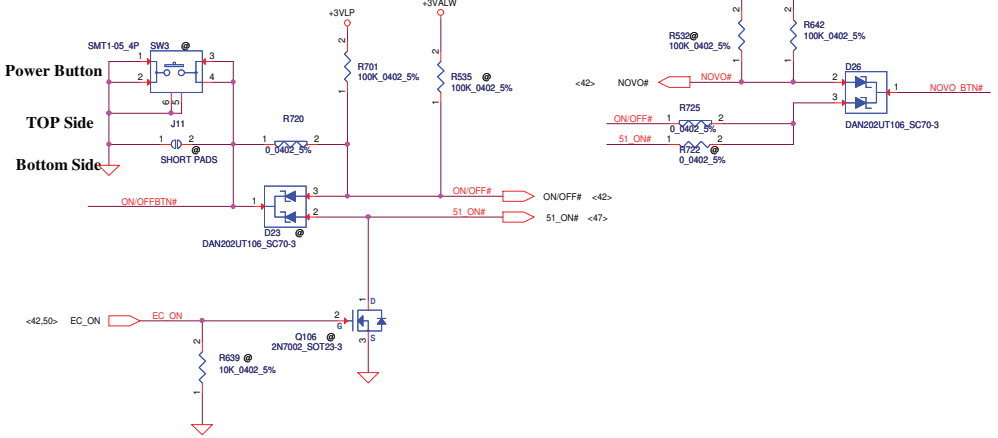
Power Bottom Board Conn. 8pin



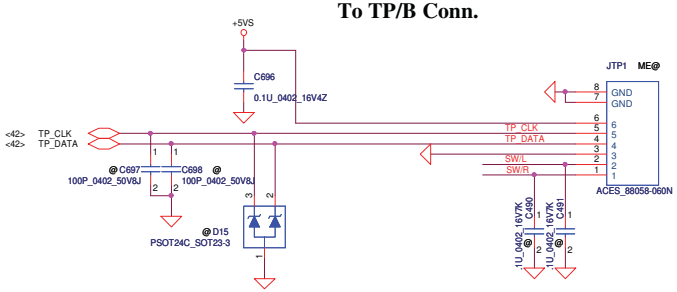
Card Reader/Audio Jack SB CONN



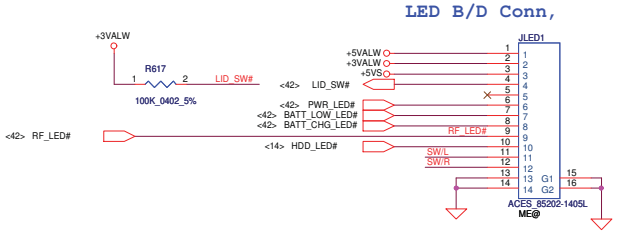
ON/OFF switch



To TP/B Conn.



LED B/D Conn,



pin 1 2 3 4 5
14 VDD CLK DAT L R GND

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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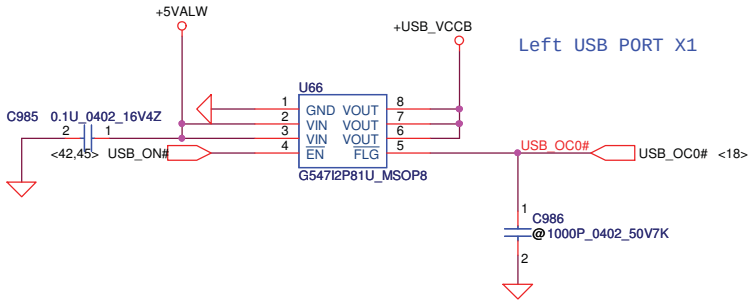
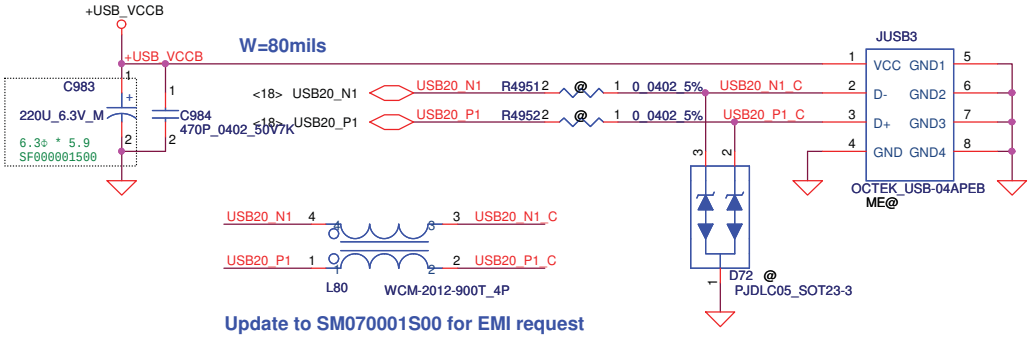
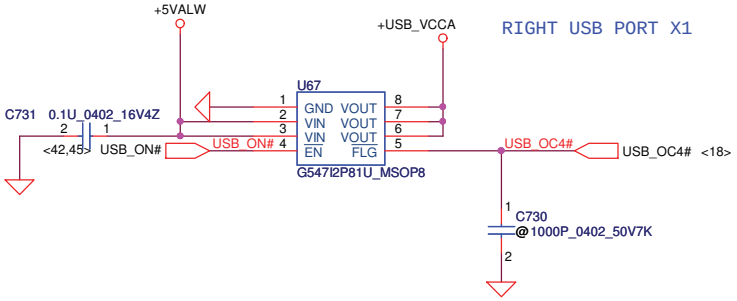
Compal Electronics, Inc.			
Title	ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA-7983P		Rev 0.3
Date: Thursday, January 05, 2012	Sheet 43 of 60		

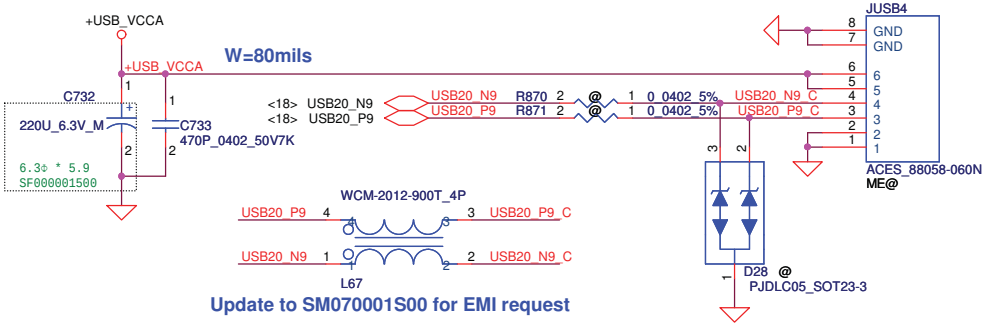
Left Ext.USB Conn.





Right Ext.USB Cable Conn.





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Compal Electronics, Inc.

Title: USB ext. ports

Size	Document Number	Rev
B	LA-7983P	0.3

Date: Thursday, January 05, 2012 Sheet 44 of 60

+1.5V to +1.05V Transfer

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

10/11 Corrected.

10/20 add 10k pu

10/14 R1172 modify to 300K

10/14 R747 modify to 430K
C832 to 1U.

10/14 Modify to +3V from +3VALW

12/07 update to SA00002AA00

For EMI request

Update to SM070001S00 for EMI request

W=80mils

2A/Active Low

Place TX AC coupling Cap (C843~C850). Close to connector

Security Classification	Compal Secret Data		
Issued Date	2011/10/27	Deciphered Date	2012/10/27

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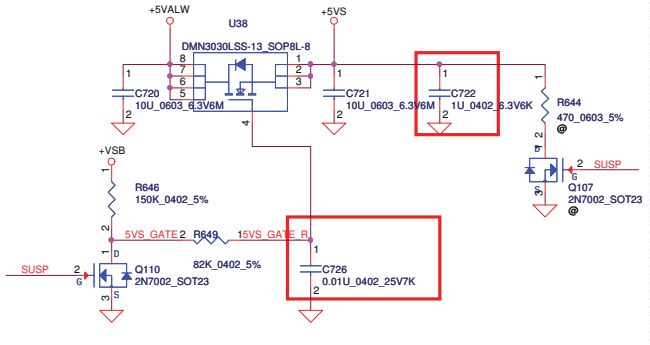
Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

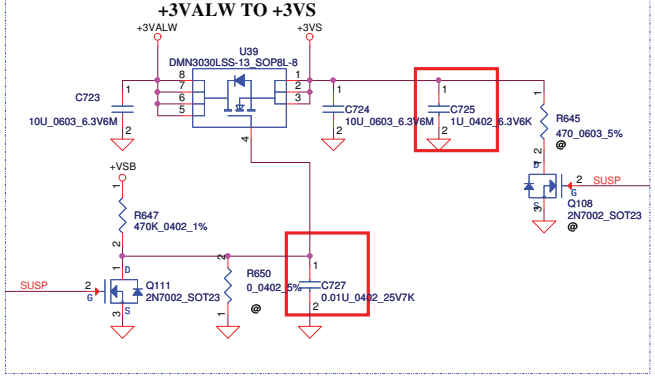
Size	Document Number	Rev
Custom		0.3

Date: Thursday, January 05, 2012 Sheet 45 of 60

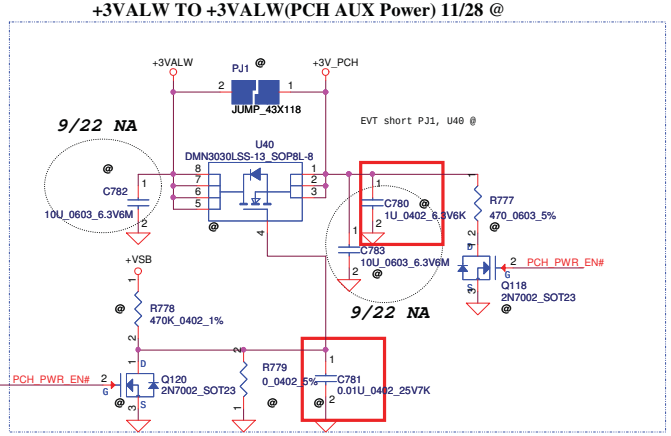
+5VALW TO +5VS

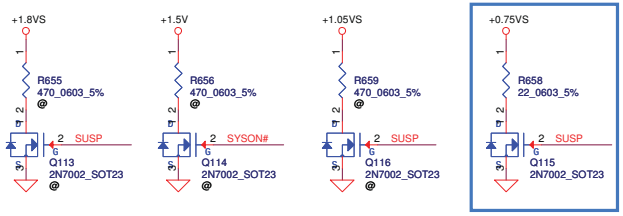


+3VALW TO +3VS



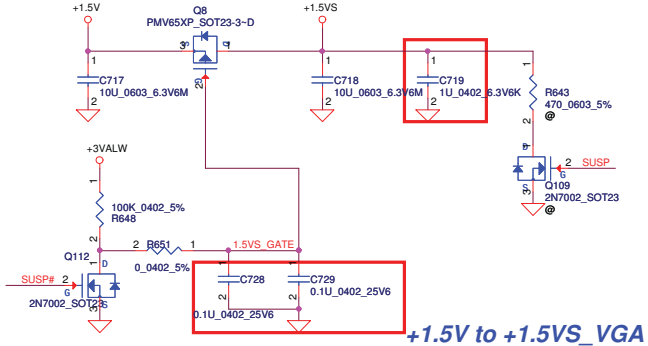
+3VALW TO +3VALW(PCH AUX Power) 11/28 @

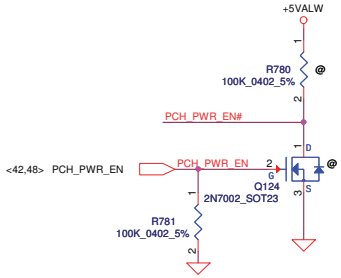


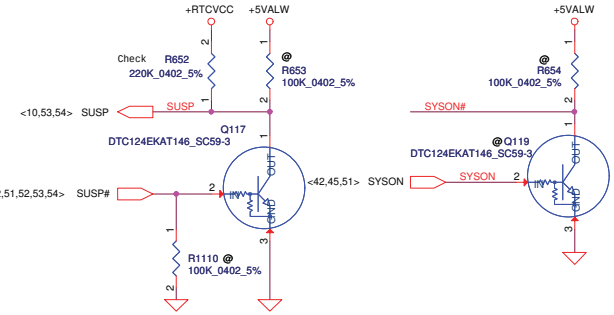


For Intel S3 Power Reduction.

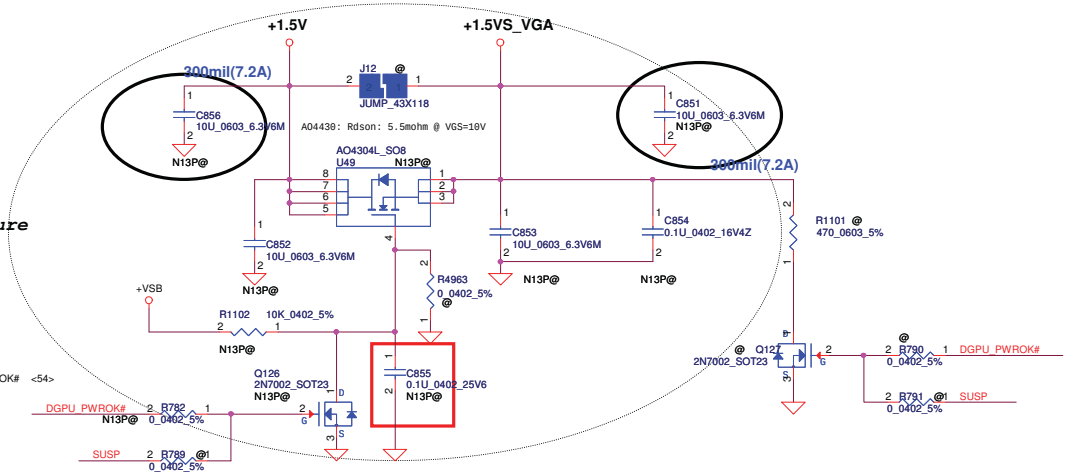
+1.5V to +1.5VS



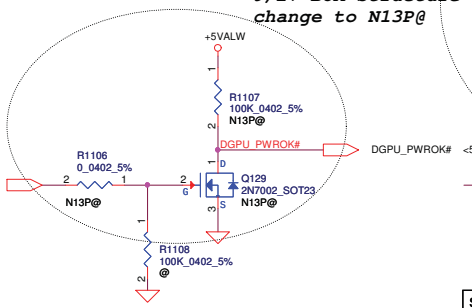




+1.5V to +1.5VS_VGA Transfer



9/27 BOM Structure change to N13P@



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Issued Date	2011/10/27	Deciphered Date	2012/10/27

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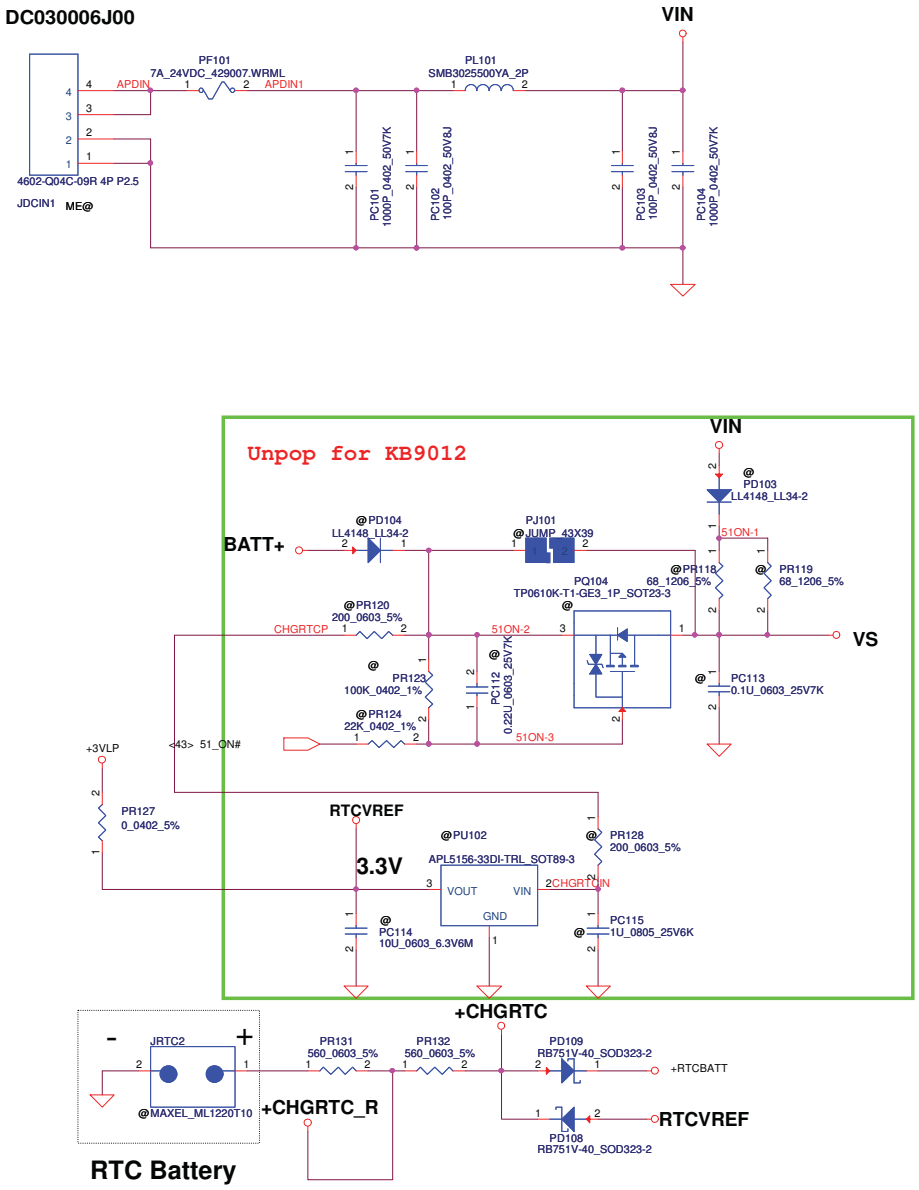
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-7983P	0.3

Date: Thursday, January 05, 2012 | Sheet 46 of 60



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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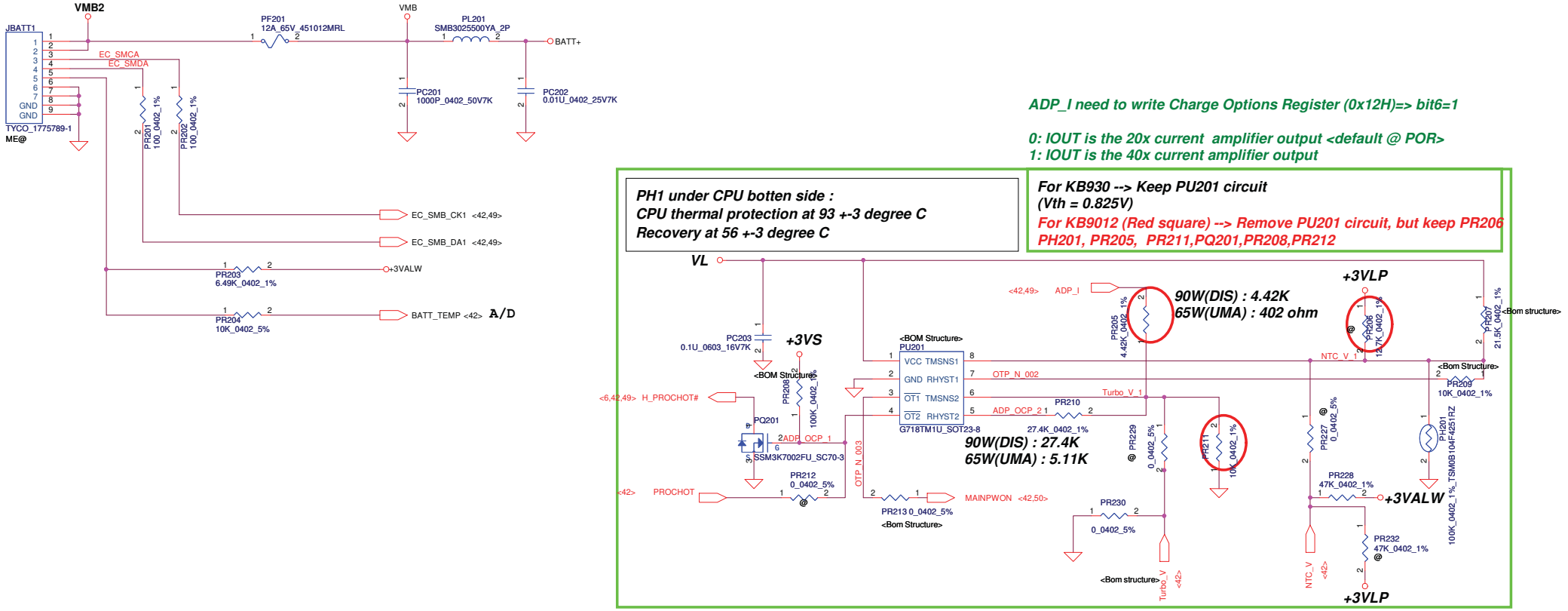
Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 05, 2012 | Sheet 47 of 60



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Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 05, 2012 | Sheet 48 of 60

Need EC write ChargeOption() bit[8]=1
Setting (ACP to PHASE Rising Threshold)=1350mV(min)

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

For disable pre-charge circuit.

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

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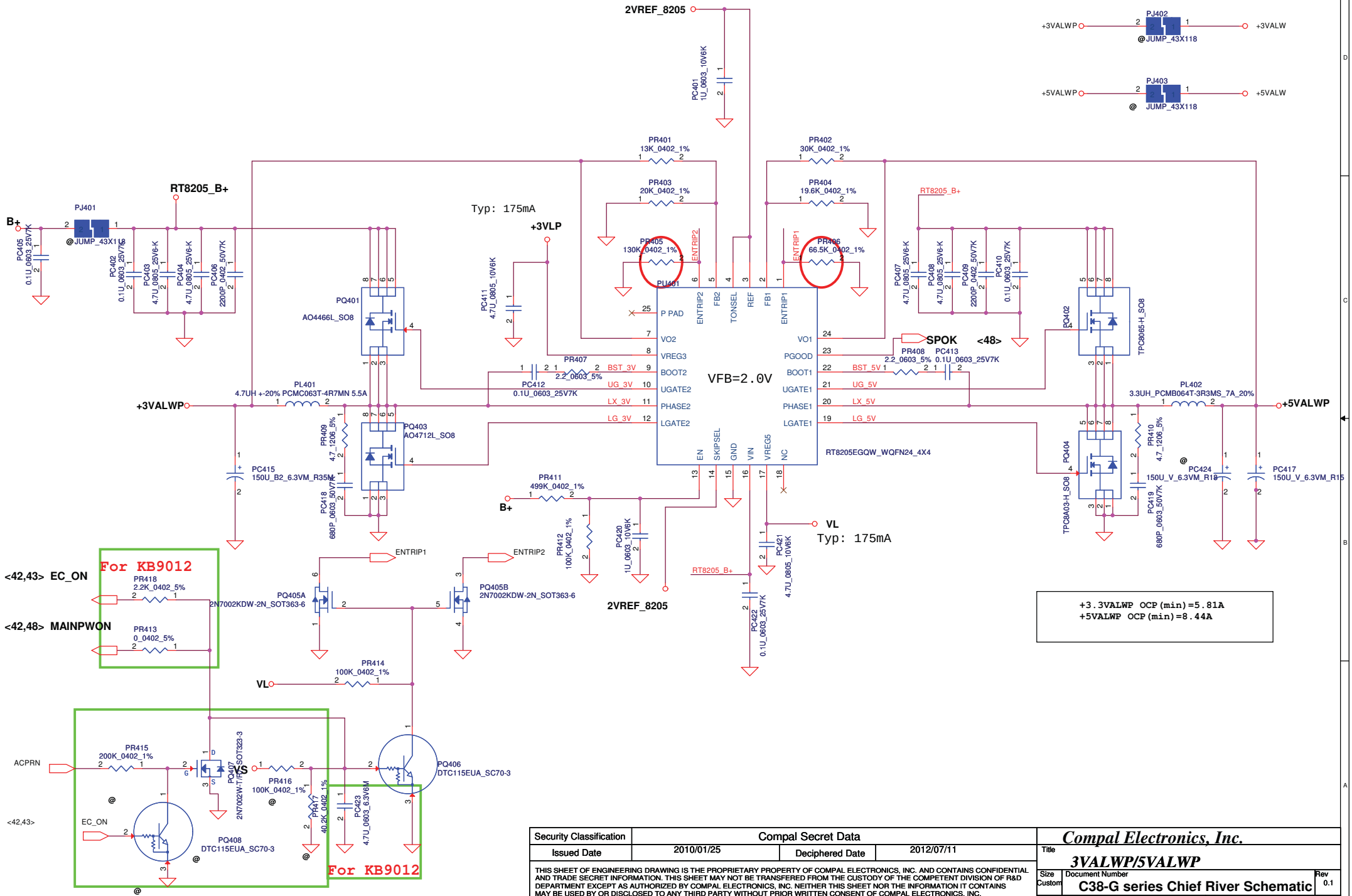
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 05, 2012 | Sheet 49 of 60

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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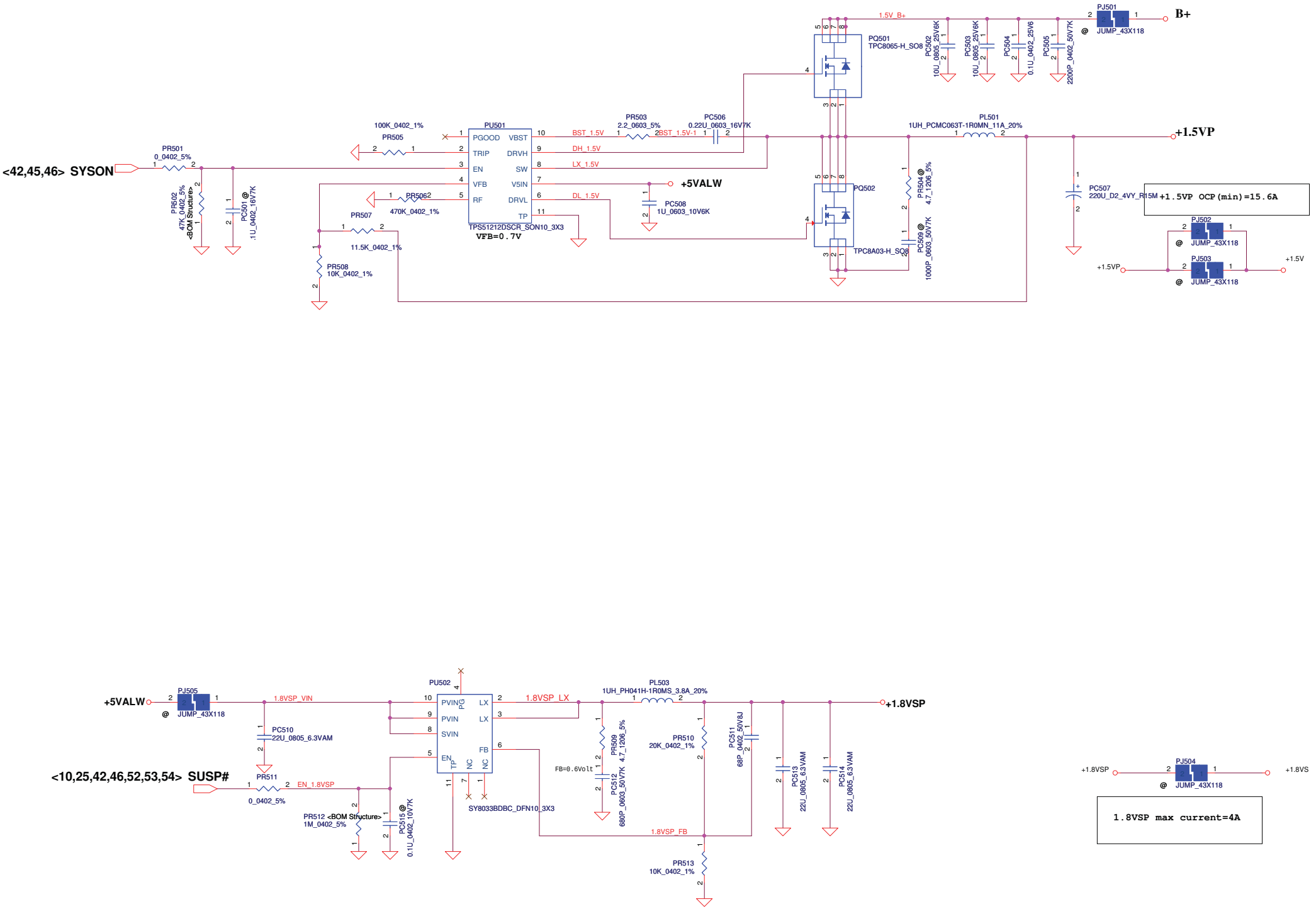
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 05, 2012 | Sheet 50 of 60



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1
Date: Thursday, January 05, 2012	Sheet 51 of 60	

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

+VCCSAP PJ602 JUMP_43X118 +VCCSA

+3VS PR601 1K_0402_5% H_VCCSA_VID1 <10>
PR602 100K_0402_5% +VCCSA_PWRGD
H_VCCSA_VID0 <10>
PR603 1K_0402_5%
<42> SA_PGOOD

+5VALW PR604 10_0402_1% PC602 2.2U_0603_10V7K
PC601 1U_0603_10V6K DGBRM_PWRGD +VCCSA_VID1 +VCCSA_VID0
+VCCSA_EN PR605 0_0402_5% +V1.05S_VCCP_PWRGOOD <53>

PU601 TPS51461RGER_QFN24_4X4
V5DRV V5FILT PGOOD VID1 VID0 EN
PGND PGND PGND VIN VIN VIN
BST SW SW SW SW SW TP
GND VREF COMP SLEW VOUT MODE

+VCCSA_BT PR606 0_0603_5% PC603 0.22U_0603_16V7K +VCCSA_BT
PL601 0.47UH_FDVE0630-H-R47M=P3_17.7A_20%
+VCCSA_PHASE PR607 4.7_1206_5% PC604 1000P_0603_50V7K
+VCCSAP
PC605 22U_0805_6.3V6M PC606 22U_0805_6.3V6M PC607 0.1U_0402_10V7K PC608 22U_0805_6.3V6M PC609 22U_0805_6.3V6M PC610 2200P_0402_50V7K PC611 22U_0805_6.3V6M PC612 22U_0805_6.3V6M

+3VALW PJ601 JUMP_43X118 +VCCSA_PWR_SRC
2200P_0402_50V7K PC613 0.1U_0603_25V7K PC614 10U_0805_6.3V6M PC615 10U_0805_6.3V6M PC616

PR608 33K_0402_5%
PC617 0.22U_0402_10V6K
PC618 3300P_0402_50V7K PR610 5.1K_0402_1%
PC619 0.01U_0402_25V7K
PR609 100_0402_5%
PR611 0_0402_5% +VCCSA_SENSE <10>

+3VS PR612 100K_0402_5%
<53> +V1.05S_VCCP_PWRGOOD
PR613 0_0603_5% PC624 0.22U_0603_16V7K
PR614 66.5K_0402_1%
PR615 0_0402_5% <10,25,42,46,51,53,54> SUSP#
PC625 0.1U_0402_16V7K
PR616 470K_0402_1%

PU602 TPS51212DSCR_SON10_3X3
PGOOD VBST TRIP DRVH EN SW VFB VSIN RF DRVL TP
TRIP_+V1.05S_VCCPP EN_+V1.05S_VCCPP FB_+V1.05S_VCCPP RF_+V1.05S_VCCPP
BST_+V1.05S_VCCPP UG_+V1.05S_VCCPP SW_+V1.05S_VCCPP +V1.05S_VCCPP_5V LG_+V1.05S_VCCPP

+5VALW PC626 1U_0603_6.3V6M

+V1.05S_VCCPP_B+ PJ603 JUMP_43X118 B+
PQ601 TPC8037-H_SO8
PC620 0.1U_0402_25V6 PC621 2200P_0402_50V7K PC622 4.7U_0805_25V6-K PC623 4.7U_0805_25V6-K
PQ602 TPC8A03-H_SO8
PL602 1UH_PCMC063T-1R0MN_11A_20%
+V1.05S_VCCPP
PR617 4.7_1206_5% PC628 1000P_0603_50V7K
PC627 0.1U_0402_10V7K
PC631 220U_D2_4VY_R15M
+V1.05S_VCCPP PJ604 JUMP_43X118 +V1.05S_VCCP

PC629 1000P_0402_50V7K PR618 1.2K_0402_1%
PR619 4.32K_0402_1%
PR620 0_0402_5% VCCIO_SENSE <9,53>

+3VS PR621 10K_0402_1% PR622 71.5K_0402_1% PR623 100K_0402_5%
PQ603 SSM3K7002FU_SC70-3
PR624 0_0402_5% VCCP_PWRCTRL <10>
PC630 .01U_0402_16V7K PR625 100K_0402_5%

VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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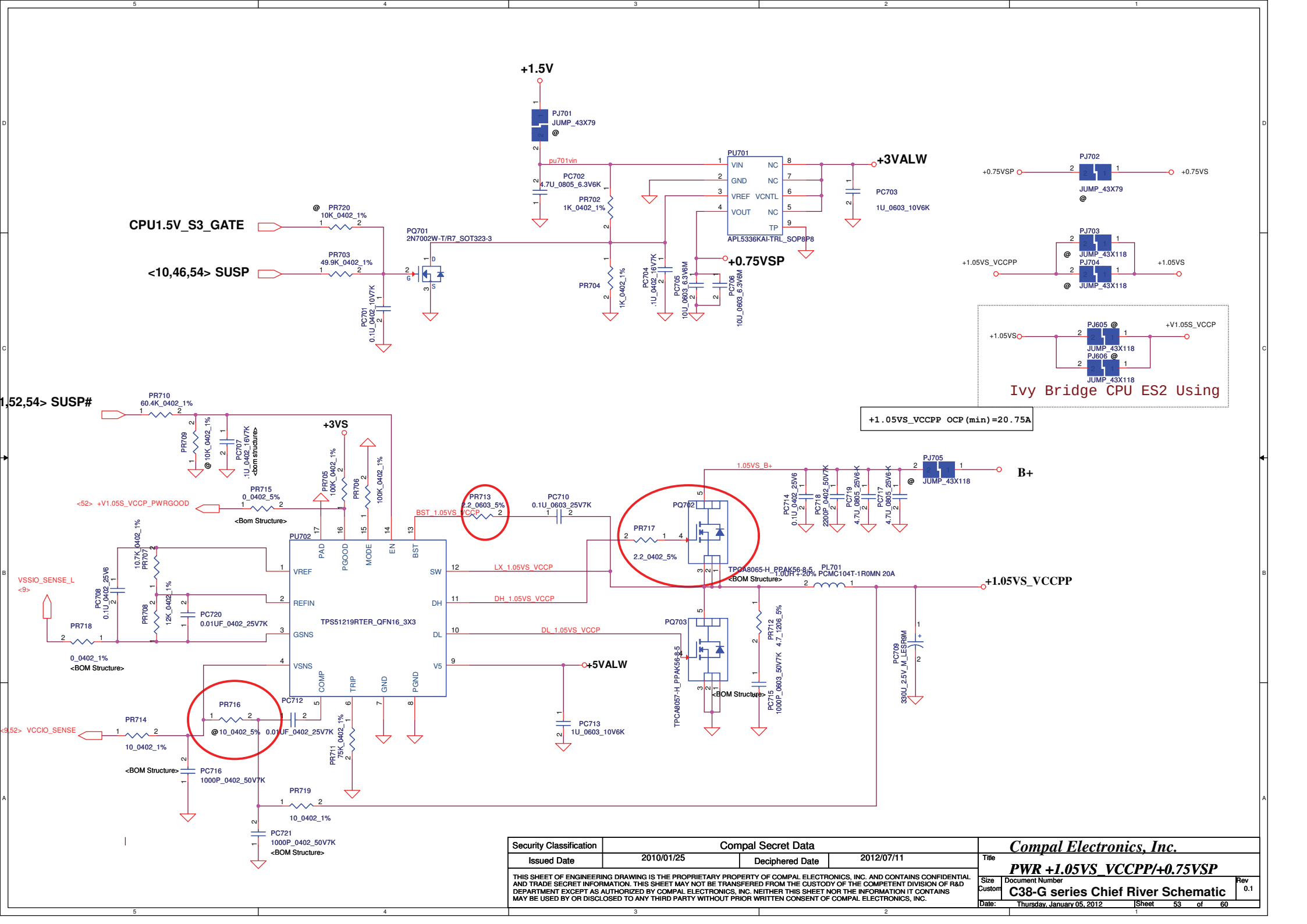
Title: PWR +VCCSAP/1.0
Size: C | Document Number: C38-G series Chief River Schematic | Rev: 0.1
Date: Thursday, January 05, 2012 | Sheet 52 of 60



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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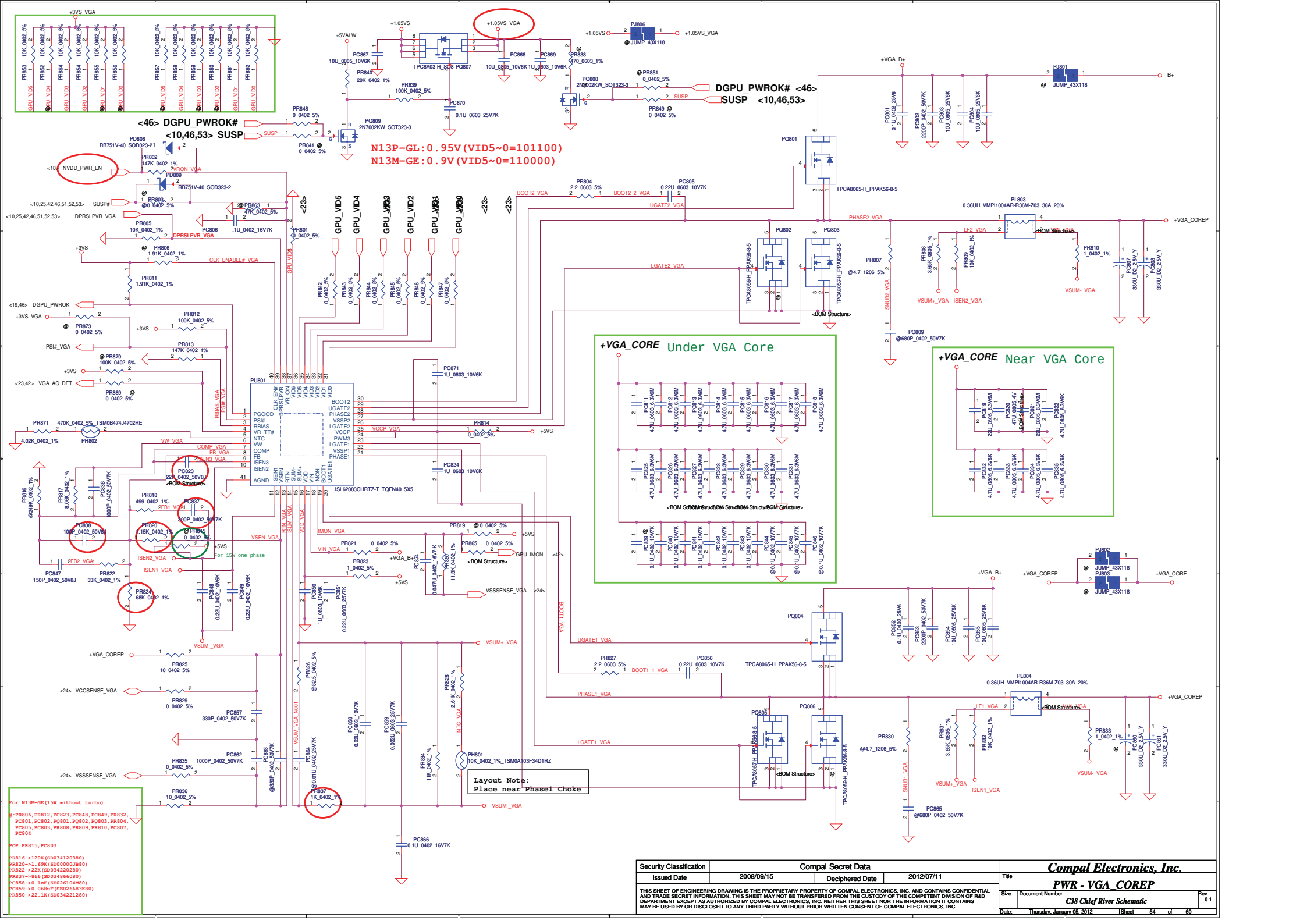
Compal Electronics, Inc.	
Title	PWR +1.05VS_VCCPP/+0.75VSP
Size: Custom	Document Number: C38-G series Chief River Schematic
Rev	0.1
Date: Thursday, January 05, 2012	Sheet 53 of 60



Security Classification	Compal Secret Data		
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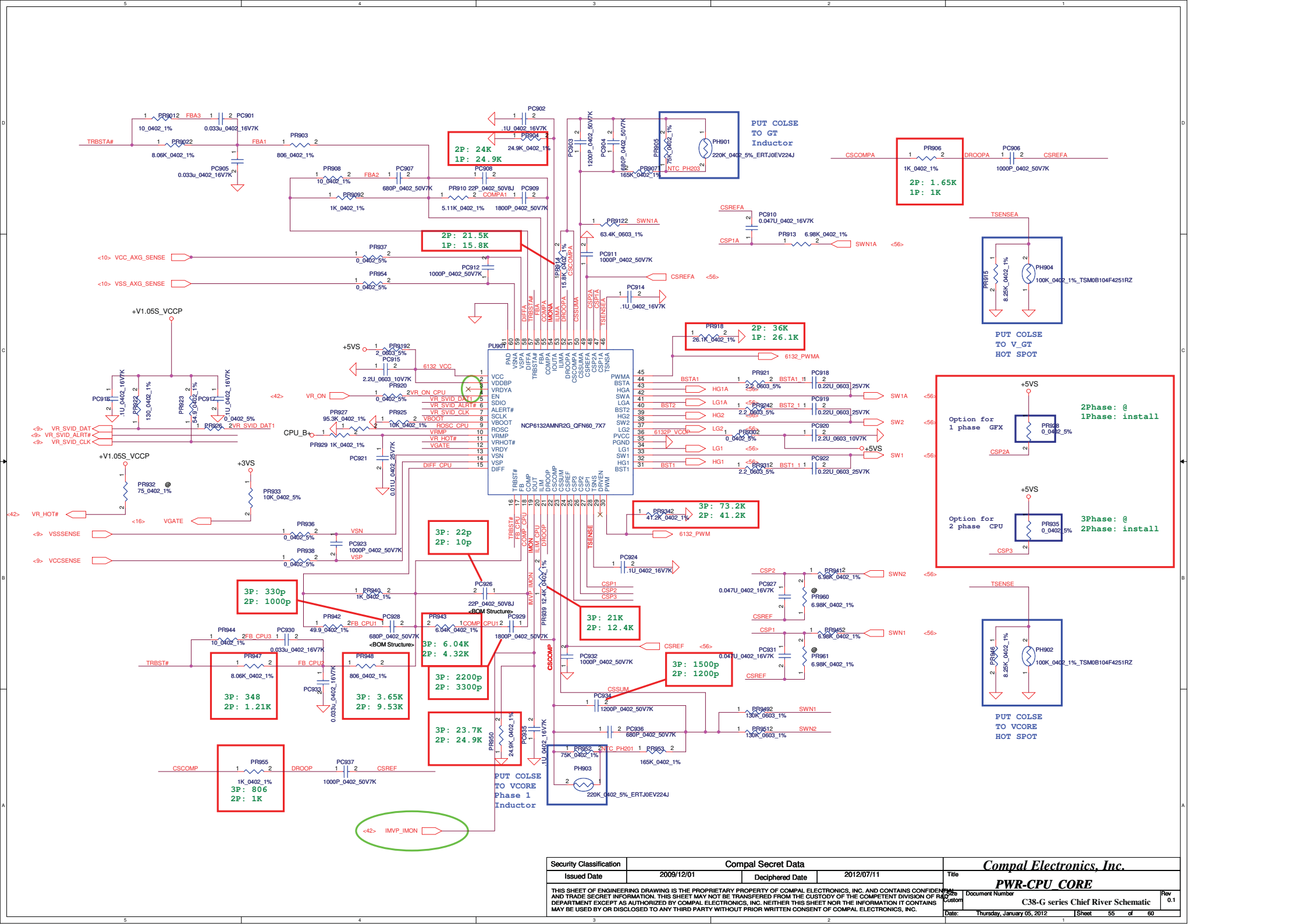
Compal Electronics, Inc.

Title: **PWR - VGA_COREP**

Size	Document Number	Rev
	C38 Chief River Schematic	0.1

Date: Thursday, January 05, 2012 | Sheet 54 of 60



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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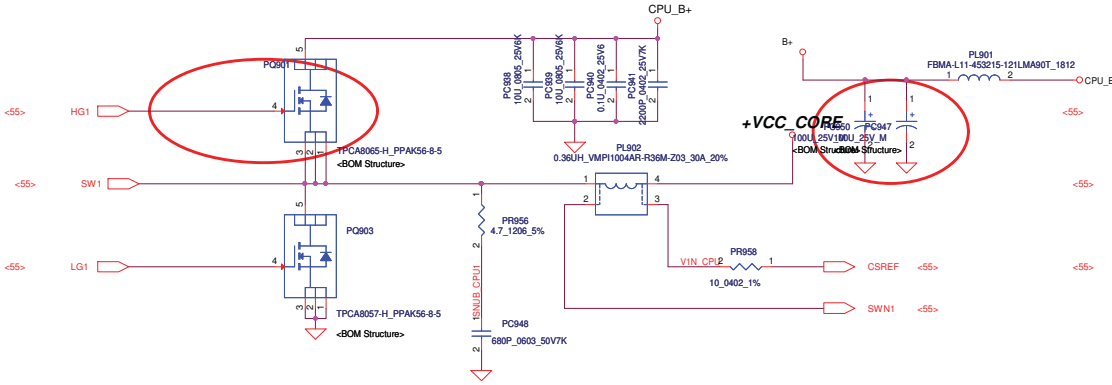
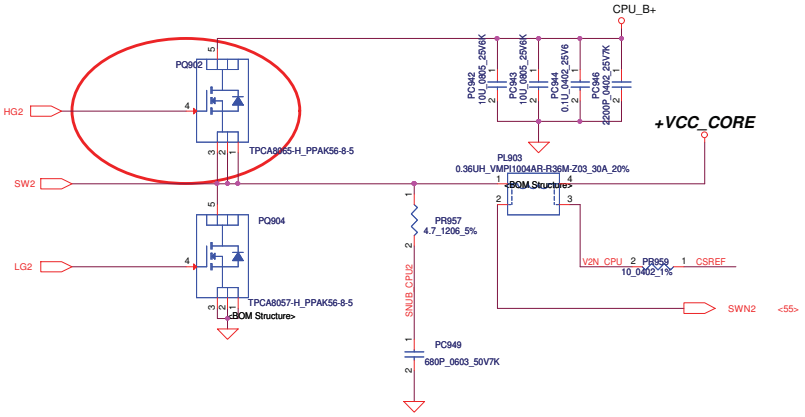
Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

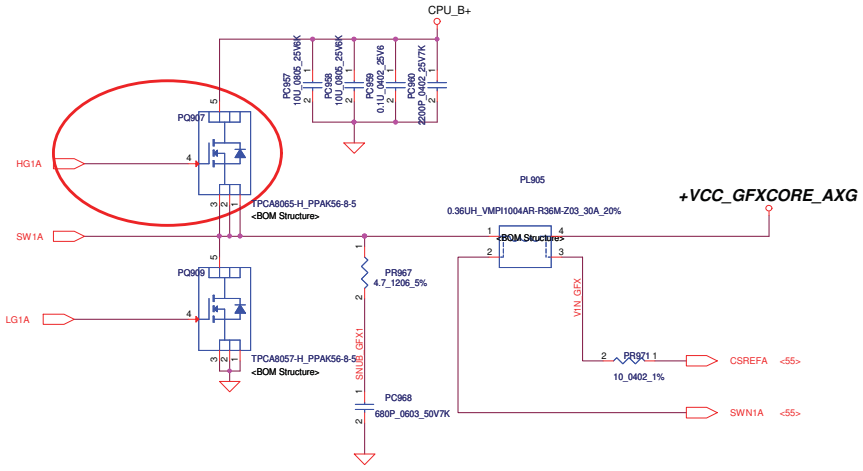
Date: Thursday, January 05, 2012 | Sheet 55 of 60





QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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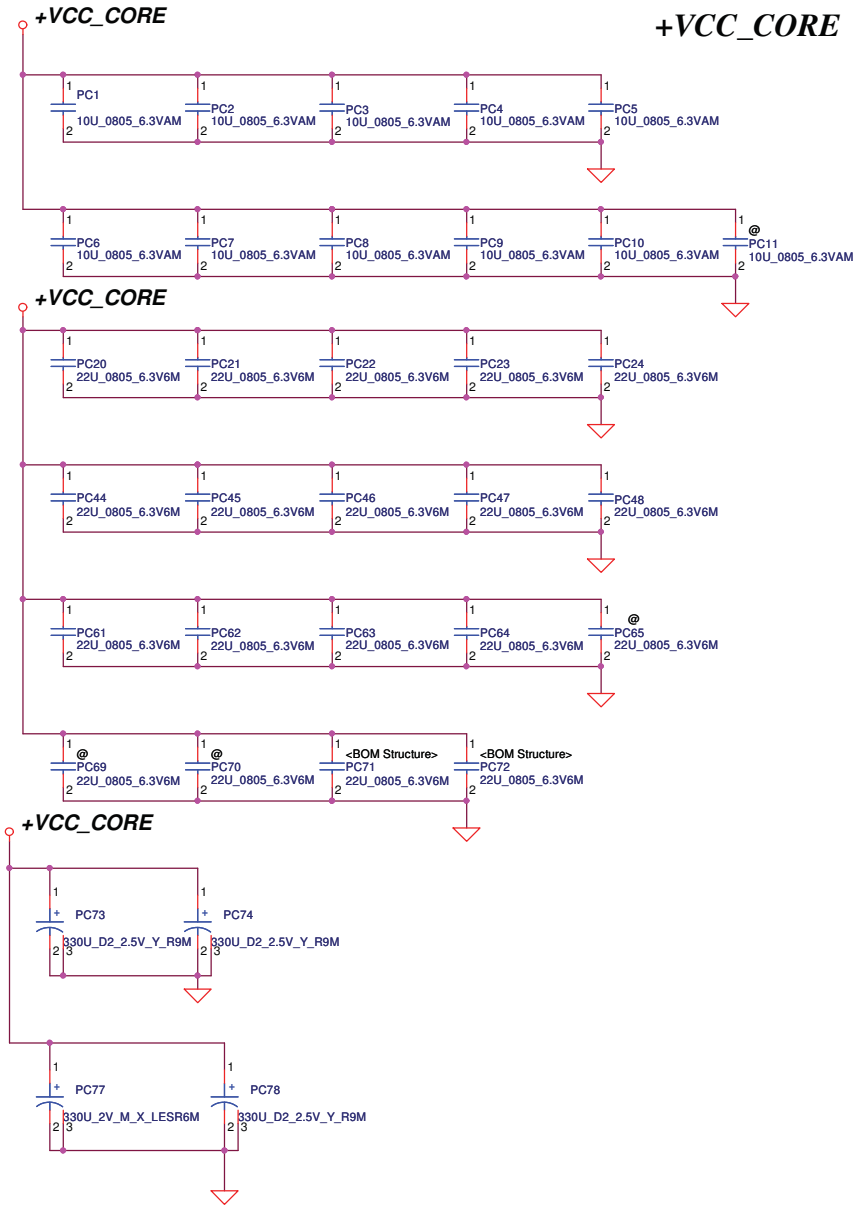
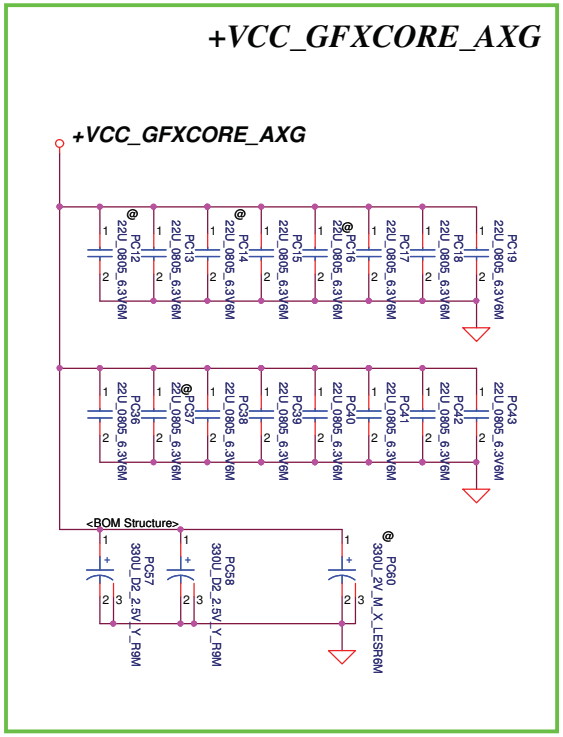
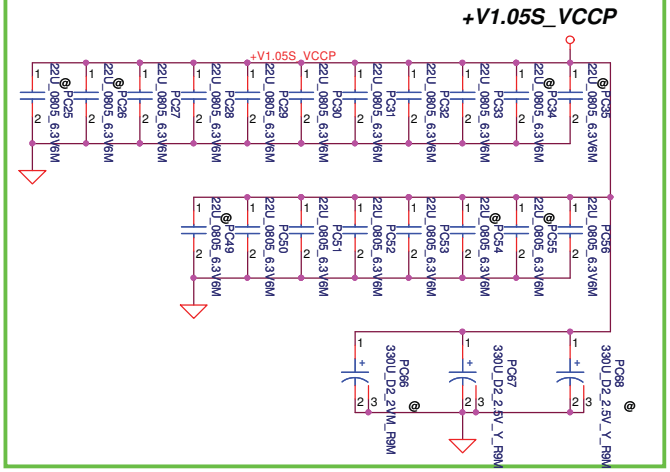
Compal Electronics, Inc.	
Title	PWR-CPU_CORE
Size	C
Document Number	C38-G series Chief River Schematic
Rev	0.1
Date:	Thursday, January 05, 2012
Sheet	56 of 60





Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	C38-G series Chief River Schematic	0.1

Date: Thursday, January 05, 2012 Sheet 57 of 60

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	To facilitate EA test	P54	Change net name of pin 1 of PR825 from +VGA_CORE to +VGA_COREP	2011/10/19	DVT
2	Sense VSSIO_SENSE_L net close to IC	P53	Add PR718	2011/10/19	DVT
3	CPU controller compensation RC tunning	P55	Change PC904, PC907, PC908, PC909, PC926, PC928, PR929, PC936 and PR943	2011/10/19	DVT
4	EMI request	P51	Change PR503	2011/10/19	DVT
5	Back to Back MOS change	P49	Change PQ302	2011/12/06	PVT
6	Sense VSSIO_SENSE_L change according to FAE	P53	Add PR719 and PC721. Change PR718 and PR714	2011/12/06	PVT
7	Add IC G718	P48	Change PR205 to 4.42k (90W) and PR210 to 27.4k (90W)	2011/12/06	PVT
8	EC_ON RC change	P50	Change PR418 from 10k to 2.2k	2011/12/06	PVT
9	Unpop PR224 and add PR231 by HW request	P48	Unpop PR224 and add PR231	2011/12/21	PVT
10	Change CPU&GFX compensation RC by FAE recommendation	P55	PR902, PR903, PR947, PR948, PC901, PC905, PC929, PC930 and PC933	2011/12/21	PVT
11	Change charger's choke from 4.7u to 10u	P49	PL302	2011/12/21	PVT
12					
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14					
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Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2012/07/11

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Title: PIR (PWR)

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 05, 2012 | Sheet 58 of 60

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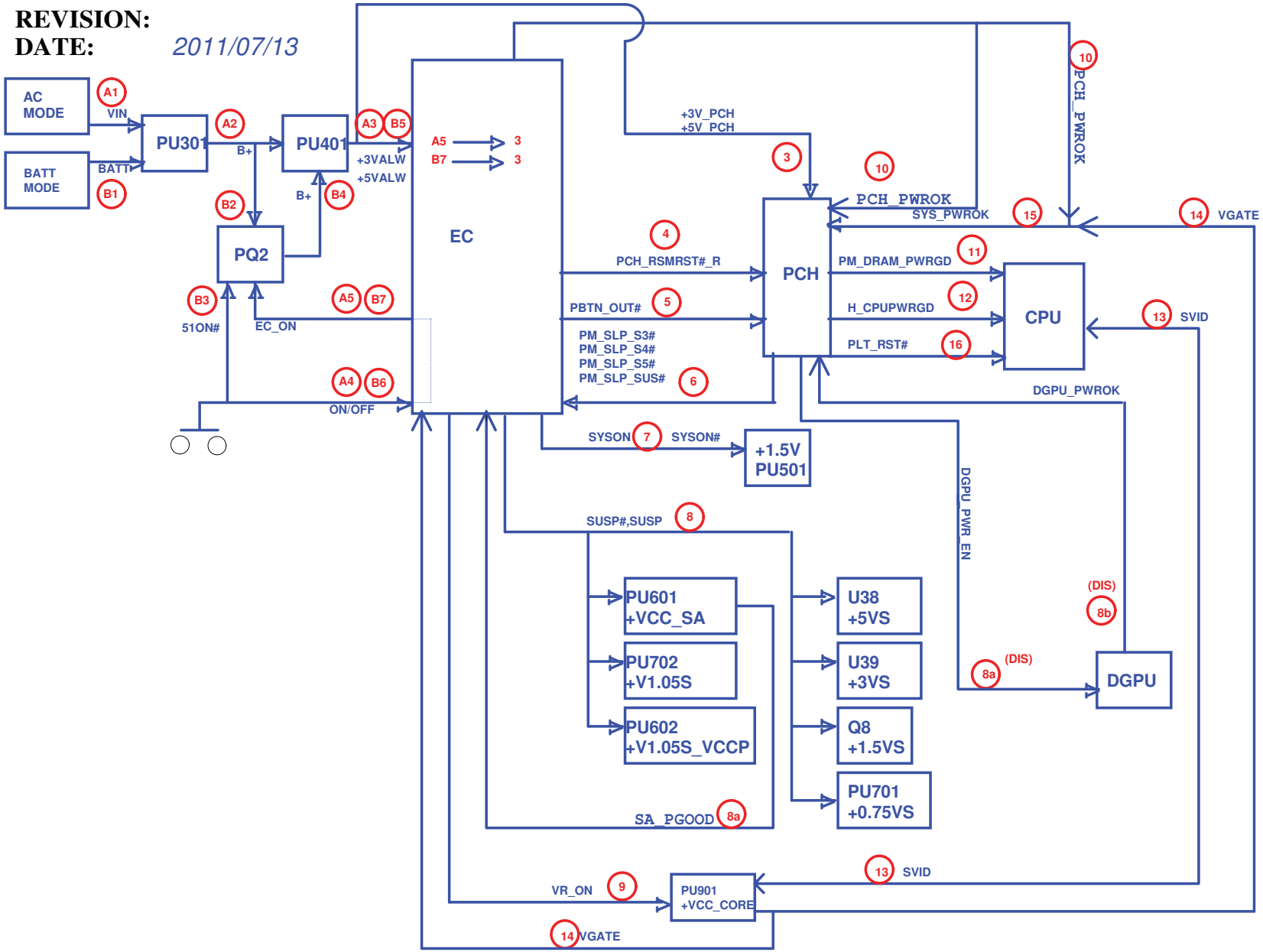
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



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Title: Power sequence			
Size: Custom	Document Number: LA-7983P		Rev: 0.3
Date: Thursday, January 05, 2012	Sheet 59 of 60		

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For NVIDIA update Strapping setting.	32	RV102 change to 10K ohm	10/11	B
2	PCIE BUS corrected for external USBcontroller	45	PCIE_PRX_DTX_P4/N4 Swapped	10/11	B
3	Modify USB3.0 Controller circuit	45	R1172 to 300k, R747 to 430k, C832 to 1U	10/14	B
4	Modify USB3.0 Controller circuit	45	U53.8 to +3V, R1177.2 to +3V . Add R4970	10/14	B
5	Modify LAN function design for surge.	38	Add R4966, R4967, R4968, R4969, for 10/100 SKU	10/18	B
6		38	Modify R1443 near to LAN chip side. Delete R1448 0 ohm.	10/18	B
7		38	Modify R1443 near to LAN chip side.	10/18	B
8		38	Add CHASSIS_GND, C989, C990, C991	10/18	B
9		38	Delete R1374, R1375, R1377, DL2~DL4.	10/25	B
10	Reserve HDMI EMI solution	35	Add C992~C999	10/25	B
11	Reserve LAN ESD solution	38	Add D74, link both MCT0_1 and chassis to ground.	10/27	B
12	Change component type.	43	C987 change to 0402 type	10/27	B
13		34	C538 change to 0402 type	10/27	B
14	Reserve LAN EMI solution	38	Add R4971~R4974	10/27	B
15	Reserve MAINPWON 0ohm.	38	Add R4978	12/21	C
16	LAN Power Switch	37	Add Q130, R4977, C1001	12/21	C
17					

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