Compal Confidential

QAQ10/11

LA-8581P REV1.0 Schematic

Intel Ivy Bridge/Pather Point

UMA&OPT

2012-04-23 Rev 1.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title			SCHEMATICS, MB A8581
Size	Document Number		Rev
	4019IE		B
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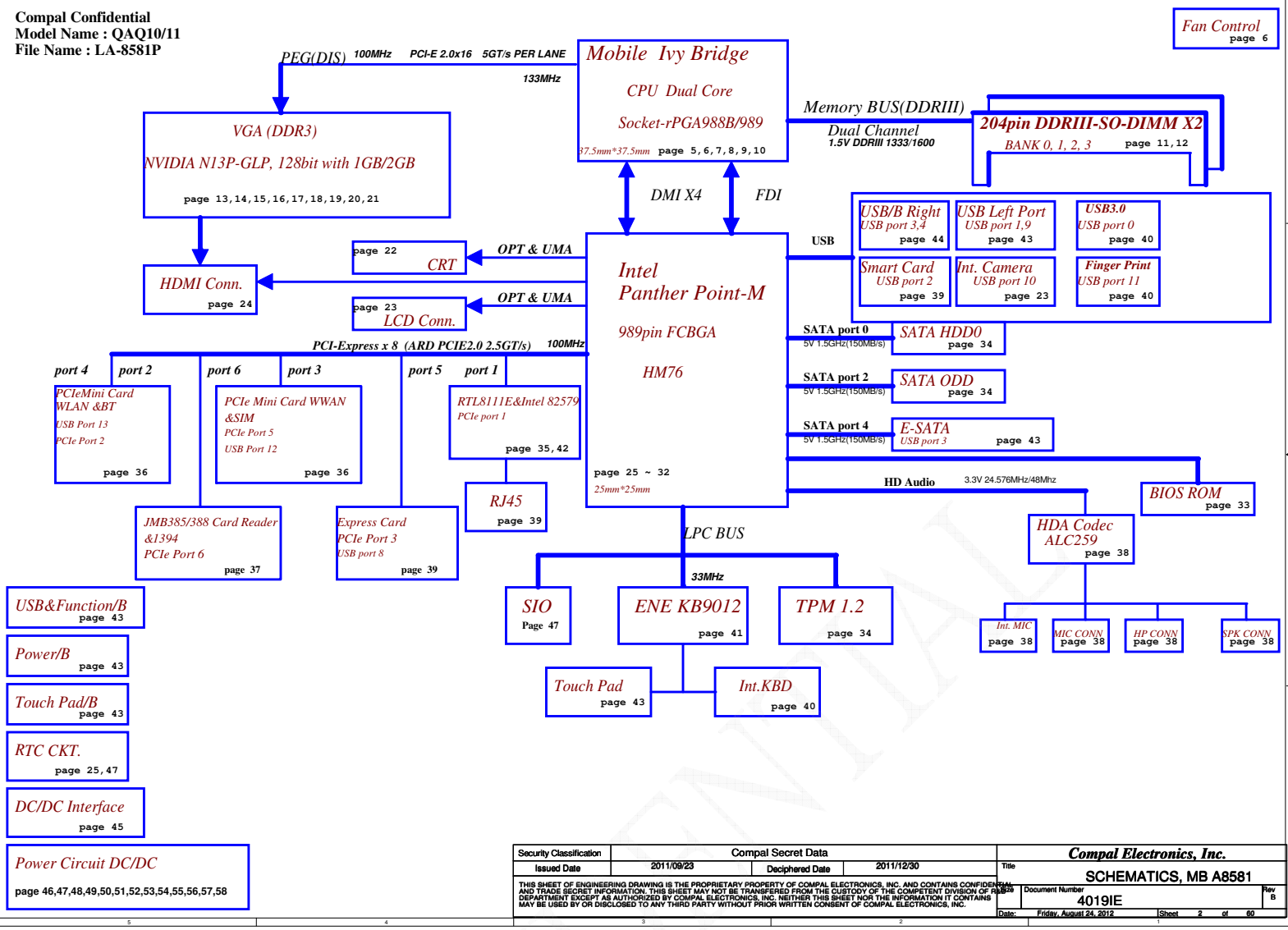
Model Name : QAQ10/11
File Name : LA-8581P



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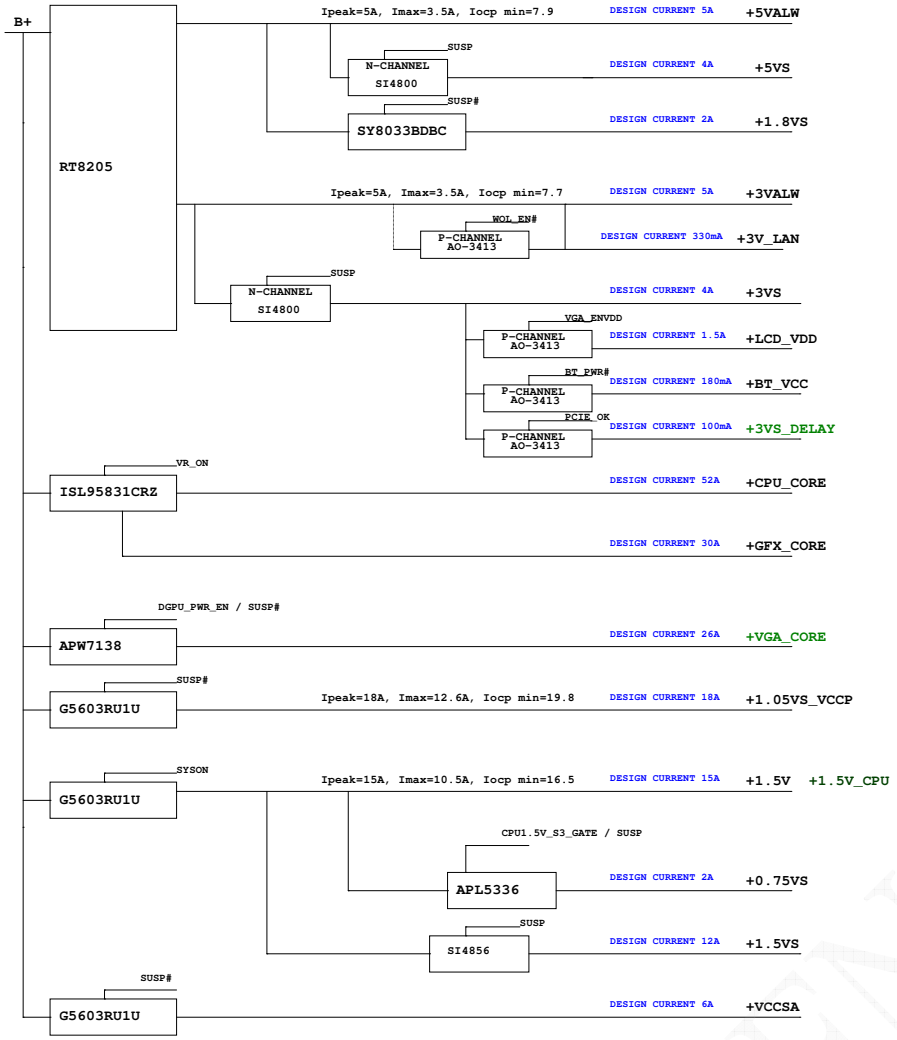

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Power	Device	Address
+3VL	charger	0x12
+3VL	Smart Battery	0x16

EC SM Bus2 address

Power	Device	Address
+3VS	VGA(N13P-GLP)	0X9E
+3VS	PCH	0x96

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1--WLAN	

BOM configu table

SKU	Description	Bom config	
1	QAQ10 UMA GIGA W/HDMI	DA8@/8111E@/UMA@/TF@/10@/WIN8@/388@/COM@	4619IE30L01
2	QAQ11 DIS N13PGLP1G W/HDMI	DA8@/8111E@/OPT@/TF@/11@/WIN8@/388@/COM@	4619IE30L11
3	QAQ13 DIS GLP2G W/HDMI/TPM	DA8@/8111E@/OPT@/030@/13@/WIN8@/388@/COM@ /TPM@/IN_TPM@	4619IE30L21
4			
5			
6			
7			
8			

DA8@/8111E@/PCH@/UMA@/OPT@/385@/388@/389@/IN_TPM@/TPM@/WB_TPM@/SM@/COM@/030@/TF@ /WIN8@/10@/11@/12@/13@/Rev02@/Rev03@/Rev04@/Rev10@/VPRO@

388@: with 1394;
389@: without 1394.

IN_TPM@: TPM chip from vendor "INFINEON";
WB_TPM@: TPM chip from vendor "Nuvoton"
With TPM SKUs: mount "TPM@ and IN_TPM@ " or "TPM@ and WB_TPM@".

If has Vpro@, no 8111E@, Rev02@,Rev03@, Rev04@ and Rev10@.

X76 AND VGA configu table

SKU	Description	Config	
1	4619IE30L11	ZZZ SAM1G@ SAM 1G; ZZZ HY1G@ Hynix 1G	QAQ11 DIS N13P-GLP
2			
3	4619IE30L21	ZZZ SAM2G@ SAM 2G; ZZZ HY2G@ Hynix 2G	QAQ13 DIS N13P-GLP
4			
5			

Board ID Table

Board ID	Rb	Ra	VCC	V min	Vtyp	Vmax	PCB Revision
0	0	100K +/- 5%	3.3V +/- 5%	0V	0V	0V	0.1
1	8.2K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.436 V	0.503 V	0.538 V	0.3
3	33K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.712 V	0.819 V	0.875 V	0.4
4	56K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.036 V	1.185 V	1.264 V	1.0
5	100K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.453 V	1.650 V	1.759 V	VPRO
6	200K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	100K +/- 5%	3.3V +/- 5%	2.500 V	3.300 V	3.300 V	

PCH And PCBA table

PCH	UPCH1 BD82HM76 SLJ8E C1 BGA 989P PCH 030! 8111E@	UPCH1 BD82QM77 QPRE C1 BGA 989P PCH VPRO@
PCB		ZZZ DA8@ PCB LA-8581P REV1 M/B; ZZZ DAZ@ PCB QAQ10

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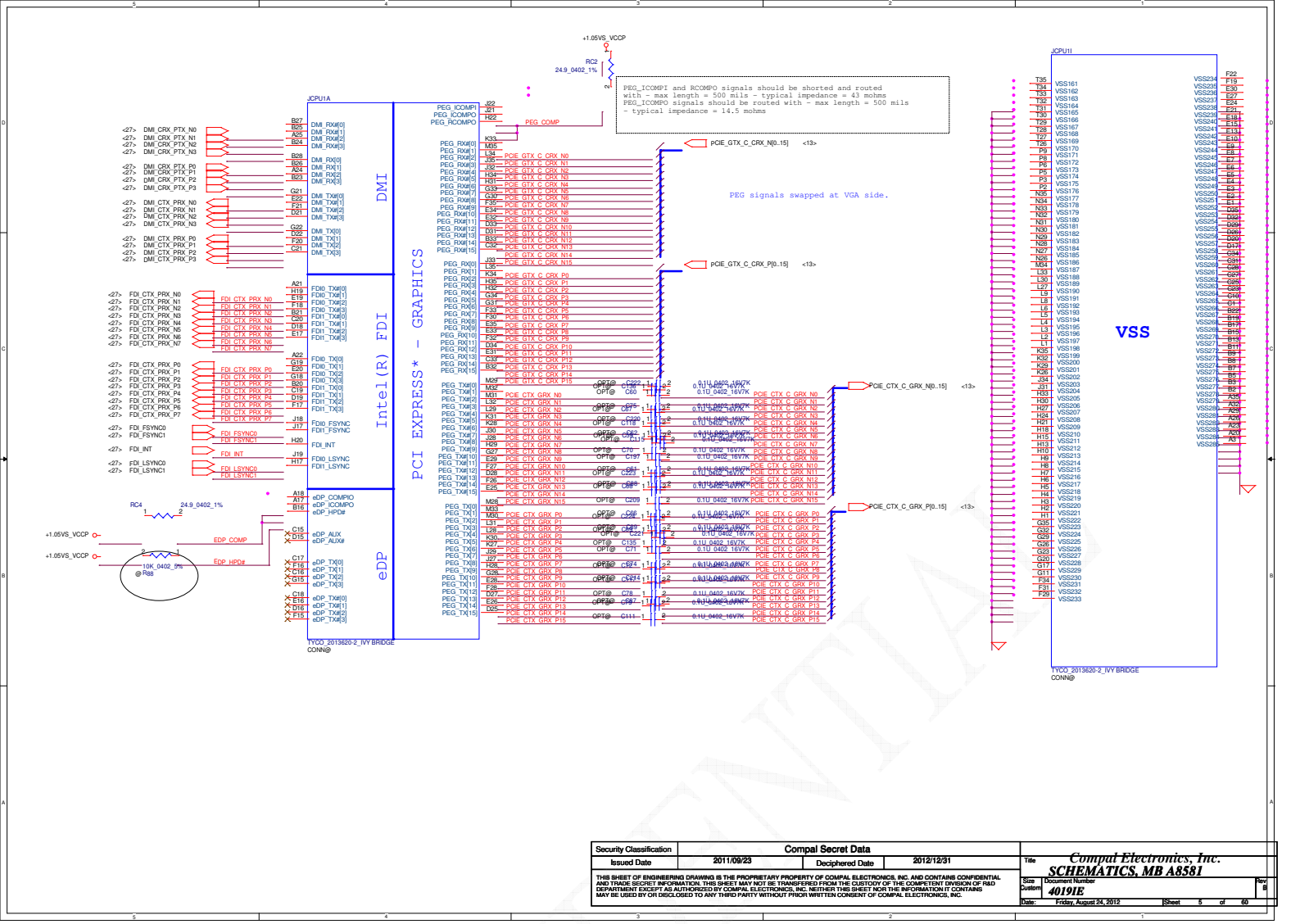

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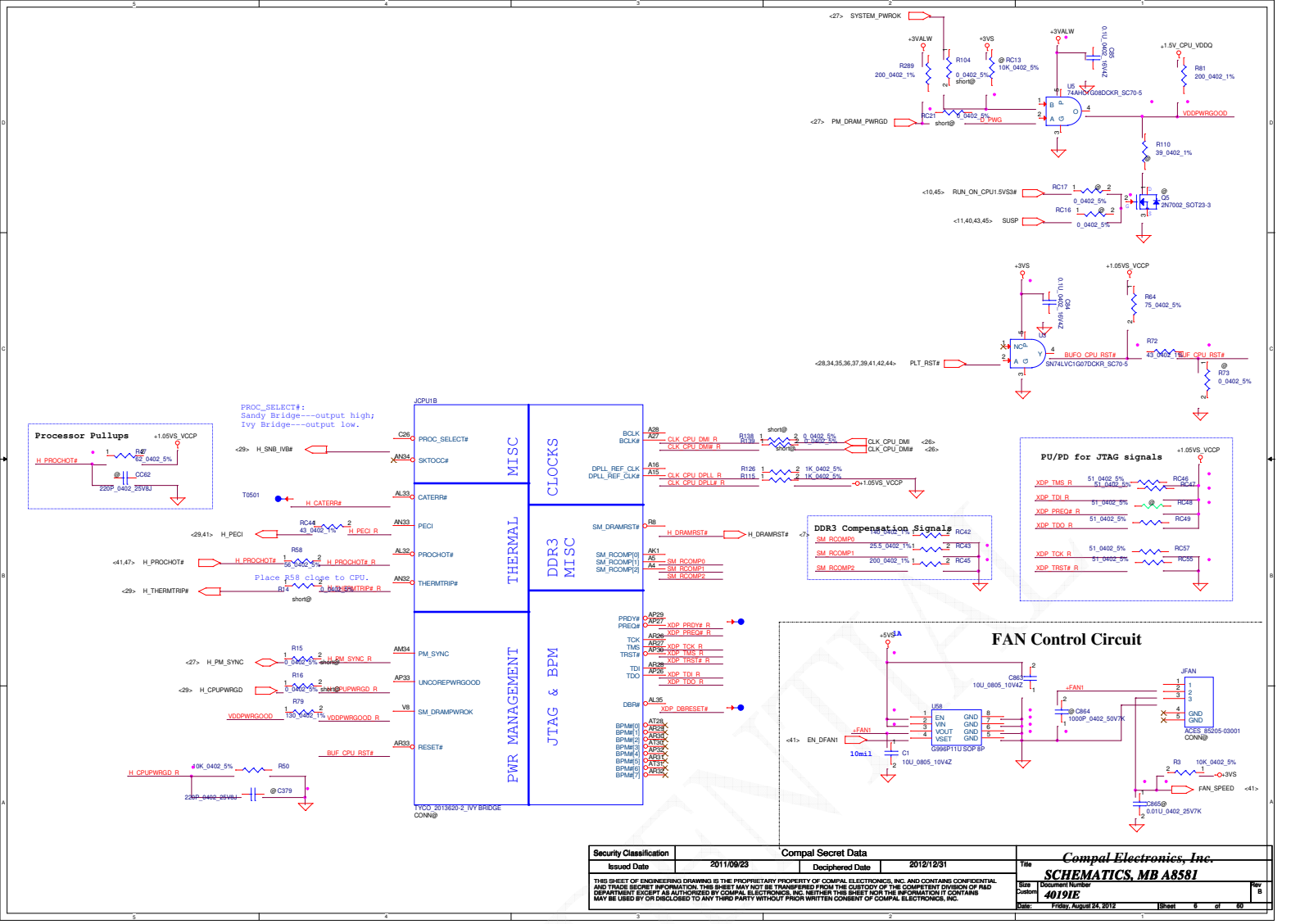

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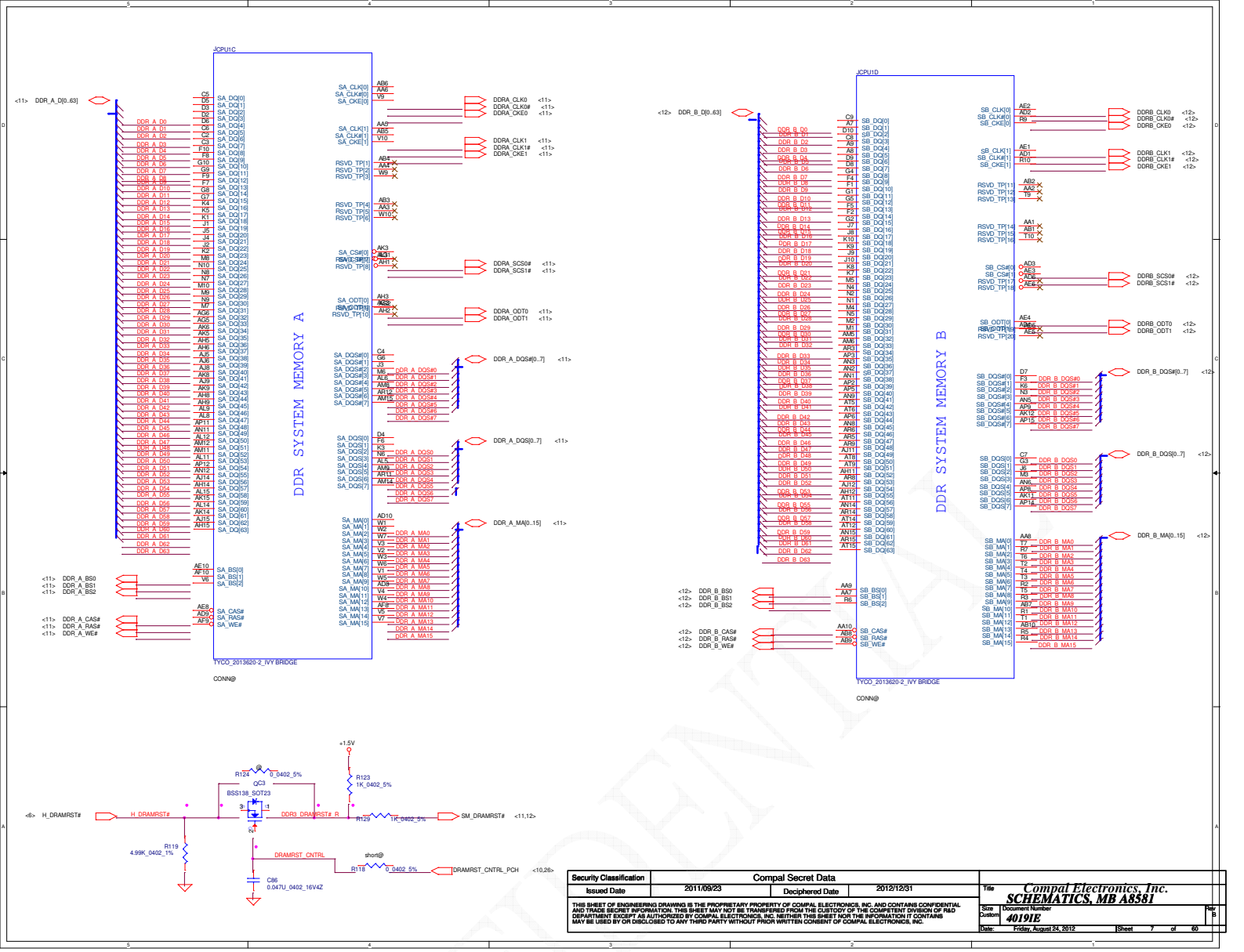

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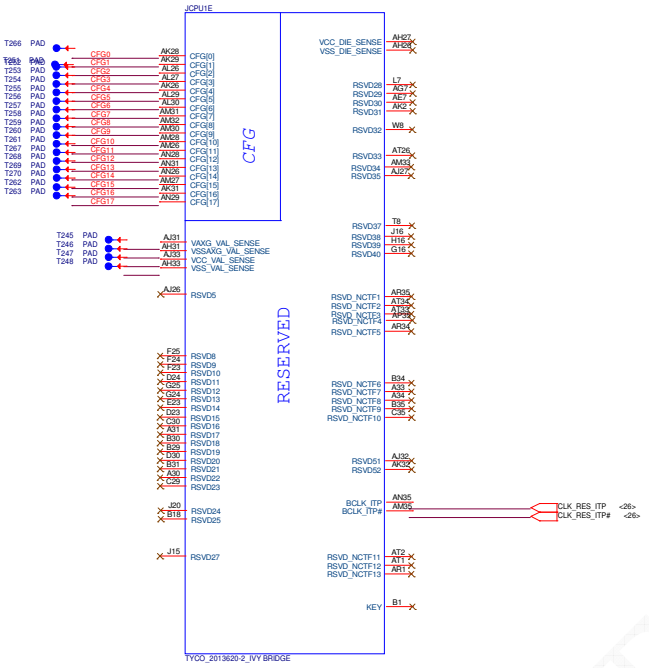
CFG Straps for Processor

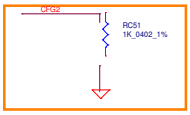
CFG[1:0]: reserved configuration lane.

CFG[3]: reserved

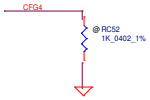
CFG[17:7]: reserved configuration lanes.

CFG[17:0]:
Processor internal pull up 5~15Kohm to VCCIO

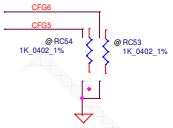




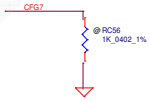
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

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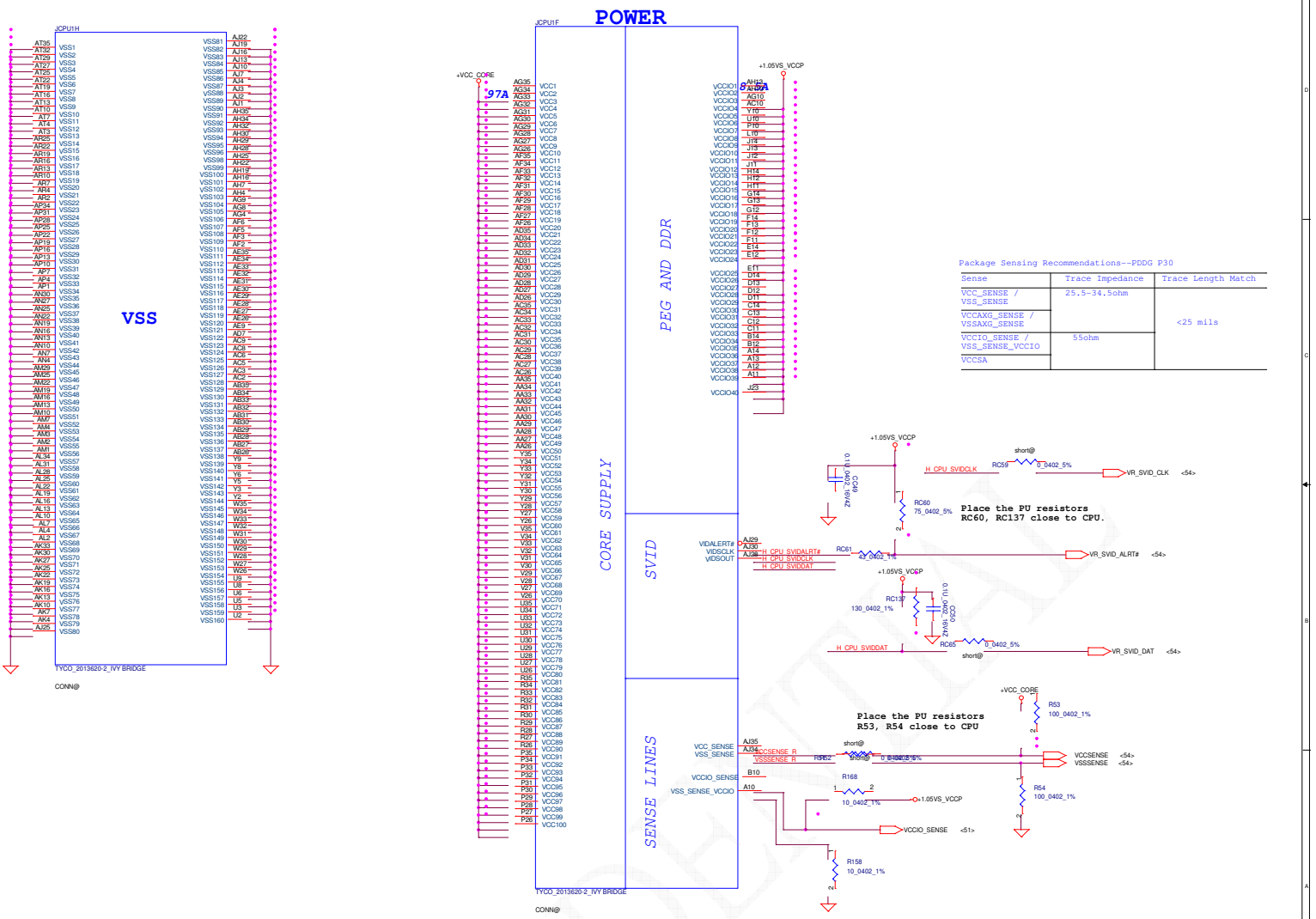

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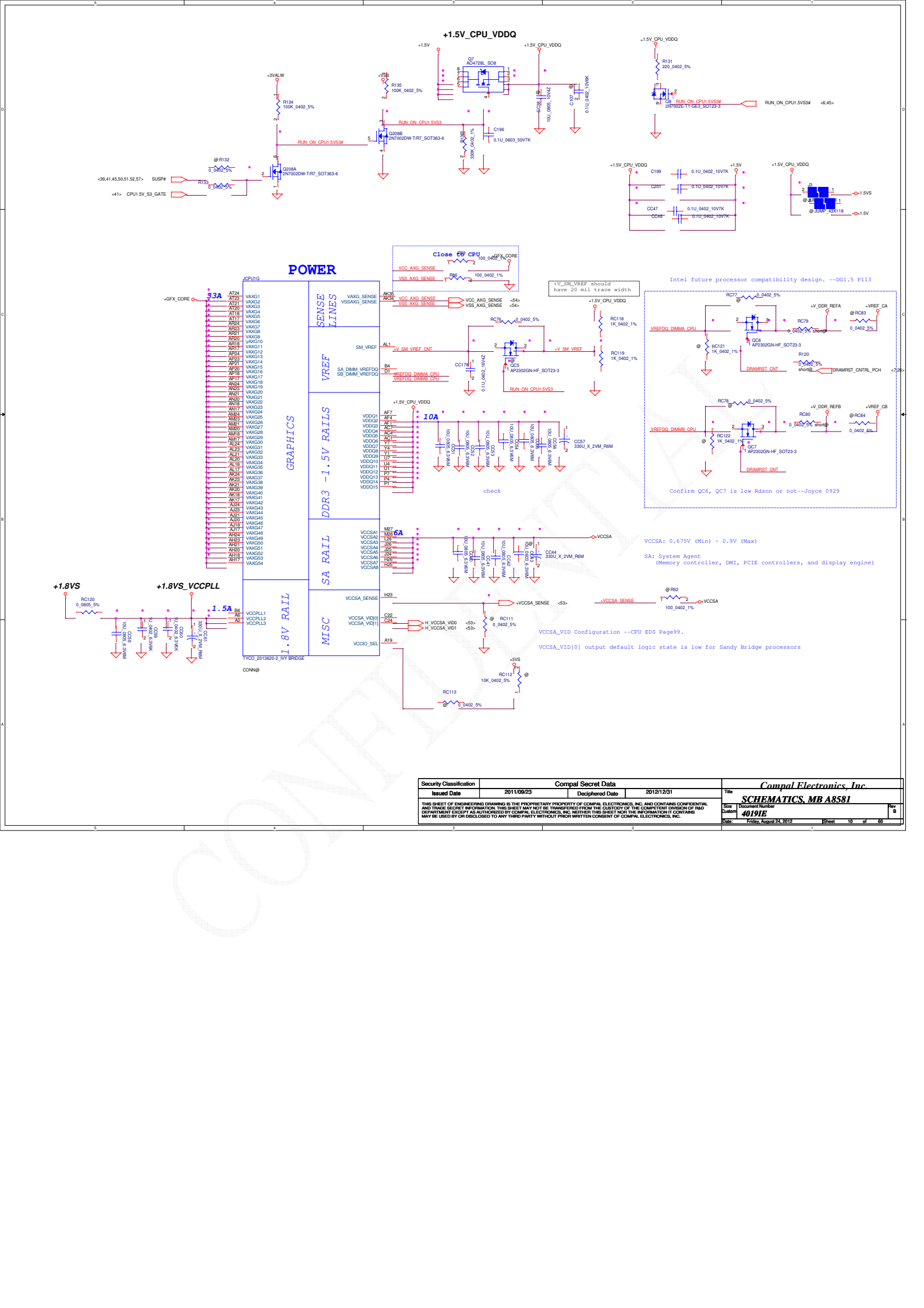
+1.5V_CPU_VDDQ
POWER
Close to CPU
SENSE LINES
VREF
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
MISC
1.8V RAIL
JCPU1G
VCC_AXG_SENSE
VSS_AXG_SENSE
SM_VREF
+V_SM_VREF_CNT
+V_SM_VREF
RUN_ON_CPU1.5VS3
RUN_ON_CPU1.5VS3#
VREFDQ_DIMMA_CPU
VREFDQ_DIMMB_CPU
+VCCSA
+VCCSA_SENSE
H_VCCSA_VID0
H_VCCSA_VID1
VCCIO_SEL
+1.8VS
+1.8VS_VCCPLL
33A
10A
6A
1.5A
check
Intel future processor compatibility design. --DG1.5 P113
Confirm QC6, QC7 is low Rdson or not--Joyce 0929
VCCSA: 0.675V (Min) ~ 0.9V (Max)
SA: System Agent
(Memory controller, DMI, PCIE controllers, and display engine)
VCCSA_VID Configuration --CPU EDS Page99.
VCCSA_VID[0] output default logic state is low for Sandy Bridge processors
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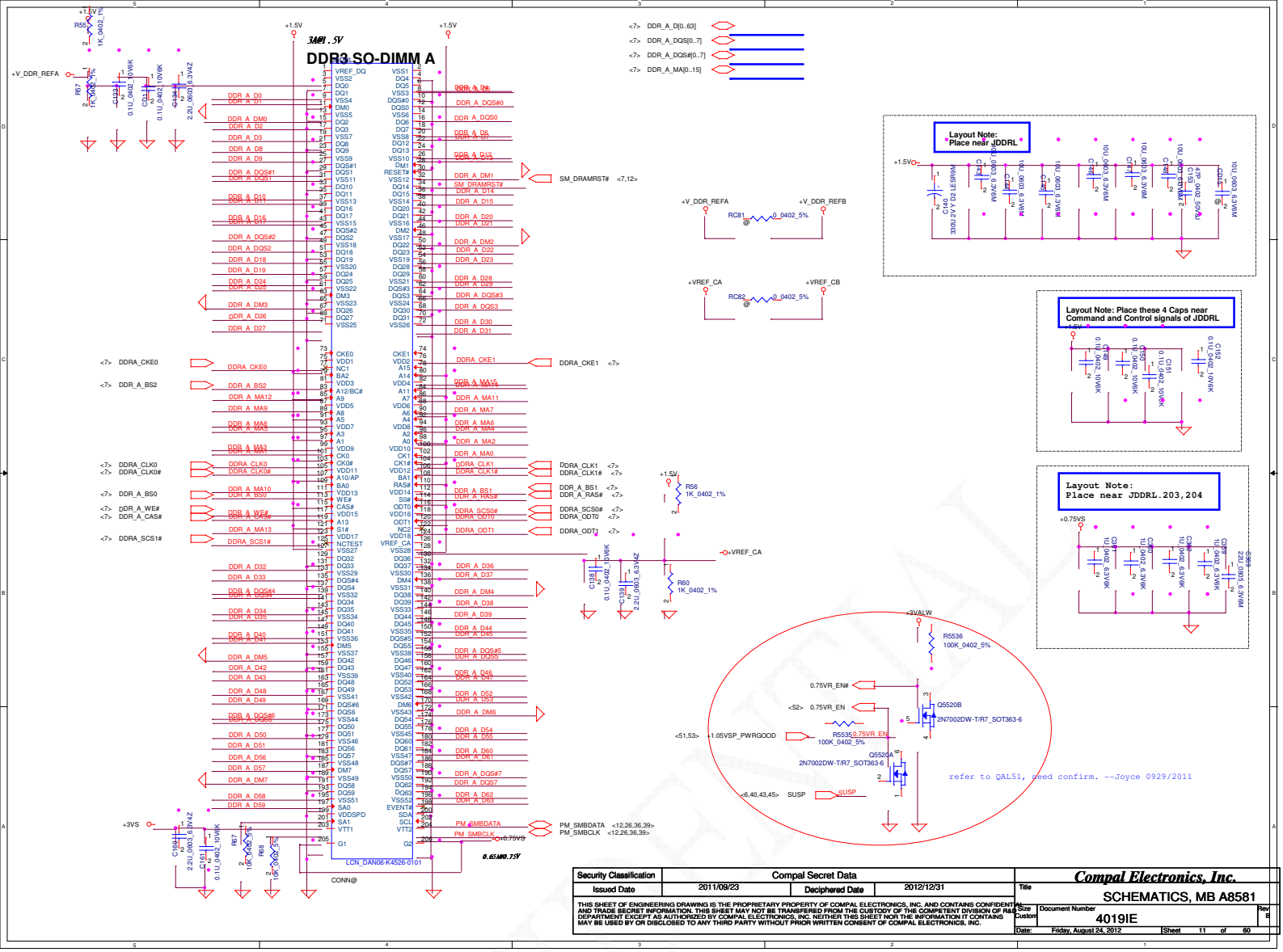

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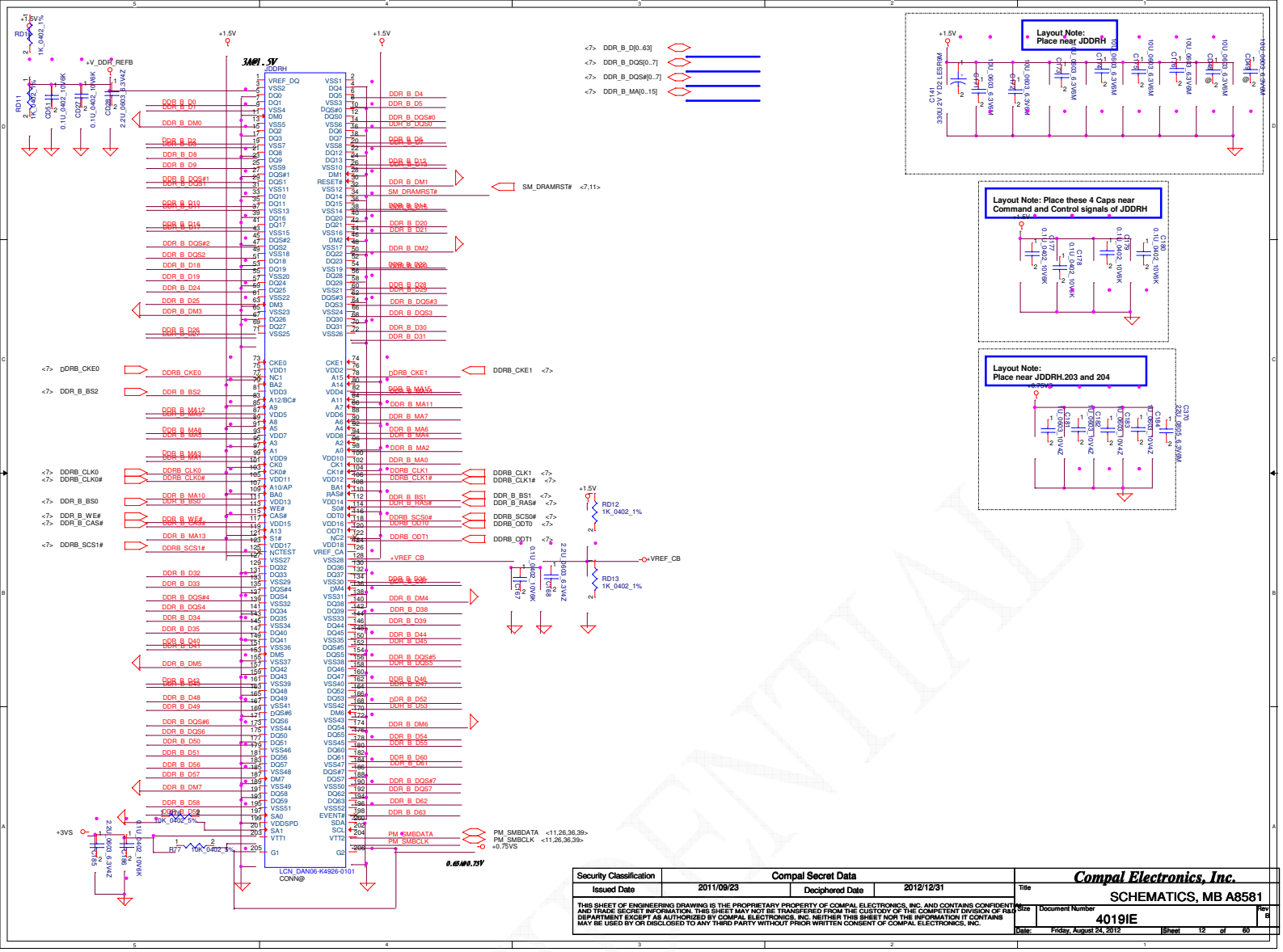

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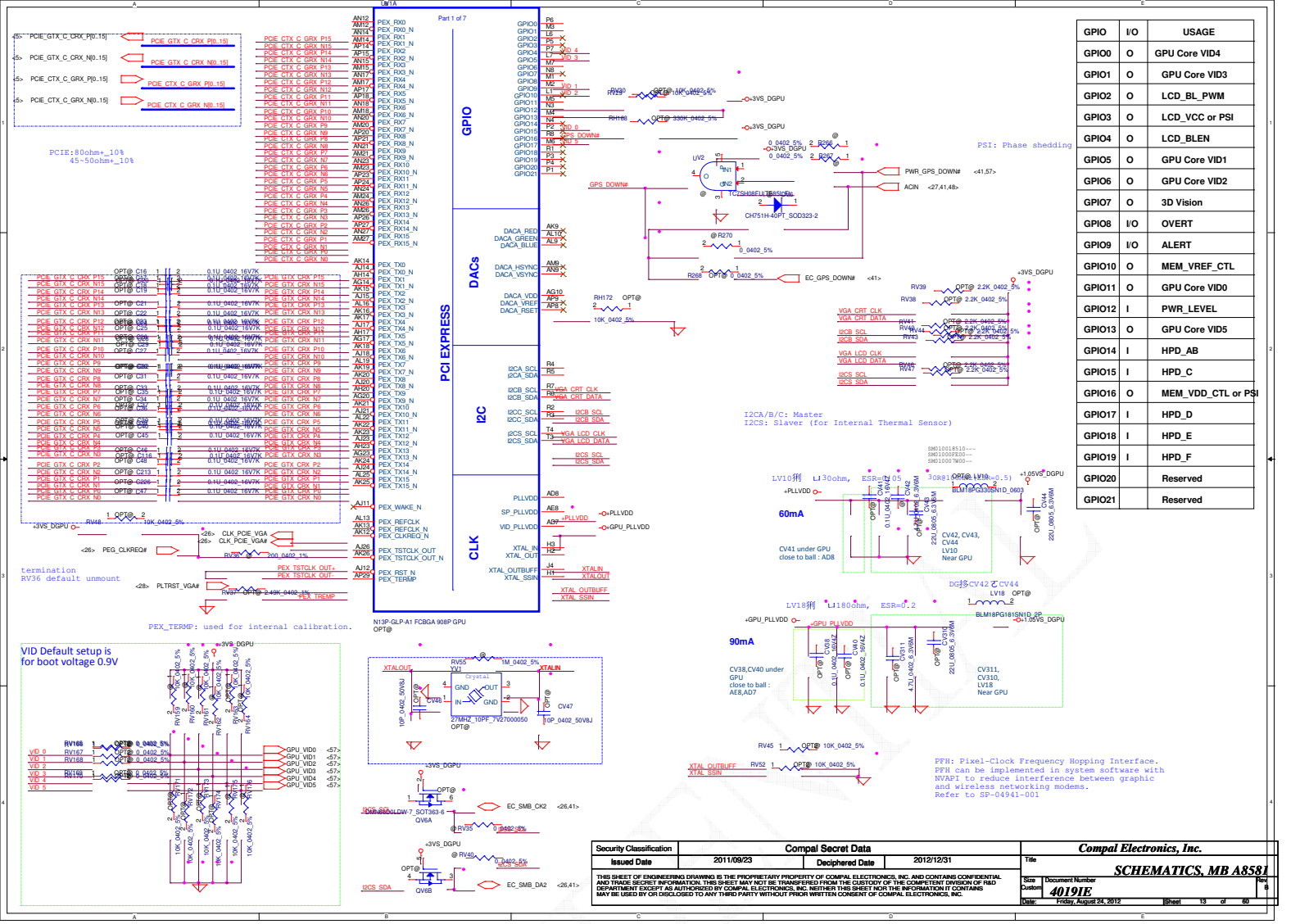

GPIO	I/O	USAGE
GPIO0	O	GPU Core VID4
GPIO1	O	GPU Core VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC or PSI
GPIO4	O	LCD_BLEN
GPIO5	O	GPU Core VID1
GPIO6	O	GPU Core VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU Core VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU Core VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL or PSI
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

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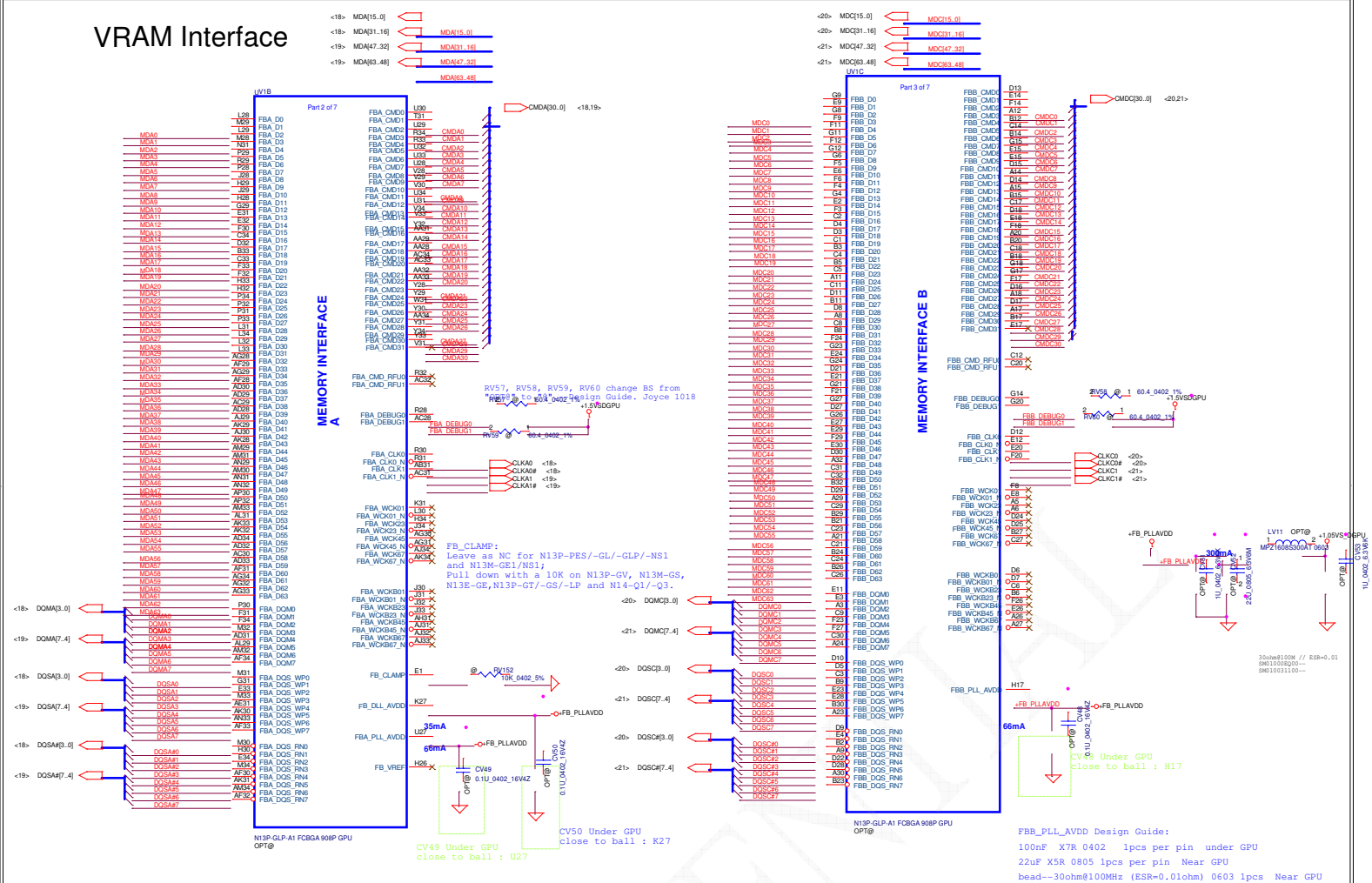
VRAM Interface



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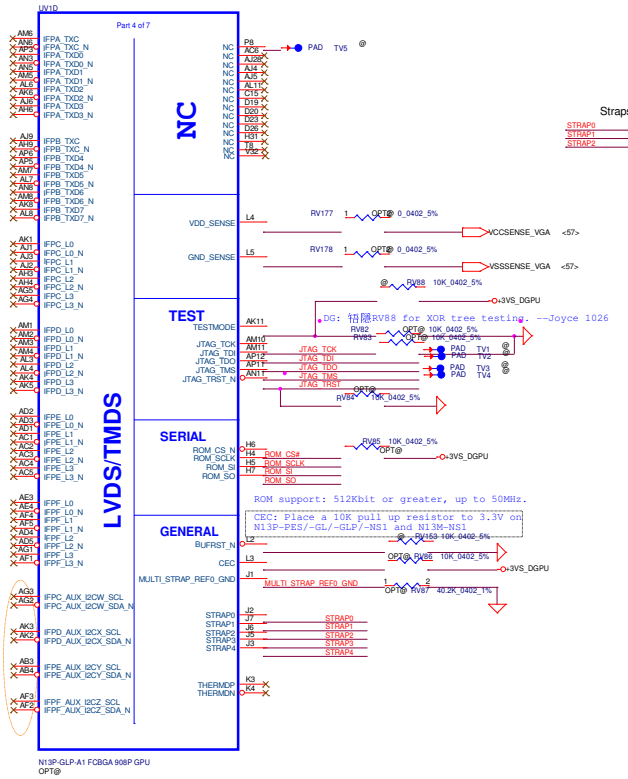

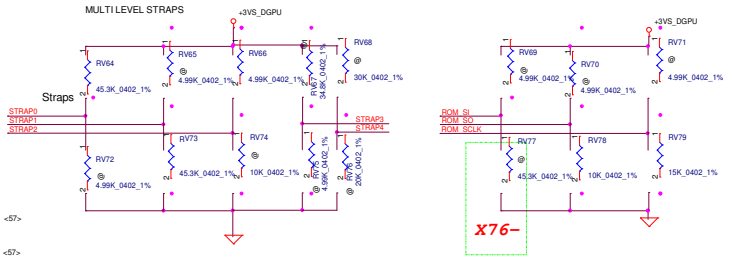

Physical strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB [1]	FB [0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER [3]	USER [2]	USER [1]	USER [0]
STRAP1	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	PCI-DEVID [3]	PCI-DEVID [2]	PCI-DEVID [1]	PCI-DEVID [0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull up to 3V	Pull down to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR
0 No VBIOS ROM
1 BIOS ROM is present (Default)

PEX_PLL_EN_TERM: PLL termination setting
0 Disable (Default)
1 Enable

PCIE_MAX_SPEED
0 Limited to PCIE GEN 1
1 PCIE GEN 2/3 capable

FB [1:0]: N13x FB Aperture Size
0 RESERVED
1 RESERVED
2 256 MB (Default)
3 RESERVED

USER Straps
1111 EDID is used
others: DG-05587 Page195

3GIO_PAD_CFG
0000~0101 RESERVED
0110 Notebook (default)
0111~1111 RESERVED

For N13P-GLP strap table

For N13P-PES :
Strap 0 : PU45
Strap 1 : PD35
Strap 2 : PU35
ROM_SCLK : PU15
ROM_SI : PD35
ROM_SO : PD10

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GLP	900 MHz	64M*16*8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 15K	RV70 PD 30K	RV71 PD 15K
	900 MHz	64M*16*8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 20K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M*16*8 2GB	Hynix SA00003YO00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 35K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M*16*8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 45K	RV70 PD 30K	RV71 PD 15K

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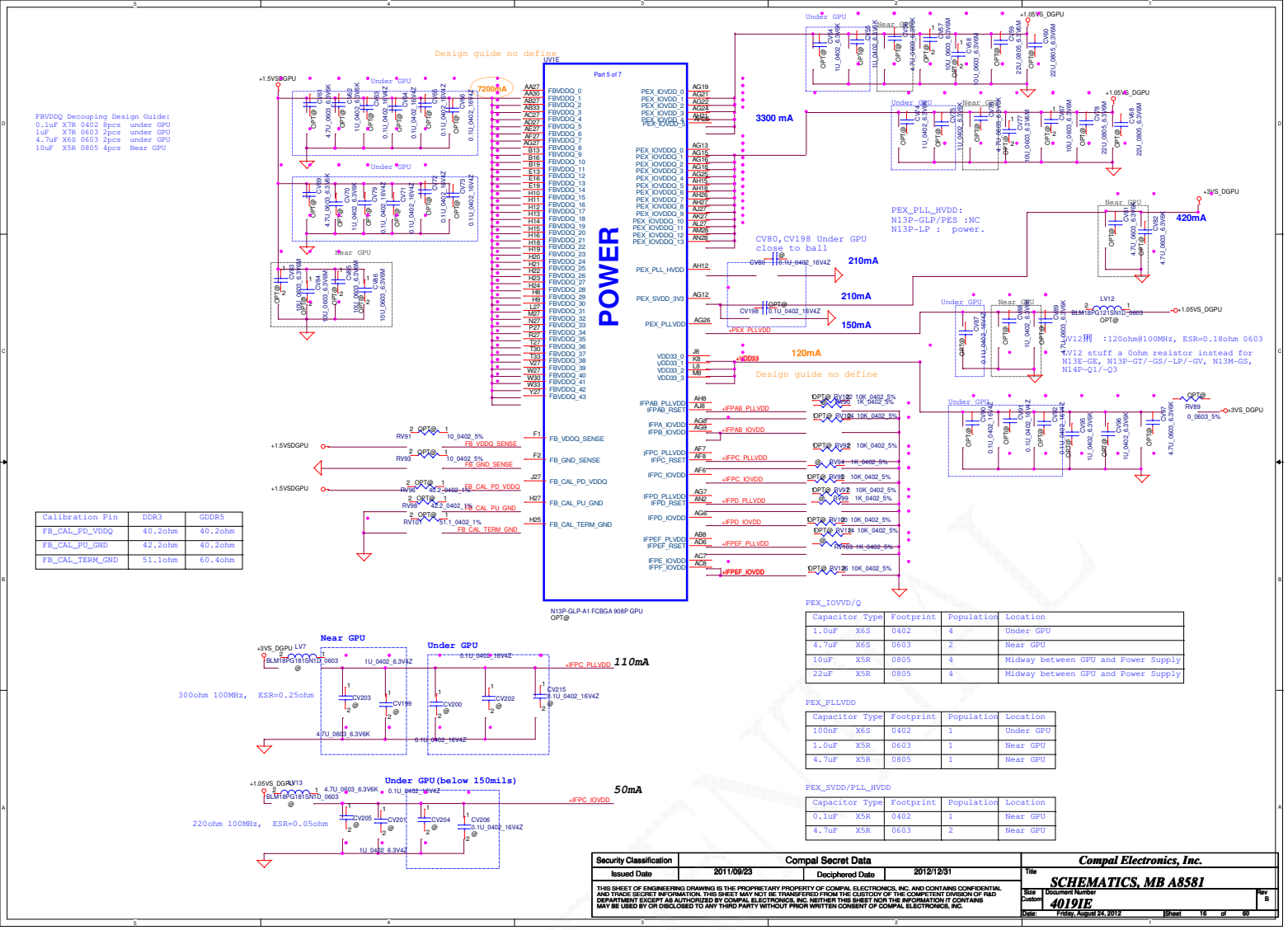

Calibration Pin	DDR3	GDDR5
FB_CAL_PD_VDDQ	40.2ohm	40.2ohm
FB_CAL_PU_GND	42.2ohm	40.2ohm
FB_CAL_TERM_GND	51.1ohm	60.4ohm

PEX_IOVVD/Q

Capacitor Type	Footprint	Population	Location
1.0uF X6S	0402	4	Under GPU
4.7uF X6S	0603	2	Near GPU
10uF X5R	0805	4	Midway between GPU and Power Supply
22uF X5R	0805	4	Midway between GPU and Power Supply

PEX_PLLVDD

Capacitor Type	Footprint	Population	Location
100nF X6S	0402	1	Under GPU
1.0uF X5R	0603	1	Near GPU
4.7uF X5R	0805	1	Near GPU

PEX_SVDD/PLL_HVDD

Capacitor Type	Footprint	Population	Location
0.1uF X5R	0402	1	Near GPU
4.7uF X5R	0603	2	Near GPU

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Issued Date	2011/09/23	Deciphered Date	2012/12/31

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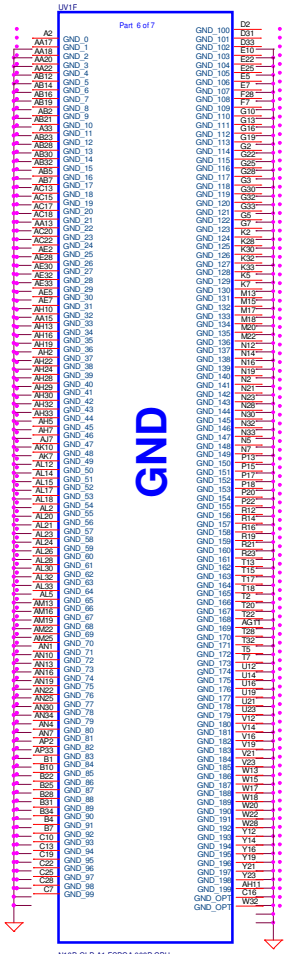

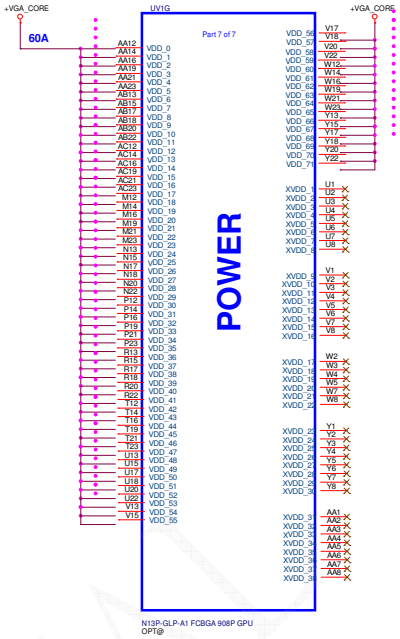

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Title	SCHEMATICS, MB A8581		
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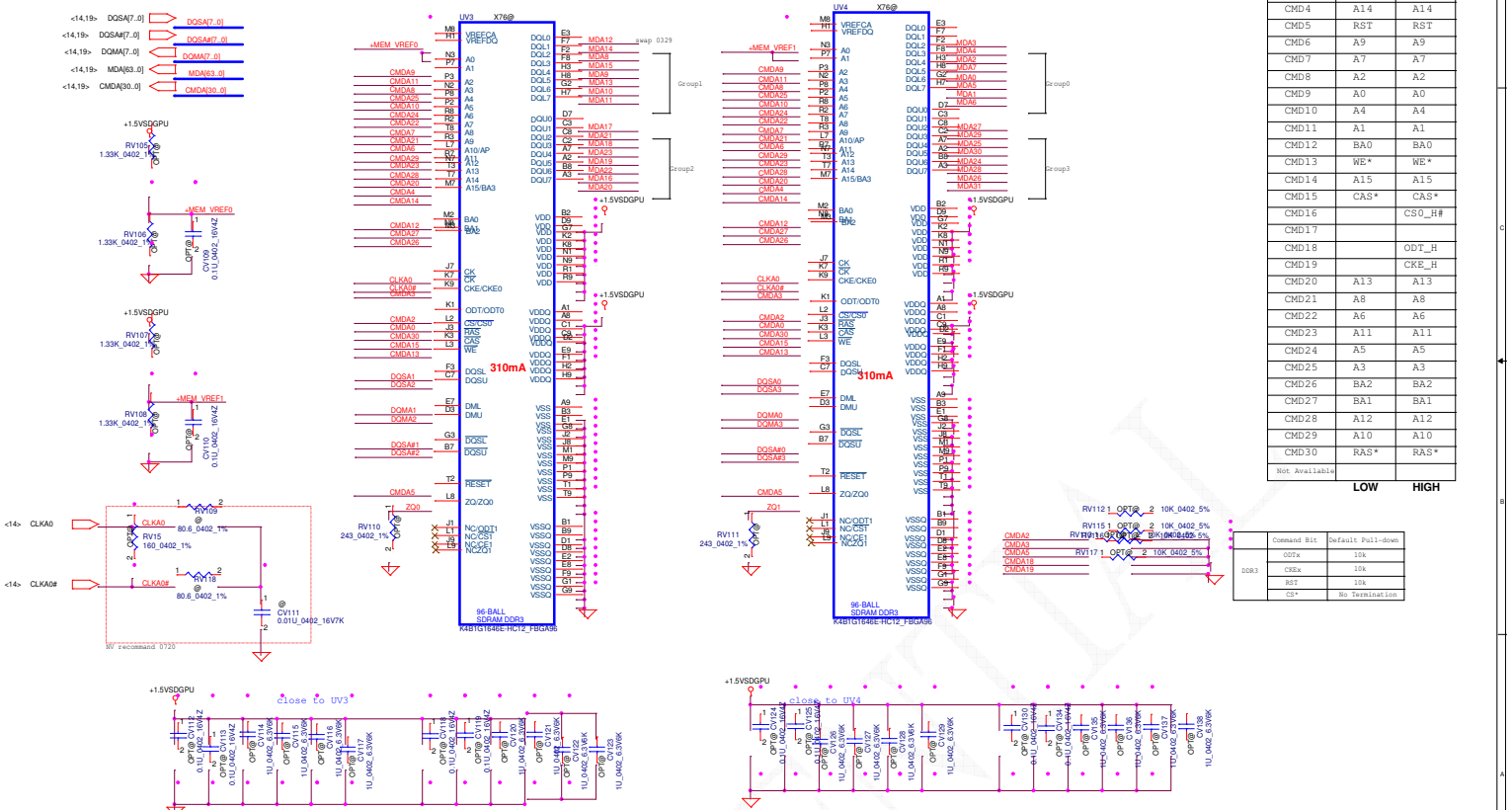
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH



Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

DDR3

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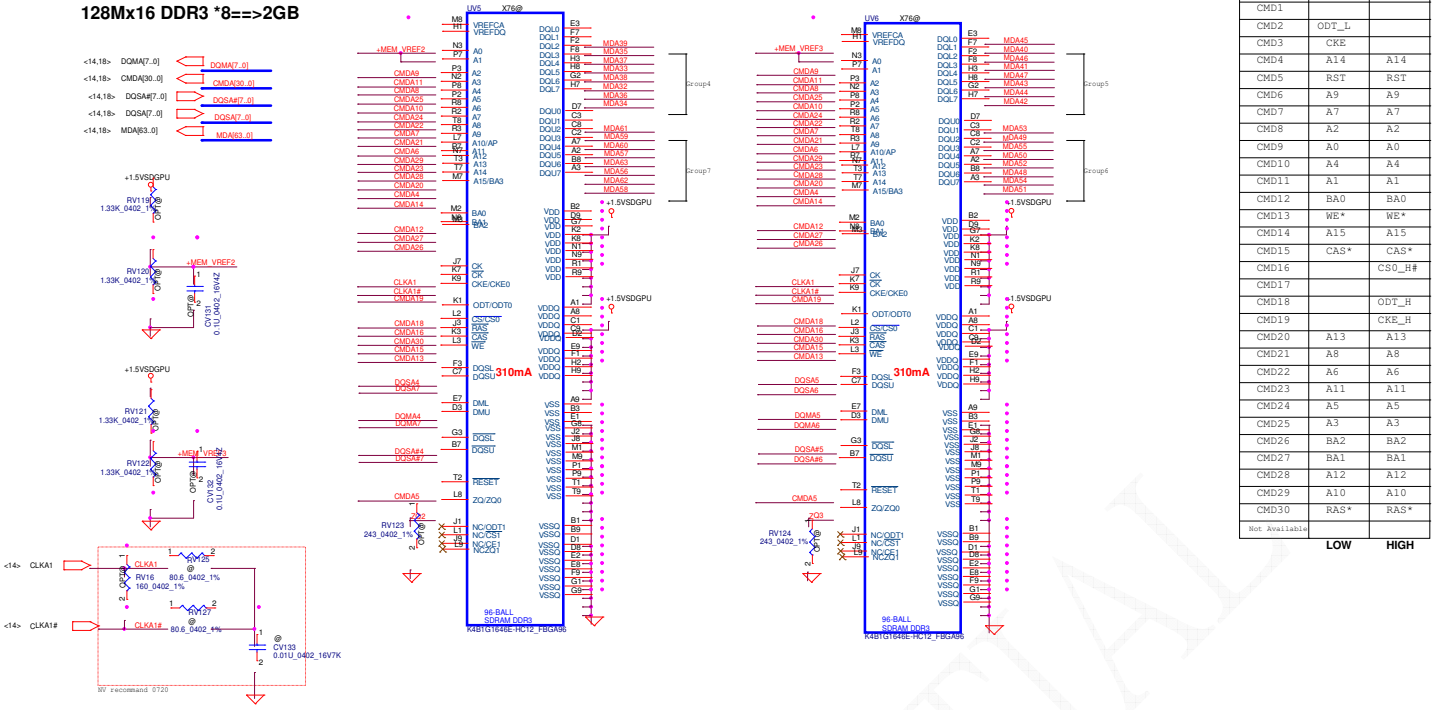
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
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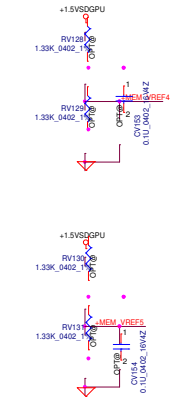
VRAM DDR3 chips (1GB)

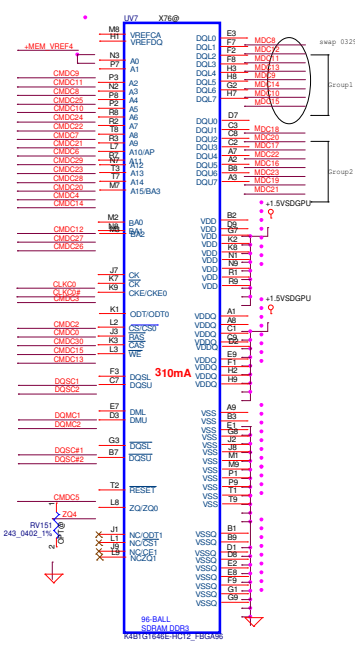
64Mx16 DDR3 *8==>1GB

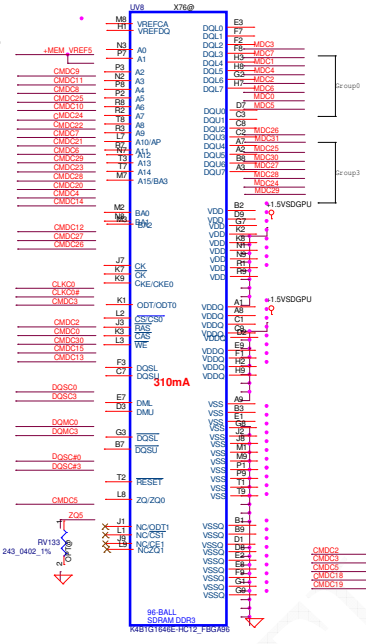
128Mx16 DDR3 *8==>2GB

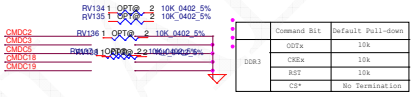
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

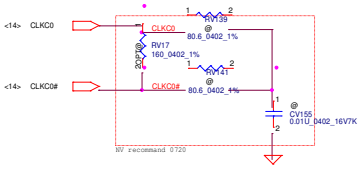


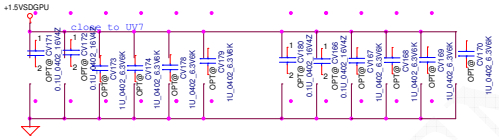


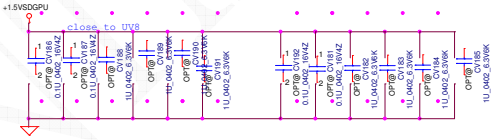




	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination







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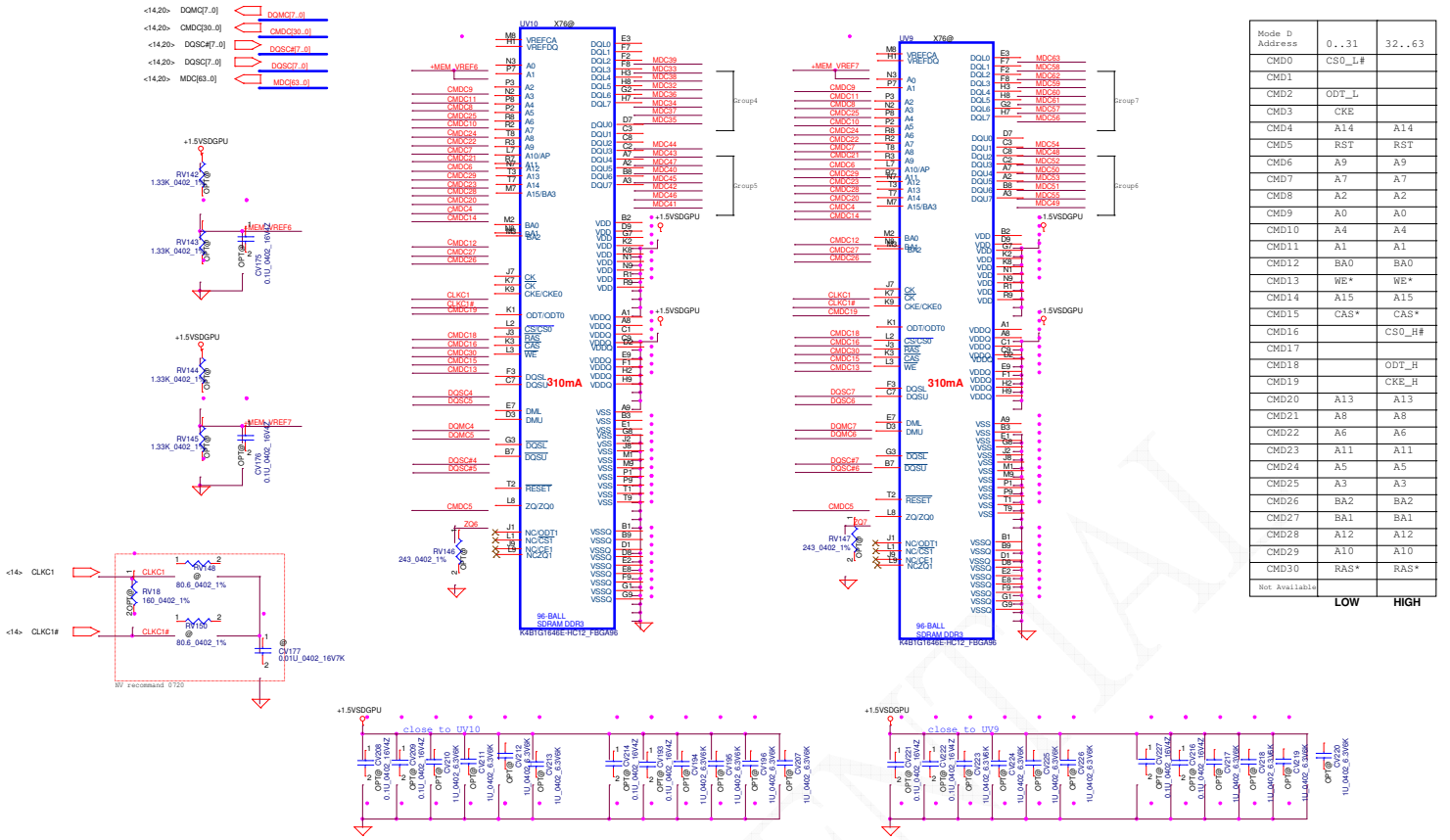
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
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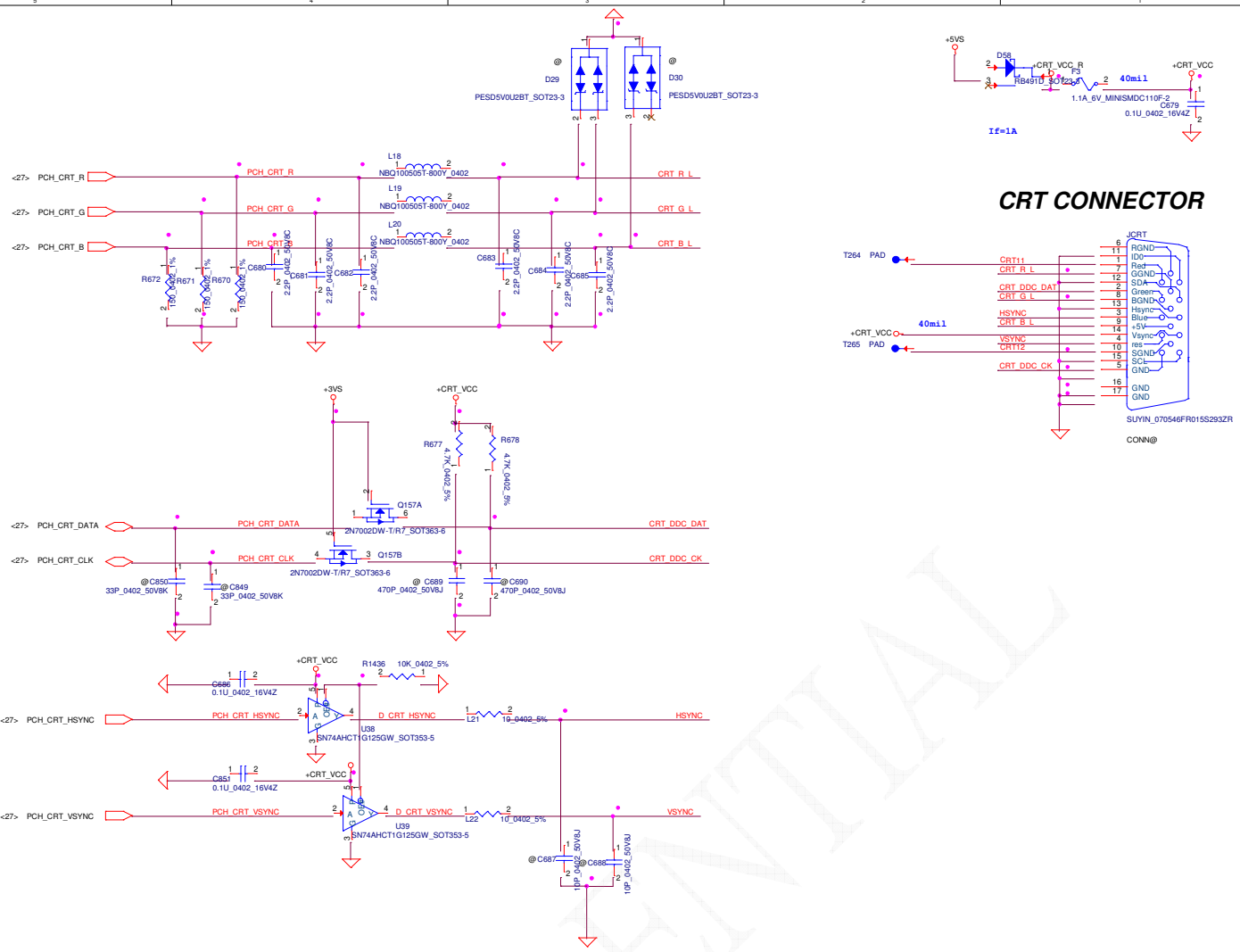

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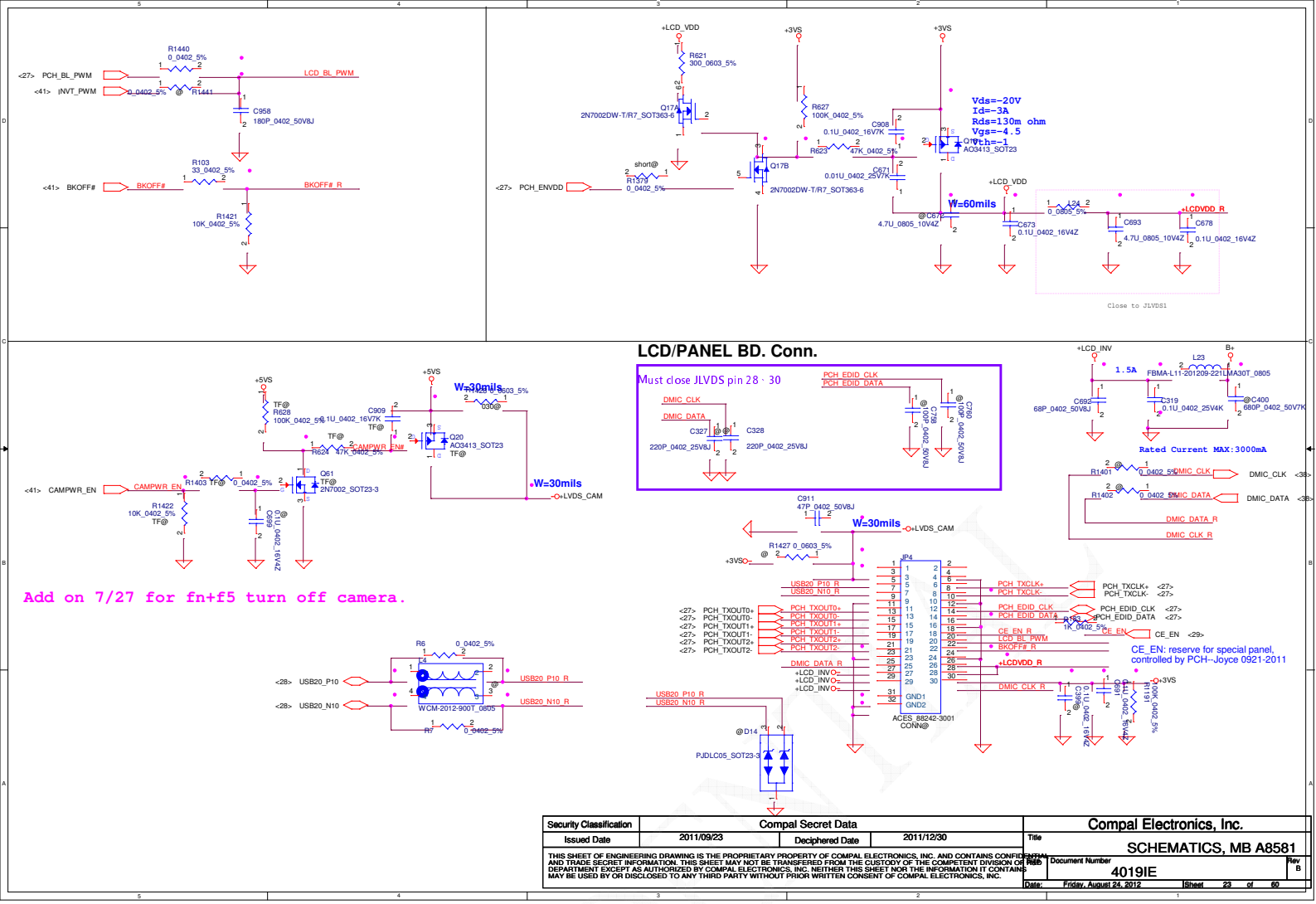
LCD/PANEL BD. Conn.
Must close JLVDS pin 28 、30
Add on 7/27 for fn+f5 turn off camera.
CE_EN: reserve for special panel, controlled by PCH--Joyce 0921-2011
Vds=-20V
Id=-3A
Rds=130m ohm
Vgs=-4.5
Vth=-1
W=30mils
W=60mils
Rated Current MAX:3000mA
Close to JLVDS1
Security Classification
Compal Secret Data
Issued Date
2011/09/23
Deciphered Date
2011/12/30
Compal Electronics, Inc.
SCHEMATICS, MB A8581
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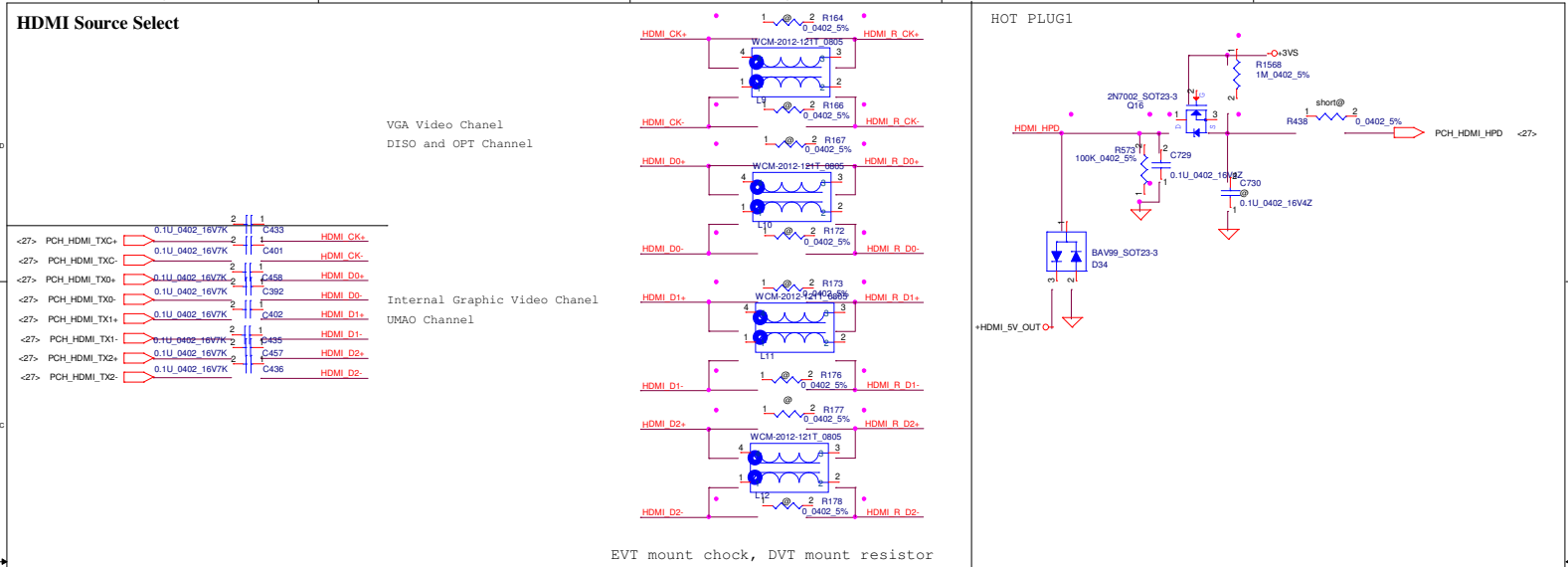
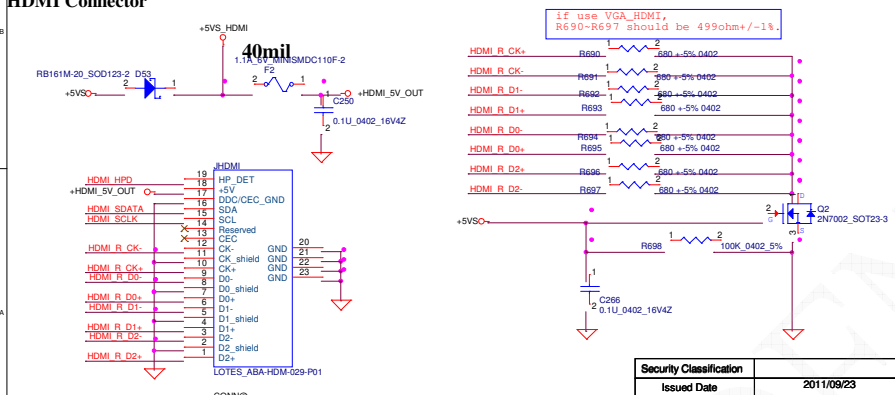
HDMI Source Select

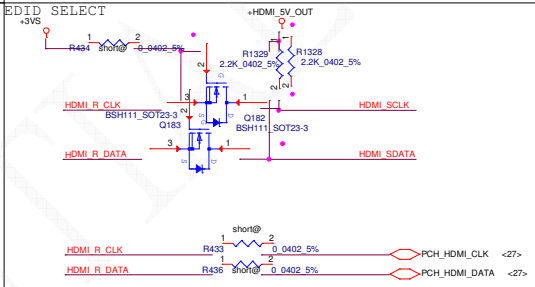


HOT PLUG1

HDMI Connector



EDID SELECT



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/09/23	Deciphered Date	2011/12/30
			Title: SCHEMATICS, MB A8581
			Size: Document Number: 4019IE Rev: B
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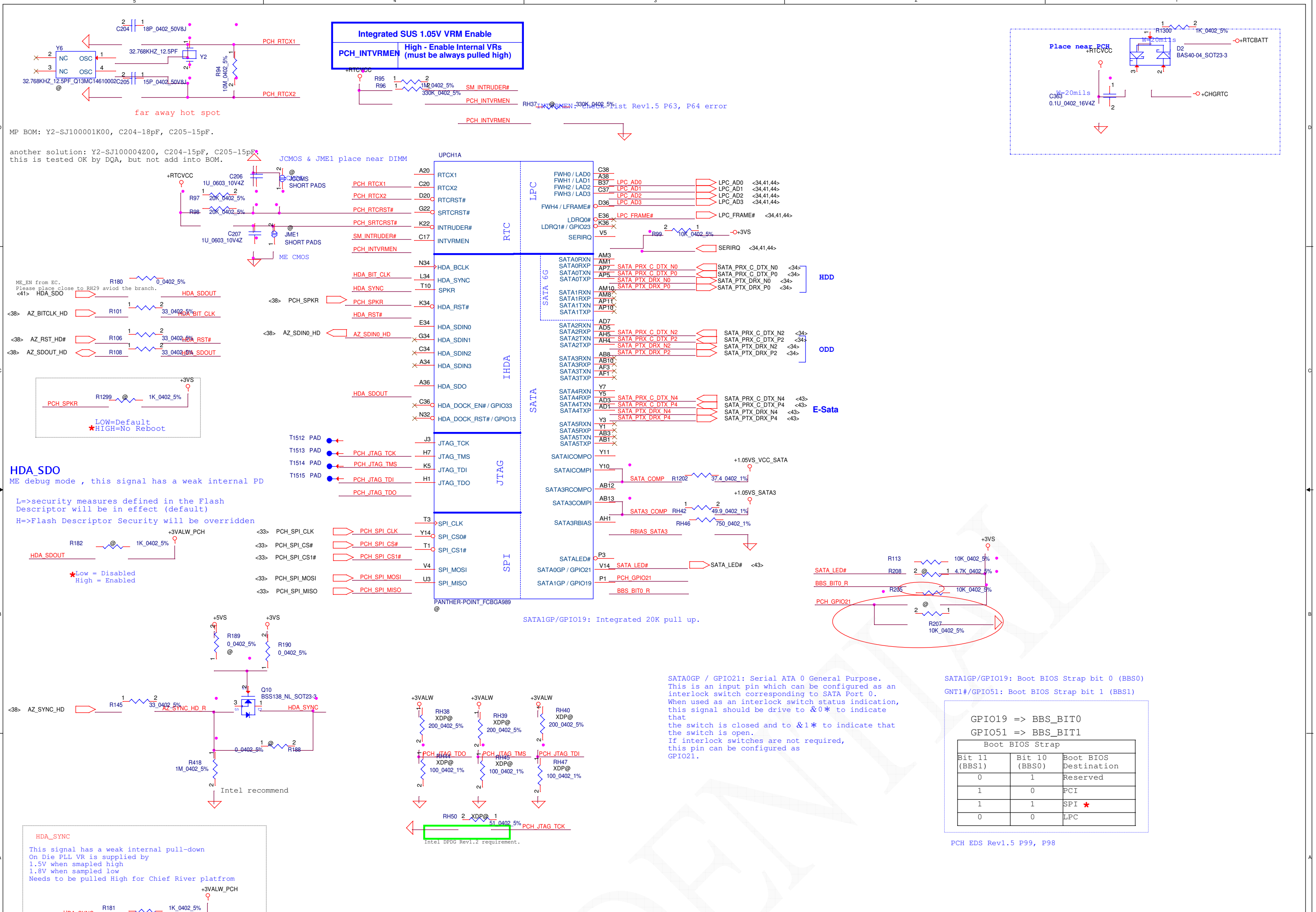

Integrated SUS 1.05V VRM Enable
PCH_INTVRMEN
High - Enable Internal VRs (must be always pulled high)
far away hot spot
MP BOM: Y2-SJ100001K00, C204-18pF, C205-15pF.
another solution: Y2-SJ100004Z00, C204-15pF, C205-15pF
this is tested OK by DQA, but not add into BOM.
JCMOS & JME1 place near DIMM
ME CMOS
Place near PCH
UPCH1A
RTC
LPC
SATA 6G
IHDA
SATA
JTAG
SPI
HDD
ODD
E-Sata
ME_EN from EC.
Please place close to RH29 aviod the branch.
LOW=Default
HIGH=No Reboot
HDA_SDO
ME debug mode , this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden
Low = Disabled
High = Enabled
PANTHER-POINT_FCBGA989
SATA1GP/GPIO19: Integrated 20K pull up.
Intel recommend
SATA0GP / GPIO21: Serial ATA 0 General Purpose. This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to ‘0’ to indicate that the switch is closed and to ‘1’ to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP/GPIO19: Boot BIOS Strap bit 0 (BBS0)
GNT1#/GPIO51: Boot BIOS Strap bit 1 (BBS1)
GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1
Boot BIOS Strap
PCH EDS Rev1.5 P99, P98
HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Chief River platfrom
CONFIDENTIAL

Boot BIOS Strap

Bit 11 (BBS1)	Bit 10 (BBS0)	Boot BIOS Destination
0	1	Reserved
1	0	PCI
1	1	SPI *
0	0	LPC

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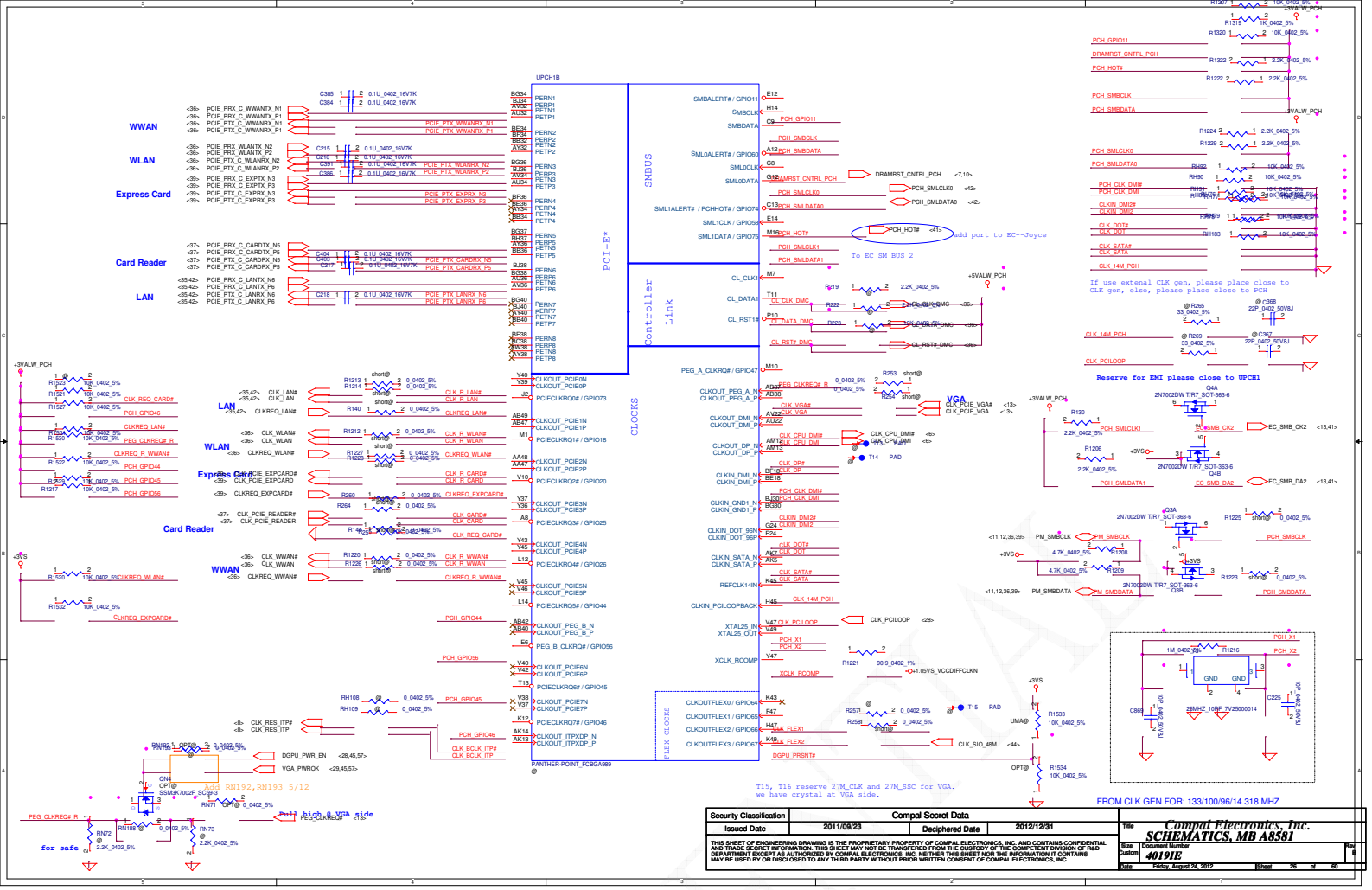

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Title	Compal Electronics, Inc. SCHEMATICS, MB A8581		
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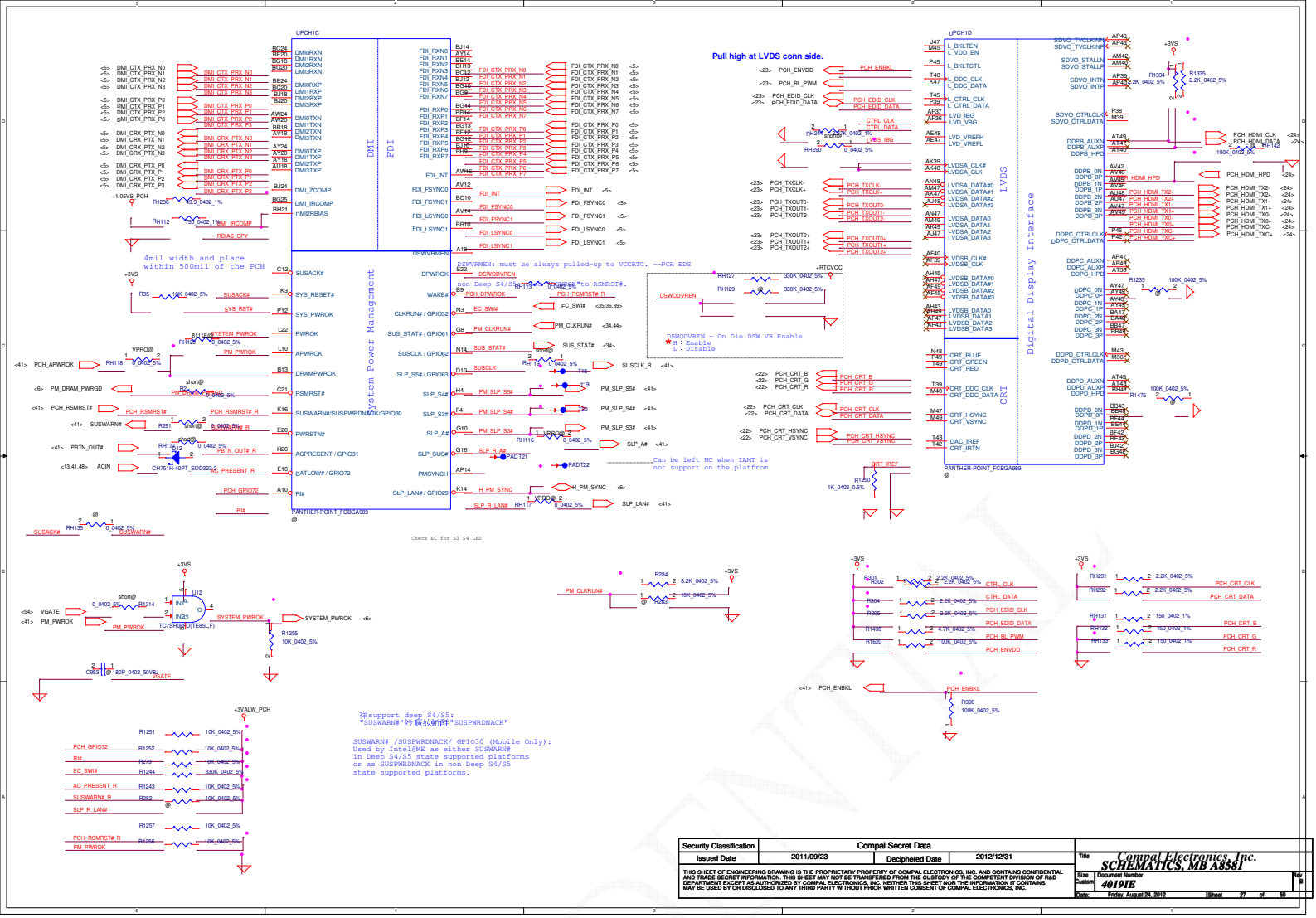

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Issued Date	2011/09/23	Deciphered Date	2012/12/31

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Size: Custom	Document Number: 4019IE		Rev: 0
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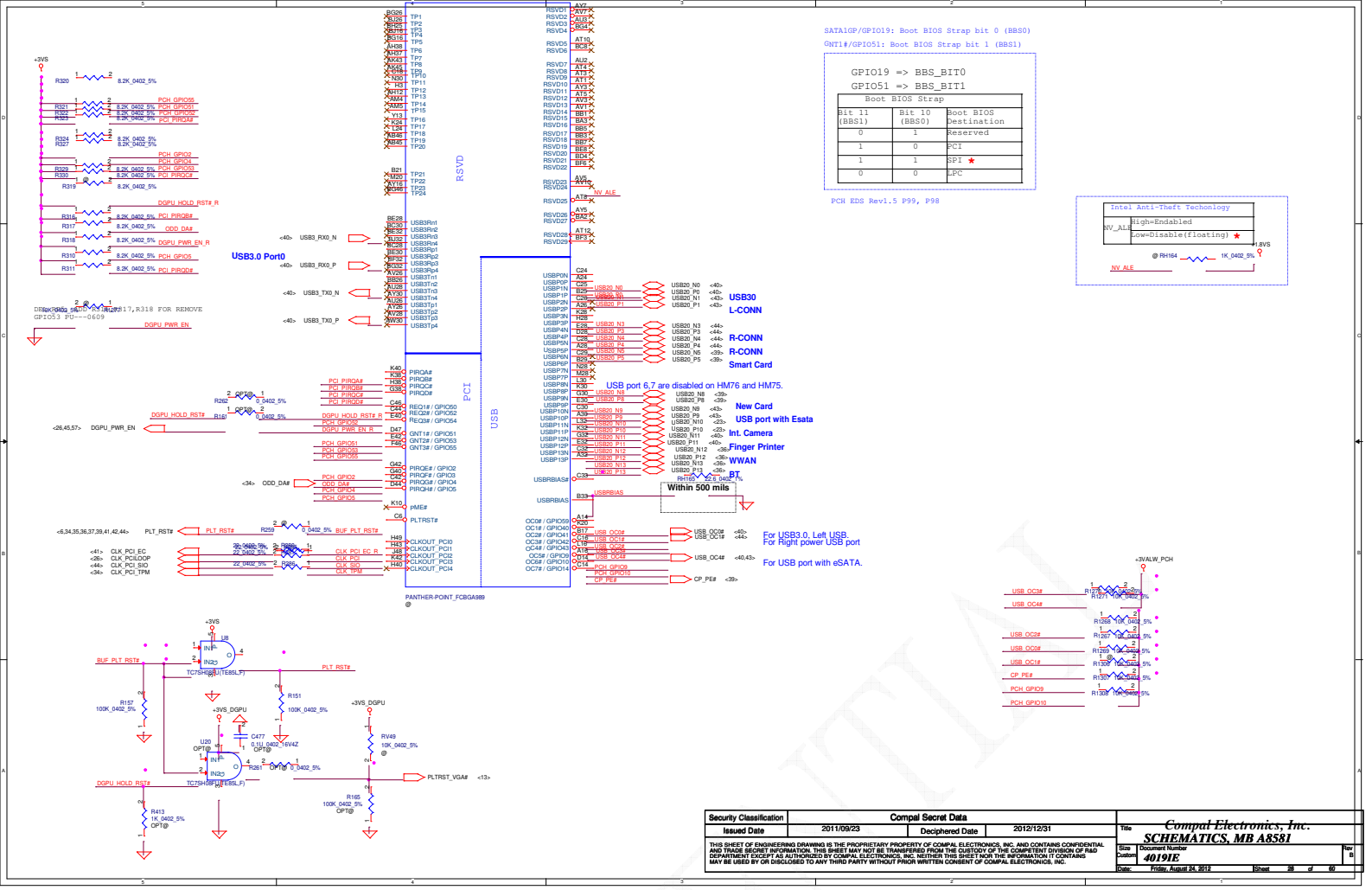

Security Classification	Compal Secret Data		
Issued Date	2011/09/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.

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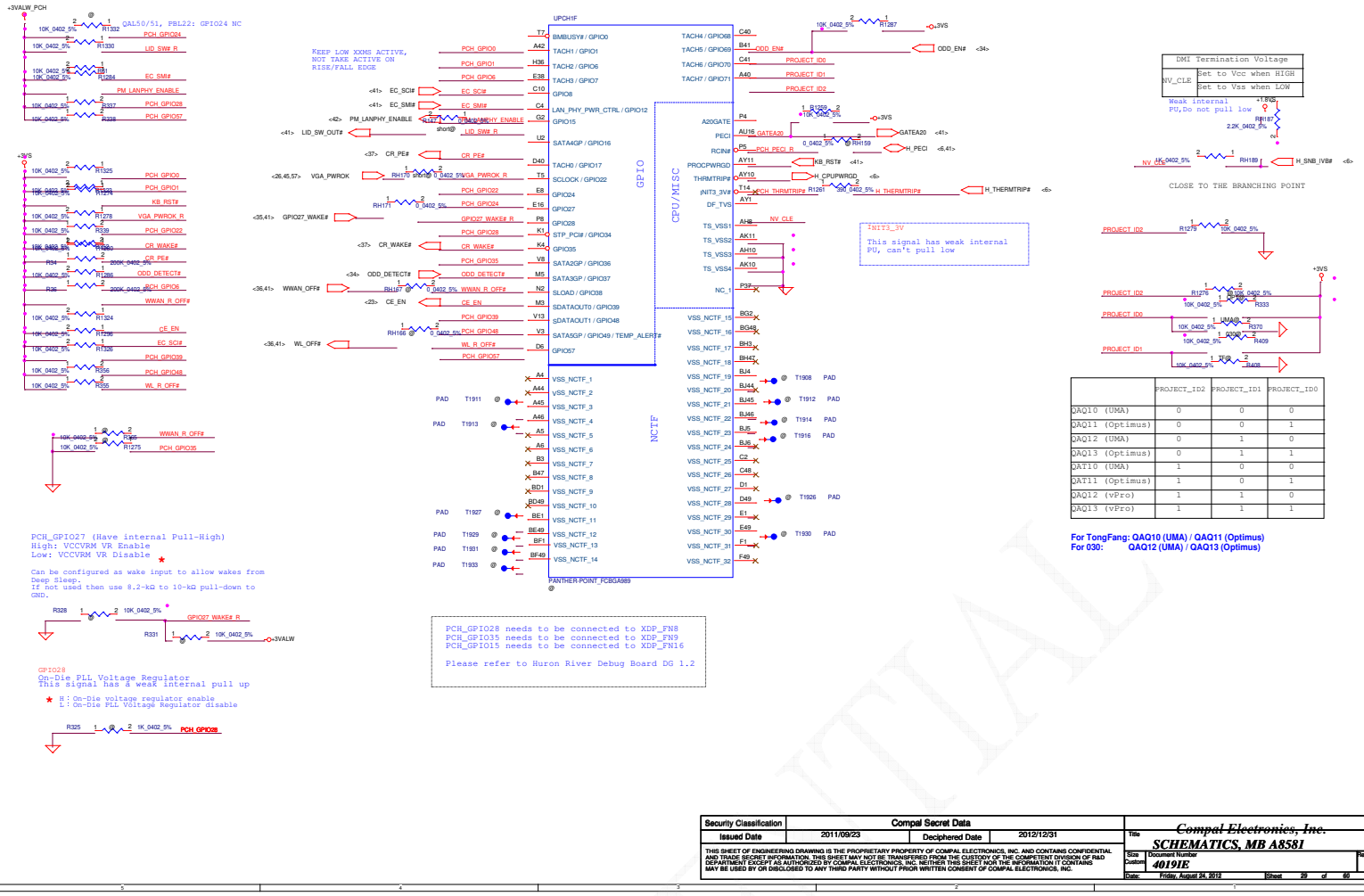

	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
QAQ10 (UMA)	0	0	0
QAQ11 (Optimus)	0	0	1
QAQ12 (UMA)	0	1	0
QAQ13 (Optimus)	0	1	1
QAT10 (UMA)	1	0	0
QAT11 (Optimus)	1	0	1
QAQ12 (vPro)	1	1	0
QAQ13 (vPro)	1	1	1

Security Classification	Compal Secret Data		
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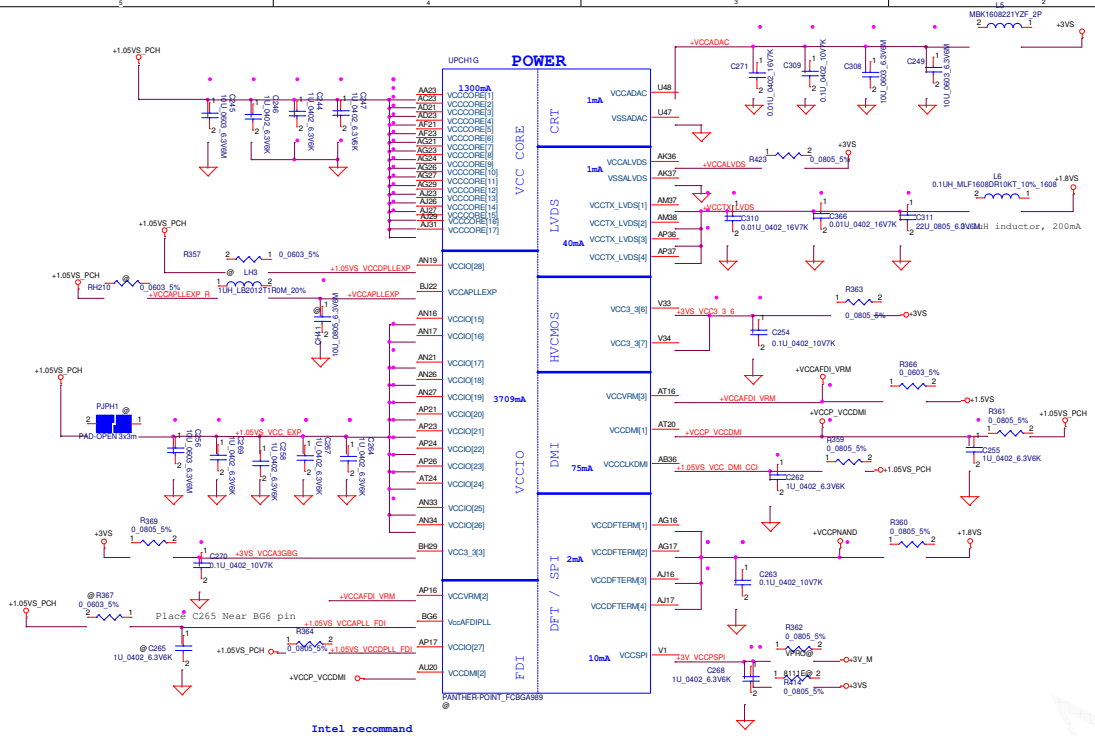

PCH Power Rail Table
Refer to PCH EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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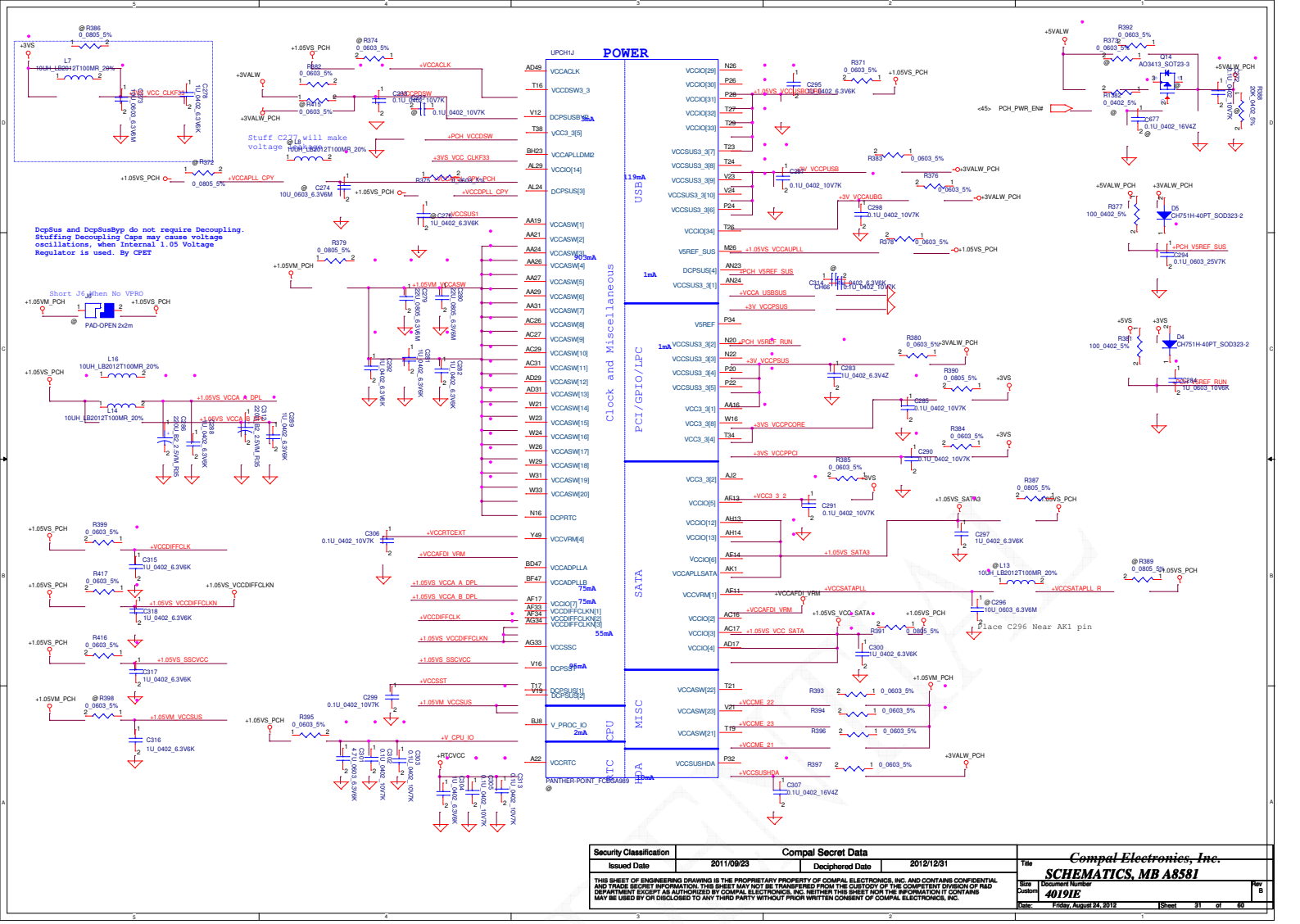

Security Classification	Compal Secret Data		
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Title	Compal Electronics, Inc.		
	SCHEMATICS, MB A8581		
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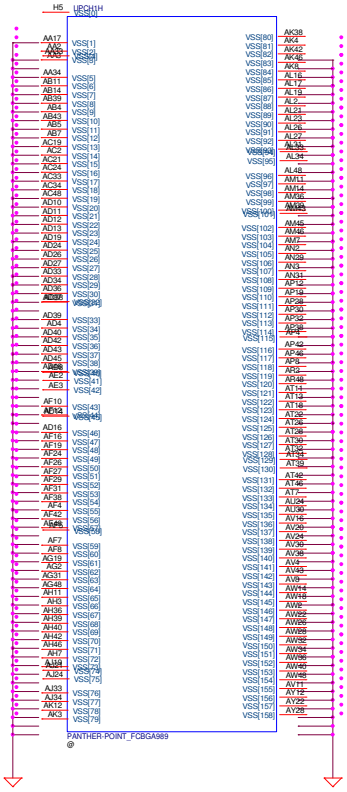

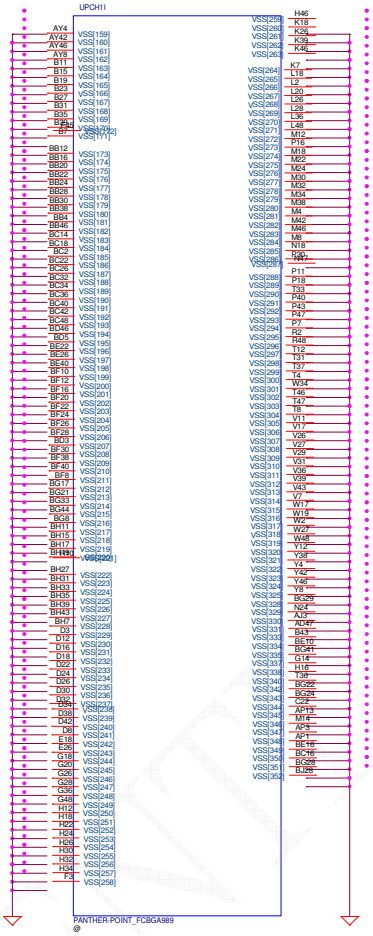

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Compal Electronics, Inc.			
Title: SCHEMATICS, MB A8581			
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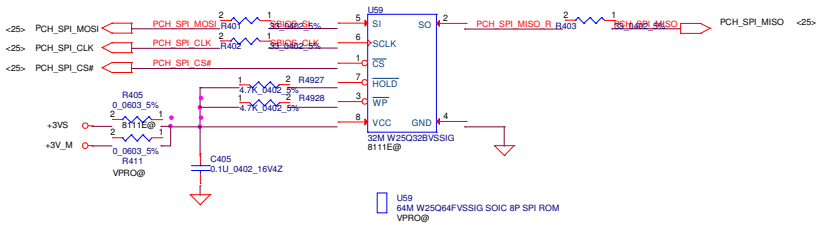
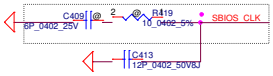
SBIOS SPI Flash

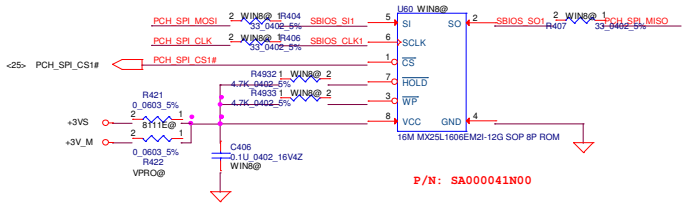


For EMI resuest.



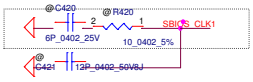
U59:
Vpro--SA000039A20 8MB
non-Vpro--SA00003K800 4MB

BIOS SPI Flash (2MByte*1) For Win8



P/N: SA000041N00

For EMI resuest.



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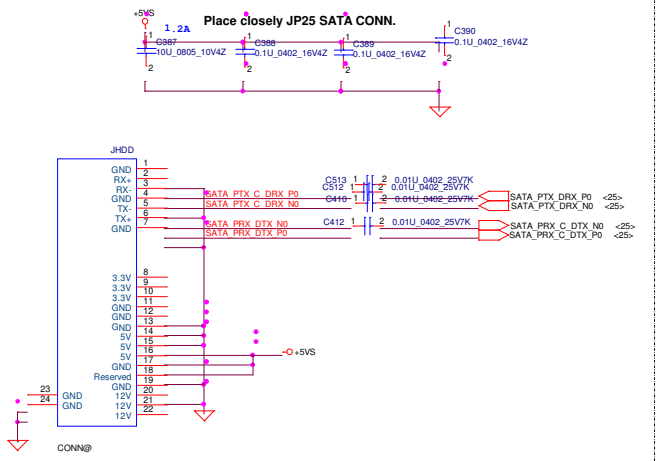
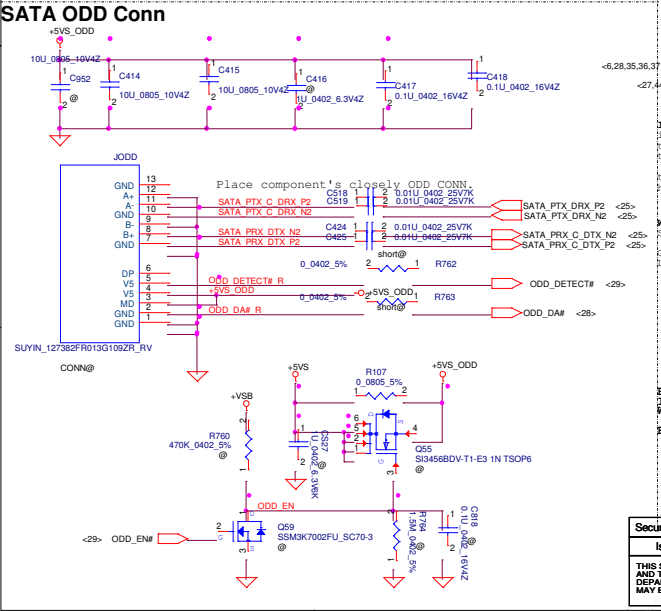
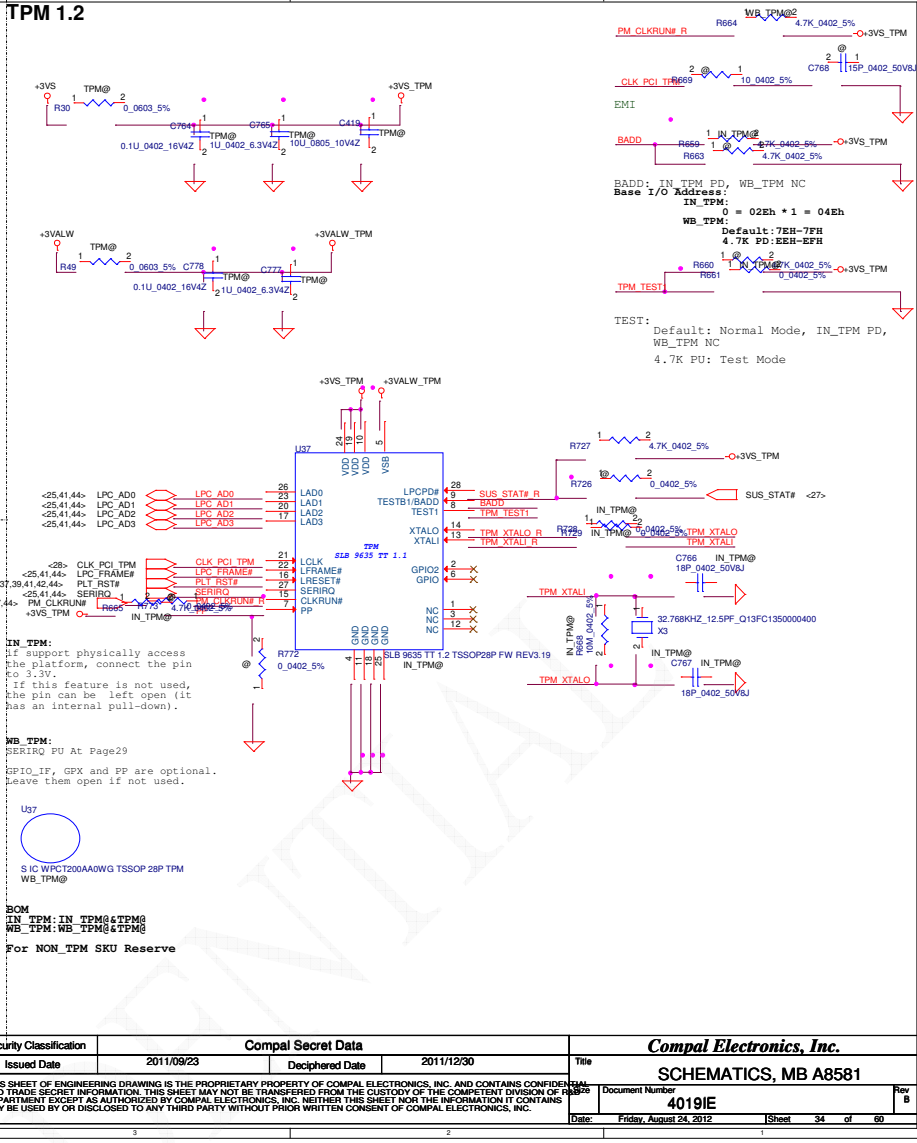
SATA HDD Conn.



SATA ODD Conn



TPM 1.2



BOM
IN_TPM:IN_TPM@&TPM@
WB_TPM:WB_TPM@&TPM@

For NON_TPM SKU Reserve

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IC function Part

	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

LanWake O/D PU at Page31. Used to reactivate PCIE slot's main PWR rail and REF CLK

ISOLATEB used to isolate 8111E from PCIE

CLKREQ O/D PU at PCH side

SMBDATA and GPO using EFuse only without ASF function.

RTL8111E-VL-CGT QFN 48P

PWR

Layout Note: LL must be within 200mil to Pin36, CL13,CL9 must be within 200mil to LL1

LL1,0L13 will be changed to 2.2uH&4.7uF after EVT test

Close to Pin 21

Close to Pin 27,39,12,47,48

CL7 close to pin12

Close to Pin 3,6,9,13,29,41,45

CL23,CL24,CL25 close to pin6,9,41, respectively

+3VALW TO +3V_LAN

Vgs=-4.5V, Rds<97mohm

Crystal

25MHZ_10PF_7V25000014

CL11 close to pin42

LAN Conn.

JLAN1 CONN@

LIYO_101002-00803-3

Transformer

UL5 NS892407 TG

Place CL34 colse to LAN chip

Intel check:Better to put 4x 0.1uF bypass cap near 4 central tap pin of Transformer.

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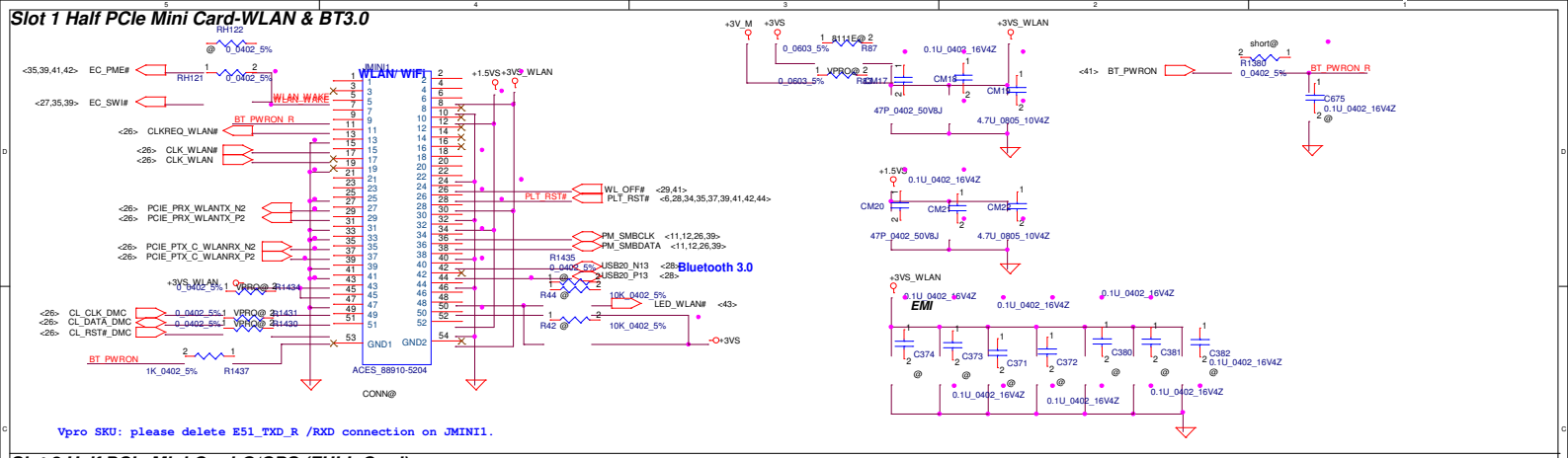
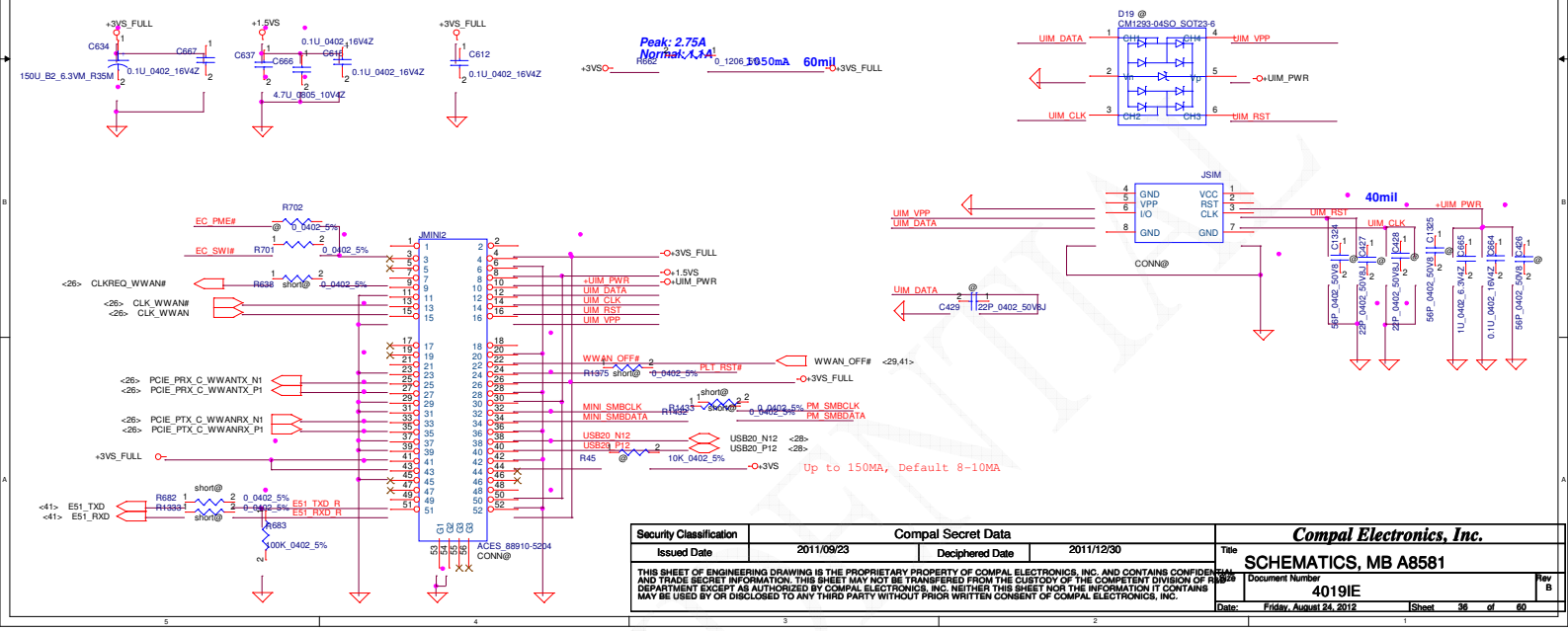
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Vpro SKU: please delete E51_TXD_R /RXD connection on JMINI1.

Slot 2 Half PCIe Mini Card-G/GPS (FULL Card)



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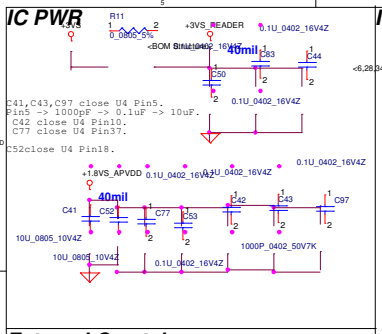
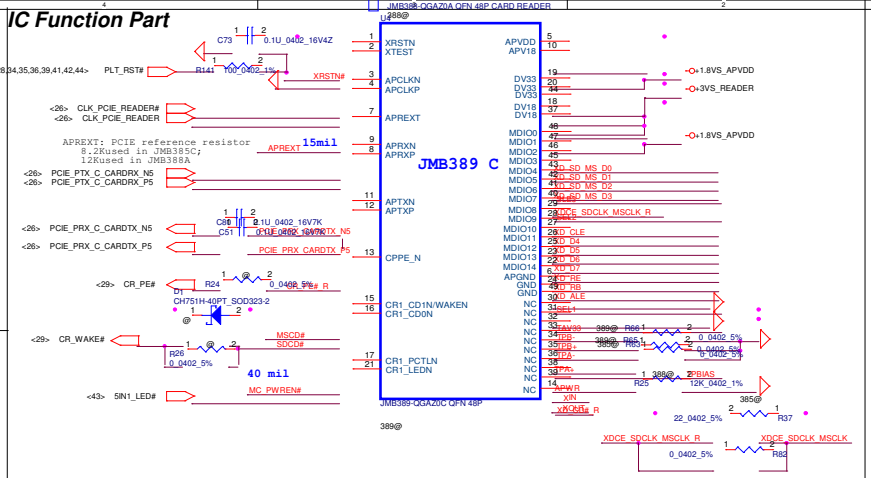
IC PWR

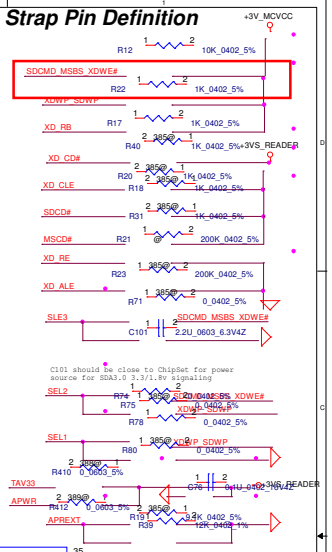


IC Function Part

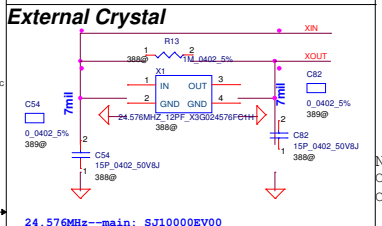


Note:
Colay With JMB385; W/1394, mount JMB388;WO/1394, mount JMB385.
CR_PE# and CR_WAKE reserve for D3 mode

Strap Pin Definition

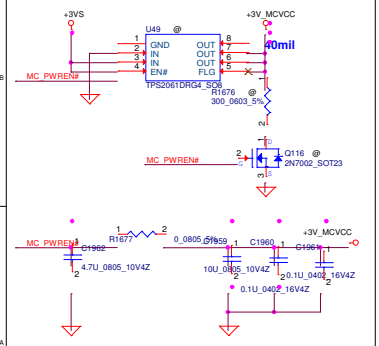


External Crystal



24.576MHz--main: SJ10000EV00

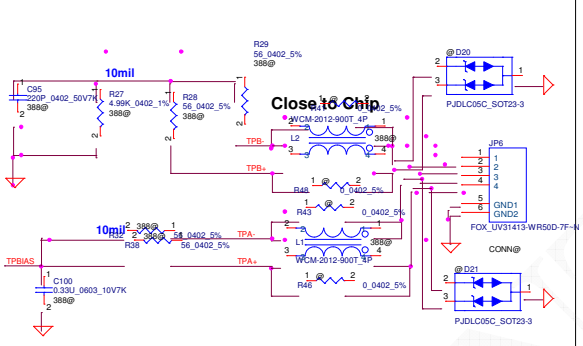
Memory Card Power



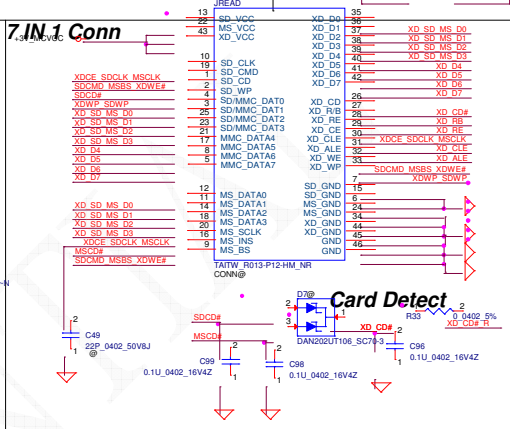
Note:

if use external PWR and change
+3V_MCPWR as control signal, Need BIOS
to change the Setting.

1394 Conn



7 IN 1 Conn



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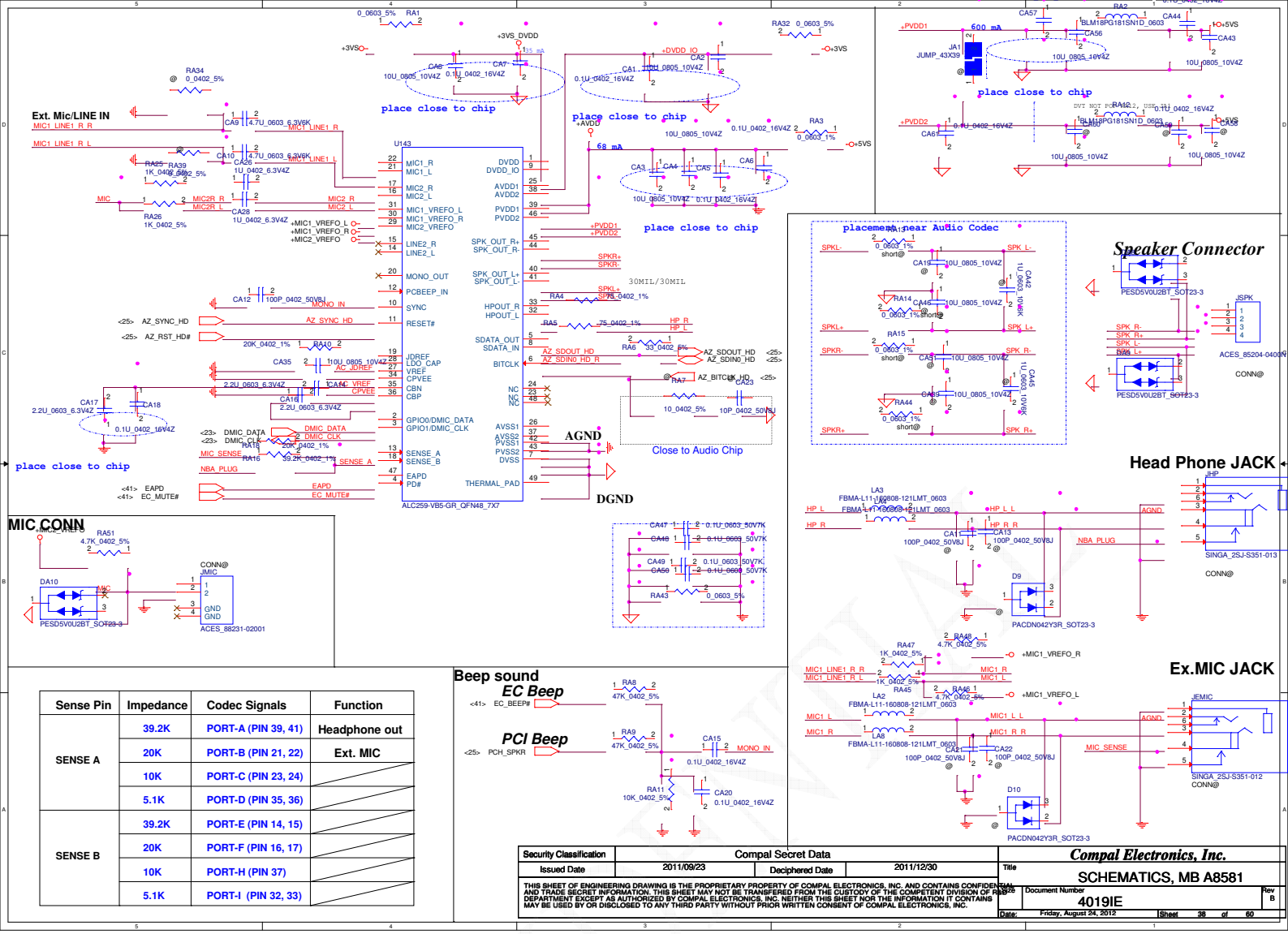

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	

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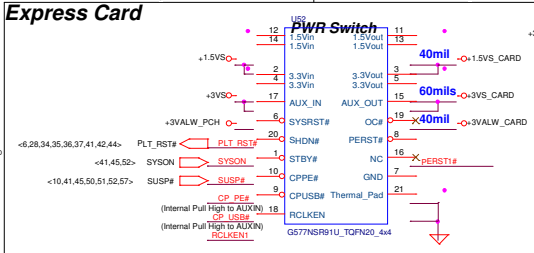
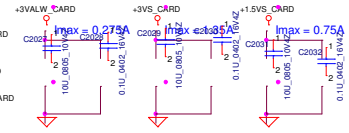
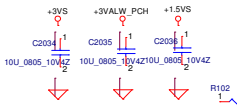
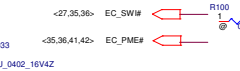
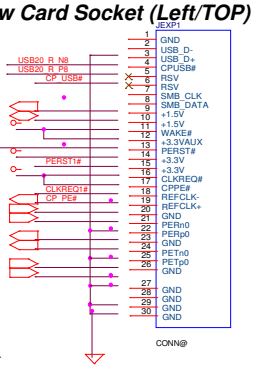
Express Card







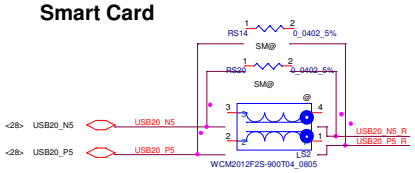


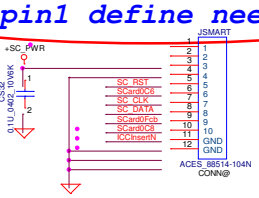


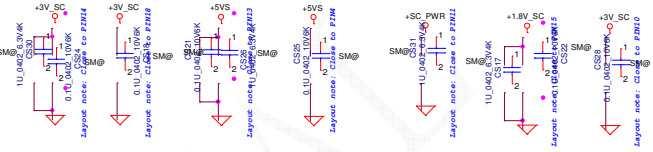
New Card Socket (Left/TOP)

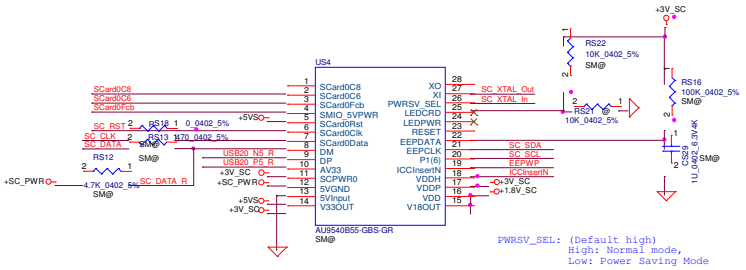
This pin1 define need check

Smart Card

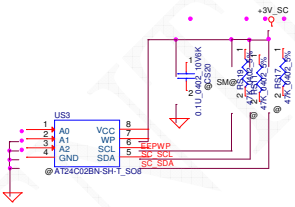


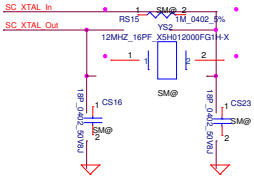






PWRSV_SEL: (Default high)
High: Normal mode,
Low: Power Saving Mode





MP: to solve issue of "Smart Card also show in Device Manager after plug out it", change US4 from SA000042I00 to SA000042I10.

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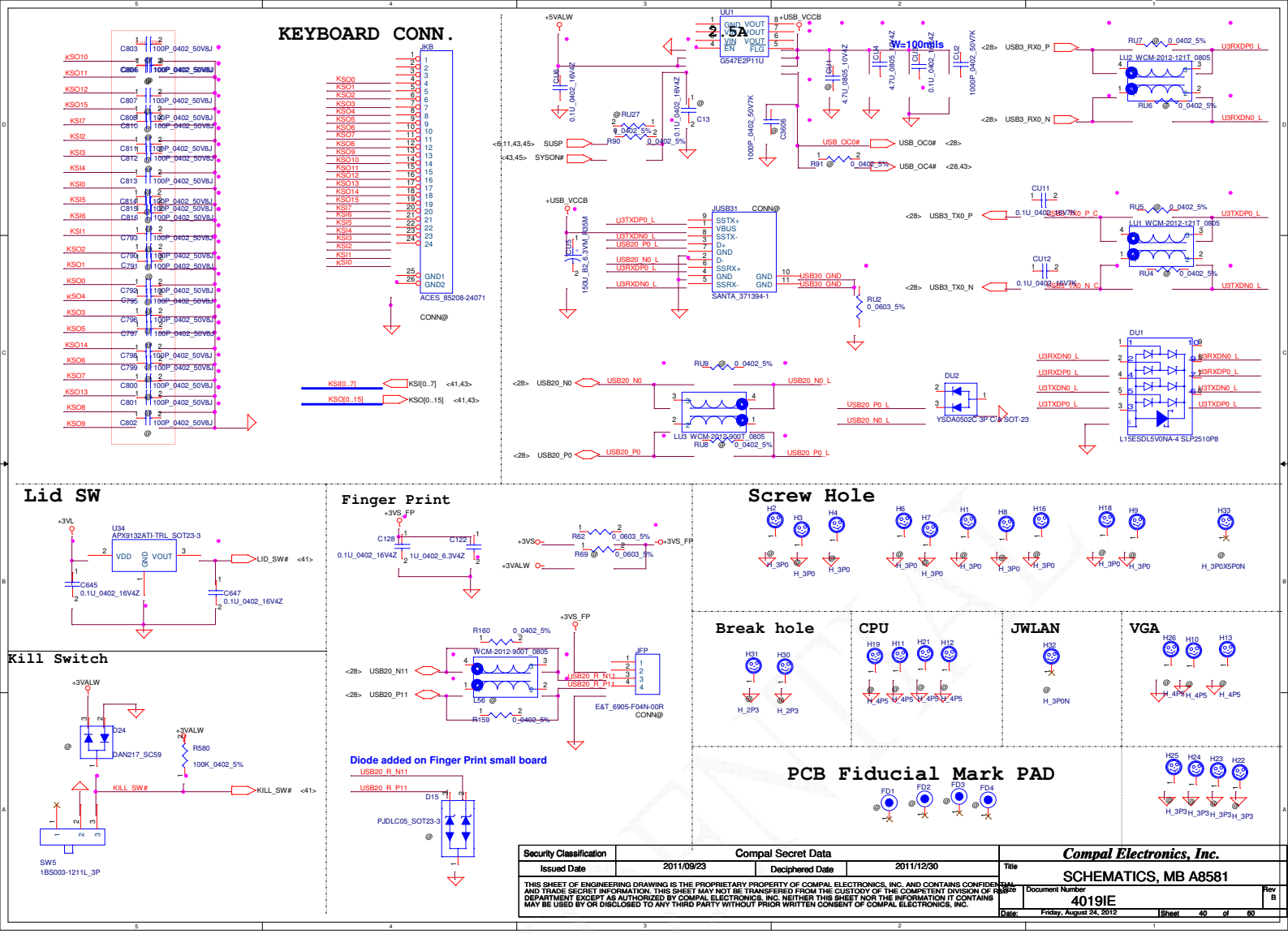

Lid SW

Kill Switch

Finger Print

Screw Hole

Break hole

CPU

JWLAN

VGA

PCB Fiducial Mark PAD

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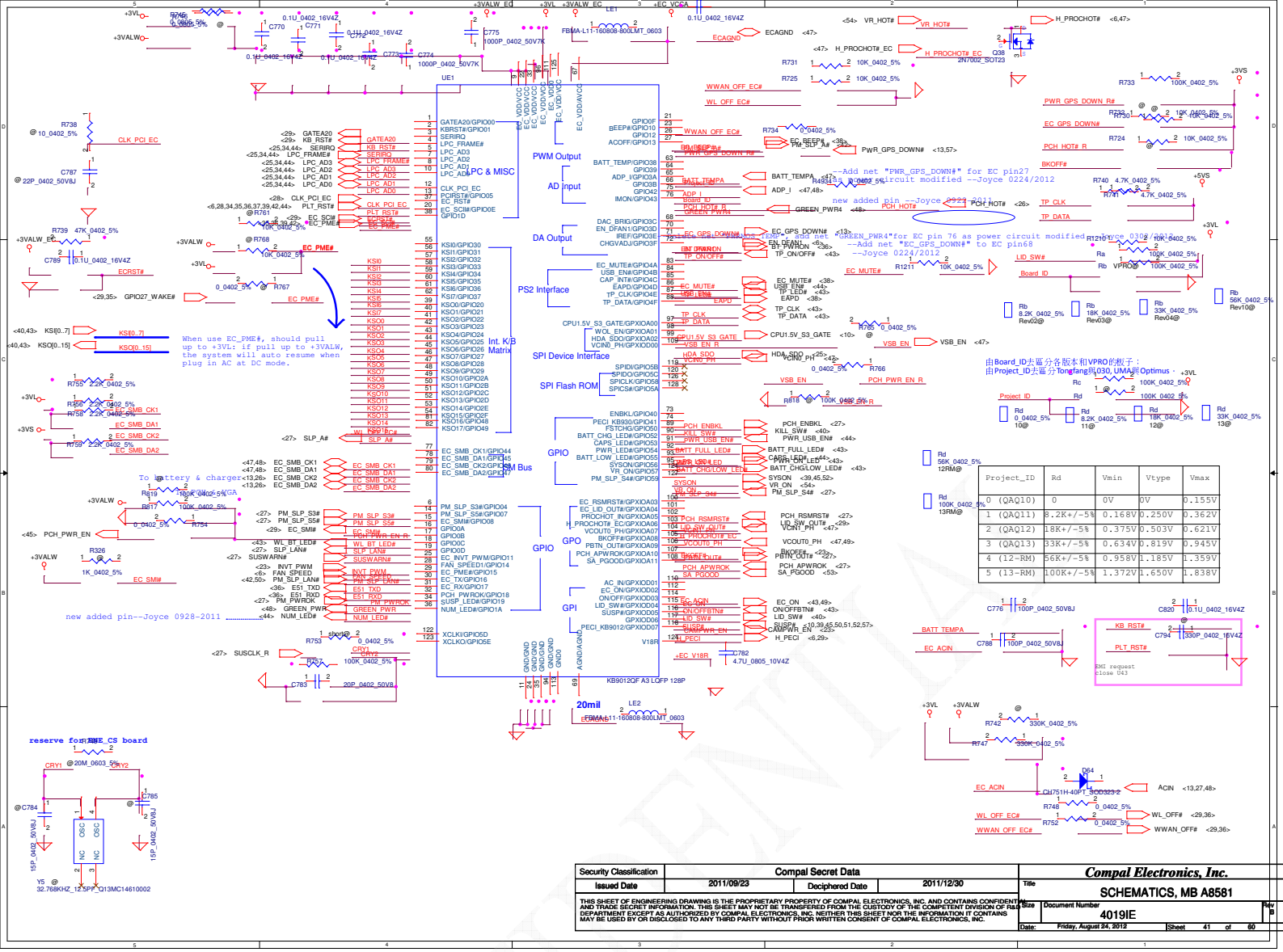

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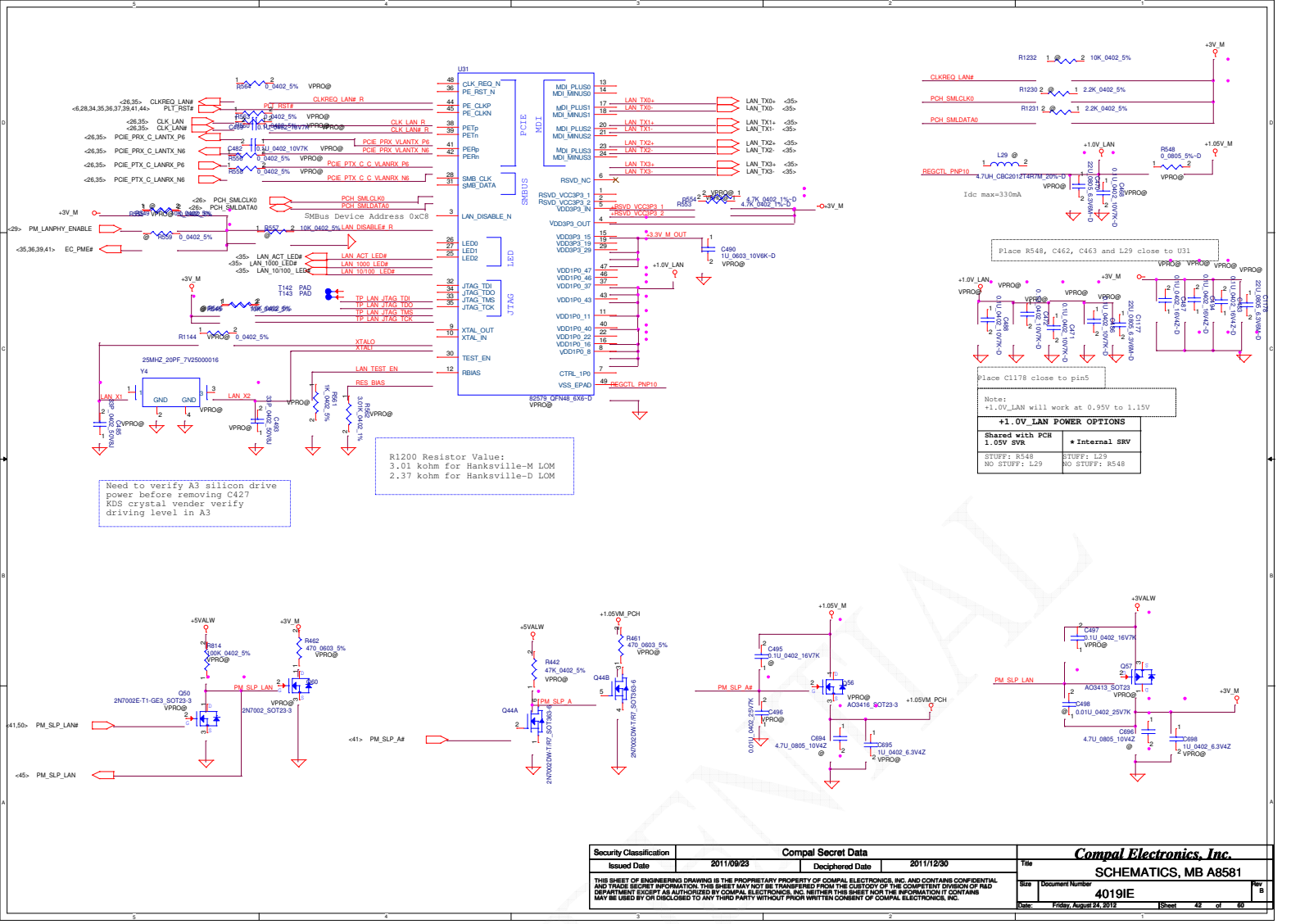

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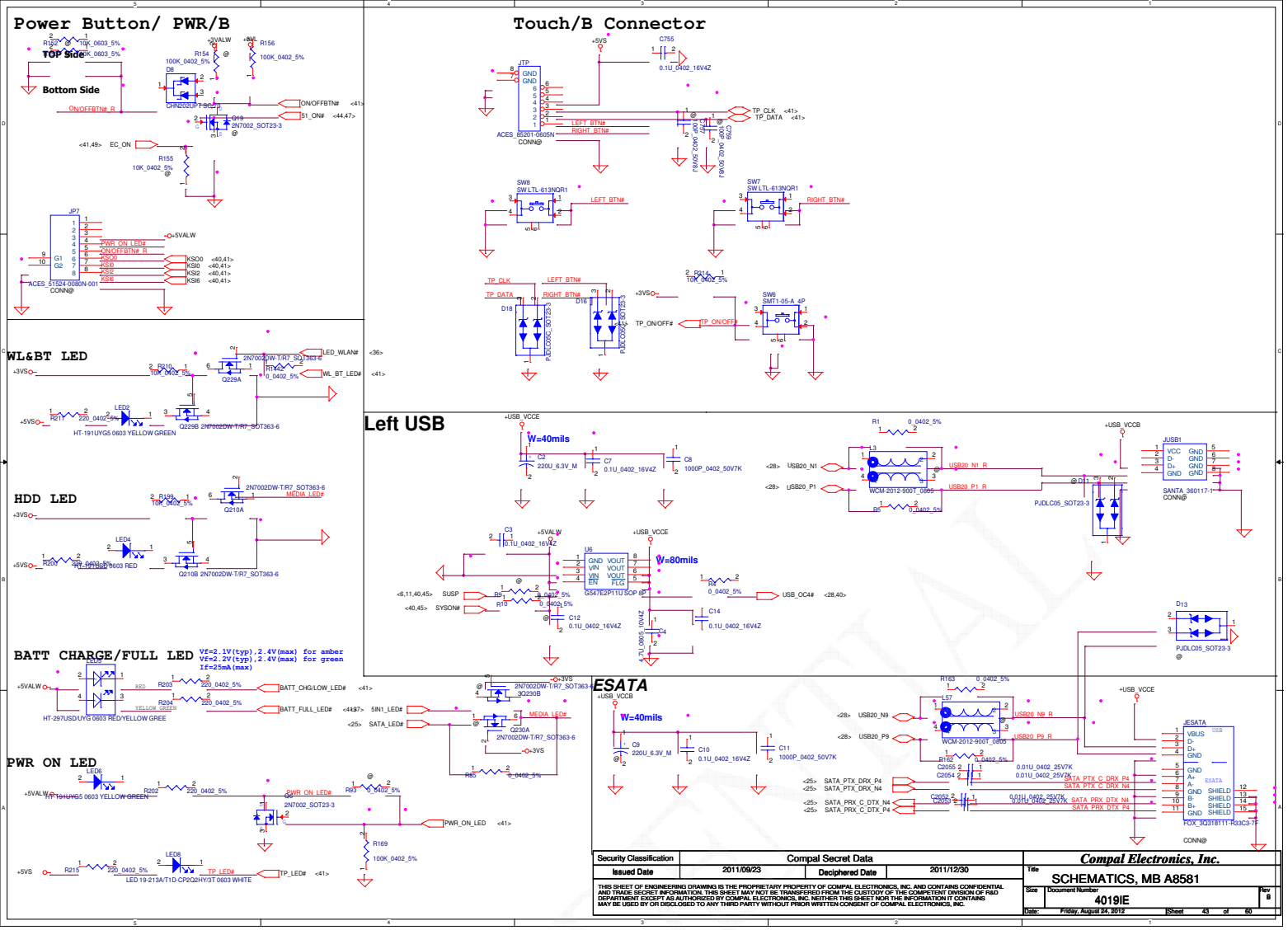

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EMI And ESD

Reserve R199,C207,R226,C208 <EMI> 0601

Place closely pin 18

Place closely pin 1

Add CR7,CC1 for EMI test fail issue--0929-2011

Reserve C292 for SIO_RST# <ESD> 0608

Base Address Selection
mount : 4E unmount : 2E

PWR USB

change from +3VALW to +3VL since EC power source changed. --Joyce 1110

W=80mils

W=60mils

E&T_6916-Q26N-00R

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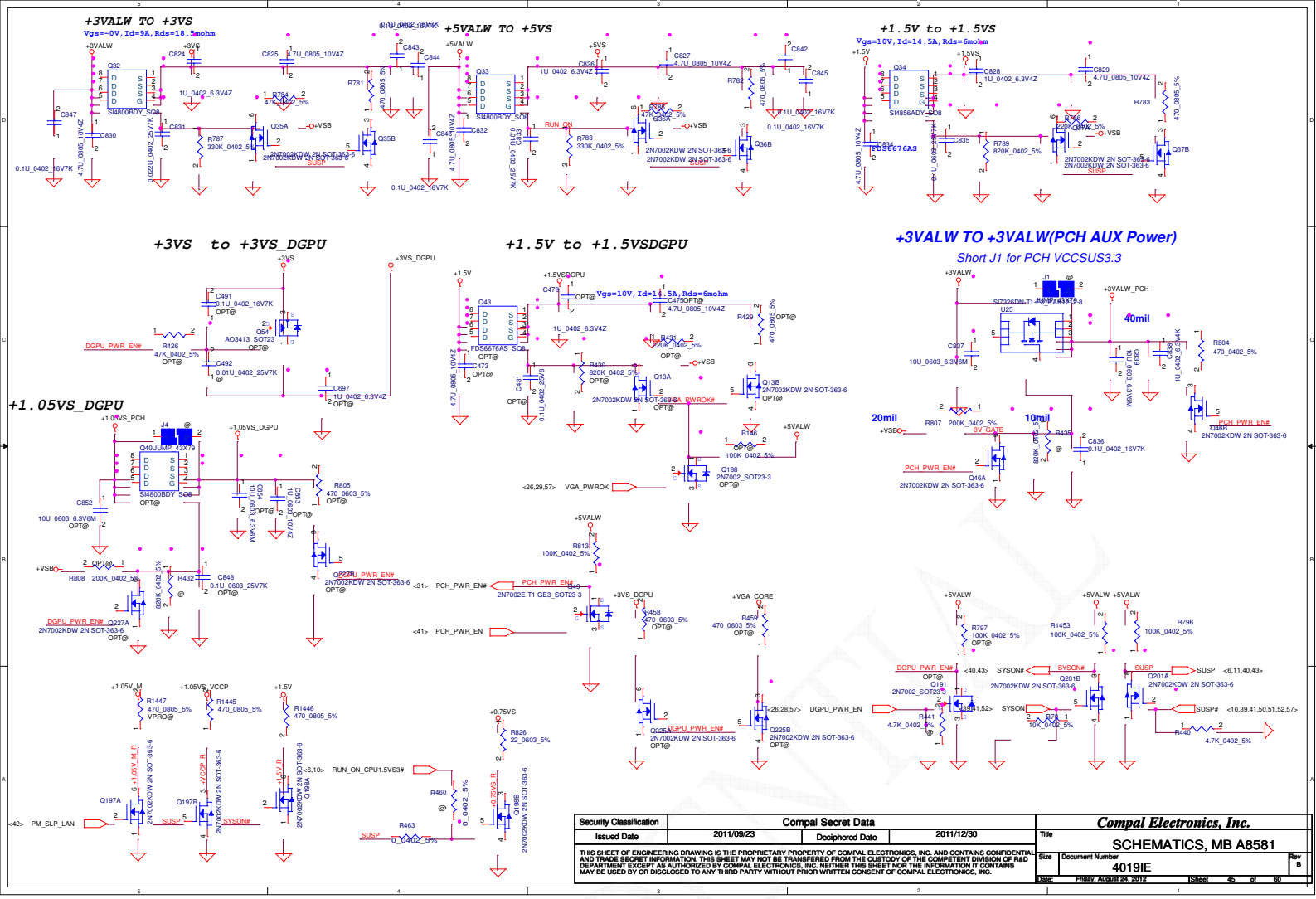
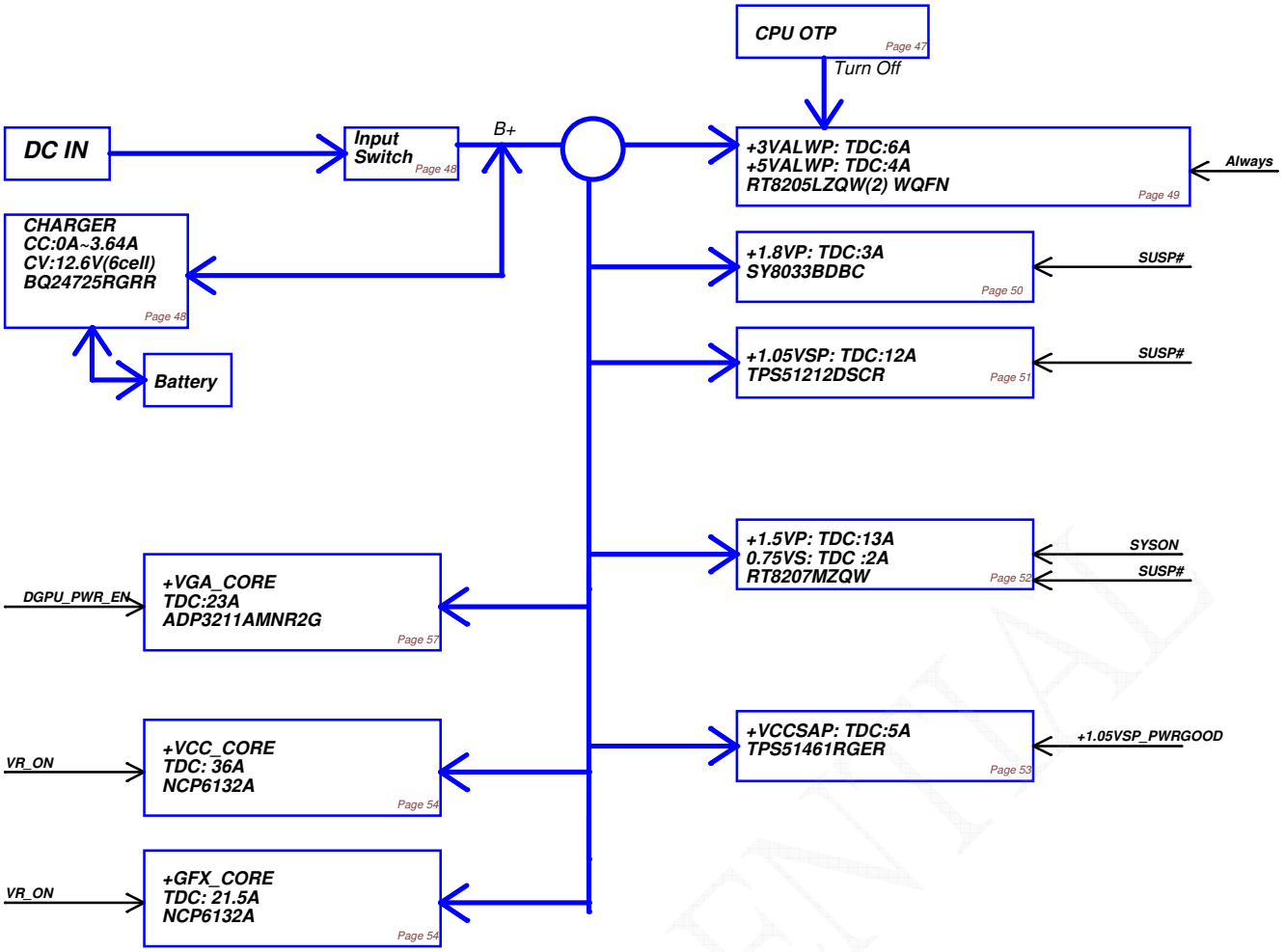


Power block



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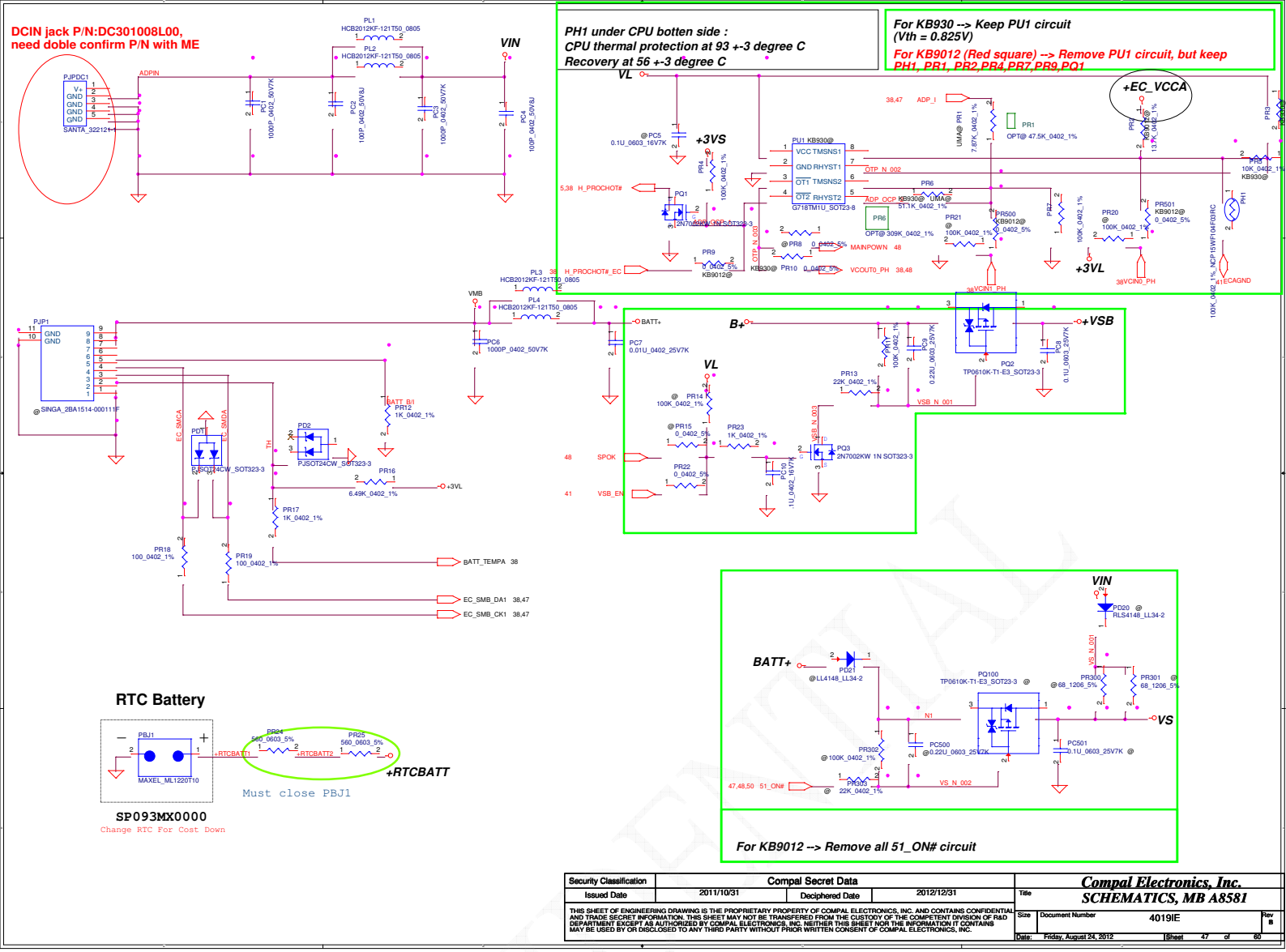

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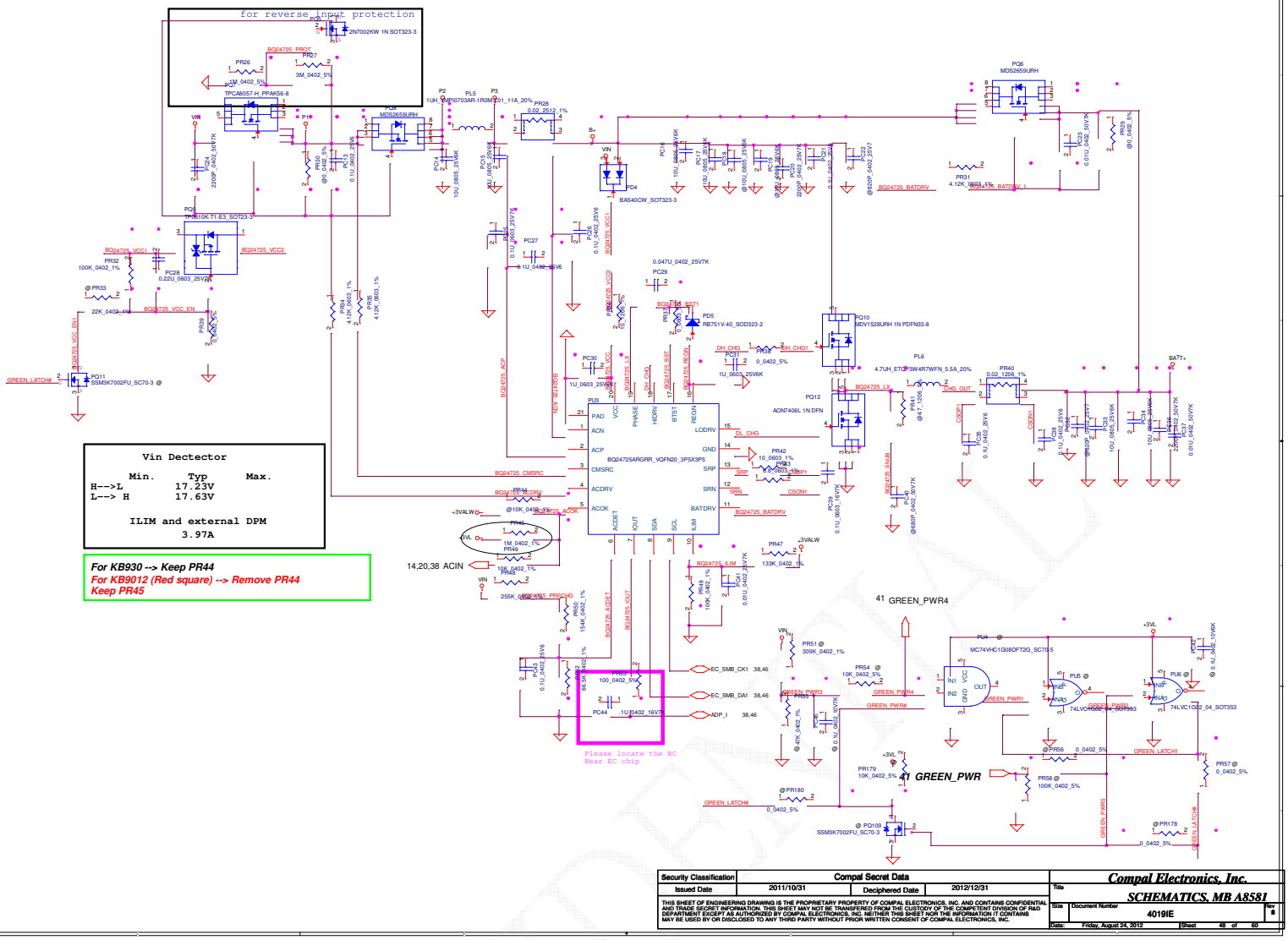
for reverse input protection
Vin Dectector
Min. Typ Max.
H-->L 17.23V
L--> H 17.63V
ILIM and external DPM
3.97A
For KB930 --> Keep PR44
For KB9012 (Red square) --> Remove PR44
Keep PR45
14,20,38 ACIN
41 GREEN_PWR4
41 GREEN_PWR
Please locate the RC Near EC chip
BQ24725ARGRR_VQFN20_3P5X3P5
AON7406L 1N DFN
MDV1528URH 1N PDFN33-8
RB751V-40_SOD323-2
BAS40CW_SOT323-3
SSM3K7002FU_SC70-3
MC74VHC1G08DFT2G_SC70-5
74LVC1G02_04_SOT353
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2012/12/31
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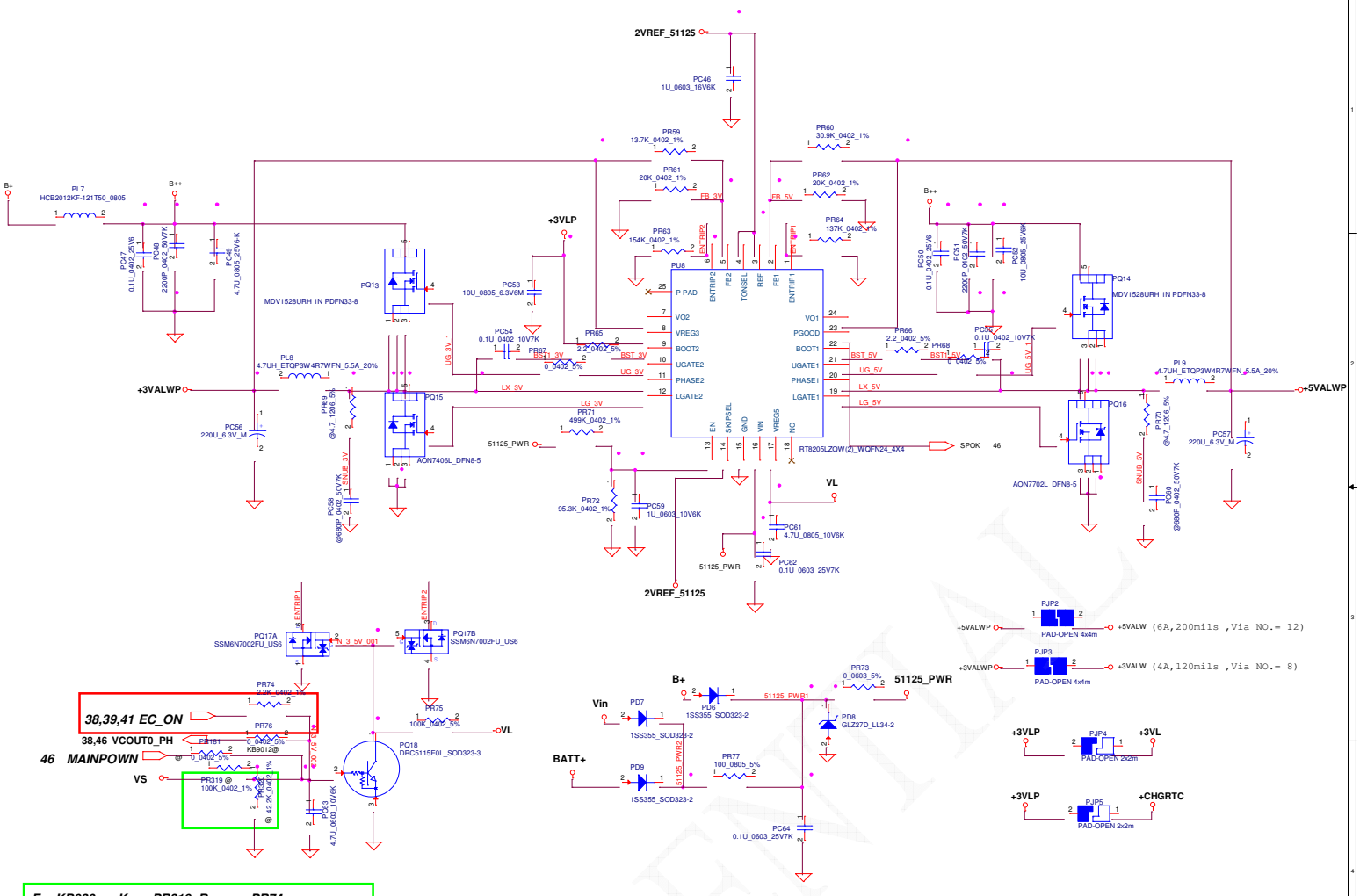

For KB930 --> Keep PR319, Remove PR74
For KB9012 (Red square) --> Remove PR319
Keep PR74

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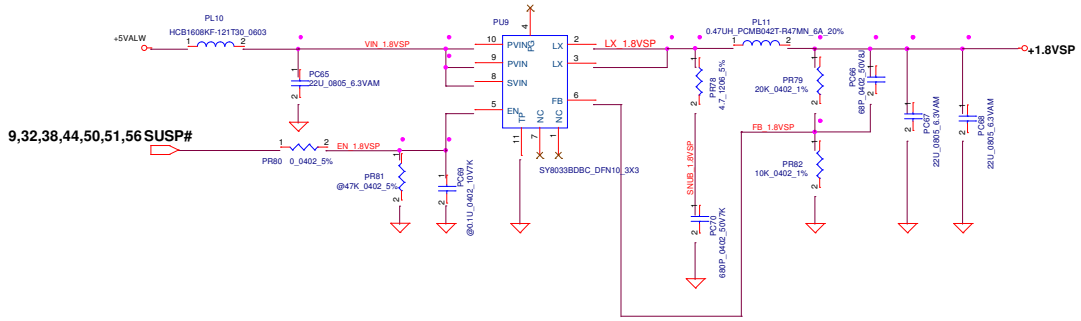

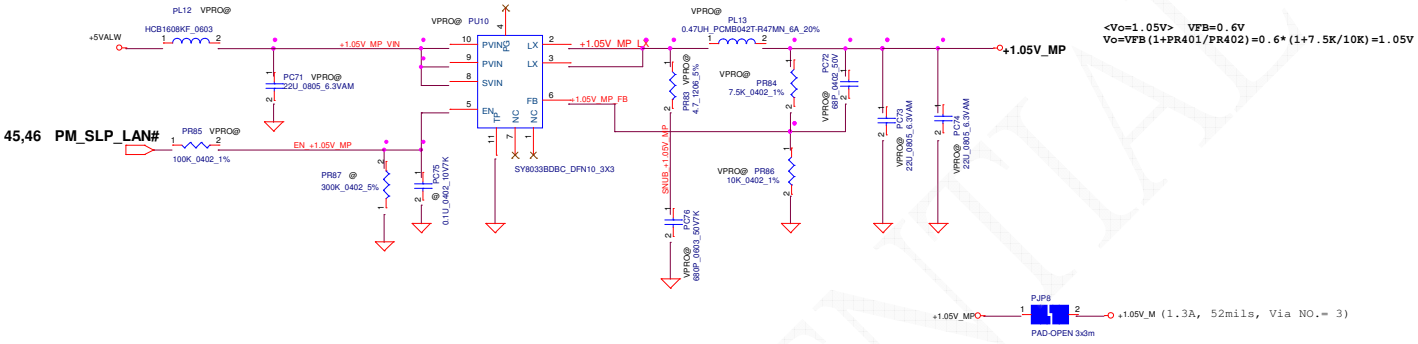

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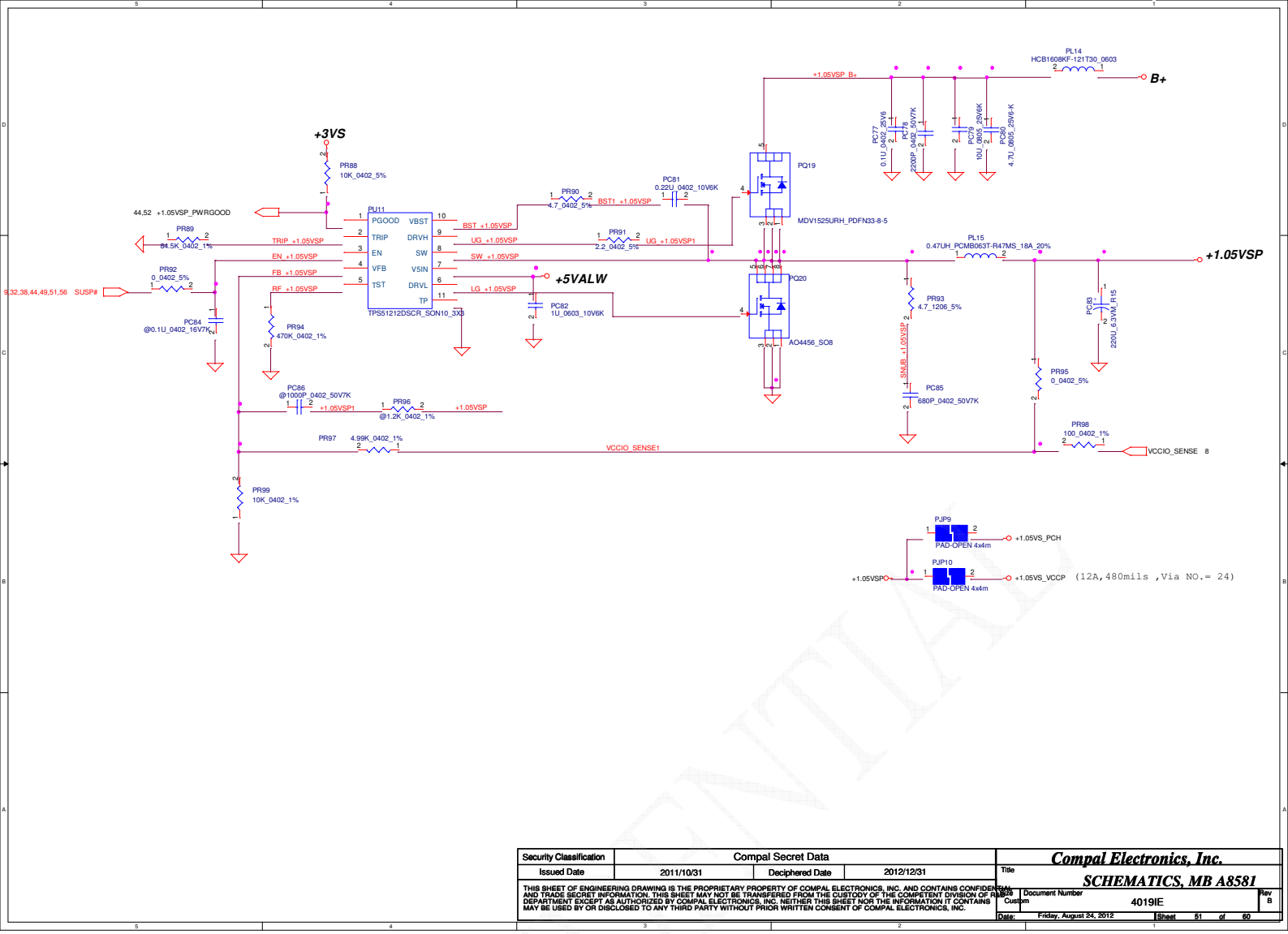

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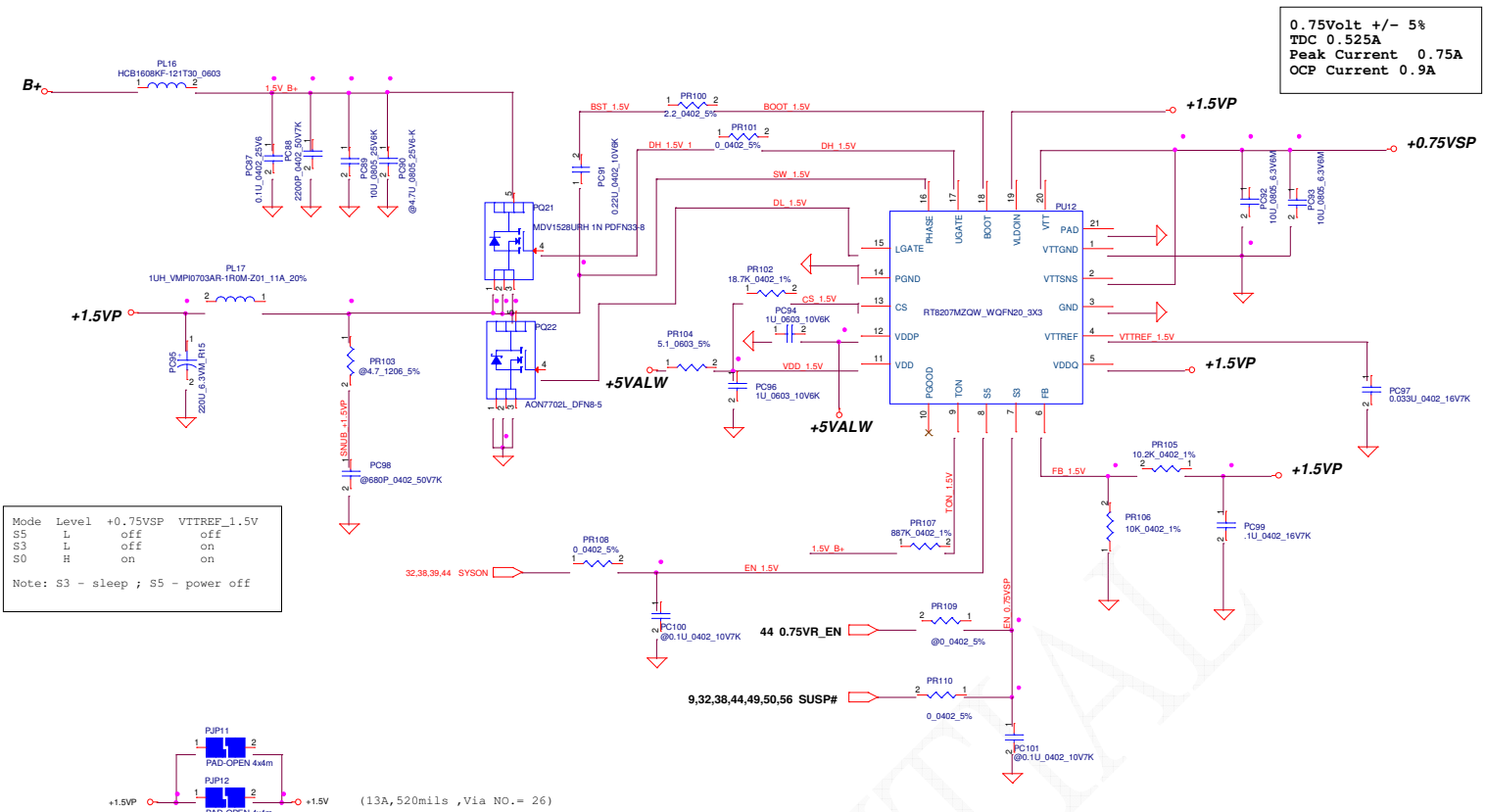

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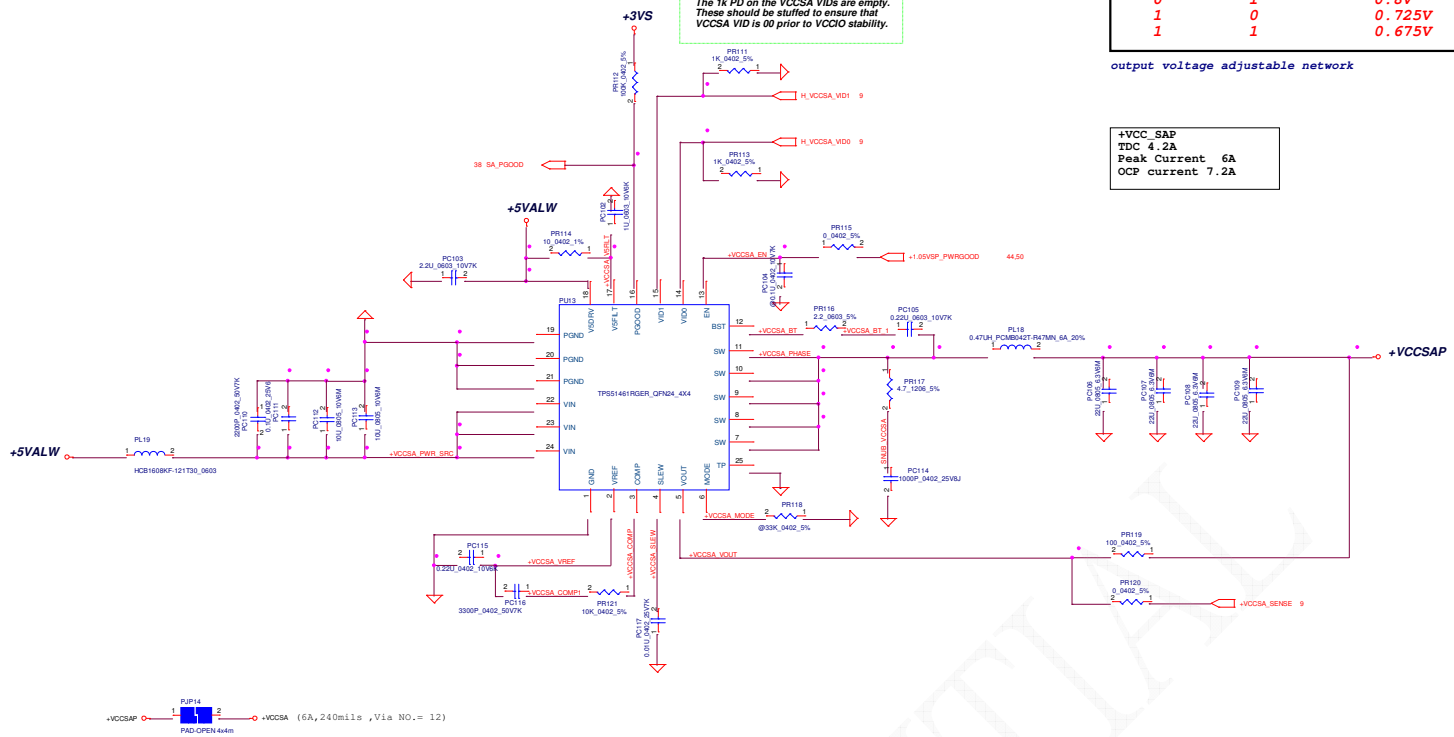
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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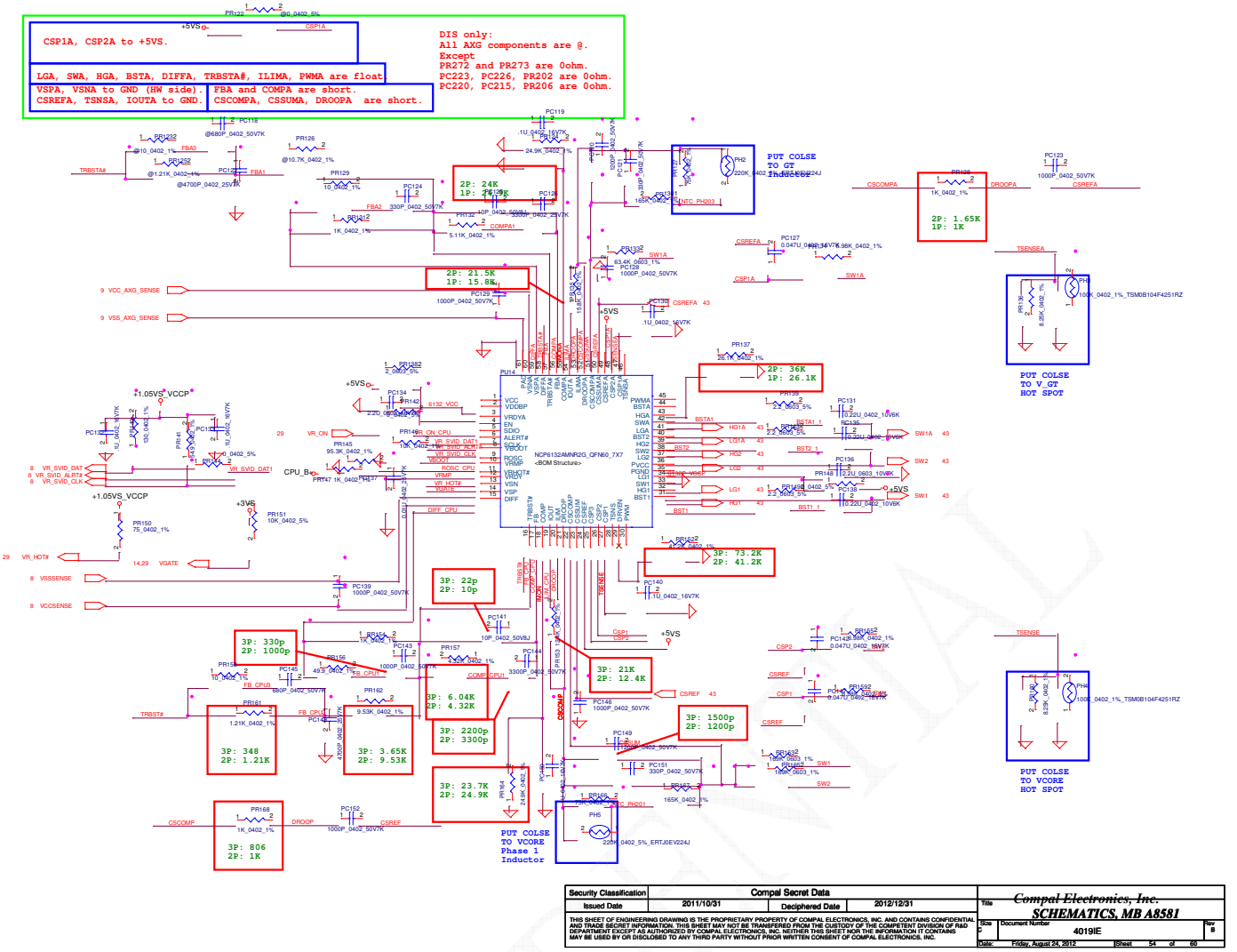

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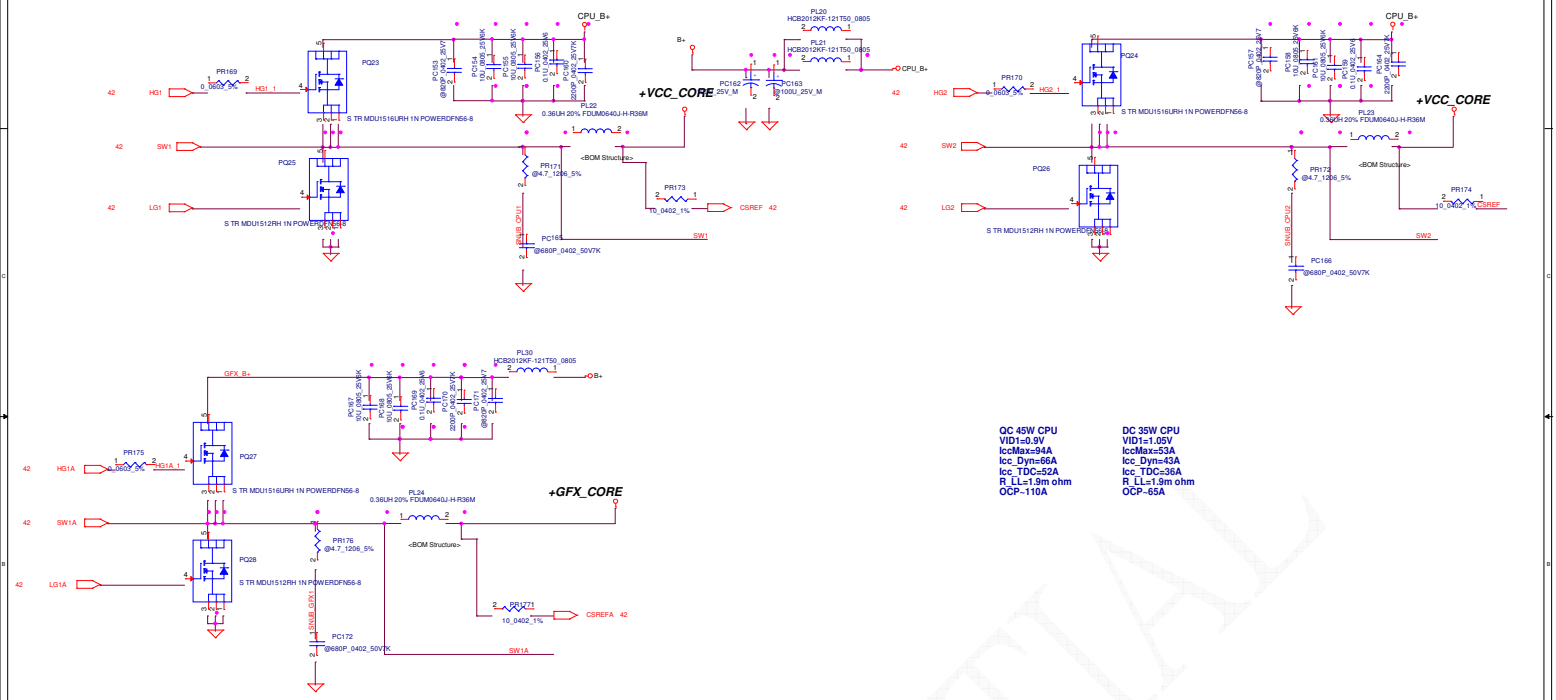

QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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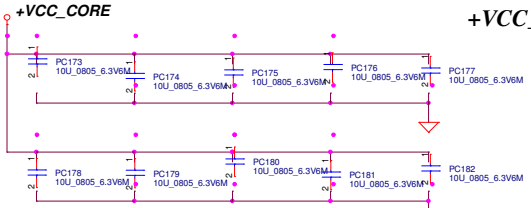
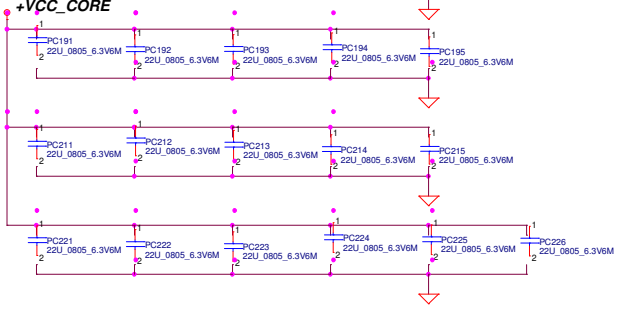
PBL22 LA-7391P M/B

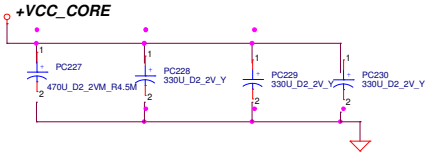
+VCC_CORE



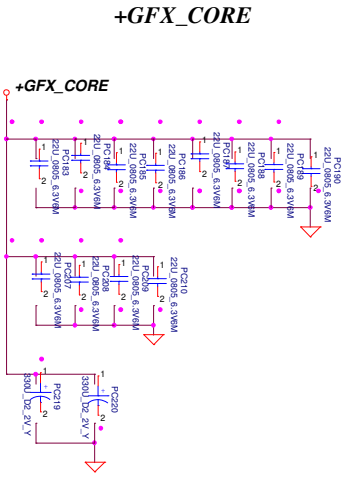
+VCC_CORE



+VCC_CORE



+GFX_CORE

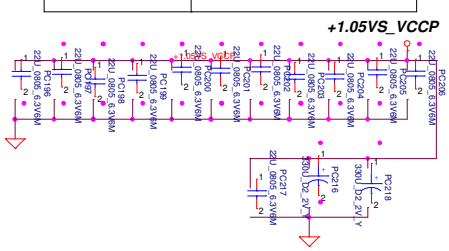


+GFX_CORE

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS_VCCP



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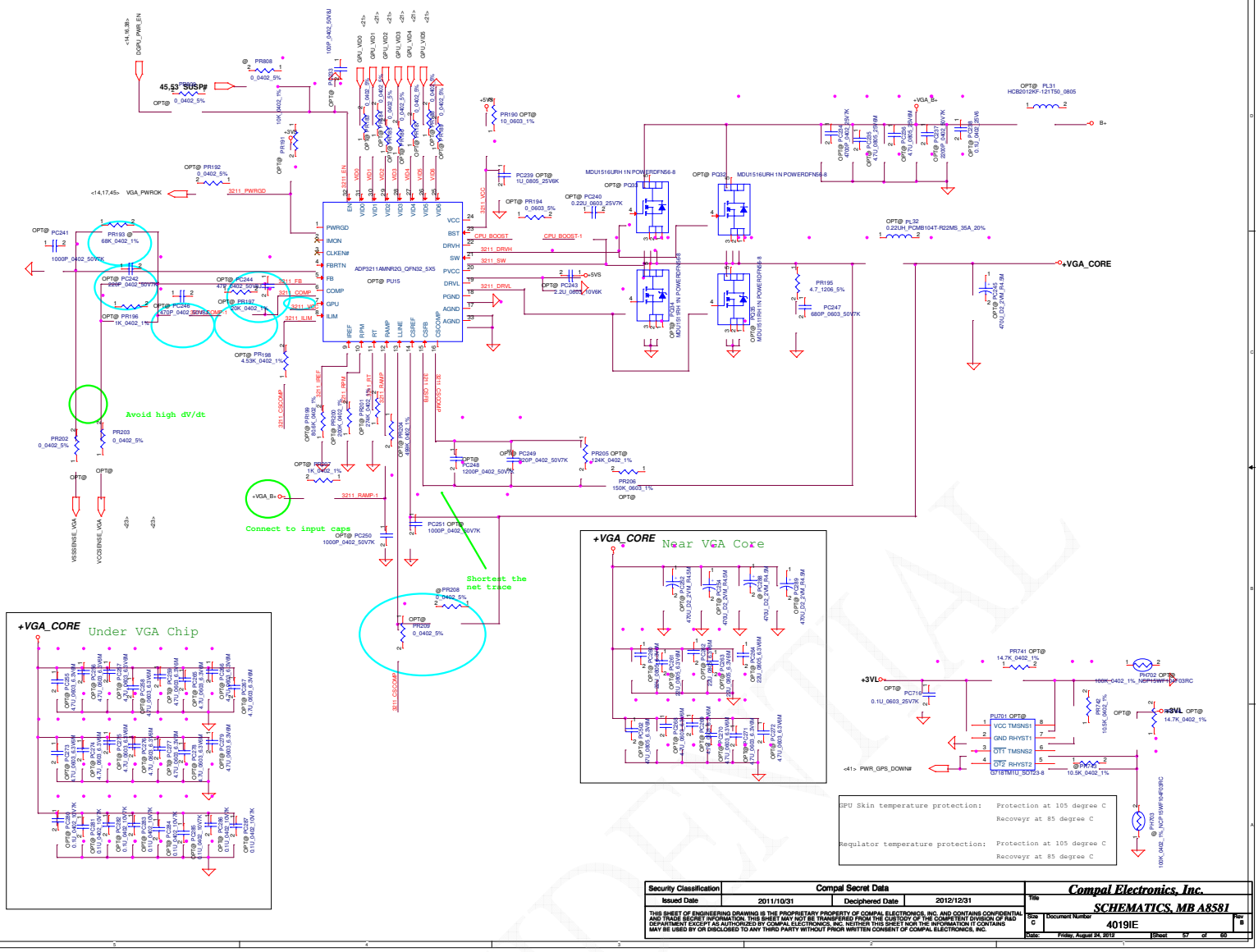

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	Page 47		2012/02/24		For DVT can't power on and need to disable EC VCIN0_PH VCIN1_PH pin detect	Reserve PR20 PR21 for DVT can't power on issue	PVT
2	Page 57		2012/02/24		3D mark06&3D mark Vantage score don't meet SPEC need to support GPS function	Add PC288 PC289 470U_D2_2VM_R4.5M PC248 1200P_0402_50V7K PR209 0_0402_5% Change PC242 to 220P_0402_50V7K PC246 to 470P_0402_50V8J PC244 to 47P_0402_50V8J PR197 to 20K_0402_1% PR198 to 4.53K_0402_1% PC249 to 820P_0402_50V7K PR205 to 124K_0402_1% PR206 to 150K_0603_1% Delete PR208 0_0402_5%	PVT
3	Page 49		2012/02/24		For DVT SMT PC56, PC57 footprint did not match issue	Change PC56,PC57 footprint from D2 to C_6SVPE220MX	PVT
4	Page 57		2012/02/24		3D mark06&3D mark Vantage score don't meet SPEC need to support GPS function	Reserve GPU Skin and Requlator temperature protection circuit for if temperature over spec issue Add PC716 SE042104K80 0.1U_0603_25V7K PR741,PR744 SD034147280 14.7K_0402_1% PR742 SD034105280 10.5K_0402_1% PH702 SL200000U00 100K_0402_1%_NCP15WF104F03RC	PVT
5	Page 47		2012/02/24		Change PH1 protect action to EC	Change PH1 pull high vcc from +3VL to +EC_VACC Change PH1 GND from normal GND to EC_AGND	PVT
6	Page 48		2012/02/27		Update Green power Circuit	Delete PU7 74LVC1G17GW TSSOP and change to PQ109 SSM3K7002FU_SC70-3 Add PR10 0_0402_5% to connect GREEN_LATCH# Reserve PR178 0_0402_5%	PVT
7	Page 48		2012/03/02		Update Green power Circuit	Connect the Green_PWR4 net to EC GPIO for AC decete for Green power circuit ACOK will drop once time issue	PVT
8	Page 47		2012/03/06		Add one control signal in order to disable B+ to VSB circuit in AC S5 for LOT6 system little than 0.5W issue	Reserve PR22 to add VSB_EN	PVT
9	Page 47 49		2012/03/06		For System can power on immediately after HW shutdown	Change PU1.3 output name from EN0 to MAINPOWN Dis-connect EN0 to PU8.13 Connect MAINPOWN to PQ18.2	
10	Page 47		2012/04/23		For EU Erp lot6 fail, need to cut off +VSB when system at S5	Add PR22, delete PR14,PR15	Pre_MP
11	Page 47 48,50,51 52,53,54 57		2012/04/23		Change to new footprint	ChangePR56,PR80,PR92,PR95,PR108,PR110,PR115,PR120,PR142,PR144,PR183, PR184,PR185,PR186,PR187,PR188,PR189,PR192,PR809 footprint from R_0402 to R0402_0ohm	Pre_MP

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QAQ1x HW PIR from EVT to DVT LA-8581P REV:0.1 -> 0.2 <2011.12.05~2012.01.02. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	12/05	Circuit, Layout, BOM	37	Sourcer require to change crystal to small size.	Change X1 from "SJ100009A00" to "SJ10000EV00"
	2	12/21	Circuit, Layout	41	EVT can't power on issue.	Change R739 pull up power source from "+3VALW" to "+3VALW_EC".
	3	12/21	Circuit, Layout	26,35,42,36	Vpro require PCIE port1 can't connect to LAN.	Swap PCH PCIE port1 and port5.
	4	12/21	Circuit, BOM	43	SW7, SW8 part number error.	change SW7,SW8 part number to "SN100005G00"
	5	12/21	BOM	27	just reserve pull up resistor for SLP_LAN#.	Add @ to R282.
	6	12/26	BOM	34	TPM IC FW update from FW3.16 to FW3.19.	Change U37 from "SA00000GG40" to "SA00000GG70".
	7	12/26	Circuit, BOM	33	Add Vpro & non-Vpro WIN8 BIOS ROM power source selection.	Add R421, R422.
	8	01/05	BOM	40, 43	issue: redetect USB HDD when resume from S3.	Add @ to RU27, delete @ to R90; add @ to R9, delete @ to R10.
	9	01/05	BOM	41	Board ID issue	Add "Rev02@", "Rev03@","Rev04@","Rev10@" serial Rb to distinguish the boards.
	10	01/09	Circuit, layout	40	LID_SW# will cause system can't power on at DC mode if use +3VALW, not +3VL.	Change U34 Pin2 VDD from +3VALW to +3VL if EC use +3VL.
	11	01/09	Circuit, layout,BOM	43	PWR ON LED will flash when doing Crisis.	Add a pull down resistor R169 100K to PWR_ON_LED; Reserve a 0ohm resistor R93.
	12	01/09	Circuit, layout,BOM	36	DVT will build Vpro SKU, delete EC port80 debug signals to WLAN connector.	Delete R684, R1336 and the EC port80 debug signals to WLAN connector.
	13	01/09	Circuit, layout,BOM	13,15 24	No need reserve VGA HDMI connection.	Change PCH net "DGPU_HPD_INT#" to PCH_GPIO6; Delete U13,CV197,RV140,RV149,C430,C378,C455,C377,C376,C434,C456,C432,R432,R435,R443,Q65,R439,R437RV132,L88.
	14	01/10	Circuit, layout	37,35,26,42	BIOS prefer LAN connect to PCIE port6 for Vpro.	Swap PCIE port5 and port6 connection.
	15	01/10	BOM	33,	Distinguish with Vpro SKU.	Change UPCH1 and U59 BOM Structure to "8111E@" for non-Vpro SKUs.
	16	01/11	Circuit, layout	43	+USB_VCCE no bulk capacitor.	Change C2,C7,C8 power source from +USB_VCCB to +USB_VCCE.
	17	01/11	Circuit, layout	41	power CPU OTP issue, and power modified schematic.	Delete net EC pin27 "PWR_GPS_DOWN#" and EC pin 76 "PWRMOS_TEMP", delete R732.

QAQ1x HW PIR from DVT to PVT LA-8581P REV:0.2 -> 0.3 <2012.02.24~2012.03.07. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	1	02/24	Circuit, BOM	35	LL1 and CL13 change after EVT, DVT schematic missed and used MEMO for change.	Change LL1 from 4.7uH "SHI00004T00" to 2.2uH "SHI0000AA00". CL13 from 22uF "SE000000I10" to 4.7uF "SE107475K80".
	2	02/24	BOM	37	DVT board card reader JMB389 can't detect 4IN1 card.	Delete R39 BOM structure "388@".
	3	02/24	BOM	27	HDMI HPD signal level is too low for HDMI detection.	Add "@" to RH142.
	4 5	02/24	Circuit, layout,BOM	41,13	PVT add GPU GPS feature.	Add R266 "@", R267 "@", R268 at Page13, add "@" to DV6. Change net ACIN_BUF to GPS_DOWN#, add net PWR_GPS_DOWN#, EC_GPS_DOWN#, PWRMOS_TEMP.
	6	02/24	Circuit, layout,BOM	28	requirement from Sourcer and buyer.	Change RP1, RP3 from row resistor "SD309820180" to single ones "SD028820180"-R320,R321,R322,R323,R324,R327,R329,R330.
	7	02/24	BOM	35	UL5 BOM structure error with vPro SKU.	Delete UL5 BOM structure "8111E@".
	8	03/01	Circuit, layout,BOM	35	LAN vendor Realtek suggest:Reserve CLKREQ_LAN# pull up 10Kohm to +3V_LAN.	Reserve CLKREQ_LAN# pull up 10Kohm to +3V_LAN: add RL25 and unmount it.
	9	03/01	BOM	35	LAN vendor Realtek suggest:Reserve UL1 pin28 "EC_SWI#"pull up 10Kohm to +3V_LAN.	Modify reserved resistor RL3 from 100Kohm to 10Kohm.
	10	03/01	Circuit, layout,BOM	35	LAN vendor Realtek suggest: 6pcs decoupling capacitor for UL1 Pin 12, 27, 39, 42, 47, 48.	Add one more piece capacitor CL12 close to UL1.
	11	03/01	Circuit, layout,BOM	41	Reserve and add pull up for added net of EC pin27,68.	Reserve R732 10Kohm and add R733 100Kohm pull up to +3VS for EC pin27,68, add R734 0ohm for PWR_GPS_DOWN# connect to EC.
	12	03/01	Circuit, layout,BOM	13	Reserve a 0ohm resistor for "GPS_DOWN#" to "PWR_GPS_DOWN#".	Reserve a 0ohm resistor R270 for "GPS_DOWN#" to "PWR_GPS_DOWN#".
	13	03/02	Circuit, layout	41	power circuit removed net "PWR_MOS_TEMP", added net "GREEN_PWR4".	Remove net "PWR_MOS_TEMP", add net "GREEN_PWR4" to EC pin 76.
	14	03/05	BOM	26 35 37,34 13	Adjust crystal loading capacitors' value according to matching test result.	Change Y3 from SJ10000DJ00 to SJ10000E800, C869 from SE071150J80 to SE071100J80, C225 from SE071120J80 to SE071100J80. Change YL1 from SJ10000DJ00 to SJ10000E800, CL26 and CL27 from SE071270J80 to SE071120J80. Change C54 and C82 from SE071120J80 to SE071150J80; C766,C767 from SE071150J80 to SE071180J80. Change YV1 from SJ10000DK00 to SJ100009700, CV46 and CV47 from SE071180J80 to SE071100J80.
	15	03/05	Circuit, layout,BOM	39	Refer to QAL50/51 design for smart card to add pull high to US4 pin26.	Add RS22 10Kohm pull up to +3V_SC for US4 Pin26. and change reserved pull down resistor RS21 from 0ohm to 10Kohm.

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QAQ1x HW PIR from DVT to PVT LA-8581P REV:0.2 -> 0.3 <2012.02.24~2012.03.07. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	16	03/05	Circuit, BOM	28,39	smart card device lost at USB 3.0 port.	Change smart card reader from USB port 2 to port 5.
	17	03/06	BOM	31	PCH VCCDSW3_3 change power connection from +3VALW_PCH to +3VALW.	Add "@" to R415, delete "@" to R382.
	18	03/06	Circuit, layout, BOM	35,36, 39,29 41,45	ErP lot 6 fail, reserve a EC pin VSB_EN to control VSB; reserve LAN WAKE to EC and PCH GPIO27.	Delete reserved net AOAC_ON (EC pin 38) and DRAMRST_GATE (EC pin 98) and their test point T23,T24. Use these two pins for new added net VSB_EN_R and EC_PME# Reserve net GPIO27_WAKE#, EC_PME# for LAN WAKE, reserve net EC_PME# to WLAN, WWAN and PCIE Express card wake. thus, add R702@, RH122@, RH171, R331@, RL8(8111E@),RL9@, RL10@, R100@, R102, R761@, R767@,R768@. Reserve net VSB_EN, thus add R765@, R766, R817, R818@, R819@; delete R816@, add @ to R754.
	19	03/06	Circuit, layout, BOM	25	Reserve big size crystal Y6 for 32.768KHz.	Reserve big size crystal Y6 for 32.768KHz.
	20	03/08	BOM	40,43	UU1 SA000047500 was forbidden, change material requirement from buyer.	Change UU1 from SA000047500 to SA000033H00; Correct U6 description and value.
	21	03/08	BOM	43,44	Change C4,C6 from SE053475Z05 to normal part SE053475Z80.	Change C4,C6 from SE053475Z05 to normal part SE053475Z80.

QAQ1x HW PIR from PVT to Pre-MP LA-8581P REV:0.3 -> 1.0 <2012.04.18~2012.04.25. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
1.0	1	04/19	Circuit, BOM,layout	25	Reserve +5VS for MOS Q10 gate of audio sync signal to PCH HDA sync signal.	Add 0ohm 0402 resistor R189@ and R190.
	2	04/19	BOM	25,34	Change 32.768KHz crystal P/N, and RTC capacitor C204 from 15pF to 18pF.	Change Y2, X3 from SJ10000BM00 to SJ100001K00. change C204 from SE071150J80 to SE071180J80.
	3	04/19	BOM	39	to solve issue of "Smart Card also show in Device Manager after plug out it".	Change US4 from SA000042I00 to SA000042I10.
	4	04/19	Circuit,layout	45	Reserve 820Kohm resistor to GND for +3VALW_PCH and +1.05VS_DGPU DC/DC MOS GATE.	Add 820Kohm R432@ and R435@.
	5	04/19	BOM	45,41	For ErP lot6, add +3VALW to +3VALW_PCH DC/DC circuit.	Delete @ for U25, Q46, Q49, R813, C837, C839, C838, R804, C836, R807, R754.
	6	04/20	BOM,layout		cost down: change some 0ohm resistors to short pad.	cost down: change some 0ohm resistors to short pad.
	7	04/23	BOM	42	vPro: Intel suggest to change R1232 from 2.2K to 10K.	vPro: change R1232@ from 2.2K to 10K.
	8	04/23	BOM	42	vPro: Intel suggest to change C470 from 10uF to 22uF.	vPro: change C470 from 10uF to 22uF.
	9	04/23	BOM	35	vPro: Intel suggest to change CL34 from 0.1uF to 1uF.	vPro: change CL34 from 0.1uF to 1uF. keep CL34 0.1uF for 8111E LAN.
		04/23	Circuit, BOM,layout	42	vPro: Reserve LAN WAKE to EC.	vPro reserve R559@ 0ohm for LAN WAKE connect to EC.
		04/25	Circuit,layout	35	There is not enough space for LAN GND ESD diodes. EMI test OK without the two ESD diodes.	Remove DL3@, DL4@.

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