

# Compal Confidential

## QAQ10/11

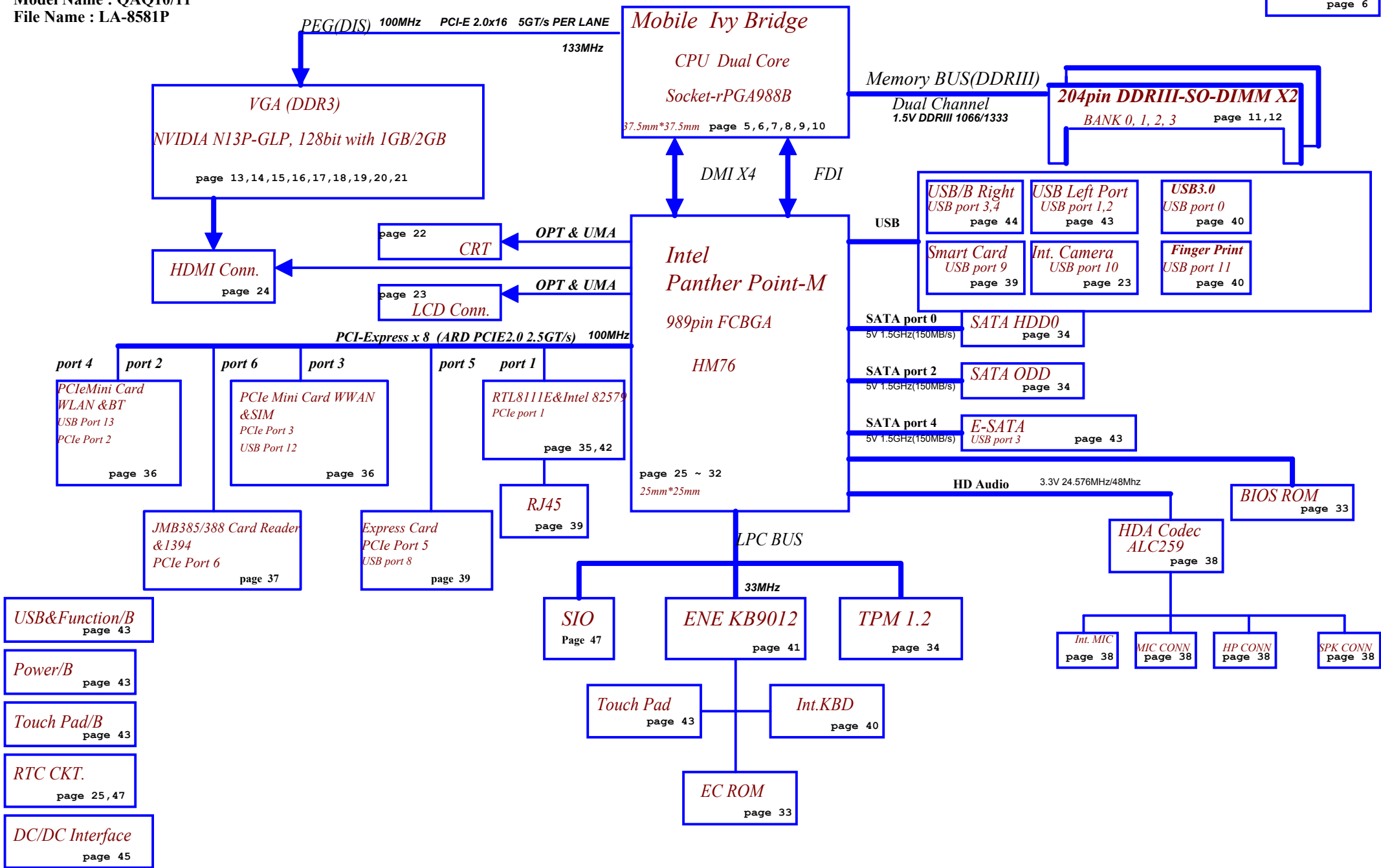
### LA-8581P REV0.1 Schematic

Intel Ivy Bridge/Pather Point

UMA&OPT

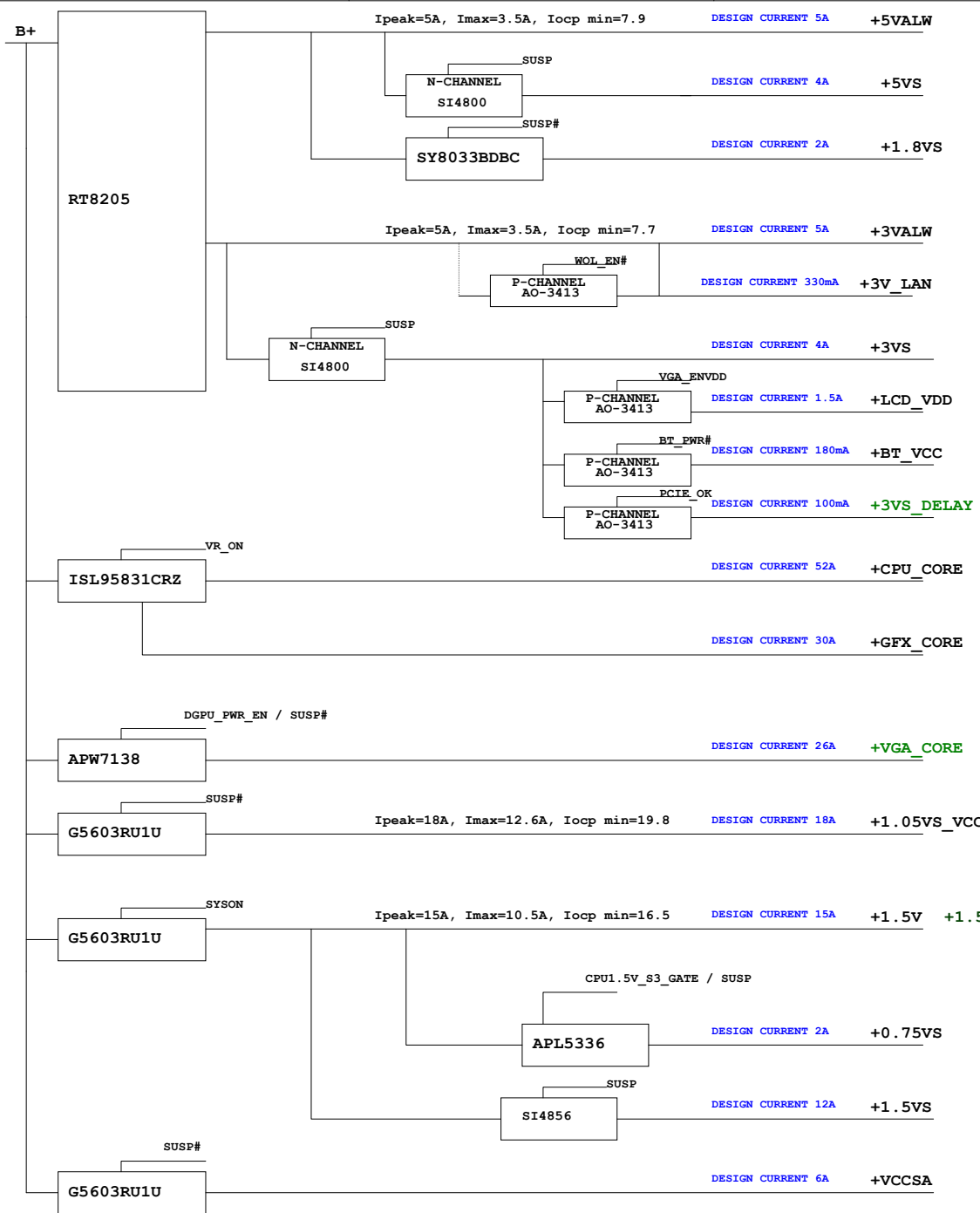
2011-09-28 Rev 0.1

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- Touch Pad/B page 43
- RTC CKT. page 25,47
- DC/DC Interface page 45
- Power Circuit DC/DC page 51, 52, 53, 54, 55, 56, 57, 58, 59, 60

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGF_X_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## EC SM Bus1 address

## EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB930		+3VS	EC KB930	
+3VL	Smart Battery	0001 011x b	+3VS	GPU Thermal Sensor	
			+3VALW	PCH	

## PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1-WLAN	

## BOM configu table

SKU	Description	Bom config	
1	QAQ00 UMA GIGA W/HDMI	DA8@/8111E@/PCH@/UMA@/385@/IN_TPM@ TPM@/SM@/USB30@	4619F230L01
2	QAQ01 DIS DU N12GE2G W/HDMI	DA8@/8111E@/PCH@/OPT@/388@/USB20@/12GE@	4619F230L11
3	QAQ02 UMA VPRO W/HDMI	DA8@/VPRO@/385@/USB20@/TPM@/IN_TPM@/SM@	4619F230L21
4			
5			
6			
7			
8			

DA8@/8111E@/PCH@/UMA@/385@/IN\_TPM@/TPM@/SM@/USB30@/OPT@/388@/USB20@/VPRO@/WB\_TPM@

## X76 AND VGA configu table

SKU	Description	Config	
1	4619F230L11	ZZZ SAM1G8@ SAM 1G	ZZZ HY1G8@ Hynix 1G
2		ZZZ SAM1G8@ SAM 1G	ZZZ HY1G8@ Hynix 1G
3		ZZZ SAM2G@ SAM 2G	ZZZ HY2G@ Hynix 2G
4			
5			
6			
7			

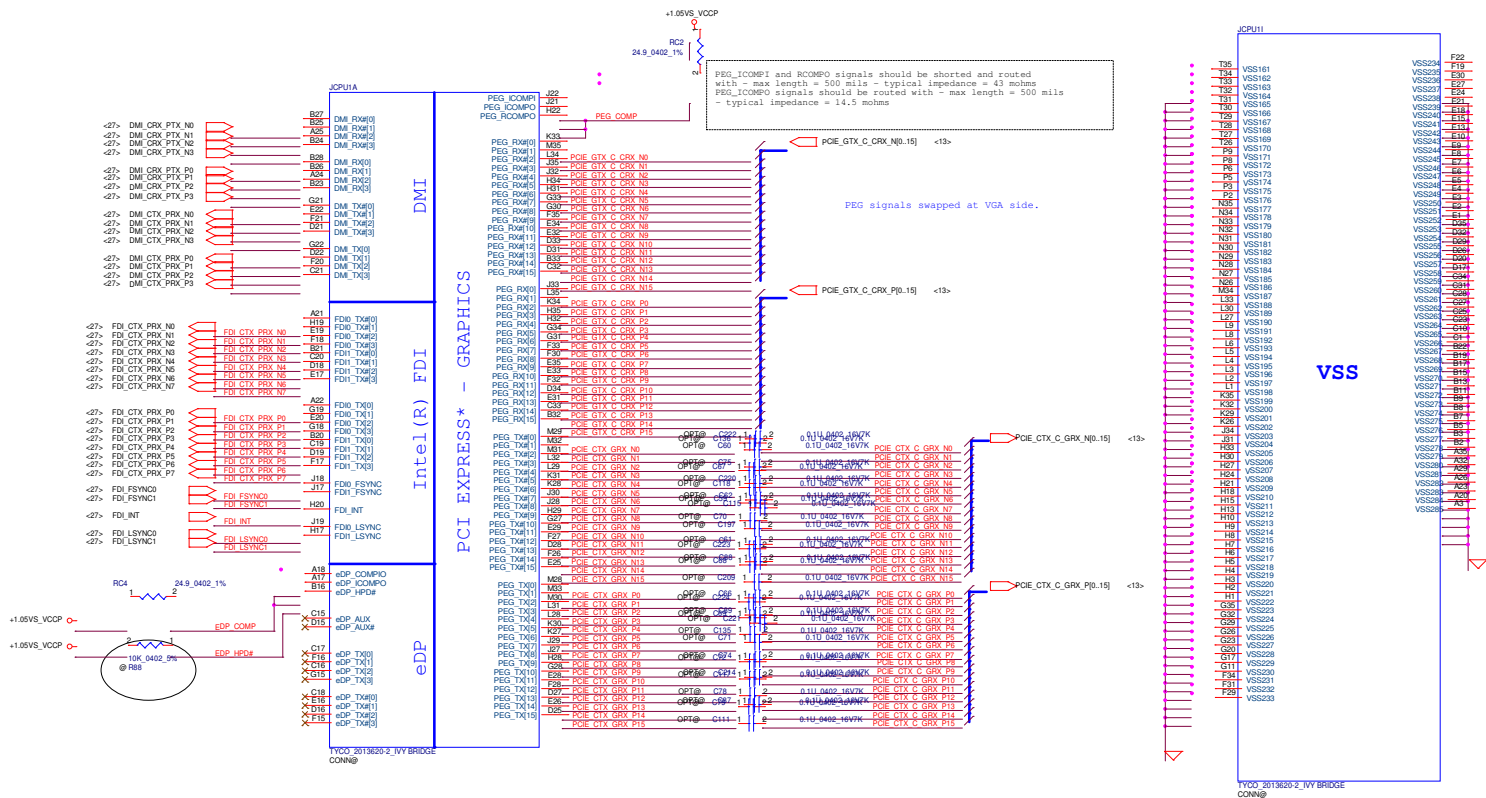
## Board ID Table

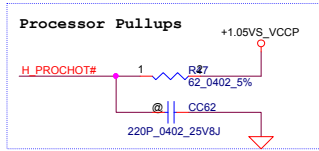
Board ID	Rb / Rd / Rf	Ra/Rc/Re	VCC	V min	Vtyp	Vmax	PCB Revision
0	0	100K +/- 5%	3.3V +/- 5%	0V	0V	0V	0.1
1	8.2K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.436 V	0.503 V	0.538 V	0.3
3	33K +/- 5%	100K +/- 5%	3.3V +/- 5%	0.712 V	0.819 V	0.875 V	0.4
4	56K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.036 V	1.185 V	1.264 V	1.0
5	100K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.453 V	1.650 V	1.759 V	0PRO
6	200K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	100K +/- 5%	3.3V +/- 5%	2.500 V	3.300 V	3.300 V	

## PCH And PCBA table

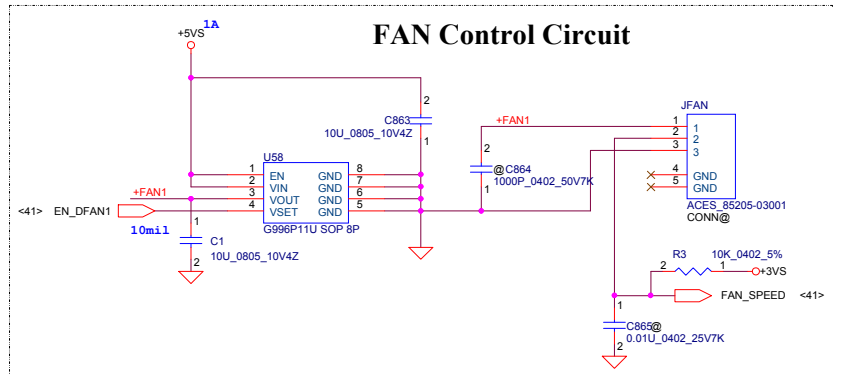
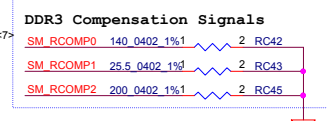
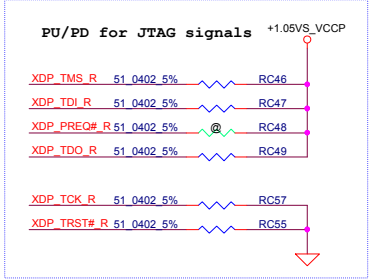
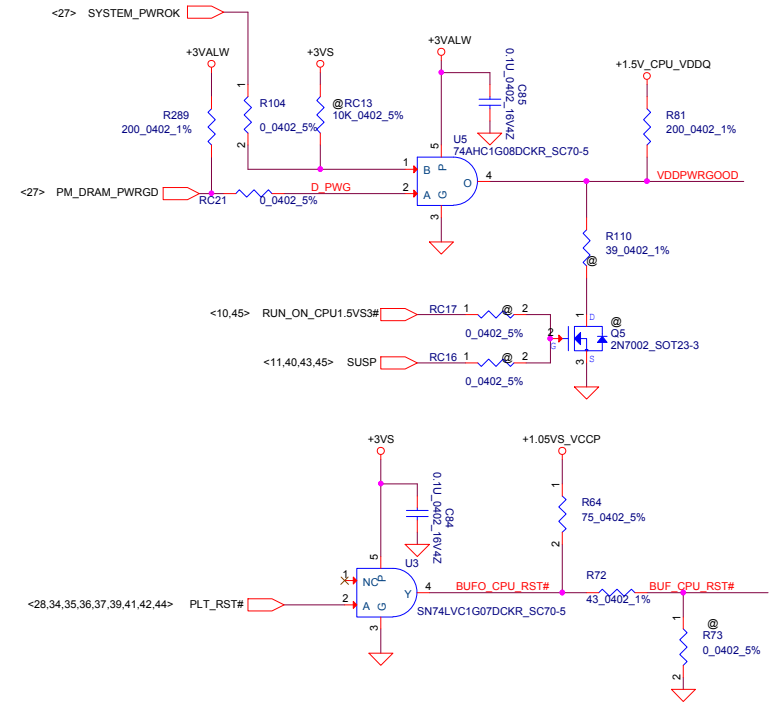
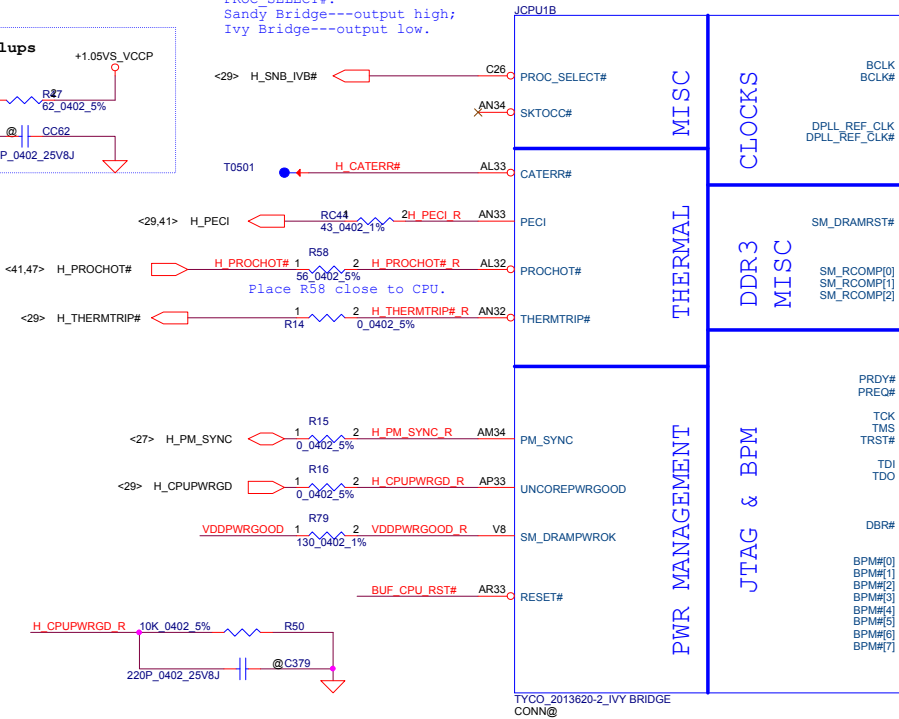
PCH	UPCH1 BD82HM65 SLH9D B2 FCBGA 989P PCH PCH@	UPCH1 BD82QM67 SLJ4M B3 FCBGA 989P PCH VPRO@
PCB		ZZZ DA8@ PCB LA-7661P REV01

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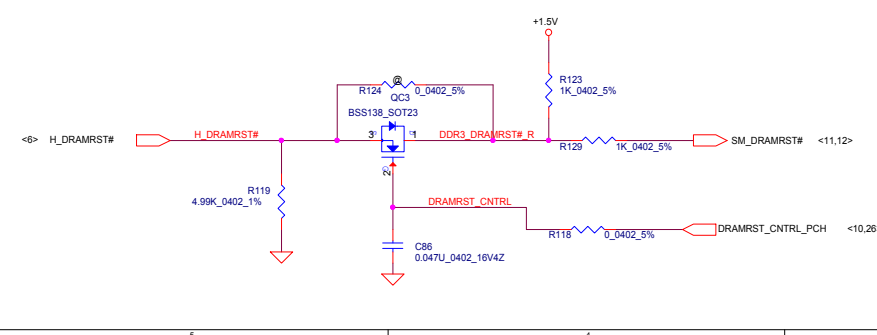
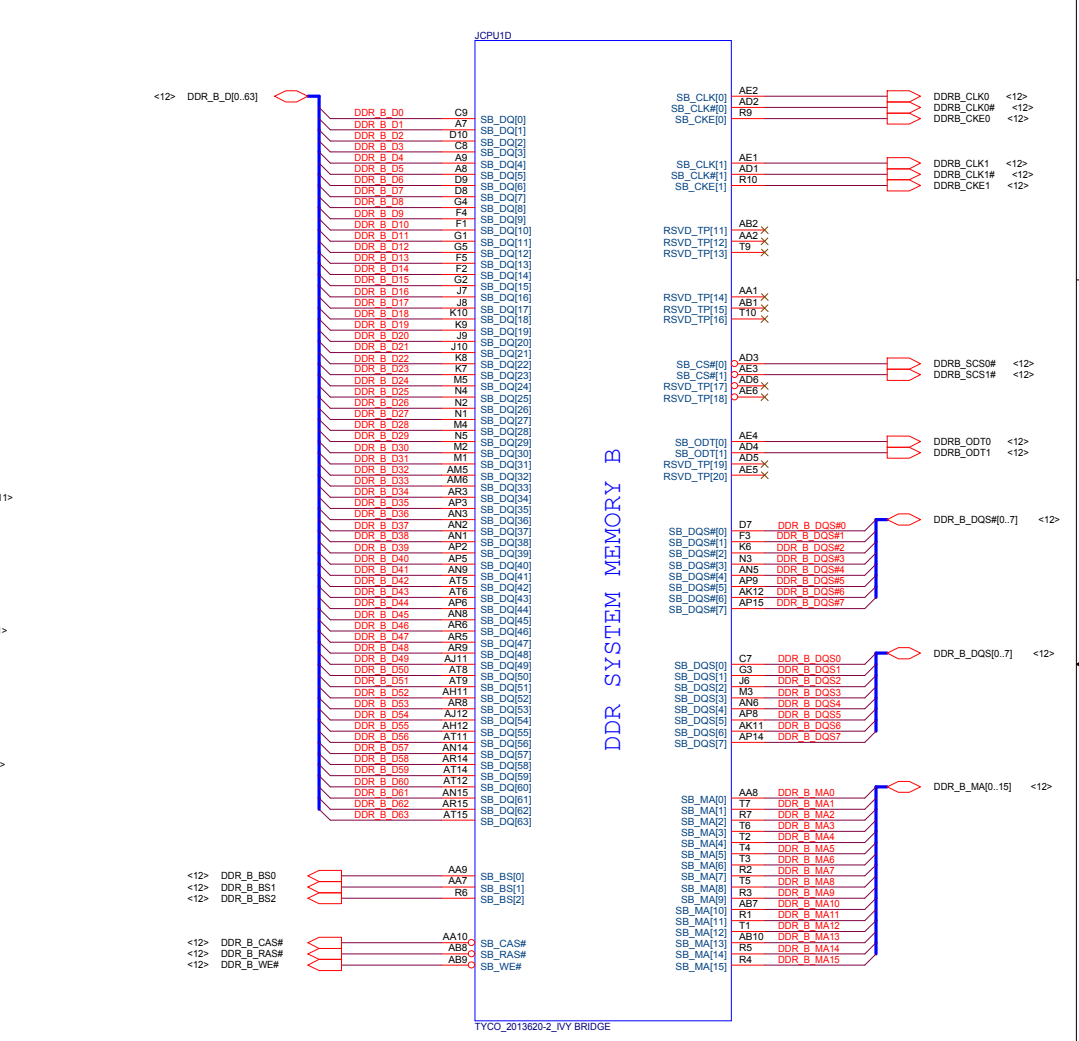
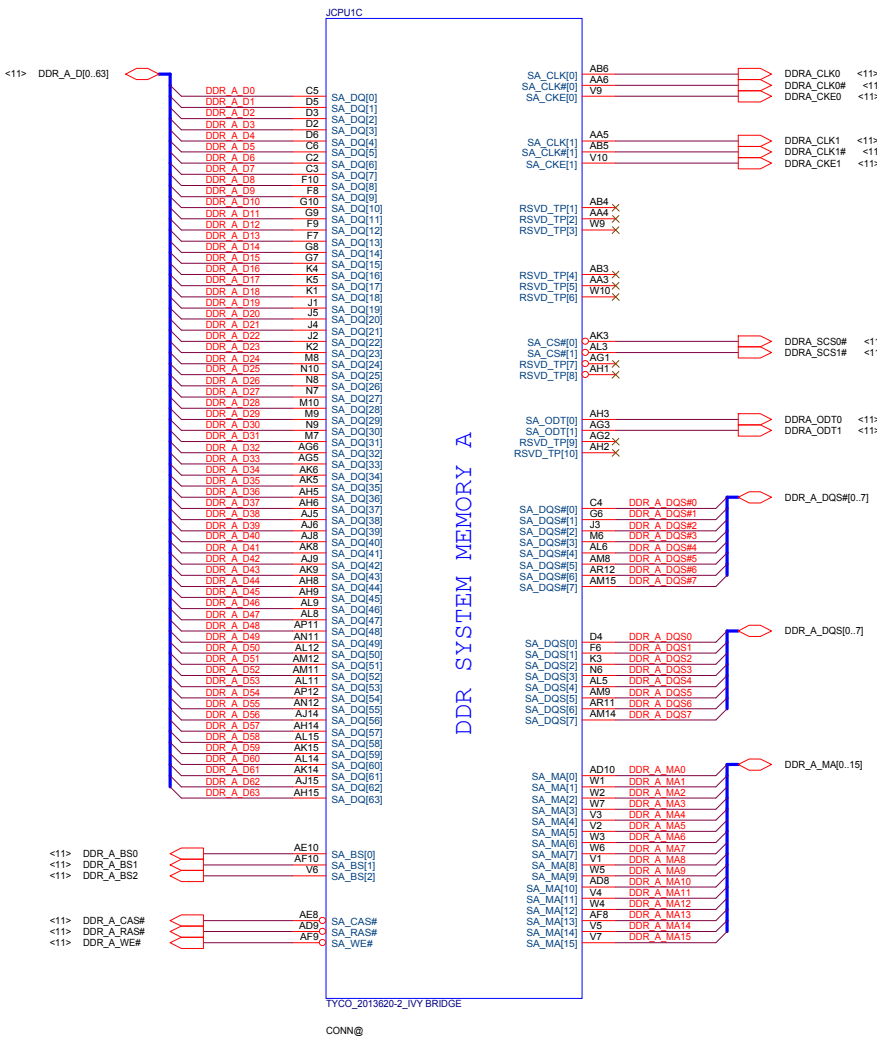




PROC\_SELECT#:  
Sandy Bridge---output high;  
Ivy Bridge---output low.

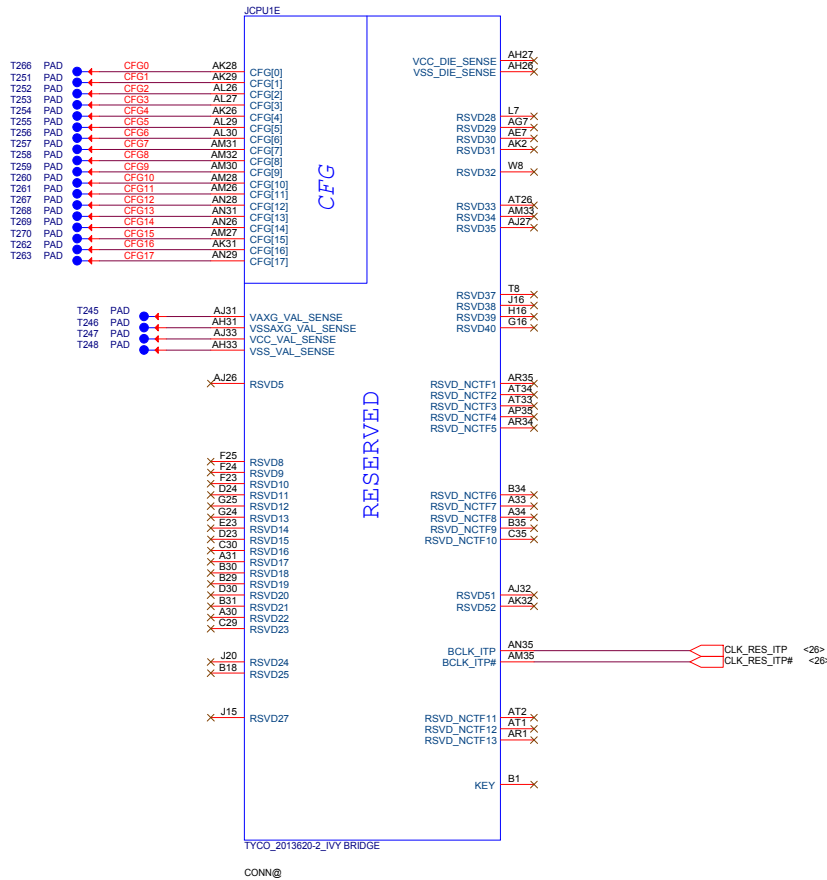


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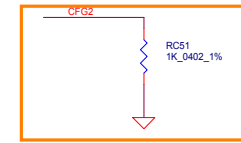


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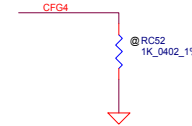
CFG[1:0]: reserved configuration lane.  
 CFG[3]: reserved  
 CFG[17:7]: reserved configuration lanes.  
 CFG[17:0]: Processor internal pull up 5-15Kohm to VCCIO



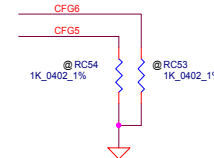
### CFG Straps for Processor



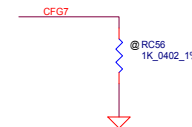
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

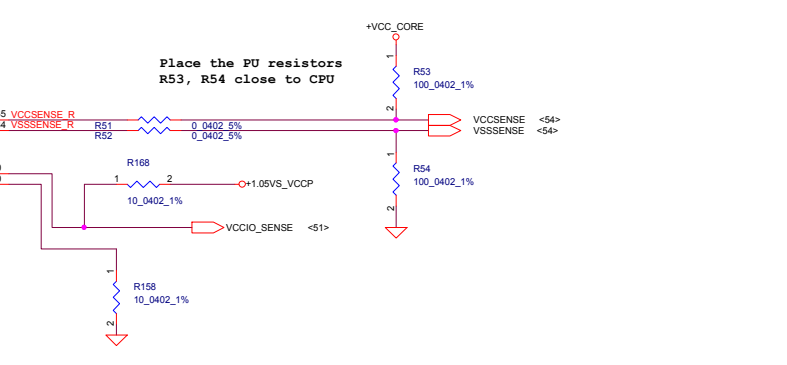
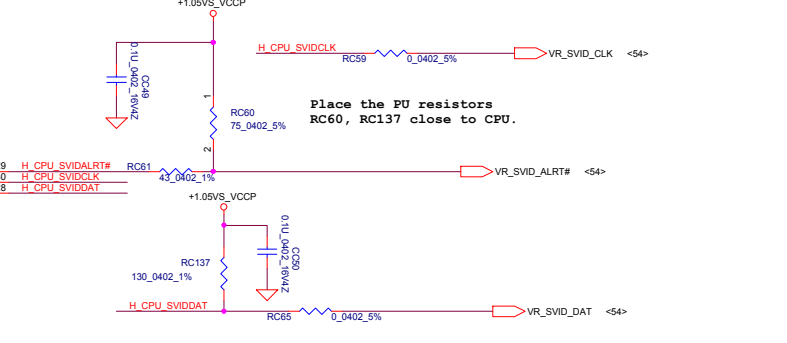
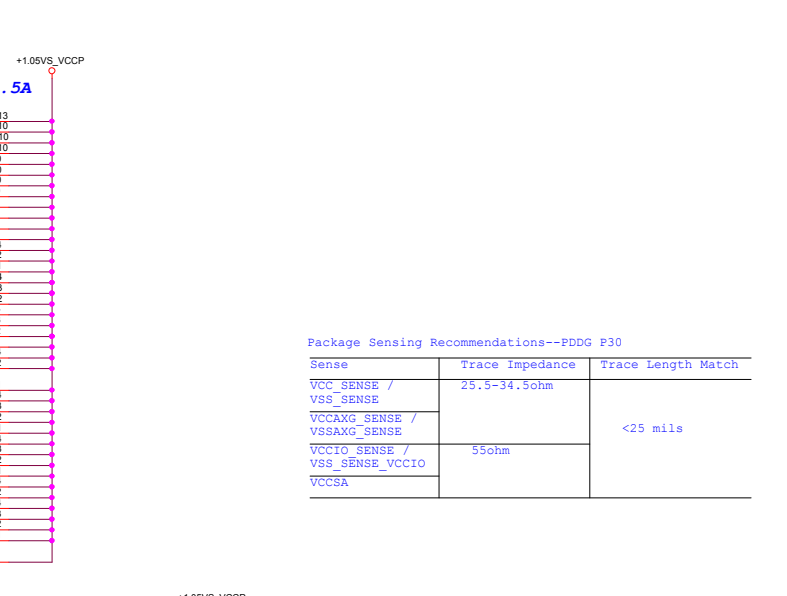
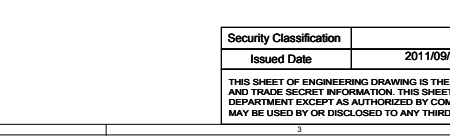
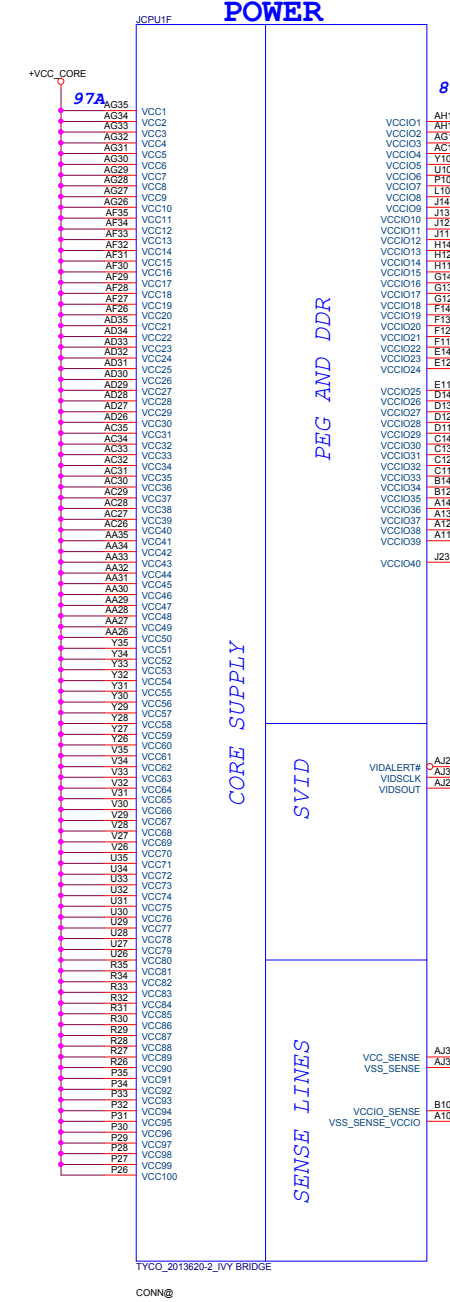
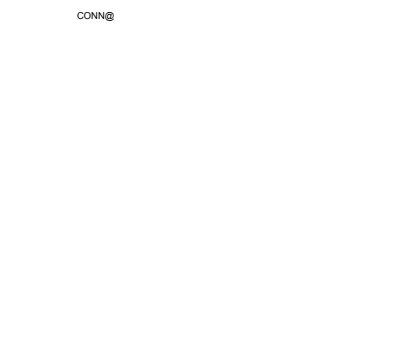
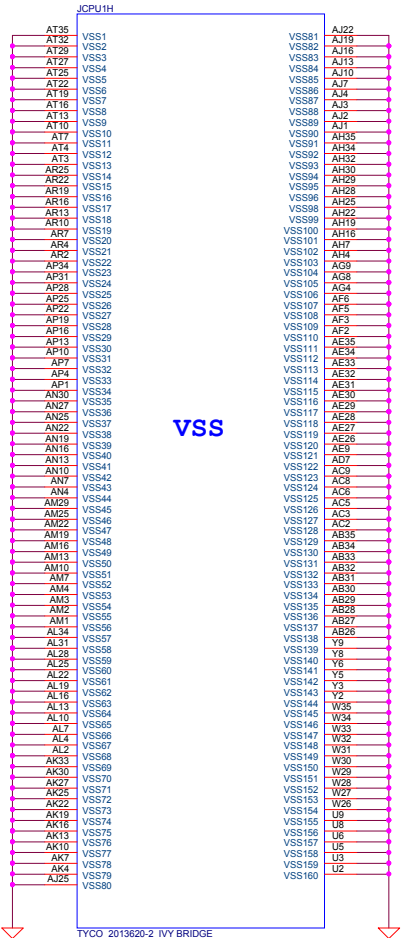


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training





Package Sensing Recommendations--PDDG P30

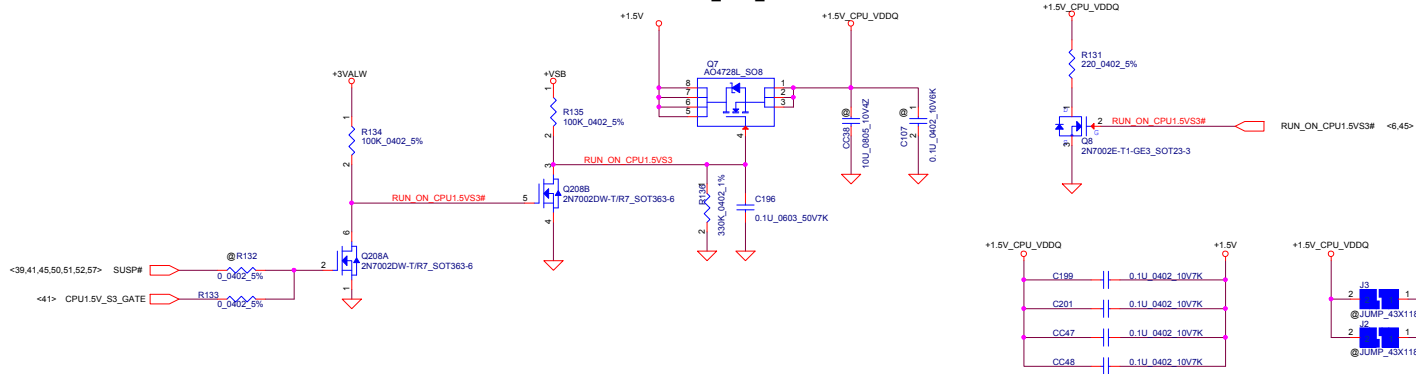
Sense	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	25.5-34.5ohm	<25 mils
VCCXG_SENSE / VSSXG_SENSE		
VCCIO_SENSE / VSS_SENSE_VCCIO	55ohm	
VCCSA		

Place the PU resistors RC60, RC137 close to CPU.

Place the PU resistors R53, R54 close to CPU

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**+1.5V\_CPU\_VDDQ**



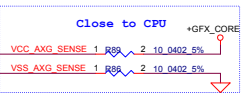
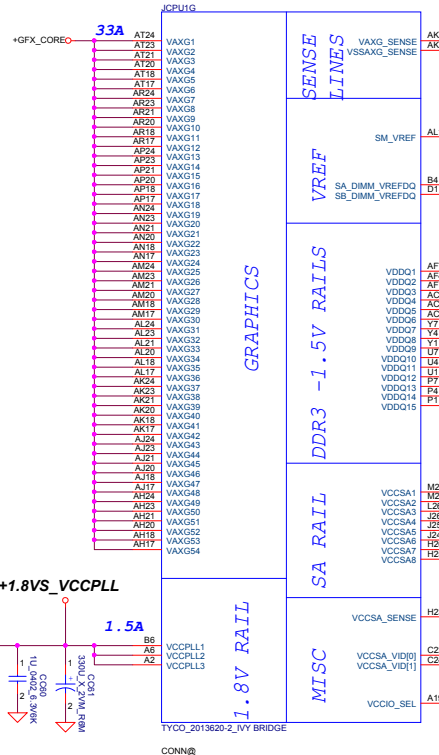
**POWER**

**GRAPHICS**

**DDR3 - 1.5V RAILS**

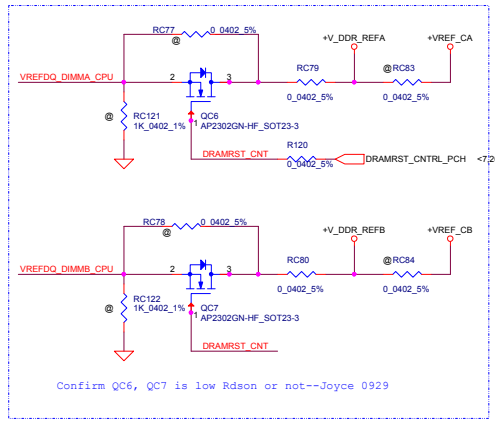
**SA RAIL**

**MISC**



+V\_SM\_VREF should have 20 mil trace width

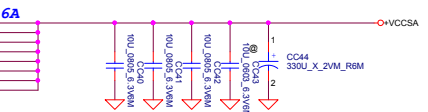
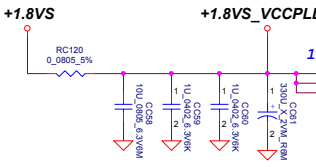
Intel future processor compatibility design. --DG1.5 P113



Confirm Q6, Q7 is low Rds(on) or not--Joyce 0929

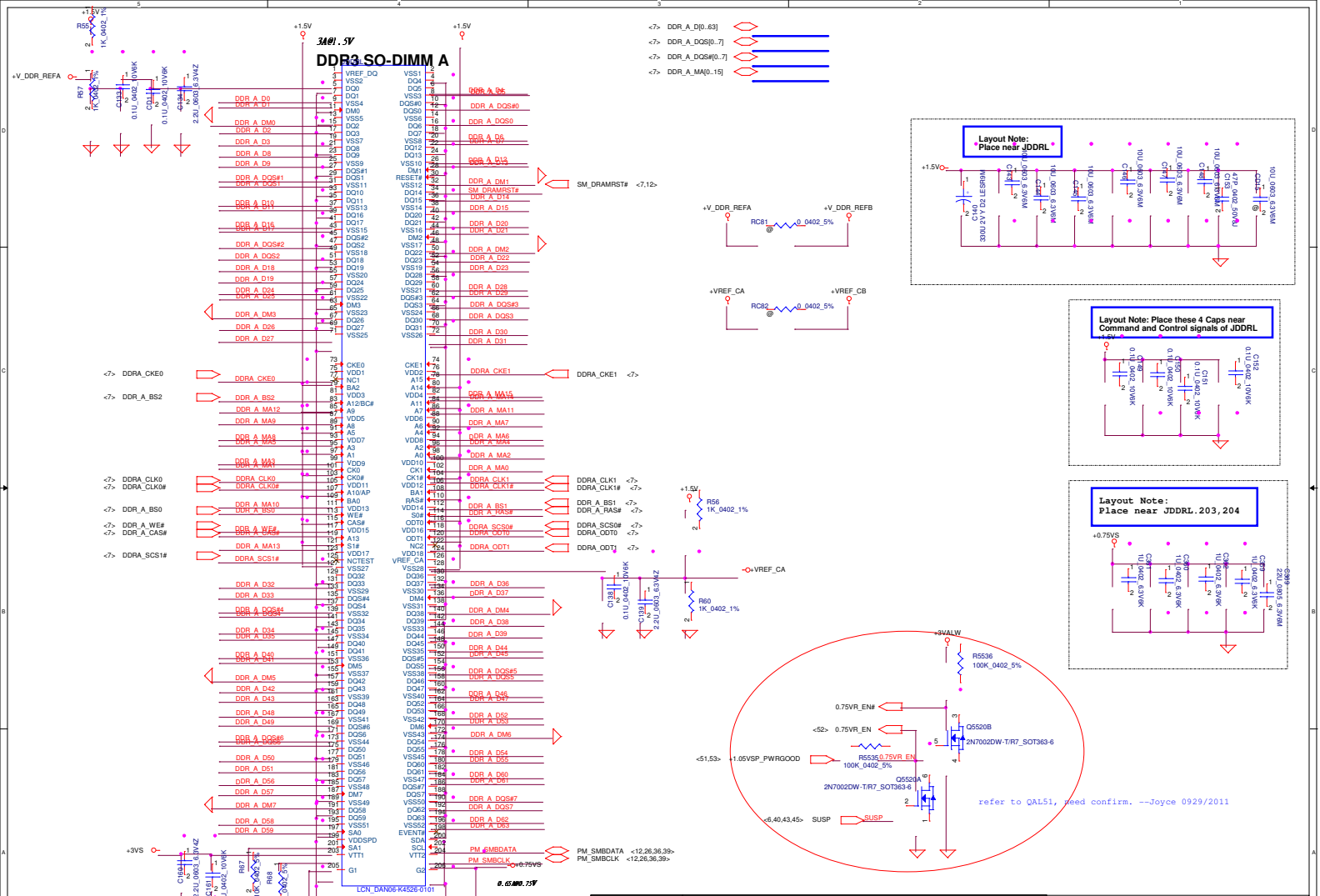
VCCSA: 0.675V (Min) ~ 0.9V (Max)

SA: System Agent (Memory controller, DMI, PCIe controllers, and display engine)

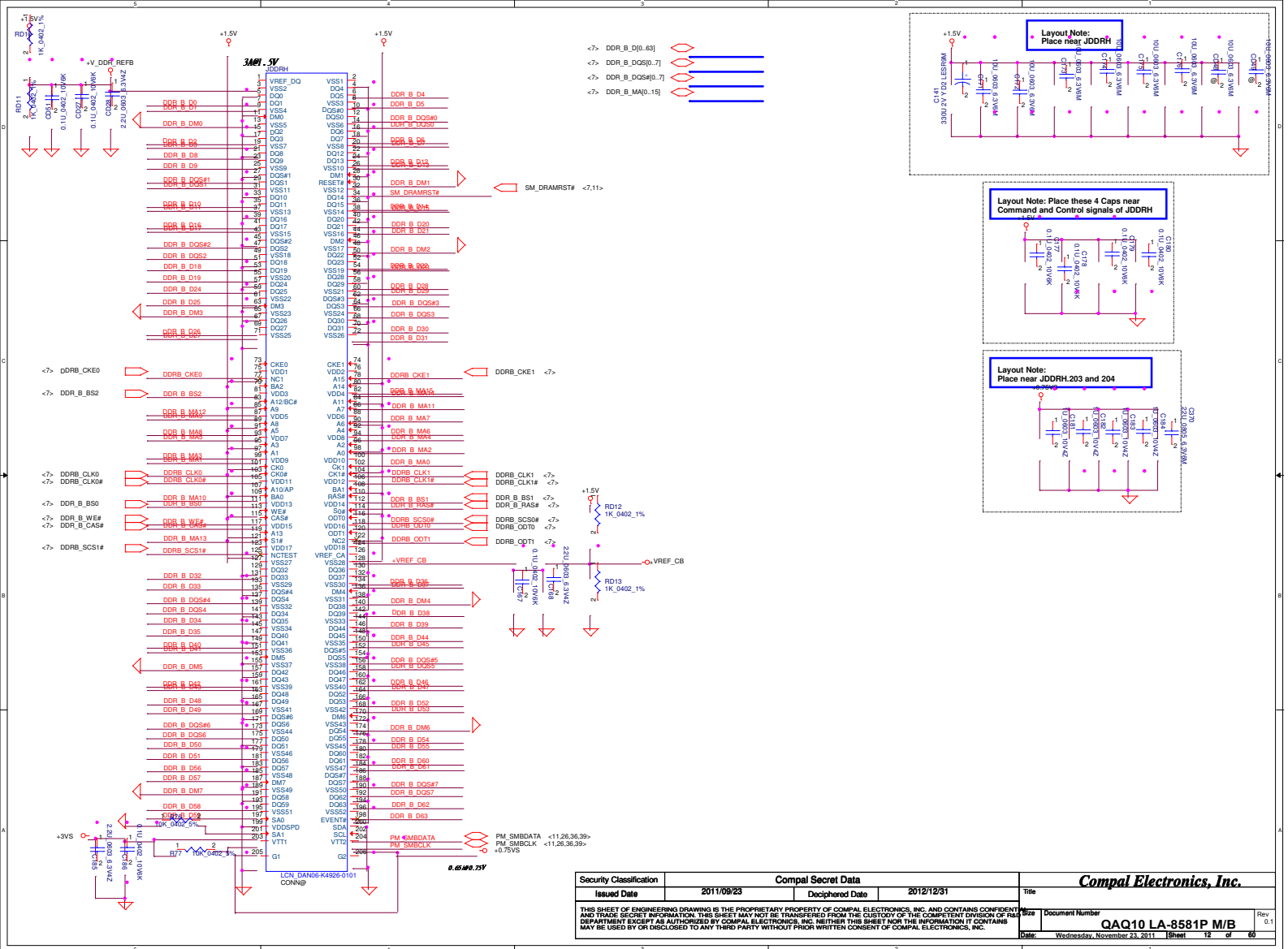


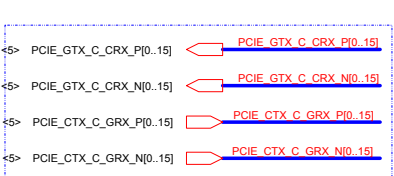
VCCSA\_VID Configuration --CPU EDS Page99.  
VCCSA\_VID[0] output default logic state is low for Sandy Bridge processors

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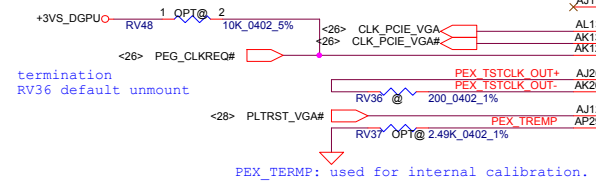
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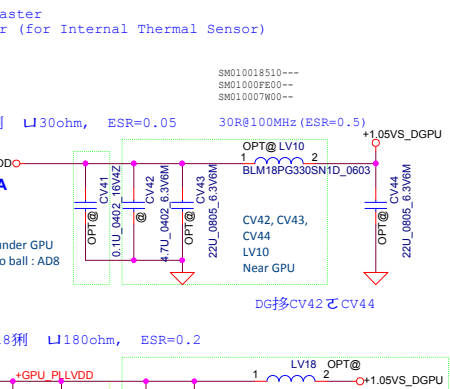
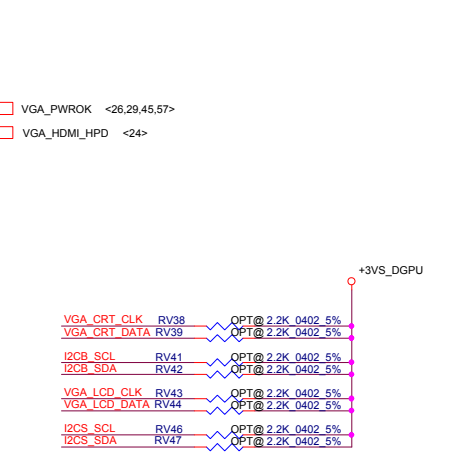
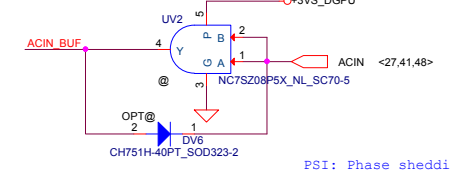
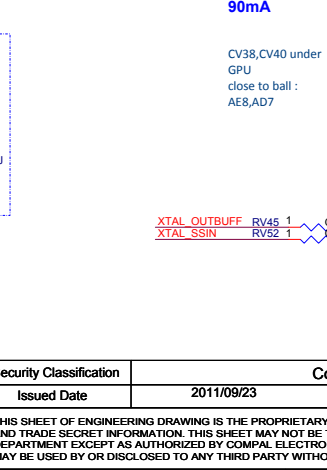
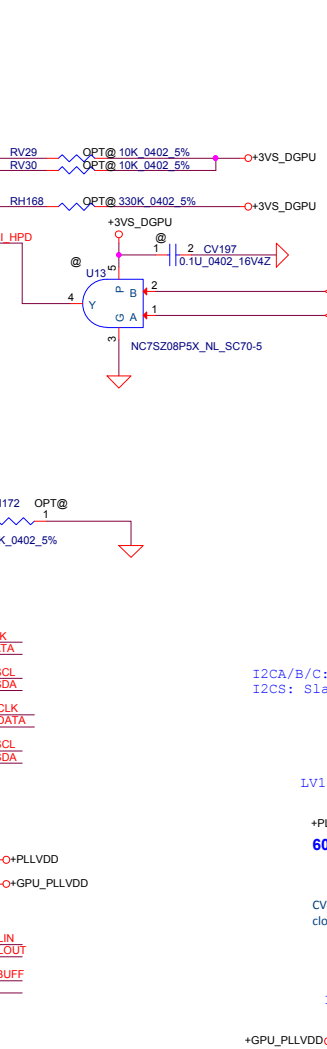
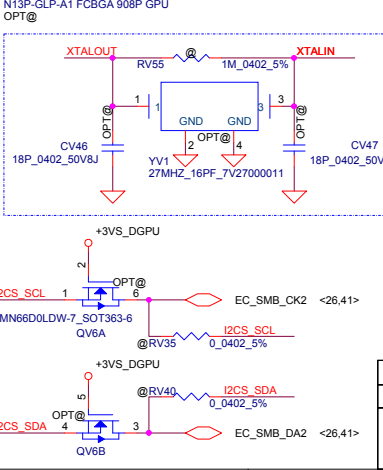
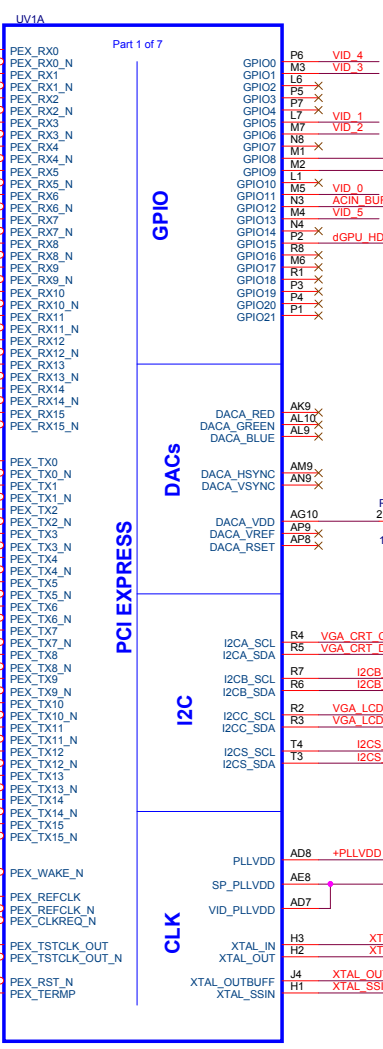
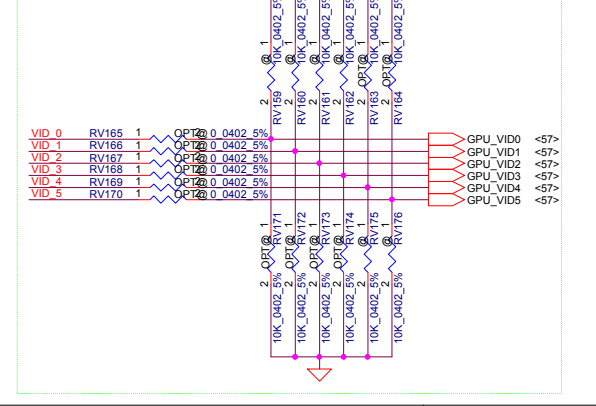


PCIE: 80ohm+10%  
45-50ohm+10%

PCIE GTX C CRX P15	OPT@C16	1	2	0.1U 0402 16V7K	PCIE GTX CRX P15	AK14	PEX_TX0
PCIE GTX C CRX N15	OPT@C17	1	2	0.1U 0402 16V7K	PCIE GTX CRX N15	AJ14	PEX_TX0_N
PCIE GTX C CRX P14	OPT@C18	1	2	0.1U 0402 16V7K	PCIE GTX CRX P14	AH14	PEX_TX1
PCIE GTX C CRX N14	OPT@C19	1	2	0.1U 0402 16V7K	PCIE GTX CRX N14	AG14	PEX_TX1_N
PCIE GTX C CRX P13	OPT@C20	1	2	0.1U 0402 16V7K	PCIE GTX CRX P13	AK15	PEX_TX2
PCIE GTX C CRX N13	OPT@C21	1	2	0.1U 0402 16V7K	PCIE GTX CRX N13	AJ15	PEX_TX2_N
PCIE GTX C CRX P12	OPT@C22	1	2	0.1U 0402 16V7K	PCIE GTX CRX P12	AL16	PEX_TX3
PCIE GTX C CRX N12	OPT@C23	1	2	0.1U 0402 16V7K	PCIE GTX CRX N12	AK16	PEX_TX3_N
PCIE GTX C CRX P11	OPT@C24	1	2	0.1U 0402 16V7K	PCIE GTX CRX P11	AK17	PEX_TX4
PCIE GTX C CRX N11	OPT@C25	1	2	0.1U 0402 16V7K	PCIE GTX CRX N11	AJ17	PEX_TX4_N
PCIE GTX C CRX P10	OPT@C26	1	2	0.1U 0402 16V7K	PCIE GTX CRX P10	AH17	PEX_TX5
PCIE GTX C CRX N10	OPT@C27	1	2	0.1U 0402 16V7K	PCIE GTX CRX N10	AG17	PEX_TX5_N
PCIE GTX C CRX P9	OPT@C28	1	2	0.1U 0402 16V7K	PCIE GTX CRX P9	AK18	PEX_TX6
PCIE GTX C CRX N9	OPT@C29	1	2	0.1U 0402 16V7K	PCIE GTX CRX N9	AJ18	PEX_TX6_N
PCIE GTX C CRX P8	OPT@C30	1	2	0.1U 0402 16V7K	PCIE GTX CRX P8	AL19	PEX_TX7
PCIE GTX C CRX N8	OPT@C31	1	2	0.1U 0402 16V7K	PCIE GTX CRX N8	AK19	PEX_TX7_N
PCIE GTX C CRX P7	OPT@C32	1	2	0.1U 0402 16V7K	PCIE GTX CRX P7	AK20	PEX_TX8
PCIE GTX C CRX N7	OPT@C33	1	2	0.1U 0402 16V7K	PCIE GTX CRX N7	AJ20	PEX_TX8_N
PCIE GTX C CRX P6	OPT@C34	1	2	0.1U 0402 16V7K	PCIE GTX CRX P6	AH20	PEX_TX9
PCIE GTX C CRX N6	OPT@C35	1	2	0.1U 0402 16V7K	PCIE GTX CRX N6	AG20	PEX_TX9_N
PCIE GTX C CRX P5	OPT@C36	1	2	0.1U 0402 16V7K	PCIE GTX CRX P5	AK21	PEX_TX10
PCIE GTX C CRX N5	OPT@C37	1	2	0.1U 0402 16V7K	PCIE GTX CRX N5	AJ21	PEX_TX10_N
PCIE GTX C CRX P4	OPT@C38	1	2	0.1U 0402 16V7K	PCIE GTX CRX P4	AL22	PEX_TX11
PCIE GTX C CRX N4	OPT@C39	1	2	0.1U 0402 16V7K	PCIE GTX CRX N4	AK22	PEX_TX11_N
PCIE GTX C CRX P3	OPT@C40	1	2	0.1U 0402 16V7K	PCIE GTX CRX P3	AK23	PEX_TX12
PCIE GTX C CRX N3	OPT@C41	1	2	0.1U 0402 16V7K	PCIE GTX CRX N3	AJ23	PEX_TX12_N
PCIE GTX C CRX P2	OPT@C42	1	2	0.1U 0402 16V7K	PCIE GTX CRX P2	AH23	PEX_TX13
PCIE GTX C CRX N2	OPT@C43	1	2	0.1U 0402 16V7K	PCIE GTX CRX N2	AG23	PEX_TX13_N
PCIE GTX C CRX P1	OPT@C116	1	2	0.1U 0402 16V7K	PCIE GTX CRX P1	AK24	PEX_TX14
PCIE GTX C CRX N1	OPT@C213	1	2	0.1U 0402 16V7K	PCIE GTX CRX N1	AJ24	PEX_TX14_N
PCIE GTX C CRX P0	OPT@C228	1	2	0.1U 0402 16V7K	PCIE GTX CRX P0	AL25	PEX_TX15
PCIE GTX C CRX N0	OPT@C47	1	2	0.1U 0402 16V7K	PCIE GTX CRX N0	AK25	PEX_TX15_N

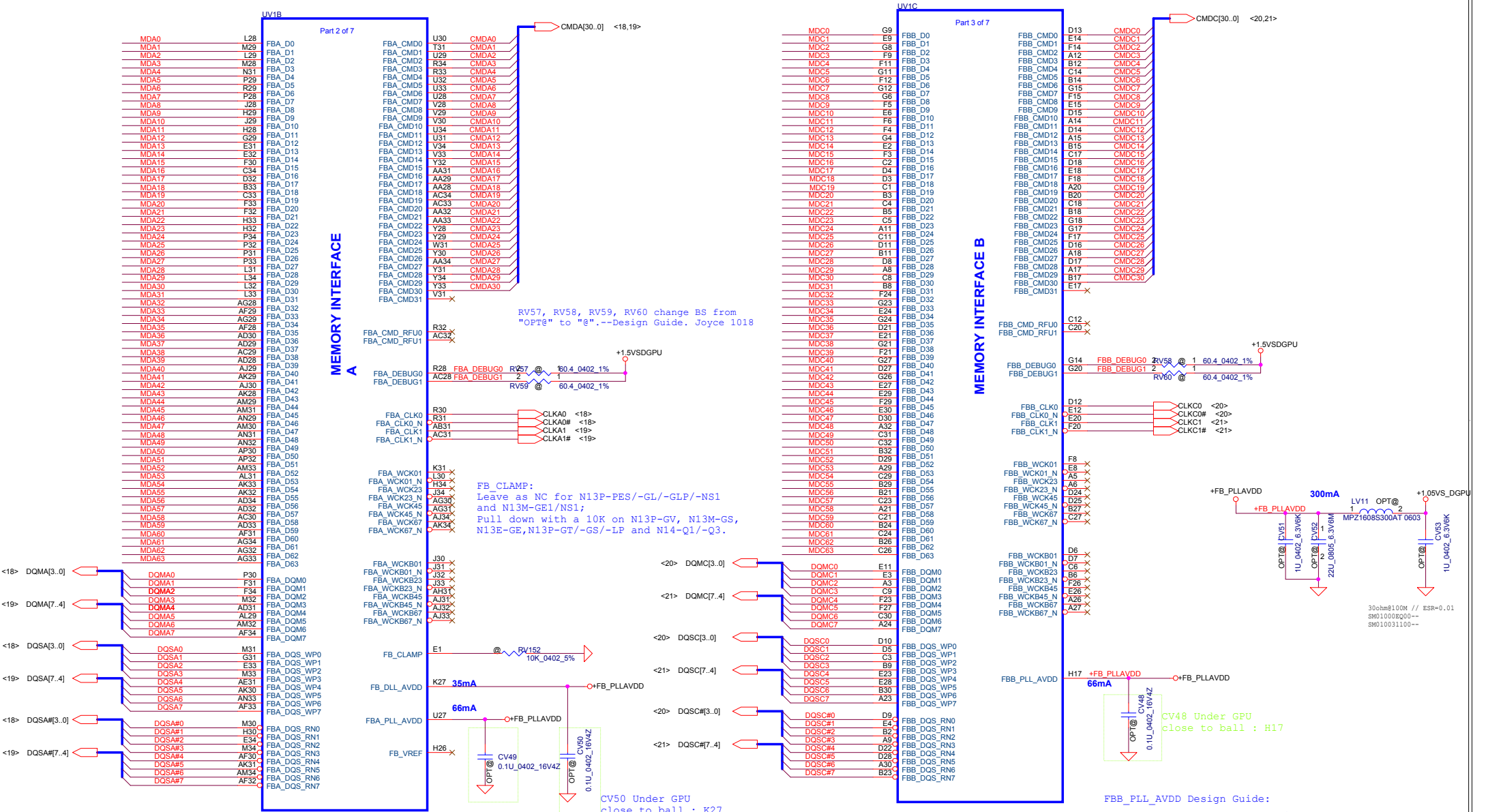
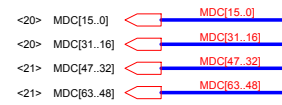
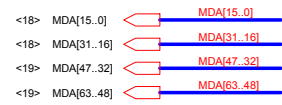


VID Default setup is for boot voltage 0.9V

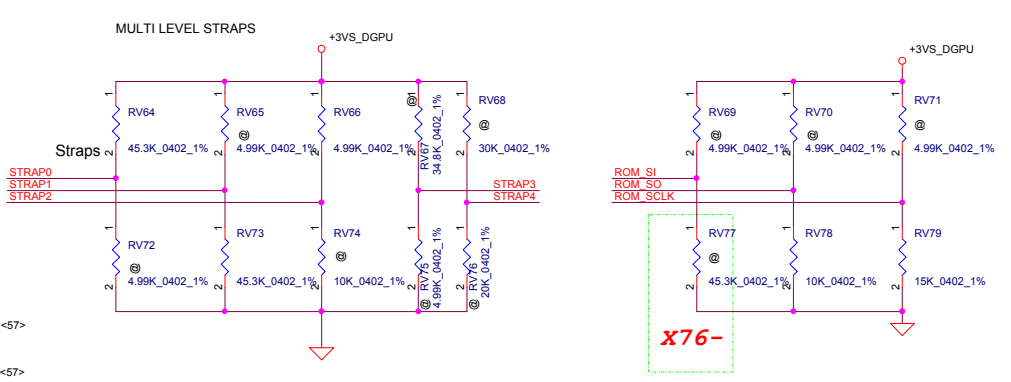
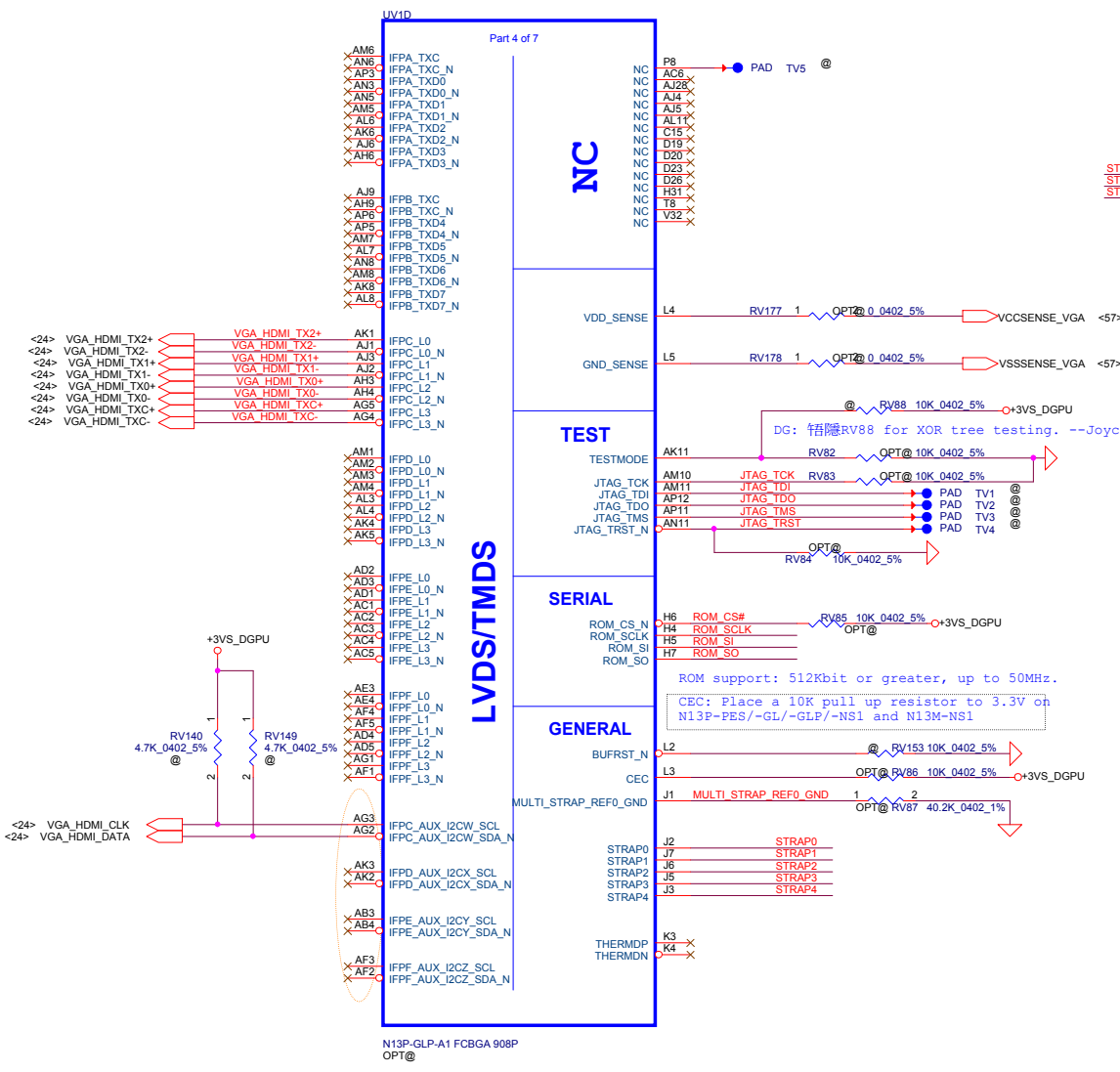


GPIO	I/O	USAGE
GPIO0	O	GPU Core VID4
GPIO1	O	GPU Core VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC or PSI
GPIO4	O	LCD_BLEN
GPIO5	O	GPU Core VID1
GPIO6	O	GPU Core VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU Core VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU Core VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL or PSI
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

# VRAM Interface



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Physical strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB [1]	FB [0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER [3]	USER [2]	USER [1]	USER [0]
STRAP1	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	PCI-DEVID [3]	PCI-DEVID [2]	PCI-DEVID [1]	PCI-DEVID [0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull up to 3V	Pull down to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	0 No VBIOS ROM 1 BIOS ROM is present (Default)	PEX_PLL_EN_TERM: PLL termination setting 0 Disable (Default) 1 Enable	PCIE_MAX_SPEED 0 Limited to PCIE GEN 1 1 PCIE GEN 2/3 capable
FB [1:0]: N13x FB Aperture Size	0 RESERVED 1 RESERVED 2 256 MB (Default) 3 RESERVED		
USER Straps	1111 EDID is used Others: DG-05587 Page195		
3GIO_PAD_CFG	0000-0101 RESERVED 0110 Notebook (default) 0111-1111 RESERVED		

**For N13P-GLP strap table**

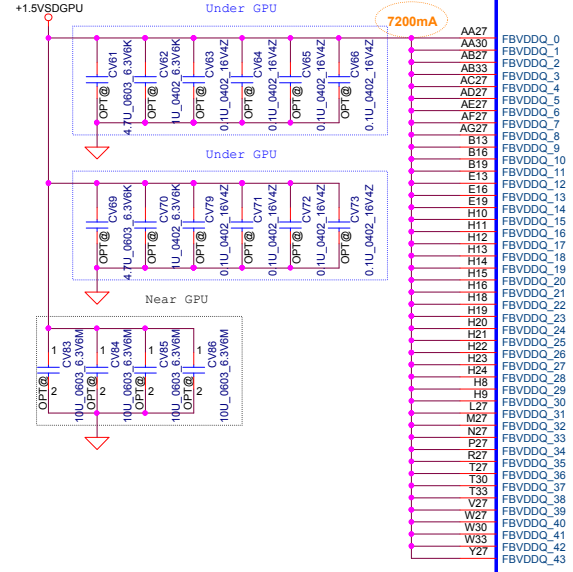
**For N13P-PES :**  
**Strap 0 : PU45**  
**Strap 1 : PD35**  
**Strap 2 : PU35**  
**ROM\_SCLK : PU15**  
**ROM\_SI : PD35**  
**ROM\_SO : PD10**

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GLP	900 MHz	84M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 15K	RV70 PD 30K	RV71 PD 15K
	900 MHz	84M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 20K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003Y000	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 35K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 45K	RV70 PD 30K	RV71 PD 15K

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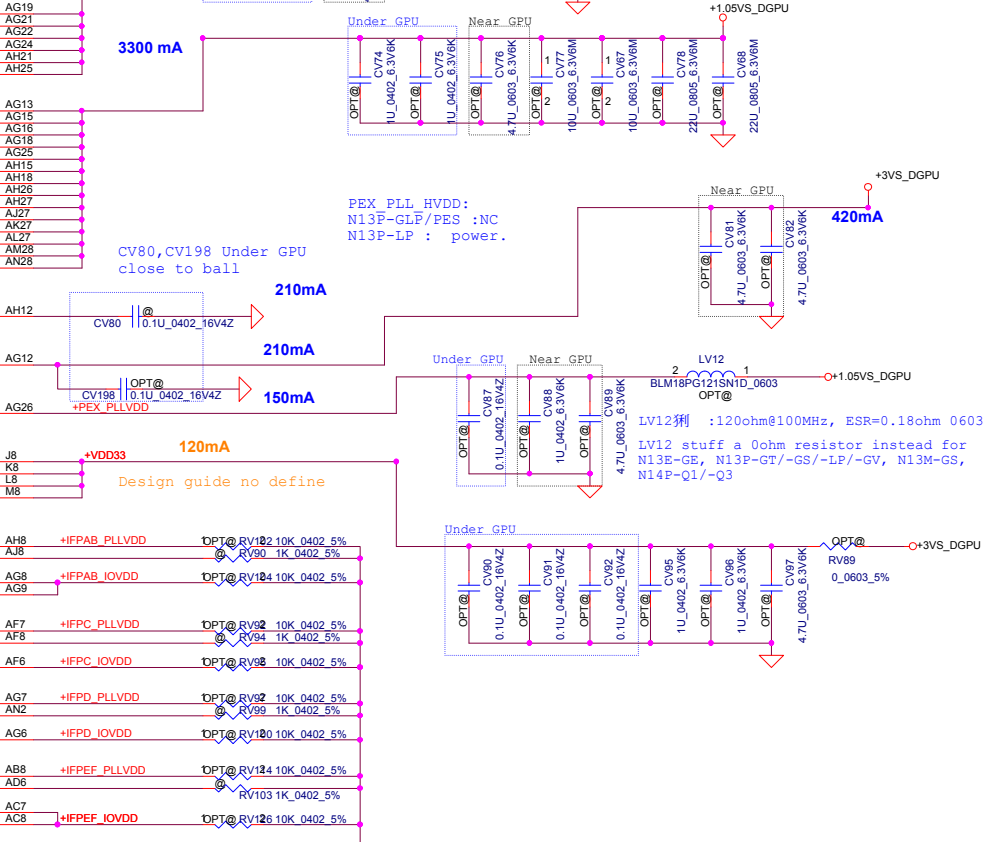
FBVDDQ Decoupling Design Guide:  
 0.1uF X7R 0402 8pcs Under GPU  
 1uF X7R 0603 2pcs Under GPU  
 4.7uF X6S 0603 2pcs Under GPU  
 10uF X5R 0805 4pcs Near GPU

Design guide no define

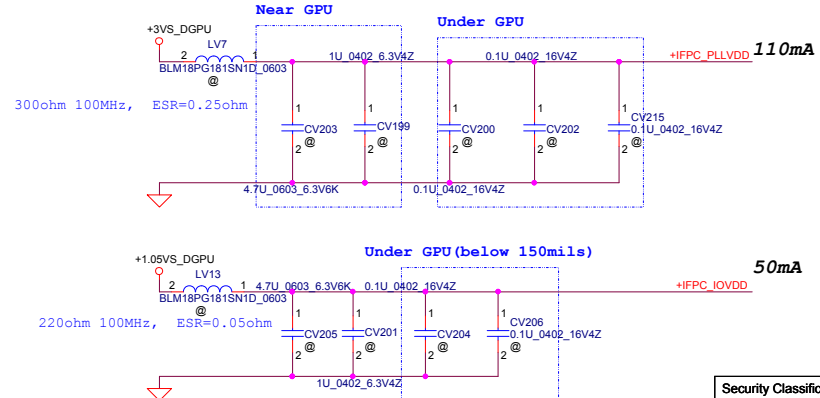


**POWER**

- AA27 FBVDDQ\_0
- AA30 FBVDDQ\_1
- AB27 FBVDDQ\_2
- AB33 FBVDDQ\_3
- AC27 FBVDDQ\_4
- AD27 FBVDDQ\_5
- AE27 FBVDDQ\_6
- AF27 FBVDDQ\_7
- AG27 FBVDDQ\_8
- B13 FBVDDQ\_9
- B16 FBVDDQ\_10
- B19 FBVDDQ\_11
- E13 FBVDDQ\_12
- E16 FBVDDQ\_13
- E19 FBVDDQ\_14
- H10 FBVDDQ\_15
- H11 FBVDDQ\_16
- H12 FBVDDQ\_17
- H13 FBVDDQ\_18
- H14 FBVDDQ\_19
- H15 FBVDDQ\_20
- H16 FBVDDQ\_21
- H18 FBVDDQ\_22
- H19 FBVDDQ\_23
- H20 FBVDDQ\_24
- H21 FBVDDQ\_25
- H22 FBVDDQ\_26
- H23 FBVDDQ\_27
- H8 FBVDDQ\_28
- H9 FBVDDQ\_29
- L10 FBVDDQ\_30
- L27 FBVDDQ\_31
- M27 FBVDDQ\_32
- N27 FBVDDQ\_33
- P27 FBVDDQ\_34
- R27 FBVDDQ\_35
- T27 FBVDDQ\_36
- T30 FBVDDQ\_37
- T33 FBVDDQ\_38
- V27 FBVDDQ\_39
- W27 FBVDDQ\_40
- W30 FBVDDQ\_41
- W33 FBVDDQ\_42
- Y27 FBVDDQ\_43



Calibration Pin	DDR3	DDR5
FB_CAL_PD_VDDQ	40.2ohm	40.2ohm
FB_CAL_PU_GND	42.2ohm	40.2ohm
FB_CAL_TERM_GND	51.1ohm	60.4ohm



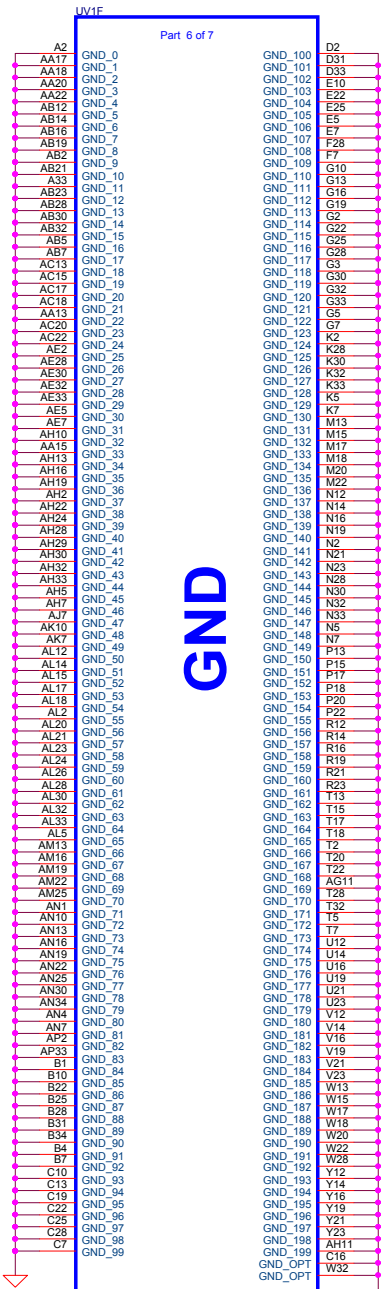
Capacitor Type	Footprint	Population	Location
1.0uF X6S	0402	4	Under GPU
4.7uF X6S	0603	2	Near GPU
10uF X5R	0805	4	Midway between GPU and Power Supply
22uF X5R	0805	4	Midway between GPU and Power Supply

Capacitor Type	Footprint	Population	Location
100nF X6S	0402	1	Under GPU
1.0uF X5R	0603	1	Near GPU
4.7uF X5R	0805	1	Near GPU

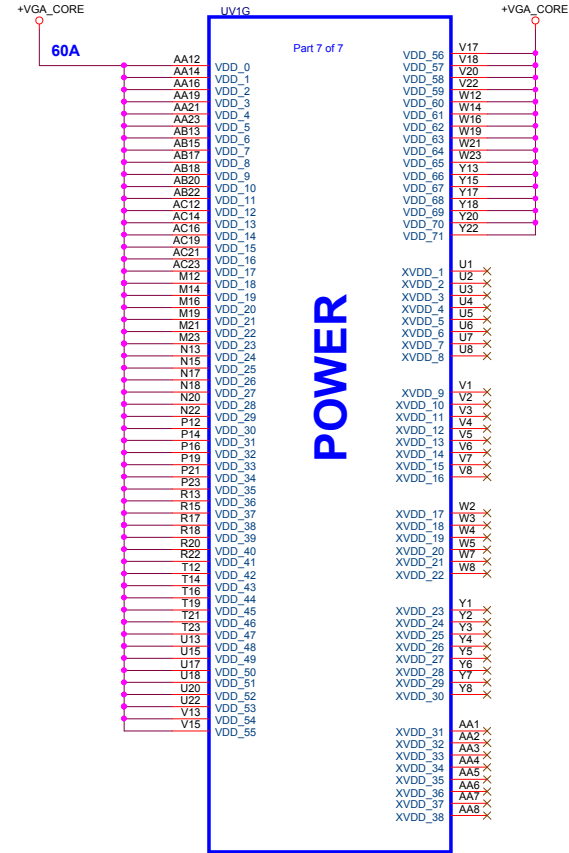
Capacitor Type	Footprint	Population	Location
0.1uF X5R	0402	1	Near GPU
4.7uF X5R	0603	2	Near GPU

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N13P-GLP-A1 FCBGA 908P  
OPT@

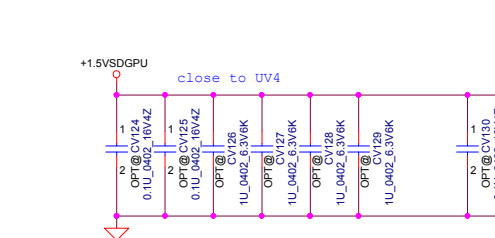
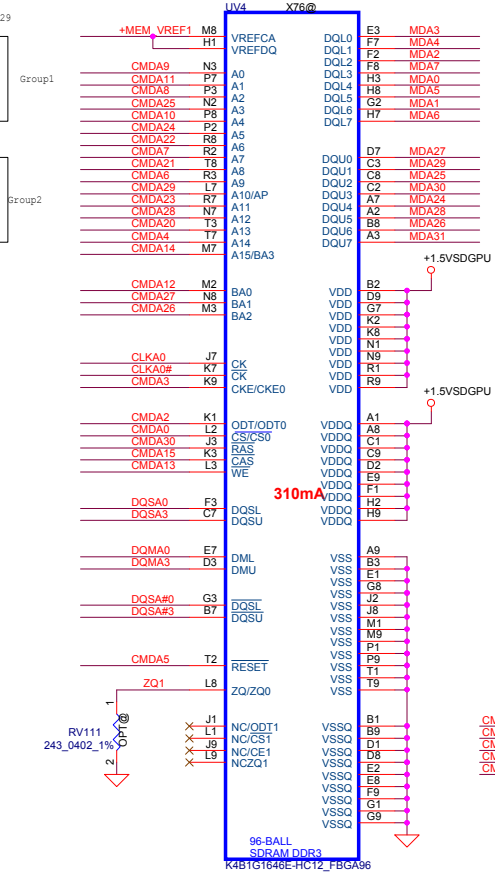
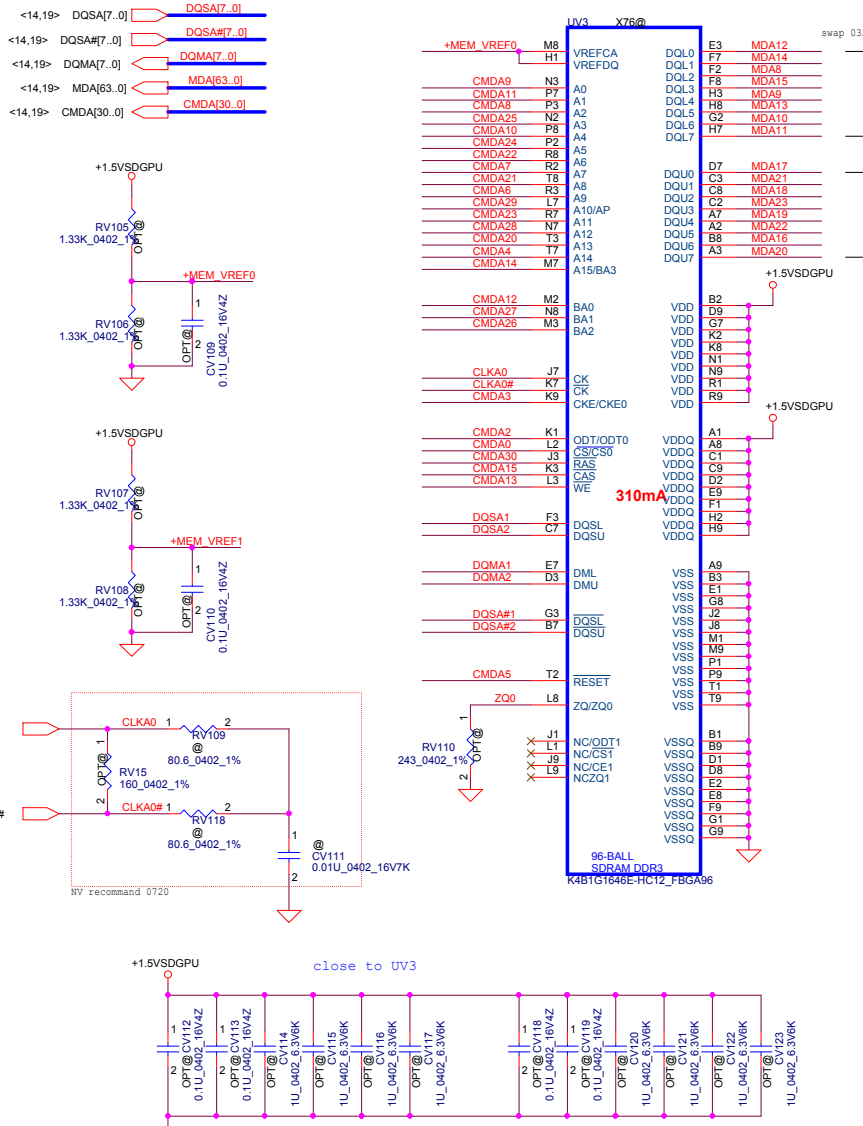


N13P-GLP-A1 FCBGA 908P GPU  
OPT@

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				Rev 0.1

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB  
128Mx16 DDR3 \*8==>2GB



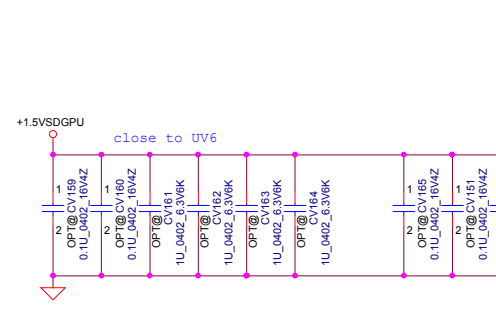
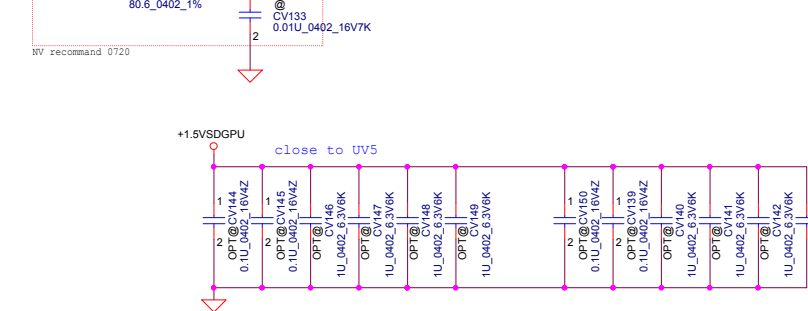
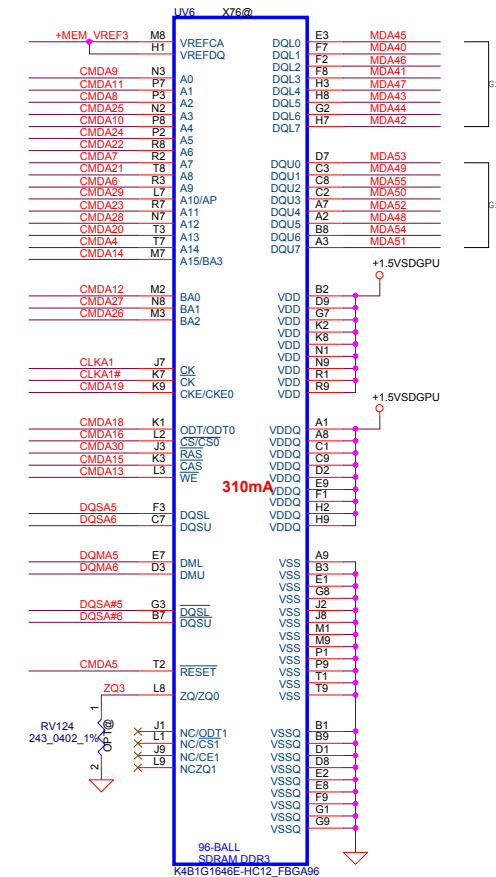
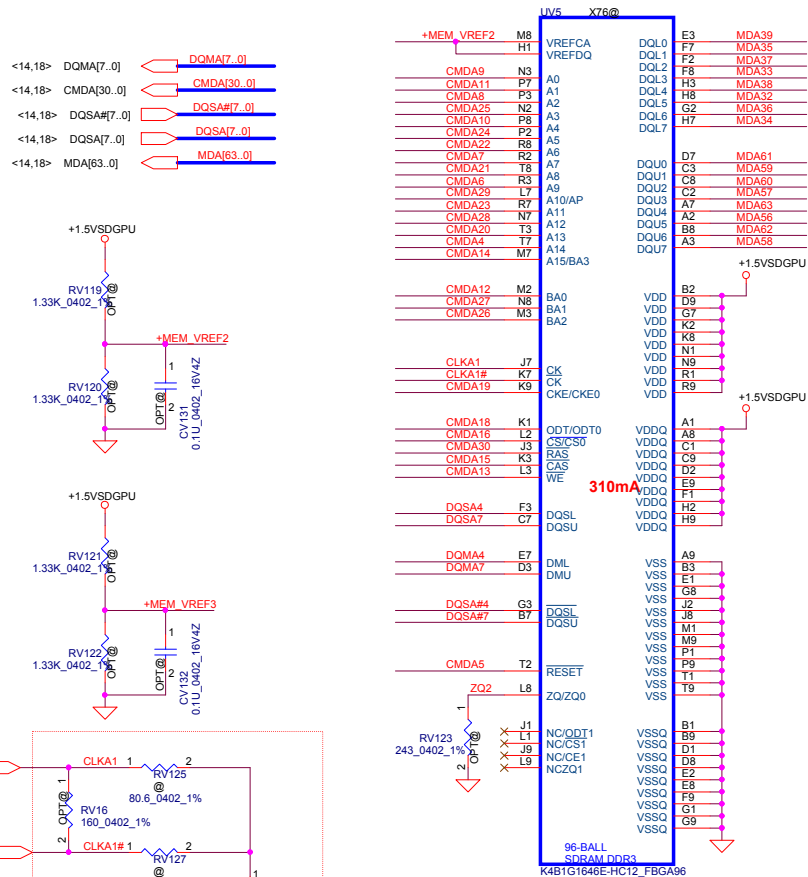
Command Bit	Default Pull-down
ODTx	10k
CKE#	10k
RST	10k
CS*	No Termination

Mode D Address	0..31	32..63
CMD0	CS0_I#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

128Mx16 DDR3 \*8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31		

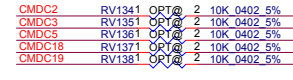
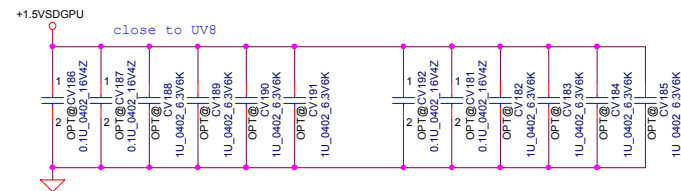
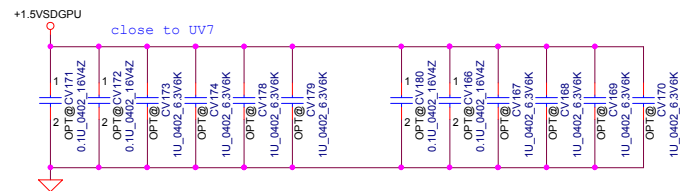
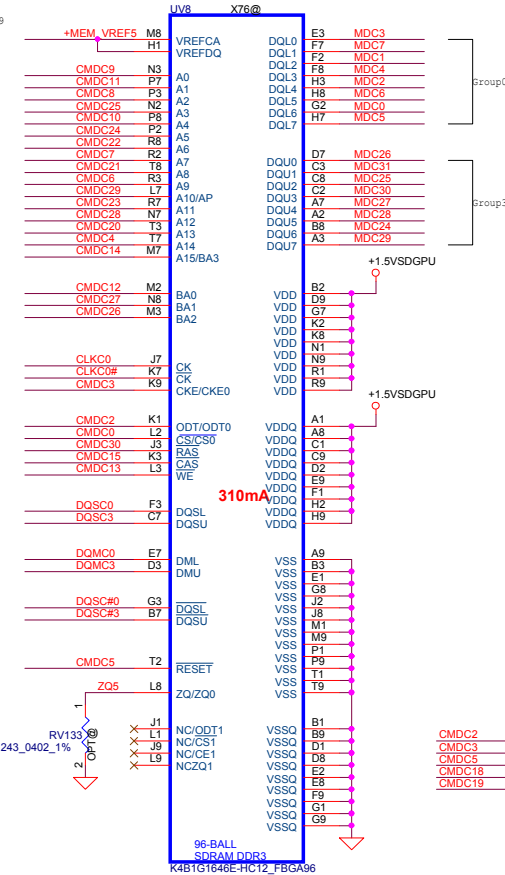
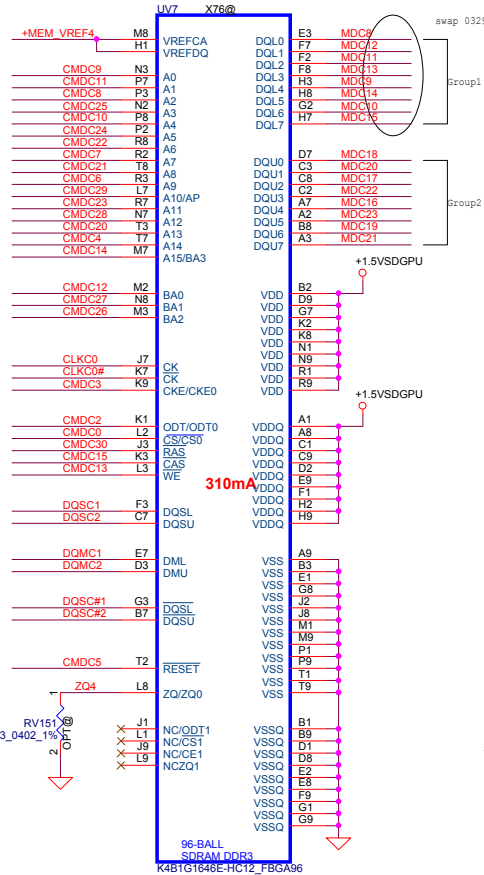
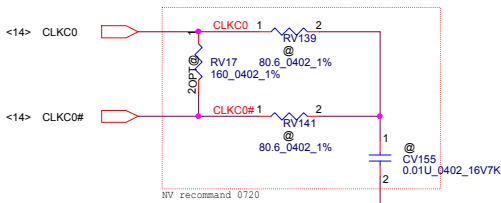
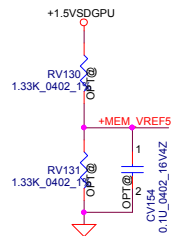
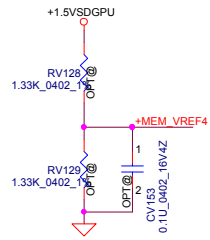
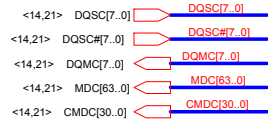
LOW HIGH

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# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

128Mx16 DDR3 \*8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Command Bit	Default Pull-down
ODTX	10k
CKE	10k
RST	10k
CAS*	No Termination

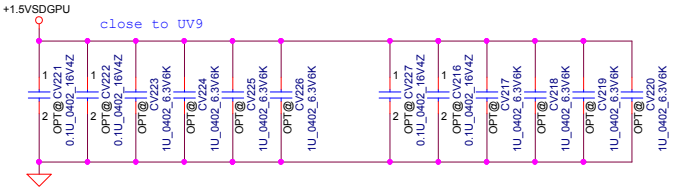
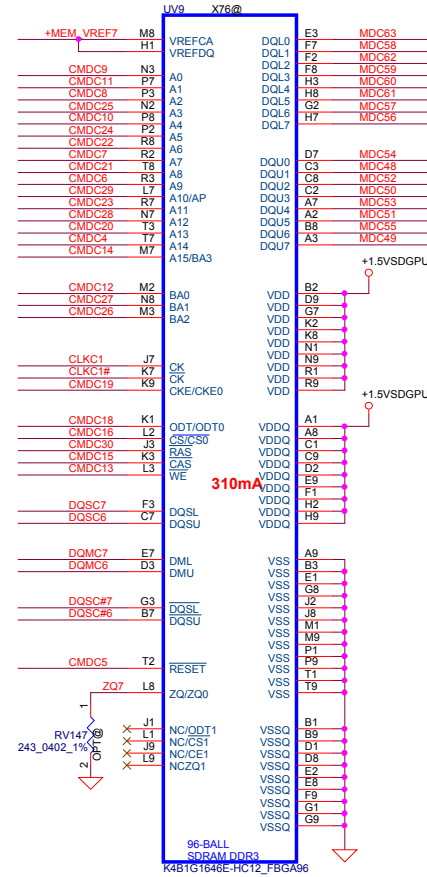
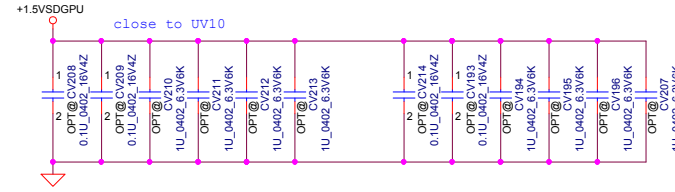
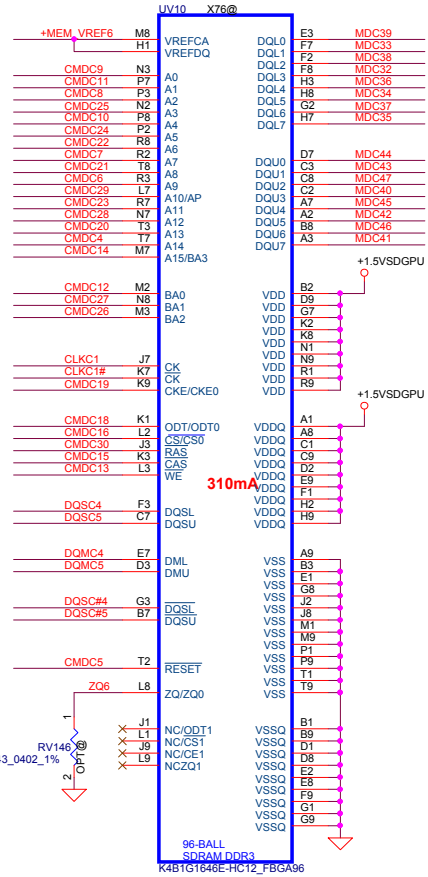
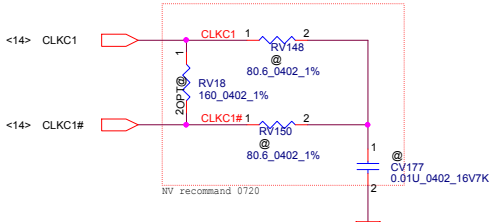
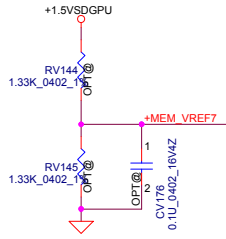
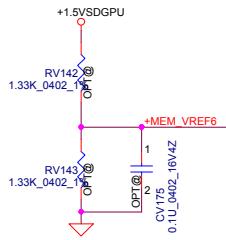
Security Classification	Compal Secret Data		Title <b>N13P DDR3 8/9</b>
Issued Date	2011/09/23	Deciphered Date	
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# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

128Mx16 DDR3 \*8==>2GB

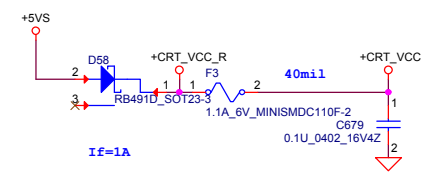
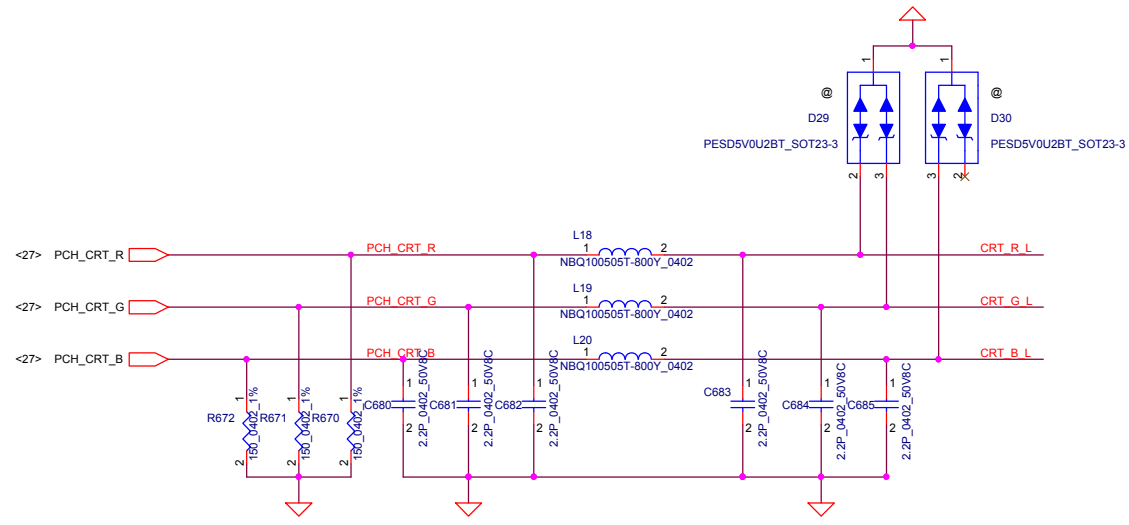
- <14,20> DQMC[7..0] DOMC[7..0]
- <14,20> CMDC[30..0] CMDC[30..0]
- <14,20> DQSC#[7..0] DQSC#[7..0]
- <14,20> DQSC[7..0] DQSC[7..0]
- <14,20> MDC[63..0] MDC[63..0]



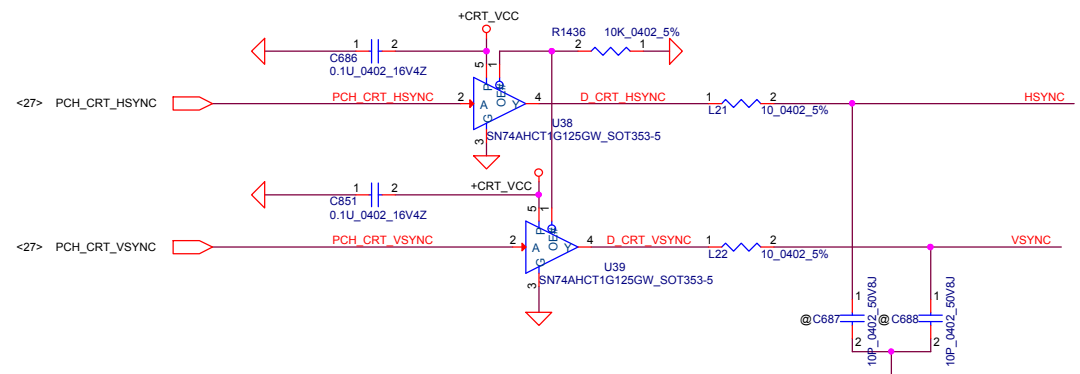
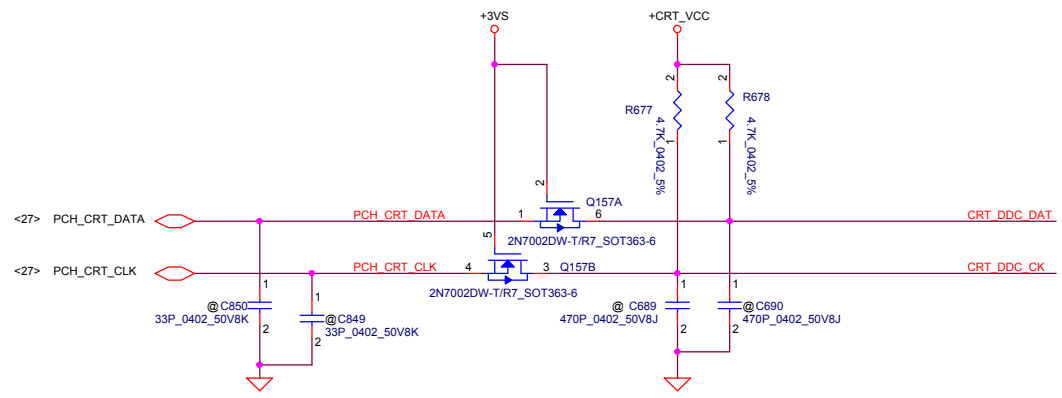
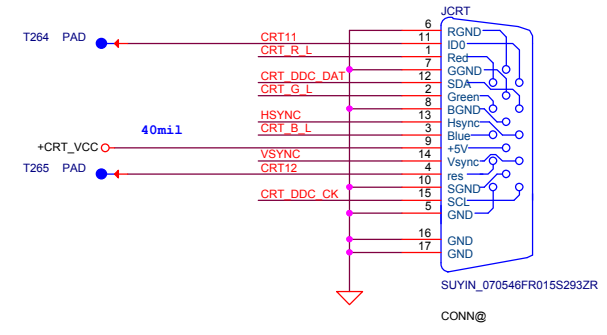
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

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				Date	Wednesday, November 23, 2011
				Sheet	21 of 59

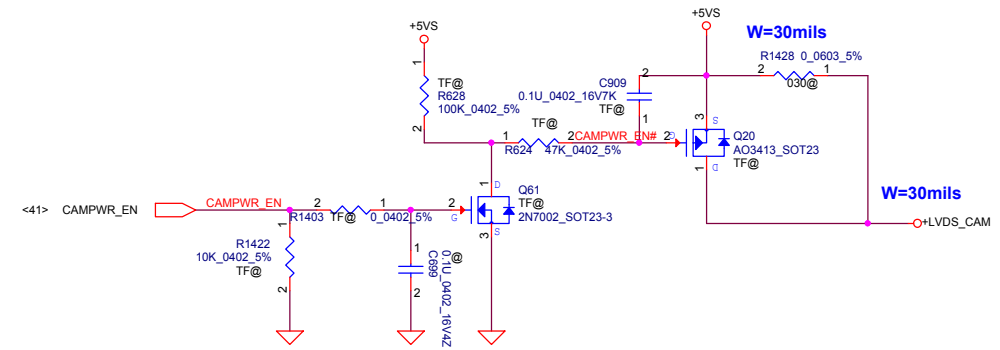
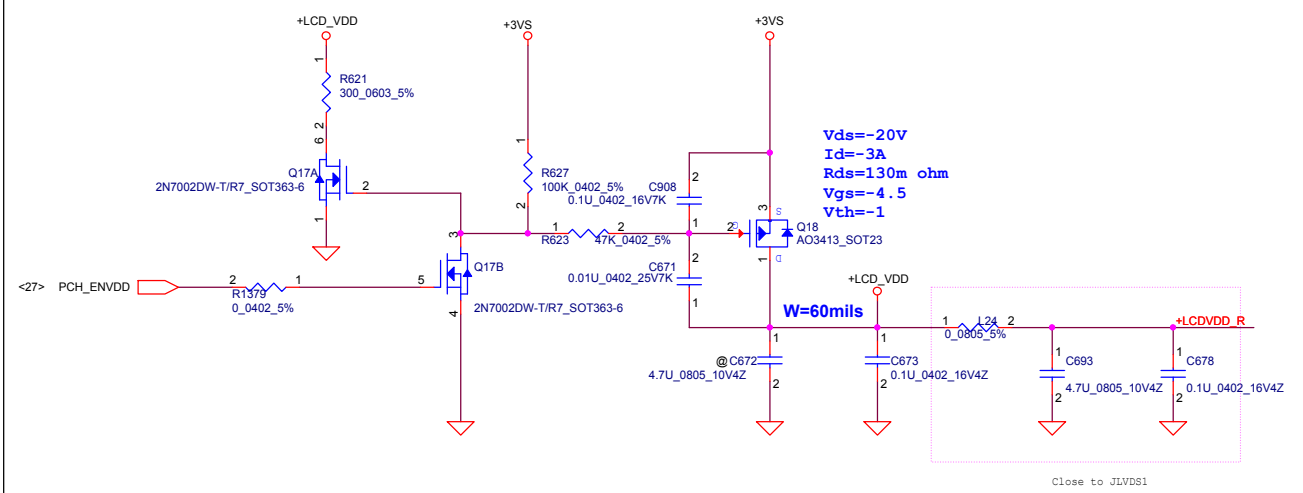
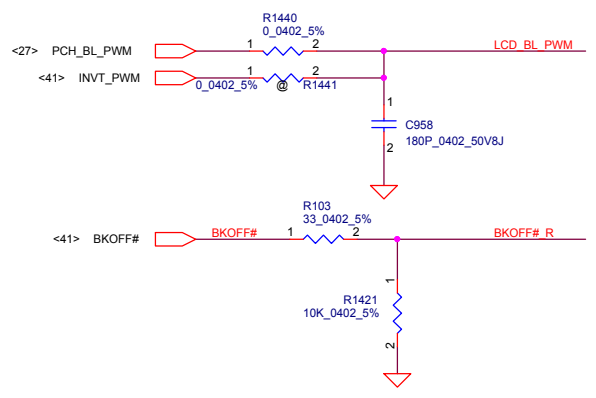


### CRT CONNECTOR

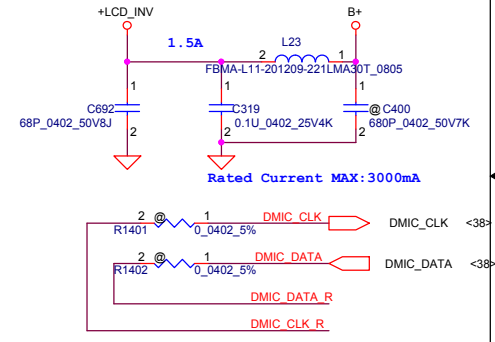
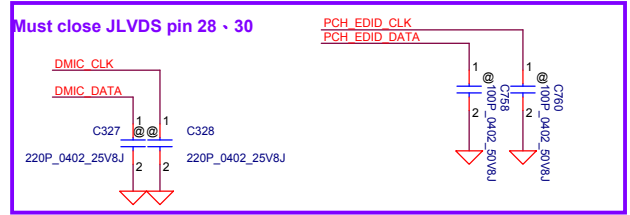


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Date: Wednesday, November 23, 2011				Sheet	22 of 59

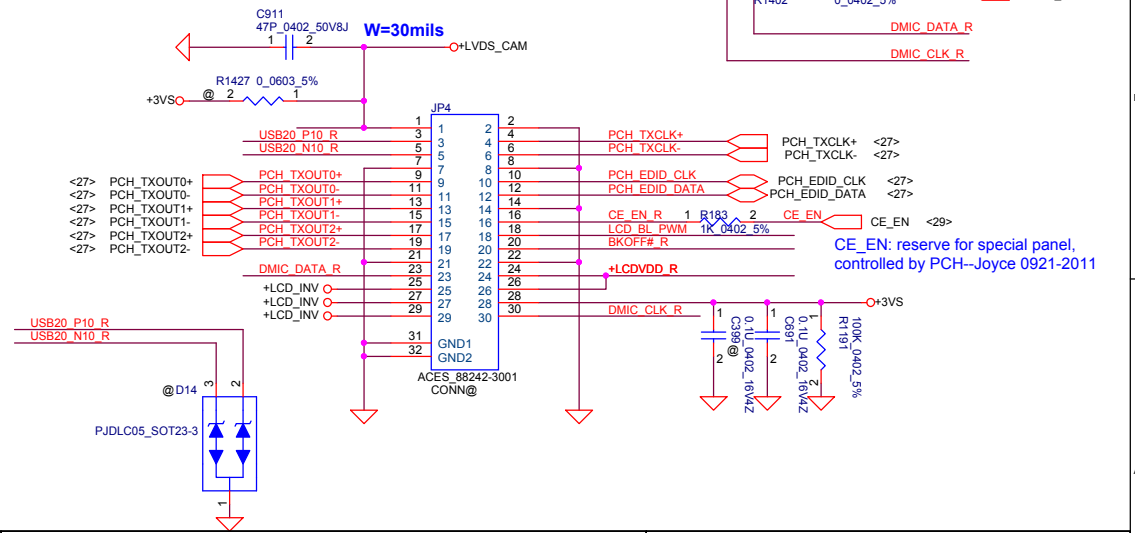
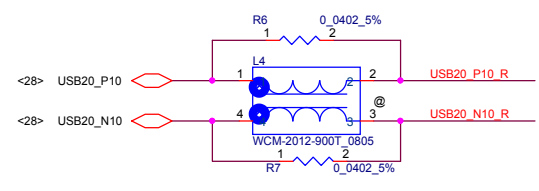
Document Number  
**QAQ10 LA-8581P M/B**  
Rev 0.1



**LCD/PANEL BD. Conn.**



Add on 7/27 for fn+f5 turn off camera.



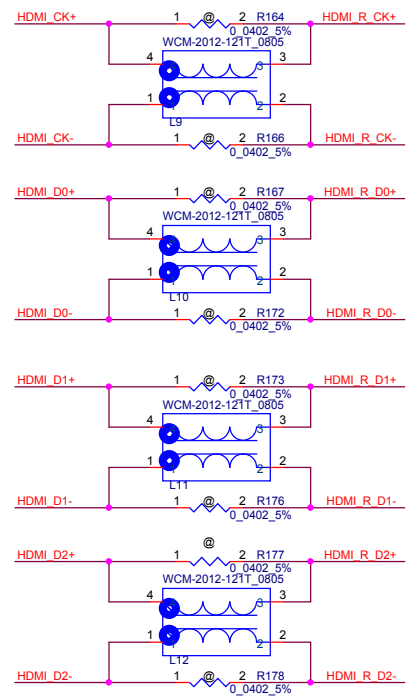
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Issued Date	2011/09/23	Deciphered Date	2011/12/30	Compal Electronics, Inc.
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				Document Number
				QAQ10 LA-8581P M/B
				Rev
				0.1
				Date: Wednesday, November 23, 2011
				Sheet 23 of 59

### HDMI Source Select



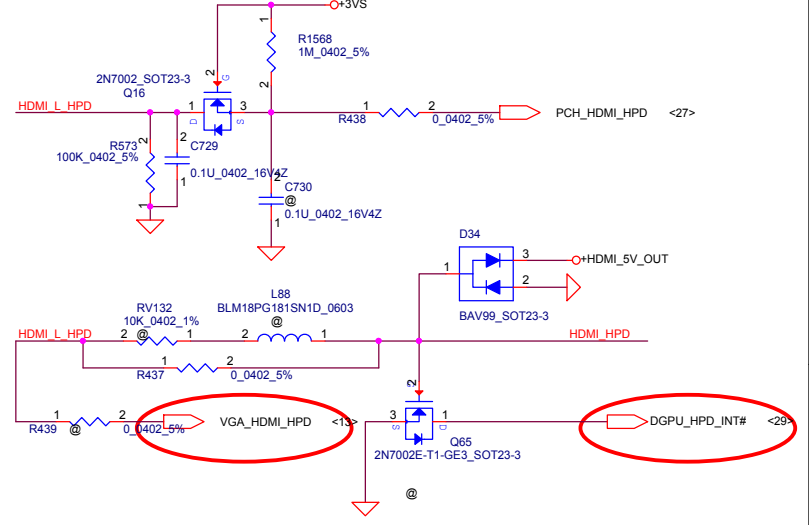
VGA Video Channel  
DISO and OPT Channel

Internal Graphic Video Channel  
UMA0 Channel

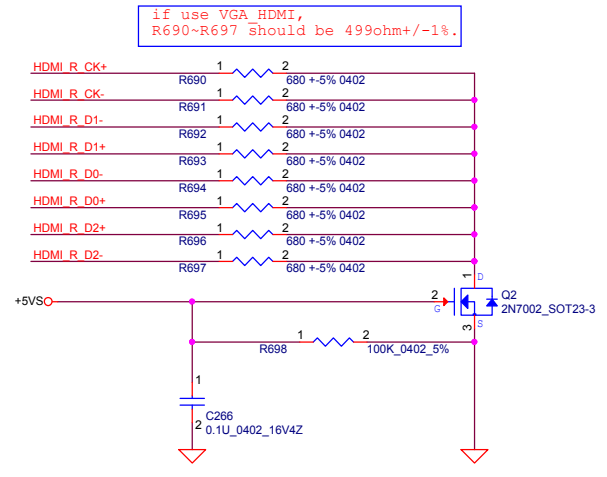
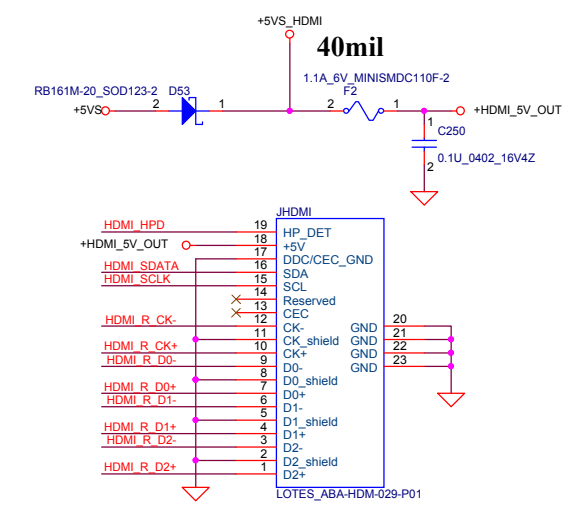


EVT mount chock, DVT mount resistor

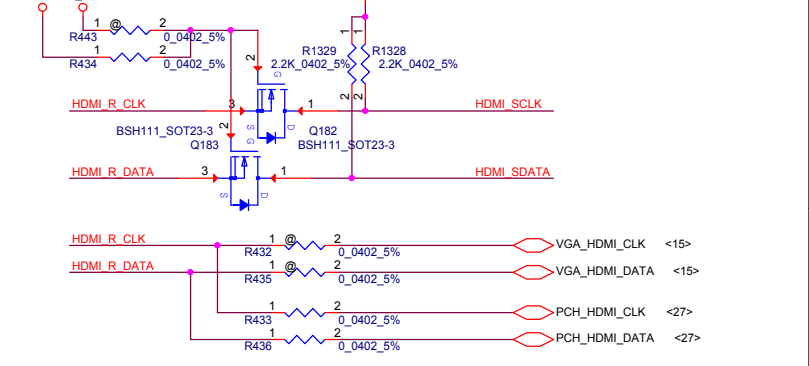
### HOT PLUG1



### HDMI Connector



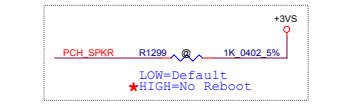
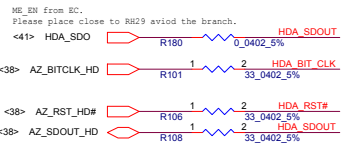
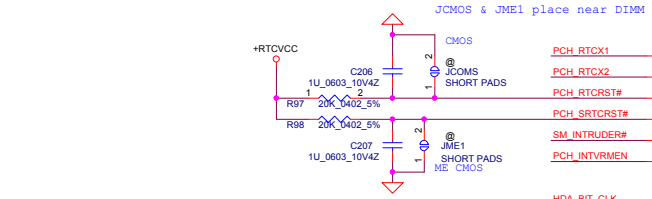
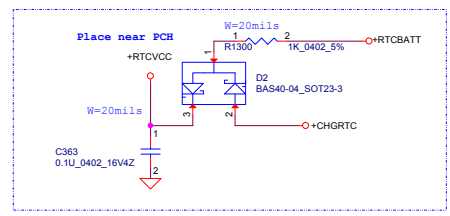
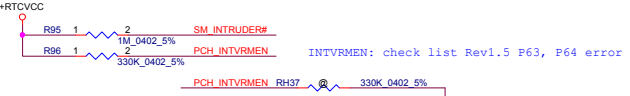
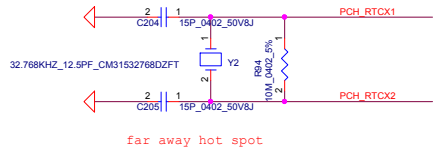
### EDID SELECT



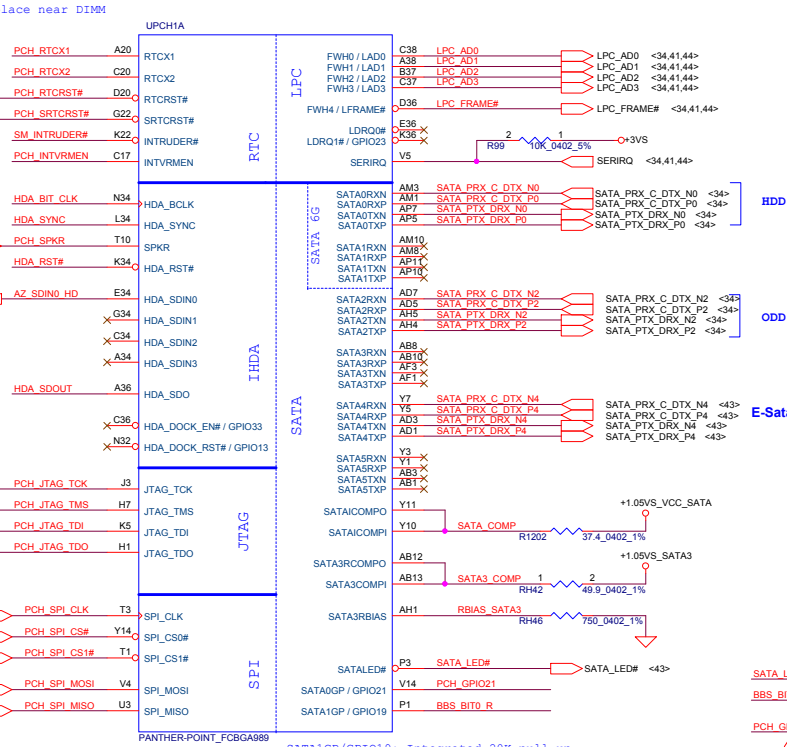
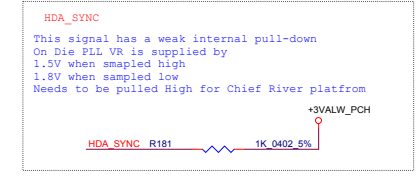
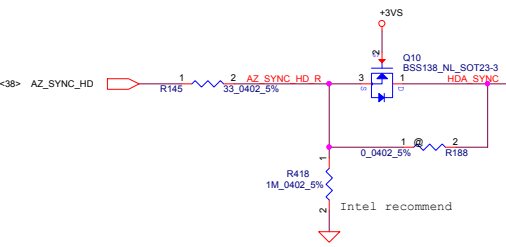
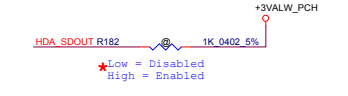
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/09/23	Deciphered Date	2011/12/30	Title	
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Size	Document Number	Date		Rev	
	QAQ10 LA-8581P M/B	Wednesday, November 23, 2011		0.1	
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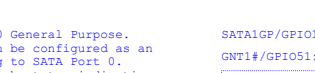
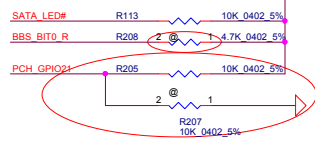
**Integrated SUS 1.05V VRM Enable**  
**PCH\_INTVRMEN** High - Enable Internal VRs  
 (must be always pulled high)



**HDA\_SDO**  
 ME debug mode, this signal has a weak internal PD  
 L=>security measures defined in the Flash Descriptor will be in effect (default)  
 H=>Flash Descriptor Security will be overridden



SATA1GP/GPIO19: Integrated 20K pull up.



SATA0GP / GPIO21: Serial ATA 0 General Purpose. This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to &0\* to indicate that the switch is closed and to &1\* to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.

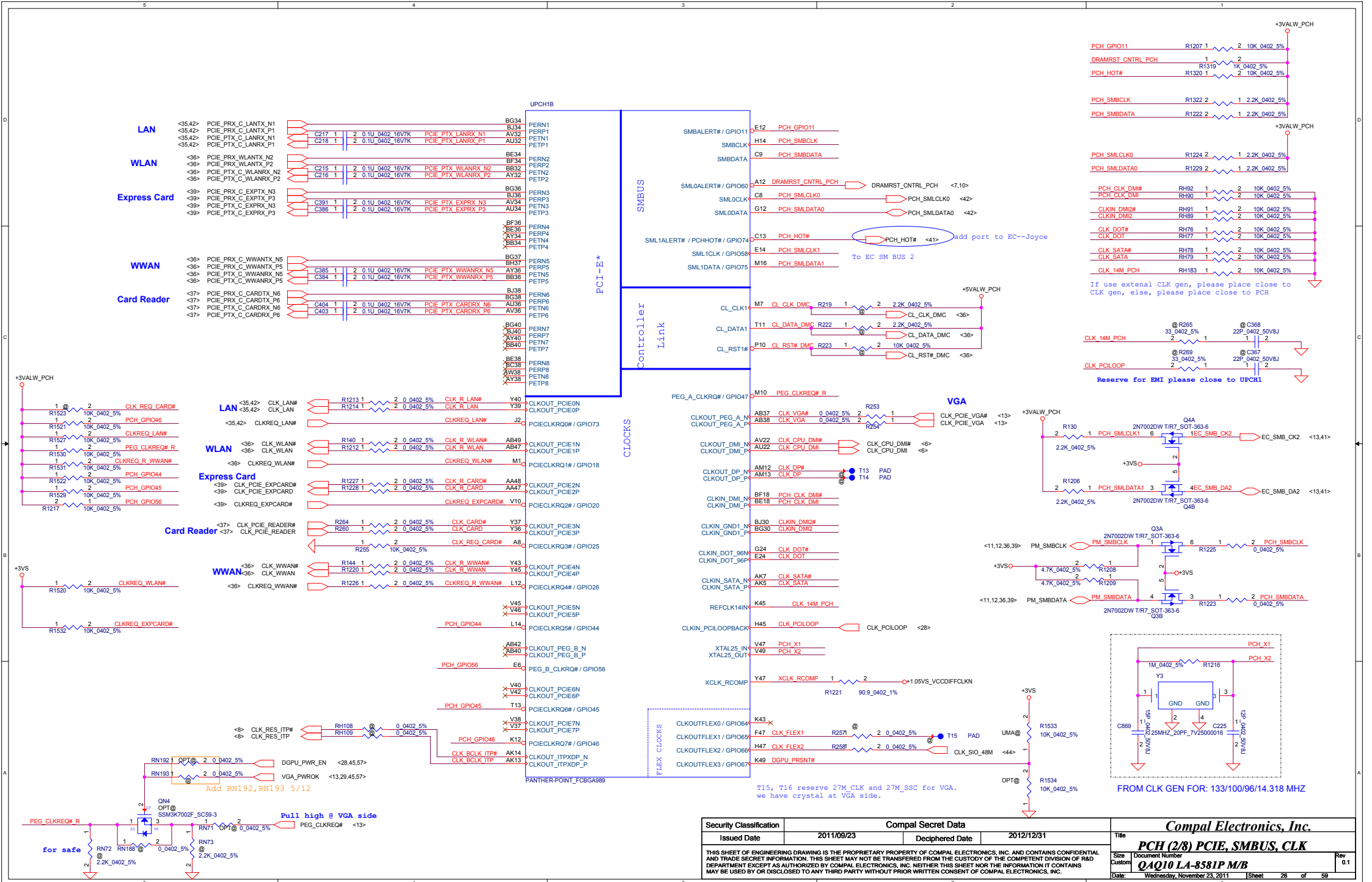
SATA1GP/GPIO19: Boot BIOS Strap bit 0 (BBS0)  
 GNT1#/GPIO51: Boot BIOS Strap bit 1 (BBS1)

GPIO19 => BBS\_BIT0  
 GPIO51 => BBS\_BIT1

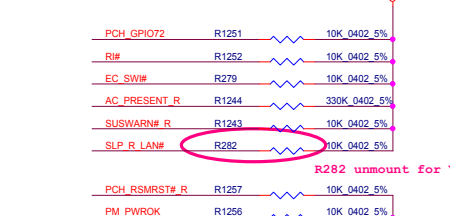
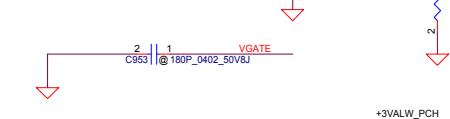
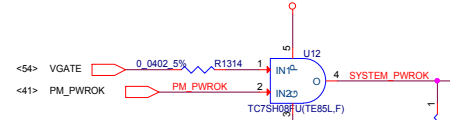
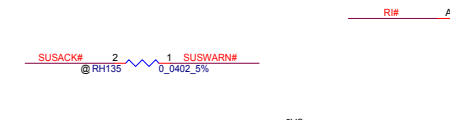
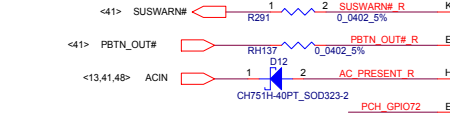
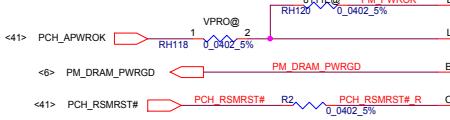
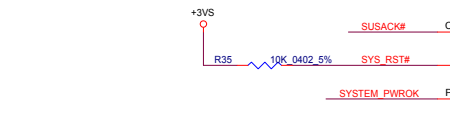
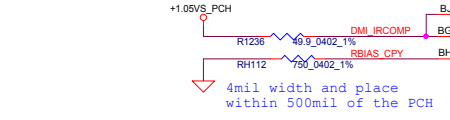
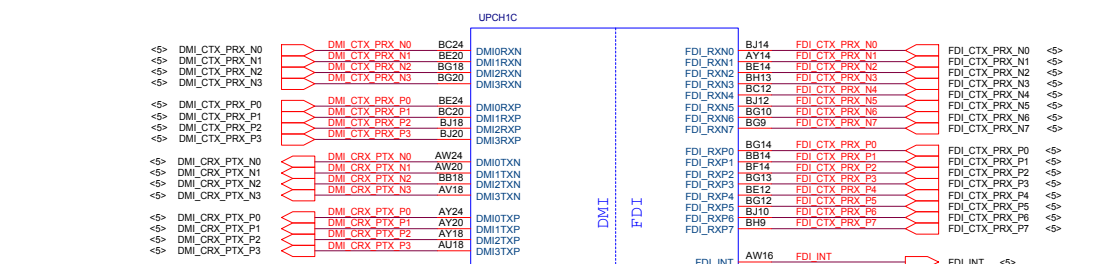
Boot BIOS Strap

Bit 11 (BBS1)	Bit 10 (BBS0)	Boot BIOS Destination
0	1	Reserved
1	0	PCI
1	1	SPI *
0	0	LPC

PCH EDS Rev1.5 P99, P98



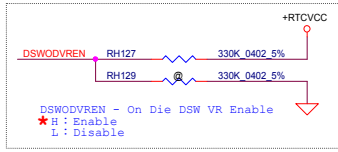
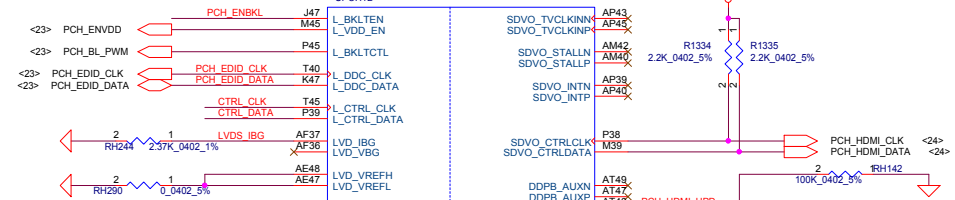
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Issued Date	2011/09/23	Deciphered Date	2012/12/31
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<p><b>Compal Electronics, Inc.</b></p> <p><b>PCH (2/8) PCIE, SMBUS, CLK</b></p>		<p>Document Number <b>QAQ10 LA-8581P M/B</b></p>	
Date:	Wednesday, November 23, 2011	Sheet	26 of 59



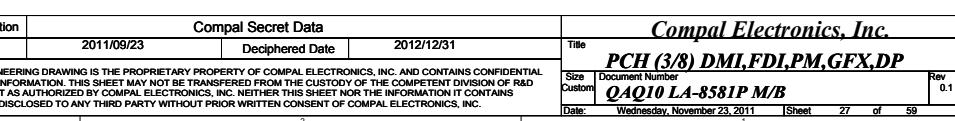
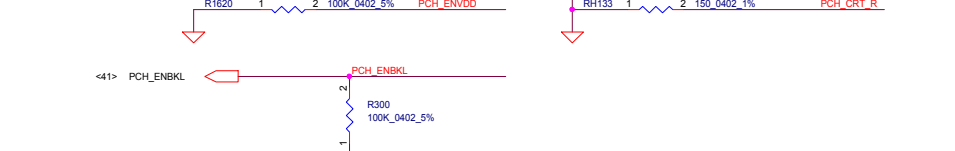
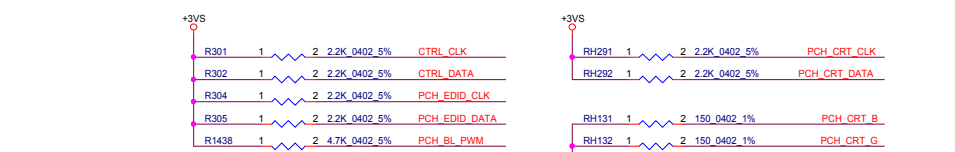
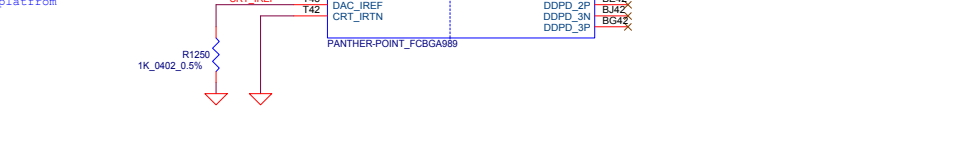
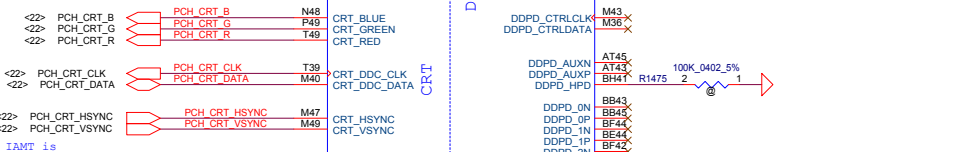
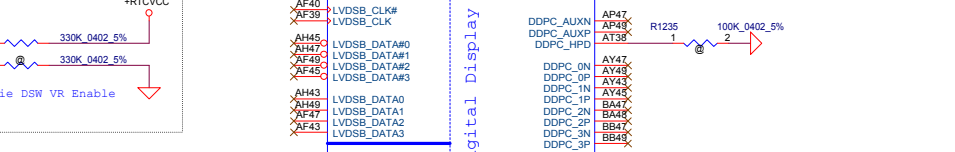
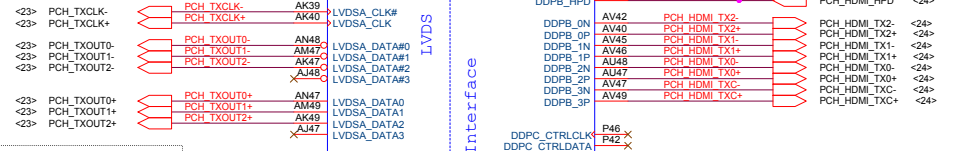
R282 unmount for Vpro SKUs.

support deep S4/S5:  
 "SUSWARN#" 均應做軟件 "SUSWRDNACK"  
 SUSWARN# /SUSWRDNACK/ GPIO30 (Mobile Only):  
 Used by Intel@ME as either SUSWARN#  
 in Deep S4/S5 state supported platforms  
 or as SUSWRDNACK in non Deep S4/S5  
 state supported platforms.

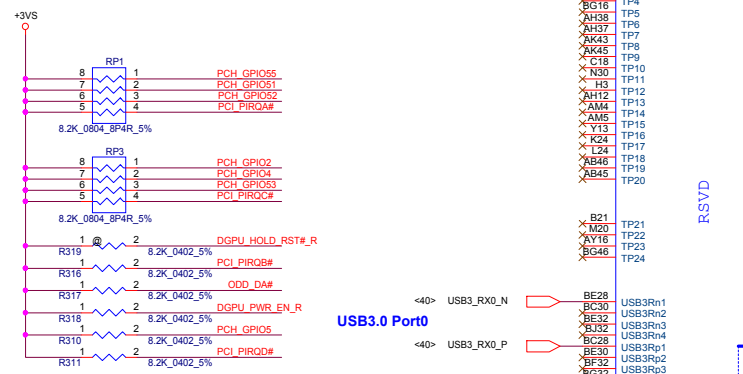
Pull high at LVDS conn side.



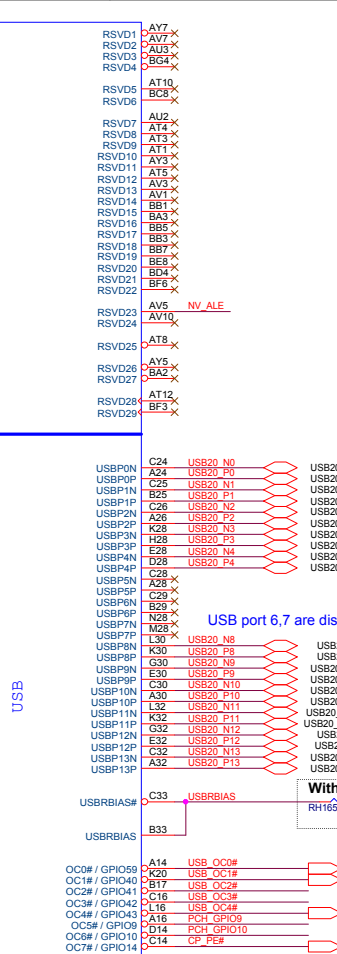
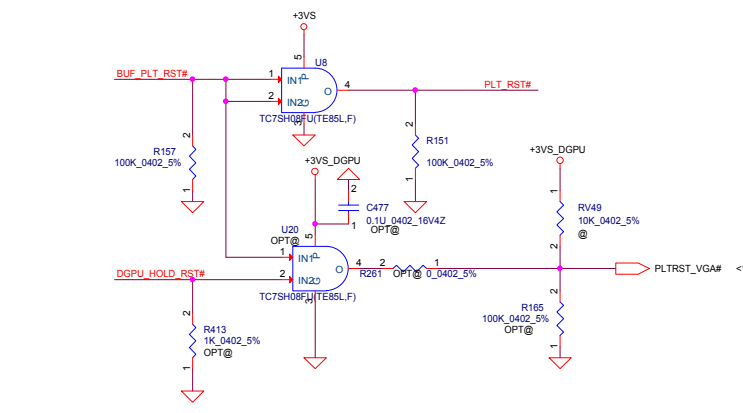
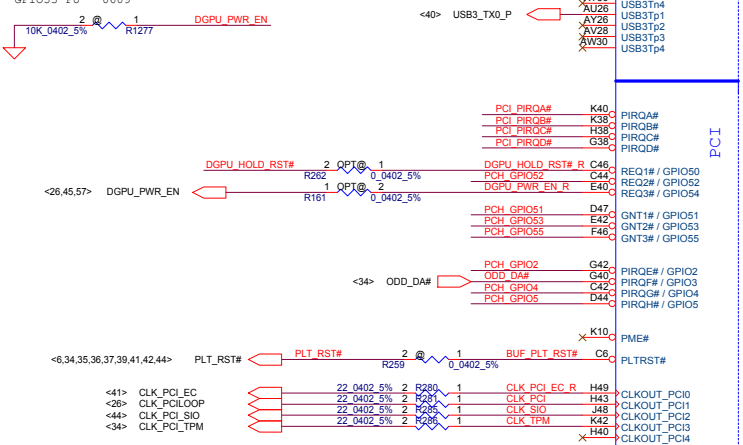
can be left NC when IAMT is not support on the platform



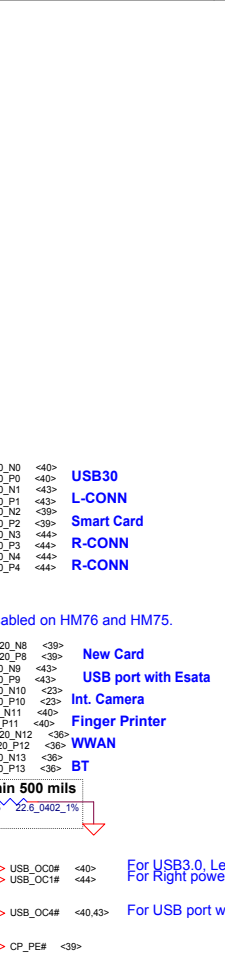
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Issued Date	2011/09/23	Deciphered Date	2012/12/31
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PCH (3/8) DMI, FDI, PM, GFX, DP		Document Number	
QAQ10 LA-851P M/B		Rev 0.1	
Date	Wednesday, November 23, 2011	Sheet	27 of 59



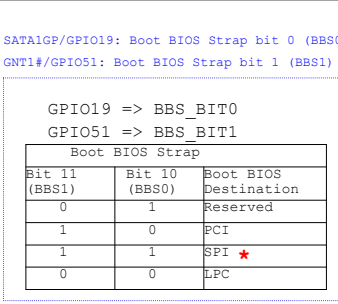
DEL R P5, ADD R316, R317, R318 FOR REMOVE  
 GPIO53 PU---0609



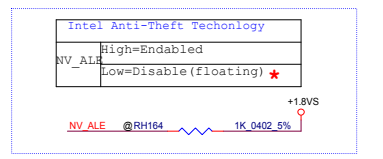
PANTHER-POINT\_FCBGA889



PANTHER-POINT\_FCBGA889



PCB EDS Rev1.5 P99, P98

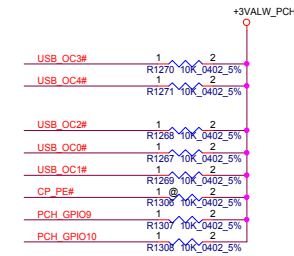


USB port 6,7 are disabled on HM76 and HM75.

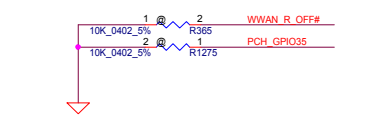
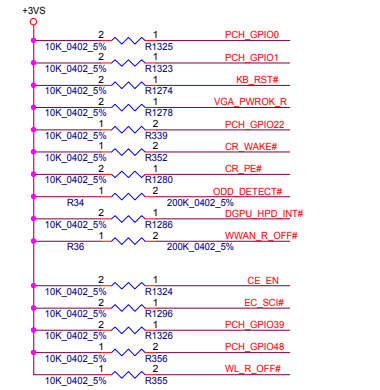
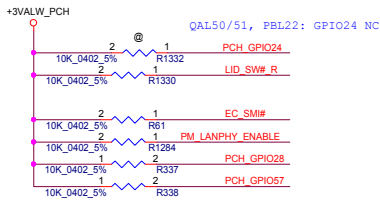


For USB3.0, Left USB.  
 For Right power USB port.

For USB port with eSATA.



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PCH\_GPIO27 (Have internal Pull-High)  
 High: VCCVRM VR Enable  
 Low: VCCVRM VR Disable \*

Can be configured as wake input to allow wakes from Deep Sleep.  
 If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

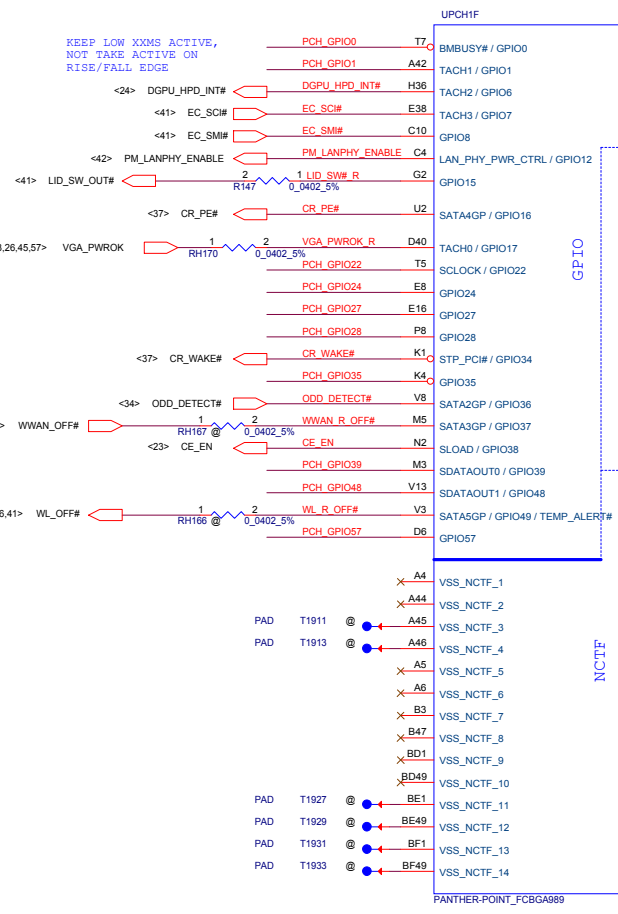


**GPIO28** On-Die PLL Voltage Regulator  
 This signal has a weak internal pull up

\* H: On-Die voltage regulator enable  
 L: On-Die PLL Voltage Regulator disable



KEEP LOW XXMS ACTIVE,  
 NOT TAKE ACTIVE ON  
 RISE/FALL EDGE



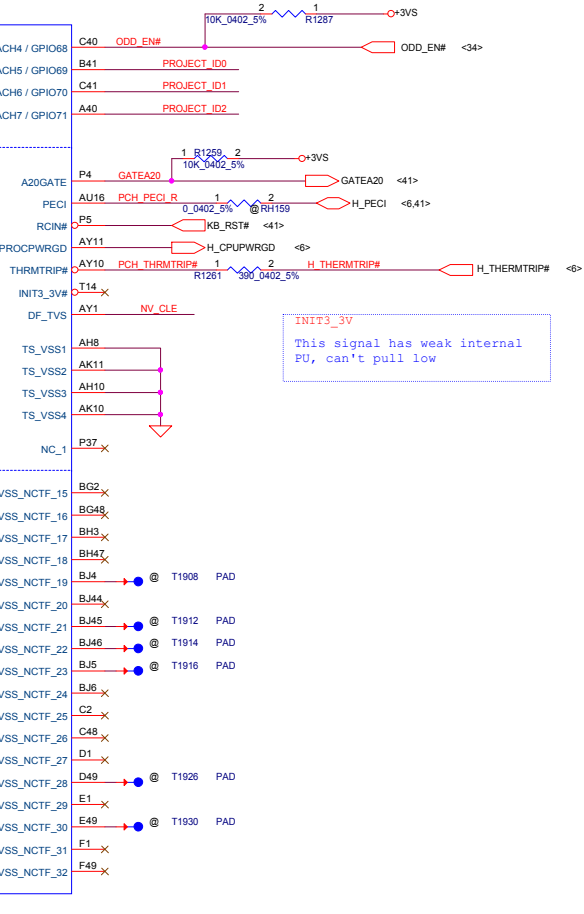
GPIO

NCTF

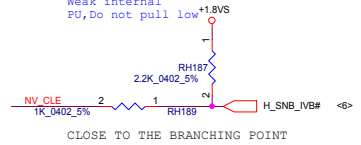
CPU/MISC

PCH\_GPIO28 needs to be connected to XDP\_FN8  
 PCH\_GPIO35 needs to be connected to XDP\_FN9  
 PCH\_GPIO15 needs to be connected to XDP\_FN16

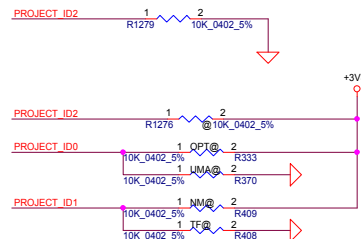
Please refer to Huron River Debug Board DG 1.2



DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW



Weak internal PU, Do not pull low



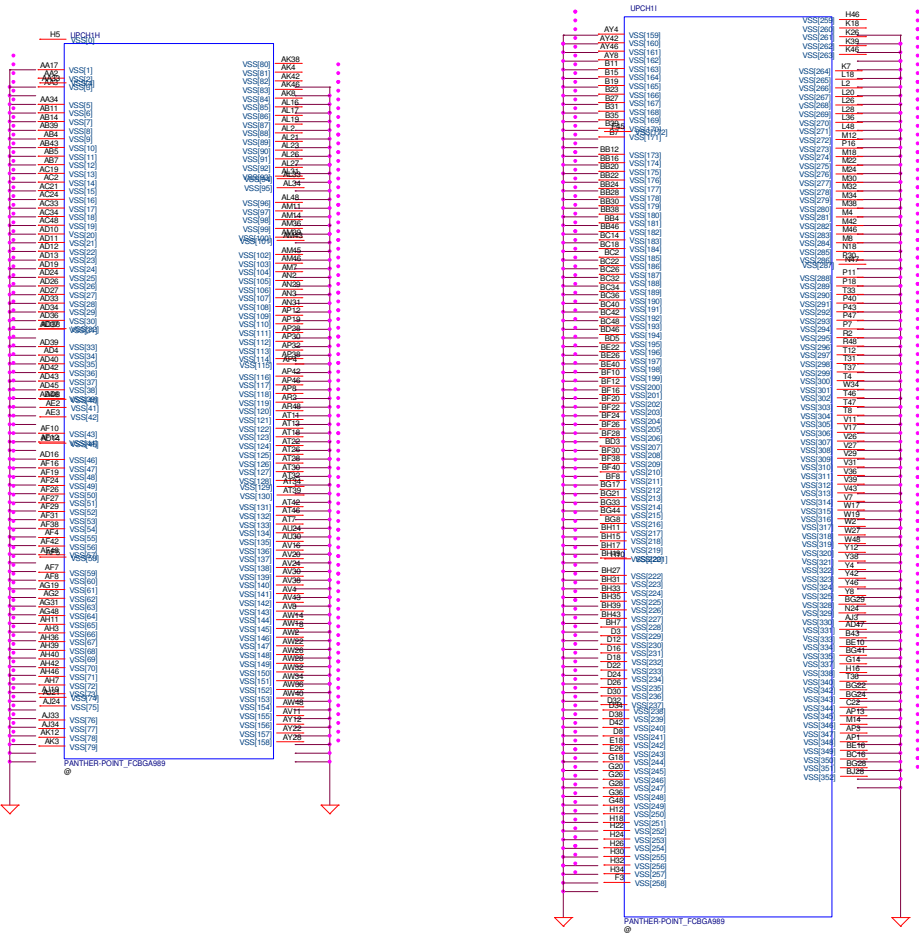
	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
QAQ10 (UMA)	0	0	0
QAQ11 (Optimus)	0	0	1
QAQ12 (UMA)	0	1	0
QAQ13 (Optimus)	0	1	1
QAT10 (UMA)	1	0	0
QAQ11 (Optimus)	1	0	1

For TongFang: QAQ10 (UMA) / QAQ11 (Optimus)  
 For 030: QAQ12 (UMA) / QAQ13 (Optimus)  
 No Vpro-project code

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Date:	Wednesday, November 23, 2011	Sheet	29	of 59

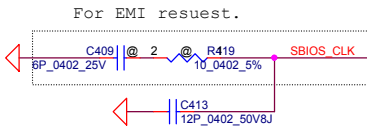
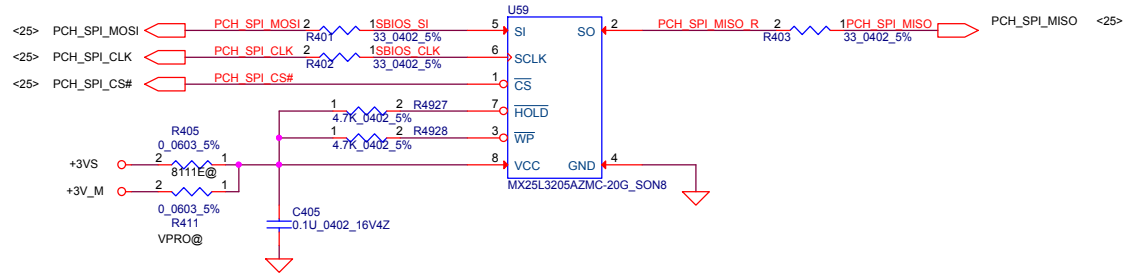






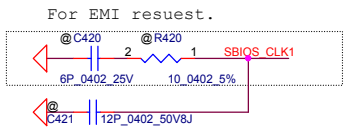
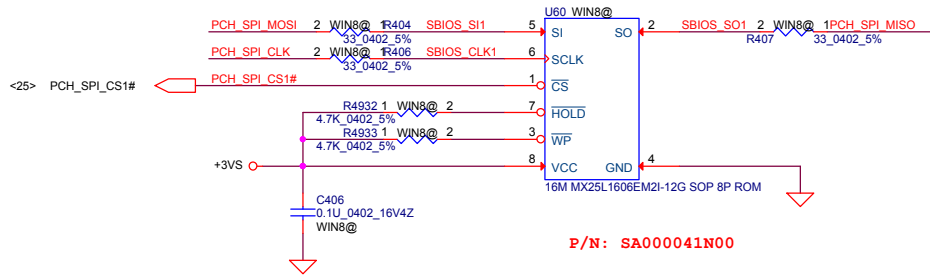


# SBIOS SPI Flash



**U59:**  
**Vpro--SA000039A00 8MB**  
**non-Vpro--SA00003K80 4MB**

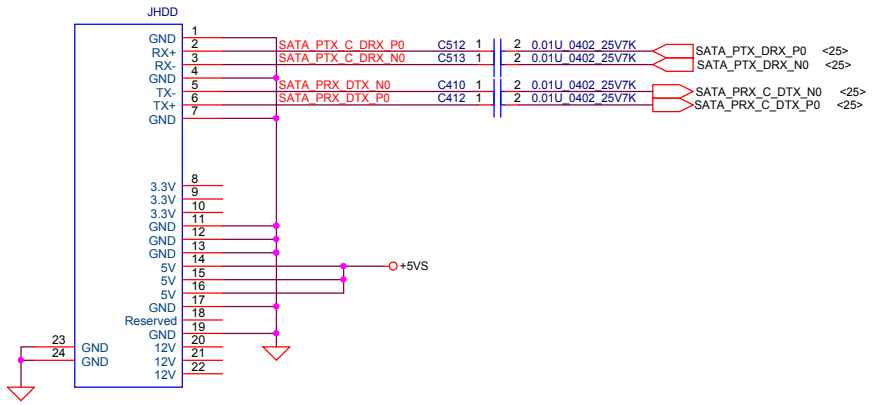
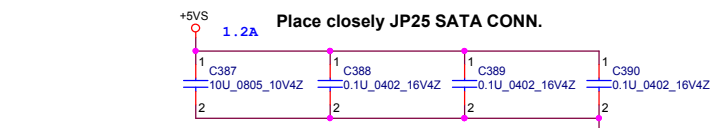
# BIOS SPI Flash (2MByte\*1) For Win8



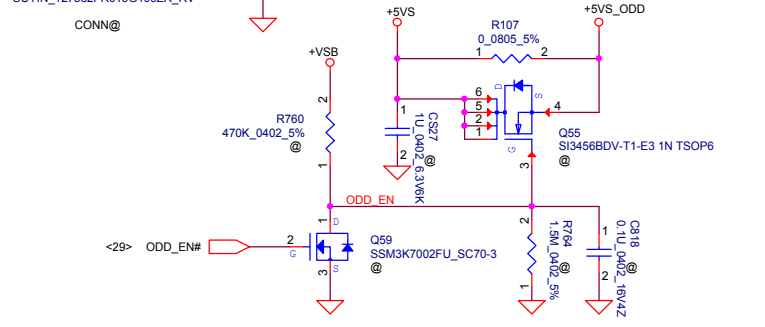
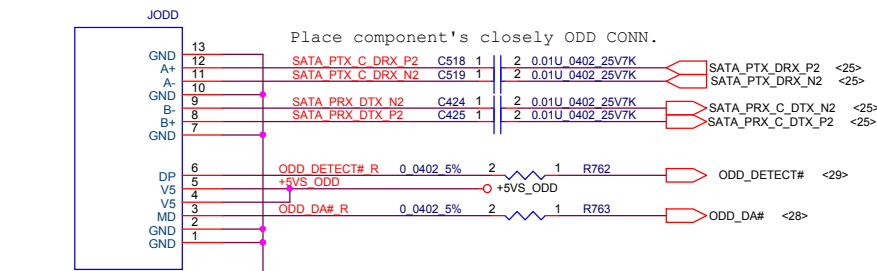
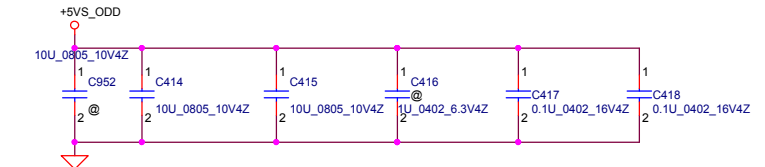
**P/N: SA000041N00**

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Issued Date	2011/09/23	Deciphered Date	2011/12/30		
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				<b>QAQ10 LA-8581P M/B</b>	
				Date:	Wednesday, November 23, 2011   Sheet 33 of 59   Rev 0.1

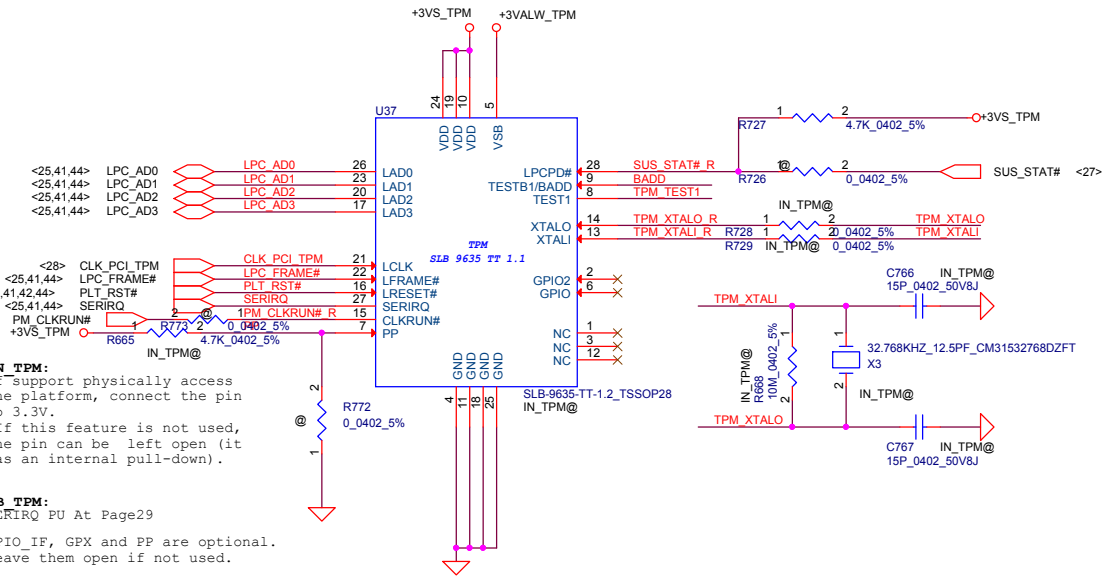
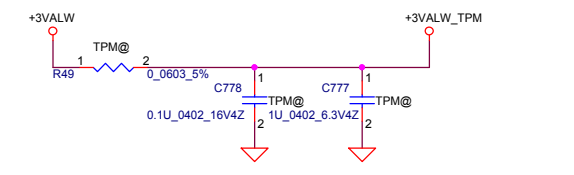
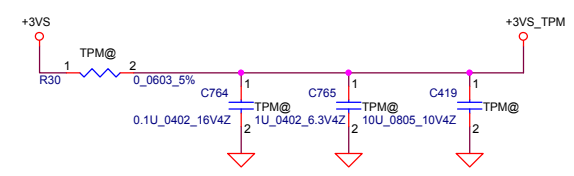
# SATA HDD Conn.



# SATA ODD Conn

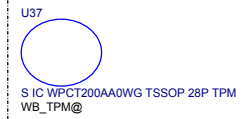


# TPM 1.2

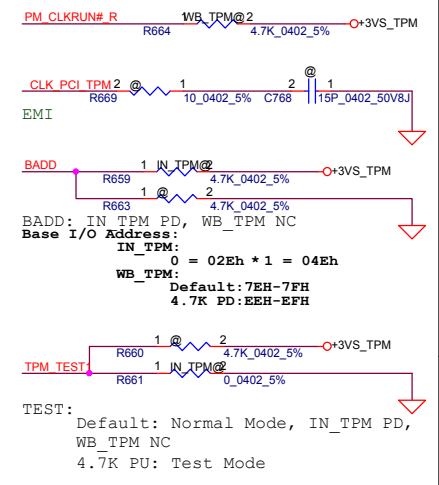


**IN TPM:**  
 If support physically access the platform, connect the pin to 3.3V.  
 If this feature is not used, the pin can be left open (it has an internal pull-down).

**WB TPM:**  
 SERIRQ PU At Page29  
 GPIO IF, GPX and PP are optional. Leave them open if not used.



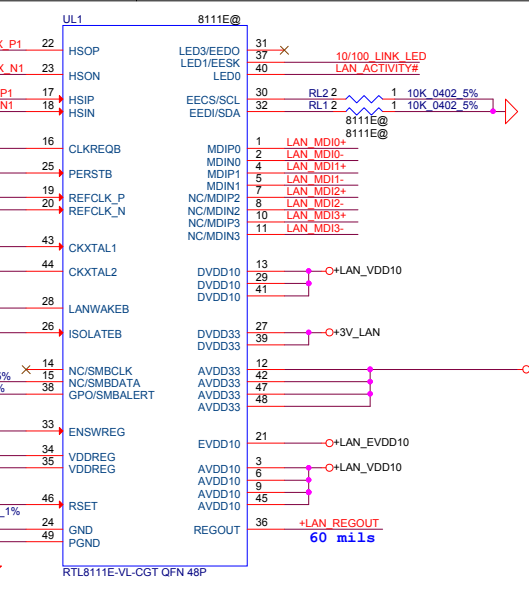
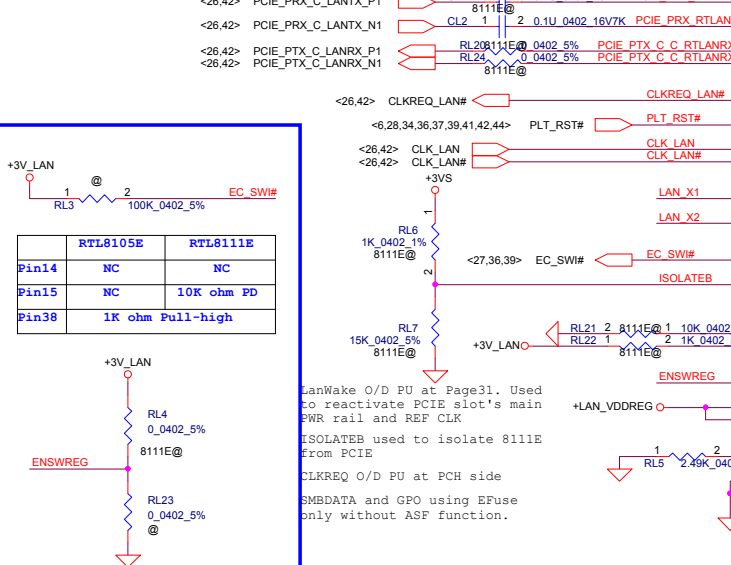
**BOM**  
 IN\_TPM: IN\_TPM@&TPM@  
 WB\_TPM: WB\_TPM@&TPM@  
 For NON\_TPM SKU Reserve



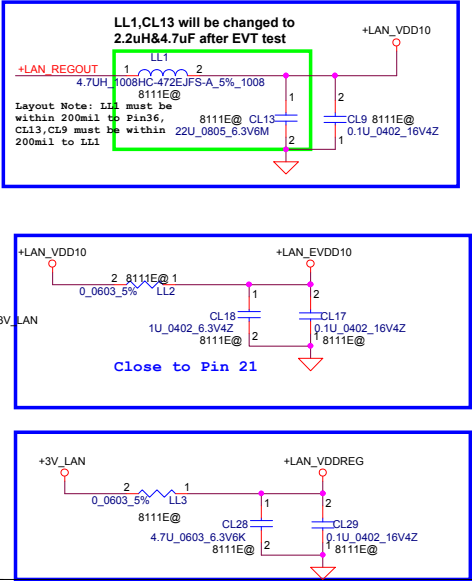
TEST: Default: Normal Mode, IN\_TPM PD, WB TPM NC  
 4.7K PU: Test Mode

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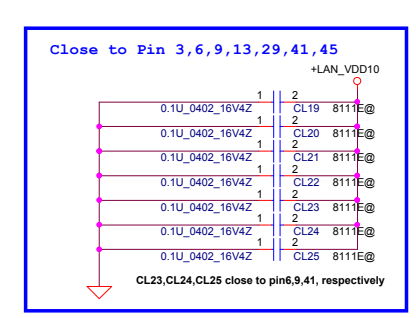
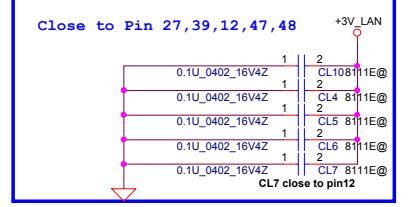
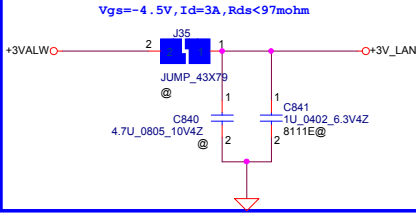
# IC function Part



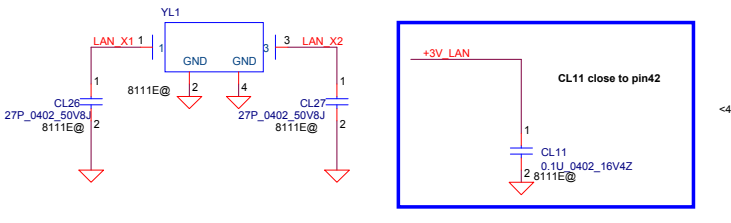
# PWR



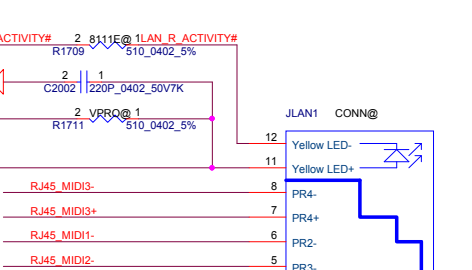
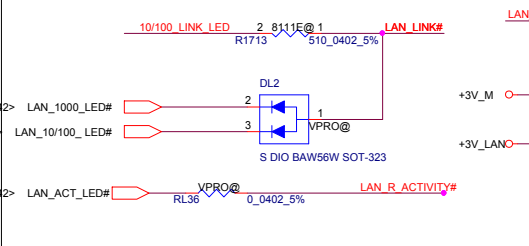
# +3VALW TO +3V\_LAN



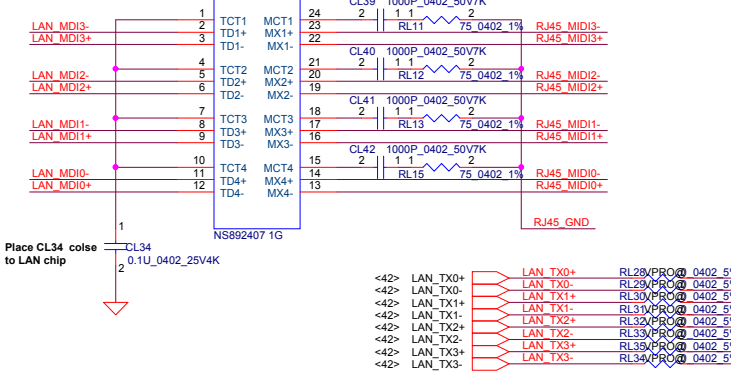
# Crystal



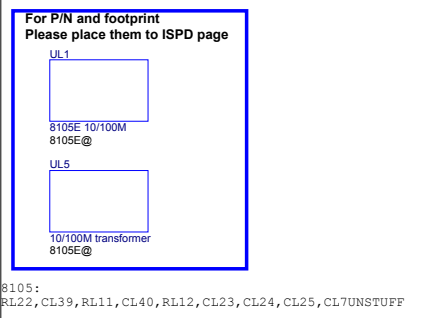
# LAN Conn.



# Transformer

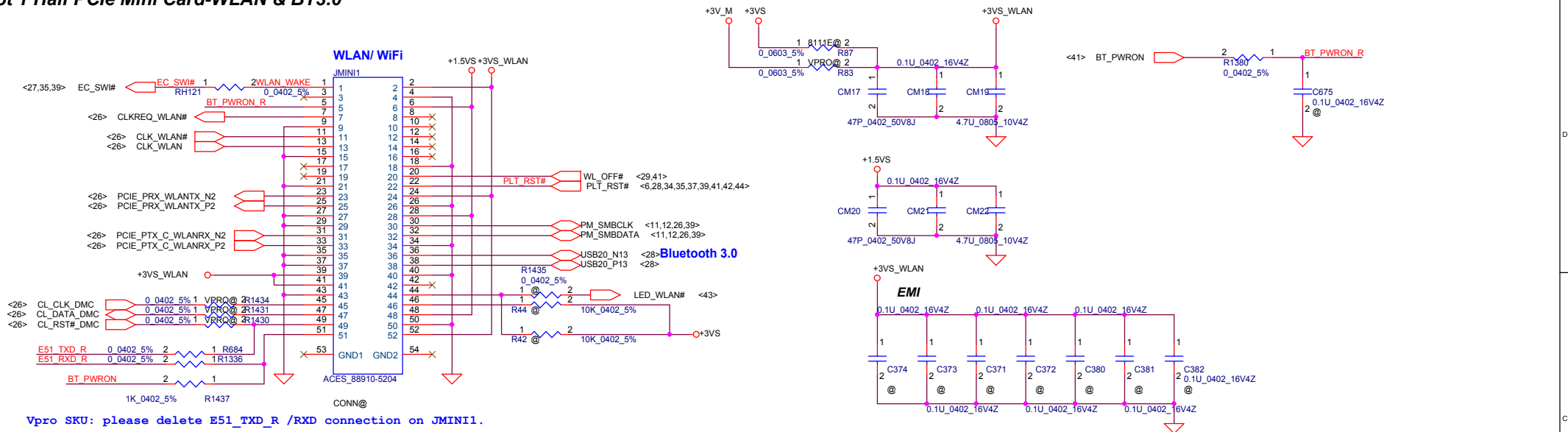


# BOM Structure

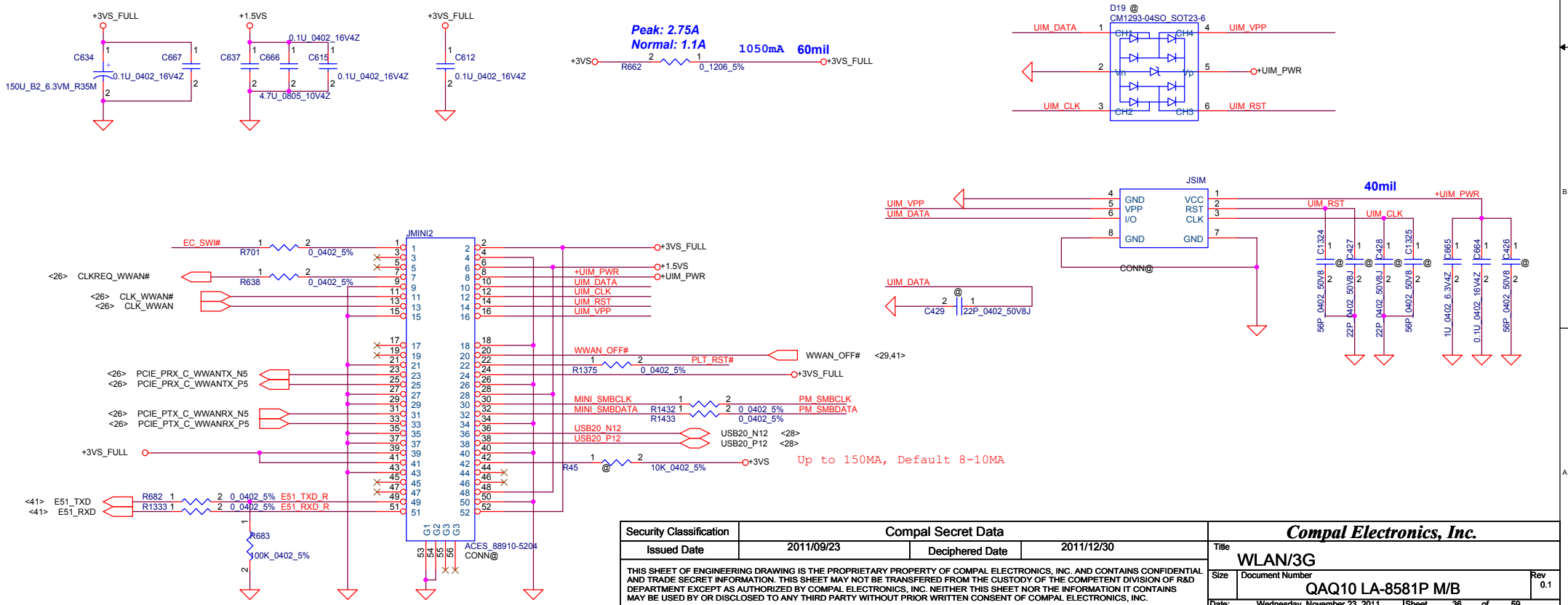


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Title	PCIe-LAN-RTL8105E/8111E		
Size	Document Number	Rev	
Custom	QAQ10 LA-8581P M/B		0.1
Date:	Wednesday, November 23, 2011	Sheet	35 of 59

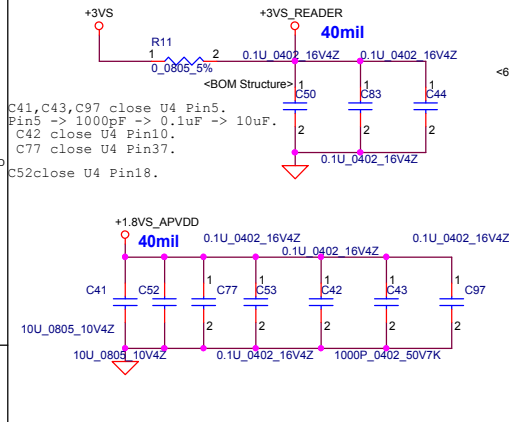
# Slot 1 Half PCIe Mini Card-WLAN & BT3.0



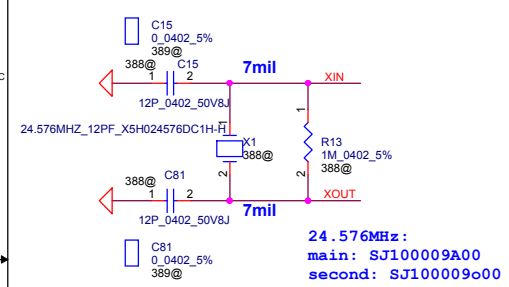
# Slot 2 Half PCIe Mini Card-G/GPS (FULL Card)



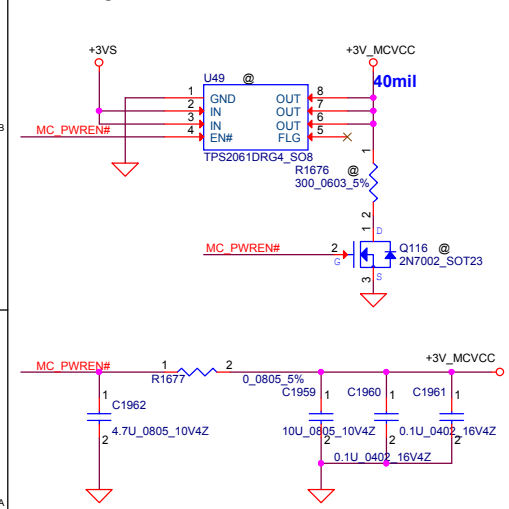
# IC PWR



# External Crystal

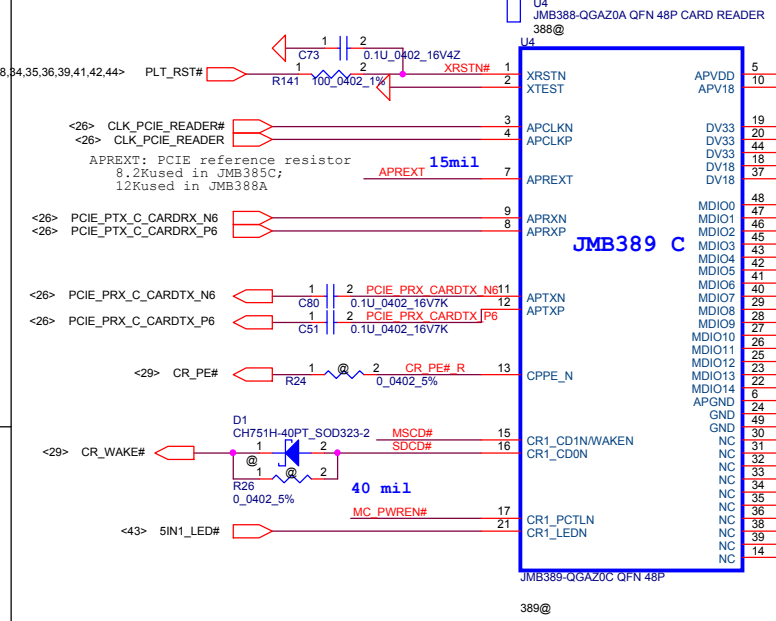


# Memory Card Power



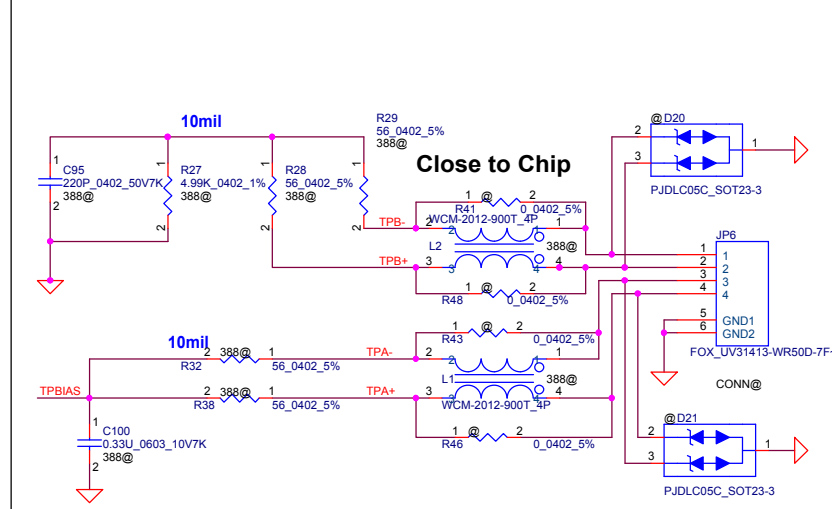
Note:  
if use external PWR and change +3V MCPWR as control signal, Need BIOS to change the Setting.

# IC Function Part

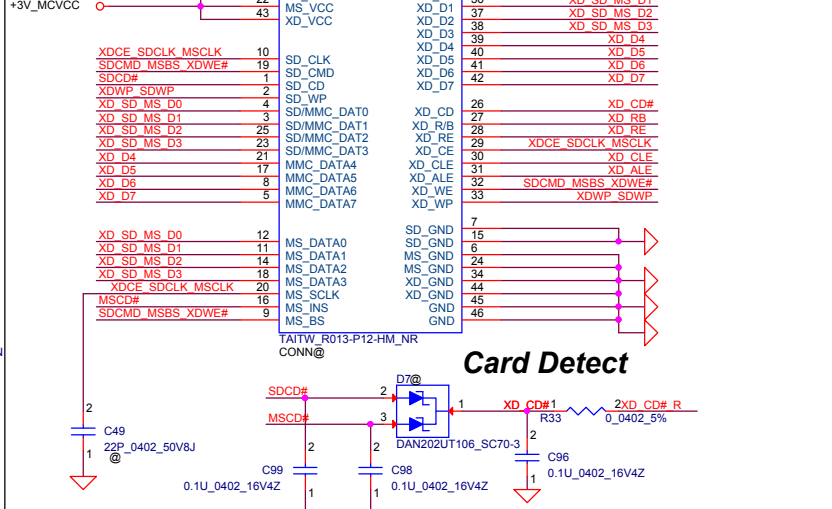


Note:  
Colay With JMB385; W/1394, mount JMB388;WO/1394, mount JMB385.  
CR\_PE# and CR\_WAKE reserve for D3 mode

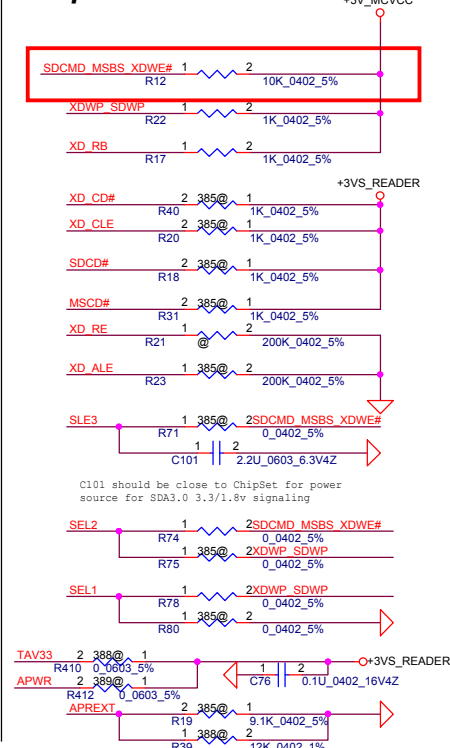
# 1394 Conn



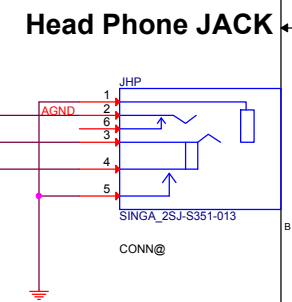
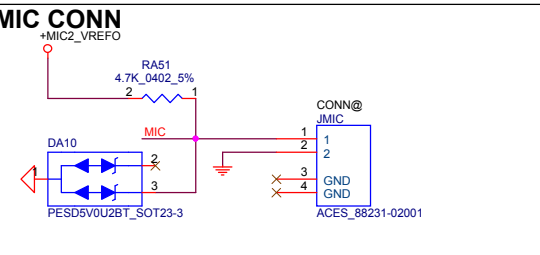
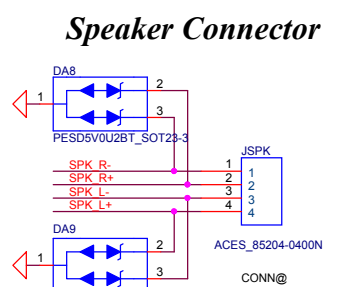
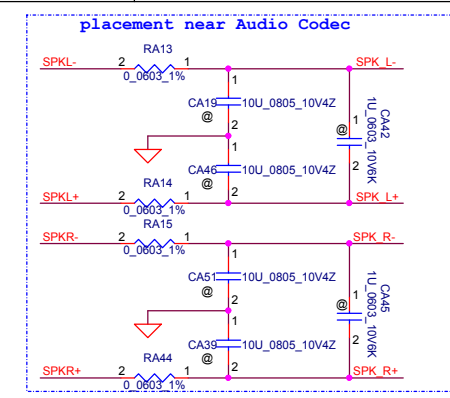
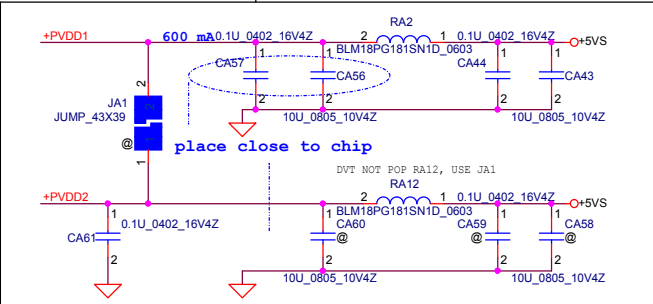
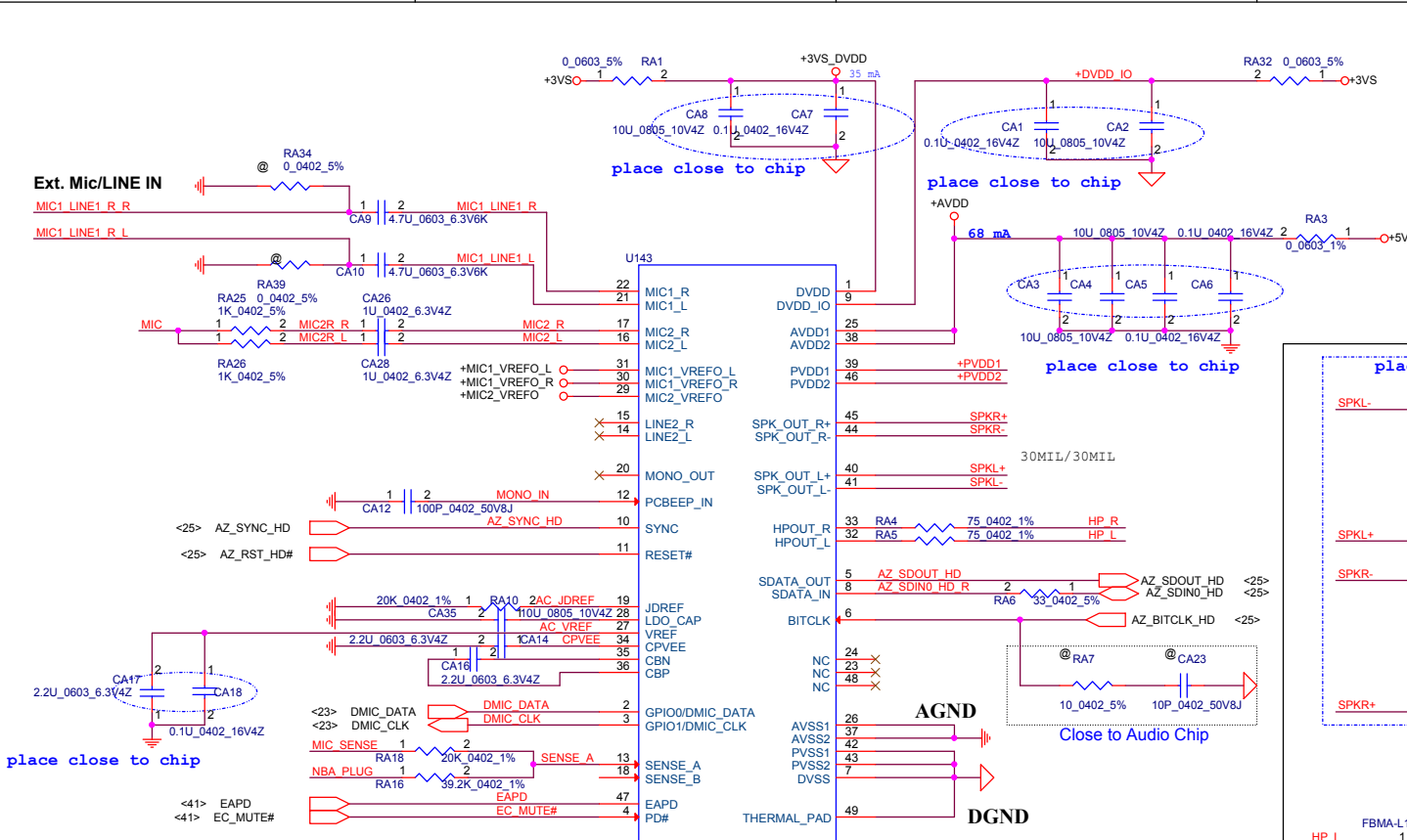
# 7 IN 1 Conn



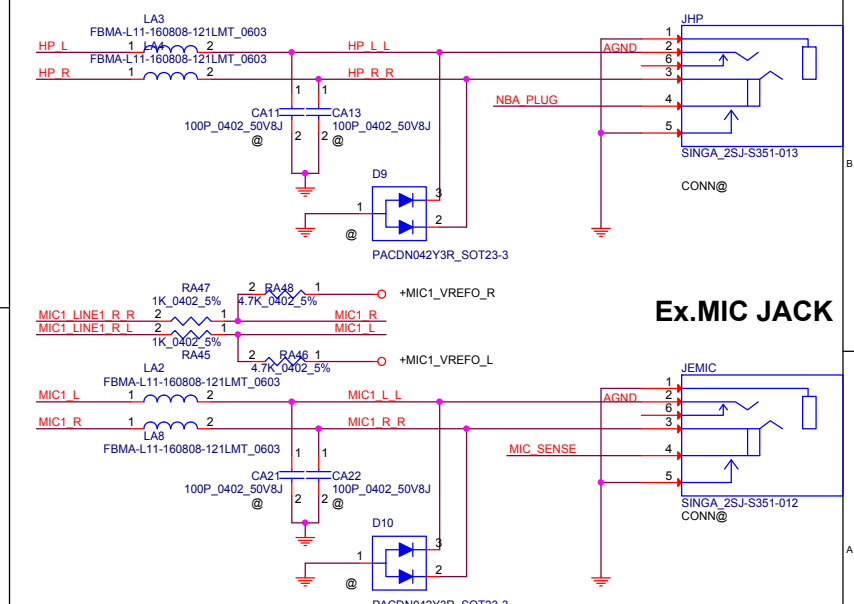
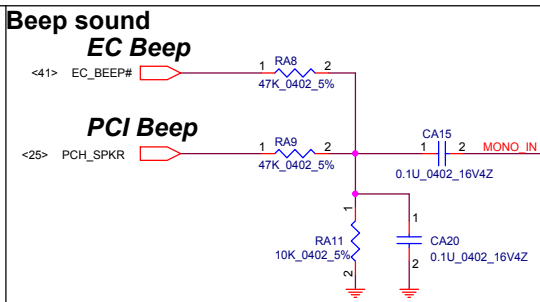
# Strap Pin Definition



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Card Reader			Size	Document Number
			QAQ10 LA-8581P M/B	
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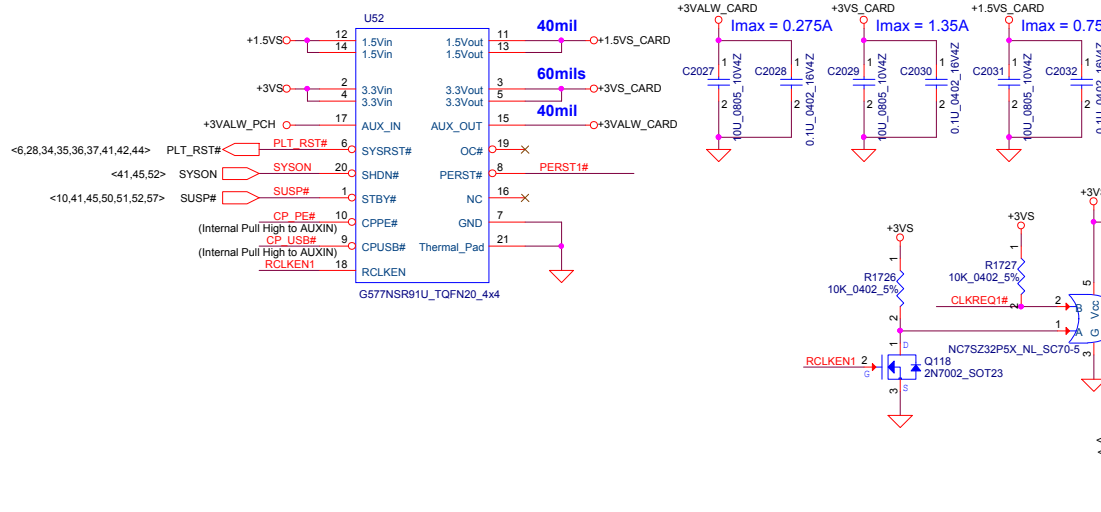


Sense Pin	Impedance	Codec Signals	Function
	39.2K	PORT-A (PIN 39, 41)	Headphone out
SENSE A	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	

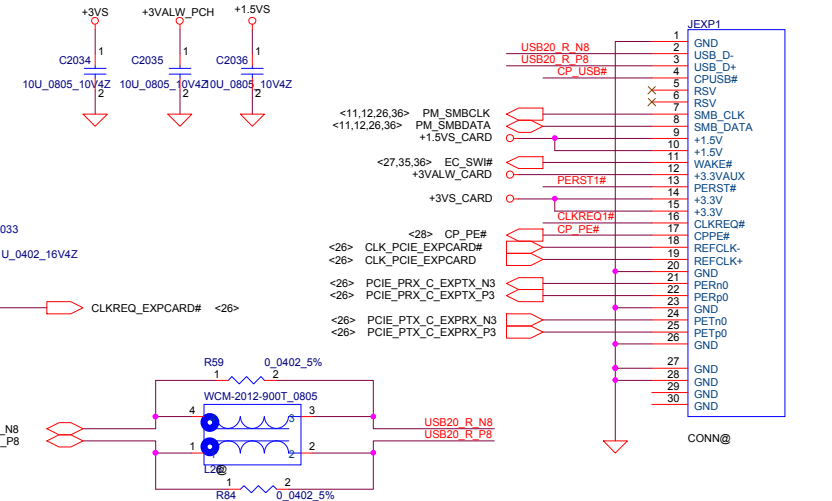


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				QAQ10 LA-8581P M/B	
				Date:	Wednesday, November 23, 2011
				Sheet	38 of 59

PWR Switch

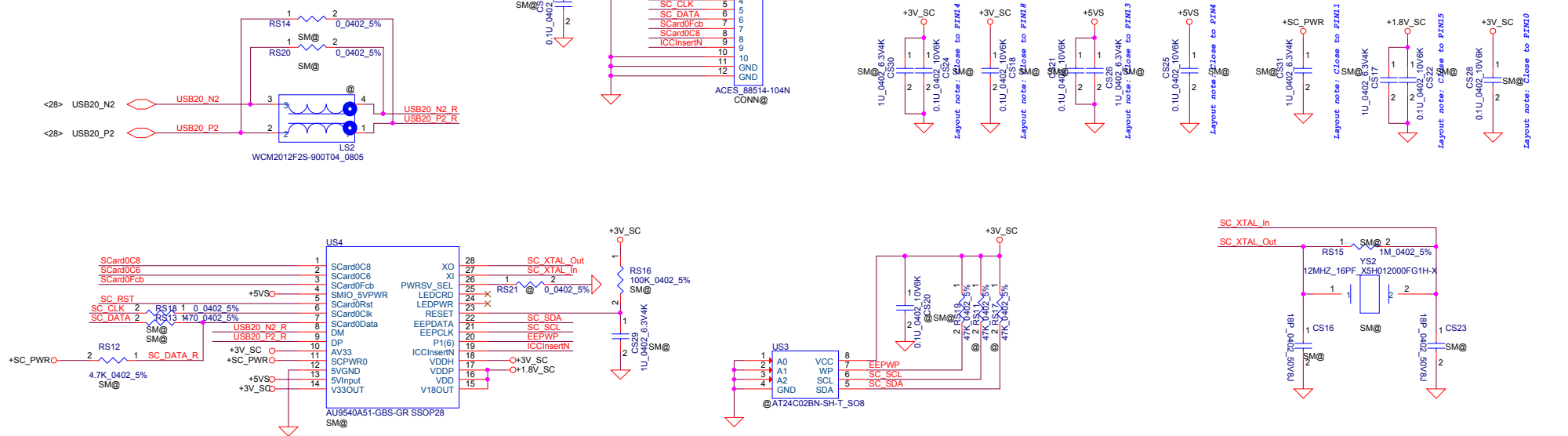


New Card Socket (Left/TOP)



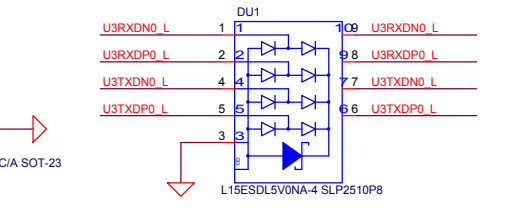
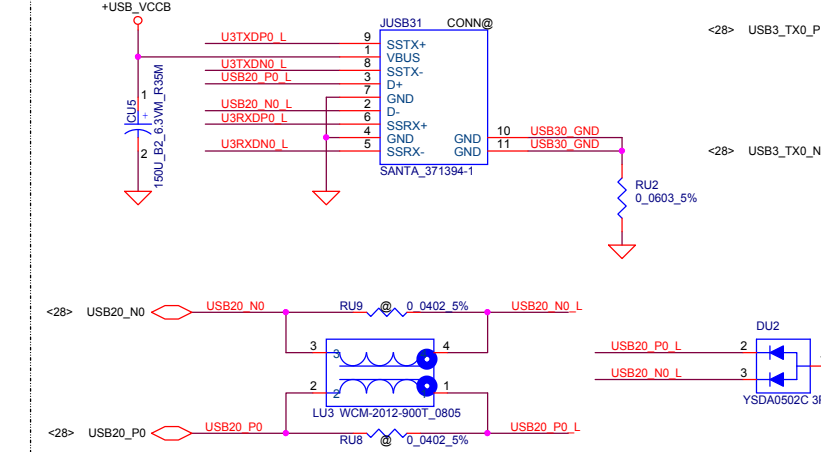
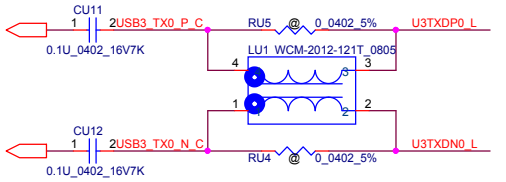
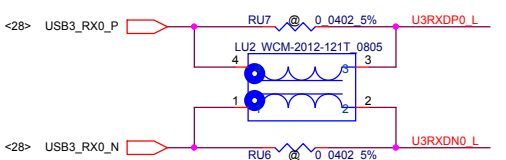
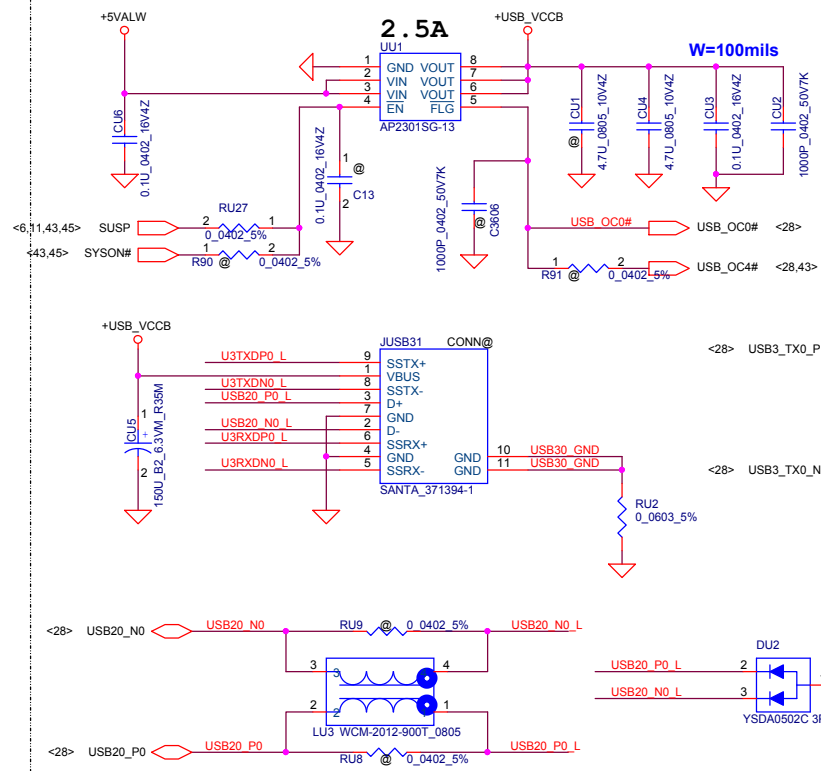
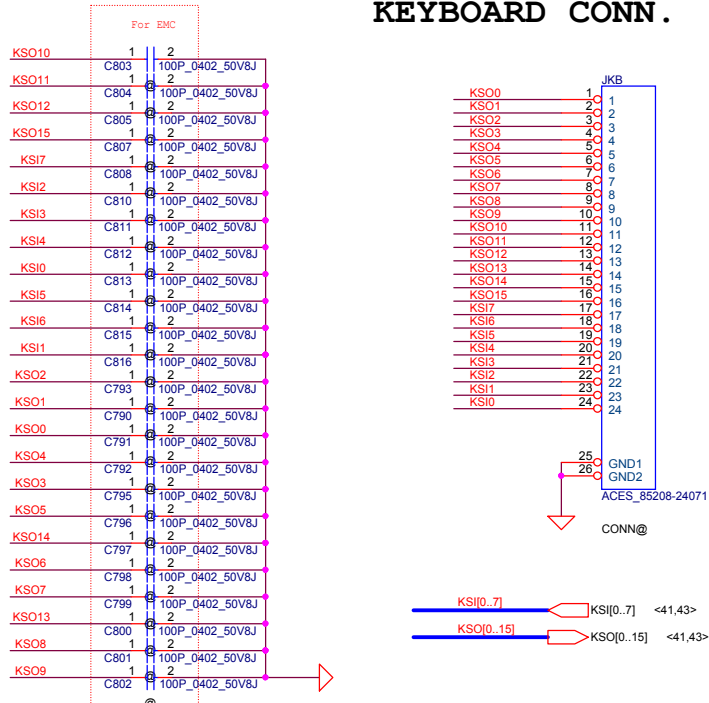
This pin1 define need check

Smart Card

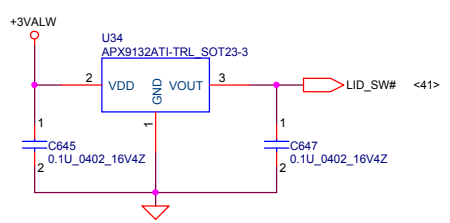


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Issued Date	2011/09/23	Deciphered Date			
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			QAQ10 LA-8581P M/B		Rev 0.1
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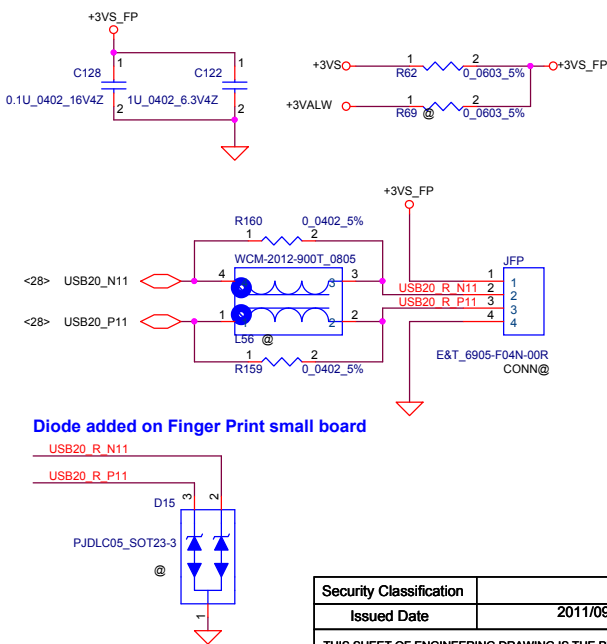
# KEYBOARD CONN.



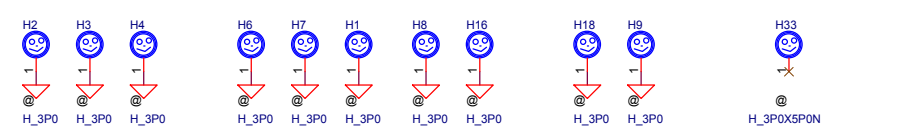
## Lid SW



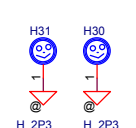
## Finger Print



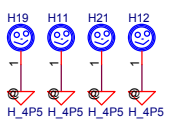
## Screw Hole



## Break hole



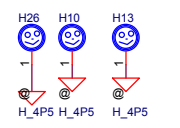
## CPU



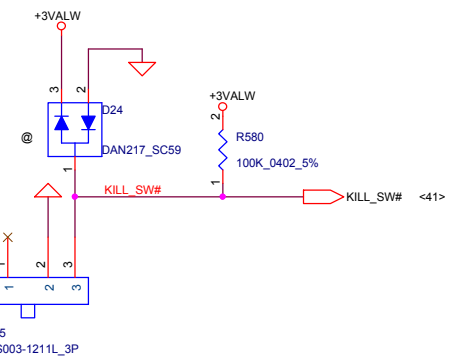
## JWLAN



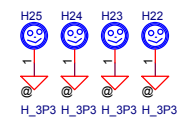
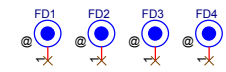
## VGA



## Kill Switch

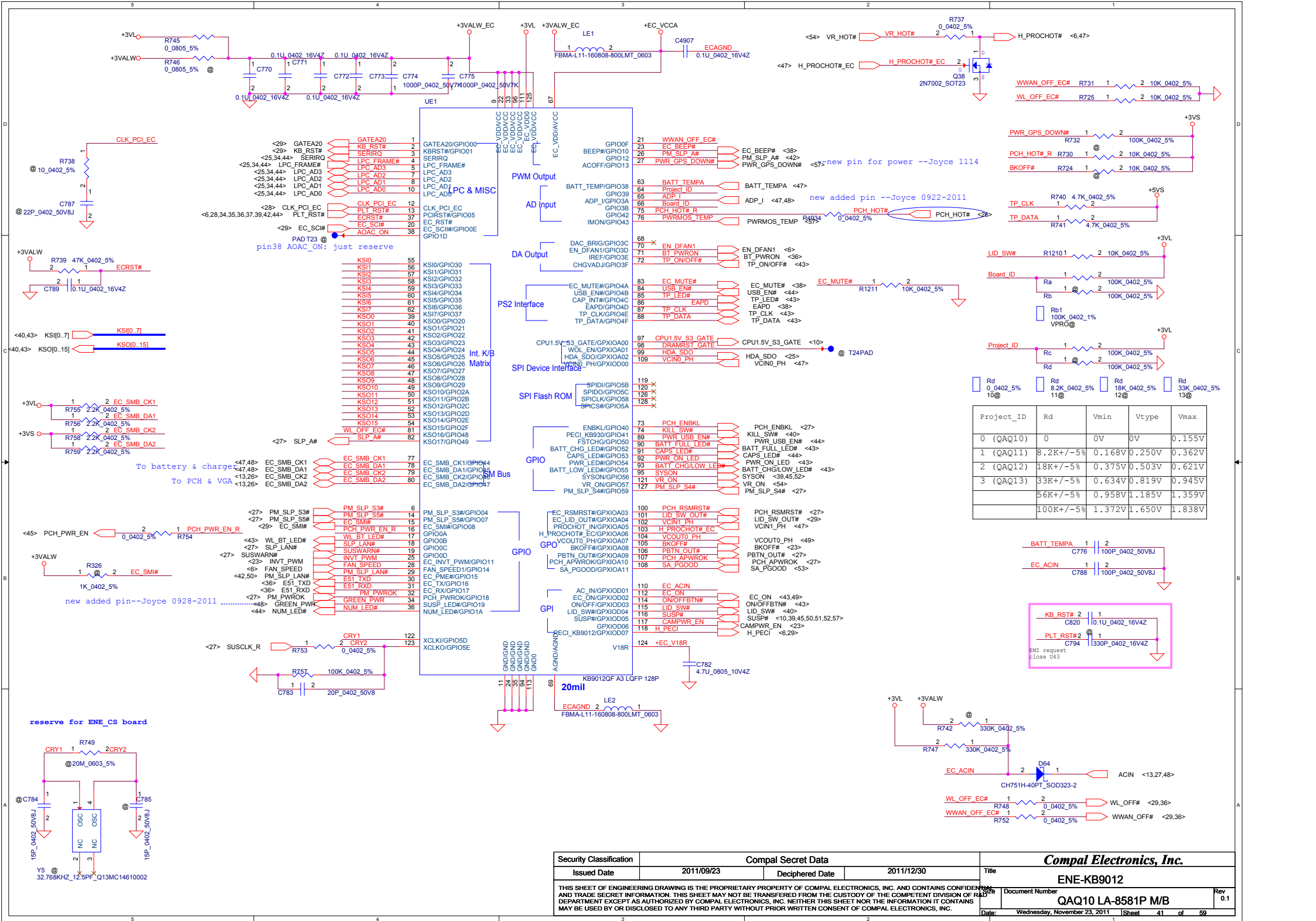


## PCB Fiducial Mark PAD



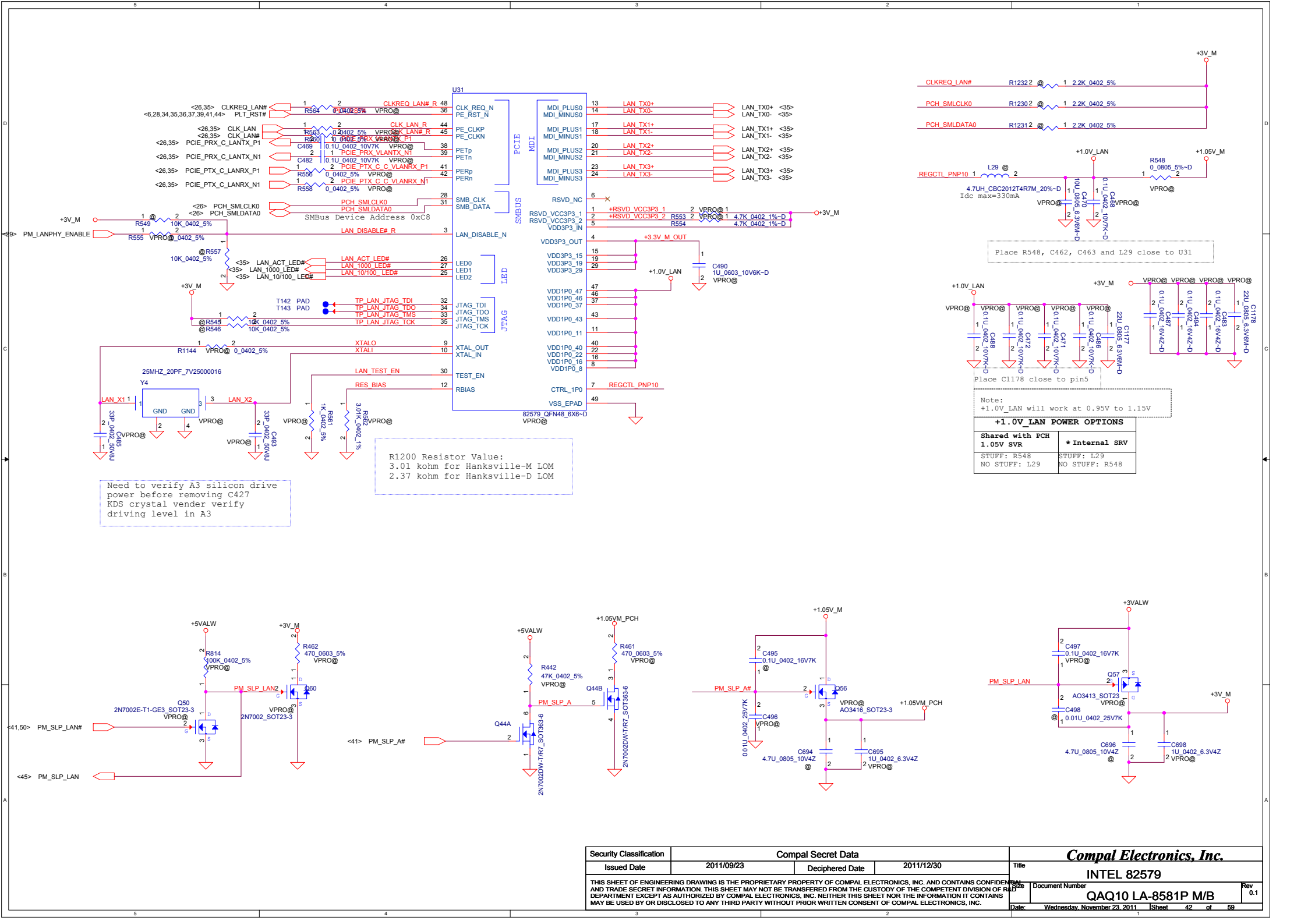
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/09/23	Deciphered Date	2011/12/30	Title	
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Project_ID	Rd	Vmin	Vtype	Vmax
0 (QAQ10)	0	0V	0V	0.155V
1 (QAQ11)	8.2K+/-5%	0.168V	0.250V	0.362V
2 (QAQ12)	18K+/-5%	0.375V	0.503V	0.621V
3 (QAQ13)	33K+/-5%	0.634V	0.819V	0.945V
	56K+/-5%	0.958V	1.185V	1.359V
	100K+/-5%	1.372V	1.650V	1.838V

Security Classification	Compal Secret Data		2011/12/30		Title	
2011/09/23	Deciphered Date	2011/12/30	2011/12/30		ENE-KB9012	
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Date: Wednesday, November 23, 2011 1 Sheet 41 of 59						



Need to verify A3 silicon drive power before removing C427  
KDS crystal vender verify driving level in A3

R1200 Resistor Value:  
3.01 kohm for Hanksville-M LOM  
2.37 kohm for Hanksville-D LOM

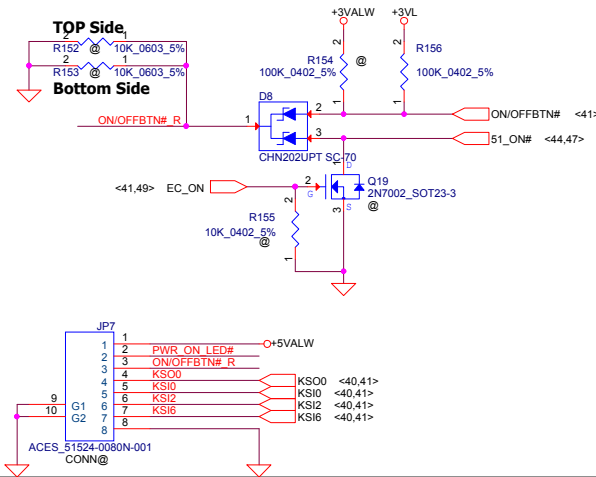
Place R548, C462, C463 and L29 close to U31

Note:  
+1.0V\_LAN will work at 0.95V to 1.15V

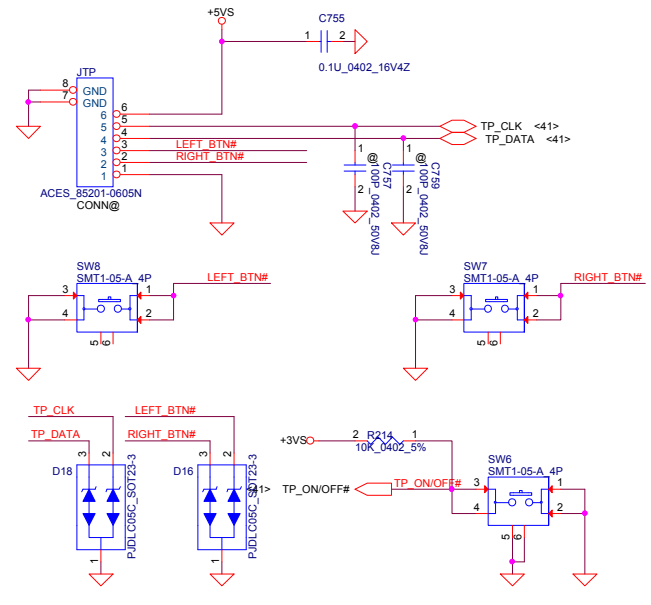
+1.0V LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548

Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2011/09/23	Deciphered Date	2011/12/30	INTEL 82579		Rev
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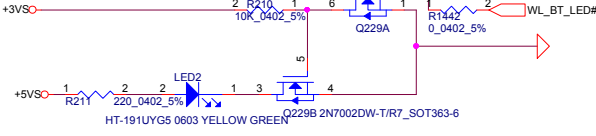
# Power Button/ PWR/B



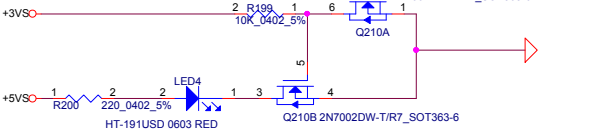
# Touch/B Connector



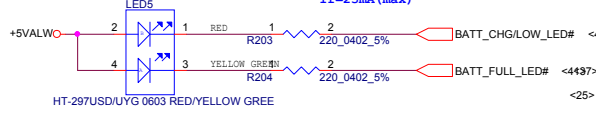
# WL&BT LED



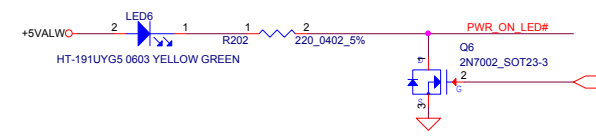
# HDD LED



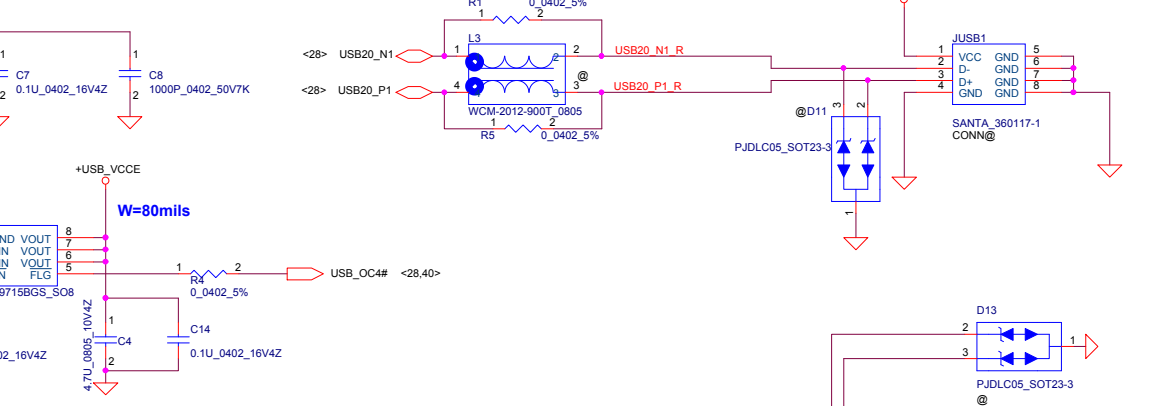
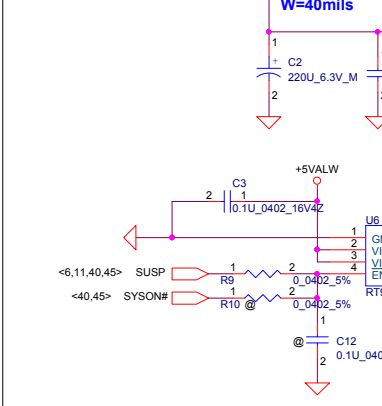
# BATT CHARGE/FULL LED



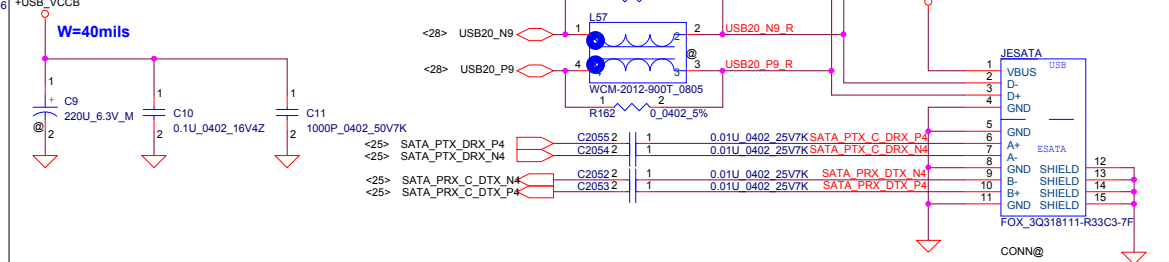
# PWR ON LED



# Left USB



# ESATA

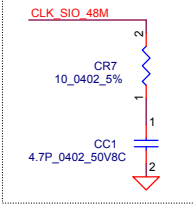


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Issued Date	2011/09/23	Deciphered Date	2011/12/30	PWR/TP/LED	
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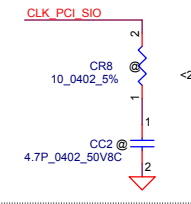
# EMI And ESD

Reserve R199,C207,R226,C208 <EMI> 0601

Place closely pin 18

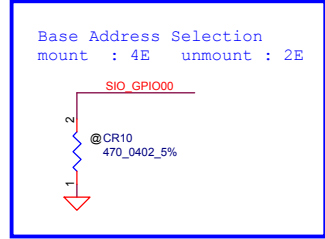
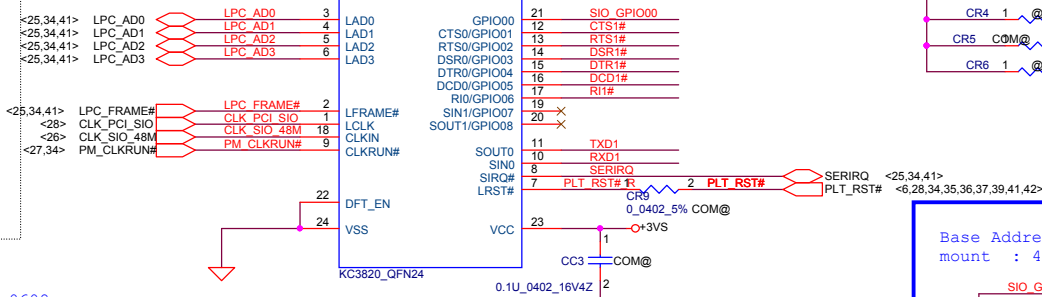
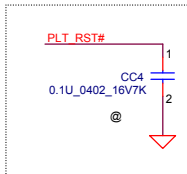


Place closely pin 1

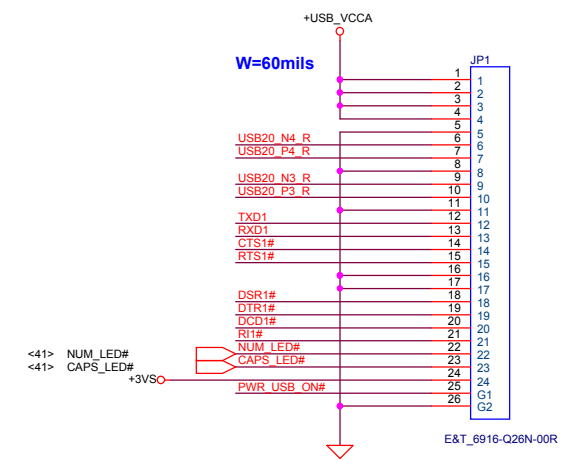
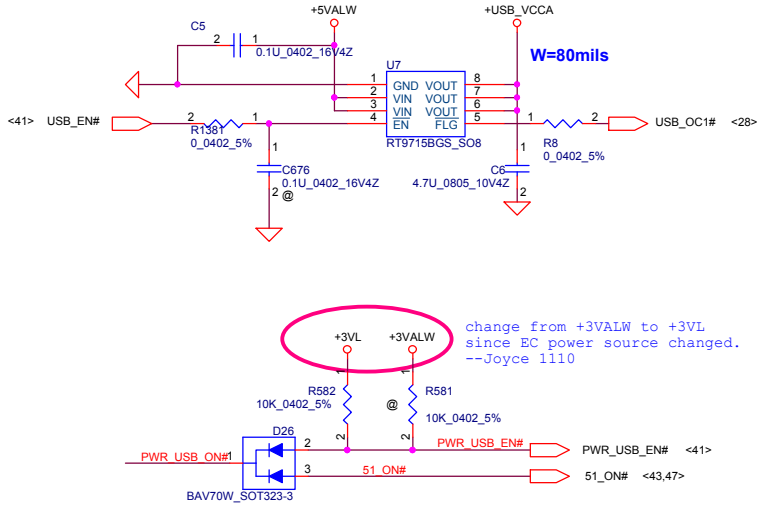
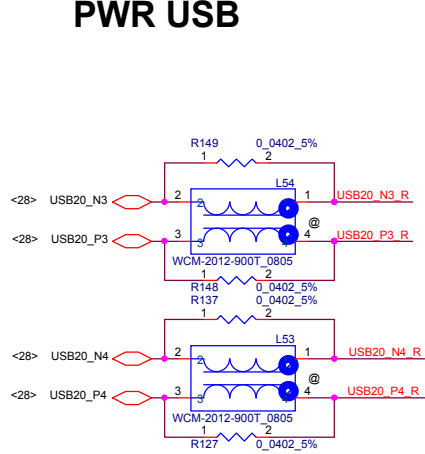


Add CR7,CC1 for EMI test fail issue--0929-2011

Reserve C292 for SIO\_RST# <ESD> 0608



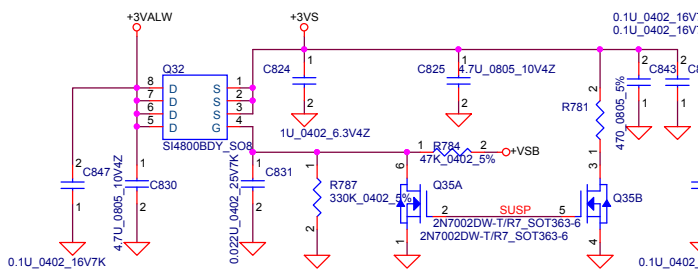
# PWR USB



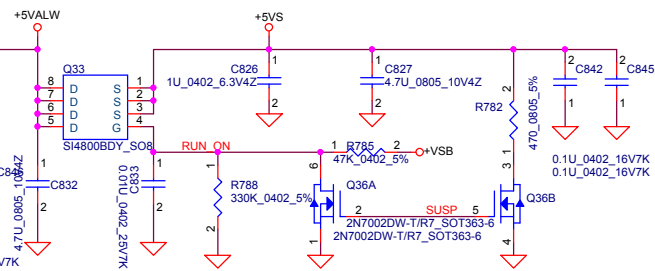
Security Classification		Compal Secret Data		Title	
Issued Date	2011/09/23	Deciphered Date	2011/12/30	POWER USB / COM	
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**+3VALW TO +3VS**

Vgs=0V, Id=9A, Rds=18.5mohm

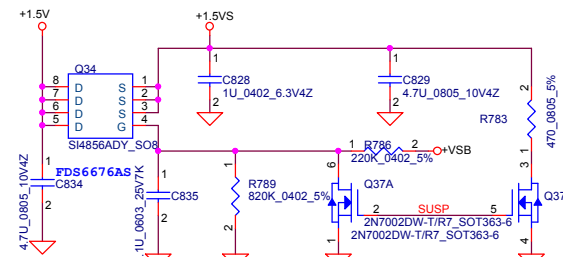


**+5VALW TO +5VS**

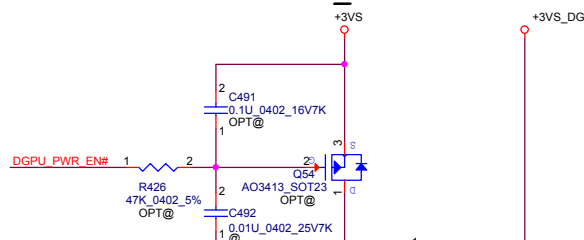


**+1.5V to +1.5VS**

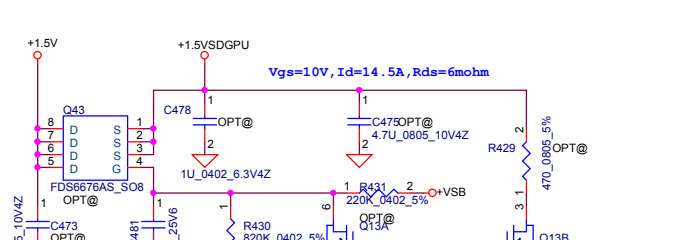
Vgs=10V, Id=14.5A, Rds=6mohm



**+3VS to +3VS\_DGPU**

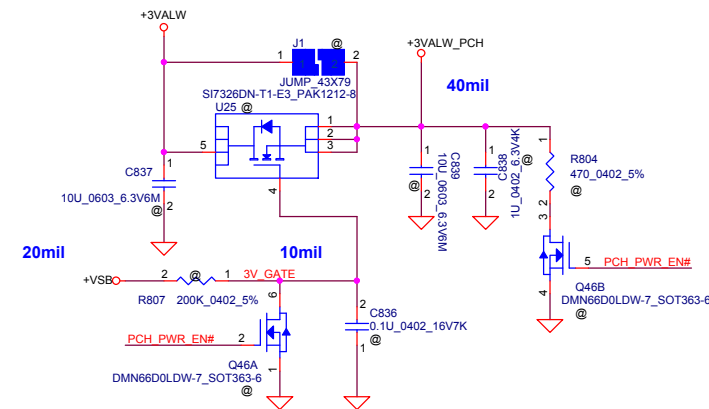


**+1.5V to +1.5VSDGPU**

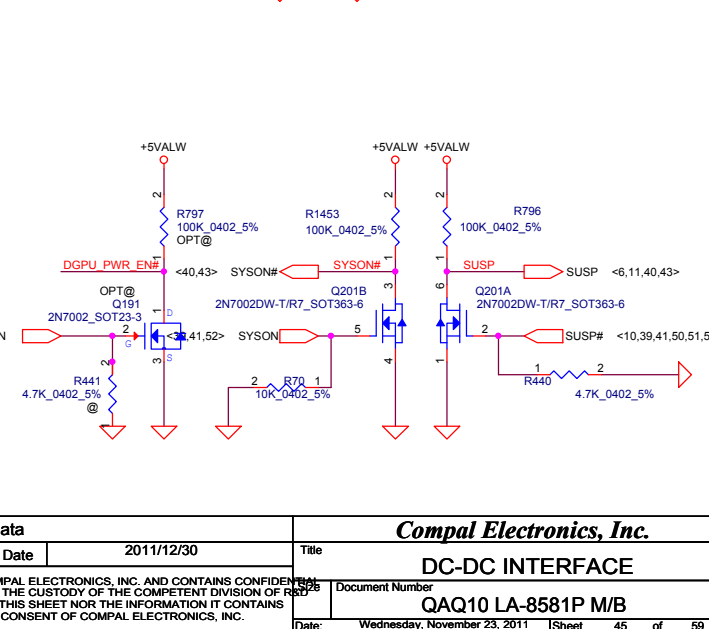
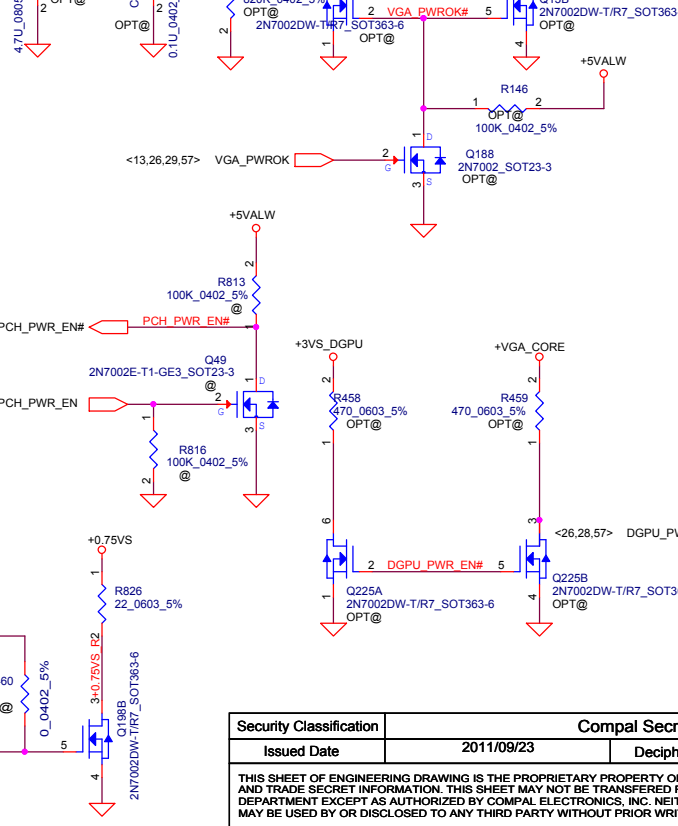
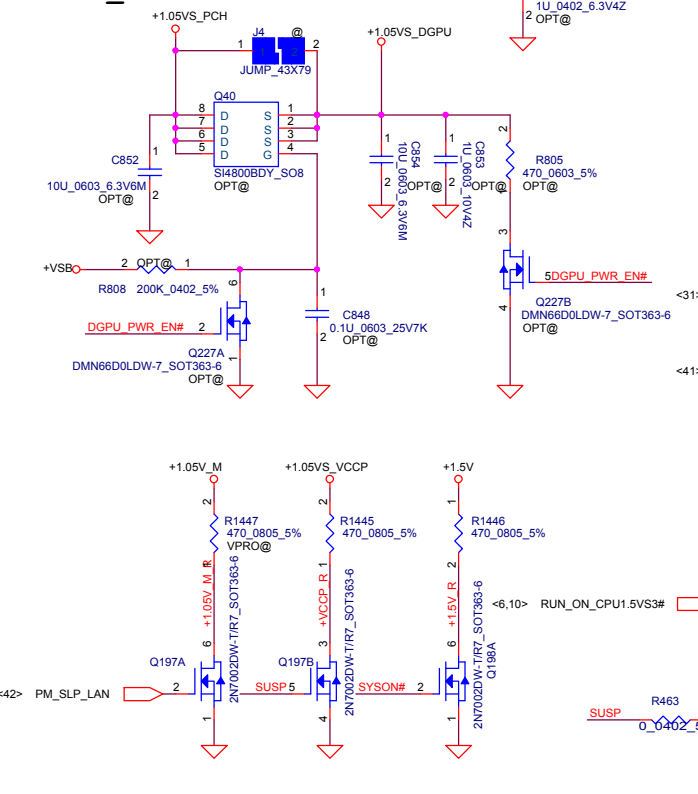


**+3VALW TO +3VALW(PCH AUX Power)**

Short J1 for PCH VCCSUS3.3

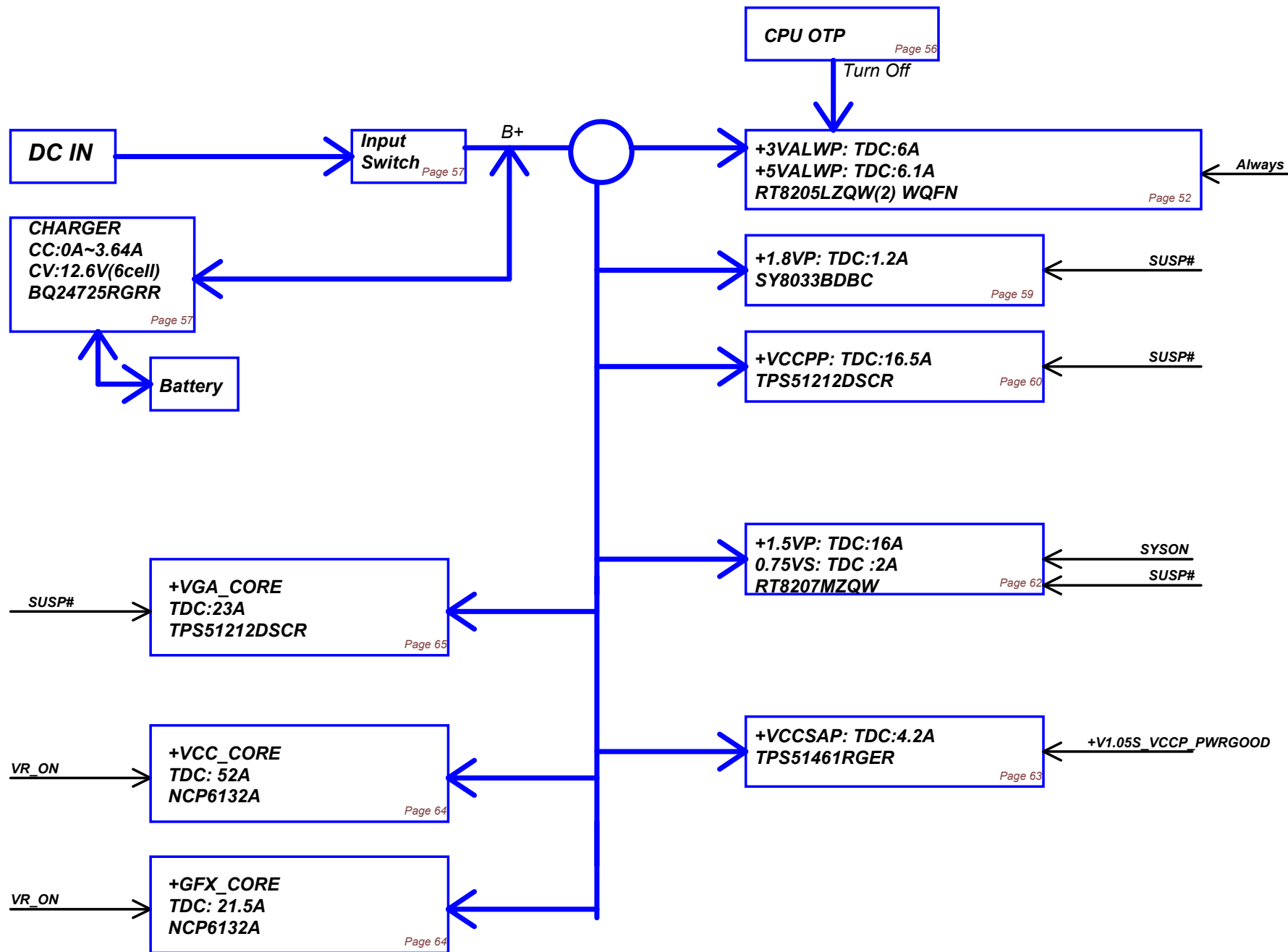


**+1.05VS\_DGPU**



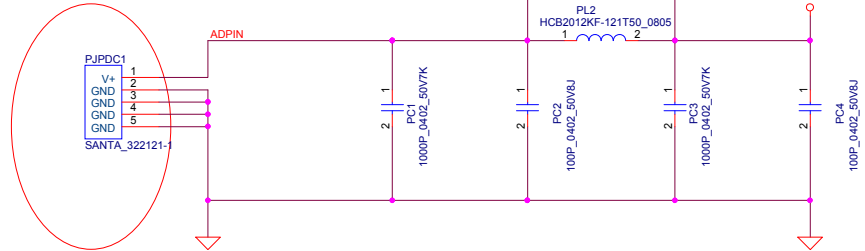
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Document Number				Rev	
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# Power block



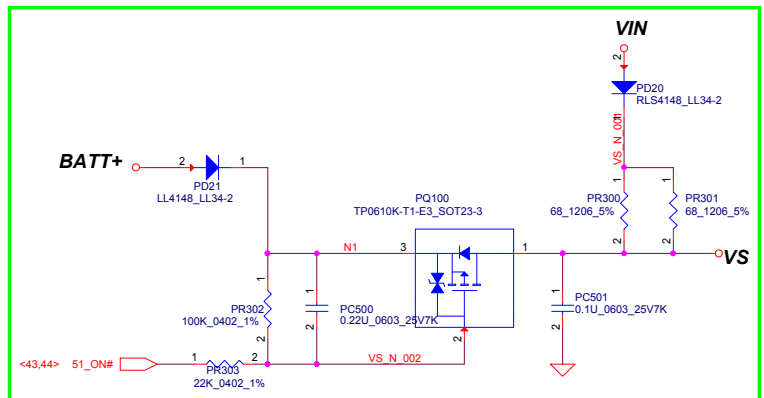
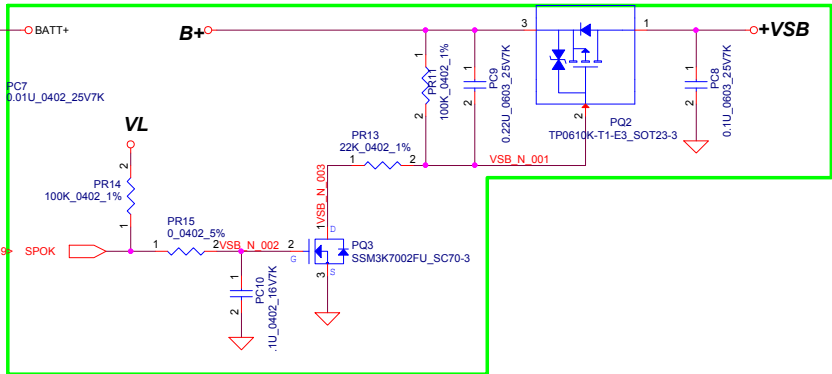
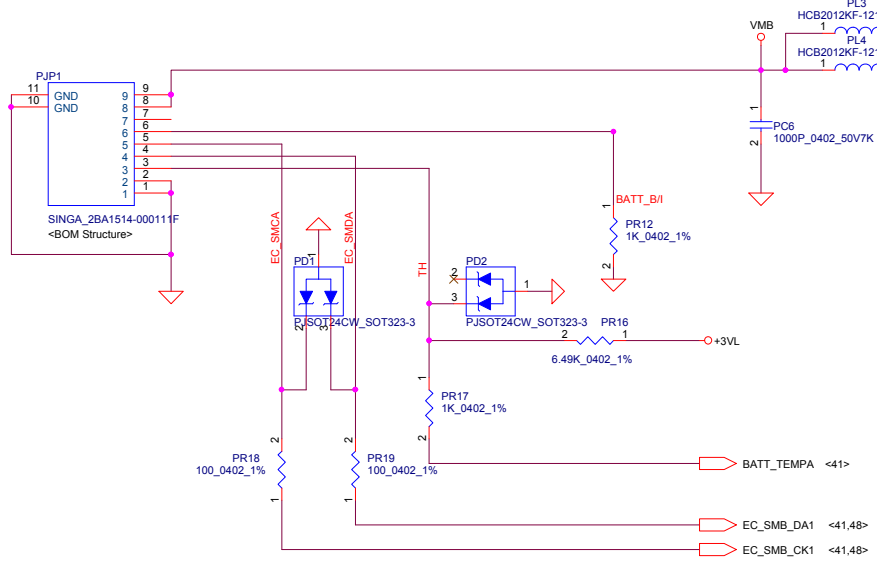
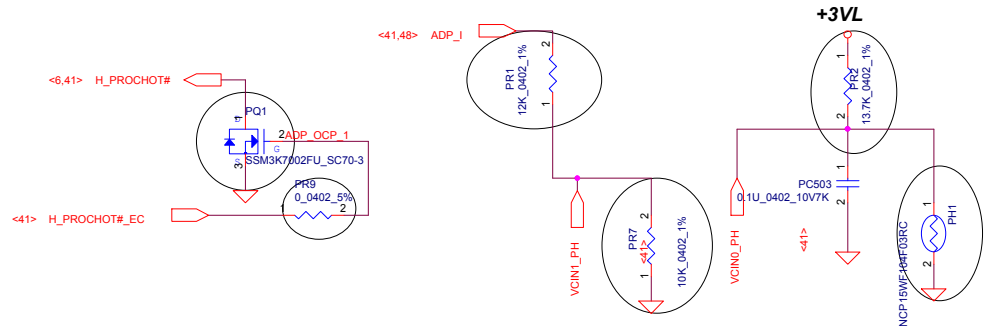
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Issued Date	2011/10/31	Deciphered Date	2012/12/31	Title
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				0.1
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DCIN jack P/N:DC301008L00,  
need double confirm P/N with ME

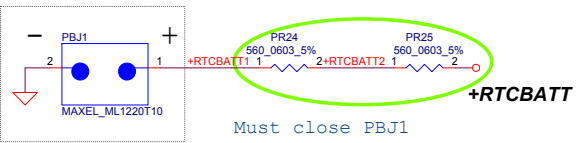


PH1 under CPU bottom side :  
CPU thermal protection at 93 +3 degree C  
Recovery at 56 +3 degree C

For KB930 --> Keep PU1 circuit  
(Vth = 0.825V)  
For KB9012 (Red square) --> Remove PU1 circuit, but keep  
PH1, PR1, PR2, PR7, PR9, PQ1



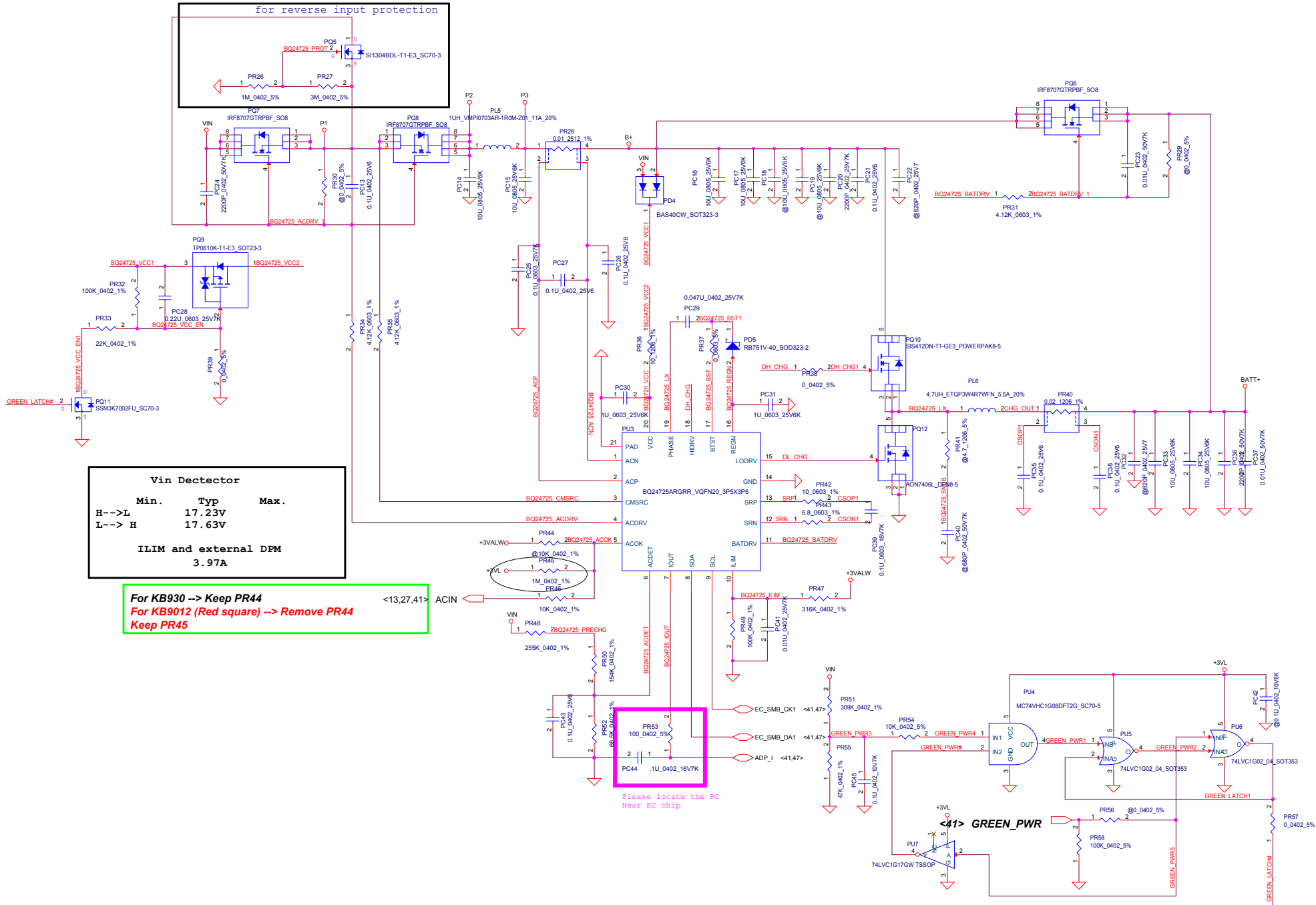
RTC Battery



SP093MX000  
Change RTC For Cost Down

For KB9012 --> Remove all 51\_ON# circuit

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				<b>PWR-DCIN / BATT CONN / OTP</b>
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Size	Document Number	Date		Rev
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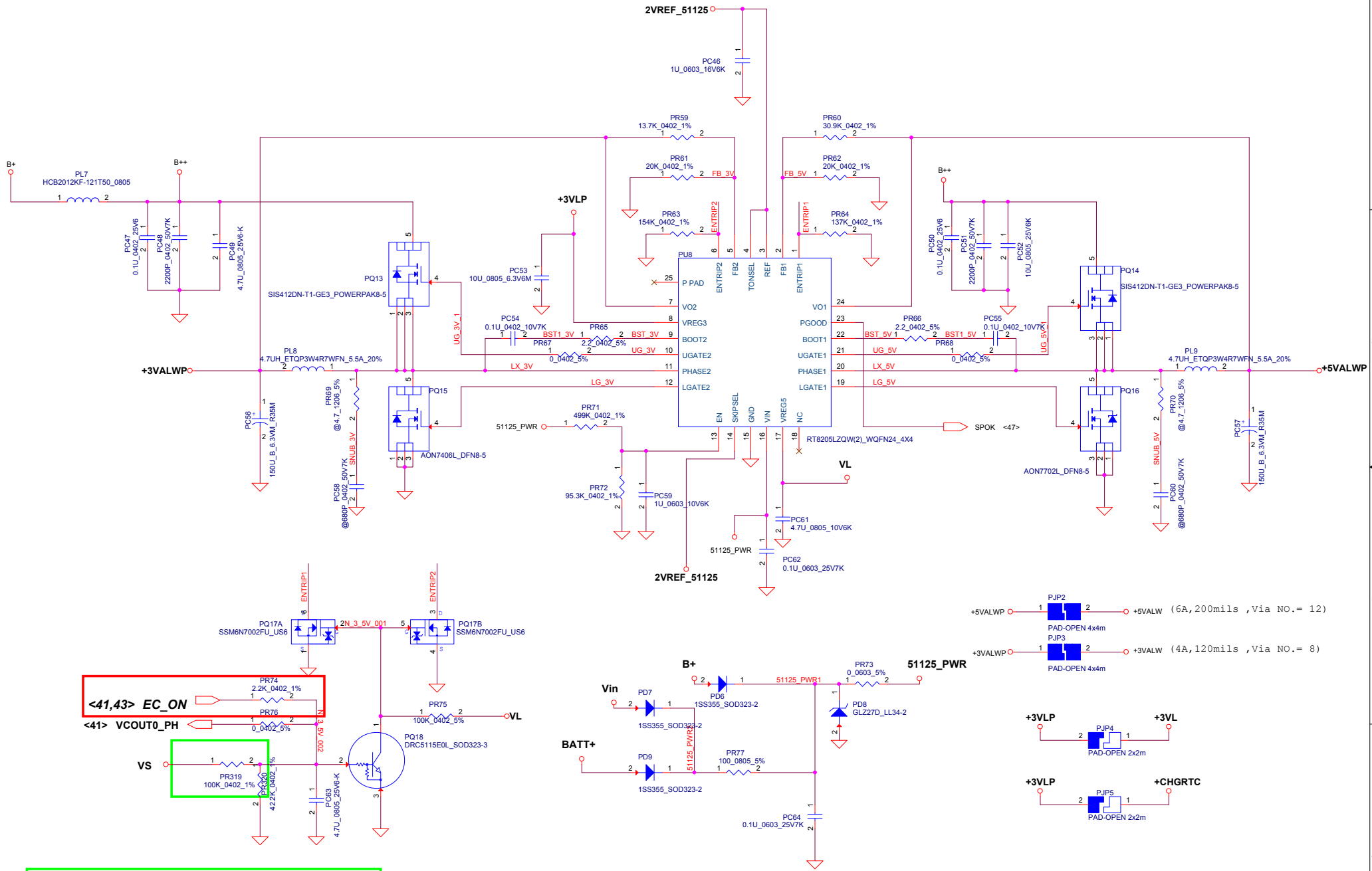
Vin Detector		
Min.	Typ	Max.
H-->L	17.23V	
L-->H	17.63V	
ILIM and external DPM		
3.97A		

For KB930 -> Keep PR44  
 For KB9012 (Red square) -> Remove PR44  
 Keep PR45

Please locate the RC  
 Near EC chip

Security Classification		Compal Secret Data		Title	
Issued Date	2011/10/31	Deciphered Date	2012/12/31	PWR-CHARGER	
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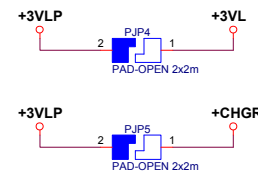
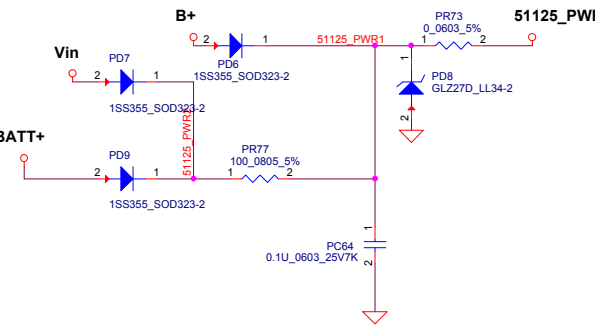




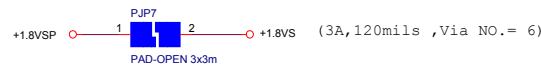
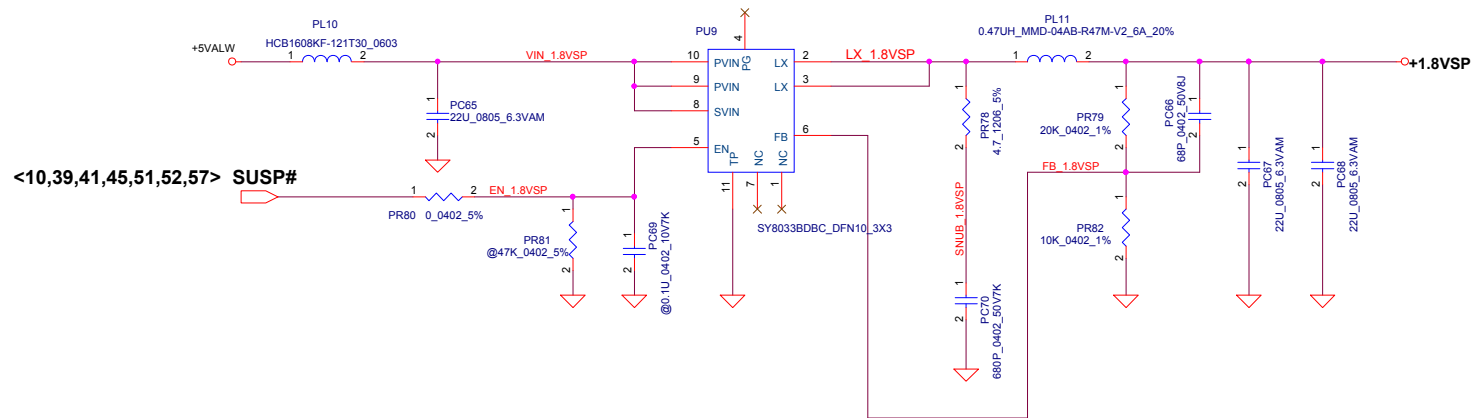
**<41,43> EC\_ON**  
**<41> VCOUT0\_PH**

**VS**

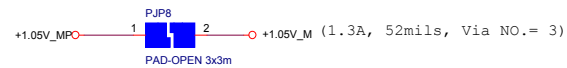
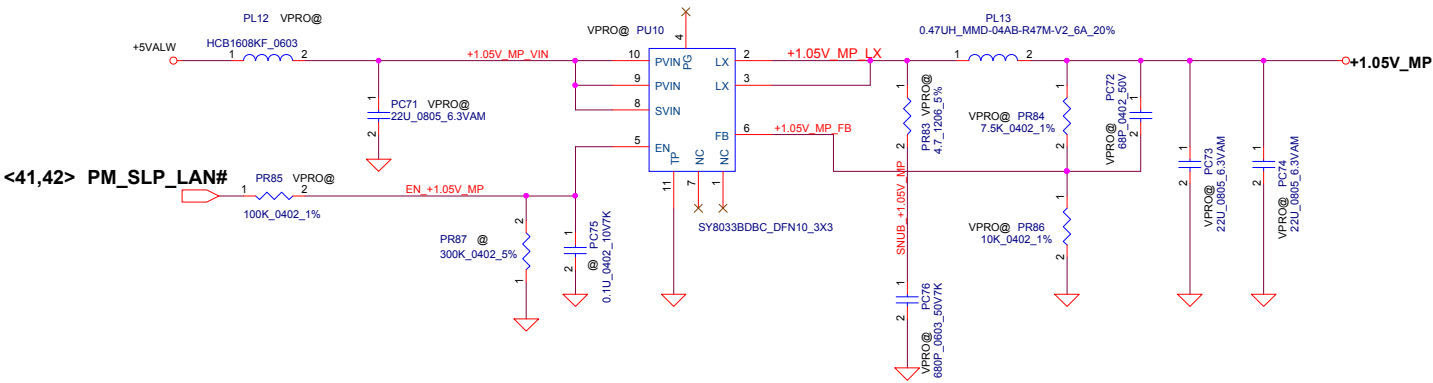
**For KB930 --> Keep PR319, Remove PR74**  
**For KB9012 (Red square) --> Remove PR319**  
**Keep PR74**



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$V_o = 1.05V$      $V_{FB} = 0.6V$   
 $V_o = V_{FB} (1 + PR401/PR402) = 0.6 * (1 + 7.5K/10K) = 1.05V$

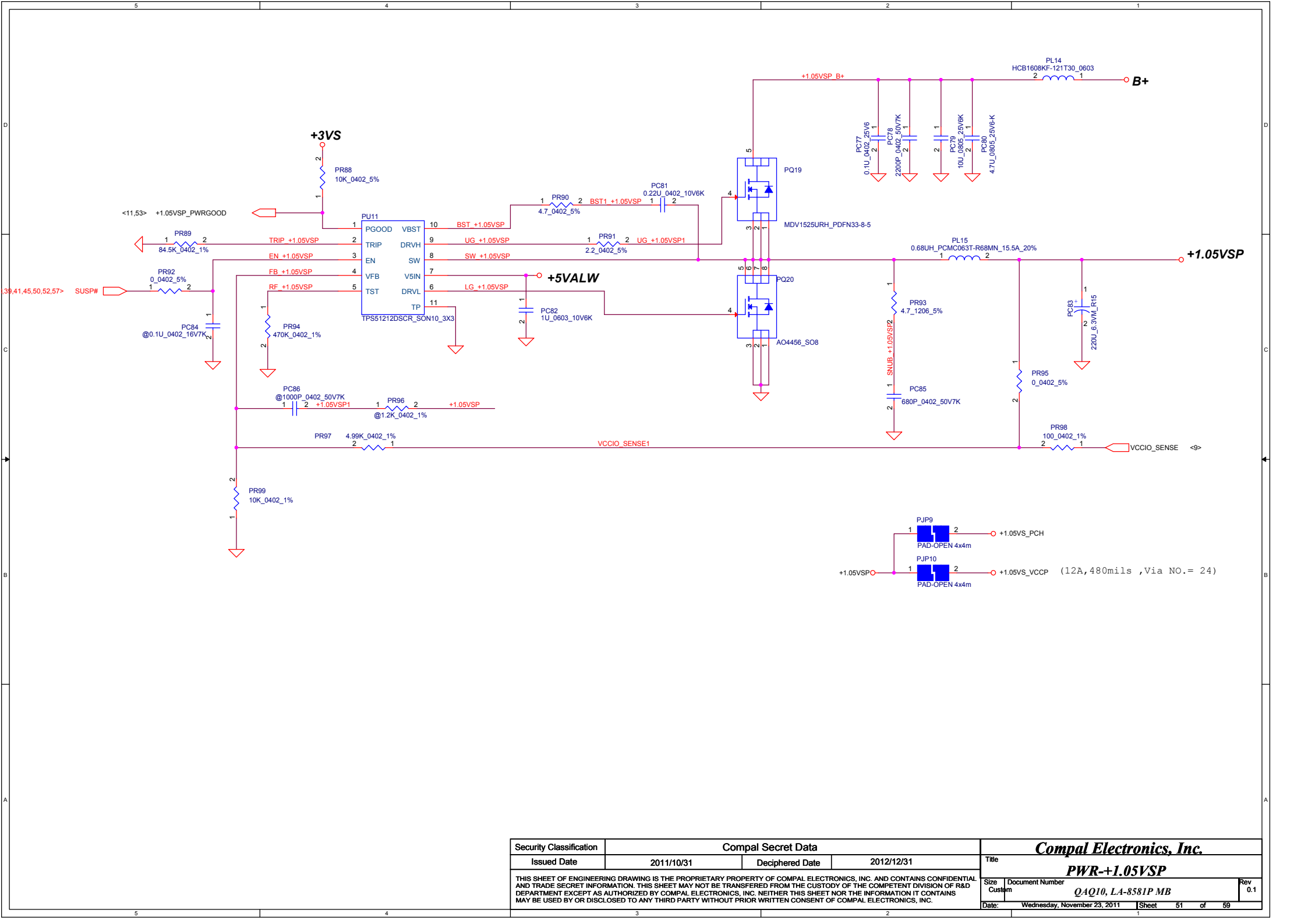


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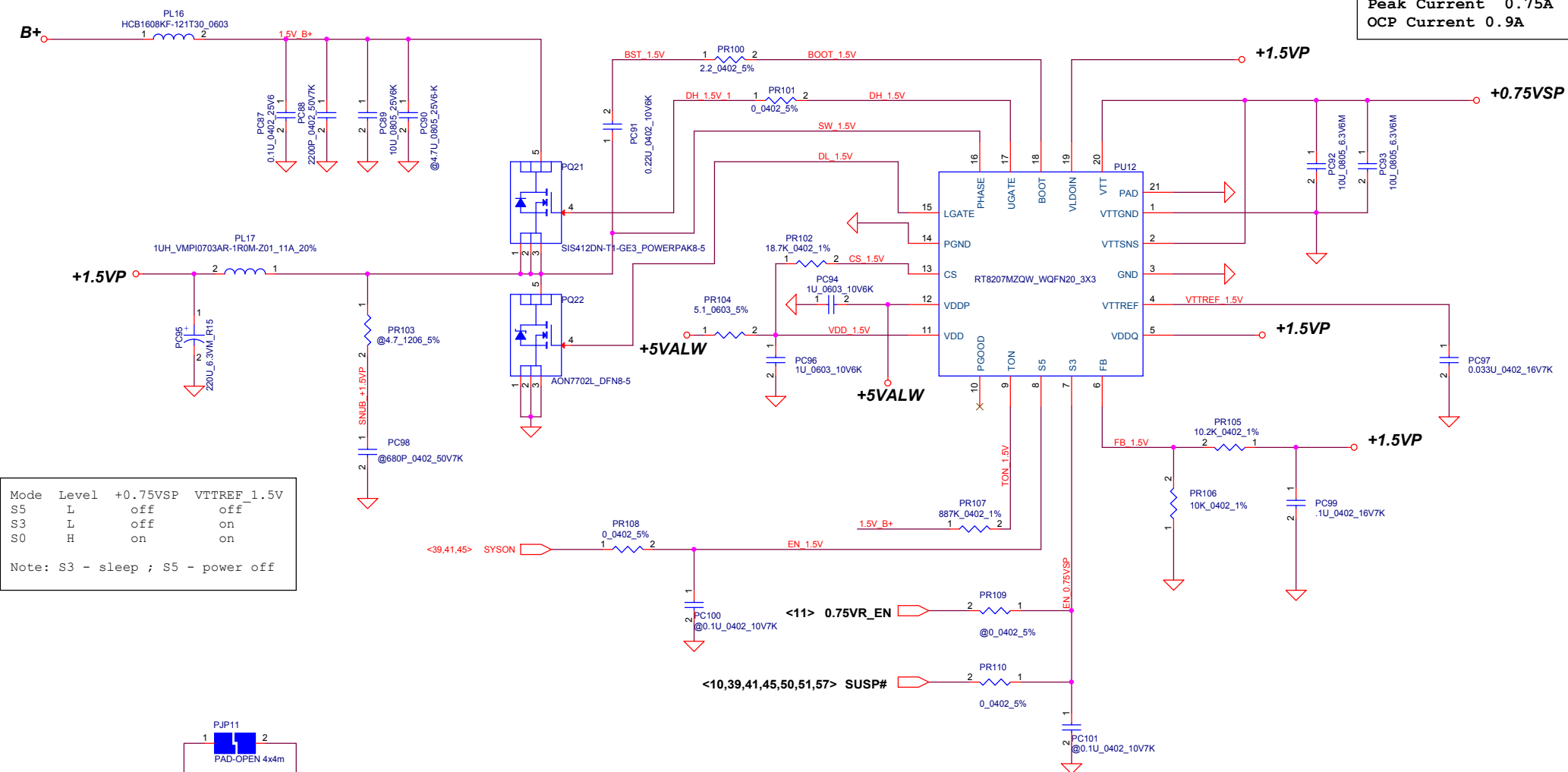
**PWR-1.8VSP,1.05V MP**

**QAQ10\_LA-8581P MB**



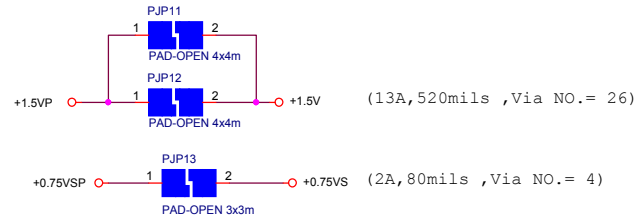
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0.75Volt +/- 5%  
 TDC 0.525A  
 Peak Current 0.75A  
 OCP Current 0.9A

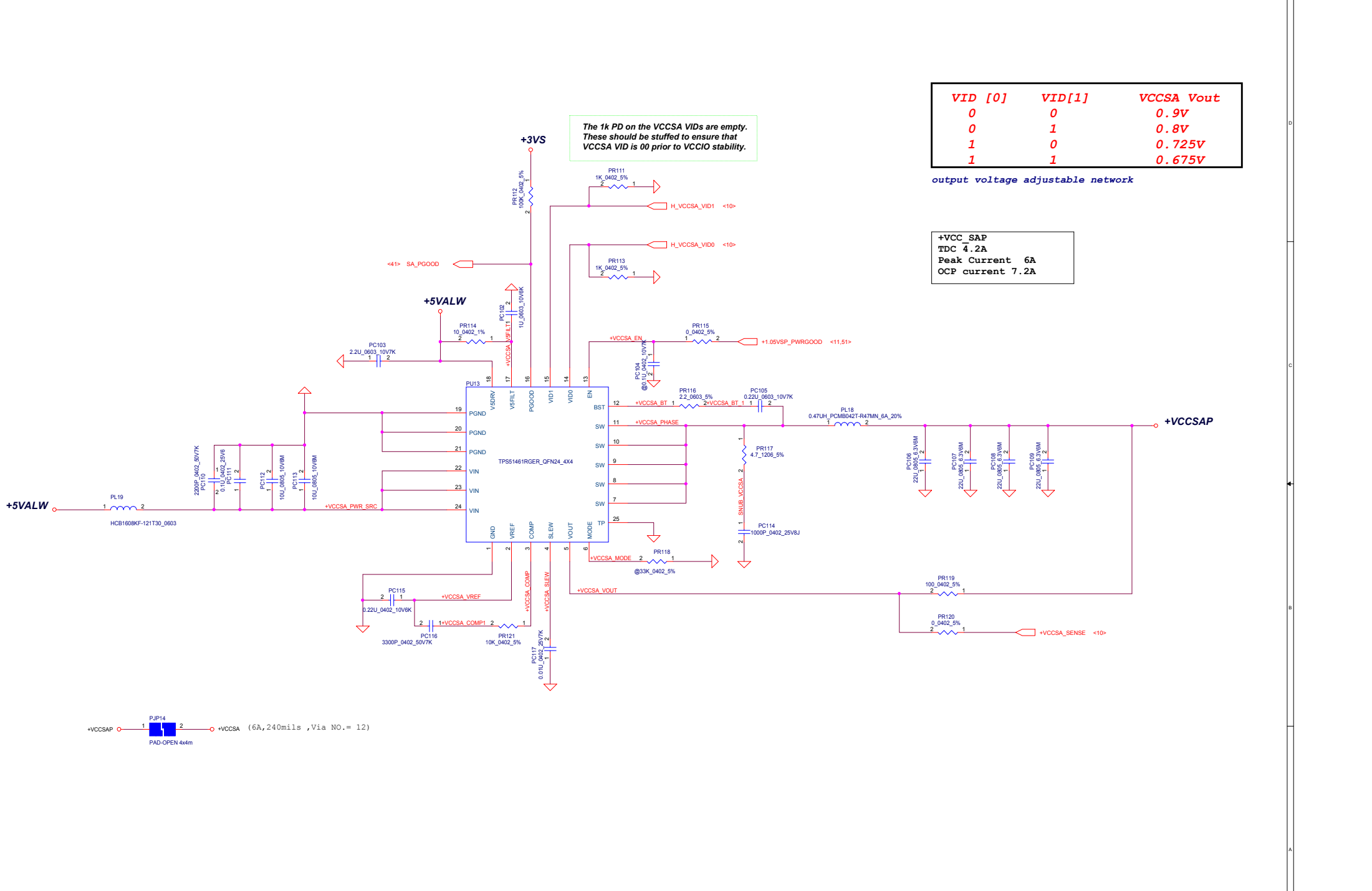


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



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The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

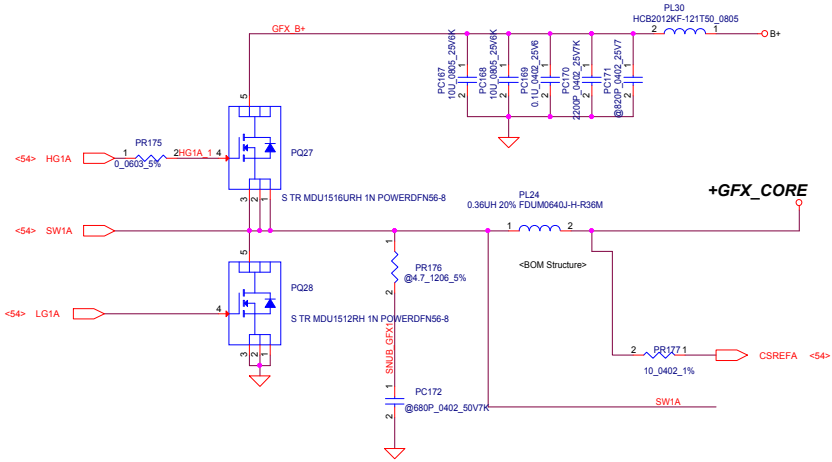
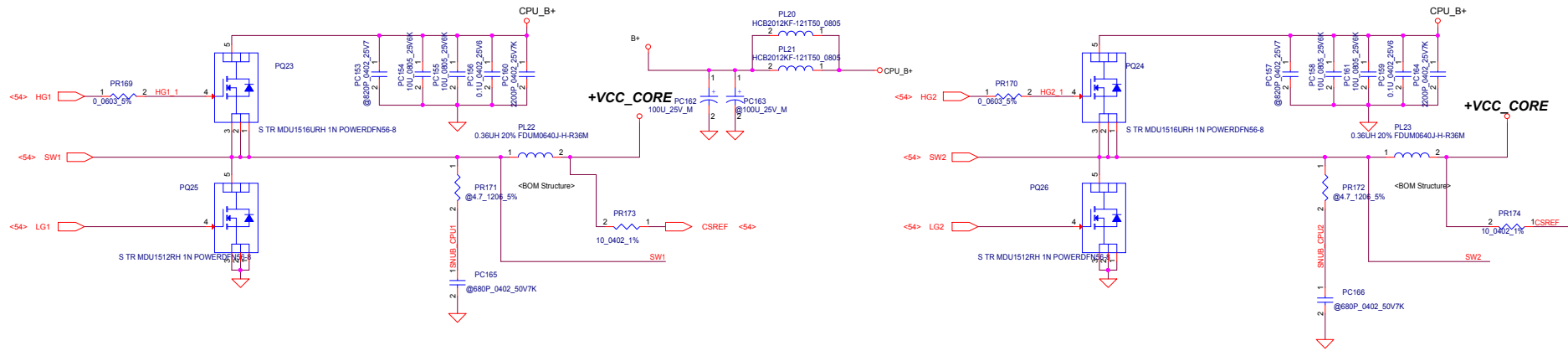
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC SAP  
 TDC 4.2A  
 Peak Current 6A  
 OCP current 7.2A





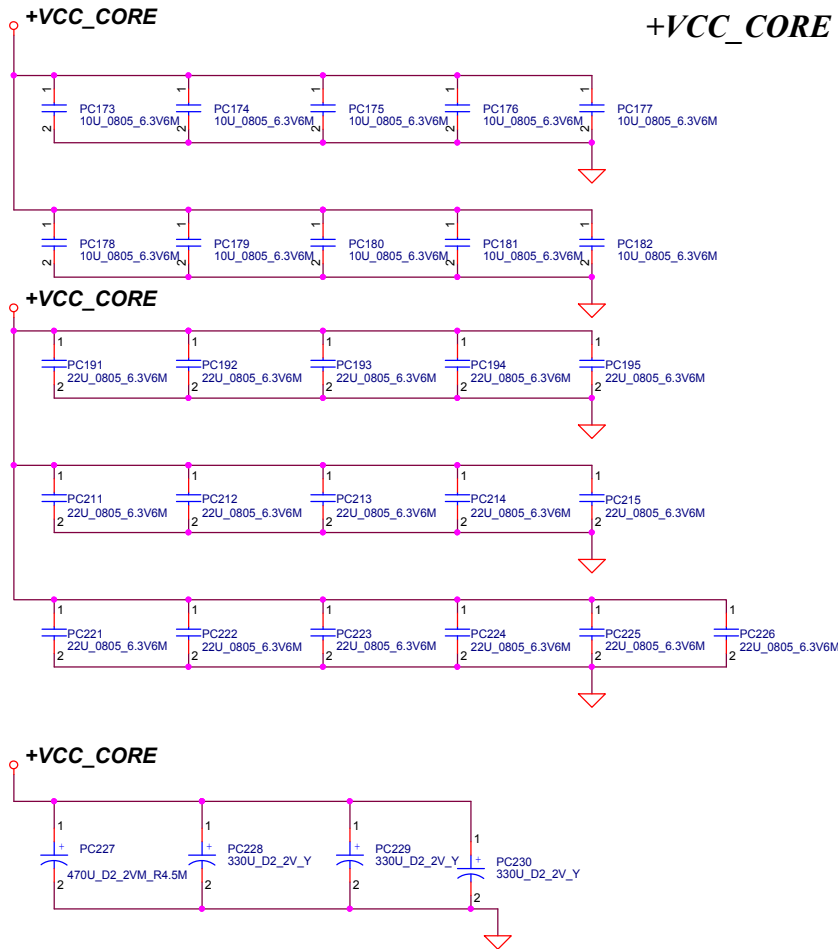


**QC 45W CPU**  
 VID1=0.9V  
 IccMax=94A  
 Icc\_Dyn=66A  
 Icc\_TDC=52A  
 R\_LL=1.9m ohm  
 OCP=110A

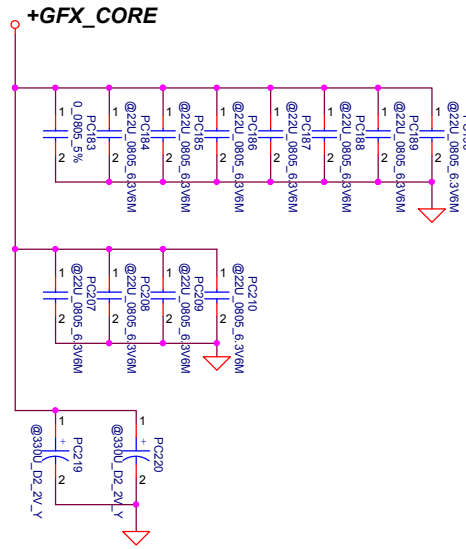
**DC 35W CPU**  
 VID1=1.05V  
 IccMax=53A  
 Icc\_Dyn=43A  
 Icc\_TDC=36A  
 R\_LL=1.9m ohm  
 OCP=65A

**DC 35W GT2**  
 VID1=1.23V  
 IccMax=33A  
 Icc\_Dyn=20.2A  
 Icc\_TDC=21.5A  
 R\_LL=3.9m ohm  
 OCP=40A

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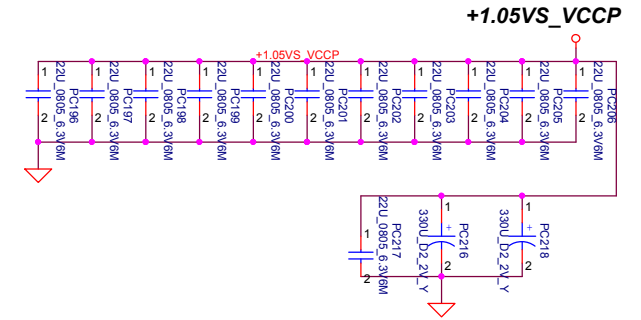


**+GFX\_CORE**



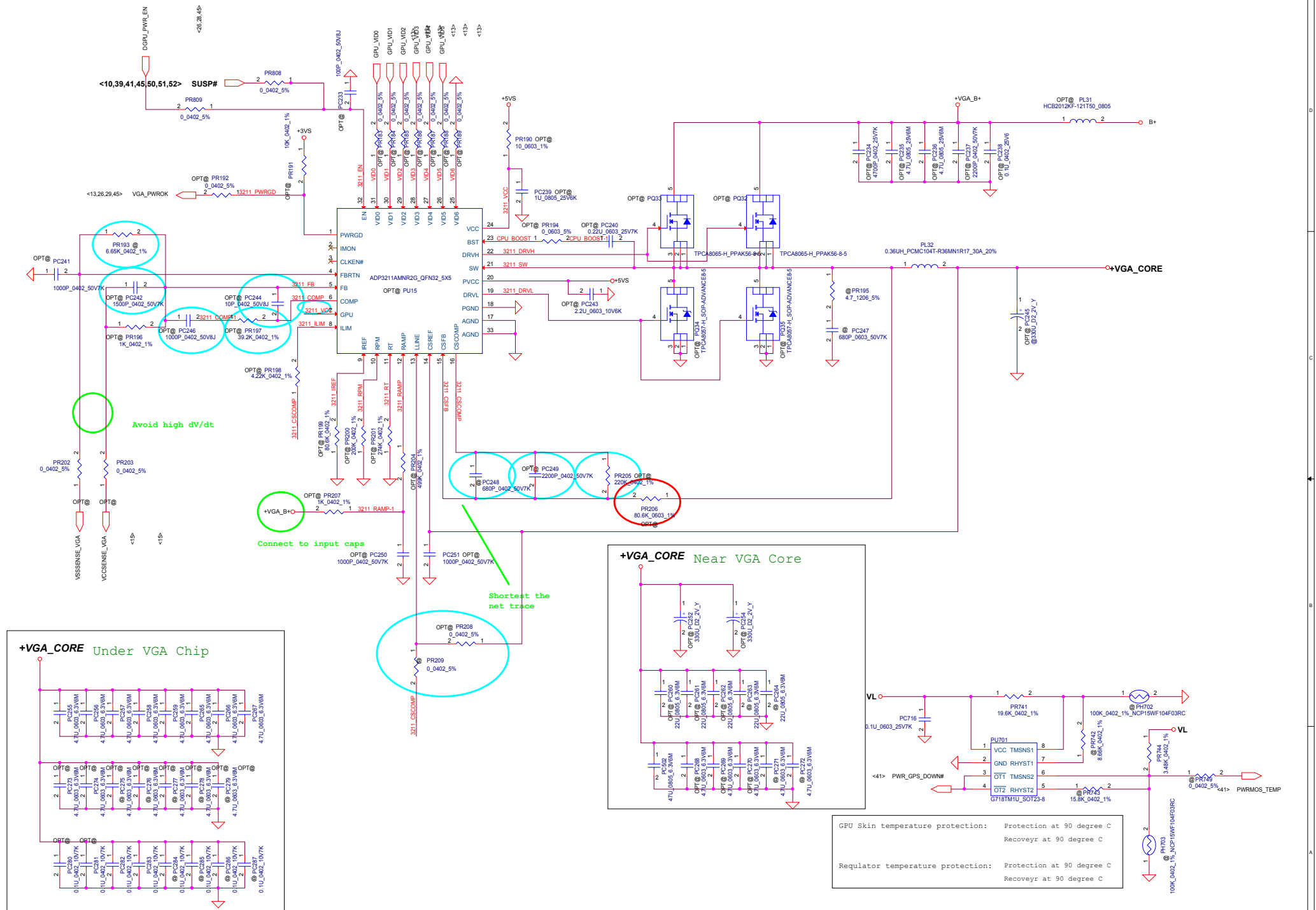
Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites



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GPU Skin temperature protection:	Protection at 90 degree C
	Recoveryr at 90 degree C
Regulator temperature protection:	Protection at 90 degree C
	Recoveryr at 90 degree C

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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