Compal Confidential

QIWG5/QIWG6 UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

2012-05-11

LA-7987P

REV:1.0

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Compal confidential
File Name : QIWG5/QIWG6

ZZZ1 DAZ_PCB DAZ0N200601 15@

ZZZ LA7987 DAZ_PCB DAZ0N100701 14@

QIWG5
LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B

QIWG6
LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B
LS7984P LED/B
LS7985P ODD/B

Intel Ivy Bridge
Socket-rPGA988B
37.5mm*37.5mm
Page4-10

DDR3 SO-DIMM *2
BANK 0, 1, 2, 3 Page11-12
Up to 8GB

Dual Channel
DDR3 1066MHz(1.5V)
DDR3 1333MHz(1.5V)
DDR3 1600MHz(1.5V)

100MHz 2.7GT/s *FDI *8* *DMI *4*

Intel Panther Point
HM75 / HM76
FCBGA 989
25mm*25mm
Page13-21

HDMI Connector Page24
CRT Connector Page23
LVDS Connector Page22
USB3.0 *2(Left)

AZALIA
Audio Codec Conexant CX20671-21Z Page30
→ **2 channel speaker** Page30
→ **Int. MIC x1** Page30
→ **Audio Jacks** Page32

*USB2.0 *14*
→ **Camera Conn.** Page22
→ **BlueTooth Conn.** Page29
→ **Mini Card Slot *1** Page25
→ **Card Reader** Page32
Reltek
RTS5178 for SDR50
SDXC/MMC
→ **USB2.0 *2(Right)** Page 32;33
→ **USB2.0 *2(Left)** Page34

*SATA *6*
→ **SATA HDD** Page29
→ **SATA ODD** Page29

*PCI-E x1 *6*

Option Page34
USB3.0
Renesas
uPD720202

SPIROM BIOS Page13

LPC BUS

EC Page31
ENE KB9012

Touch Pad Page32
Int. KBD Page32
Thermal Sensor
EMC1403 Page28

Arthros
AR8161(GLAN)
AR8162(10/100)
Page26

RJ-45 Connector Page27

PCI Express Mini Card Slot *1
WLAN Page25
PCI-E(WLAN)

(Port 0/Port 1 support SATA3)

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Right Side CR-BD)
	UHCI1	2	USB Port (Left Side) USB3.0
		3	USB Port (Left Side) USB3.0
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Cameara	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@
G5/G6/G9(Low/Mid END)	nonBBH@
G9 High-END	BBH@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

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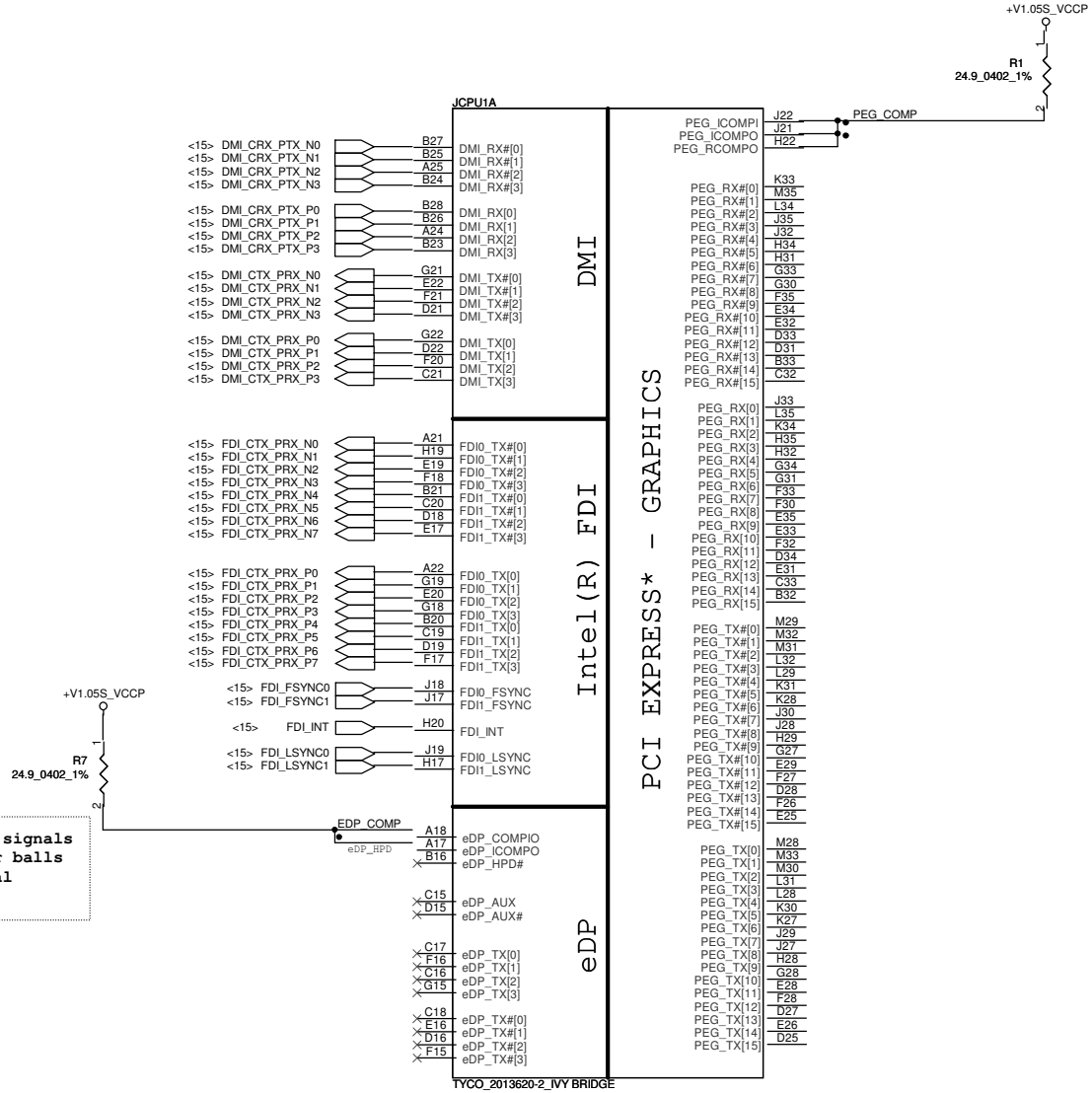
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

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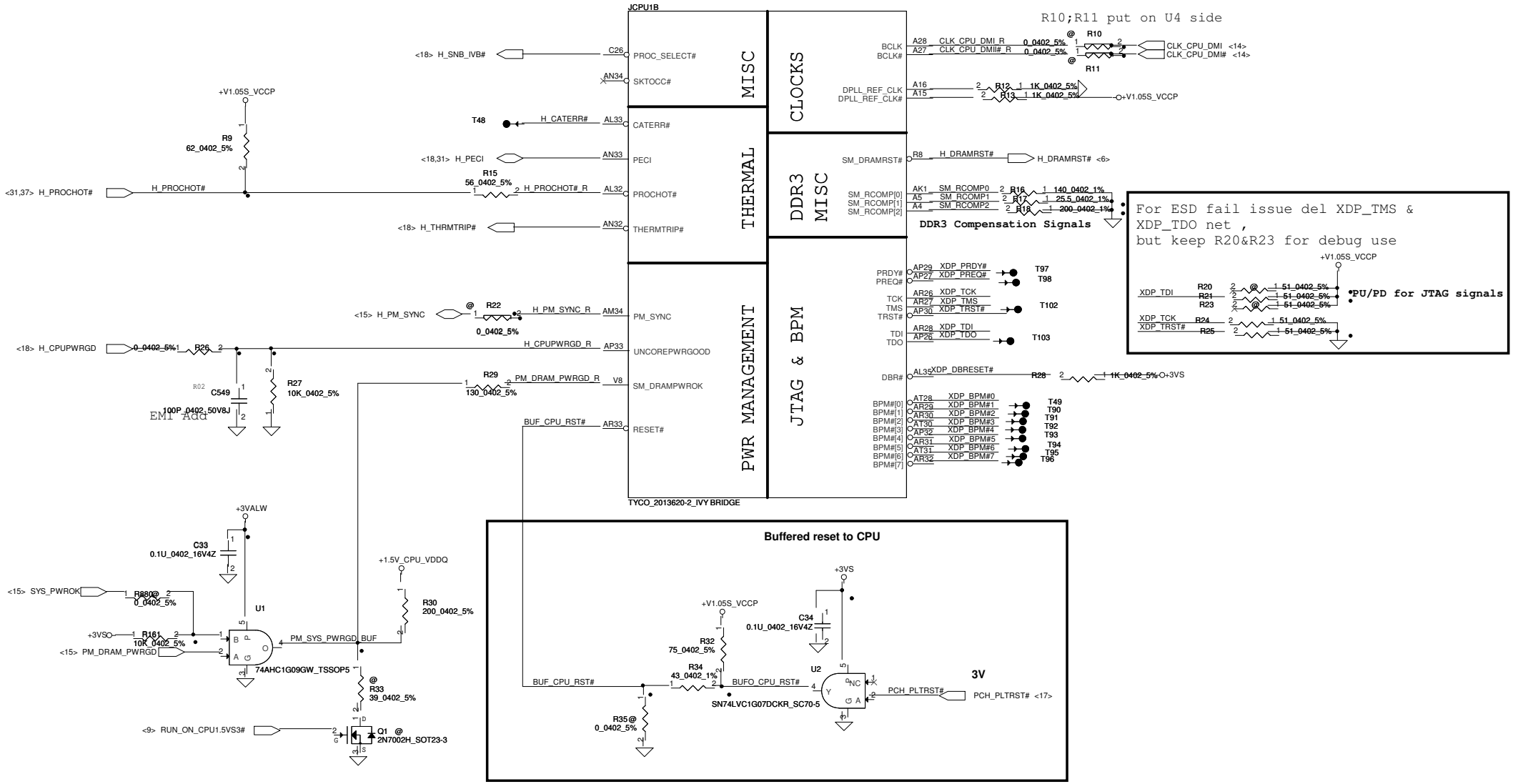

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Title: PROCESSOR(2/7) PM,XDP,CLK

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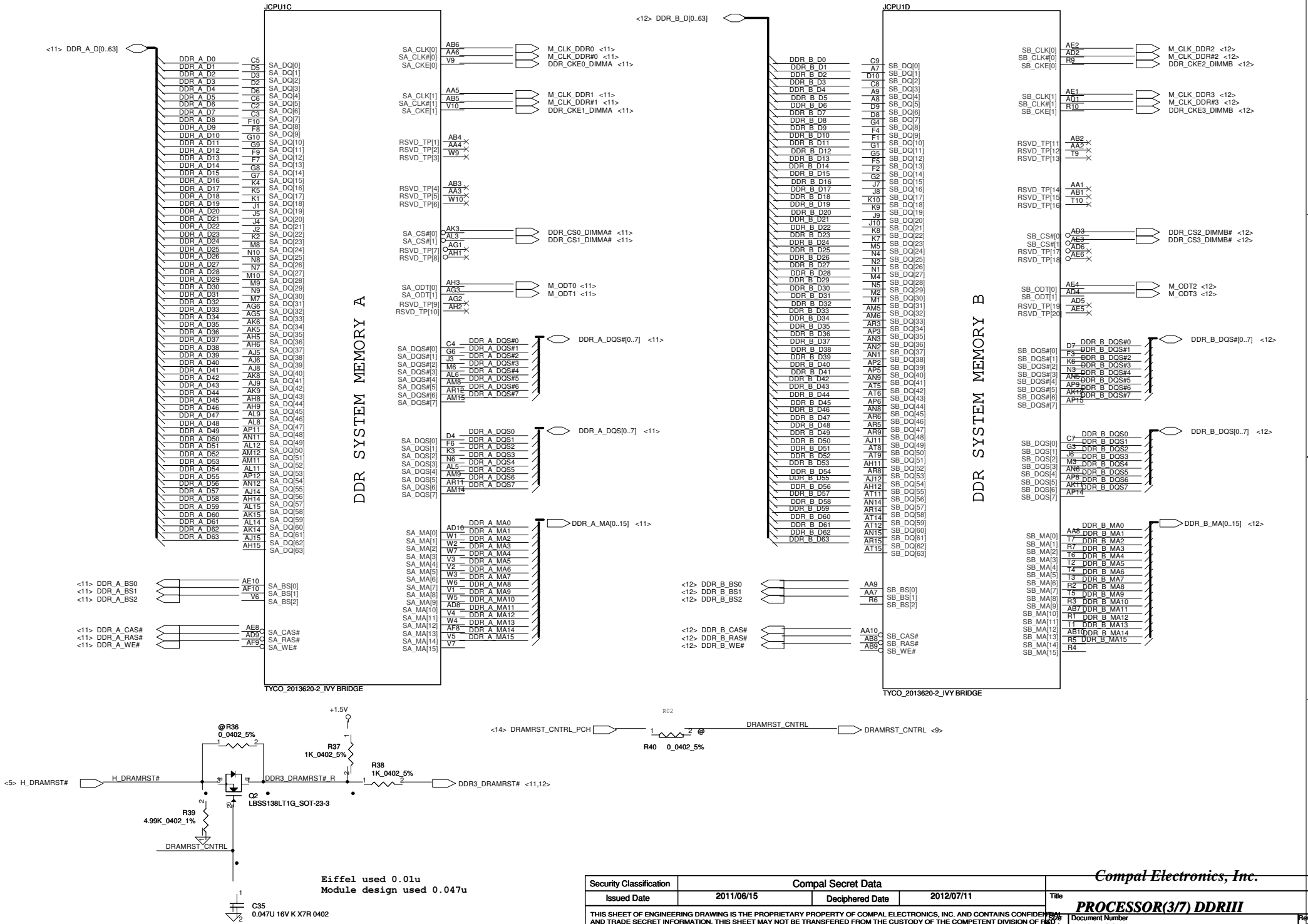

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Title: PROCESSOR(3/7) DDRIII

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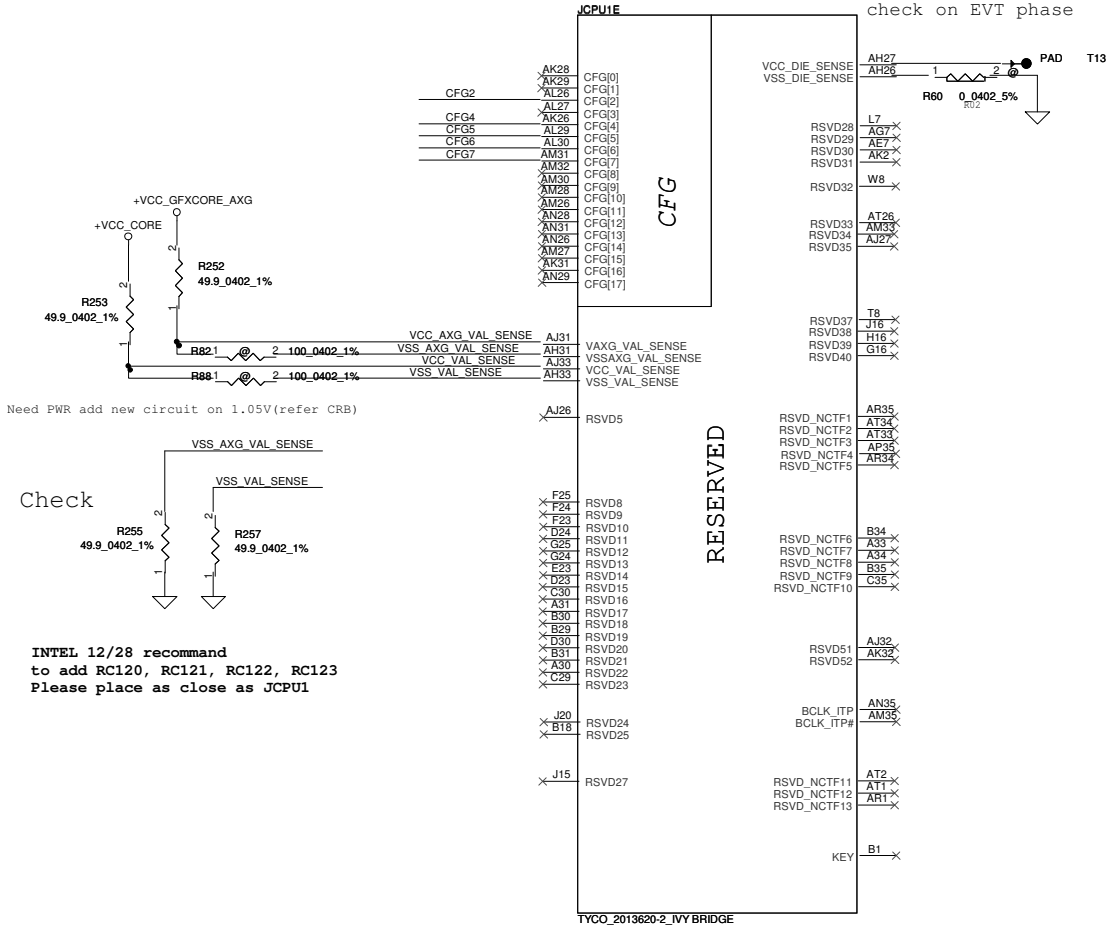
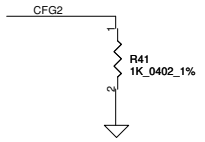
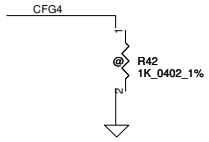
CFG Straps for Processor

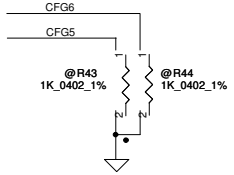




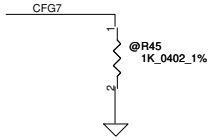
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG		
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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

TYCO_2013620-2_IVY BRIDGE

+V1.05S_VCCP

C99
0.1U_0402_10V6K

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

R47 0_0402_5%
R48 @
R49 @

VR_SVID_ALRT# <43>
VR_SVID_CLK <43>
VR_SVID_DAT <43>

R50 130_0402_5% +V1.05S_VCCP

0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

+VCC_CORE

R51
100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R

R52 @0_0402_5%
R53 @0_0402_5%

VCCSENSE <43>
VSSSENSE <43>

VCCIO_SENSE B10 VSSIO_SENSE_L
VSS_SENSE_VCCIO A10

R74 @ 10_0402_1%

VSSIO_SENSE

VCCIO_SENSE <41,42>

R66 @ 100_0402_1%

R54
100_0402_1%

R74 & R79 put together

VSSIO_SENSE_L <42>

+V1.05S_VCCP

R79
10_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

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Title: PROCESSOR(5/7) PWR,BYPASS

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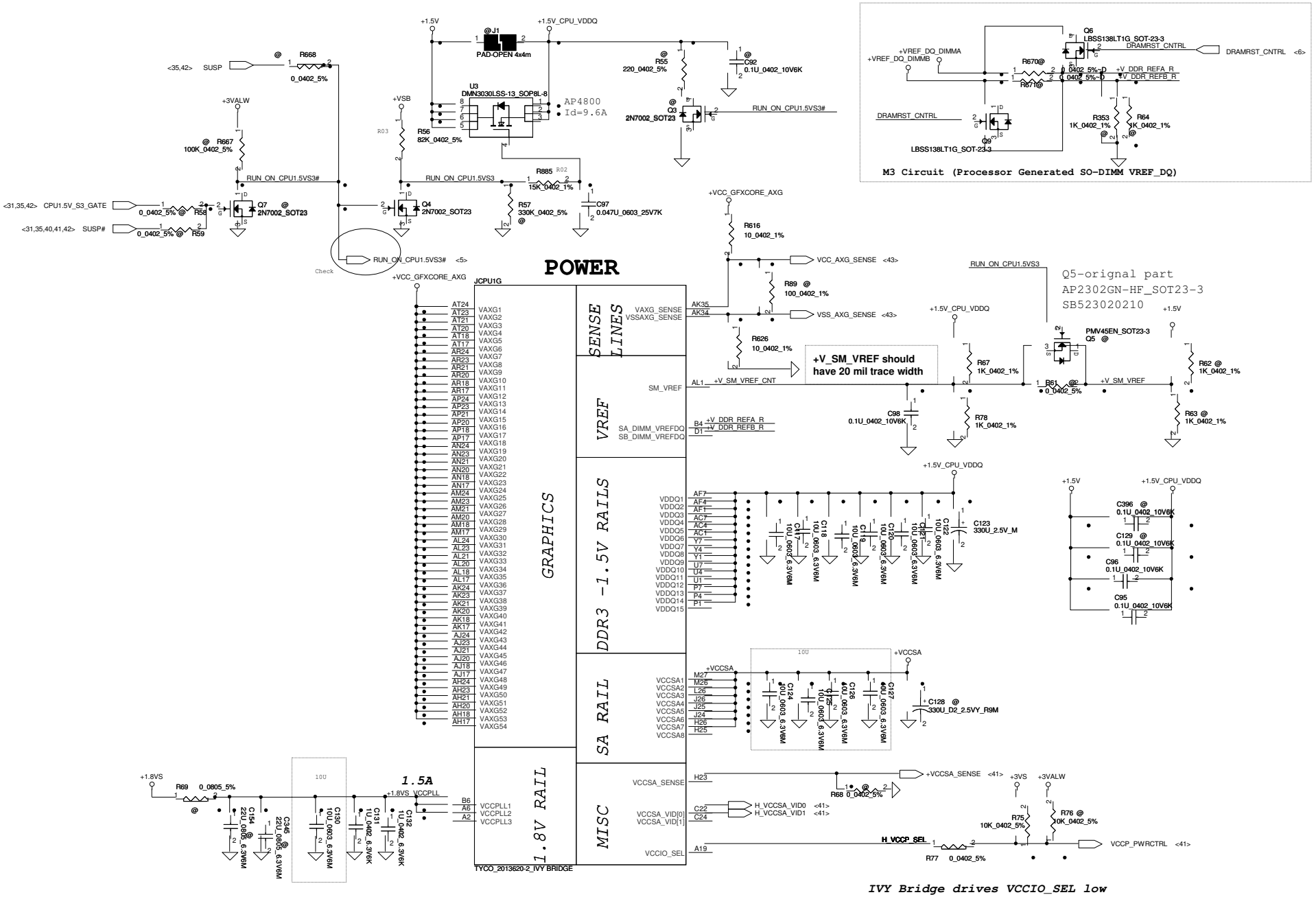

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Title	PROCESSOR(6/7) PWR		
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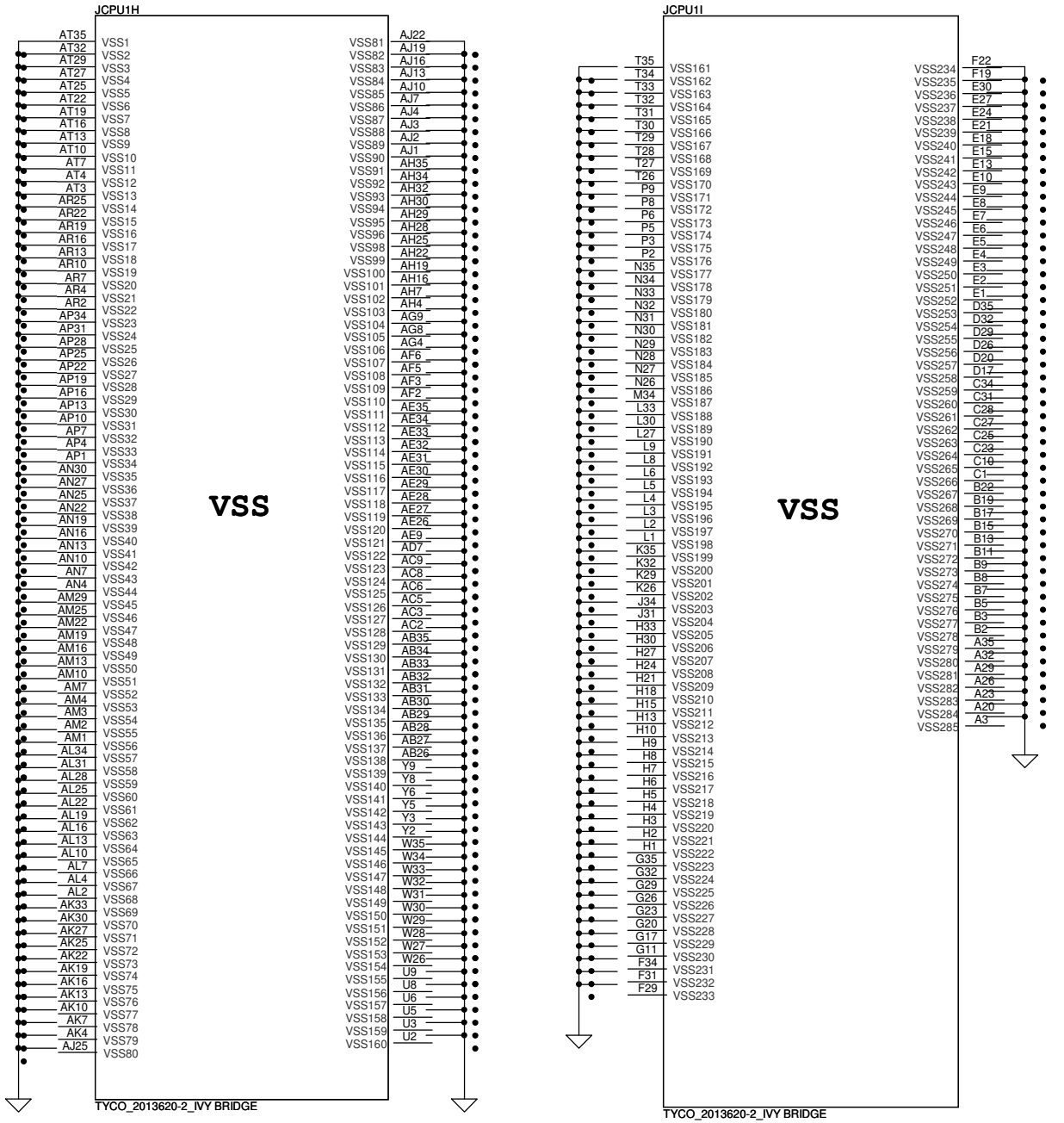

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Title: PROCESSOR(7/7) VSS

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DDR3 SO-DIMM A

JDIMM1

<6> DDR_A_D[0..63]
<6> DDR_A_DQS[0..7]
<6> DDR_A_DQS#[0..7]
<6> DDR_A_MA[0..15]

+VREF_DQ_DIMMA
R70 1K_0402_1%
R71 1K_0402_1%
C134 2.2U_0603_6.3V4Z
C133 0.1U_0402_10V6K

DDR_A_D0 DDR_A_D1 DDR_A_DM0 DDR_A_D2 DDR_A_D3 DDR_A_D8 DDR_A_D9 DDR_A_DQS#1 DDR_A_DQS1 DDR_A_D10 DDR_A_D11 DDR_A_D16 DDR_A_D17 DDR_A_DQS#2 DDR_A_DQS2 DDR_A_D18 DDR_A_D19 DDR_A_D24 DDR_A_D25 DDR_A_DM3 DDR_A_D26 DDR_A_D27 DDR_A_D32 DDR_A_D33 DDR_A_DQS#4 DDR_A_DQS4 DDR_A_D34 DDR_A_D35 DDR_A_D40 DDR_A_D41 DDR_A_DM5 DDR_A_D42 DDR_A_D43 DDR_A_D48 DDR_A_D49 DDR_A_DQS#6 DDR_A_DQS6 DDR_A_D50 DDR_A_D51 DDR_A_D56 DDR_A_D57 DDR_A_DM7 DDR_A_D58 DDR_A_D59

VREF_DQ VSS1 DQ0 DQ4 DQ1 DQ5 VSS4 VSS3 DM0 DQS#0 VSS5 DQS0 DQ2 VSS6 DQ3 DQ6 VSS7 DQ7 DQ8 VSS8 DQ9 DQ12 VSS9 DQ13 DQS#1 VSS10 DQS1 DM1 VSS11 RESET# DQ10 VSS12 DQ11 DQ14 VSS13 DQ15 DQ16 VSS14 DQ17 DQ20 VSS15 DQ21 DQS#2 VSS16 DQS2 DM2 VSS18 VSS17 DQ18 DQ22 DQ19 DQ23 VSS20 VSS19 DQ24 DQ28 DQ25 DQ29 VSS22 VSS21 DM3 DQS#3 VSS23 DQS3 DQ26 VSS24 DQ27 DQ30 VSS25 DQ31 VSS26

DDR_A_D4 DDR_A_D5 DDR_A_DQS#0 DDR_A_DQS0 DDR_A_D6 DDR_A_D7 DDR_A_D12 DDR_A_D13 DDR_A_DM1 DDR3_DRAMRST# DDR_A_D14 DDR_A_D15 DDR_A_D20 DDR_A_D21 DDR_A_DM2 DDR_A_D22 DDR_A_D23 DDR_A_D28 DDR_A_D29 DDR_A_DQS#3 DDR_A_DQS3 DDR_A_D30 DDR_A_D31

DDR3_DRAMRST# <6,12>

DDR_CKE0_DIMMA DDR_CKE1_DIMMA DDR_CKE1_DIMMA <6>

CKE0 CKE1 VDD1 VDD2 NC1 A15 BA2 A14 VDD3 VDD4 A12/BC# A11 A9 A7 VDD5 VDD6 A8 A6 A5 A4 VDD7 VDD8 A3 A2 A1 A0 VDD9 VDD10 CK0 CK1 CK0# CK1# VDD11 VDD12 A10/AP BA1 BA0 RAS# VDD13 VDD14 WE# S0# CAS# ODT0 VDD15 VDD16 A13 ODT1 S1# NC2 VDD17 VDD18 NCTEST VREF_CA VSS27 VSS28 DQ32 DQ36 DQ33 DQ37 VSS29 VSS30 DQS#4 DM4 DQS4 VSS31 VSS32 DQ38 DQ34 DQ39 VSS33 VSS34 DQ44 DQ40 DQ45 VSS35 VSS36 DQS#5 DM5 VSS37 DQ42 DQ46 DQ43 DQ47 VSS39 VSS40 DQ48 DQ52 DQ49 DQ53 VSS41 VSS42 DQS#6 DM6 DQS6 VSS43 VSS44 DQ54 DQ50 DQ55 DQ51 VSS45 VSS46 DQ60 DQ56 DQ61 DQ57 VSS47 VSS48 DQS#7 DM7 VSS49 DQ62 DQ58 DQ63 DQ59 VSS50 VSS51 VSS52 SA0 EVENT# VDDSPD SDA SA1 SCL VTT1 VTT2

DDR_A_D36 DDR_A_D37 DDR_A_DM4 DDR_A_D38 DDR_A_D39 DDR_A_D44 DDR_A_D45 DDR_A_DQS#5 DDR_A_DQS5 DDR_A_D46 DDR_A_D47 DDR_A_D52 DDR_A_D53 DDR_A_DM6 DDR_A_D54 DDR_A_D55 DDR_A_D60 DDR_A_D61 DDR_A_DQS#7 DDR_A_DQS7 DDR_A_D62 DDR_A_D63 SMB_DATA_S3 SMB_CLK_S3

SMB_DATA_S3 <12,14,25>
SMB_CLK_S3 <12,14,25>

DDR_A_MA15 DDR_A_MA14 DDR_A_MA11 DDR_A_MA7 DDR_A_MA6 DDR_A_MA4 DDR_A_MA2 DDR_A_MA0 M_CLK_DDR1 M_CLK_DDR#1 DDR_A_BS1 DDR_A_RAS# DDR_CS0_DIMMA# M_ODT0 M_ODT1

M_CLK_DDR1 <6>
M_CLK_DDR#1 <6>
DDR_A_BS1 <6>
DDR_A_RAS# <6>
DDR_CS0_DIMMA# <6>
M_ODT0 <6>
M_ODT1 <6>

<6> DDR_CKE0_DIMMA
<6> M_CLK_DDR0
<6> M_CLK_DDR#0
<6> DDR_A_BS2
<6> DDR_A_WE#
<6> DDR_A_CAS#
<6> DDR_CS1_DIMMA#

DDR_A_MA12 DDR_A_MA9 DDR_A_MA8 DDR_A_MA5 DDR_A_MA3 DDR_A_MA1 DDR_A_MA10 DDR_A_BS0 DDR_A_WE# DDR_A_CAS# DDR_A_MA13 DDR_CS1_DIMMA#

+VREF_CA
R72 1K_0402_1%
R73 1K_0402_1%
C135 0.1U_0402_10V6K
C136 2.2U_0603_6.3V4Z

R81 10K_0402_5%
R83 10K_0402_5%
C156 0.1U_0402_10V6K
C155 2.2U_0603_6.3V4Z

FOX_AS0A626-U4SN-7F
ME@

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note: Place near DIMM

C137 10U_0603_6.3V6M @
C138 10U_0603_6.3V6M @
C139 10U_0603_6.3V6M
C140 10U_0603_6.3V6M
C141 10U_0603_6.3V6M
C142 10U_0603_6.3V6M
C143 10U_0603_6.3V6M
C144 10U_0603_6.3V6M
C145 0.1U_0402_10V6K
C146 0.1U_0402_10V6K
C147 0.1U_0402_10V6K
C148 0.1U_0402_10V6K
C149 @ 220U_6.3V_M
EVT Check

Layout Note: Place near DIMM

C150 1U_0402_6.3V6K
@C151 1U_0402_6.3V6K
C152 1U_0402_6.3V6K
@C153 1U_0402_6.3V6K

7/28 Update connect GND directly

DDR_A_DM0 DDR_A_DM1 DDR_A_DM2 DDR_A_DM3 DDR_A_DM4 DDR_A_DM5 DDR_A_DM6 DDR_A_DM7

Layout Note: Place near DIMM

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Title: DDRIII-SODIMM SLOT1

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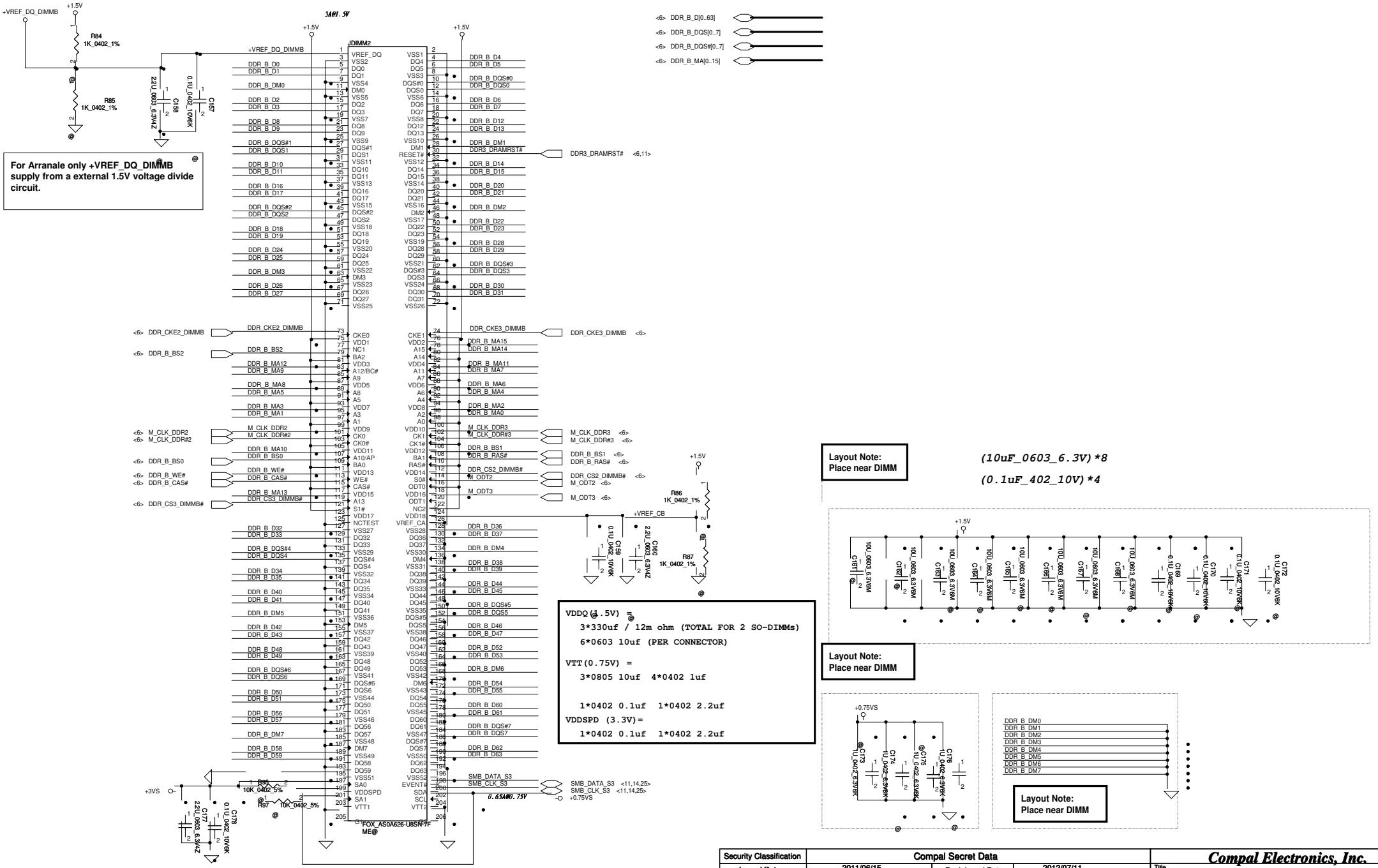

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Title: DDRIII-SODIMM SLOT2		
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W=20mils
W=20mils
+RTCVCC
+RTCBATT
R99 1K_0402_5%
C179 1U_0603_10V4Z
CLRP1 SHORT PADS

PCH_RTCX1
PCH_RTCX2
R98 10M_0402_5%
Y1 32.768KHZ_12.5PF_CM31532768DZFT
C180 18P_0402_50V8J
C181 18P_0402_50V8J

+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS
R105 @ 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
★ LOW= Disable (Default)

+3V_PCH
R106 @ 1K_0402_5% HDA_SDOUT

★ Low = Disable (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH
R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
★ 1.8V when sampled low
Needs to be pulled High for Chief River platfrom

<30> HDA_BITCLK_AUDIO R112 33_0402_5% HDA_BIT_CLK
<30> HDA_SYNC_AUDIO R114 33_0402_5% HDA_SYNC_R
<30> HDA_RST_AUDIO# R116 33_0402_5% HDA_RST#
<30> HDA_SDOUT_AUDIO R118 33_0402_5% HDA_SDOUT

+3V_PCH @R121 200_0402_5% PCH_JTAG_TDO
+3V_PCH @R122 200_0402_5% PCH_JTAG_TMS
+3V_PCH @R123 200_0402_5% PCH_JTAG_TDI
@R125 100_0402_1%
@R126 100_0402_1%
@R128 100_0402_1%
DPDG1.1

CMOS
+RTCVCC
C183 1U_0603_10V4Z
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0603_10V4Z
CLRP2 SHORT PADS
CLRP3 SHORT PADS

U4A

PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
<30> HDA_SPKR HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
<30> HDA_SDIN0 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
<31> ME_FLASH ME_FLASH R109 0_0402_5% HDA_SDOUT A36 HDA_SDO
PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
+3V_PCH R107 10K_0402_5% @ R264 1K_0402_1% N32 HDA_DOCK_RST# / GPIO13
IHDA

PCH_JTAG_TCK R110 51_0402_5% J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

+5VS
Q10 LBSS138LT1G_SOT-23-3
HDA_SYNC
R878 1M_0402_5%
R175 @ 0_0402_5%
Del Q10 check with codec
VDDIO using 3VALW

SPI_CLK_PCH_R T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
SPI_SB_CS1# T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI

PANTHER-POINT_FCBGA989

LPC
FWH0 / LAD0 C38 LPC_AD0 → LPC_AD0 <25,31>
FWH1 / LAD1 A38 LPC_AD1 → LPC_AD1 <25,31>
FWH2 / LAD2 B37 LPC_AD2 → LPC_AD2 <25,31>
FWH3 / LAD3 C37 LPC_AD3 → LPC_AD3 <25,31>
EC and Mini card debug port
FWH4 / LFRAME# D36 LPC_FRAME# → LPC_FRAME# <25,31>
LDRQ0# E36
LDRQ1# / GPIO23 K36
R104 10K_0402_5% +3VS
SERIRQ V5 SERIRQ <31>

SATA 6G
SATA0RXN AM3 SATA_DTX_C_IRX_N0 → SATA_DTX_C_IRX_N0 <29>
SATA0RXP AM4 SATA_ITX_C_DRX_N0 0.01U_0402_25V7K C184 SATA_ITX_DRX_N0 → SATA_ITX_DRX_N0 <29>
SATA0TXN AP7 SATA_ITX_C_DRX_P0 0.01U_0402_25V7K C185 SATA_ITX_DRX_P0 → SATA_ITX_DRX_P0 <29>
SATA0TXP AP5
CAP on Comm. side
HDD
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10

SATA
SATA2RXN AD7 SATA_DTX_C_IRX_N2 → SATA_DTX_C_IRX_N2 <29>
SATA2RXP AD5 SATA_DTX_C_IRX_P2 → SATA_DTX_C_IRX_P2 <29>
SATA2TXN AH5 SATA_ITX_C_DRX_N2 → SATA_ITX_C_DRX_N2 <29>
SATA2TXP AH4 SATA_ITX_C_DRX_P2 → SATA_ITX_C_DRX_P2 <29>
ODD
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11 R111 37.4_0402_1% +1.05VS_VCC_SATA
SATAICOMPI Y10 SATA_COMP
SATA3RCOMPO AB12 R113 49.9_0402_1% +1.05VS_SATA3
SATA3COMPI AB13 SATA3_COMP
SATA3RBIAS AH1 RBIAS_SATA3 R115 750_0402_1%
SATALED# P3 SATALED#
GPIO21 V14 PCH_GPIO21
SATA0GP / GPIO21 V14 BBS_BIT0_R
SATA1GP / GPIO19 P1
R117 10K_0402_5% +3VS
R119 10K_0402_5% +3VS
R187 10K_0402_5% +3VS

HM76@ U4 HM70@
BD82HM70 SJTNV C1
SA00005MQ80

SPI_CLK_PCH_R
R124 33_0402_5% @
R124;c190 close to U4.T3 pin
C190 22P_0402_50V8J @

+3VS
R266 3.3K_0402_5% SPI_WP#1
R221 3.3K_0402_5% SPI_HOLD#1
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#

8MB SPI ROM FOR ME & Non-share ROM.

SPI_SB_CS1# R291 0_0402_5% SPI_CS1#
SPI_SO_R SPI_SO1
SPI_WP#1
R188 33_0402_5%
U6 16M W25Q16BVSSIG SOIC 8P
CS# VCC
SO HOLD#
WP# SCLK
GND SI
+3VS
SPI_HOLD#1
SPI_CLK1
SPI_SI1
R199 0_0402_5% SPI_CLK_PCH_R
SPI_SI
R196 33_0402_5%

U6 Rerserver 4M+2M Solution

SPI_SB_CS0# R130 0_0402_5% SPI_SO_L
SPI_SO_R SPI_WP#
R131 33_0402_5%
U5 32M W25Q32BVSSIG SOIC 8P
CS# VCC
SO HOLD#
WP# SCLK
GND SI
+3VS
C191 0.1U_0402_16V4Z
SPI_HOLD#
SPI_CLK_PCH
SPI_SI_R
R132 0_0402_5% SPI_CLK_PCH_R
SPI_SI
R133 33_0402_5%

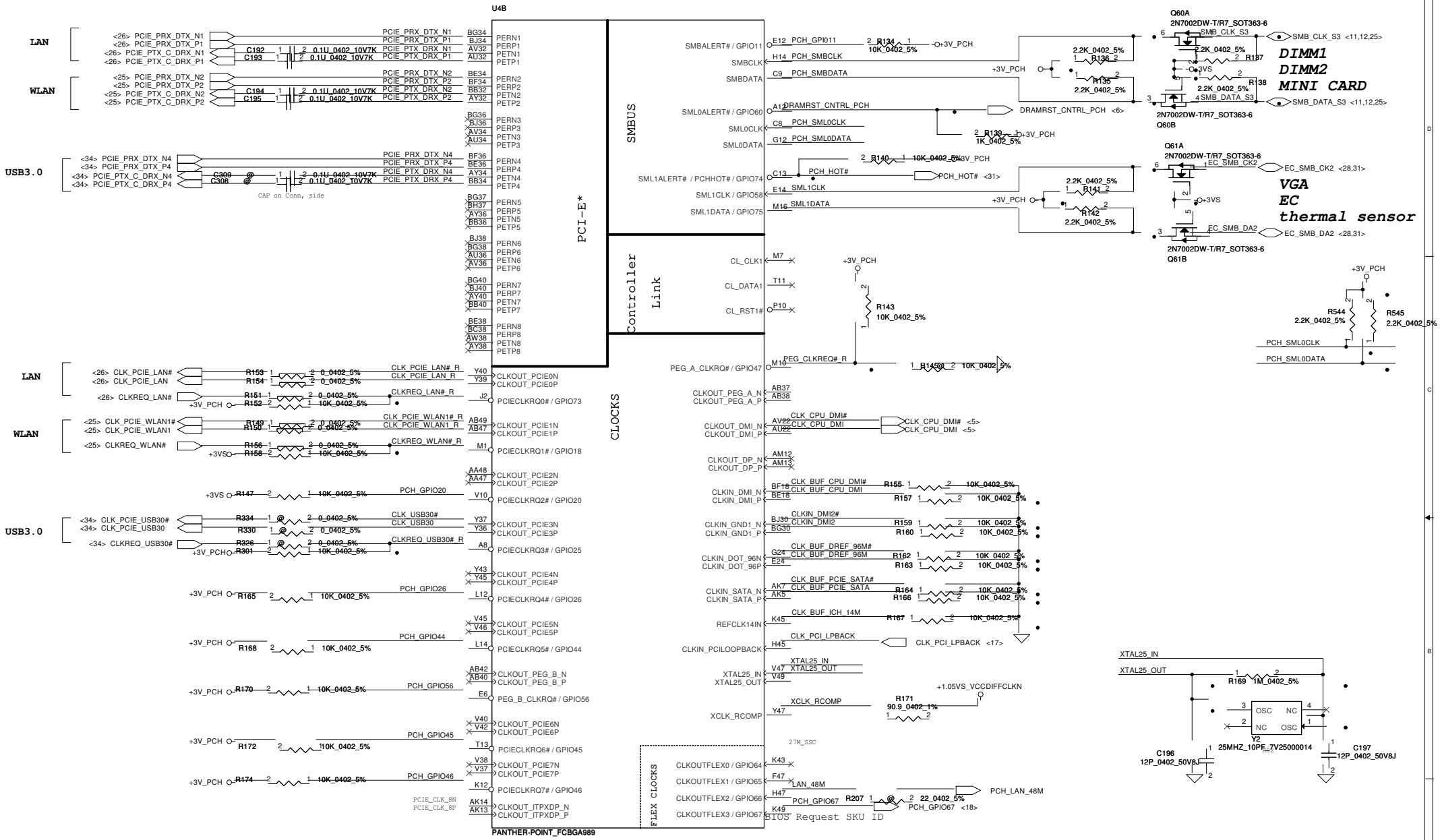
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: LA-7987P | Rev: 1.0

Date: Tuesday, October 30, 2012 | Sheet 13 of 50



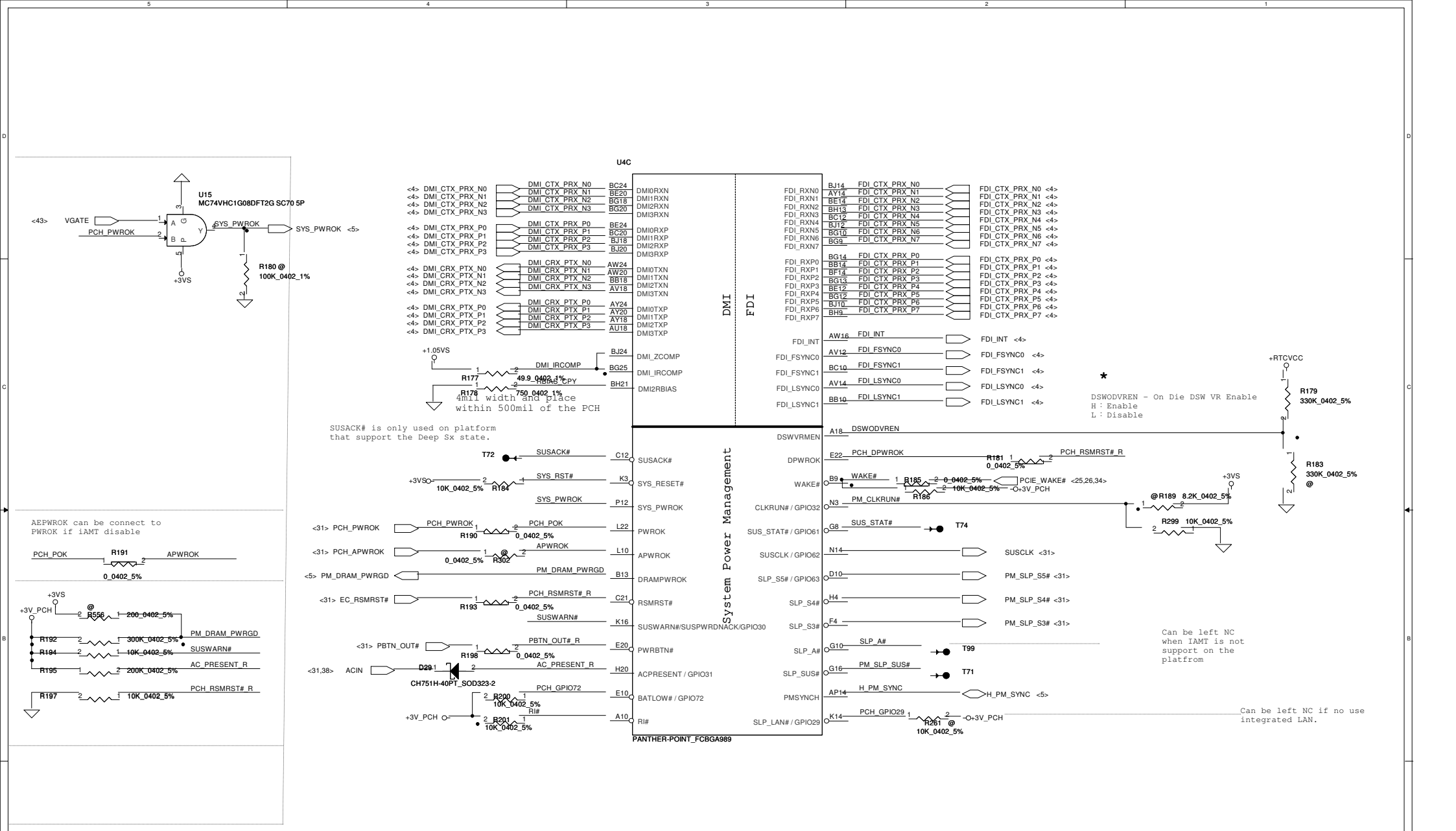
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-7987P	1.0

Date: Tuesday, October 30, 2012 | Sheet 14 of 50



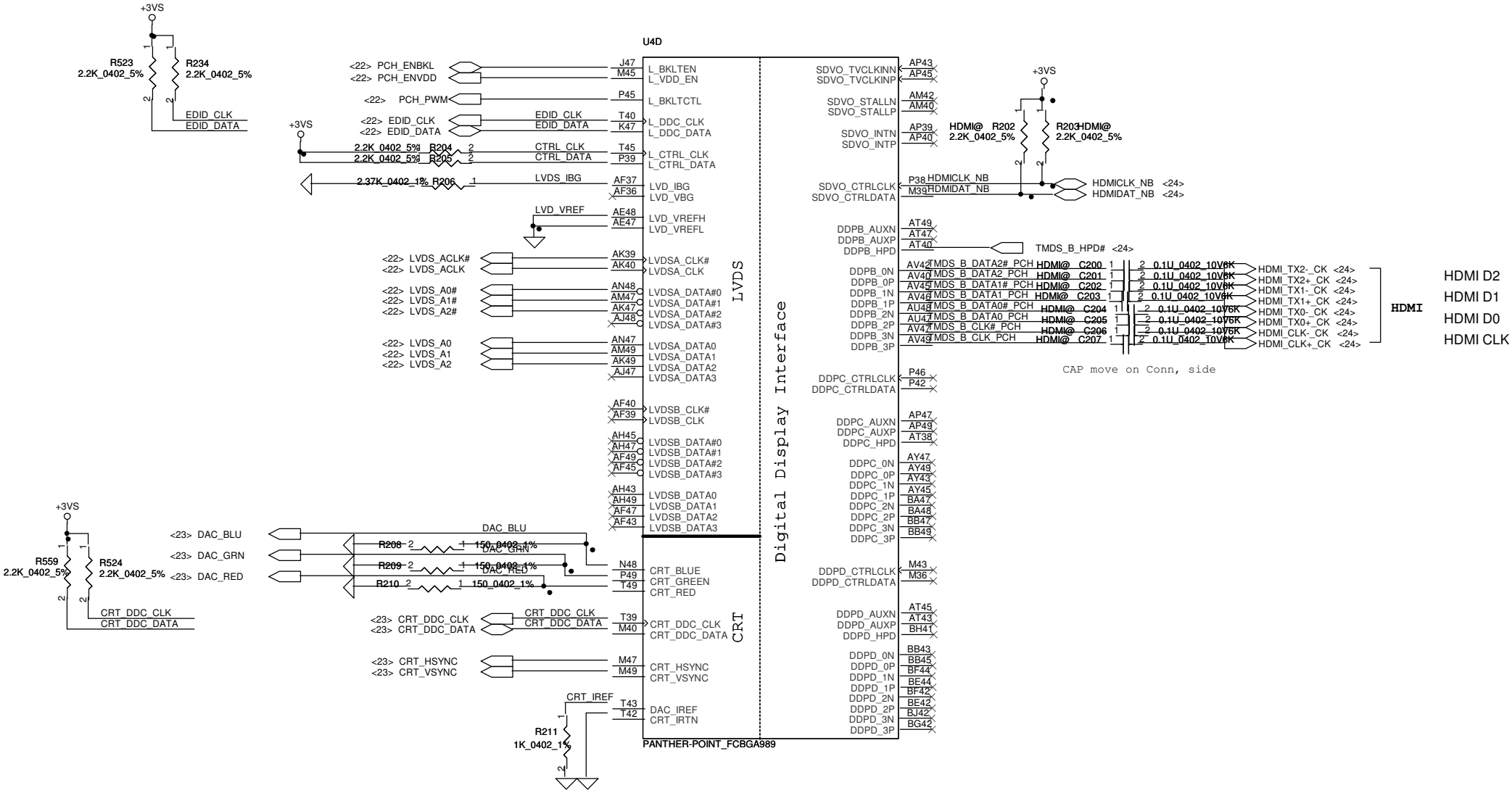
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom | Document Number: LA-7987P | Rev: 1.0

Date: Tuesday, October 30, 2012 | Sheet 15 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size	Document Number	Rev
B	LA-7987P	1.0

Date: Tuesday, October 30, 2012 Sheet 16 of 50

+3VS

RP2
8 7 6 5 — 1 2 3 4
PCI_PIRQA#
PCI_PIRQD#
PCI_PIRQC#
PCI_PIRQB#
8.2K_0804_8P4R_5%

RP1
8 7 6 5 — 1 2 3 4
PCH_GPIO2
DGPU_PWR_EN_R
PCH_GPIO4
ODD_DA#_R
8.2K_0804_8P4R_5%

R213 1 2 8.2K_0402_5% PCH_GPIO5
R225 1 2 8.2K_0402_5% PCH_WL_OFF#
R292 1 @ 2 8.2K_0402_5% PCH_GPIO51
R557 1 @ 2 8.2K_0402_5% PCH_GPIO53
R259 1 2 8.2K_0402_5% DGPU_PWR_EN1
R212 1 2 8.2K_0402_5% DGPU_HOLD_RST#_R
R214 1 @ 2 8.2K_0402_5% DGPU_HOLD_RST#_R

PPT EDS DOC#474146

Boot BIOS Strap bit1 BBS1

	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	Reserved
	1	1	* SPI (Default)
	0	0	LPC

GPIO55

PCH_WL_OFF# — R215 1 @ 2 1K_0402_5%

A16 swap overide Strap/Top-Block Swap Override jumper

PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

U4E

RSVD: TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24

USB3: USB3_RX1_N USB3_RX2_N USB3_RX3_N USB3_RX4_N USB3_RX1_P USB3_RX2_P USB3_RX3_P USB3_RX4_P USB3_TX1_N USB3_TX2_N USB3_TX3_N USB3_TX4_N USB3_TX1_P USB3_TX2_P USB3_TX3_P USB3_TX4_P
T1829 T1825 T1832 T1826 T1831 T1827 T1830 T1828

PCI: PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD# DGPU_HOLD_RST#_R DGPU_PWR_EN1 DGPU_PWR_EN_R PCH_GPIO51 PCH_GPIO53 PCH_WL_OFF# PCH_GPIO2 ODD_DA#_R PCH_GPIO4 PCH_GPIO5 PCH_PME# PCH_PLTRST# CLK_PCI_LPBACK_R CLK_PCI_EC_R CLK_PCI_DB_R

USB: USB20_N0 USB20_P0 USB20_N1 USB20_P1 USB20_N2 USB20_P2 USB20_N3 USB20_P3 USB20_N8 USB20_P8 USB20_N9 USB20_P9 USB20_N10 USB20_P10 USB20_N11 USB20_P11

USB DEBUG=PORT1 AND PORT9

USB20_N0 / USB20_P0	LEFT USB (USB 3.0)	
USB20_N1 / USB20_P1	LEFT USB (CR-B/D USB)	
USB20_N2 / USB20_P2	USB Camera	
USB20_N3 / USB20_P3		
USB20_N8 / USB20_P8	Bluetooth	
USB20_N9 / USB20_P9	RIGHT USB	
USB20_N10 / USB20_P10	WLAN	
USB20_N11 / USB20_P11	CARD READER	

USBRBIAS — C33 1 — R218 2 200_0402_1% — Within 500 mils

USB_OC0# Share with USB_OC4# due to same power switch

USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC5# SMIB USB_OC7#

+3V_PCH

RP3 10K_1206_8P4R_5%: USB_OC2# USB_OC7# USB_OC0# USB_OC1# USB_OC3#

RP4 10K_1206_8P4R_5%: SMIB — R262 — 10K_0402_5%

PANTHER-POINT_FCBGA989

<34> USB3_RX1_N <34> USB3_RX2_N
<34> USB3_RX1_P <34> USB3_RX2_P
<34> USB3_TX1_N <34> USB3_TX2_N
<34> USB3_TX1_P <34> USB3_TX2_P

<25> PCH_WL_OFF#
<29,31> ODD_DA# — R715 1 @ 2 0_0402_5%
<31> PCI_PME#
<5> PCH_PLTRST#
<14> CLK_PCI_LPBACK — 22_0402_5% — R219
<31> CLK_PCI_EC
<25> CLK_PCI_DB — 22_0402_5% — @ — R220

R222 1 2 0_0402_5%
<25,26,31,34> PLT_RST#
U7@ MC74VHC1G08DFT2G SC70 5P
PCH_PLTRST#
C208 @ 1U_0402_6.3V4Z
R223 100K_0402_5%
+3VS

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (5/9) PCI, USB
Size: Custom
Document Number: LA-7987P
Rev: 1.0
Date: Tuesday, October 30, 2012
Sheet 17 of 50

PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

Reserved for BIOS Request

PCH_GPIO70	Function
0	14/15"
1	17"
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

+3V_PCH

Weak internal pull-high

R235 2 10K_0402_5% EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

R244 @ 10K_0402_5% PCH_GPIO37 R881 10K_0402_5%

R250 @ 10K_0402_5% PCH_GPIO36 R547 10K_0402_5%

BIOS Request SKU ID

R711 10K_0402_5% R245 10K_0402_5% PCH_GPIO38 PCH_GPIO67 PCH_GPIO67 <14>

R709 @ 10K_0402_5% R298 @ 10K_0402_5%

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

U4F

GPIO

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 PCH_GPIO71
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15		
U2	SATA4GP / GPIO16		
D40	TACH0 / GPIO17		
T5	SCLOCK / GPIO22		
E8	GPIO24		
E16	GPIO27		
P8	GPIO28		
K1	STP_PCI# / GPIO34		
K4	GPIO35		
V8	SATA2GP / GPIO36		
M5	SATA3GP / GPIO37		
N2	SLOAD / GPIO38		
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48		
V3	SATA5GP / GPIO49 / TEMP_ALERT#		
D6	GPIO57		

CPU/MISC

P4	A20GATE	GATEA20 <31>
AU16	PECI	H_PECI <5,31>
P5	RCIN#	KBRST# <31>
AY11	PROCPWRGD	H_CPUPWRGD <5>
AY10	THRMTRIP#	H_THRMTRIP# <5>
T14	INIT3_3V#	
AY1	DF_TVS	
AH8	TS_VSS1	
AK1	TS_VSS2	
AH10	TS_VSS3	
AK10	TS_VSS4	
P37	NC_1	

NCTF

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

PANTHER-POINT_FCBGA989

R233 10K_0402_5% PCH_GPIO1
R227 10K_0402_5% PCH_GPIO6
R228 10K_0402_5% EC_SCI#
EC_SMI#
R229 @ 10K_0402_5% PCH_GPIO12
R230 1K_0402_5% EC_LID_OUT#
R231 10K_0402_5% PCH_GPIO16
R232 @ 10K_0402_1% DGPU_PWROK_R
R238 10K_0402_5% BT_DISABLE
ODD_EN
R241 10K_0402_5% PCH_GPIO27
R242 10K_0402_5% PCH_BT_ON#
R243 10K_0402_5% PCH_GPIO35
PCH_GPIO36
R247 10K_0402_5% PCH_GPIO39
R248 10K_0402_5% PCH_GPIO48
R249 10K_0402_5% PCH_GPIO49
R251 10K_0402_5% PCH_GPIO57

R702 10K_0402_5% PCH_GPIO69 @R707 10K_0402_5%

@R703 10K_0402_5% PCH_GPIO70 R02 R705 200K_0402_5%

@R704 10K_0402_5% PCH_GPIO71 R02 R706 200K_0402_5%

R236 10K_0402_5%

PCH_PECI_R 0_0402_5% R237

KBRST# R226 10K_0402_5%

PCH_THRMTRIP#_R R239 390_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

R216 2.2K_0402_5%

NV_CLE R217 1K_0402_5% H_SNB_IVB# <5>

Weak internal PU,Do not pull low

CLOSE TO THE BRANCHING POINT

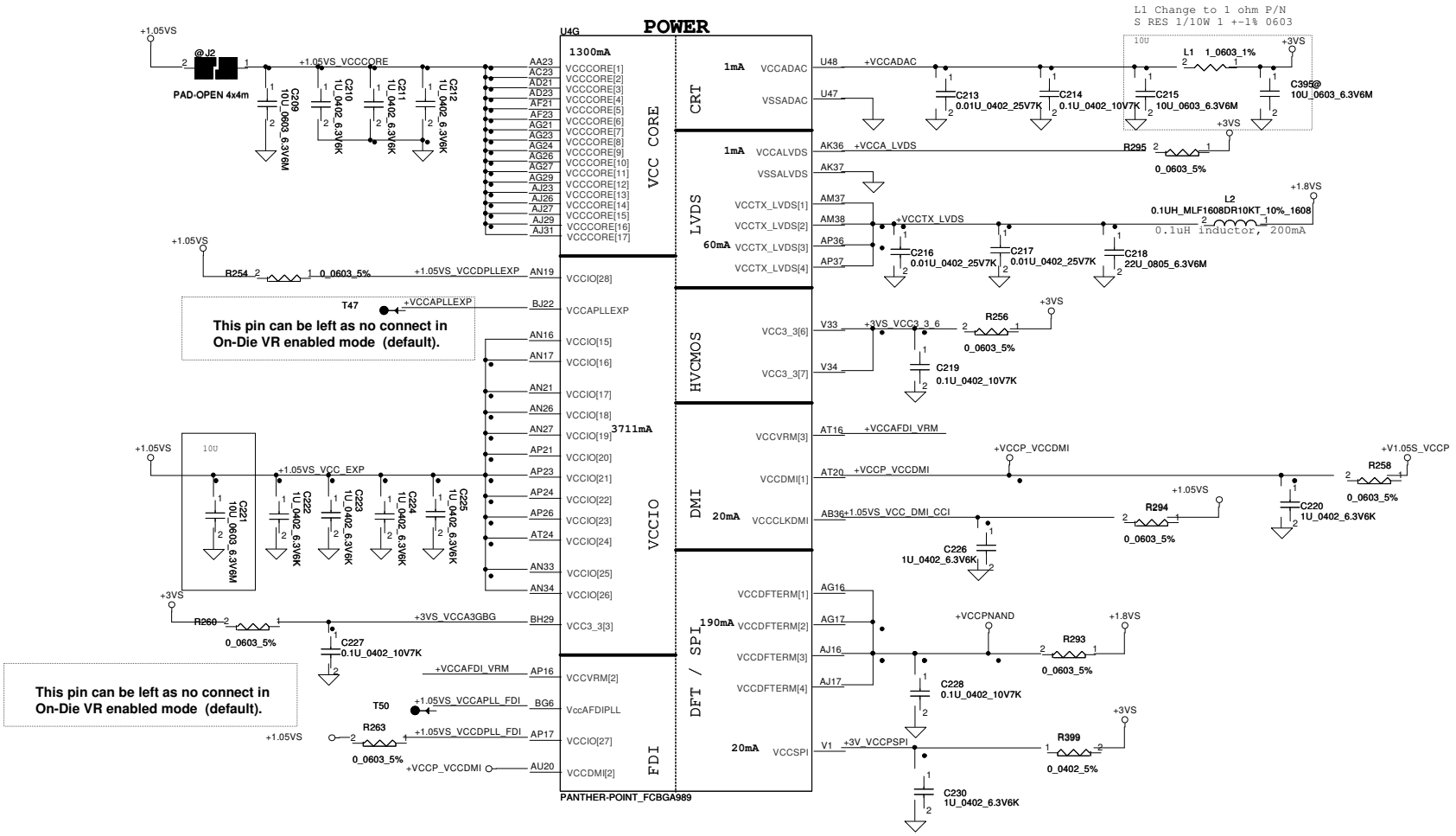
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-7987P	1.0

Date: Tuesday, October 30, 2012 Sheet 18 of 50

Compal Electronics, Inc.



PCH Power Rail Table
Refer to CPU EDS R1.5

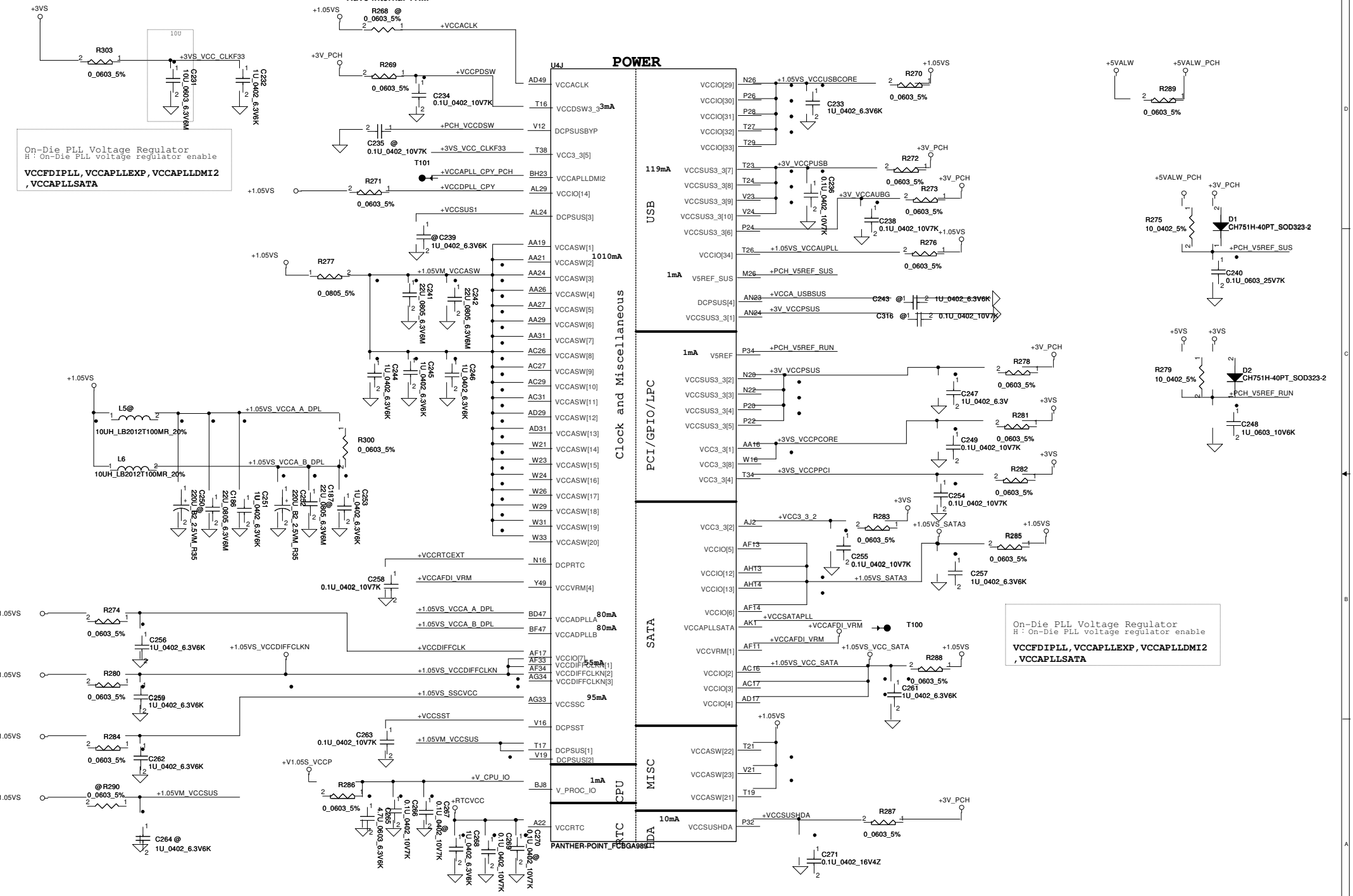
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-7987P | Rev: 1.0

Date: Tuesday, October 30, 2012 | Sheet 19 of 50



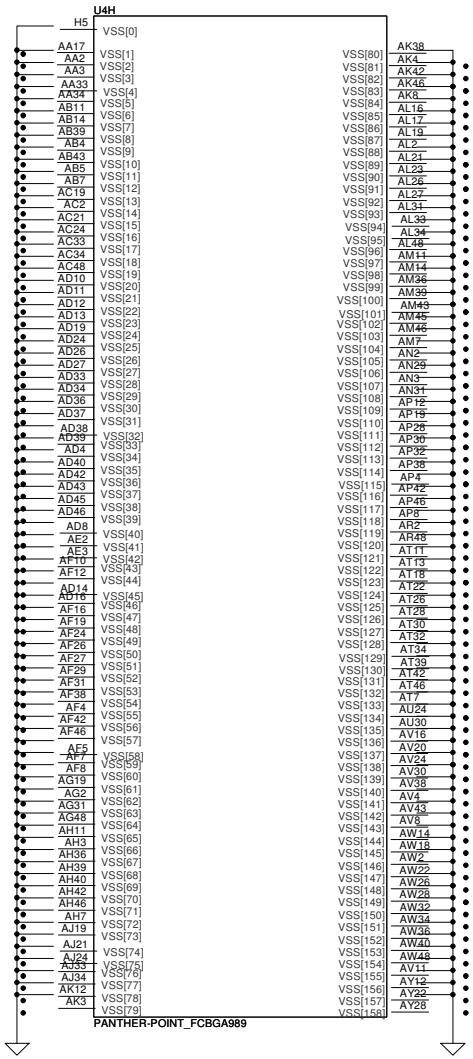
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

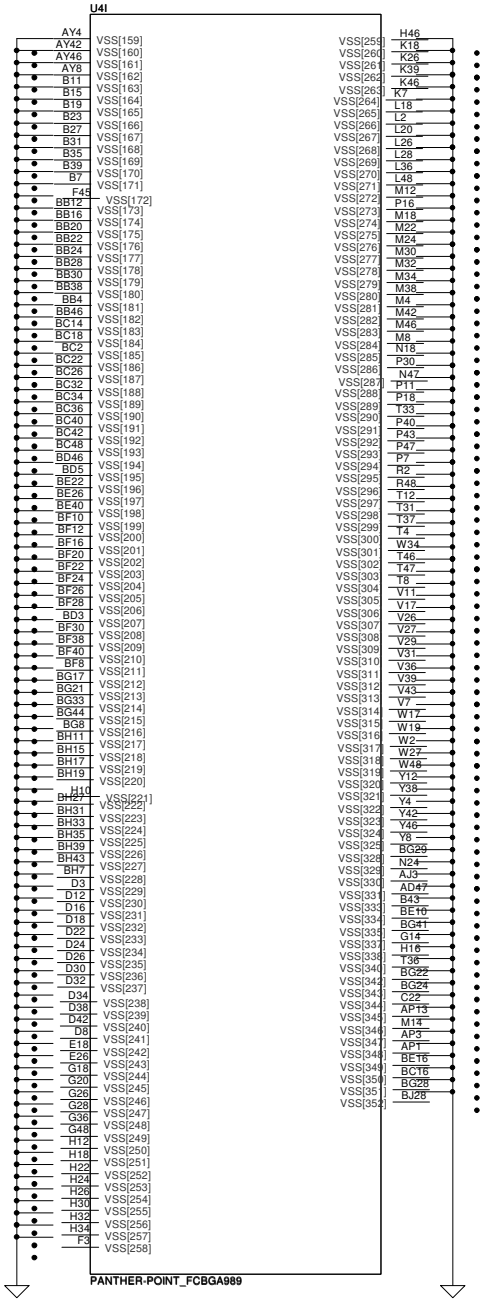
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-7987P | Rev: 1.0

Date: Tuesday, October 30, 2012 | Sheet 20 of 50





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

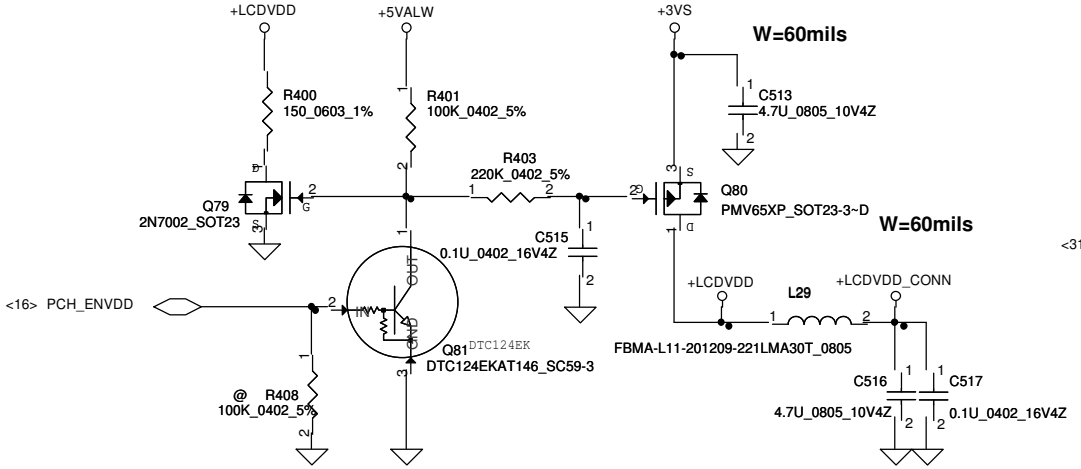
Compal Electronics, Inc.

Title: PCH (9/9) VSS

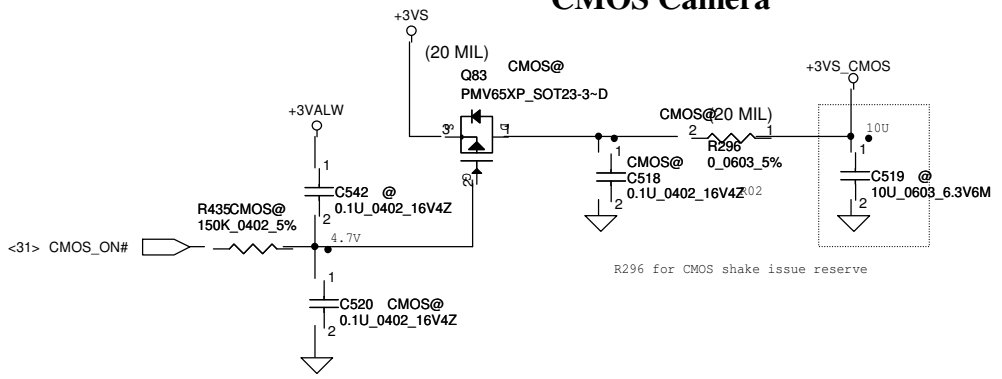
Size: Custom | Document Number: LA-7987P | Rev: 1.0

Date: Tuesday, October 30, 2012 | Sheet 21 of 50

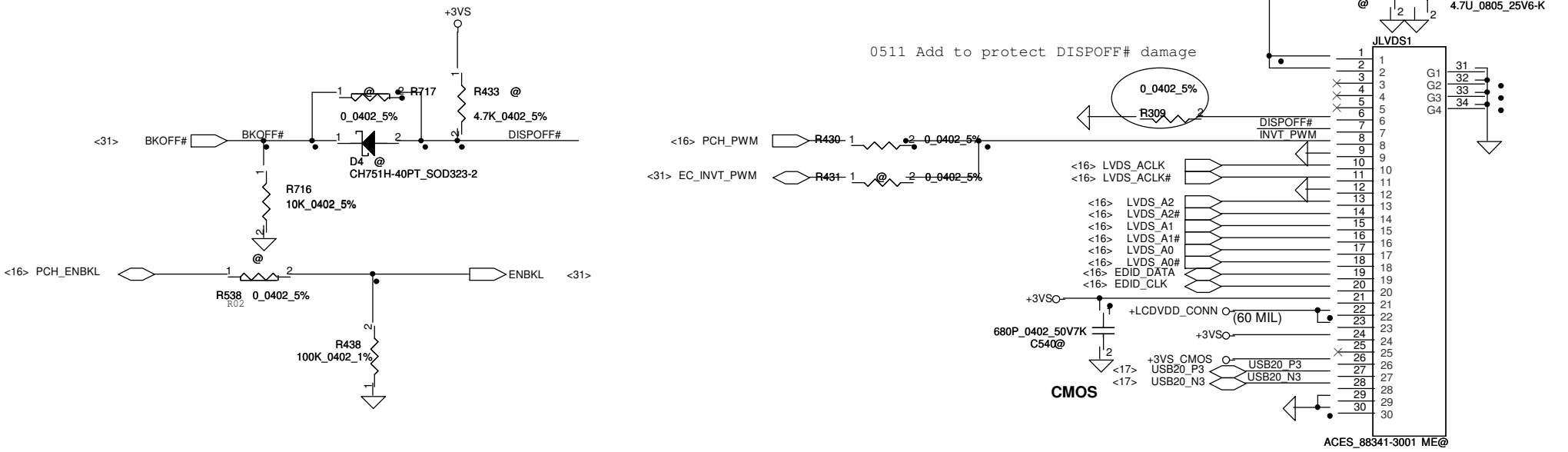
LCD POWER CIRCUIT



CMOS Camera



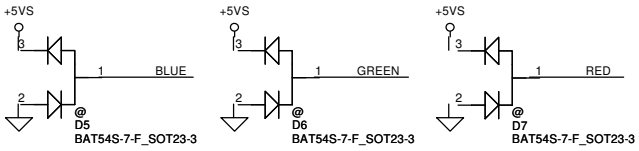
VGA LCD/PANEL BD. Conn.

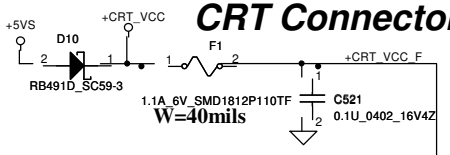


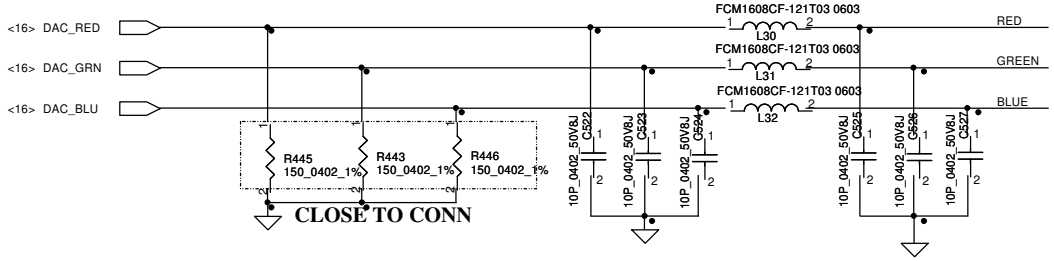
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

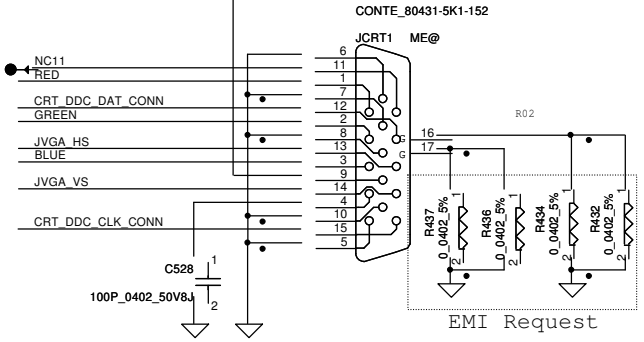
Compal Electronics, Inc.		
Title: LVDS/CAMERA		
Size: Custom	Document Number: LA-7987P	Rev: 1.0
Date: Tuesday, October 30, 2012	Sheet 22 of 50	

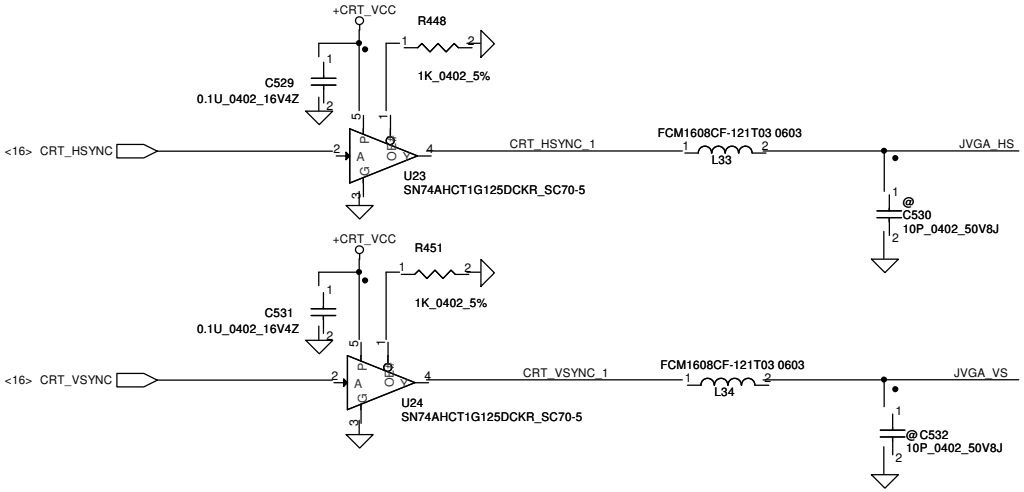
CRT Connector

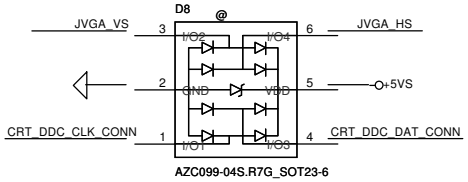


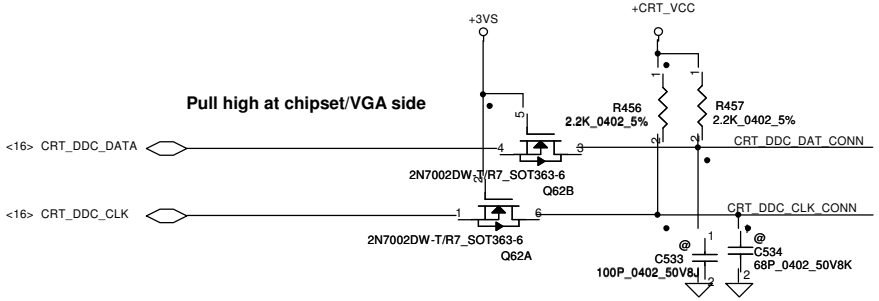












Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	LA-7987P	1.0

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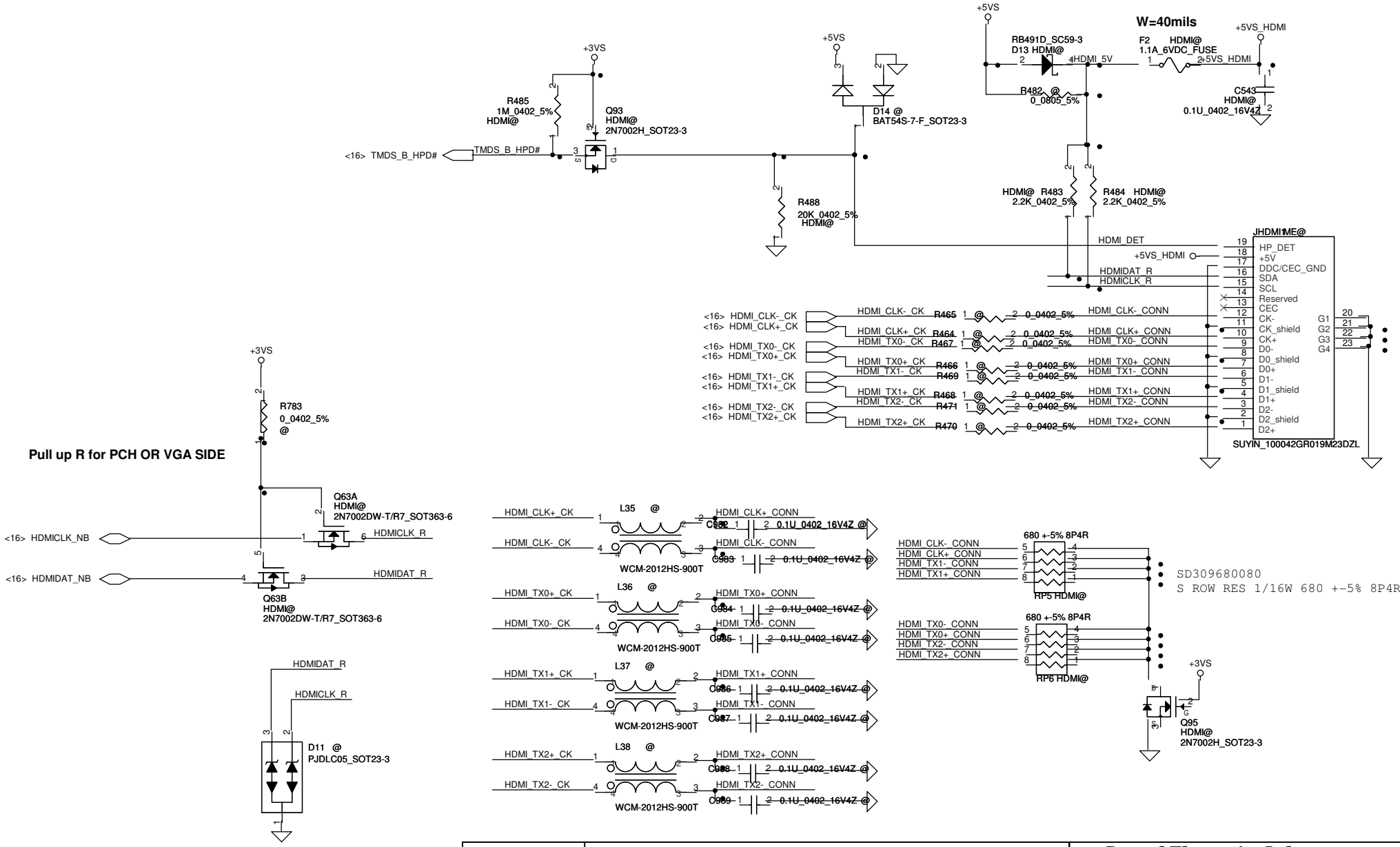

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-7987P	1.0

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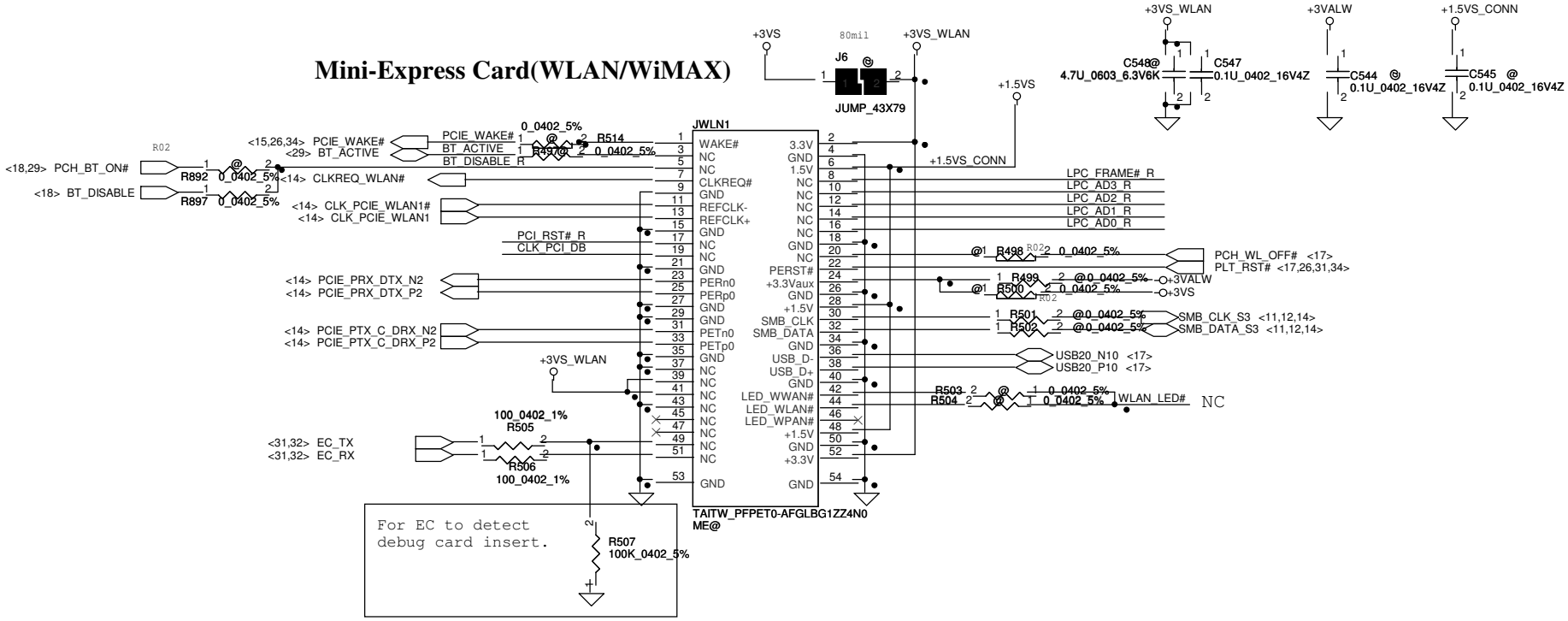
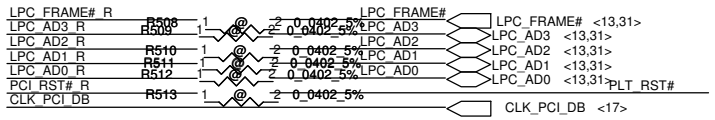
Mini-Express Card for WLAN/WiMAX(Half)

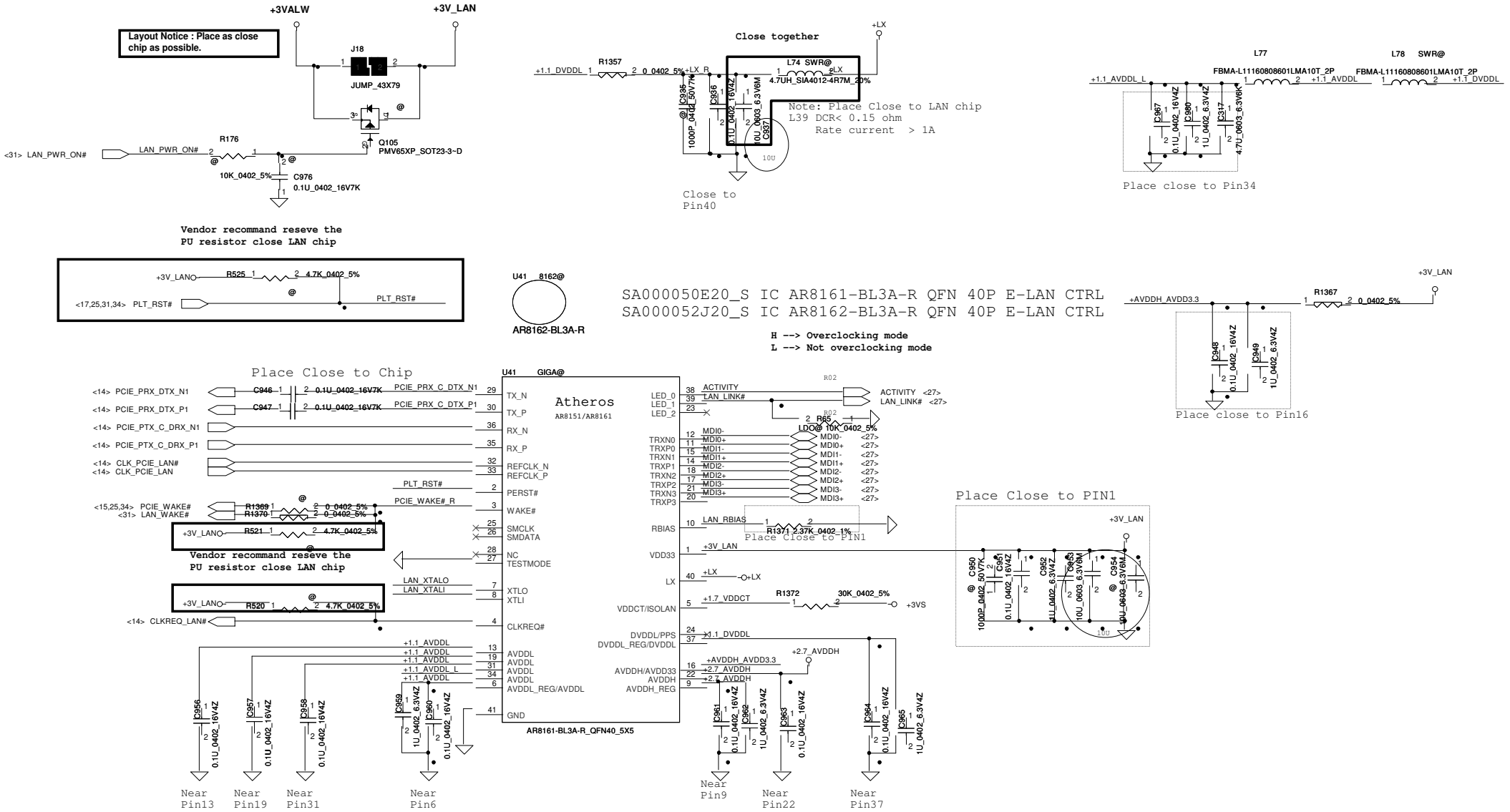


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



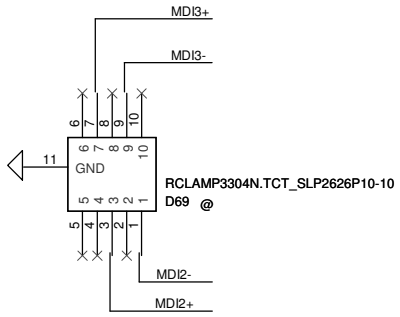
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: Mini-Card/NEW Card/SIM			
Size	Document Number: LA-7987P		Rev: 1.0
Date: Tuesday, October 30, 2012	Sheet 25 of 50		

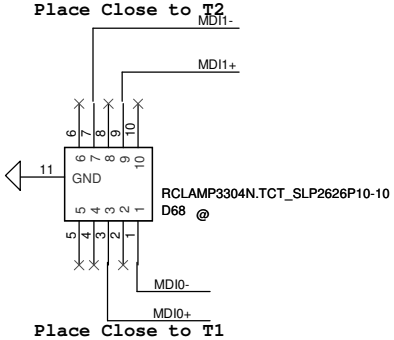


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

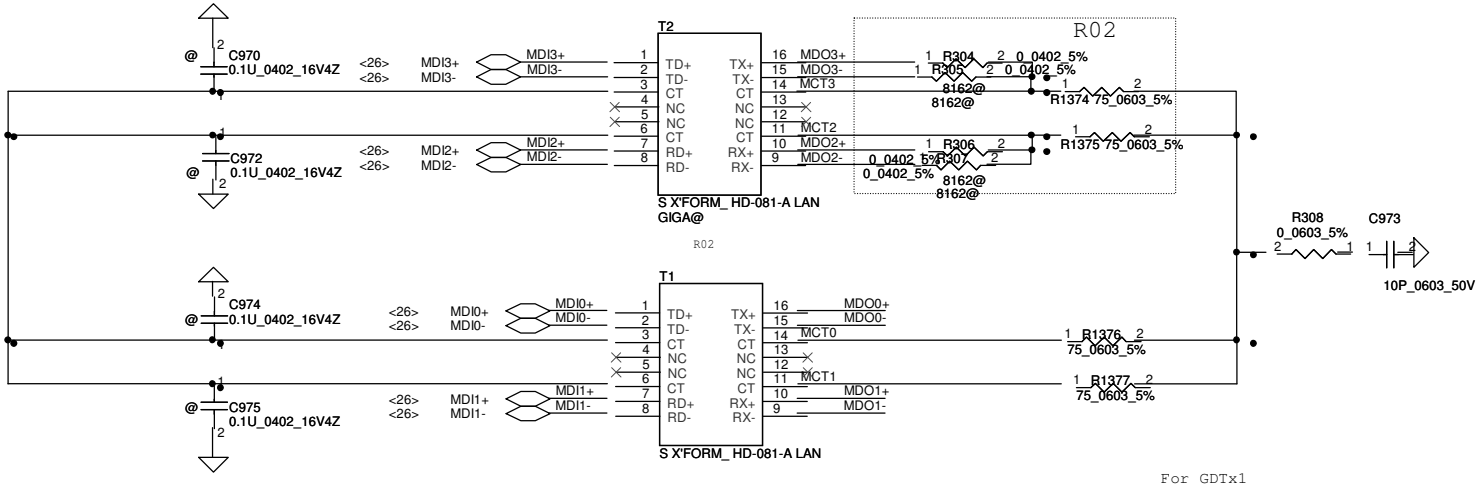
Compal Electronics, Inc.	
Title	LAN-AR8151/8161
Size: Custom	Document Number: LA-7987P
Rev	1.0
Date: Tuesday, October 30, 2012	Sheet 26 of 50



Place Close to T2

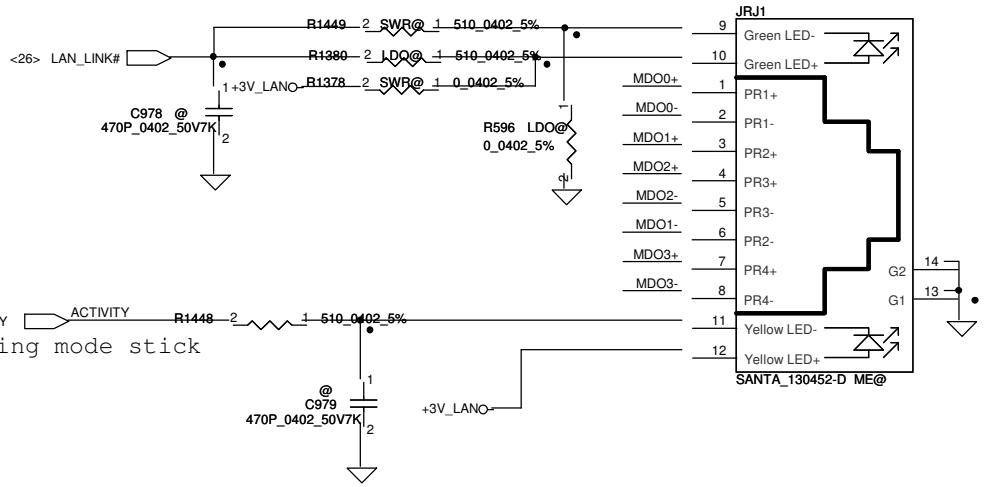


Place Close to T1

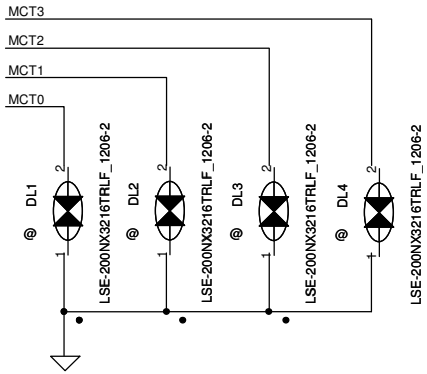


For GDTx1
DL1- Mount
DL2/DL3/DL4- NC
R308- 75 ohm
R1374/R1375/R1376/R1377- 0 ohm

LDO Mode: pop R1380;R596
SWR Mode: pop R1449;R1378



Overclocking mode stick



Reserve for EMI go rural solution

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	LAN_Transformer		
Size	Document Number		Rev
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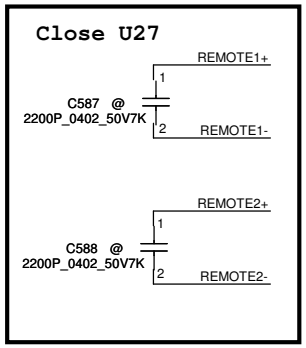
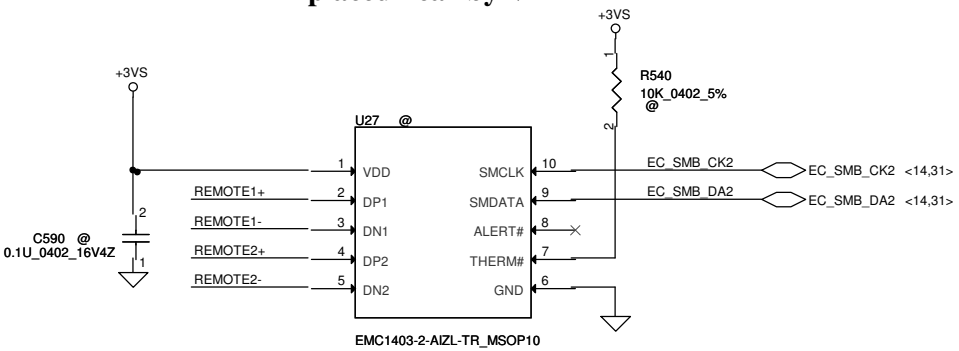
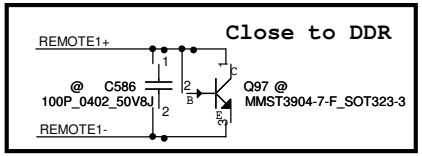
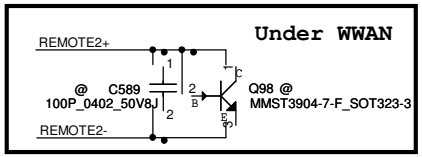
SMSC thermal sensor placed near by VRAM



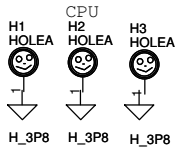


Address 1001_101xb

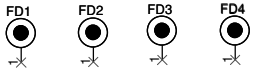




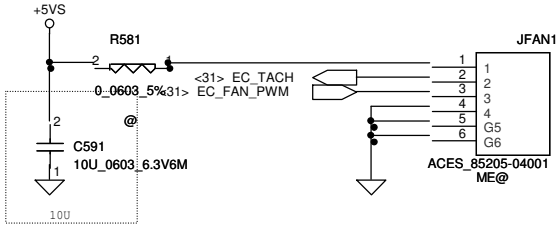
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

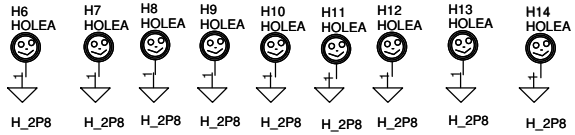


A



FAN1 Conn



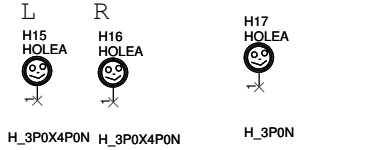


D

2P8 * 9 pcd

M/B 橢圓孔 L R

M/B 圓孔

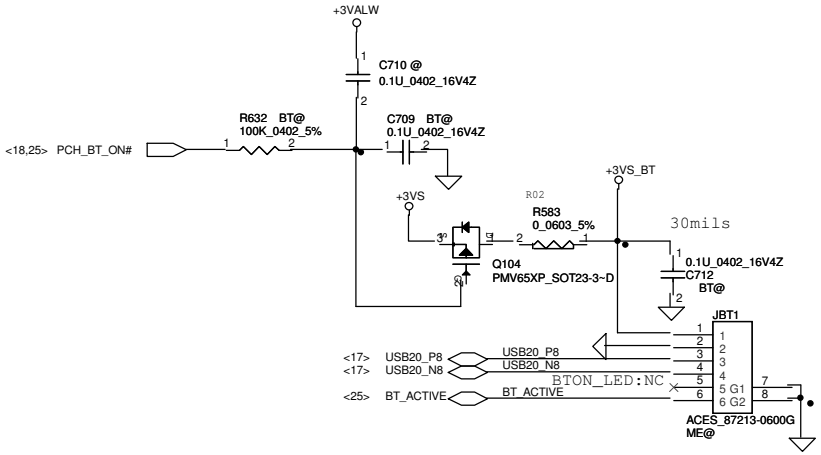


E

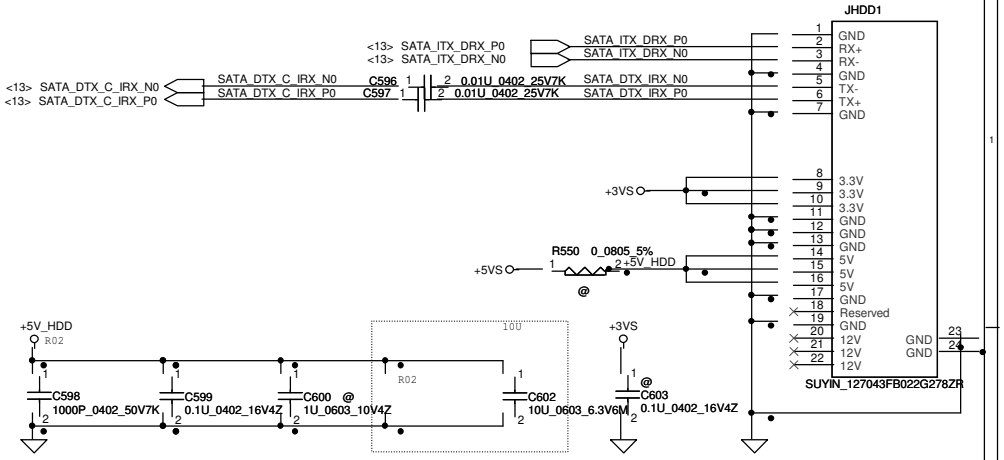
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.			
Title: Fintek-Thermal IC/FAN/screw			
Size: B	Document Number: LA-7987P		Rev: 1.0
Date: Tuesday, October 30, 2012	Sheet 28 of 50		

BT MODULE CONN

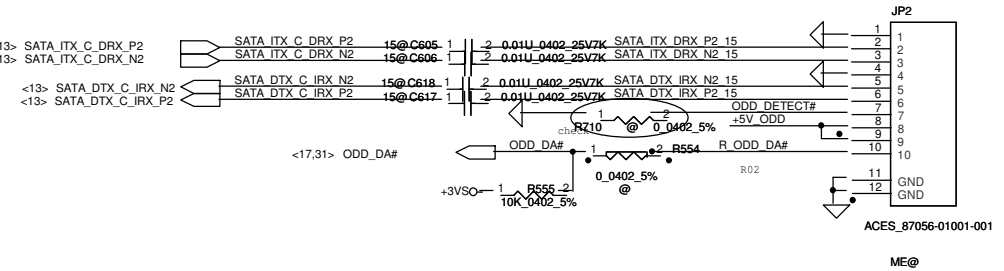


SATA HDD Conn.



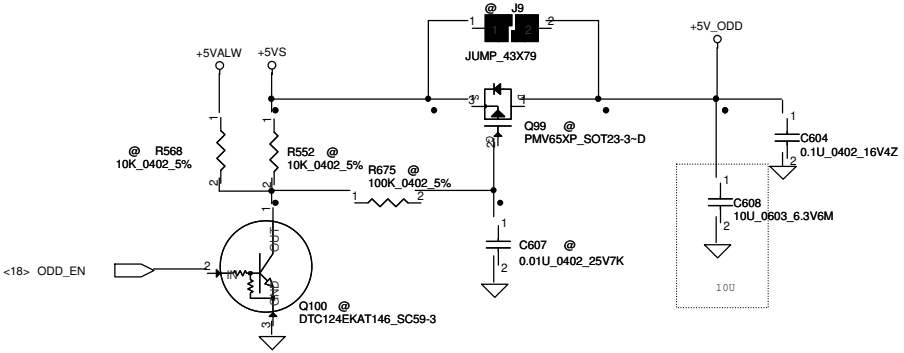
FOR 15"

SATA ODD FFC Conn.



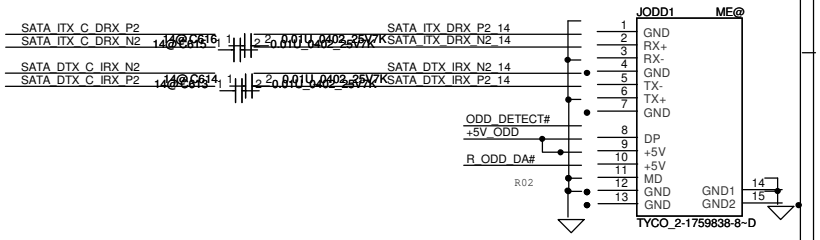
Co-lay

ODD Power Control



FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-7987P	1.0

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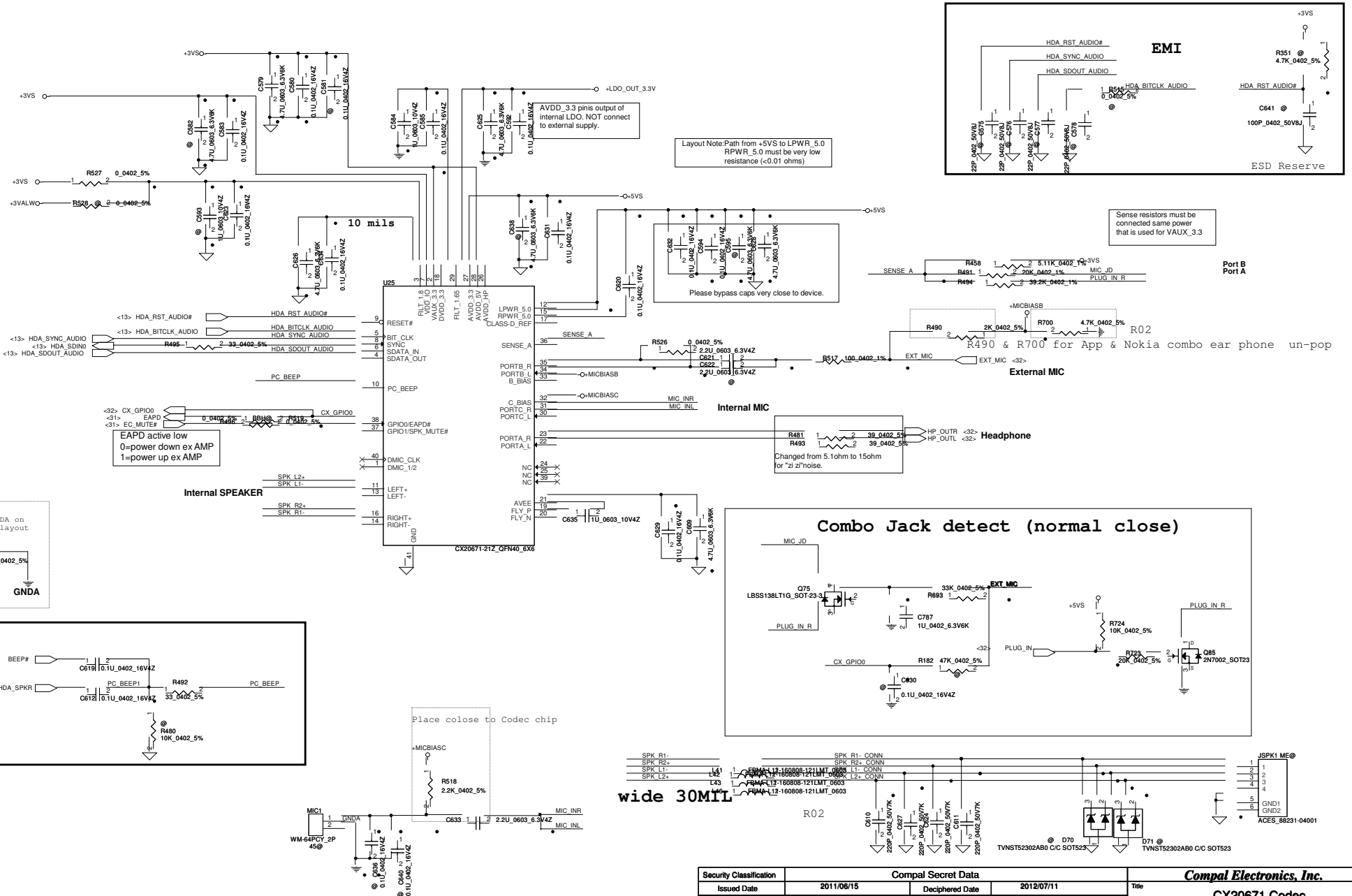
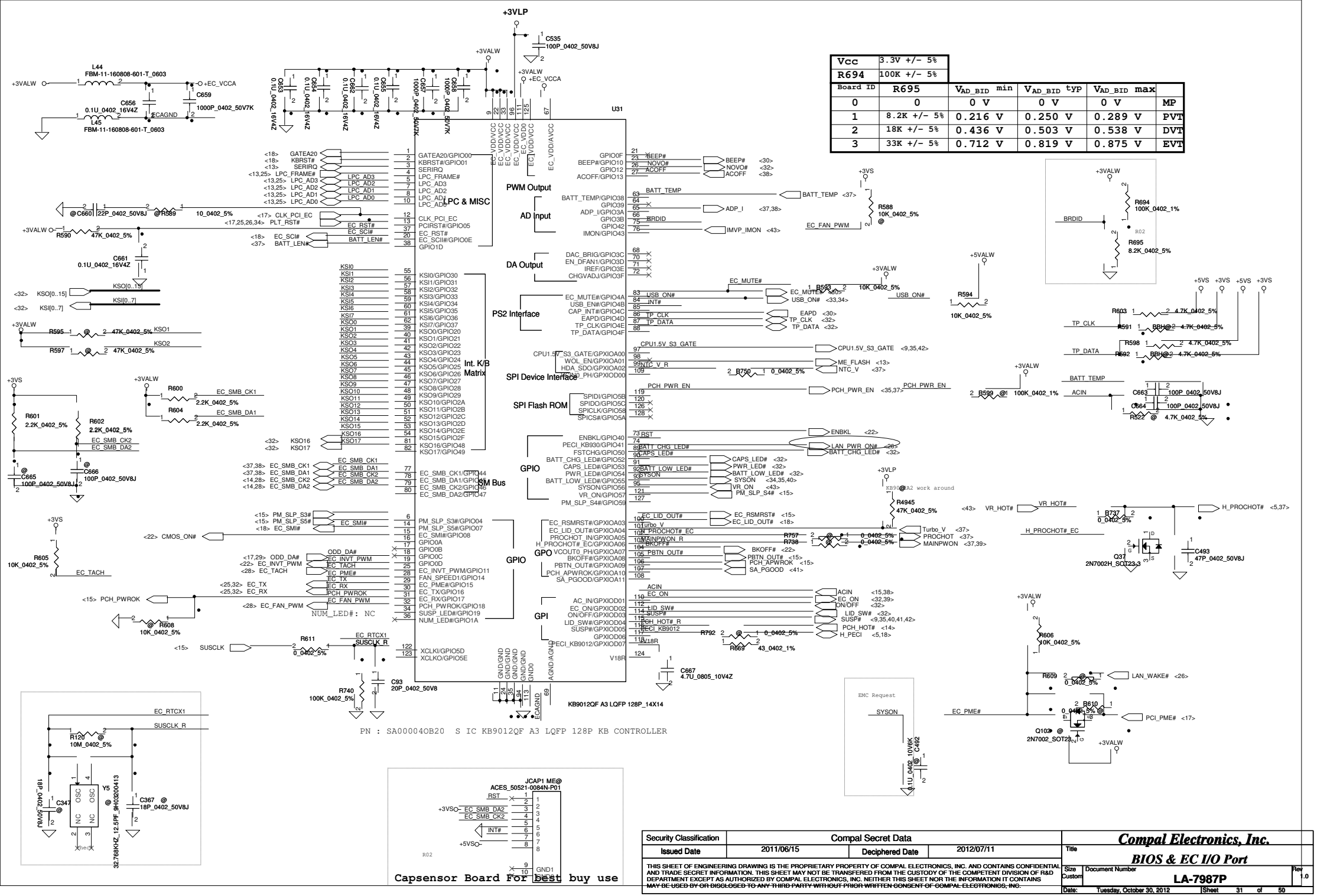
CX20671
High Definition Audio Codec SoC With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).

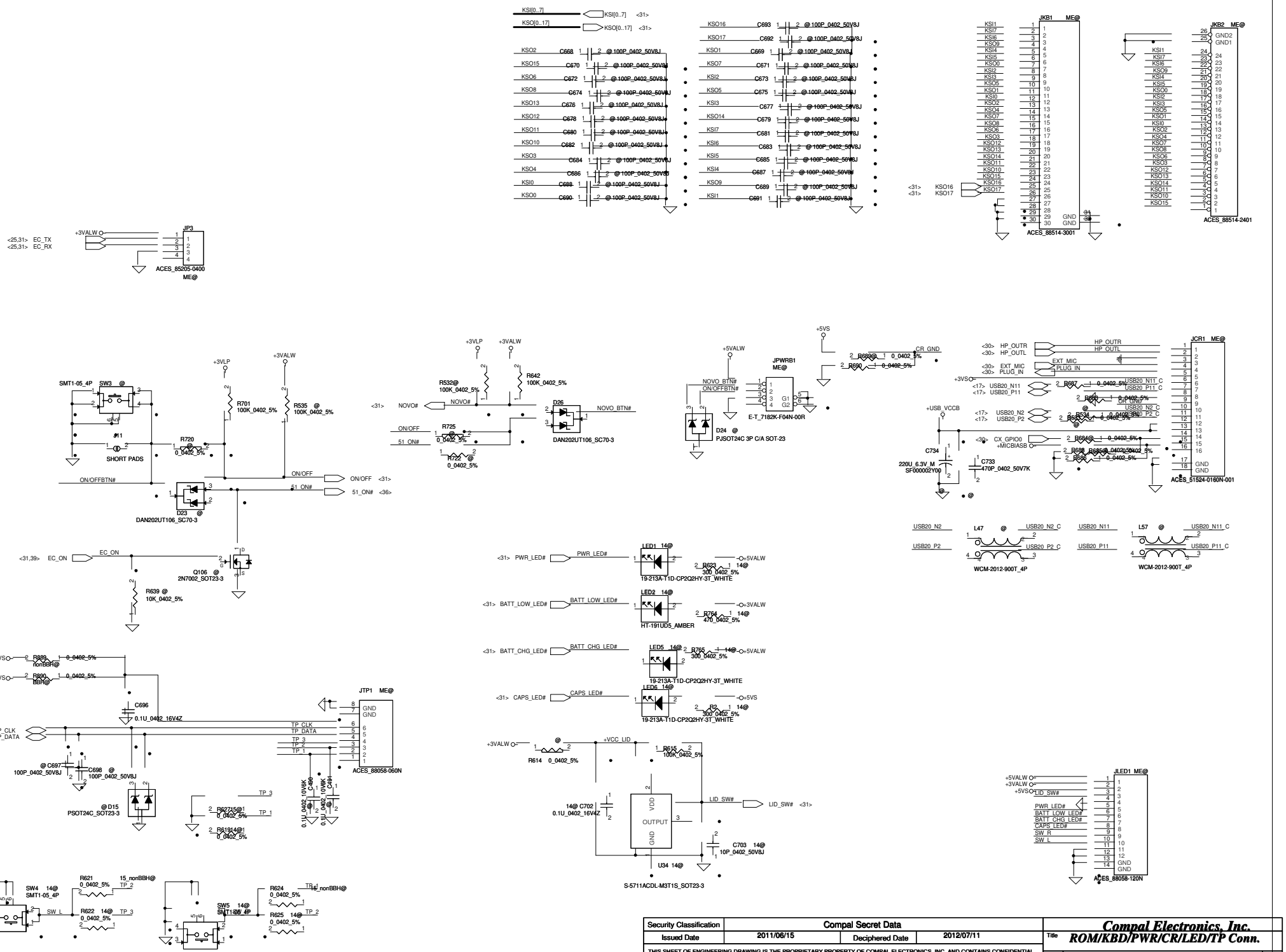




Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

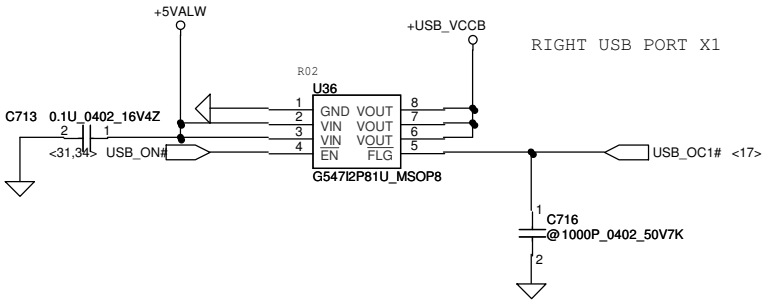
Compal Electronics, Inc.			
Title: BIOS & EC I/O Port			
Size: Custom	Document Number: LA-7987P		Rev: 1.0
Date: Tuesday, October 30, 2012	Sheet 31 of 50		

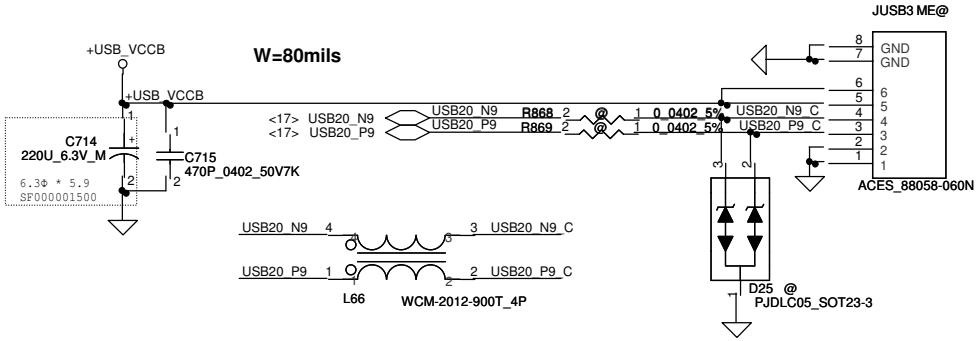


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: ROM/KBD/PWR/CR/LED/TP Conn.			
Size: C	Document Number: LA-7987P		Rev: 1.0
Date: Tuesday, October 30, 2012	Sheet 32 of 50		

Right Ext.USB Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: USB ext. ports

Size	Document Number	Rev
B	LA-7987P	1.0

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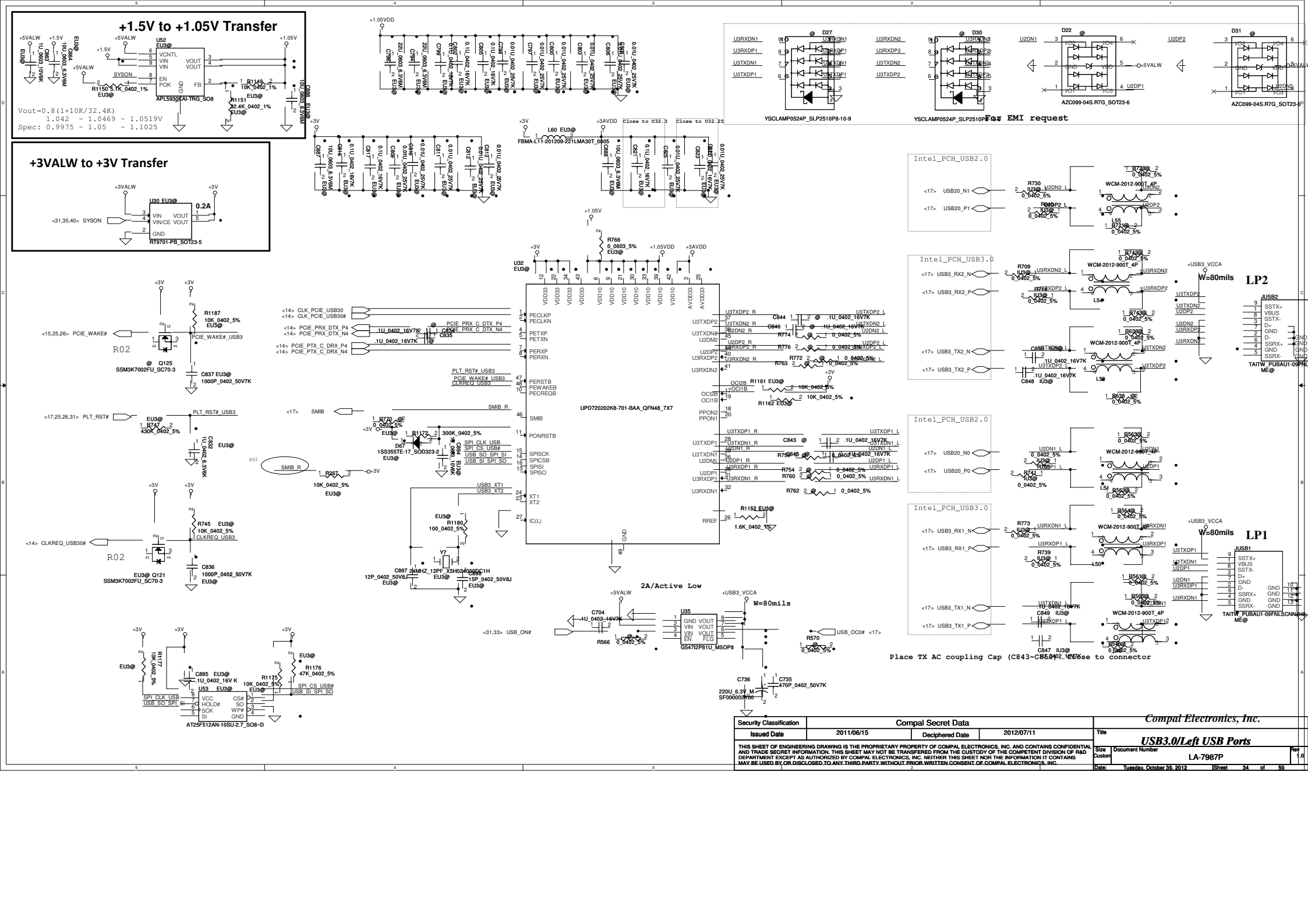
+1.5V to +1.05V Transfer
Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025
APL5930KAI-TRG_SO8
+3VALW to +3V Transfer
RT9701-PB_SOT23-5
0.2A
+1.05VDD
+3AVDD
+3VALW
+1.5V
+1.05V
+3V
+5VALW
+3AVDD
+USB3_VCCA
W=80mils
2A/Active Low
For EMI request
Intel_PCH_USB2.0
Intel_PCH_USB3.0
LP2
LP1
UPD720202K8-701-BAA_QFN48_7X7
YSCLAMP0524P_SLP2510P8-10-9
AZC099-04S.R7G_SOT23-6
AZC099-04S.R7G_SOT23-5
FBMA-L11-201209-221LMA30T_0805
SSM3K7002FU_SC70-3
AT25F512AN-10SU-2.7_SO8-D
TAITW_PUBAU1-09FNLSCNN4HE
Place TX AC coupling Cap (C843~C850) close to connector
Security Classification
Compal Secret Data
Issued Date
2011/06/15
Deciphered Date
2012/07/11
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Compal Electronics, Inc.
Title
USB3.0/Left USB Ports
Size
Custom
Document Number
LA-7987P
Rev
1.0
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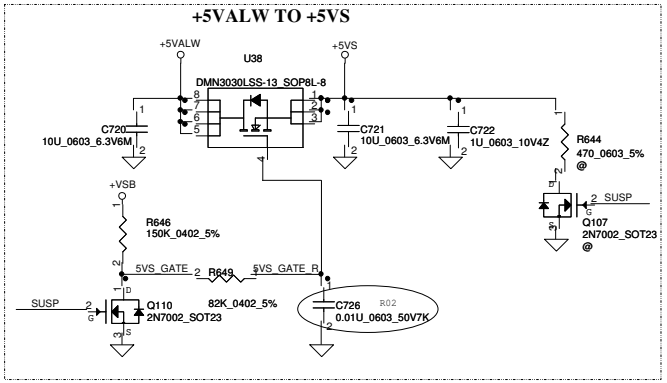
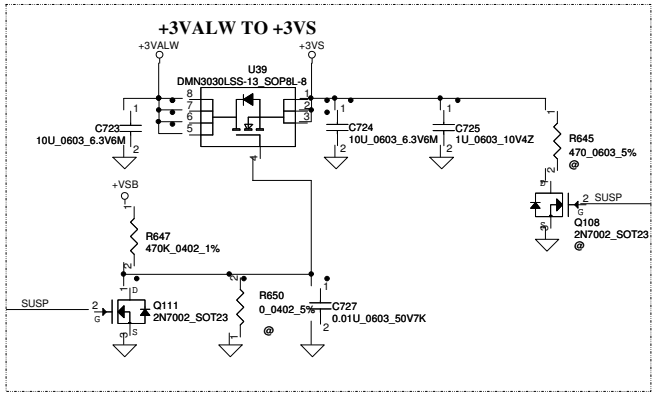
of
50

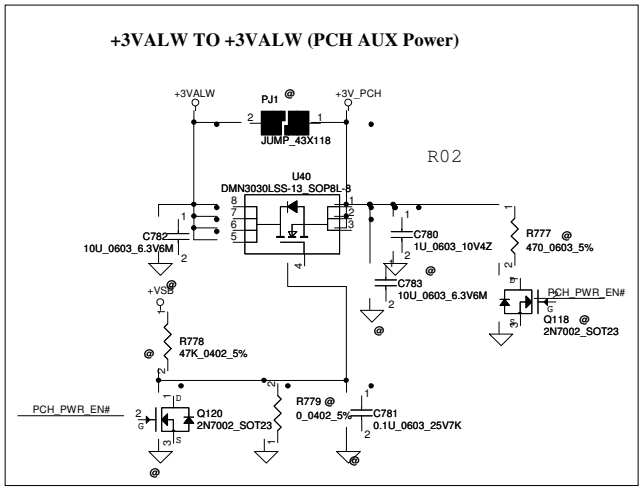
+5VALW TO +5VS

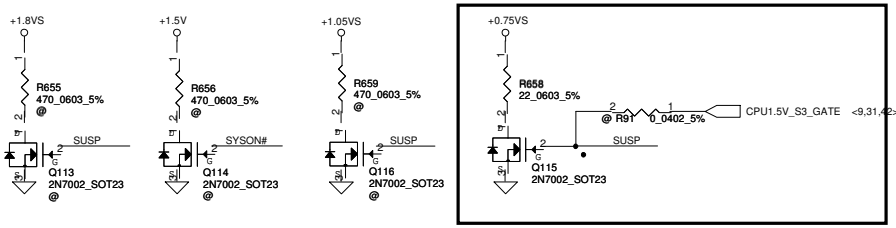


+3VALW TO +3VS



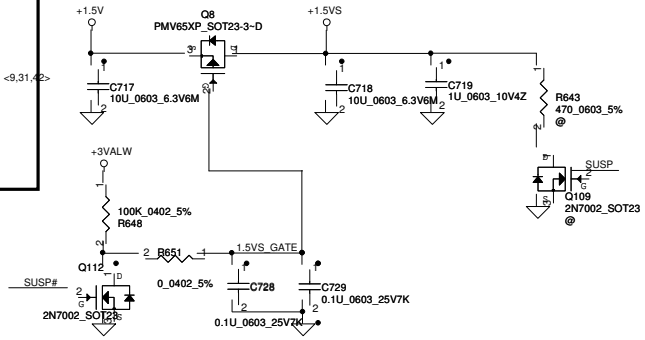
+3VALW TO +3VALW (PCH AUX Power)

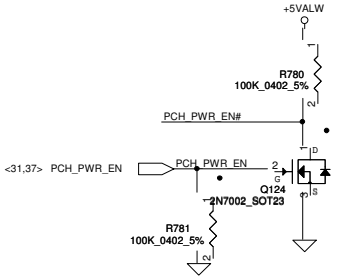


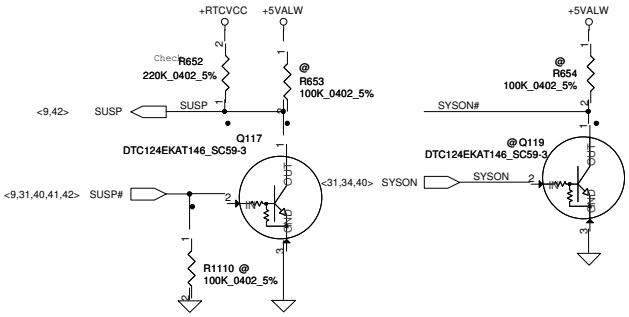


For Intel S3 Power Reduction.

+1.5V to +1.5VS







Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: DC Interface
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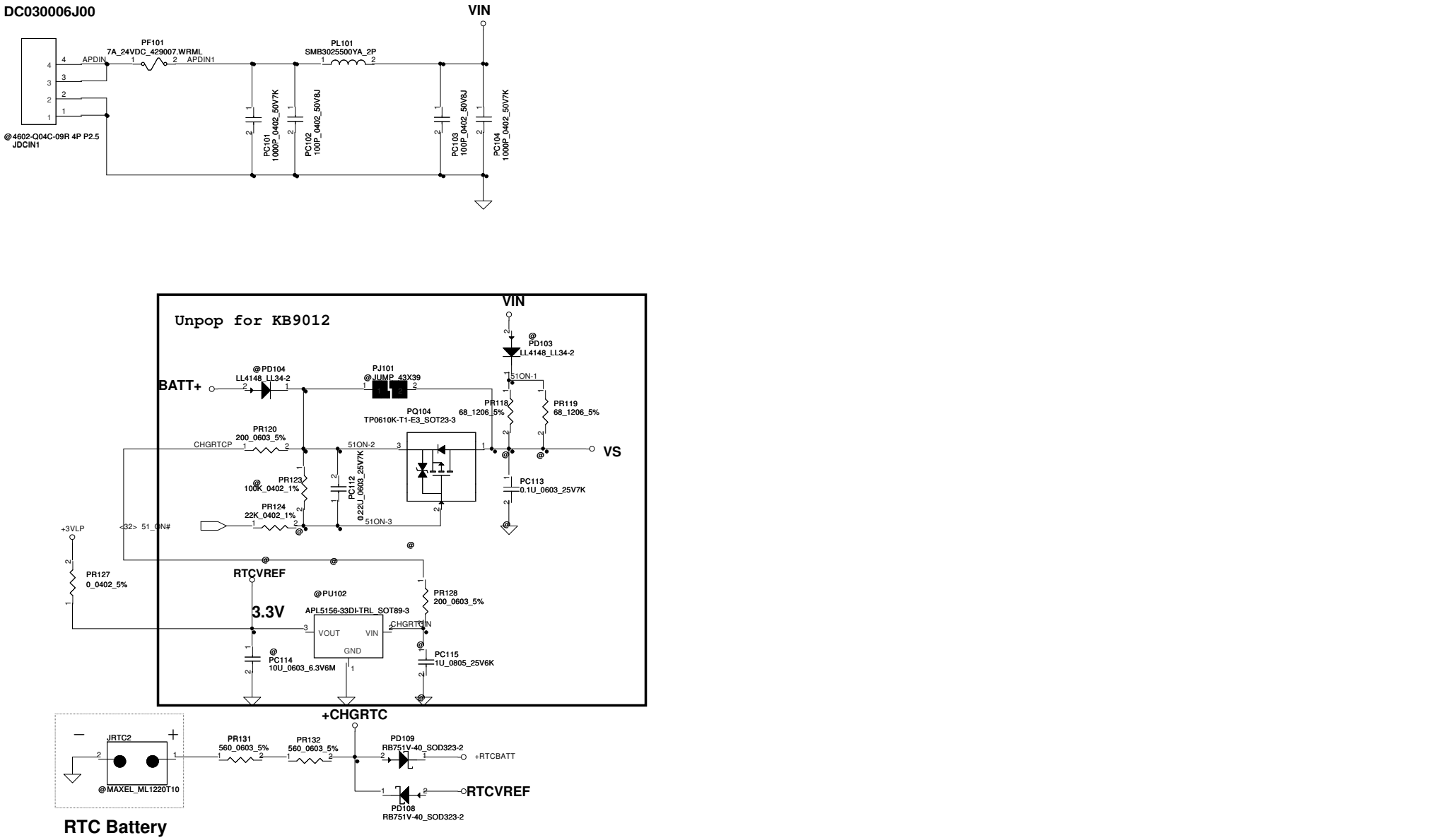

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

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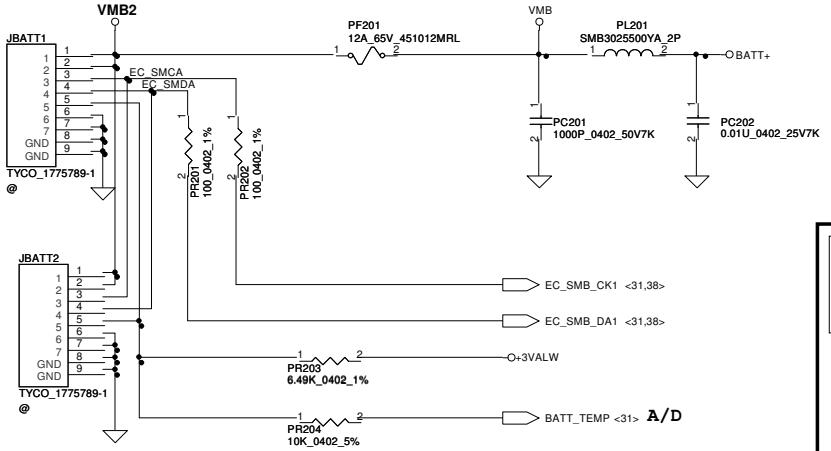
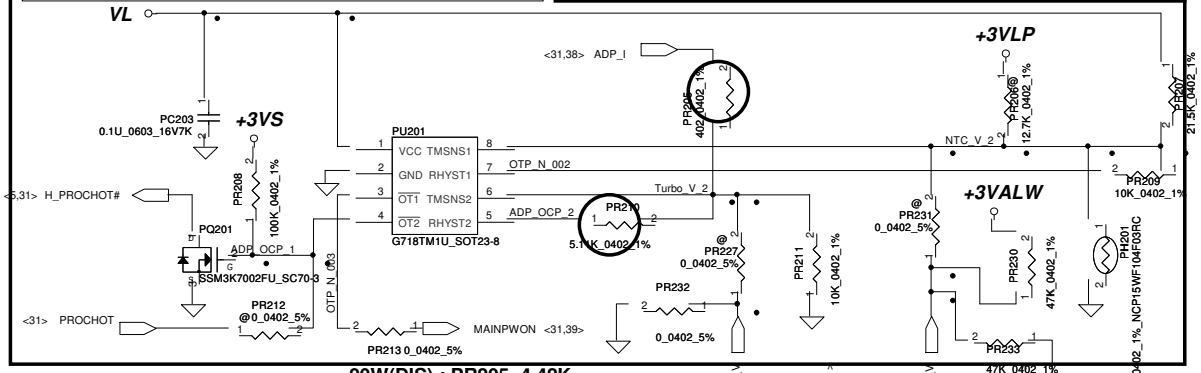


ADP_I need to write Charge Options Register (0x12H)=> bit6=1

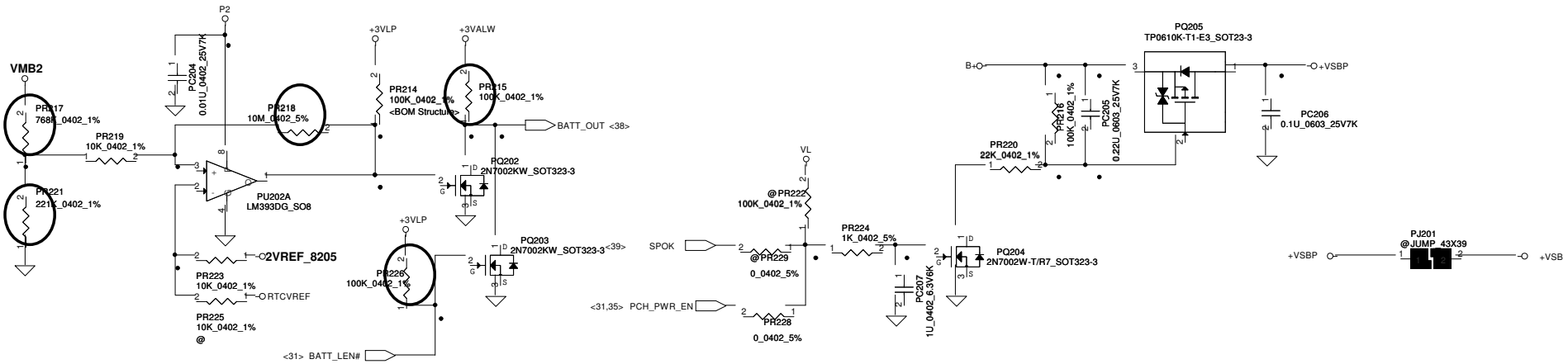
0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth =1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211,PQ201,PR208,PR212



90W(DIS) : PR205=4.42K
PR210=27.4K
65W(UMA) : PR205=402(SD034020080)
PR210=5.11K



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***PWR-BATTERY CONN/OTP***

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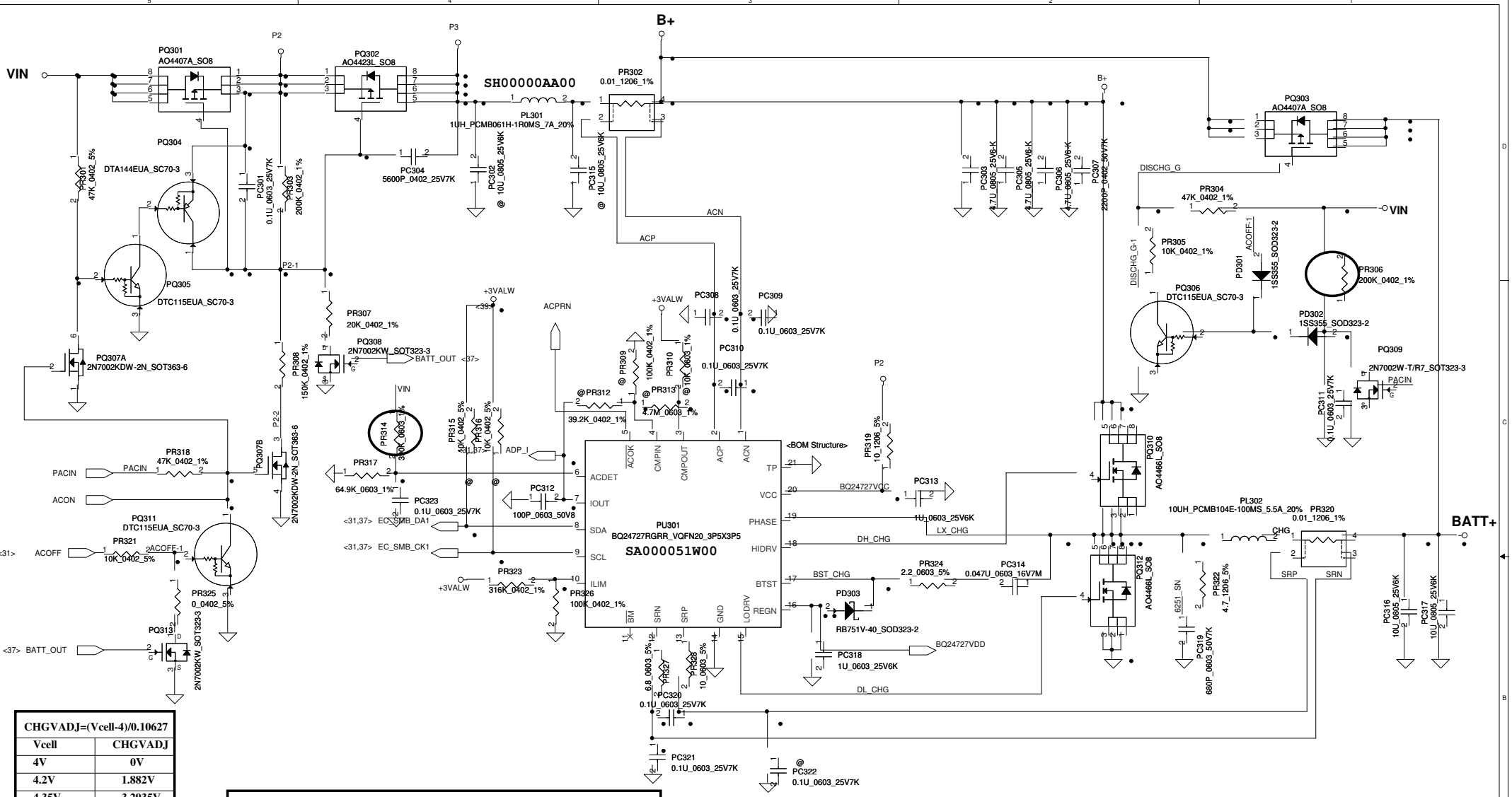

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CHARGER

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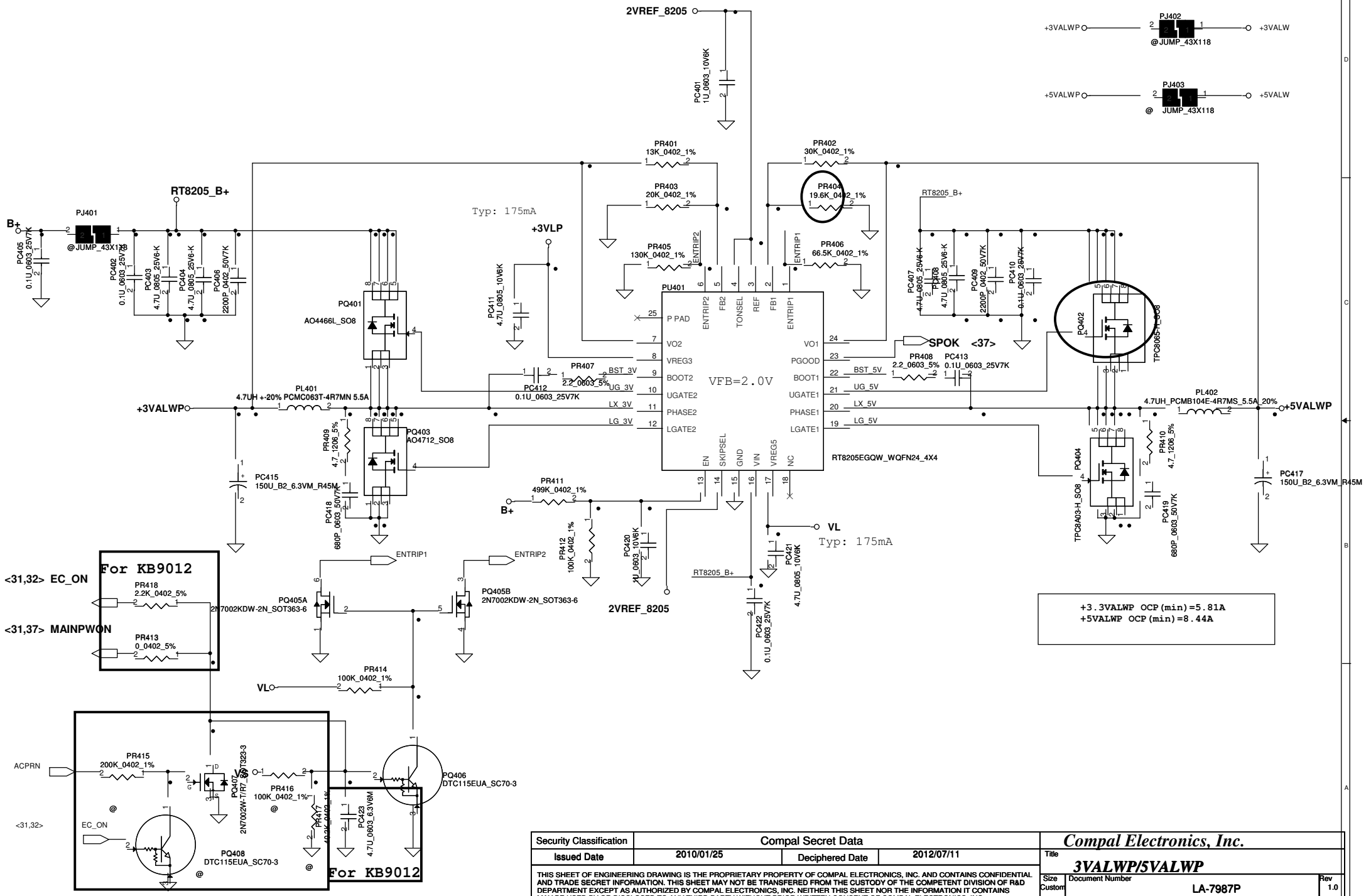
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
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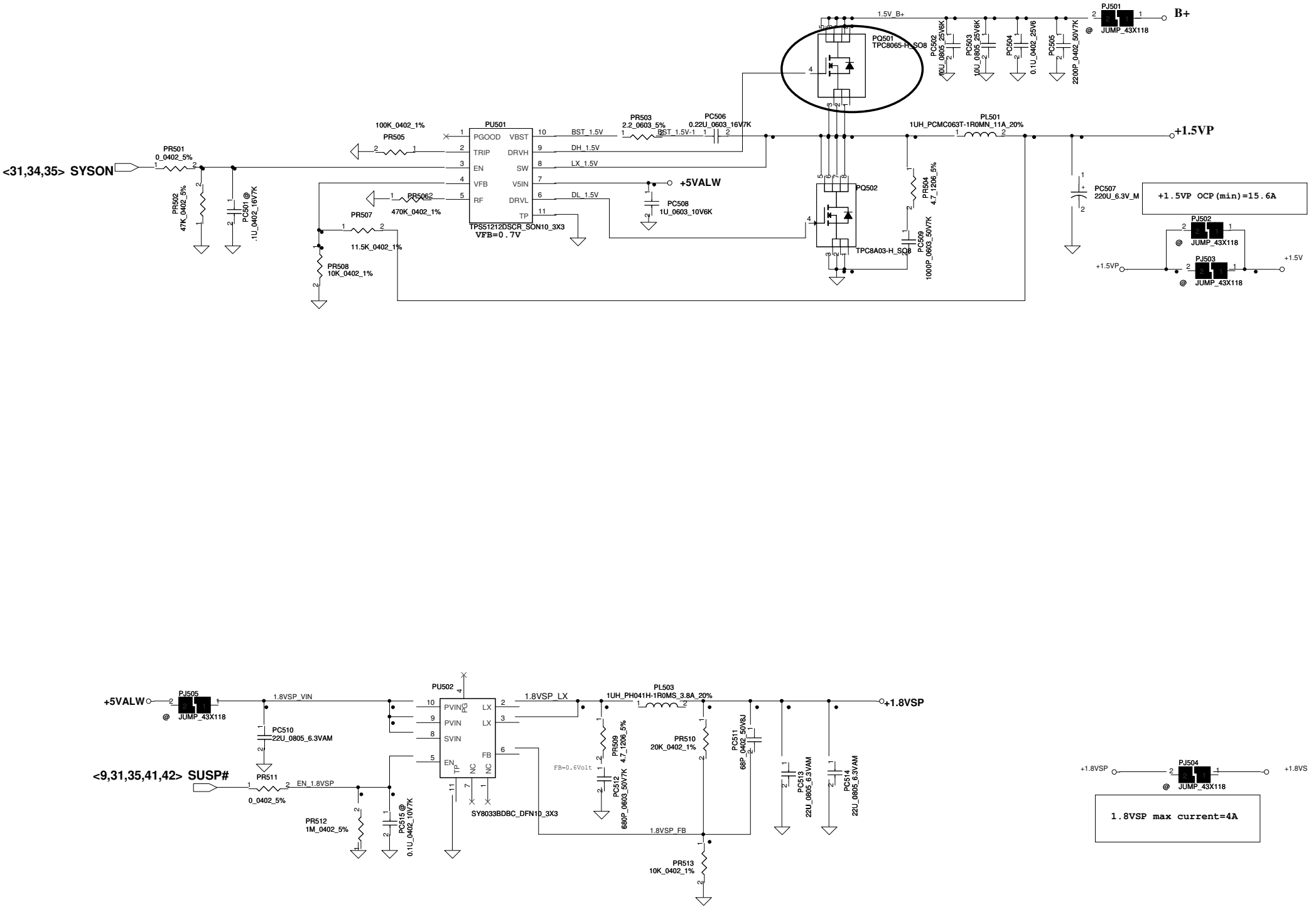
Date: Tuesday, October 30, 2012 Sheet 39 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

+VCCSAP PJ602 JUMP_43X118 +VCCSA

+3VS PR601 1K_0402_5% H_VCCSA_VID1 <9>
PR602 100K_0402_5% +VCCSA_PWRGD
H_VCCSA_VID0 <9>
PR603 1K_0402_5%
<31> SA_PGOOD

+5VALW PR604 10_0402_1% PC601 1U_0603_10V6K
PC602 2.2U_0603_10V7K
+VCCSA_EN PR605 0_0402_5% +V1.05S_VCCP_PWRGOOD <42>

PU601 TPS51461RGER_QFN24_4X4
V5DRV V5FILT PGOOD VID1 VID0 EN
PGND PGND PGND VIN VIN VIN
BST SW SW SW SW SW TP
GND VREF COMP SLEW VOUT MODE

PR606 0_0603_5% +VCCSA_BT PC603 0.22U_0603_16V7K
PL601 0.47UH_FDVE0630-H-R47M=P3_17.7A_20%
PR607 4.7_1206_5%
PC604 1000P_0603_50V7K
+VCCSAP

+3VALW PJ601 JUMP_43X118 +VCCSA_PWR_SRC
PC613 2200P_0402_50V7K
PC614 0.1U_0603_25V7K
PC615 10U_0805_6.3V6M
PC616 10U_0805_6.3V6M
PC605 22U_0805_6.3V6M
PC606 22U_0805_6.3V6M
PC607 0.1U_0402_10V7K
PC608 22U_0805_6.3V6M
PC609 22U_0805_6.3V6M
PC610 2200P_0402_50V7K
PC611 22U_0805_6.3V6M
PC612 22U_0805_6.3V6M

PR608 33K_0402_5%
PC617 0.22U_0402_10V6K
PC618 3300P_0402_50V7K
PR610 5.1K_0402_1%
PC619 .01U_0402_25V7K
PR609 100_0402_5%
PR611 0_0402_5% +VCCSA_SENSE <9>

+3VS PR612 100K_0402_5% <42> +V1.05S_VCCP_PWRGOOD
PR613 0_0603_5%
PC624 0.22U_0603_16V7K
PU602 TPS51212DSCR_SON10_3X3
PGOOD VBST TRIP DRVH EN SW VFB V5IN RF DRVL TP
BST +V1.05S_VCCPP
UG +V1.05S_VCCPP
SW +V1.05S_VCCPP
+V1.05S_VCCPP_5V
LG +V1.05S_VCCPP
PR614 66.5K_0402_1% TRIP +V1.05S_VCCPP
EN +V1.05S_VCCPP
FB +V1.05S_VCCPP
RF +V1.05S_VCCPP
PR615 0_0402_5% <9,31,35,40,42> SUSP#
PC625 0.1U_0402_16V7K
PR616 470K_0402_1%
PC626 1U_0603_6.3V6M

+V1.05S_VCCPP PJ603 JUMP_43X118 B+
PC601 TPC8037-H_SO8
PC620 0.1U_0402_25V6
PC621 2200P_0402_50V7K
PC622 4.7U_0805_25V6-K
PC623 4.7U_0805_25V6-K
PL602 1UH_PCMC063T-1R0MN_11A_20%
+V1.05S_VCCPP
PC602 TPC8A03-H_SO8
PR617 4.7_1206_5%
PC628 1000P_0603_50V7K
PC627 0.1U_0402_10V7K

+V1.05S_VCCPP PJ604 JUMP_43X118 +V1.05S_VCCP
PC631 150U_B2_6.3VM_R45M

PC629 1000P_0402_50V7K
PR618 1.2K_0402_1%
PR619 4.32K_0402_1%
PR620 0_0402_5% VCCIO_SENSE <8,42>

+3VS PR621 10K_0402_1%
PR622 71.5K_0402_1%
PR623 100K_0402_5%
PR624 0_0402_5% VCCP_PWRCTRL <9>
PQ603 SSM3K7002FU_SC70-3
PC630 .01U_0402_16V7K
PR625 100K_0402_5%

VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

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Title: PWR +VCCSAP/1.0

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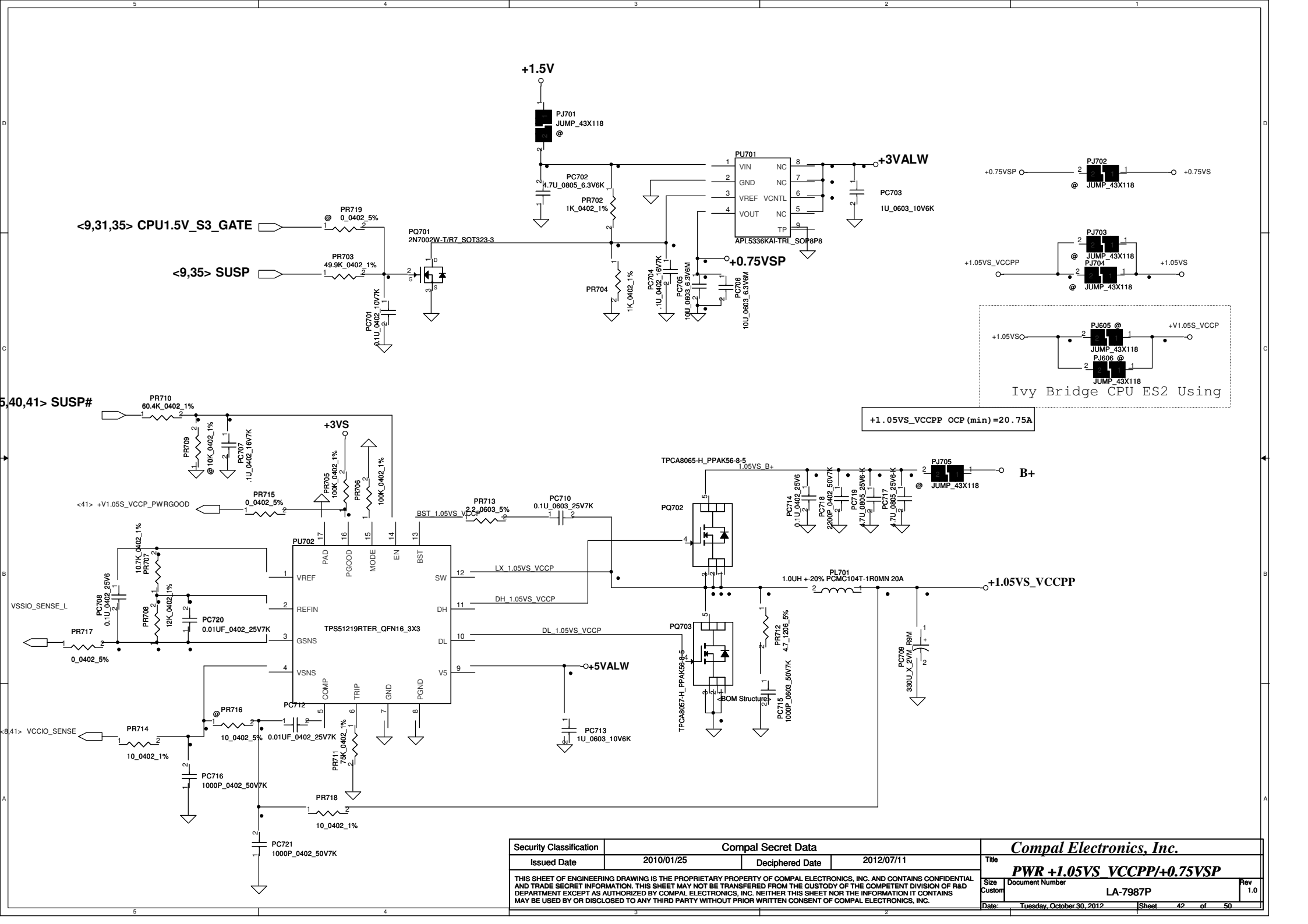

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Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: PWR +1.05VS_VCCPP/+0.75VSP			
Size: Custom	Document Number: LA-7987P		Rev: 1.0
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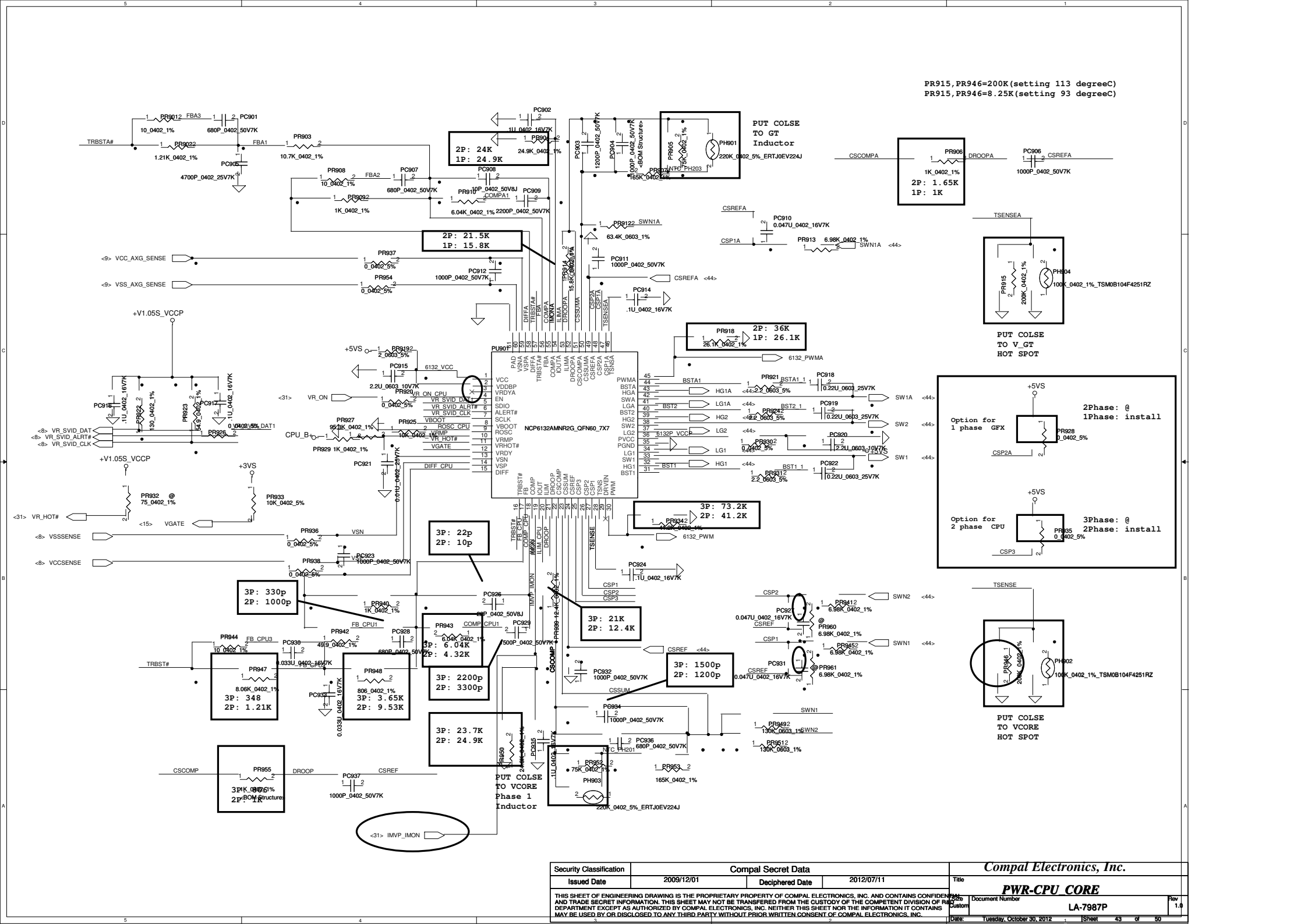

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Issued Date	2009/12/01	Deciphered Date	2012/07/11

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Title: ***PWR-CPU_CORE***

Size	Document Number	Rev
Custom	LA-7987P	1.0

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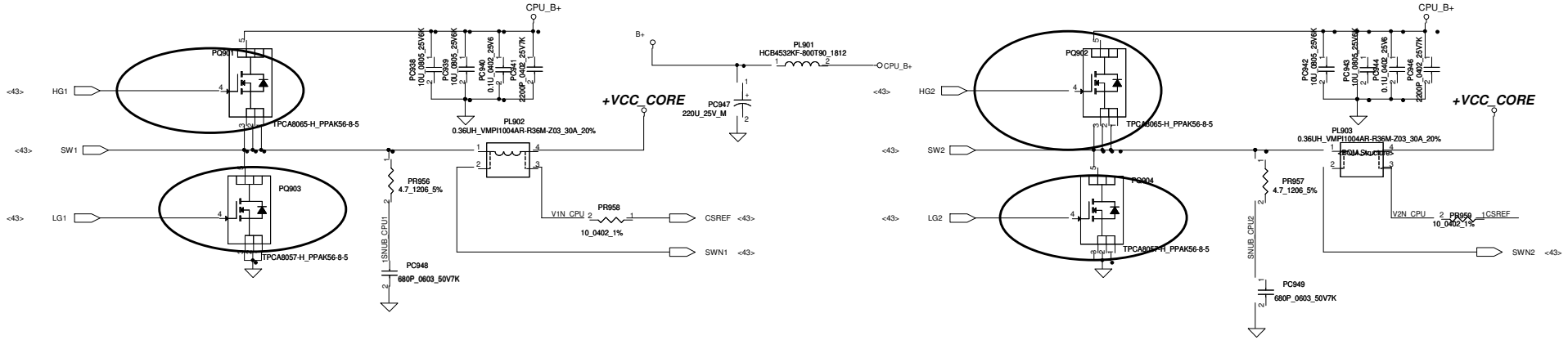
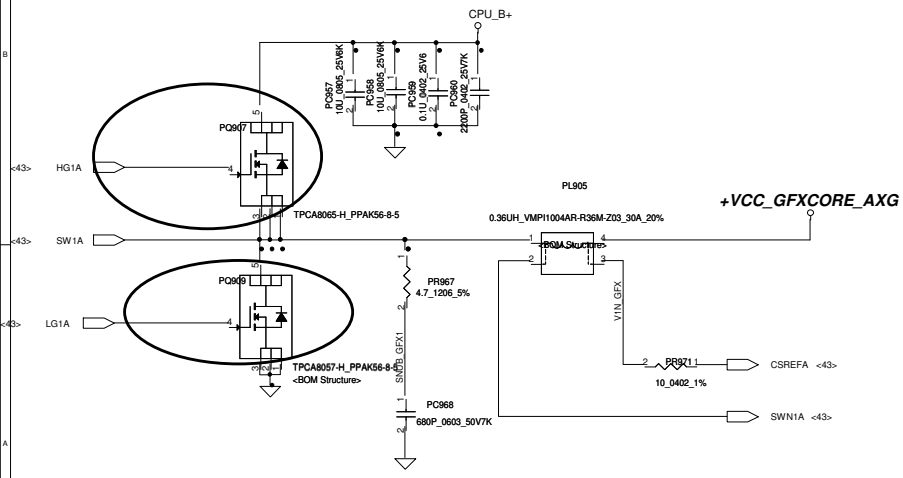


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***PWR-CPU_CORE***

Size	Document Number	Rev
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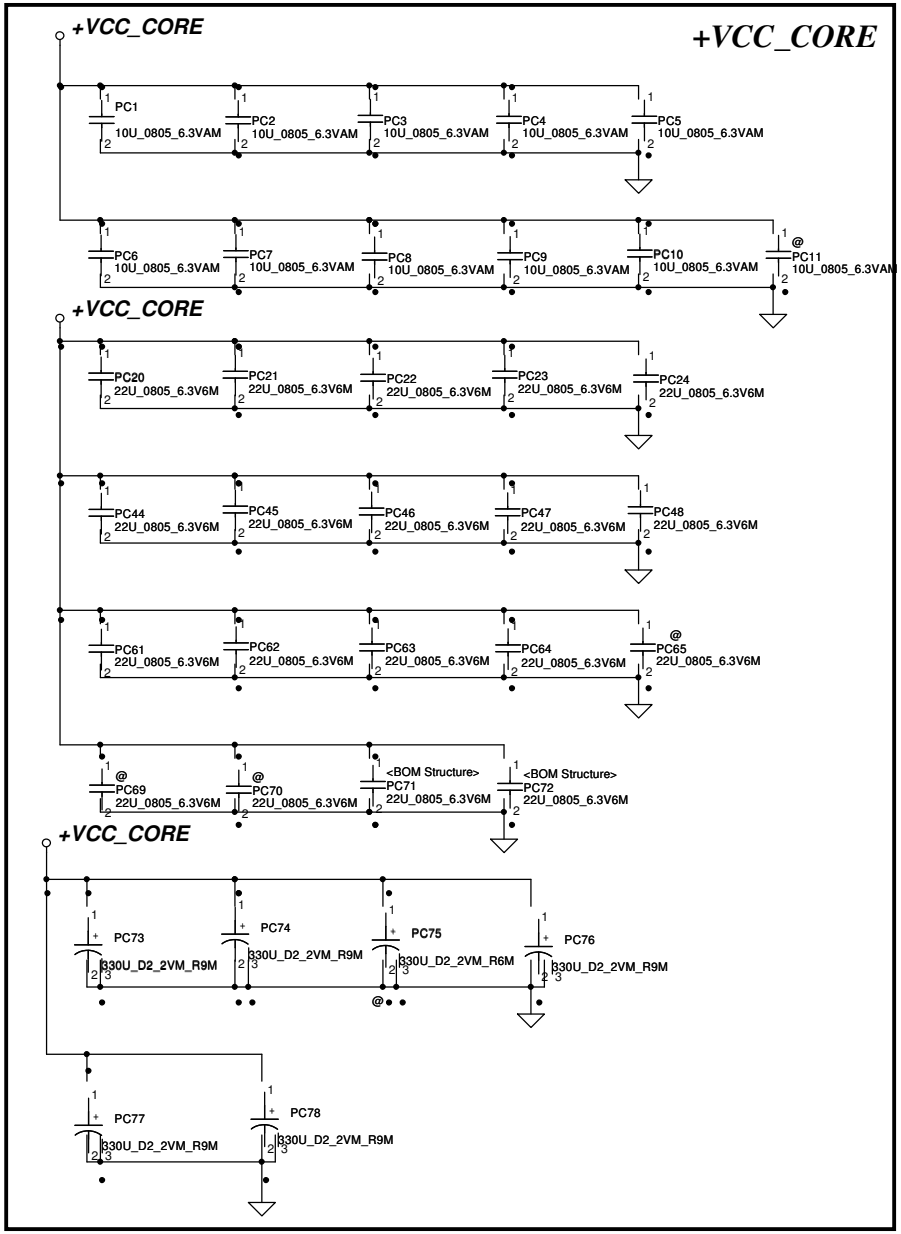
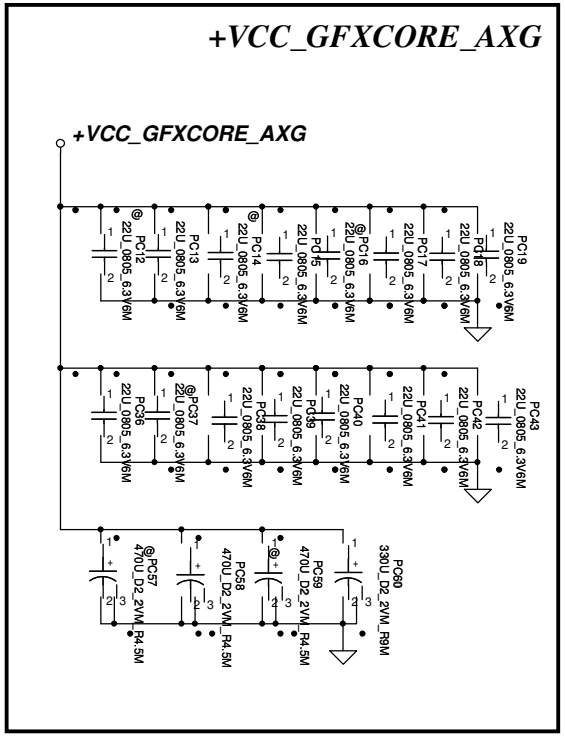
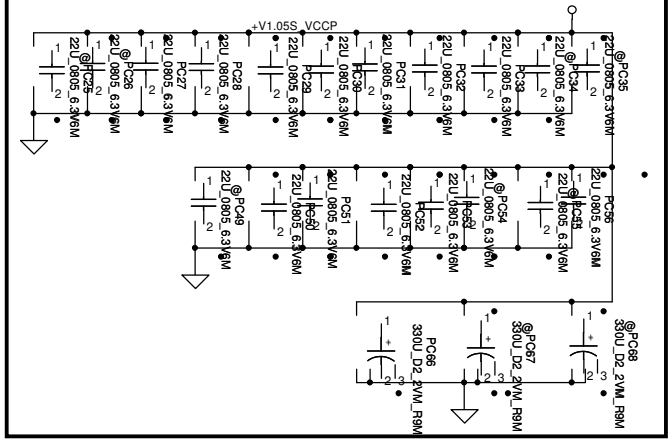




Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



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Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size	Document Number	Rev
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	unpop PR315,PR316 for SMBus SPEC.	P38	unpop PR315,PR316		
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

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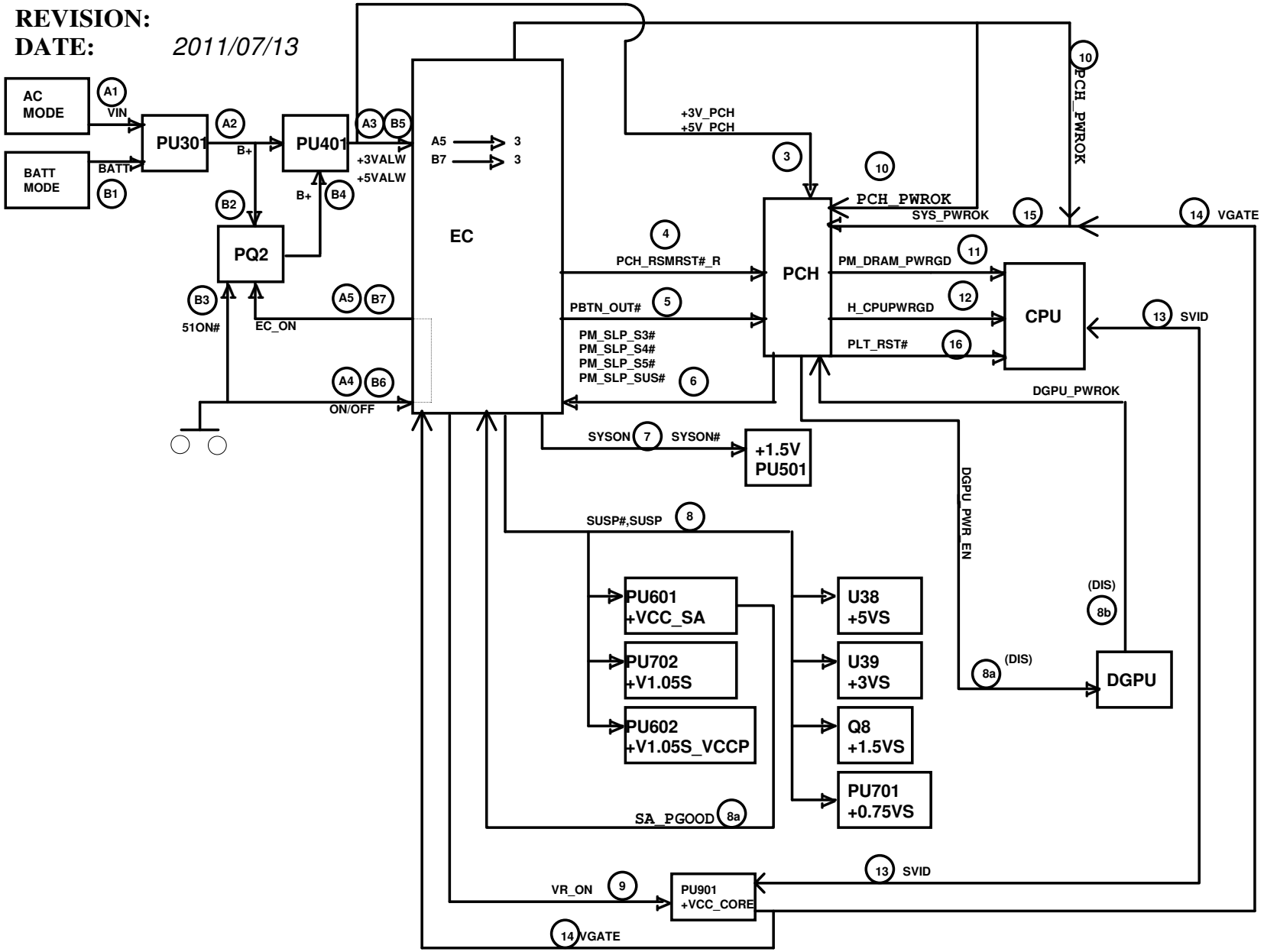
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***Power sequence***

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Item	Reason for change	PG#	Modify List	Date	Phase
1	HDD no function	29	Add R550		DVT
2	10/100 lan no function & change to overclocking mode	26	ADD R1372 ; DEL R31		DVT
3	For DGPU_PWROK leakage issue.(Let timing +5VS > +3VS)	35	Change C726 from 0.1uF to 0.01uF		DVT
4	For S3 can't wake up	9	Change R56 from 15K to 4.7K change R885 from 0 ohm to 15K		DVT
5	PCH 25Mhz for vender crystal test report change CL to 12pF	14	C196;C197		DVT
6	EC_LID_OUT# internal PD 20K, follow ORB change R230 from 10k to 1K	18	R230		DVT
7	For GPIO70;GPIO71 voltage level issue (internal Pull High 20k)	18	R705;R706 Change from 10K to 200K		DVT
8	for DVT board ID Change R695 from 33k to 18k	31	R695		DVT
9	LAN Surge test fail change P/N from SP050006E00 to SP050006W00	27	T1;T2		DVT
10	Del ODD Power Control function component	29	R568;Q100;R675;C607;Q99		DVT
11	Del (PCH AUX Power) Reserve component no use	35	C780;C781;C782;C783;R778;Q120		DVT
12	PCH(U4) P/N Change from SA00004NQ30 to SA00004NQ80	13	U4		DVT
13	For ESD test fail add C549 100p	5	C549		DVT
14	EXT USB 3.0 IC PCIE_WAKE# ; CLKREQ_USB30# leakage on S4	34	Swap Q125;Q121 pin1 & pin3		DVT
15	No function	34	DEL R769		DVT
16	add LAN LDO mode function	26;27	ADD R65;R596;R1449;R1380		DVT
17	USB_OC0# Share with USB_OC4# due to same power switch	17	short USB_OC0#;USB_OC4# ; del R267		DVT
18	Add Capsensor B/D Conn. For best buy use	31	ADD JCAP1 Conn.		DVT
19	L1 change to 1 ohm R	19	L1 change to R footprint		DVT
20	Reserve 0 ohm for CMOS Camera shake	22	add R296 0 ohm		DVT
21	For HDD +5VS Power plant del C601; change C598 pin1 power name for good power plant	29	change from +5VS to +5V_HDD ;DEL C601		DVT
22	For Audio jack support APPLE and NOKIA function Reserve	32	add R684;R685;R688;R686 0ohm R		DVT
23	For standard part cost down change 10uF 0805 type to 0603 type	9,19 20,22 26,28 29,35	C124;C125;C126;C127;C130;C221;C215;C395; C231;C519;C937;C953;C954;C591;C608;C602; C720;C721;C723;C724;C782;C783;C717;C718;		DVT

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Title: <Title>

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Item	Reason for change	PG#	Modify List	Date	Phase
24	change Crystal foot print follow standard parts from 5032 to 3225 package	14;26	Y2;Y6		DVT
25	change 0ohm to short-pad (R0402_0ohm)	6;7; 9;14; 15;19; 22;25; 29;32	R40;R60;R77;R190;R193;R198;R181;R185;R265 ;R538;R498;R500;R583;R614		DVT
26	Reserve BT_DISABLE (GPI022) for combo card(BT+WLAN)	18	ADD R892;R897		DVT
27	U35;U36 Change footprint without thermal PAD type	33;34	U35;U36		DVT DVT
28	LED5 和LED2 Location sawp ; Location name D9 change to LED6	32	LED2;LED5;LED6		DVT DVT
29	For Lan surge fail add 0 ohm on MDO2-;MDO2+;MDO3-;MDO3+	27	R304;R305;R306;R307		DVT
30	For ESD fail issue del TDI & TDO net ,but keep R21 &R23 for debug use	5	R20 pin2 & R23 pin2 NC add T102;T103		DVT DVT
31	Change 2M BIOS ROM from SA00003FO00 to SA00003FO10	13	U6	09/29	DVT
32	Correct PCIE_PRX_DTX_P4/N4 of U32 (SWAP)	34	U32	10/03	DVT
33	Reserve +5VS to JCR1, add R689 ,R690	32	R689 (@),R690	10/03	DVT
34	Update Power sheet of 1003 version	47~58		10/04	DVT
35					DVT
36					DVT
37					DVT

Item	Reason for change	PG#	Modify List	Date	Phase
44	CPU Symbol Update	5,6,7,8,9,10,11	Location : Jcpu1		PVT
45	Change 10P 50V Cap from 1206 to 0603	38	Location : C973		PVT
46	S3 Reduction	53	Reserve PR719 for 0.75V		PVT
47	LAN CO-lay x1 GDT & 75ohm	38	Location : R308,R304,R305,R306,R307,DL1,DL2,DL3,DL4		PVT
48	R750 for Power request	42	Location :R750		PVT
49	JUSB3 From 4PIN TO 6 PIN FOR VOLTAGE DROP	44	Location : JUSB3		PVT
50	Add C535 100pF on +3VLP for ESD request - Pony	42	Location : C535		PVT
51	FOR TP POWER SOLUTION	42	Location :R598.R603		
52	FOR POWER REQUEST	42	Location : R738		
53	FOR PCH HM70 SOLUTION	18	Location : R718,R719,R726,R727,R729,R731,R732,R733		

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Title	HW-PIR2	
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