

Compal Confidential

G470/G570 DIS+UMA+Muxless M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Robson/PX3.0,PX4.0

2010-10-22

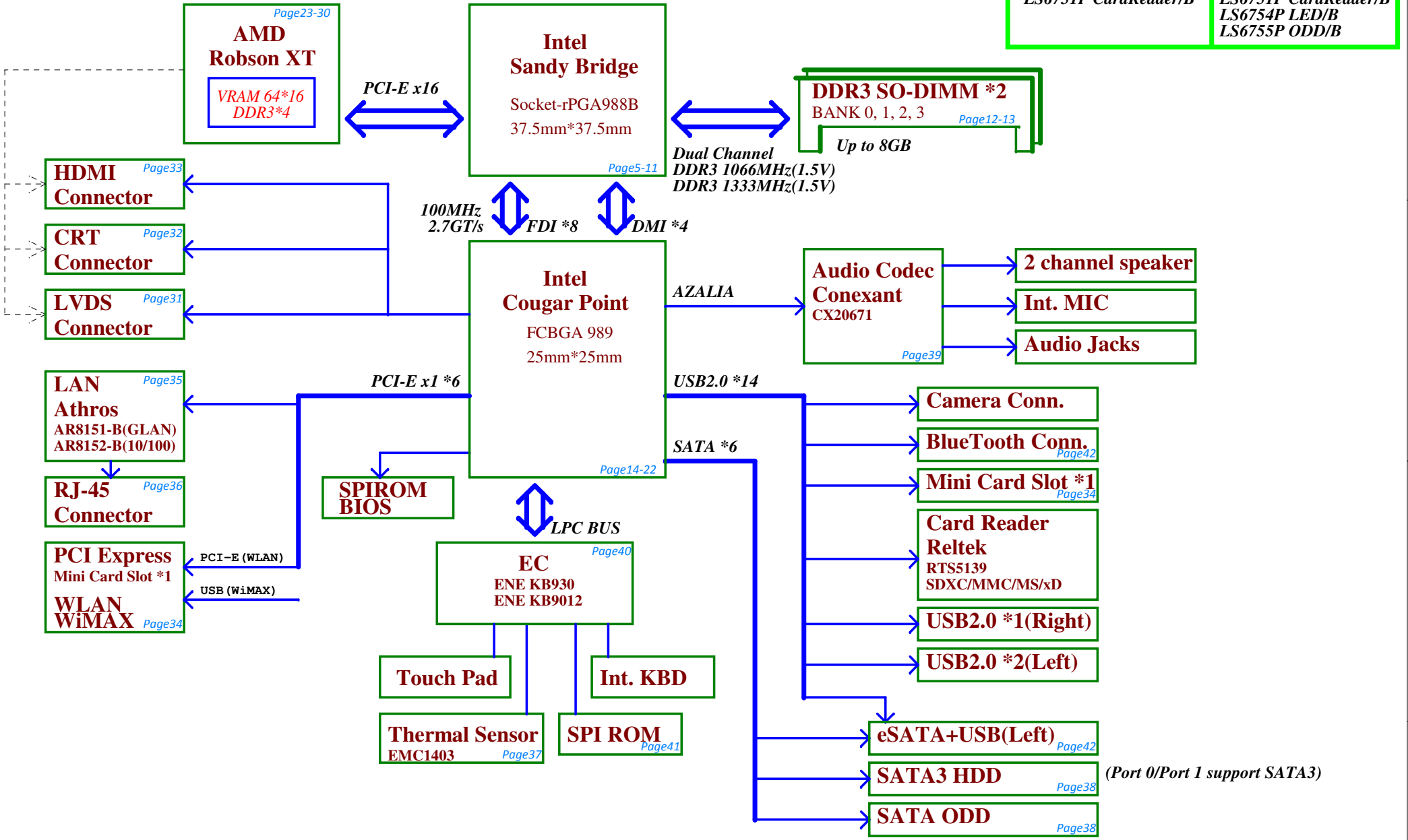
LA-6751P / LA-6753P

REV: 0.3

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| | | | | Date: | Friday, November 26, 2010 | Sheet 1 of 59 |

For 14"(Page 4x)
LS6753P PWR/B
LS6751P CardReader/B

For 15"(Page 4x+1)
LS6753P PWR/B
LS6751P CardReader/B
LS6754P LED/B
LS6755P ODD/B



| | | | | | |
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Voltage Rails

| | | | | |
|--------------------------------|----|--------|-------|--|
| power plane | +B | +5VALW | +1.5V | +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS |
| | | | | |
| S0 | ○ | ○ | ○ | ○ |
| S3 | ○ | ○ | ○ | ✗ |
| S5 S4/AC | ○ | ○ | ✗ | ✗ |
| S5 S4/ Battery only | ○ | ✗ | ✗ | ✗ |
| S5 S4/AC & Battery don't exist | ✗ | ✗ | ✗ | ✗ |

EC SM Bus1 address EC SM Bus2 address

| Device | Address | Device | Address |
|---------------|-------------|--------------------------|------------|
| Smart Battery | 0001 011X b | Thermal Sensor EMC1403-2 | 1001_101xb |
| | | Thermal Sensor EMC1402-1 | 100_1100 b |

PCH SM Bus address

| Device | Address |
|-----------|------------|
| DDR DIMM0 | 1001 000Xb |
| DDR DIMM2 | 1001 010Xb |

SMBUS Control Table

| | SOURCE | VGA | BATT | KE930 | SODIMM | WLAN WWAN | Thermal Sensor | PCH |
|------------|--------|------|--------|-------|--------|-----------|----------------|------|
| SMB_EC_CK1 | KB930 | ✗ | ✓ | ✗ | ✗ | ✗ | ✗ | ✗ |
| SMB_EC_DA1 | +3VALW | | +3VALW | | | | | |
| SMB_EC_CK2 | KB930 | ✗ | ✗ | ✗ | ✗ | ✗ | ✗ | ✓ |
| SMB_EC_DA2 | +3VALW | | | | | | | +3VS |
| SMBCLK | PCH | ✗ | ✗ | ✗ | ✓ | ✓ | ✗ | ✗ |
| SMBDATA | +3VALW | | | | +3VS | +3VS | | |
| SML0CLK | PCH | ✗ | ✗ | ✗ | ✗ | ✗ | ✗ | ✗ |
| SML0DATA | +3VALW | | | | | | | |
| SML1CLK | PCH | ✓ | ✗ | ✓ | ✗ | ✗ | ✓ | ✗ |
| SML1DATA | +3VALW | +3VS | | +3VS | | | +3VS | |

| STATE | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|-----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1 (Power On Suspend) | | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0 | 0.1 |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

Board ID / SKU ID Table for AD channel

| Vcc | 3.3V +/- 5% | | | | |
|----------|--------------|-------------|-------------|-------------|-----|
| Ra/Rc/Re | 100K +/- 5% | | | | |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max | EVT |
| 0 | 0 | 0 V | 0 V | 0 V | EVT |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | DVT |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | PVT |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | MP |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V | |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V | |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V | |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V | |

USB Port Table

| USB 2.0 | USB 1.1 | Port | 3 External USB Port |
|---------|---------|------|----------------------|
| EHCI1 | UHCI0 | 0 | USB/B (Right Side) |
| | | 1 | USB Port (Left Side) |
| | | 2 | USB Port (Left Side) |
| | UHCI1 | 3 | USB Port (Left Side) |
| | | 4 | |
| | UHCI2 | 5 | Camera |
| | | 6 | |
| EHCI2 | UHCI3 | 7 | |
| | | 8 | Mini Card(WLAN) |
| | UHCI4 | 9 | |
| | | 10 | |
| | UHCI5 | 11 | Card Reader |
| | | 12 | |
| | | 13 | Blue Tooth |

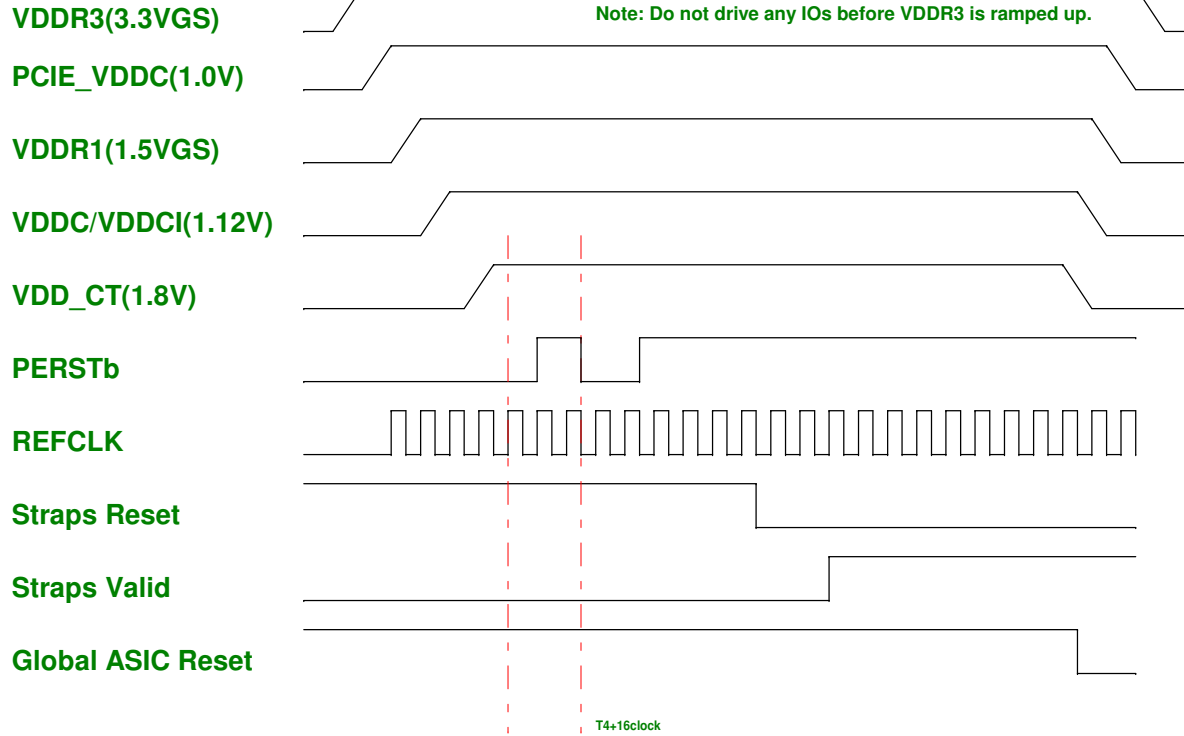
BOM Structure Table

| BTO Item | BOM Structure |
|--------------------------|---------------|
| UMA and PX bus | PX@ |
| Discrete Only | DIS@ |
| PX3.0 only, not for BACO | PX3@ |
| BACO | BACO@ |
| COMMON HDMI | HDMI@ |
| UMA HDMI | UMA_HDMI@ |
| Discrete HDMI | VGA_HDMI@ |
| eSATA | ESATA@ |
| Blue Tooth | BT@ |
| Connector | ME@ |
| 45 LEVEL | 45@ |
| 10/100 LAN | 8152@ |
| GIGA LAN | GIGA@ |
| Camera | CMOS@ |
| Unpop | @ |

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Power-Up/Down Sequence

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDR3 should ramp-up before or simultaneously with VDDC.
- For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
- The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



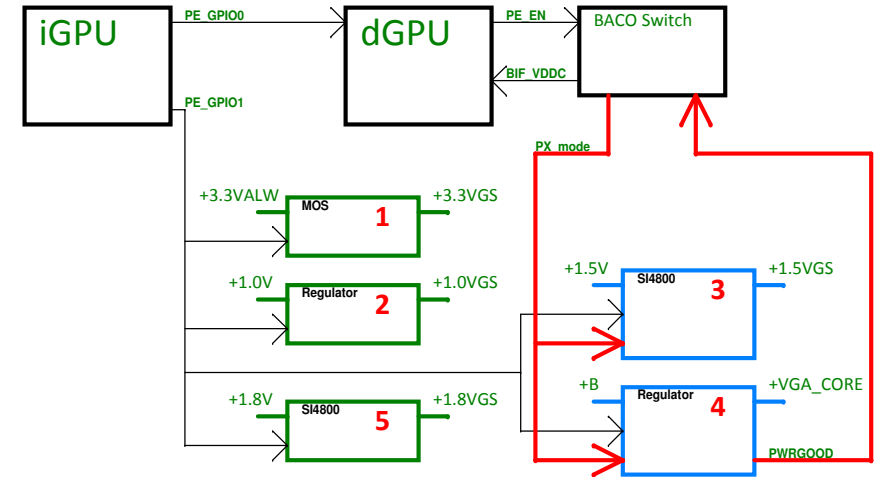
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

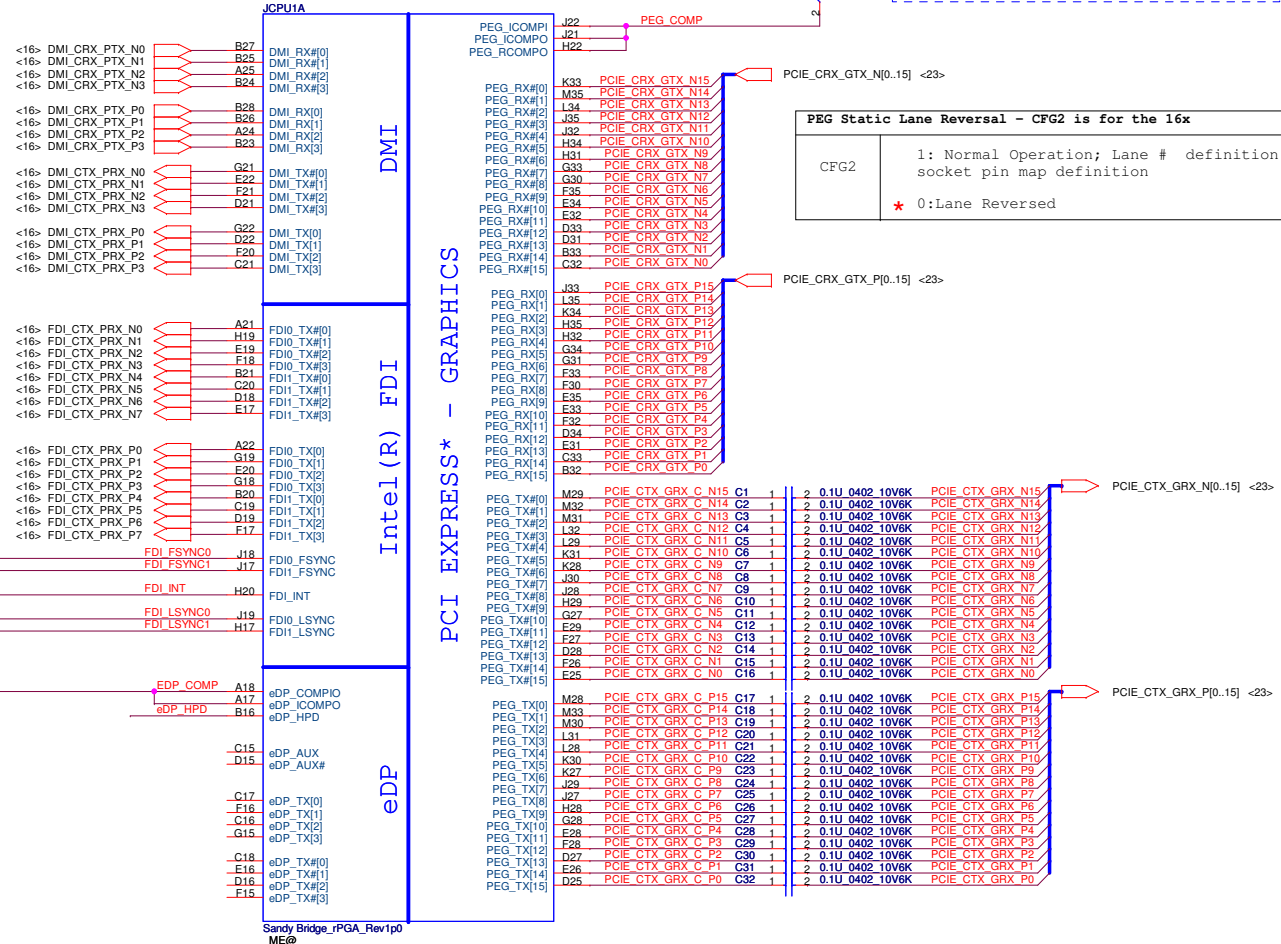
PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

| dGPU Power Pins | Voltage | PX 3.0 | BACO Mode | Max current |
|---|--------------|--------|----------------------|-------------|
| PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18 | 1.8V | OFF | ON | 1679mA |
| DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10 | 1.0V | OFF | ON | 575mA |
| PCIE_VDDC | 1.0V | OFF | ON | 2A |
| VDDR3 , and A2VDD | 3.3V | OFF | ON | 190mA |
| BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) | Same as VDDC | OFF | ON Same as PCIE_VDDC | 70mA |
| VDDR1 | 1.5V | OFF | OFF | 2.8A |
| VDDC/VDDCI | 1.12V | OFF | OFF | 12.9A |



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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



PEG Static Lane Reversal - CFG2 is for the 16x

| | |
|------|--|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition |
| * | 0: Lane Reversed |

DISCRETE ONLY

1K 0402 5% 2 DIS@ 1 R2 FDI_FSXNC0

1K 0402 5% 2 DIS@ 1 R3 FDI_FSXNC1

1K 0402 5% 2 DIS@ 1 R4 FDI_INT

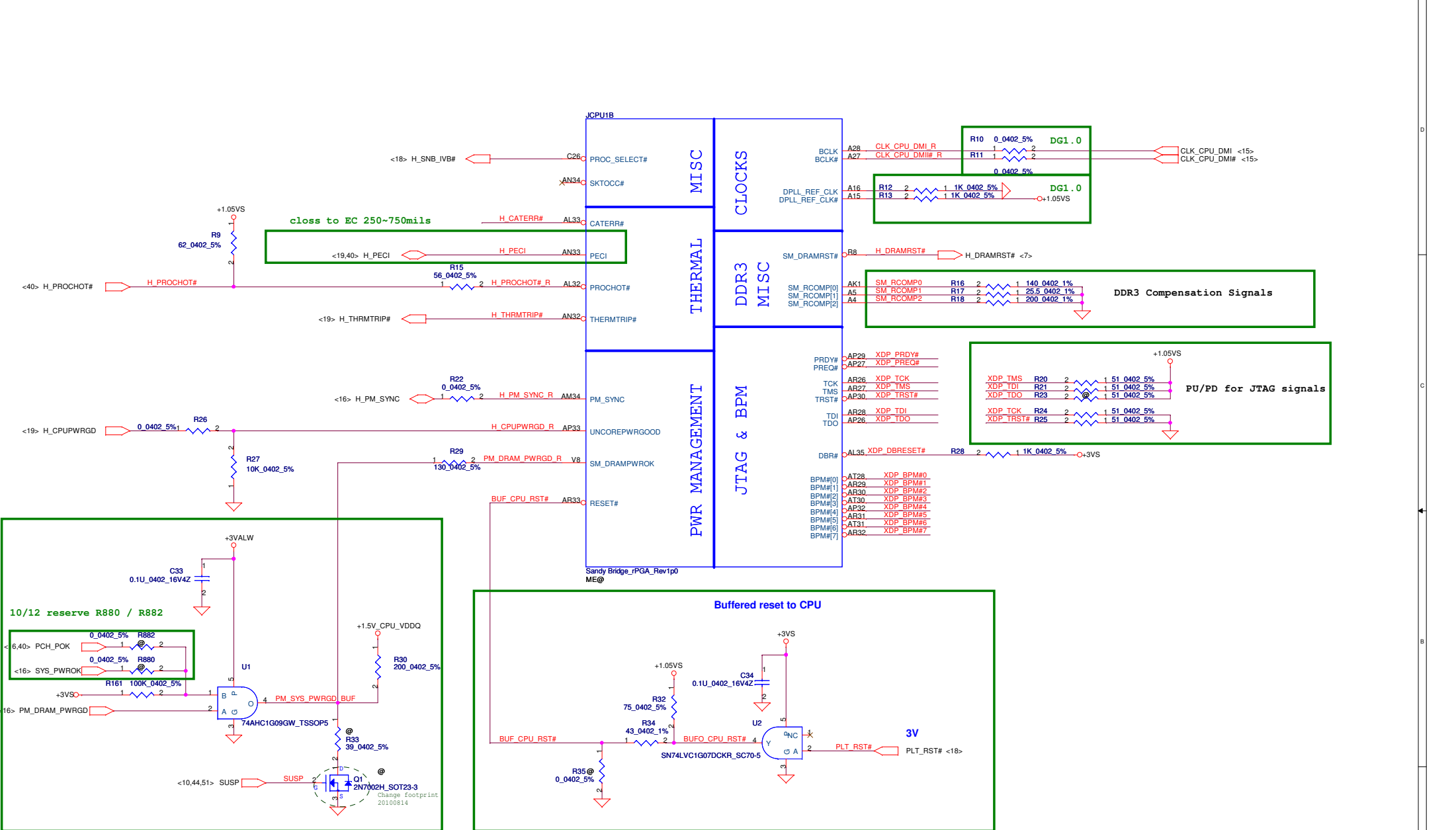
1K 0402 5% 2 DIS@ 1 R5 FDI_LSYNC0

1K 0402 5% 2 DIS@ 1 R6 FDI_LSYNC1

eDP_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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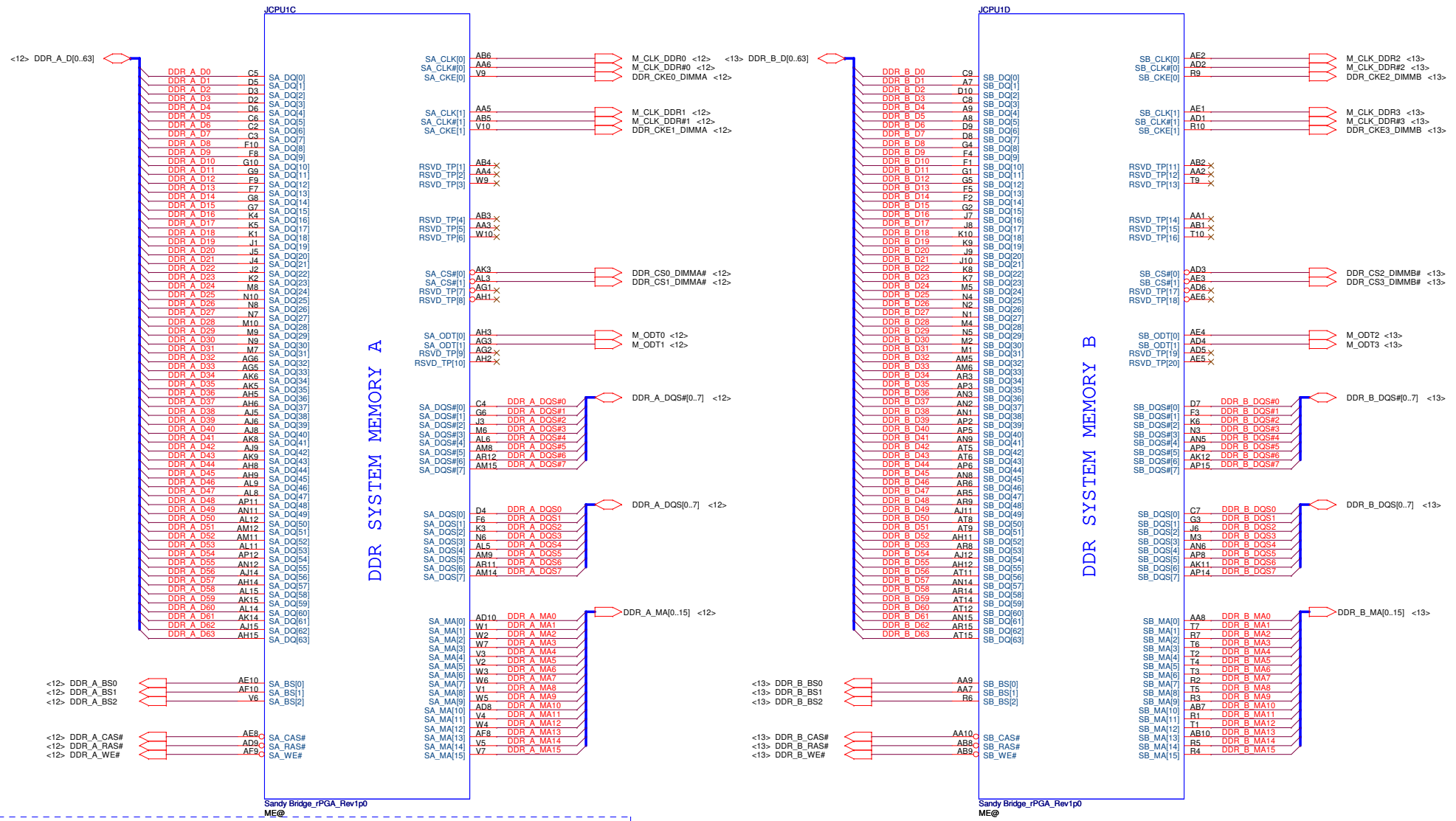
| | | |
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| PROCESSOR(I7) DMI,FDI,PEG | | |
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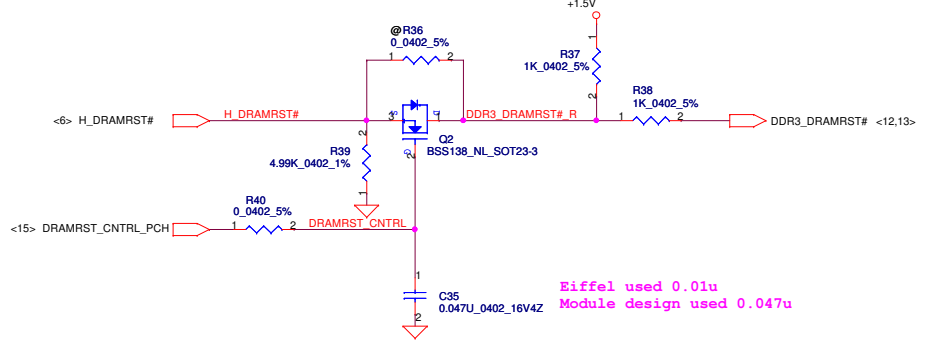
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|--------|---------------------------|----------------------------------|---------|
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| | | PROCESSOR(2/7) PM,XDP,CLK | |
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DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

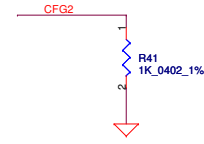
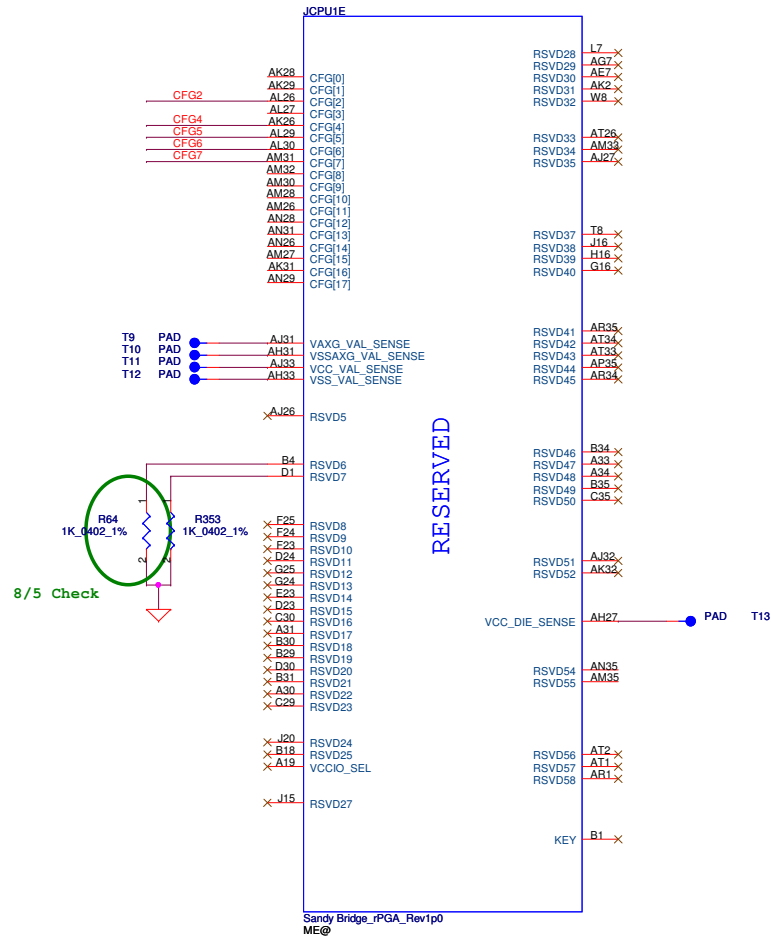
Sandy Bridge_rPGA_Rev1p0 ME@



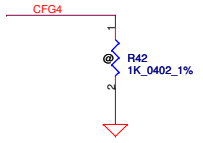
Eiffel used 0.01u
Module design used 0.047u

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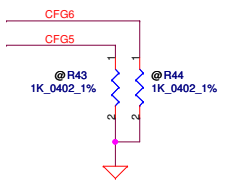
CFG Straps for Processor



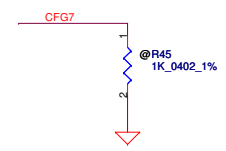
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed |



| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | * 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

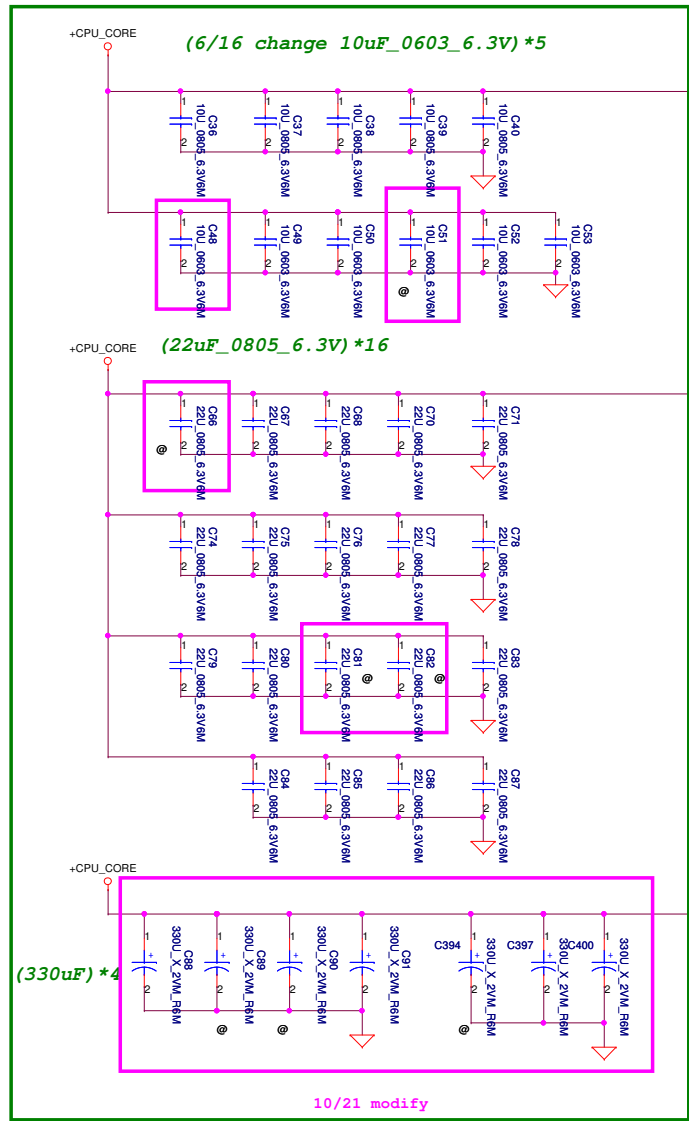


| PCIe Port Bifurcation Straps | |
|------------------------------|--|
| CFG[6:5] | * 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |



| PEG DEFER TRAINING | |
|--------------------|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training |

POWER



QC=94A
DC=53A

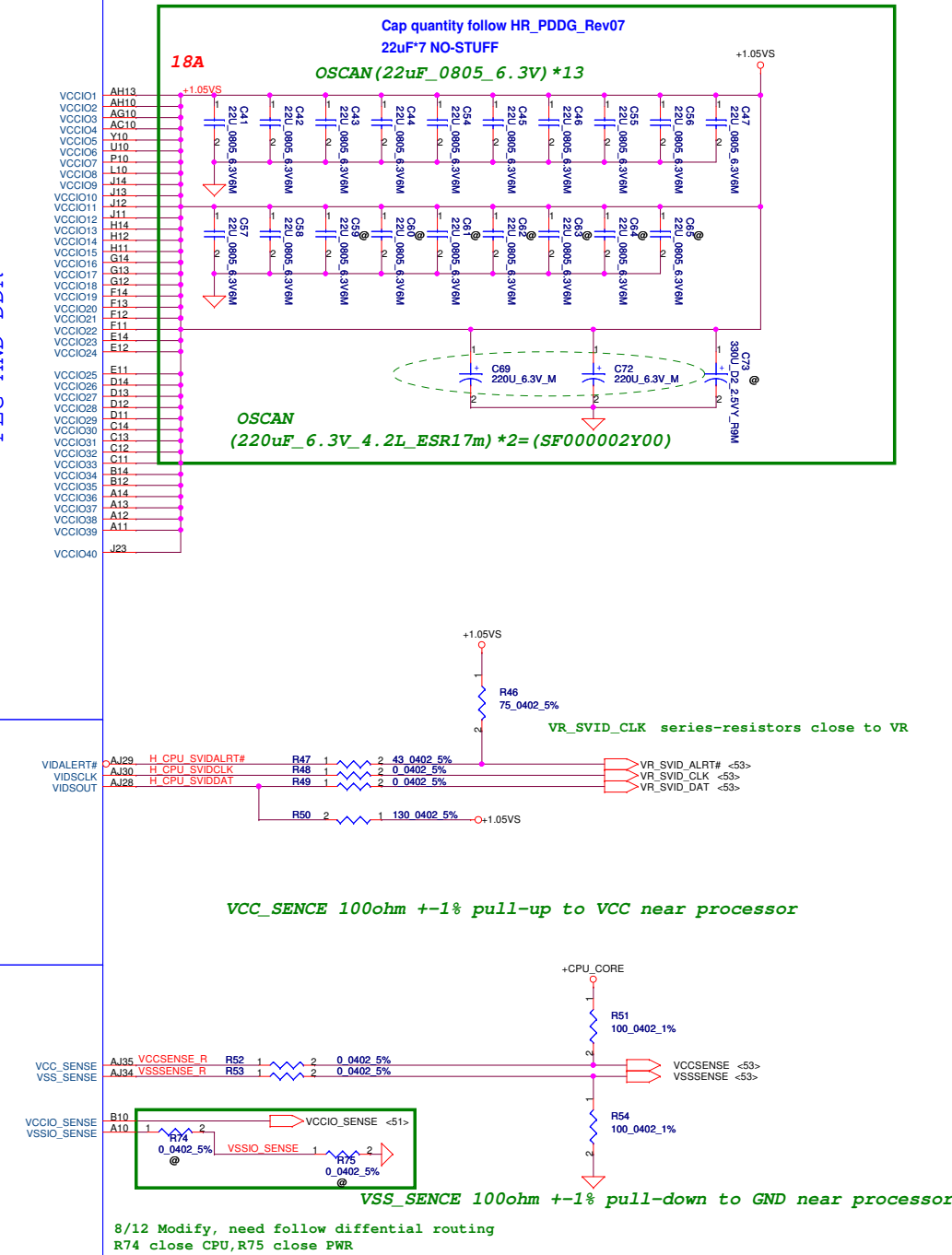
| | |
|------|--------|
| AG35 | VCC1 |
| AG34 | VCC2 |
| AG33 | VCC3 |
| AG32 | VCC4 |
| AG31 | VCC5 |
| AG30 | VCC6 |
| AG29 | VCC7 |
| AG28 | VCC8 |
| AG27 | VCC9 |
| AG26 | VCC10 |
| AF35 | VCC11 |
| AF34 | VCC12 |
| AF33 | VCC13 |
| AF32 | VCC14 |
| AF31 | VCC15 |
| AF30 | VCC16 |
| AF29 | VCC17 |
| AF28 | VCC18 |
| AF27 | VCC19 |
| AF26 | VCC20 |
| AD35 | VCC21 |
| AD34 | VCC22 |
| AD33 | VCC23 |
| AD32 | VCC24 |
| AD31 | VCC25 |
| AD30 | VCC26 |
| AD29 | VCC27 |
| AD28 | VCC28 |
| AD27 | VCC29 |
| AD26 | VCC30 |
| AC35 | VCC31 |
| AC34 | VCC32 |
| AC33 | VCC33 |
| AC32 | VCC34 |
| AC31 | VCC35 |
| AC30 | VCC36 |
| AC29 | VCC37 |
| AC28 | VCC38 |
| AC27 | VCC39 |
| AC26 | VCC40 |
| AA35 | VCC41 |
| AA34 | VCC42 |
| AA33 | VCC43 |
| AA32 | VCC44 |
| AA31 | VCC45 |
| AA30 | VCC46 |
| AA29 | VCC47 |
| AA28 | VCC48 |
| AA27 | VCC49 |
| AA26 | VCC50 |
| Y35 | VCC51 |
| Y34 | VCC52 |
| Y33 | VCC53 |
| Y32 | VCC54 |
| Y31 | VCC55 |
| Y30 | VCC56 |
| Y29 | VCC57 |
| Y28 | VCC58 |
| Y27 | VCC59 |
| Y26 | VCC60 |
| Y25 | VCC61 |
| Y24 | VCC62 |
| Y23 | VCC63 |
| Y22 | VCC64 |
| Y21 | VCC65 |
| Y20 | VCC66 |
| Y19 | VCC67 |
| Y18 | VCC68 |
| Y17 | VCC69 |
| Y16 | VCC70 |
| Y15 | VCC71 |
| Y14 | VCC72 |
| Y13 | VCC73 |
| Y12 | VCC74 |
| Y11 | VCC75 |
| Y10 | VCC76 |
| Y09 | VCC77 |
| Y08 | VCC78 |
| Y07 | VCC79 |
| Y06 | VCC80 |
| Y05 | VCC81 |
| Y04 | VCC82 |
| Y03 | VCC83 |
| Y02 | VCC84 |
| Y01 | VCC85 |
| R30 | VCC86 |
| R29 | VCC87 |
| R28 | VCC88 |
| R27 | VCC89 |
| R26 | VCC90 |
| R25 | VCC91 |
| R24 | VCC92 |
| P33 | VCC93 |
| P32 | VCC94 |
| P31 | VCC95 |
| P30 | VCC96 |
| P29 | VCC97 |
| P28 | VCC98 |
| P27 | VCC99 |
| P26 | VCC100 |

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

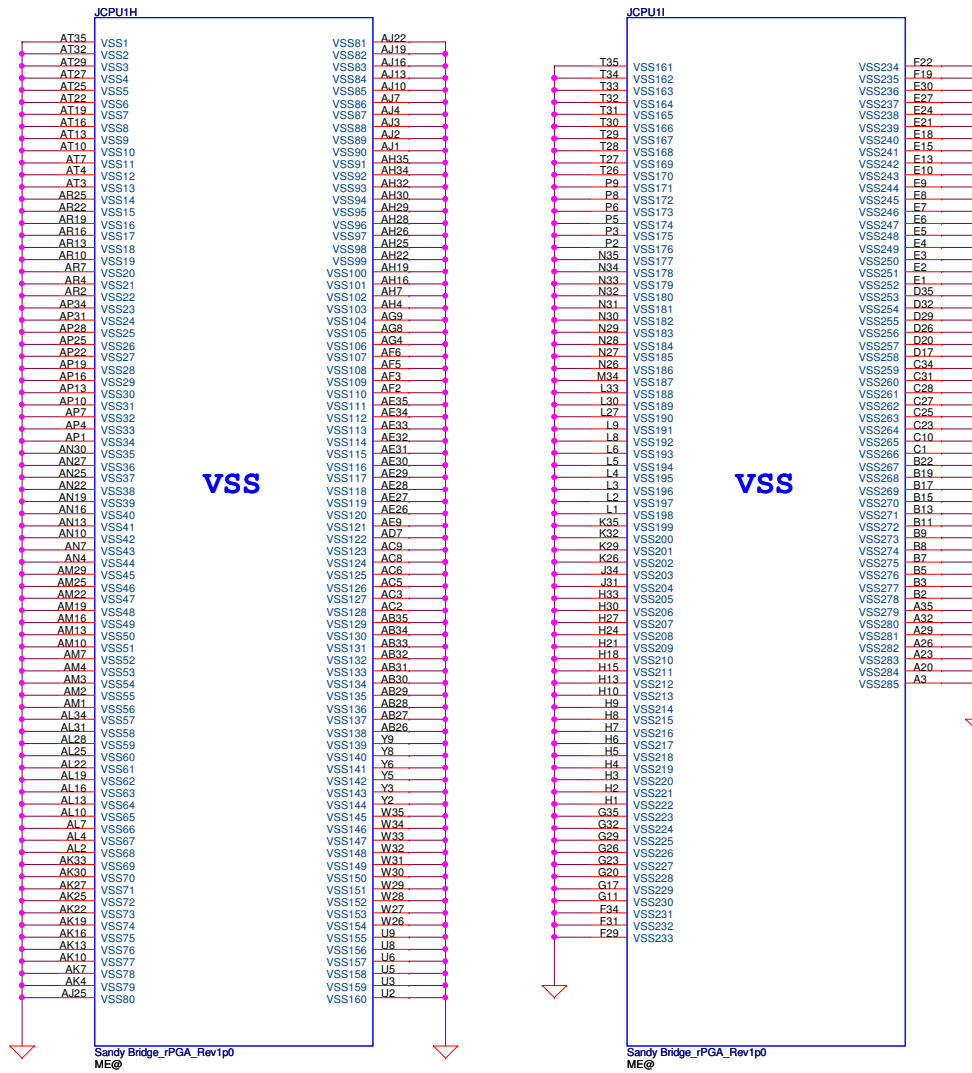


Sandy Bridge_PPGA Rev1.0
ME@

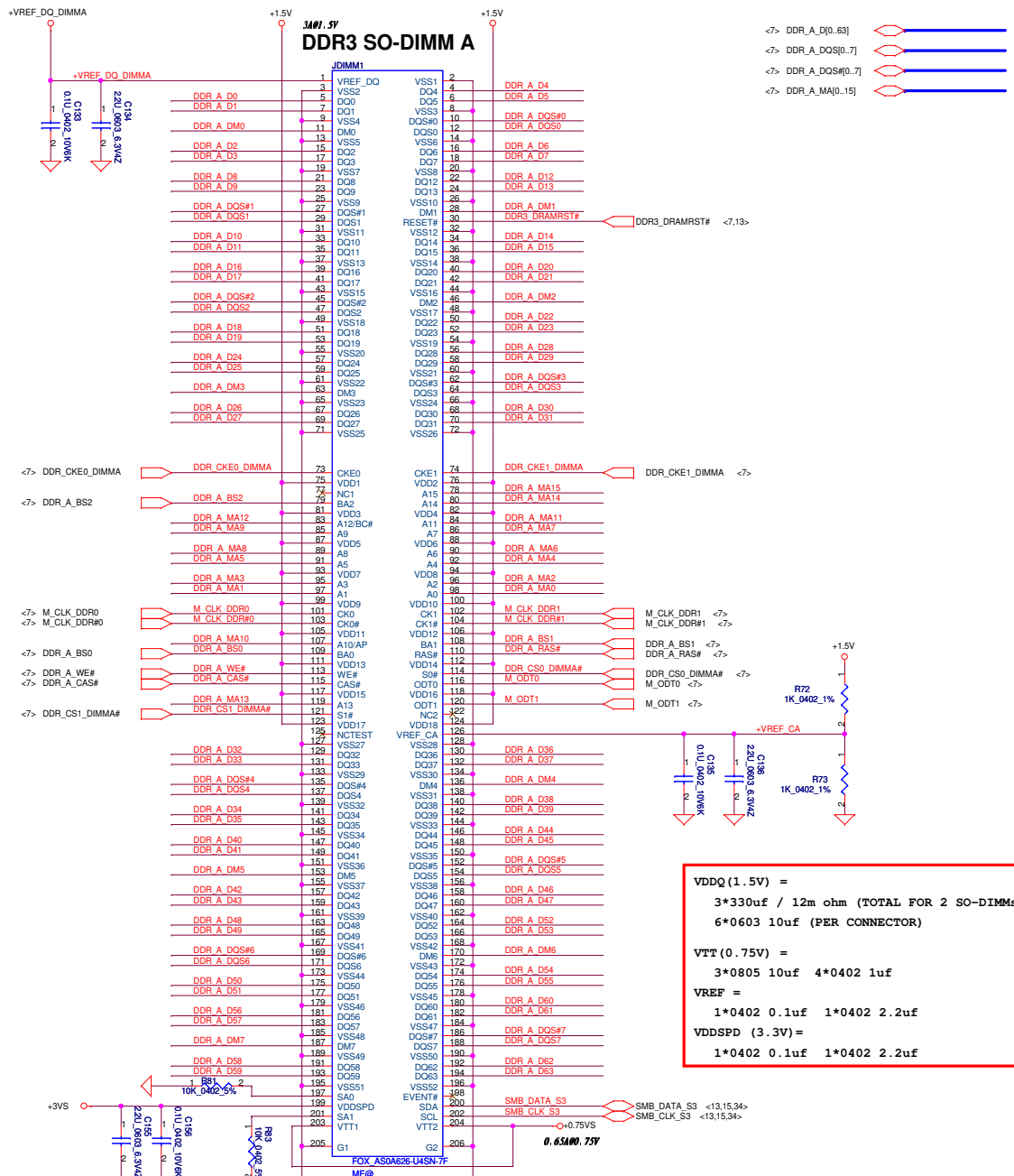
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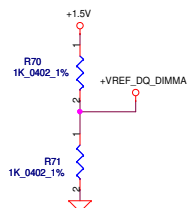
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| Custom | LA-6751P | 0.2 | | |
| Date: | Friday, November 26, 2010 | Sheet | 11 | of 59 |

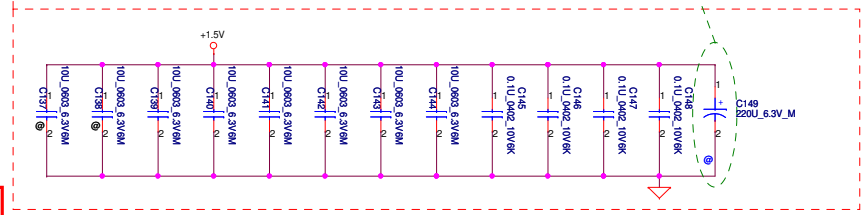


- <7> DDR_A_D[0..63]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_DQS#0..7]
- <7> DDR_A_MAI[0..15]



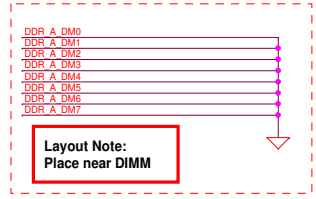
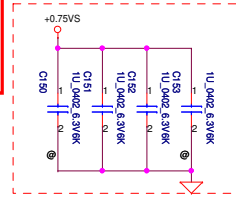
Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
 (10uF_0603_6.3V)*8
 (0.1uF_402_10V)*4



Layout Note:
Place near DIMM

7/28 Update connect GND directly



Layout Note:
Place near DIMM

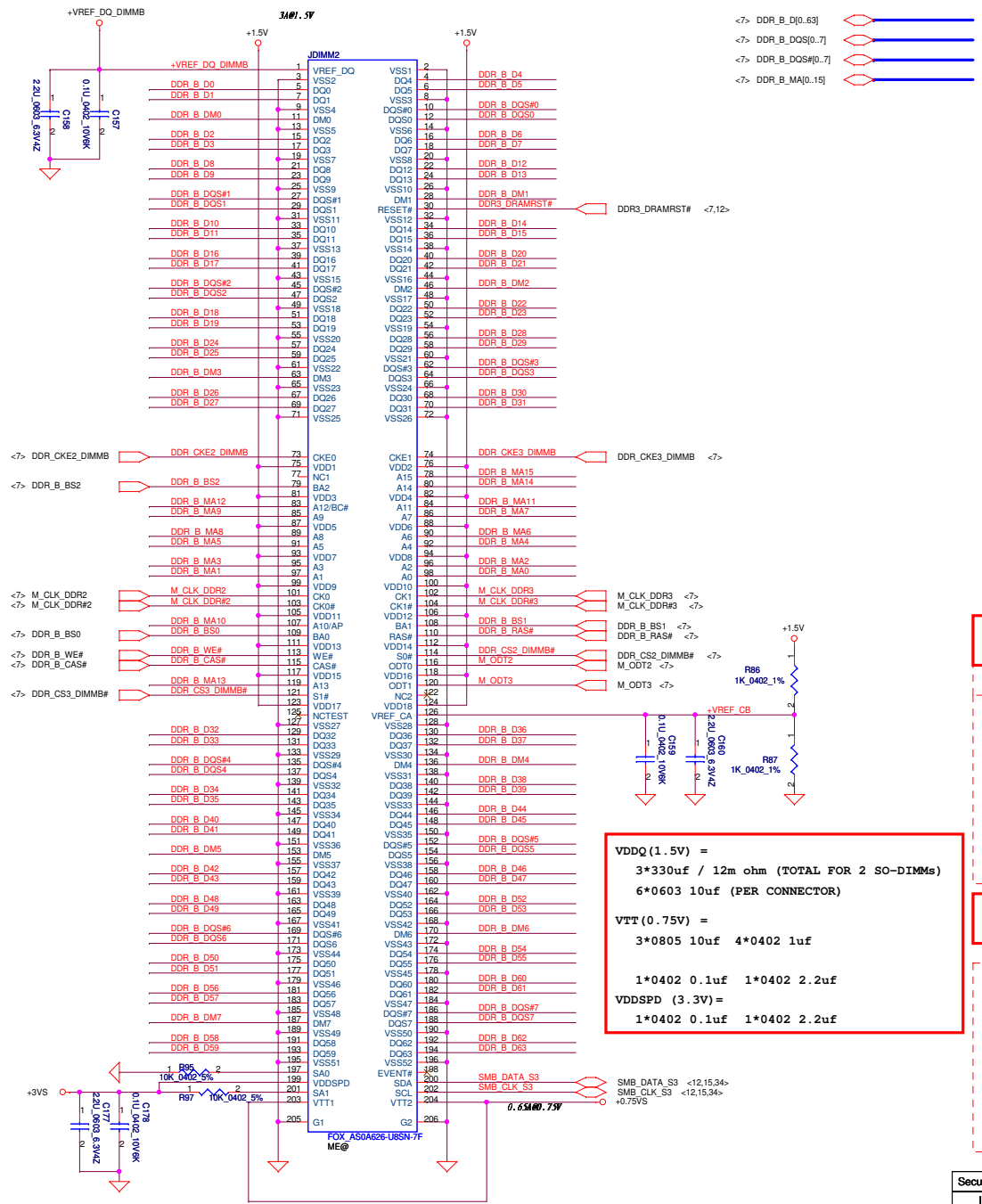
VDDQ (1.5V) =
 3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
 6*0603 10uf (PER CONNECTOR)

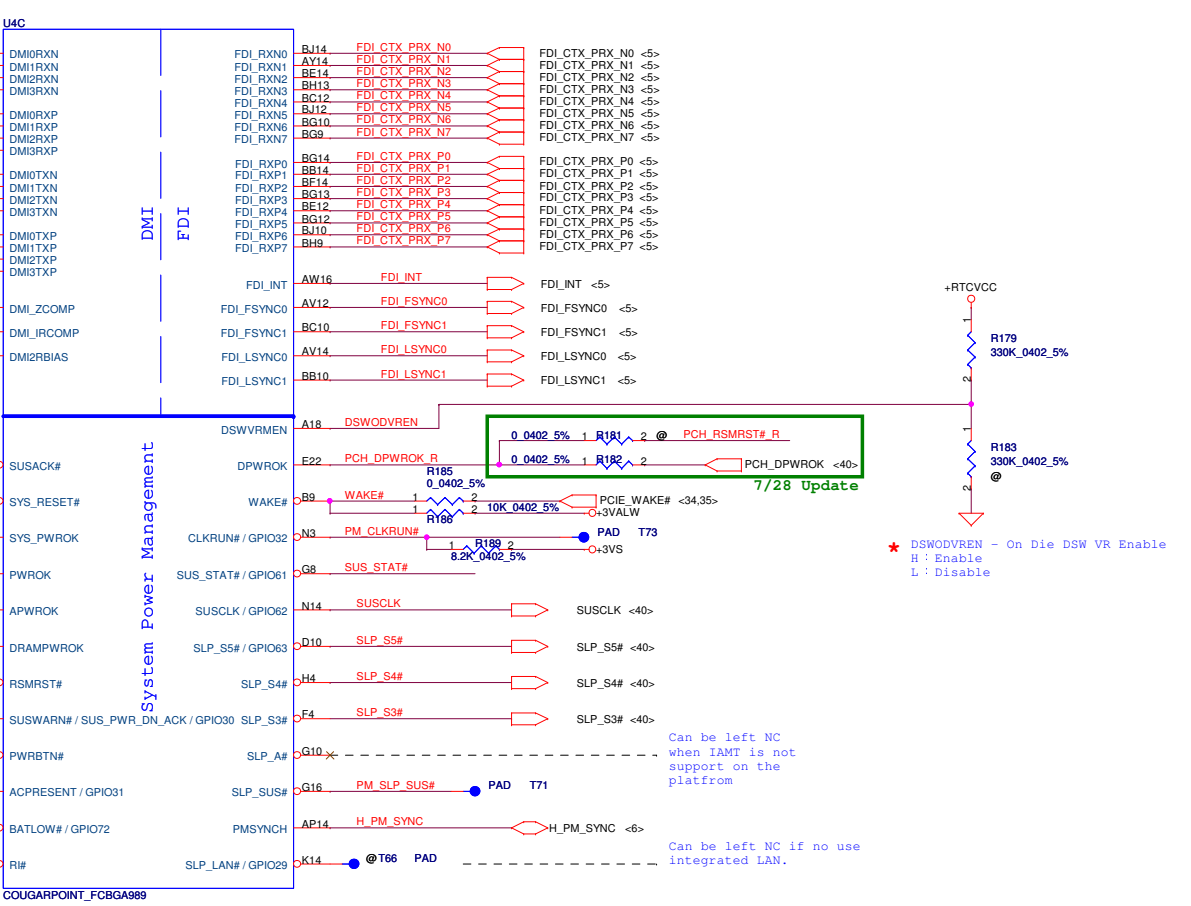
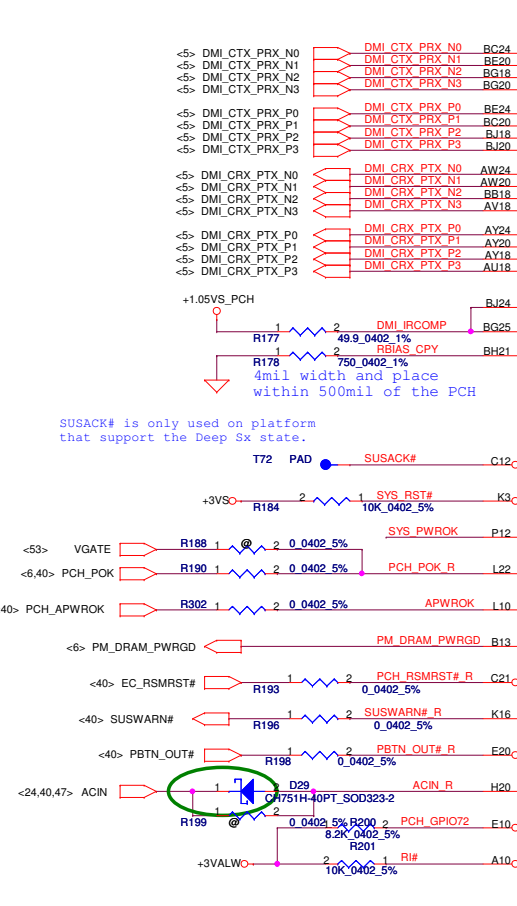
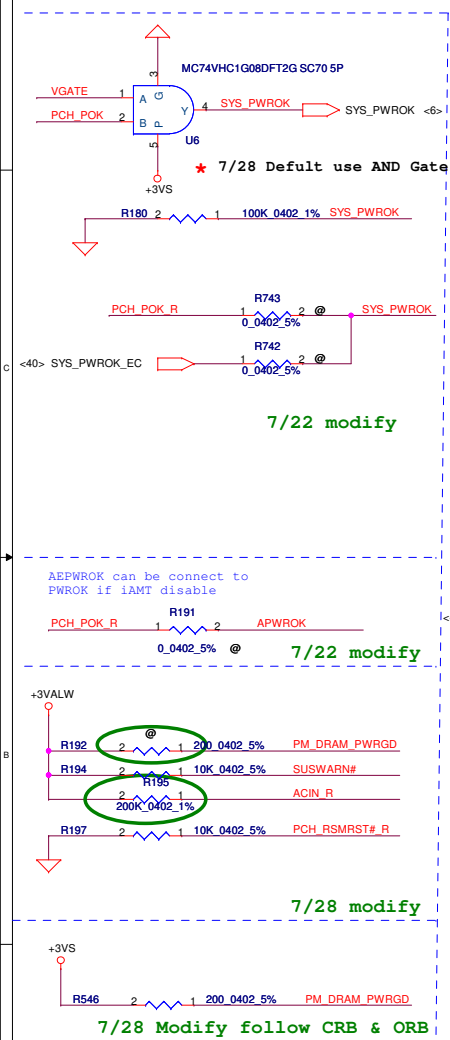
VTT (0.75V) =
 3*0805 10uf 4*0402 1uf

VREF =
 1*0402 0.1uf 1*0402 2.2uf

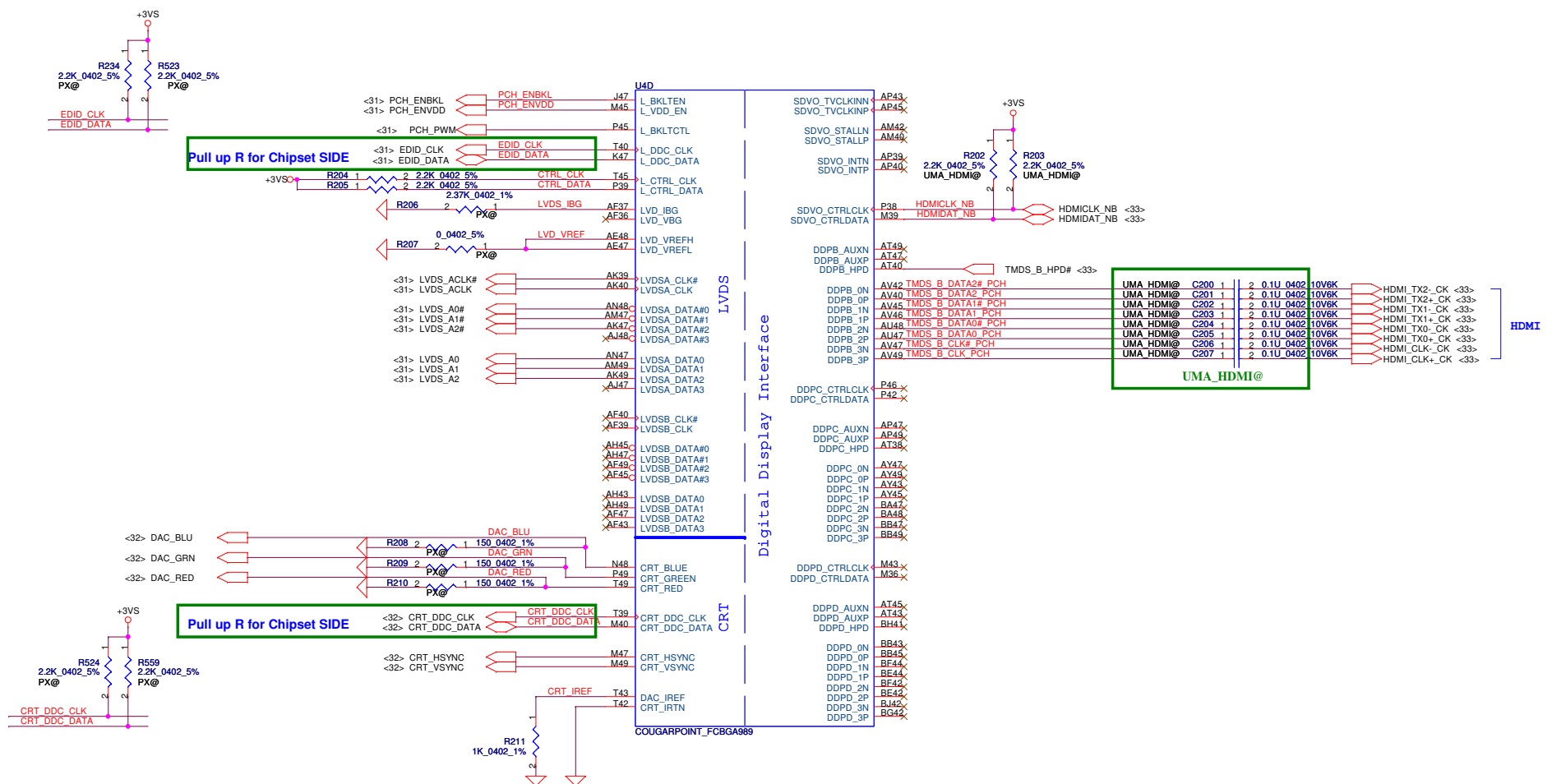
VDDSPD (3.3V) =
 1*0402 0.1uf 1*0402 2.2uf

| | | | | | |
|---|---------------------------|-----------------|------------|---------------------------------|---------|
| Security Classification | Compal Secret Data | | Title | Compal Electronics, Inc. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | DDR3-SODIMM SLOT1 | |
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| Date: | Friday, November 26, 2010 | ISheet | 12 | of | 59 |





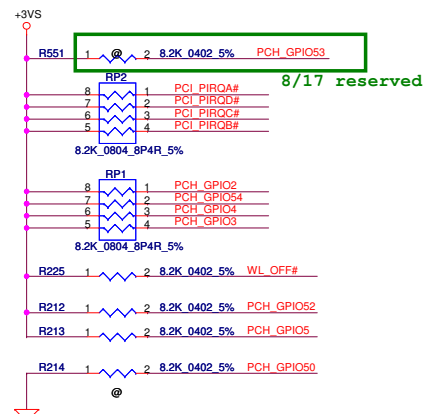
| | | | | | |
|---|------------|--------------------|------------|--------------------------|---------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title | |
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| | | | | Customer | LA-6751P |
| | | | | Date: | Friday, November 26, 2010 |
| | | | | Sheet | 16 of 59 |
| | | | | Rev | 0.2 |



| | | |
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| Issued Date | 2010/07/12 | Deciphered Date |
| | | 2012/07/11 |

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| | | |
|--|---------------------------|----------------|
| Compal Electronics, Inc. PCH (4/9) LVDS,CRT,DP,HDMI | | |
| Title | | |
| Size | Document Number | Rev |
| Customer | LA-6751P | 0.2 |
| Date: | Friday, November 26, 2010 | Sheet 17 of 59 |



PCH_GPIO51 R221 1 2 1K 0402 5%

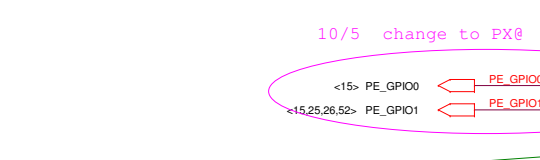
WL_OFF# R215 1 2 1K 0402 5%

| Boot BIOS Strap bit1 BBS1 | | |
|---------------------------|-------|-----------------------|
| Bit11 | Bit10 | Boot BIOS Destination |
| 0 | 0 | Reserved |
| 1 | 0 | Reserved |
| 1 | 1 | * SPI (Default) |
| 0 | 0 | LPC |

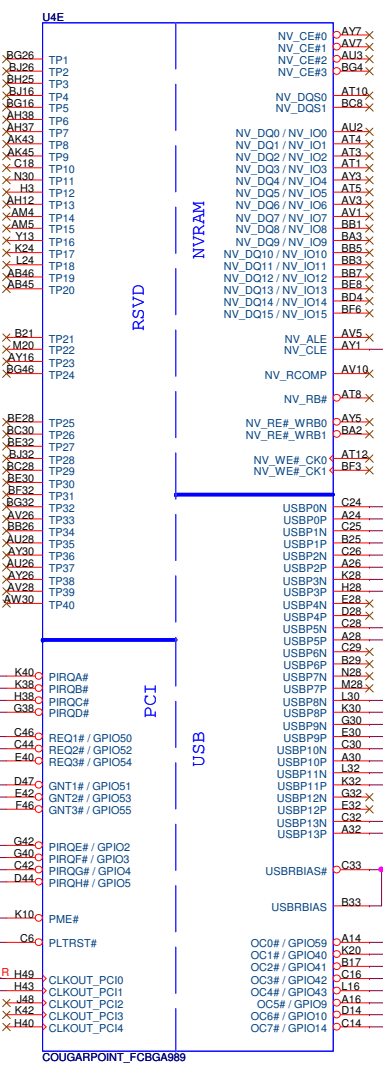
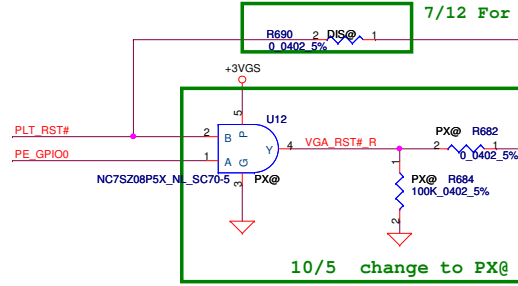
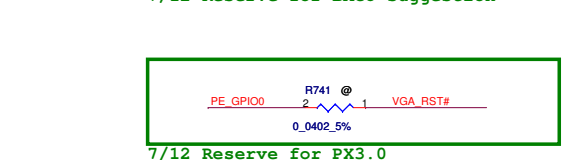
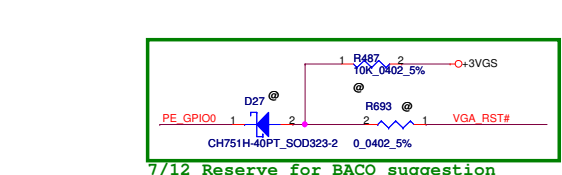
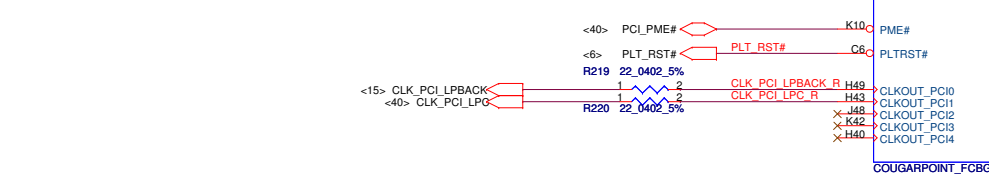
A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled High=Default *

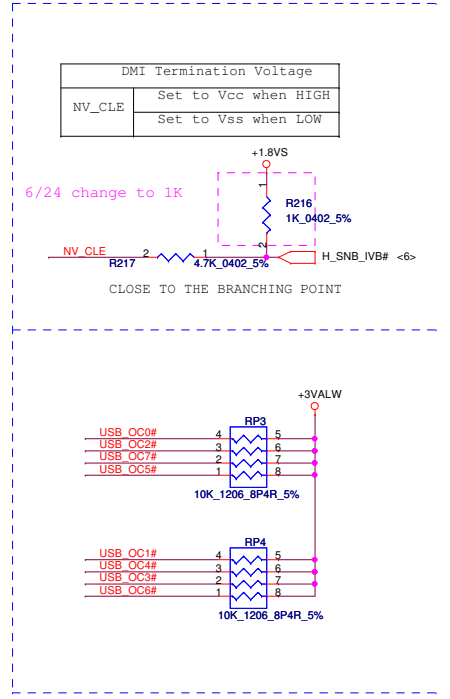
PCI_GNT13#



GPIO53=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



- USB20_N0 <-56,57> RIGHT USB
- USB20_P0 <-56,57> LEFT USB
- USB20_N1 <-38> LEFT USB
- USB20_P1 <-38> USB charger
- USB20_N2 <-2> LEFT USB
- USB20_P2 <-2> LEFT USB (COMBO)
- USB20_N3 <-2> LEFT USB
- USB20_P3 <-2> LEFT USB
- USB20_N4 <-2> LEFT USB
- USB20_P4 <-2> LEFT USB
- USB20_N5 <-31> USB Camera
- USB20_P5 <-31> USB Camera
- USB20_N6 <-31> USB Camera
- USB20_P6 <-31> USB Camera
- USB20_N7 <-31> USB Camera
- USB20_P7 <-31> USB Camera
- USB20_N8 <-31> USB Camera
- USB20_P8 <-31> USB Camera
- USB20_N9 <-34> 8/6 WLAN change
- USB20_P9 <-34> WLAN to port 9
- USB20_N10 <-34> CARD READER
- USB20_P10 <-34> CARD READER
- USB20_N11 <-43> CARD READER
- USB20_P11 <-43> CARD READER
- USB20_N12 <-42> Bluetooth
- USB20_P12 <-42> Bluetooth
- USB20_N13 <-42> Bluetooth
- USB20_P13 <-42> Bluetooth
- USB20_N14 <-42> Bluetooth
- USB20_P14 <-42> Bluetooth
- USB20_N15 <-42> Bluetooth
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- USB20_N97 <-42> Bluetooth
- USB20_P97 <-42> Bluetooth
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- USB20_P98 <-42> Bluetooth
- USB20_N99 <-42> Bluetooth
- USB20_P99 <-42> Bluetooth
- USB20_N100 <-42> Bluetooth
- USB20_P100 <-42> Bluetooth

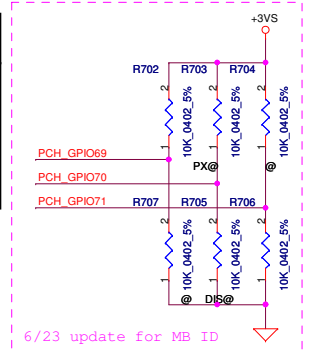


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| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 |

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| | | |
|--------------------------|---------------------------|----------------|
| Compal Electronics, Inc. | | |
| PCH (5/9) PCI, USB | | |
| Size | Document Number | Rev |
| Custom | LA-6751P | 0.1 |
| Date: | Friday, November 26, 2010 | Sheet 18 of 59 |

| PCH_GPIO69 | PCH_GPIO70 | PCH_GPIO71 | Function |
|------------|------------|------------|----------|
| 0 | 0 | 0 | UMA |
| 1 | 0 | 0 | DIS |
| 0 | 1 | 0 | PX3.0 |
| 1 | 1 | 0 | PX4.0 * |



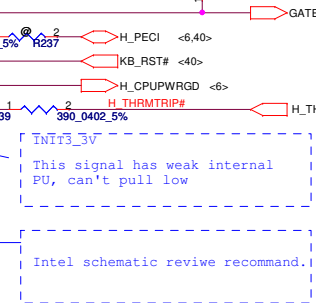
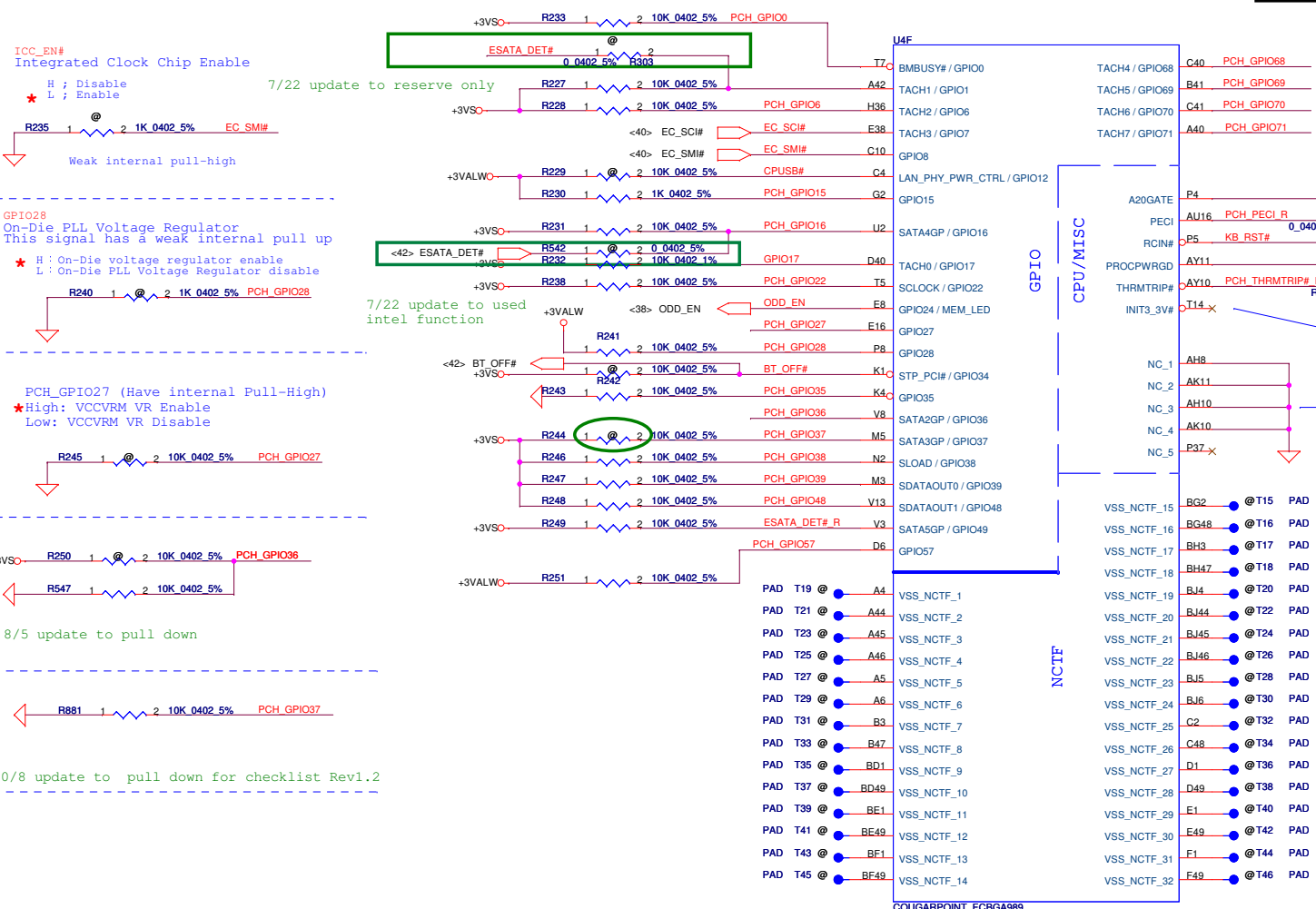
ICCNEN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
★ ; Enable

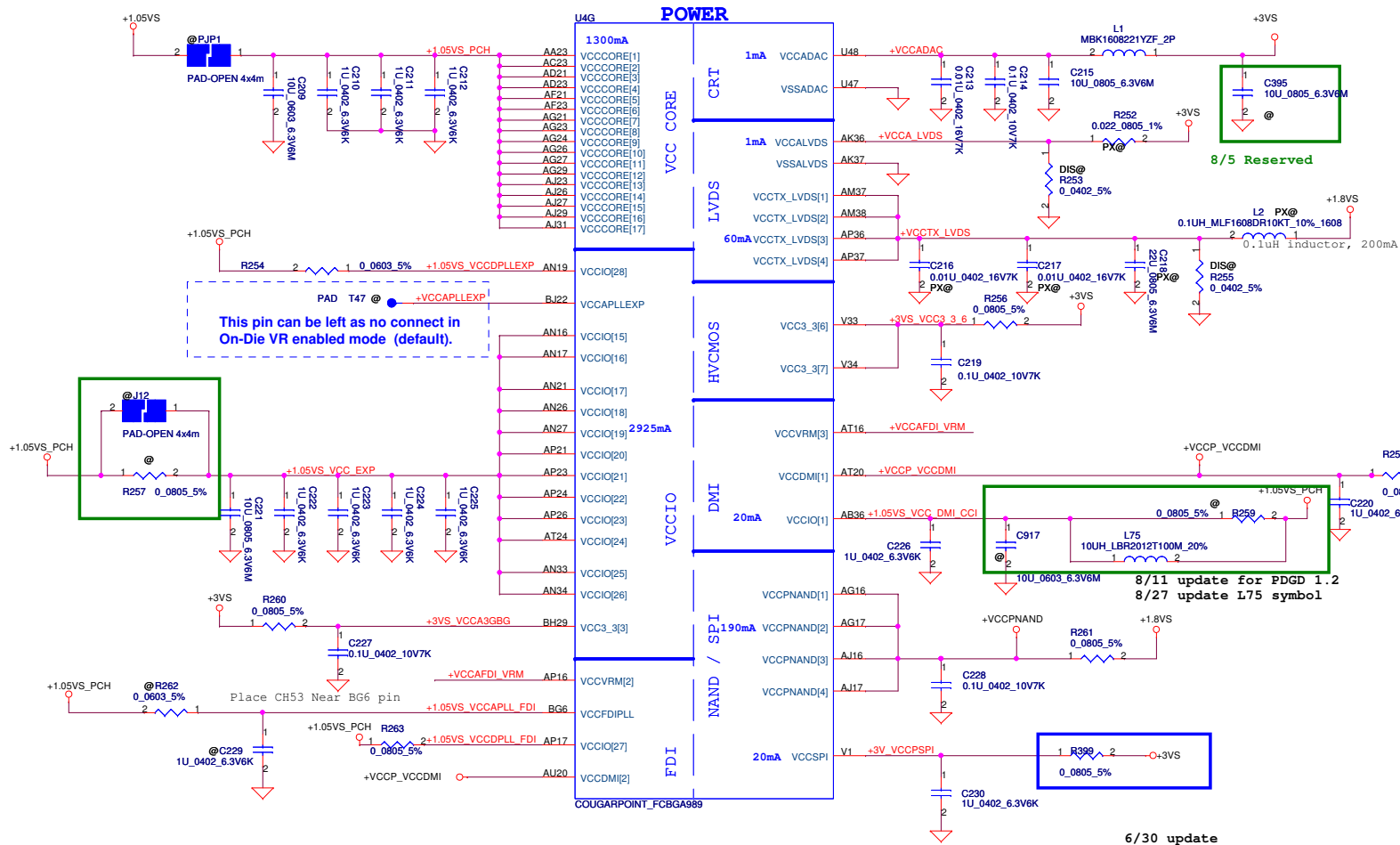
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
★ ; Enable

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable

8/5 update to pull down

10/8 update to pull down for checklist Rev1.2

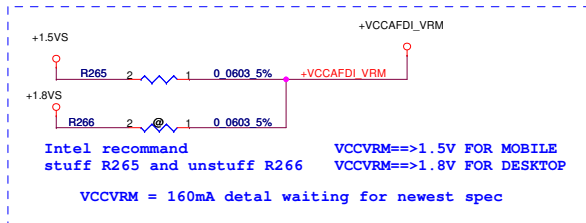




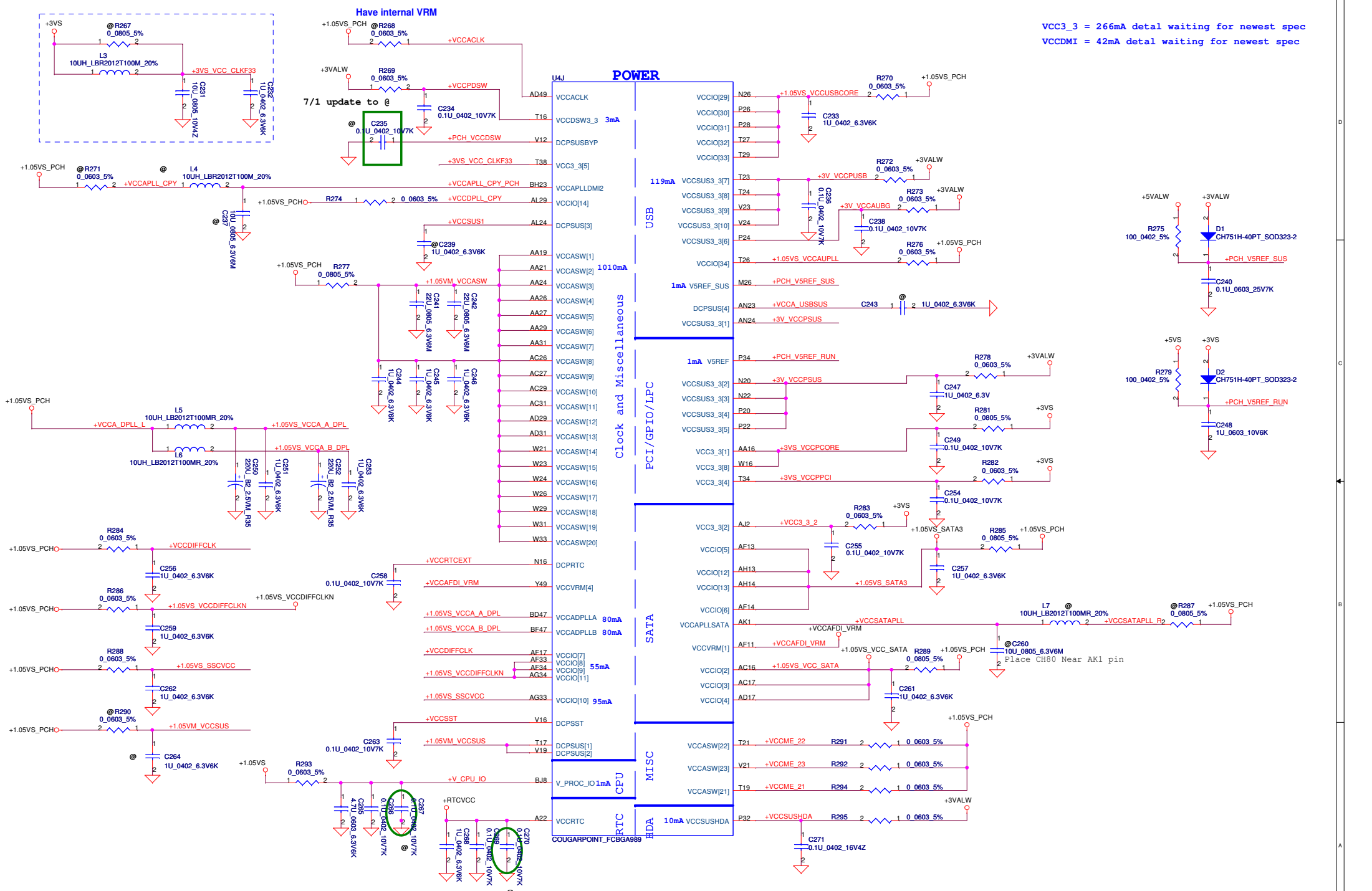
This pin can be left as no connect in On-Die VR enabled mode (default).

8/11 update for PDGD 1.2
8/27 update L75 symbol

6/30 update



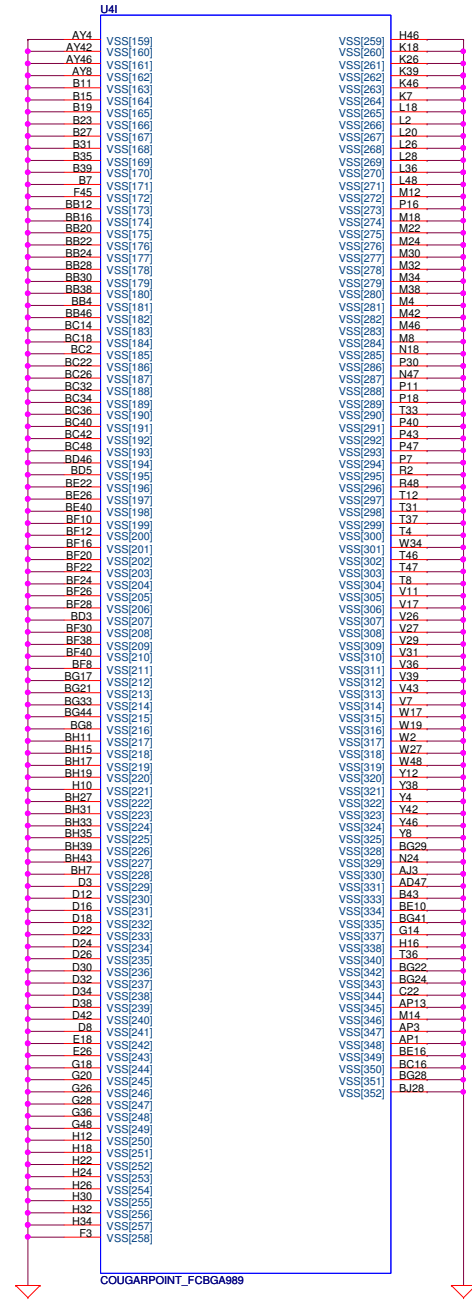
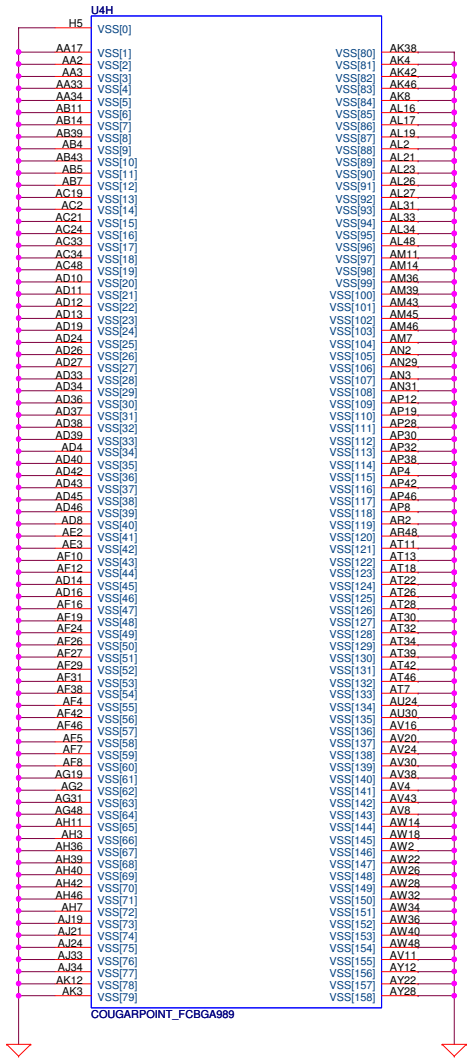
| PCH Power Rail Table | | |
|----------------------|-----------|-----------------------|
| Voltage Rail | Voltage | SO Iccmax Current (A) |
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_Sus | 5 | 0.001 |
| Vcc3_3 | 3.3 | 0.266 |
| VccADAC | 3.3 | 0.001 |
| VccADPLLA | 1.05 | 0.08 |
| VccADPLLB | 1.05 | 0.08 |
| VccCore | 1.05 | 1.3 |
| VccDMI | 1.05 | 0.042 |
| VccIO | 1.05 | 2.925 |
| VccASW | 1.05 | 1.01 |
| VccSPI | 3.3 | 0.02 |
| VccDSW | 3.3 | 0.003 |
| VccpNAND | 1.8 | 0.19 |
| VccRTC | 3.3 | 6 uA |
| VccSus3_3 | 3.3 | 0.119 |
| VccSusHDA | 3.3 / 1.5 | 0.01 |
| VccVRM | 1.8 / 1.5 | 0.16 |
| VccCLKDMI | 1.05 | 0.02 |
| VccSSC | 1.05 | 0.095 |
| VccDIFFCLKN | 1.05 | 0.055 |
| VccALVDS | 3.3 | 0.001 |
| VccTX_LVDS | 1.8 | 0.06 |



VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

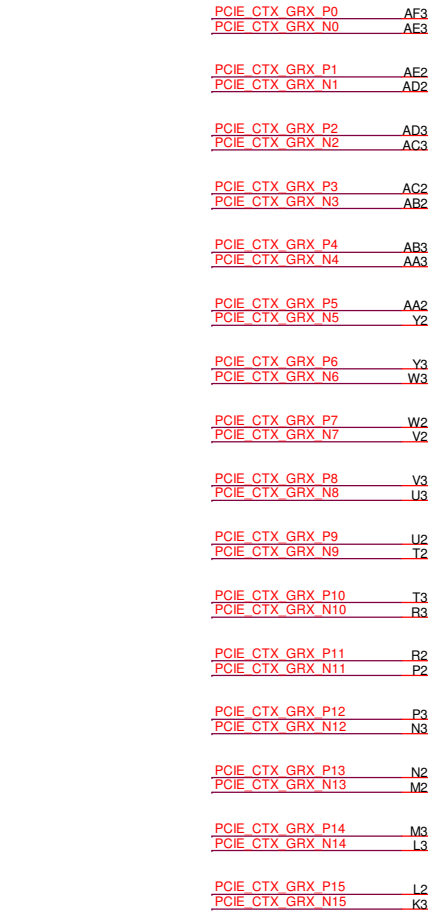
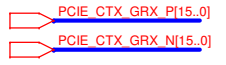
| Security Classification | Compal Secret Data | | |
|---|--------------------|-----------------|------------|
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 |
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| | | | | |
|--------|---------------------------|-------|---------------------------------|-------|
| Title | | | Compal Electronics, Inc. | |
| Title | | | PCH (8/9) PWR | |
| Size | Document Number | | | Rev |
| Custom | LA-6751P | | | 0.2 |
| Date: | Friday, November 26, 2010 | Sheet | 21 | of 59 |



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|
| Security Classification | Compal Secret Data | | | Title | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Compal Electronics, Inc. | |
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| | | | | Customer | 0.2 |
| | | | | Date: | Friday, November 26, 2010 |
| | | | | Sheet | 22 of 59 |

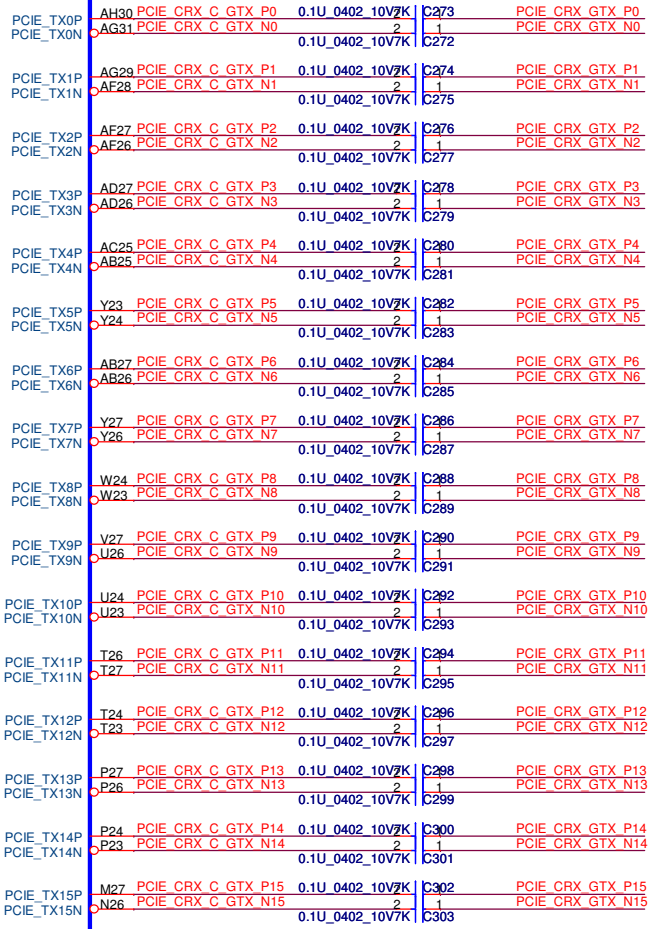
<5> PCIE_CTX_GRX_P[15..0]
 <5> PCIE_CTX_GRX_N[15..0]



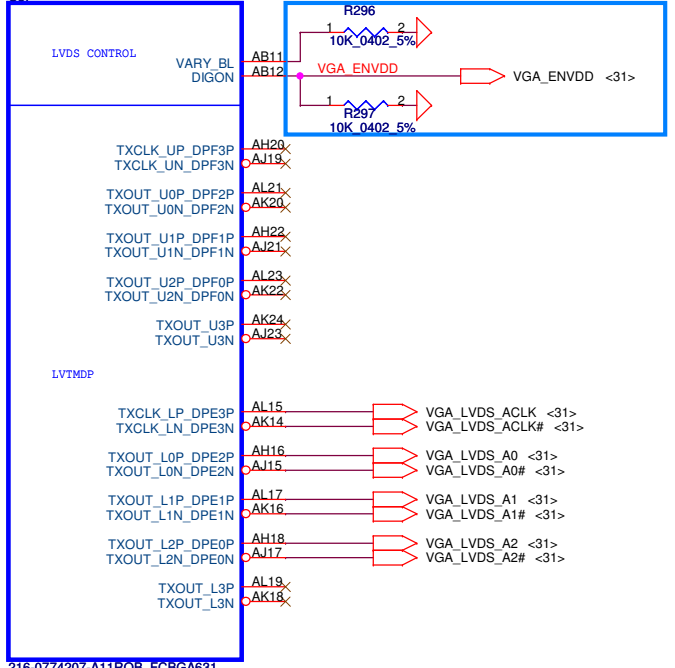
U8A

PCI EXPRESS INTERFACE

PCIE_CRX_GTX_P[15..0]
 PCIE_CRX_GTX_N[15..0]

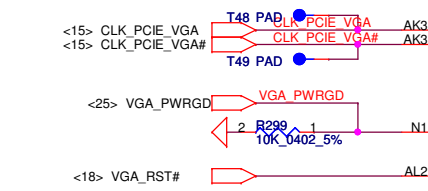


U8F



216-0774207-A11ROB_FCBGA631

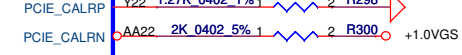
LVDS



CLOCK



CALIBRATION

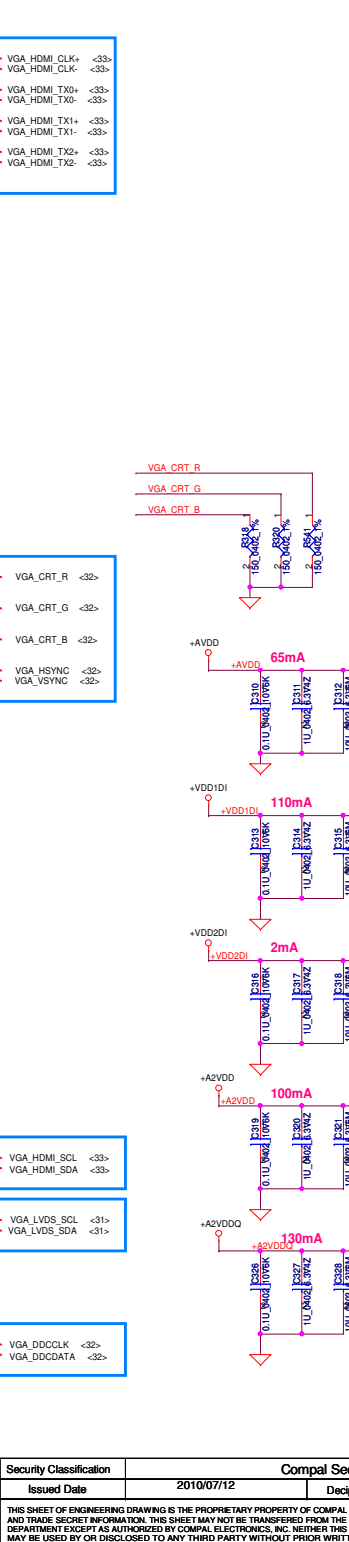
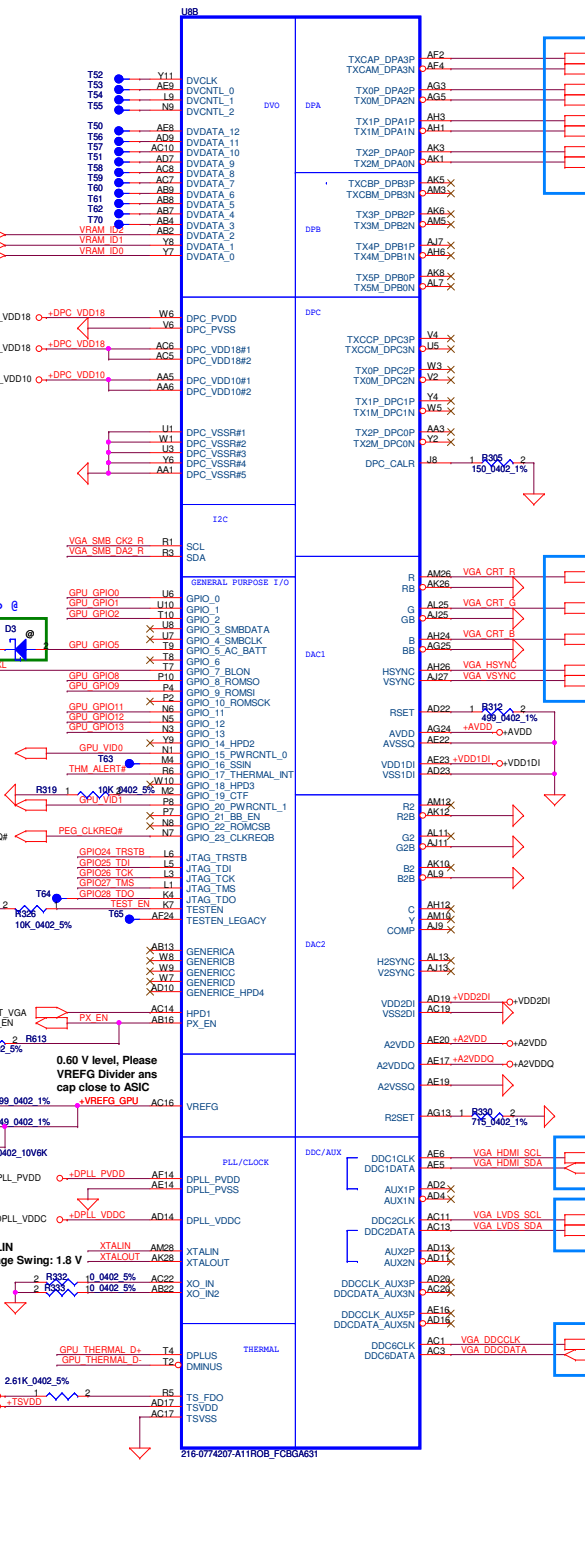
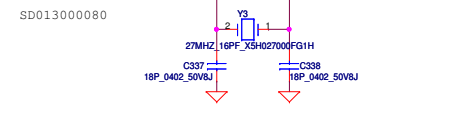
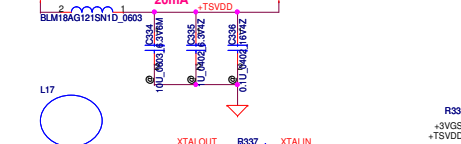
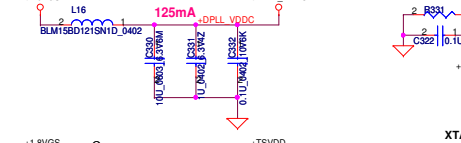
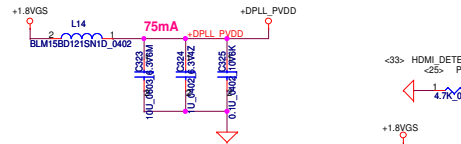
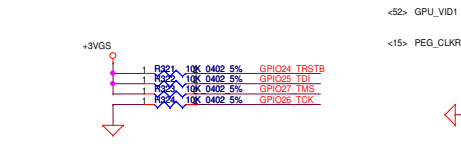
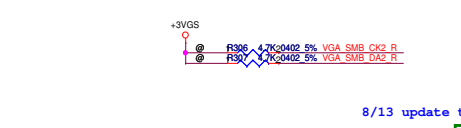
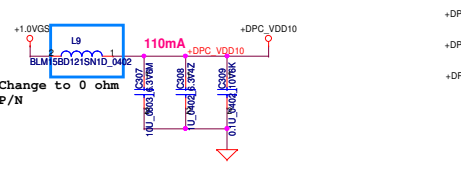
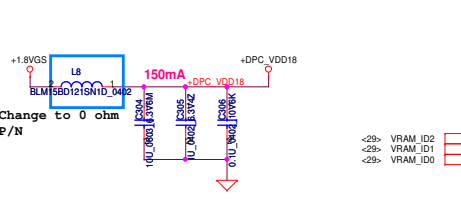


216-0774207-A11ROB_FCBGA631

PCIE LANE

| | | | | | |
|---|---------------------------|--------------------|------------|--------------------------|-----|
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| Size | Document Number | | | Rev | 0.1 |
| Date: | Friday, November 26, 2010 | Sheet | 23 | of | 59 |

| | | |
|--------------|-------|---|
| TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop) |
| TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop) |



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

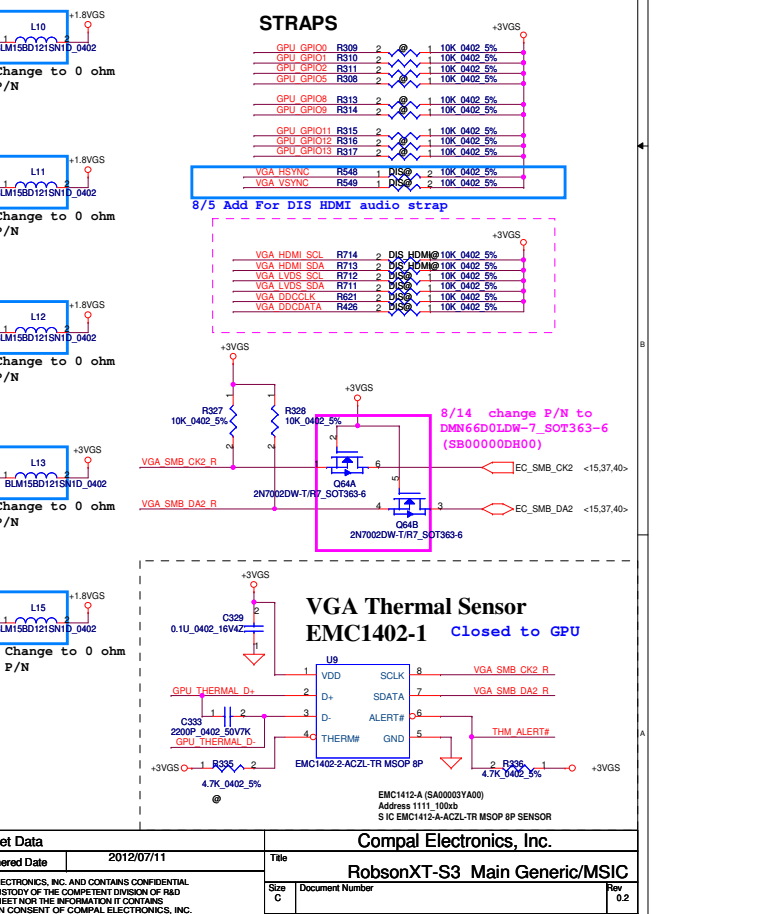
| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS |
|----------------------|----------------|---|----------------------|
| TX_PWRS_ENB | GPIO0 | POE FULL TX OUTPUT SWING | X |
| TX_DEEMPH_EN | GPIO1 | POE TRANSMITTER DE-EMPHASIS ENABLED | X |
| RSVD | GPIO2 | RESERVED | 0 |
| RSVD | GPIO8 | RESERVED | 0 |
| BIF_VGA_DIS | GPIO9 | VGA ENABLED | 0 |
| RSVD | GPIO21 | RESERVED | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM | X |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | XXX |
| VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | 0 |
| RSVD | H2SYNC | | 0 |
| RSVD | GENERICC | | 0 |
| AUD[0] | HSYNC | AUD[0] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI | 11 |

RECOMMENDED SETTINGS
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEFENDANT
NA = NOT APPLICABLE

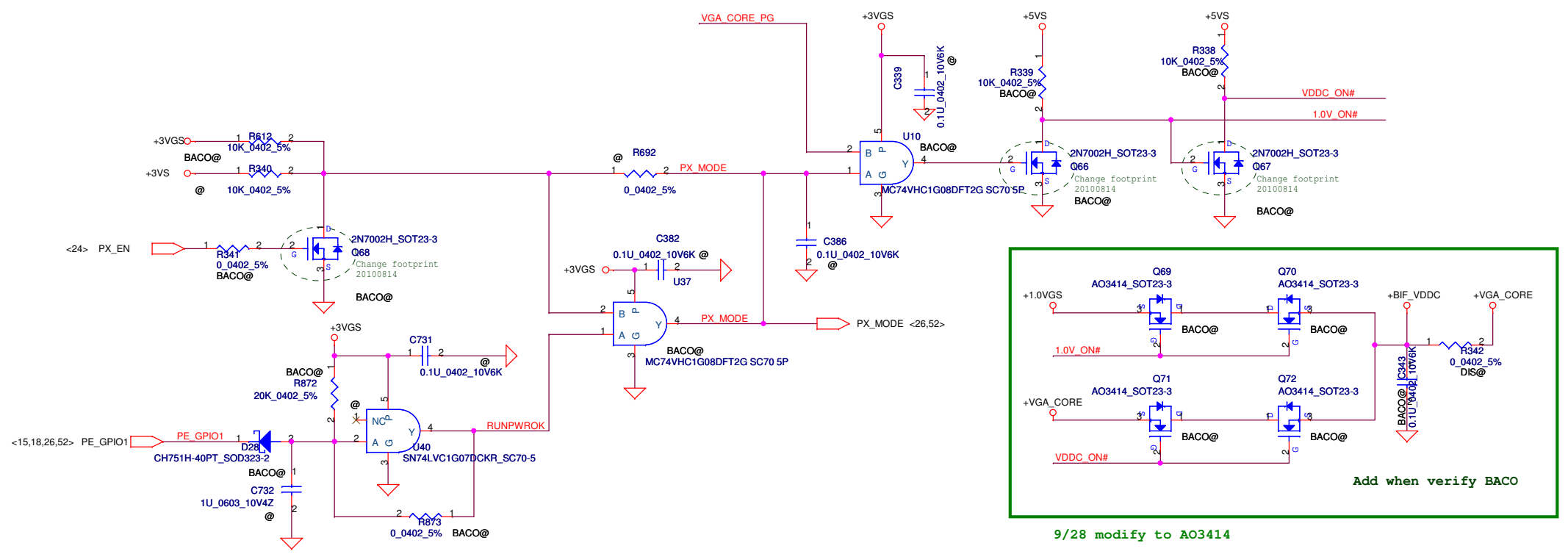
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS |
|--------|--------|---------------------------------|----------------------|
| GPIO21 | H2SYNC | | 0 |
| GPIO2 | GPIO2 | | 0 |
| GPIO8 | GPIO8 | | 0 |



<52> VGA_CORE_PG @ 0_0402_5% R669 1 2 VGA_PWRGD <23>

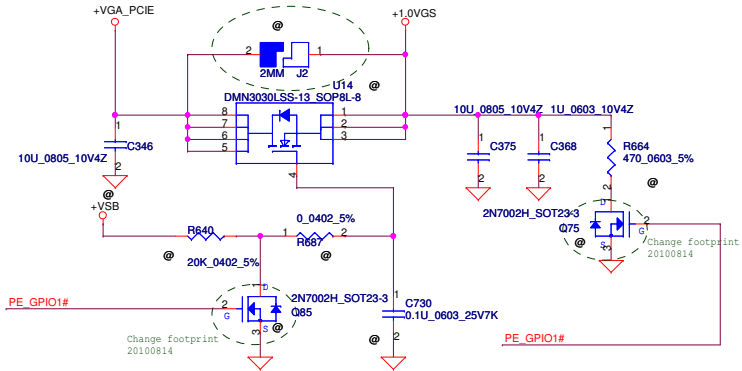


D28 with leakage need to check

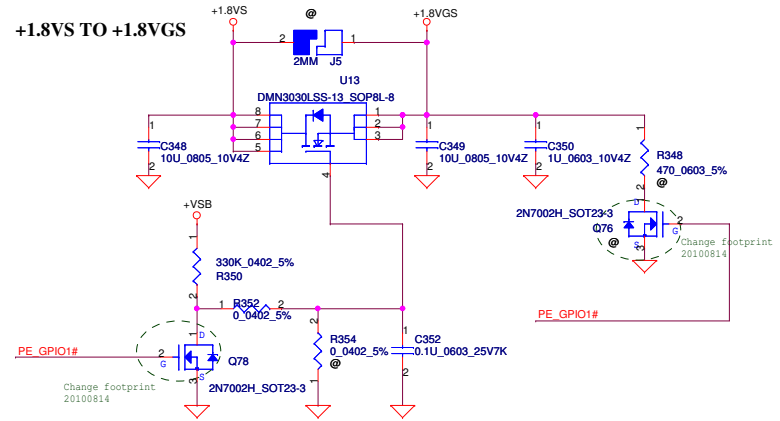
| | | | | | |
|---|------------|--------------------|------------|------------------------------------|-----------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title PARK-S3 Main Generic/MSIC | |
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| | | | | Date: Friday, November 26, 2010 | Sheet 25 of 59 |

+VGA_PCIE TO +1.0VGS

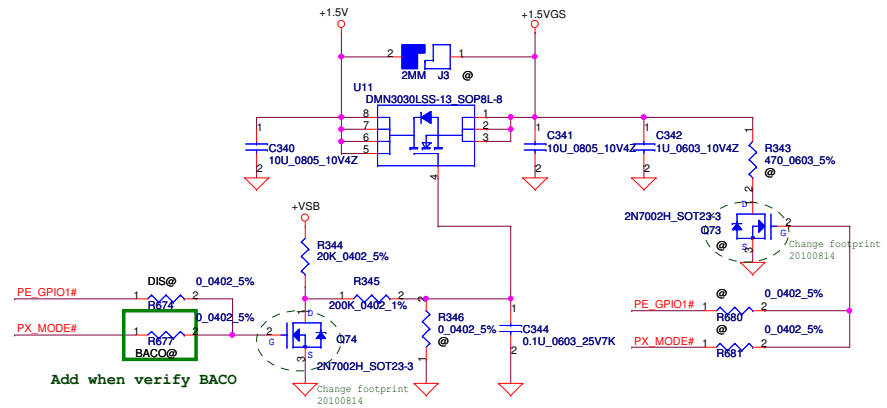
Short J2 for control sequence at PWM



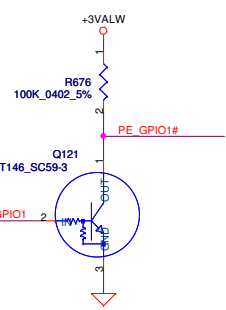
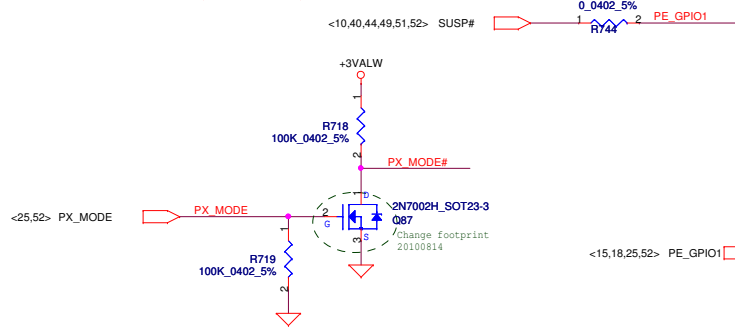
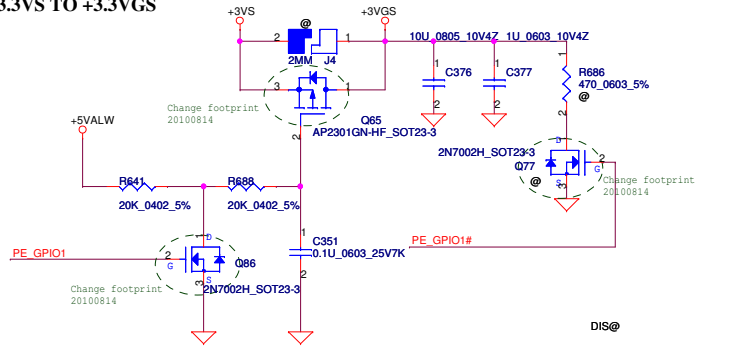
+1.8VS TO +1.8VGS



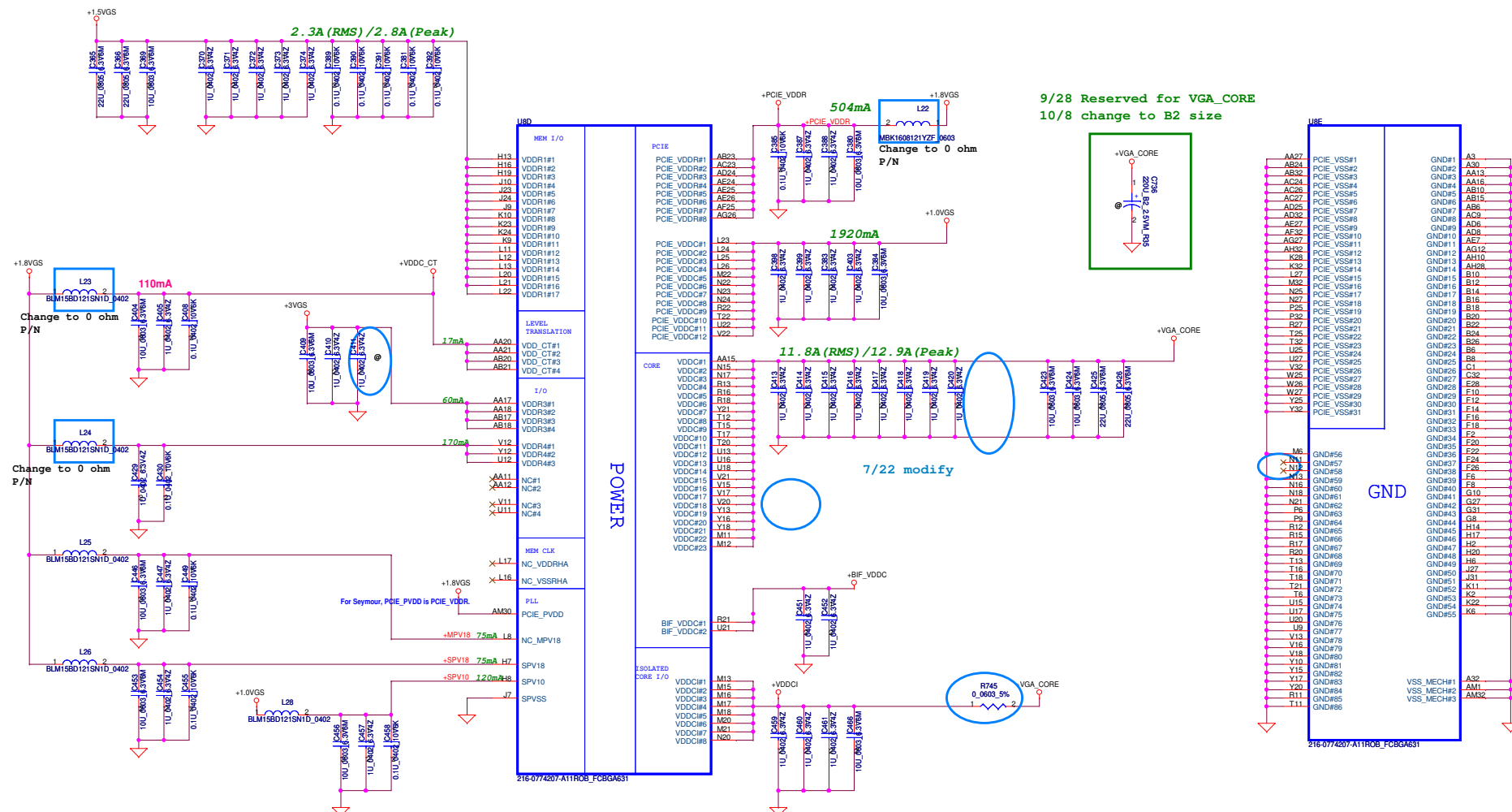
+1.5VS TO +1.5VGS



+3.3VS TO +3.3VGS



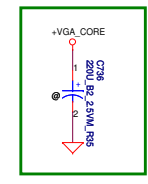
| | | | | |
|---|--------------------|-----------------|--------------------------|--------------------------------|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title |
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| Date: Friday, November 26, 2010 | | | | Rev 0.1 |
| Sheet 26 of 59 | | | | |



+1.8VGS
2.3A (RMS) / 2.8A (Peak)

+PCIE_VDDR
504mA
MBK1608121Y2Z 0603
Change to 0 ohm P/N

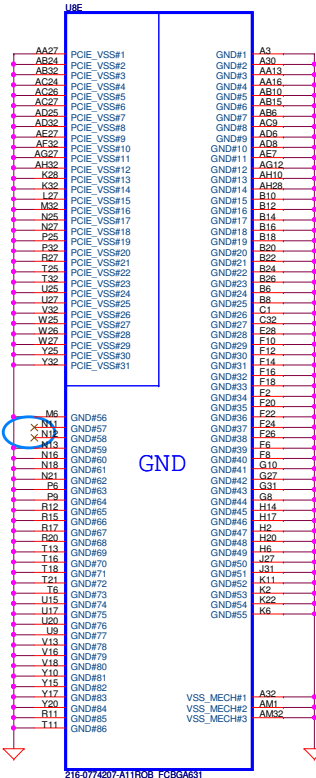
9/28 Reserved for VGA_CORE
10/8 change to B2 size



+1.8VGS
1920mA

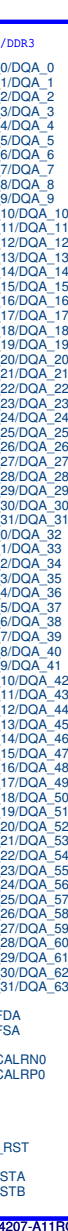
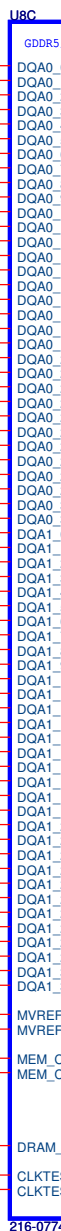
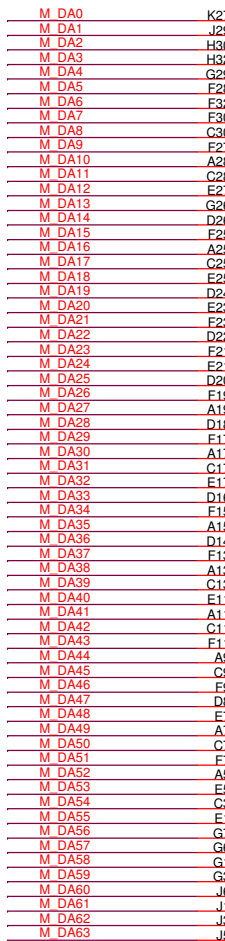
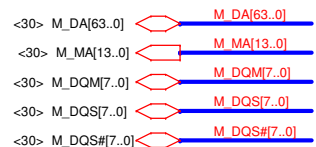
11.8A (RMS) / 12.9A (Peak)

7/22 modify

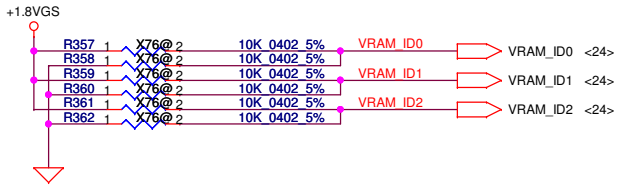
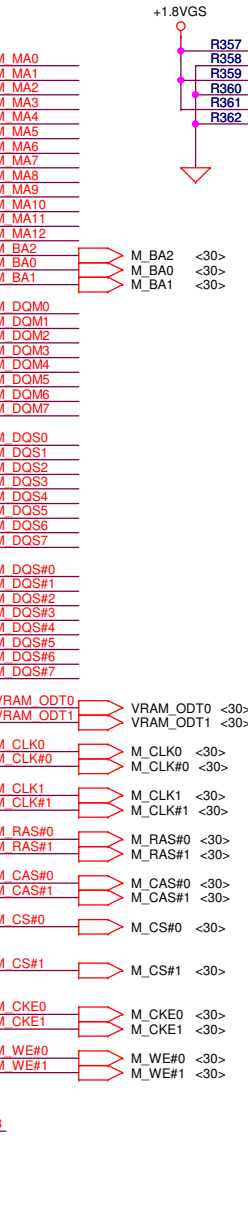
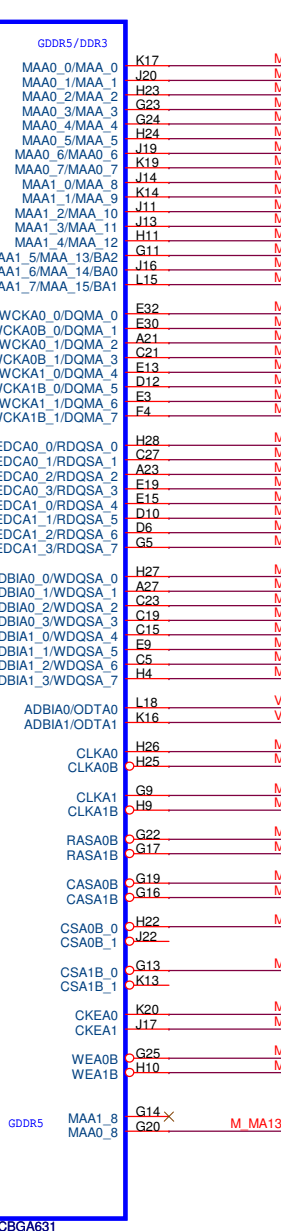


| | | |
|--|--------------------|----------------------------|
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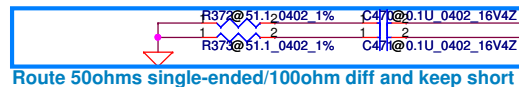
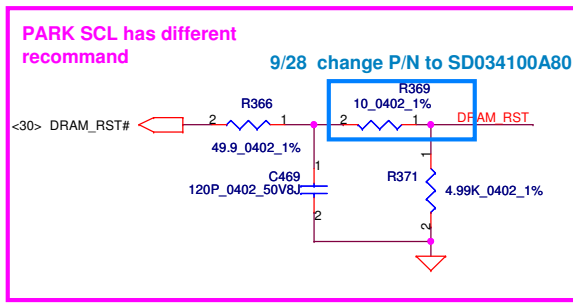
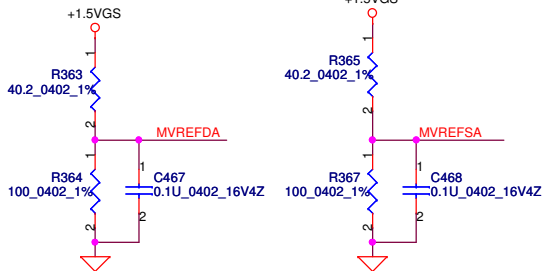
| | | |
|---------------------------------|-----------------|---------|
| Compal Electronics, Inc. | | |
| RobsonXT-S3 PWR/GND | | |
| Size C | Document Number | Rev 0.2 |
| Date: Friday, November 26, 2010 | Sheet 28 | of 59 |



MEMORY INTERFACE



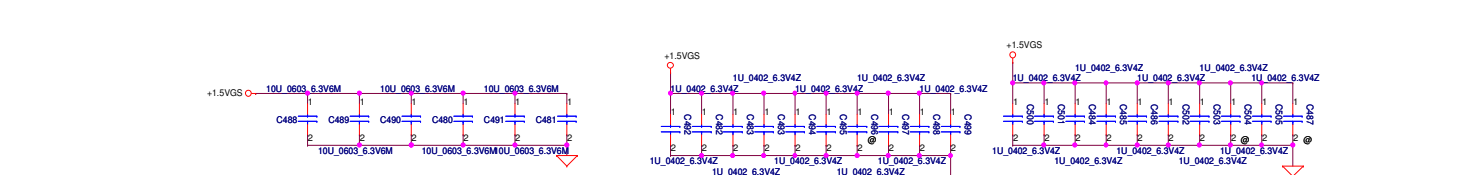
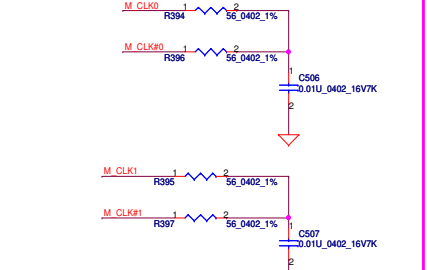
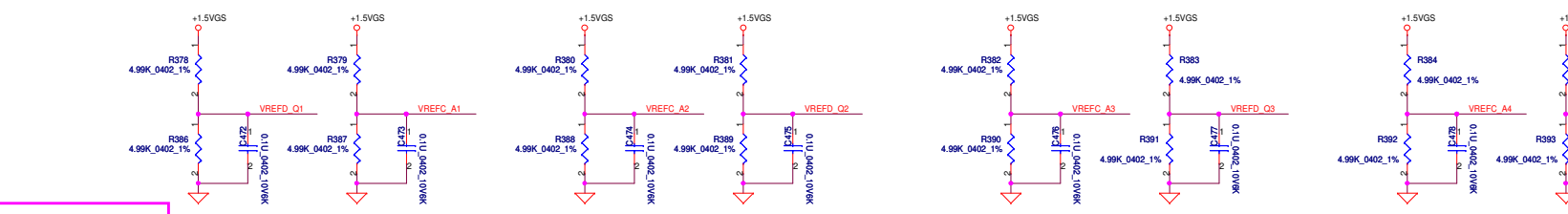
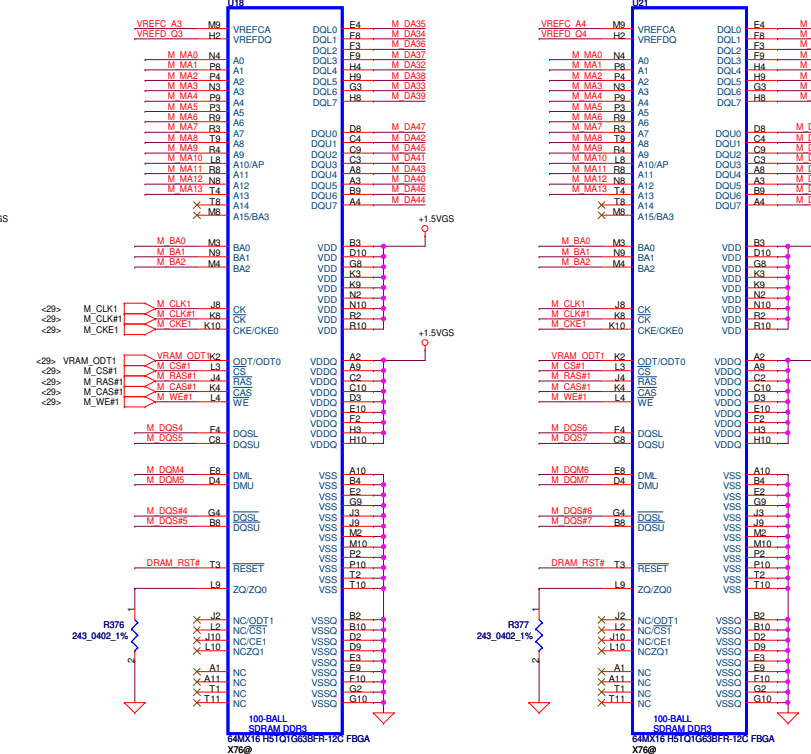
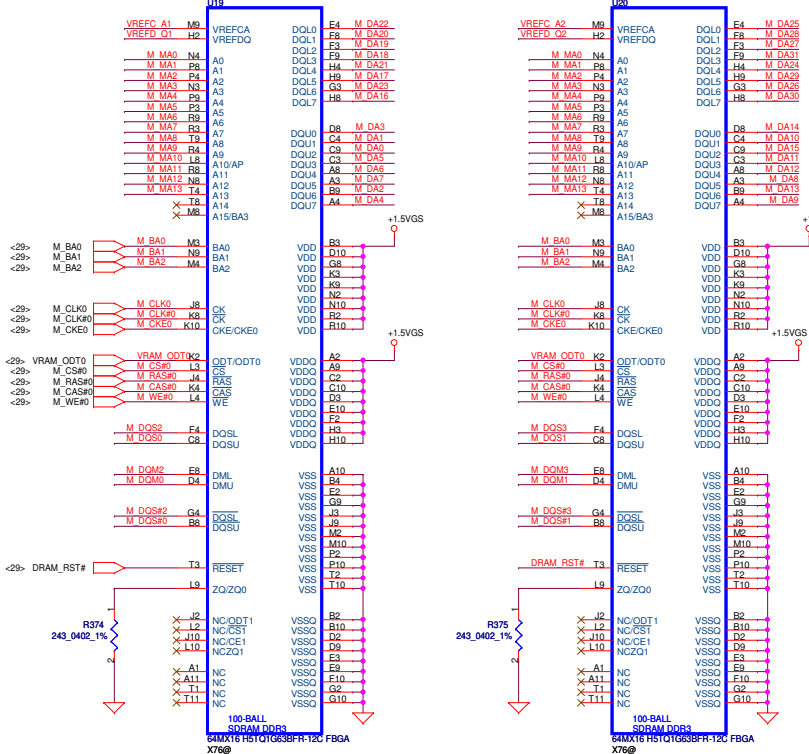
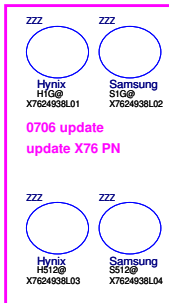
| Vendor | VRAM_ID0 | VRAM_ID1 | VRAM_ID2 |
|---------------------------------|----------|----------|----------|
| Hynix 512MB PN:SA000032460 | R357 | R360 | R362 |
| Samsung 512MB PN:SA000035700 | R358 | R359 | R362 |
| Hynix 1GB PN:SA00003VS20 | R357 | R360 | R361 |
| Samsung 1GB PN:SA00003MQ20 | R358 | R359 | R361 |



Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation,if not need, DNI.

| | | | | | |
|---|---------------------------|-----------------|------------|---------------------------|-----|
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| Date: | Friday, November 26, 2010 | Sheet | 29 | of | 59 |

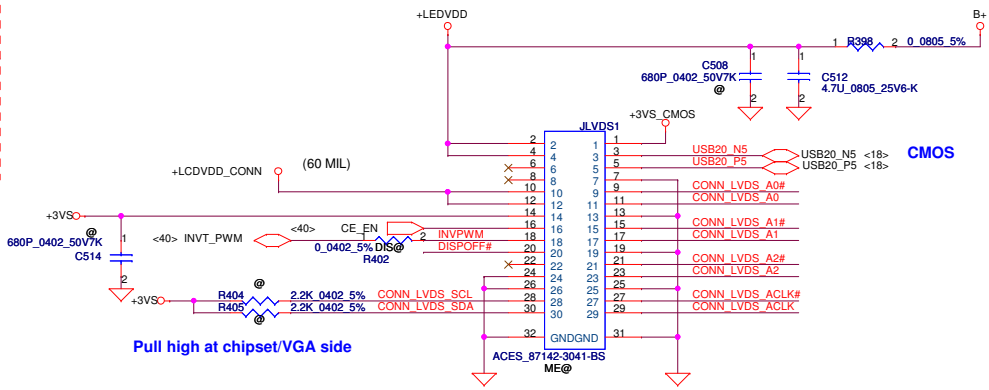
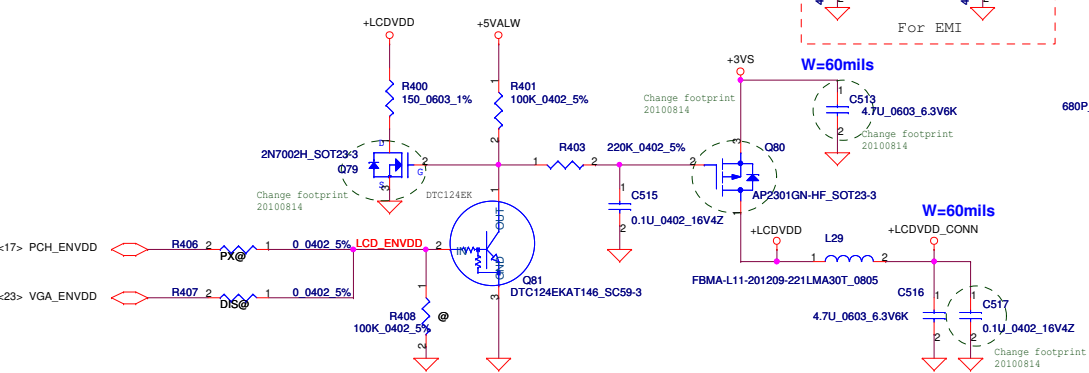
- <29> M_DA[63..0] M_DA63_0
- <29> M_MA[13..0] M_MA13_0
- <29> M_DQM[7..0] M_DQM7_0
- <29> M_DQS[7..0] M_DQS7_0
- <29> M_DQS#[7..0] M_DQS#7_0



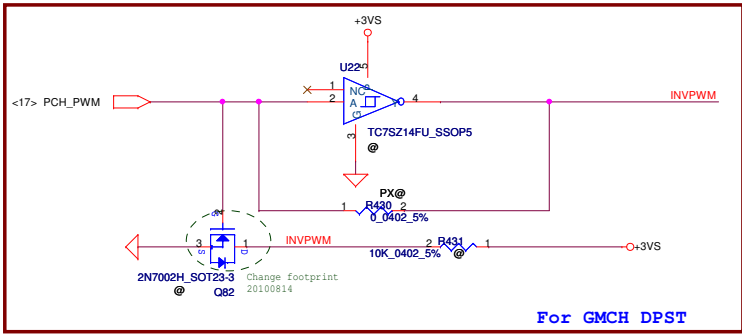
ref 139-02 recommend
add off page
Park SCL recommend pu 60.4 ohm to
06V9 update

VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646-HC11 FBGA C38!)
update VRAM PN 0619 update

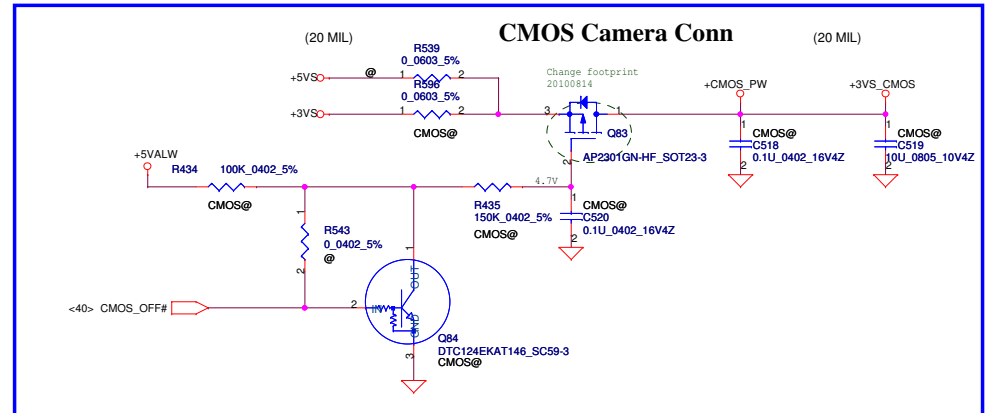
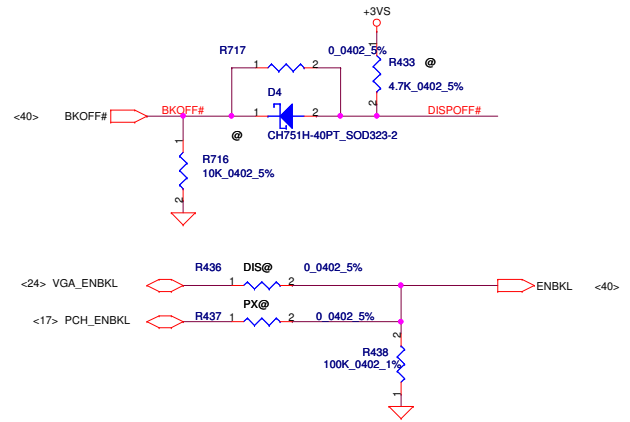
LCD POWER CIRCUIT



- <17> PCH_ENVDD
- <23> VGA_ENVDD
- <24> VGA_LVDS_SCL
- <24> VGA_LVDS_SDA
- <23> VGA_LVDS_A0
- <23> VGA_LVDS_A0#
- <23> VGA_LVDS_A1
- <23> VGA_LVDS_A1#
- <23> VGA_LVDS_A2
- <23> VGA_LVDS_A2#
- <23> VGA_LVDS_ACLK
- <23> VGA_LVDS_ACLK#
- <17> EDID_CLK
- <17> EDID_DATA
- <17> LVDS_A0
- <17> LVDS_A0#
- <17> LVDS_A1
- <17> LVDS_A1#
- <17> LVDS_A2
- <17> LVDS_A2#
- <17> LVDS_ACLK
- <17> LVDS_ACLK#

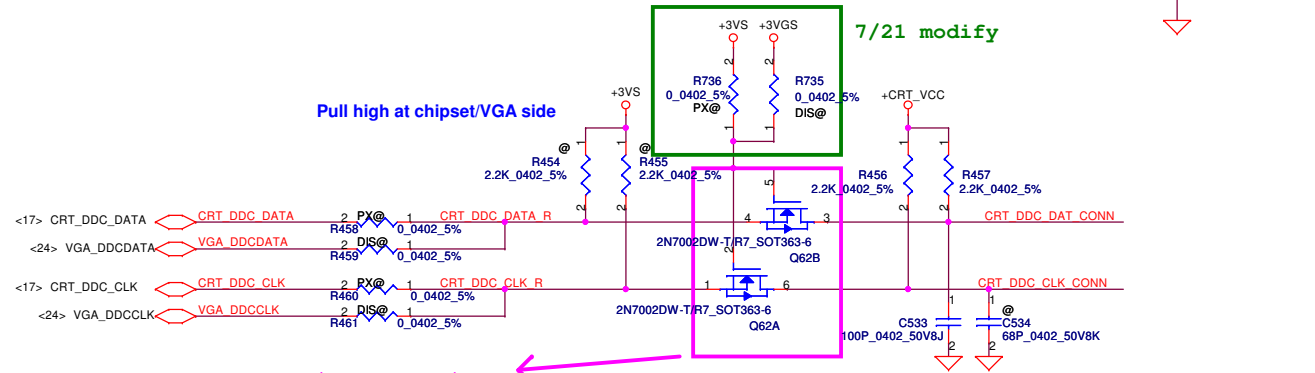
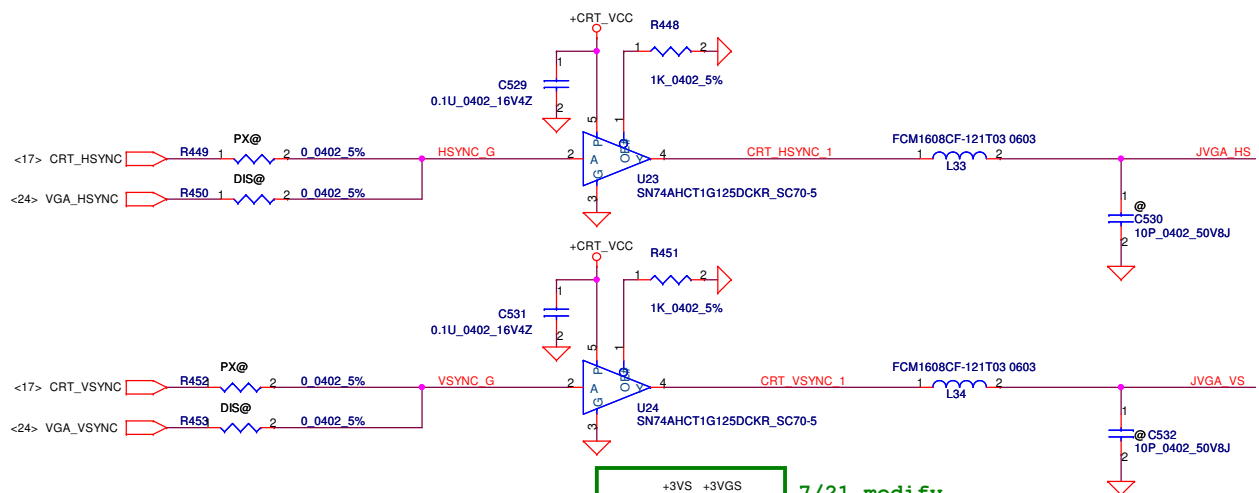
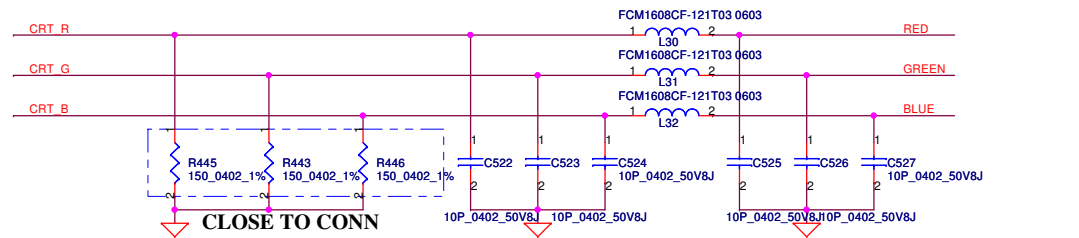
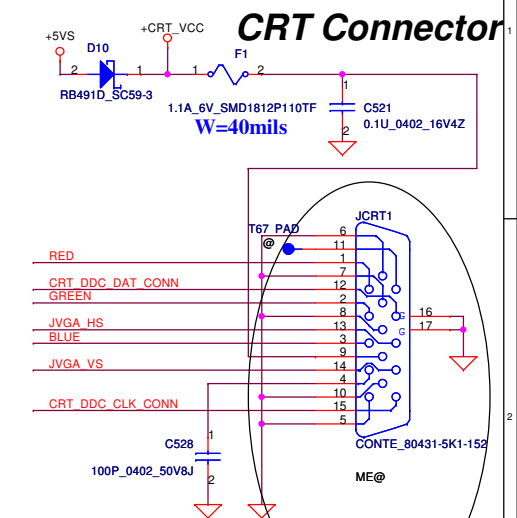
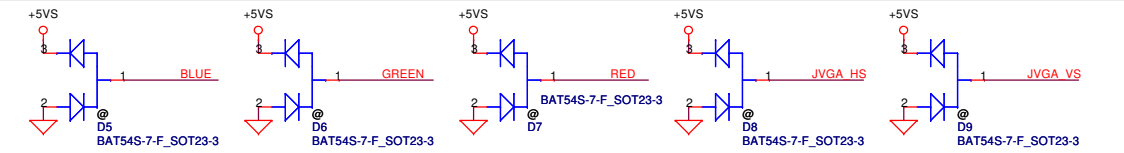
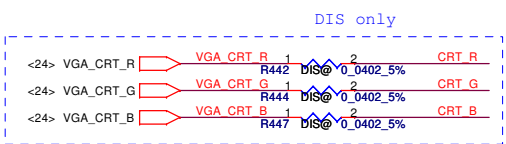
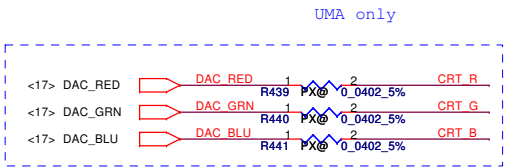


For GMCH DPST



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|-------------------------|-----------------|---------------------------|------------|--------------------------|----------------|
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| | | | | LVDS/CAMERA | |
| Size | Document Number | Date | | Rev | |
| B | LA-6751P | Friday, November 26, 2010 | | 0.2 | |
| | | | | 1 | Sheet 31 of 59 |

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8/14 change P/N to DMN66D0LDW-7_SOT363-6 (SB00000DH00)

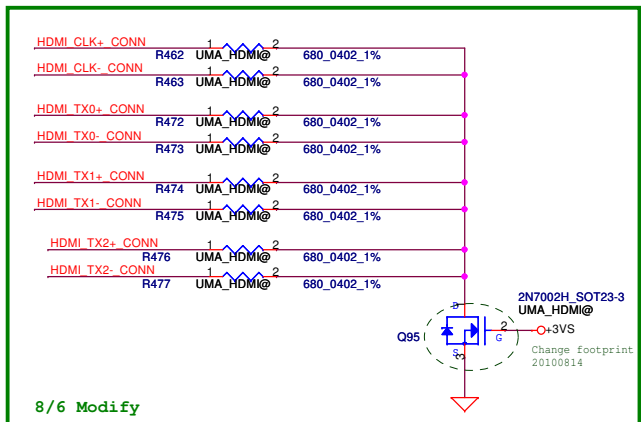
| | | | |
|---|------------|--------------------|------------|
| Security Classification | | Compal Secret Data | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 |
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Check CRT footprint 7/20_OTIS

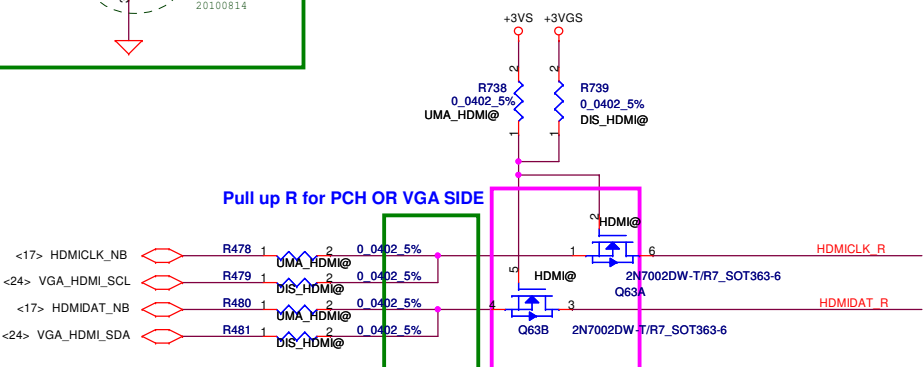
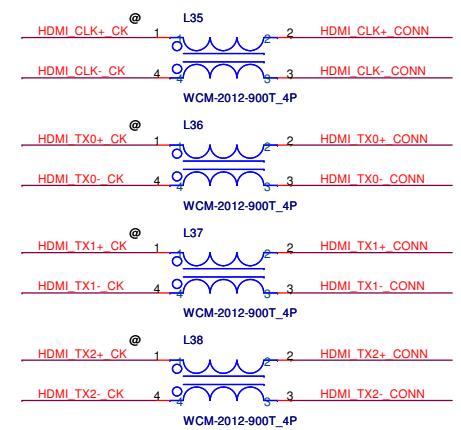
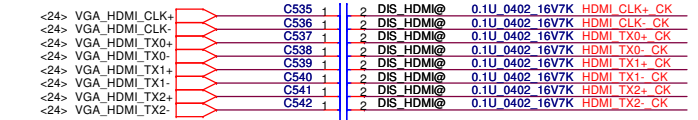
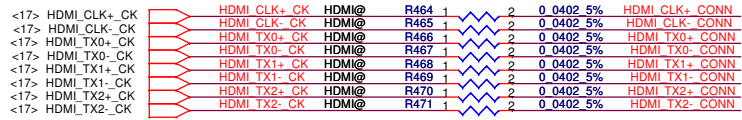
Compal Electronics, Inc.

CRT Connector

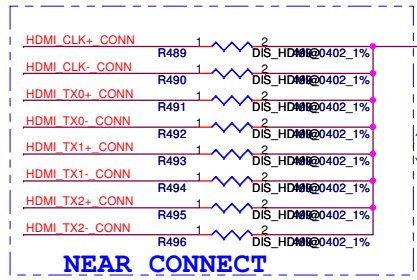
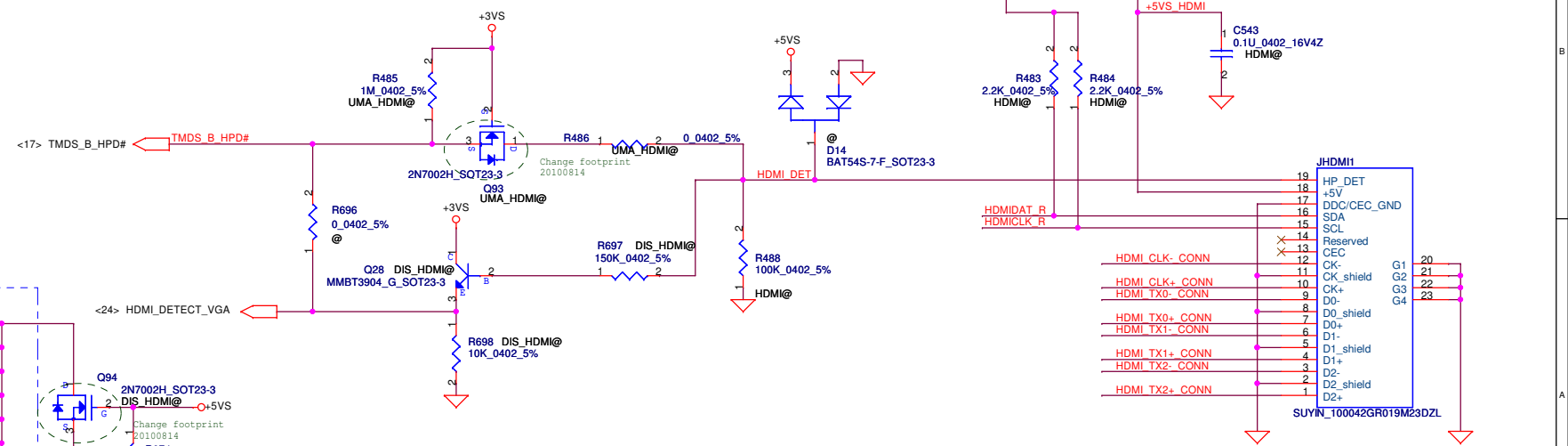
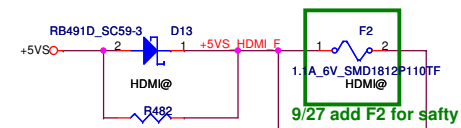
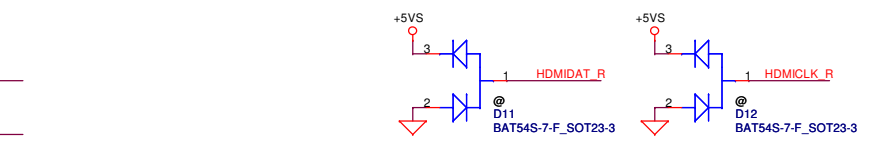
| | | |
|--------|---------------------------|----------------|
| Size | Document Number | Rev |
| Custom | LA-6751P | 0.2 |
| Date: | Friday, November 26, 2010 | Sheet 32 of 59 |



8/6 Modify

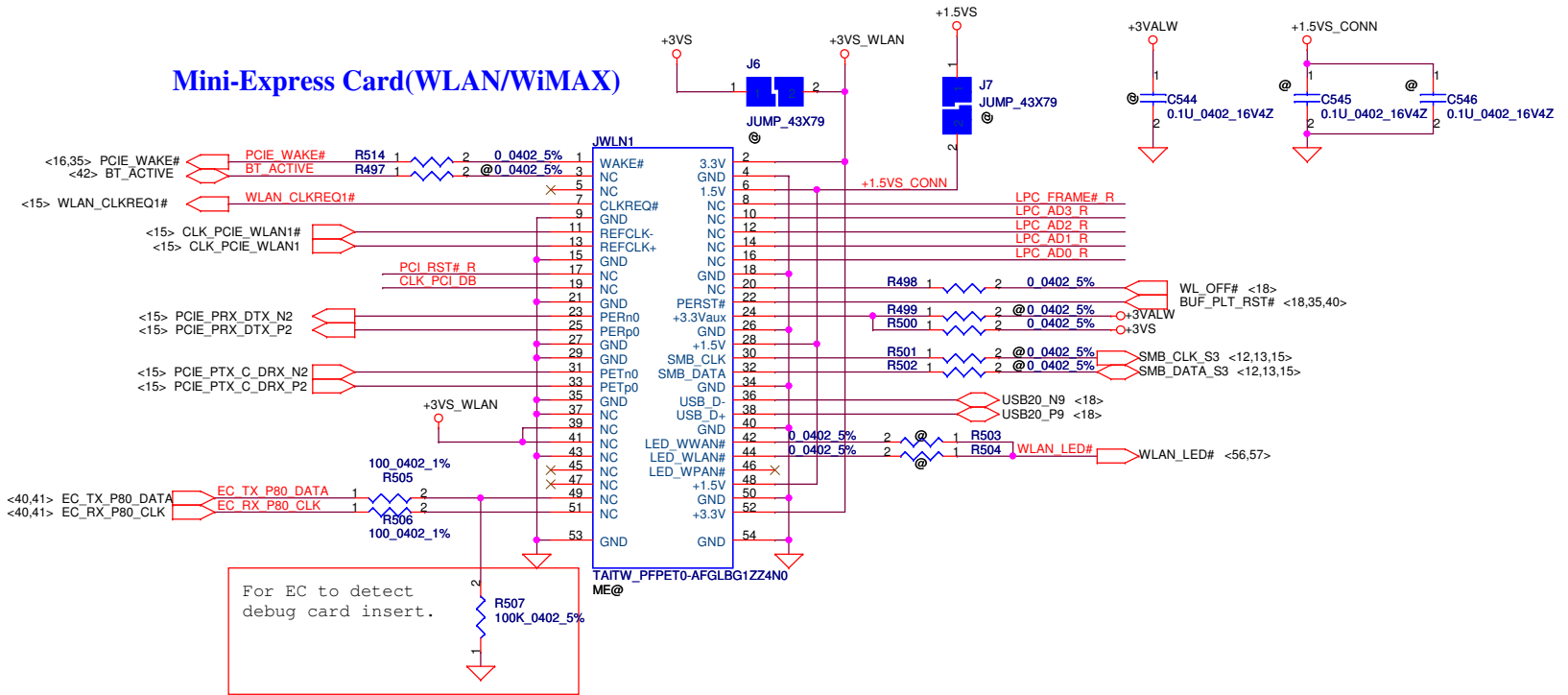


8/14 change P/N to DMN66D0LDW-7_SOT363-6 (SB00000DH00)



| | | | | | |
|---|-----------------|---------------------------------|------------|--------------------------|-----------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Ltd. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title | HDMI CONN |
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| Size Custom | Document Number | Date: Friday, November 26, 2010 | | Sheet | 33 of 59 |
| | | | | Rev | 0.2 |
| | | | | LA-6751P | |

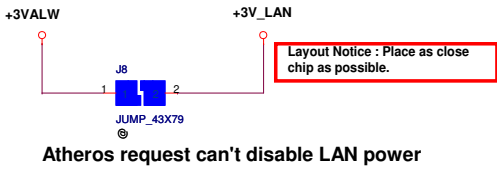
Mini-Express Card for WLAN/WiMAX(Half)



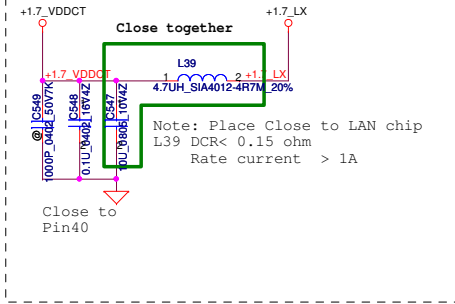
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

| | | | | | | | |
|--------------|------|---|---|---|-----------|------------|--------------------|
| LPC_FRAME# R | R508 | 1 | @ | 2 | 0.0402 5% | LPC_FRAME# | LPC_FRAME# <14,40> |
| LPC_AD3 R | R509 | 1 | @ | 2 | 0.0402 5% | LPC_AD3 | LPC_AD3 <14,40> |
| LPC_AD2 R | R510 | 1 | @ | 2 | 0.0402 5% | LPC_AD2 | LPC_AD2 <14,40> |
| LPC_AD1 R | R511 | 1 | @ | 2 | 0.0402 5% | LPC_AD1 | LPC_AD1 <14,40> |
| LPC_AD0 R | R512 | 1 | @ | 2 | 0.0402 5% | LPC_AD0 | LPC_AD0 <14,40> |
| PCI_RST# R | R513 | 1 | @ | 2 | 0.0402 5% | PCI_RST# | BUF_PLT_RST# |
| CLK_PCI_DB | | | | | | CLK_PCI_DB | <15> |

| | | | | | |
|---|--------------------|-----------------|------------|--|---------------------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. Mini-Card/NEW Card/SIM | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | | |
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| | | | | Size | Document Number |
| | | | | Date: | Friday, November 26, 2010 |
| | | | | Sheet | 34 of 59 |
| | | | | Rev | 0.2 |



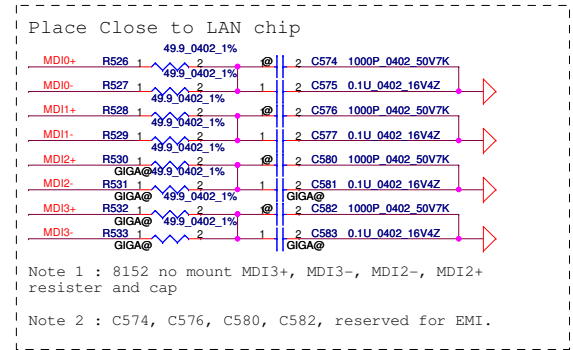
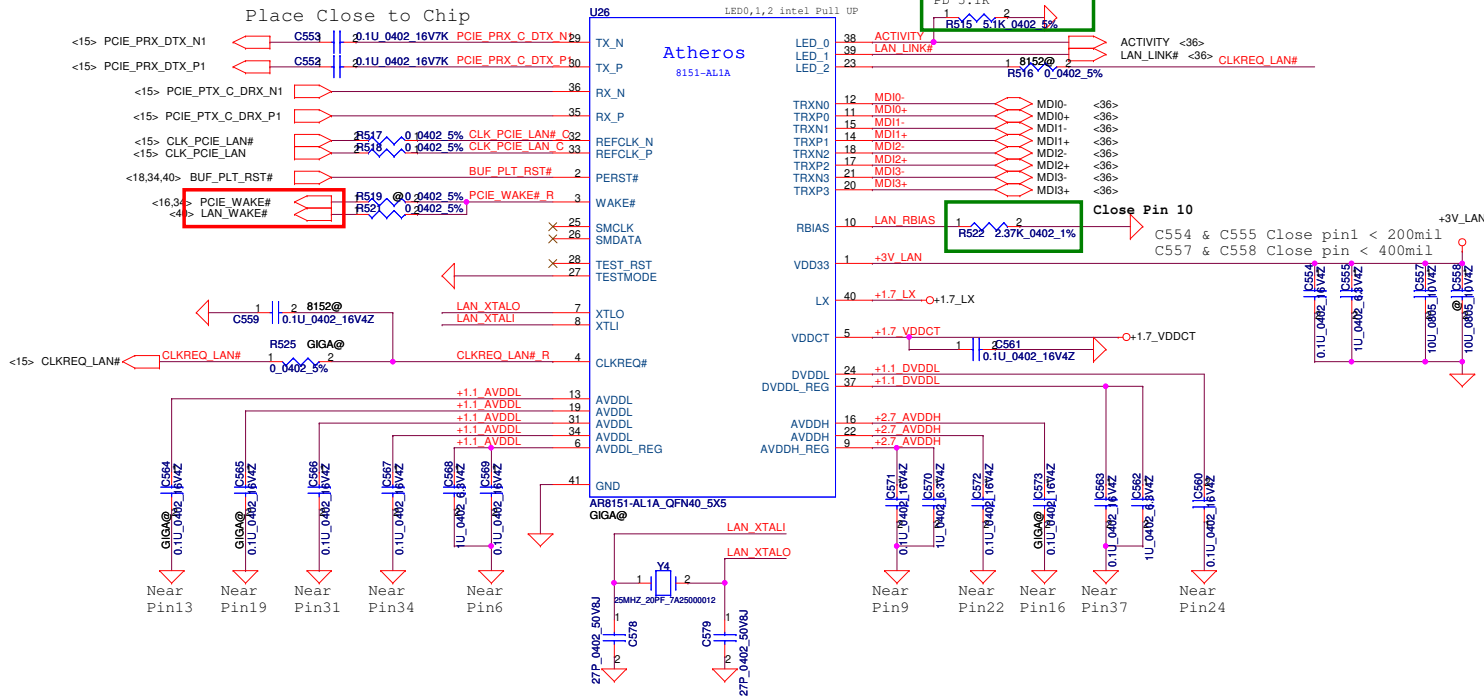
Atheros request can't disable LAN power



Power On strapping

| Pin | Description | Chip Default |
|------|---|--------------|
| LED0 | H:Over Clock Enable L:Over Clock Disable * | H |
| LED2 | H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ | -- |

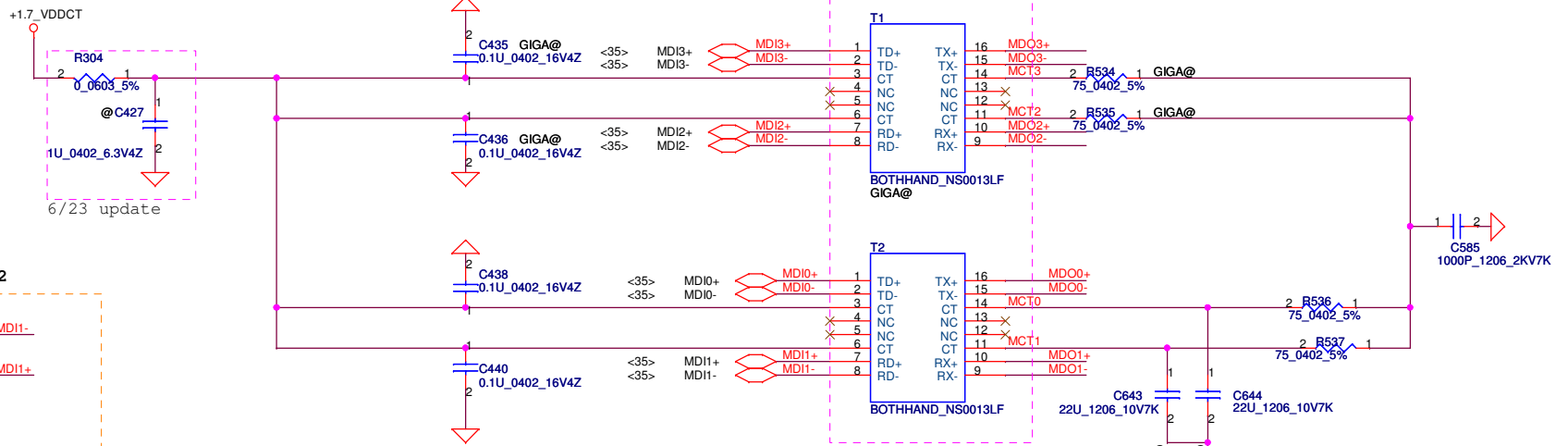
U26 8152@
S IC AR8152-AL1E QFN 40P E-LAN CTRL



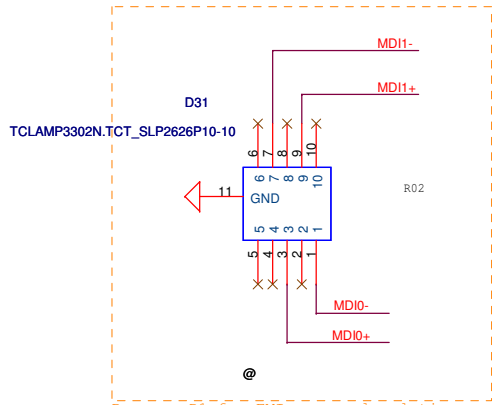
| | Pin4 | Configure | | Pin23 | Configure |
|--------|-----------|-----------|------|---------|-----------|
| | | R525 | C559 | | |
| AR8152 | VDDCT_REG | | * | CLKREQn | * |
| AR8151 | CLKREQn | * | | LED [2] | |

| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
|---|---------------------------|-----------------|--------------------------|-----------------|
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title |
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| Size Custom | Document Number | Rev | | |
| | LA-6751P | 0.1 | | |
| Date: | Friday, November 26, 2010 | Sheet | 35 | of 59 |

8/23 Change T1,T2 P/N to SP050006E00

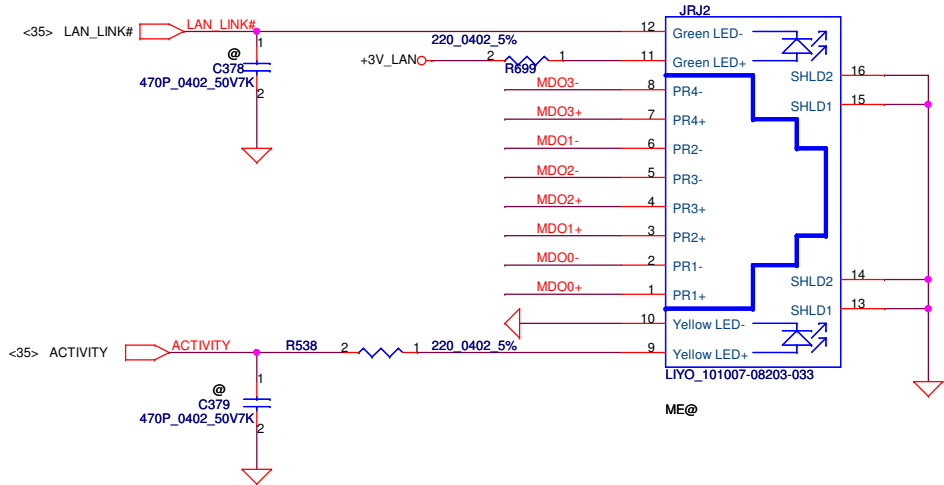


Place Close to T2

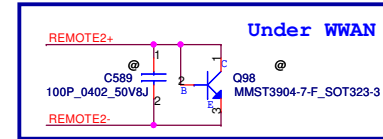
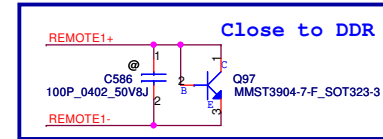
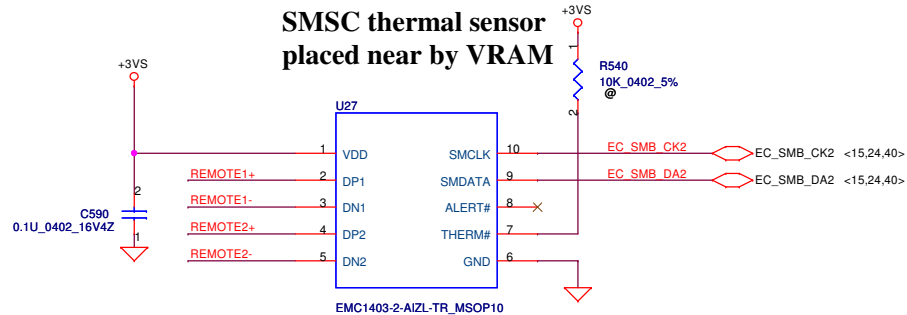
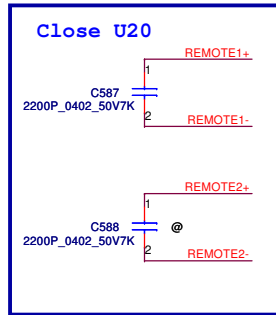


Reserve D1 for EMI go rural solution 20101006

Reserve gas tube for EMI go rural solution 20101006

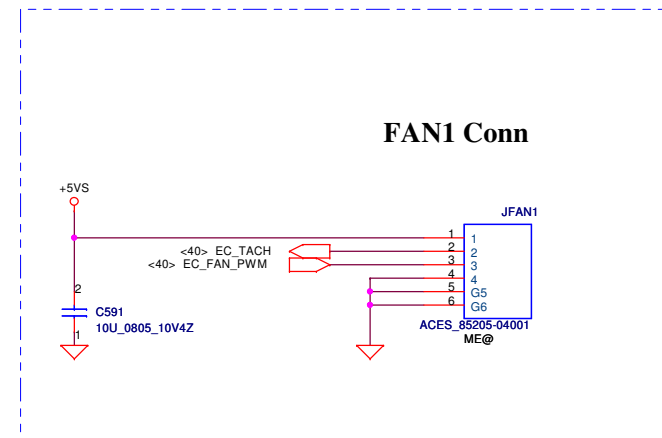


| | | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|---------------------------|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title LAN_Transformer | | |
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| | | | | B | LA-6751P | 0.2 |
| | | | | Date: | Friday, November 26, 2010 | Sheet 36 of 59 |



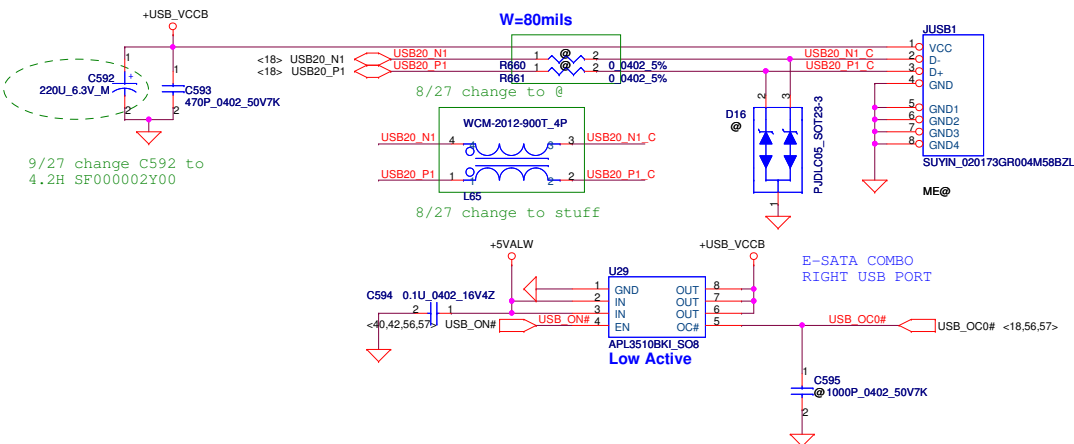
REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

Address 1001_101xb
10/5 change P/N to SA000046C00

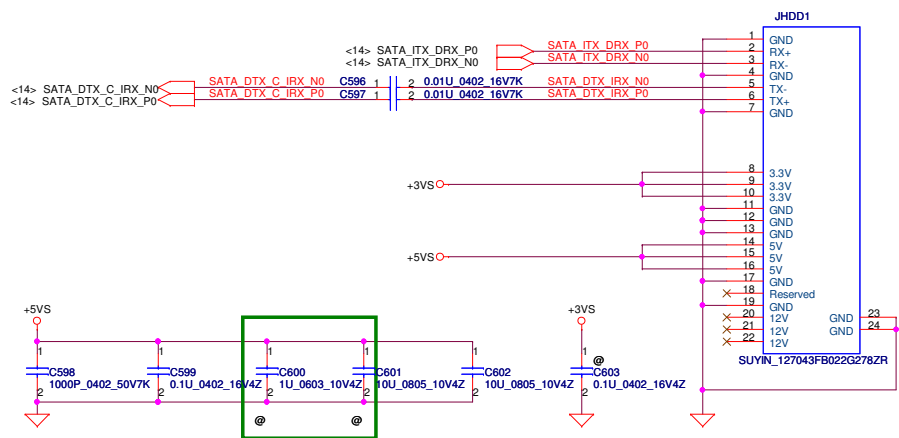


| | | | | | |
|---|------------|--------------------|------------|---------------------------------|------------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Ltd. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title | EMC1403 Thermal sensor/FAN |
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| | | | | Date: Friday, November 26, 2010 | Rev 0.2 Sheet 37 of 59 |

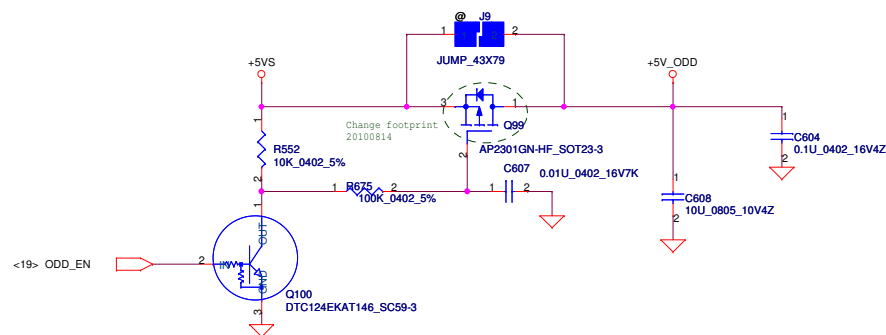
Left USB Conn.



SATA HDD Conn.



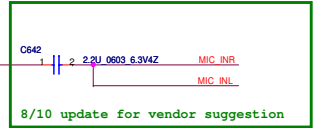
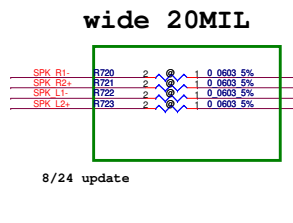
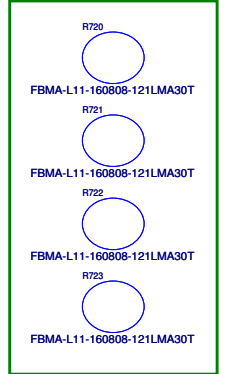
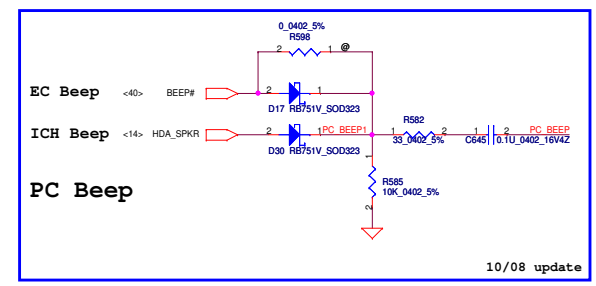
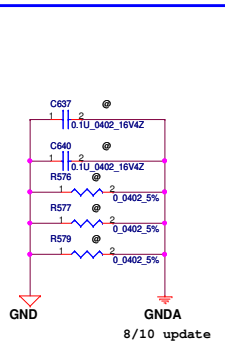
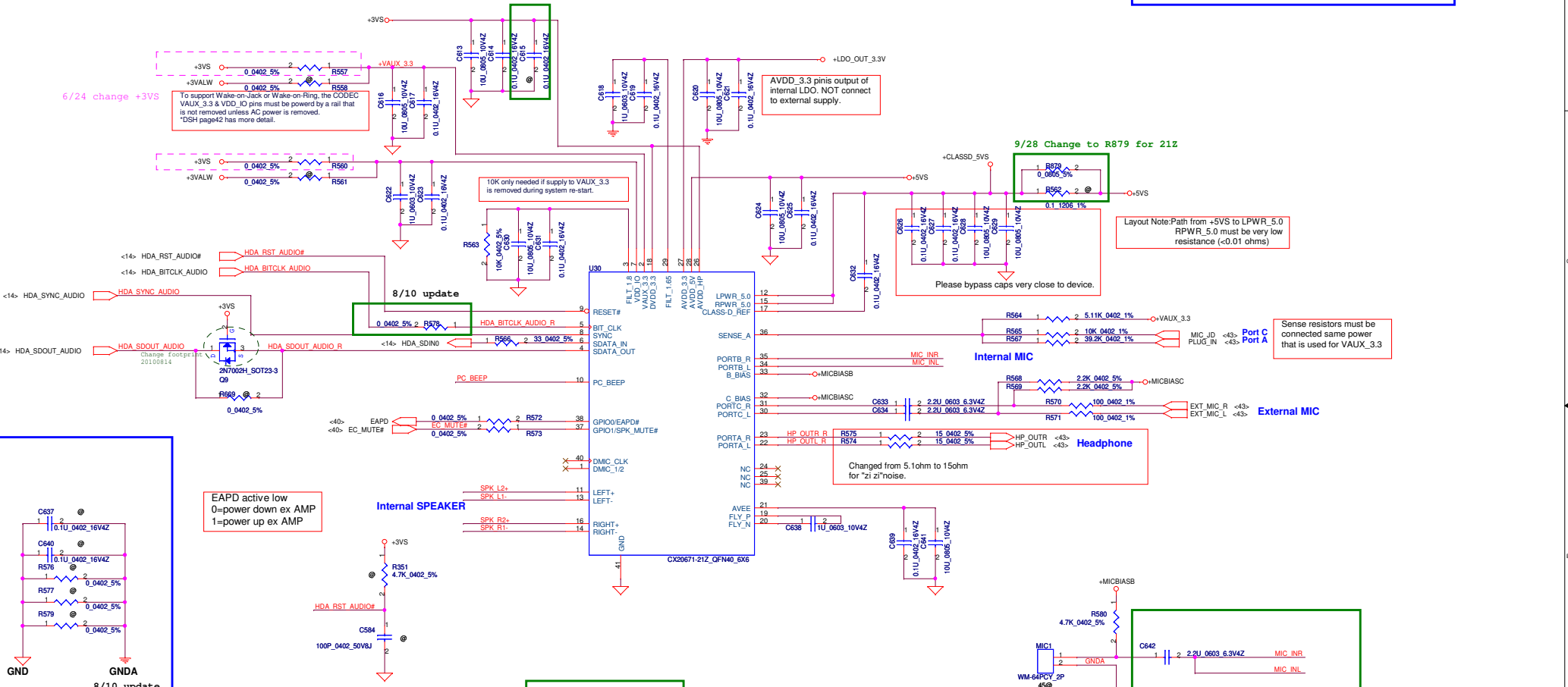
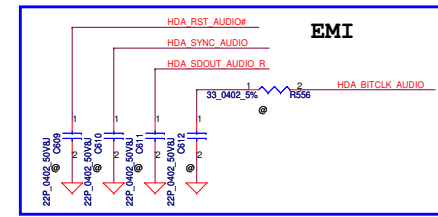
ODD Power Control



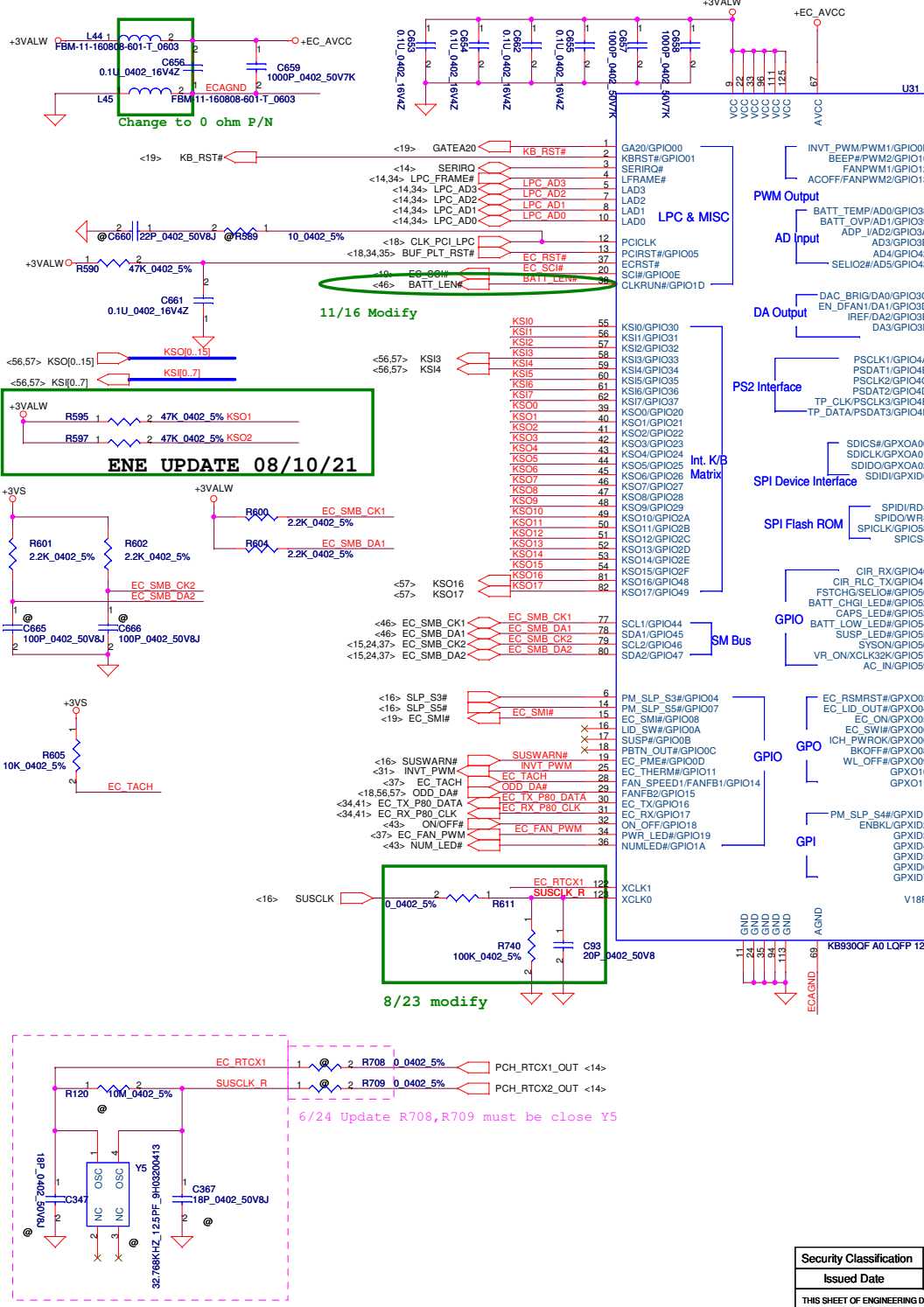
| | | | | |
|---|---------------------------|-----------------|------------|--------------------------|
| Security Classification | Compal Secret Data | | Title | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Compal Electronics, Inc. |
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| Size B | Document Number | Rev | LA-6751P | |
| Date: | Friday, November 26, 2010 | Sheet | 38 | of 59 |

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).

9/27 Update U30 P/N to SA00003K410

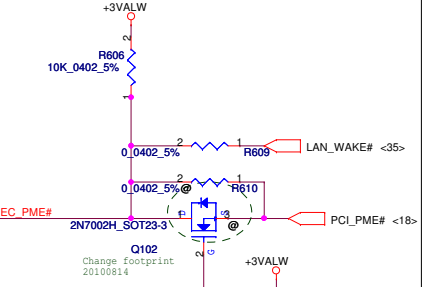
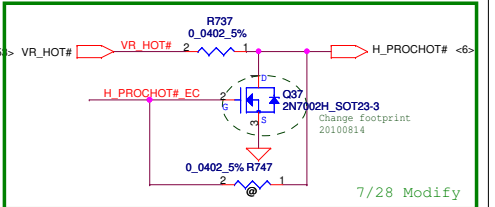
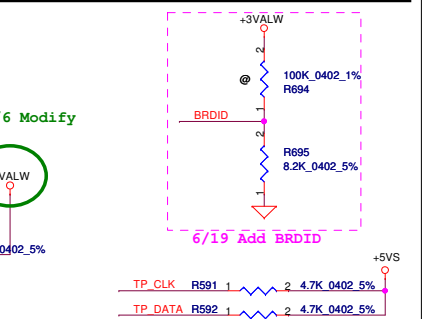


| | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|-----------------|
| Security Classification | Compal Secret Data | | Title | | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | CX20671 Codec | |
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| | | | | LA-6751P | |
| | | | | Rev 0.1 | |
| | | | | Date: Friday, November 26, 2010 | |
| | | | | Sheet 39 of 59 | |



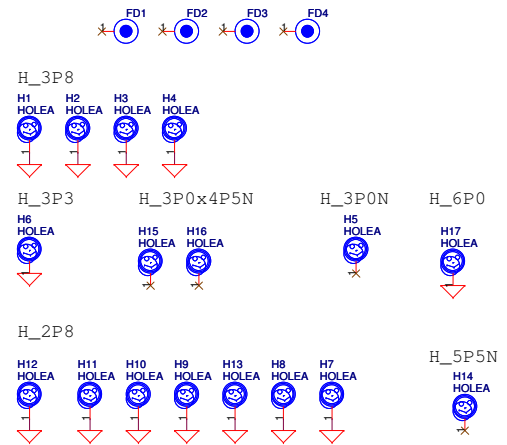
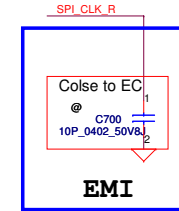
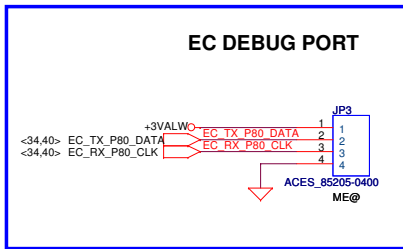
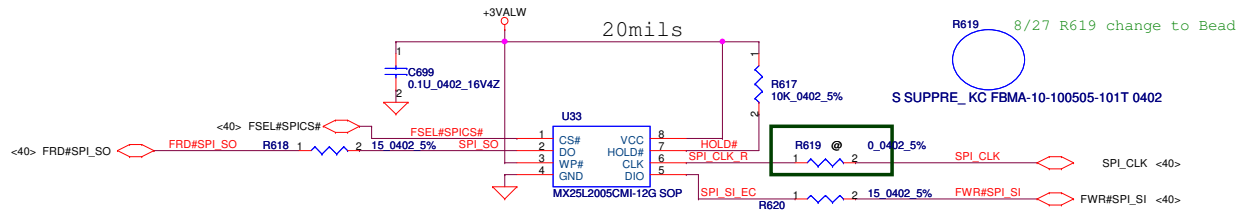
| | |
|------|-------------|
| Vcc | 3.3V +/- 5% |
| R694 | 100K +/- 5% |

| Board ID | R695 | V _{AD_BID} min | V _{AD_BID} typ | V _{AD_BID} max | MP |
|----------|-------------|-------------------------|-------------------------|-------------------------|-----|
| 0 | 0 | 0 V | 0 V | 0 V | MP |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | PVT |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | DVT |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | EVT |



| | | | | |
|---|--------------------|-----------------|---------------------------|--------------------|
| Security Classification | Compal Secret Data | | Title | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | BIOS & EC I/O Port |
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| Size | Document Number | Rev | Date | |
| Custmr | LA-6751P | 0.2 | Friday, November 26, 2010 | |
| Date | Sheet | 40 | of 59 | |

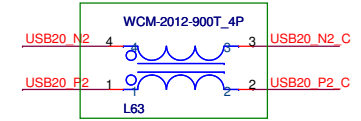
**FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00**



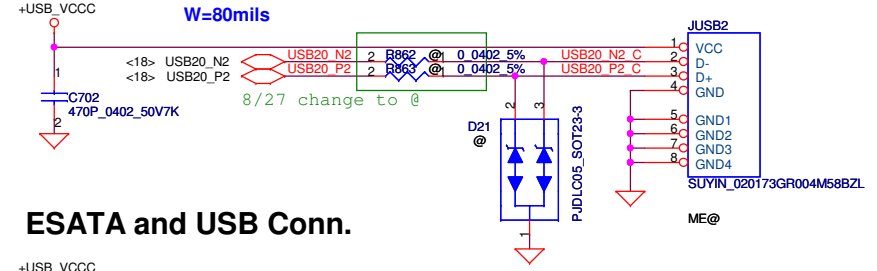
| | | | | |
|---|------------------------------------|-----------------------------------|---|------------------------------|
| Security Classification | Compal Secret Data | | Title Compal Electronics, Inc. LED/EC SPI ROM | |
| Issued Date | 2010/07/12 | Deciphered Date | | |
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| Size B | Document Number LA-6751P | Date Friday, November 26, 2010 | | Rev 0.2 Sheet 41 of 59 |

(220uF_6.3V_5.9L_ESR17m) *2= (SF000001500)

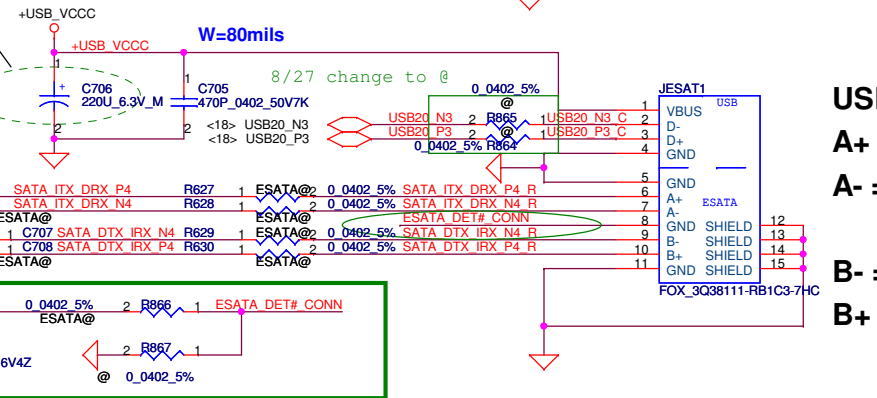
8/27 change to stuff



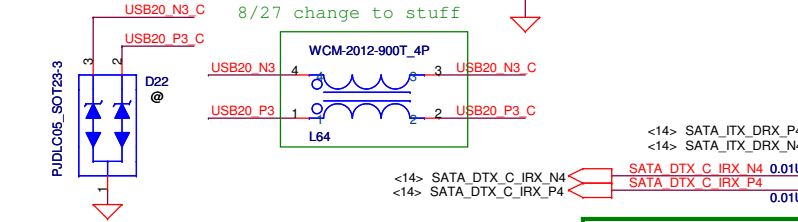
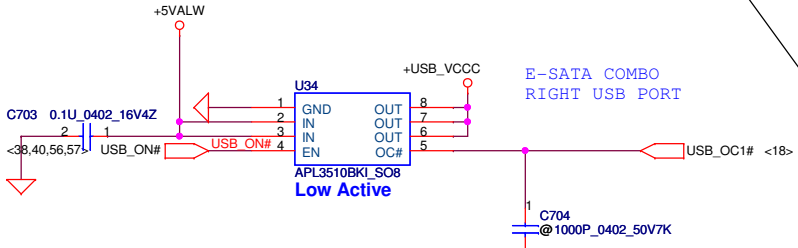
Left USB Conn.



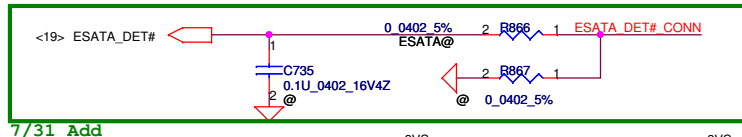
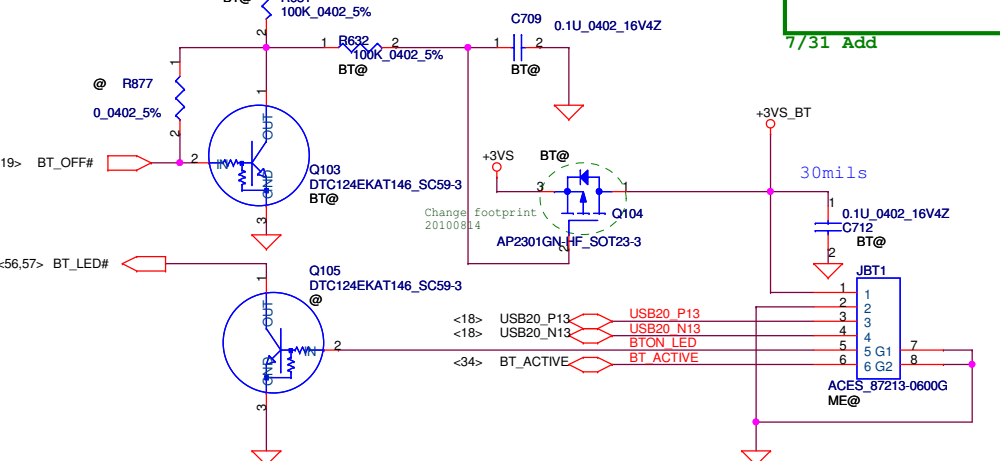
ESATA and USB Conn.



USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

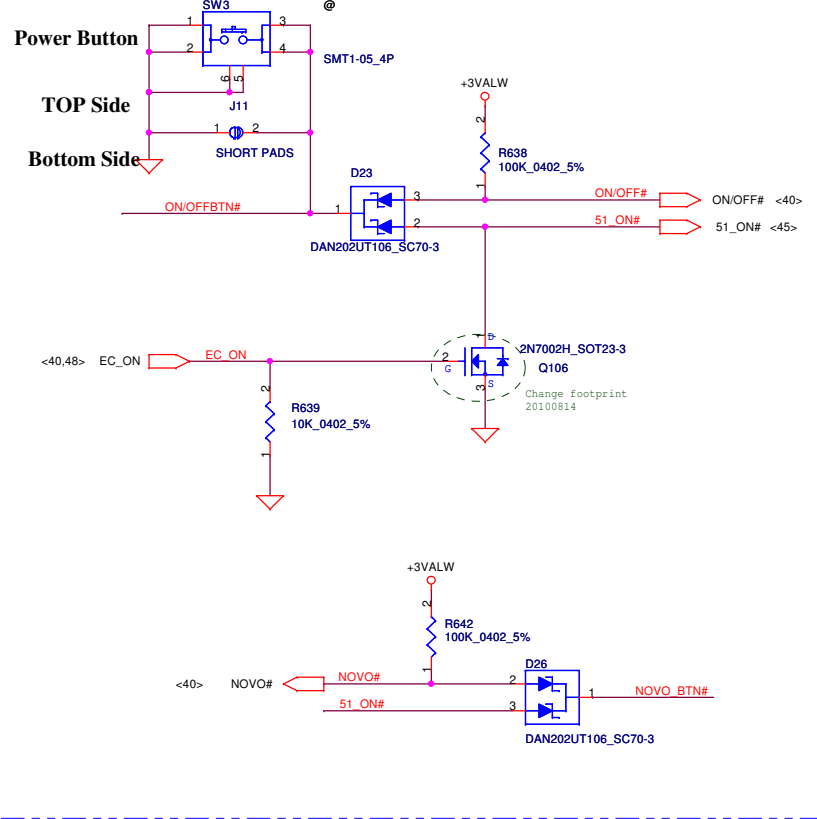


BT MODULE CONN

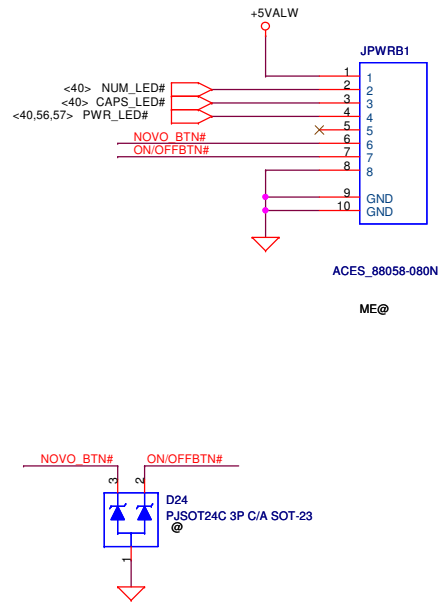


| | | | | | |
|---|-----------------|--------------------|------------|---------------------------|----------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title | |
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| Size | Document Number | Rev | | Date | |
| Custom | LA-6751P | 0.2 | | Friday, November 26, 2010 | |
| | | | | Sheet | 42 of 59 |

ON/OFF switch

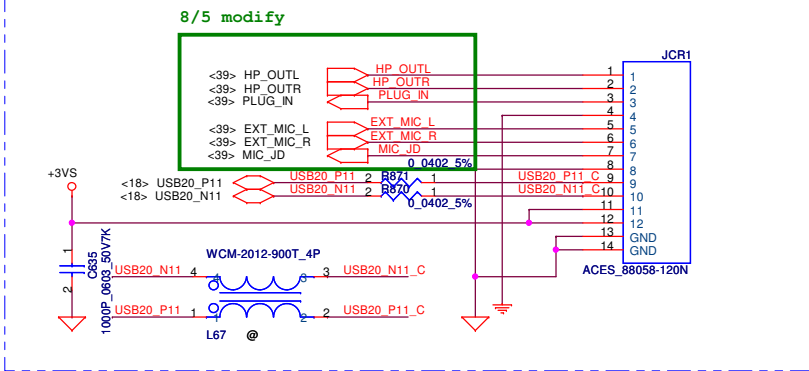


Power Bottom Board Conn. 8pin

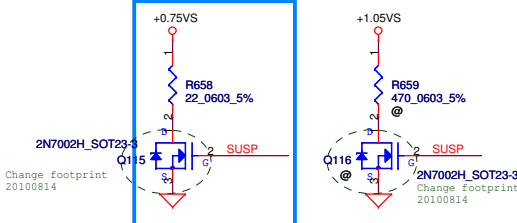
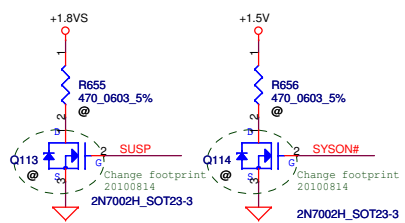
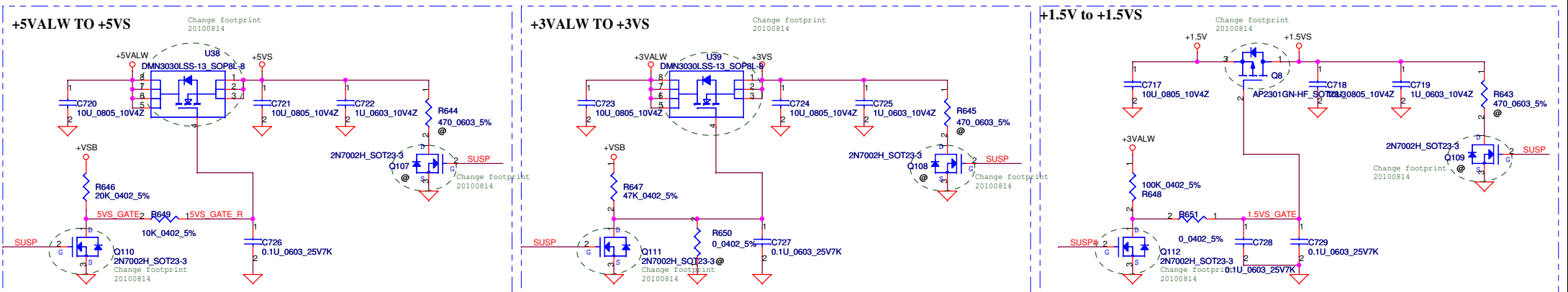


EMI REQUEST 1ST = SCA00000E00
 2ST = SCA00000R00

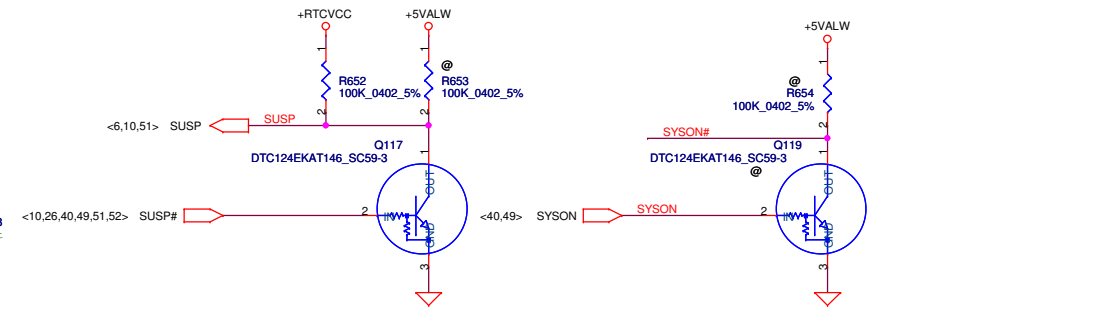
Card Reader/Audio Jack SB CONN



| | | | | |
|---|--------------------|-----------------|--------------------------|--------------------|
| Security Classification | Compal Secret Data | | Compal Electronics, Ltd. | |
| Issued Date | 2010/07/12 | Deciphered Date | 2012/07/11 | Title |
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| | | | | Size Custom |
| Date: Friday, November 26, 2010 | | | Sheet 43 of 59 | LA-6751P 0.2 |

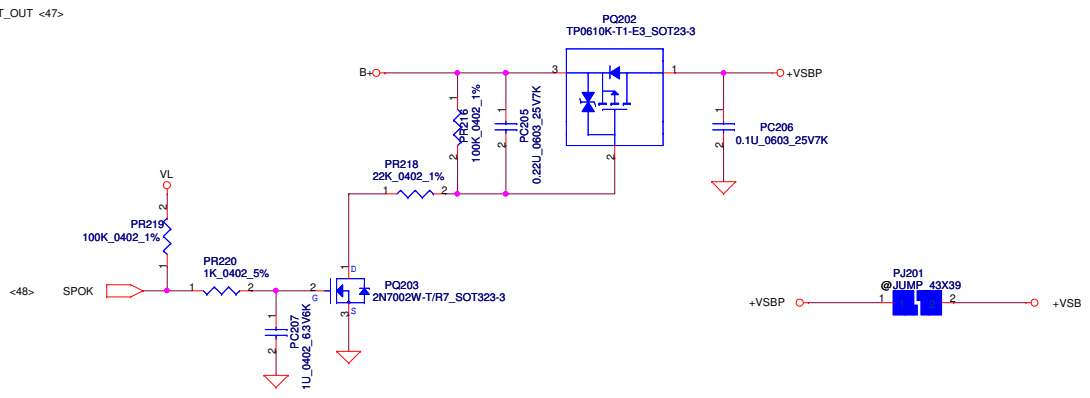
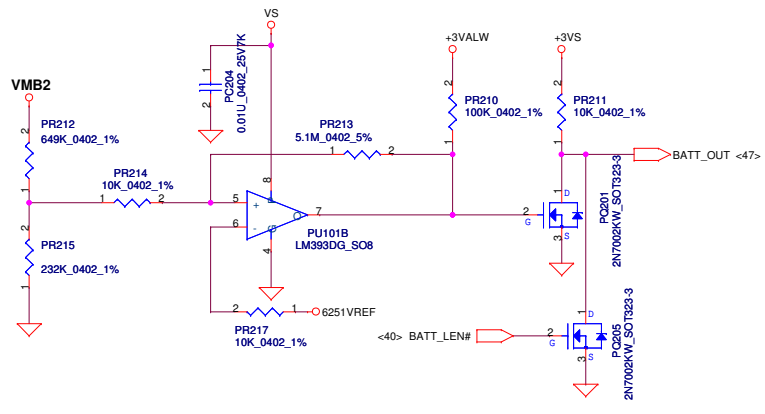
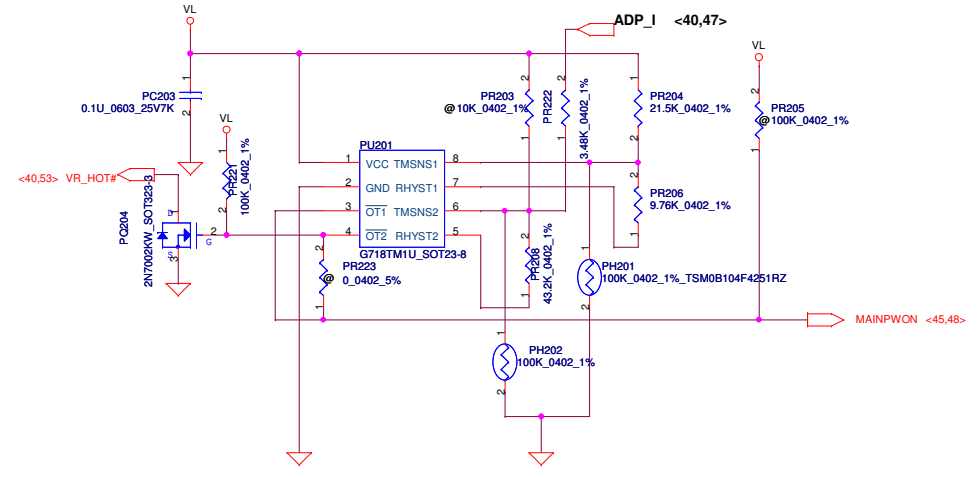
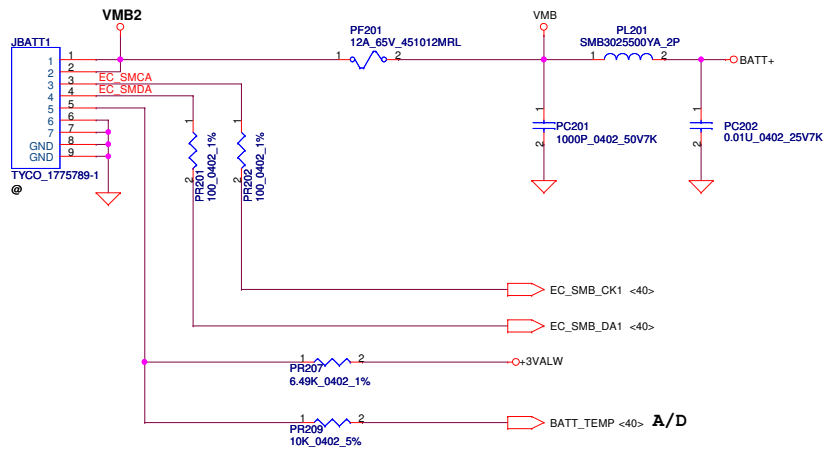


For Intel S3 Power Reduction.



| | | | | | |
|---|-----------------|--------------------|------------|--------------------------|---------------------------|
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| Size | Document Number | Rev | | LA-6751P | |
| Custom | LA-6751P | 0.2 | | Date: | Friday, November 26, 2010 |
| | | | | Sheet | 44 of 59 |

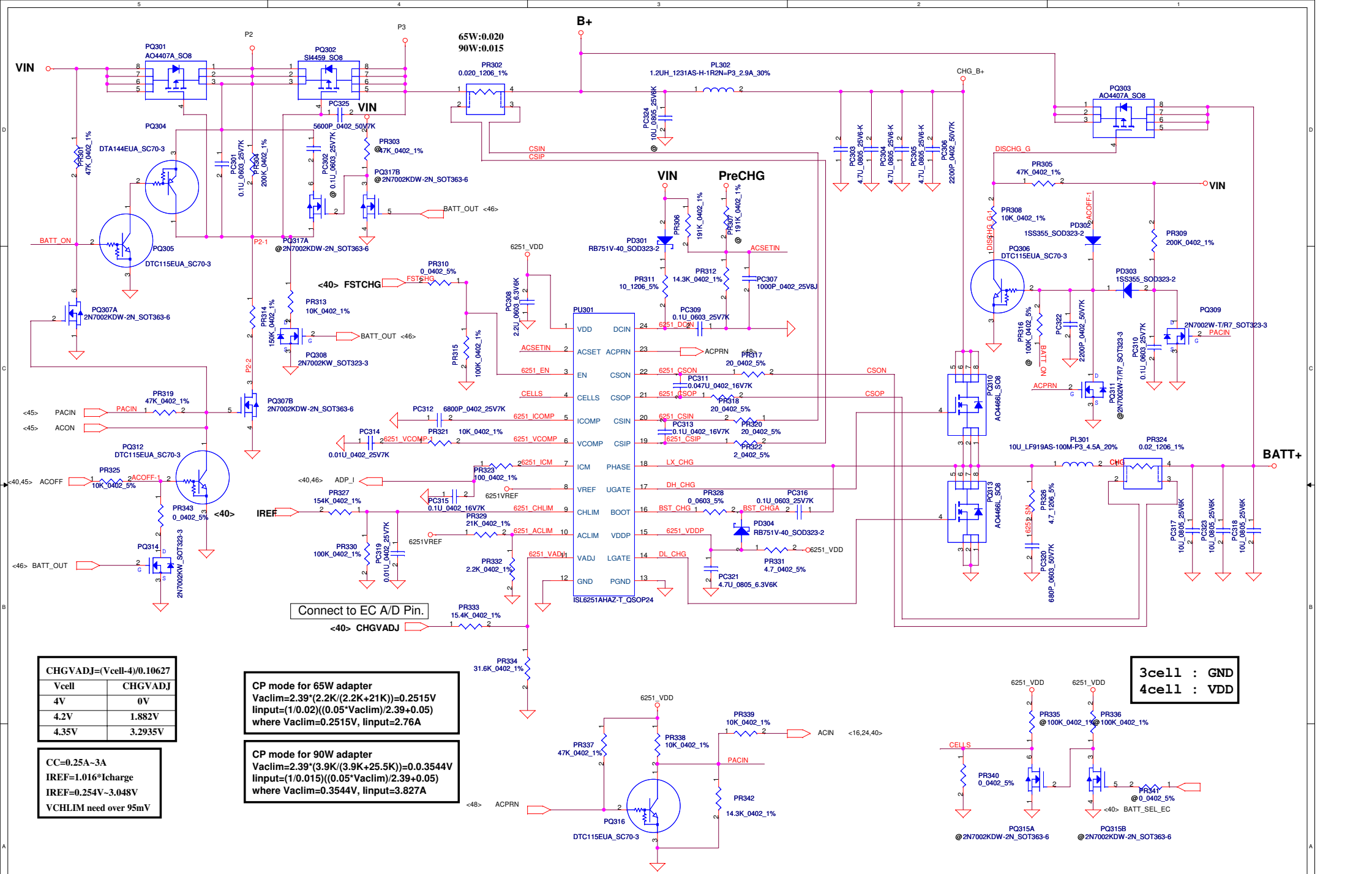
PH201 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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|-------------------------|--------------------|-----------------|
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| | | 2010/12/31 |

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| | | |
|--|-----------------------------|----------------|
| Compal Electronics, Inc. PWR-BATTERY CONN/OTP | | |
| Title | | |
| Size | Document Number | Rev |
| Custom | PIWG1/G2(LA-6751P/LA-6753P) | 0.1 |
| Date: | Friday, November 26, 2010 | Sheet 46 of 54 |



| | |
|--------------------------------------|---------|
| $CHGVADJ = (V_{cell} - 4) / 0.10627$ | |
| V _{cell} | CHGVADJ |
| 4V | 0V |
| 4.2V | 1.882V |
| 4.35V | 3.2935V |

CC=0.25A-3A
 IREF=1.016*I_{charge}
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

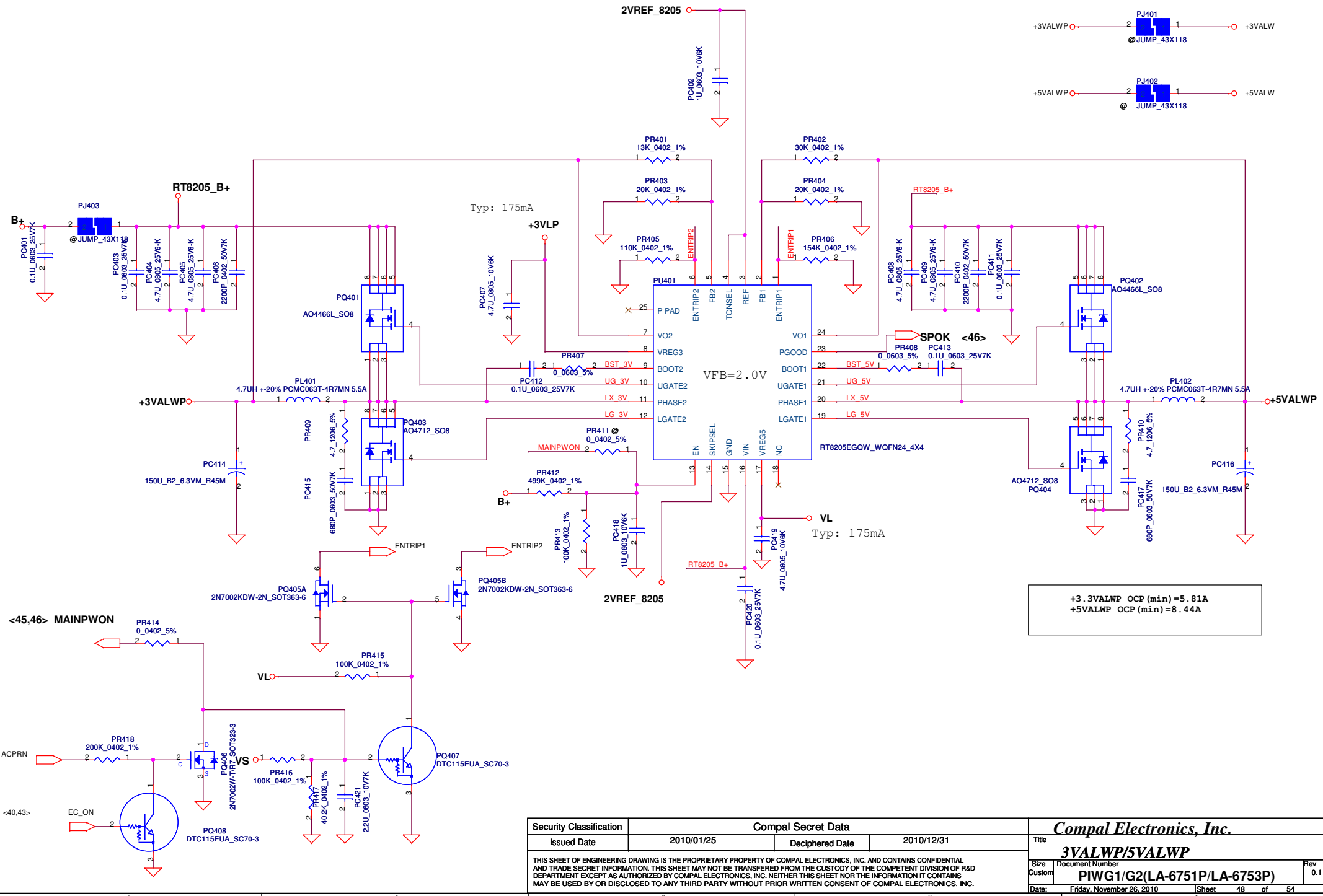
CP mode for 65W adapter
 $V_{aclip} = 2.39 * (2.2K / (2.2K + 21K)) = 0.2515V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 0.2515V$, $I_{input} = 2.76A$

CP mode for 90W adapter
 $V_{aclip} = 2.39 * (3.9K / (3.9K + 25.5K)) = 0.3544V$
 $I_{input} = (1/0.015) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 0.3544V$, $I_{input} = 3.827A$

3cell : GND
 4cell : VDD

| | | | | |
|---|-----------------------------|-----------------|------------|--------------------------|
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| Size | Document Number | Rev | | |
| | PIWG1/G2(LA-6751P/LA-6753P) | 0.2 | | |
| Date: | Friday, November 26, 2010 | Sheet | 47 | of 54 |

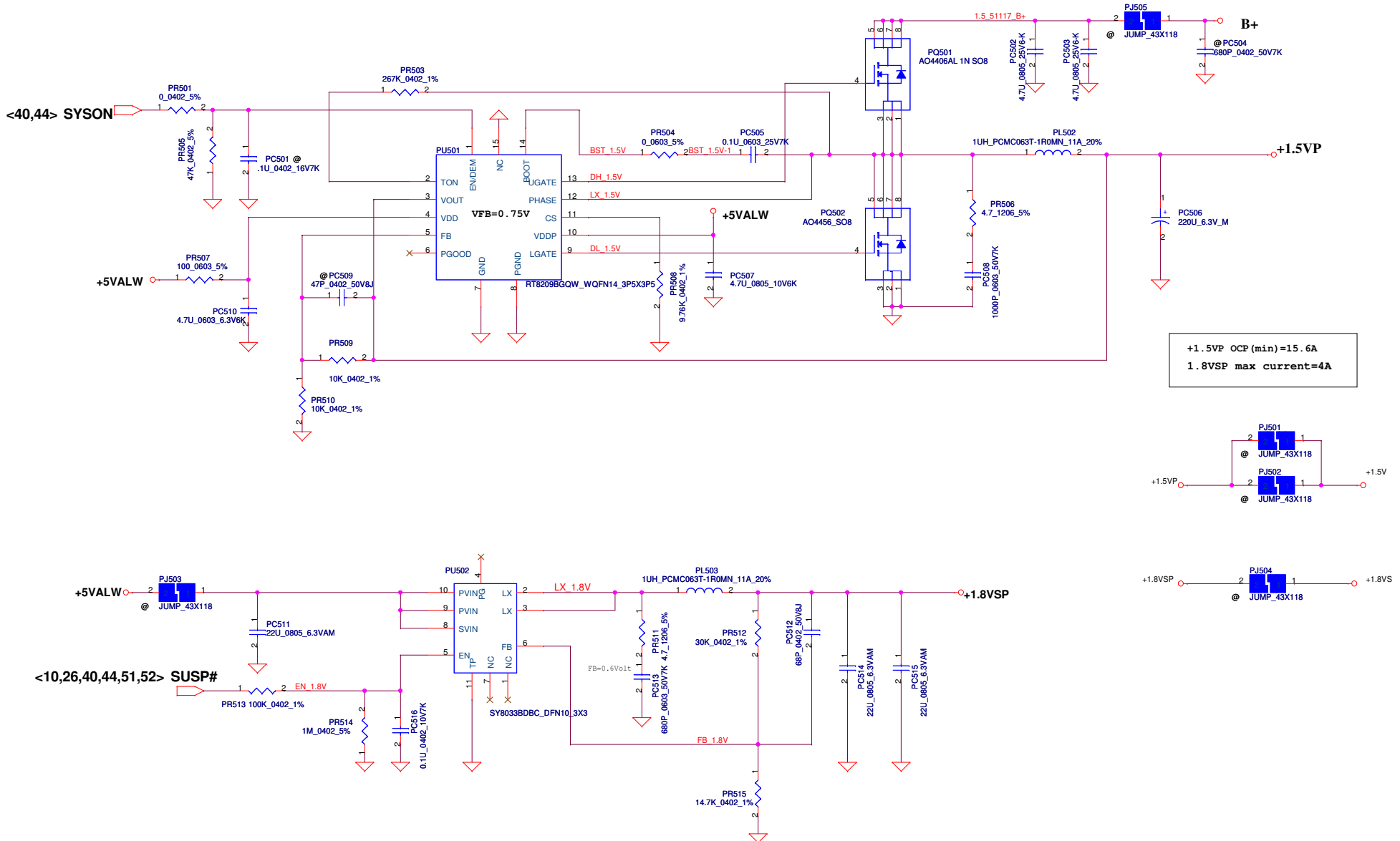
Note:
 Use TPS51125 IC can remove RTC referenece LDO
 Use TPS51427 IC must keep RTC referenece LDO



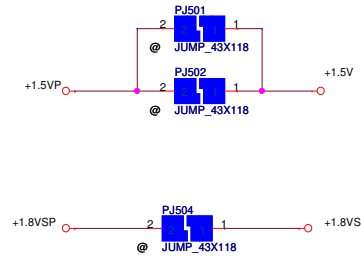
+3.3VALWP OCP (min)=5.81A
 +5VALWP OCP (min)=8.44A

| | | | |
|---|------------|--------------------|------------|
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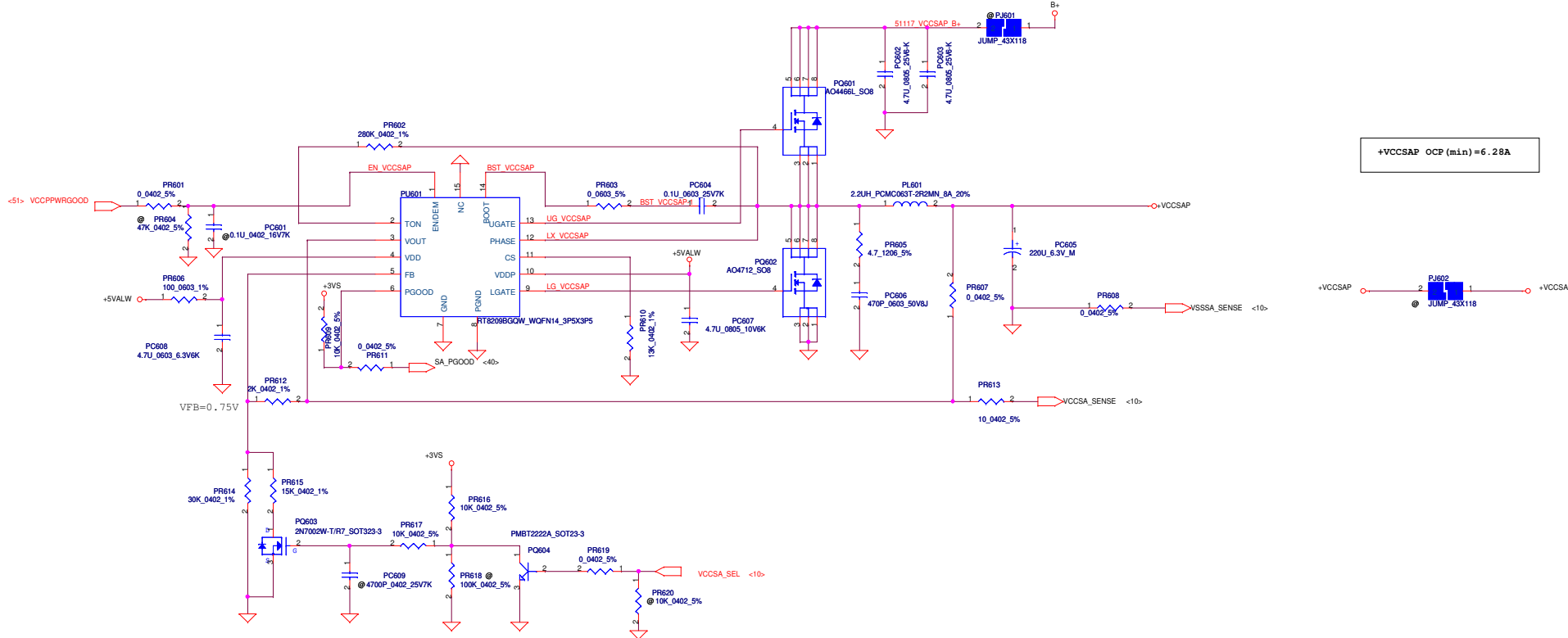
| | | | |
|---------------------------------|------------------------------------|-------|----------|
| Compal Electronics, Inc. | | | |
| Title | 3VALWP/5VALWP | | |
| Size | Document Number | Rev | |
| Custom | PIWG1/G2(LA-6751P/LA-6753P) | 0.1 | |
| Date: | Friday, November 26, 2010 | Sheet | 48 of 54 |



+1.5VP OCP (min)=15.6A
1.8VSP max current=4A



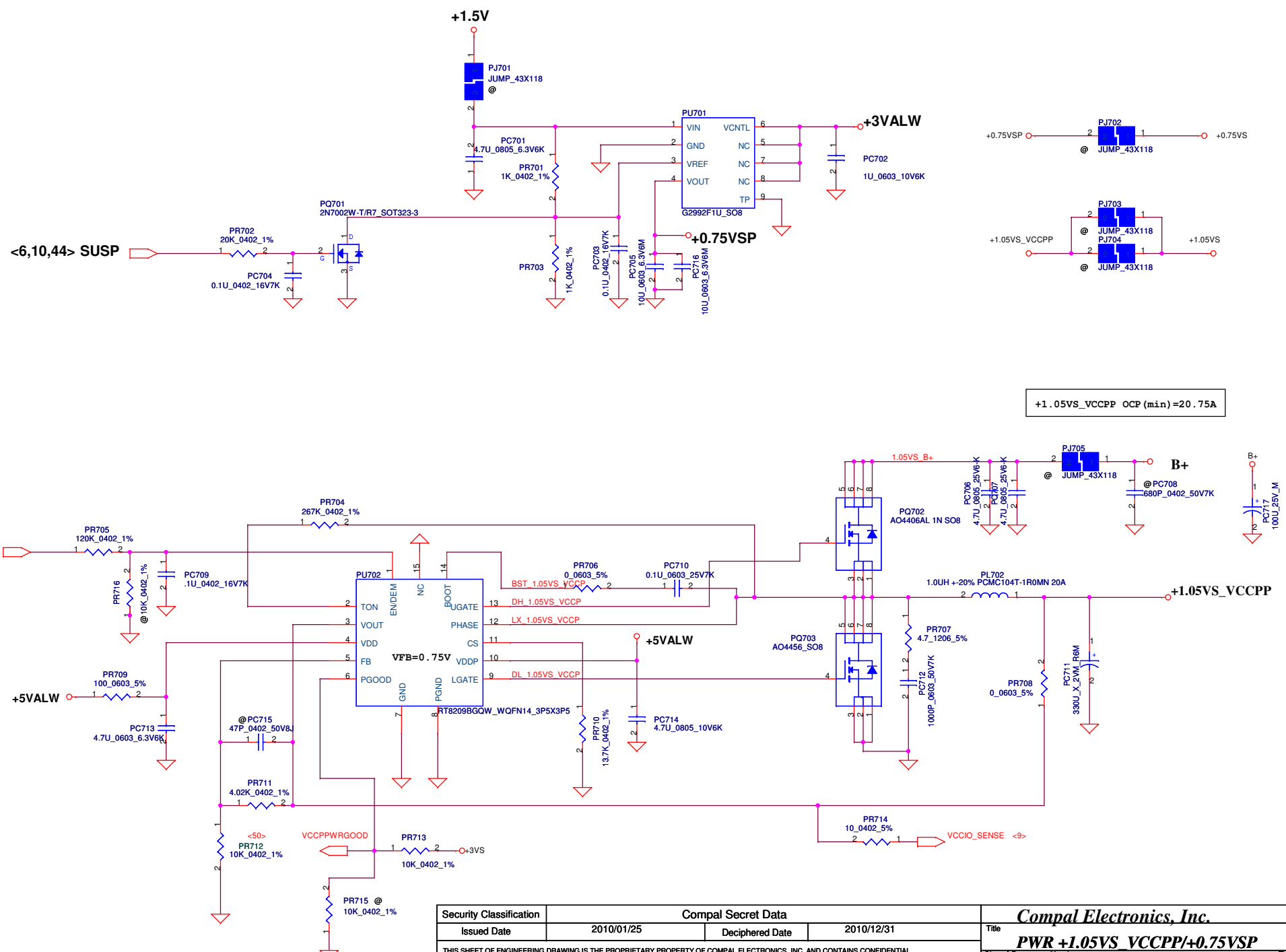
| | | | | | |
|---|-----------------------------|---------------------------|------------|--------------------------|-----|
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| Issued Date | 2010/01/25 | Deciphered Date | 2010/12/31 | Title | |
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| Size | Document Number | Date | | Sheet | Rev |
| Custom | PIWG1/G2(LA-6751P/LA-6753P) | Friday, November 26, 2010 | | 49 | 0.1 |
| | | | | of | 54 |



+VCCSAP OCP (min)=6.28A

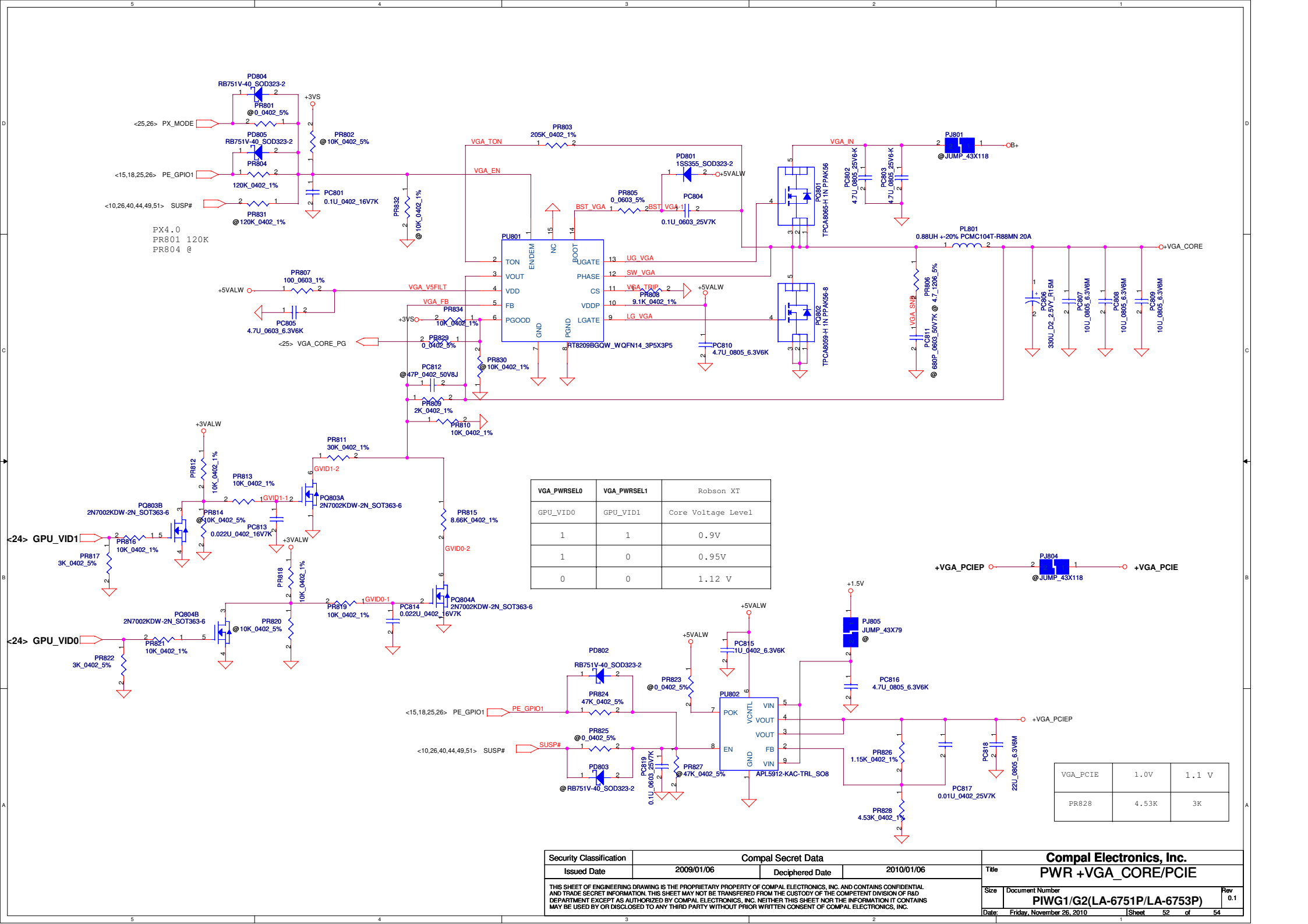
| VID[0] | VID[1] | VCCSA Vout | Require on 2011/ 2012 | Required |
|--------|--------|------------|-----------------------|----------|
| 0 | 0 | 0.9 V | Yes/Yes | Yes/Yes |
| 0 | 1 | 0.8 V | Yes/Yes | Yes/Yes |
| 1 | 1 | 0.725V | No/Yes | No/Yes |
| 1 | 1 | 0.675V | No/Yes | No/Yes |

Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (i.e. VCCSA_SEL) due to the VID[0] is don't care for this setting.



+1.05VS_VCCPP OCP (min) = 20.75A

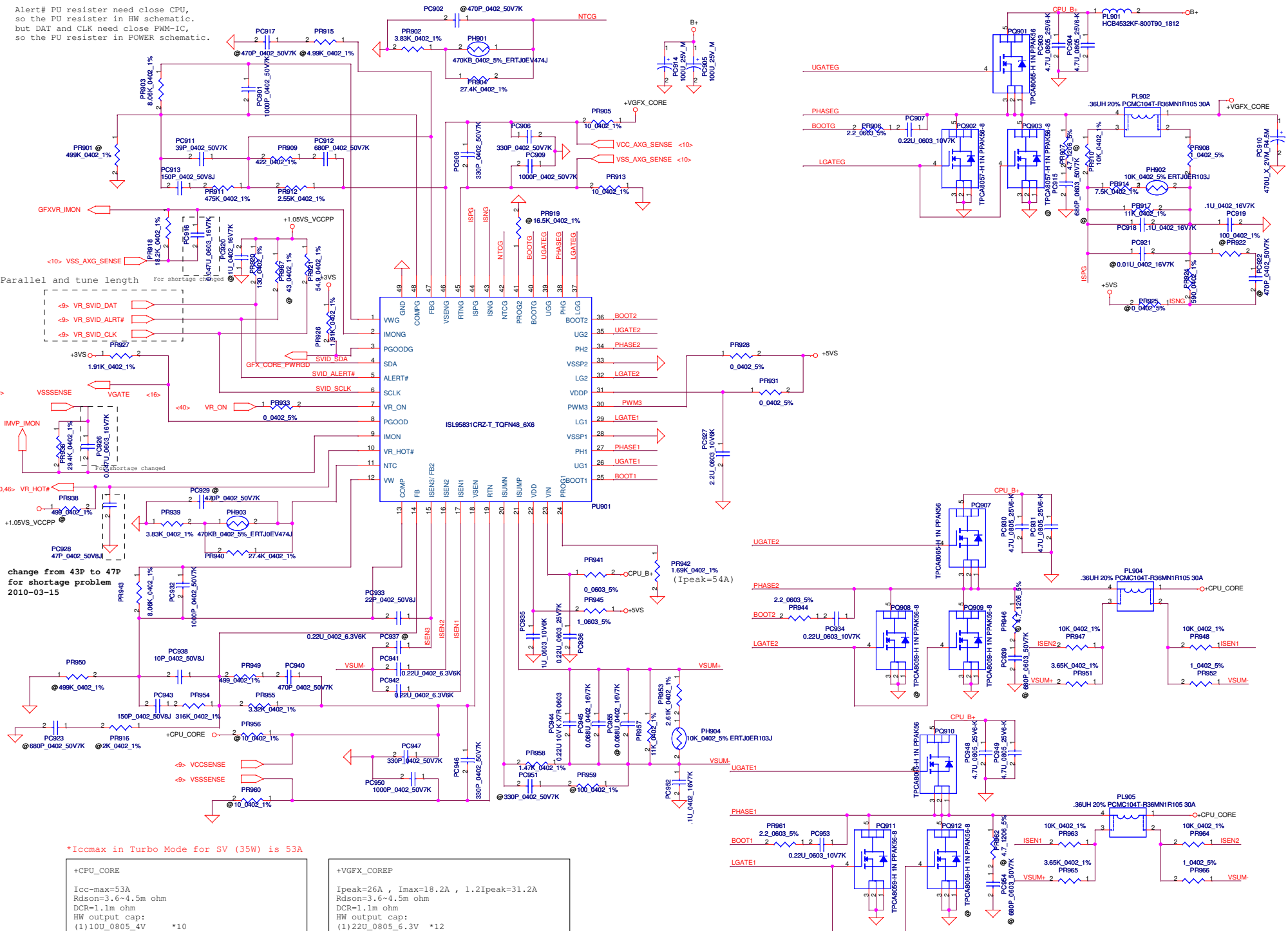
| | | | | | |
|---|---------------------------|--------------------|------------|--------------------------|---|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/01/25 | Deciphered Date | 2010/12/31 | Title | PWR +1.05VS_VCCPP/+0.75VSP |
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| Date: | Friday, November 26, 2010 | Sheet | 51 | of | 54 |



| VGA_PWRSEL0 | VGA_PWRSEL1 | Robson XT |
|-------------|-------------|--------------------|
| GPU_VID0 | GPU_VID1 | Core Voltage Level |
| 1 | 1 | 0.9V |
| 1 | 0 | 0.95V |
| 0 | 0 | 1.12 V |

| VGA_PCIE | 1.0V | 1.1 V |
|----------|-------|-------|
| PR828 | 4.53K | 3K |

Alert# PU resistor need close CPU, so the PU resistor in HW schematic. but DAT and CLK need close PWM-IC, so the PU resistor in POWER schematic.



*Iccmax in Turbo Mode for SV (35W) is 53A

| +CPU_CORE | |
|----------------------------------|--|
| Icc-max=53A | |
| Rdson=3.6-4.5m ohm | |
| DCR=1.1m ohm | |
| HW output cap: | |
| (1) 10U_0805_4V *10 | |
| (2) 22U_0805_6.3V *15 | |
| (3) 470U_D2_2V *4 (ESR=4.5m ohm) | |

*OCP setting value=71.5A

| +VGF_X_COREP | |
|---|--|
| Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A | |
| Rdson=3.6-4.5m ohm | |
| DCR=1.1m ohm | |
| HW output cap: | |
| (1) 22U_0805_6.3V *12 | |
| (2) 470U_D2_2V *2 (ESR=4.5m ohm) | |

*OCP setting value=37A

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| | | 2010/12/31 |

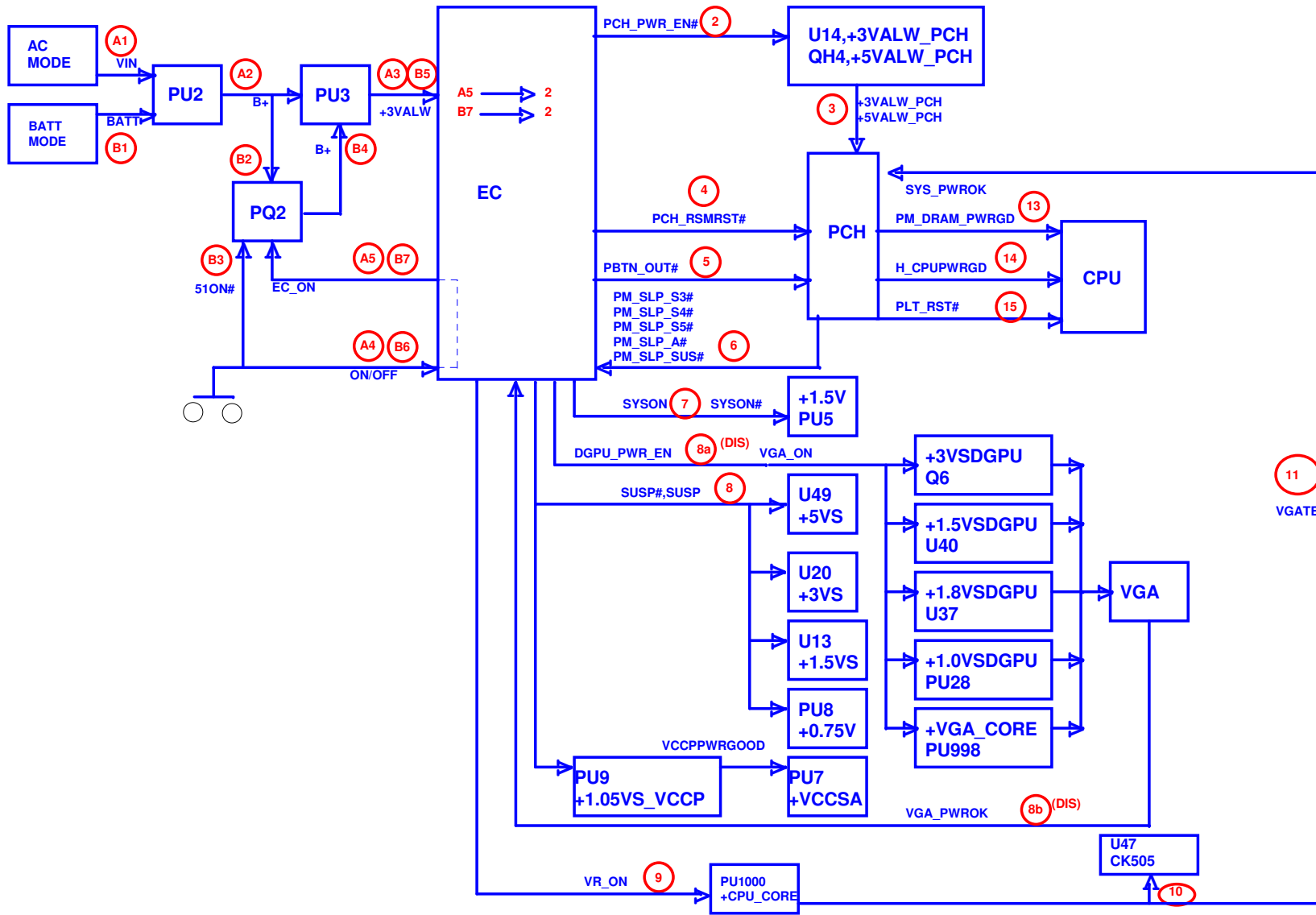
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|--|------------------------------------|----------------|
| Title PWR +CPU_CORE/+VGF_X_CORE | | |
| Size | Document Number | Rev |
| Custom | PIWG1/G2(LA-6751P/LA-6753P) | 0.1 |
| Date: | Friday, November 26, 2010 | Sheet 53 of 54 |

Version change list (P.I.R. List)

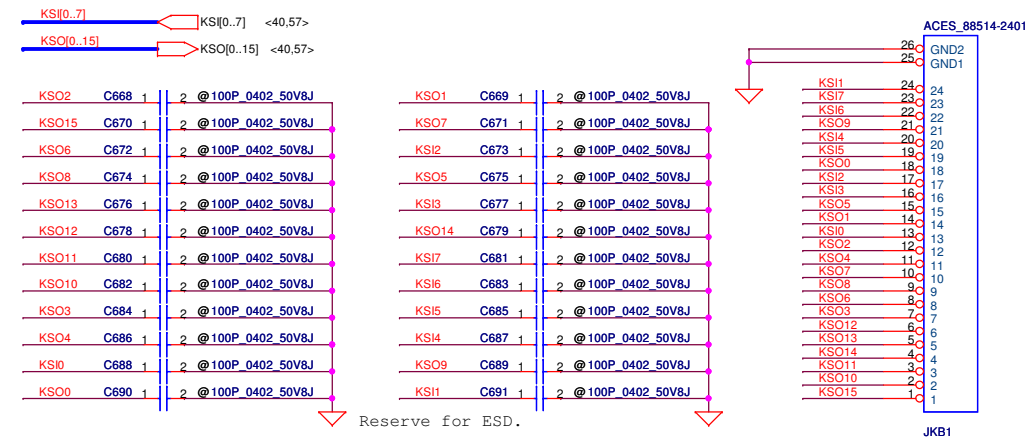
| Item | Reason for change | PG# | Modify List | Date | Phase |
|------|-------------------------------|-----|---|------------|-------|
| 1 | To reduce charger ripple | 47 | Add PC323 | 2010.08.15 | DVT |
| 2 | HW request for power sequence | 51 | Change +VGA_PCIE enable signal from PX_MODE to PE_GPIO1 PR804:120K PR831,PR801,PR825 UN-POP PR824:47K PC819:0.2uF | 2010.08.15 | DVT |
| 3 | Change Vboot setting | 52 | Change PR942 as 4.32K | 2010.08.15 | DVT |
| 4 | Change OCP setting | 52 | Change PR958 as 1.47K | 2010.08.15 | DVT |
| 5 | Add PC955 for loadline adjust | 52 | Add PC955 | 2010.08.15 | DVT |
| 6 | Reserve pull low resistor | 51 | Add PR718,PR832 | 2010.09.29 | PVT |
| 7 | Remove jump | 51 | Remove PJ802,PJ803 | 2010.09.29 | PVT |
| 8 | Adapter protect circuit | 46 | Pop PR222,PR208,PH202,PR221,PQ204 Un-Pop PR223,PR203 | 2010.09.29 | PVT |
| 9 | EMI Request | 47 | Remove PJ301 Add PL302 and reserve PC324 | 2010.09.29 | PVT |
| 10 | | | | | |
| 11 | | | | | |
| 12 | | | | | |
| 13 | | | | | |
| 14 | | | | | |
| 15 | | | | | |
| 16 | | | | | |
| 17 | | | | | |

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| Size | Document Number | PIWG1/G2 | | Rev | 0.1 |
| Date: | Friday, November 26, 2010 | Sheet | 54 | of | 54 |

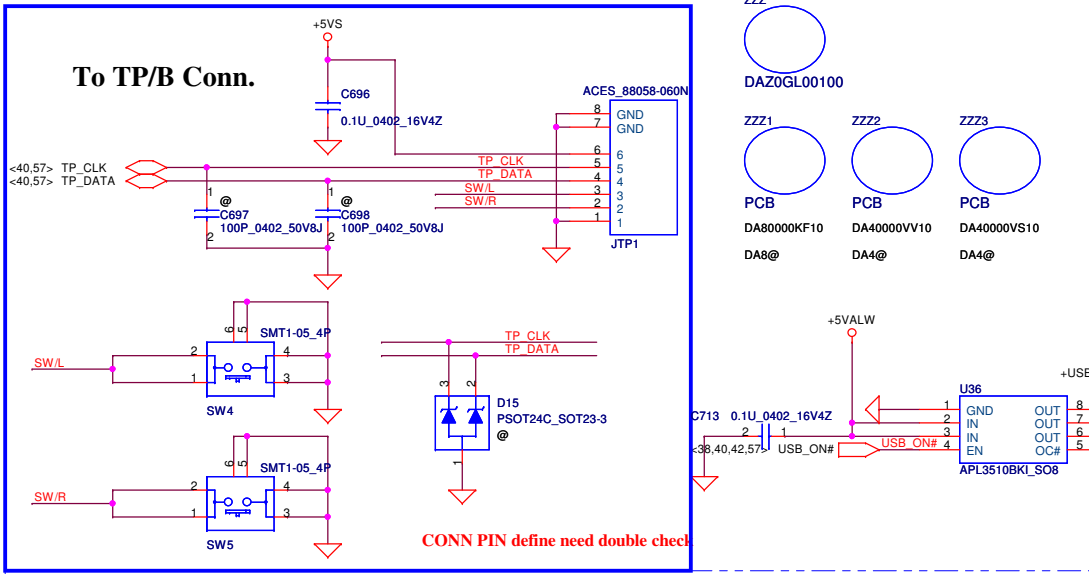


| | | | | |
|---|---------------------------|-----------------|------------|--------------------------|
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| Size | Document Number | Rev | | |
| Custom | LA-6751P | 0.2 | | |
| Date: | Friday, November 26, 2010 | Sheet | 55 | of 59 |

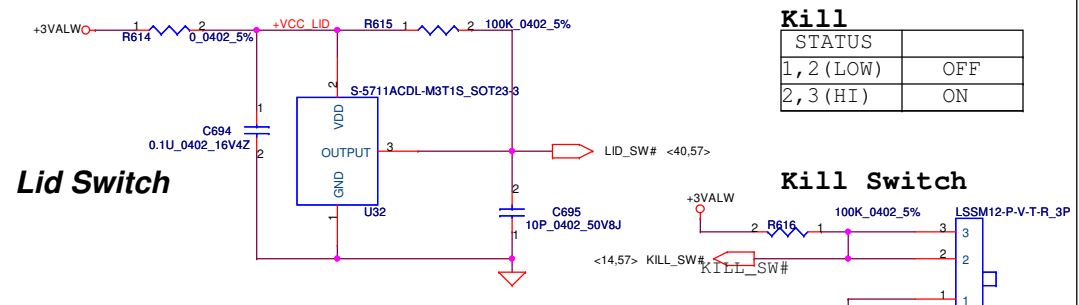
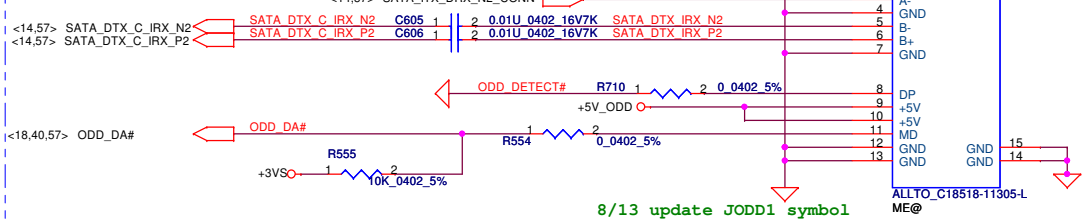
INT_KBD Conn.



CONN PIN define need double check

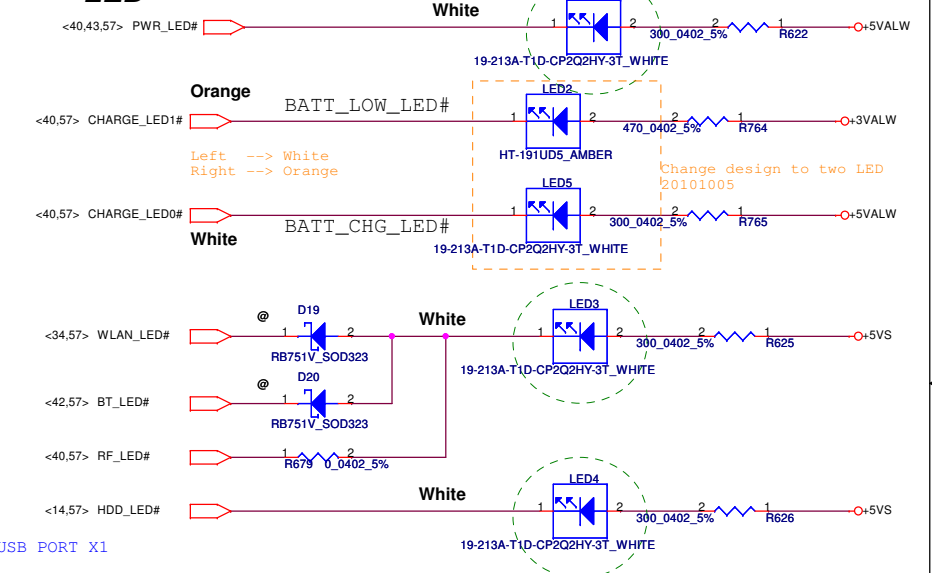


SATA ODD Conn.

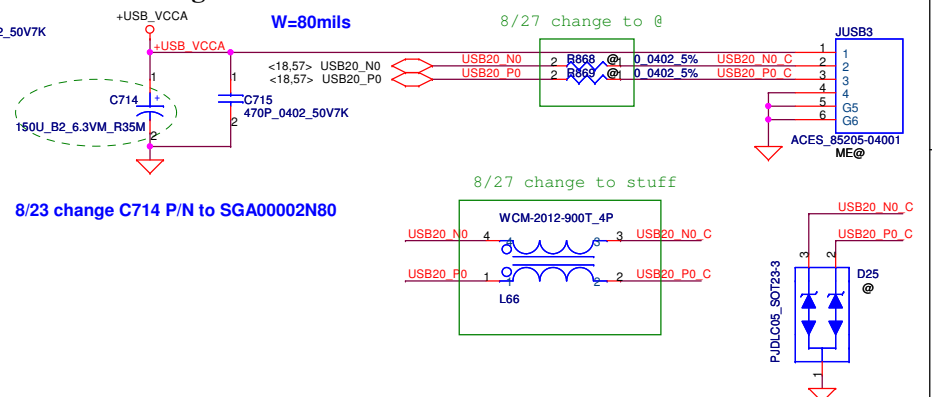


8/23 Change LED1/LED3/LED4 P/N to SC50000A300

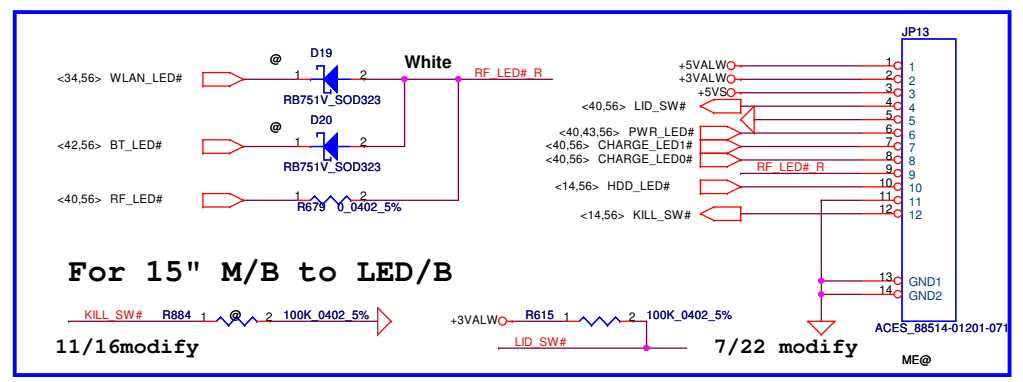
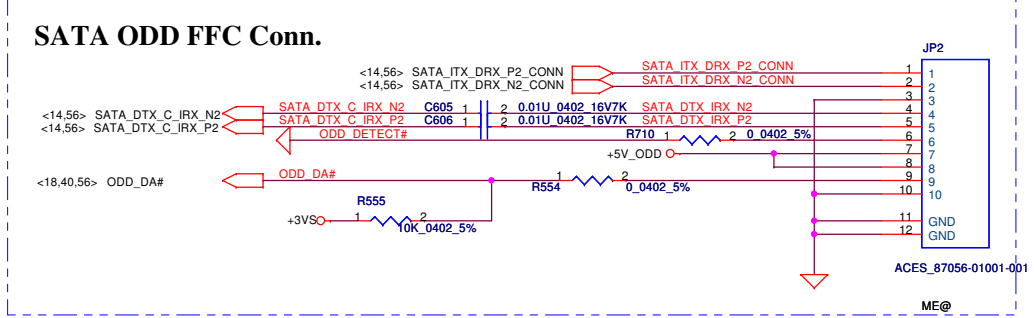
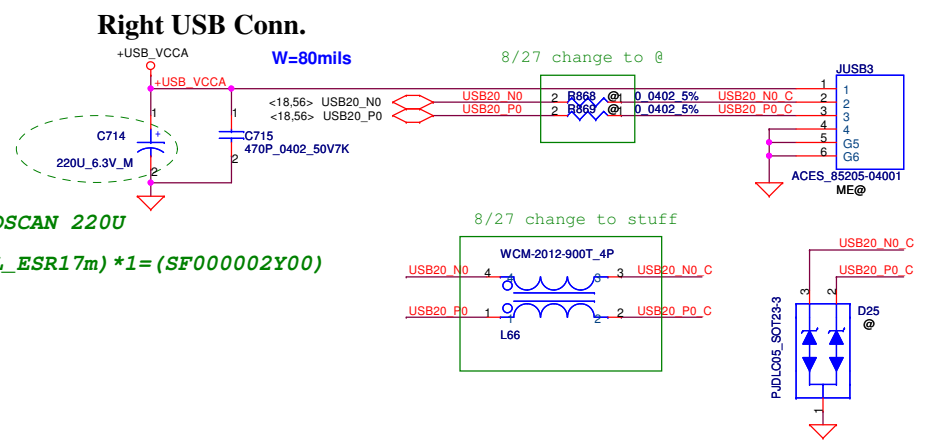
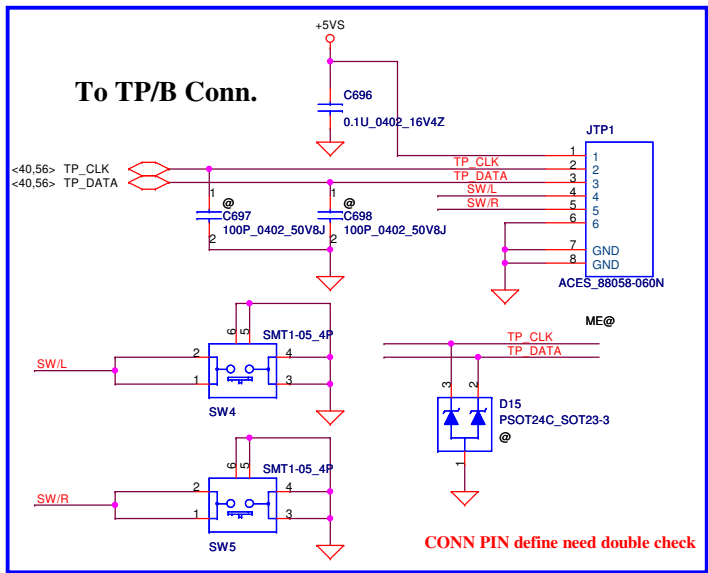
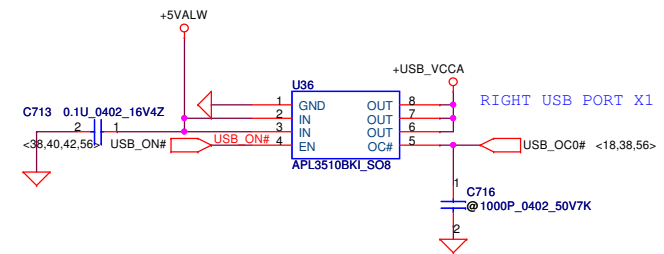
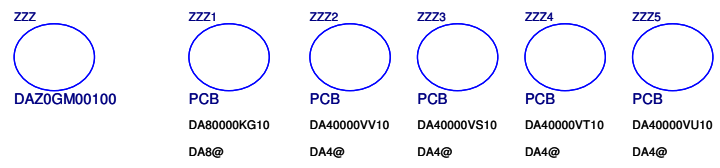
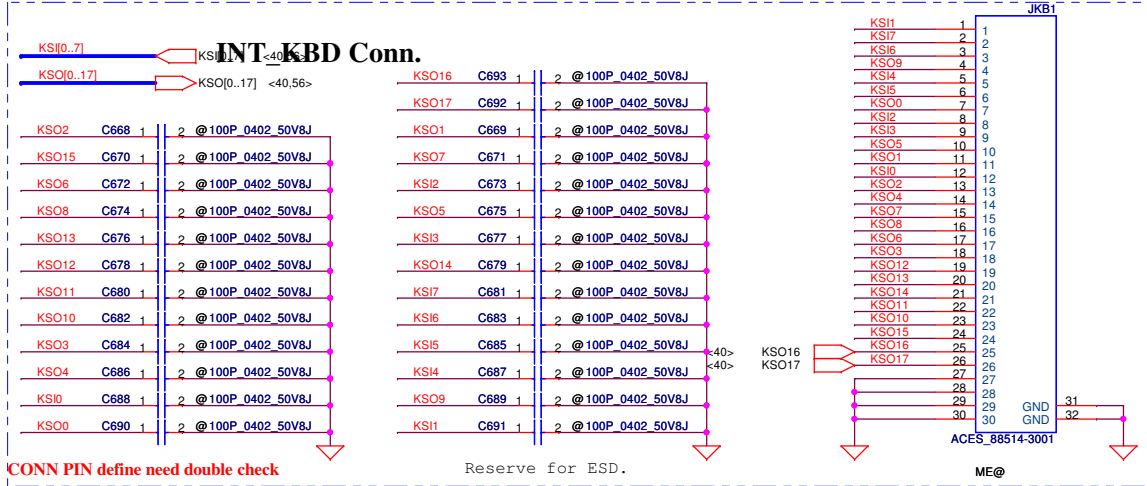
LED



Right USB Conn.



| | | | | | |
|---|-----------------|---------------------------|------------|--------------------------|--|
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| Size | Document Number | Date | | Rev | |
| B | LA-6751P | Friday, November 26, 2010 | | 56 of 59 | |



| | | | | | |
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| Size | Document Number | | | Rev | |
| B | LA-6751P | | | 0.2 | |
| Date: | Friday, November 26, 2010 | Sheet | 57 | of 59 | |

| PHASE | PAGE | Modification list | PURPOSE |
|-------|-----------|--|---|
| 0.2 | P31 | Change CRT Symbol | For CRT footprint issue |
| 0.2 | P31 | Del C510 | For Non-used part |
| 0.2 | P39 | change C610 pin 1 net name | change C610 pin 1 net name to correct |
| 0.2 | P35 | U25 change to U26 | For co-lay 10/100 and GIGA |
| 0.2 | P32 | Add R735,R736 | For DIS only SMBus pull high |
| 0.2 | P33 | Add R738,R739 | For DIS only SMBus pull high |
| 0.2 | P33 | Change Q63 BOM structure to HDMI@ | For DIS HDMI function |
| 0.2 | P40 | Add R740, C93 | For EC request |
| 0.2 | P18 | Change R215 pin1 net name | Change R215 pin1 net name to correct |
| 0.2 | P18 | Add R741 | Add R741 for Reserved PE_GPIO0 |
| 0.2 | P16 | Add R742, R743 | For PCH power sequence |
| 0.2 | P38 | Del U28, R542-R551 , J12 | Del USB charger circuit |
| 0.2 | P40 | Add EC pin 97,98,103 | Add EC pin 97 for SYS_PWROK_EC , pin 98 for CE_EN , pin 103 for BATT_SEL_EC |
| 0.2 | P24 | Change R662 pin 2 net name | Change R662 pin 2 net name to correct |
| 0.2 | P28 | Del C421,C422,C431,C432,C433, L27, Add R745, U8 pin N11,N12 change to NC | For AMD new document suggestion |
| 0.2 | P26 | Add R744 | Add R744 for control PE_GPIO1 from SUSP# |
| 0.2 | P39 | Change J10 footprint and Add J13 | Change J10 footprint by Dfx request and Add J13 by vendor suggestion |
| 0.2 | P39 | Change PC_Beep circuit | Change PC_Beep circuit |
| 0.2 | P6 | Add R161, R182, R192 BOM structure hange to @ | Follow ORB circuit |
| 0.2 | P58/59 | Add R615 in 15" and 17" page | Pull high LID_SW# at M/B side |
| 0.2 | P31 | Add Q83 pin 1 power net name +CMOS_PW | For power trace net |
| 0.2 | P56/57/58 | Change JF21 to JKBl | Change connector to standard name |
| 0.2 | P56/57/58 | Change JF4 to JTP1 | Change connector to standard name |
| 0.2 | P43/60 | Change JP6 to JPPWRB1 | Change connector to standard name |
| 0.2 | P34 | Change JP1 to JWLN1 | Change connector to standard name |
| 0.2 | P42 | Change JP5 to JBT1 | Change connector to standard name |
| 0.2 | P43/60 | Change JP7 to JCR1 | Change connector to standard name |
| 0.2 | P19 | Add R542 | For ESATA detect function |
| 0.2 | P42 | Add R886, R887 , C735 | For ESATA detect function |
| 0.2 | P31 | Add R543 | For reserve EC control directly |
| 0.2 | P39 | Change J10 footprint, Del C635, C636 | Change J10 for Dfx and Del component for layout |
| 0.2 | P42 | Add R877 | For reserve EC control directly |
| 0.2 | P42 | SW3 BOM structure change to @ | For ME ASSY concern |
| 0.2 | P24 | R324 BOM structure change, del @ | For AMD update |
| 0.2 | P25 | Change Q69,Q70,Q71,Q72 to BSS138, change Q66,Q67 pin 1 net name, D28 change to @ | For Change BACO part follow AMD reference DATA ,D28 change to @ for leakage |
| 0.2 | P42 | Change ESATA from port 5 to port 4 | For intel risk |
| 0.2 | P15 | Add R544,R545 | For Pull high SMBus |
| 0.2 | P12/13 | Del R74-R80,R82 R88-R94,R96 | For DDR3 DM Bus to GND |
| 0.2 | P16 | Add R182,R546 | Add 186 for reserve sequence, Add R546 for follow CRB & ORB |
| 0.2 | P20 | Del Add J12, R257 change to @ | For voltage drop |
| 0.2 | P26 | R161 Change Q6 to U14 | Change SI2301 to SI4800 for loading current |
| 0.2 | P6 | R161 change to 100K | Follow CRB |
| 0.2 | P19 | Add R547 , R250 change to @ | Follow Module and CRB |
| 0.2 | P18 | WLAN USB port for port8 to port9 | For debug port |
| 0.2 | P25 | AND Gate power change to +3VGS | For VGA circuit |
| 0.2 | P24 | Add R548, R549 | For DIS HDMI audio strap |
| 0.2 | P39 | Del J13 | For layout space |
| 0.2 | P20,39,42 | Add C395 , R581 , R583 , R584 , R586 , R587 | For customer request reserved |
| 0.2 | P20 | Add C129, C396 , Del R264 | For reserved |
| 0.2 | P40 | Add PIN 66 , R740,C93 change to @ | Add IMVP_IMON |
| 0.2 | P9 | Add R74 | For VCCIO_SENSE / VSSIO_SENSE differential routing |

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| PHASE | PAGE | Modification list | PURPOSE |
|-------|------|--|--|
| 0.2 | P33 | Del R051 ~ Q54 Add Q95 | For DIS HDMI |
| 0.2 | P39 | Del J10, C637, C640, R576, R577, R579 change to @ , L40-L43 change to R720-R723 Del C643, R578 , MIC_INR connect MIC_INL , Add R578 | For Vendor suggestion and EMI Del C653, R578 connect MIC_INR/L for vendor suggestion , Add R578 for EMI |
| 0.2 | P20 | Add L75 , R264 , C917, R259 C226 change to @ | For intel PDDG update |
| 0.2 | P20 | Change JCR1 pin define , MIC change with HP | For correct ID |
| 0.2 | P9 | Add C394, C397 , C400 , Add R75 | For CPU_CORE power reserved at Bottom side, Add R75 for reserved at cpu side and pwr side |
| 0.2 | P26 | Add R688 change to 20k, R345 change to 200k , R350 change to 330k , Q65 stuff | For VGA power sequence |
| 0.2 | P42 | Change C706 P/N to SF000001500 | Change to H=6 OSCAN |
| 0.2 | P10 | Change CI28 to @ | For Reserved |
| 0.2 | P26 | Change D3 change to @ | For VGA leakage |
| 0.2 | P25 | Change BIF_VDDC control pin net name | For correct behavior |
| 0.2 | P56 | Update JODDI symbol | For ME update drawing |
| 0.2 | P16 | D29 change to @ | For AC detect issue |
| 0.2 | P24 | R548, R549 change to DIS@ | For AC detect issue |
| 0.2 | P10 | CI28 change to stuff | For test on DVT |
| 0.2 | P44 | Del Q118, R657 | For not need |
| 0.2 | P57 | Change I5" C714 to OSCAN | For ME Space ok |
| 0.2 | | Change R513, R516 , R667 P/N and from 0805 to 0603 | For common part |
| 0.2 | | Change C633, C634 , C642 | For common part |
| 0.2 | | Change D3, D29 P/N and symbol | For common part |
| 0.2 | | Change U3, U11, U13, U14, U38, U39 P/N and symbol | For common part |
| 0.2 | | Change U3, U11, U13, U14, U38, U39 P/N and symbol | For common part |
| 0.2 | | Change Q8, Q65, Q80, Q83, Q99, Q104 P/N and symbol | For common part |
| 0.2 | | Change Q1, Q37, Q93 P/N and symbol | For common part |
| 0.2 | | Change Q94, Q95 P/N and symbol | For common part |
| 0.2 | | Change Q3, Q4, Q7, Q9, Q66, Q67, Q68, Q73, Q74, Q75, Q76, Q77, Q78, Q79, Q82, Q85, Q86, Q87, Q102, Q106, Q107, Q108, Q109, Q110, Q111, Q112, Q113, Q114, Q115, Q116 P/N and symbol | For common part |
| 0.2 | P43 | Change C635 part and change to @ | For EMI |
| 0.2 | P18 | Reserved R551 | Reserved |
| 0.2 | P9 | Change C53, C85, C86, C87 , C394, C397, C400 to stuff and change C48, C80, C81, C82, C89, C90, C91 to @ | For CPU_CORE |
| 0.2 | P10 | Change C110, C111, C112, C113 to stuff | For VGF_X_CORE |
| 0.2 | P56 | Change LED1/LED3/LED4 P/N to SC50000A300 | Change P/N |
| 0.2 | P36 | Change T1, T2 P/N to SP050003N00 | For test pass part |
| 0.2 | P40 | Change R611, R740, C93 to stuff and change Y5, C347, C367 to @ Change R695 to 18K, Q37 change to @, R747 change to stuff, | For SUS_CLK R695 for Board ID, Q37, R747 for VR_HOT |
| 0.2 | P41 | Change U33 P/N to SA00003FL10 | For BIOS ROM |
| 0.2 | | Change C509, C511, C635 to stuff | For EMI request |
| 0.2 | P56 | Change I4" C714 P/N to SGA00002N80 | For Sourcer request |
| 0.2 | P39 | Change R720, R721, R722, R723 P/N to SM01000BZ00 (Bead), and Change C647, C649, C650, C651 to Stuff | For EMI request |
| 0.2 | P19 | Change R303 to Stuff, and change R542 to @ | For BIOS ESATA detect function |
| 0.2 | P56 | Change U32 P/N to SA00003IC00 | For common part |
| 0.2 | P36 | Change T1, T2 P/N to SP050006E00 | For correct part |
| 0.2 | P10 | R688 change to stuff , R687 , Q7 change to @ | For S3 power reduction |
| 0.2 | | Change R660, R661, R862, R863, R864, R865, R868, R869 to @ , change L63, L64, L65, L66 to stuff , change R619 to Bead (SM01000DI00) | For EMI |
| 0.2 | P20 | Change L75 symbol | For common part |

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PHASE PAGE Modification list

PURPOSE

| | | | |
|-----|-----|--|--|
| 0.3 | P10 | Update Q5 symbol | For update symbol |
| 0.3 | P33 | Add F2 | For safty request |
| 0.3 | P39 | Update U30 P/N to SA00003K410 and Add R879 | For Audio update to 21Z |
| 0.3 | P10 | Change CI28 to D2 size and e | Change size for M/E issue |
| 0.3 | P14 | Add reserve R878 | For Intel DG 1.5 |
| 0.3 | P37 | C592 change P/N to SF000001500 (H=6) | For ME Z high ok |
| 0.3 | P25 | Update Q69-Q72 to A03414 ,D28 R873 change to BACO@ , U40 change to @ | For PX4.0 |
| 0.3 | P28 | Add reserve C94 | For reserve VGA_CORE |
| 0.3 | P29 | R369 P/N change to SD034100A80 | For GP part |
| 0.3 | P18 | R553,R691,R684,R682,U12 change to PX@ | For PX 4.0 |
| 0.3 | P6 | Reserved R880 to SYS_PWR0K | Follow ORB |
| 0.3 | P10 | R62,R63 change to 1K | Follow CRB |
| 0.3 | P19 | R303 change to @, Change M/B ID to PX4.0 | For ESATA and PX4.0 |
| 0.3 | P25 | Q69-Q72 change to BACO @ | For PX4.0 |
| 0.3 | P26 | R719 change to stuff, R744 change to @ , R677 change to BACO@ | For PX4.0 |
| 0.3 | P33 | R483,R484 change connect to +5V_HDMI_F | For Add F2 |
| 0.3 | P37 | Change U27 P/N to SA000046C00 | For Fintek |
| 0.3 | P40 | Change R594 pull high to +5VALW | For leakage issue |
| 0.3 | P19 | R881 change to Dstuff, R244 change to @ | For intel MRC Rev0.9 |
| 0.3 | P14 | R878 change to stuff | For intel DG 1.5 |
| 0.3 | P31 | Del R432 | For non-used part |
| 0.3 | P36 | Reserved D31 , C643 , C644 | For reserved EMI parts |
| 0.3 | P37 | Del R581 | For non-used part |
| 0.3 | P38 | Del R550 | For non-used part |
| 0.3 | P38 | Change C592 P/N to SF000002Y00 | For M/E Z high limlt |
| 0.3 | P39 | Del R584, R586 , R587 | For non-used part |
| 0.3 | P40 | Change R600, R604 to 2.2K Change R695 to 8.2k | Change R600, R604 for Battery SMBus, R695 for Board ID |
| 0.3 | P42 | Del R583 | For non-used part |
| 0.3 | P6 | Reserved R882 connect to PCH_PWR0K | Reserved for intel |
| 0.3 | P56 | R765 change to 300 ohm | For LED |
| 0.3 | P25 | R324, R744 , R674 change DIS@ | For DIS only sku |

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