

Compal Confidential

VALGC_GD M/B Schematics Document

AMD Fs1r2 Richland Processor with DDRIII + Bolton-M3 FCH

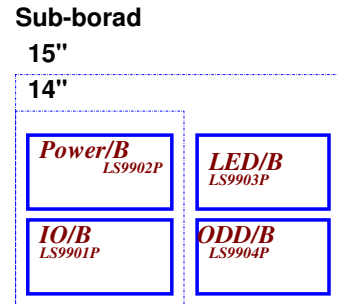
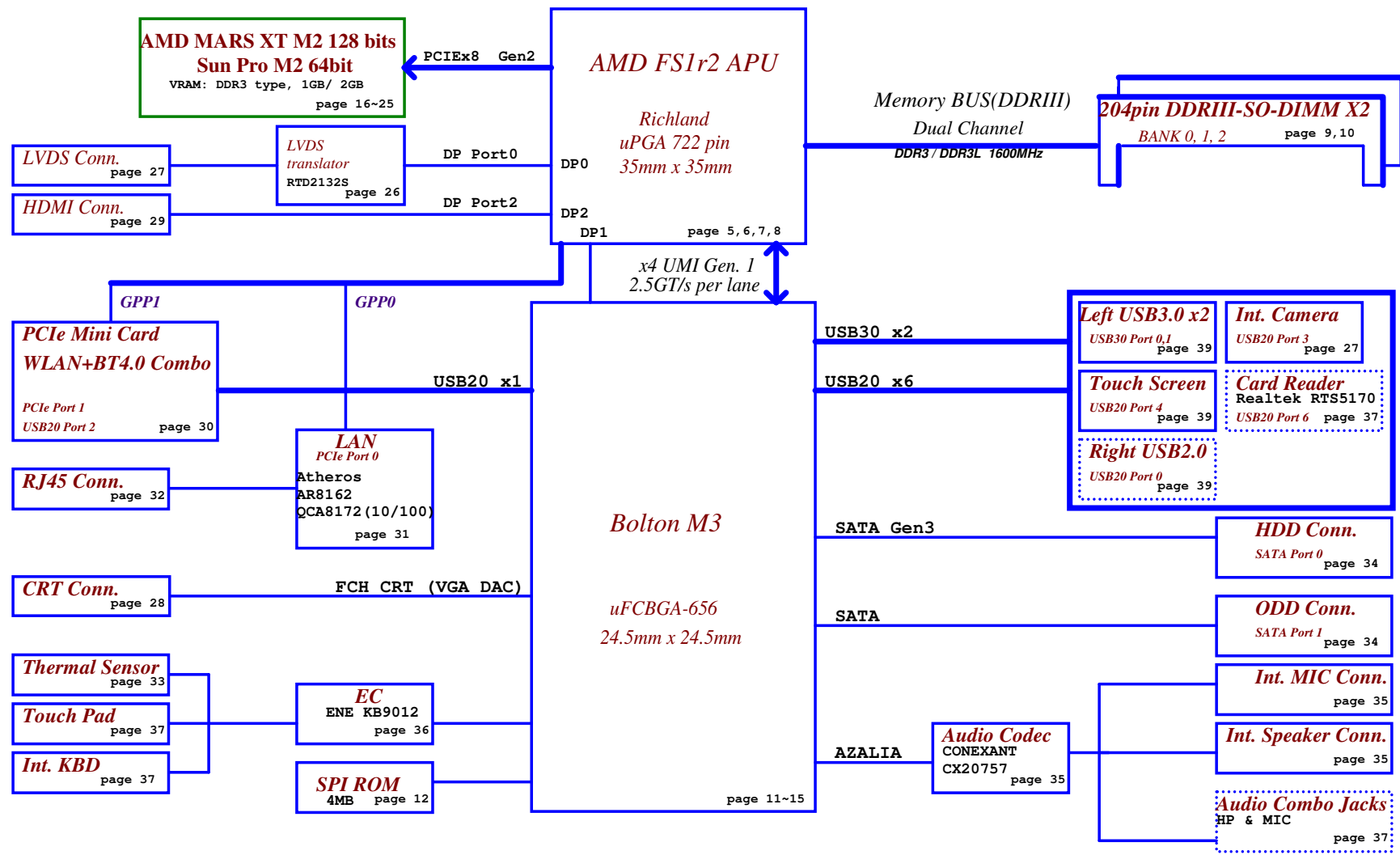
AMD Mars XT M2

LA-A091P

2013-04-16

REV: 1.0

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Compal Electronics, Inc.
MB Block Diagram

Voltage Rails

power plane	State	+B	+5VALW	+1.5V	+1.5V_APU	+3VALW	+1.1VALW
S0		○	○	○	○		
S3		○	○	○	○		✗
S5 S4/AC		○	○	✗	✗		✗
S5 S4/ Battery only		○	✗	✗	✗		✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗		✗

- +5VS
- +3VS
- +2.5VS
- +1.5VS
- +1.2VS
- +1.1VS
- +0.75VS
- +APU_CORE
- +APU_CORE_NB
- +VGA_CORE
- +3.3VGS
- +1.8VGS
- +1.5VGS
- +0.95VGS

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.2
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Ra = R310
Rb = R311

BOM Structure Table

BOM Structure	BTO Item
PX@	VGA circuit
14@	For 14"
15@	For 15"
45@	HDMI LOGO
CMOS@	CMOS Camera part
8162@	AR8162 LAN part
8172@	AR8172 LAN part
CMOS@	For CMOS circuit
TS@	For Touch Screen circuit
X76@	X76 Level part for VRAM
GCLK@	Use GCLK circuit
NOGCLK@	No use GCLK circuit
GCLK302@	302 part for DIS
GCLK238@	238 part for UMA
LVDS@	LVDS circuit
PXNOGCLK@	No use GCLK circuit in GPU
LDO@	LDO mode for LAN
SWR@	SWR mode for LAN
DEBUG@	For debug
ME@	ME part
MIC@	MIC part
885N@	Unpop in KBC page
JUMP@	JUMP
TEST POINT@	TSET POINT
SHORT PAD@	SHORT PAD
EMI@	EMI part
@ESD@	Reserve for ESD
@EMI@	Reserve for EMI
@	Unpop
MARS@	VRAM CHB parts for MARS
2132S@	Panel PWM part for RTD2132S
2132R@	Panel PWM part for RTD2132R
ShareROM@	Reserve for ShareROM
Strap@	Reserve for Strap pin

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
		0	USB Port 2.0 (Right Side)
		1	
		2	Mini Card(WLAN)
		3	Camera /
		4	Touch Screen
		5	
		6	Card Reader
		7	
		8	
		9	
		0	10 USB 2.0 Port (Left Side)
		1	11 USB 2.0 Port (Left Side)
		2	12
		3	13

USB OC MAPPING

OC#	USB Port	
0	USB20 port10,port11	USB30 port0,port1
1	USB20 port0	
2		
3		

APU PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	

FCH PCIE PORT LIST

Port	Device
1	
2	
3	
4	

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
SMB_EC_DA1	KB9012 +3VALW	X	X	X	X	X	X	X	V +1.5V	X
SMB_EC_CK2_SUS	KB9012 +3VALW	X	X	X	X	X	X	X	V	X
SMB_EC_DA2_SUS	KB9012 +3VALW	X	X	X	X	X	X	X	V	X
FCH_SCLK0	FCH +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
FCH_SDATA0	FCH +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2	KB9012 +3VS (LV shifter)	V	X	X	X	X	V	X	X	V
SMB_EC_DA2	KB9012 +3VS (LV shifter)	V	X	X	X	X	V	X	X	V

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor	1001_101xb
		SB-TSI(default)	1001_100xb
		VGA(int. thermal)	1000_001xb
		RTD2132S	1010_1000b
		VGA(ext. thermal)	0100_1101b

EC SM Bus2 address

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

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X76@ Mars XT VRAM STRAP

X76@

	Vendor UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
MS2G	Samsung 2048Mbits SA000068000 128Mx16 K4W2G1646E-BC1A FBGA	0	0	0	NC	4.75K
MM2G	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:k	0	0	1	8.45K	2K
MH2G	Hynix 2048Mbits SA000065300 128Mx16 H5TQ2G63DFR-NOC FBGA	0	1	0	4.53K	2K

X76@ Sun PRO VRAM STRAP

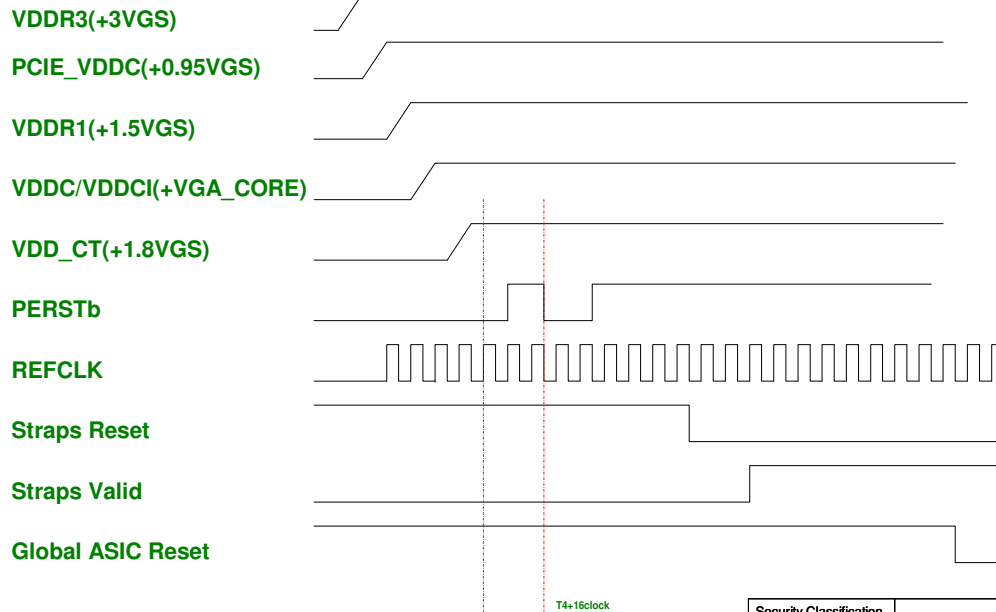
X76@

	Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
SS2G	Samsung 2048Mbits SA000068000 256Mx16 K4W2G1646E-BC11 FBGA	0	0	0	NC	4.75K
SM2G	Micron 2048Mbits SA000065000 256Mx16 MT41K256M16HA-107G	0	0	1	8.45K	2K
SS1G	Samsung 1024Mbits SA000068000 128Mx16 K4W2G1646E-BC1A FBGA	0	1	1	6.98K	4.99K
SM1G	Micron 1024Mbits SA000067500 128Mx16 MT41J128M16JT-093G:k	1	1	0	3.4K	10K
SH1G	Hynix 1024Mbits SA000065300 128Mx16 H5TQ2G63DFR-NOC FBGA	1	1	1	4.75K	NC

Power-Up/Down Sequence

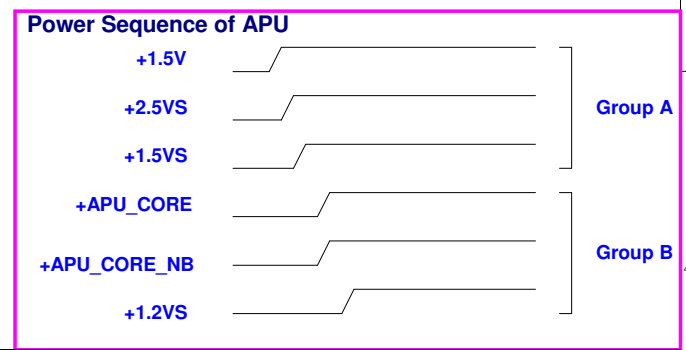
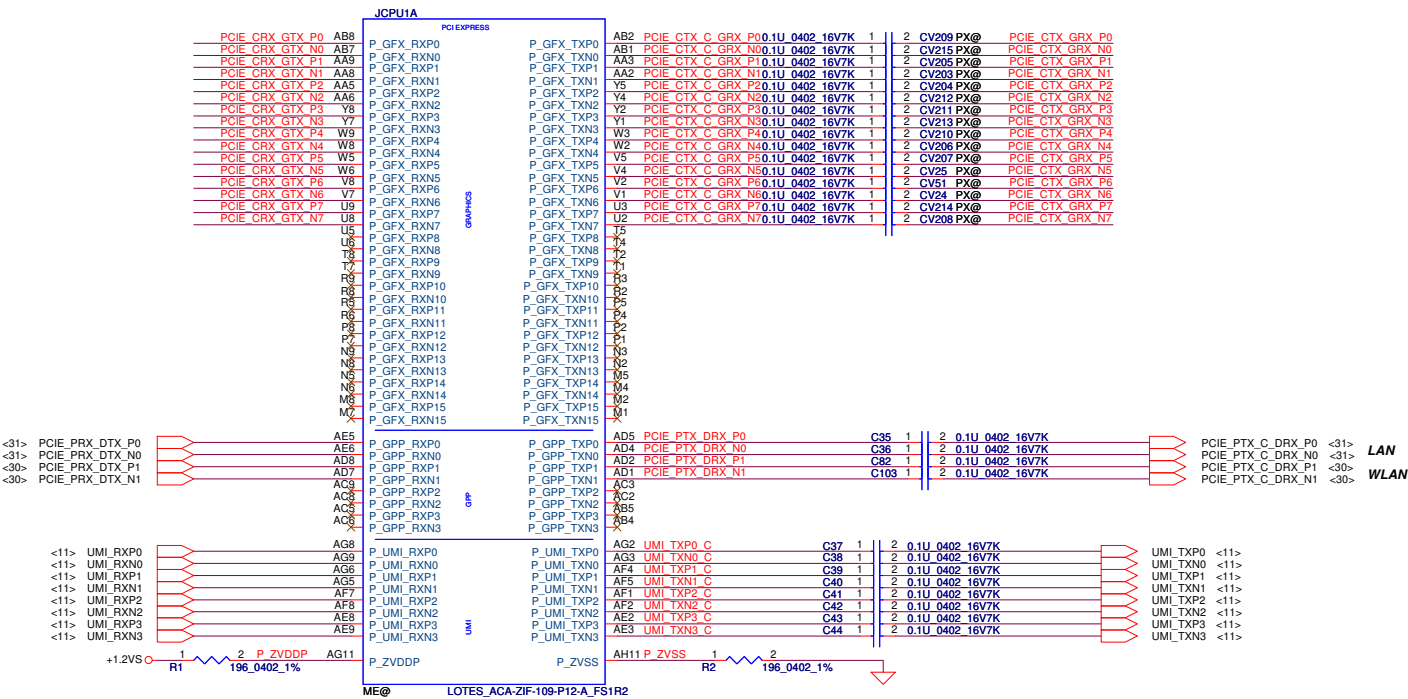
"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

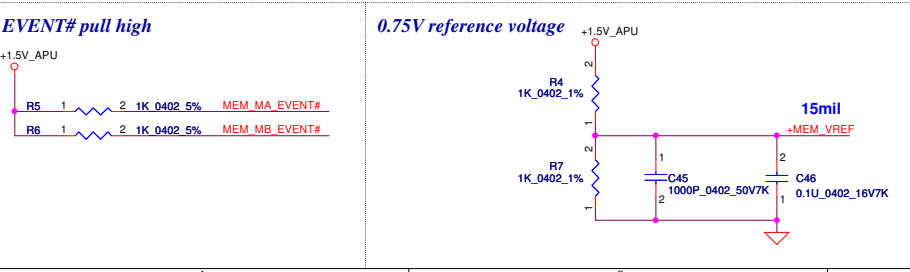
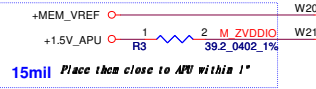
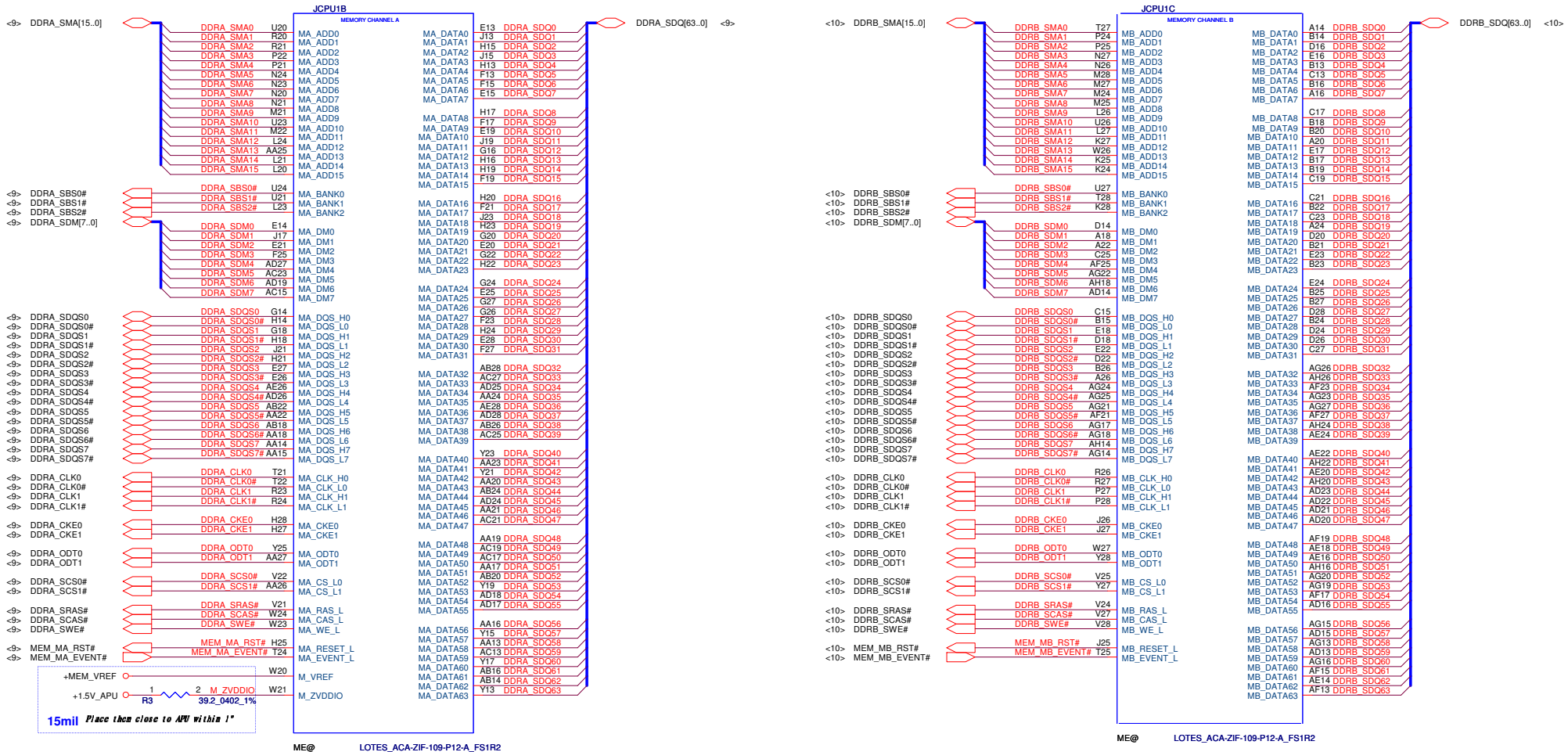


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<16> PCIE_CRX_GTX_P[0..7] <16> PCIE_CTX_GRX_P[0..7]
 <16> PCIE_CRX_GTX_N[0..7] <16> PCIE_CTX_GRX_N[0..7]



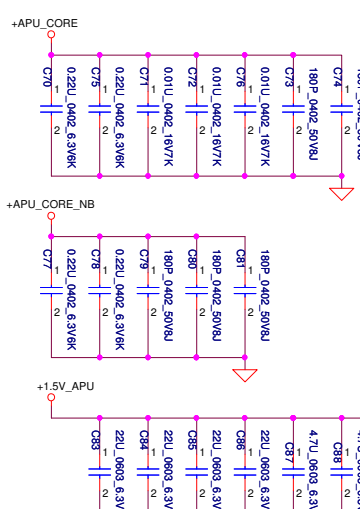
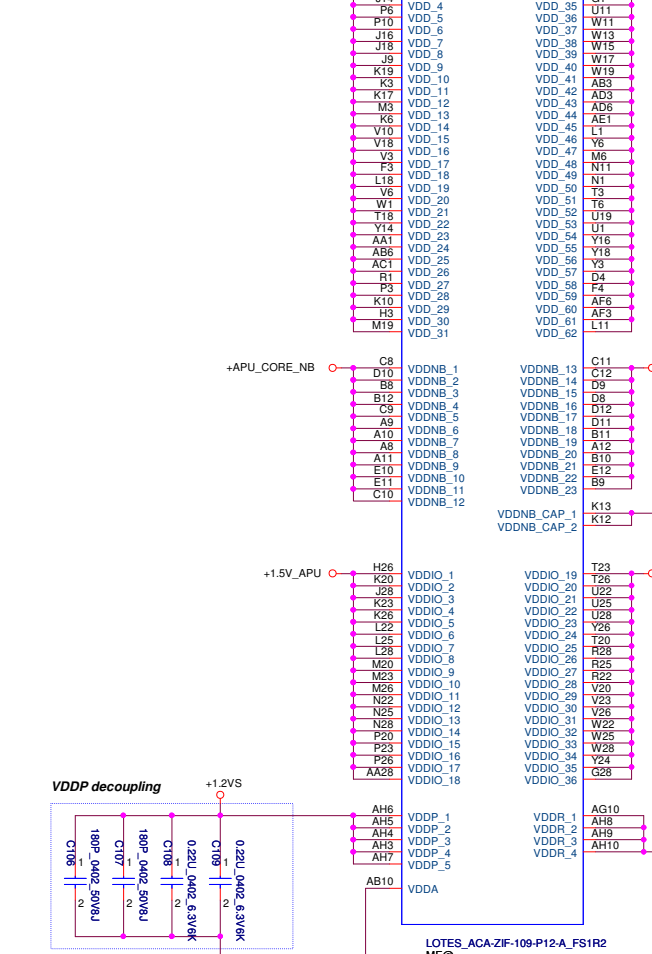
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				FS1r2 PCIE/UMI
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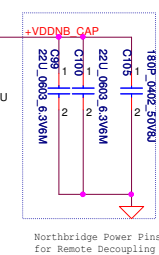
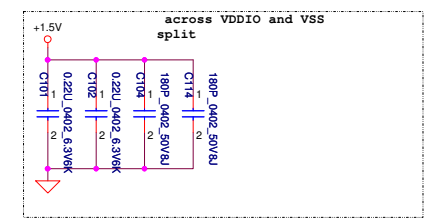
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Issued Date	2012/11/13	Deciphered Date	2013/11/12	FS1R2 DDRIII Memory I/F
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 FS1R2 DDRIII Memory I/F
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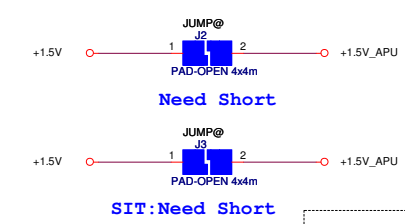
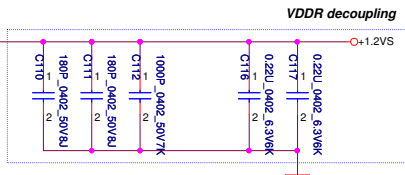
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



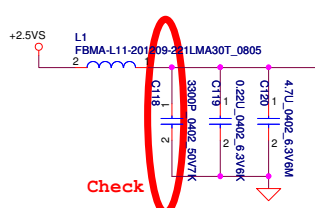
(330uF_6.3V_4.2L_ESR17m) *1=(SF000002Z00)



Northbridge Power Pins for Remote Decoupling



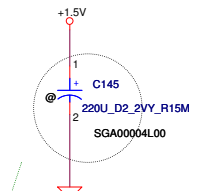
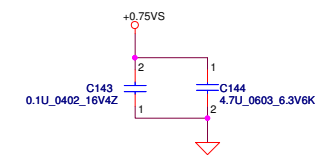
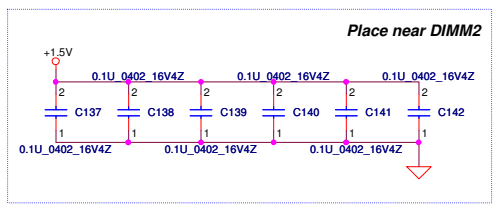
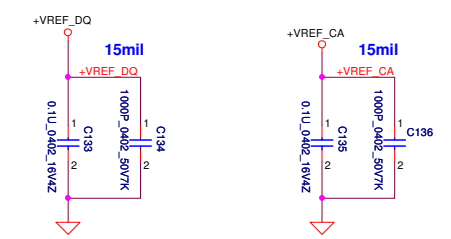
JCPUIF		
J20	VSS_1	VSS_73
L4	VSS_2	VSS_74
R7	VSS_3	VSS_75
W18	VSS_4	VSS_76
A15	VSS_5	VSS_77
AB17	VSS_6	VSS_78
AC22	VSS_7	VSS_79
AE21	VSS_8	VSS_80
AF24	VSS_9	VSS_81
AH23	VSS_10	VSS_82
AH25	VSS_11	VSS_83
B7	VSS_12	VSS_84
C14	VSS_13	VSS_85
C16	VSS_14	VSS_86
C2	VSS_15	VSS_87
C20	VSS_16	VSS_88
C22	VSS_17	VSS_89
C24	VSS_18	VSS_90
C26	VSS_19	VSS_91
C28	VSS_20	VSS_92
D13	VSS_21	VSS_93
D15	VSS_22	VSS_94
D17	VSS_23	VSS_95
D19	VSS_24	VSS_96
D23	VSS_25	VSS_97
D25	VSS_26	VSS_98
D27	VSS_27	VSS_99
E4	VSS_28	VSS_100
E9	VSS_29	VSS_101
F14	VSS_30	VSS_102
F16	VSS_31	VSS_103
F18	VSS_32	VSS_104
F20	VSS_33	VSS_105
F22	VSS_34	VSS_106
F26	VSS_35	VSS_107
F28	VSS_36	VSS_108
G13	VSS_37	VSS_109
G15	VSS_38	VSS_110
G17	VSS_39	VSS_111
G19	VSS_40	VSS_112
G21	VSS_41	VSS_113
G23	VSS_42	VSS_114
G25	VSS_43	VSS_115
G4	VSS_44	VSS_116
J22	VSS_45	VSS_117
J24	VSS_46	VSS_118
J4	VSS_47	VSS_119
J7	VSS_48	VSS_120
K11	VSS_49	VSS_121
K14	VSS_50	VSS_122
K9	VSS_51	VSS_123
K11	VSS_52	VSS_124
L19	VSS_53	VSS_125
L7	VSS_54	VSS_126
MT1	VSS_55	VSS_127
AF11	VSS_56	VSS_128
V19	VSS_57	VSS_129
V9	VSS_58	VSS_130
W4	VSS_59	VSS_131
W7	VSS_60	VSS_132
Y11	VSS_61	VSS_133
Y20	VSS_62	VSS_134
Y22	VSS_63	VSS_135
Y9	VSS_64	VSS_136
A17	VSS_65	VSS_137
A13	VSS_66	VSS_138
K16	VSS_67	VSS_139
F24	VSS_68	VSS_140
H7	VSS_69	VSS_141
G8	VSS_70	VSS_142
J8	VSS_71	VSS_143
J8	VSS_72	VSS_144



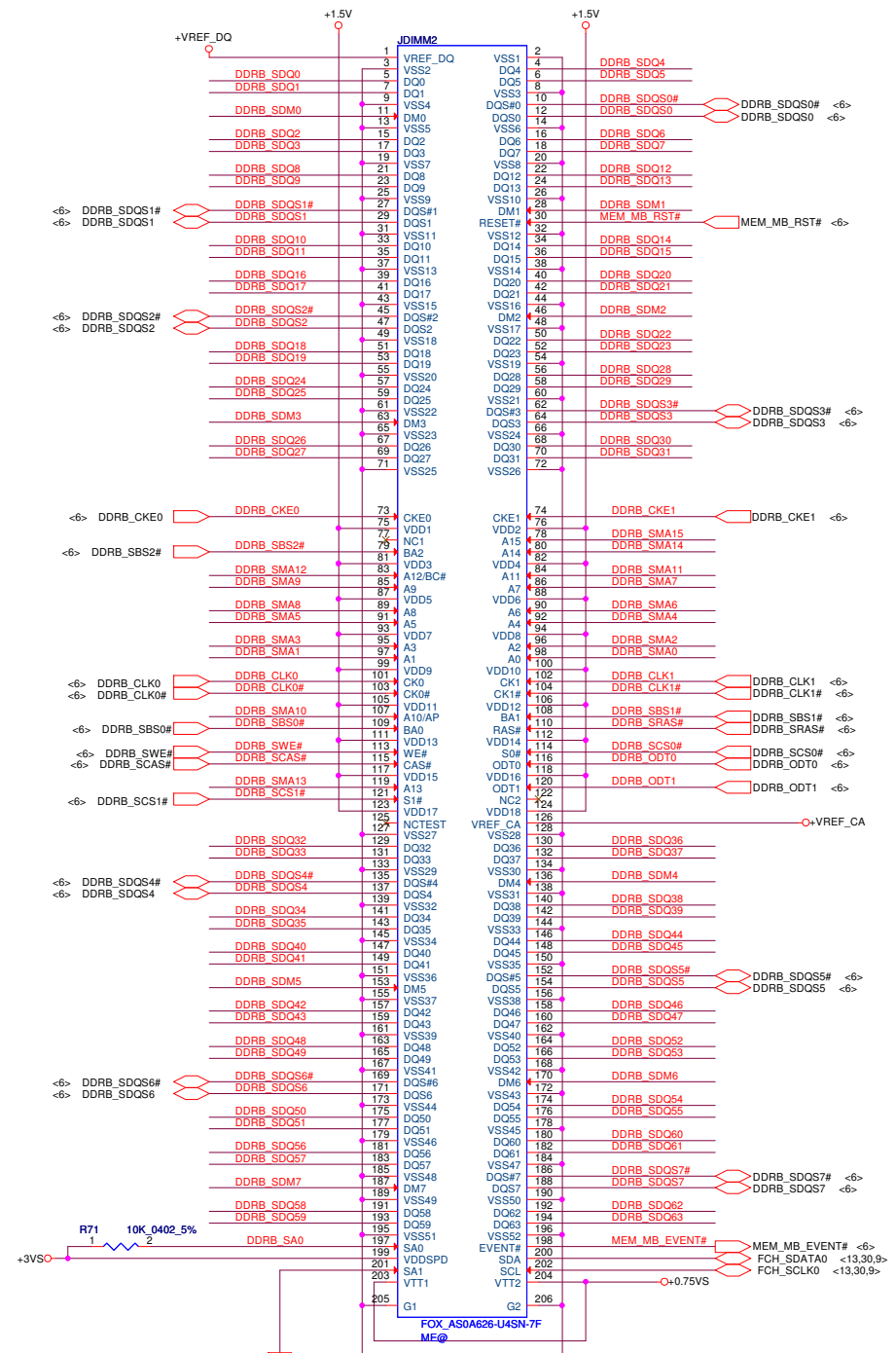
Check

Demo Board Capacitor			
APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

— DDRB_SDO[0..63] DDRB_SDO[0..63] <6>
— DDRB_SDM[0..7] DDRB_SDM[0..7] <6>
— DDRB_SMA[0..15] DDRB_SMA[0..15] <6>

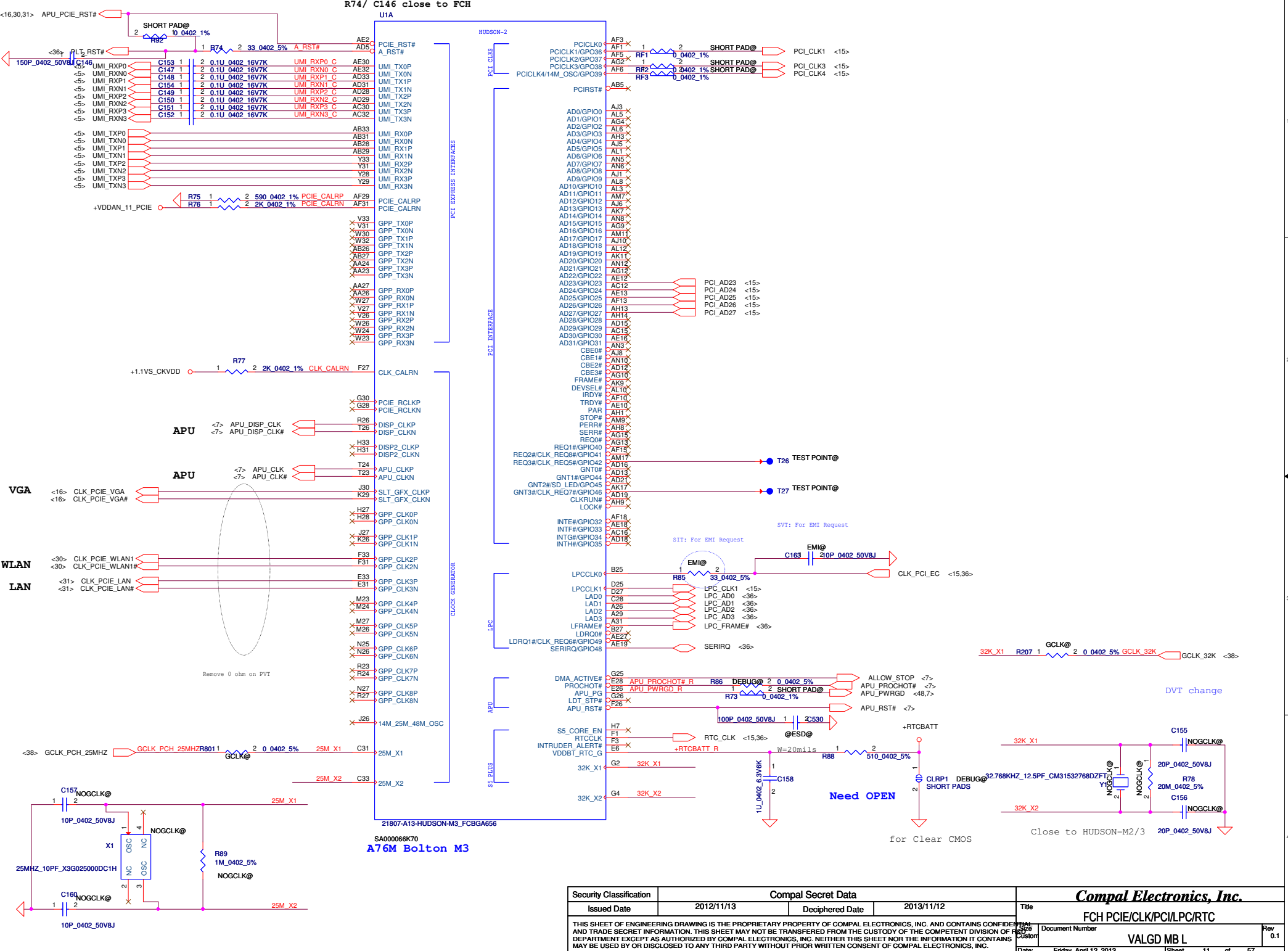


SIT:1/26 change to POLY



Standard H:4mm
 <Address: 01>

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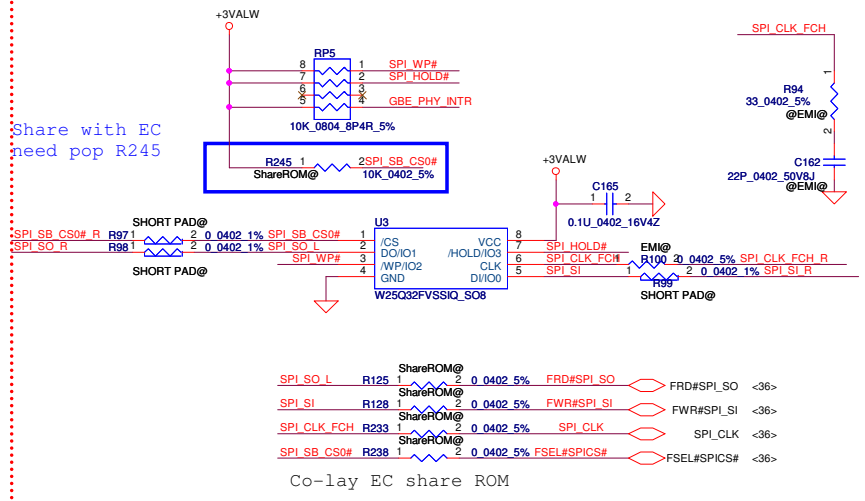
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Compal Electronics, Inc.	
FCH PCIE/CLK/PCI/LPC/RTC	
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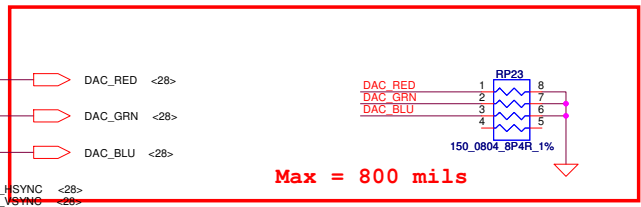
Rev 0.1

4MB SPI ROM

Share with EC
need pop R245



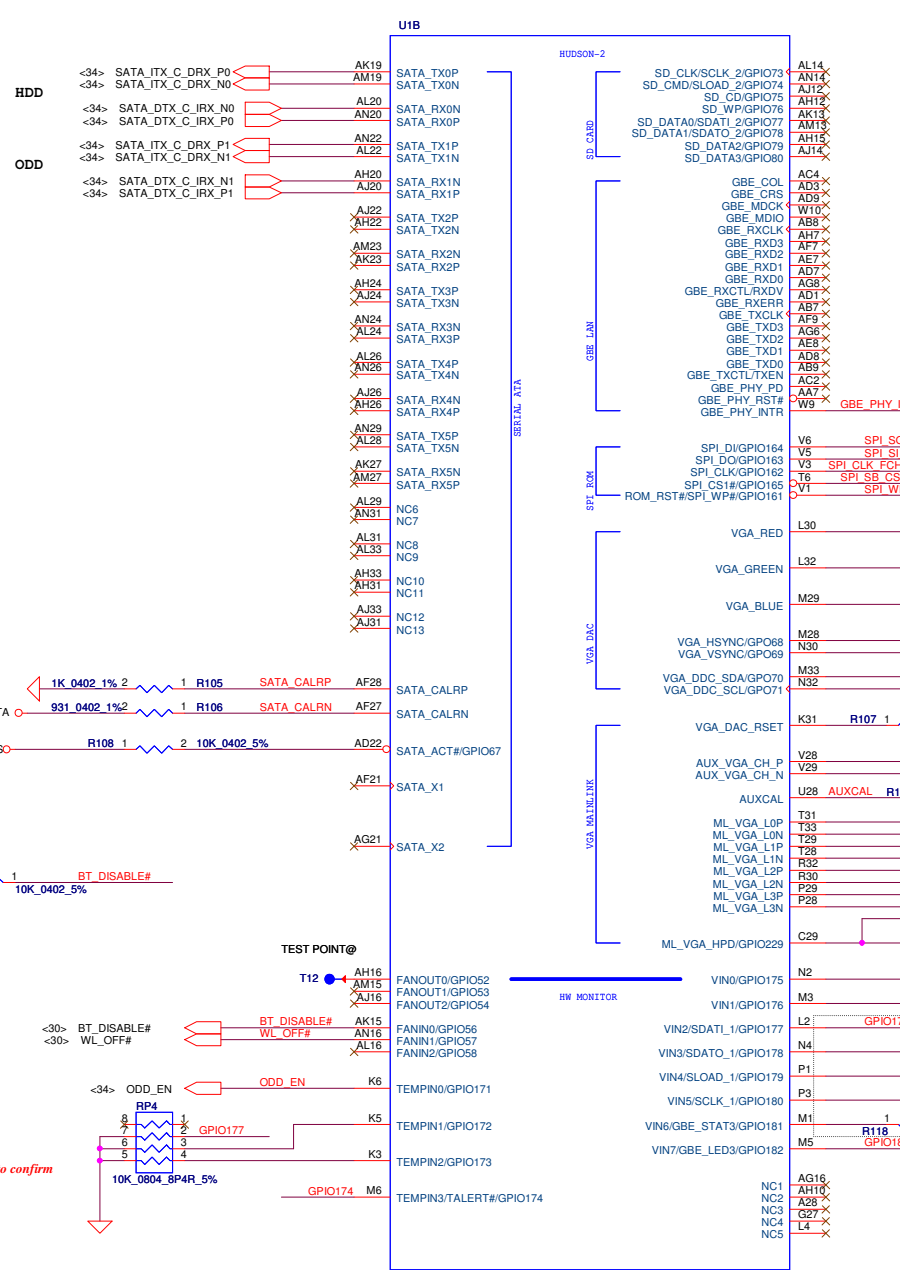
Co-layer EC share ROM



Max = 800 mils

Module design FCH_CRT_HPD pull up 110K now 10 K

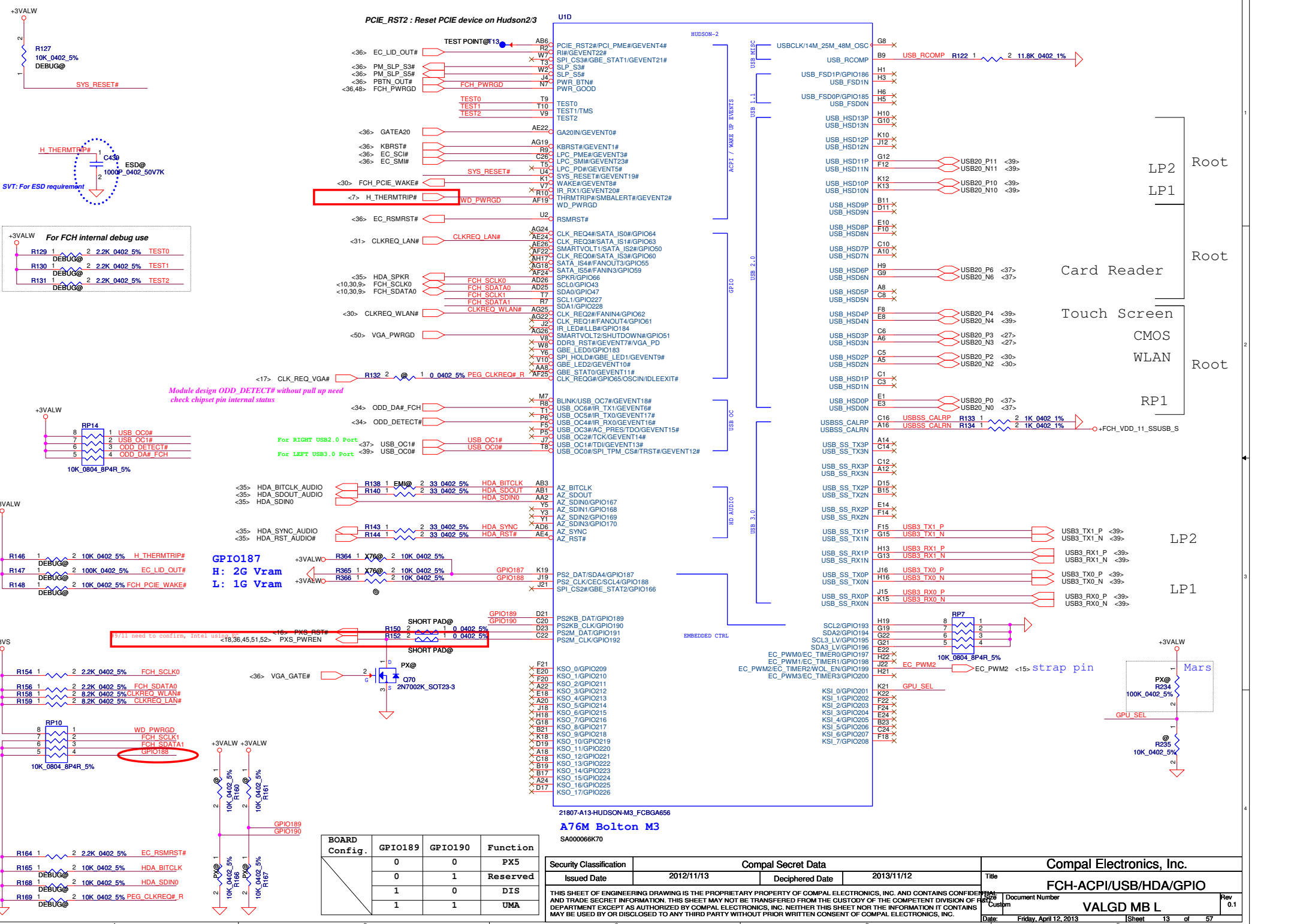
Need to enable internal pull down to leave unconnected



#117: without pull up/down need to confirm or check chipset pin internal status

21807.A13-HUDSON-M3_FCBGA656
SA000068K70
A76M Bolton M3

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Issued Date	2012/11/13	Deciphered Date	2013/11/12	FCH SATA/SPI/VGA/HWM/SD
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VALGD MB L			Rev	0.1
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PCIE_RST2 : Reset PCIE device on Hudson2/3

UID

HUDSON-2

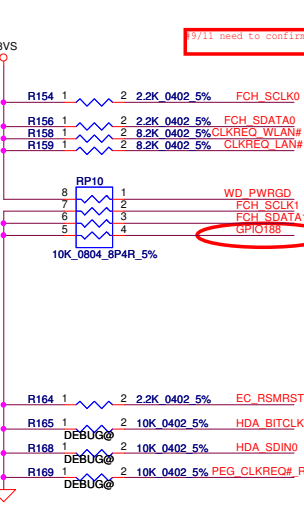
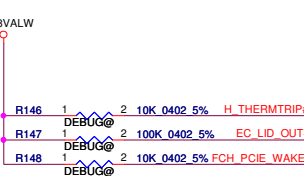
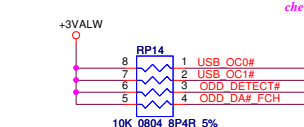
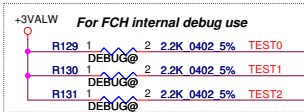
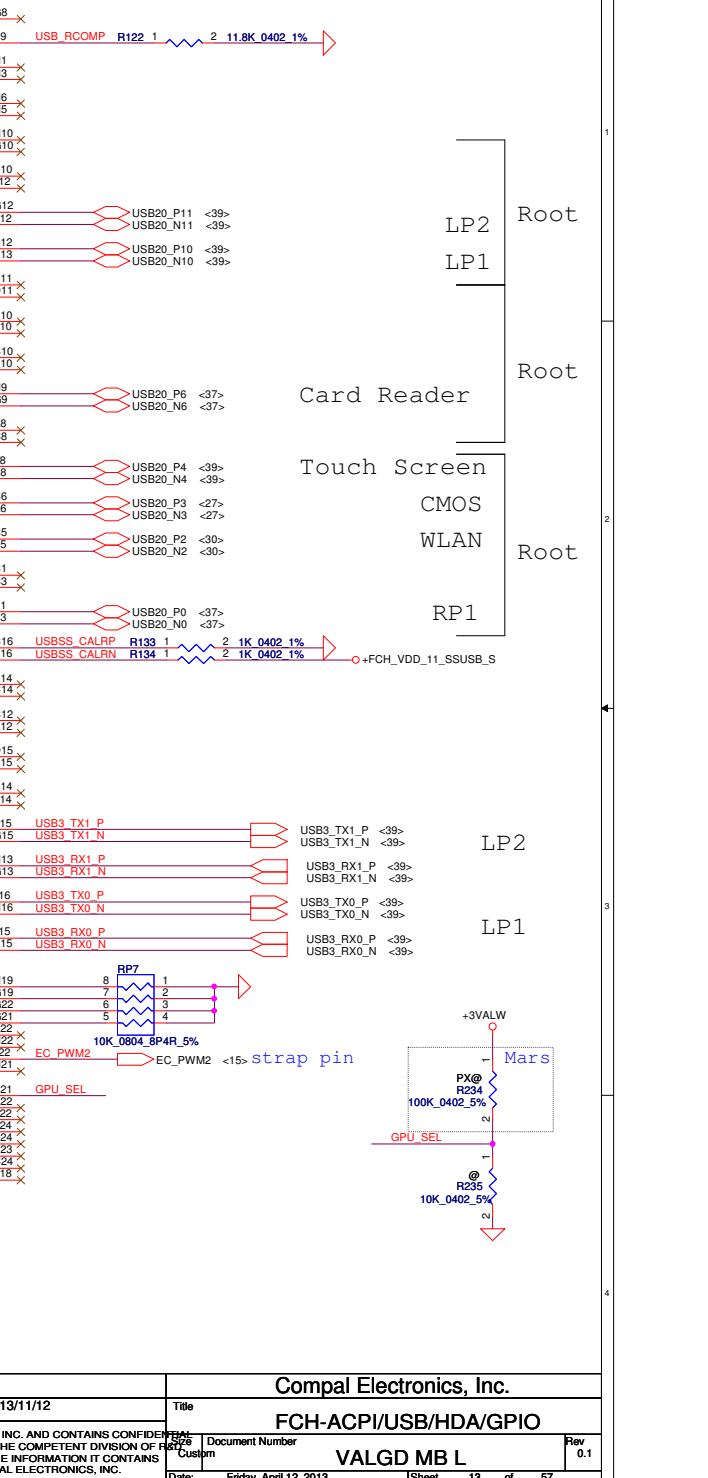
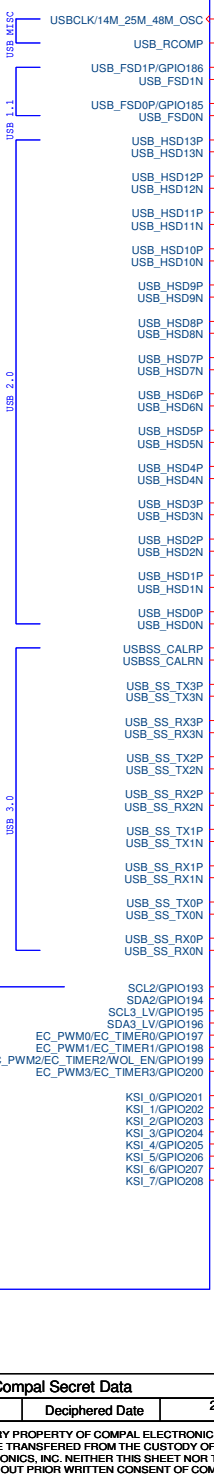
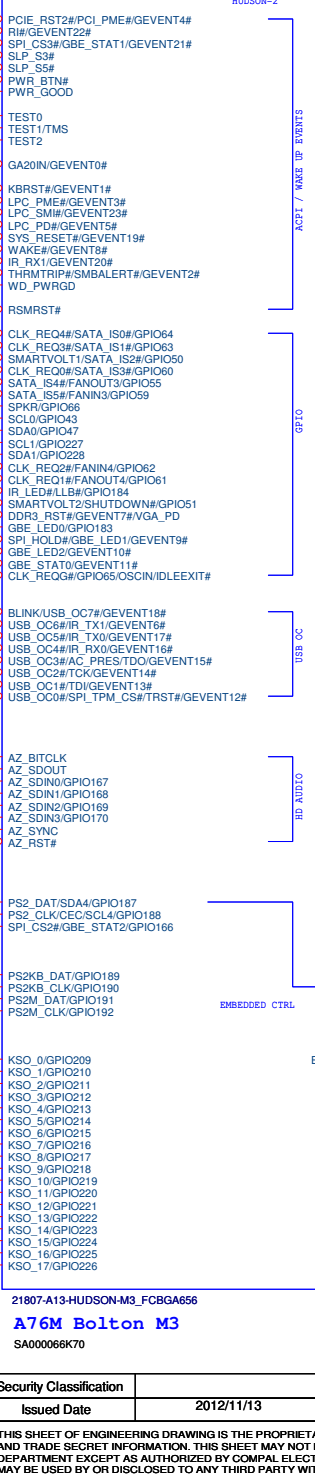
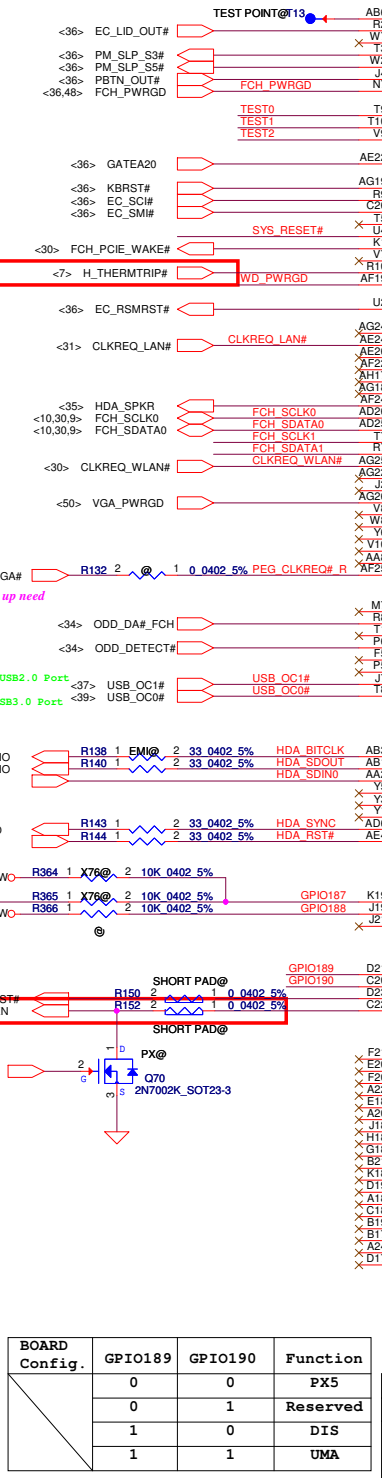
USB

GPIO

USB OC

HD AUDIO

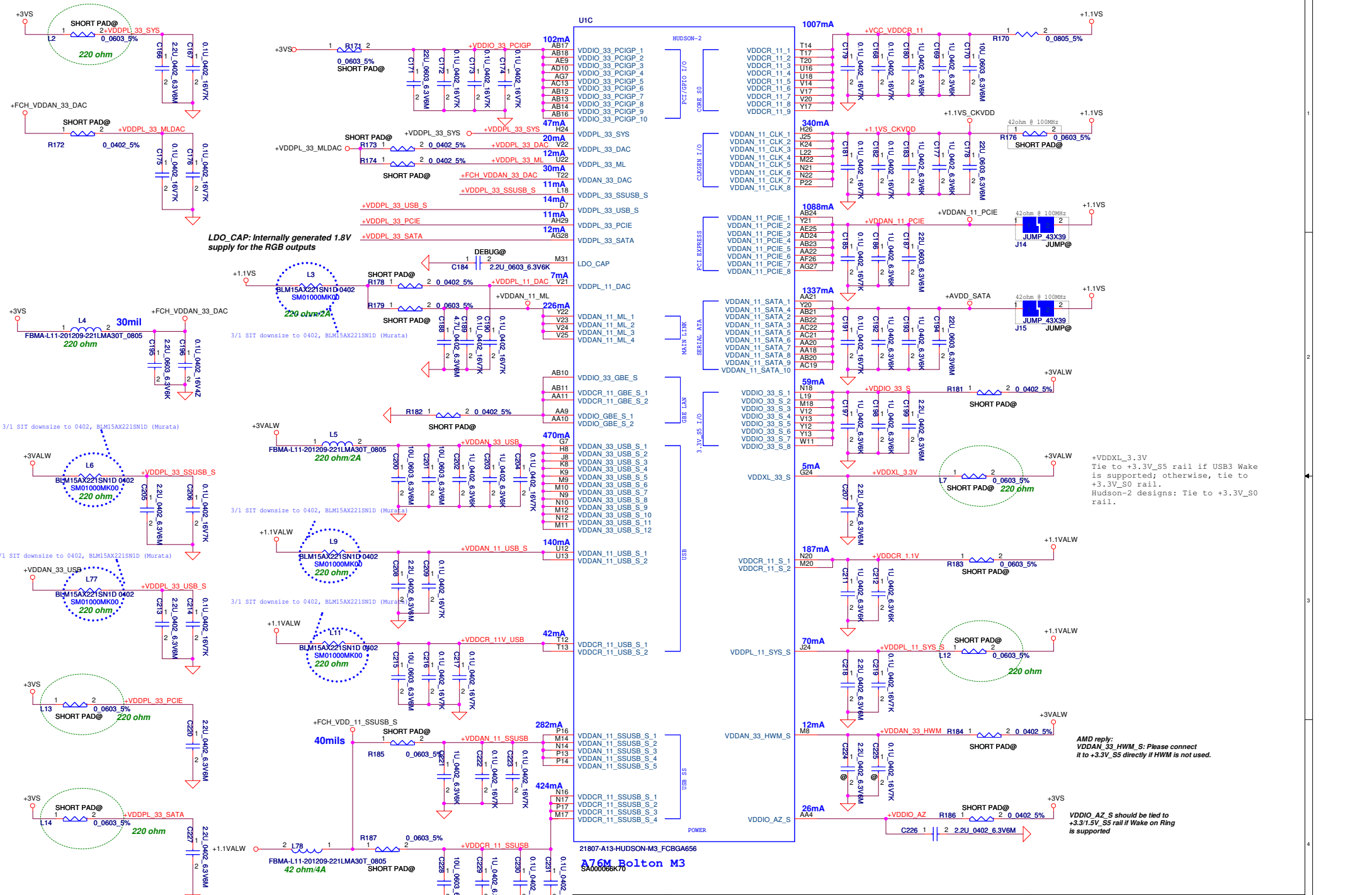
EMBEDDED CTRL



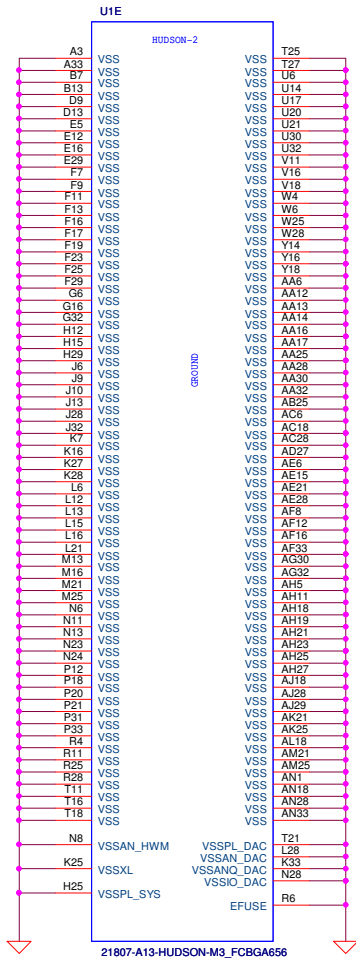
BOARD Config.	GPIO189	GPIO190	Function
	0	0	PX5
	0	1	Reserved
	1	0	DIS
	1	1	UMA

21807-A13-HUDSON-M3_FCBGA656
A76M Bolton M3
 SA00066K70

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<p>Compal Electronics, Inc. FCH-ACPI/USB/HDA/GPIO</p>			<p>Customer VALGD MB L Rev 0.1</p>	
<p>Page 13 of 57</p>				



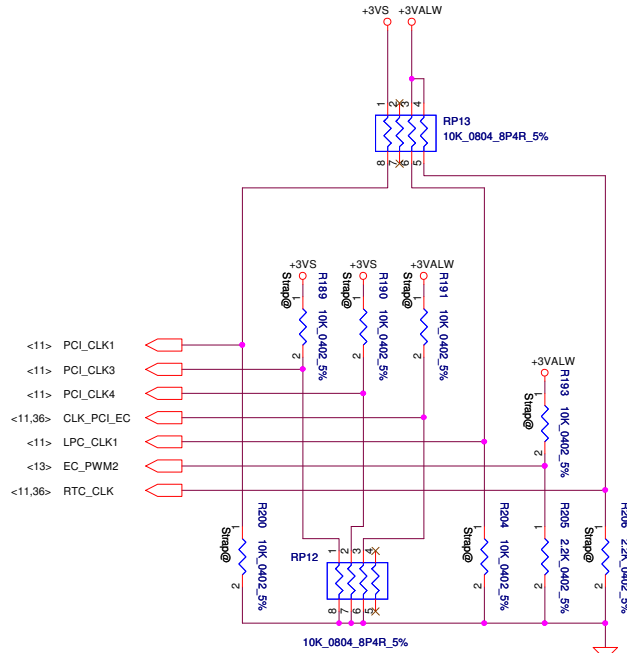
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				Date: Friday, April 12, 2013	Sheet 14 of 57



A76M Bolton M3
SA000066K70

STRAP PINS

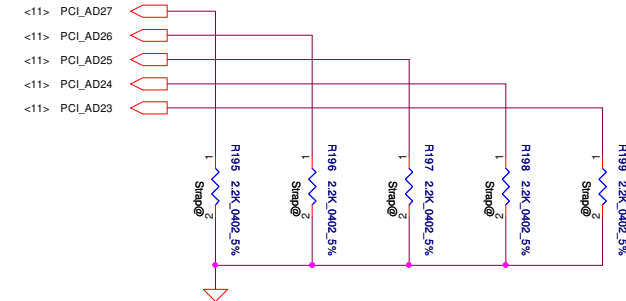
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCI GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCI GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



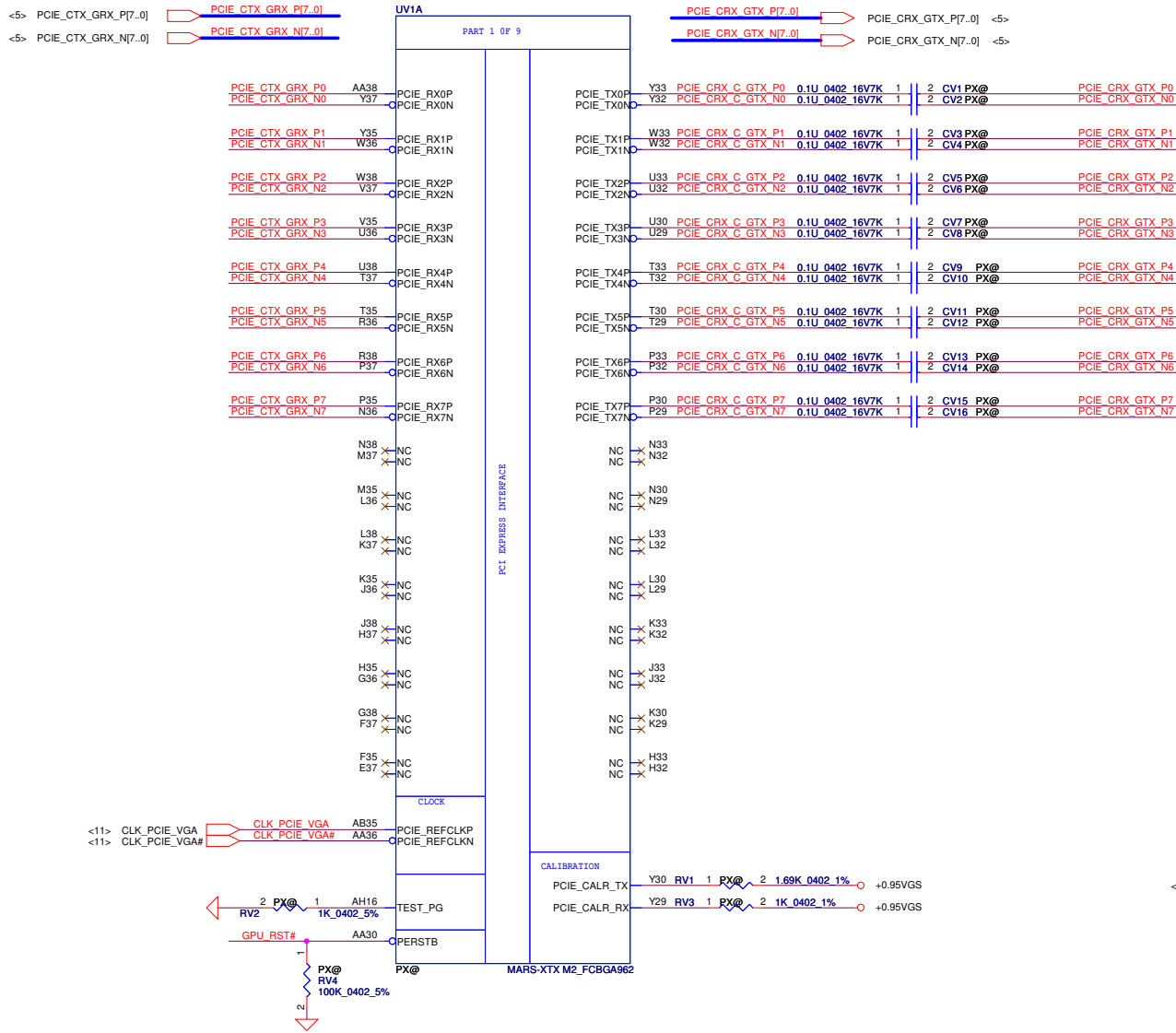
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

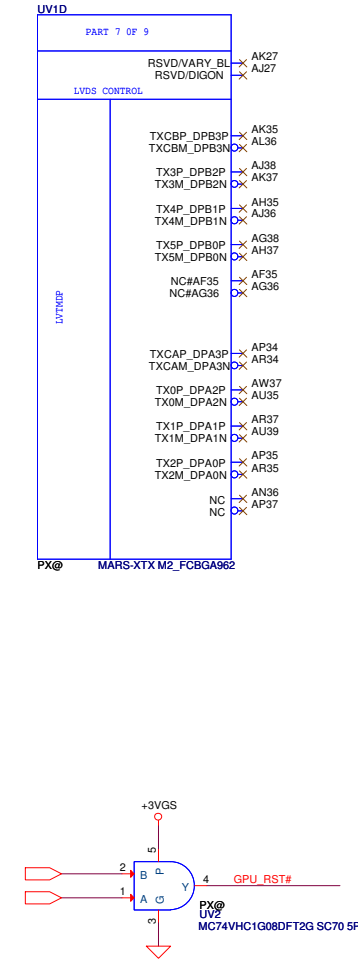
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



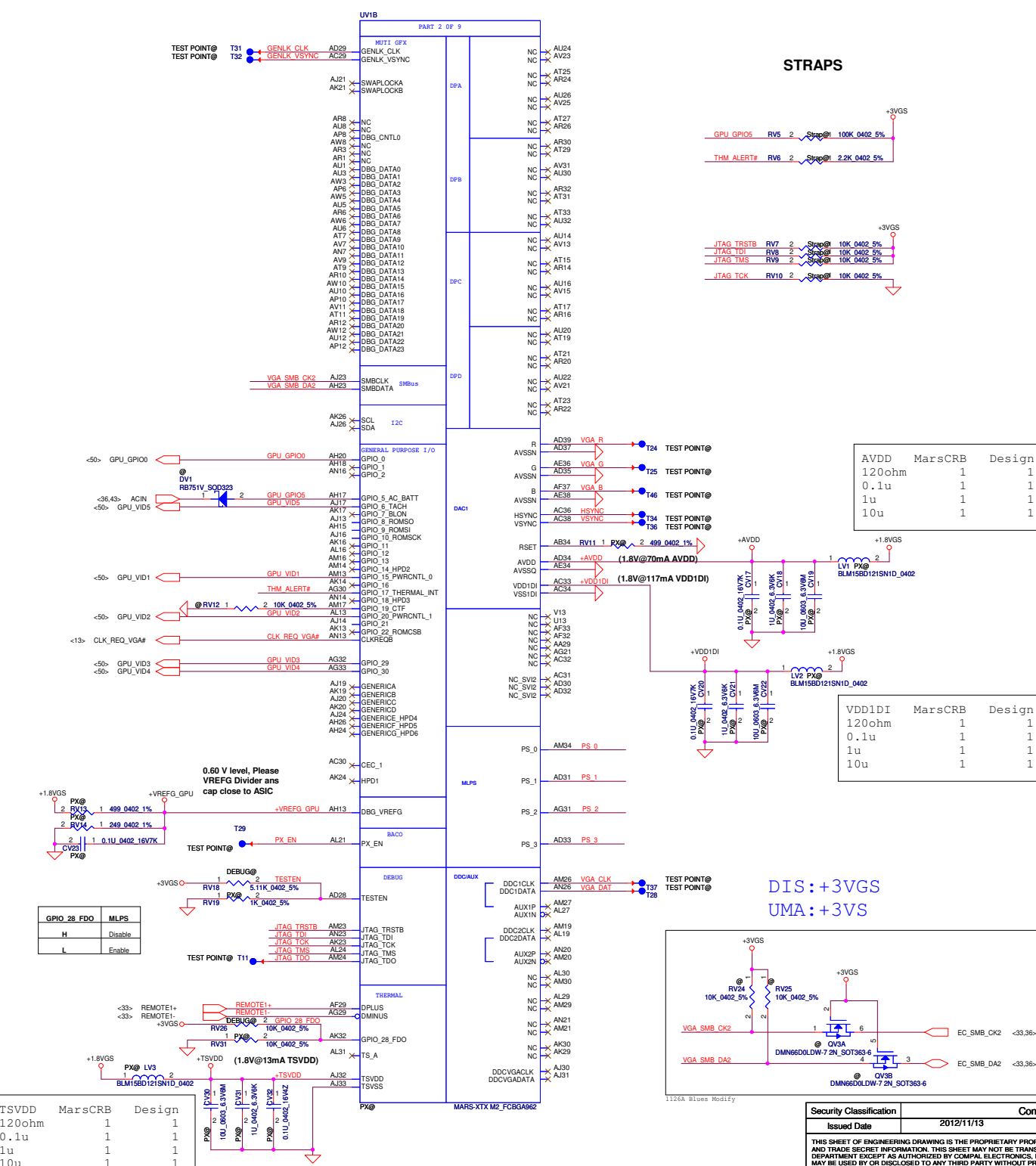
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Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title
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LVDS Interface



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				Rev 0.1 Sheet 16 of 57



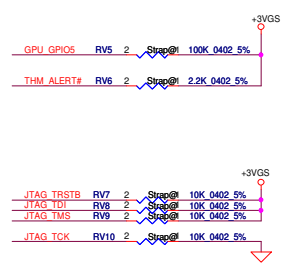
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X= DESIGN DEPENDANT
 NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRFS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M2SP05A (ST) 101 - 1Mbit M2SP10A (ST) 101 - 2Mbit M2SP20 (ST) 101 - 4Mbit M2SP40 (ST) 101 - 8Mbit M2SP80 (ST) 100 - 512Kbit Pm2SLV010 (Chingis) 101 - 1Mbit Pm2SLV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1]	NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
RESERVED	PS_1[3]	NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 - 0 usable endpoints 110 - 1 usable endpoints 101 - 2 usable endpoints 100 - 3 usable endpoints 011 - 4 usable endpoints 010 - 5 usable endpoints 001 - 6 usable endpoints 000 - all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

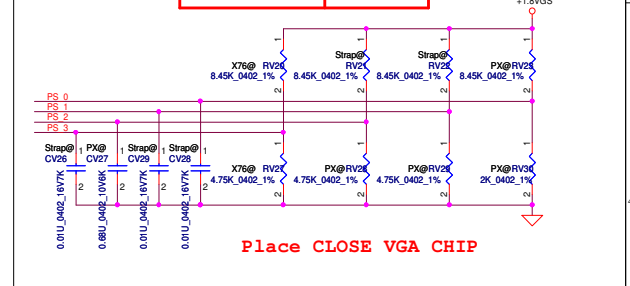
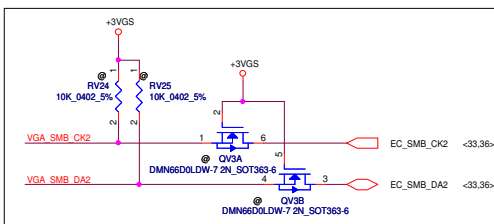
VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

MLPS Strap

Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K 2K
PS_1[5:1]	1 1	0 0 0	NC	NC 4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC 4.75K
PS_3[5:1]	1 1	X X X	NC	X X

Mapping to VRAM type please refer to page 21

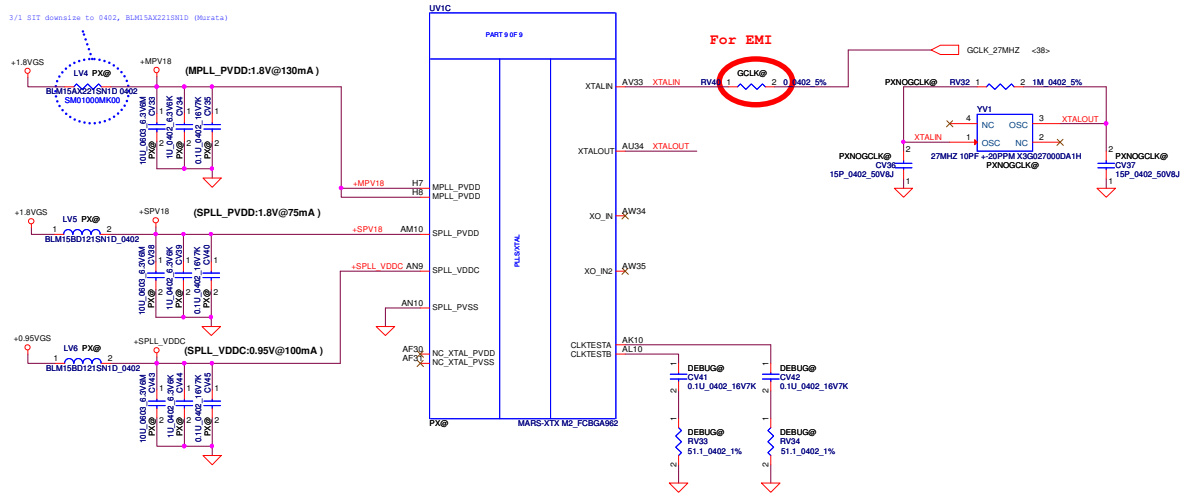
DIS: +3VGS
 UMA: +3VS



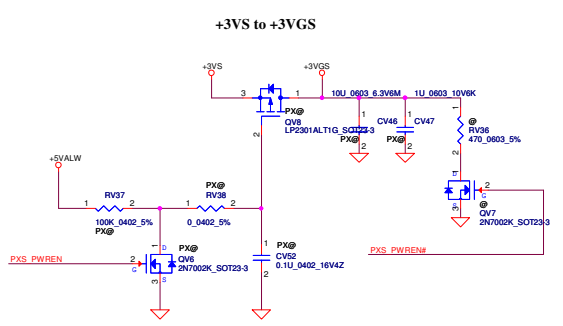
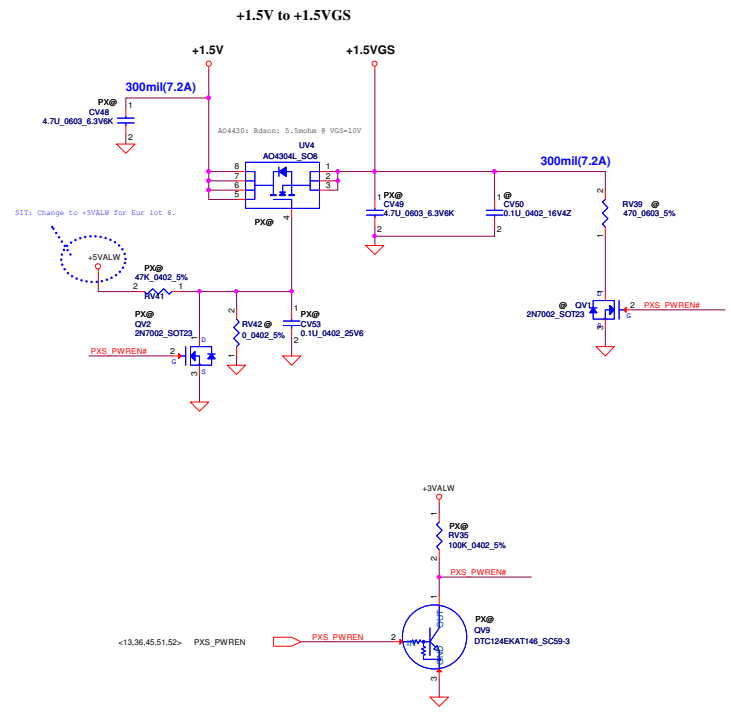
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



#9/11 need to confirm w/ Power team



SIT : 220U 4V Y D2 ESR15M = SGA00000Y80

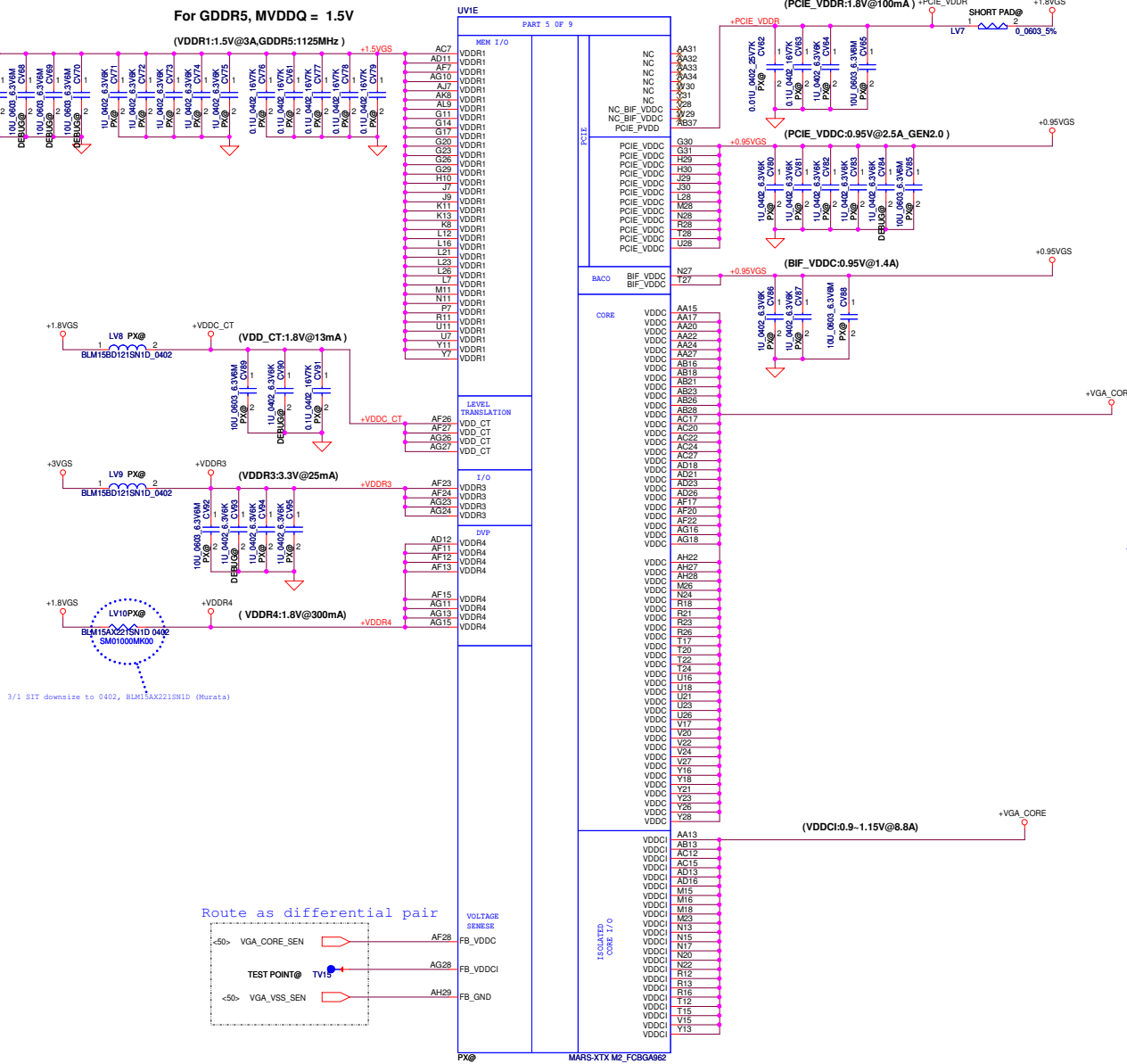
For GDDR5, MVDDQ = 1.5V
(VDDR1:1.5V@3A,GDDR5:1125MHz)

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

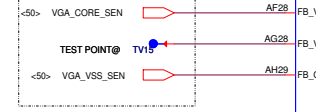
VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



3/1 SIT downside to 0402, BLM15AX221SN1D (Murata)

Route as differential pair



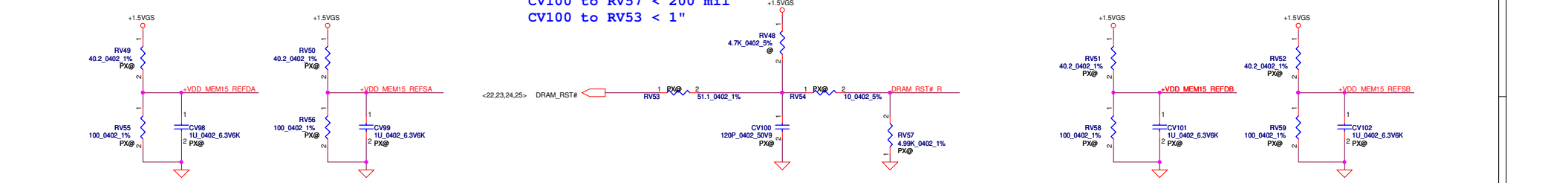
PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA_CORE Cap in power side sheet

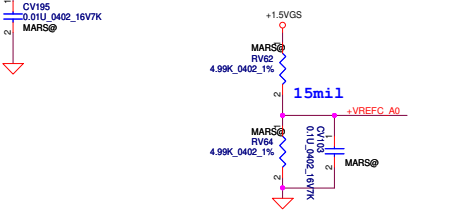
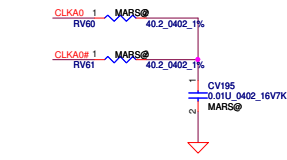
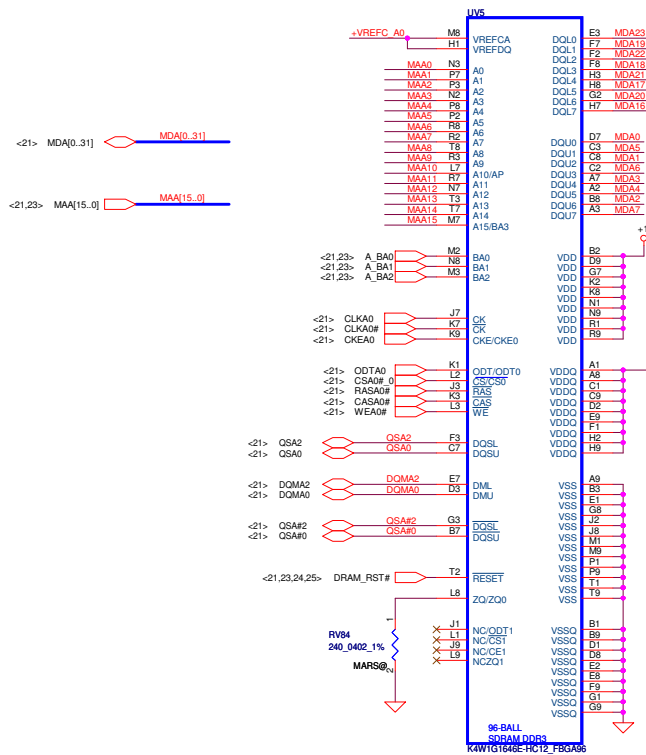


Ball to RV57 < 1"
 CV100 to RV57 < 200 mil
 CV100 to RV53 < 1"

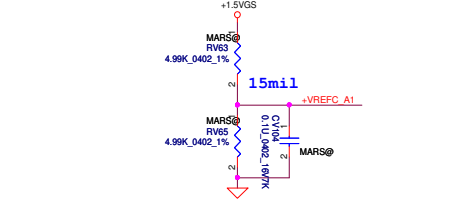
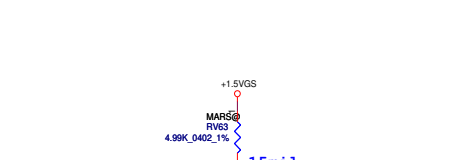
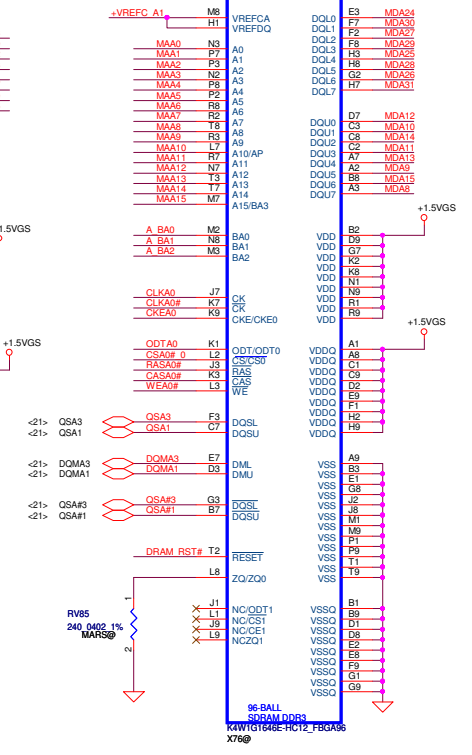


DRAM_RST# is a daisy-chain net that connects to all VRAM
 This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and |I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.
 Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

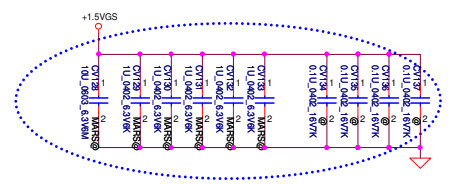
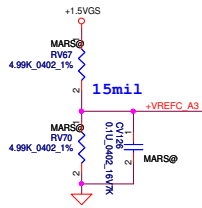
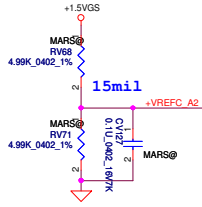
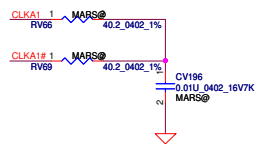
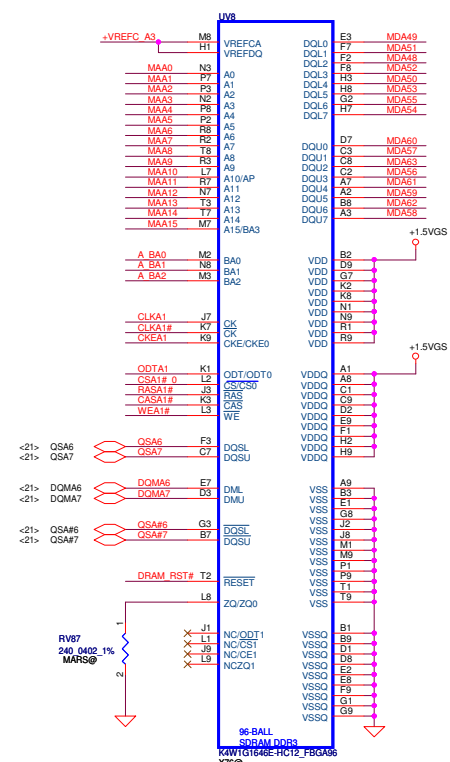
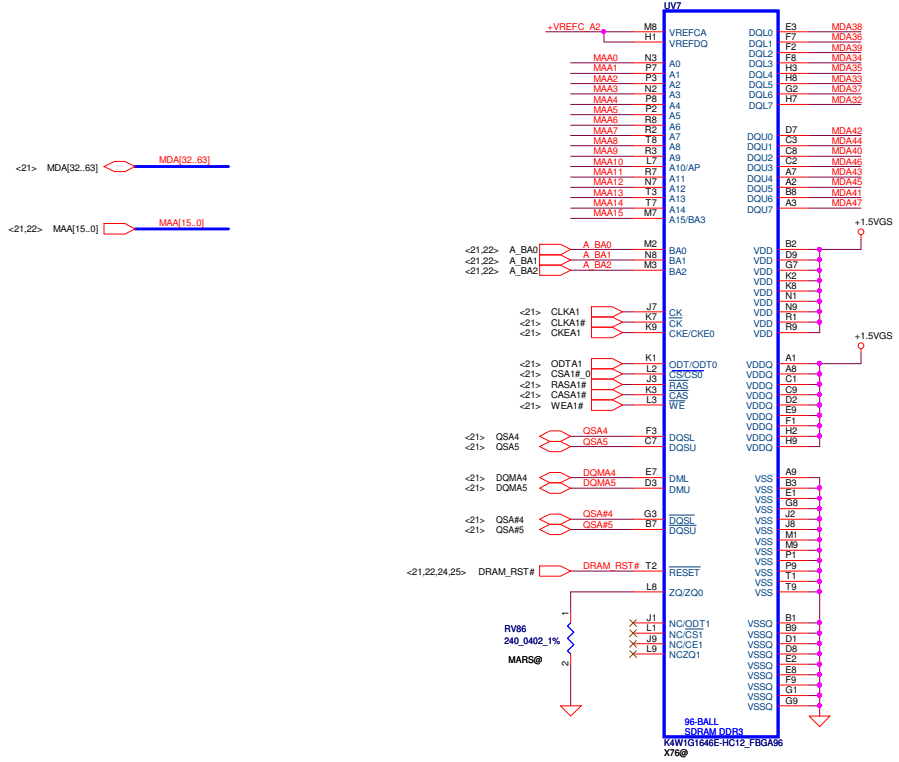
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Size	Document Number	VALGD MB L		Rev 0.1
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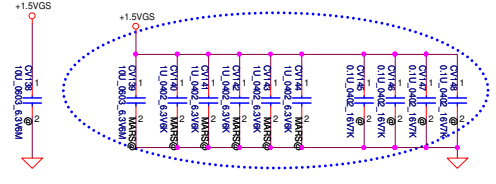
SIT: Placed close to the UV5



SIT: Placed close to the UV6

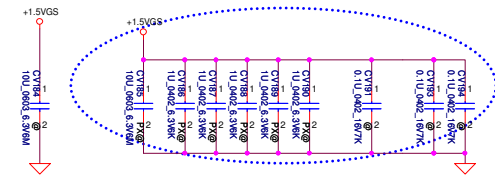
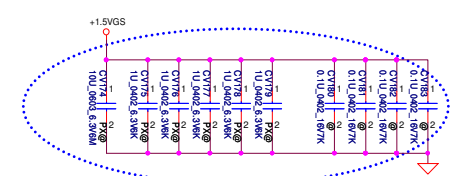
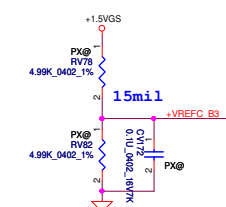
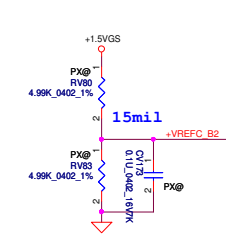
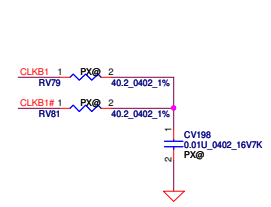
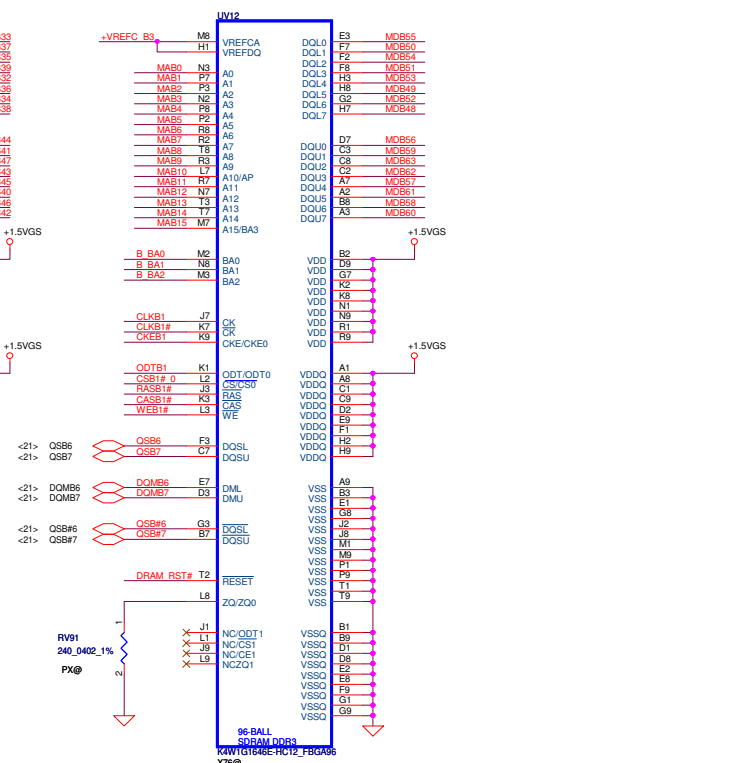
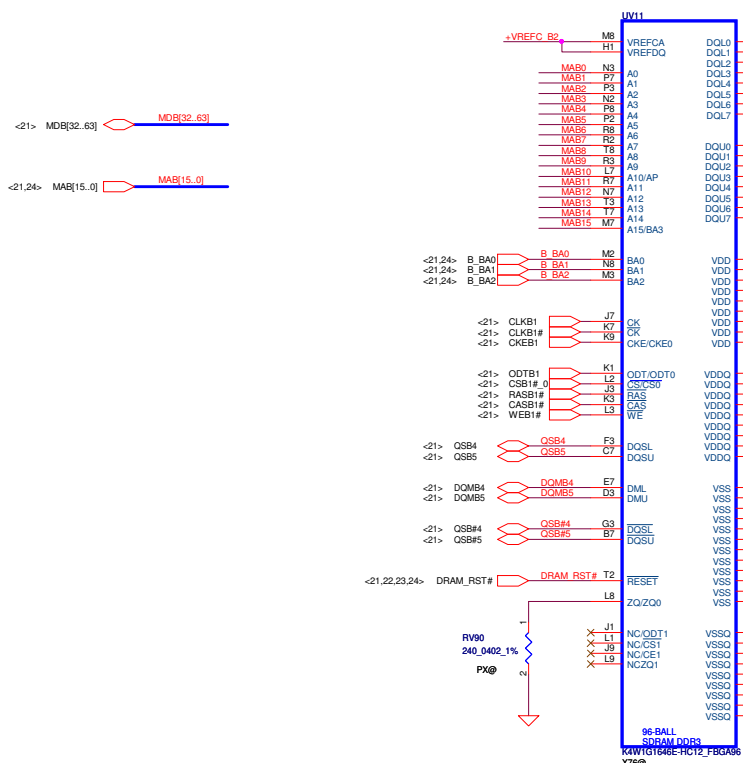


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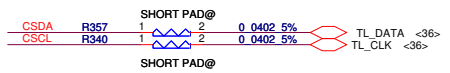
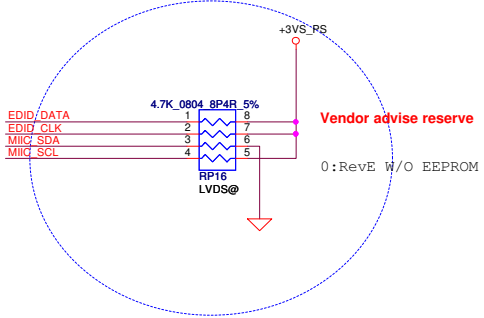
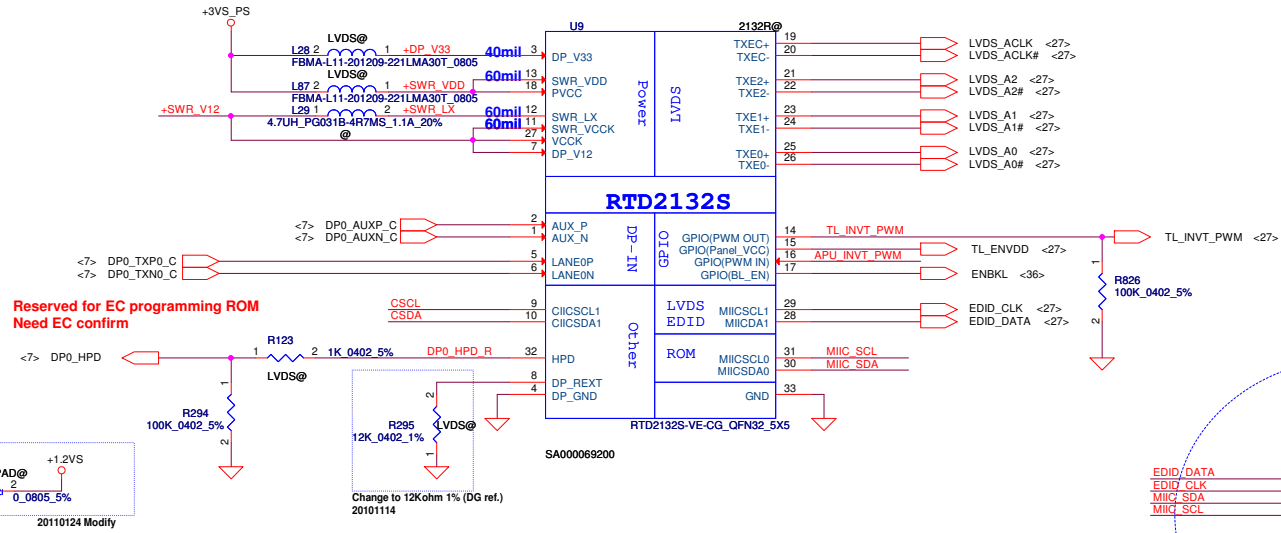
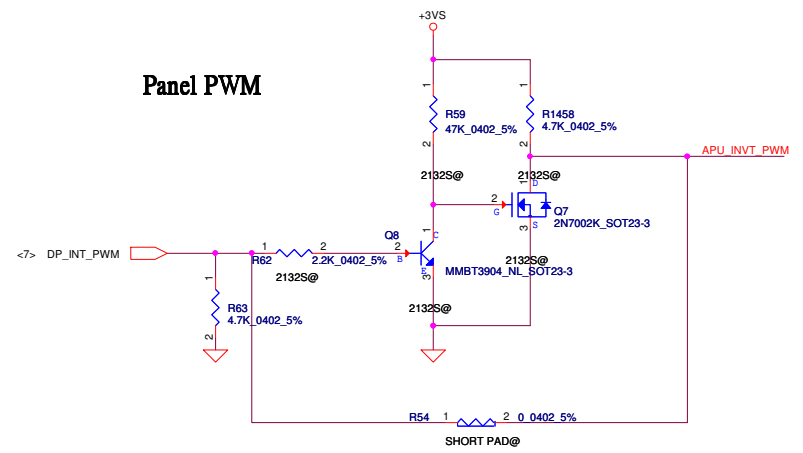
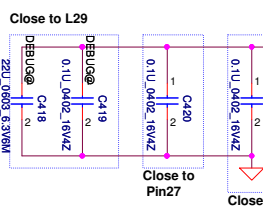
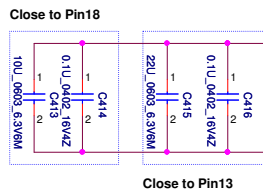
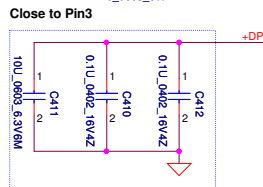
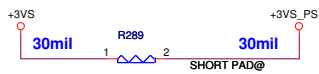


SIT: Placed close to the UV8

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Size	C	Document Number	VALGD MB L	Rev
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Size	C	Document Number	VALGD MB L
Date:	Friday, April 12, 2013	Sheet	25 of 57

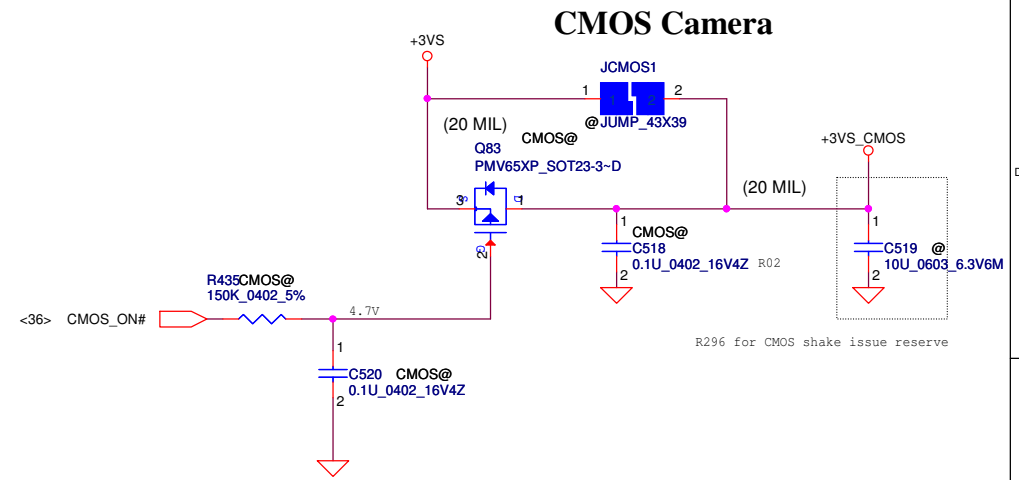
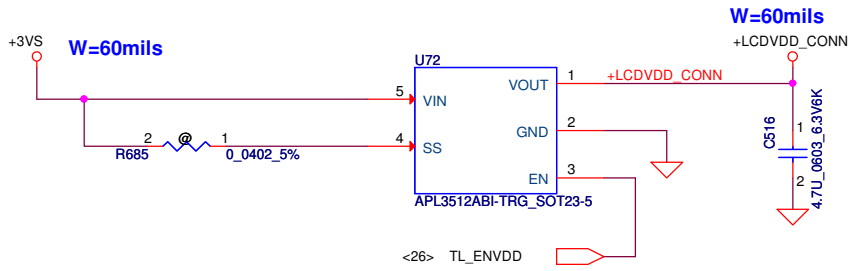


Panel PWM

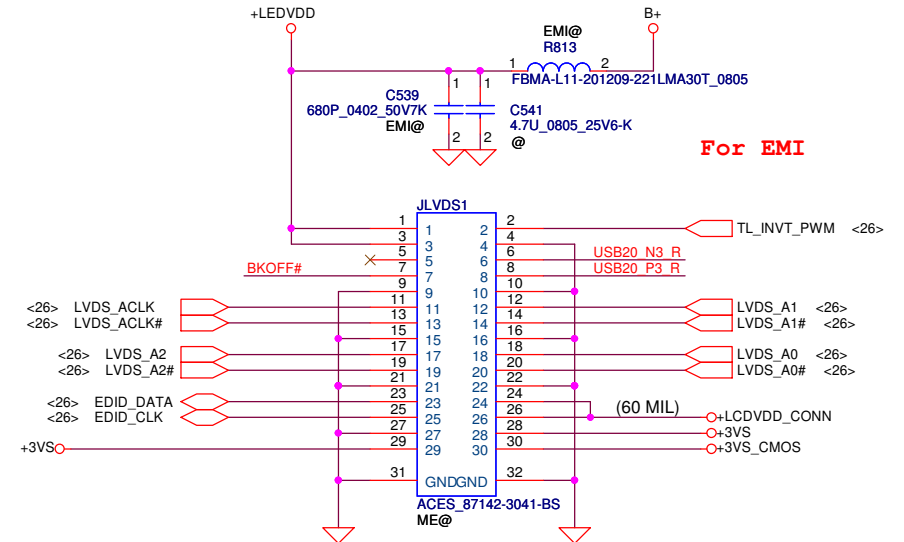
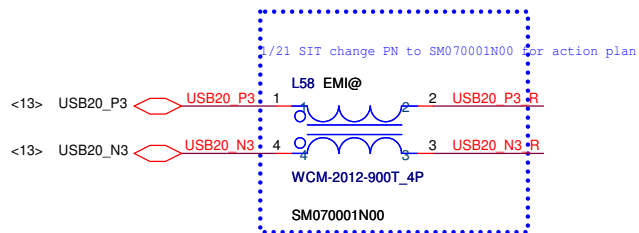
3/1: SIT

Config.	SDA/Pin#30	SCL/Pin#31	Function
0	0	0	Reserved
0	1	1	Internal mode 2132s
1	0	0	EP mode 2132s
1	1	1	Reserved

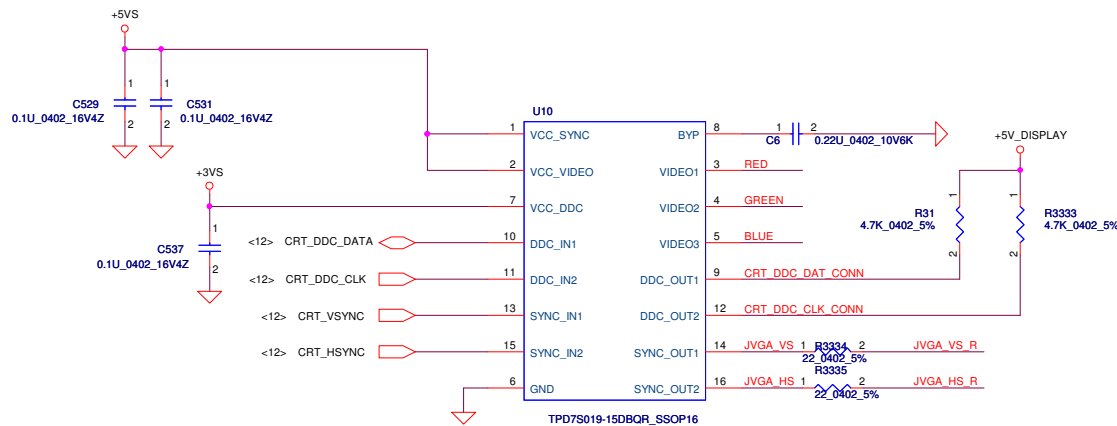
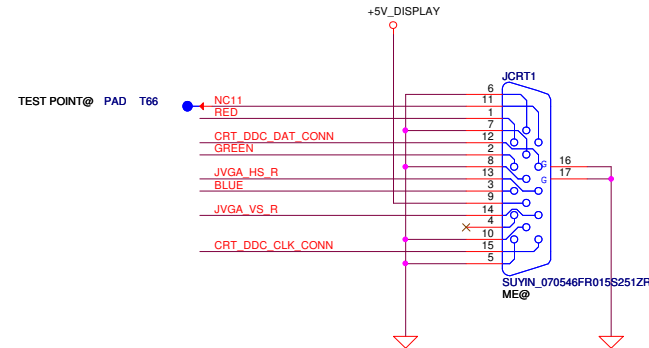
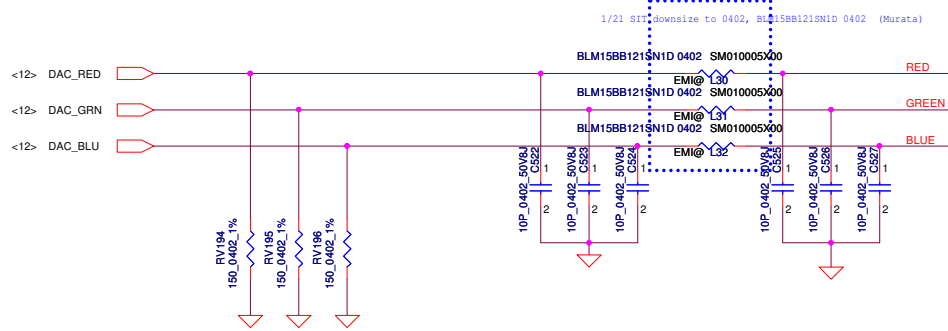
LCD POWER CIRCUIT



VGA LCD/PANEL BD. Conn.



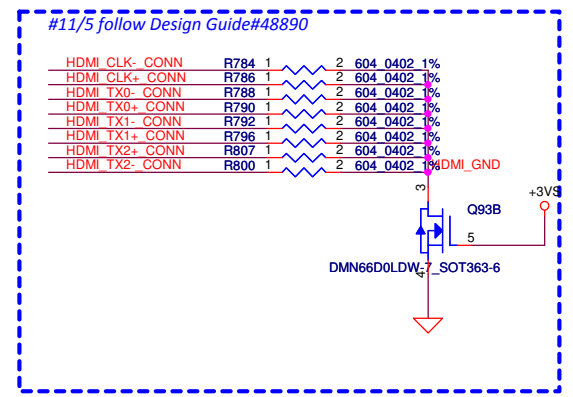
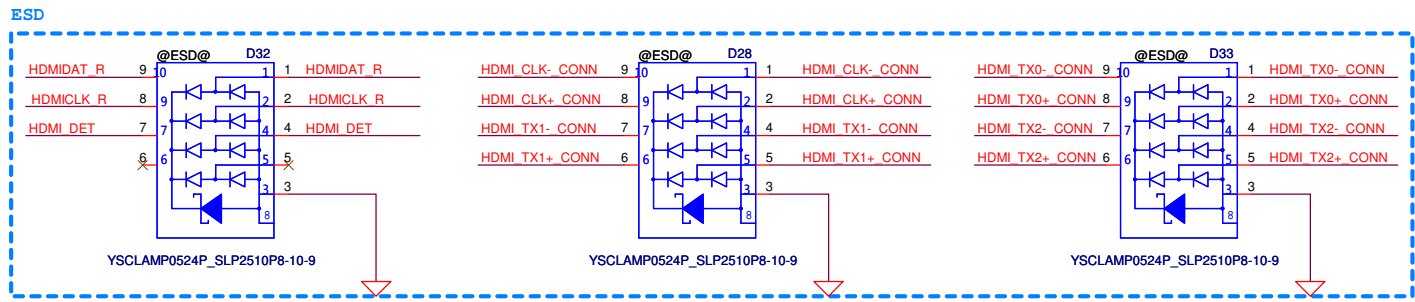
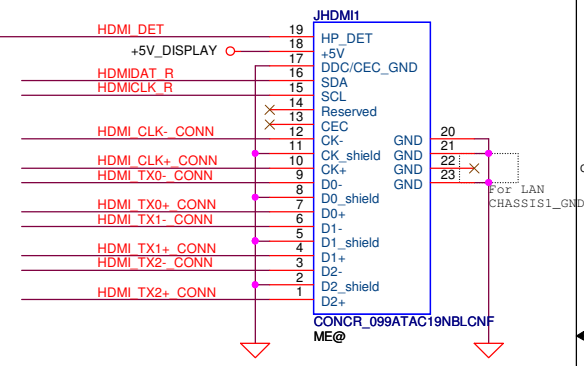
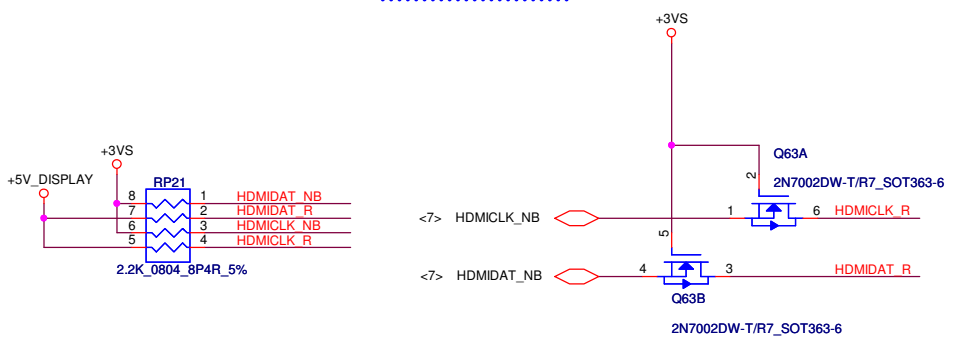
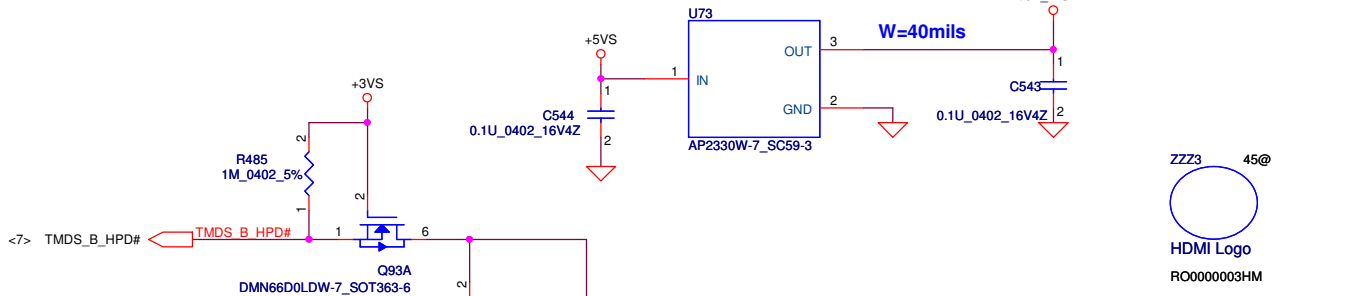
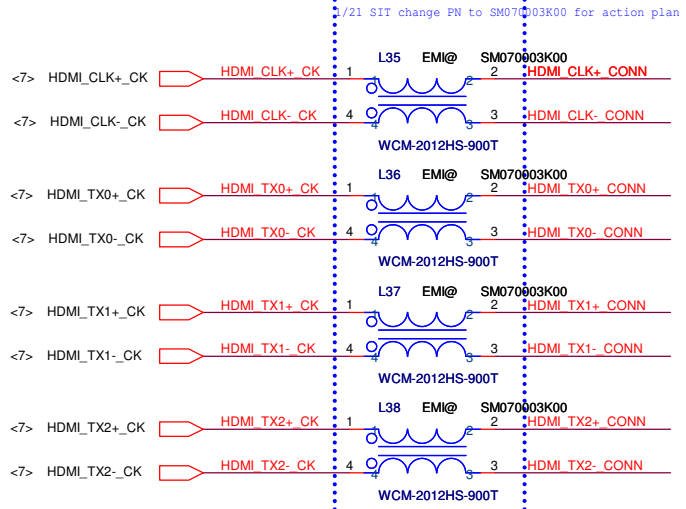
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				Date: Friday, April 12, 2013		Sheet 28 of 57

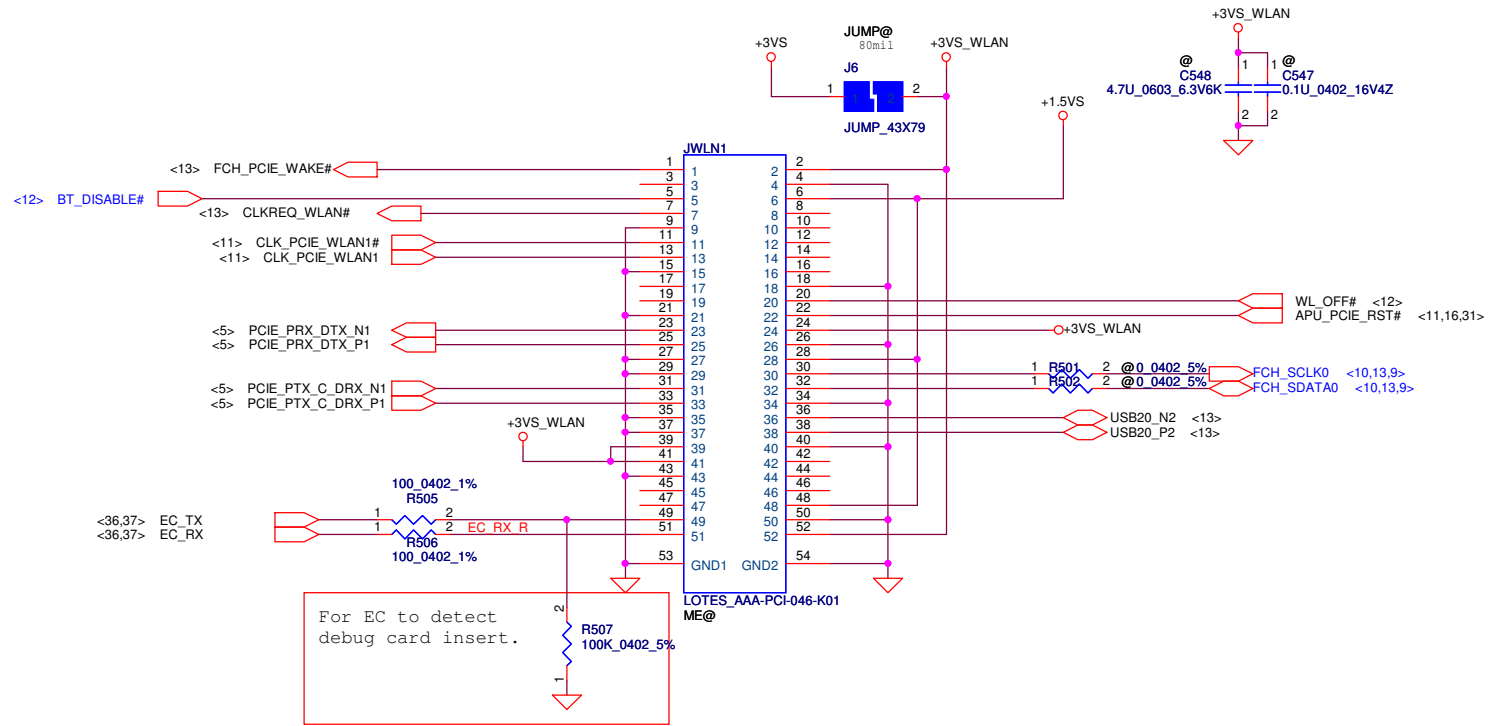
CRT Connector

VALGD MB L



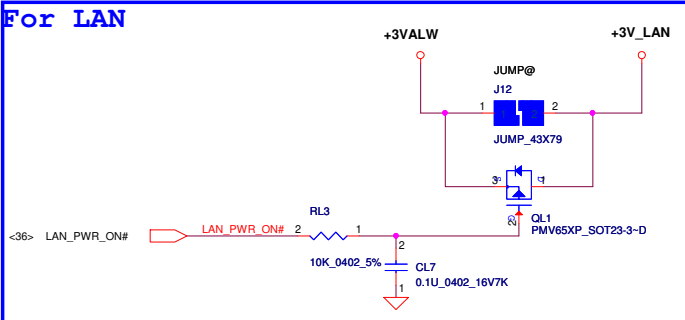
Security Classification	Compal Secret Data		Title	
Issued Date	2012/11/13	Deciphered Date	2013/11/12	HDMI CONN
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Mini-Express Card for WLAN/WiMAX(Half)

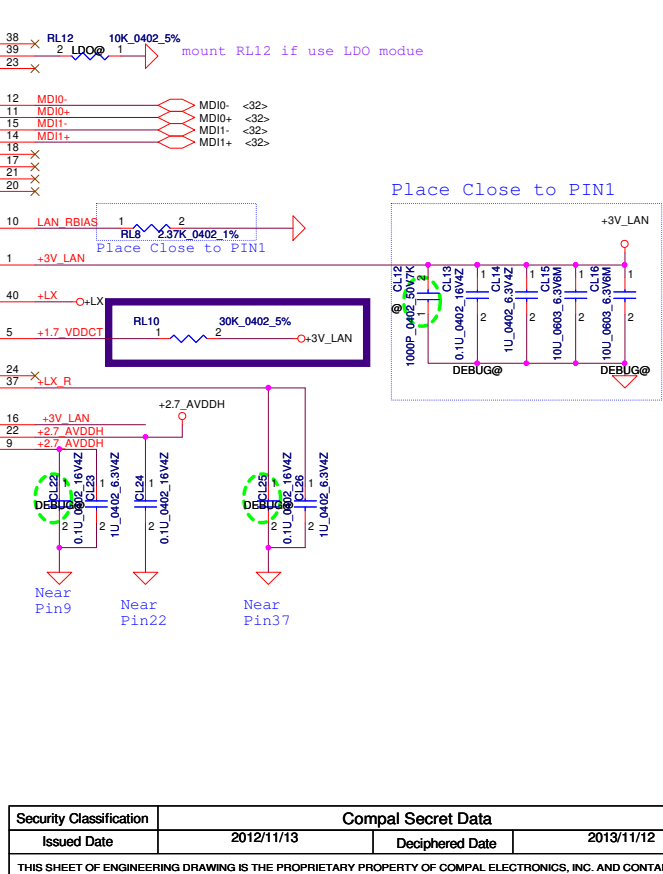
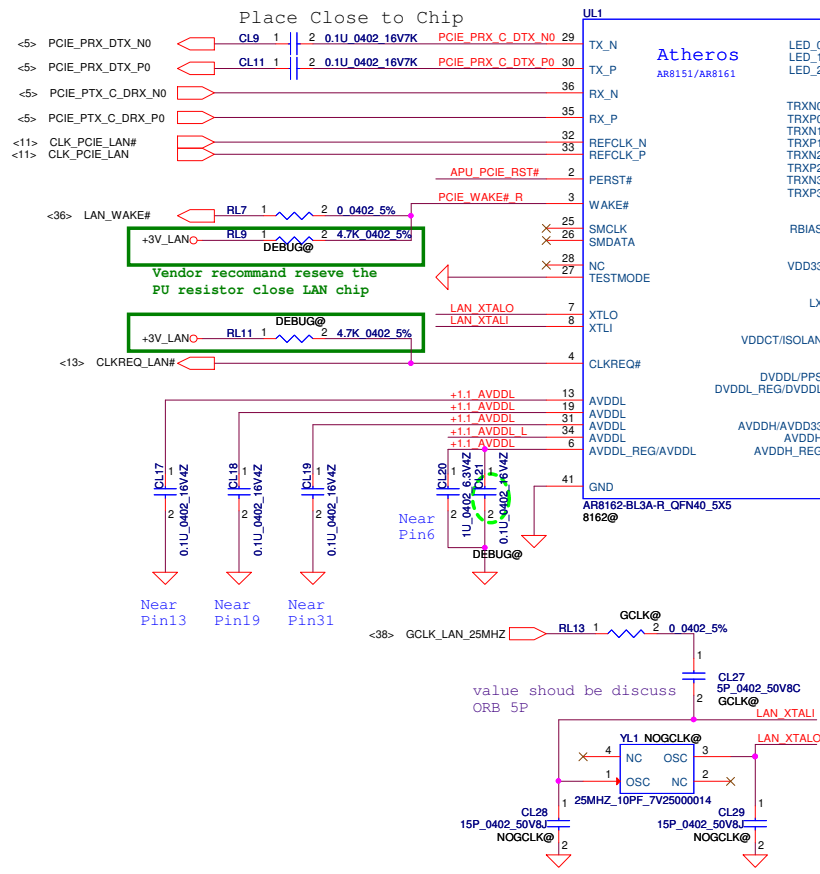
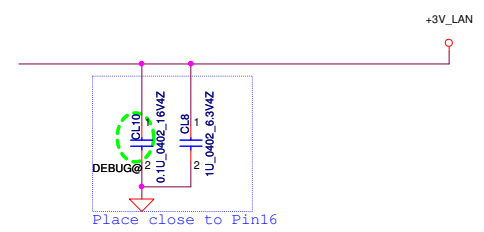
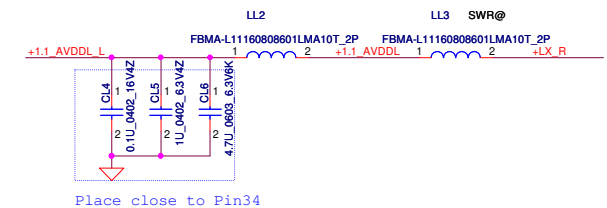
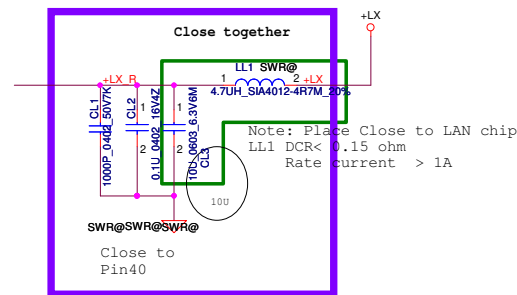
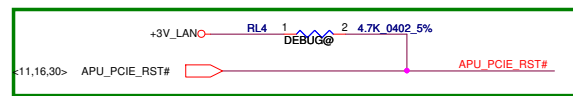


**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

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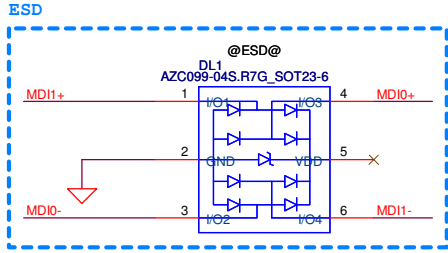
Vendor recommend reseve the PU resistor close LAN chip



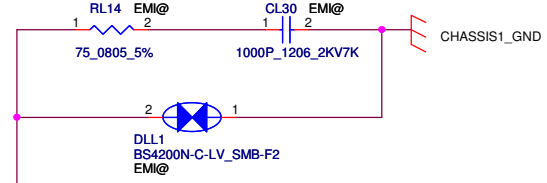
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title	
				LAN-AR8162/8172	
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DL1
 1'S PN:SC300001G00
 2'S PN:SC300002E00

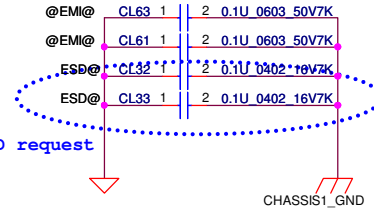
Place Close to TL1



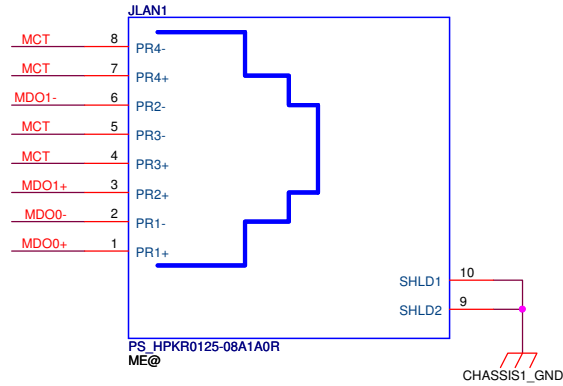
Reserve gas tube for EMI go rural solution



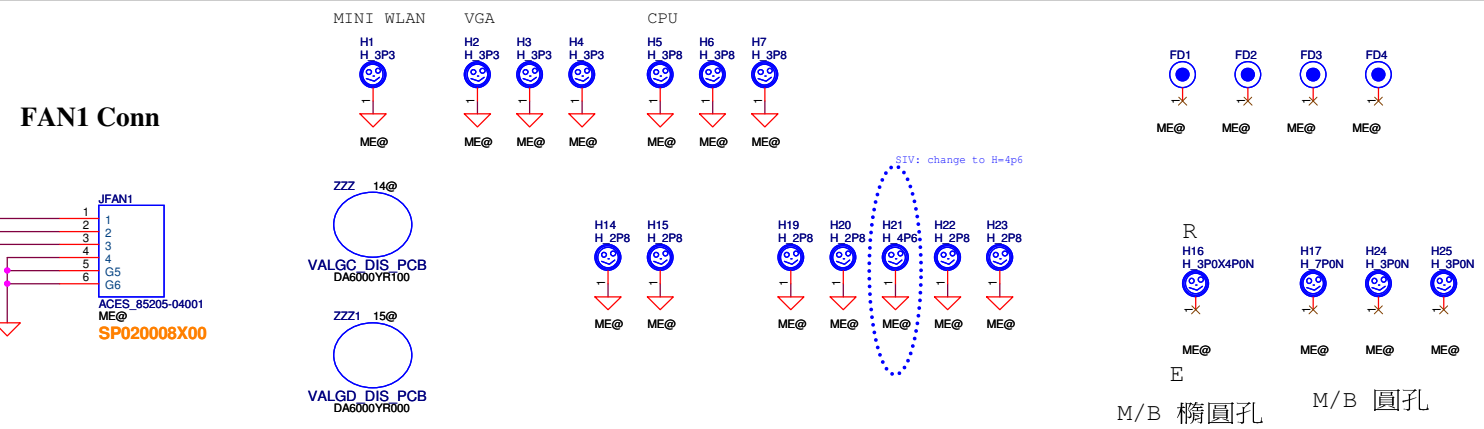
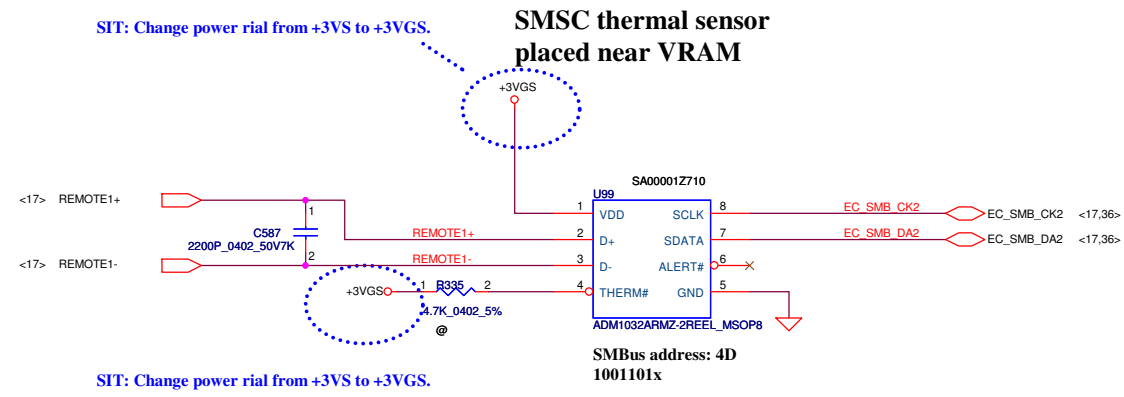
Place Close to TL1



SIT: For ESD request

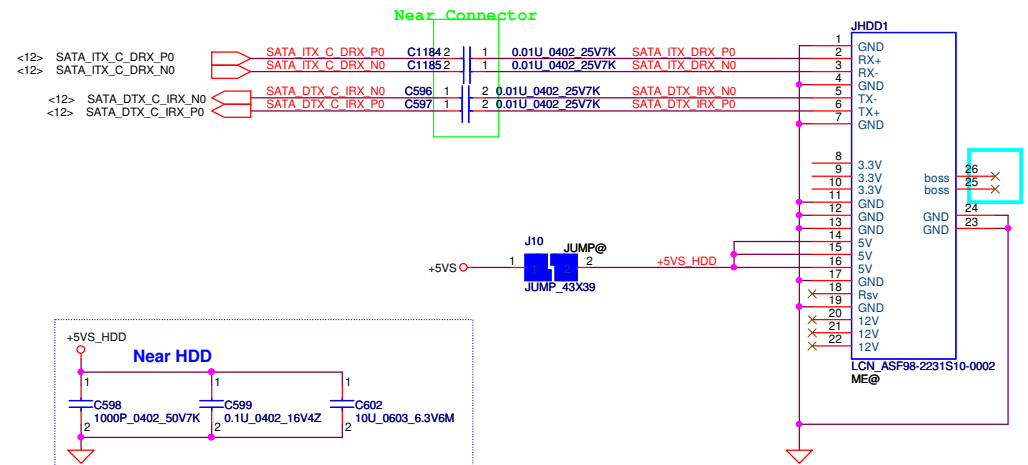


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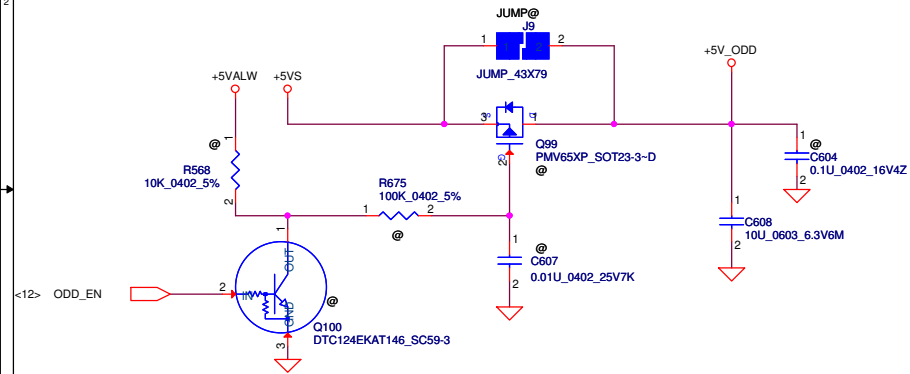
SATA HDD Conn.



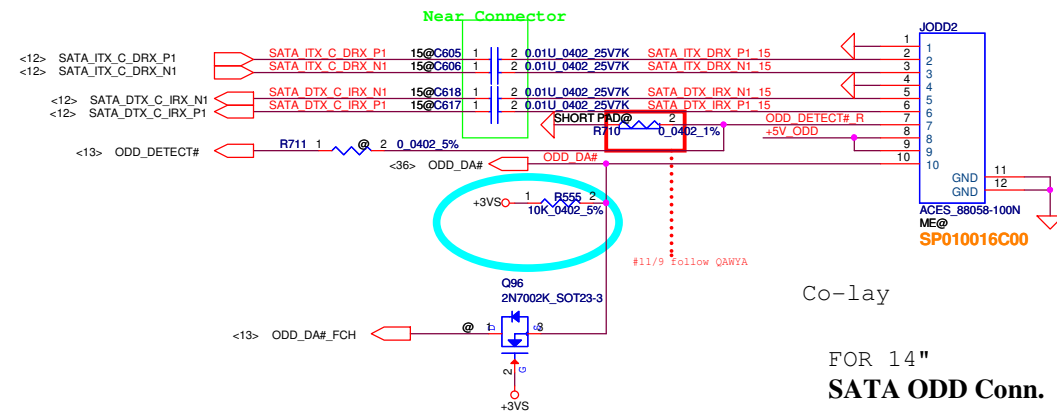
SIT: 3/1 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 to DC010009C00)

ODD Power Control

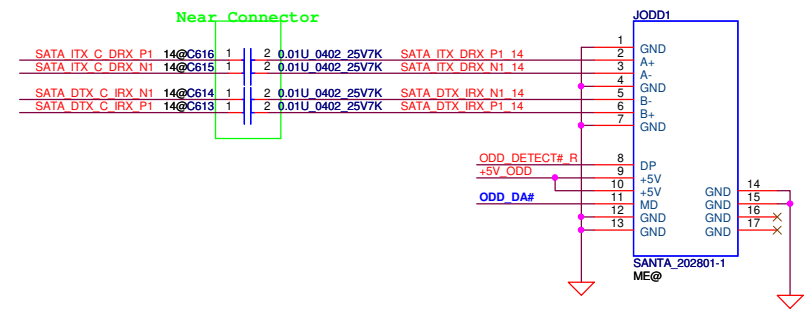
Per-MP: 4/3 un-pop ODD power control circuits



FOR 15" SATA ODD FFC Conn.

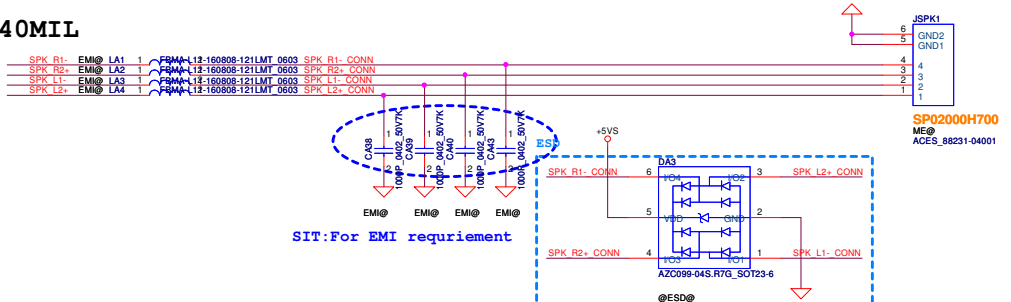
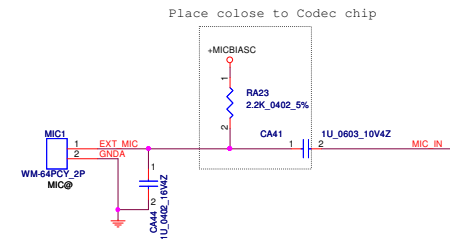
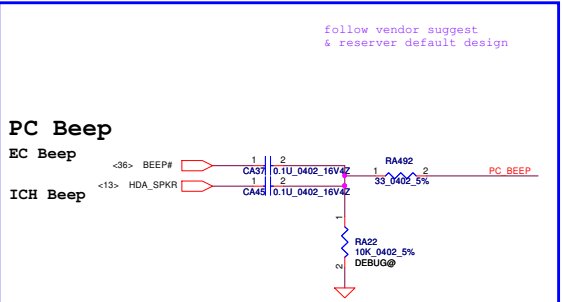
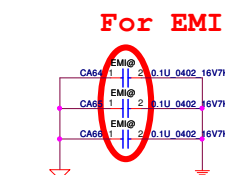
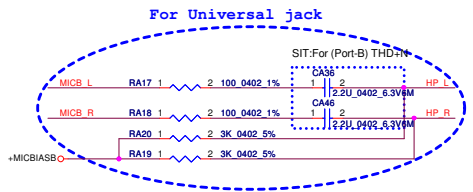
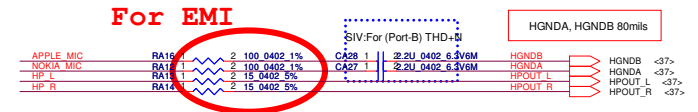
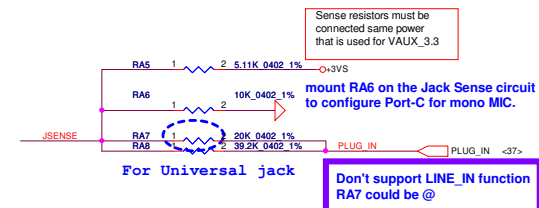
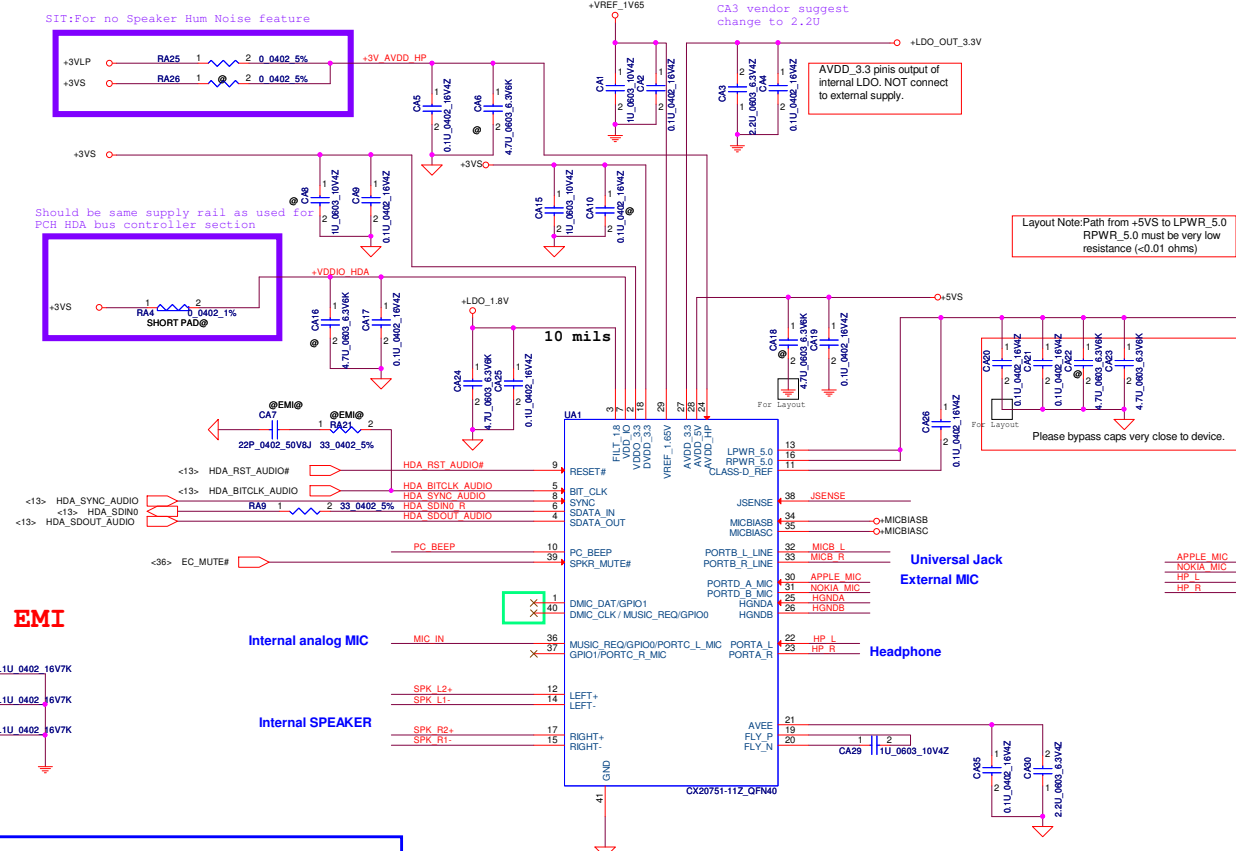


FOR 14" SATA ODD Conn.



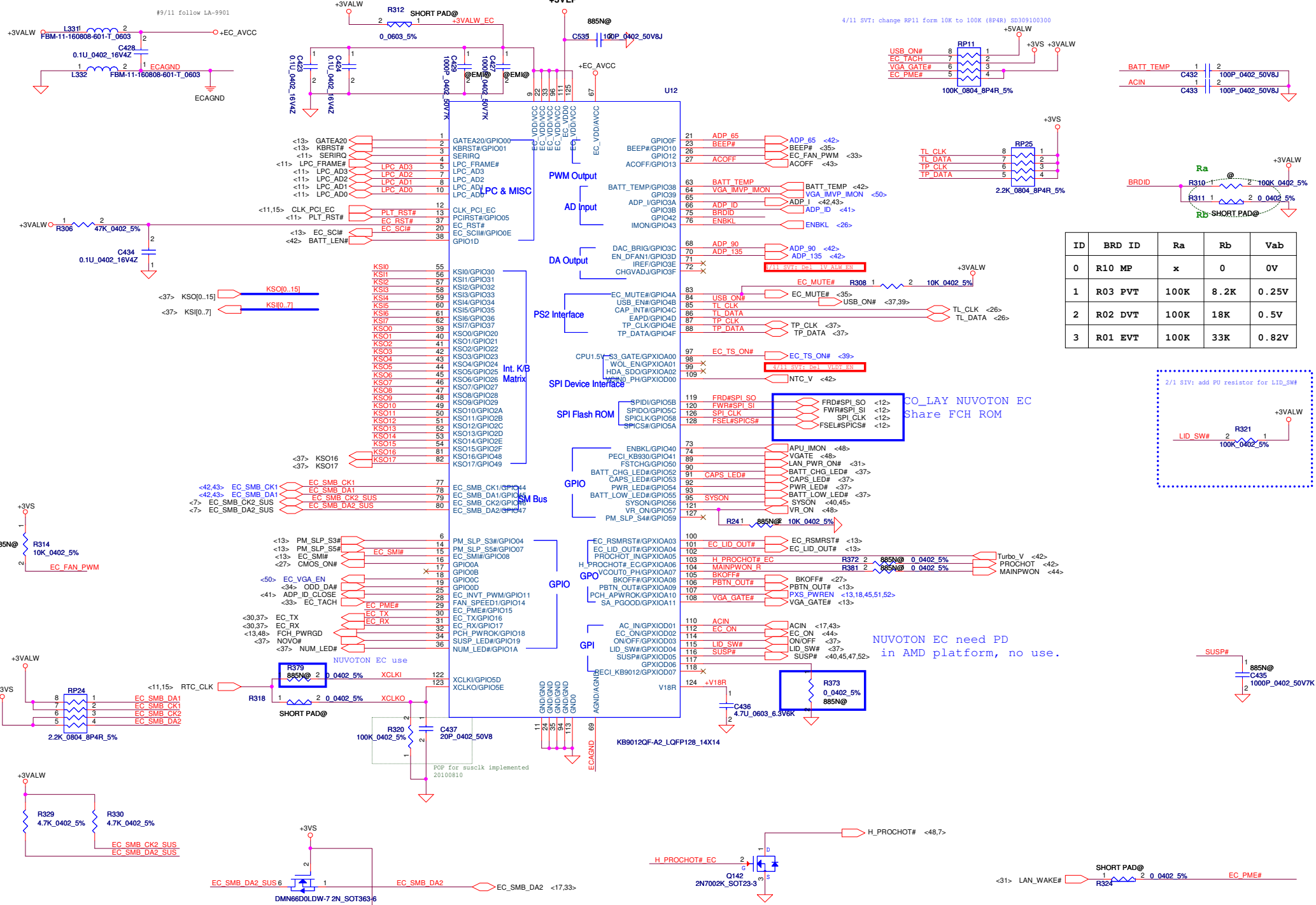
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CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

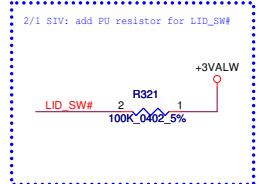


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Compal Electronics, Inc.



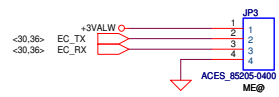
ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V



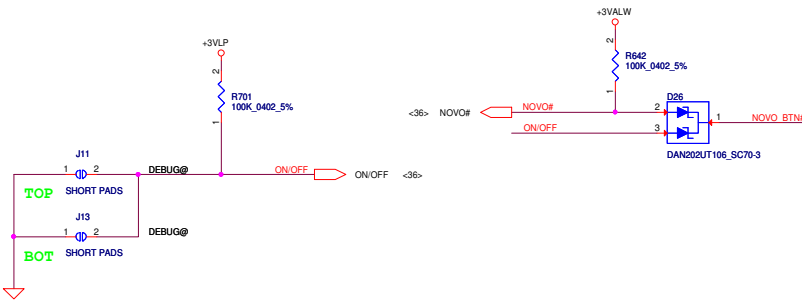
CO_LAY NUVOTON EC Share FCH ROM

NUVOTON EC need PD in AMD platform, no use.

For EC Debug



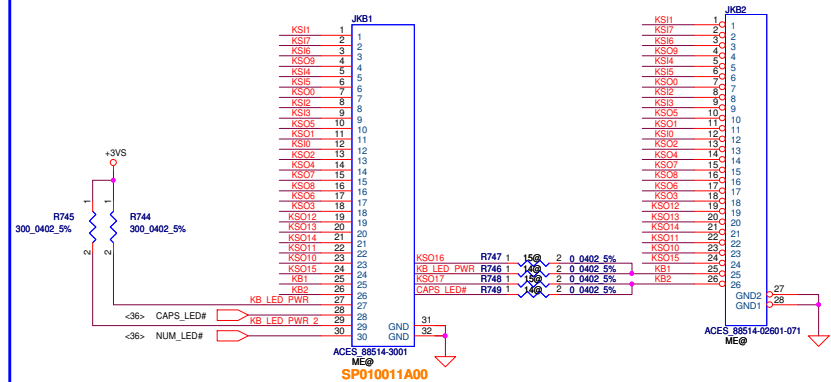
PWR Button



Key Board Conn.

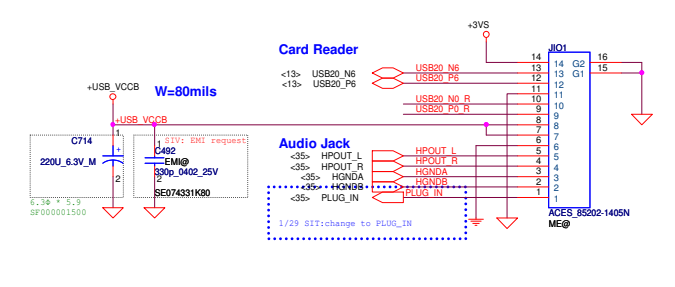
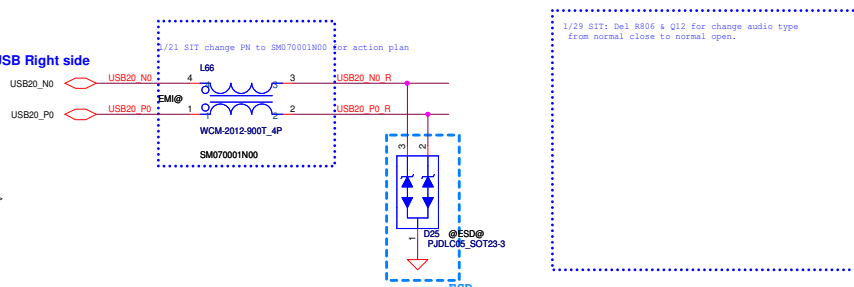
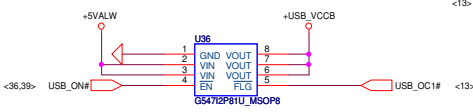
For 15"

For 14"

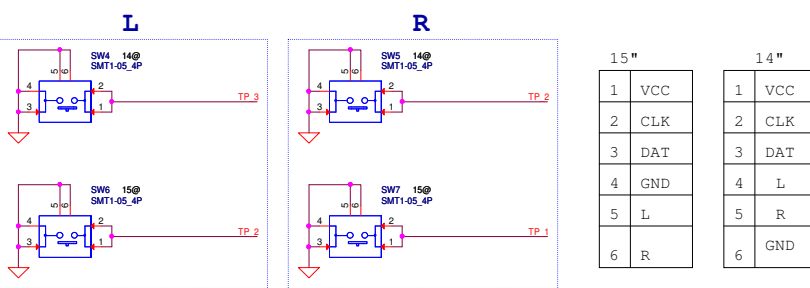
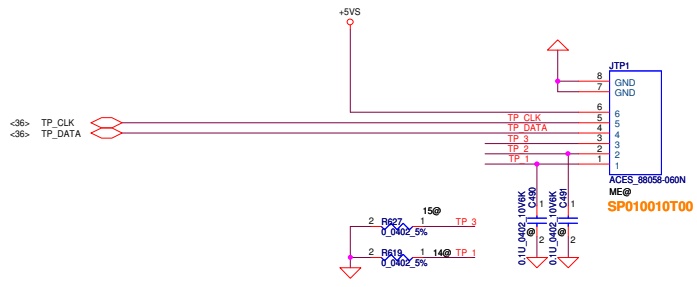


IO/B Conn.

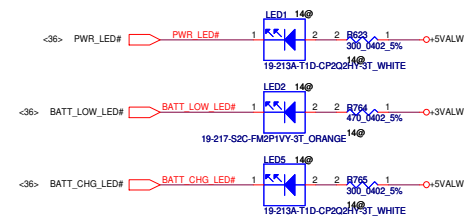
Ext. USB2.0



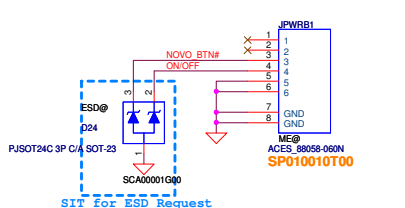
TP Switch & TP Conn.



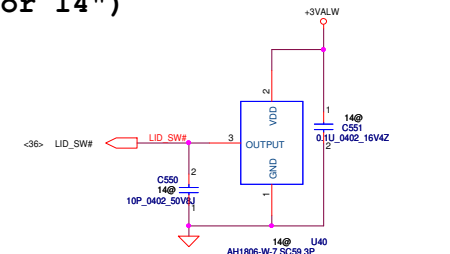
LED



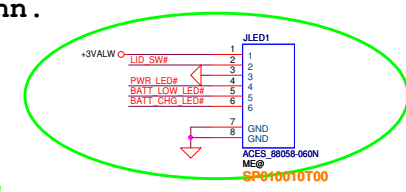
PWR/B Conn.



Lid SW (For 14")



LED/B Conn.



For 15"

15"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND

Security Classification	Compal Secret Data		Title Compal Electronics, Inc. ROM/KB/D/PWR/CR/LED/TP Conn.
Issued Date	2012/11/13	Deciphered Date	
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For UMA

U71 GCLK238@

P/N: SA00005D000

SLG3NB244VTR_TQFN16_2X3

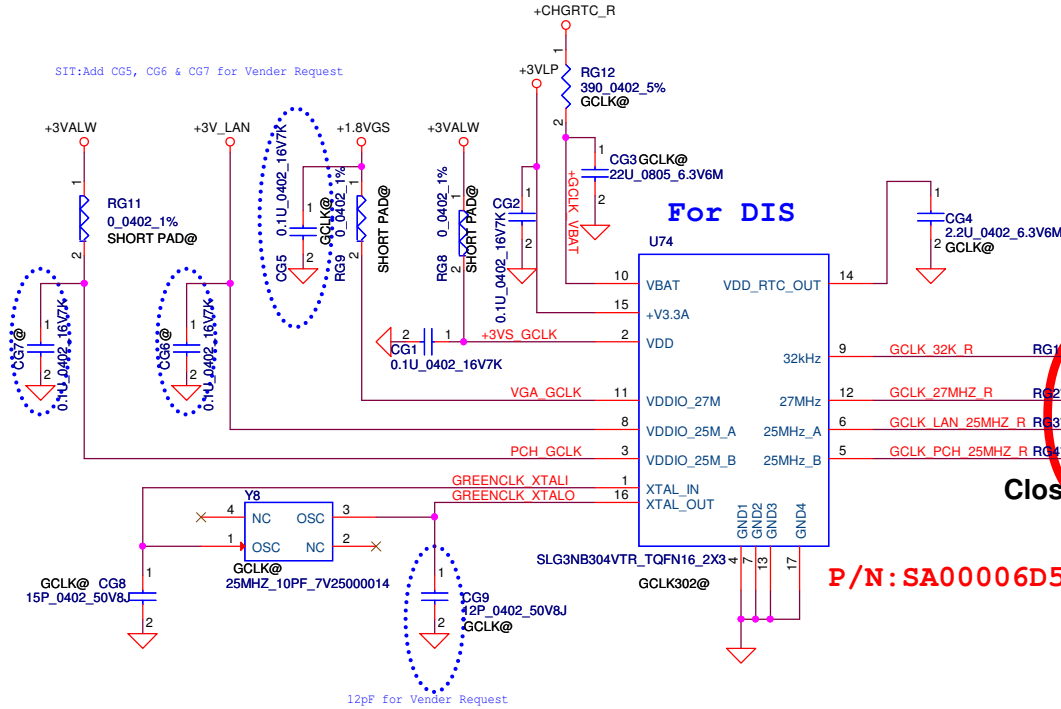
Every power trace need:
W=20mils

For GreenCLK generate CLK:

Mount: All parts in this page except
Swing Level RES (Marked "****")

NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969

SIT:Add CG5, CG6 & CG7 for Vender Request



For DIS

For EMI

Typical CLK_32K_FCH trace <= 6"
Max. length <= 24"

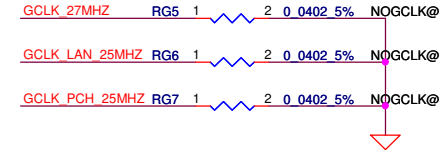
P/N: SA00006D500

Close to GCLK

Typical CLK_25M_FCH trace <= 8"
Typical CLK_25M_LAN trace <= 8"
Max. length <= 12"

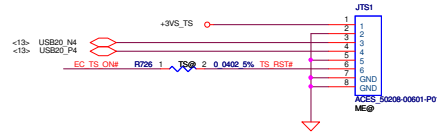
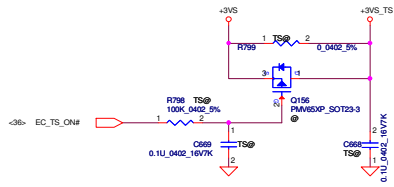
FCH_32.768K
dGPU
LAN
FCH_25M

Reserved for Swing Level adjustment
(Close GCLK side)

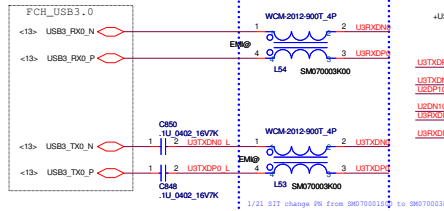
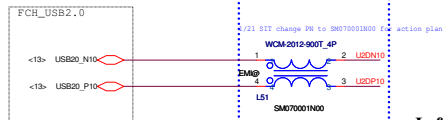
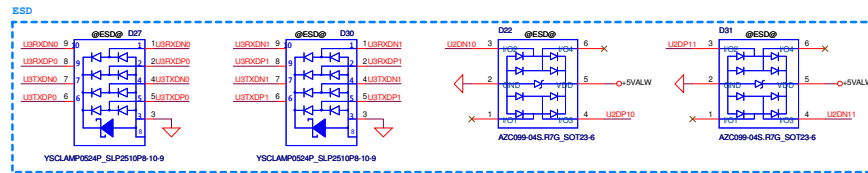
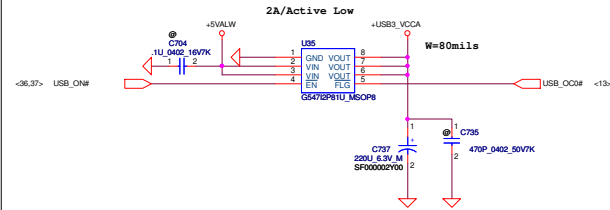


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Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title GCLK	
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				VALGD MB L	

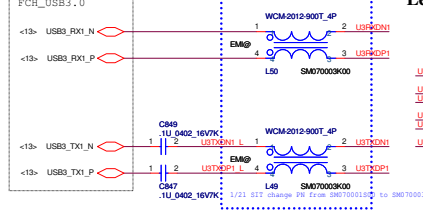
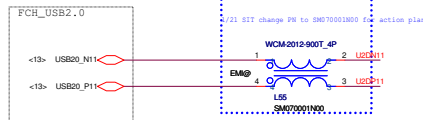
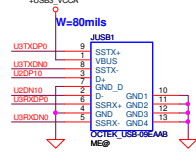
Touch Screen



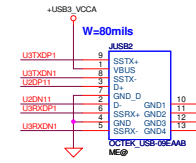
USB3.0



Left Ext.USB Conn. 1



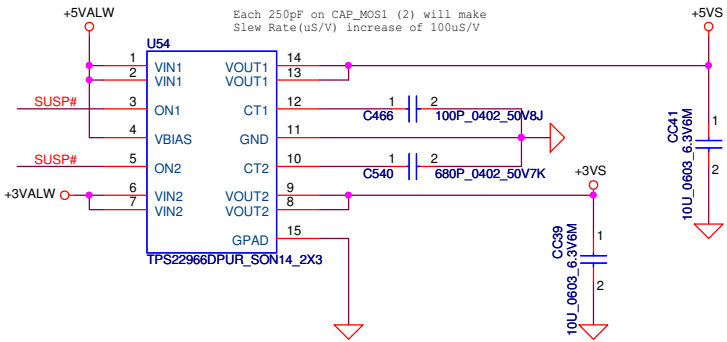
Left Ext.USB Conn. 2



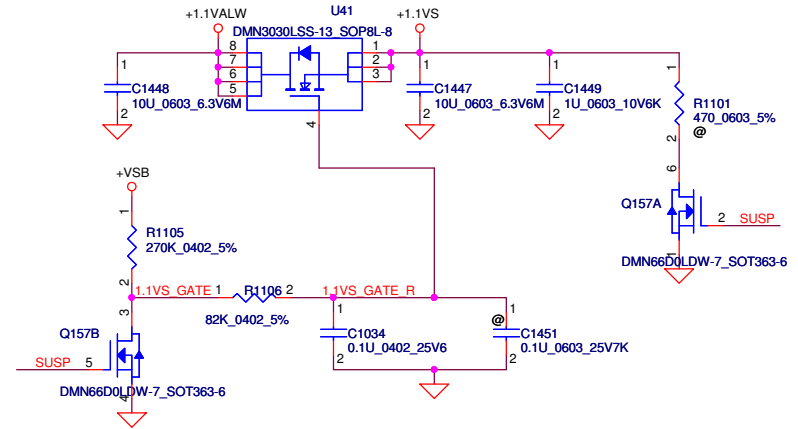
Place TX AC coupling Cap (C843-C850) Close to connector

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Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title
				USB3.0/Left USB Ports
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				Date: Friday, April 12, 2013 Sheet 39 of 67

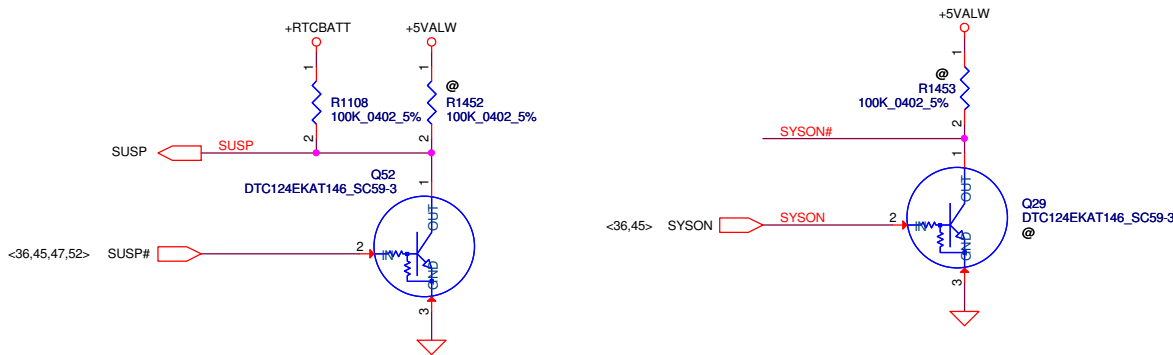
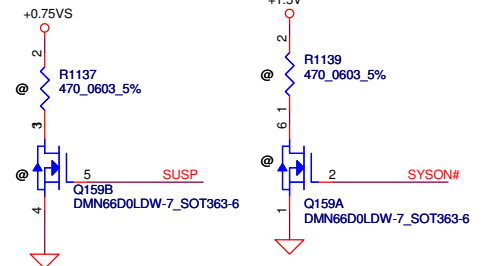
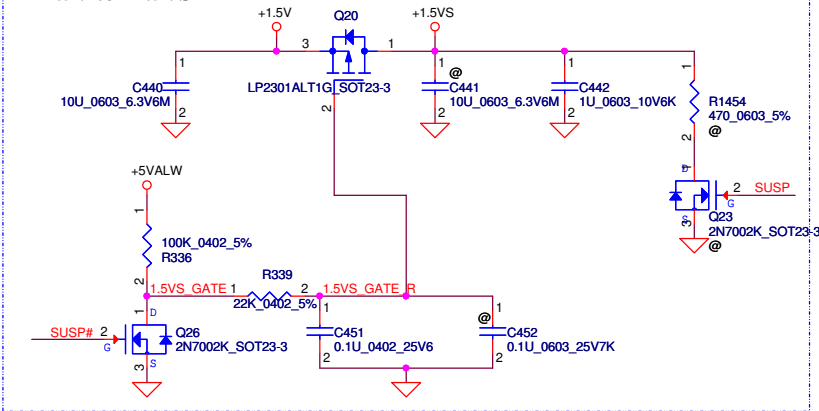
+5VALW to +5VS combine with +3VALW to +3VS



+1.1VALW TO +1.1VS (5.15A)

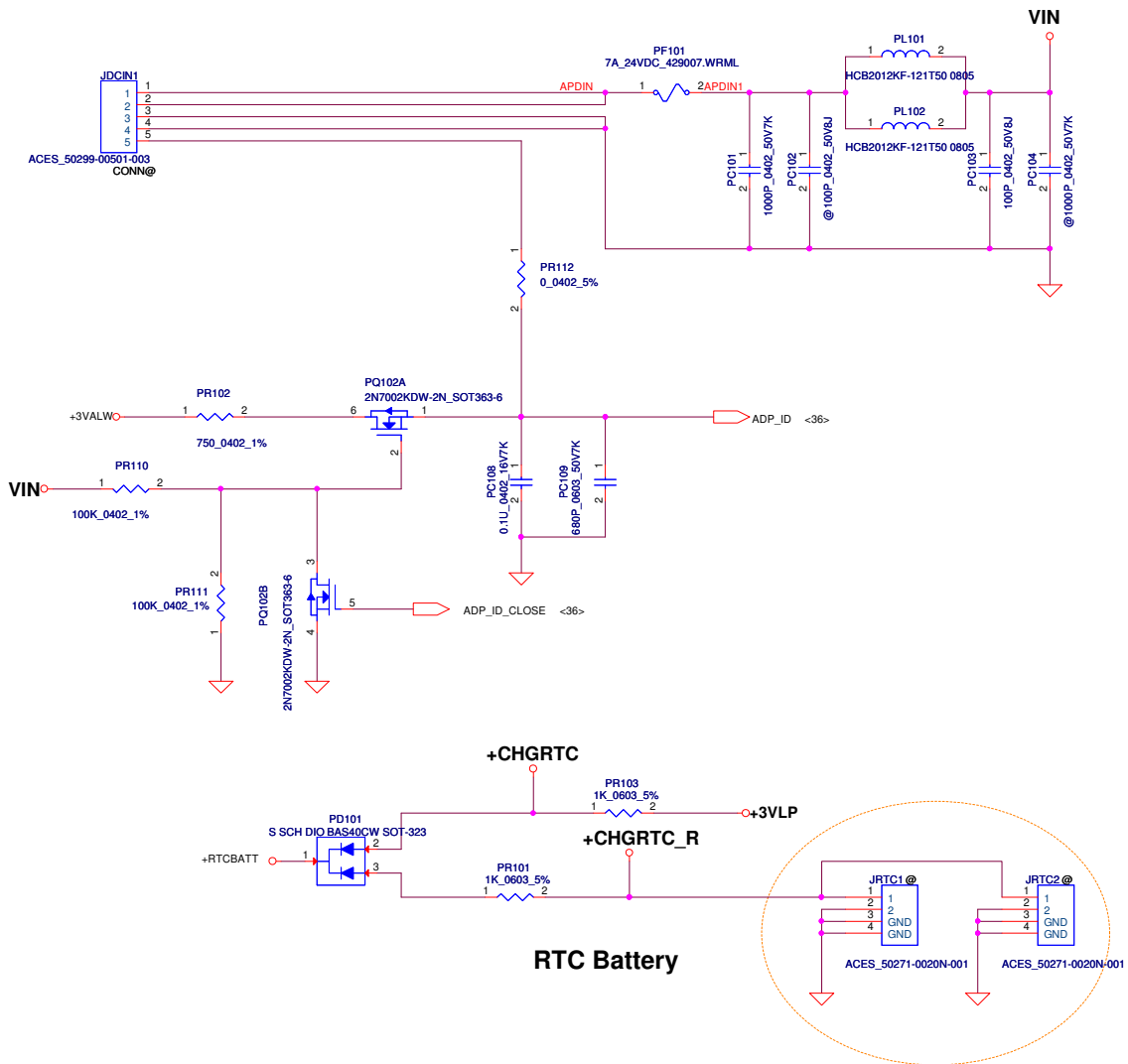


+1.5V to +1.5VS



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title	
				DC Interface	
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File Name	Document Number	Rev			
Custom	VALGD MB L	0.1			
Date:	Friday, April 12, 2013	Sheet	40	of	57

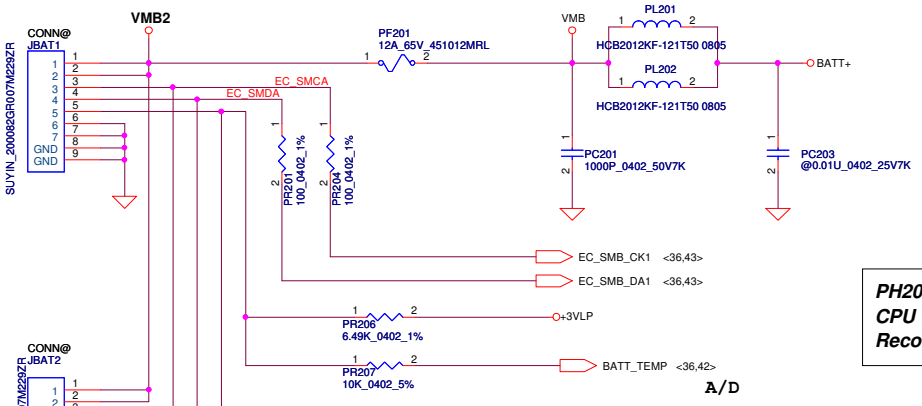
ADP_ID	90W	65W
AC Adapter	open	10
R(K ohm)	3.3	1.65
ADP_ID(V)	>2.64	1.32~1.98
Detection voltage		



Security Classification	Compal Secret Data	
Issued Date	2011/06/15	Deciphered Date
		2012/07/11

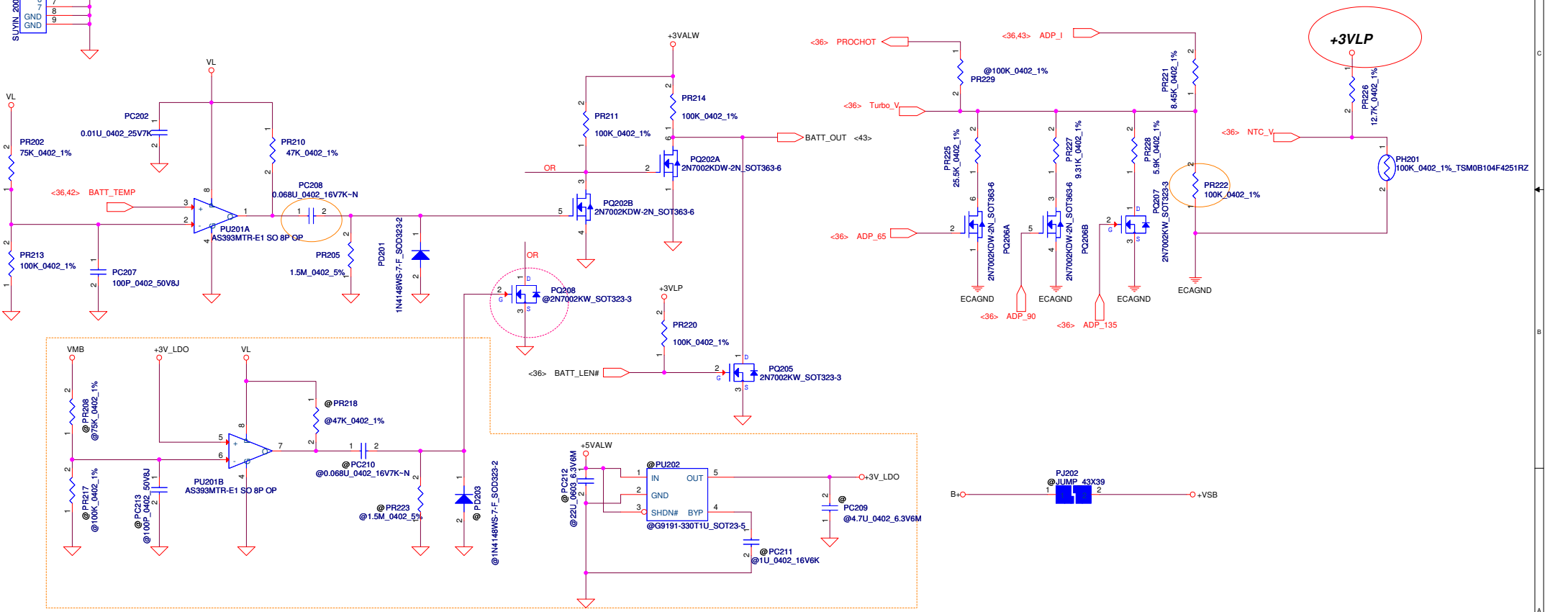
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Compal Electronics, Inc.	
PWR DCIN / RTC Battery	
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Date: Friday, April 12, 2013	Sheet 41 of 62



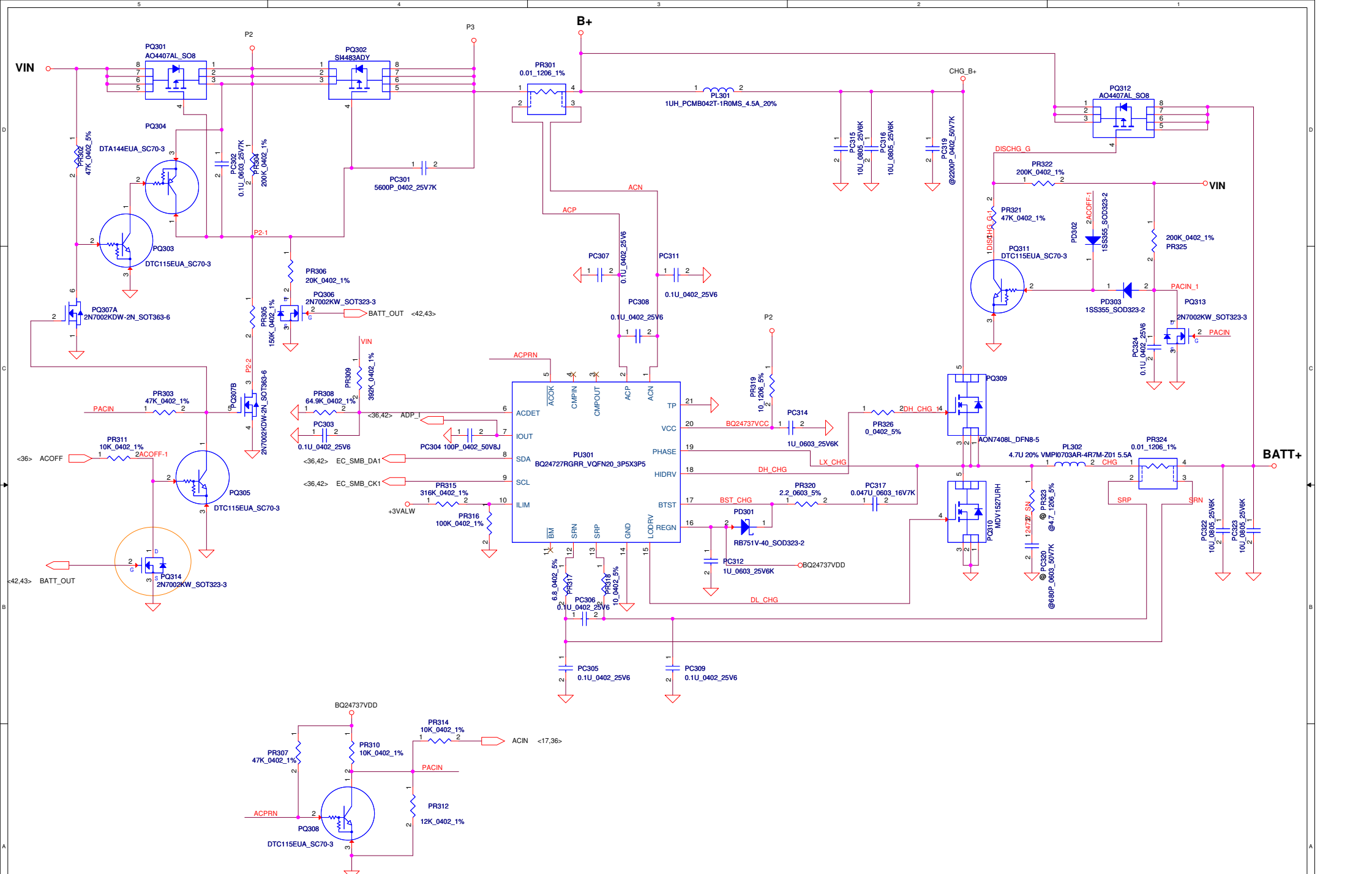
PH201 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA) : 1.65K 70W active 65W recovery

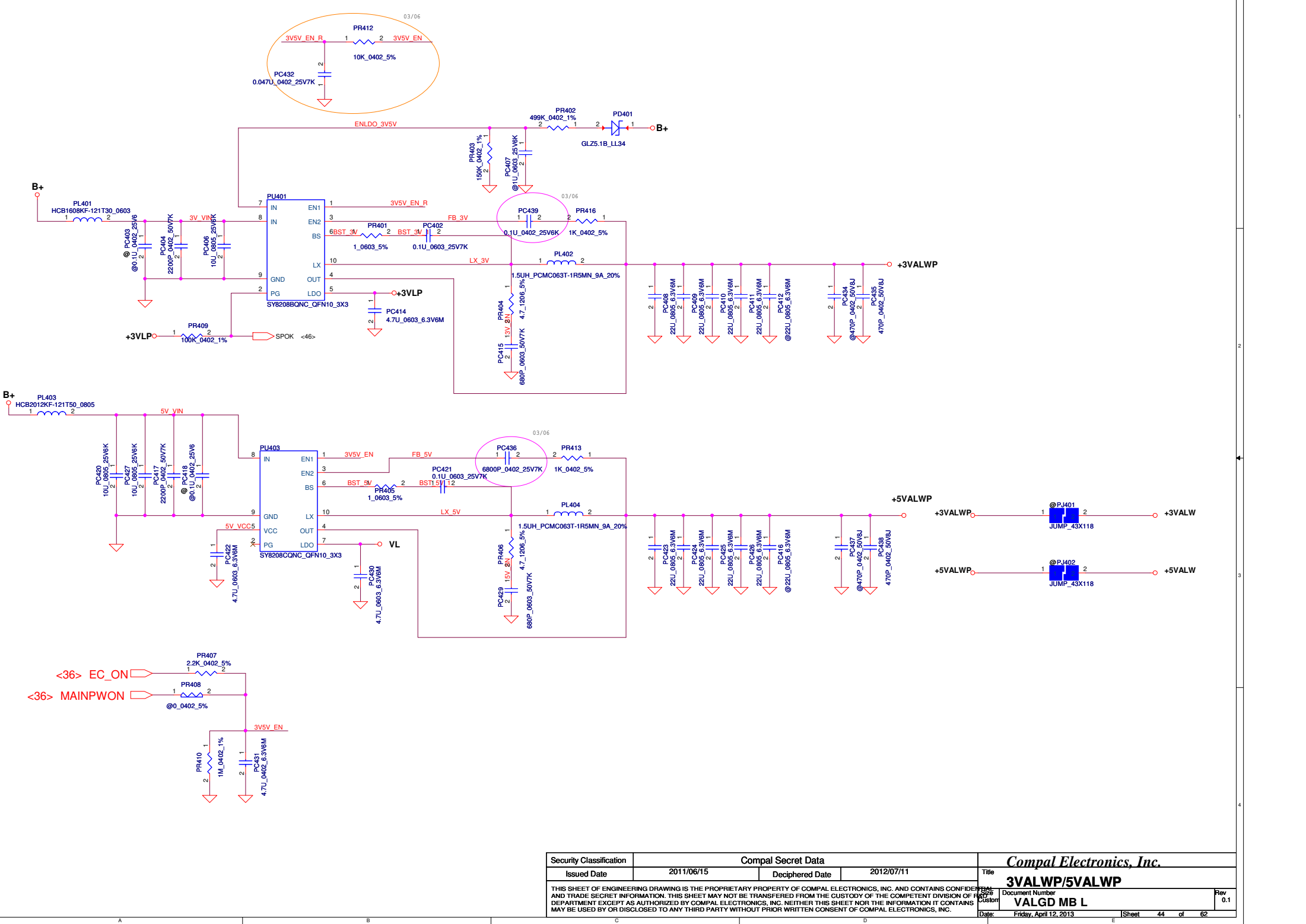


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11
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Compal Electronics, Inc.	
PWR-BATTERY CONN/OTP	
Document Number	Rev
VALGD MB L	0.1
Date: Friday, April 12, 2013	Sheet 42 of 62



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	CHARGER
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Size	Document Number			Rev	0.1
	VALGD MB L				
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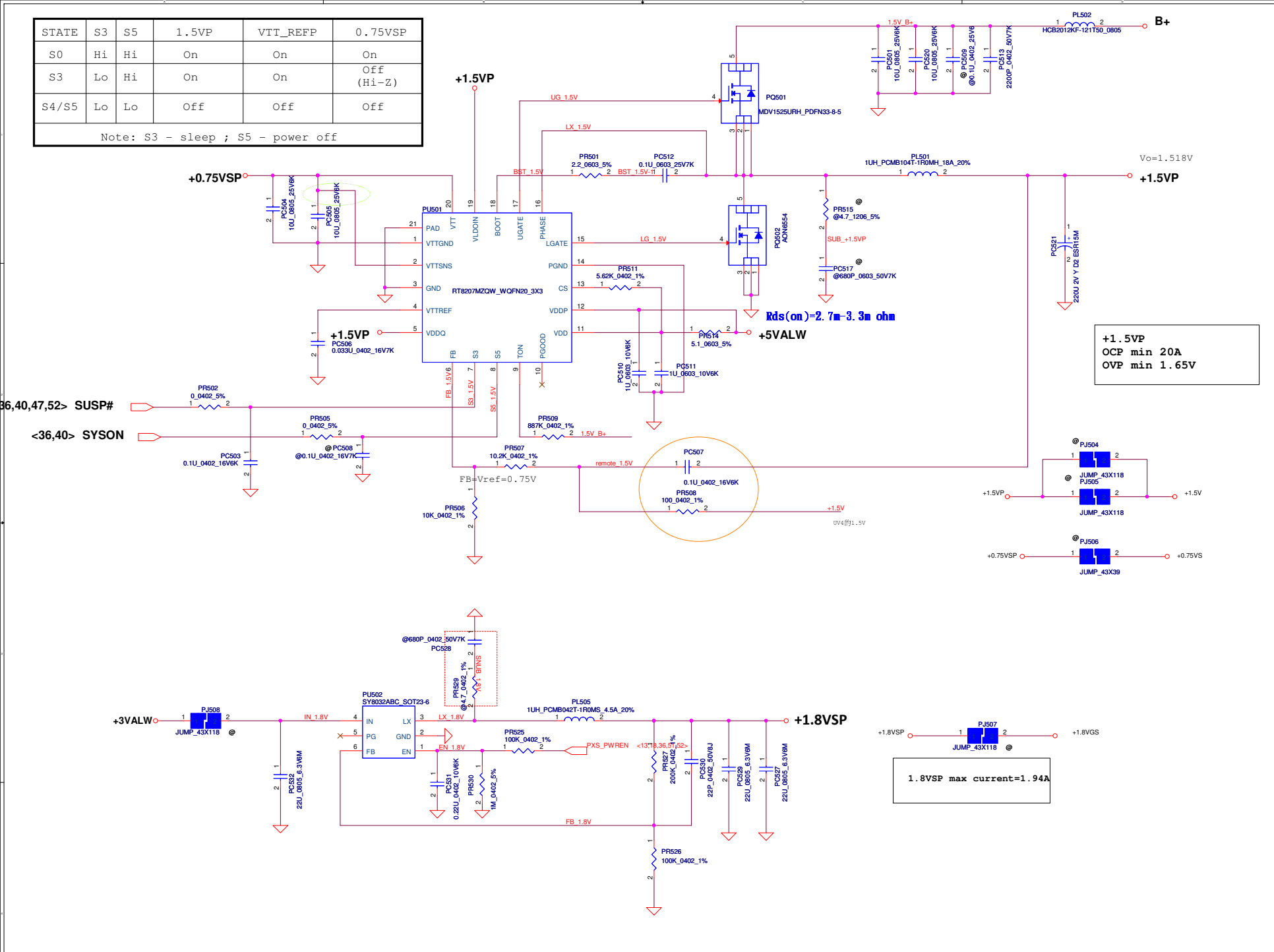
Security Classification	Compal Secret Data	
Issued Date	2011/06/15	Deciphered Date
		2012/07/11

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Compal Electronics, Inc.	
3VALWP/5VALWP	
Document Number	Rev
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Date: Friday, April 12, 2013	Sheet 44 of 62

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

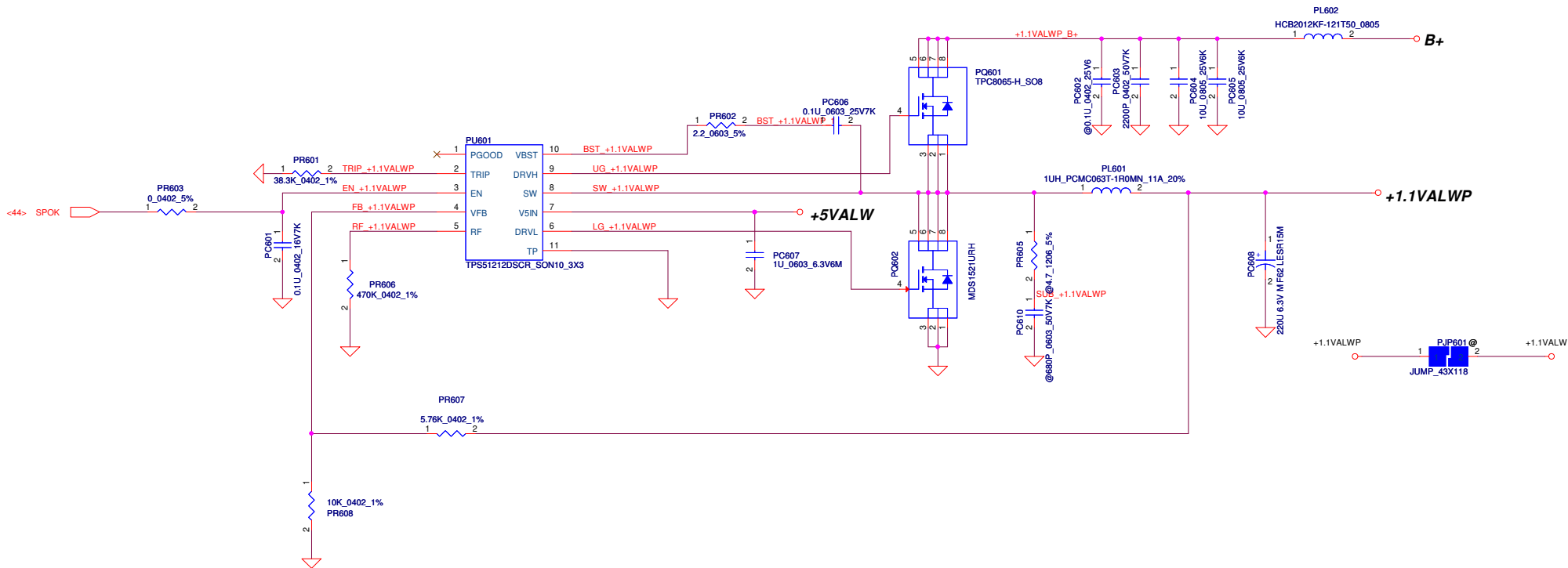
Note: S3 - sleep ; S5 - power off



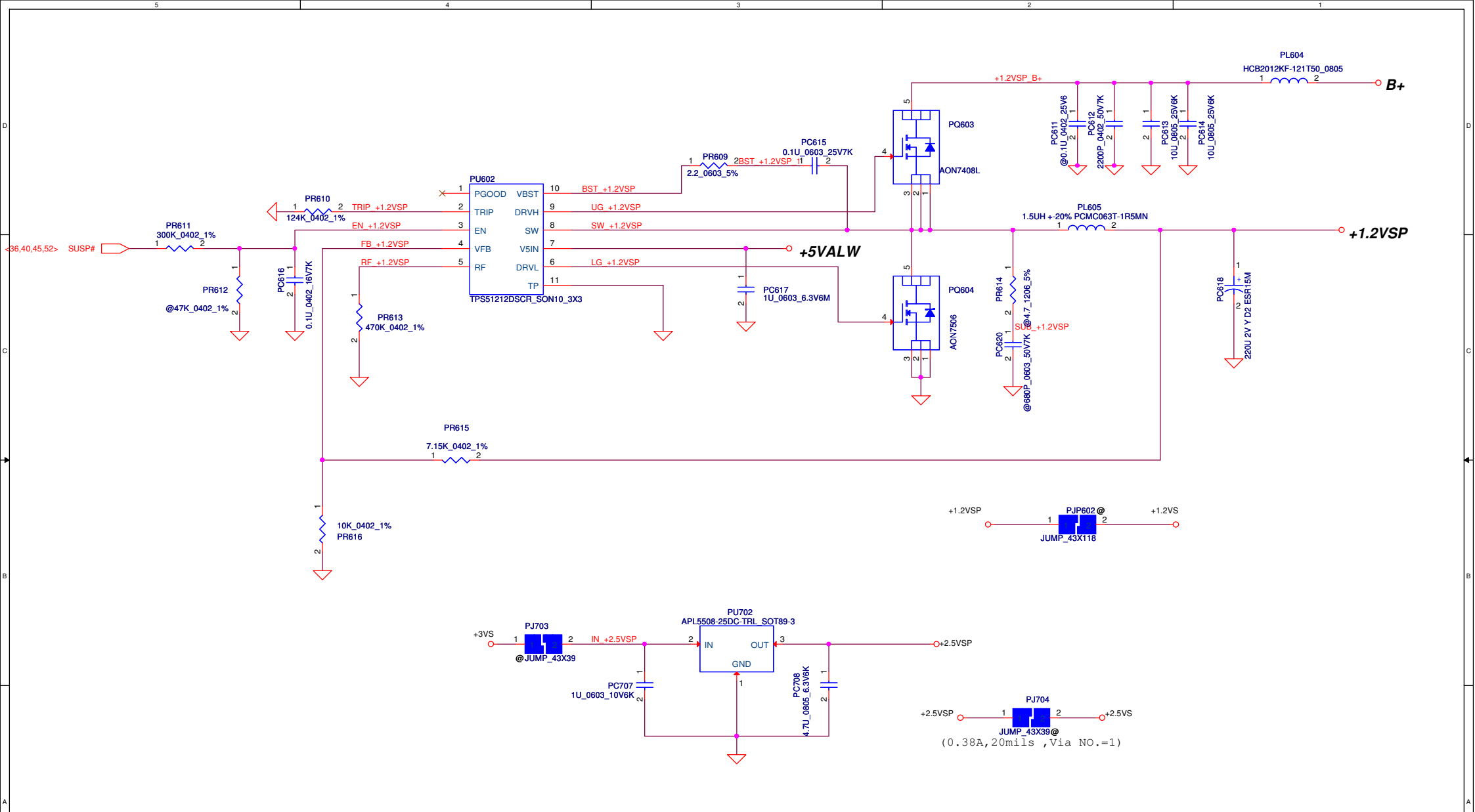
+1.5VP
 OCP min 20A
 OVP min 1.65V

1.8VSP max current=1.94A

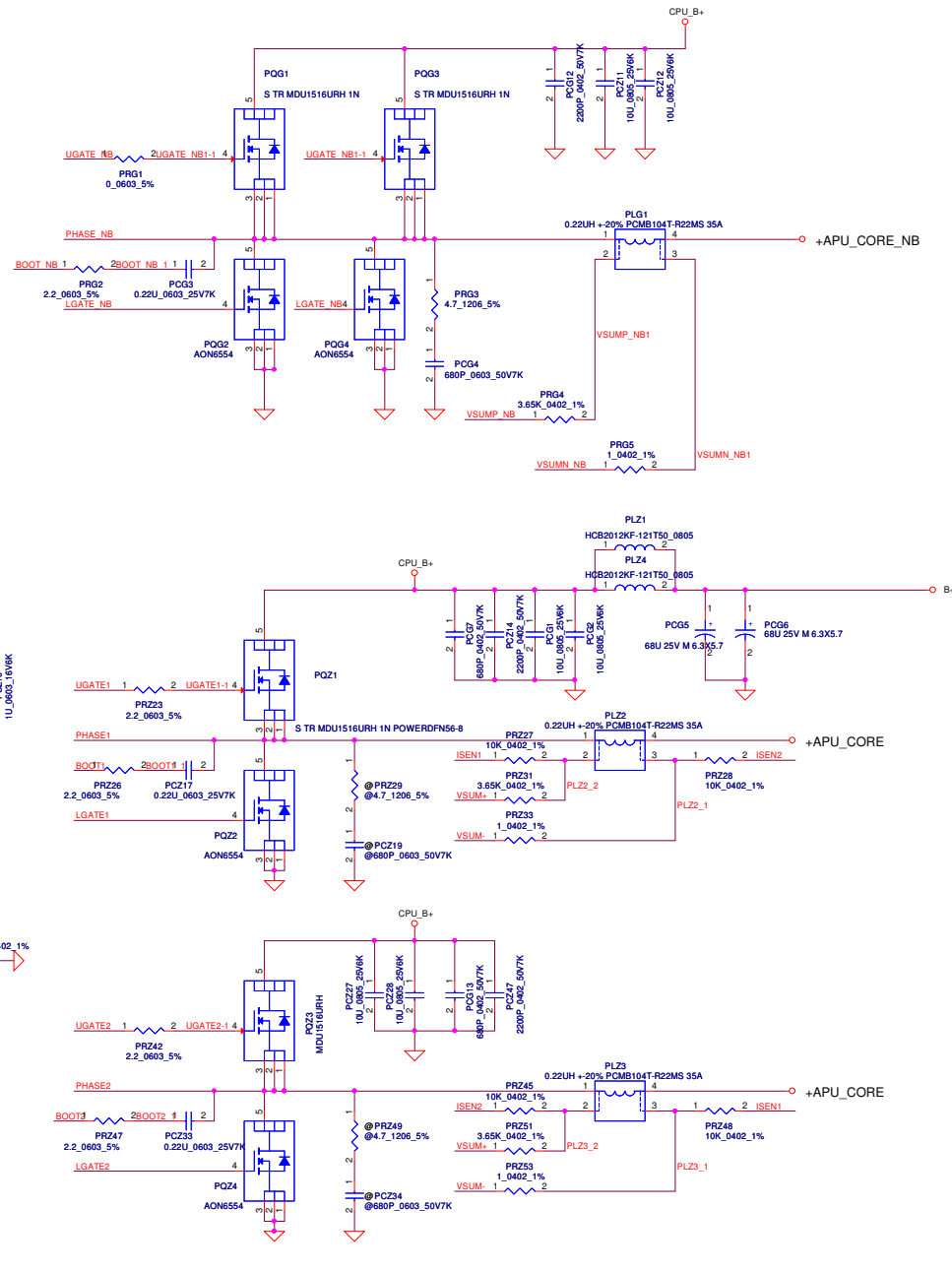
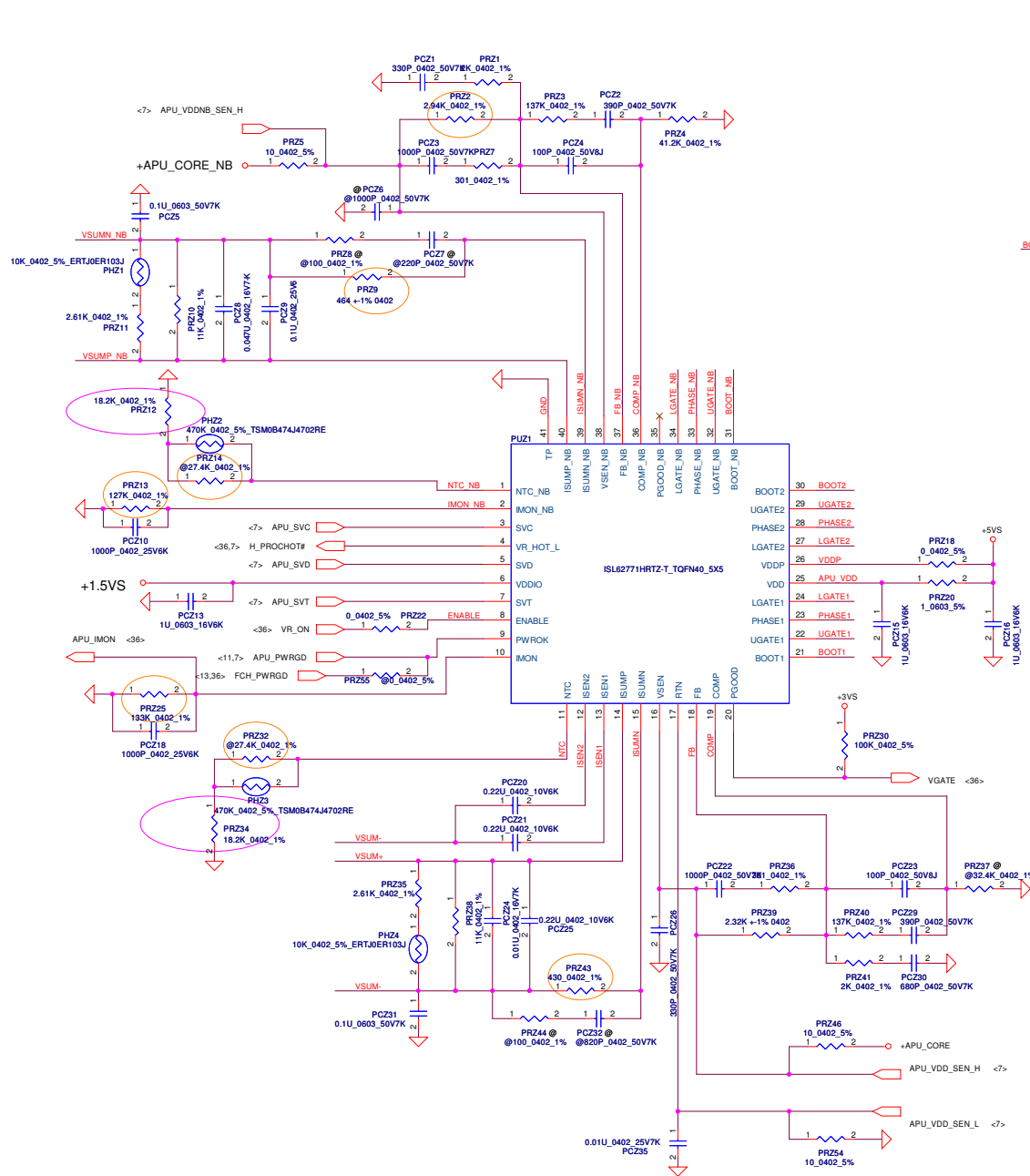
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	+1.5VP/+1.8VSP	
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Date:	Friday, April 12, 2013	Sheet	45	of	62



Security Classification	Compal Secret Data		Title	PWR +1.1VALWP	
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Document Number	VALGD MB L
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				Date:	Friday, April 12, 2013
				Sheet	46 of 51



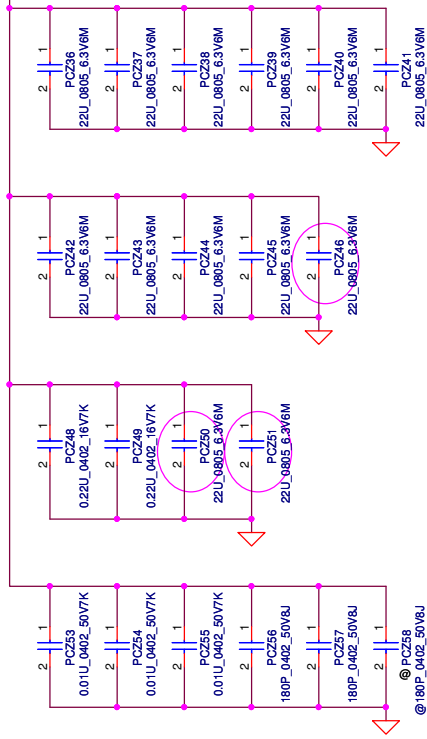
Security Classification	Compal Secret Data			Title	PWR +1.2VSP/2.5VSP	
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Document Number	VALGD MB L	
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Date:	Friday, April 12, 2013	Sheet	47 of 51			



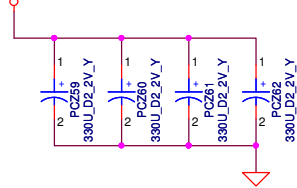
Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/18	Deciphered Date	2015/07/08	Compal Electronics, Inc.
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				Sheet 48 of 2

+APU_CORE

+APU_CORE

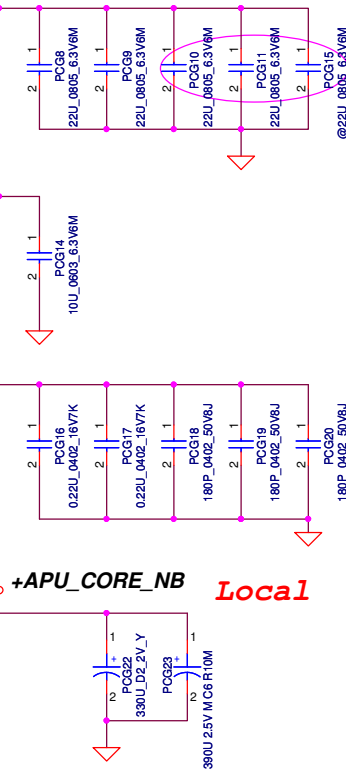


+APU_CORE Local

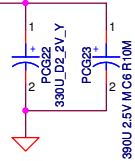


+APU_CORE_NB

+APU_CORE_NB

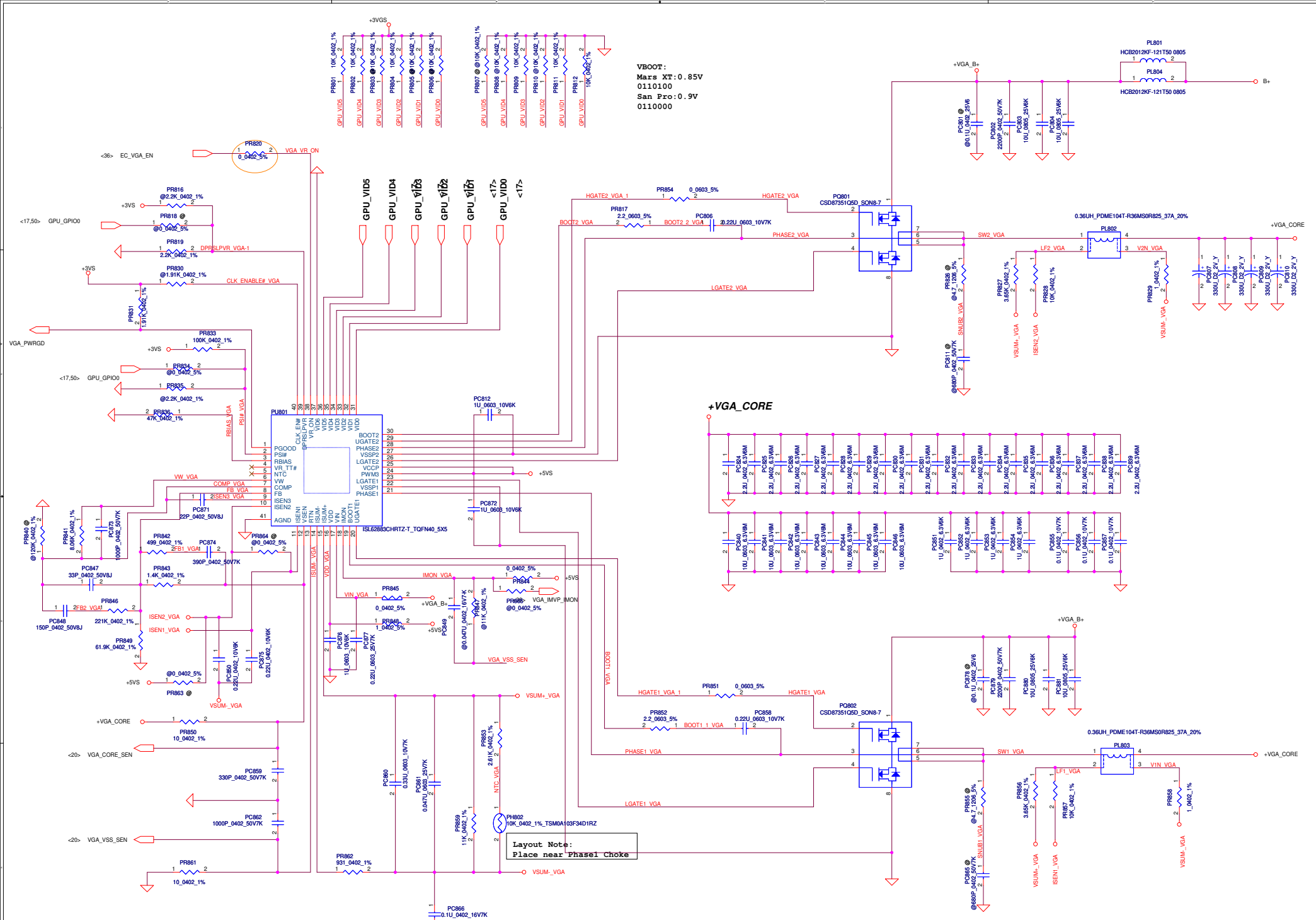


+APU_CORE_NB Local



	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
APU_CORE	4	10	2		3	2
APU_CORE_NB	2	2	2	1		3

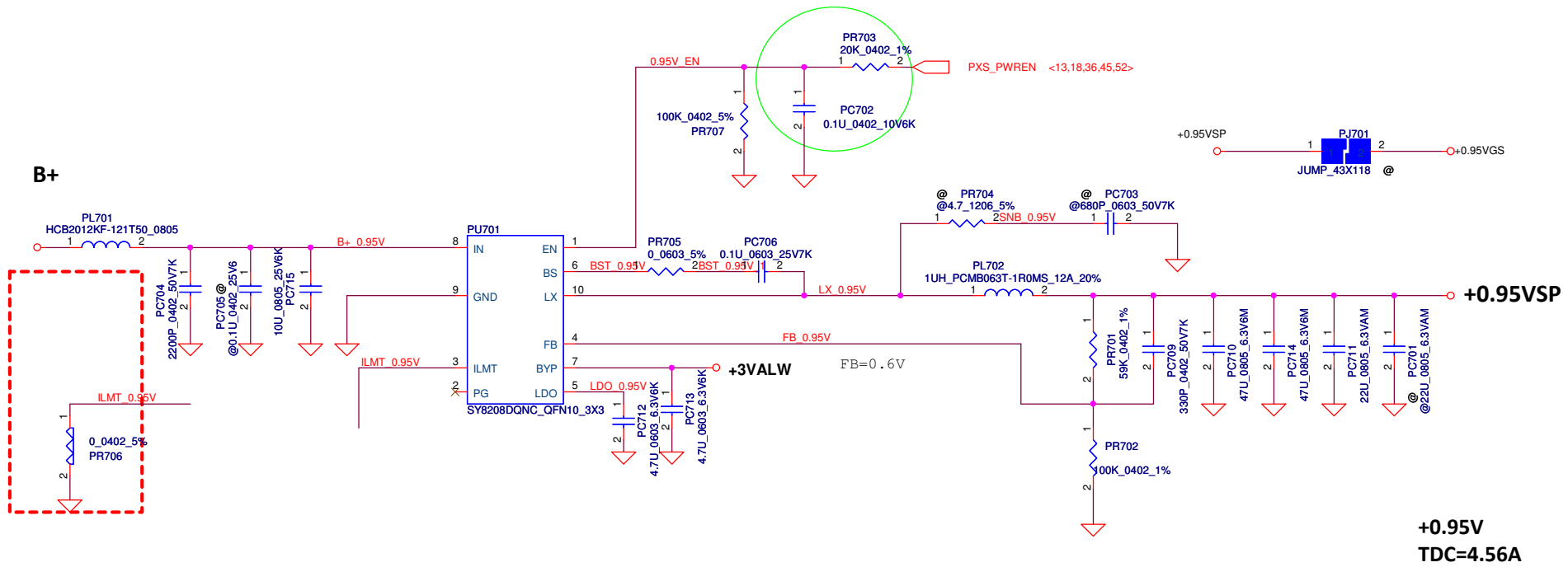
Security Classification	Compal Secret Data		Compal Electronics, Inc. PROCESSOR DECOUPLING		
Issued Date	2011/07/29	Deciphered Date			
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Date:	Friday, April 12, 2013	Sheet	49	of	2



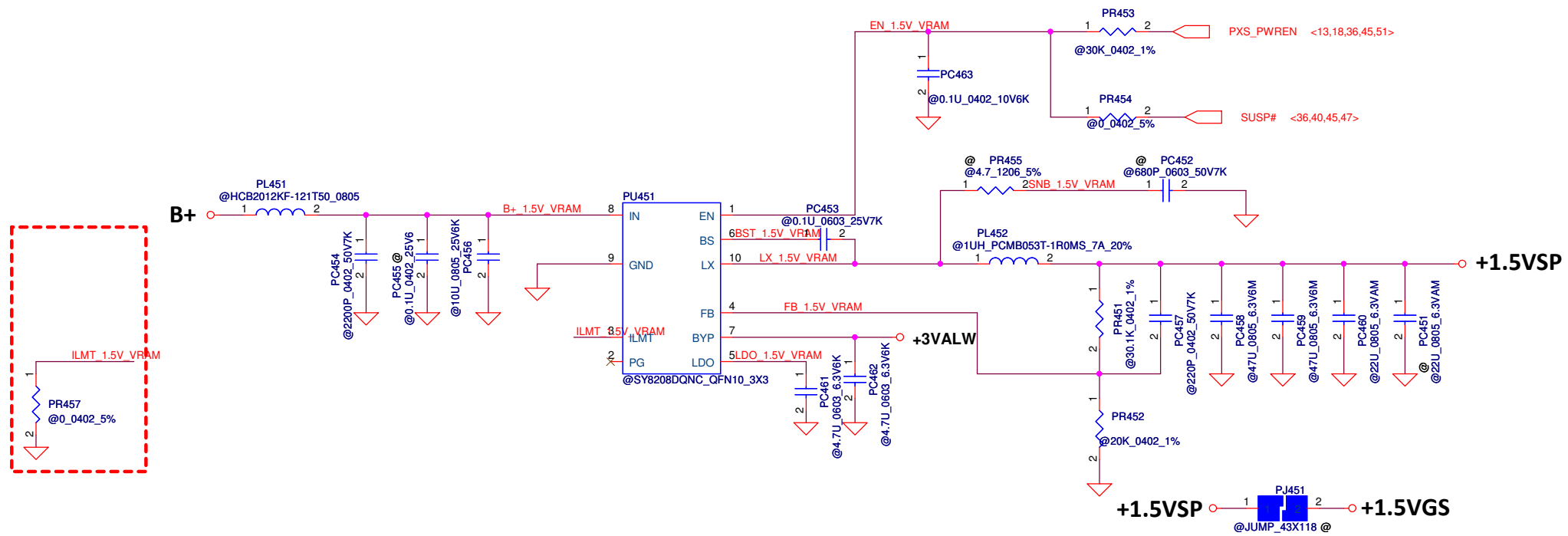
VBOOT:
Mars XT:0.85V
0110100
San Pro:0.9V
0110000

Layout Note:
Place near Phase1 Choke

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/30	Deciphered Date	2012/12/31	VGA_COREP	
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Size	Document Number	Rev		Date	
	VALGD MB L	1.0		Friday, April 12, 2013	
				Sheet	50 of 59



Security Classification	Compal Secret Data			Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	+0.95VSP	
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				VALGD MB L	0.1
				Date:	Friday, April 12, 2013
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Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31
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Compal Electronics, Inc.		
+1.5VSP(VRAM)		
Size	Document Number	Rev
Custom	VALGD MB L	0.1
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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P41	P41-PWR-DCIN / RTC Battery	12/11	PWR	add smart Adapter function	ADD PQ208,PQ102,PR111,PR225,PR228,PR227;Del PR973,PR974,PR972,PR975	
2	P42	P42-PWR-BATTERY CONN/OTP	12/11	PWR	add smart Adapter function	change PQ206,PR110,PR222,PR221,PC109 part number	
3	P51	P51-PWR--0.95VSP	12/11	PWR	modify 1.5V output level	modify PR701&PR702 to 59K&100K	
4	P50	P50-PWR--VGA_CORE	PWR	PWR	EMI rule	Add PC802 CAP	
5	P50	P50-PWR--VGA_CORE	01/08	PWR	vender FAE request	change VGA enable pin from SUSP# to EC_VGA_EN	
6	P45	P45-PWR--1.5VP/+1.8VSP	01/08	PWR	0.75V can't power on	change 0.75V enable pin from SUSP to SUSP#	
7	P42	P42-PWR-BATTERY CONN/OTP	01/08	PWR	modify smart Adapter schematic	modify smart Adapter schematic	
8	P44	P44-PWR-3VALWP/5VALWP	02/23	PWR	Add RC delay for 3V power sequence	Add RC delay for 3V power sequence	
9	P48	P48-PWR-CPU_CORE/CPU_CORE_NB	02/23	PWR	modify over temperature setting	modify over temperature setting	
10	P42	P42-PWR-BATTERY CONN/OTP	02/23	PWR	Units will shut down on Optimized Battery Health mode when plug out battery	modify battery health mode schematic	
11	P45	P45-PWR--1.5VP/+1.8VSP	02/23	PWR	VRAM transient fail	Add remote sense schematic	
12	P50	P50-PWR--VGA_CORE	02/23	PWR	AMD change VBOOT SPEC	change Mars XI VBOOT from 1.1V to 0.85V change Sun pro VBOOT from 1.1V to 0.9V	
13	P41,42,48,50	P41,42,48,50	01/10	PWR	Add bead for cost down plan	Add bead for cost down plan	

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				Document Number	Rev 0.1
Date: Friday, April 12, 2013				Sheet	53 of 46

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37		1114		1.SW3 add DEB008 2.add J13		
2	38		1114		1.change netname form +3VS_VGA to +3VGS 2.change netname form +V1.05S_VCCP to +3VALM 3.remove RG10 4.change U71 P/N form SA000063300 to SA000060500 for DIS, .change U71 P/N form SA000057100 to SA00005D000 for UMA		
3	36		1114		1.VR_ON reserve PD 10K		
4	17		1114A		1.remove RV16,RV17		
5	27		1114A		1.reserve RV687,RV92		
6	12,30		1115		1.change netname from PCH_BT_ON# to BT_ON# 2.change netname from PCH_ML_OFF# to ML_OFF#		
7	40		1115		1.change 1.1VALM to 1.1VS circuit follow QAWYA 2. remove R138,Q158,R140(include discharge of 1.2VS and 2.5VS) 3.change SUSP reverse circuit follow QAWYA 4.change SYSON reverse circuit follow QAWYA 5.remove VLDI_EN reverse circuit 6.add +1.5V to +1.5VS follow QAWYA		
8	13		1116		1.change netname from LAN_CLKREQ# to CLKREQ_LAN#		
9	13		1116A		1.change netname from WLAN_CLKREQ# to CLKREQ_WLAN#		
10	13,27,30,37		1116B		1.CMOS change port from port1 to port3 2.WLAN change port from port7 to port2 3.USB(B)change port from port8 to port0		
11	35		1119C		1.change netname from +3V_PCH to +3VALM		
12	11		1119D		1.remove R84		
13	7		1119D		1.change net name from APU_VDD_BUN_FB_L to APU_VDD_SEN_L 2.change net name from APU_VDD_SEN to APU_VDD_SEN_H 3. change net name from APU_VDDNB_SEN to APU_VDDNB_SEN_H		
14	20		1119D		1.change net name from VCCSENSE_VGA to VGA_CORE_SEN 2.change net name from VSSSENSE_VGA to VGA_VSS_SEN		
15	36		1119D		1.remove EC_VGA_EN 2.remove VGA_AC_DET		
16	34		1120A		1.reserve Q96,R711		
17	7		1120C		1.remove C159,C161,C210,C164 2.change net name from LVDS_A1 to DP0_TXP1_C 3:change net name from LVDS_A1# to DP0_TXM1_C		
18	26		1120C		1.add RP26,R241,R242		
19	26		1121C		1.remove R301,R302,R826,C422,U11		
20	27		1121C		1.remove R687		
21	19		1122		1.remove CV54,CV55,CV56,CV57,CV58,CV59		
22	20		1122		1.remove CV96,CV97		
23	36		1122A		1.remove C431,R305,C438,C439		
24	7,26,36		1123A		1.remove C113,C115,RP26,R239-242 for eDP circuit 2.add R826 3.add "ENBK1"signal 4. change EC GPIO(VGATE and EC_TS_ON)		
25	17,33,39		1126A		1. Change C736 from SGA00003000 to SE00000780 2. Remove Q11 3. Set RV24,RV25,OV3 are 8 4. Add REMOTE1+ to UV1.AP29 & REMOTE1- to UV1.AG29		
26	38		1127		1. Change net name from +3VGS to +1.8VGS on U71 pin11		
27	27		1127A		1.Change net name from DISPOFF# to BKOFF# 2.update P04 table		
28	33		1127A		1add ZZZ for MB PCB		

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	11,18,31,38		1128		1.remove R801,R207,RV40,RL13,CL27 for GCLK circuit 2.GCLK circuit in p.38		
30	31		1128		1.remove GCLK# in RL3,CL7,OL1 2.change LLI P/N to SH100008W00		
31	37		1128		1.change U40 P/N to SA00005LN00		
32	28		1128A		1.change RP22 to RV94-RV96		
33	32		1128B		1.change CL30 P/N to SE067102K80		
34	11		1128B		1.change CLK_PCIE_LAN/CLK_PCIE_LAN# form port0 to port3 2.change CLK_PCIE_MLAN1/CLK_PCIE_MLAN1# from port1 to port2		
35	28		1128B		1.add R3334,R3335		
36	26		1129		1.add RA10,RA11,RA15,RA24,R1459,R1460		
37	36,41		1129		1.add signal*ADP_ID_CLOSE*for smart adapter function		
38	32,33		1130		1.remove OPT# of C587 2.change from @EMI# to EMI# for CL30		
39	5,16		1130		1.change cap form .22u to .1u for PCIE Gen2		
40	35		1130		1.change shot pad to .1u for CA64-CA66		
41	39		1204		1.change JTS1 conn to SP010013W10		
42	12,30		1204A		1.remove BT_ON#, add BT_DISABLE#		
43	07		1204A		1.RP9.4 connect to +1.5V_APU,R348.1 connect to +1.5VS for leakage issue		
44	11,18,31,38		1204B		1.add R801,R207,RV40,RL13,CL27 for GCLK circuit 2.add GCLK circuit in p.38		
45	36		1205		1.change net name form NOV0# to EC_FAN_PWM in EC 2.change net name form EC_FAN_PWM to NOV0# in EC 3.change net name form ENBK1 to APU_IMON in EC 4.change net name form APU_IMON to ENBK1 in EC		
46	38		1206		1.change RG2 to 10ohm, RG3 to 33ohm, RG4 to 33ohm 2.U74.2 change from +3V_LAN to +3VALM		
47	39		1206A		1.change C736 to SE00000PL00 (0805 package)		
48	38		1210		1.add GCLK# in RG2, RG3, RG4		
49	55,56		1210A		1.add P55,P56		
50	03,12,33,37,39		1212		1.update BOM Structure Table 2.change U3 symbol to SA00003K820 3.change U35,U36 symbol to SA00003TV00 4.change U99 P/N to SA000012710		
51	41-52		1213		1.update PWR circuit for BOM		
52	20		1220		1.change LV7 BOM structure from PX# to SHORT PAD#		
53	40		1220		1.remove @ in Q157A		
54	20		1224		1.add TEST POINT# to TV15		
55	18		1224		1.change net name from PXS_PWREN to PXS_PWREN# in QV2.2		
56	28		1224		1.remove C528 based on LA-9901 DVT schematic		
57	37		1224		1.change JK#1 from SP01000WK00 to SP010011A00 2.change JTPL,JPWRB1 from SP010014M10 to SP010010T00		
58	34		1224		1.change JODD2 from SP01001FJ00 to SP010016C00		

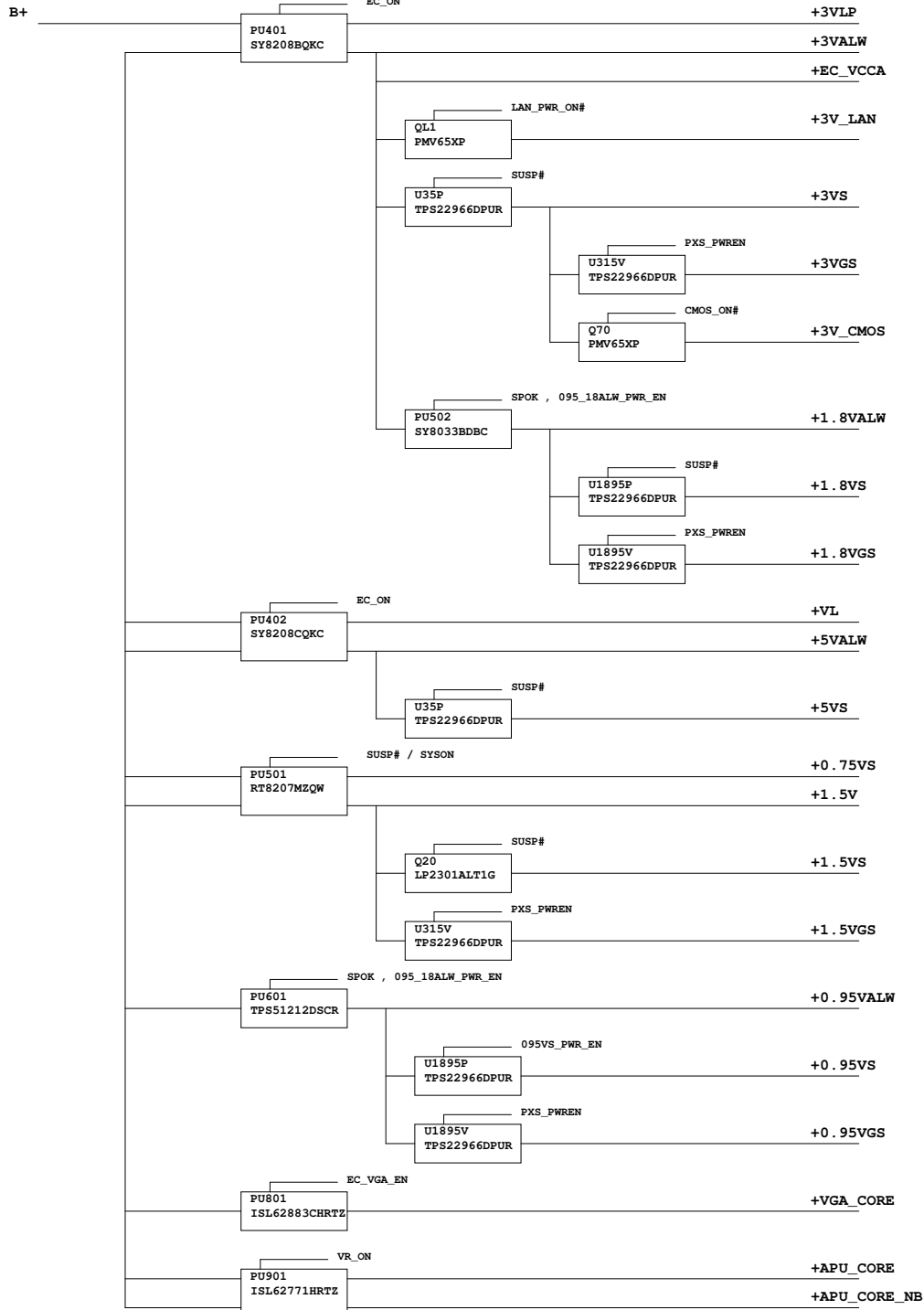
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59	35		1224		1.change JSPK1 from SP02000RR00 to SP02000H700		
60	37		1224		1.change JLED1 from SP01001A900 to SP010010T00		
61	33		1225		1.change U99 from SA000012710 to SA000067P00		
62	24,25		1225		1.change CHB form PX8 to MARS8		
63	26		1225		1.change Panel PWM circuit 2132R8		
63	29		1225		1.change Q93 & Q95 to Q93A & Q93B		
64	27		0105		1.Change BID R311=>18K		
65	35		0107		1.RA12,RA16 change to 100-ohm., RA13, RA14 to 15-ohm, ADD CA27,CA28 to IuF		
65	36		0108		1.add FXS_PWREN & EC_VGA_EN		
66	14 , 34		0108		1.Change R177 ,180 & R550 from 0805 short pad to Jumper (J14, J15, & J10)		
66	35		0110		1.RA22=>DEBUG8 for Beep 2. CA28 CA27=>2.2u for THD+N		
67	27, 32 and 37		0110		1.R813=>220 ohm Bead 2.Add C492 for EMI request 3.DLL1=>EMI8		
68	33		0111		1.ADD ZZ2 & ZZ1 for 14*_DIS & 15*_DIS pcb		
69	12		0114		1.ADD GF1054 for RTD2132R8 2.change U99		
70	33		0116		1.change H21 from 2P8 to 4P6 2.change U99 to 1001101x (4D)		
71	39		0116		1.add C737 & C7358 for USB droop (follow Intel)		
72			0121		1.change D24 to SCA00001G00 for ESD request		
73	28		0121		1.L30, L31 & L32 downsize to 0402,SM010005X00		
74	39		0121		1/21 L51,L55,L58 & L66 change PN to SM070001N00 for action plan		
75	29		0121		1/21 L35,L36,L37 & L38(HDMI) L49,L50,L53 & L54(USB3) change PN from SM070001S00 to SM070003K00 for action plan		
76	10		0126		SIT: change C145 from OS-Con to POLY		
77	37		0129		1/29 SIT: Del R806 & Q12 for change audio type from normal close to normal open.		
78	36		0201		2/1 SIV: add PU resistor for LID_SW#		
79	35		0221		1.upgrade capacitors of CA36 & CA46 from 1uF to 2.2uF/X5R 2.AVDD_HP connect to standby power rail (+3VLP) for prevent speaker hum noise issue.		
80	20		0221		1.Change Cap of CV66 to 220U 4V Y D2 ESR15M = SGA00000Y80 for PWR request		
81	38		0221		1.add CG5 on 1.8VGS for GCLK 2.reserve CG6 & CG7 for vender request.		
82	22-25		0221		1. p22 & p23=>Channel B Mars8 2.p24 & p25=>ChannelA FX8		
83	35		0225		1. add speaker bypass Cap CA38,CA39,CA40 & CA43 for EMI requirement		
84	07		0226		1. add C438 100pF on H_THERMTRIP# for ESD requirement		
85	34		0301		SIT: 3/1 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_A5F98-2231S10-0002_22P (DC010005N00 toDC010009C00)		
86	34		0301		Del CV168 ,CV159,CV160 & CV189 for VRAM body size issue		
87	37		0301		change C492, SE00000FB80 to SE074331K80 by Sourcer requiremnt.		
88			0301		LV4,LV10,L3,L6,L9,L11,L16 L77 Downsize to 0402 BLM15AX221SN1D (Murata) ,SM01000MR00 by Sourcer requiremnt.		
89	36		0301		Add R311=8.2K for SIT		
90	11		0301		Change R85 from 0 ohm short pad 8 to 33 ohm EMI8		

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91	26		0301		1.add R1461 for RTD2132R ,MIIC_SDA :MIIC_SCL=0 : 1		
92	35		0301		1.Change +VDDIO_HDA power rail from +3VALW to +3VS.		
93	26		0304		1.add R1462 for RTD2132R ,MIIC_SDA :MIIC_SCL=0 : 1 2.Del RP16.3 & RP16.4		
94	12,13		0304		1.Change R367 from 10K to 100K. 2.Change R234 from 10K to 100K		
94	32		0305		1.add CL32 & CL33 for ESD request.		
95	32		0306		1.add R236 & R237 (LVDS_SEU) for C build only.		
96	8		0306		1.add J3 for 1.5V		
96	33		0306		1.Change Power rail of the U99 from +3VS to +3VGS.		
97	12		0306		1.Change Power rail of the GP1054 from +3VALW to +3VS.		
98	12		0307		1.Change +1.5GV5 enable pin from +VSB to +5Valw for Eup lot 6.		
99	12,36		0311		1.Change BOM structure of R367 & R368 to 8,2132S only 2.R237 & R236 =>8		
Pre-MP 100	33		0311		1.Change U99 to SA000012710		
Pre-MP 101	12,36 & 26		0403		1.Reduce part count for RTD2132R only		
Pre-MP 102	12,36 & 26		0403		1.Reduce part count for RTD2132R only		
Pre-MP 103	34		0403		1.ODD Power Control cuicuits =>8		
Pre-MP 104	33		0410		1.Change H17 form H_8PON to H_7PON SD309100280		
Pre-MP 105	36		0410		1.Change RP11 form SD309100280(10K) to SD309100300(100K)		
Pre-MP 106	18		0410		1.Change RV41 to 47K for Erp Lot6		
Pre-MP 107	18		0410		1.Change RV37 from 20Kto 100K ,RV38 from 20K to 0 ohm.		
Pre-MP 108	18		0410		1.Change RV37 from 20Kto 100K ,RV38 from 20K to 0 ohm.		
Pre-MP 109	36		0411		1.Del Net VLDI_EN & IV_ALM_EN		
Pre-MP 110	7, 13		0412		1.change C438 from 100p to 1000p. 2. add C439, 1000p for ESD request.		

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