UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :None Installed
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CRV:Chief River

JV10-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
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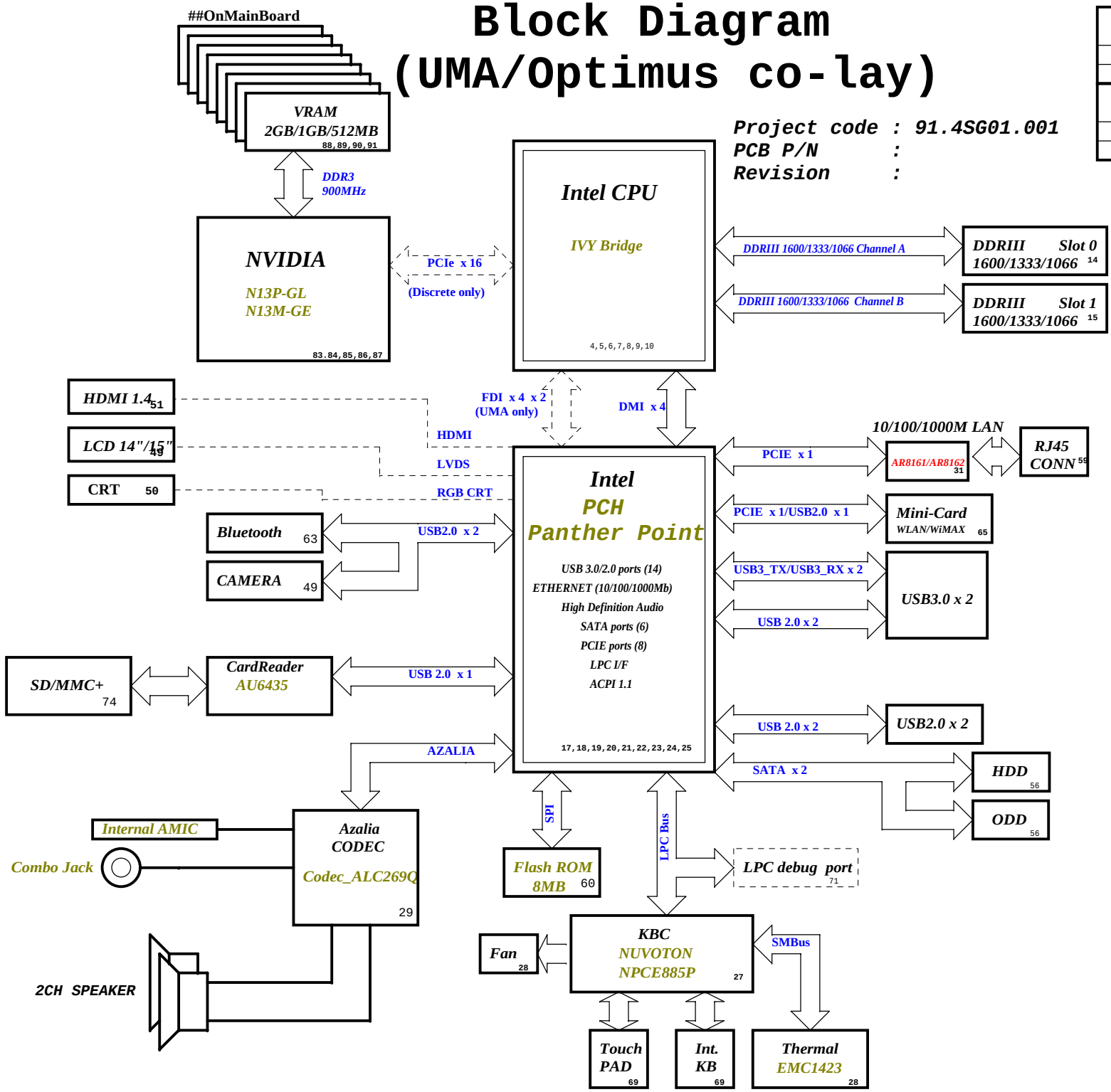
Block Diagram (UMA/Optimus co-lay)

##OnMainBoard

Project code : 91.4SG01.001
PCB P/N :
Revision :



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	VCCSA

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC G977F 45	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA ISL62882C 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24745 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

VGA switchs 93	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

All Not update

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	N/A
1	HDD1
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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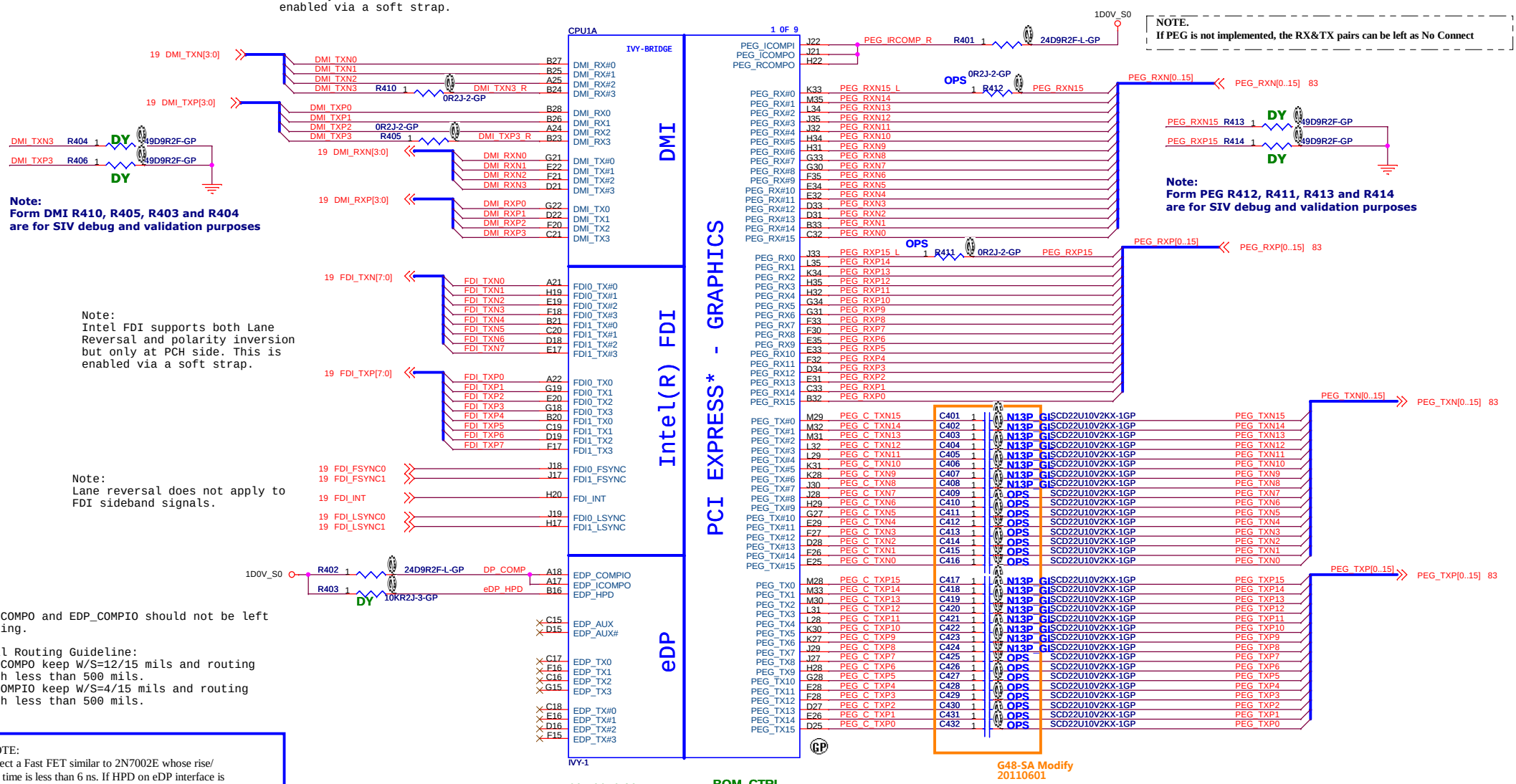
SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Form DMI R410, R405, R403 and R404 are for SIV debug and validation purposes

Note:
Form PEG R412, R411, R413 and R414 are for SIV debug and validation purposes

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

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Title	CPU (PCIE/DMI/FDI)		
Size A3	Document Number G48/G58		Rev SC
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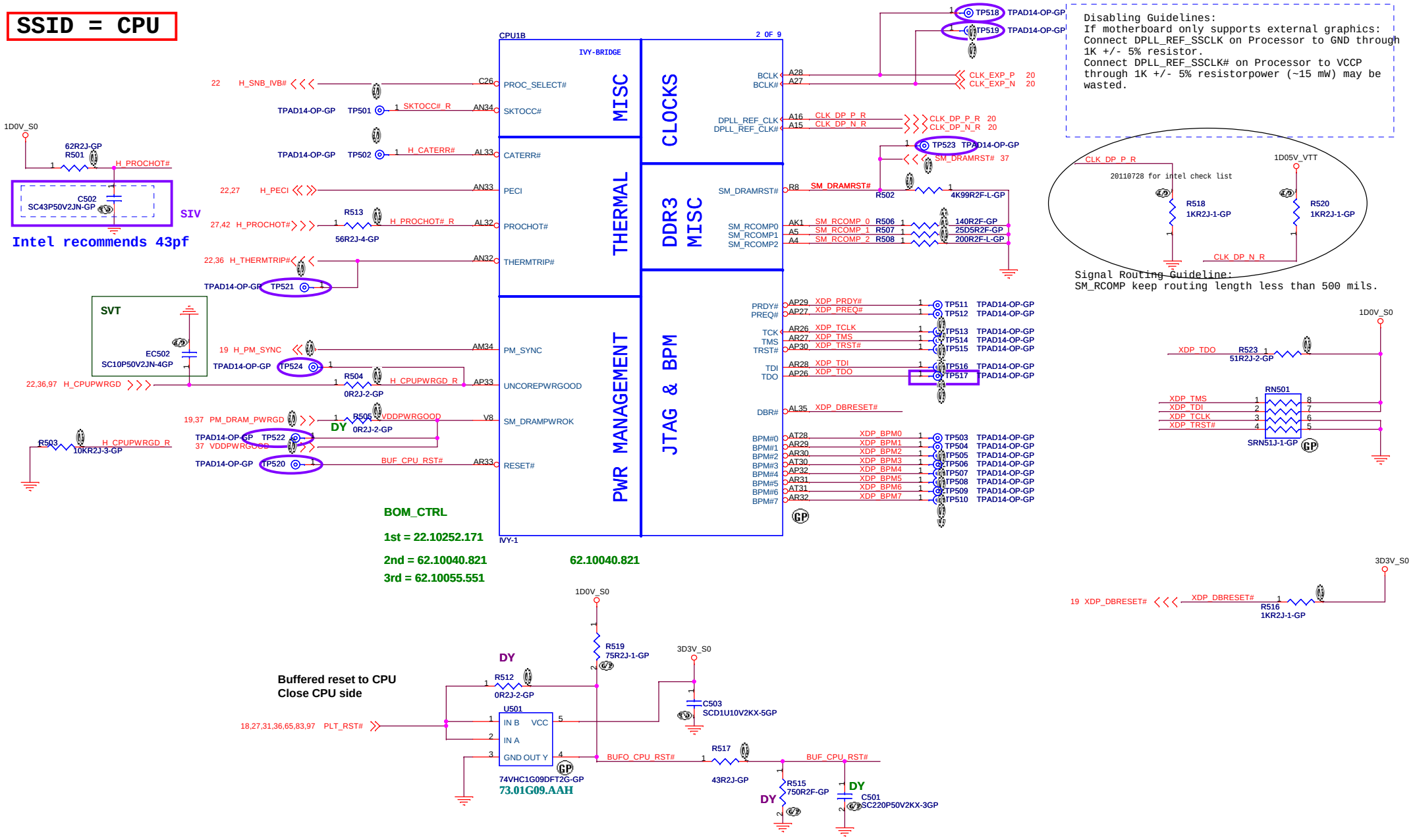
SSID = CPU



NOTE

	U501	R512	R519	R517	R515	C503	C501
HR	DY	0 ohm 63.R0034.1DL	DY	1.5K ohm 64.15015.6DL	750 ohm 64.75005.6DL	DY	DY
CRV	73.01G09.AAH	DY	75 ohm 63.75034.1DL	43 ohm 63.43034.1DL	DY	0.1uF 78.10423.2FL	DY

Default CRV

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Title	THERMAL/CLOCK/PM	
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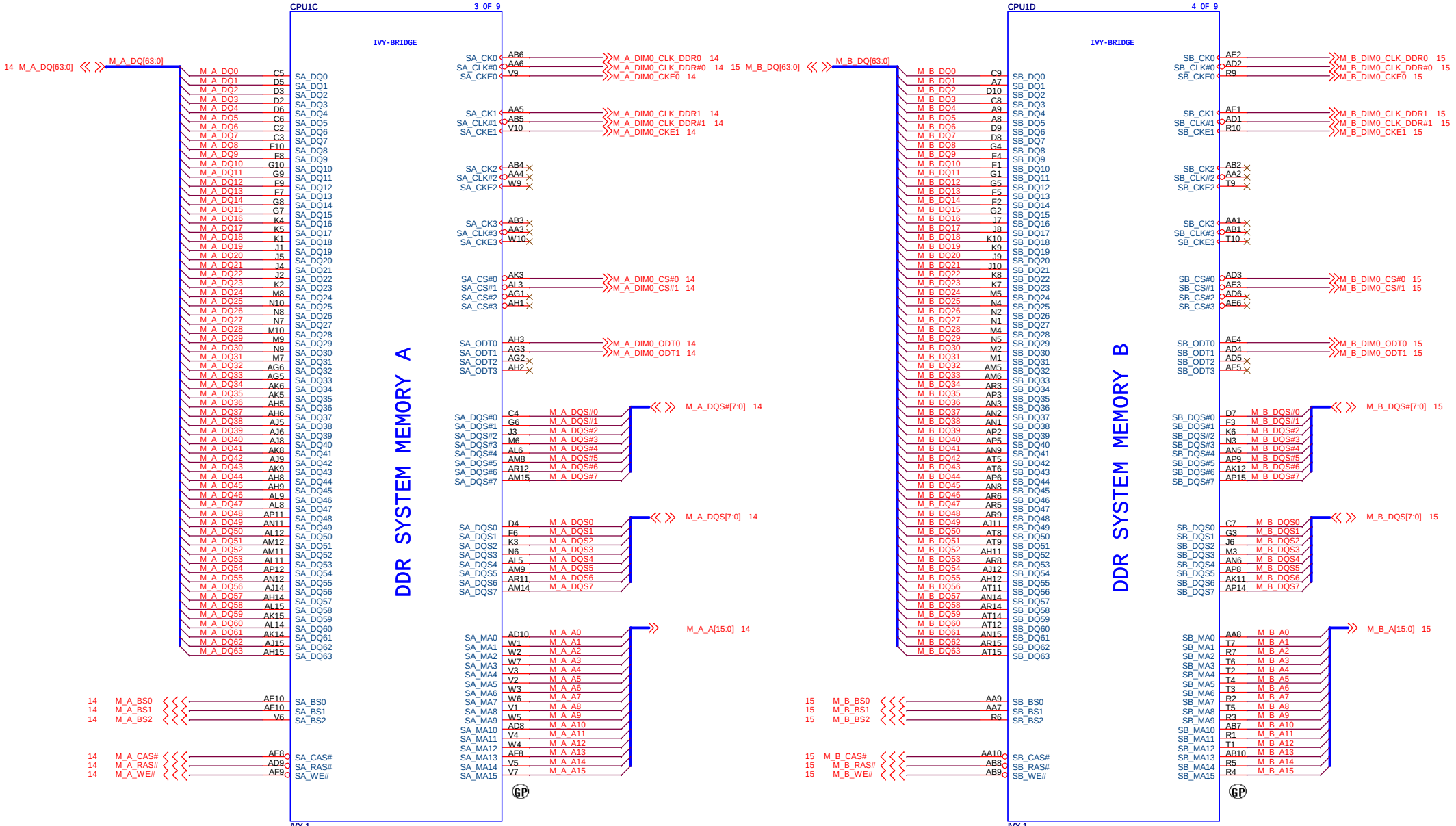
SSID = CPU



62.10040.821

BOM_CTRL

1st = 22.10252.171
2nd = 62.10040.821
3rd = 62.10055.551

62.10040.821

BOM_CTRL

1st = 22.10252.171

2nd = 62.10040.821

3rd = 62.10055.551

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Title: *CPU (DDR)*		
Size: A3	Document Number: G48/G58	Rev: SC
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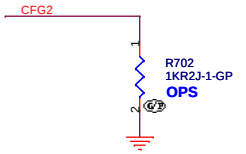
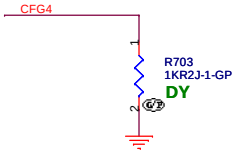
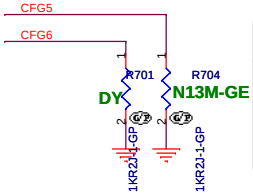
SSID = CPU



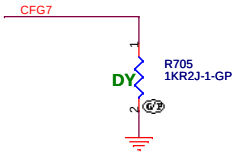
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition **0:Lane Reversed**



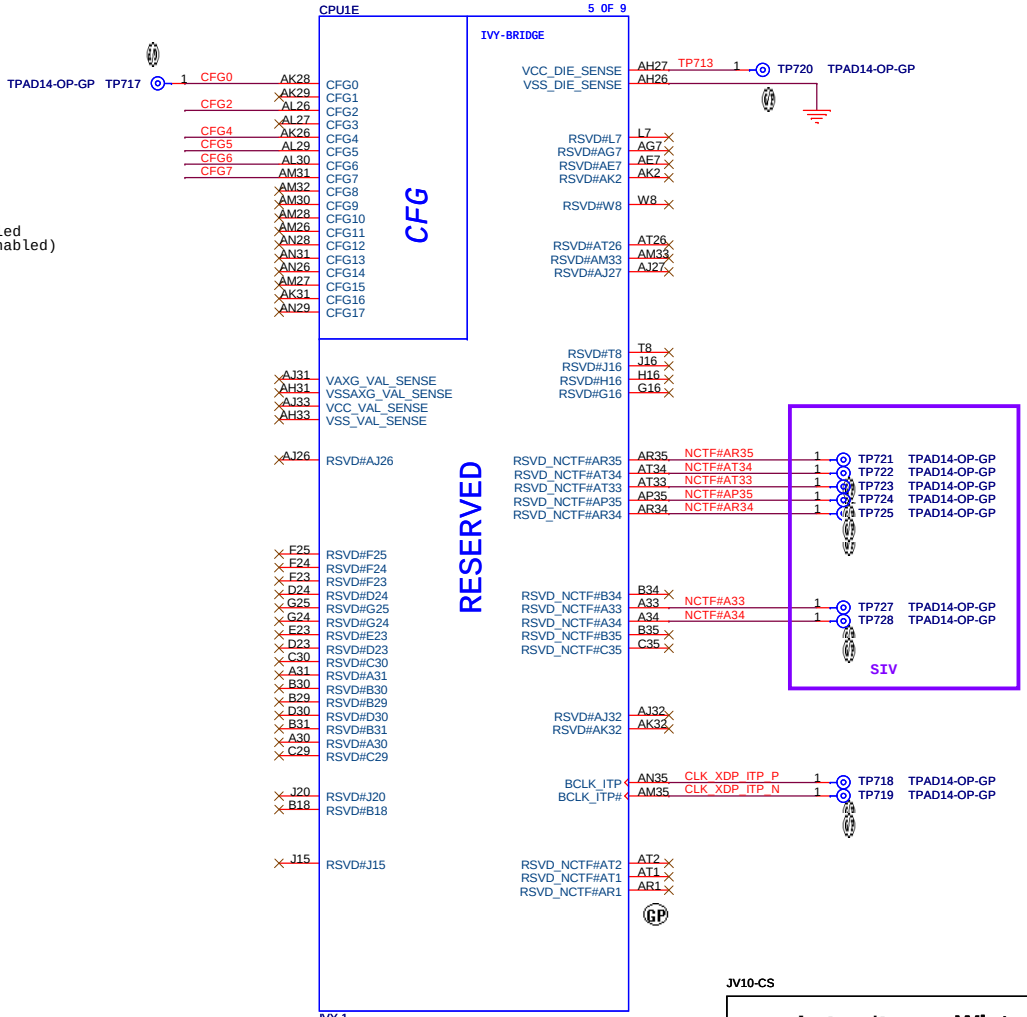
Display Port Presence Strap	
CFG4	**1: Disabled; No Physical Display Port attached to Embedded Display Port** 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	**11: x16 - Device 1 functions 1 and 2 disabled** 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	**1: PEG Train immediately following xxRESETB de assertion** 0: PEG Wait for BIOS for training



IVY-1

62.10040.821

BOM_CTRL

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SSID = CPU

POWER

CPU1F

6 OF 9

IVY-BRIDGE

PEG AND DDR

SVID

SENSE LINES

CORE SUPPLY

VCC_CORE

VCC CORE:53A

VCCIO:8.5A

1D0V_S0

-to 17pcs

TC8xx

470uF x2

R807 need to close to CPU

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7

For CRB VIDALERT# need to pull high 75 ohm close to CPU

R801, R802 need to close to CPU

BOM_CTRL

IVY-1

62.10040.821

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Title: mCPU (VCC_CORE)

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SSID = CPU

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

POWER

M3 - Processor Generated SO-DIMM VREF_DQ

M_VREF_DQ_DIMM0 — R915 1 — DY — 0R2J-2-GP
M_VREF_CA_DIMM0 — R916 1 — DY — 0R2J-2-GP
RN903 SRN1KJ-7-GP DY
12 DDR_WR_VREF01
12 DDR_WR_VREF02

VCC_GFXCORE

CPU1G — 7 OF 9 — IVY-BRIDGE

SENSE LINES
VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF
SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37
SA_DIMM_VREFDQ — B4
SB_DIMM_VREFDQ — D1

GRAPHICS VAXG1–VAXG54

DDR3 -1.5V RAILS
VDDQ1–VDDQ15: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

PROCESSOR VDDQ: 12A
C909–C914: SC10U6D3V5KX-1GP
SIV — TC902 ST330U2D5VDM-17GP — DY — 1D5V_S0
TC9xx 330uF

SA RAIL
VCCSA1–VCCSA8: M27, M26, L26, J26, J25, J24, H26, H25

PROCESSOR VCCSA: 6A
VCCSA
C916, C915, C917: SC10U6D3V5KX-1GP
TC9xx 330uF

R902 need be close to pin H23.

MISC
VCCSA_SENSE — H23 — VCCSA_SENSE — VCCSA_SENSE 48
VCCSA_VID0 — C22 — VCCSA_SELECT0 48
VCCSA_VID1 — C24 — VCCSA_SELECT1 48
VCC_IO_SEL — A19 — GP

1.8V RAIL
VCCPLL1–VCCPLL3: B6, A6, A2

1D8V_S0
VCCPLL:1.5A
C925: SC10U6D3V5KX-1GP
C923: SC10U6D3V5KX-1GP
C922: SC1U10V2KX-1GP
C924: SC1U10V2KX-1GP
TC9xx 330uF

IVY-1

62.10040.821

BOM_CTRL
SIV
3D3V_S5
R913 10KR2F-2-GP DY
ES2 dummy R913
H_VCC_SEL

1D0V_S0
R917 10KR2J-3-GP DY — VCCSA_SELECT0
R920 10KR2J-3-GP DY — VCCSA_SELECT1
R918 1KR2J-1-GP
R919 1KR2J-1-GP
SIT

Close to CPU
VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U
SIV for intel recommend

NOTE

	R906/R907
HR	100 ohm 64.10005.6DL
CRV	10 ohm 64.10R05.6DL

Default CRV

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Title: mCPU (VCC_GFXCORE)
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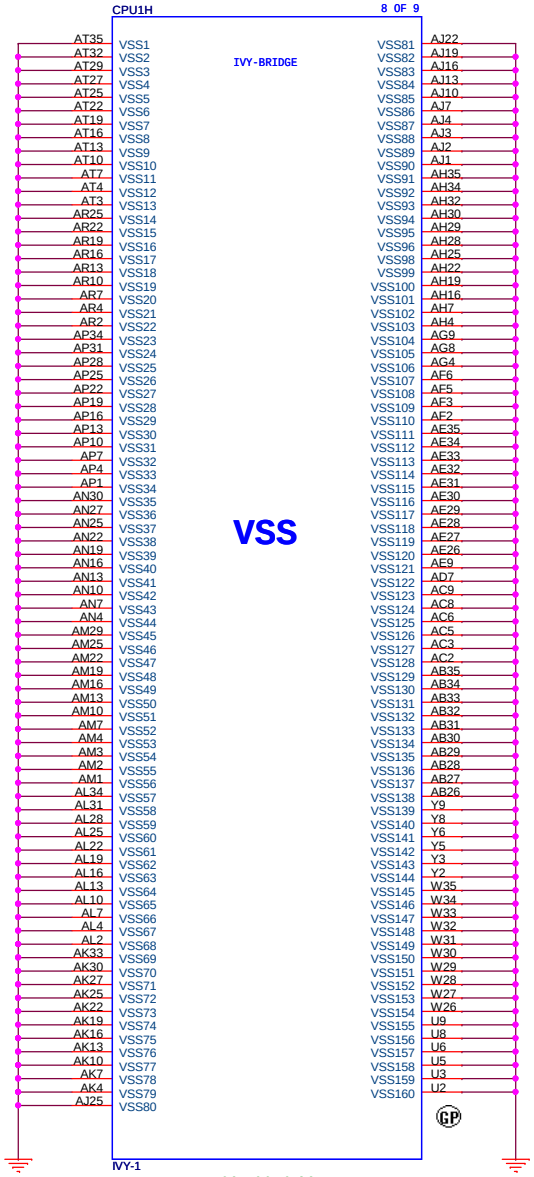
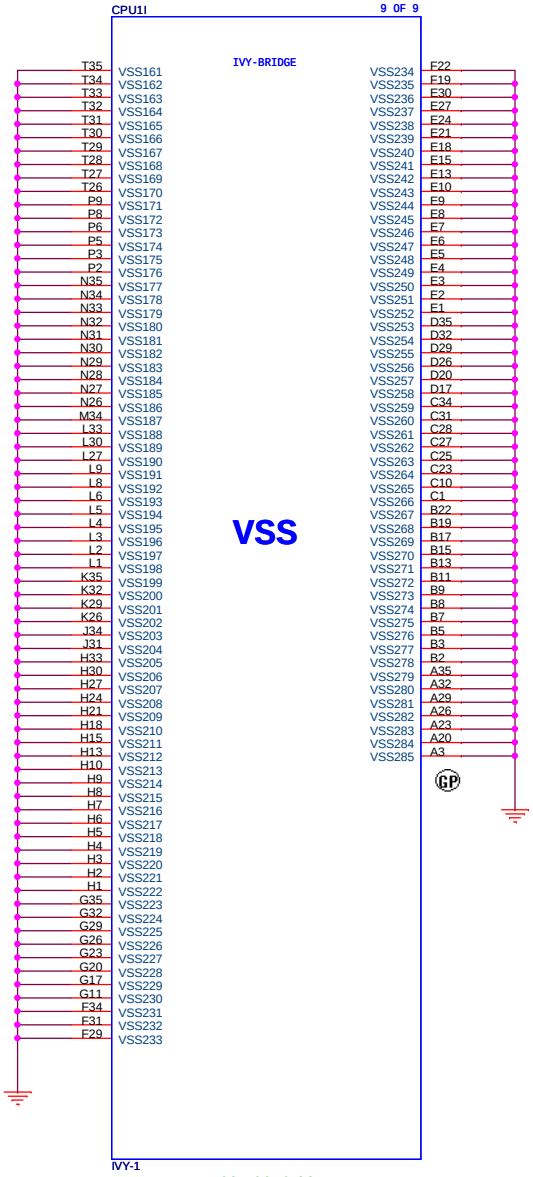
SSID = CPU



62.10040.821

BOM_CTRL



62.10040.821

BOM_CTRL

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Title	***XDP***	
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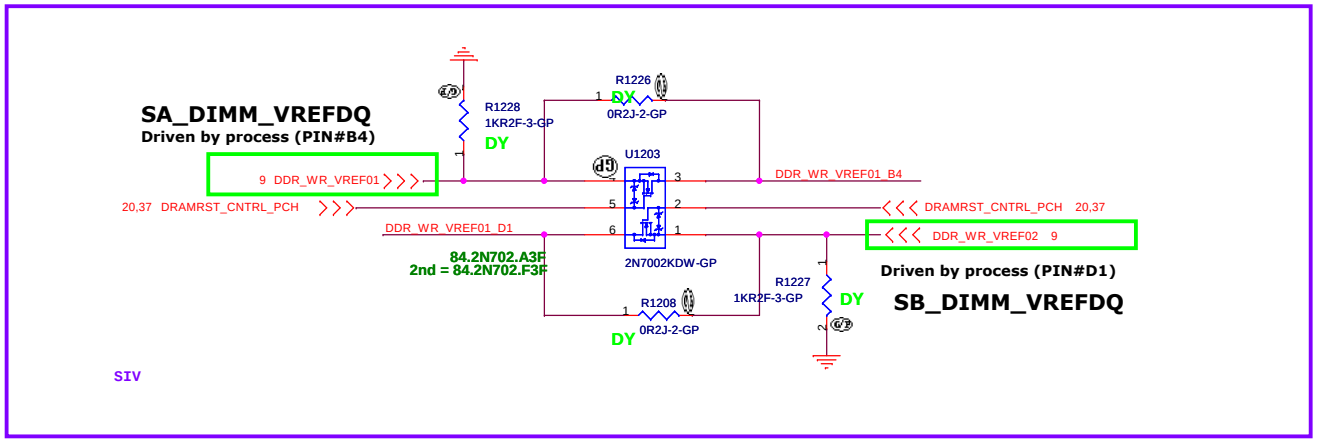
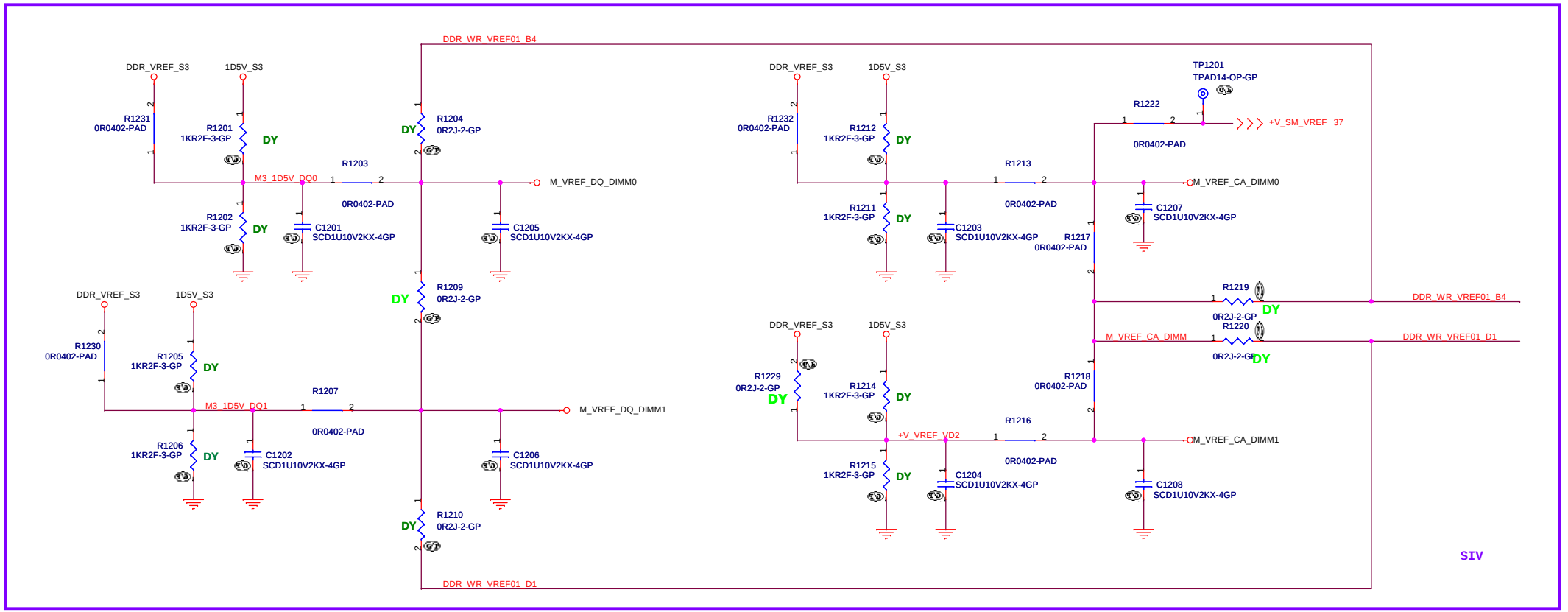
VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

For CRV:





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Title	*M1 & M3 Implementation*	
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(Blanking)

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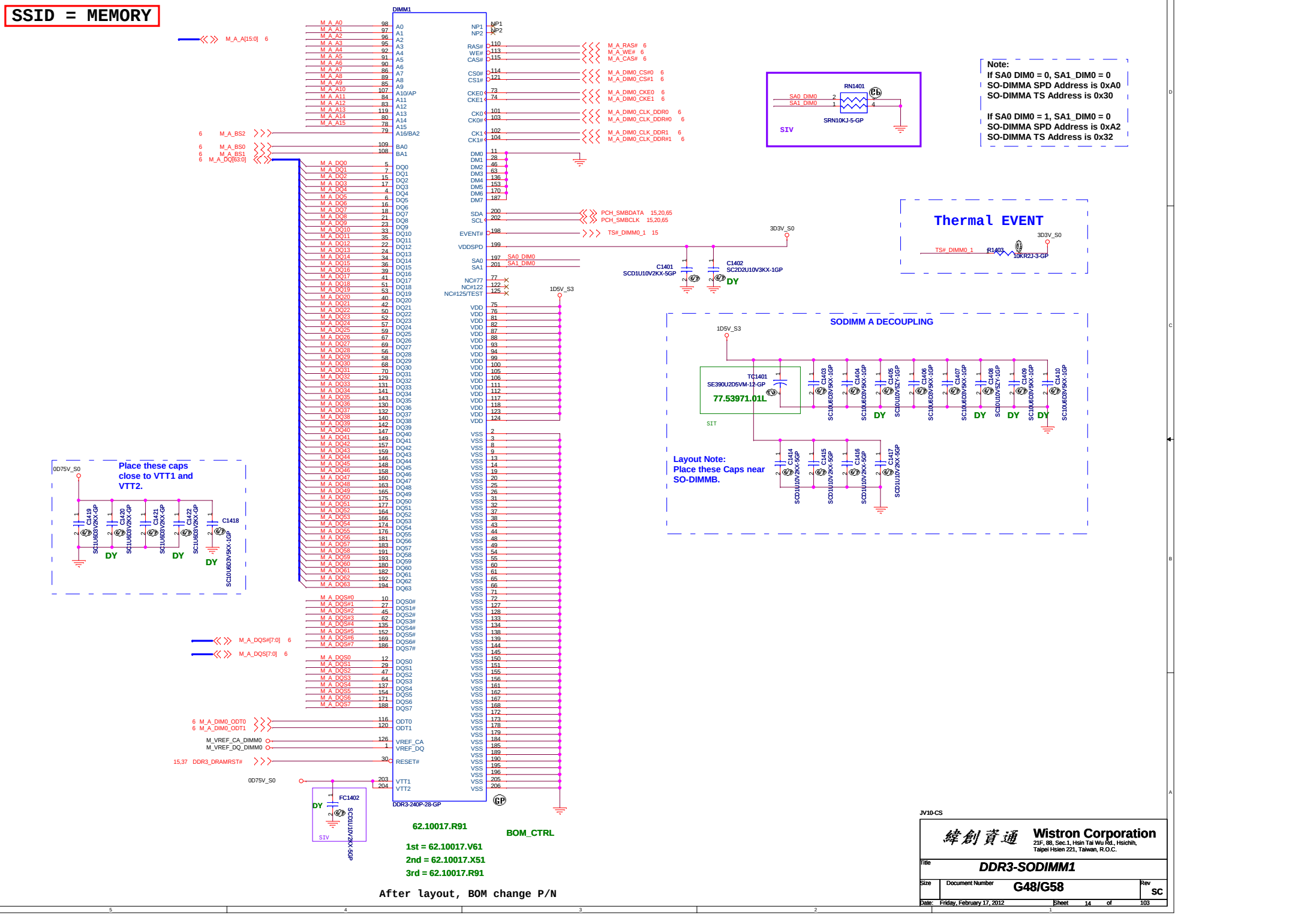
SSID = MEMORY



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Title: **DDR3-SODIMM1**

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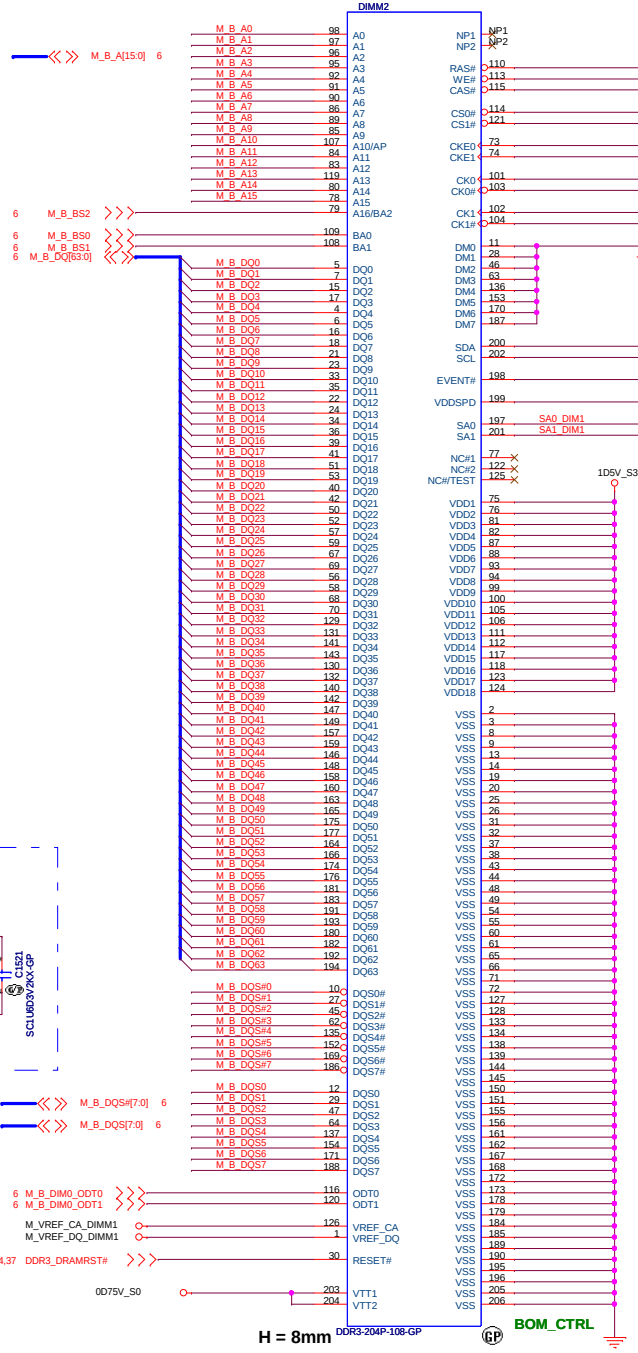
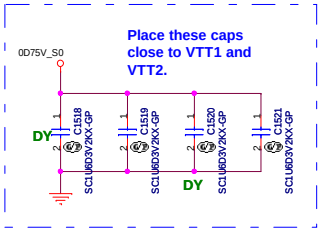
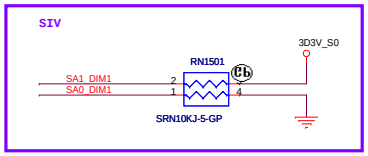
SSID = MEMORY



H = 8mm

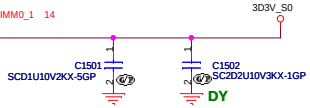
Place these caps close to VTT1 and VTT2.

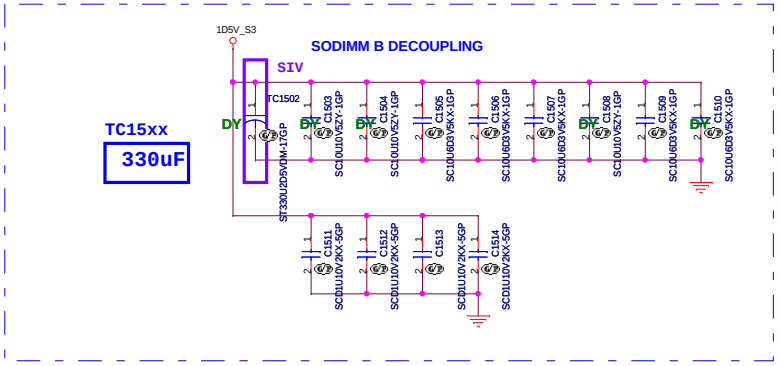




Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA





After layout, BOM change P/N

62.10017.X41

1st = 62.10024.G21

2nd = 62.10017.X41

3rd = 62.10017.M51

JV10-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
	G48/G58	SC

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(Blanking)

JV10-CS

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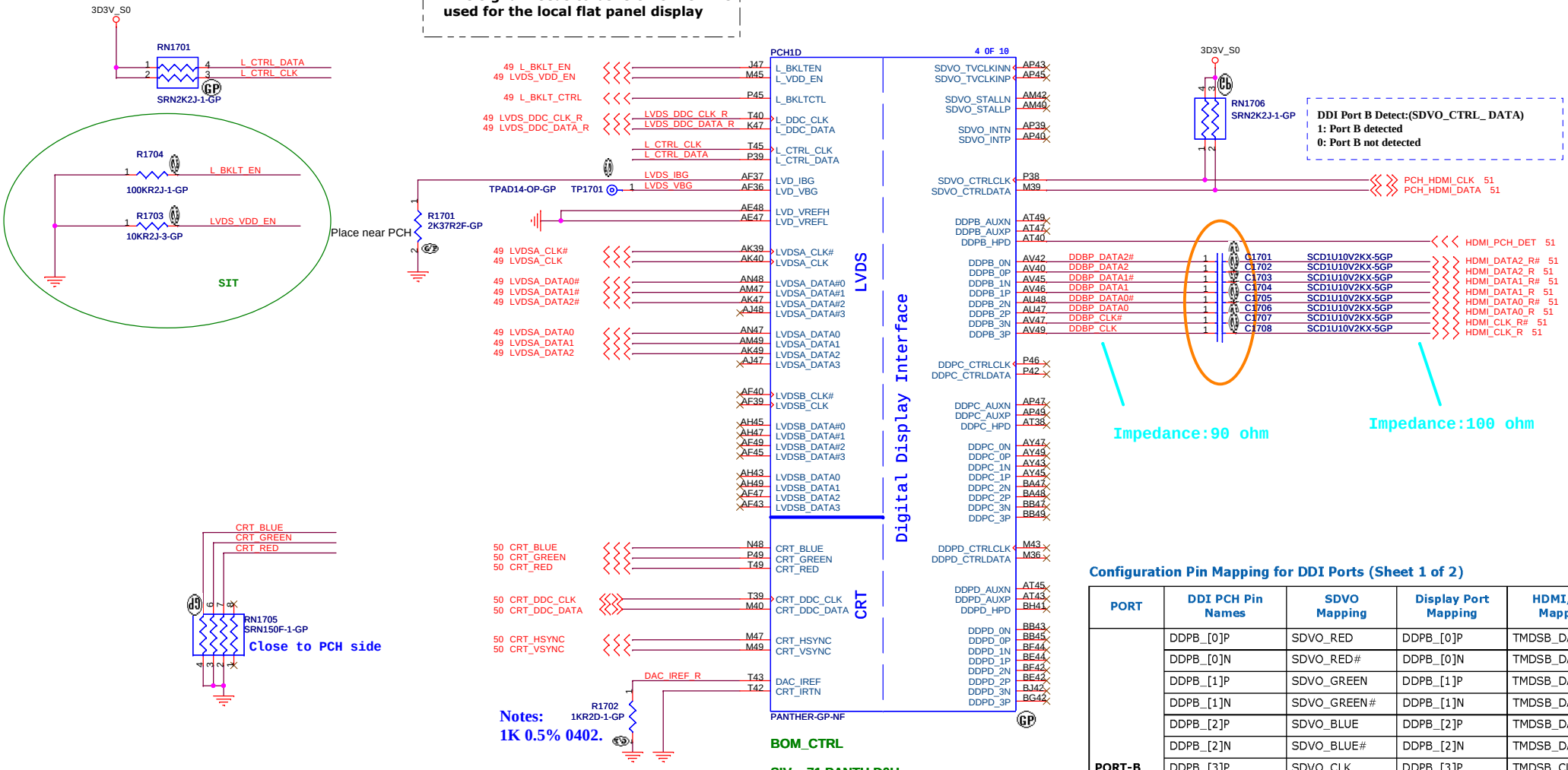
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DDR3-SODIMM3***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 16 of 103	

L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

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Title	PCH (LVDS/CRT/HDMI)	
Size	Document Number G48/G58	Rev SC
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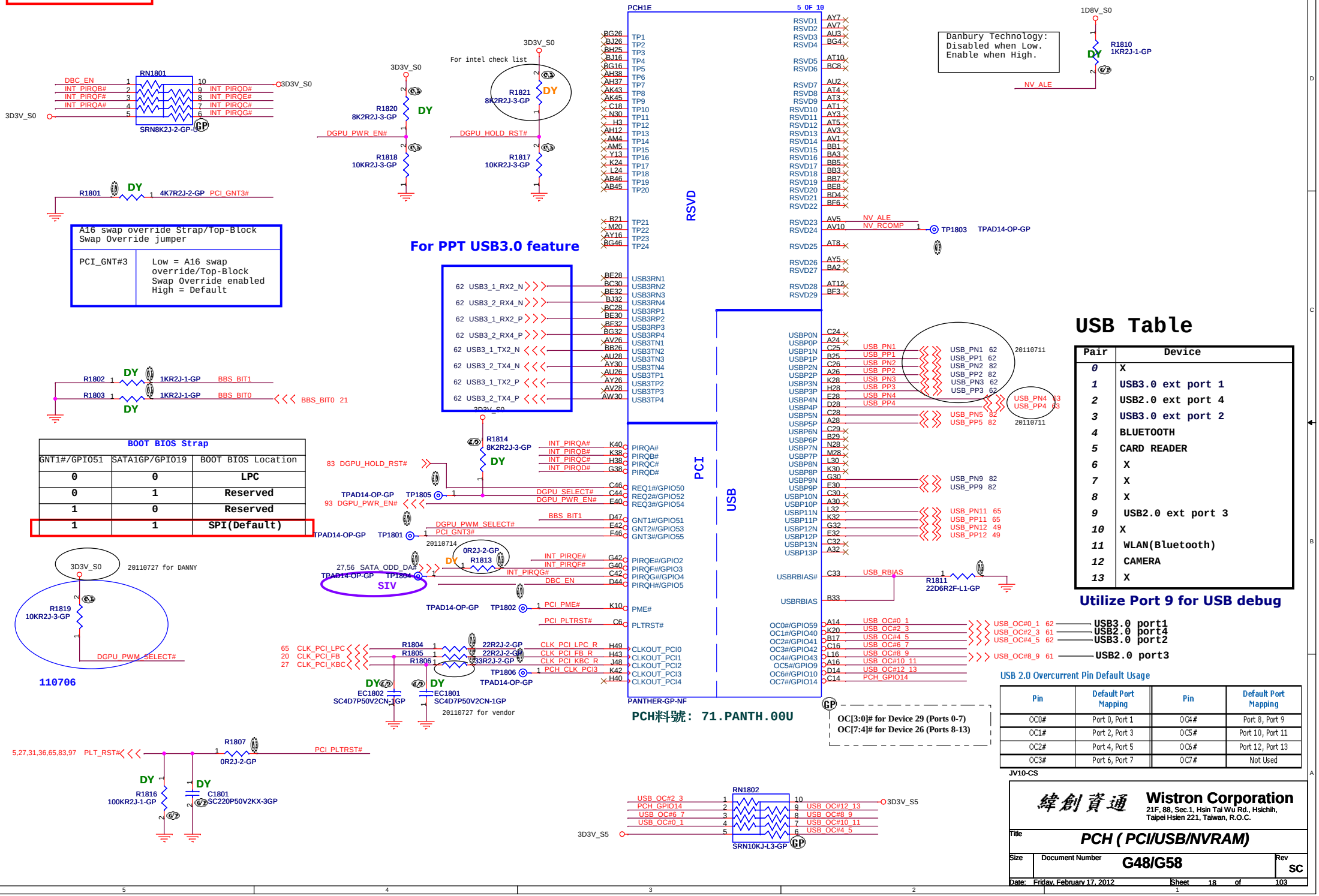
SSID = PCH



USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

Utilize Port 9 for USB debug

USB3.0 port1
USB2.0 port4
USB3.0 port2
USB2.0 port3

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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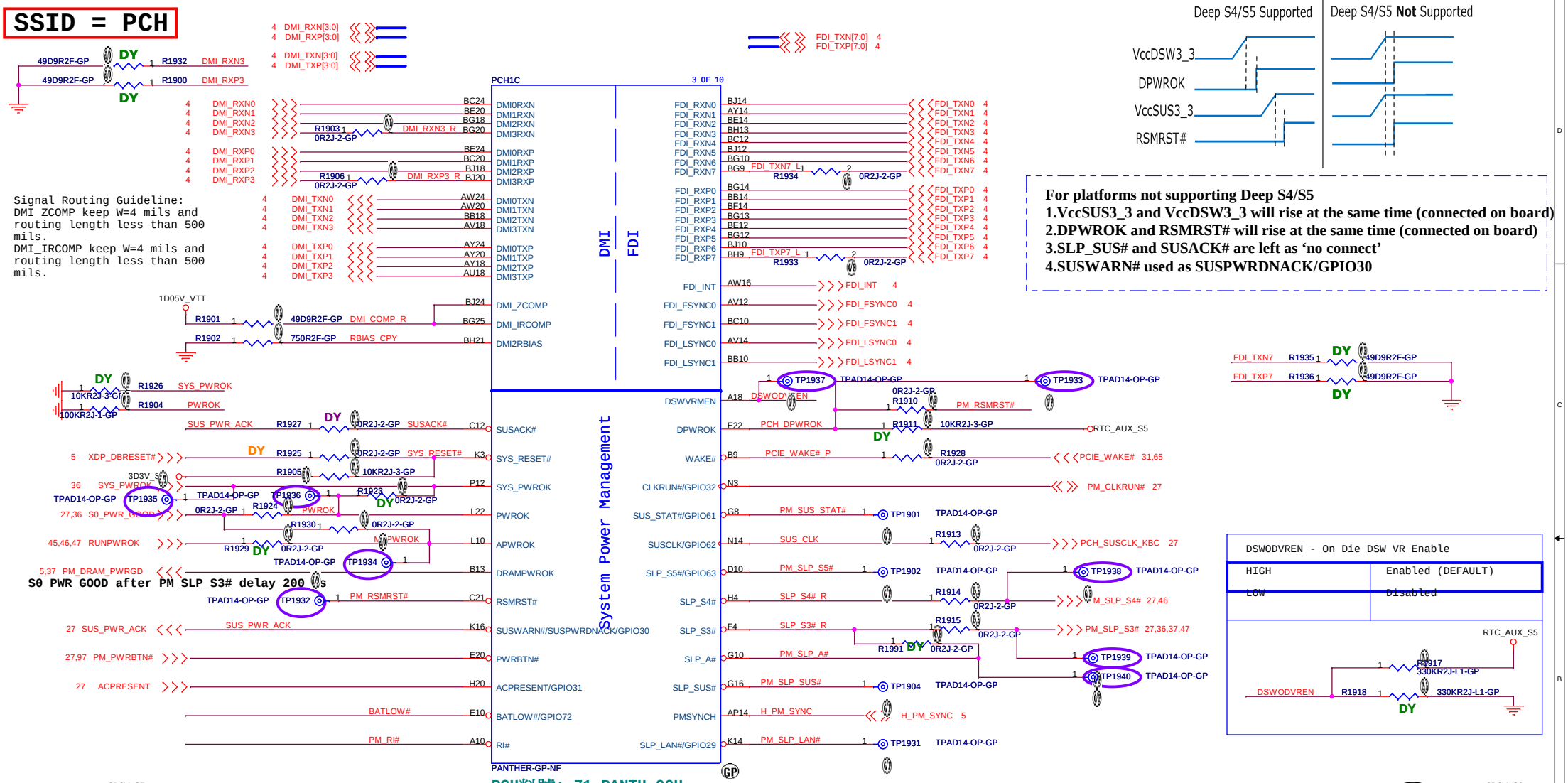
Title	PCH (PCI/USB/NVRAM)		
Size	Document Number G48/G58	Rev SC	
Date: Friday, February 17, 2012	Sheet 18 of 103		

SSID = PCH



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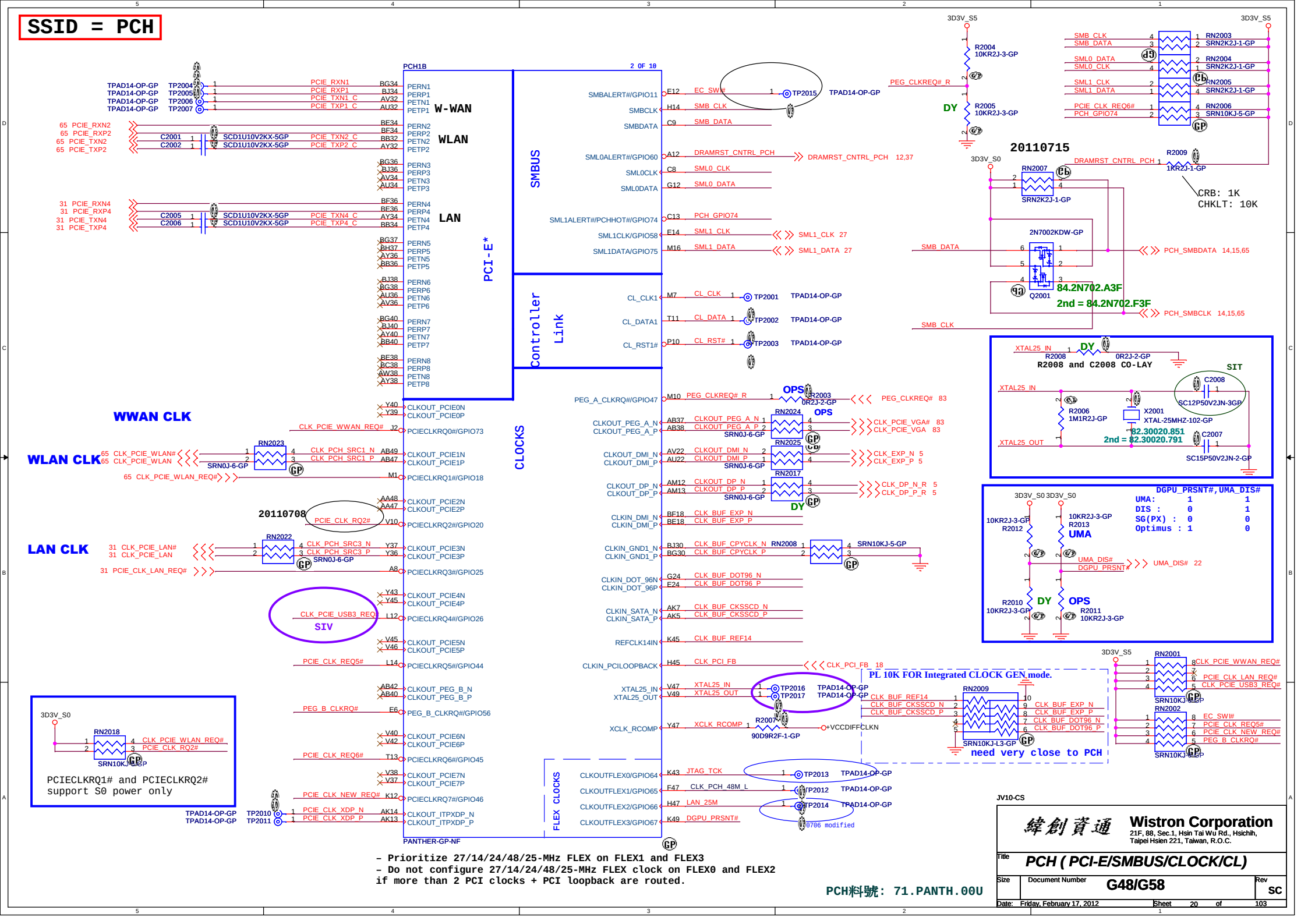
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (DMI/FDI/PM)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 19 of 103	

SSID = PCH



- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

PCH料號: 71.PANTH.00U

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Title	PCH (PCI-E/SMBUS/CLOCK/CL)		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 20 of 103		

SSID = PCH

NOTE

	R2111,R2118~R2120,R2125
HR	0 ohm 63.R0034.1DL
CRV	22 ohm 64.22R05.6DL

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide

HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap

HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V (Default) High = 1.5V

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

Move Cap close to Device or Connector.

LA37/LA57/CRV-Std:750ohm
LA47: 806 ohm

PCH料號: 71.PANTH.00U

JV10-CS

110706 modified

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Title	PCH (SPI/RTC/LPC/SATA/IHDA)	
Size	Document Number G48/G58	Rev SC
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SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

	R2202	----
HR	200K ohm 64.20035.6DL	
CRB	10K ohm 63.10334.1DL	

GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regurator, should not place external pull down.

LOW: ODD exist
HIGH: ODD non-exist

PCH_GPIO15 pull high => HM76
PCH_GPIO15 pull Low => HM70

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PCH料號: 71.PANTH.00U

JV10-CS

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Title	PCH (GPIO/CPU)		
Size	Document Number	G48/G58	Rev SC
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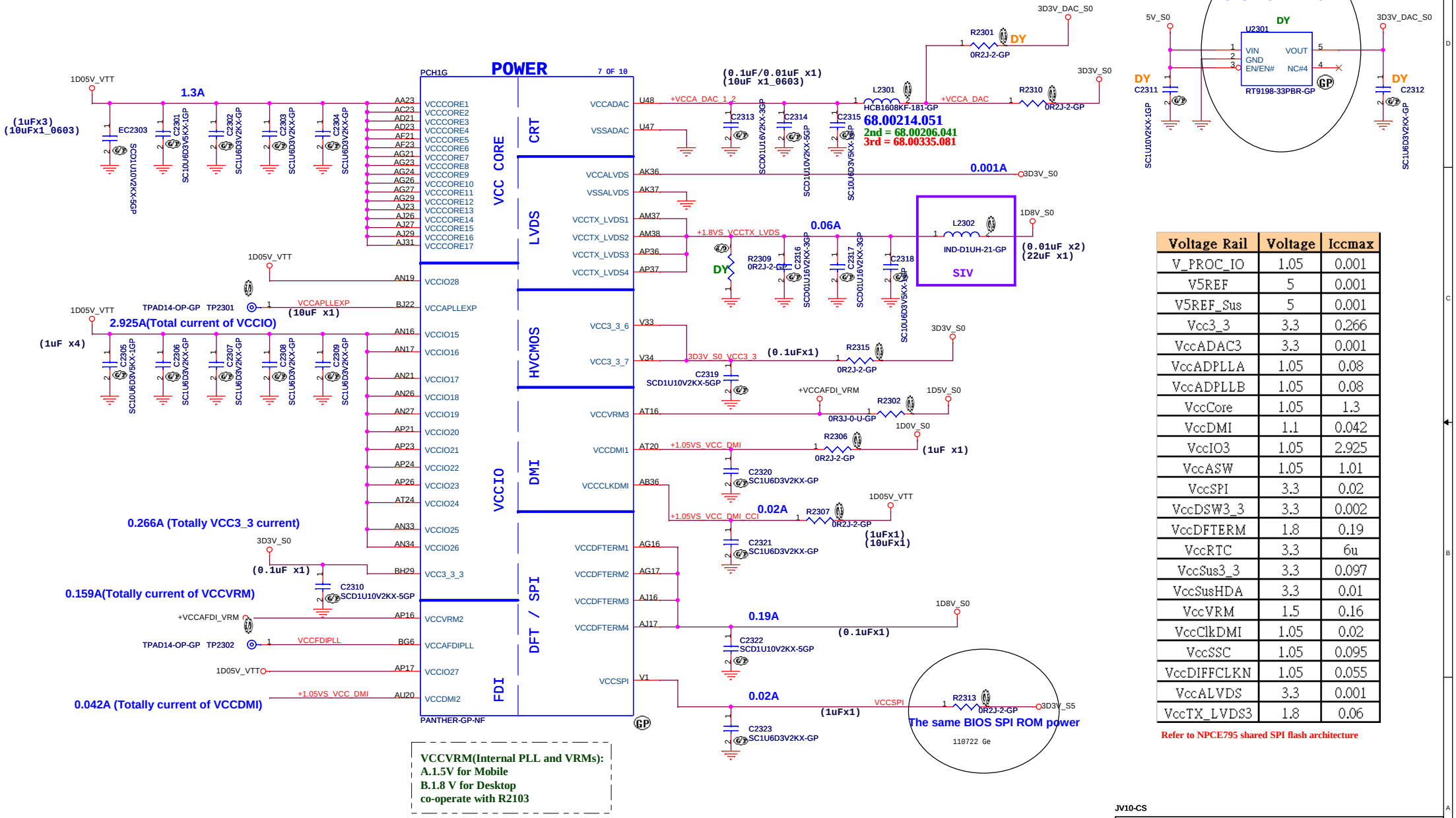
SSID = PCH 6A



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture

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Title	PCH (POWER1)	
Size	Document Number G48/G58	Rev SC
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SSID = PCH

POWER

PCH1J — 10 OF 10

Clock and Miscellaneous

- TPAD14-OP-GP TP2401 — VCCACLK — AD49 VCCACLK — 0.002A
- 3D3V_S5 (0.1uFx1) — T16 VCCDSW3_3
- TPAD14-OP-GP TP2405 — DCPSUSBYP — V12 DCPSUSBYP
- +V3.3S_VCC_CLKF33 — T38 VCC3_3_5
- TPAD14-OP-GP TP2404 — +VCCAPLL_CPY_PCH — BH23 VCCAPLLDMI2 — (10uFx1)
- 1D05V_VTT — AL29 VCCIO14
- TPAD14-OP-GP TP2402 — +VCCSUS1 — AL24 DCPSUS3

USB

- VCCIO29 N26, VCCIO30 P26, VCCIO31 P28, VCCIO32 T27, VCCIO33 T29 — 1D05V_VTT (1uFx1) — C2423 SC1U6D3V2KX-GP
- VCCSUS3_3_7 T23, VCCSUS3_3_8 T24, VCCSUS3_3_9 V23, VCCSUS3_3_10 V24 — 3D3V_S5 — 0.097A (Totally current of VCCSUS3_3) — (0.1uFx1) — C2424 SCD1U10V2KX-5GP
- VCCSUS3_3_6 P24 — 3D3V_S5 (0.1uFx1) — C2425 SCD1U10V2KX-5GP
- VCCIO34 T26 — 1D05V_VTT
- V5REF_SUS M26 — +5VA_PCH_VCC5REFSUS — 0.001A
- DCPSUS4 AN23 — +VCCA_USBSUS — TP2403 TPAD14-OP-GP
- VCCSUS3_3_1 AN24 — +V3.3A_VCCPSUS

SVT — 83.R0304.A8F / 2nd = 83.R3004.A8F — D2401 CH751H-40PT-GP — R2408 10R2J-2-GP (0.1uFx1) — C2426 SCD1U10V2KX-5GP — 3D3V_S5 / 5V_S5

SVT — 83.R0304.A8F / 2nd = 83.R3004.A8F — D2402 CH751H-40PT-GP — R2407 10R2J-2-GP (1uFx1) — C2427 SC1U10V2KX-1GP — 3D3V_S0 / 5V_S0

PCI/GPIO/LPC

- V5REF P34 — +5VS_PCH_VCC5REF — 0.001A
- VCCSUS3_3_2 N20, VCCSUS3_3_3 N22, VCCSUS3_3_4 P20, VCCSUS3_3_5 P22 — +V3.3A_VCCPSUS — R2410 0R3J-0-U-GP (1uFx1) — 3D3V_S5 — C2428 SC1U6D3V2KX-GP
- VCC3_3_1 AA16, VCC3_3_8 W16, VCC3_3_4 T34 — 3D3V_S0 (0.1uFx2) — C2430 SCD1U10V2KX-5GP — C2431 SCD1U10V2KX-5GP
- VCC3_3_2 AJ2 — 3D3V_S0 (0.1uFx1) — C2429 SCD1U10V2KX-5GP

SATA

- VCCIO5 AF13, VCCIO12 AH13, VCCIO13 AH14 — 1D05V_VTT (1uFx1) — C2432 SC1U6D3V2KX-GP
- VCCIO6 AF14, VCCAPLLSATA AK1 — +V1.05S_VCCAPLL_SATA3 — R2411 0R3J-0-U-GP (10uFx1) — 1D05V_VTT — DY C2434 SC10U6D3V5KX-1GP
- VCCVRM1 AF11 — +VCCAFDI_VRM
- VCCIO2 AC16, VCCIO3 AC17, VCCIO4 AD17 — +V1.05S_VCC_SATA — R2412 0R3J-0-U-GP (1uFx1) — 1D05V_VTT — C2435 SC1U6D3V2KX-GP

MISC

- VCCASW22 T21, VCCASW23 V21, VCCASW21 T19 — 1D05V_VTT — +3VS_+1.5VS_HDA_IO
- VCCSUSHDA P32 — 0.01A (0.1uFx1) — C2433 SCD1U10V2KX-5GP

+3VS_+1.5VS_HDA_IO — R2409 0R3J-0-U-GP — 3D3V_S5

CPU

- VCCASW1 AA19, VCCASW2 AA21, VCCASW3 AA24, VCCASW4 AA26, VCCASW5 AA27, VCCASW6 AA29, VCCASW7 AA31, VCCASW8 AC26, VCCASW9 AC27, VCCASW10 AC29, VCCASW11 AC31, VCCASW12 AD29, VCCASW13 AD31, VCCASW14 W21, VCCASW15 W23, VCCASW16 W24, VCCASW17 W26, VCCASW18 W29, VCCASW19 W31, VCCASW20 W33 — 1D05V_VTT — 1.01A (Total current of VCCASW)
  - C2405 SC10U6D3V3MX-GP, C2403 SC10U6D3V3MX-GP, C2404 SC20U6D3V3MX-GP — (1uFx3)
  - C2406 SC1U6D3V2KX-GP, C2407 SC1U6D3V2KX-GP, C2408 SC1U6D3V2KX-GP
- VCCIO7 AF17, VCCDIFFCLKN1 AE33, VCCDIFFCLKN2 AE34, VCCDIFFCLKN3 AG34 — +VCCDIFFCLK — 0.055A
- VCCSSC AG33 — +V1.05S_SSCVCC — 0.095A — C2415 SCD1U10V2KX-5GP (0.1uFx1)
- DCPSST V16 — +VCCSST (1uFx1)
- DCPSUS1 T17, DCPSUS2 V19 — DCPSUS — TP2406 TPAD14-OP-GP
- V_PROC_IO BJ8 — +V_PROC_IO — 0.001A — (0.1uFx2) (4.7uFx1_0603) — C2417 SC4D7U06D3V3KX-GP — C2418 SCD1U10V2KX-5GP — C2419 SCD1U10V2KX-5GP
- VCCRTC A22 — RTC_AUX_S5 — 6uA — (0.1uFx2) (1uFx1) — C2420 SC1U6D3V2KX-GP — C2421 SCD1U10V2KX-5GP — C2422 SCD1U10V2KX-5GP

RTC

PANTHER-GP-NF

3D3V_S0 — L2401 IND-10UH-218-GP — +V3.3S_VCC_CLKF33 — 68.10050.10Y / 2nd = 68.10090.10B — SIV — C2401 SC10U6D3V5KX-1GP — C2402 SC1U10V2KX-1GP (10uFx1) (1uFx1) — DY

after layout, place 4.7uF *3

1D05V_VTT — L2402 IND-10UH-218-GP — R2413 0R2J-2-GP — +1.05VS_VCCA_A_DPL — 68.10050.10Y / 2nd = 68.10090.10B — (1uFx1) (220uFx1) — 0.08A — DY — C2445 SC10U6D3V5KX-1GP — C2447 ST220U2D5VBM-7GP — C2409 SC1U6D3V2KX-GP

L2403 IND-10UH-218-GP — R2414 0R2J-2-GP — +1.05VS_VCCA_B_DPL — 68.10050.10Y / 2nd = 68.10090.10B — SIV — C2410 SC1U6D3V2KX-GP — C2446 SC10U6D3V5KX-1GP — (1uFx1) (220uFx1) — 0.08A — DY — C2448 ST220U2D5VBM-7GP

1D05V_VTT — R2404 0R2J-2-GP — +VCCDIFFCLK (1uFx1) — C2412 SC1U6D3V2KX-GP

1D05V_VTT — R2405 0R2J-2-GP — +V1.05S_SSCVCC (1uFx1) — C2413 SC1U6D3V2KX-GP

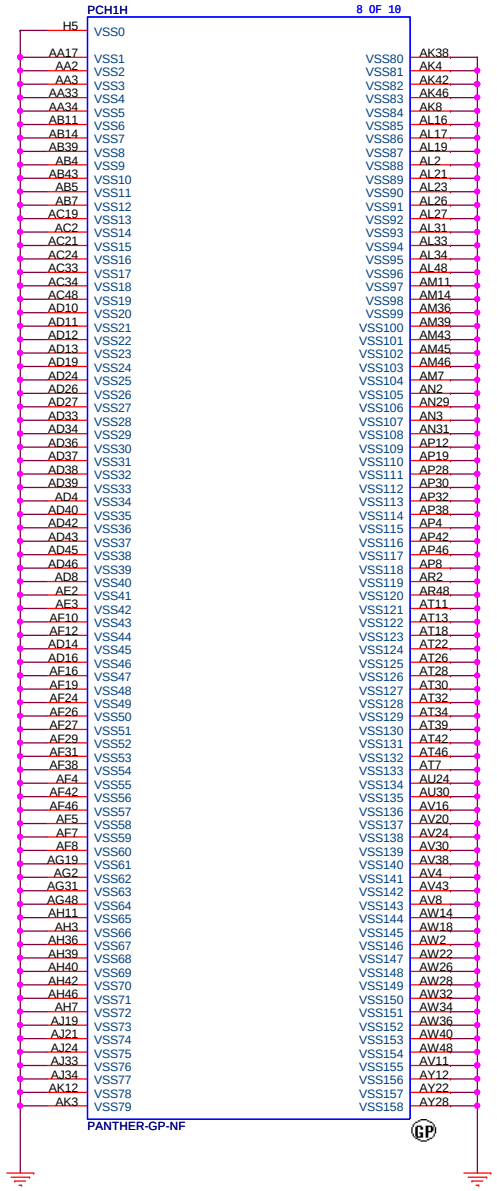
+VCCRTCEXT — C2411 SCD1U10V2KX-5GP (0.1uFx1) — 0.16A (Totally current of VCCVRM) — +VCCAFDI_VRM

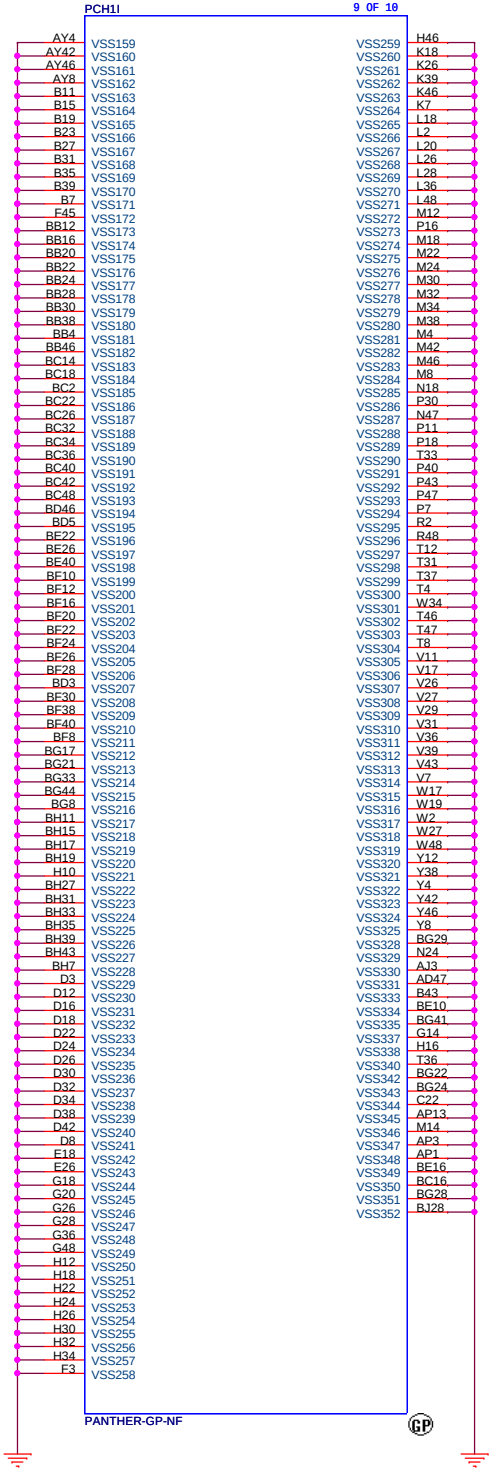
1D05V_VTT — R2406 0R3J-0-U-GP (1uFx1) — C2414 SC1U6D3V2KX-GP

1D0V_S0 — 0R2J-2-GP — R2417

RTC_AUX_S5

SSID = PCH





JV10-CS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size | Document Number: **G48/G58** | Rev: SC

Date: Friday, February 17, 2012 | Sheet 25 of 103

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JV10-CS

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Title	***Reserved***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 26 of 103	

SSID = KBC

If use PSL function, please connect to 3D3V_AUX_S5
If no use PSL function, please connect 3D3V_AUX_KBC

NOTE:
Locate resistors R2719 and R2722 close to the NPCE885P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

71.00885.A0G

EC_GPIO47 High Active

84.2N702.J31
2nd = 84.2N702.W31

83.00016.K11
2ND = 83.00016.F11

84.T3906.A11
2nd = 84.03906.F11

Prevent BIOS data loss solution

74.00690.I7B

EC GPIO standard PH/PL

LILI Multi GPIO setting

84.DMN66.03F
2ND = 84.2N702.A3F

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

64.47025.6DL

65W_90W#
High: 65W / Low 90W

MODEL_ID_AD (Pin100)	Pull-Low Register	Pull-High Register	Voltage	
LG48 UMA	100.0 K	10.0 K	3.000 V	64.10025.6DL
LG48 OPTIMUS	100.0 K	20.0 K	2.750 V	64.20025.6DL
LG58 UMA	100.0 K	33.0 K	2.481 V	64.33025.6DL
LG58 OPTIMUS	100.0 K	47.0 K	2.245 V	64.47025.6DL

64.47025.6DL

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795
Size: Document Number: G48/G58 Rev: SC
Date: Friday, February 17, 2012 Sheet 27 of 103

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA 0905 change to 390p

3

Q6
MMBT3904WT1G-GP

C183
SC390P50V2KX-GP

2200p close to smsc2103 chip

2

DY

Q42
MMBT3904WT1G-GP

C434
SC390P50V2KX-GP
DY

REMOTE2-

C569
SC2200P50V2KX-2GP

REMOTE2+

between CPU, VGA and DIMM on bottom side

T8

1

Q9
MMBT3904WT1G-GP

2200p close to smsc2103 chip

H_THERMDA

C389
SC2200P50V2KX-2GP

H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

3D3V_S0

R2803
6K8R2J-GP

THERM_SYS_SHDN#

3D3V_S0

R2802
15KR2J-1-GP

THERM_SCI#

T8= 86 degree

3D3V_S0

R260
68R2-GP

C388 SCD1U10V2KX-4GP

2103_VDD

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-

U2801

VDD
DP1
DN1
DP2/DN3
DN2/DP3

SMCLK
SMDATA
ALERT#
SYS_SHDN#
GND

THERM_SCI#
THERM_SYS_SHDN#

SMBC_THERM 27,86
SMBD_THERM 27,86

R272 0R2J-2-GP

THERM_SCI#

EMC1423-1-AIZL-TR-GP

4 WIRE PWM Fan Control circuit

5V_S0

Close to connector

D2801
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
DY

C39
SC47U6D3VKX-GP

R426
10KR2J-3-GP

R2801
0R3J-0-U-GP

R427
0R0402-PAD
SIT

FAN1

27 FAN_PWM
FAN_PWM
FAN_PWM_C

27 FAN_TACH
FAN_TACH

5V_S0_FAN

EC2801
SC470P50V2JN-GP

EC2802
SC470P50V2JN-GP

SIT

ACES-CON4-GP-U1

20.F0714.004
2nd = 20.D0196.104

TP2803
TP2802
TP2801
AFTP2804

FAN_PWM_C
FAN_TACH
5V_S0_FAN

3D3V_AUX_S5

D2803
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
DY

27,36,86 PURE_HW_SHUTDOWN#

R2812
10KR2J-3-GP
DY

C2811
SCD1U10V2KX-5GP
DY

Q2802
2N7002K-2-GP

84.2N702.J31
2ND = 84.2N702.W31

THERM_SYS_SHDN#

IMVP_PWRGD_T

3D3V_S0

R2809
100KR2J-1-GP
DY

SIV

3D3V_S0

R2810
0R2J-2-GP

DY

R2811
0R2J-2-GP

JVID-CS

3D3V_S0

R2814
10KR2J-3-GP
SIT

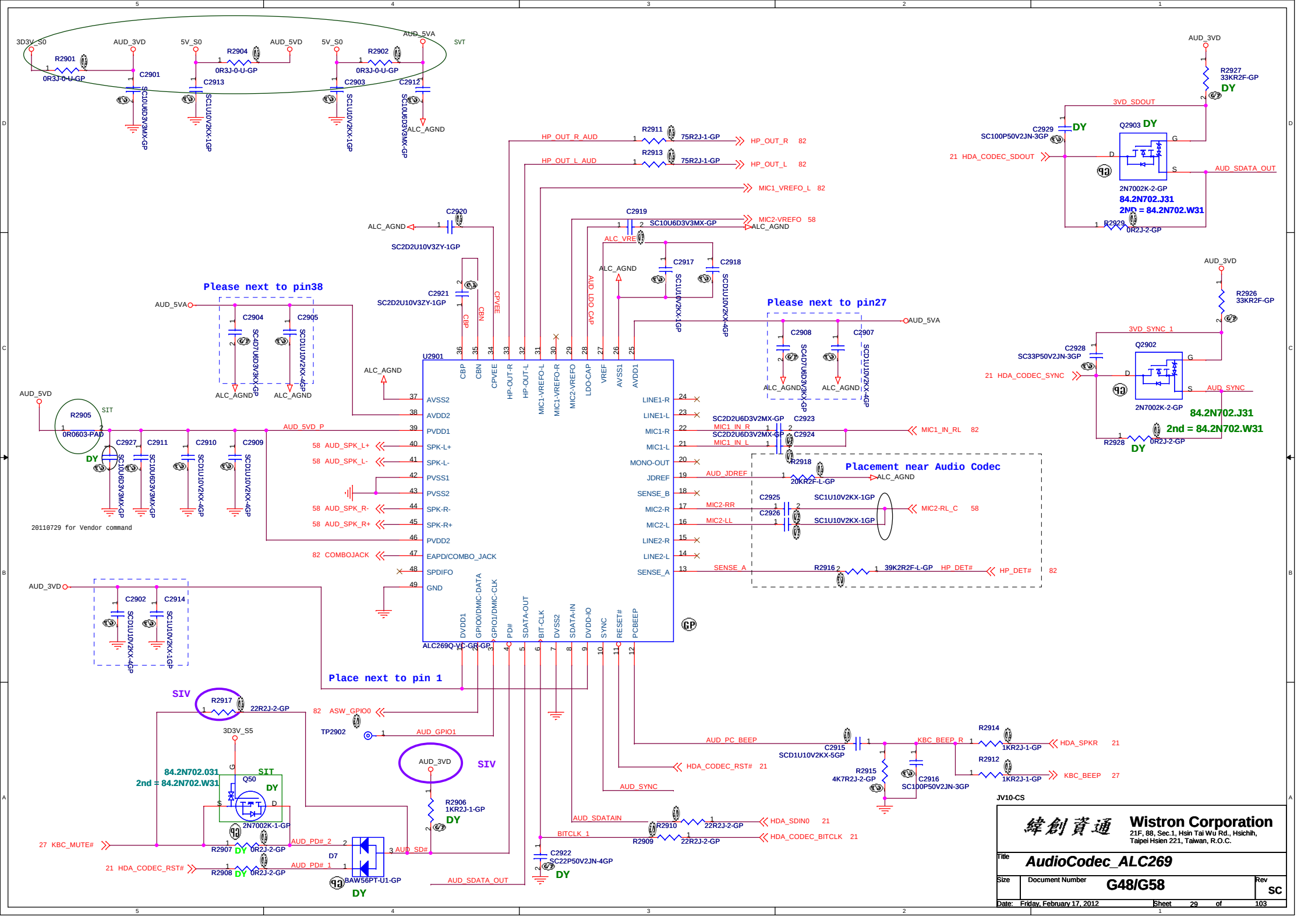
IMVP_PWRGD 36,42

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL EMC1423

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 28 of 103

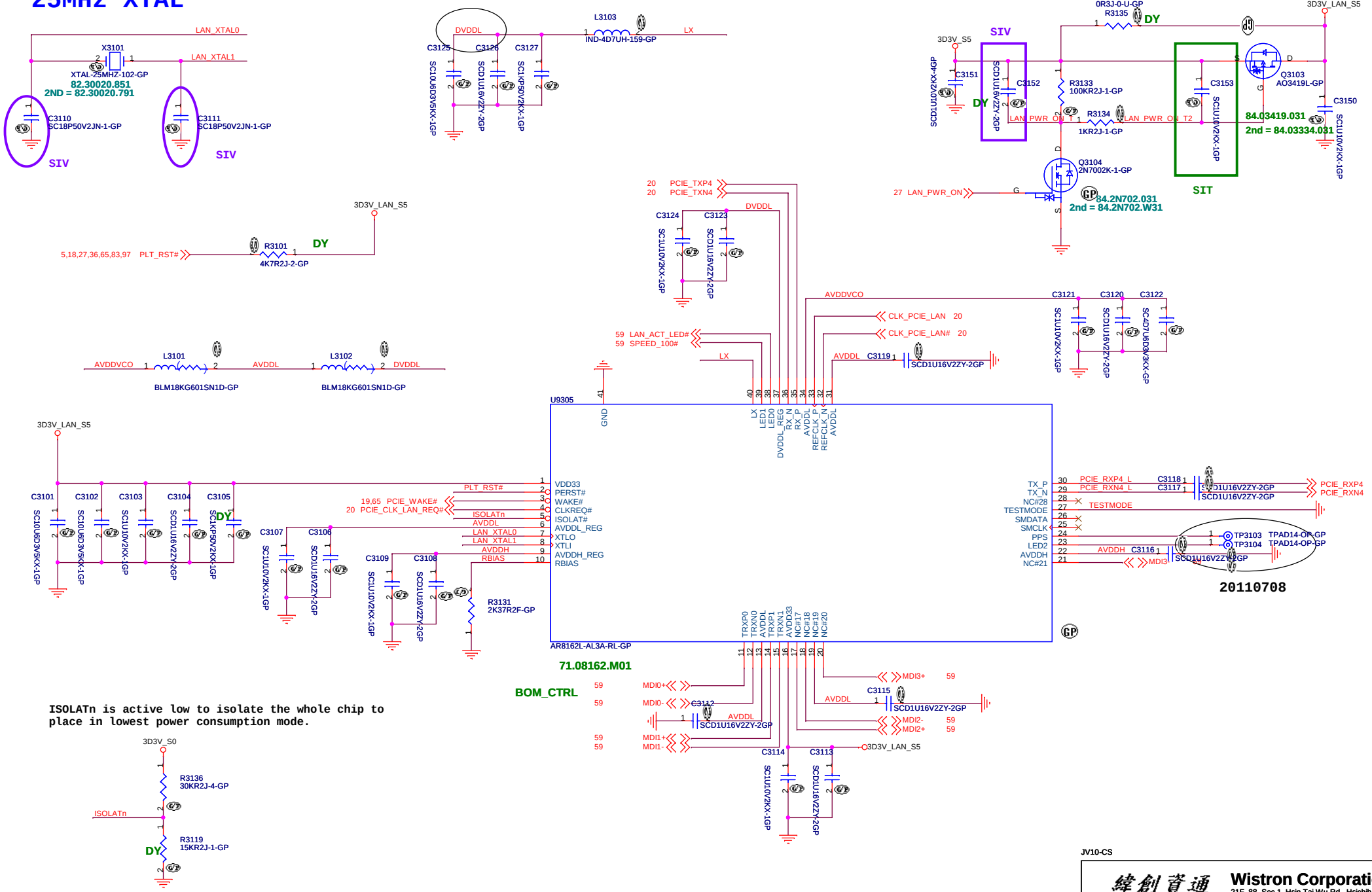

3D3V_S0
AUD_3VD
5V_S0
AUD_5VD
AUD_5VA
SVT
R2901
0R3J-0-U-GP
C2901
C2913
C2903
C2912
SC1U10V2KX-1GP
SC10U6D3V3MX-GP
ALC_AGND
R2904
R2902
HP_OUT_R_AUD
HP_OUT_L_AUD
R2911
R2913
75R2J-1-GP
HP_OUT_R 82
HP_OUT_L 82
MIC1_VREFO_L 82
MIC2-VREFO 58
C2920
C2919
C2921
SC2D2U10V3ZY-1GP
ALC_VRE
C2917
C2918
SC1U10V2KX-1GP
SC1D1U10V2KX-4GP
Please next to pin38
Please next to pin27
C2904
C2905
SC4D7U6D3V3KX-GP
SC1D1U10V2KX-4GP
C2908
C2907
U2901
CBP
CBN
CPVEE
HP-OUT-R
HP-OUT-L
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDD1
AVSS2
AVDD2
PVDD1
SPK-L+
SPK-L-
PVSS1
PVSS2
SPK-R-
SPK-R+
PVDD2
EAPD/COMBO_JACK
SPDIFO
GND
LINE1-R
LINE1-L
MIC1-R
MIC1-L
MONO-OUT
JDREF
SENSE_B
MIC2-R
MIC2-L
LINE2-R
LINE2-L
SENSE_A
DVDD1
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BIT-CLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
ALC269Q-VC-GR-GP
58 AUD_SPK_L+
58 AUD_SPK_L-
58 AUD_SPK_R-
58 AUD_SPK_R+
82 COMBOJACK
AUD_5VD_P
R2905
0R0603-PAD
SIT
DY
C2927
C2911
C2910
C2909
SC10U6D3V3MX-GP
SC1D1U10V2KX-4GP
20110729 for Vendor command
MIC1_IN_R
MIC1_IN_L
SC2D2U6D3V2MX-GP
C2923
C2924
MIC1_IN_RL 82
R2918
20KR2F-L-GP
AUD_JDREF
ALC_AGND
Placement near Audio Codec
C2925
C2926
SC1U10V2KX-1GP
MIC2-RR
MIC2-LL
MIC2-RL_C 58
R2916
39K2R2F-L-GP
HP_DET#
HP_DET# 82
SENSE_A
C2902
C2914
SC1D1U10V2KX-4GP
SC1U10V2KX-1GP
Place next to pin 1
SIV
R2917
22R2J-2-GP
82 ASW_GPIO0
TP2902
AUD_GPIO1
3D3V_S5
84.2N702.031
2nd = 84.2N702.W31
Q50
2N7002K-1-GP
R2906
1KR2J-1-GP
27 KBC_MUTE#
R2907
0R2J-2-GP
AUD_PD# 2
21 HDA_CODEC_RST#
R2908
AUD_PD# 1
D7
BAW56PT-U1-GP
AUD_SD#
AUD_SDATA_OUT
C2922
SC22P50V2JN-4GP
AUD_PC_BEEP
C2915
SCD1U10V2KX-5GP
KBC_BEEP_R
R2914
1KR2J-1-GP
HDA_SPKR 21
R2912
KBC_BEEP 27
R2915
4K7R2J-2GP
C2916
SC100P50V2JN-3GP
HDA_CODEC_RST# 21
AUD_SYNC
AUD_SDATAIN
R2910
R2909
22R2J-2-GP
HDA_SDIN0 21
BITCLK_1
HDA_CODEC_BITCLK 21
R2927
33KR2F-GP
3VD_SDOUT
C2929
SC100P50V2JN-3GP
Q2903
21 HDA_CODEC_SDOUT
AUD_SDATA_OUT
2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.W31
R2929
0R2J-2-GP
R2926
33KR2F-GP
3VD_SYNC_1
C2928
SC33P50V2JN-3GP
Q2902
21 HDA_CODEC_SYNC
AUD_SYNC
2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.W31
R2928
0R2J-2-GP
JV10-CS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AudioCodec_ALC269
Size
Document Number
G48/G58
Rev
SC
Date: Friday, February 17, 2012
Sheet 29 of 103

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Audio_AMP***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 30 of 103	

25MHz XTAL



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LOM***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 31 of 103	

(Blanking)

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Card reader***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 32 of 103	

(Blanking)

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***1394***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 33 of 103	

(Blanking)

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

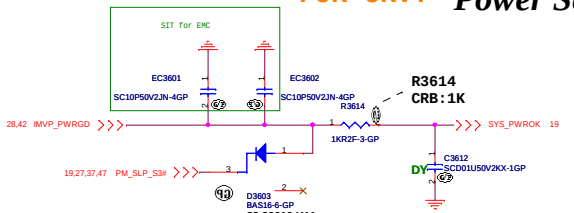
Title	***Smart card***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 34 of 103	

Reserved

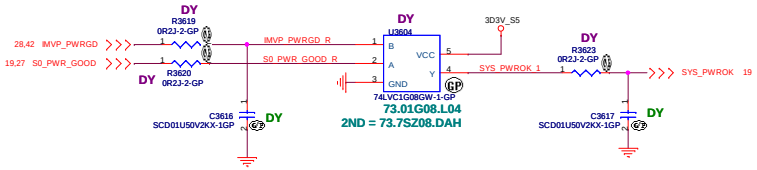
JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB 3.0 CONTROLLER***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 35 of 103	

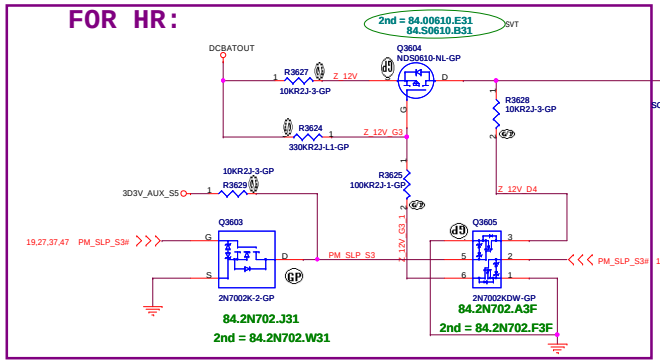
FOR CRV: Power Sequence

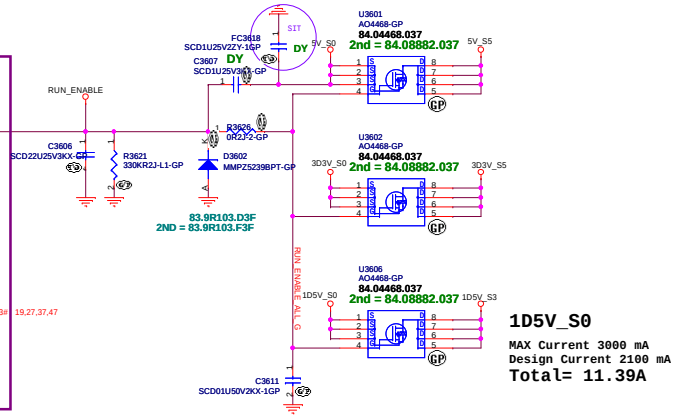


FOR HR:



FOR HR:

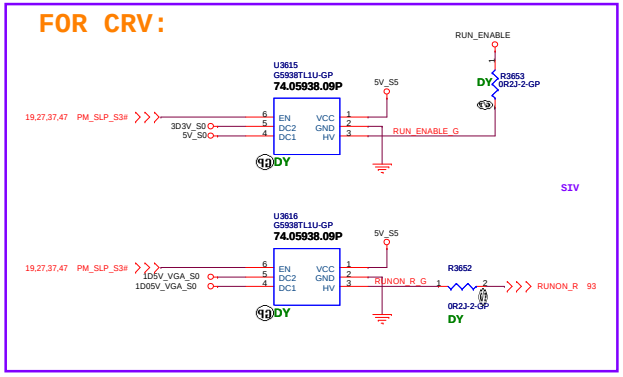


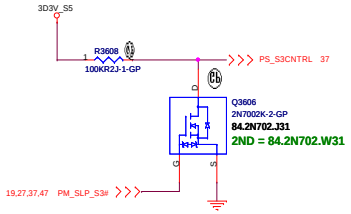


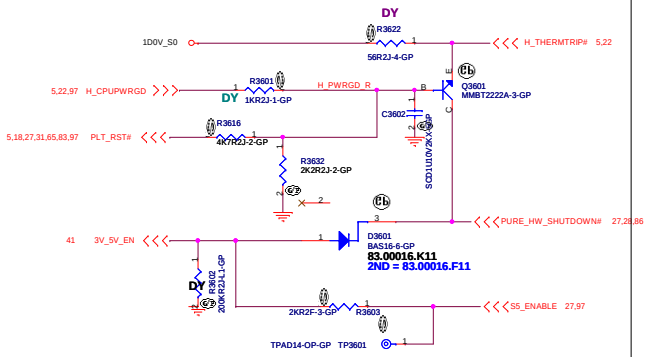
1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

FOR CRV:

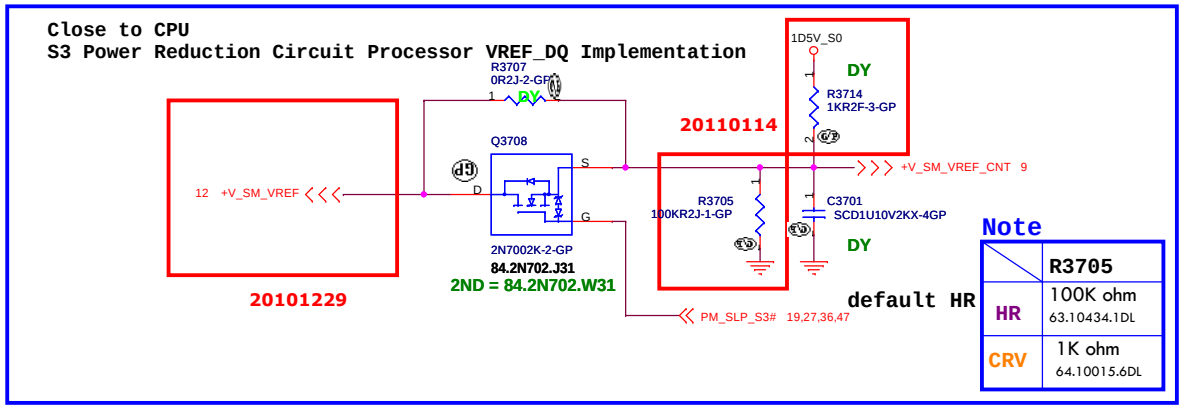


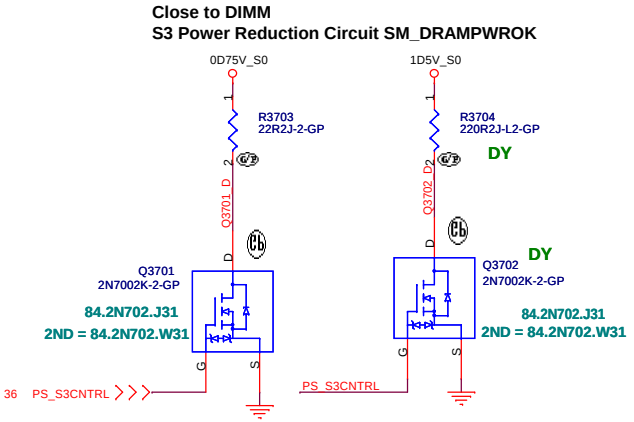


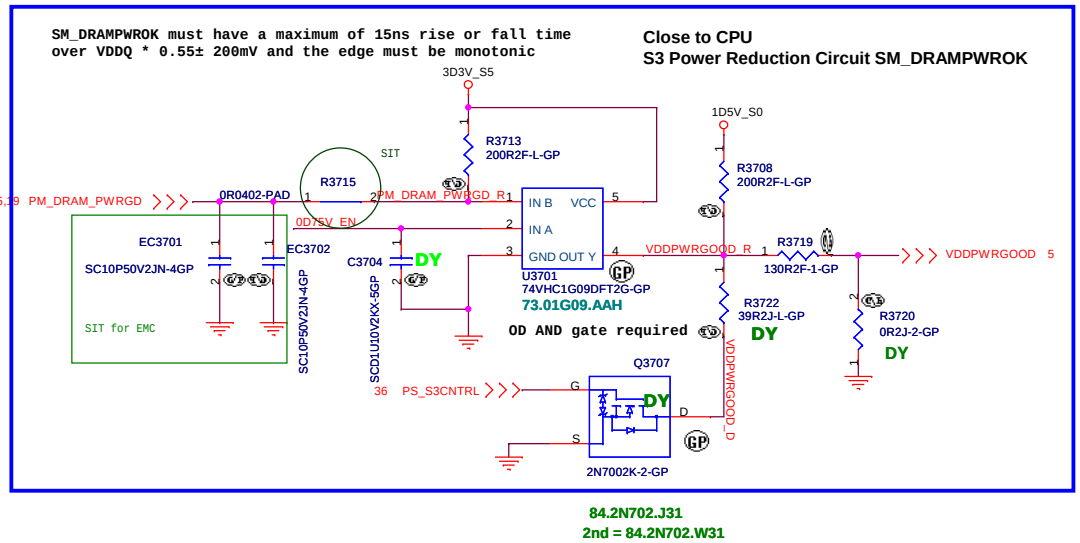


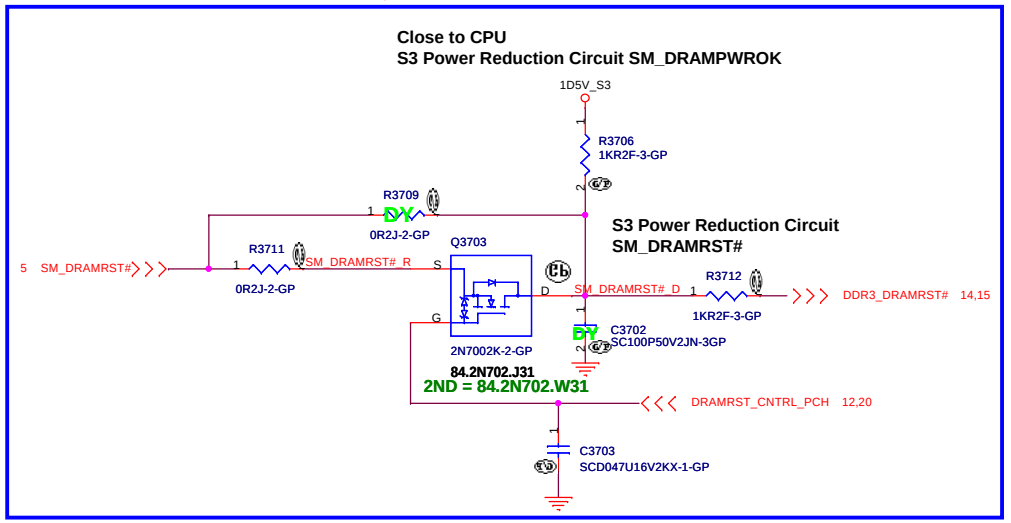
JV10-CS

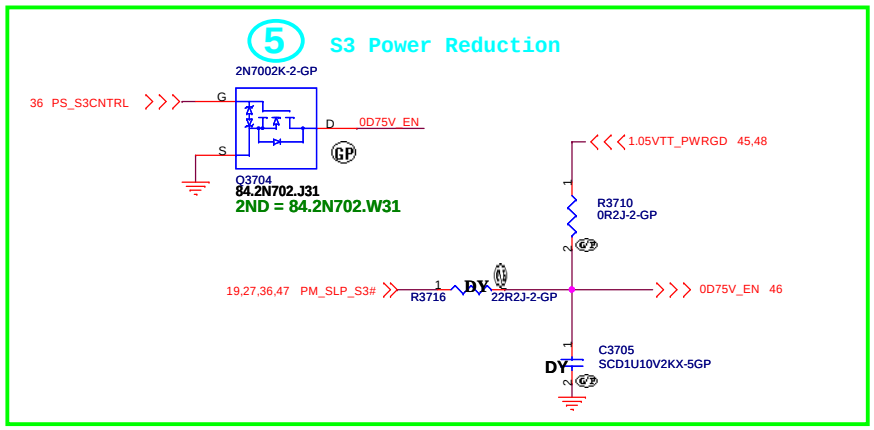
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	PowerPlane Enable&Sequence	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 36 of 103	







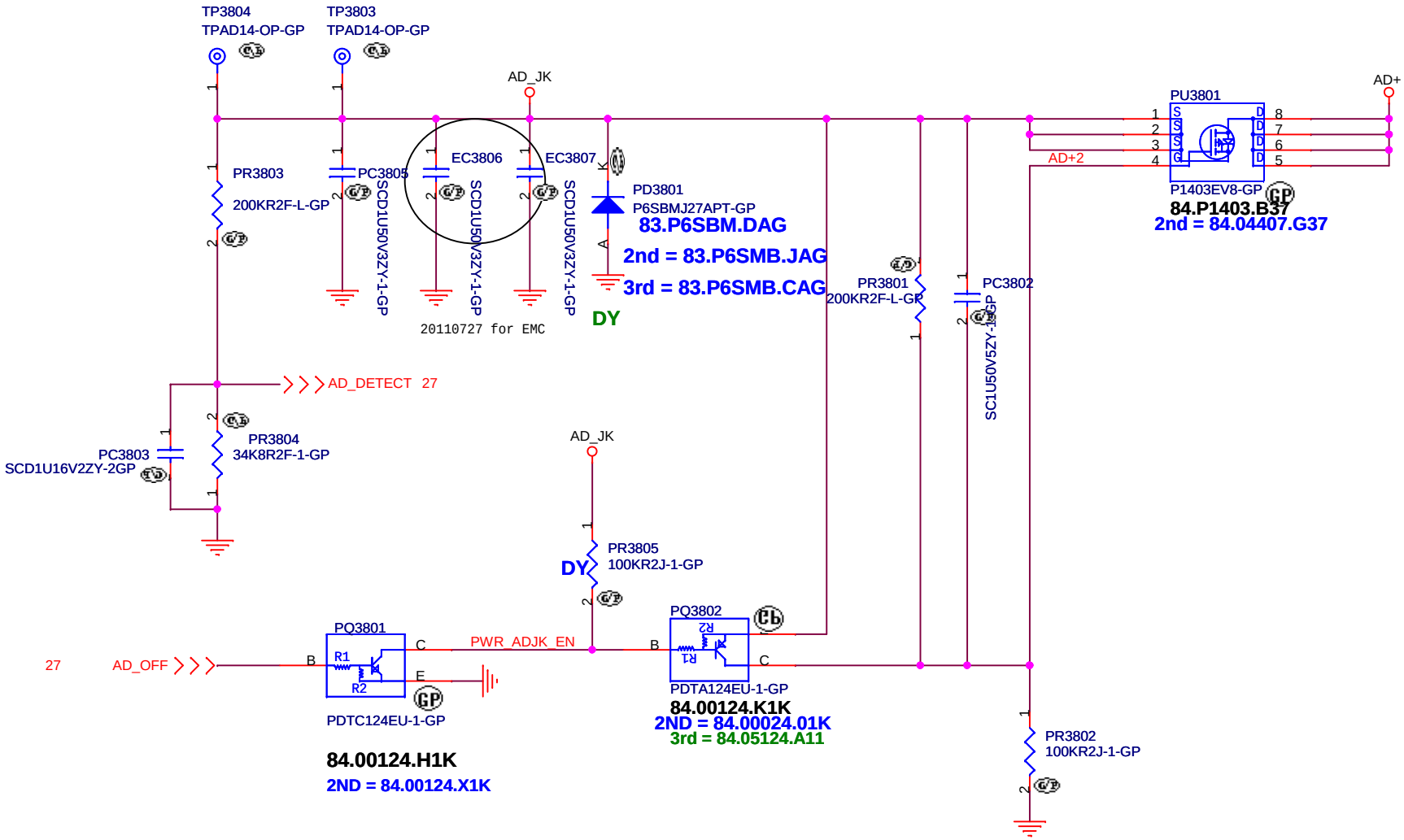




JV10-CS

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ADAPTER OCP / S3 reduction
Size / Document Number	G48/G58
Rev	SC
Date: Friday, February 17, 2012	Sheet 37 of 103

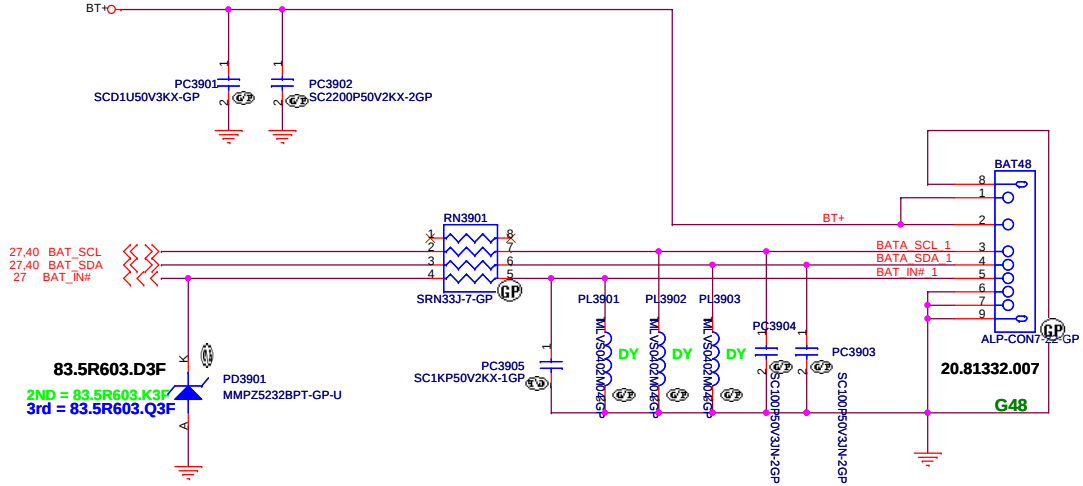
Adaptor in to generate DCBATOUT

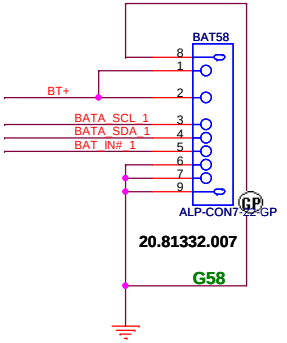


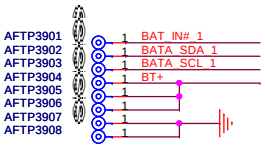
JV10-CS

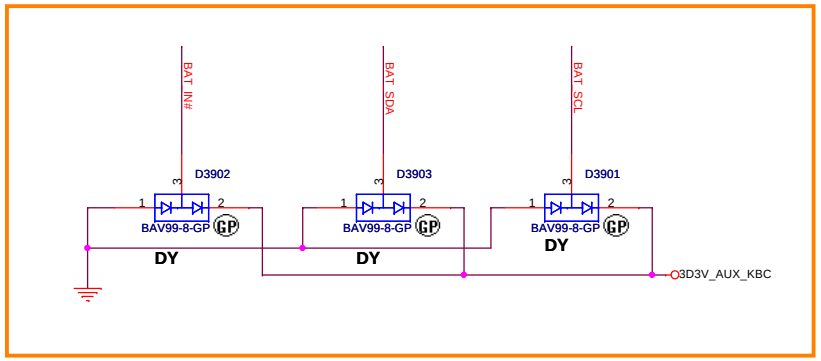
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN JACK***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 38 of 103	

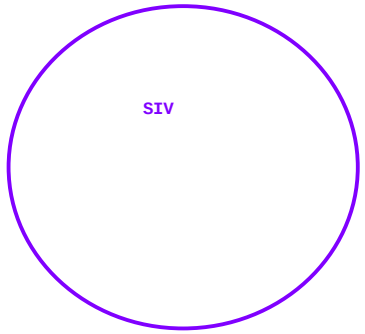
BATTERY CONNECTOR











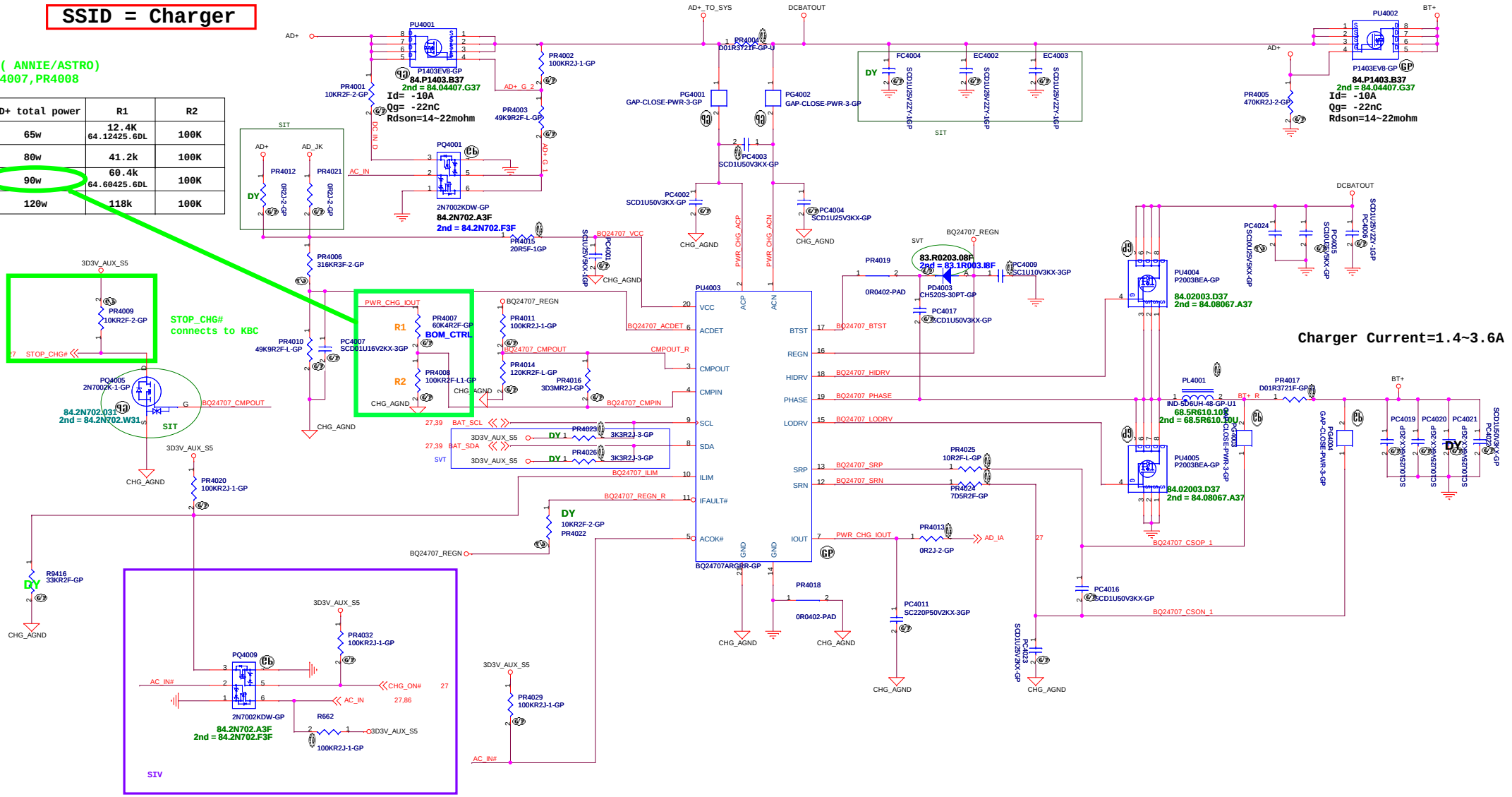
JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT CONN		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 39 of 103	

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118k	100K

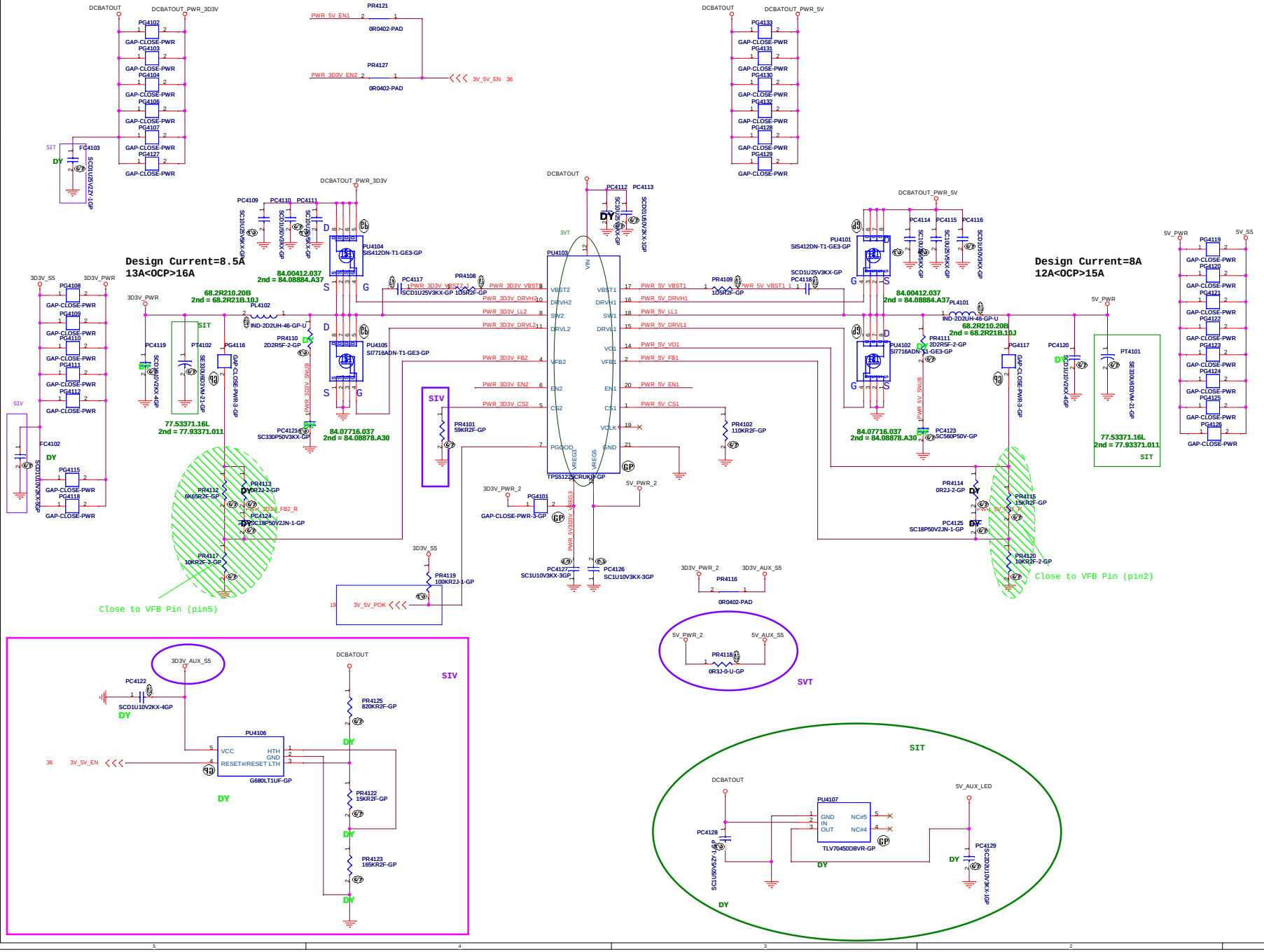


JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BQ24745_Charger	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 40 of 103	

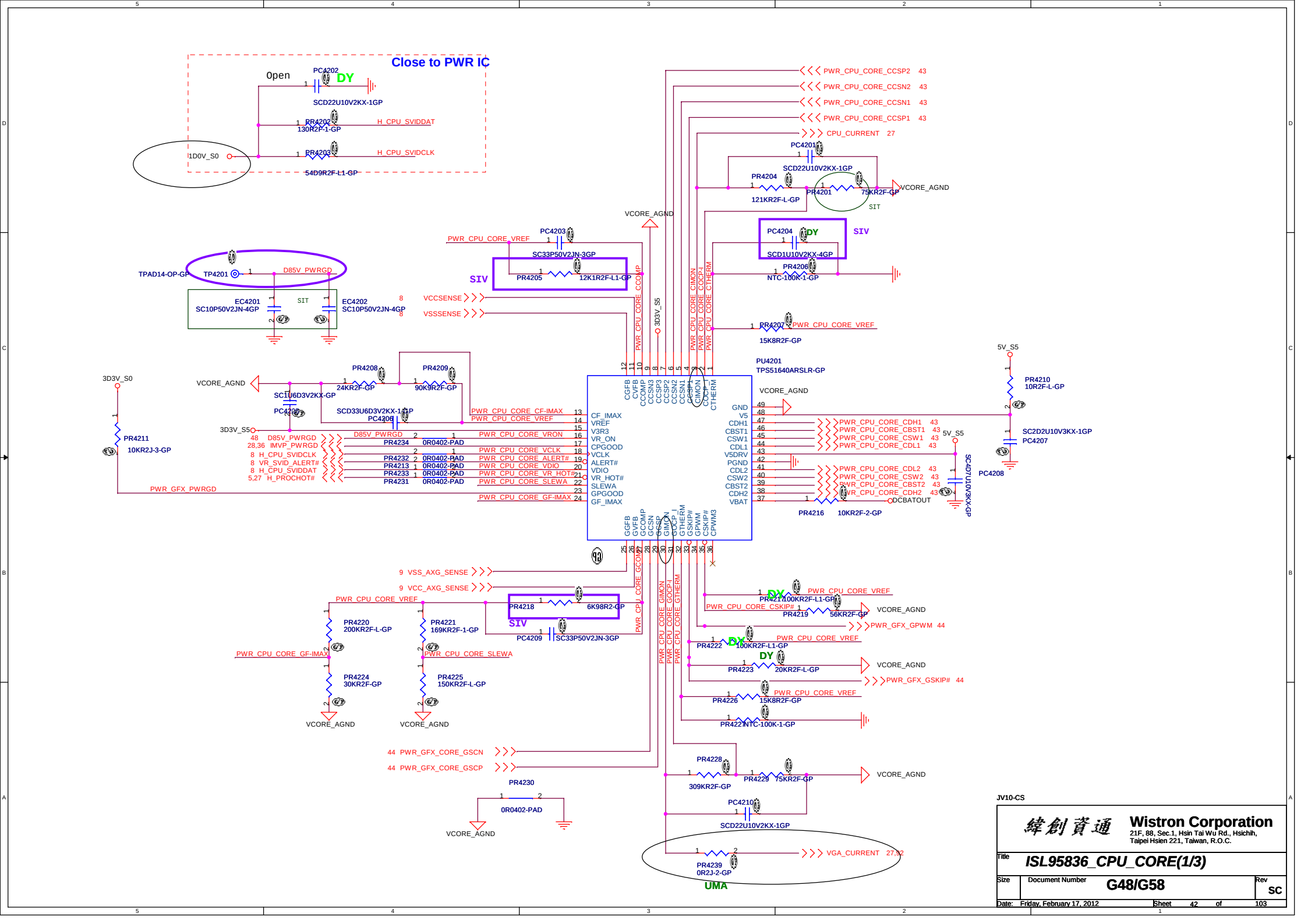
SSID = PWR.Plane.Regulator_5v3p3v

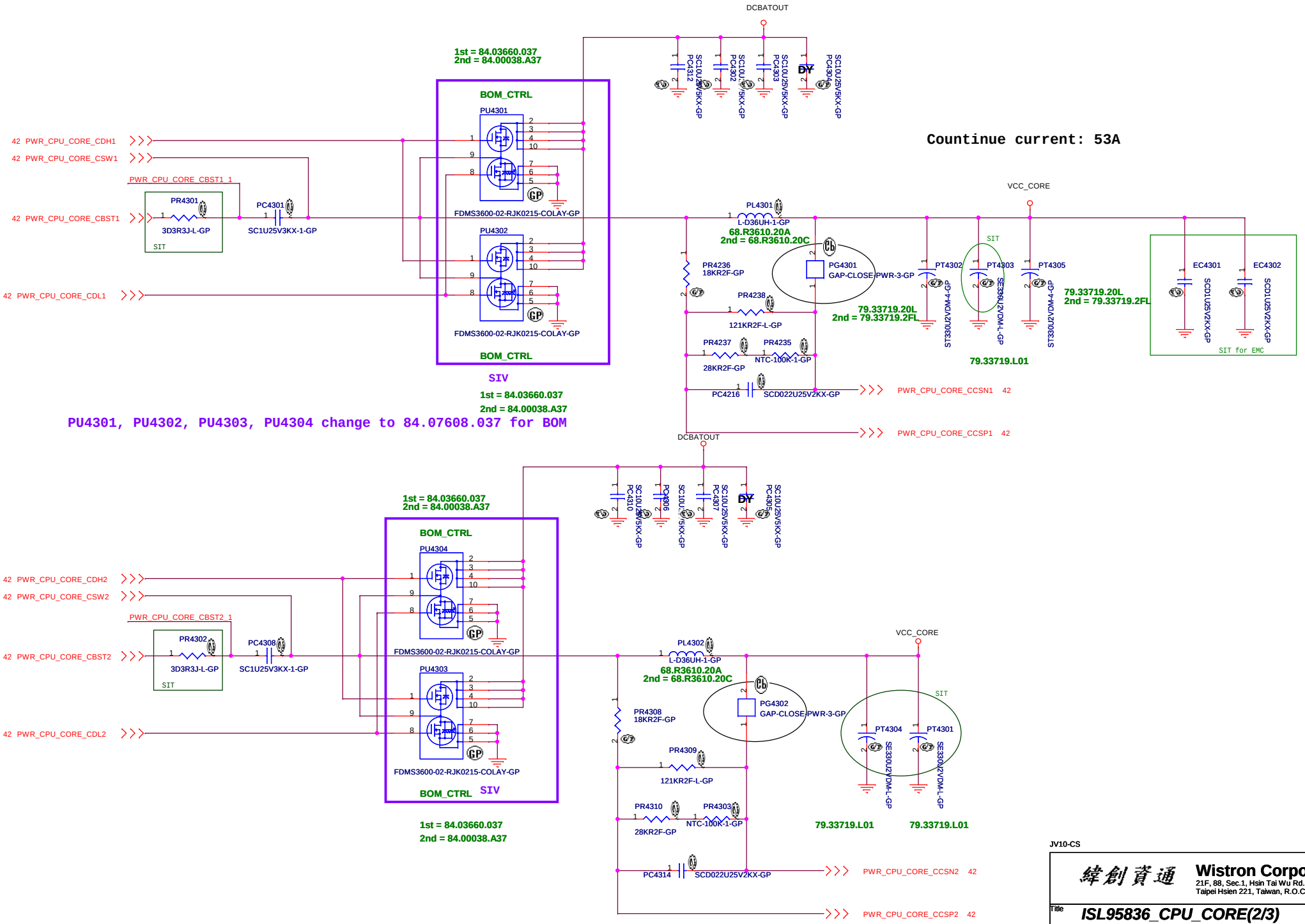


JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

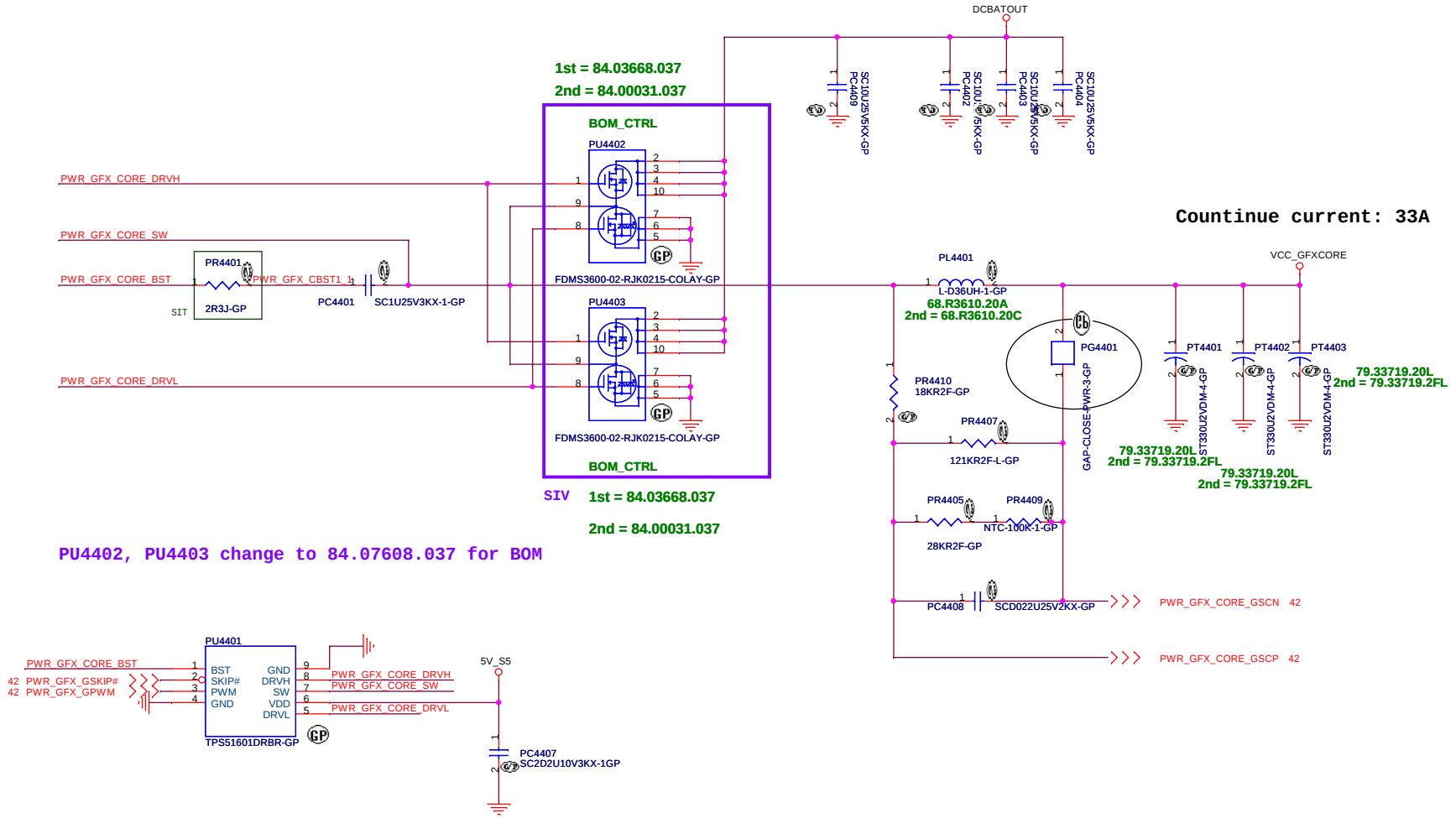
Title	*TPS51123_5V_3D3V*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 41 of 103	


Close to PWR IC
0pen
PC4202
DY
SCD22U10V2KX-1GP
PR4202
130R2F-1-GP
H_CPU_SVIDDAT
1D0V_S0
PR4203
54D9R2F-L1-GP
H_CPU_SVIDCLK
PWR_CPU_CORE_CCSP2 43
PWR_CPU_CORE_CCSN2 43
PWR_CPU_CORE_CCSN1 43
PWR_CPU_CORE_CCSP1 43
CPU_CURRENT 27
PC4201
SCD22U10V2KX-1GP
PR4204
121KR2F-L-GP
PR4201
75KR2F-GP
SIT
VCORE_AGND
VCORE_AGND
PC4204
DY
SIV
SCD1U10V2KX-4GP
PR4206
NTC-100K-1-GP
TPAD14-OP-GP
TP4201
D85V_PWRGD
EC4201
SC10P50V2JN-4GP
SIT
EC4202
SC10P50V2JN-4GP
PWR_CPU_CORE_VREF
PC4203
SC33P50V2JN-3GP
SIV
PR4205
12K1R2F-L1-GP
VCCSENSE 8
VSSSENSE 8
PR4207
15K8R2F-GP
PWR_CPU_CORE_VREF
3D3V_S5
PWR_CPU_CORE_CCOMP
PWR_CPU_CORE_CIMON
PWR_CPU_CORE_COCP1
PWR_CPU_CORE_CTHERM
PU4201
TPS51640ARSLR-GP
3D3V_S0
PR4211
10KR2J-3-GP
VCORE_AGND
PR4208
24KR2F-GP
PR4209
90K9R2F-GP
SC1U6D3V2KX-GP
PC4205
SCD33U6D3V2KX-1GP
PC4206
3D3V_S5
PWR_GFX_PWRGD
PWR_CPU_CORE_CF-IMAX
PWR_CPU_CORE_VREF
PWR_CPU_CORE_VRON
PWR_CPU_CORE_VCLK
PWR_CPU_CORE_ALERT#
PWR_CPU_CORE_VDIO
PWR_CPU_CORE_VR_HOT#
PWR_CPU_CORE_SLEWA
PWR_CPU_CORE_GF-IMAX
D85V_PWRGD
IMVP_PWRGD
H_CPU_SVIDCLK
VR_SVID_ALERT#
H_CPU_SVIDDAT
H_PROCHOT#
PR4234 0R0402-PAD
PR4232 0R0402-PAD
PR4213 0R0402-PAD
PR4233 0R0402-PAD
PR4231 0R0402-PAD
CF_IMAX
VREF
V3R3
VR_ON
CPGOOD
VCLK
ALERT#
VDIO
VR_HOT#
SLEWA
GPGOOD
GF_IMAX
GND
V5
CDH1
CBST1
CSW1
CDL1
V5DRV
PGND
CDL2
CSW2
CBST2
CDH2
VBAT
PWR_CPU_CORE_CDH1 43
PWR_CPU_CORE_CBST1 43
PWR_CPU_CORE_CSW1 43
PWR_CPU_CORE_CDL1 43
PWR_CPU_CORE_CDL2 43
PWR_CPU_CORE_CSW2 43
PWR_CPU_CORE_CBST2 43
PWR_CPU_CORE_CDH2 43
DCBATOUT
PR4216
10KR2F-2-GP
5V_S5
PR4210
10R2F-L-GP
SC2D2U10V3KX-1GP
PC4207
PC4208
SC4D7U10V3KX-GP
9 VSS_AXG_SENSE
9 VCC_AXG_SENSE
PWR_CPU_CORE_VREF
PR4218
6K98R2-GP
SIV
PC4209
SC33P50V2JN-3GP
PR4220
200KR2F-L-GP
PR4221
169KR2F-1-GP
PWR_CPU_CORE_GF-IMAX
PWR_CPU_CORE_SLEWA
PR4224
30KR2F-GP
PR4225
150KR2F-L-GP
VCORE_AGND
VCORE_AGND
PWR_CPU_CORE_GSCN
PWR_CPU_CORE_GSCP
PWR_CPU_CORE_GIMON
PWR_CPU_CORE_GOCP1
PWR_CPU_CORE_GTHERM
PR4221 100KR2F-L-GP
DY
PWR_CPU_CORE_CSKIP#
PR4219
56KR2F-GP
VCORE_AGND
PWR_GFX_GPWM 44
PR4222
100KR2F-L1-GP
DY
PWR_CPU_CORE_VREF
PR4223
20KR2F-L-GP
DY
VCORE_AGND
PWR_GFX_GSKIP# 44
PR4226
15K8R2F-GP
PWR_CPU_CORE_VREF
PR4227
NTC-100K-1-GP
44 PWR_GFX_CORE_GSCN
44 PWR_GFX_CORE_GSCP
PR4230
0R0402-PAD
VCORE_AGND
PR4228
309KR2F-GP
PR4229
75KR2F-GP
VCORE_AGND
PC4210
SCD22U10V2KX-1GP
PR4239
0R2J-2-GP
VGA_CURRENT 27,32
UMA
JV10-CS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL95836_CPU_CORE(1/3)
Size
Document Number
G48/G58
Rev
SC
Date: Friday, February 17, 2012
Sheet 42 of 103



JV10-CS

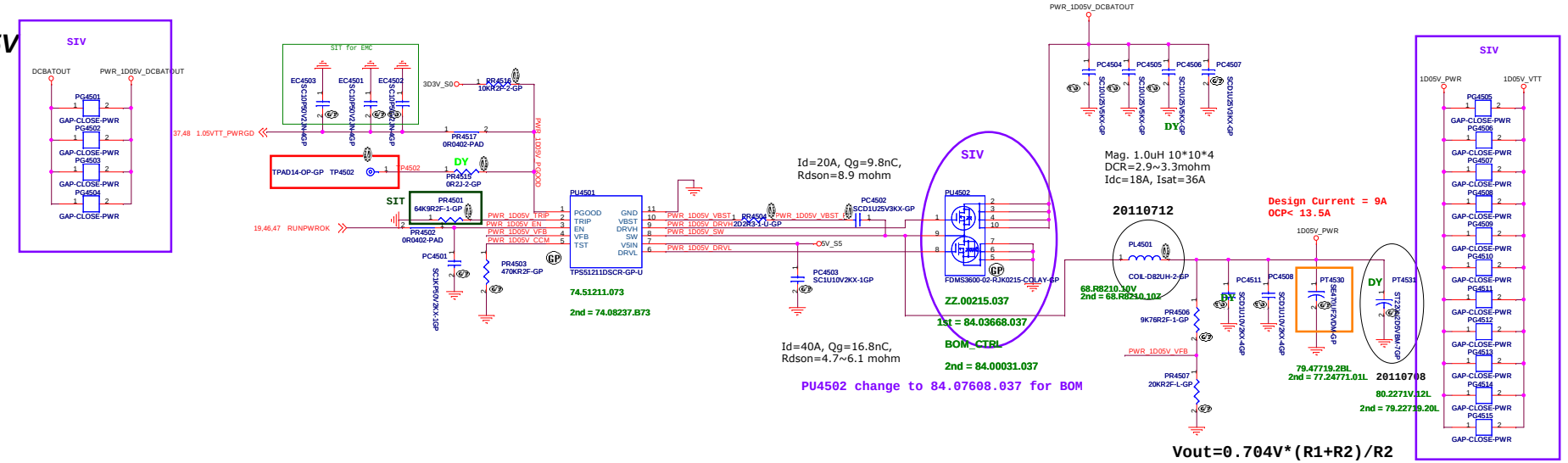
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL95836_CPU_CORE(2/3)	
Size	Document Number: G48/G58	Rev: SC
Date: Monday, February 20, 2012	Sheet 43 of 103	



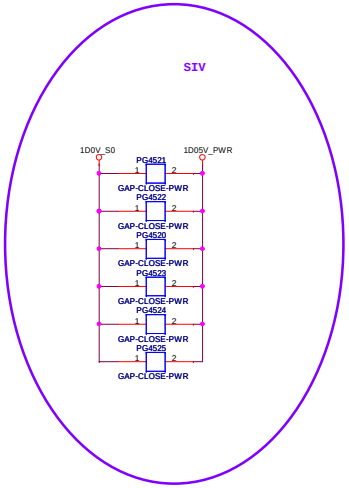
JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ISL95836_CPU_CORE(3/3)		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 44 of 103	

TPS51211 for 1D05V



APL5916 for 1D0V

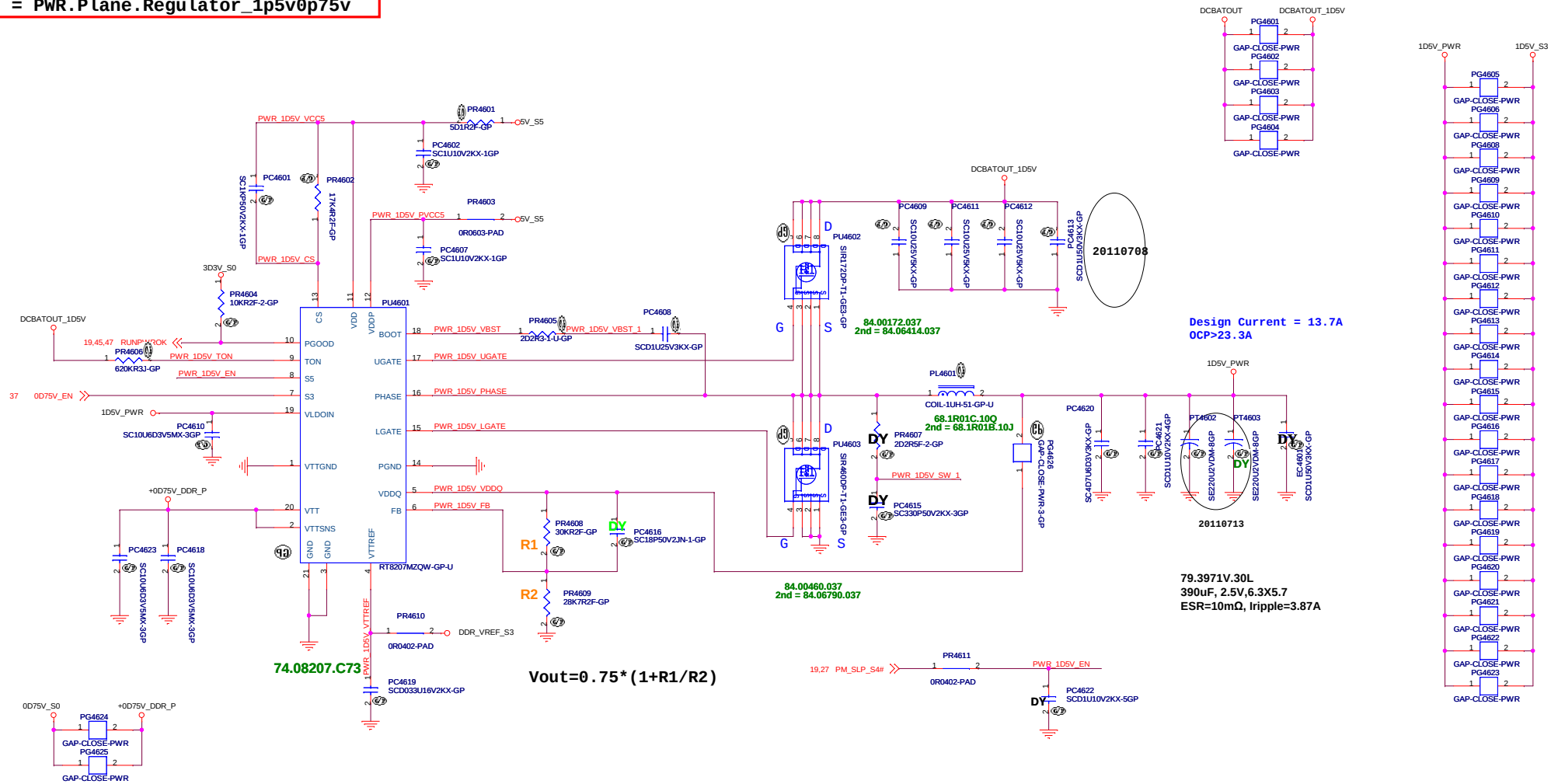


JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51211_1D05V&TPS51219_1D0V	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 45 of 103	

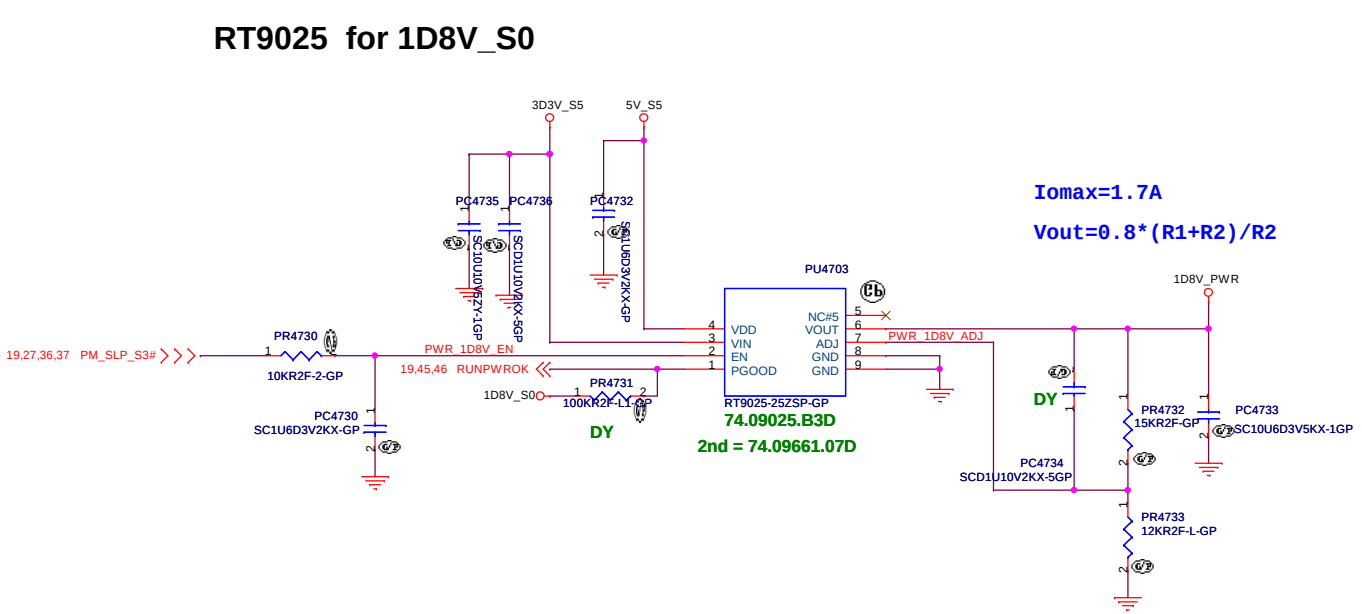
SSID = PWR.Plane.Regulator_1p5v0p75v

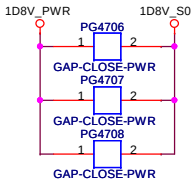


JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8207_1D5V_0D75V		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 46 of 103	

RT9025 for 1D8V_S0



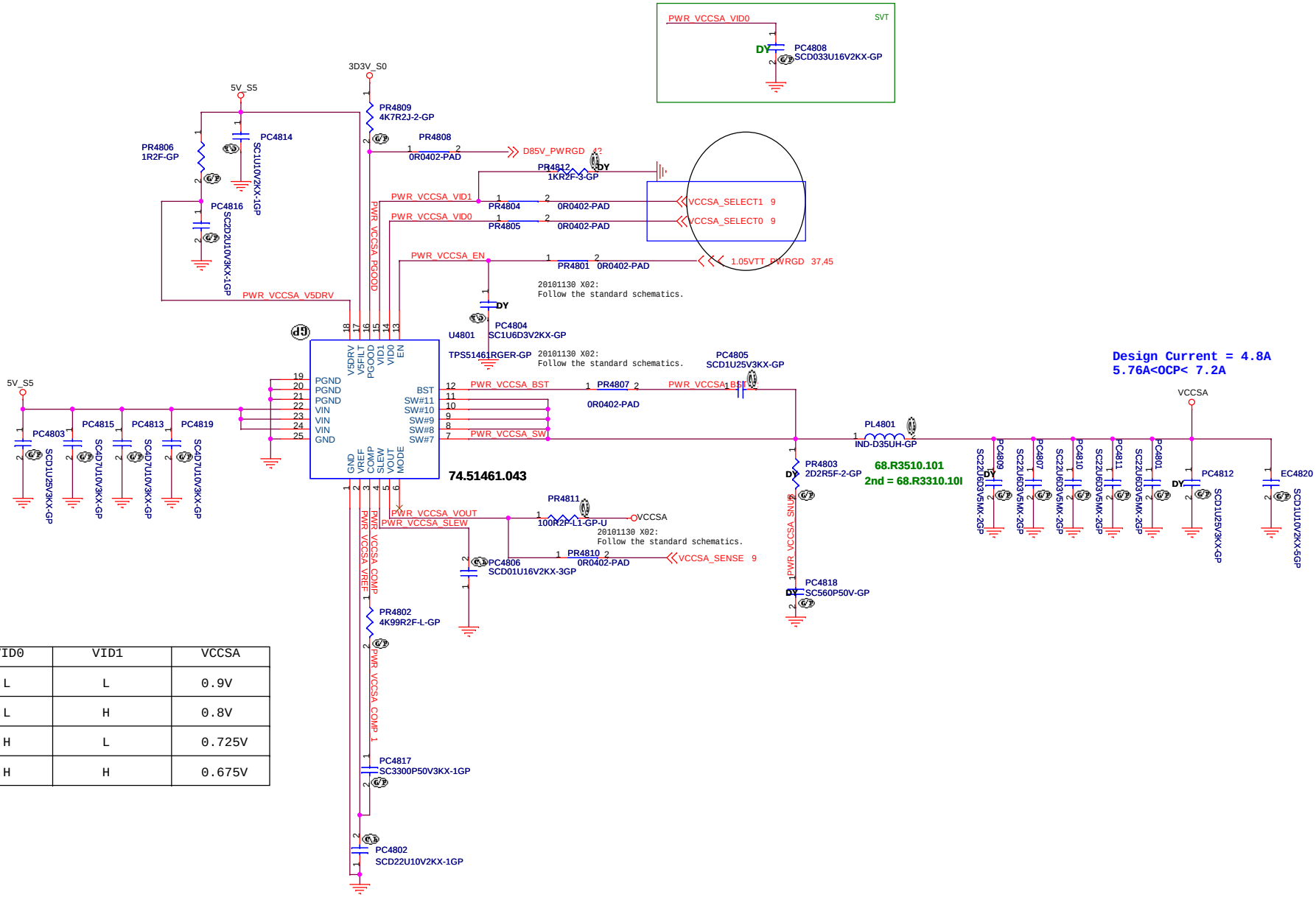


JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT9205_1D8V***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

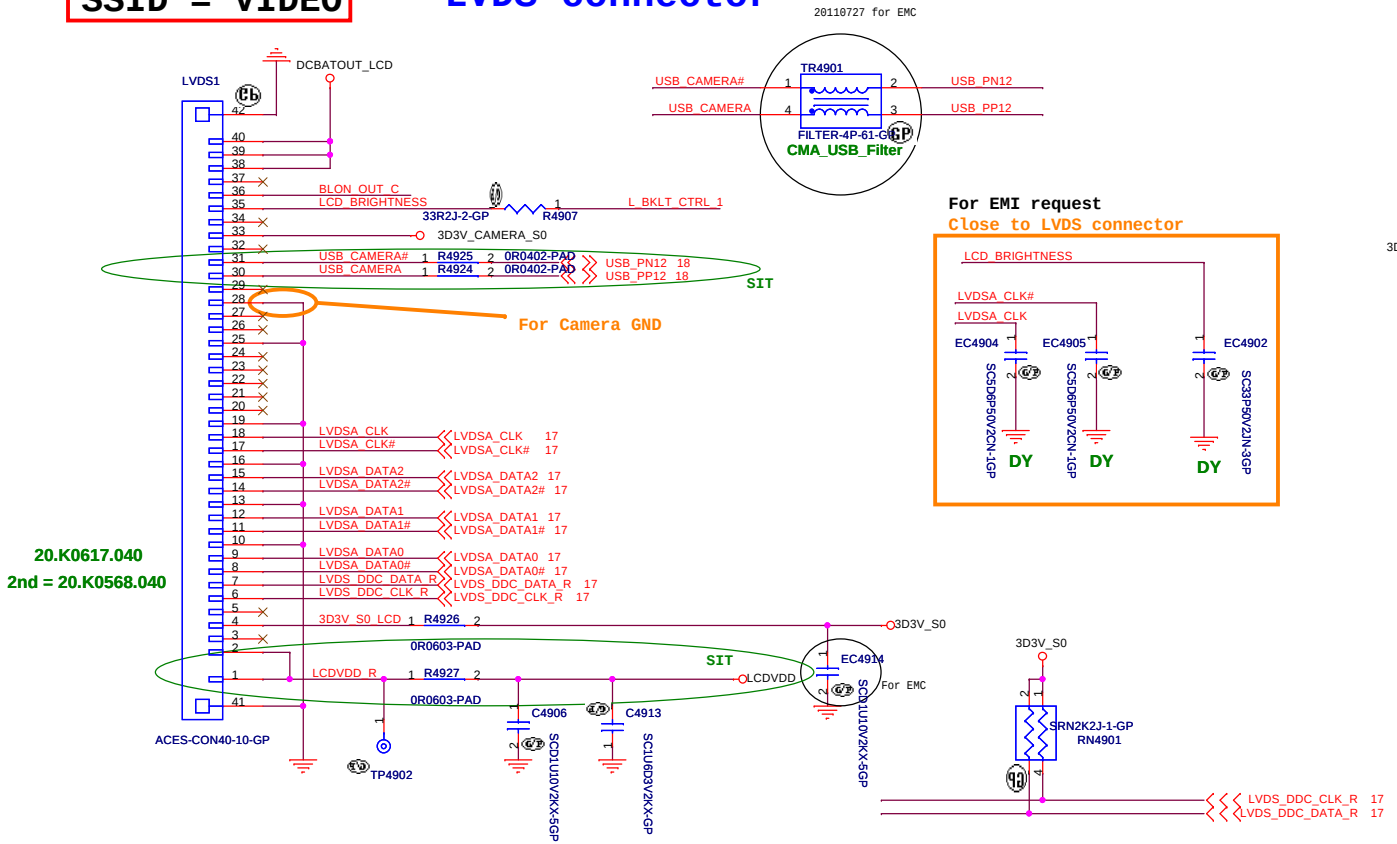
JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA_TPS51461	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 48 of 103	

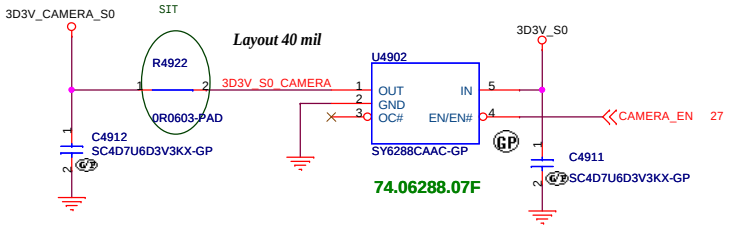
SSID = VIDEO

LVDS connector



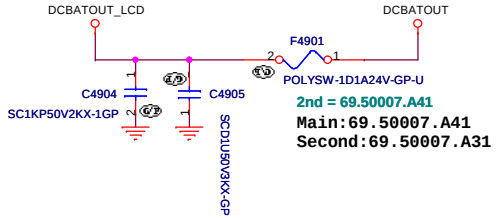
For EMI request
Close to LVDS connector

CAMERA POWER

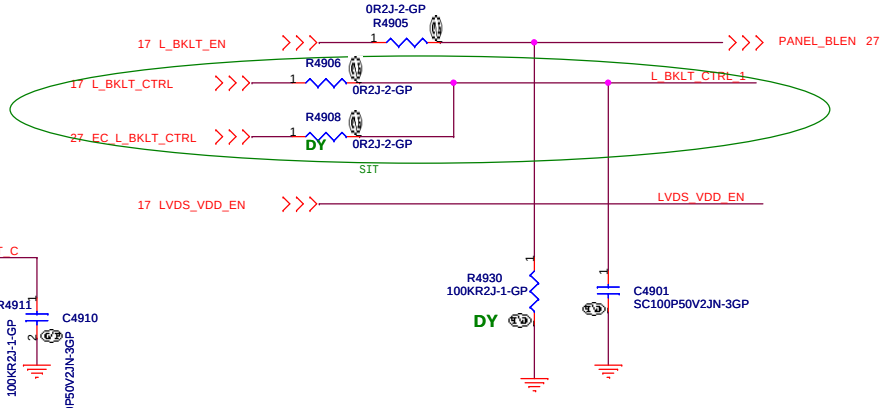


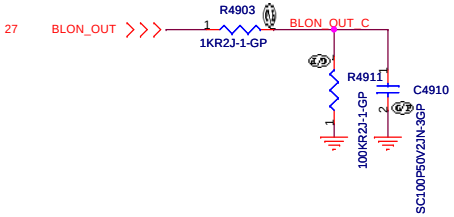
U4902 Change to 74.07534 from 74.05240.A7F for obsoleted part

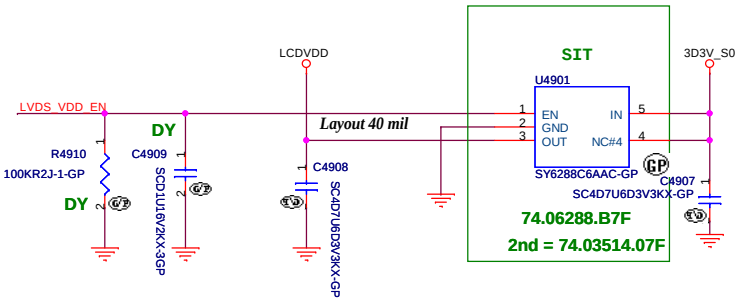
LCD POWER



Panel BL brightness/Power En/BL En



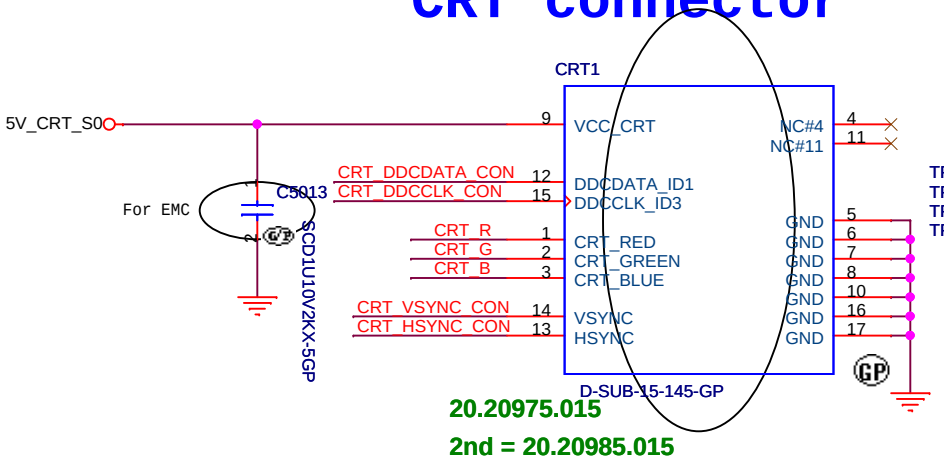




JV10-CS

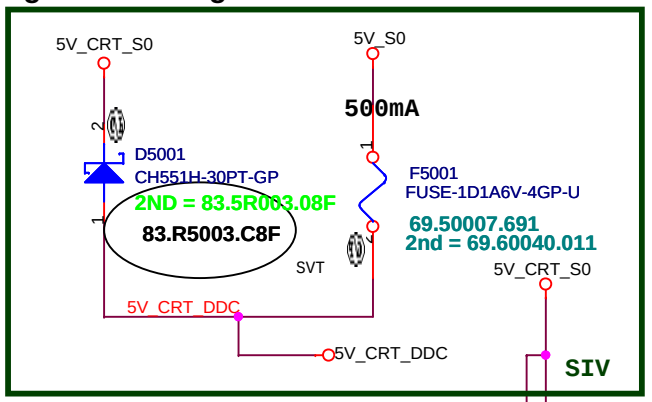
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD/Inverter Connector		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 49 of 103	

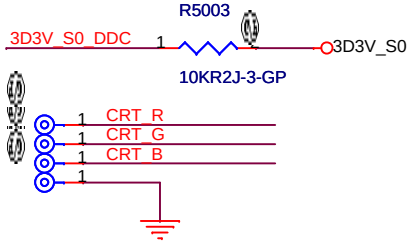
CRT connector



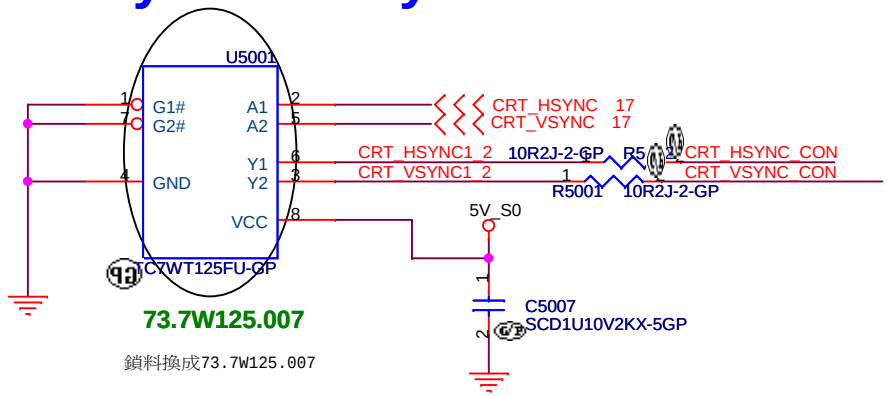
CRT DDCDATA & DDCCLK level shift

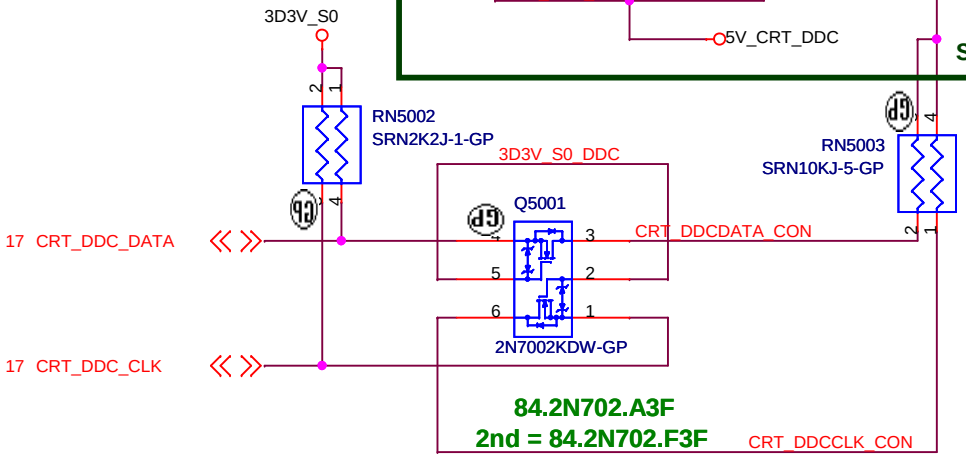
Pull High 5V Design on CRT Board





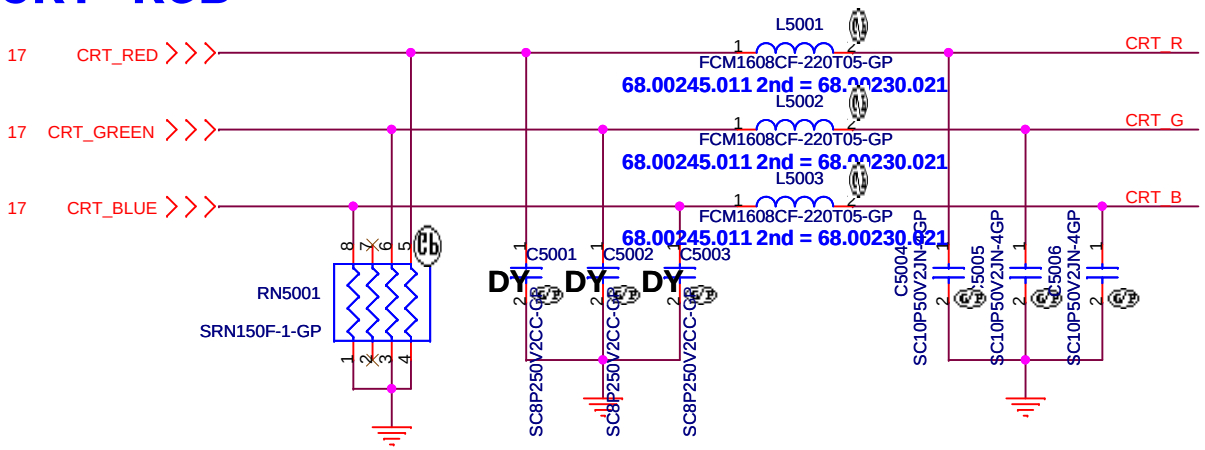
CRT Hsync & Vsync level shift

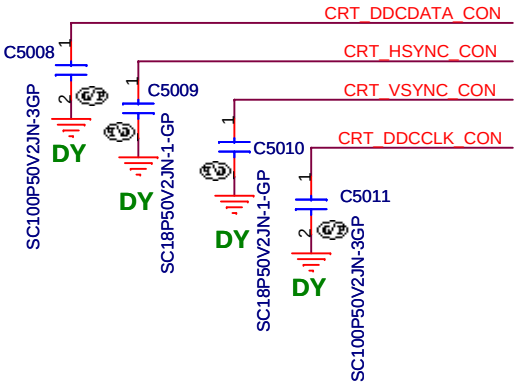




CRT RGB

R,G,B place 22pF and ESD diode for intel check list





JV10-CS

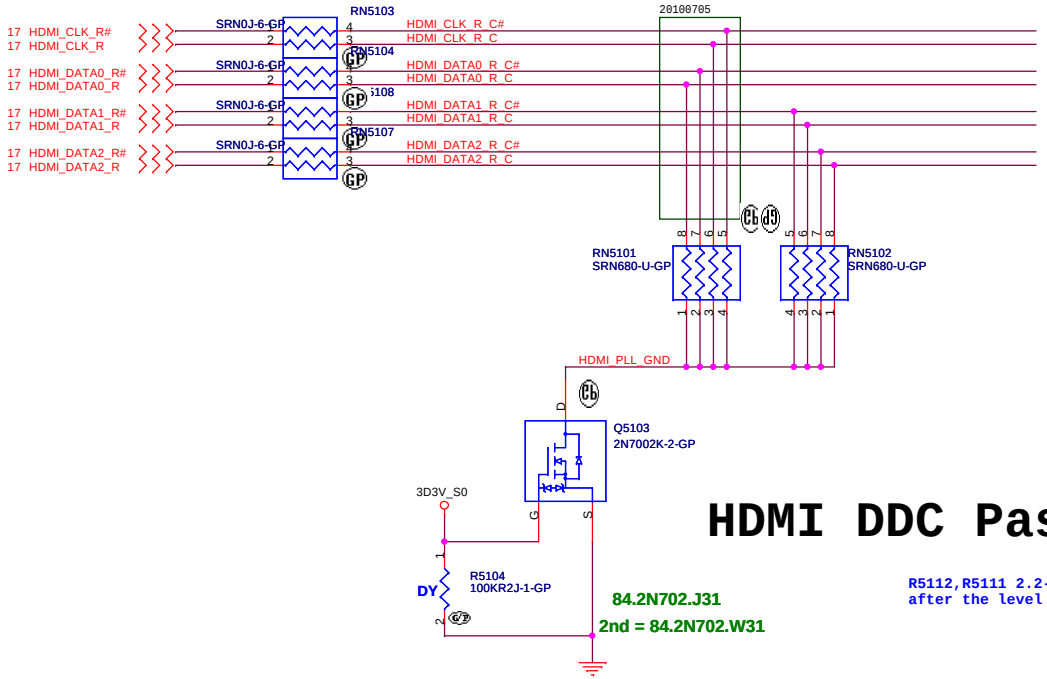
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Board Connector***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 50 of 103	

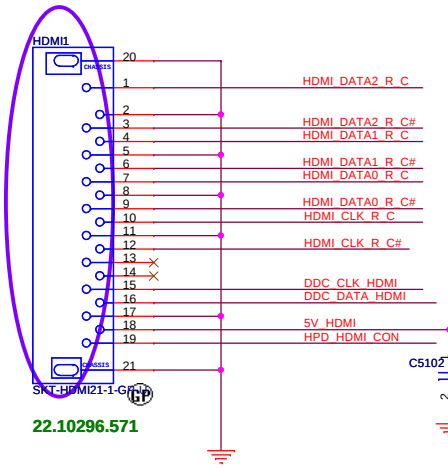
SSID = VIDEO

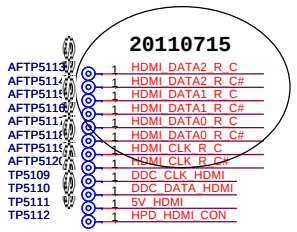
HDMI CONNECTOR

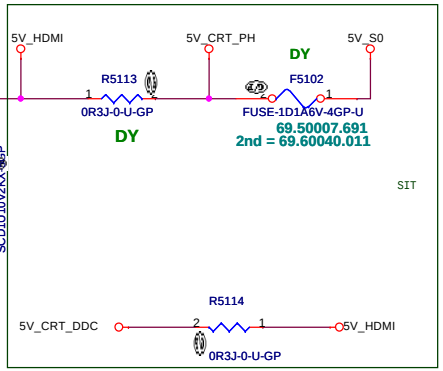
HDMI Passive Level Shifter

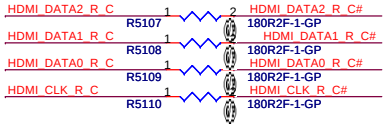
Close to HDMI Connector





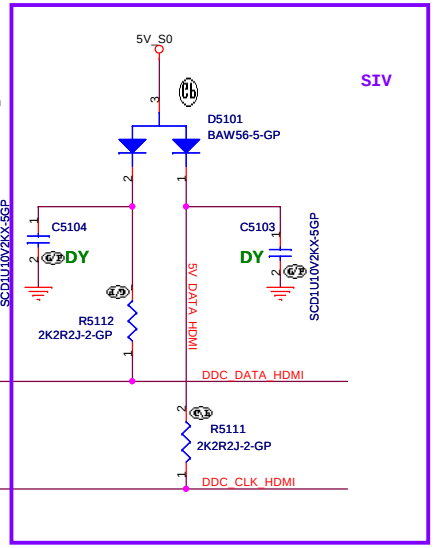


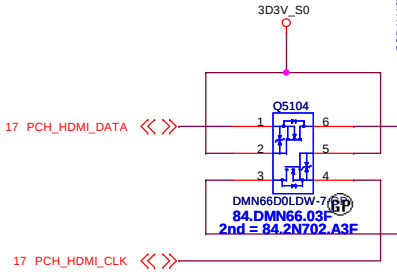


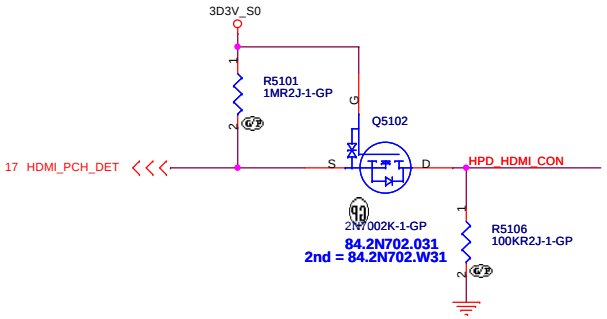


HDMI DDC Passive Level Shifter

R5112,R5111 2.2-kΩ ±5% pull-up to 5 V
after the level shifter for intel check list







JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Conn	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 51 of 103	

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Display Port*

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 52 of 103

(Blanking)

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)S-Video***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 53 of 103	

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)DVI***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 54 of 103	

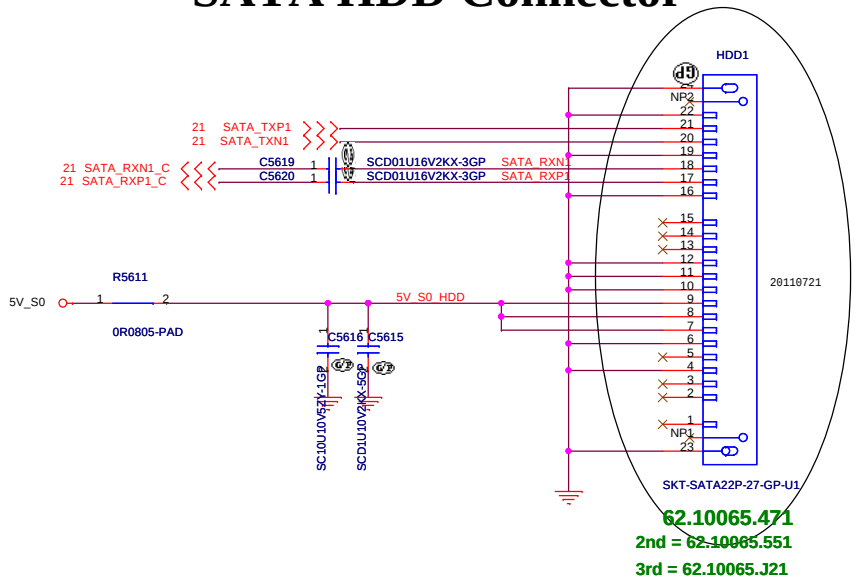
(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)ITP***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 55 of 103	

SSID = SATA

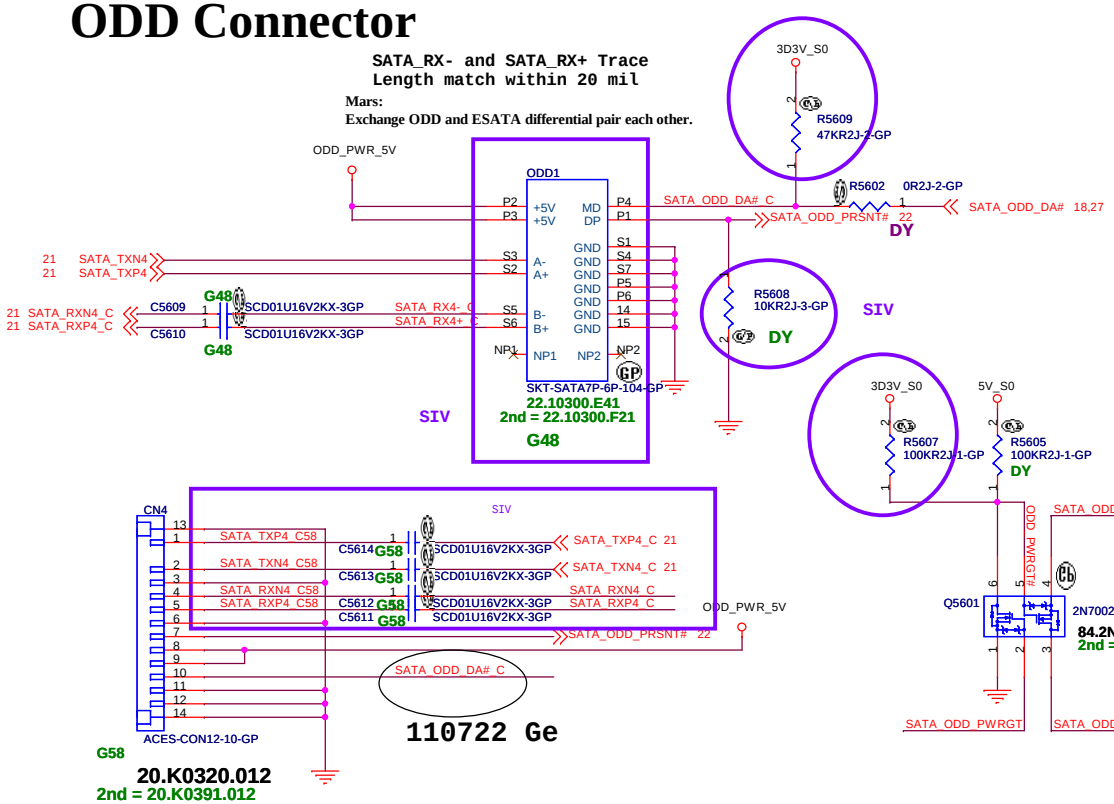
SATA HDD Connector



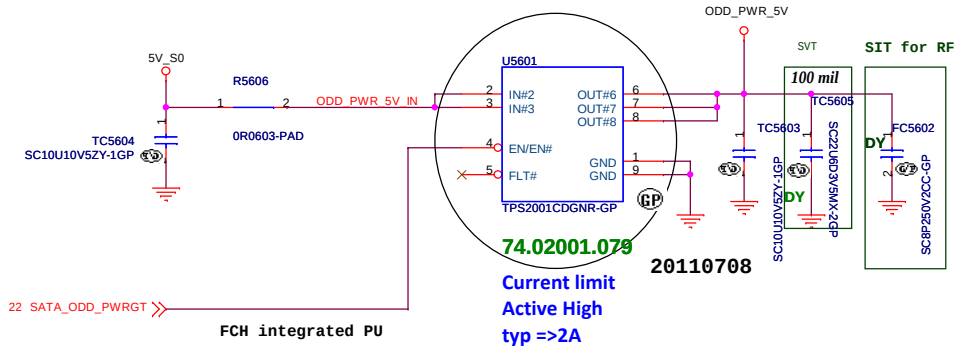
ODD Connector

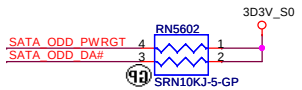
SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD





SUPPORT ZERO SATA ODD

JV10-CS

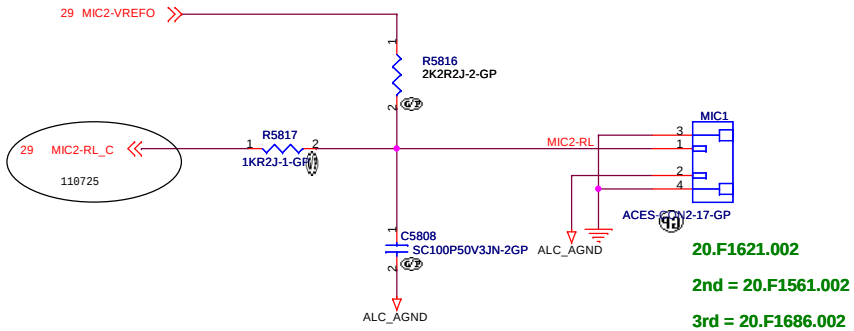
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 56 of 103	

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)E-SATA***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 57 of 103	

Analog Internal Mic



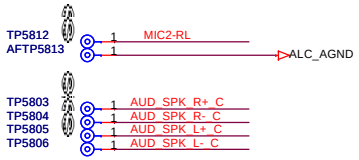
20.F1621.002

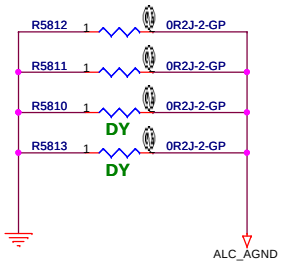
2nd = 20.F1561.002

3rd = 20.F1686.002

4nd = 20.F0693.002

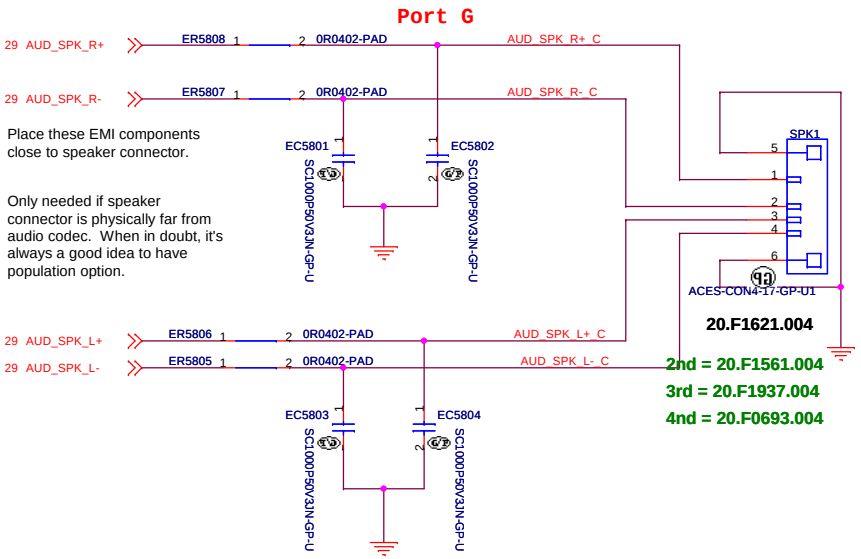
For EMI request:
Change C5801,C5802 to varister 69.80024.001





SIV
Remove bestbuy

INTERNAL STEREO SPEAKERS



20.F1621.004

2nd = 20.F1561.004

3rd = 20.F1937.004

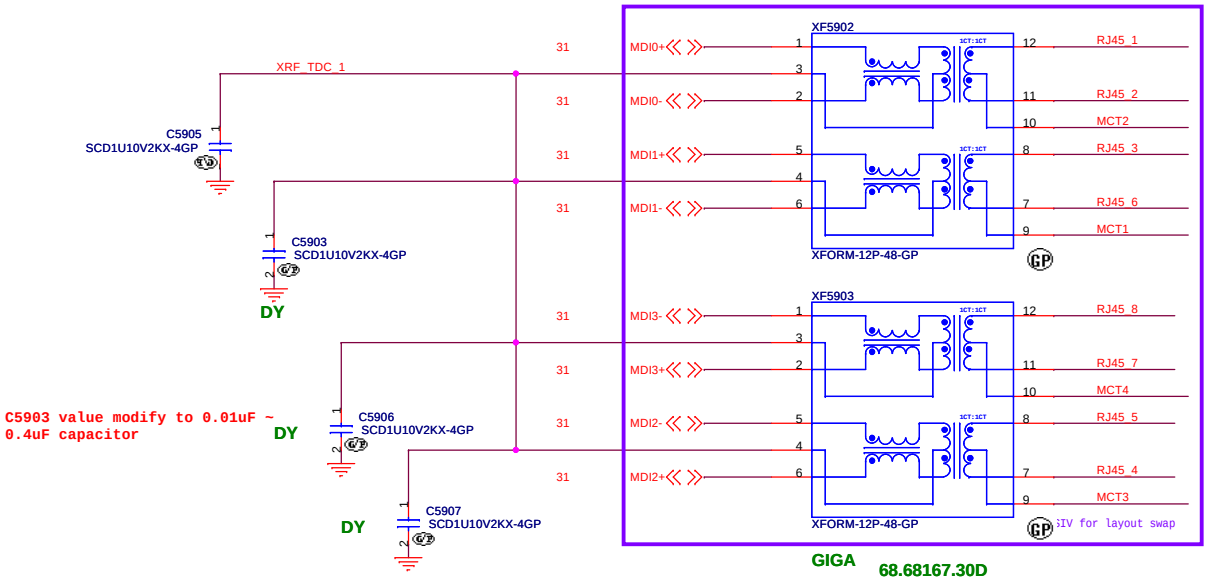
4nd = 20.F0693.004

JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MIC/SPEAKER/AUDIO JACK		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 58 of 103	

10/100M Lan Transformer

FOR CO-LAY GIGA Lan Transformer



68.68167.30D

2nd = 68.0NS14.301

3rd = 68.HD081.30B

68.68167.30D

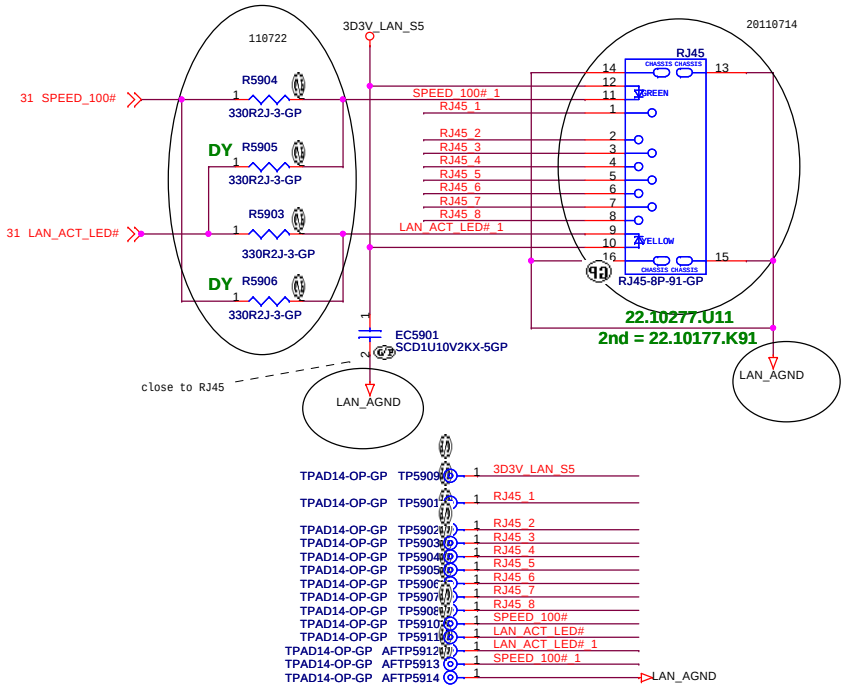
2nd = 68.0NS14.301

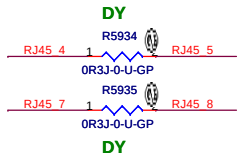
3rd = 68.HD081.30B

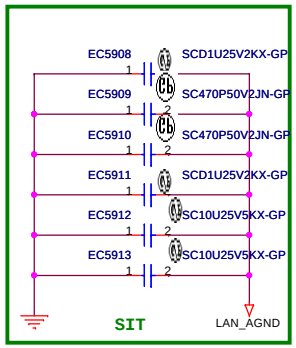
1.route as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For AR8162(10/100M): C5906, C5907,R5938, R5939 can be DY.
For AR8161(GIGA): Dummy R5934, R5935, R5940,R5941

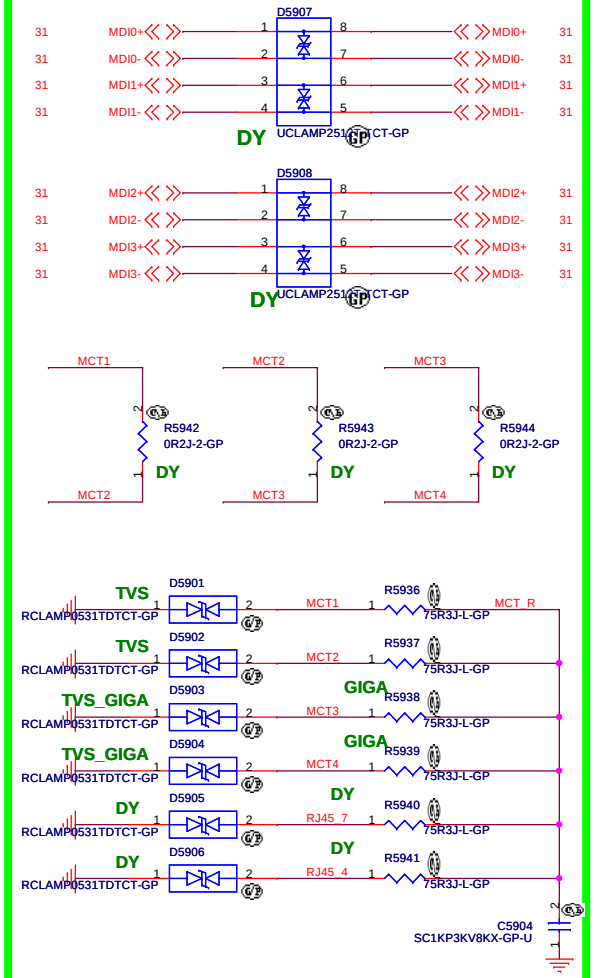
LAN Connector







10/100 LAN surge circuit



83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

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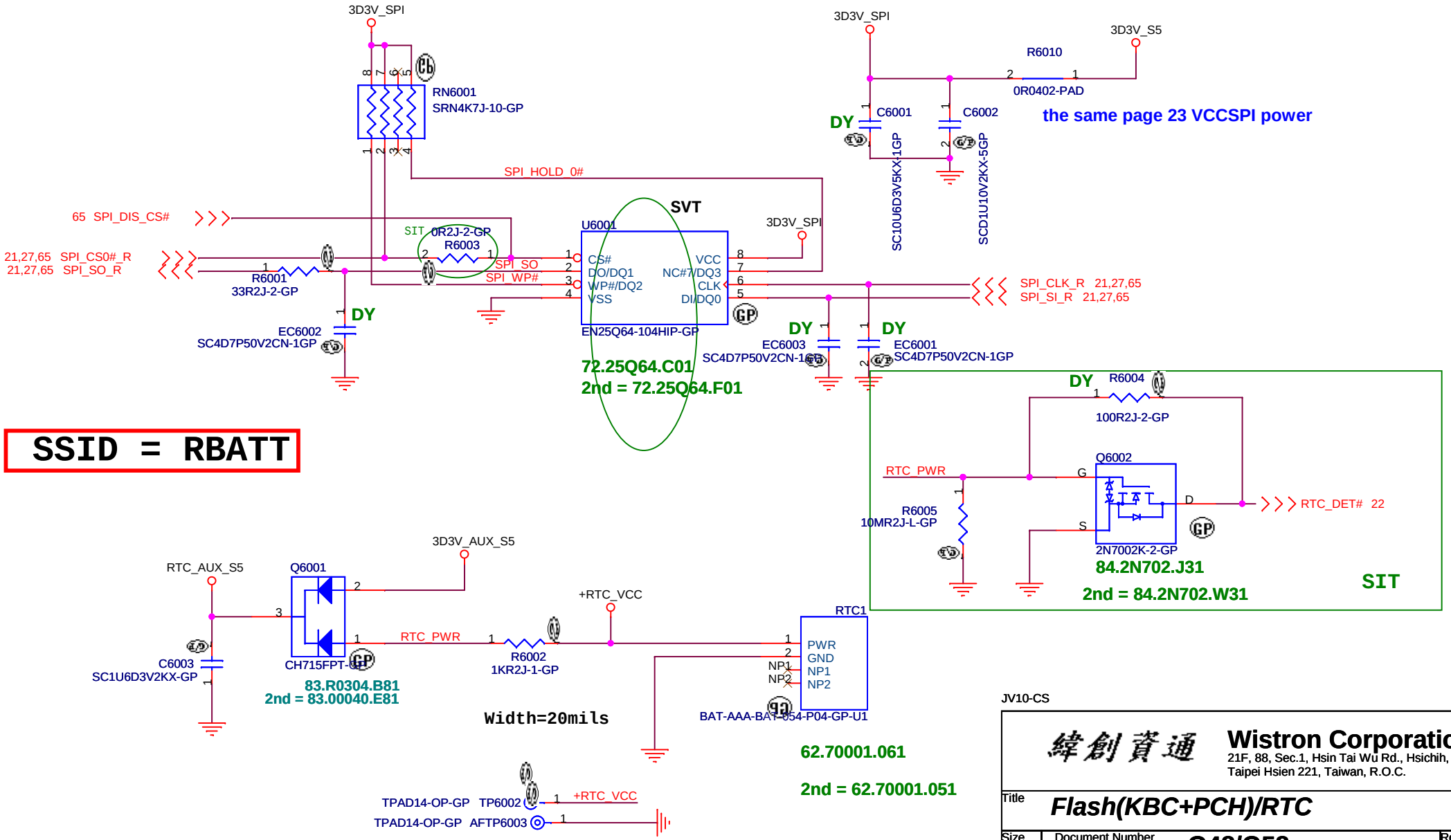
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RJ45		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



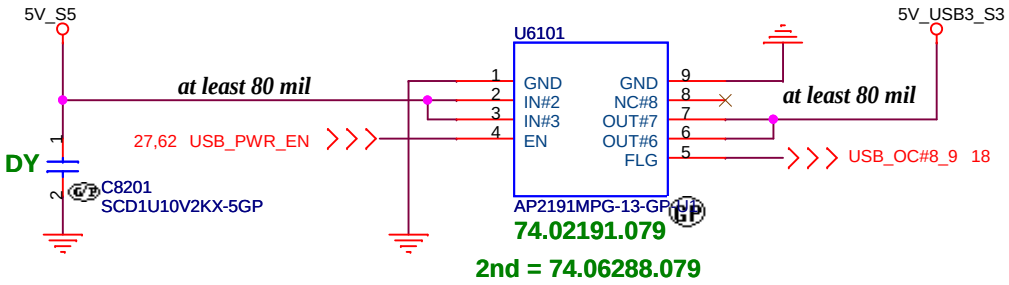
JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Flash(KBC+PCH)/RTC*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 60 of 103	

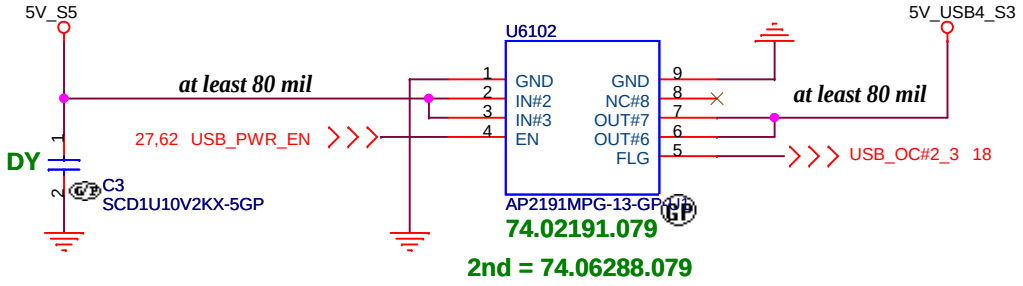
SSID = USB

USB Ext. port3 power SW



U6101 place near to USBCN3

USB Ext. port4 power SW



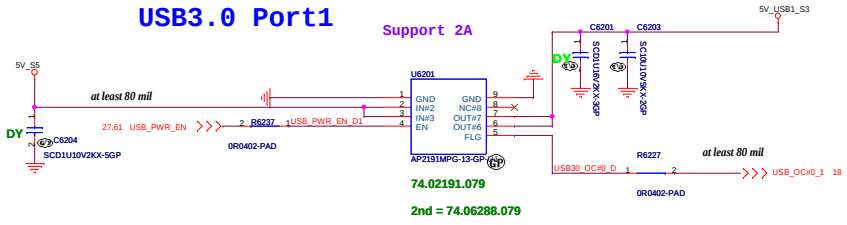
U6102 place near to CDRCN2

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB2.0 Port Power SW***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 61 of 103	

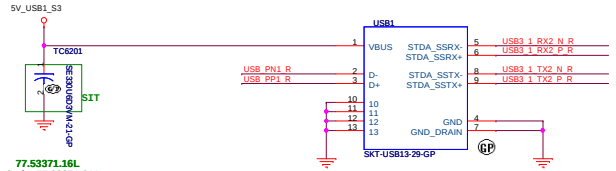
USB3.0 Port1

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

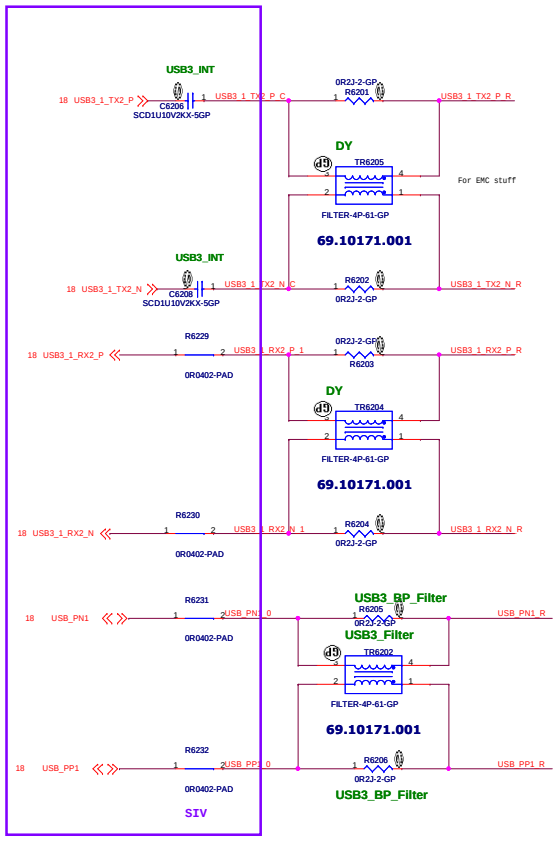
2nd = 77.93371.011

22.10339.931

2nd = 22.10339.C11

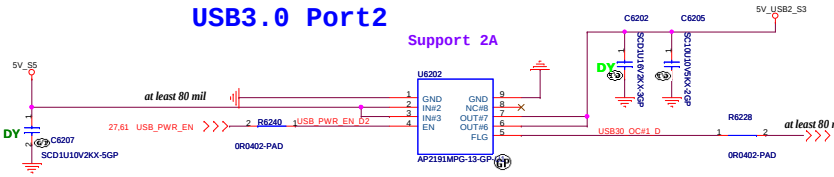
TC6201 place near
the USB1 connector

Co-Layout USB2.0 22.10321.S01



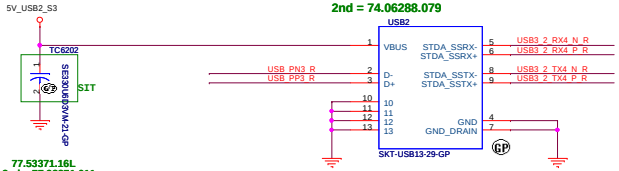
USB3.0 Port2

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

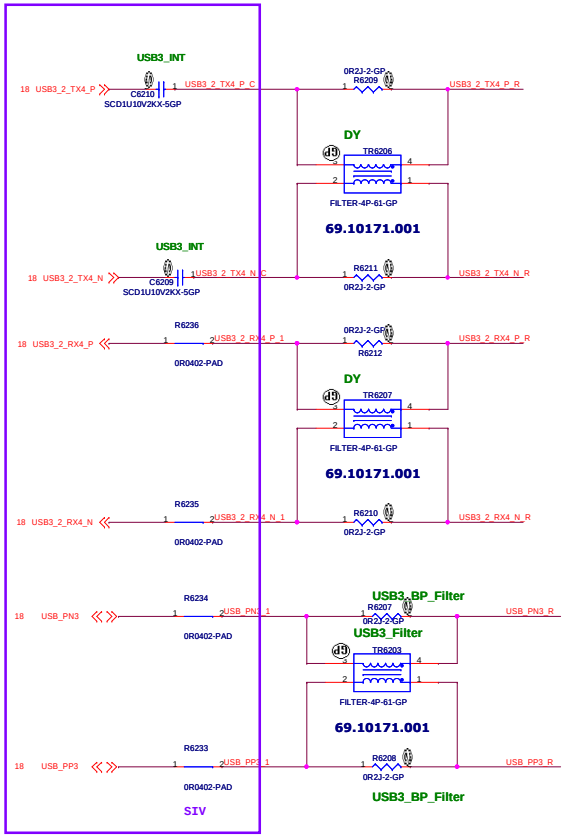
2nd = 77.93371.011

22.10339.931

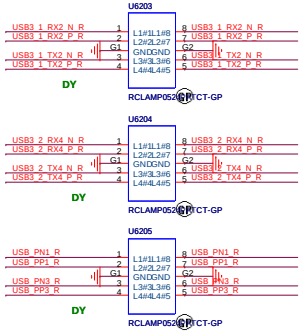
2nd = 22.10339.C11

TC6202 place near
the USB2 connector

Co-Layout USB2.0 22.10321.S01



LAN surge circuit



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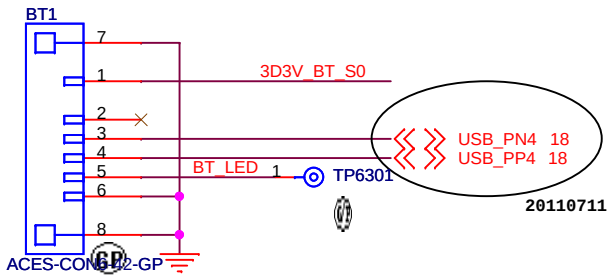
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 Port1/2	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 62 of 103	

SSID = User.Interface

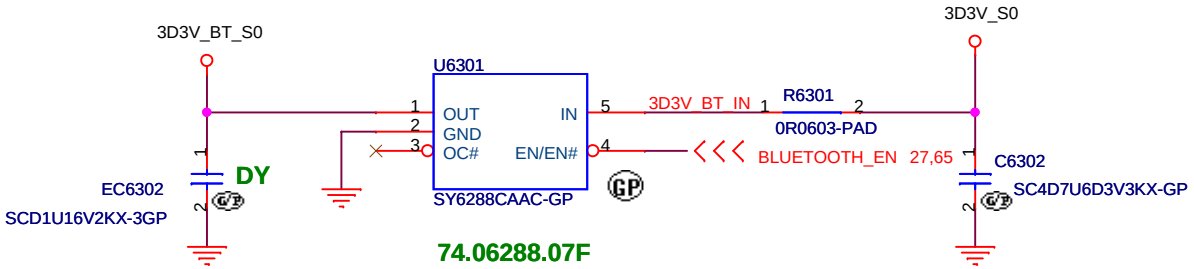
Bluetooth conn.



20.F1705.006

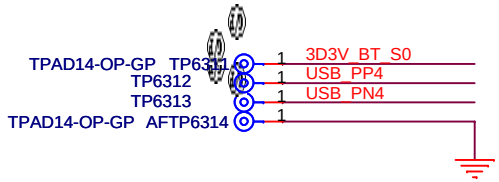
2nd = 20.F1804.006

3rd = 20.F1571.006



74.06288.07F

EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BLUETOOTH***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 63 of 103	

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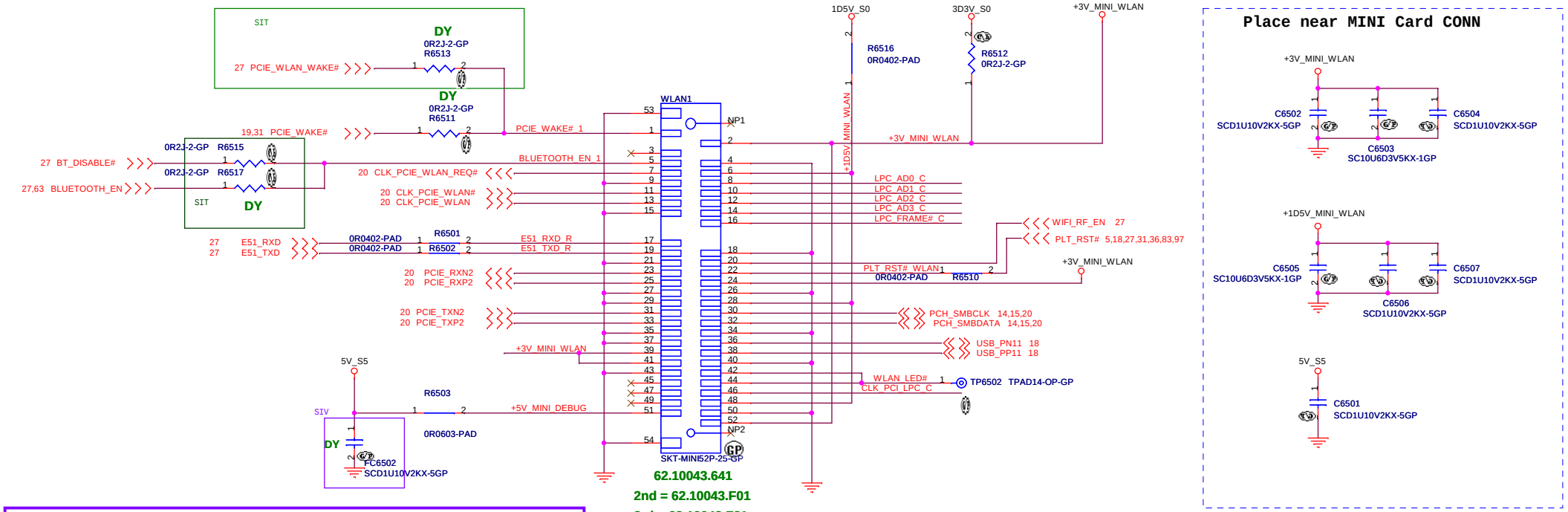
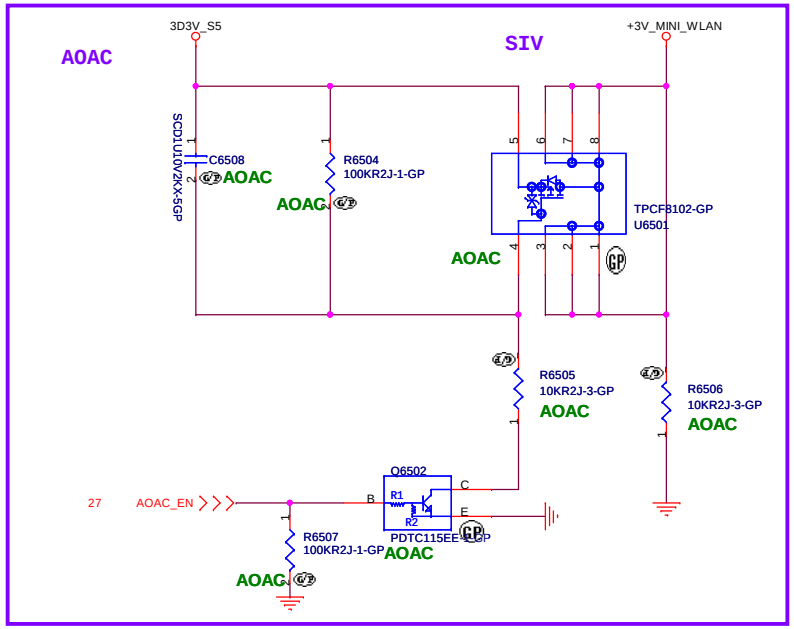
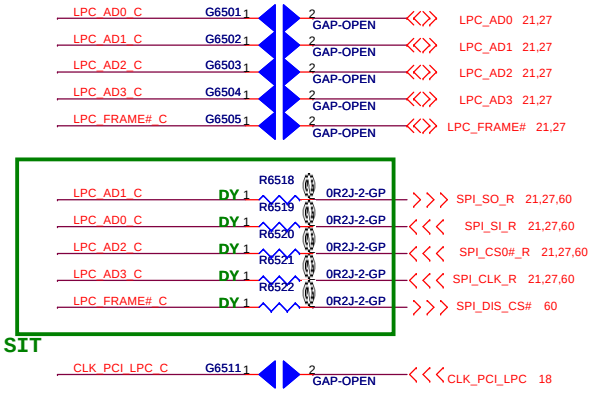
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)Finger Print Con.***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 64 of 103	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)







JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***WLAN***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 65 of 103	

SSID = Wireless

Mini Card Connector(WWAN)

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)WWAN CONN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 66 of 103	

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JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

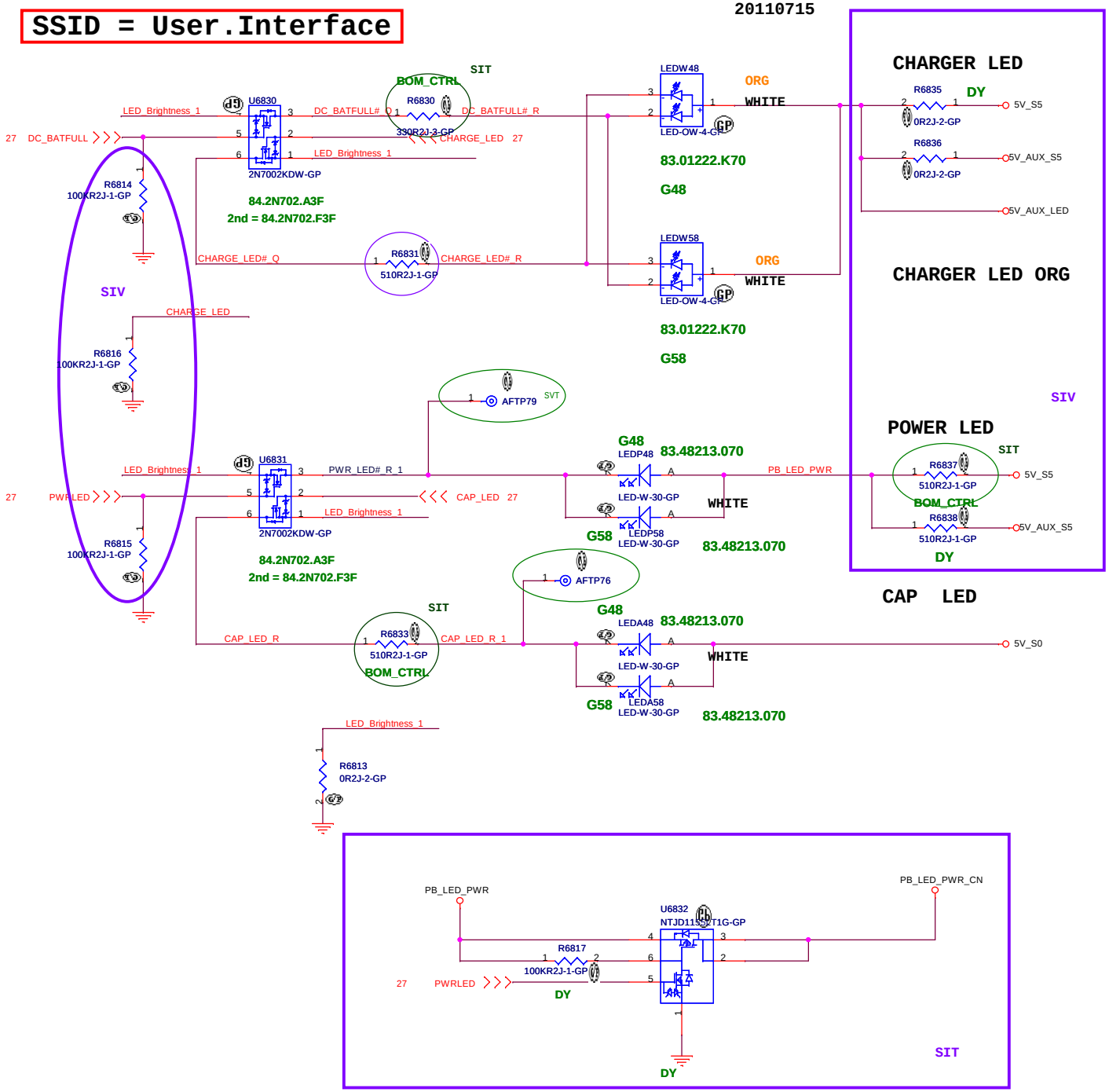
Title: ***(Reserved)3rd MINICARD***

Size	Document Number	Rev
	G48/G58	**SC**

Date: Friday, February 17, 2012 Sheet 67 of 103

SSID = User.Interface

20110715



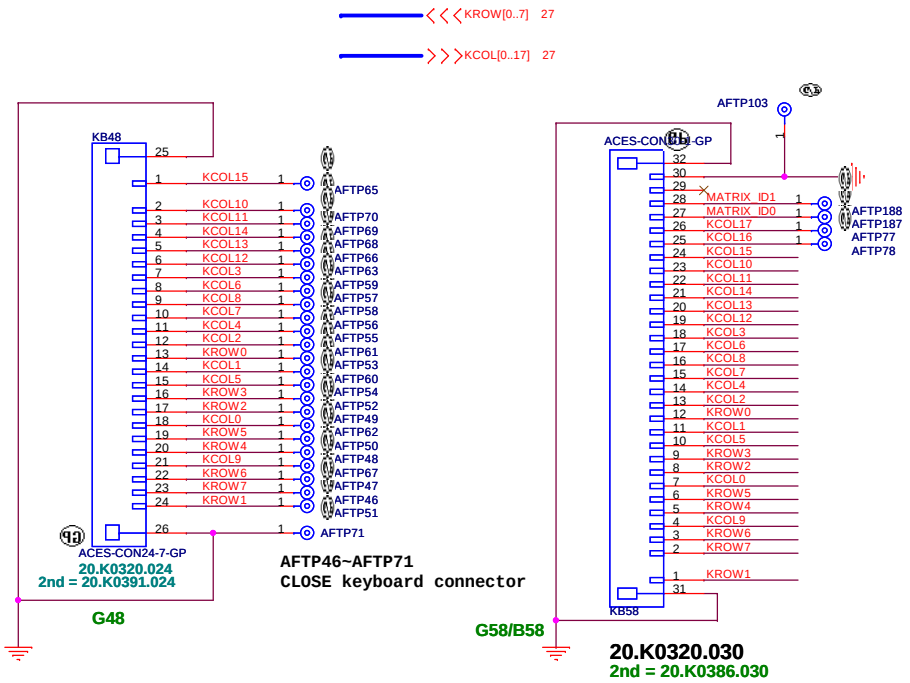
JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LED/Power Button/key*		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 68 of 103	

SSID = KBC

KB1 Follow LA47

Internal KeyBoard Connector



14"

* Membrane Pin Out Top View :

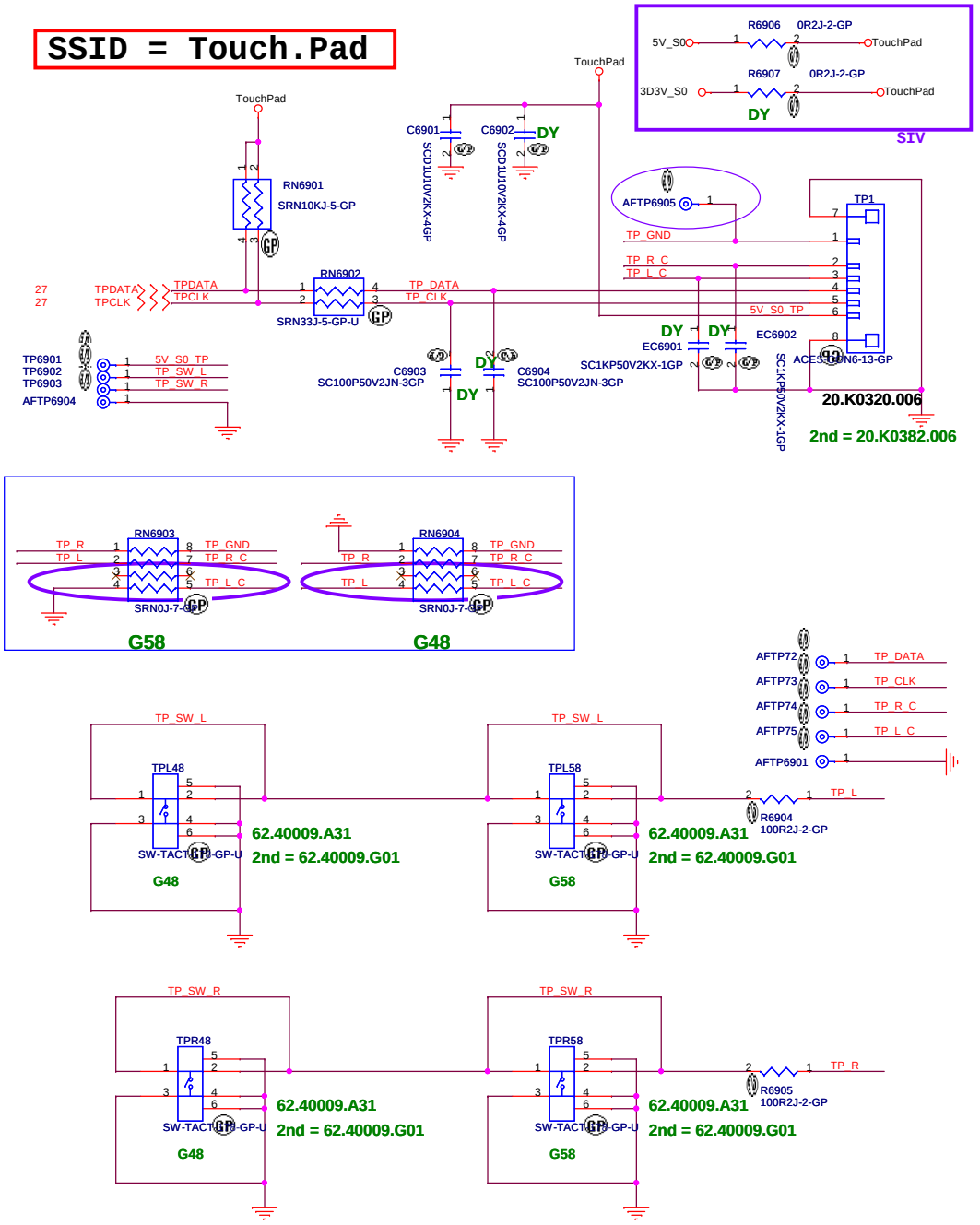
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	S1	S2	S3	S4	S5	S6	S7	S8

15"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
As-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	S1	S2	S3	S4	S5	S6	S7	S8

SSID = Touch.Pad



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Key Board/Touch Pad	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 69 of 103	

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Hall Sensor***

Size	Document Number	Rev
	G48/G58	**SC**

Date: Friday, February 17, 2012 Sheet 70 of 103

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Debug connector*

Size	Document Number	Rev
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Date: Friday, February 17, 2012 Sheet 71 of 103

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JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)RJ11+MDC***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 72 of 103	

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)1394 CONN*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 73 of 103	

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)CARD Reader CONN*

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 74 of 103

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JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Express Card***

Size	Document Number	Rev
	G48/G58	**SC**

Date: Friday, February 17, 2012 Sheet 75 of 103

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)Smart Card Socket*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 76 of 103	

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JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)TPM***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 77 of 103	

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)SIO*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 78 of 103	

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JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)G-Sensor***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 79 of 103	

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JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)RF/Other*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 80 of 103	

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JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)Screw Holes,SPR***

Size	Document Number	Rev
	G48/G58	**SC**

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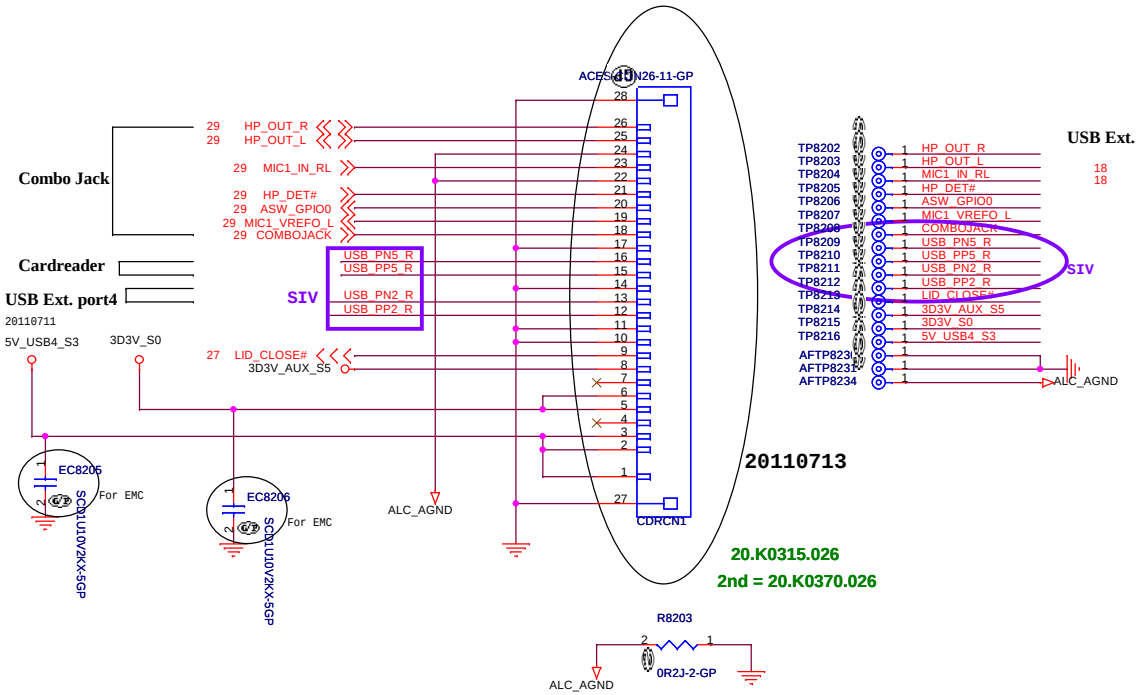
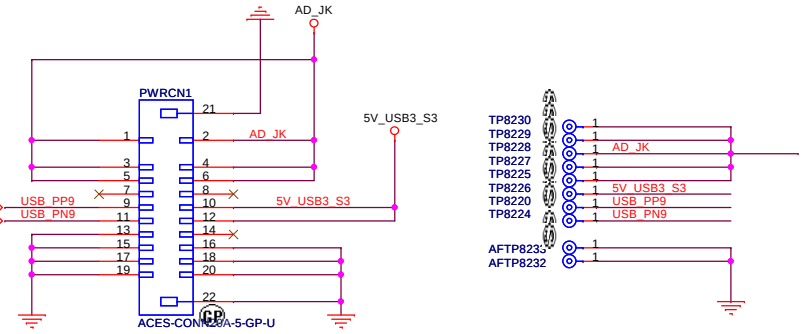
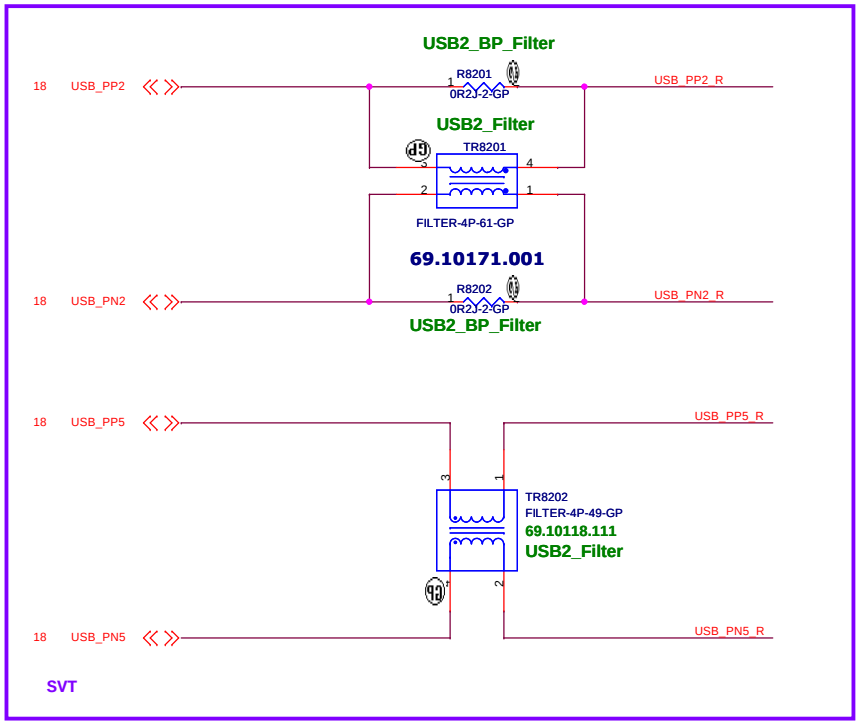
Cardreader BD connector (Cardreader/Combo Jack/USB2.0 port4)



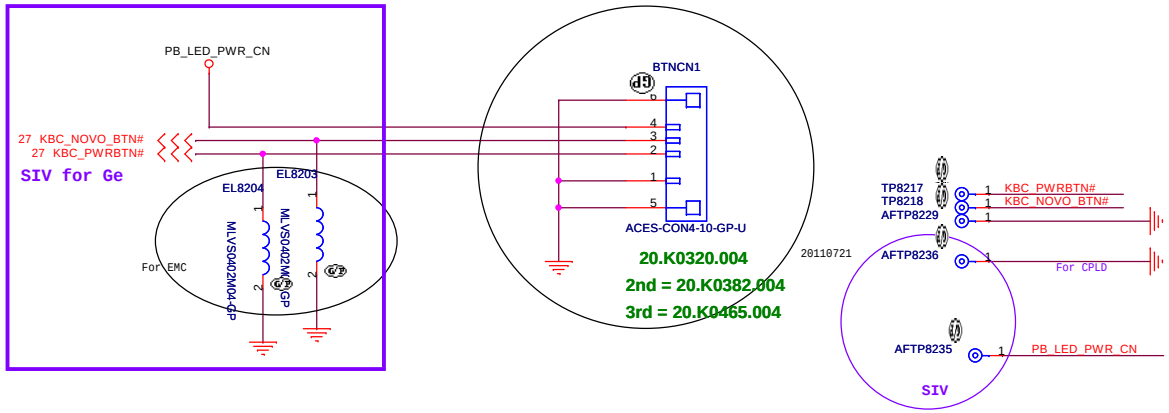
USB Ext. port3

USB BD connector (DC Jack/USB2.0 port3)



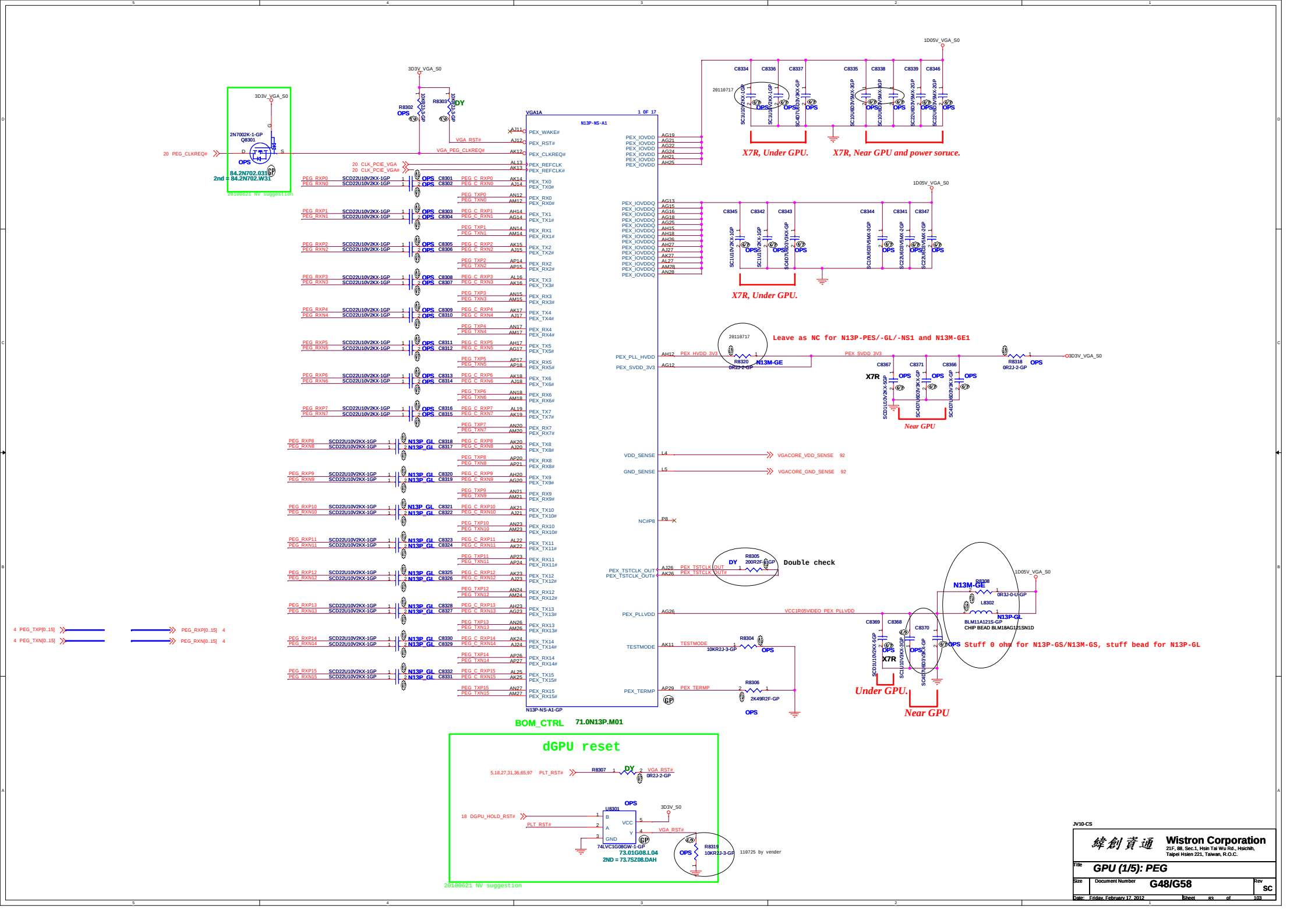


Button BD connector (Power button/NOVO button)



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	IO Board Connector	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 82 of 103	


VGA1A
1 OF 17
N13P-NS-A1
N13P-NS-A1-GP
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
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PEX_TX5
PEX_TX5#
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PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
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PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
PEX_IOVDD
PEX_IOVDDQ
PEX_PLL_HVDD
PEX_SVDD_3V3
VDD_SENSE
GND_SENSE
NC#P8
PEX_TSCLK_OUT
PEX_TSCLK_OUT#
PEX_PLLVDD
TESTMODE
PEX_TERMP
VGA_RST#
VGA_PEG_CLKREQ#
20 PEG_CLKREQ#
20 CLK_PCIE_VGA
20 CLK_PCIE_VGA#
PEG_RXP0
PEG_RXN0
PEG_TXP0
PEG_TXN0
PEG_RXP1
PEG_RXN1
PEG_TXP1
PEG_TXN1
PEG_RXP2
PEG_RXN2
PEG_TXP2
PEG_TXN2
PEG_RXP3
PEG_RXN3
PEG_TXP3
PEG_TXN3
PEG_RXP4
PEG_RXN4
PEG_TXP4
PEG_TXN4
PEG_RXP5
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PEG_RXP15
PEG_RXN15
PEG_TXP15
PEG_TXN15
4 PEG_TXP[0..15]
4 PEG_TXN[0..15]
PEG_RXP[0..15] 4
PEG_RXN[0..15] 4
3D3V_VGA_S0
1D05V_VGA_S0
2N7002K-1-GP
Q8301
84.2N702.031
2nd = 84.2N702.W31
20100621 NV suggestion
X7R, Under GPU.
X7R, Near GPU and power soruce.
X7R, Under GPU.
Leave as NC for N13P-PES/-GL/-NS1 and N13M-GE1
Near GPU
Double check
Under GPU.
Near GPU
Stuff 0 ohm for N13P-GS/N13M-GS, stuff bead for N13P-GL
BOM_CTRL 71.0N13P.M01
dGPU reset
18 DGPU_HOLD_RST#
PLT_RST#
5,18,27,31,36,65,97 PLT_RST#
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
110725 by vender
20100621 NV suggestion
JV10-CS
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (1/5): PEG
Size
Document Number G48/G58
Rev SC
Date: Friday, February 17, 2012
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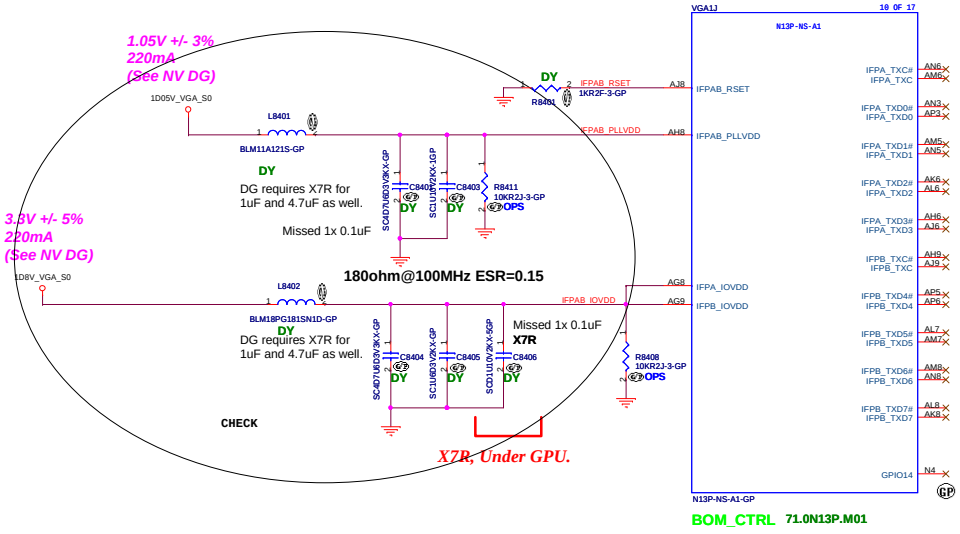
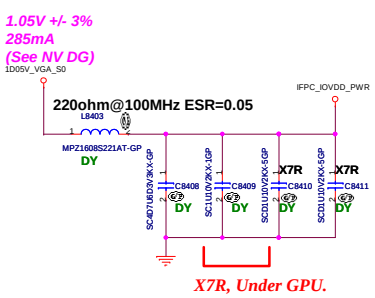
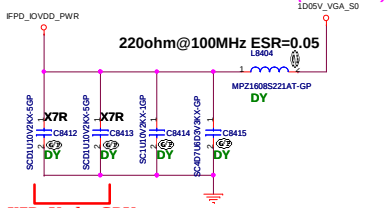
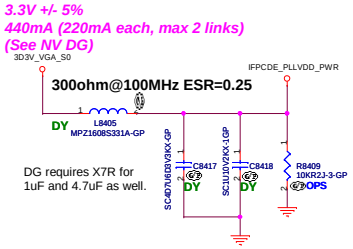
RD480_SA:71.0N12P.M08

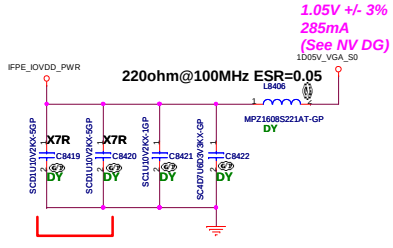
LVDS Interface

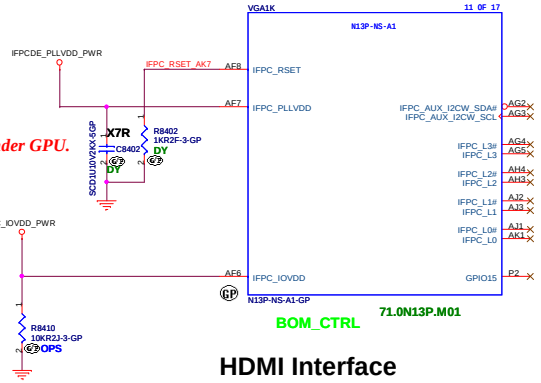




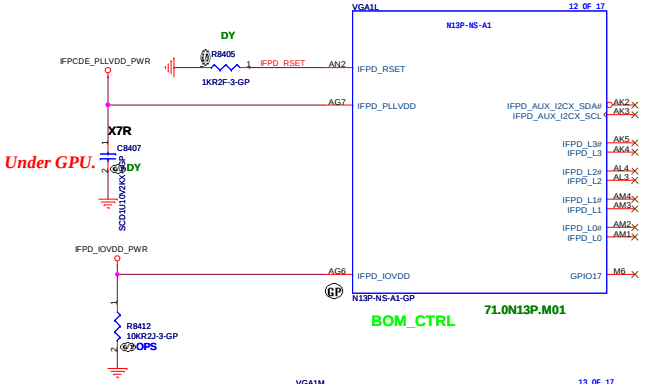


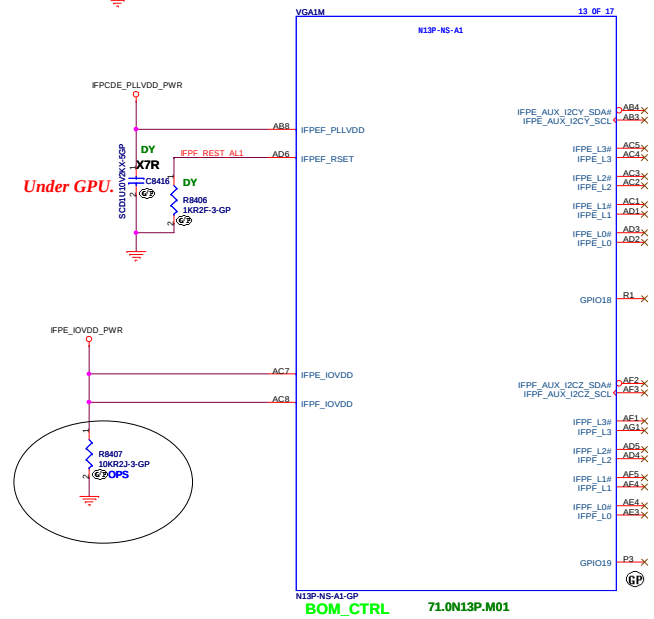






HDMI Interface





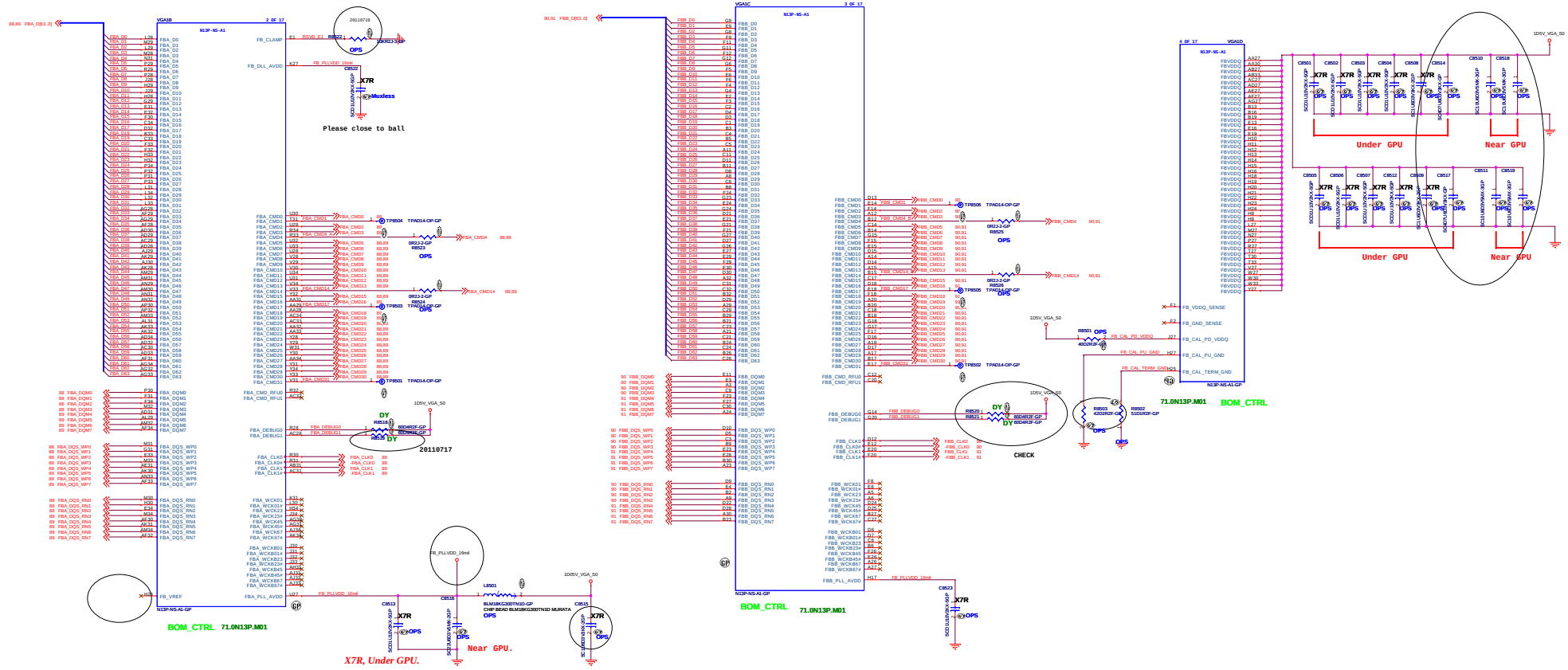
JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

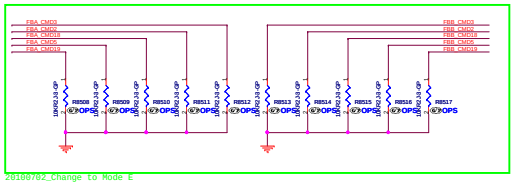
Title: GPU (2/5): DIGITALOUT

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 84 of 103



FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

JV0-CS

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU (3/5): VRAM I/F	
Size:	Document Number: G48/G58 Rev: SC
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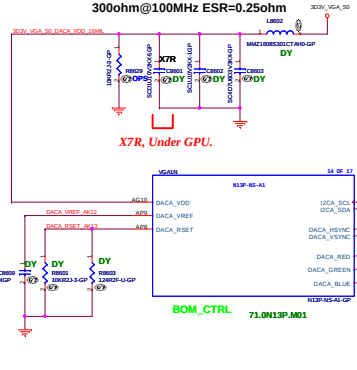
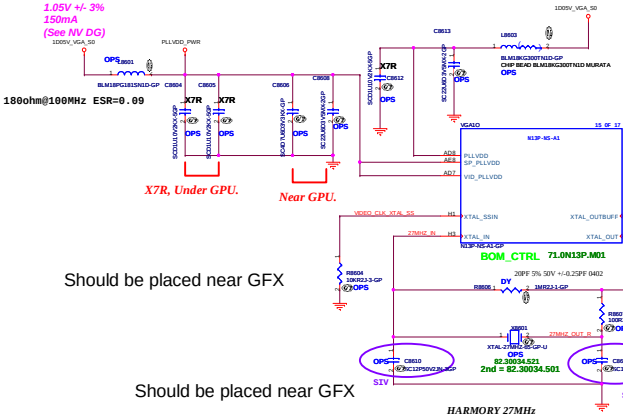
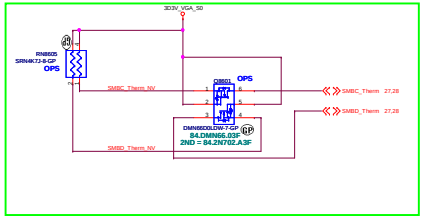
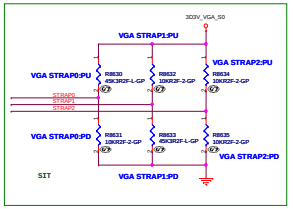
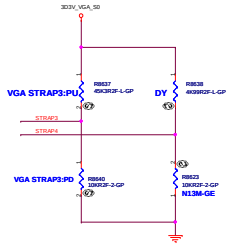
RD480_SA:71.0N12P.M08











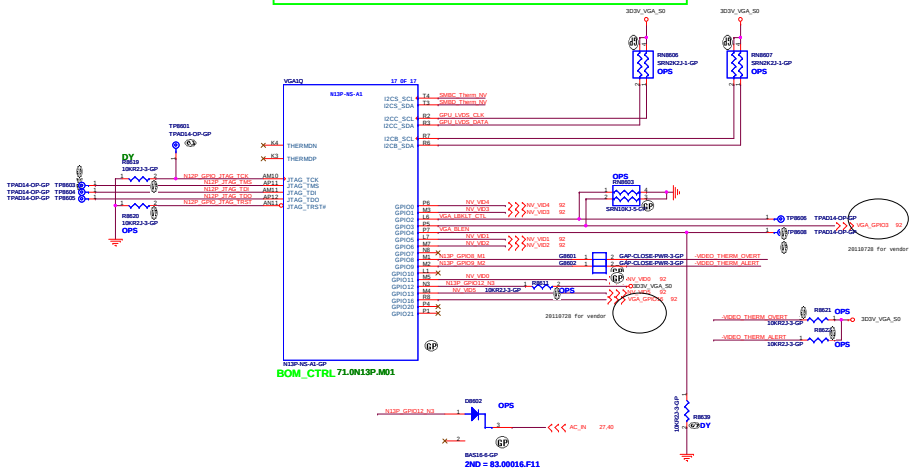
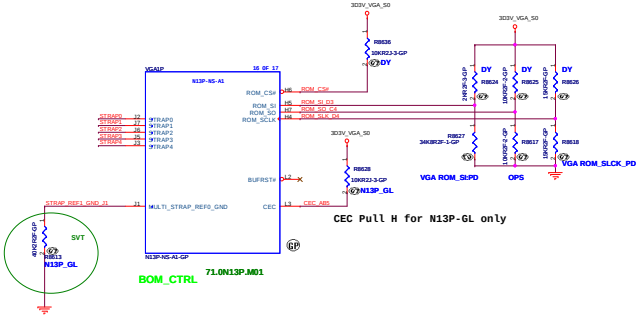


	TABLE NVIDIA	N13P-GL(PS) DEV ID: 0x0DE9
STRAP0	R8630(PU)	45.3Kohm 64.45325.6DL
	R8631(PD)	DY
STRAP1	R8632(PU)	DY
	R8633(PD)	45.3Kohm 64.45325.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL
	R8635(PD)	DY
STRAP3	R8637(PU)	DY
	R8640(PD)	DY
STRAP4	R8638(PU)	DY
	R8623(PD)	DY

	N13M-GE(PS)				
	TABLE NVIDIA	SAMSUNG 128Mx16 72.42164.D0U	SAMSUNG 128Mx16 72.42164.G0U	HYNIX 128Mx16 72.52G63.C0U	Samsung 64Mx16	HYNIX 64Mx16
STRAP0	R8630(PU)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8631(PD)	DY	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP1	R8632(PU)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8633(PD)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
	R8635(PD)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
STRAP3	R8637(PU)	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	DY
	R8640(PD)	10Kohm 64.10025.6DL	DY	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
STRAP4	R8638(PU)	DY	DY	DY	DY	DY
	R8623(PD)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL



VGA	N13P-GL(PS) 71.0N13P.E0U	N13M-GE(PS) 71.0N13M.B1U
ROM_SO PD R8617	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
ROM_SCLK PD R8618	15Kohm 64.15025.6DL	10Kohm 64.10025.6DL

TABLE
VIDEO MEMORY

Nvidia VGA	900MHz	HYNIX 128Mx16	SAMSUNG 128Mx16	HYNIX 64Mx16	Samsung 64Mx16
		72.52G63.C0U	72.42164.D0U 72.42164.G0U	72.51G63.H0U	72.41646.Q0U
N13P-GL	ROM_SI PD R8627	30.1Kohm 64.30125.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL
N13M-GE	ROM_SI PD R8627	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL

JV0-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (4/5): GPIO/STRAP
Size: Document Number: G48/G58 Rev: SC
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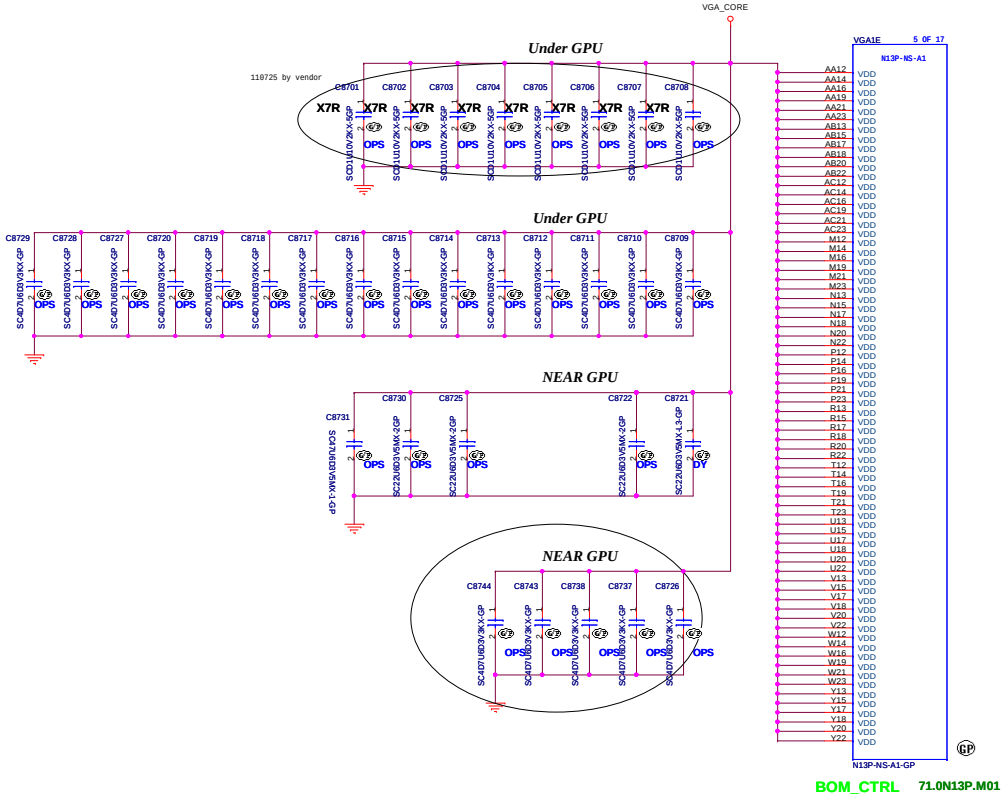
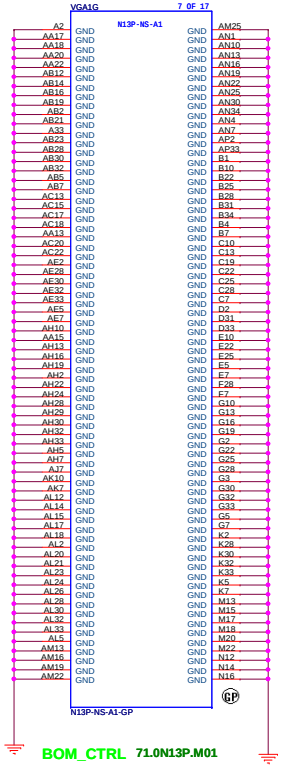
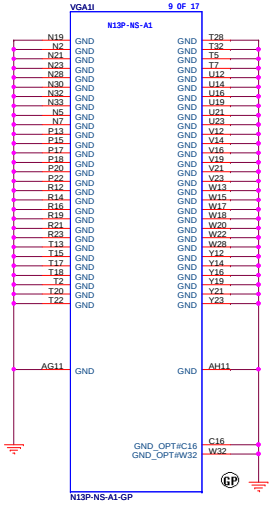
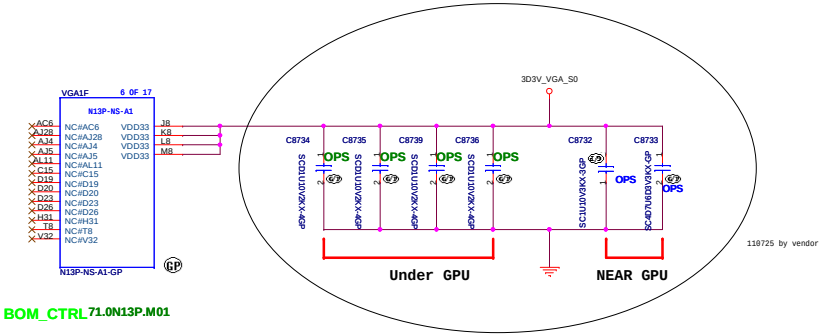
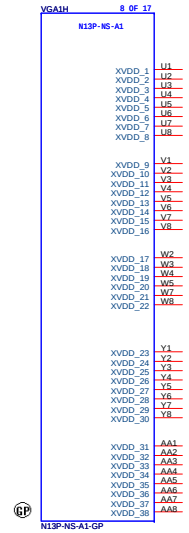








BOM_CTRL 71.0N13P.M01



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (5/5): PWR/GND

Size: | Document Number: G48/G58 | Rev: SC

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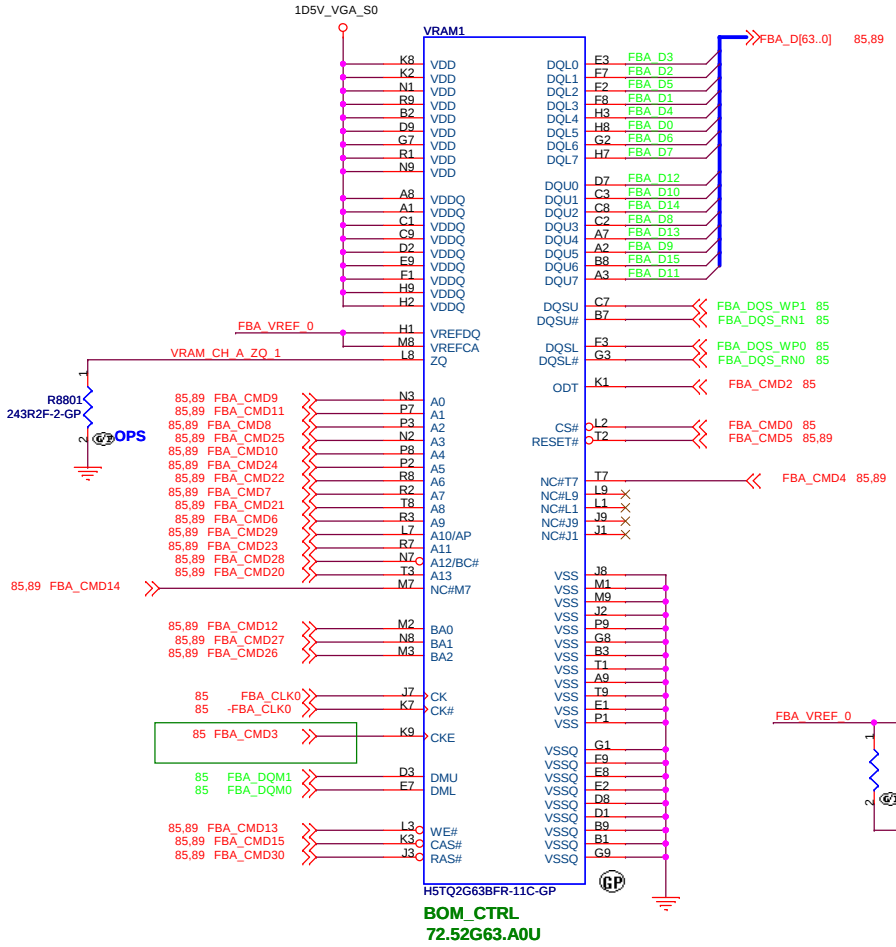
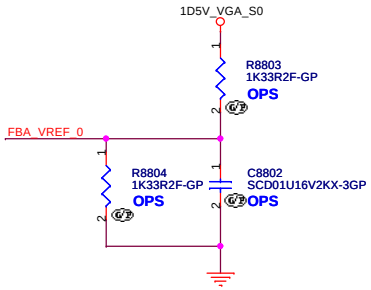
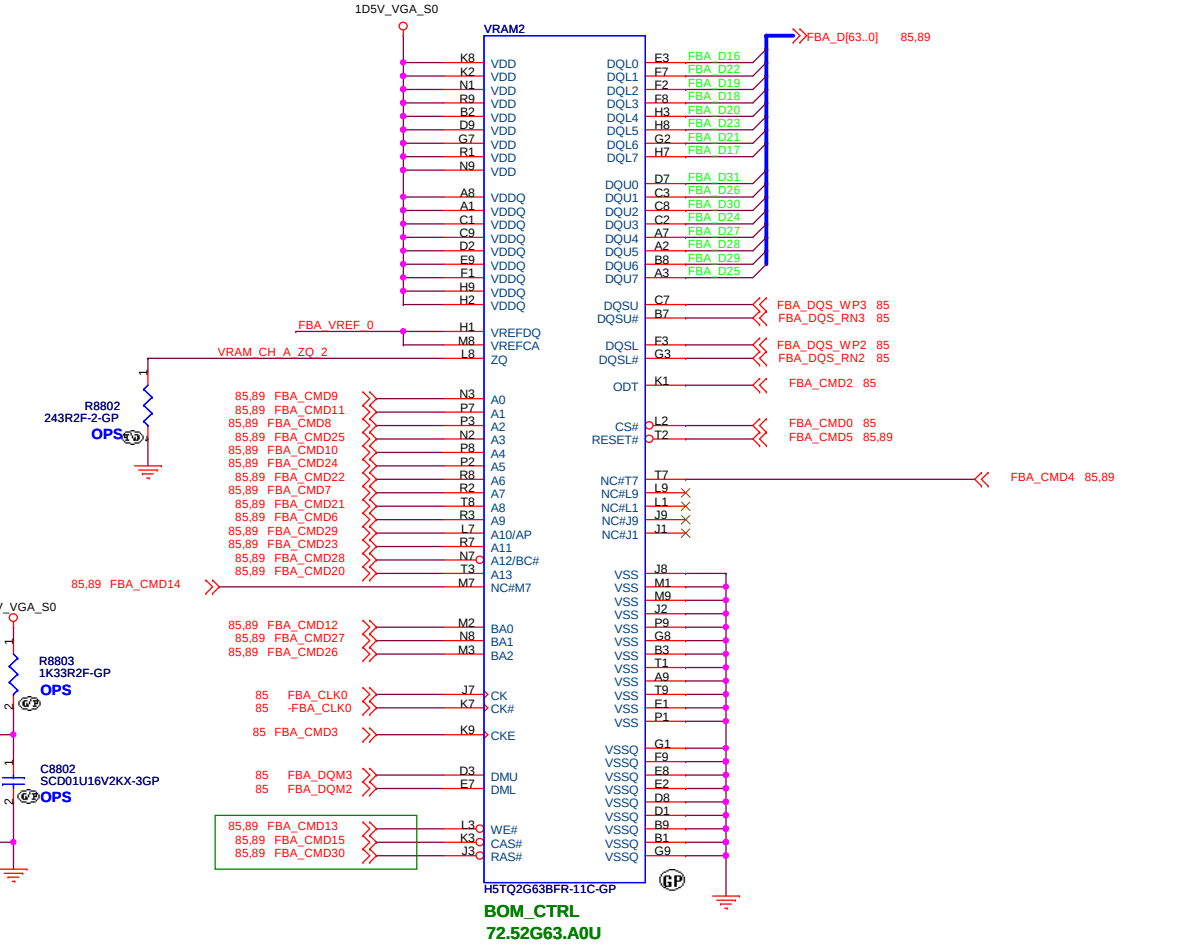
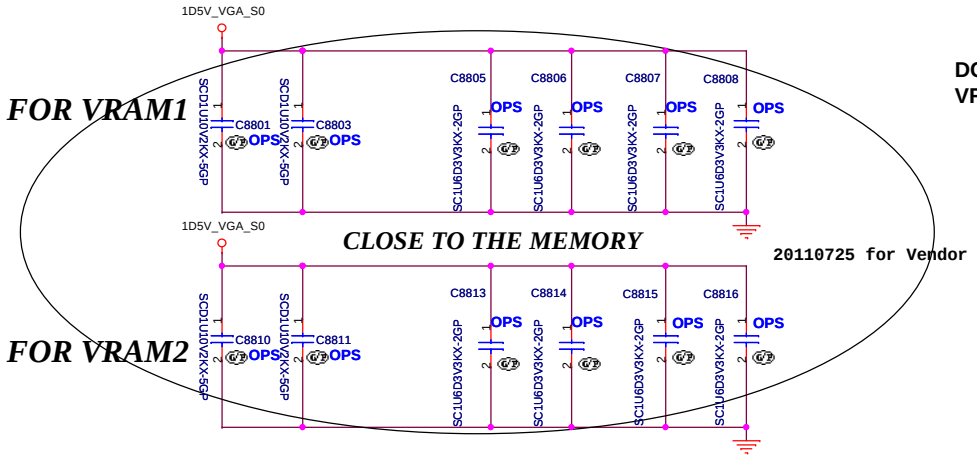
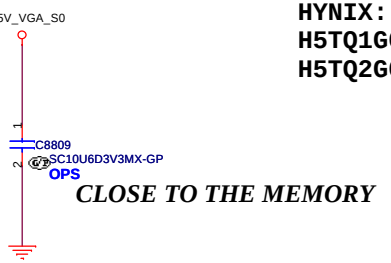








DG requires 4x0.1uF and 8x1.0uF per VRAM chip



20110725 for Vendor

VRAM

SAMSUNG:

K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz

K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:

H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz

H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT A

JV10-CS

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM1,2 (1/4)*		
Size	Document Number	G48/G58	Rev SC
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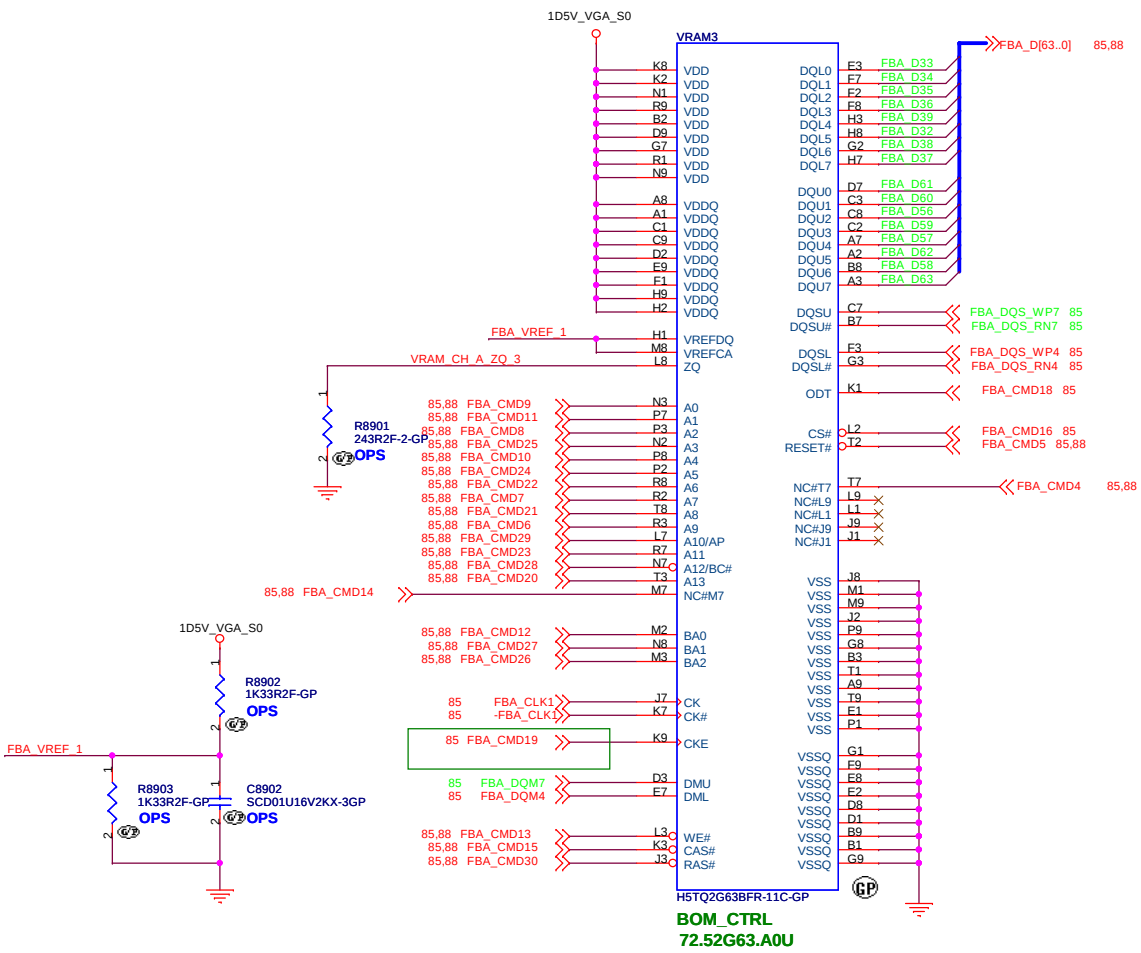

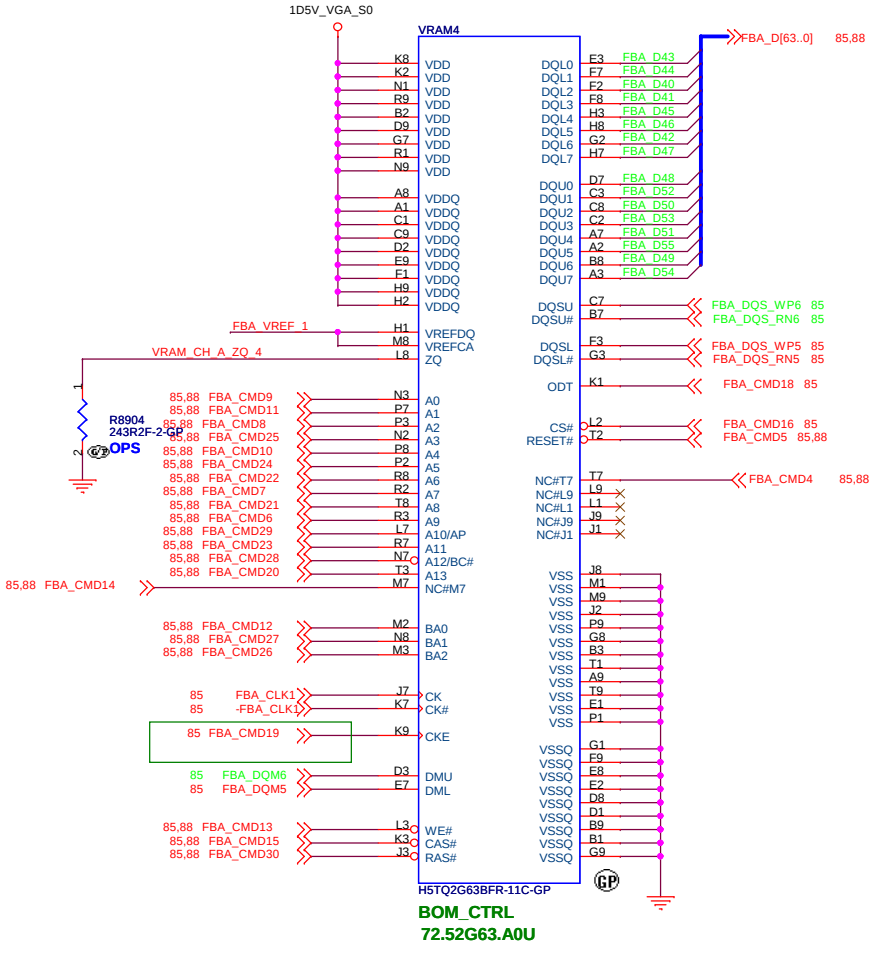

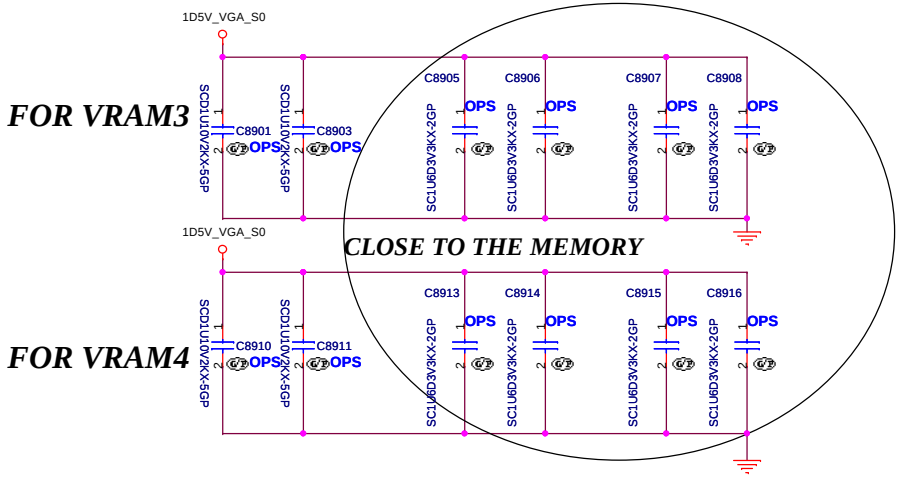

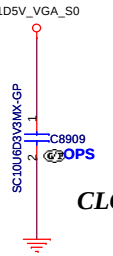

CLOSE TO THE MEMORY

VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT A

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM3,4 (2/4)	
Size	Document Number G48/G58	Rev SC
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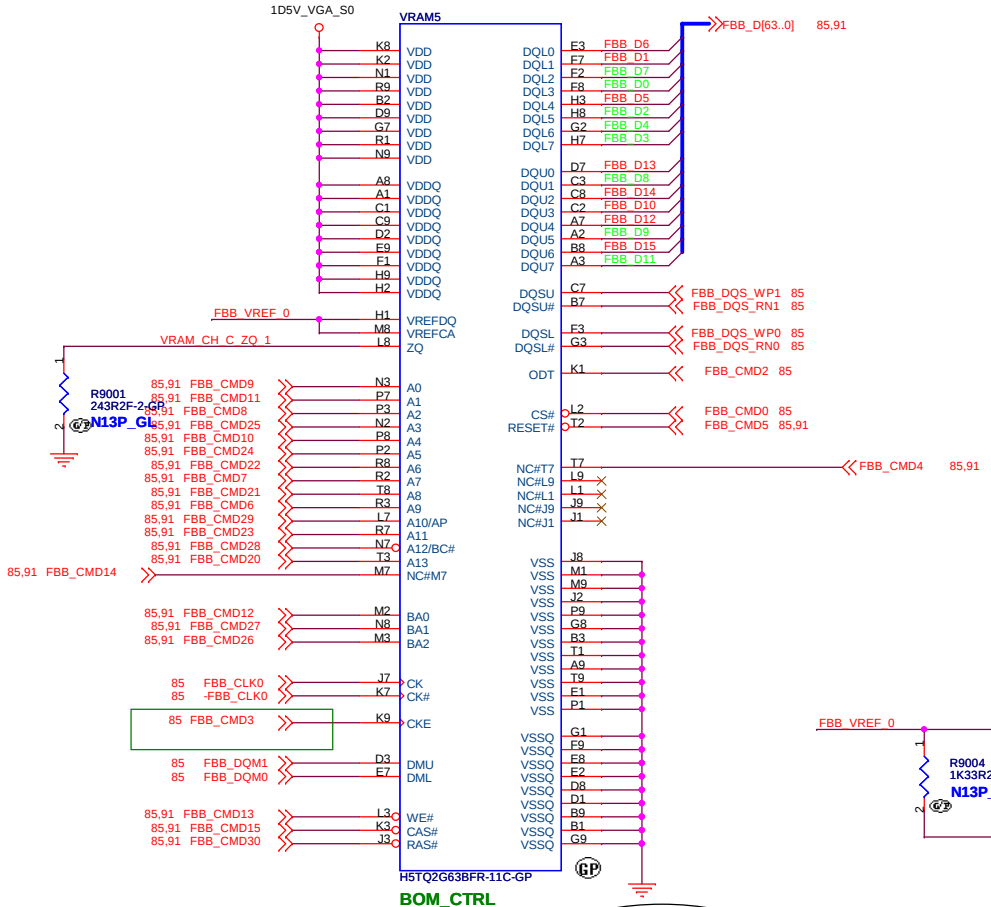
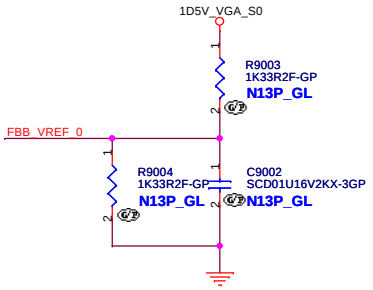
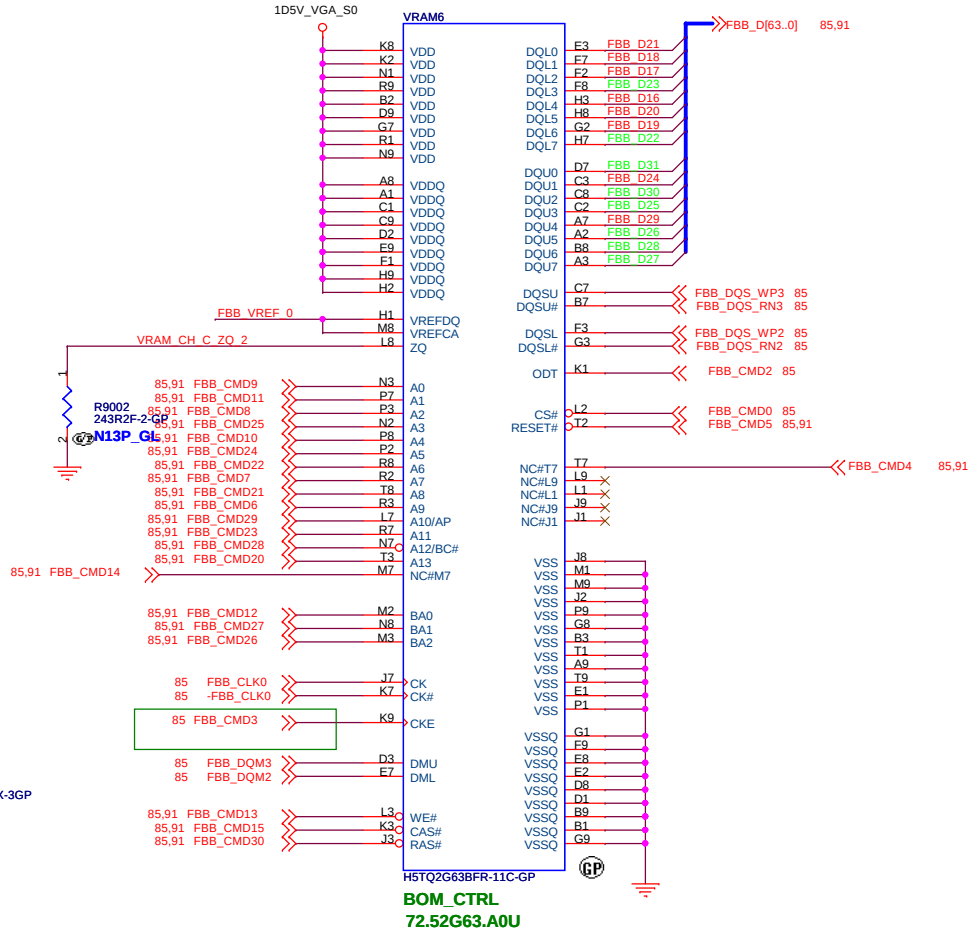


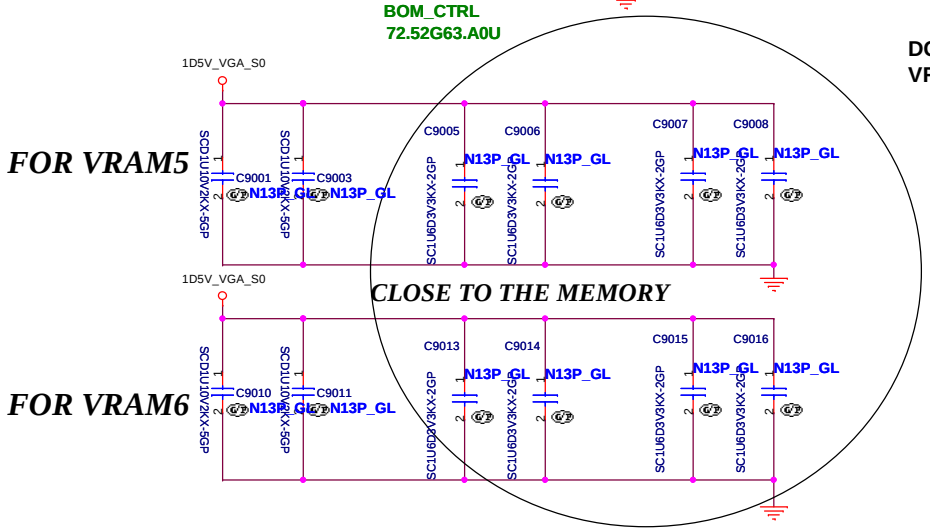


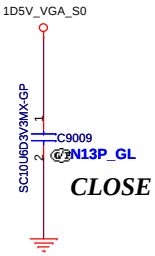


BOM_CTRL
72.52G63.A0U

BOM_CTRL
72.52G63.A0U

DG requires 4x0.1uF and 8x1.0uF per VRAM chip





CLOSE TO THE MEMORY

VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

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VIDEO FRAME BUFFER PORT C

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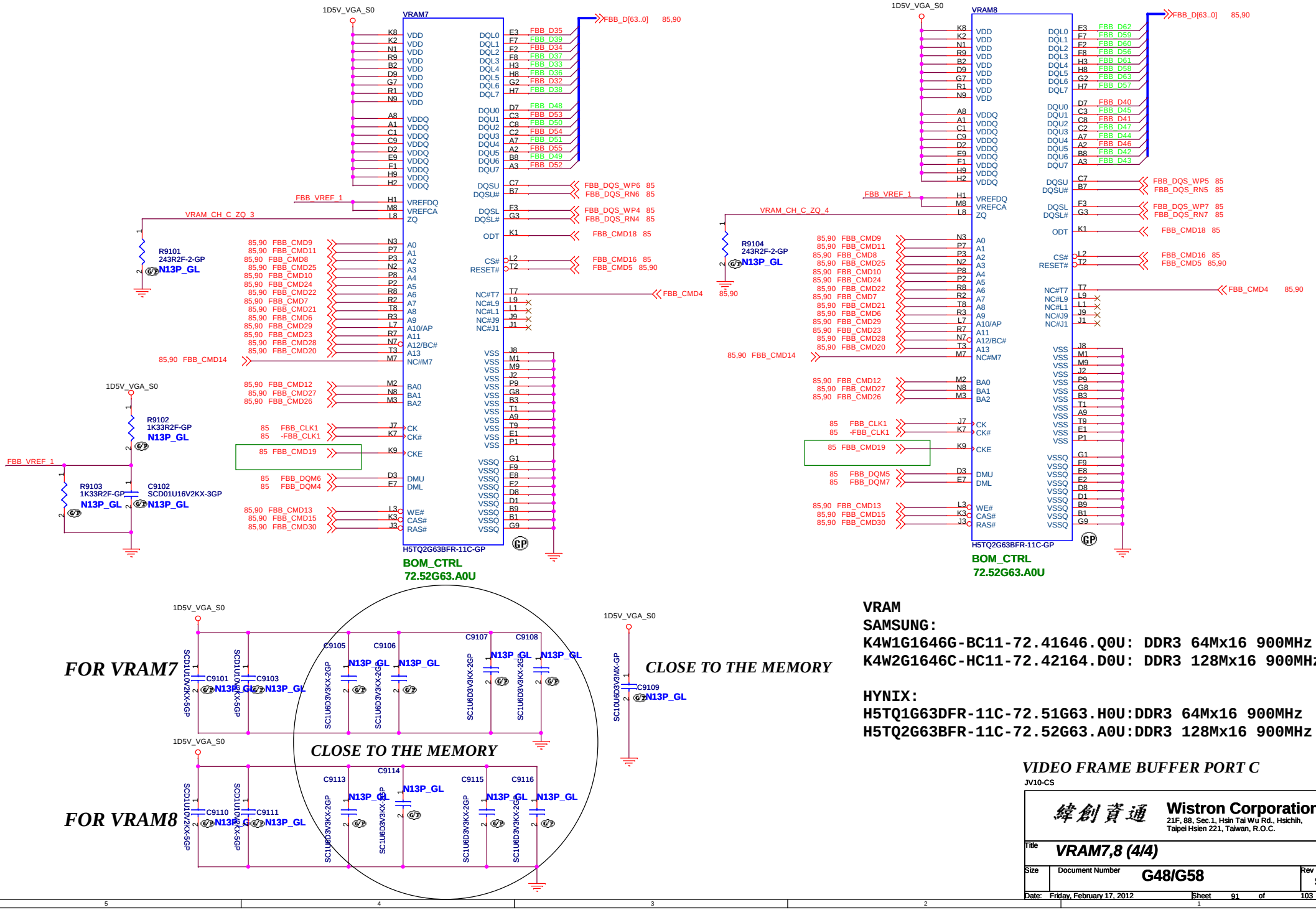
Title	VRAM5,6 (3/4)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 90 of 103	



VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT C

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Title	***VRAM7,8 (4/4)***	
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SSID = PWR.Plane.Regulator_VGACORE

NV_VID0-GPIO11
NV_VID1-GPIO5
NV_VID2-GPIO6
NV_VID3-GPIO1
NV_VID4-GPIO0
NV_VID5-GPIO13
NV_VID6-pull down to GND

VID[5..0]
101100 = 0.95 => N13P-GL
110010 = 0.875V => N13M-GE

Design current=

PU9202, PU9203 BOM CTRL

IMON
An analog output. IMON outputs a current proportional to the regulator output current.

Place near PL9201

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Title: ISL62882C_GPU_CORE		
Size	Document Number: G48/G58	Rev: SC
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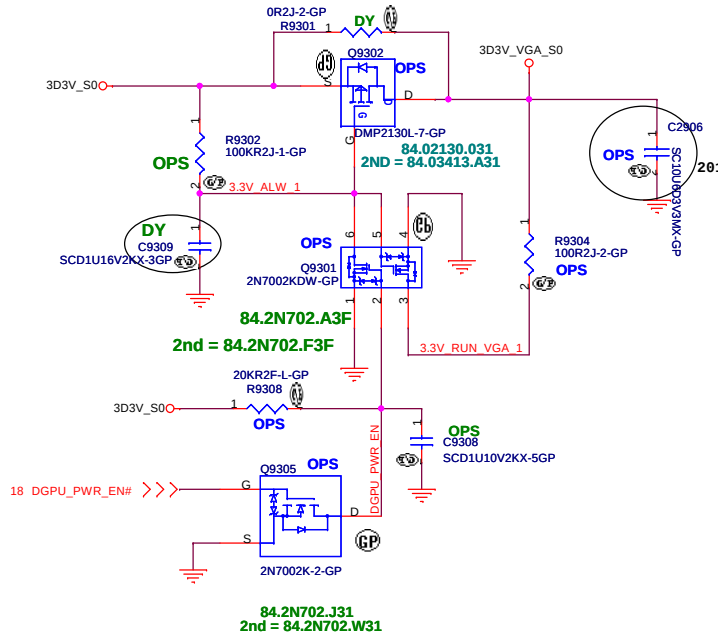
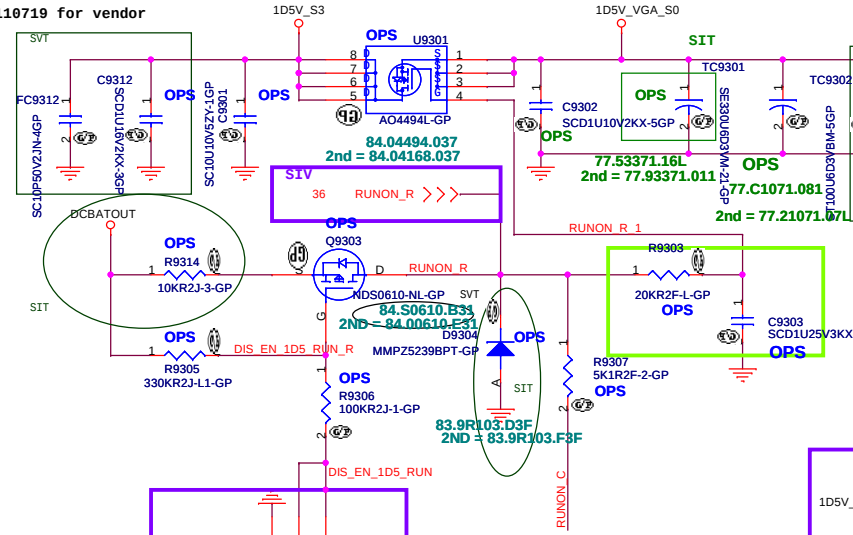
+3VS to 3.3V_DELAY Transfer



AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

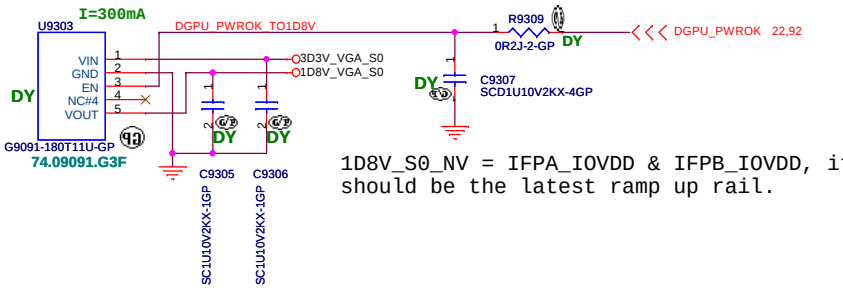
20110719 for vendor

1D5V_VGA_S0

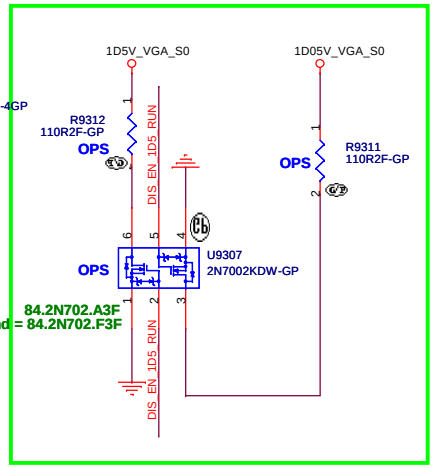


1.05V to 1.05V_VGA_S0 Transfer

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



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Title: DISCRETE VGA POWER		
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Title	*(Reserved)SW GFX LCD(1/2)*	
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Title: *(Reserved)SW GFX CRT(2/2)*

Size	Document Number	Rev
	G48/G58	SC

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Title: ***(Reserved)Touch panel CONN***

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CPU Plate

H3 HOLE276R178-GP — ZZ.00PAD.N11 — DY
H4 HOLE276R178-GP — ZZ.00PAD.N11 — DY
H5 HOLE276R178-GP — ZZ.00PAD.N11 — DY

VGA Std-Off

H2 STF237R128H42-GP — 34.4GD01.101 / 2nd = 34.4GD01.001 — OPS
H1 STF237R128H42-GP — 34.4GD01.101 / 2nd = 34.4GD01.001 — OPS

Check test point

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
19,27 PM_PWRBTN#	AFTP10
5,22,36 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12
5,18,27,31,36,65,83 PLT_RST#	AFTP13

Structure boss

SIT
H6 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H8 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H9 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H10 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H11 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H13 HOLE355X355R111-S1-GP — DY — ZZ.00PAD.571
H14 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581

Spring

H16 SPRING-24-GP-U
H17 SPRING-24-GP-U
H18 SPRING-24-GP-U
H19 SPRING-52-GP
H22 SPRING-12-GP-U1
SIT

Washer

H20 SPRING-53-GP-U — G48_PLED
H21 SPRING-53-GP-U — G58_PLED

SIV

EMI Cap.

DCBATOUT
EC9719 EC9718 EC9717 EC9716 EC9715 EC9714 EC9713 EC9712 EC9711 — SCD1U50V3KX-GP
DCBATOUT
EC9705 — SCD1U25V2KX-GP — DY

AD+
EC9709 EC9708 — SCD1U50V3KX-GP

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Title	UNUSED PARTS/EMI Capacitors	
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Title	***Change-History***	
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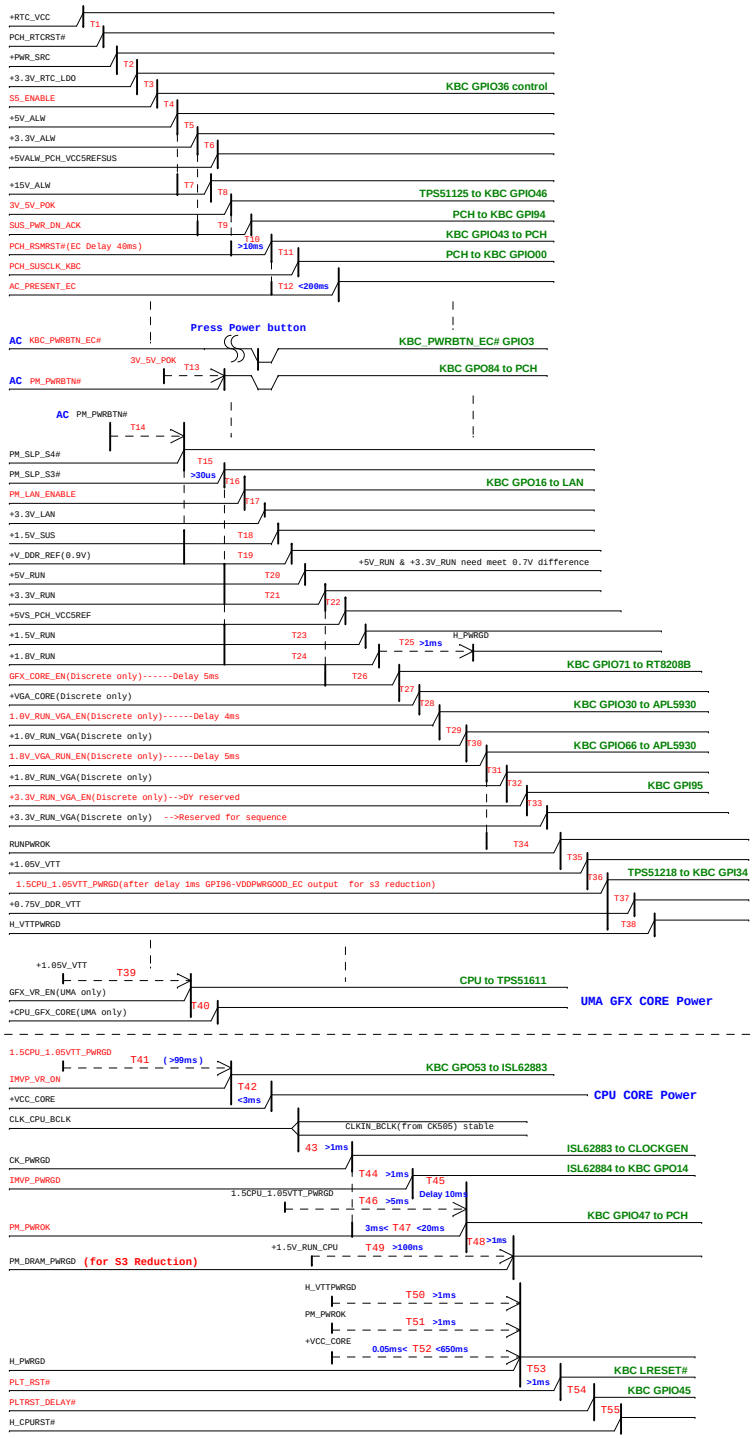
Intel-Power Up Sequence

Not Update

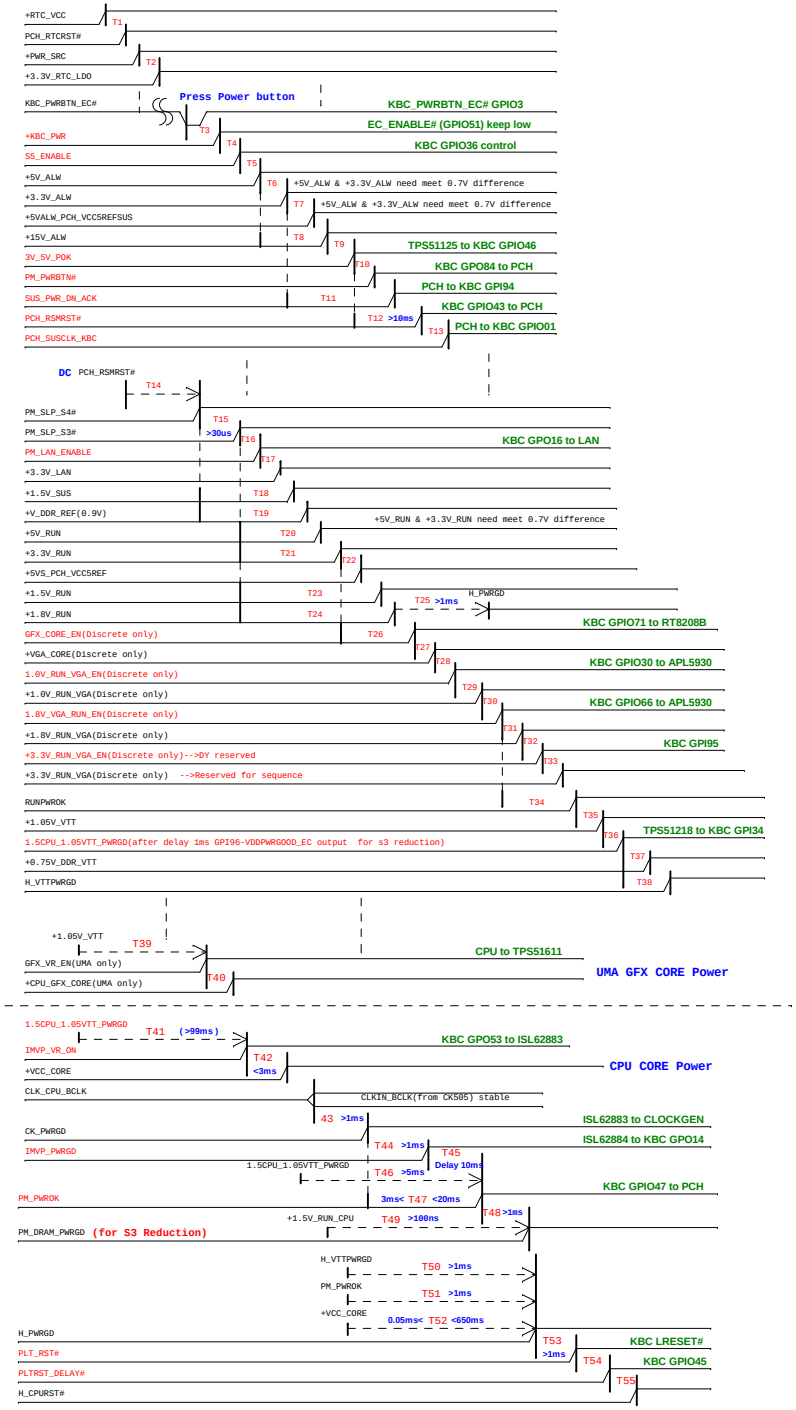
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



JVID:CS

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Title: Power Sequence

Size: | Document Number: G48/G58 | Rev: SC

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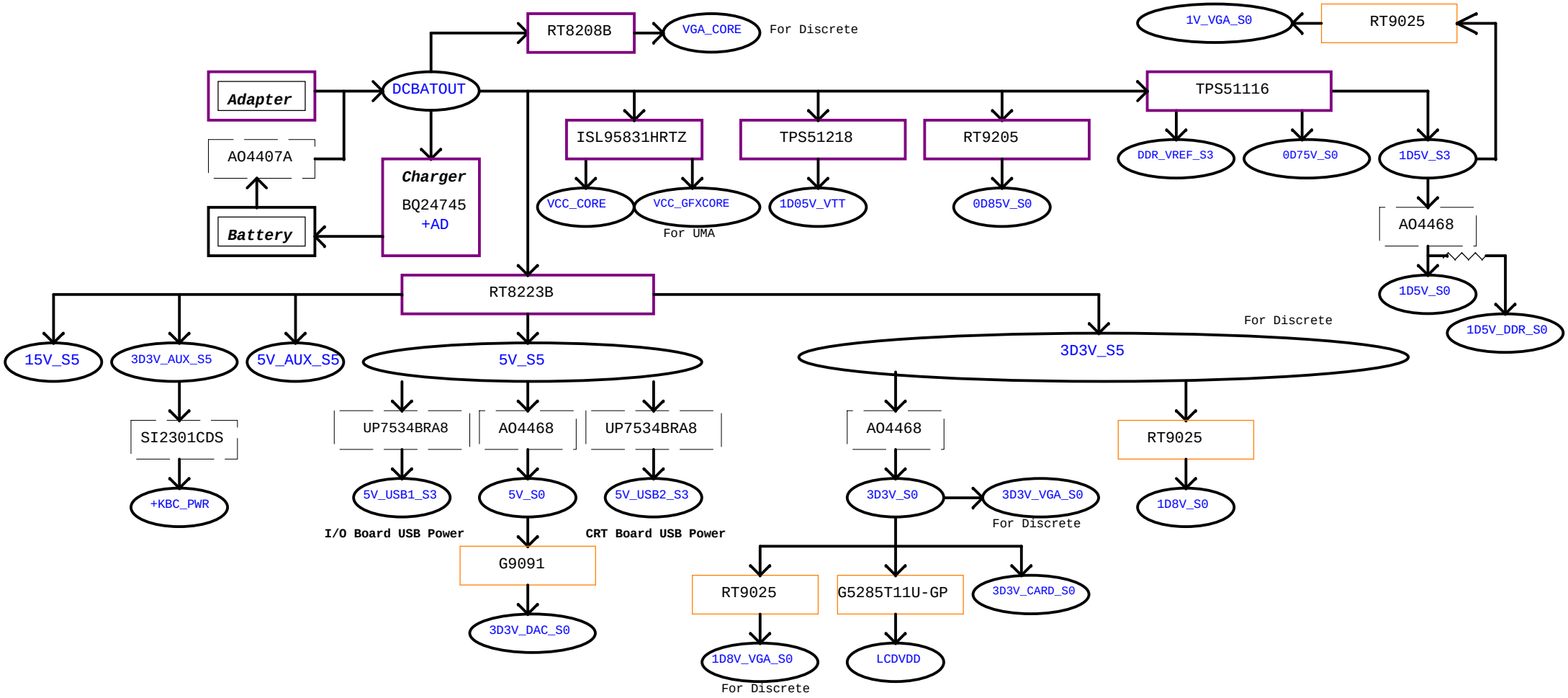
Not Update



Power Shape

Regulator	LDO	Switch

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Title	Power Block Diagram		
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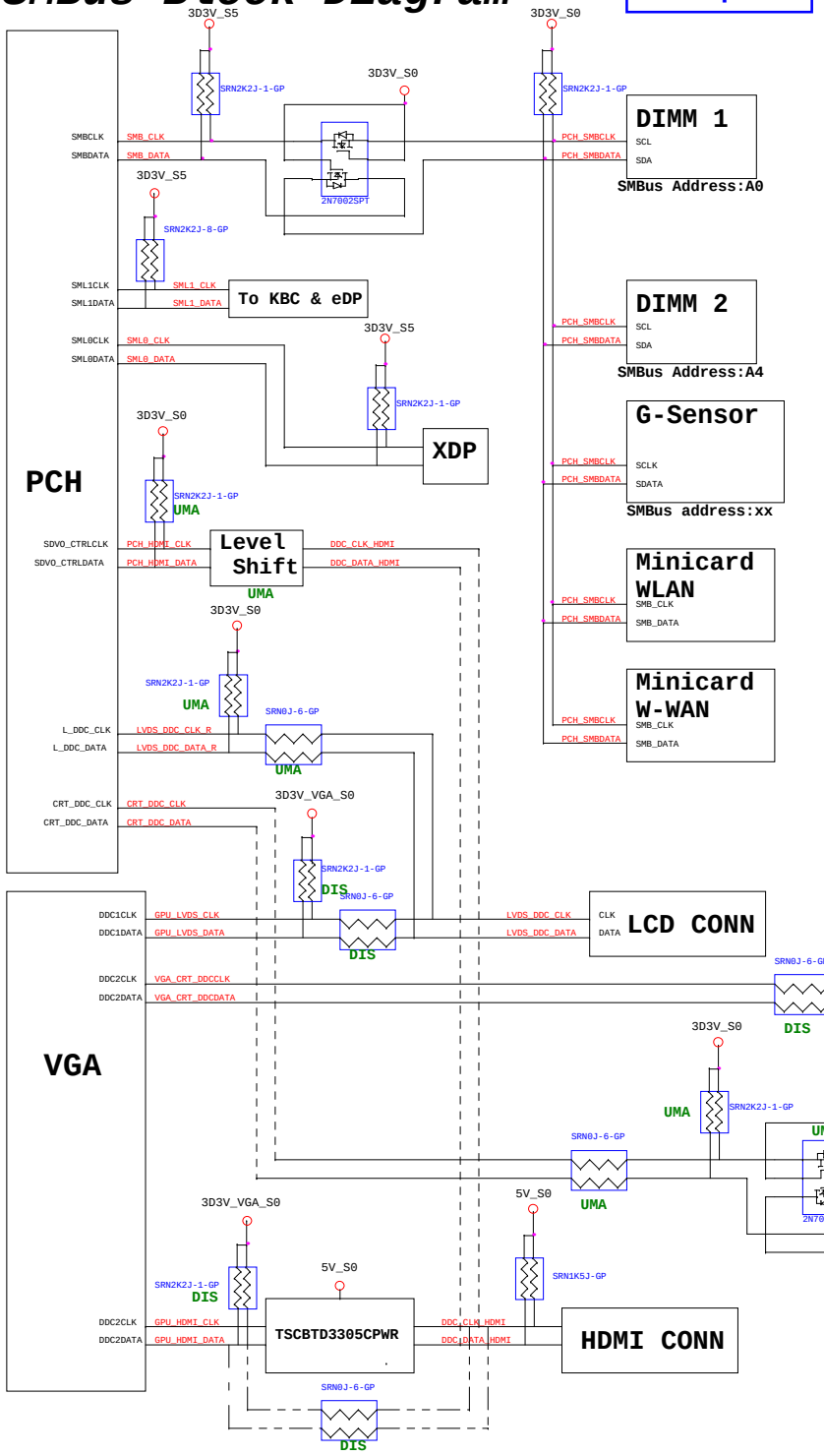
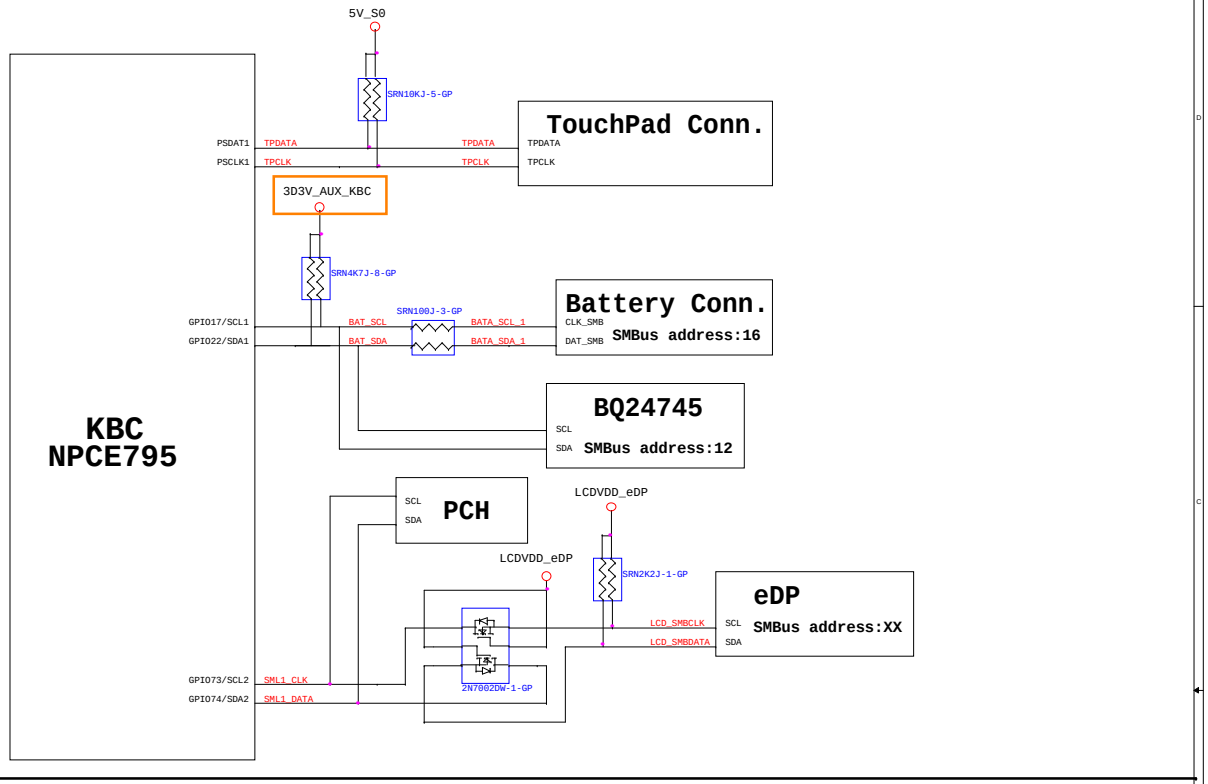
PCH SMBus Block Diagram

Not Update



KBC SMBus Block Diagram



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Title	SMBUS BLOCK DIAGRAM	
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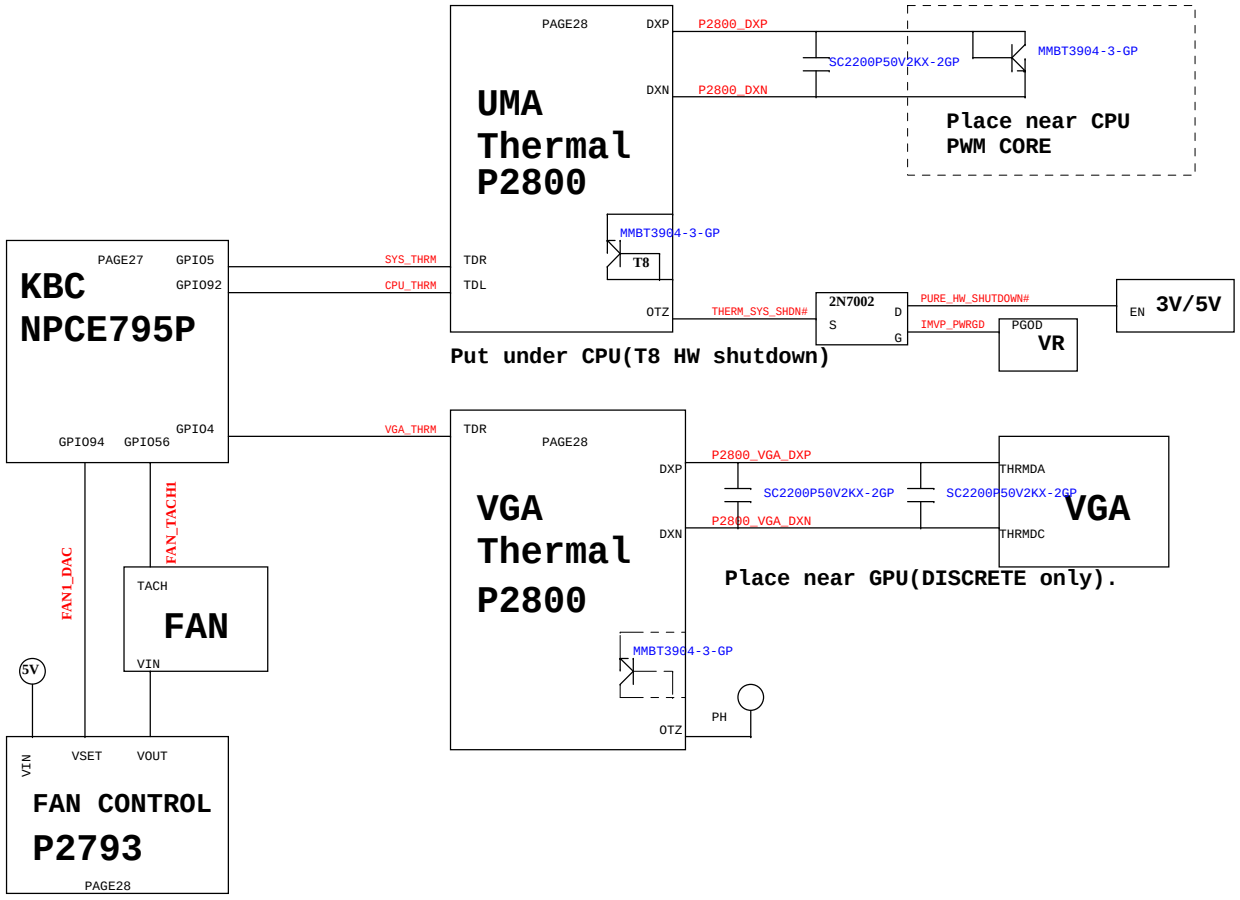
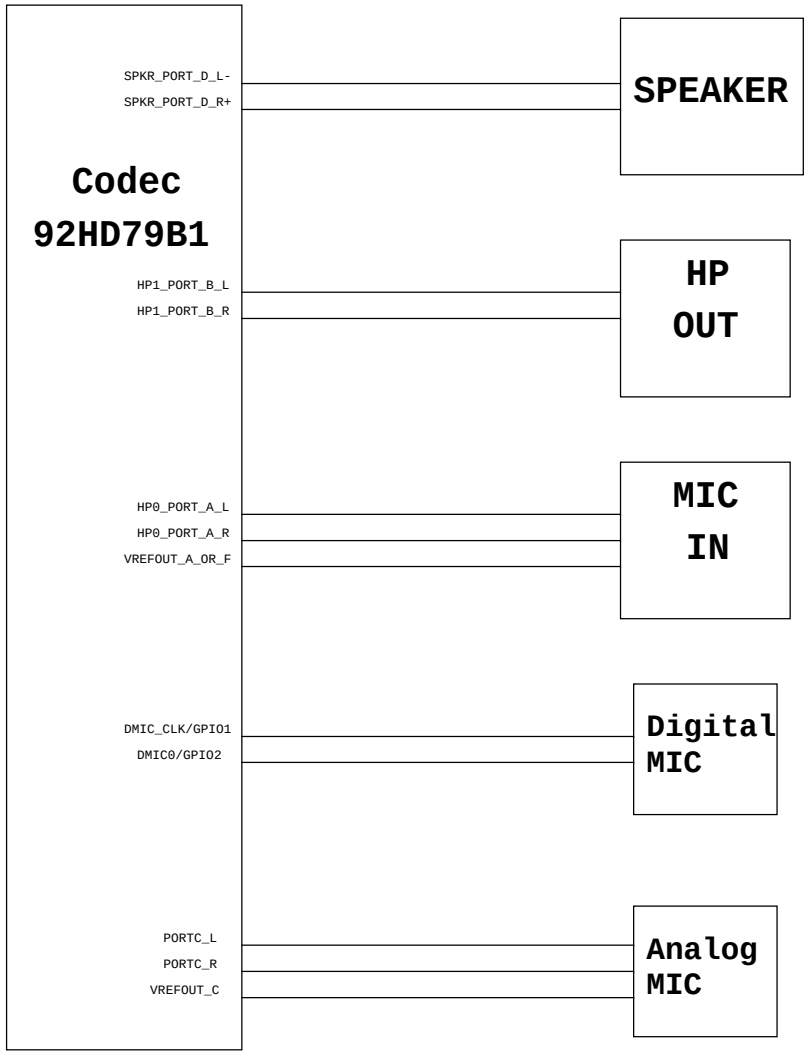
Thermal Block Diagram

Not Update



Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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Title ***Change History***

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