

Compal Confidential

G470/G570 DIS+UMA+Muxless M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Robson/PX3.0,PX4.0

2010-07-22

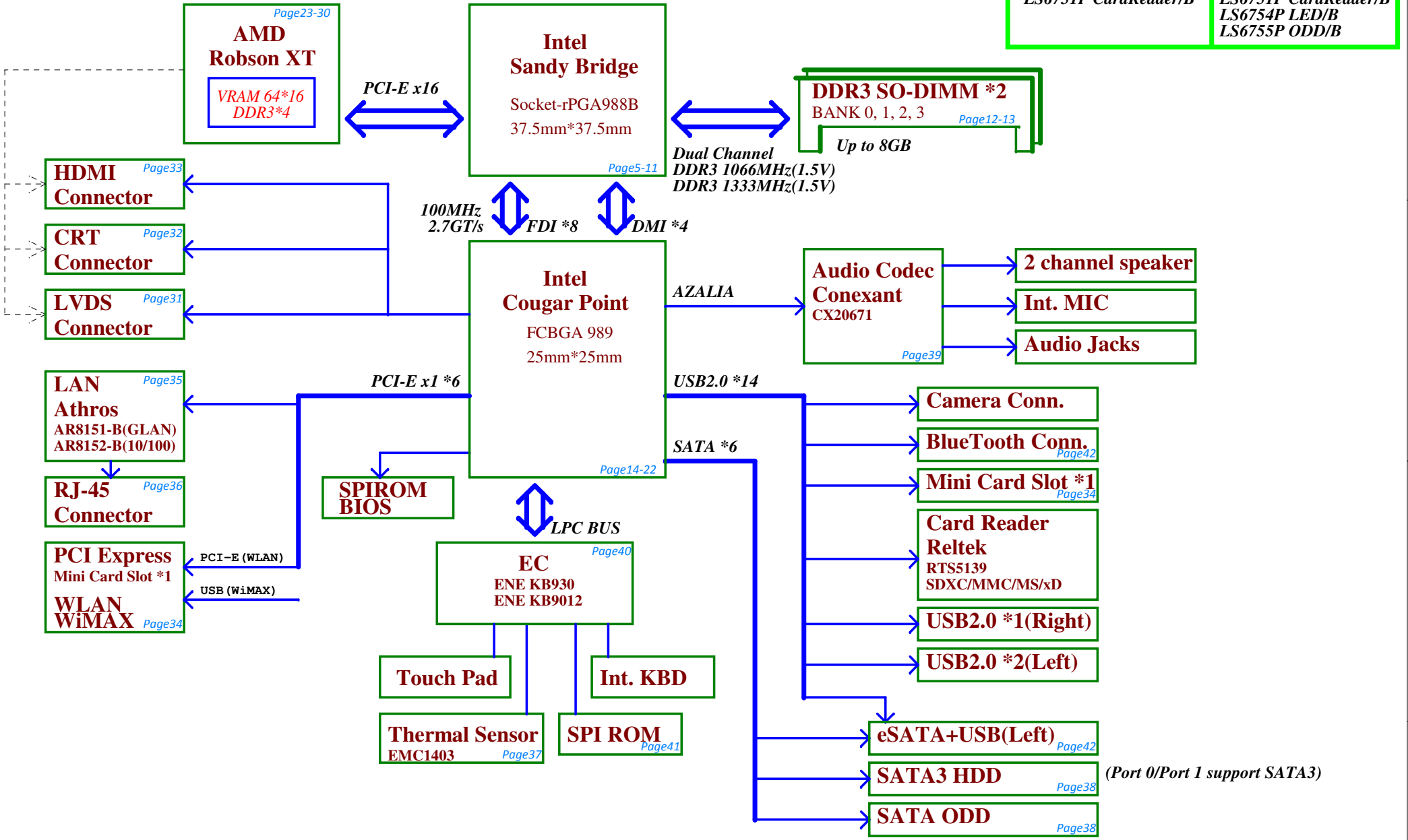
LA-6758P

REV: 0.1

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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	Cover Page		
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				Date:	Tuesday, August 17, 2010	Sheet	1 of 57

For 14"(Page 4x)
LS6753P PWR/B
LS6751P CardReader/B

For 15"(Page 4x+1)
LS6753P PWR/B
LS6751P CardReader/B
LS6754P LED/B
LS6755P ODD/B



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				Date:	Tuesday, August 17, 2010
				Sheet	2 of 57
				Rev	0.1

Voltage Rails

power plane	+B	+5VALW	+1.5V	+3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	EVT
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	Thermal Sensor EMC1403-2	1001_101xb
		Thermal Sensor EMC1402-1	100_1100 b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
		6	
7			
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
UMA only	PX@
Muxless	PX@+VGA@
Discrete Only	DIS@+VGA@
PX3.0 only, not for BACO	PX3@
BACO	BACO@
COMMON HDMI	HDMI@
UMA HDMI	UMA_HDMI@
Discrete HDMI	VGA_HDMI@
eSATA	ESATA@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Camera	CMOS@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB930	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB930	✗	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

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				LA-6758P	0.1
				Date	Tuesday, August 17, 2010
				Sheet	3 of 57

Power-Up/Down Sequence

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDR3 should ramp-up before or simultaneously with VDDC.
- For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
- The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VGS)

PCIE_VDDC(1.0V)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

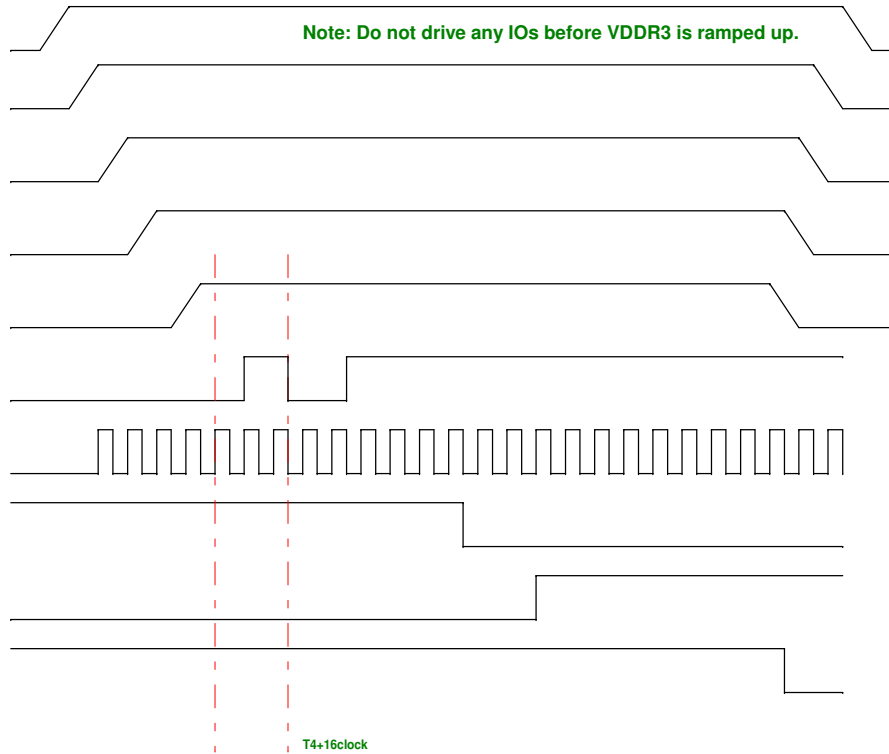
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset



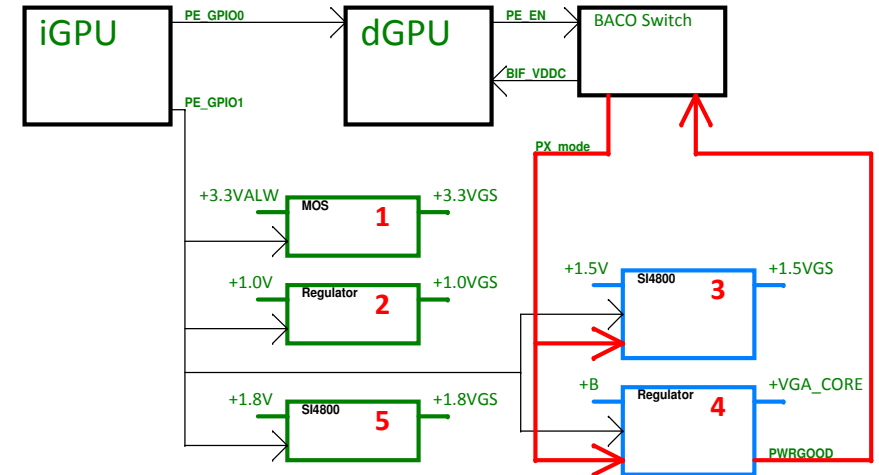
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

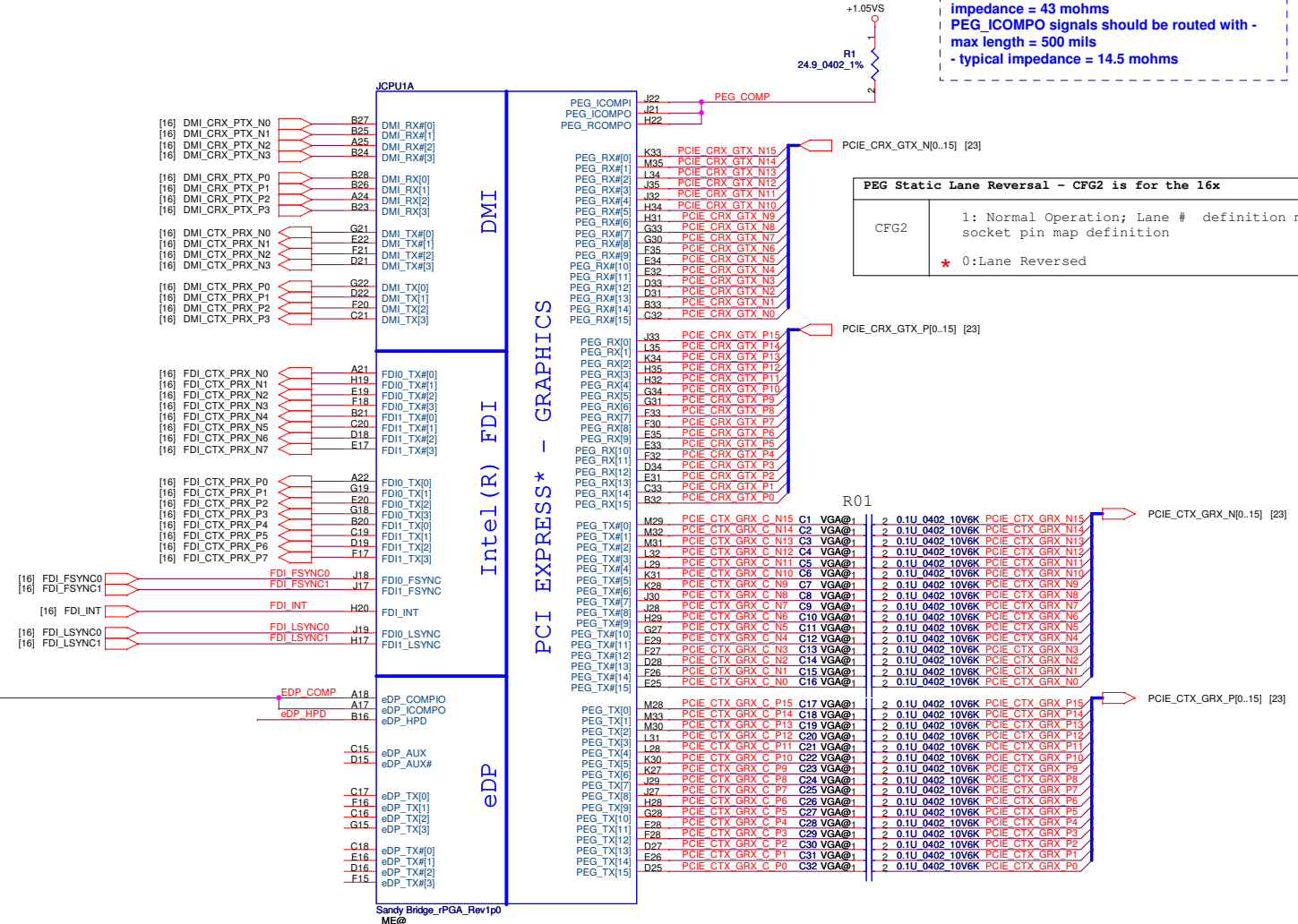
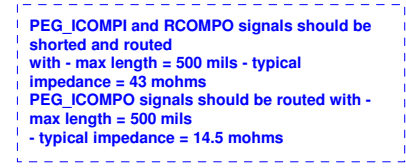
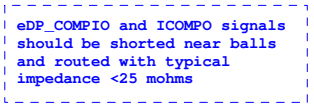
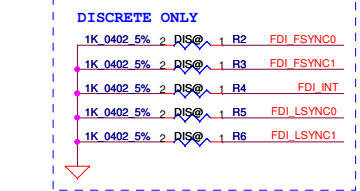
BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



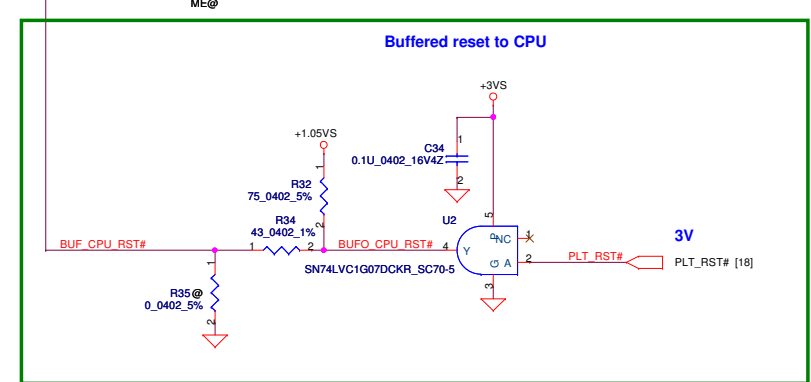
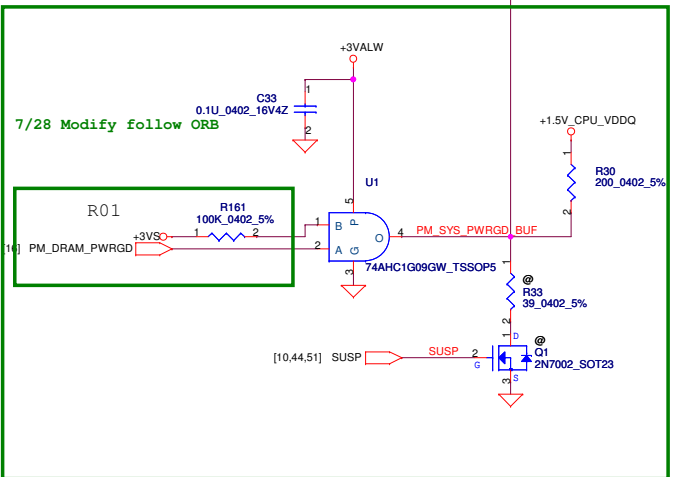
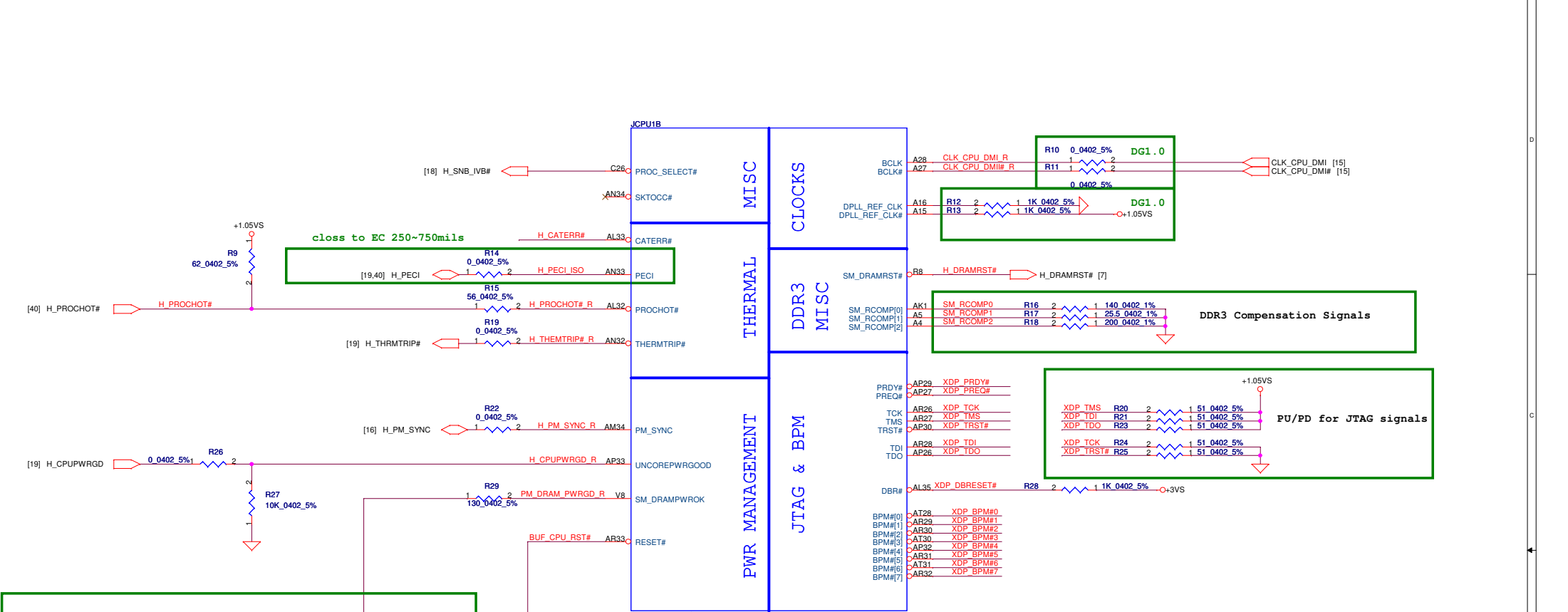
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Date:	Tuesday, August 17, 2010	Sheet	4 of 57	Rev	0.1



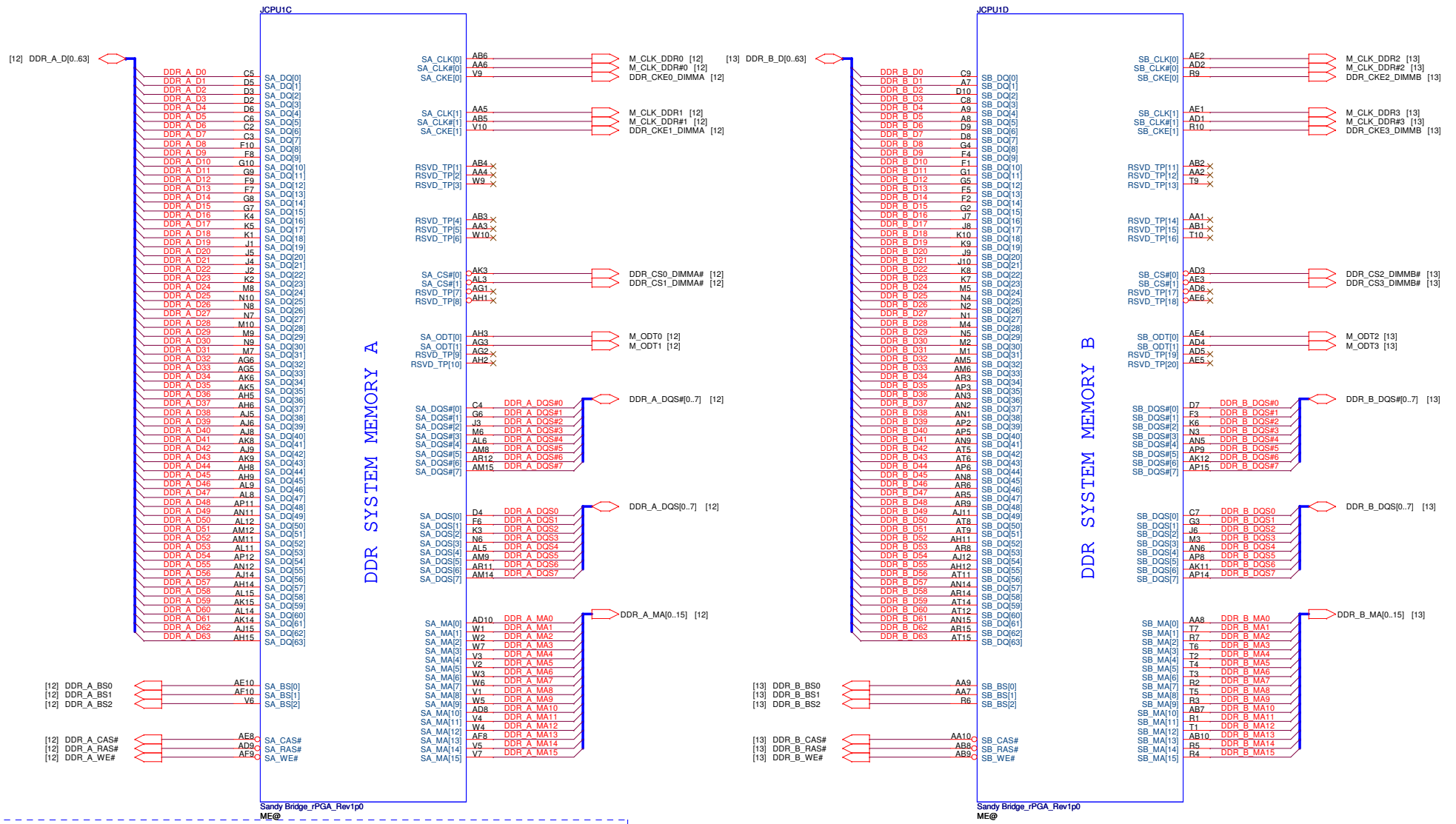
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
*	0: Lane Reversed

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Customer	LA-6758P	Rev	0.1	Date: Tuesday, August 17, 2010
Sheet		5	of 57	



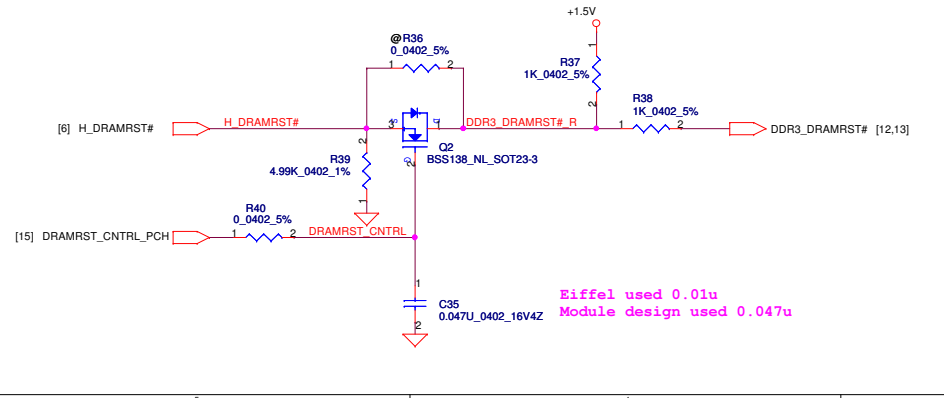
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Date: Tuesday, August 17, 2010				Rev 0.1
Sheet 6 of 57				



DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

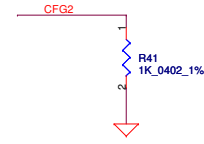
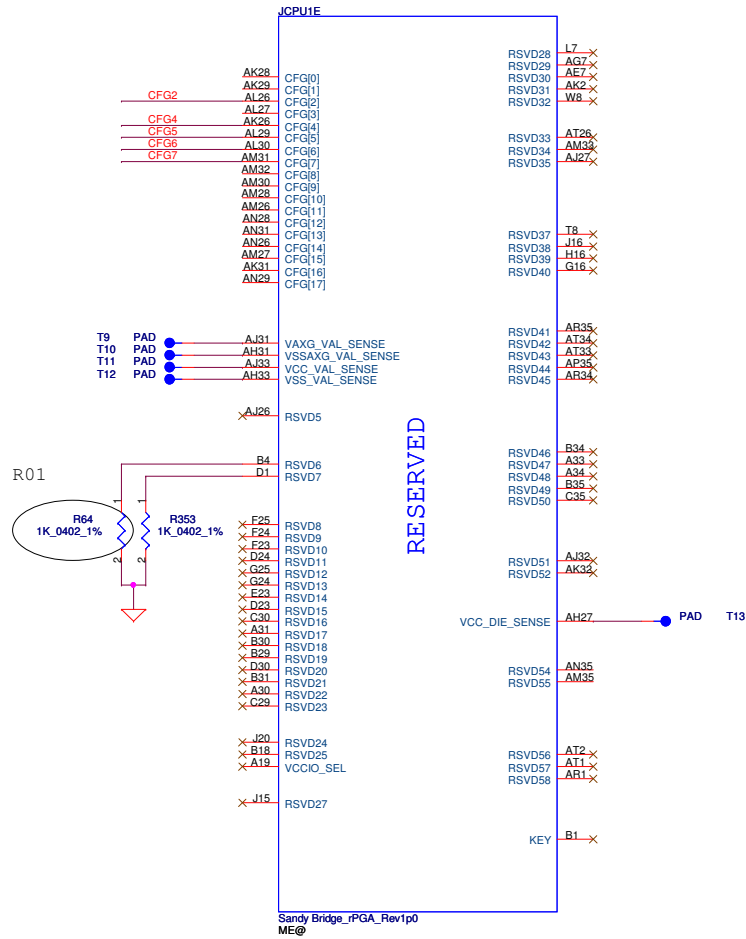
Sandy Bridge_rPGA_Rev1p0 ME@



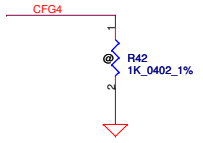
Eiffel used 0.01u
Module design used 0.047u

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				Rev 0.1 Sheet 7 of 57

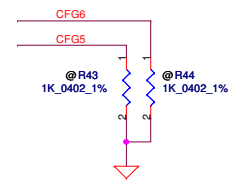
CFG Straps for Processor



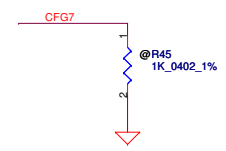
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



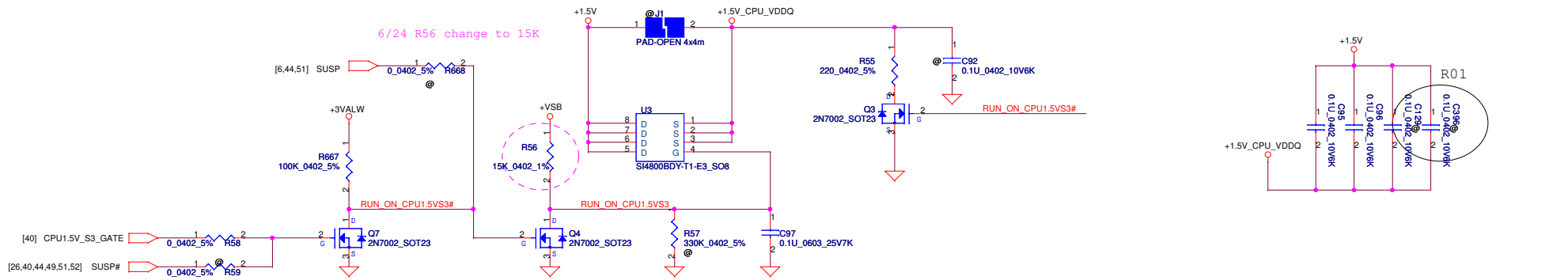
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



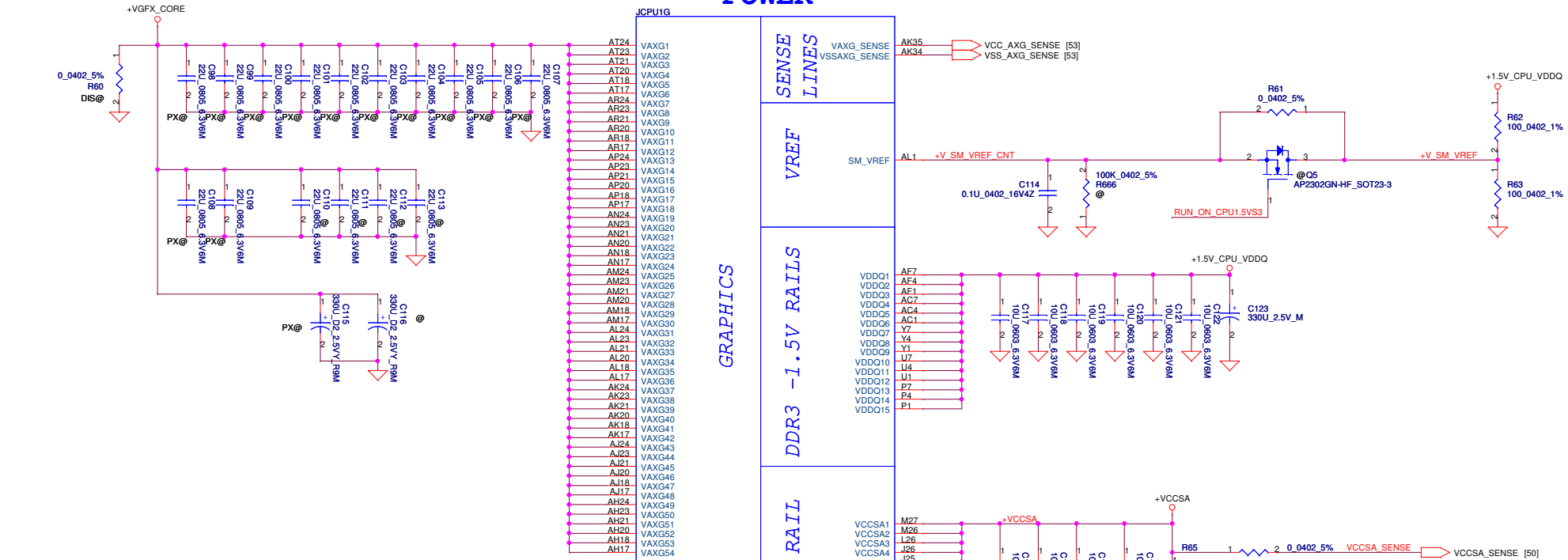
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

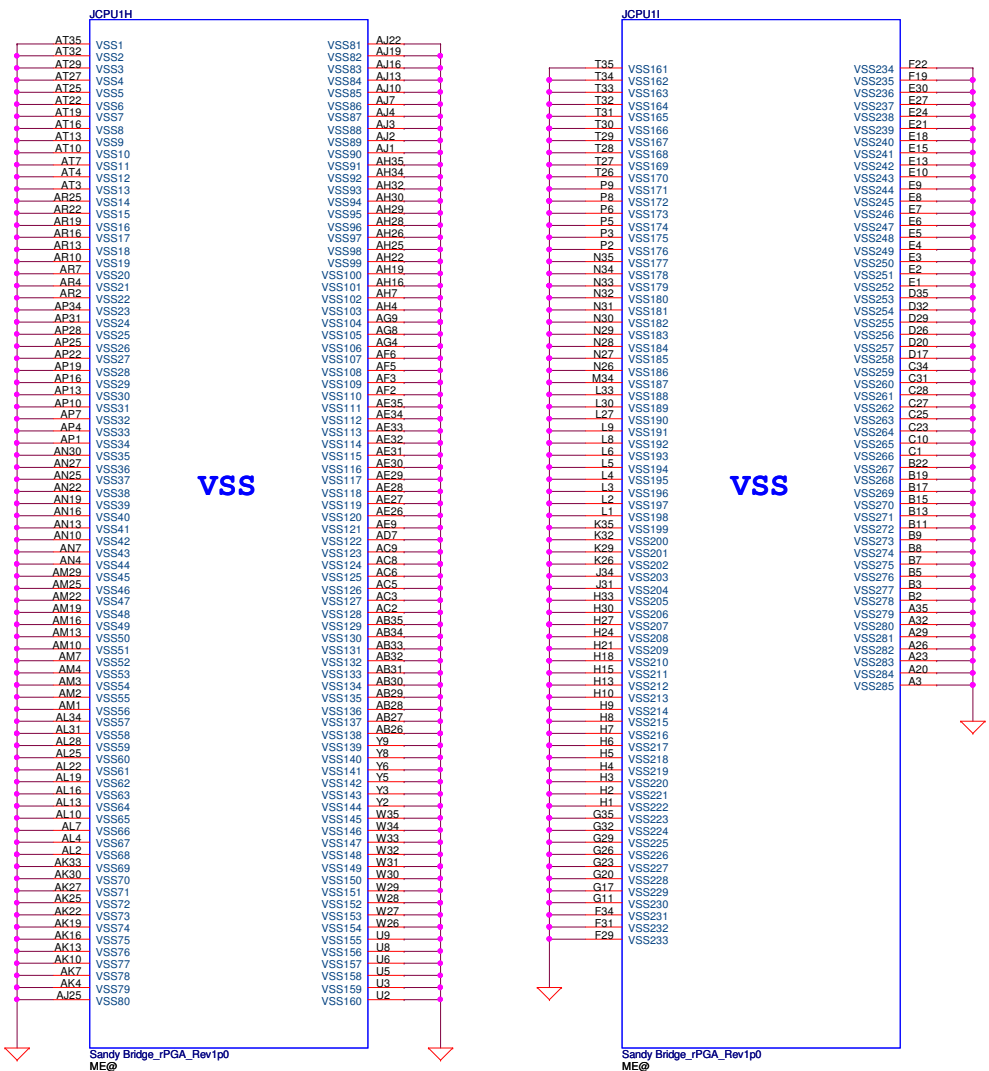


POWER

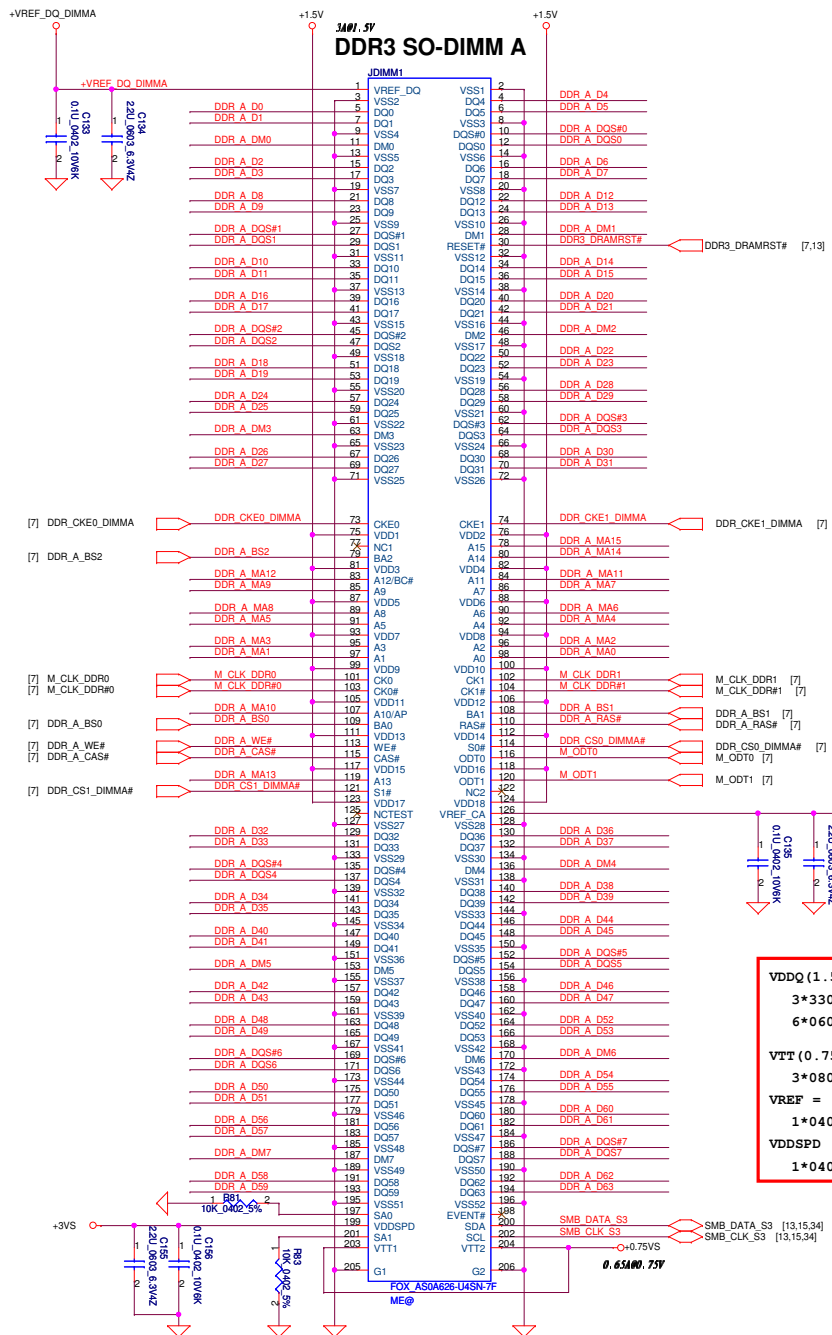


6/9 change 330U to 22U X2

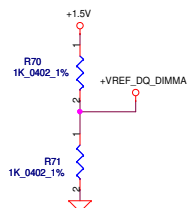
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				LA-6758P	0.1
				Date: Tuesday, August 17, 2010	Sheet 11 of 57

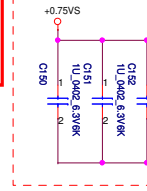


- [7] DDR_A_D[0..63]
- [7] DDR_A_DQS[0..7]
- [7] DDR_A_DQS#0..7]
- [7] DDR_A_MA[0..15]

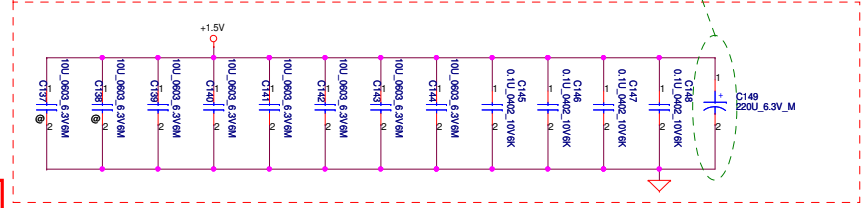


Layout Note:
Place near DIMM

Layout Note:
Place near DIMM



*OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)*
*(10uF_0603_6.3V)*8*
*(0.1uF_402_10V)*4*



VDDQ (1.5V) =
 $3*330\mu\text{f} / 12\text{m ohm (TOTAL FOR 2 SO-DIMMs)}$
 $6*0603\ 10\mu\text{f (PER CONNECTOR)}$

VTT (0.75V) =
 $3*0805\ 10\mu\text{f} + 4*0402\ 1\mu\text{f}$

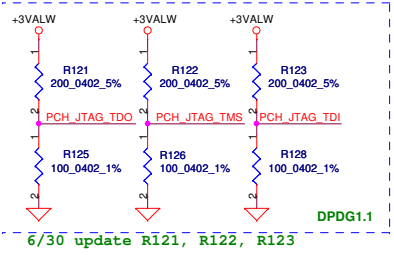
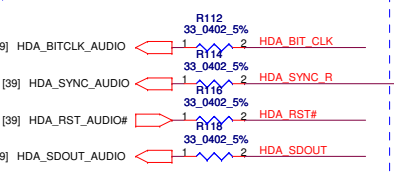
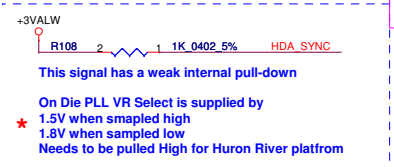
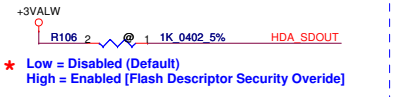
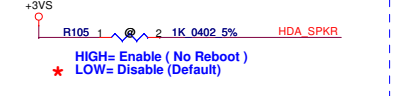
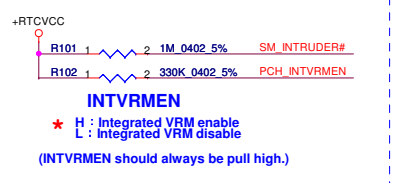
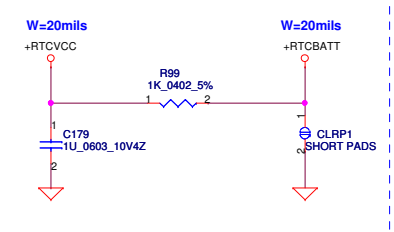
VREF =
 $1*0402\ 0.1\mu\text{f} + 1*0402\ 2.2\mu\text{f}$

VDS SPD (3.3V) =
 $1*0402\ 0.1\mu\text{f} + 1*0402\ 2.2\mu\text{f}$

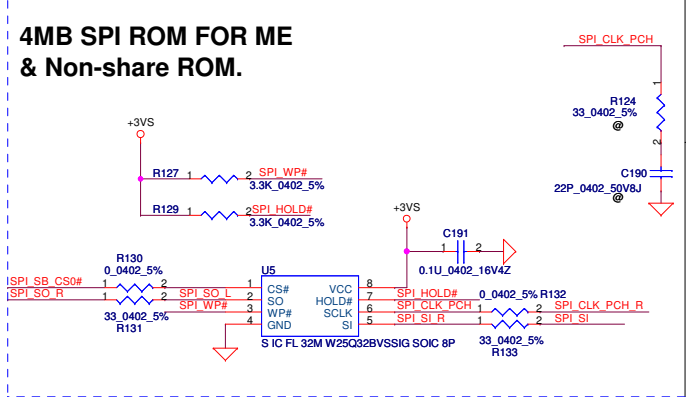
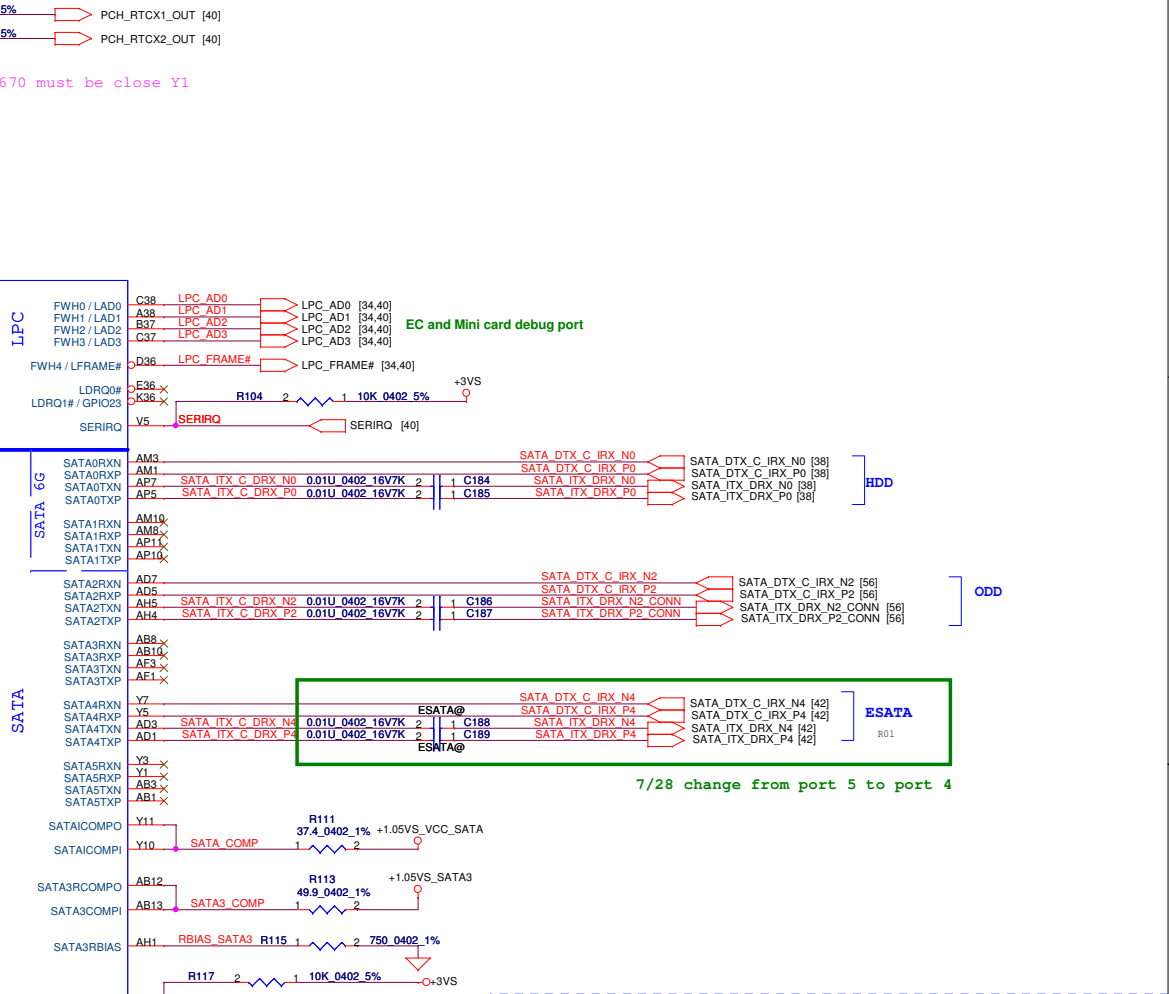
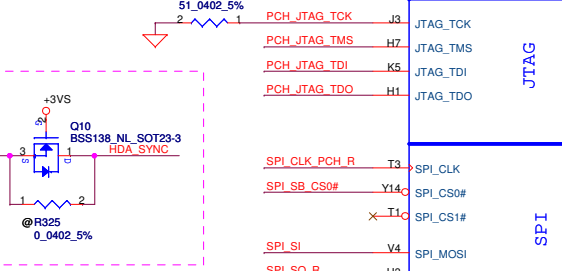
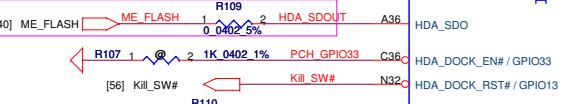
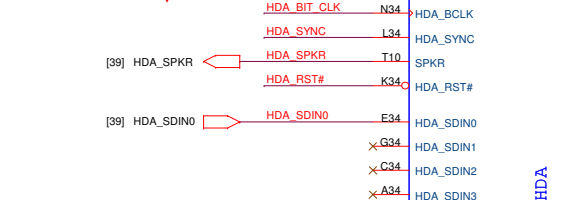
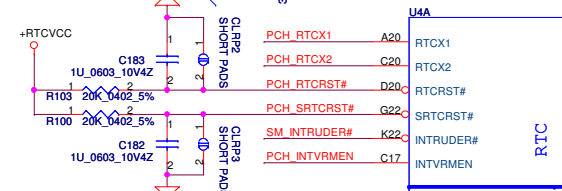
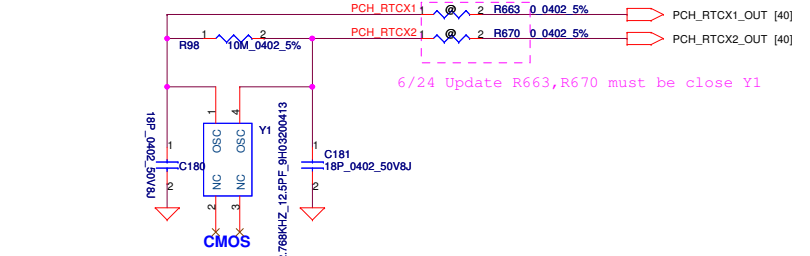
7/28 Update connect GND directly

Layout Note:
Place near DIMM

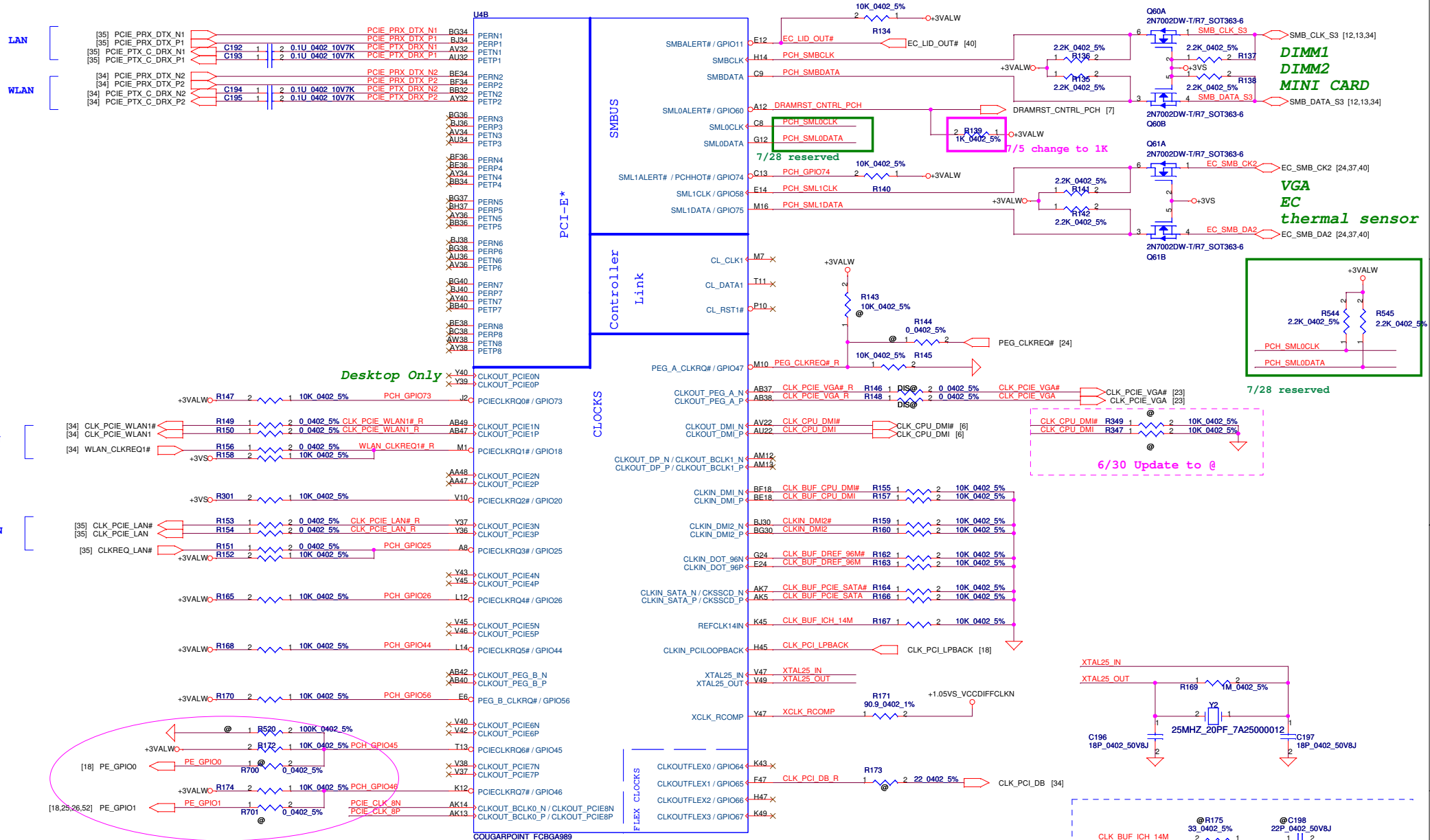
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	DDR3-SODIMM SLOT1	
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				LA-6758P	
Date:	Tuesday, August 17, 2010	ISheet	12	of	57



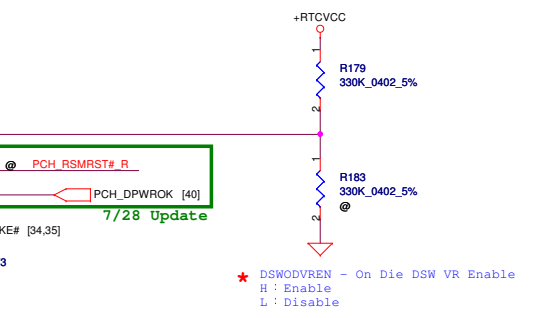
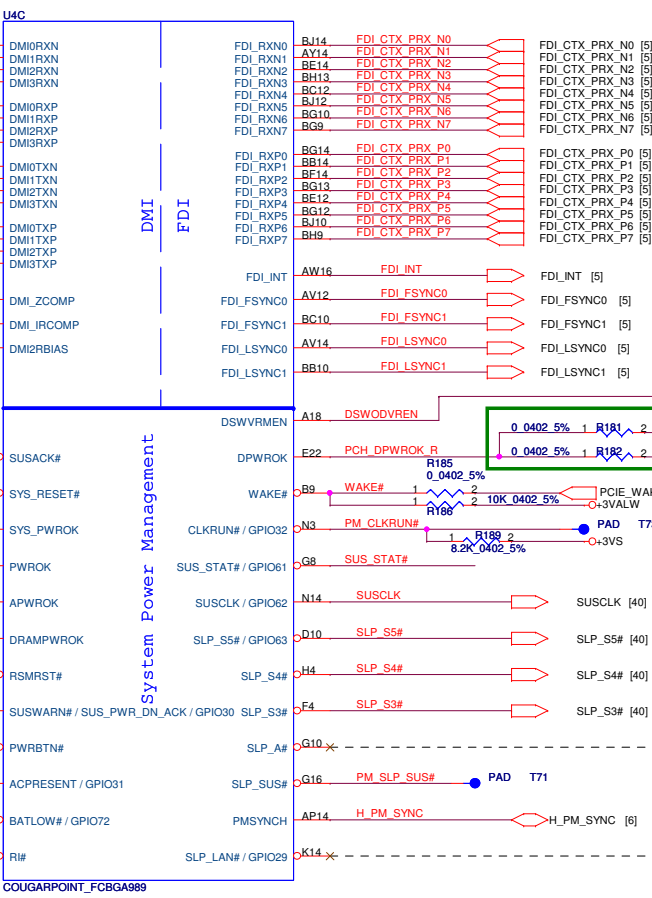
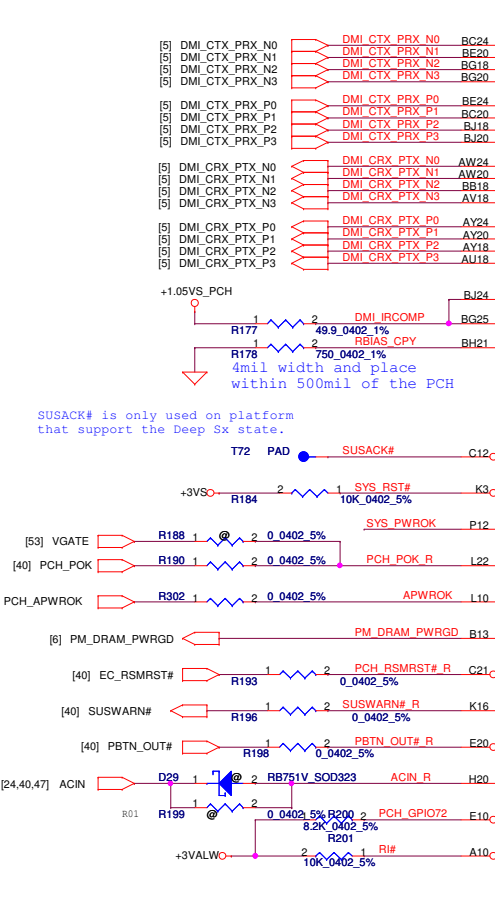
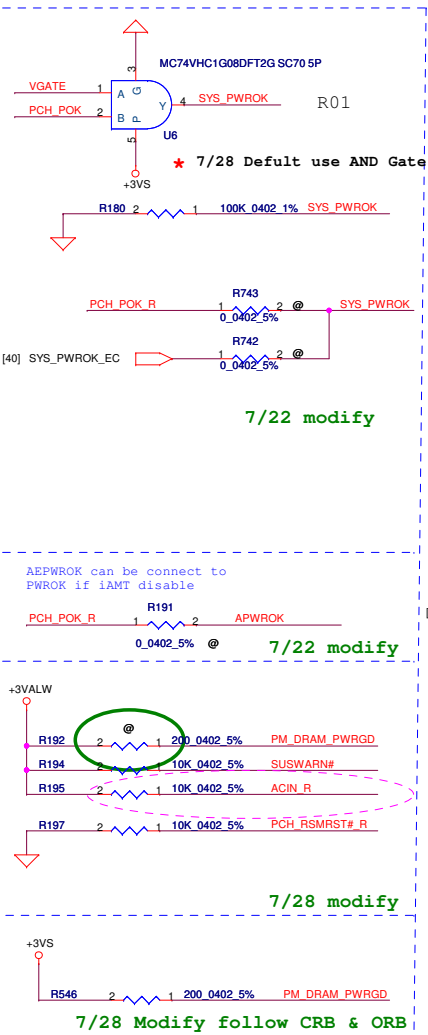
6/30 update R121, R122, R123

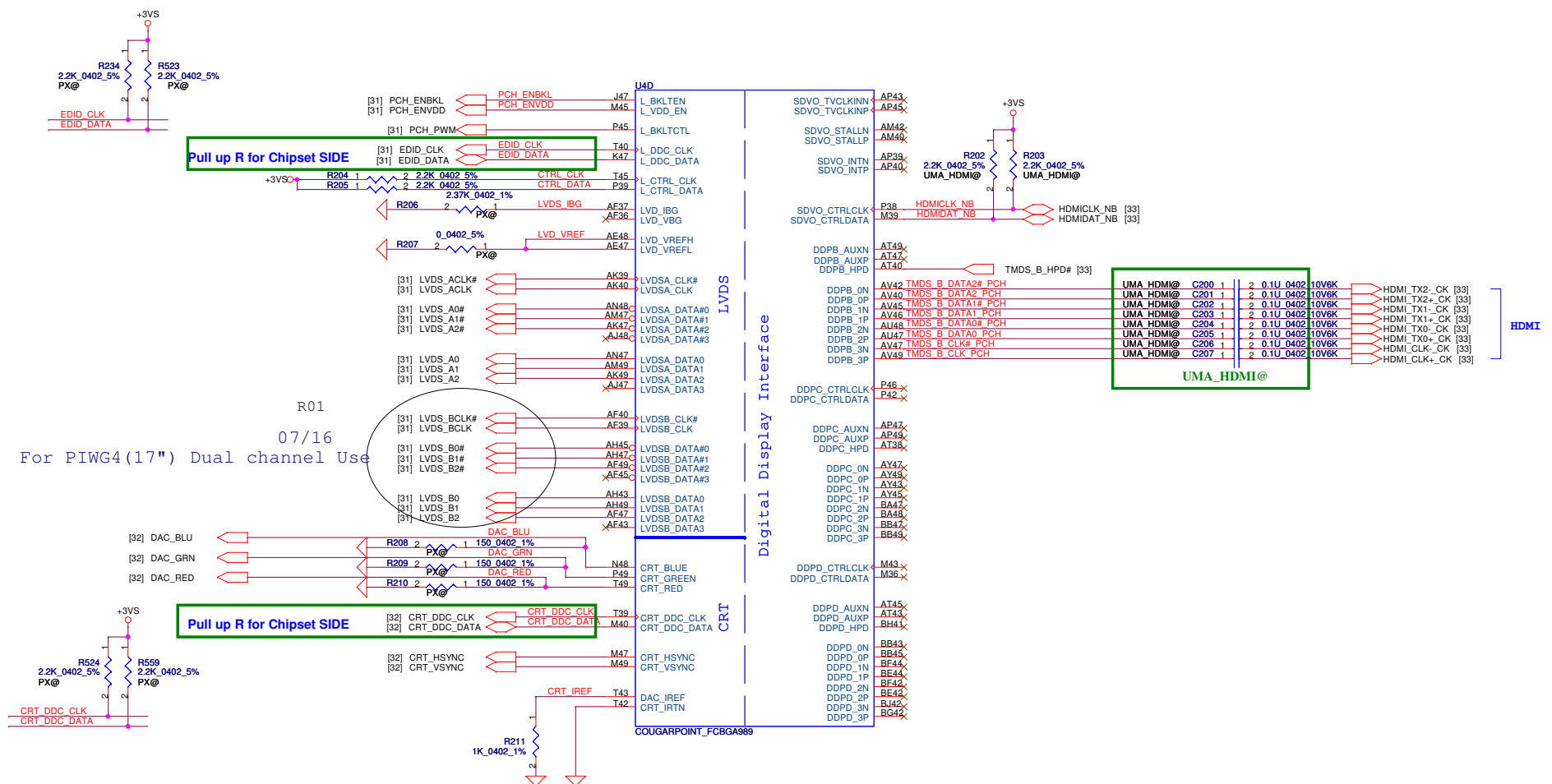


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Revision	1	Document Number	LA-6758P	Page	0.1
Date	Tuesday, August 17, 2010	Sheet	14	of	57

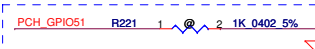
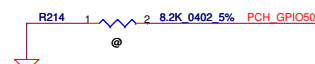
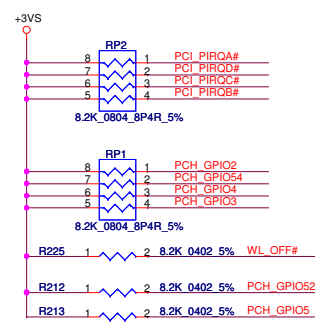


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Compal Electronics, Inc. PCH (2/8) PCIE, SMBUS, CLK				
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Date:	Tuesday, August 17, 2010	Sheet	15	of 57





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				Rev 0.1



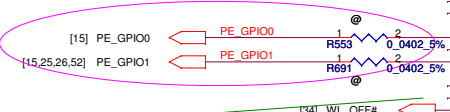
PCH_GPIO51 R221 1 2 1K 0402 5%

Boot BIOS Strap bit1 BBS1		
Bit11	Bit10	Destination
0	1	Reserved
1	0	Reserved
1	1	* SPI (Default)
0	0	LPC

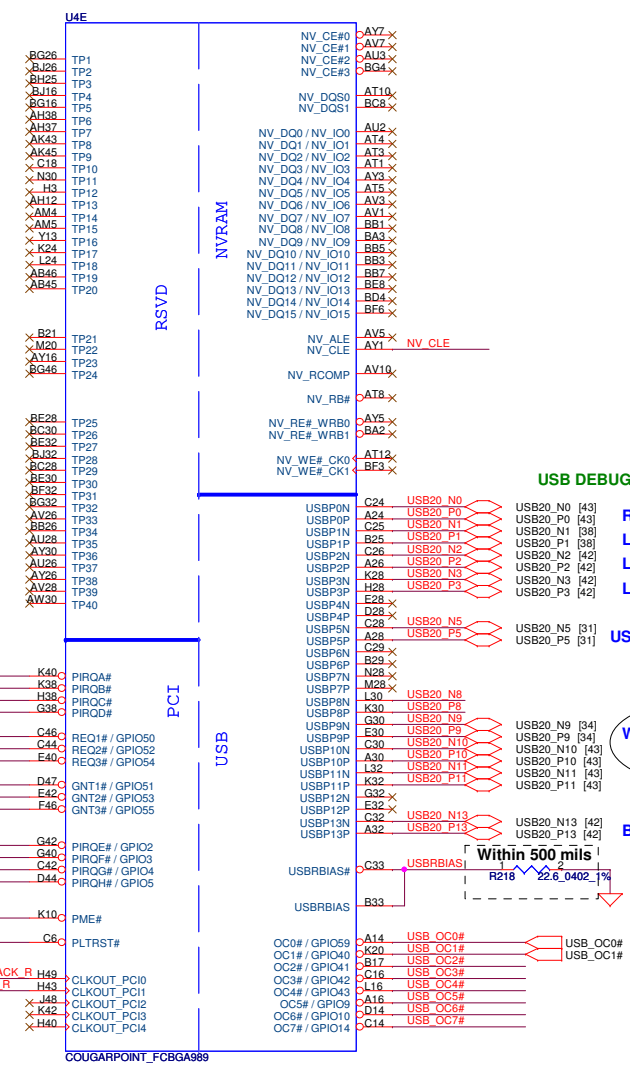
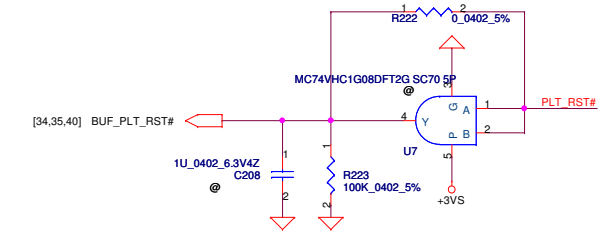
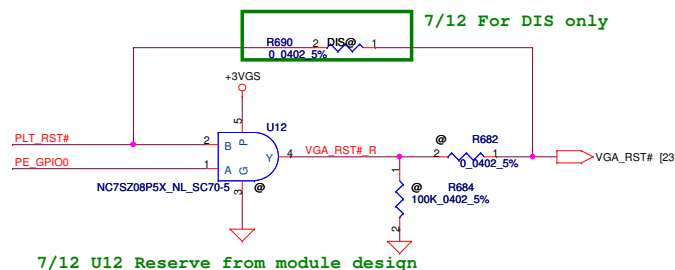
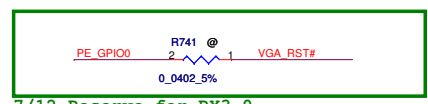
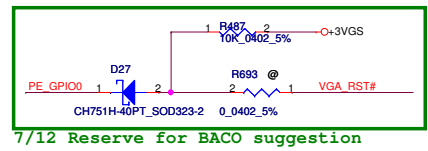
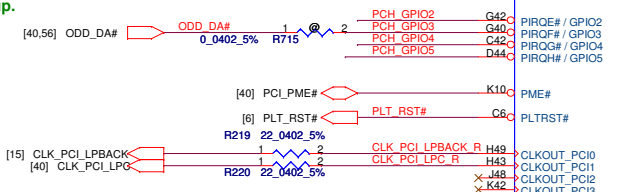
WL_OFF# R215 1 2 1K 0402 5%

A16 swap override Strap/Top-Block Swap Override jumper	
Low=A16 swap override/Top-Block Swap Override enabled	High=Default *
PCI_GNT13#	

6/23 Reserve for GPU?



GPIO53=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



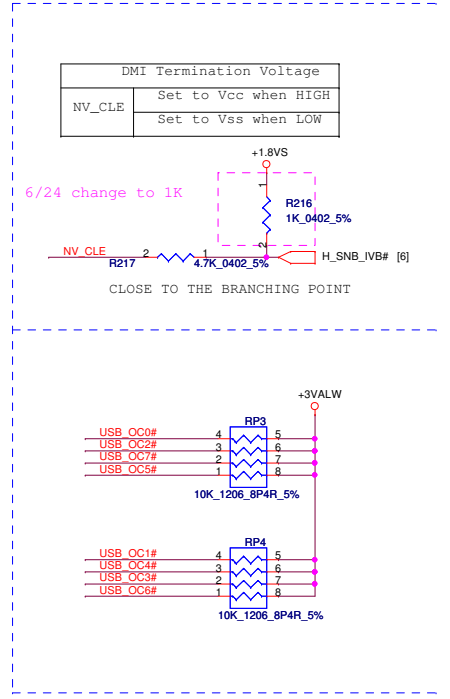
USB DEBUG=PORT1 AND PORT9

RIGHT USB
LEFT USB
LEFT USB (COMBO)
USB charger

USB Camera

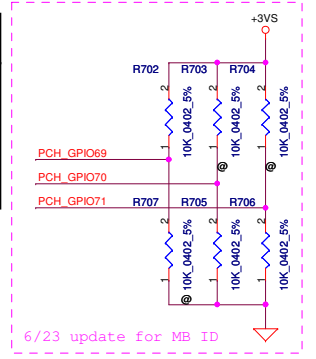
WLAN R01
CARD READER

Bluetooth



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PCH (5/9) PCI, USB				Rev 0.1
Date: Tuesday, August 17, 2010				Sheet 18 of 57

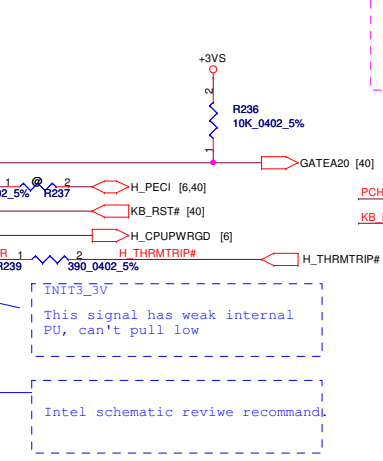
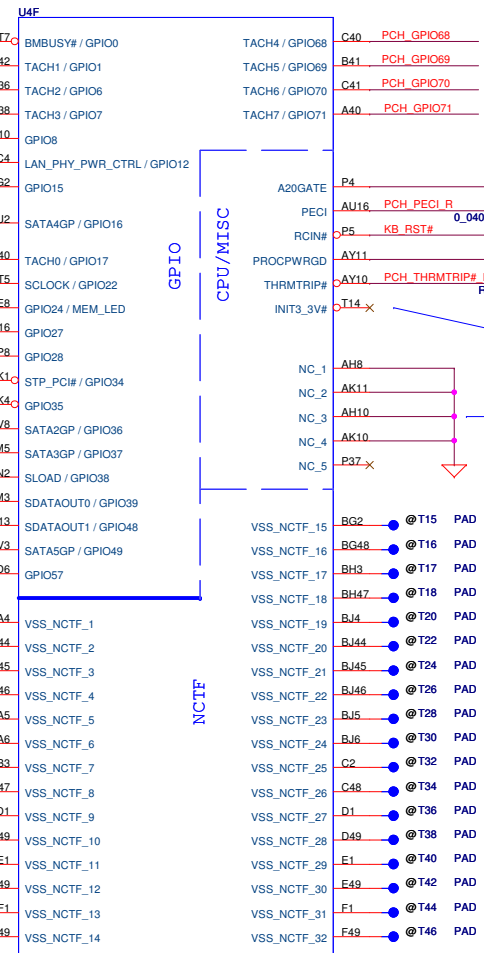
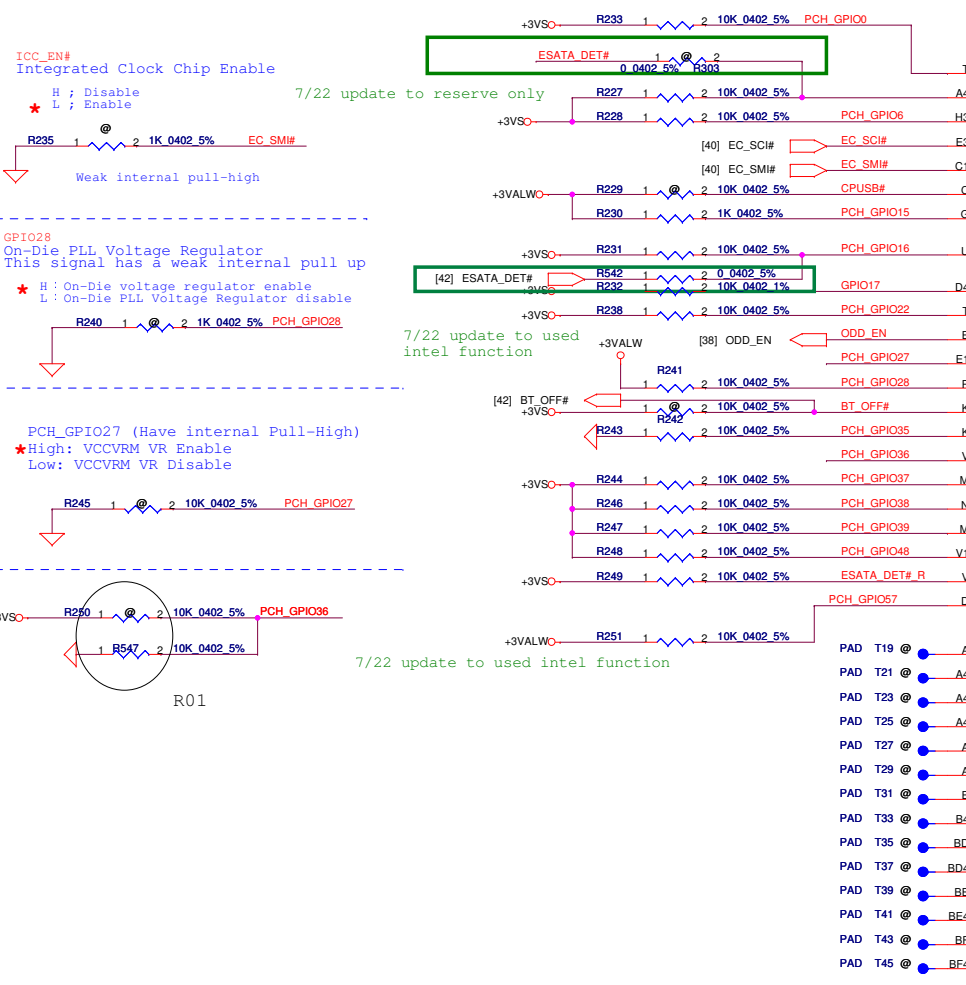
PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	0	0	DIS *
0	1	0	PX3.0
1	1	0	PX4.0



ICCNEN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
★ ; Enable

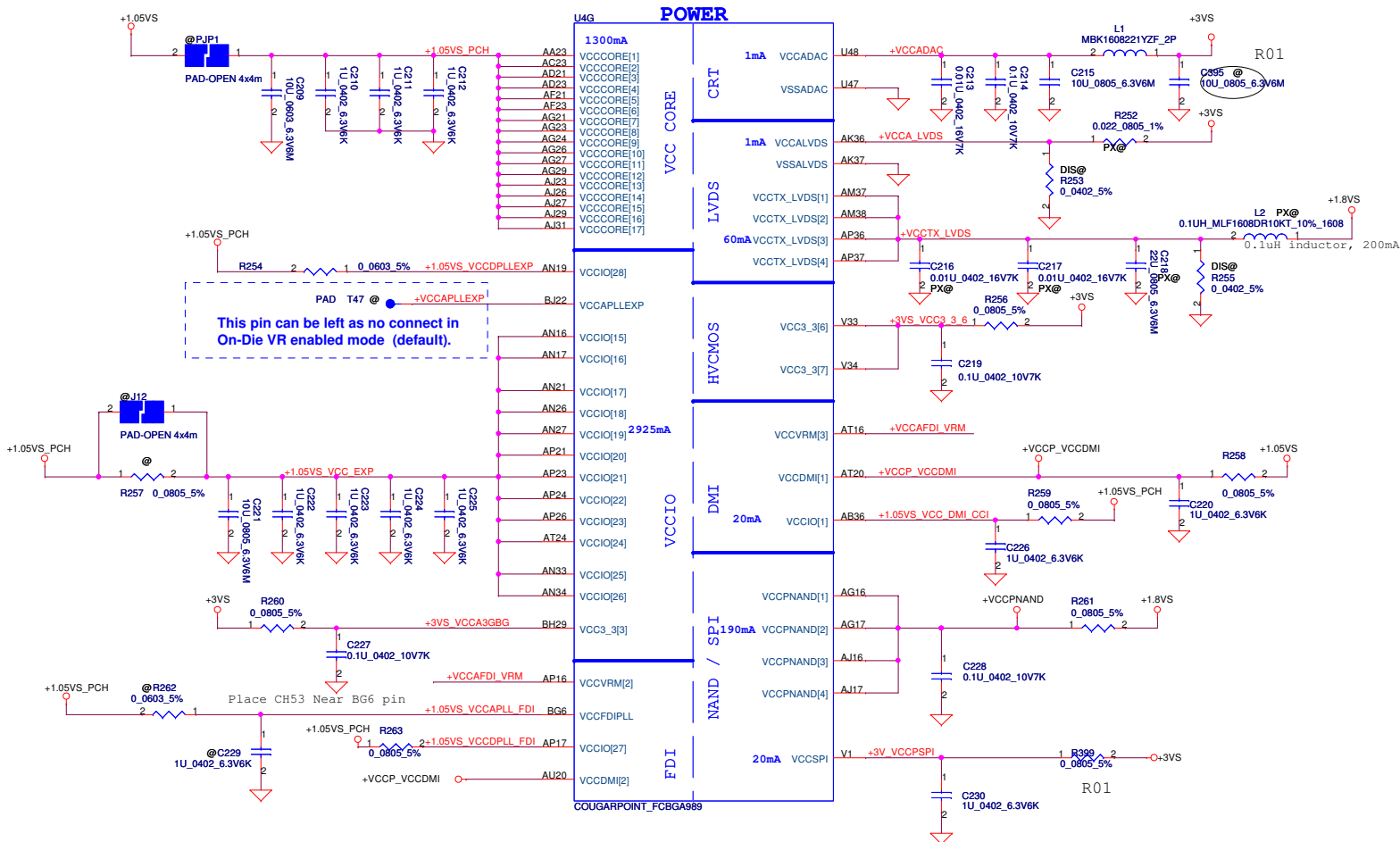
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
★ ; On-Die PLL Voltage Regulator disable
L : On-Die PLL Voltage Regulator disable

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable

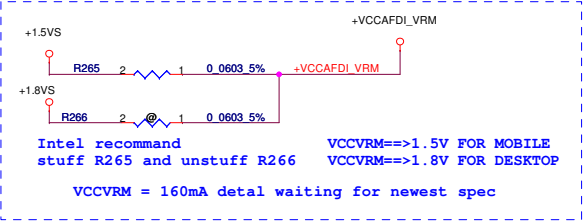


INIT3_3V
This signal has weak internal PU, can't pull low
Intel schematic revieve recommend

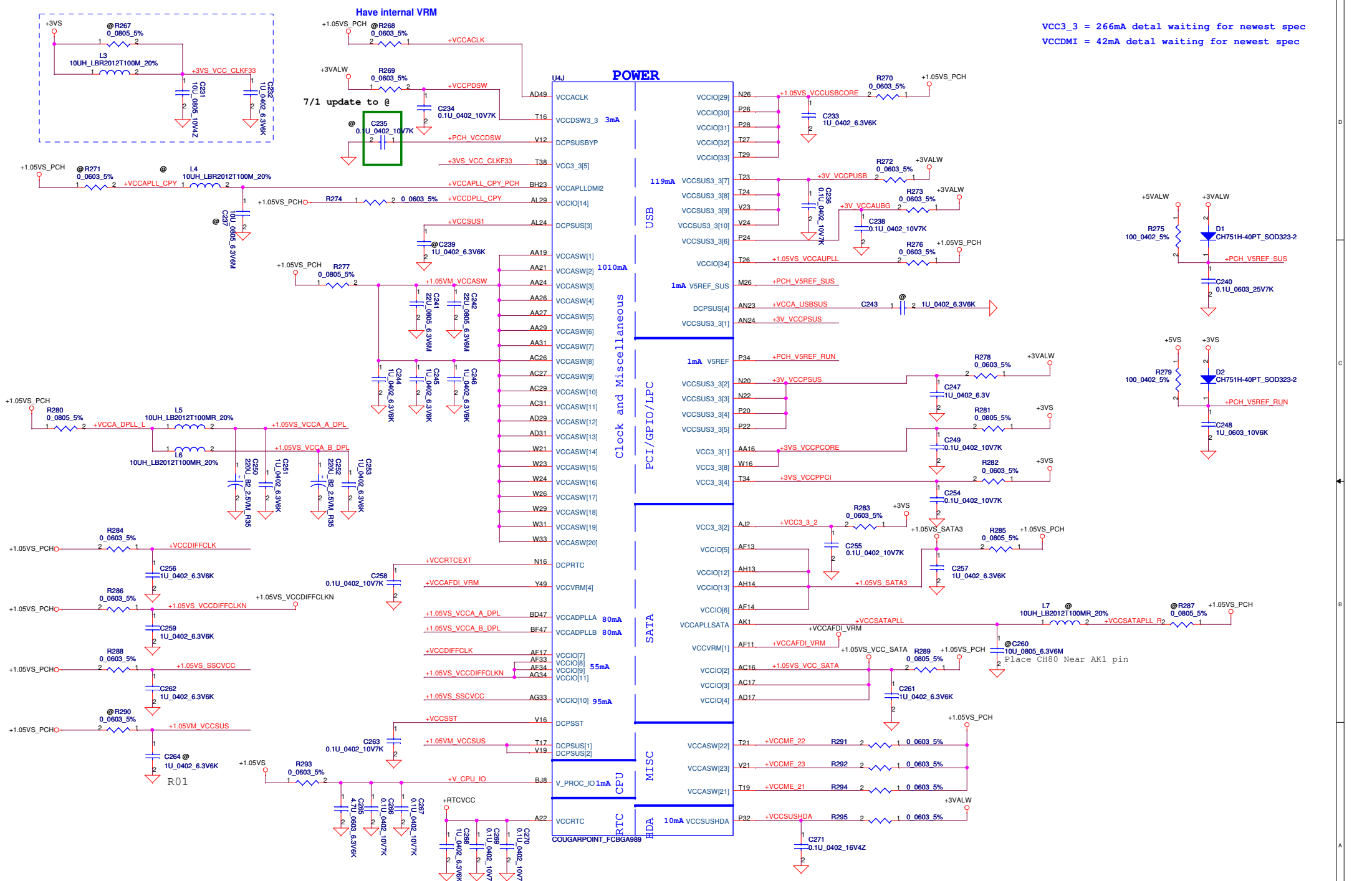
COUGARPOINT_FCBGA989



This pin can be left as no connect in On-Die VR enabled mode (default).



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

Have internal VRM

7/1 update to @

POWER

USB

Clock and Miscellaneous

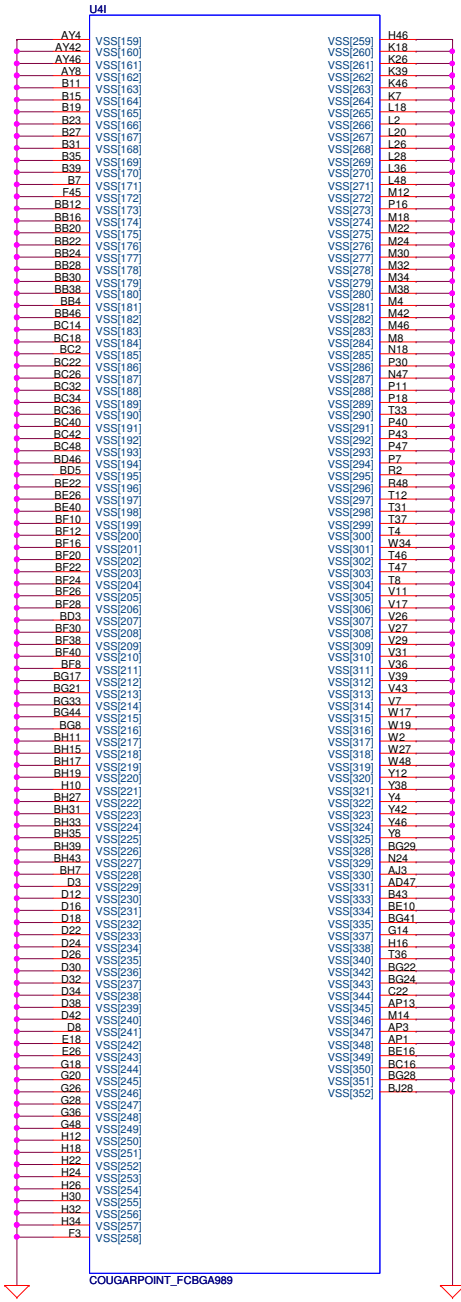
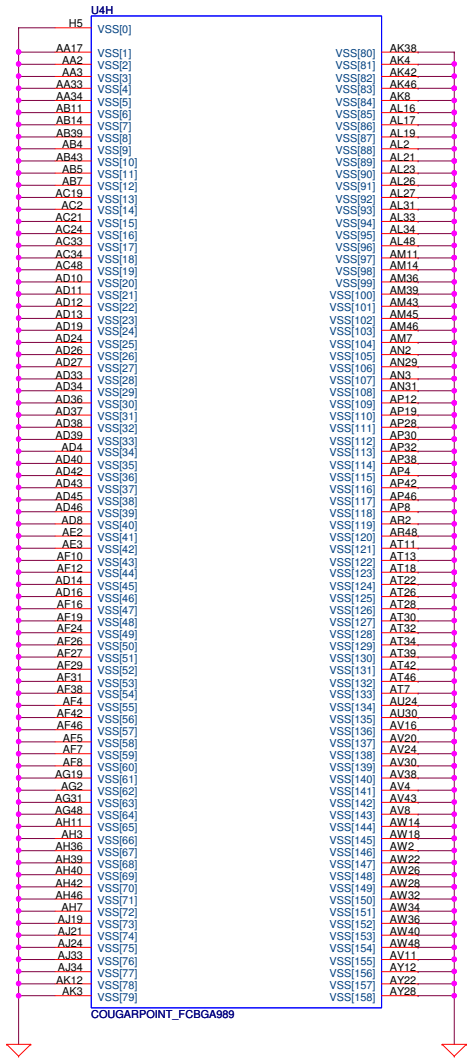
SATA

MISC

CPU

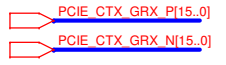
RTC

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				Rev 0.1

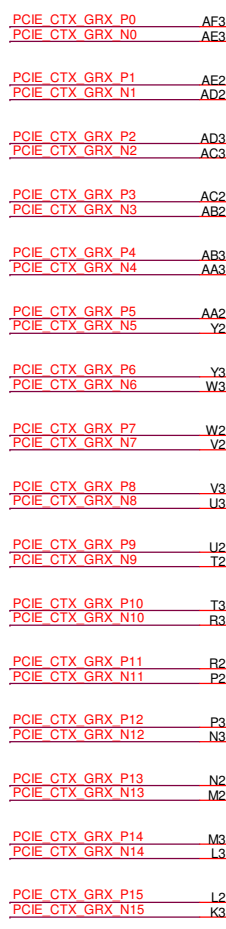


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Date: Tuesday, August 17, 2010				Sheet	22 of 57

[5] PCIE_CTX_GRX_P[15..0] → PCIE_CTX_GRX_P[15..0]
 [5] PCIE_CTX_GRX_N[15..0] → PCIE_CTX_GRX_N[15..0]

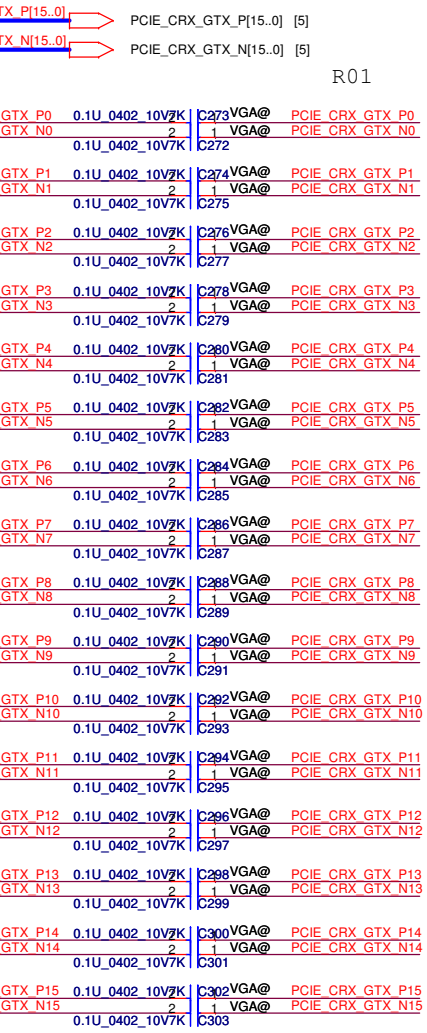
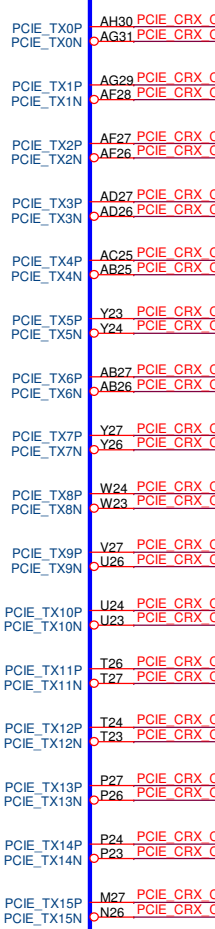


PCIE_CRX_GTX_P[15..0] → PCIE_CRX_GTX_P[15..0] [5]
 PCIE_CRX_GTX_N[15..0] → PCIE_CRX_GTX_N[15..0] [5]

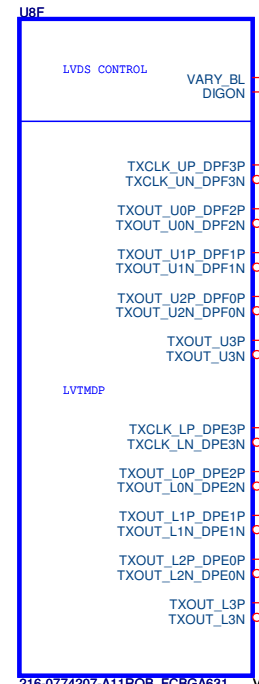


U8A_VGA@

PCI EXPRESS INTERFACE

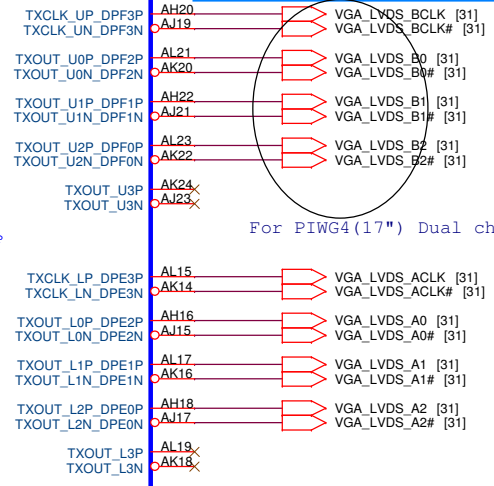
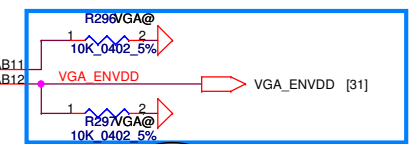


R01



216-0774207-A11ROB_FCBGA631

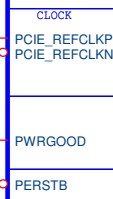
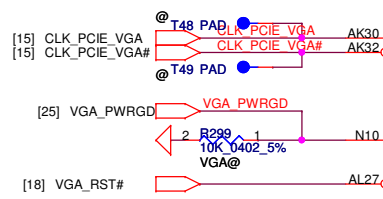
LVDS



R01
07/16

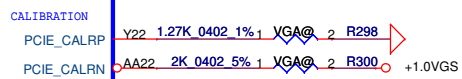
For PIWG4(17") Dual channel Use

VGA 0609



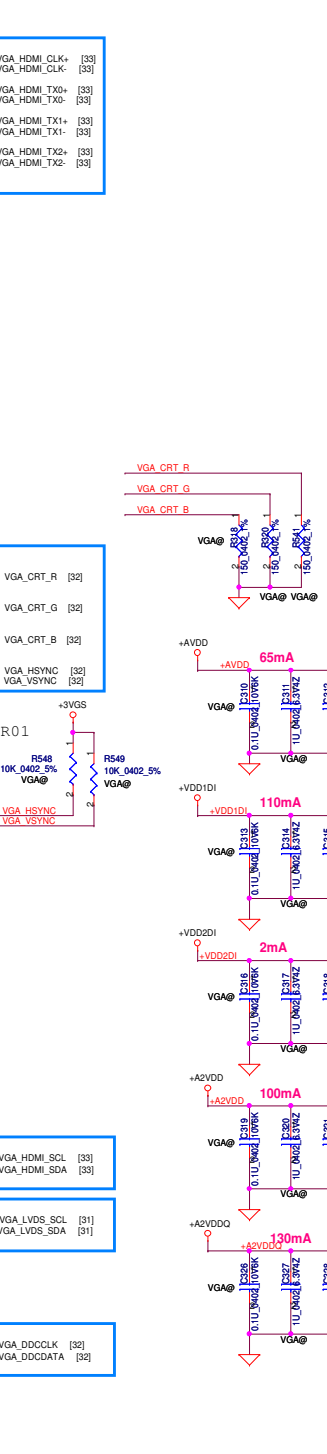
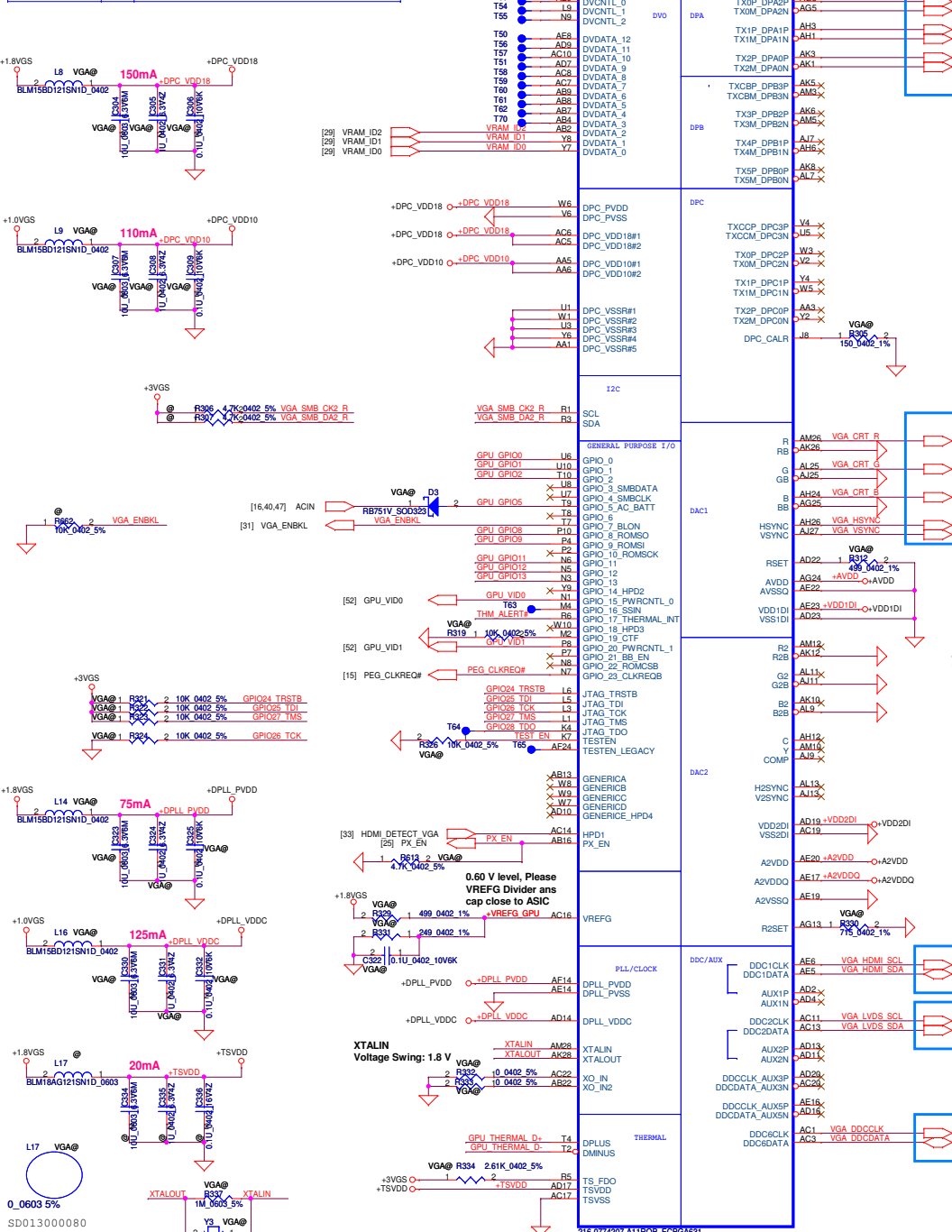
216-0774207-A11ROB_FCBGA631

PCIE LANE



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Date:	Tuesday, August 17, 2010	Sheet	23 of 57	Rev 0.1

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



CONFIGURATION STRAPS

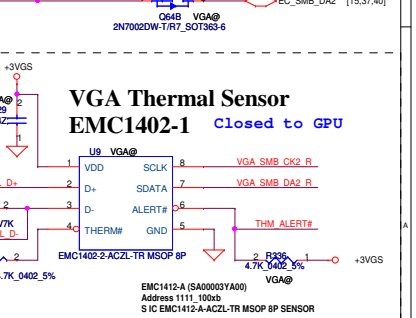
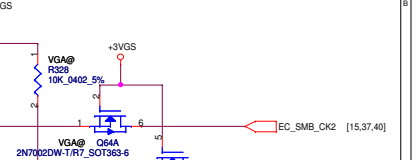
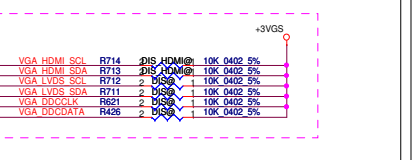
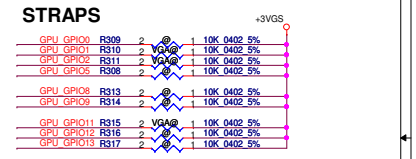
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

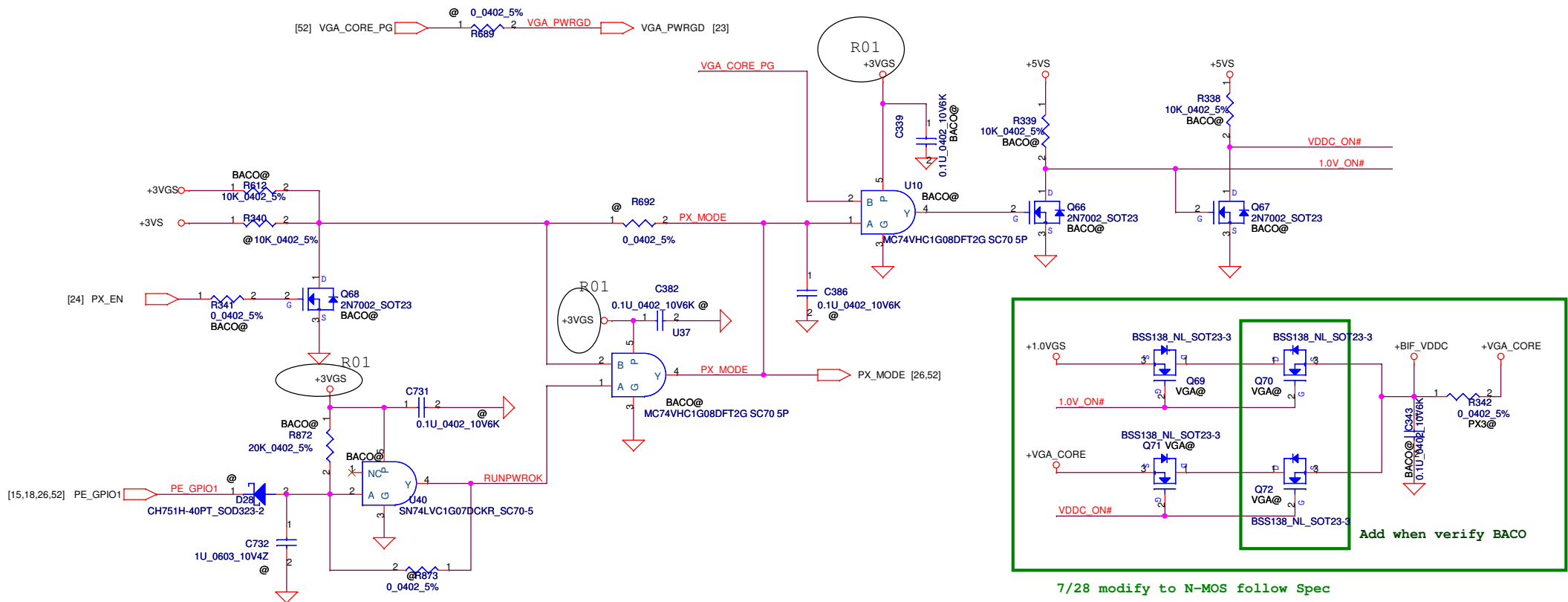
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	POE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[3:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

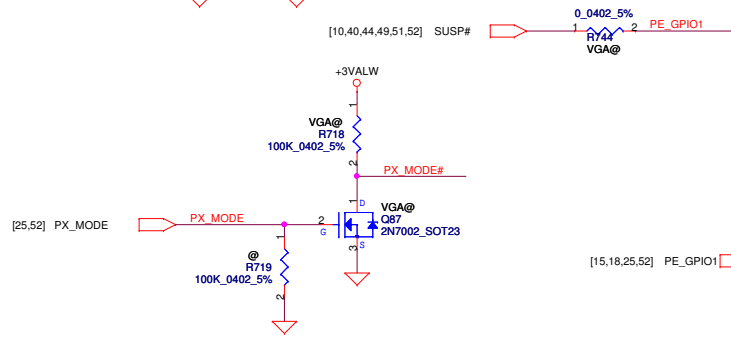
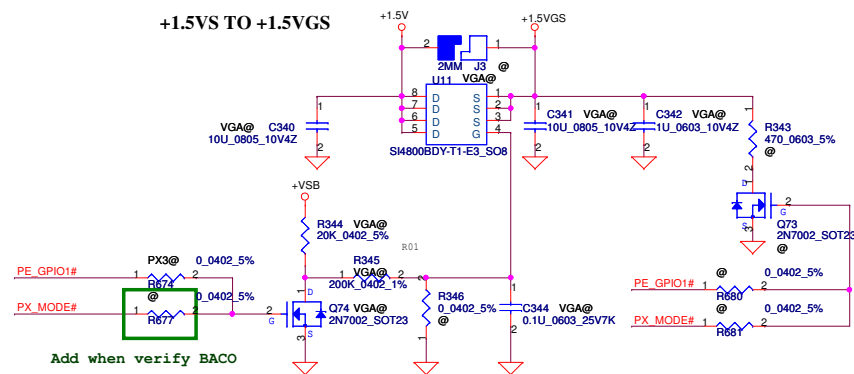
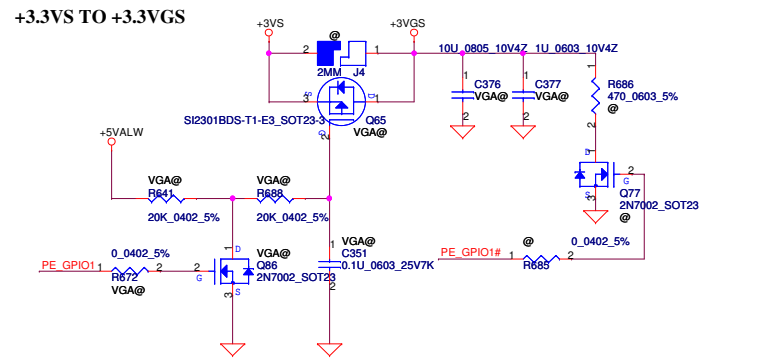
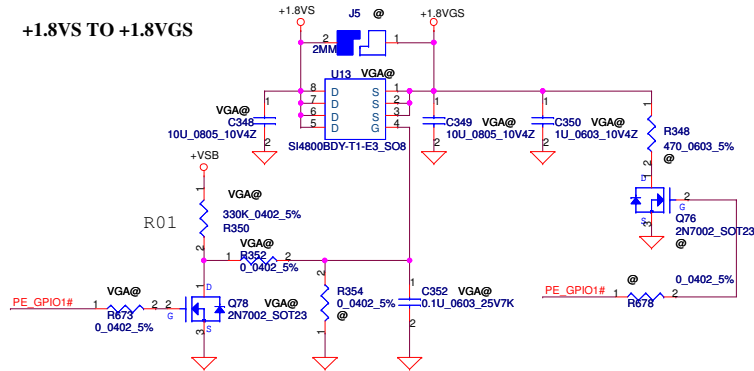
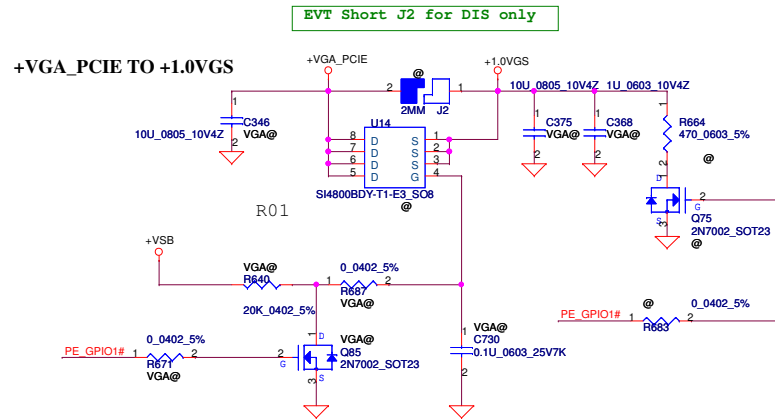
GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8
--------	--------	----------	-------	-------



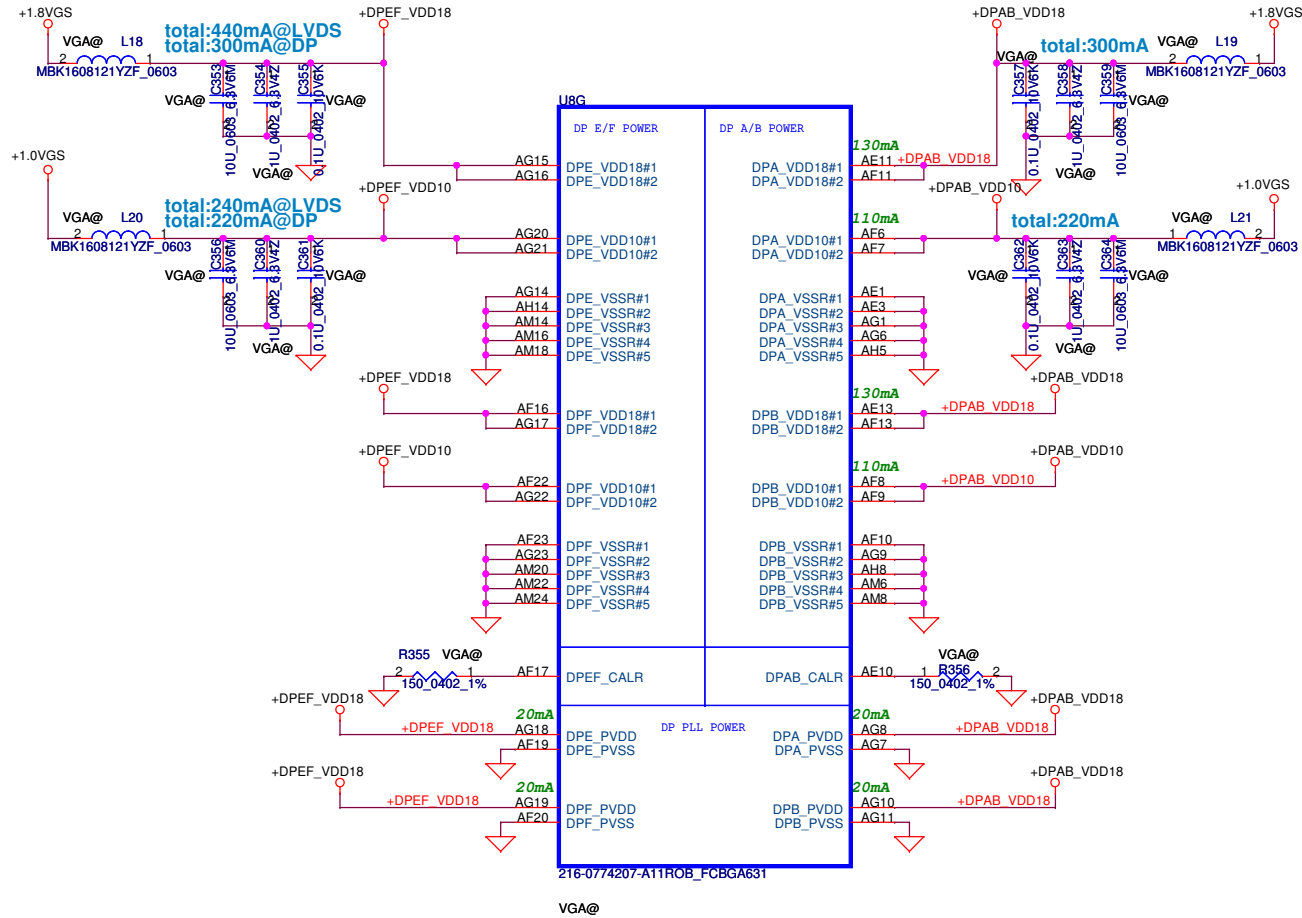


D28 with leakage need to check

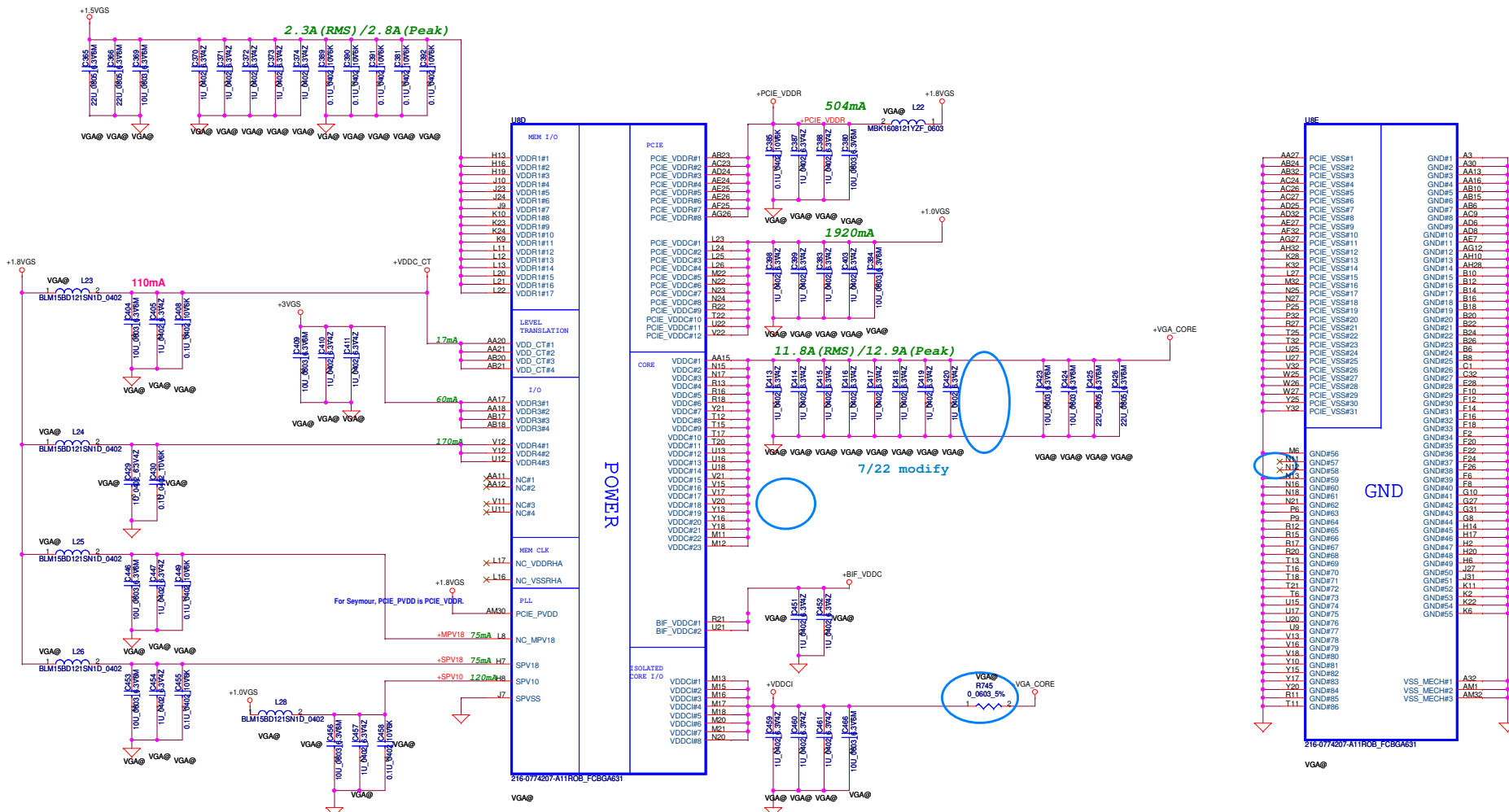
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				LA-6758P	
Date:	Tuesday, August 17, 2010	Sheet	25	of	57



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				LA-6758P
				Rev 0.1
				Date: Tuesday, August 17, 2010 Sheet 26 of 57

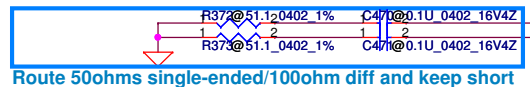
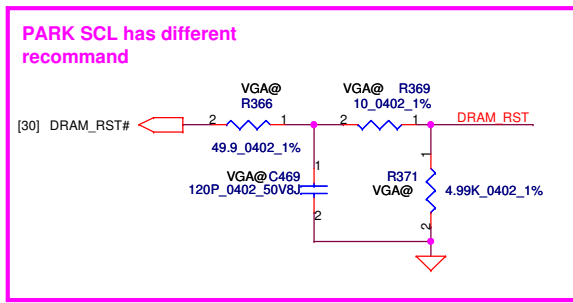
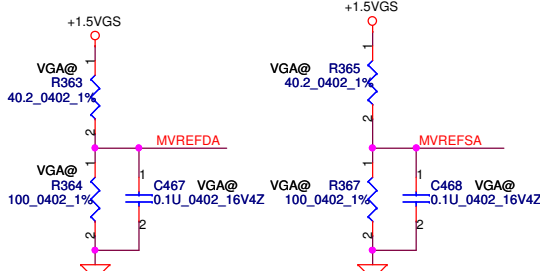


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title RobsonXT-S3 DP PWR	
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				Date: Tuesday, August 17, 2010	Sheet 27 of 57



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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title
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Size	C	Document Number		Rev
Date:	Tuesday, August 17, 2010	Sheet	28	of 57

- [30] M_DA[63..0] M_DA[63..0]
- [30] M_MA[13..0] M_MA[13..0]
- [30] M_DQM[7..0] M_DQM[7..0]
- [30] M_DQS[7..0] M_DQS[7..0]
- [30] M_DQS#[7..0] M_DQS#[7..0]

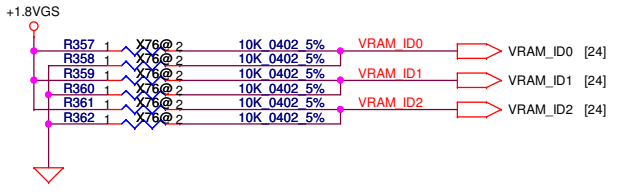


Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation,if not need, DNI.

- M_DA0 K27
- M_DA1 J29
- M_DA2 H30
- M_DA3 H32
- M_DA4 G29
- M_DA5 F28
- M_DA6 F32
- M_DA7 F30
- M_DA8 C30
- M_DA9 F27
- M_DA10 A28
- M_DA11 C28
- M_DA12 E27
- M_DA13 G26
- M_DA14 D26
- M_DA15 F25
- M_DA16 A25
- M_DA17 C25
- M_DA18 E25
- M_DA19 D24
- M_DA20 E23
- M_DA21 F23
- M_DA22 D22
- M_DA23 F21
- M_DA24 E21
- M_DA25 D20
- M_DA26 E19
- M_DA28 D18
- M_DA29 E17
- M_DA30 A17
- M_DA31 C17
- M_DA32 E17
- M_DA33 D16
- M_DA34 F15
- M_DA35 A15
- M_DA36 D14
- M_DA37 F13
- M_DA38 A13
- M_DA39 C13
- M_DA40 E13
- M_DA41 A11
- M_DA42 C11
- M_DA43 F11
- M_DA44 A9
- M_DA45 C9
- M_DA46 F9
- M_DA47 D8
- M_DA48 E7
- M_DA49 A7
- M_DA50 C7
- M_DA51 A5
- M_DA52 E5
- M_DA53 A3
- M_DA54 C3
- M_DA55 E1
- M_DA56 G7
- M_DA57 G6
- M_DA58 G1
- M_DA59 G3
- M_DA60 J6
- M_DA61 J1
- M_DA62 J3
- M_DA63 J5

MEMORY INTERFACE

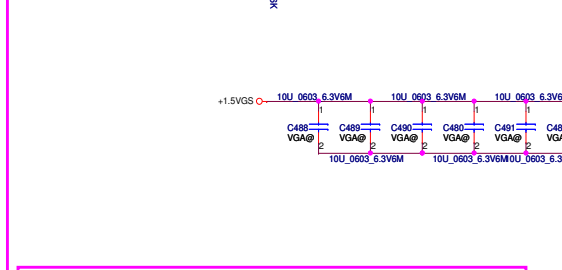
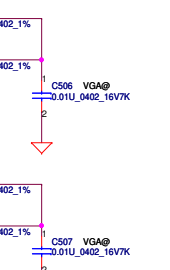
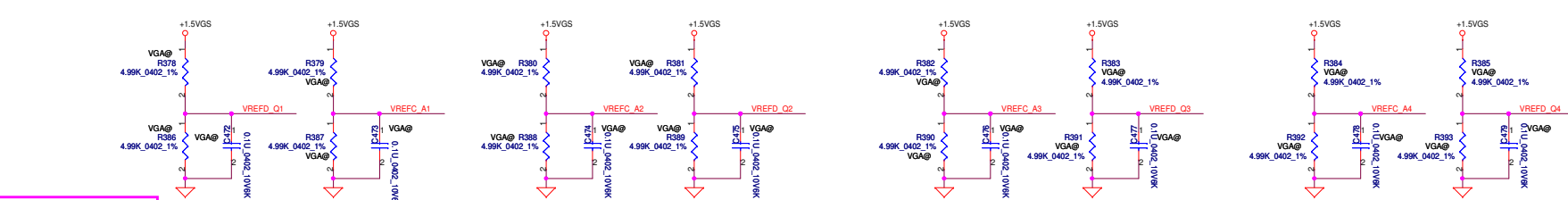
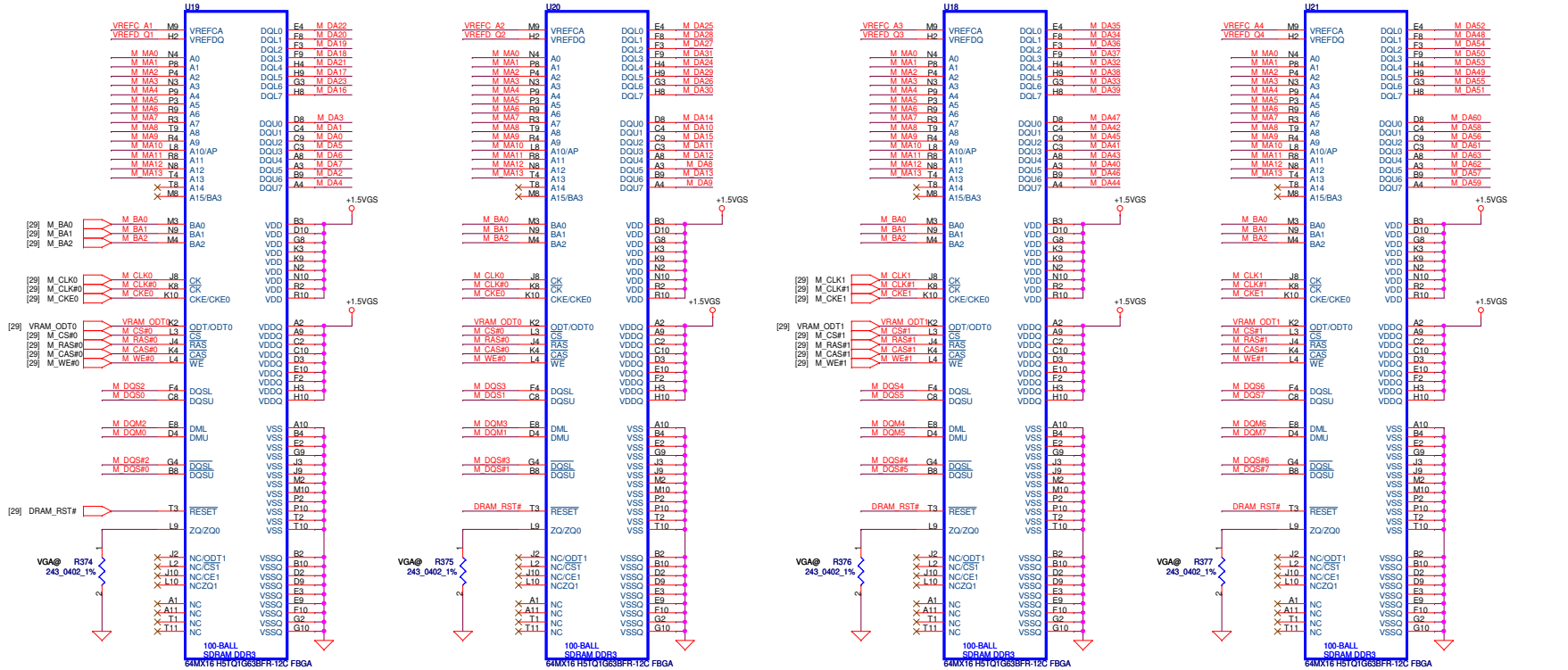
- GDDR5/DDR3 DQA0_0/DQA_0 MAA0_0/MAA_0 K17 M_MA0
- DQA0_1/DQA_1 MAA0_1/MAA_1 J20 M_MA1
- DQA0_2/DQA_2 MAA0_2/MAA_2 H23 M_MA2
- DQA0_3/DQA_3 MAA0_3/MAA_3 G23 M_MA3
- DQA0_4/DQA_4 MAA0_4/MAA_4 H24 M_MA4
- DQA0_5/DQA_5 MAA0_5/MAA_5 J19 M_MA5
- DQA0_6/DQA_6 MAA0_6/MAA_6 K19 M_MA6
- DQA0_7/DQA_7 MAA0_7/MAA_7 J14 M_MA7
- DQA0_8/DQA_8 MAA0_8/MAA_8 J14 M_MA8
- DQA0_9/DQA_9 MAA1_1/MAA_9 K14 M_MA9
- DQA0_10/DQA_10 MAA1_2/MAA_10 J11 M_MA10
- DQA0_11/DQA_11 MAA1_3/MAA_11 J11 M_MA11
- DQA0_12/DQA_12 MAA1_4/MAA_12 H11 M_MA12
- DQA0_13/DQA_13 MAA1_5/MAA_13/BA2 G11 M_BA2 [30]
- DQA0_14/DQA_14 MAA1_6/MAA_14/BA0 J16 M_BA0 [30]
- DQA0_15/DQA_15 MAA1_7/MAA_15/BA1 L15 M_BA1 [30]
- DQA0_16/DQA_16 WCKA0_0/DQMA_0 E32 M_DQM0
- DQA0_17/DQA_17 WCKA0B_0/DQMA_1 E30 M_DQM1
- DQA0_18/DQA_18 WCKA0_1/DQMA_2 A21 M_DQM2
- DQA0_19/DQA_19 WCKA0B_1/DQMA_2 C21 M_DQM3
- DQA0_20/DQA_20 WCKA0_2/DQMA_3 E13 M_DQM4
- DQA0_21/DQA_21 WCKA1_0/DQMA_4 D12 M_DQM5
- DQA0_22/DQA_22 WCKA1B_0/DQMA_5 E3 M_DQM6
- DQA0_23/DQA_23 WCKA1_1/DQMA_6 F4 M_DQM7
- DQA0_24/DQA_24 WCKA1B_1/DQMA_7 H28 M_DQS0
- DQA0_25/DQA_25 EDCA0_0/RDQSA_0 C27 M_DQS1
- DQA0_26/DQA_26 EDCA0_1/RDQSA_1 A23 M_DQS2
- DQA0_27/DQA_27 EDCA0_2/RDQSA_2 E19 M_DQS3
- DQA0_28/DQA_28 EDCA0_3/RDQSA_3 E15 M_DQS4
- DQA0_29/DQA_29 EDCA1_0/RDQSA_4 D10 M_DQS5
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- DQA0_31/DQA_31 EDCA1_2/RDQSA_6 G5 M_DQS7
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- DQA1_1/DQA_33 DBBIA0_0/WDQSA_0 A27 M_DQS#1
- DQA1_2/DQA_34 DBBIA0_1/WDQSA_1 C23 M_DQS#2
- DQA1_3/DQA_35 DBBIA0_2/WDQSA_2 C19 M_DQS#3
- DQA1_4/DQA_36 DBBIA0_3/WDQSA_3 C15 M_DQS#4
- DQA1_5/DQA_37 DBBIA1_0/WDQSA_4 E9 M_DQS#5
- DQA1_6/DQA_38 DBBIA1_1/WDQSA_5 C5 M_DQS#6
- DQA1_7/DQA_39 DBBIA1_2/WDQSA_6 H4 M_DQS#7
- DQA1_8/DQA_40 DBBIA1_3/WDQSA_7 L18 VRAM_ODT0 [30]
- DQA1_9/DQA_41 ADBIA0_0/ODTA0 K16 VRAM_ODT1 [30]
- DQA1_10/DQA_42 ADBIA1_0/ODTA1 H26 M_CLK0 [30]
- DQA1_11/DQA_43 CLKA0 H25 M_CLK#0 [30]
- DQA1_12/DQA_44 CLKA0B G9 M_CLK1 [30]
- DQA1_13/DQA_45 CLKA1 H9 M_CLK#1 [30]
- DQA1_14/DQA_46 CLKA1B G22 M_RAS#0 [30]
- DQA1_15/DQA_47 RASA0 G17 M_RAS#1 [30]
- DQA1_16/DQA_48 RASA1B G19 M_CAS#0 [30]
- DQA1_17/DQA_49 DQA1_24/DQA_55 CASA0 G16 M_CAS#1 [30]
- DQA1_18/DQA_50 DQA1_25/DQA_57 CSA0B_0 H22 M_CS#0 [30]
- DQA1_19/DQA_51 DQA1_26/DQA_58 CSA0B_1 J22 M_CS#1 [30]
- DQA1_20/DQA_52 DQA1_27/DQA_59 CSA1B_0 G13 M_CKE0 [30]
- DQA1_21/DQA_53 DQA1_28/DQA_60 CSA1B_1 K13 M_CKE1 [30]
- DQA1_22/DQA_54 DQA1_29/DQA_61 K20 M_WE#0 [30]
- DQA1_23/DQA_55 DQA1_30/DQA_62 J17 M_WE#1 [30]
- DQA1_24/DQA_56 DQA1_31/DQA_63 H10 M_WE#0 [30]
- DQA1_25/DQA_57 DQA1_32/DQA_63 H10 M_WE#1 [30]
- GDDR5 MAA1_8 G14 M_MA13
- MAA0_8 G20



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 512MB PN:SA000032460	R357	R360	R362
Samsung 512MB PN:SA000035700	R358	R359	R362
Hynix 1GB PN:SA00003VS20	R357	R360	R361
Samsung 1GB PN:SA00003MQ20	R358	R359	R361

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Issued Date	2010/07/12	Deciphered Date	2012/07/11	RobsonXT-S3 MEM Interface
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Date:	Tuesday, August 17, 2010	Sheet	29	of 57

- [29] M_DA6[3..0] M_DA6[3..0]
- [29] M_MA[13..0] M_MA[13..0]
- [29] M_DQM[7..0] M_DQM[7..0]
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- [29] M_DQS#[7..0] M_DQS#[7..0]



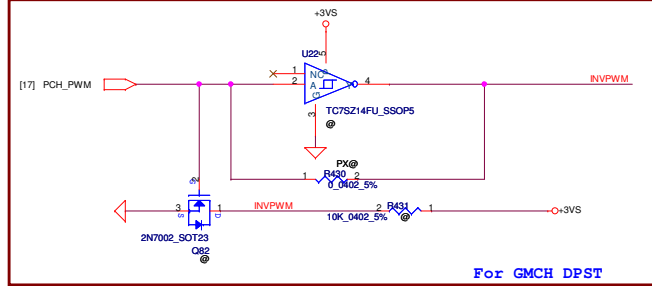
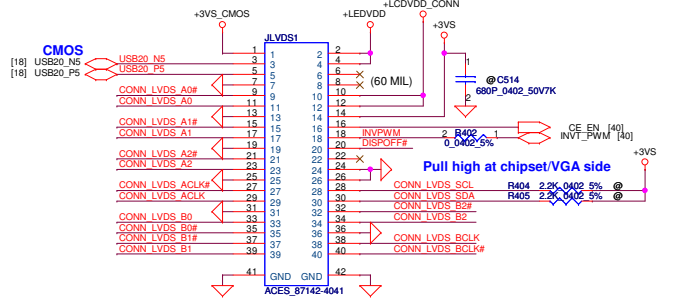
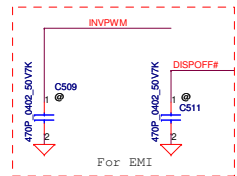
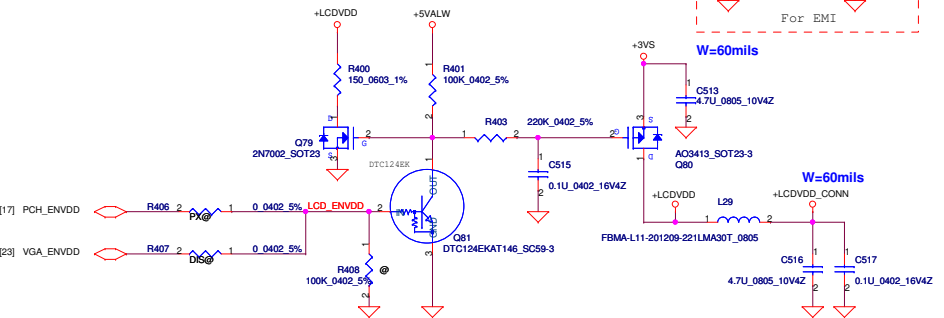
VRAM P/N :
 Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
 Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
 update VRAM PN 0619 update

ref 139-02 recommend
 add off page
 Park SCL recommend pu 60.4 ohm to
 0.5V update

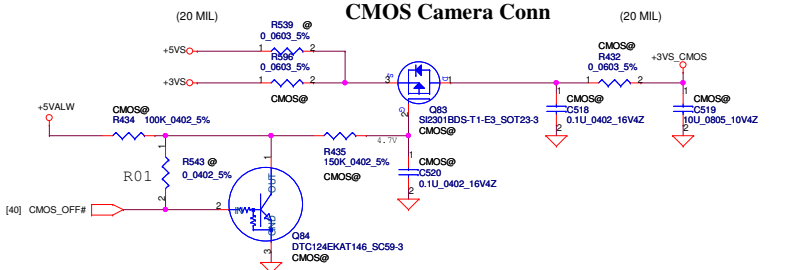
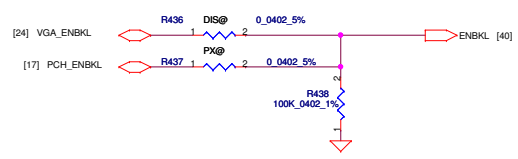
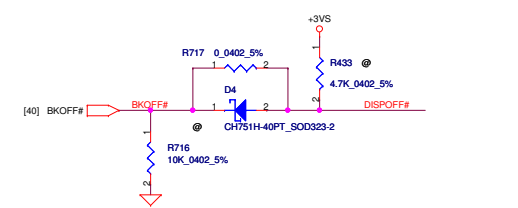
Security Classification	Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	RobsonXT-S3 VRAM
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VGA LCD/PANEL BD. Conn.

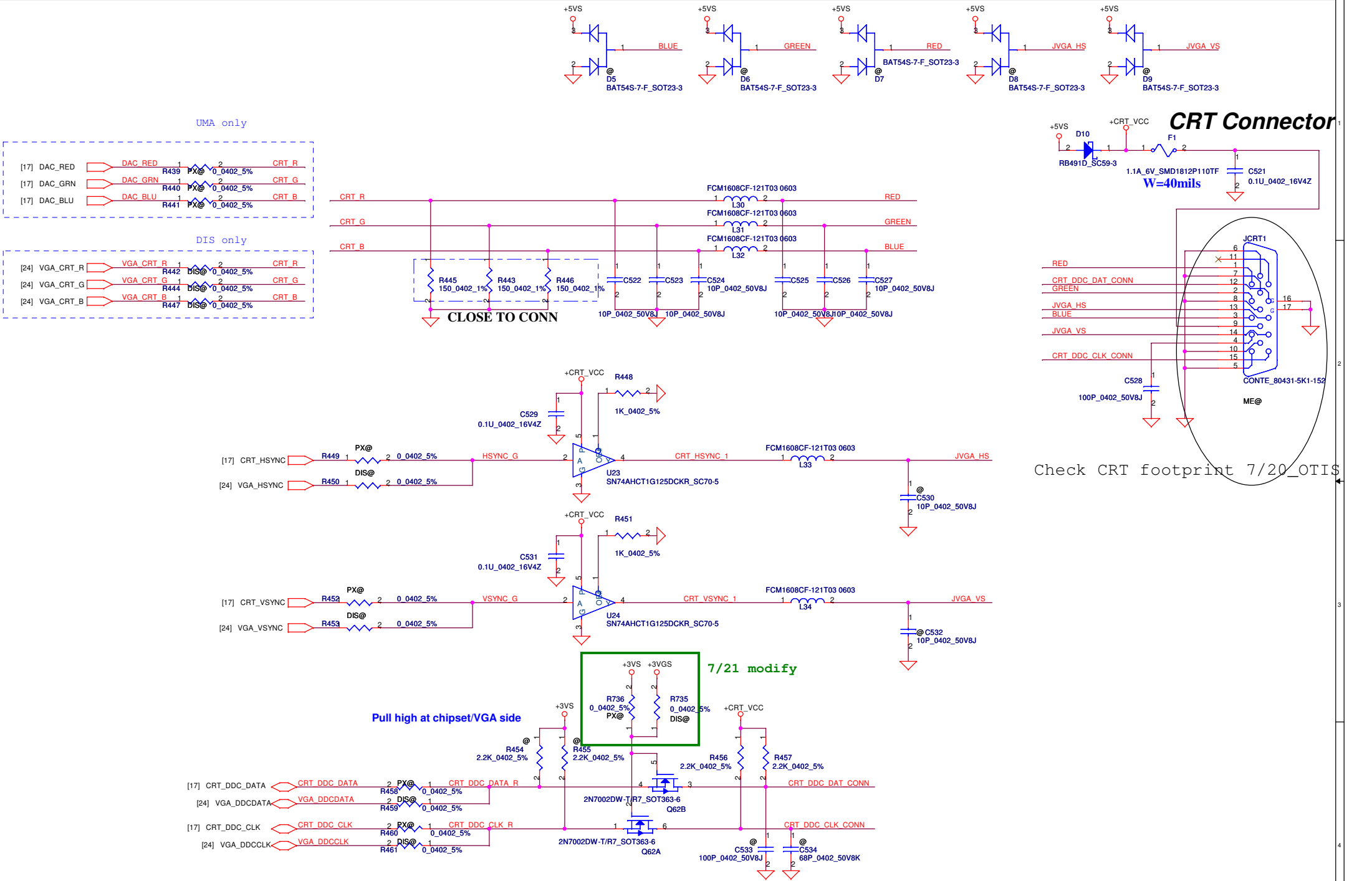
LCD POWER CIRCUIT



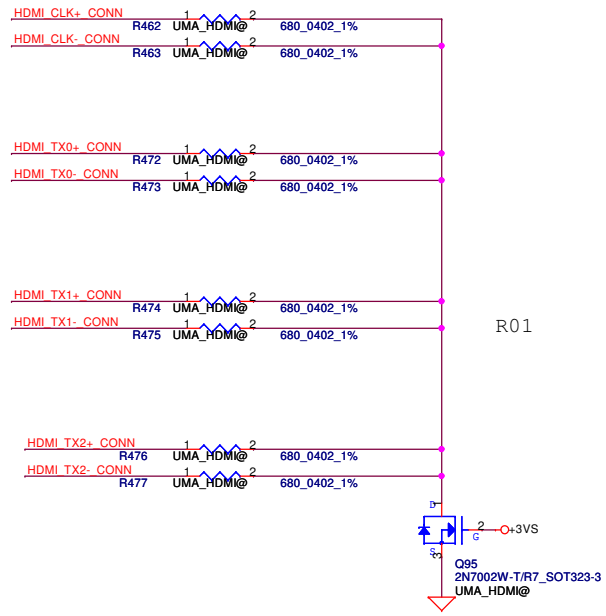
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[24] VGA_LVDS_SDA	VGA_LVDS_SDA	0.0402_5%	2	DIS@	1	R410	CONN LVDS_SDA
[23] VGA_LVDS_A0	VGA_LVDS_A0	0.0402_5%	2	DIS@	1	R411	CONN LVDS_A0
[23] VGA_LVDS_A0#	VGA_LVDS_A0#	0.0402_5%	2	DIS@	1	R412	CONN LVDS_A0#
[23] VGA_LVDS_A1	VGA_LVDS_A1	0.0402_5%	2	DIS@	1	R413	CONN LVDS_A1
[23] VGA_LVDS_A1#	VGA_LVDS_A1#	0.0402_5%	2	DIS@	1	R414	CONN LVDS_A1#
[23] VGA_LVDS_A2	VGA_LVDS_A2	0.0402_5%	2	DIS@	1	R415	CONN LVDS_A2
[23] VGA_LVDS_A2#	VGA_LVDS_A2#	0.0402_5%	2	DIS@	1	R416	CONN LVDS_A2#
[23] VGA_LVDS_ACLK	VGA_LVDS_ACLK	0.0402_5%	2	DIS@	1	R417	CONN LVDS_ACLK
[23] VGA_LVDS_ACLK#	VGA_LVDS_ACLK#	0.0402_5%	2	DIS@	1	R418	CONN LVDS_ACLK#
[23] VGA_LVDS_B0	VGA_LVDS_B0	0.0402_5%	2	DIS@	1	R722	CONN LVDS_B0
[23] VGA_LVDS_B0#	VGA_LVDS_B0#	0.0402_5%	2	DIS@	1	R723	CONN LVDS_B0#
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[17] EDID_DATA	EDID_DATA	0.0402_5%	2	PX@	1	R420	CONN LVDS_SDA
[17] LVDS_A0	LVDS_A0	0.0402_5%	2	PX@	1	R421	CONN LVDS_A0
[17] LVDS_A0#	LVDS_A0#	0.0402_5%	2	PX@	1	R422	CONN LVDS_A0#
[17] LVDS_A1	LVDS_A1	0.0402_5%	2	PX@	1	R423	CONN LVDS_A1
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[17] LVDS_A2	LVDS_A2	0.0402_5%	2	PX@	1	R425	CONN LVDS_A2
[17] LVDS_A2#	LVDS_A2#	0.0402_5%	2	PX@	1	R427	CONN LVDS_A2#
[17] LVDS_ACLK	LVDS_ACLK	0.0402_5%	2	PX@	1	R428	CONN LVDS_ACLK
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[17] LVDS_B1	LVDS_B1	0.0402_5%	2	PX@	1	R732	CONN LVDS_B1
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[17] LVDS_B2	LVDS_B2	0.0402_5%	2	PX@	1	R734	CONN LVDS_B2
[17] LVDS_B2#	LVDS_B2#	0.0402_5%	2	PX@	1	R733	CONN LVDS_B2#
[17] LVDS_BCLK	LVDS_BCLK	0.0402_5%	2	PX@	1	R728	CONN LVDS_BCLK
[17] LVDS_BCLK#	LVDS_BCLK#	0.0402_5%	2	PX@	1	R729	CONN LVDS_BCLK#



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Issued Date	2010/07/12	Deciphered Date	2012/07/11	LVDS/CAMERA
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Customer	Document Number	Rev	LA-6758P	
Date	Tuesday, August 17, 2010	Sheet	31	of 57

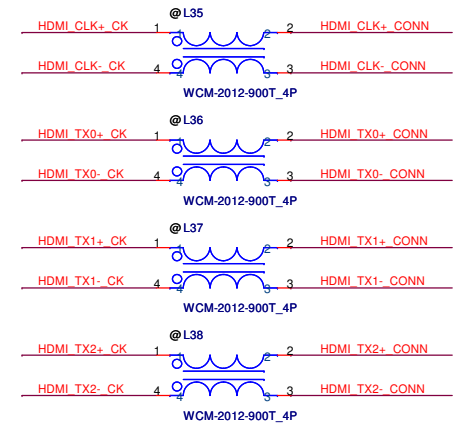


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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Date:	Tuesday, August 17, 2010	Sheet	32	of	57

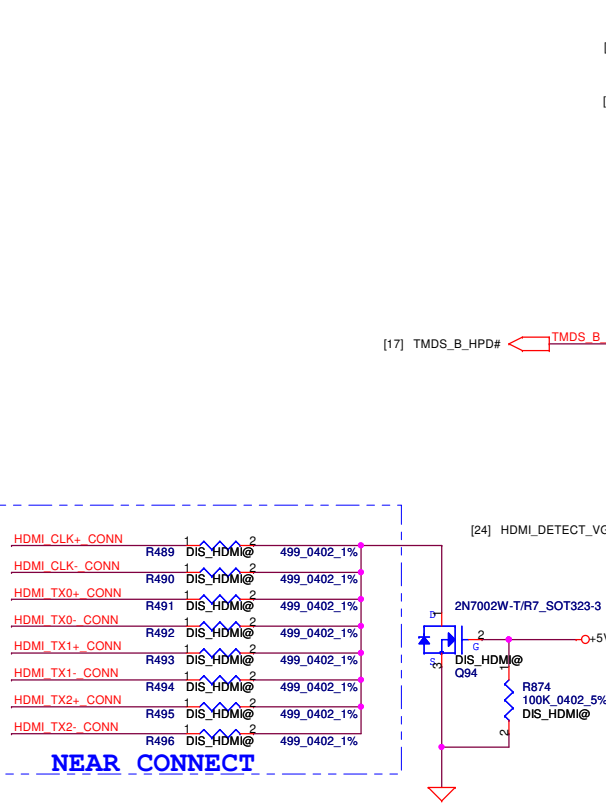


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[17]	HDMI_CLK- CK	HDMI@	R465	1	2	0.0402	5%	HDMI_CLK- CONN
[17]	HDMI_TX0+ CK	HDMI@	R466	1	2	0.0402	5%	HDMI_TX0+ CONN
[17]	HDMI_TX0- CK	HDMI@	R467	1	2	0.0402	5%	HDMI_TX0- CONN
[17]	HDMI_TX1+ CK	HDMI@	R468	1	2	0.0402	5%	HDMI_TX1+ CONN
[17]	HDMI_TX1- CK	HDMI@	R469	1	2	0.0402	5%	HDMI_TX1- CONN
[17]	HDMI_TX2+ CK	HDMI@	R470	1	2	0.0402	5%	HDMI_TX2+ CONN
[17]	HDMI_TX2- CK	HDMI@	R471	1	2	0.0402	5%	HDMI_TX2- CONN

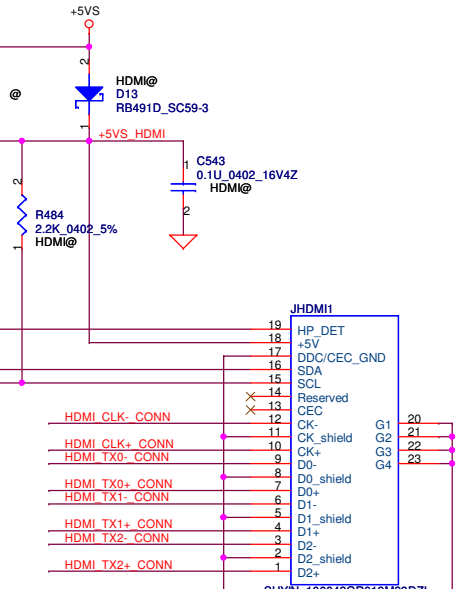
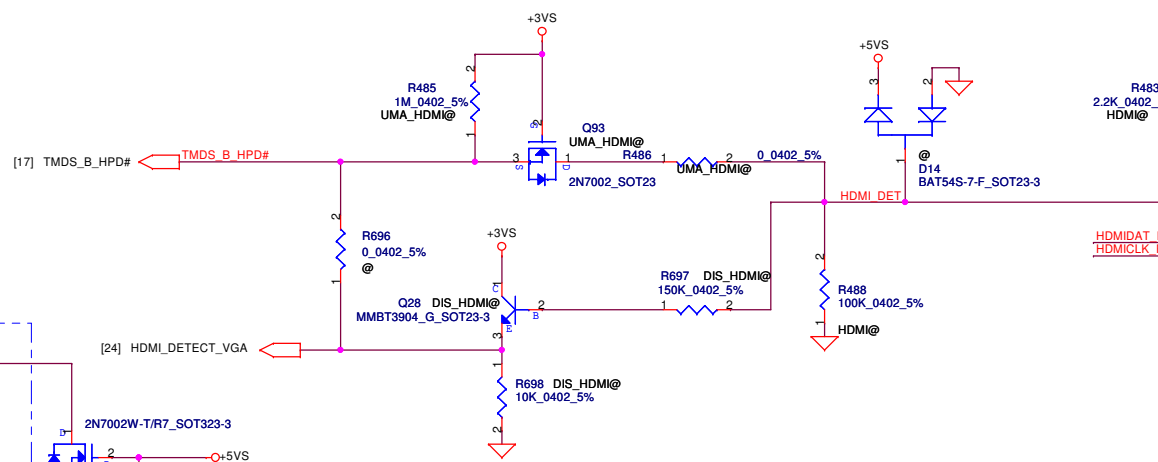
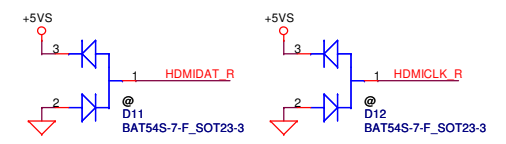
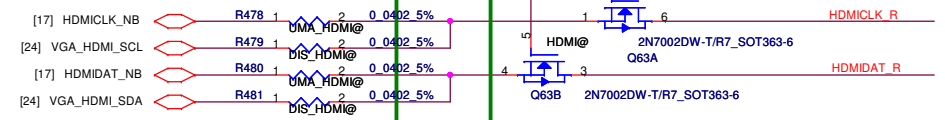
[24]	VGA_HDMI_CLK+	C535	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_CLK+ CK
[24]	VGA_HDMI_CLK-	C536	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_CLK- CK
[24]	VGA_HDMI_TX0+	C537	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_TX0+ CK
[24]	VGA_HDMI_TX0-	C538	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_TX0- CK
[24]	VGA_HDMI_TX1+	C539	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_TX1+ CK
[24]	VGA_HDMI_TX1-	C540	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_TX1- CK
[24]	VGA_HDMI_TX2+	C541	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_TX2+ CK
[24]	VGA_HDMI_TX2-	C542	1	2	DIS_HDMI@	0.1U_0402_16V7K	HDMI_TX2- CK



R01



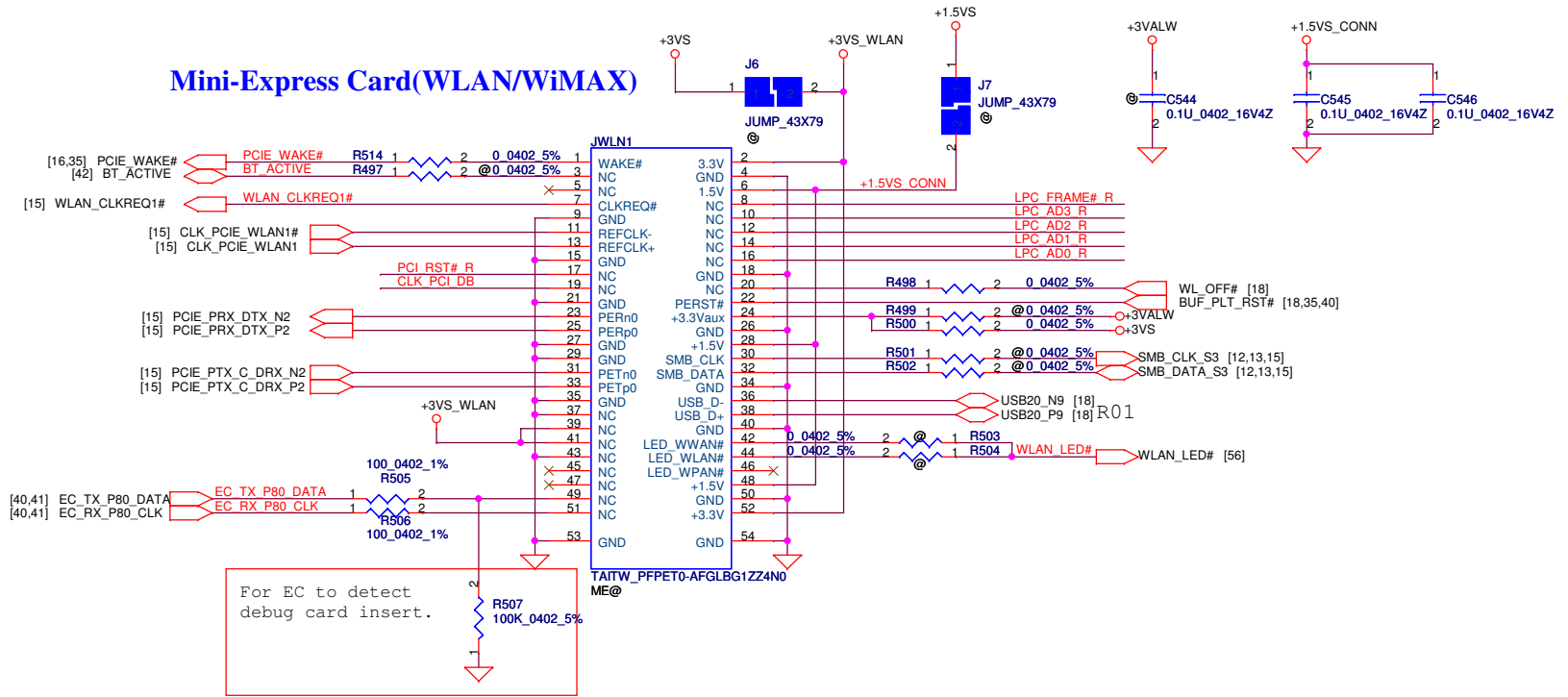
Pull up R for PCH OR VGA SIDE



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Compal Electronics, Ltd.			
Title			
HDMI CONN			
Size	Document Number	Rev	
Custom	LA-6758P	0.1	
Date	Tuesday, August 17, 2010	Sheet	33 of 57

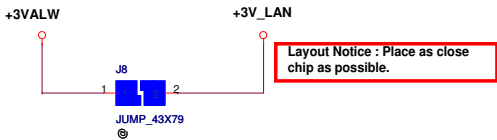
Mini-Express Card for WLAN/WiMAX(Half)



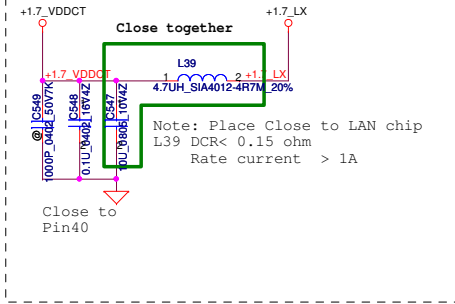
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R508	1	@	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	[14,40]
LPC_AD3 R	R509	1	@	2	0.0402 5%	LPC_AD3	LPC_AD3	[14,40]
LPC_AD2 R	R510	1	@	2	0.0402 5%	LPC_AD2	LPC_AD2	[14,40]
LPC_AD1 R	R511	1	@	2	0.0402 5%	LPC_AD1	LPC_AD1	[14,40]
LPC_AD0 R	R512	1	@	2	0.0402 5%	LPC_AD0	LPC_AD0	[14,40]
PCI_RST# R	R513	1	@	2	0.0402 5%	PCI_RST#	PCI_RST#	[15]
CLK_PCIE_DB						CLK_PCIE_DB	CLK_PCIE_DB	[15]

Security Classification	Compal Secret Data			Compal Electronics, Inc. Mini-Card/NEW Card/SIM			
Issued Date	2010/07/12	Deciphered Date	2012/07/11			Title	
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					Date	Tuesday, August 17, 2010	Sheet



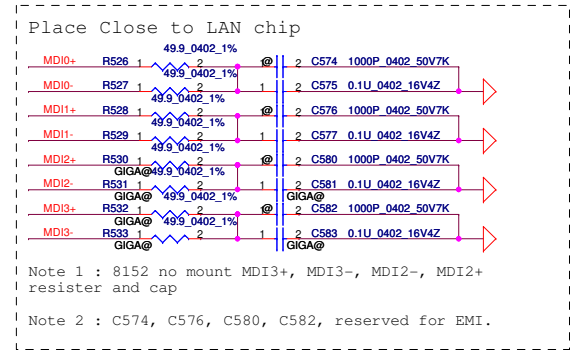
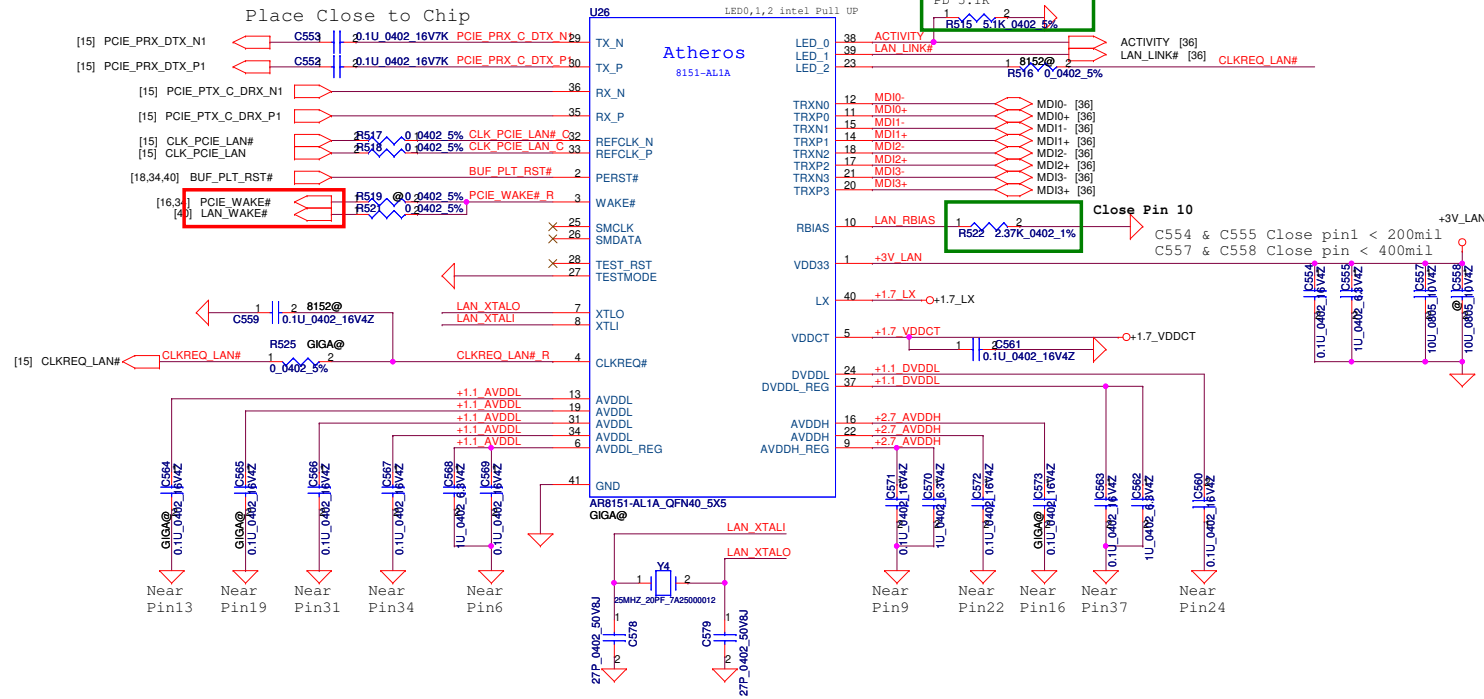
Atheros request can't disable LAN power



Power On strapping

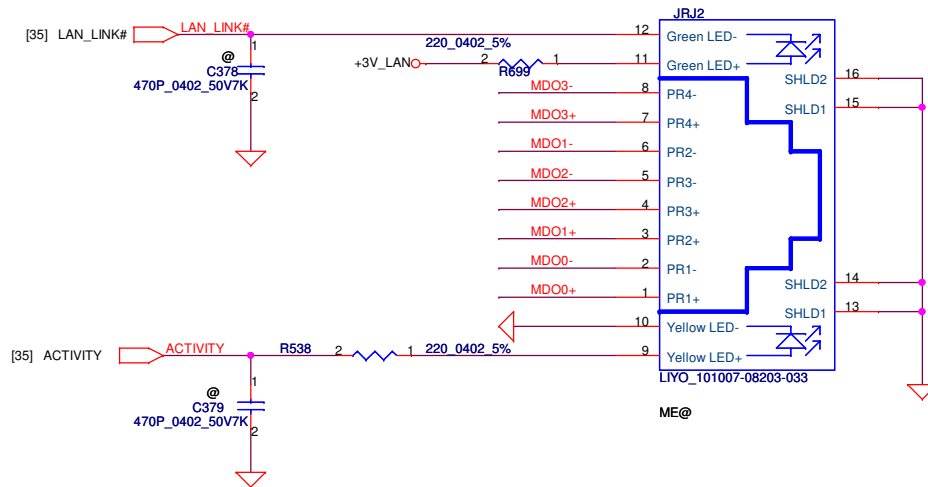
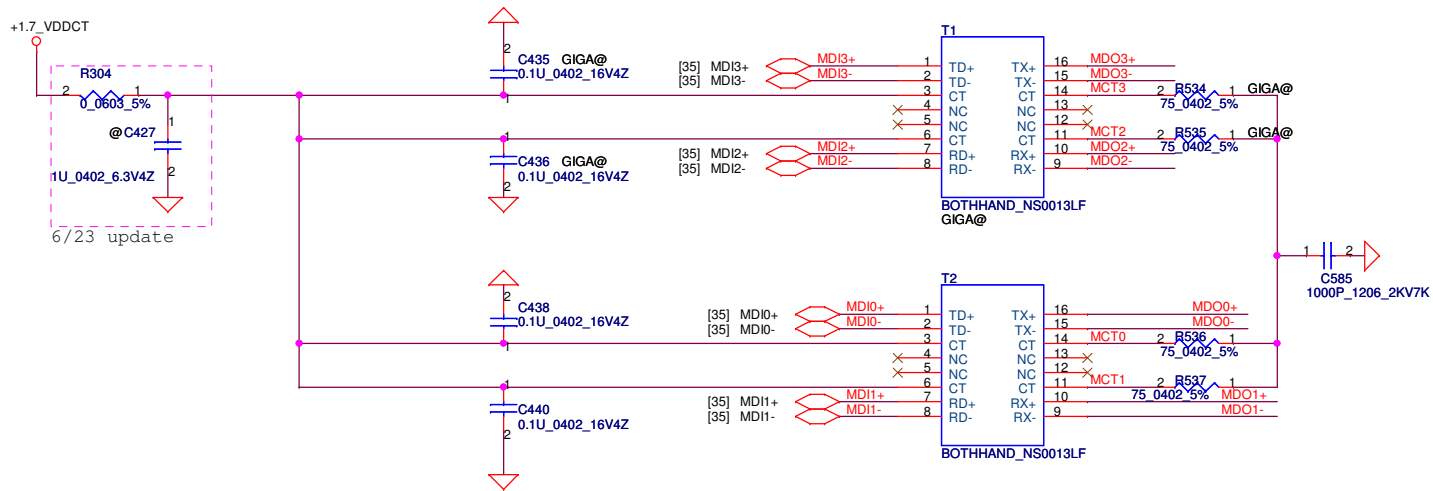
Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

U26 8152@
S IC AR8152-AL1E QFN 40P E-LAN CTRL

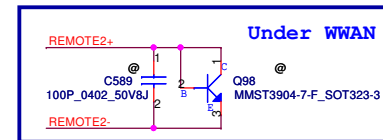
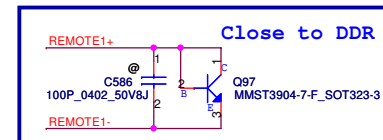
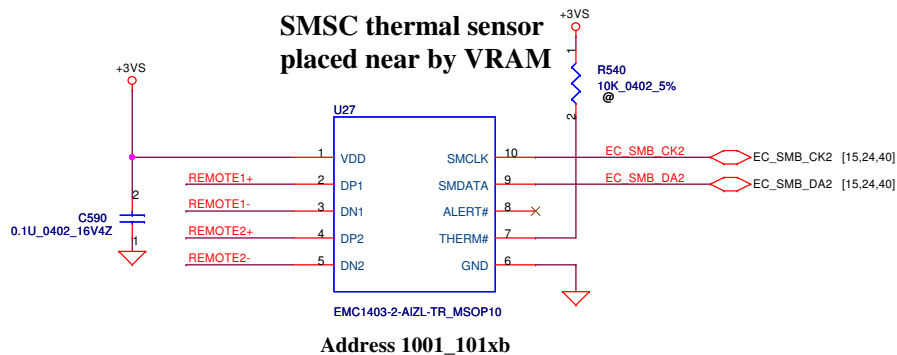
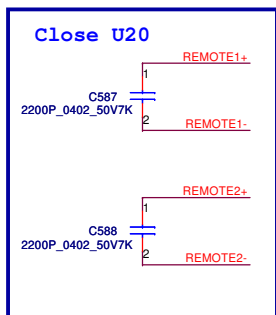


	Pin4	Configure		Pin23	Configure
		R525	C559		
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED [2]	

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				LAN-AR8151/8152
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Date:	Tuesday, August 17, 2010	Sheet	35	of 57

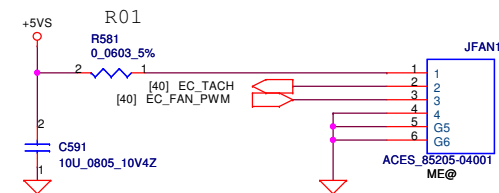


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title LAN_Transformer	
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				Document Number	0.1
Date: Tuesday, August 17, 2010				Sheet	36 of 57



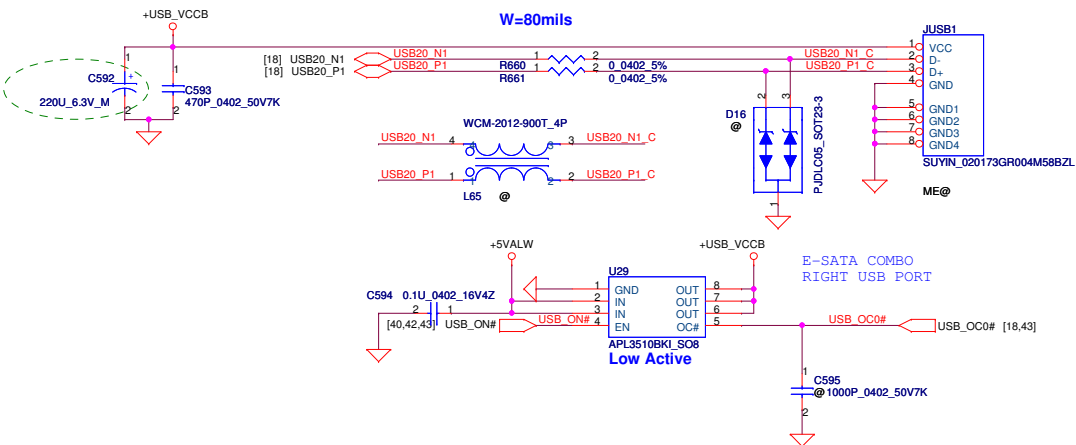
REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

FAN1 Conn

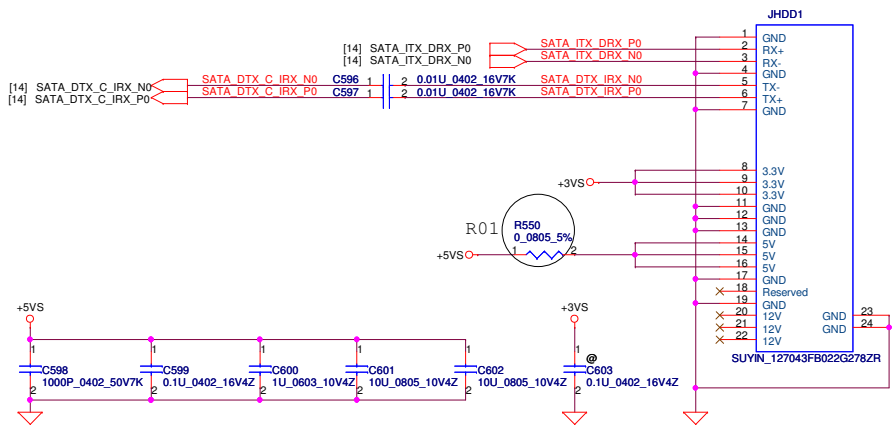


Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
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				Date: Tuesday, August 17, 2010	Rev 0.1
				Sheet 37	of 57

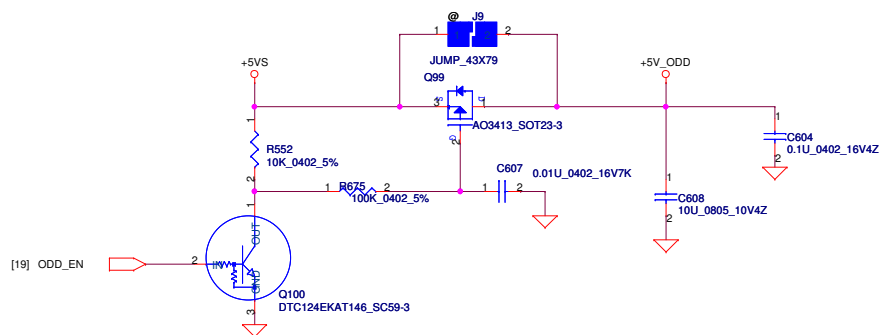
Left USB Conn.



SATA HDD Conn.

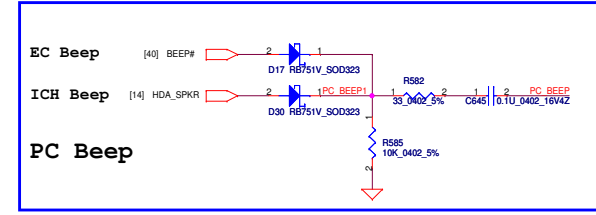
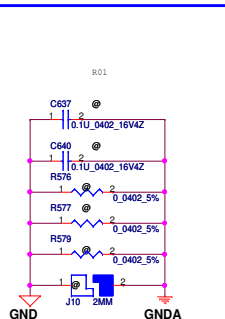
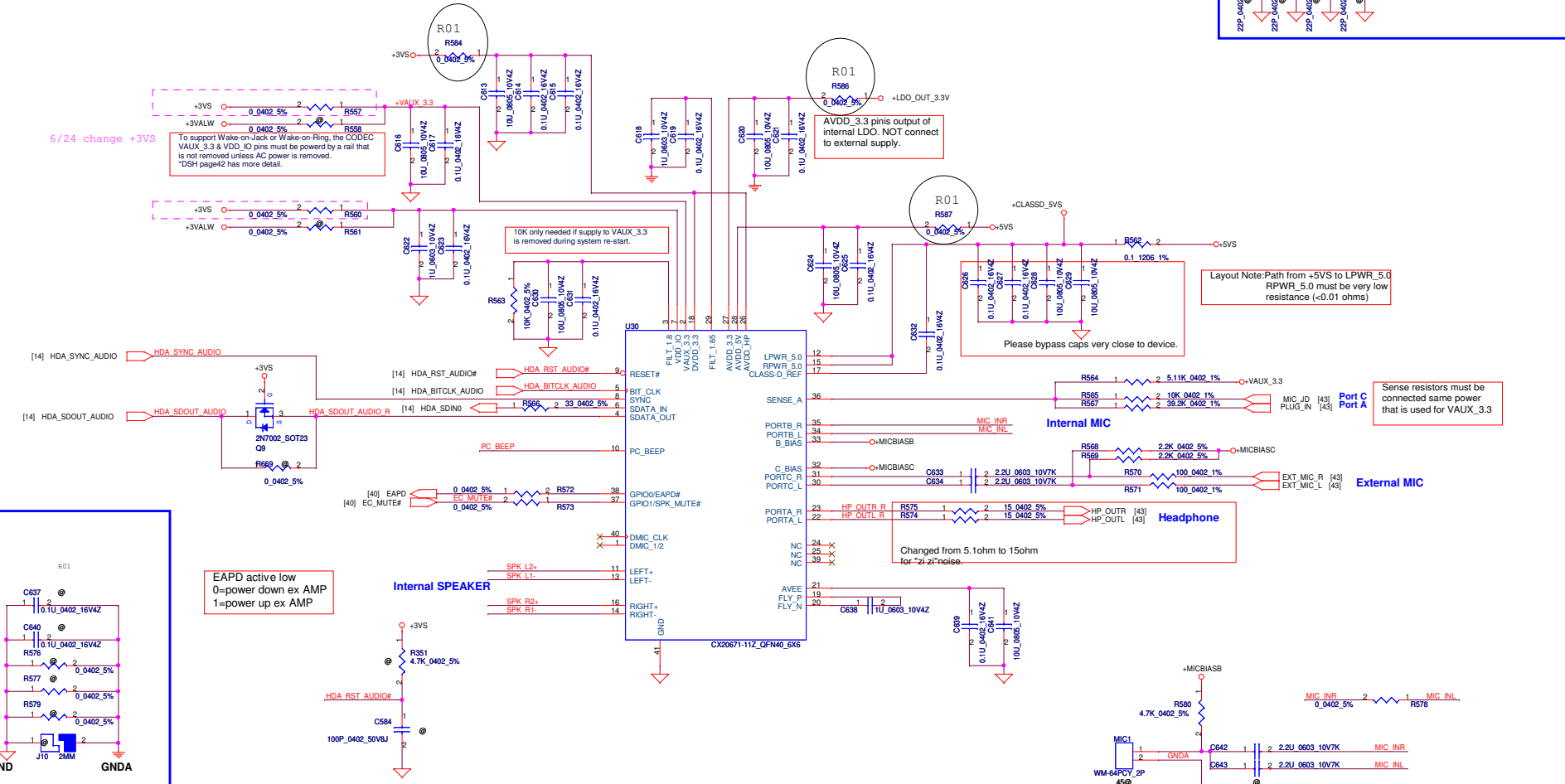
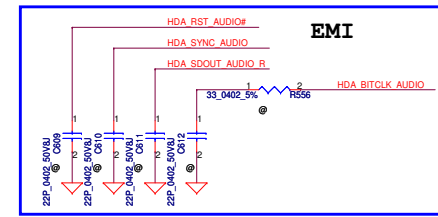


ODD Power Control

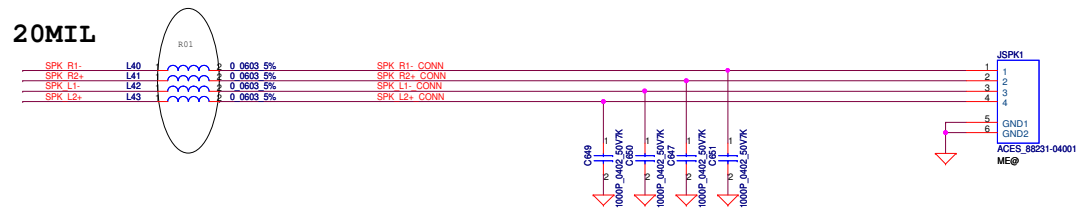


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Date:	Tuesday, August 17, 2010	Sheet	38	of 57	

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).

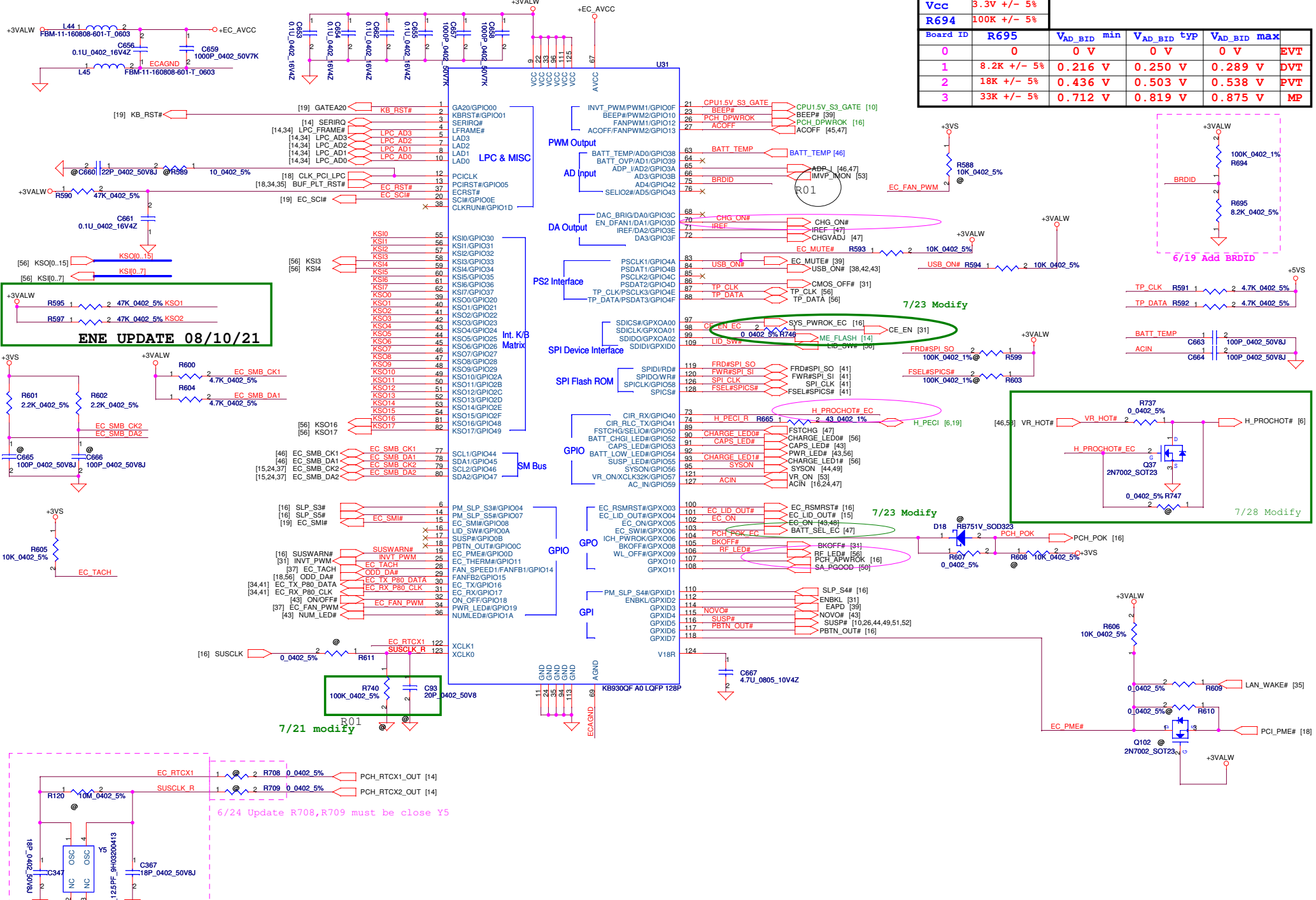


wide 20MIL



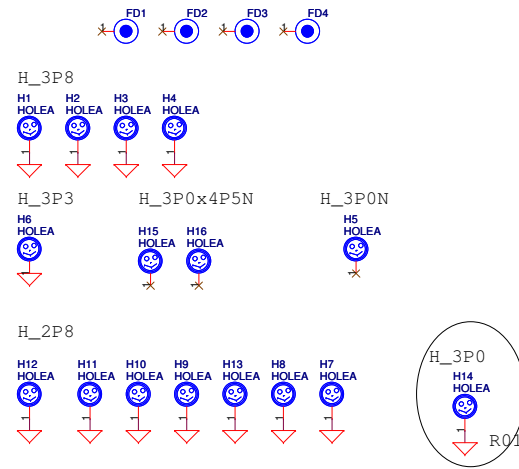
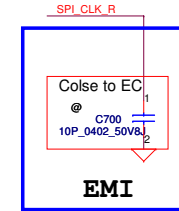
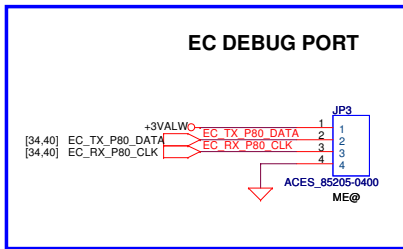
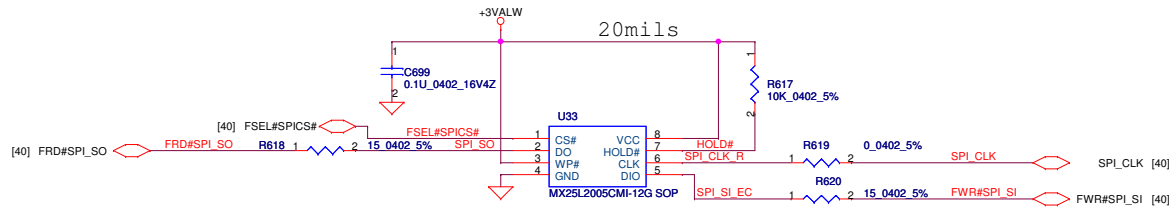
Security Classification	Compal Secret Data	© © © ©		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	CX20671 Codec	
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					LA-6758P
				Date:	Tuesday, August 17, 2010
				Sheet	39 of 57

Vcc	3.3V +/- 5%				
R694	100K +/- 5%	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	
Board ID	R695				
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP



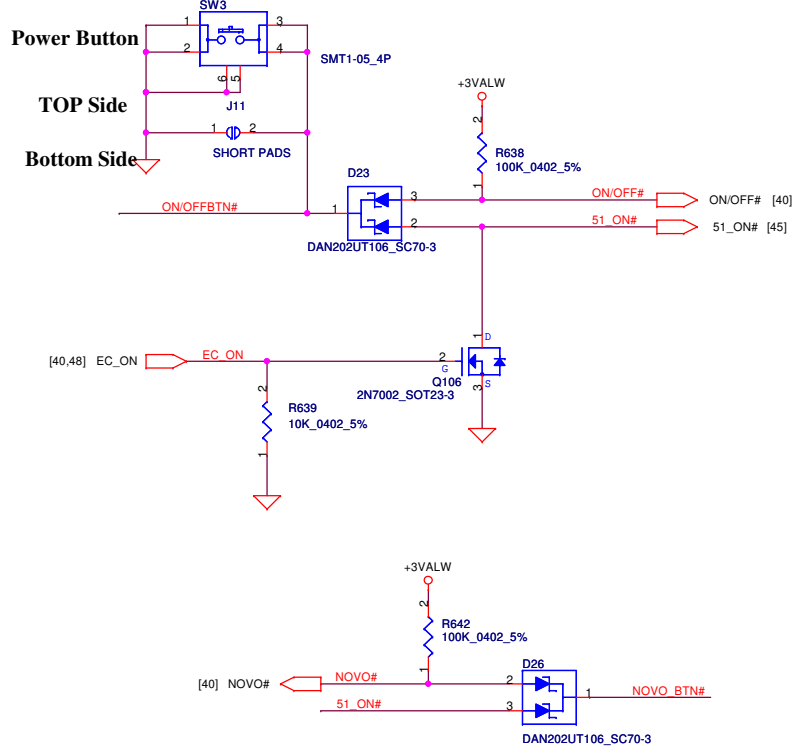
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	BIOS & EC I/O Port	
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<p>Document Number LA-6758P</p>				<p>Rev 0.1</p>	
Date	Tuesday, August 17, 2010	Sheet	40	of 57	

**FOR EC 256KB SPI ROM
(150mil PACKAGE)**

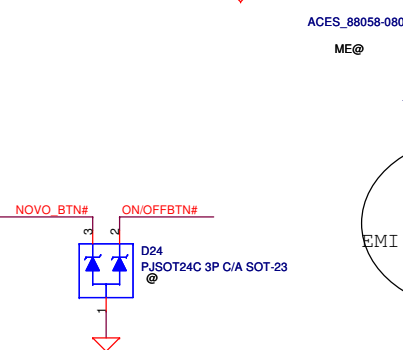
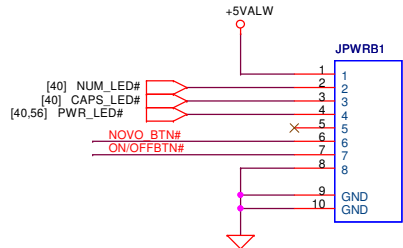


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				LA-6758P
Date: Tuesday, August 17, 2010				Rev 0.1
Sheet 41 of 57				

ON/OFF switch

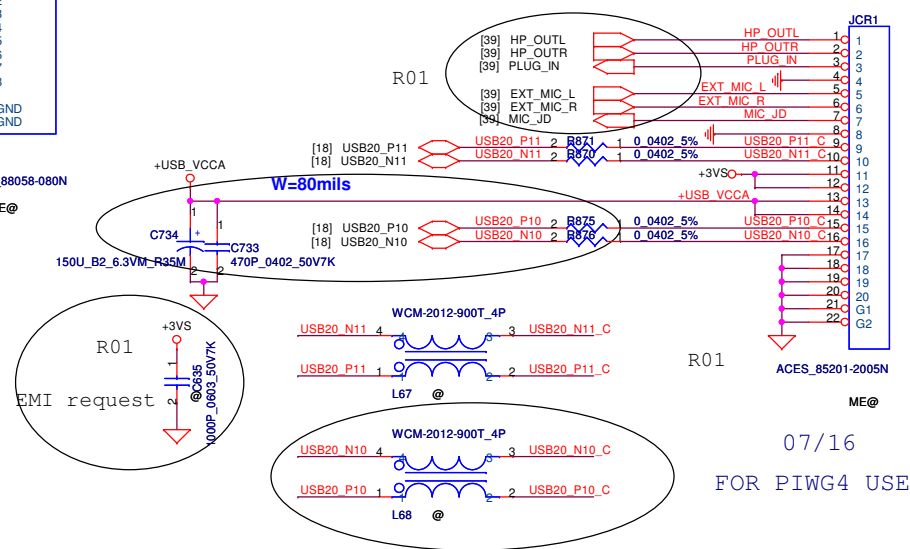


Power Bottom Board Conn. 8pin



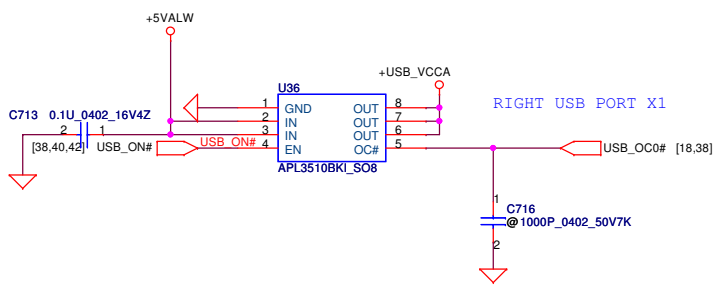
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Card Reader/Audio Jack SB CONN

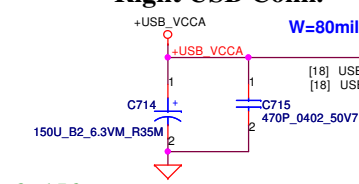


07/16
FOR PIW4 USE

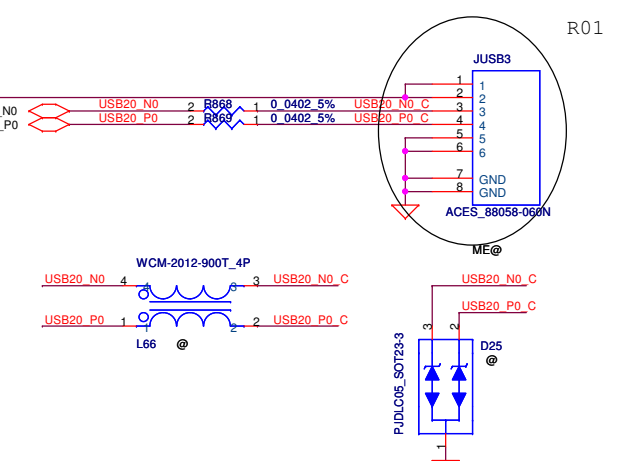
07/16
FOR PIW4 USE



Right USB Conn.

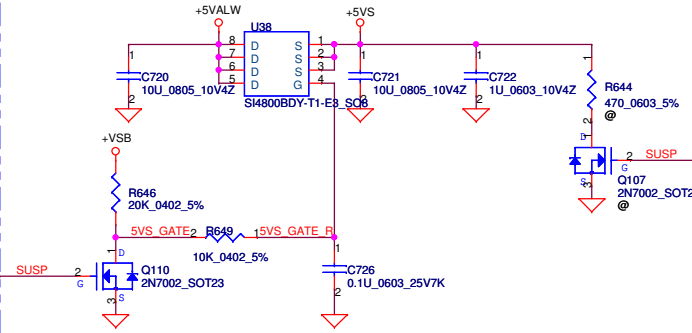


6/9 change to B2 150U
(220uF_6.3V_5.8L_ESR17m) *1=(SF000001500)

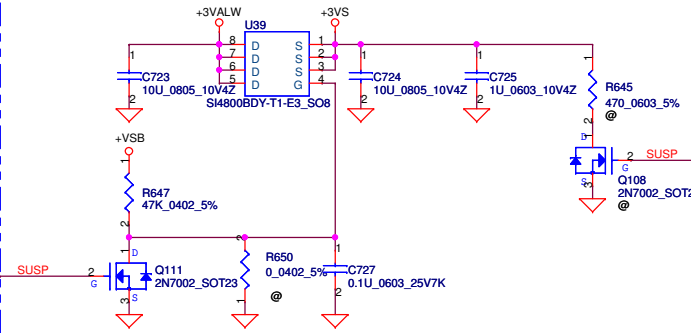


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Size Custom	Document Number	LA-6758P		Rev 0.1
Date:	Tuesday, August 17, 2010	Sheet	43 of 57	

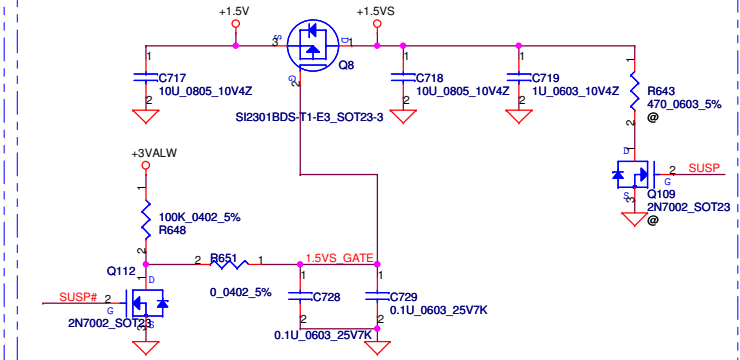
+5VALW TO +5VS



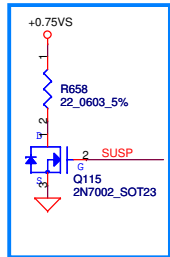
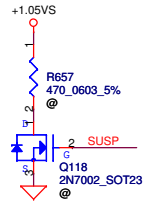
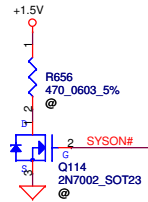
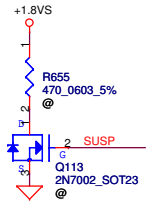
+3VALW TO +3VS



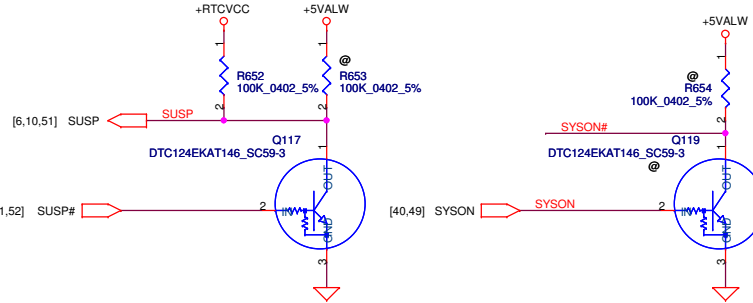
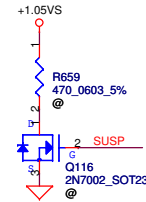
+1.5V to +1.5VS



6/13 change SI4800 to SI2301

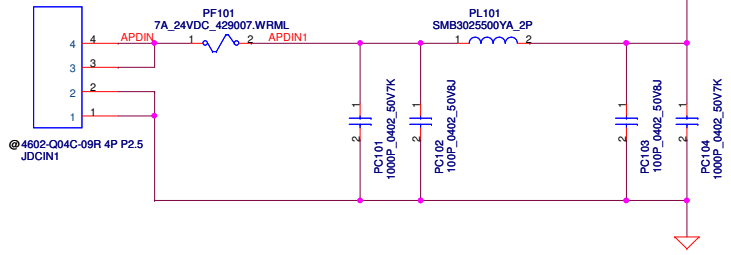


For Intel S3 Power Reduction.

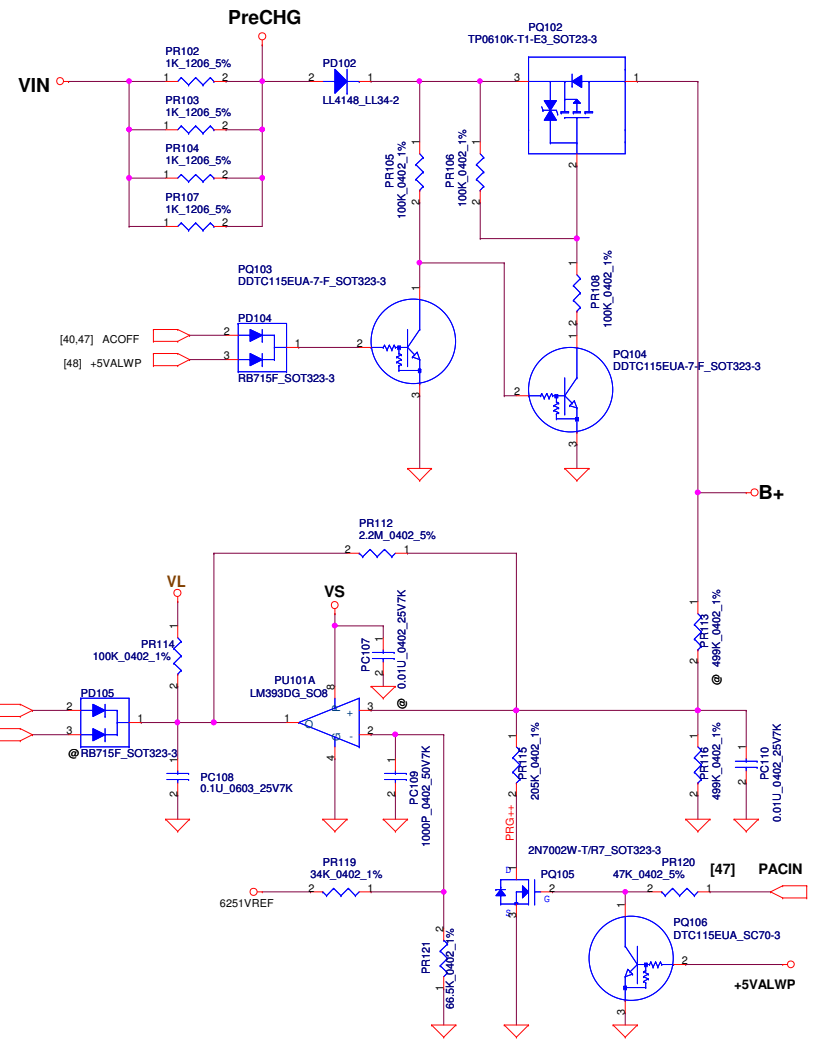


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				LA-6758P	0.1
				Date: Tuesday, August 17, 2010	Sheet 44 of 57

DC030006J00



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**



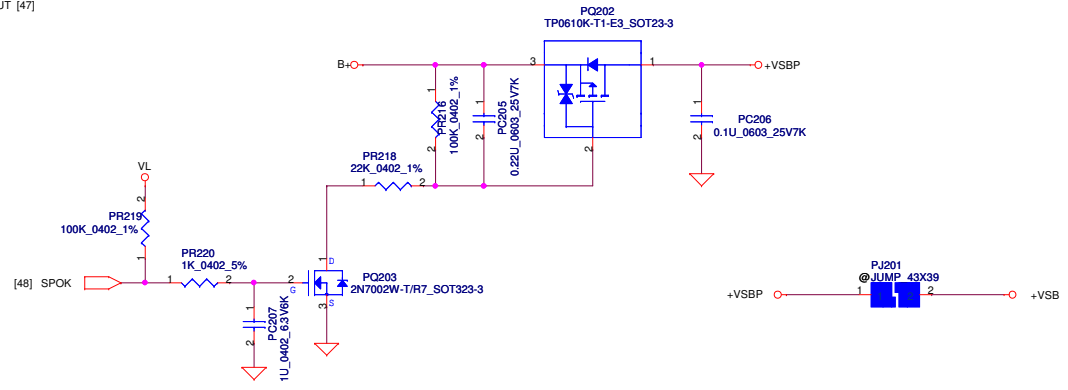
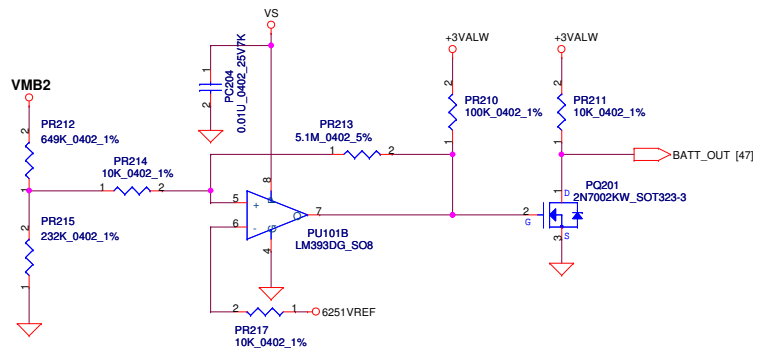
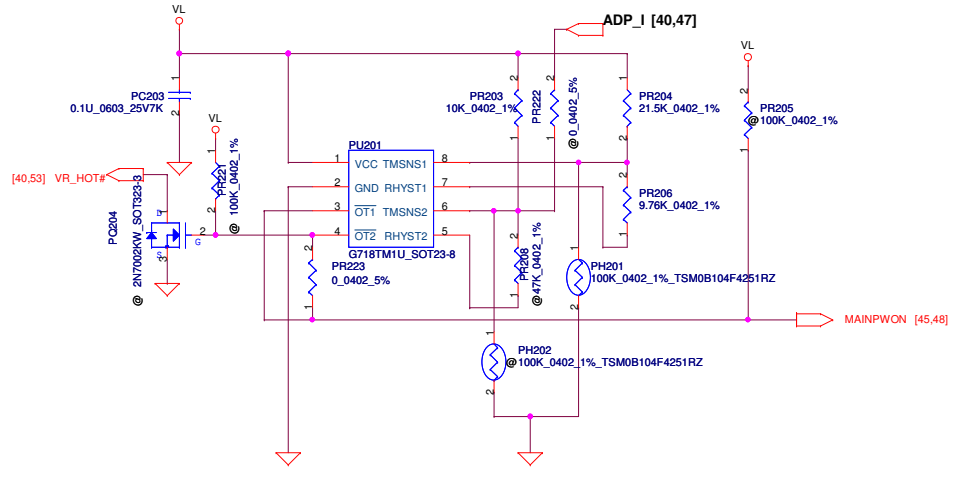
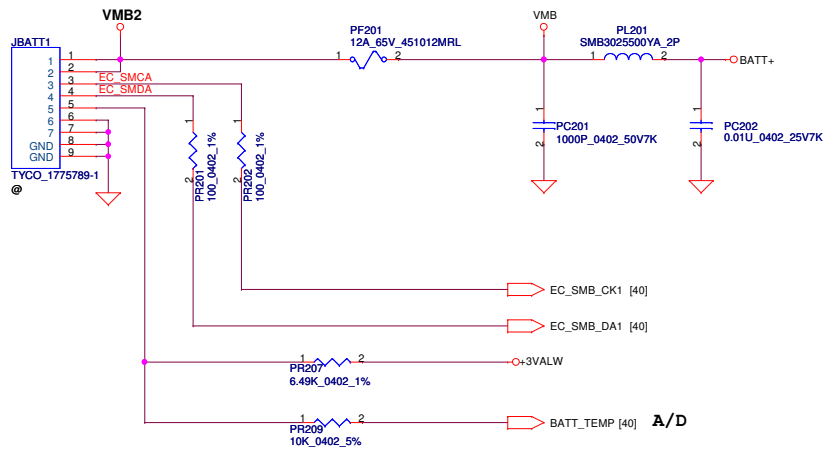
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

PH201 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

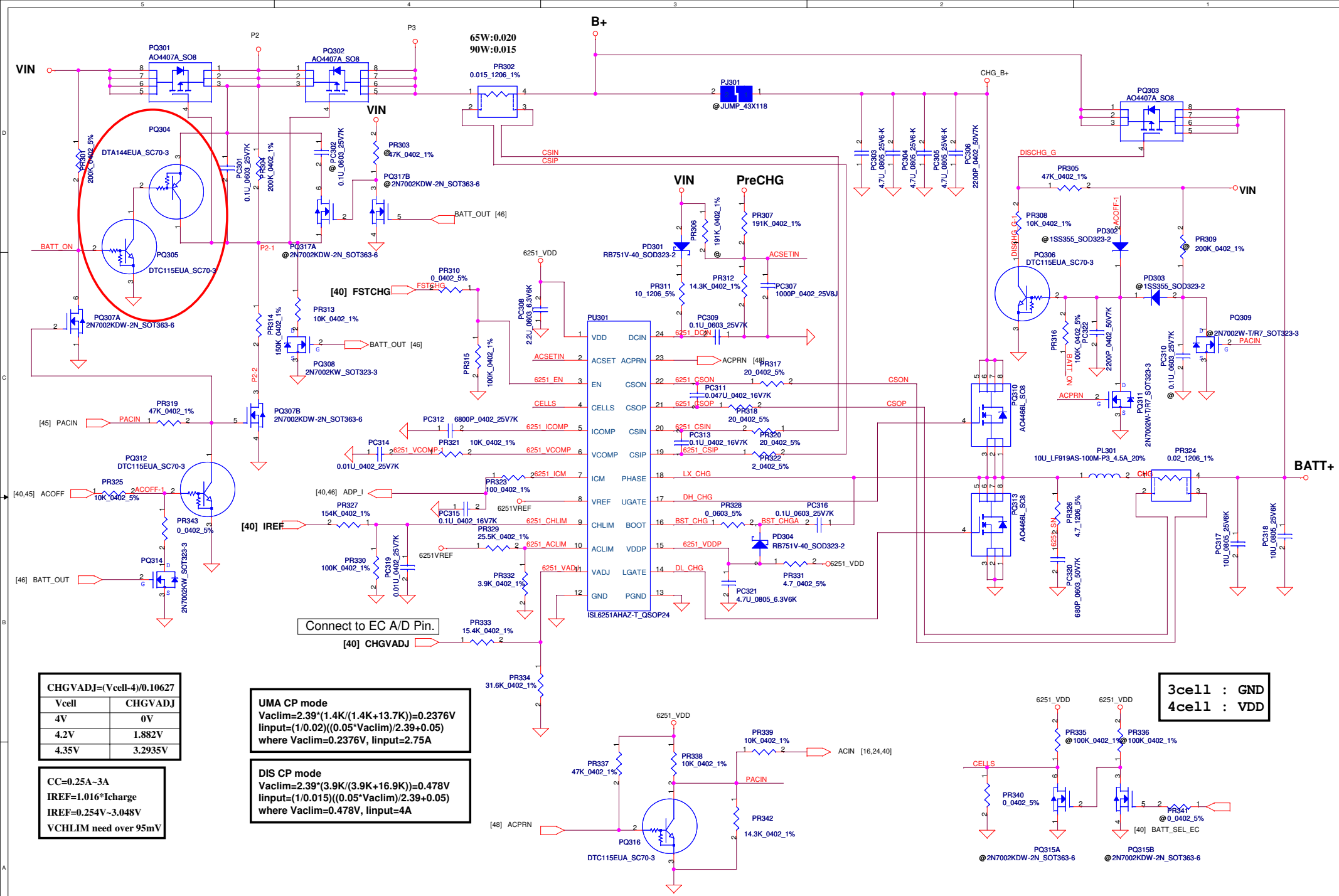


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		2010/12/31

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PWR-BATTERY CONN/OTP

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Document Number
PIWG4
 Date: Tuesday, August 17, 2010 | Sheet 46 of 57



$CHGVADJ = (V_{cell} - 4) / 0.10627$	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

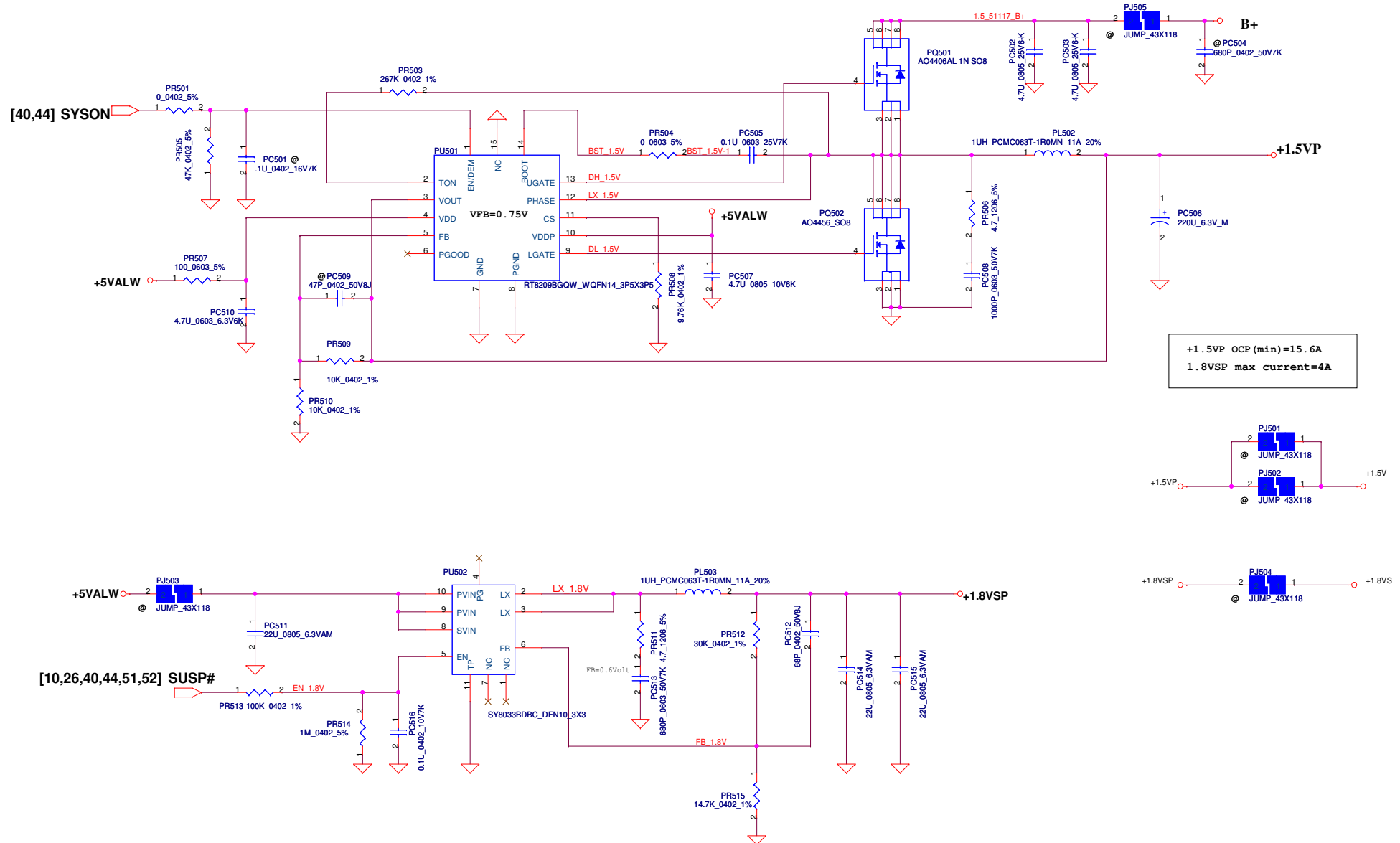
CC=0.25A-3A
 IREF=1.016*I_{charge}
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

UMA CP mode
 $V_{aclip} = 2.39 * (1.4K / (1.4K + 13.7K)) = 0.2376V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 0.2376V$, $I_{input} = 2.75A$

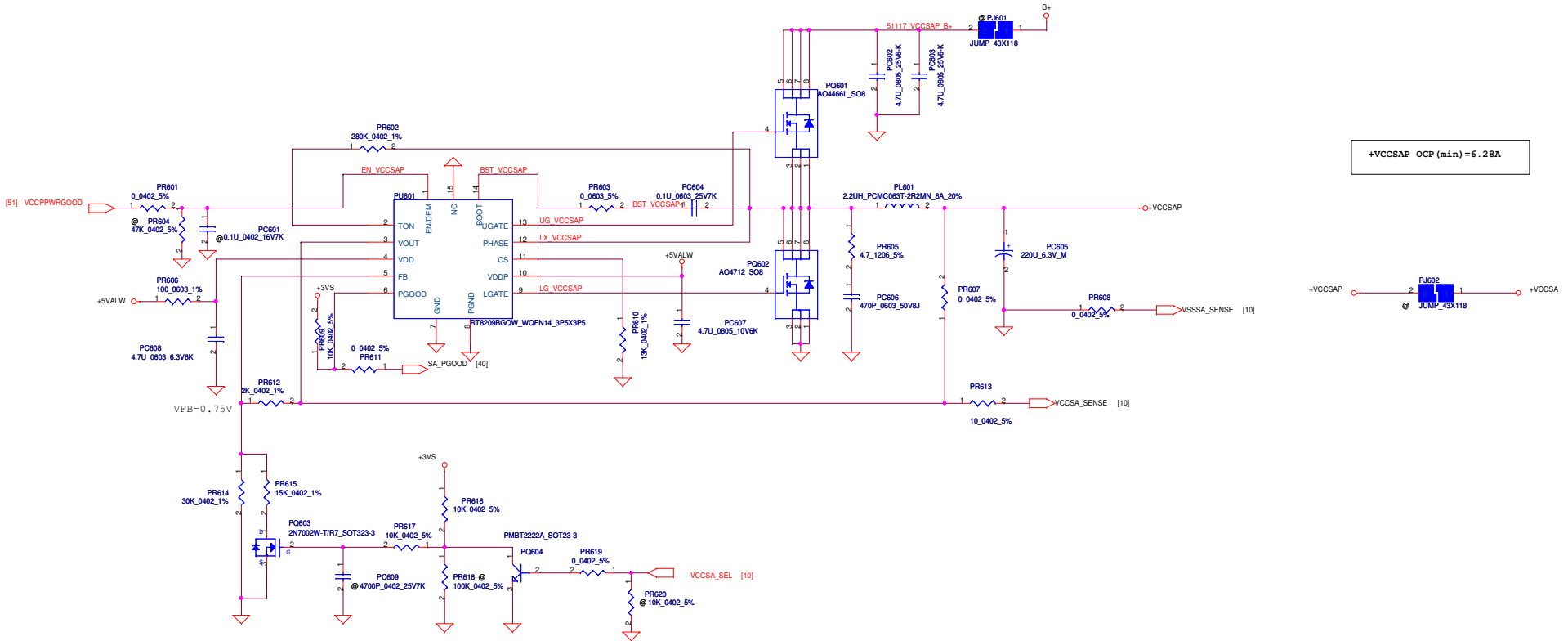
DIS CP mode
 $V_{aclip} = 2.39 * (3.9K / (3.9K + 16.9K)) = 0.478V$
 $I_{input} = (1/0.015) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 0.478V$, $I_{input} = 4A$

3cell : GND
 4cell : VDD

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Size	Document Number	Date: Tuesday, August 17, 2010		Sheet	47 of 57
				PIWG4	Rev 0.1

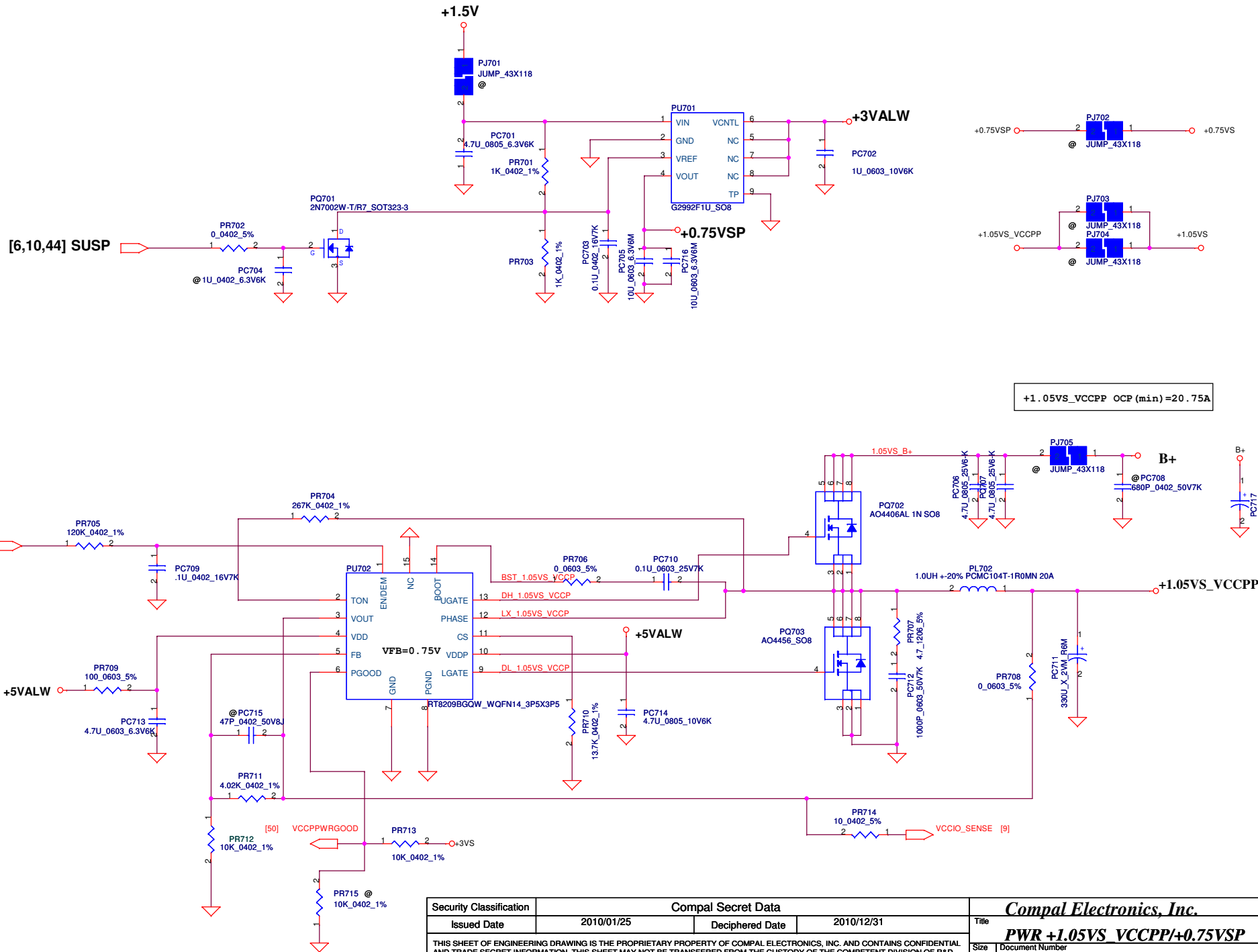


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Size	Custom	Document Number	PIWG4	Rev	0.1
Date:	Tuesday, August 17, 2010	Sheet	49	of	57



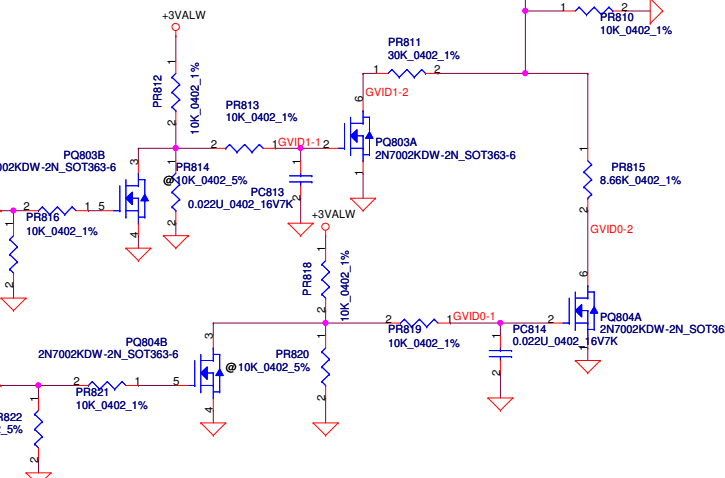
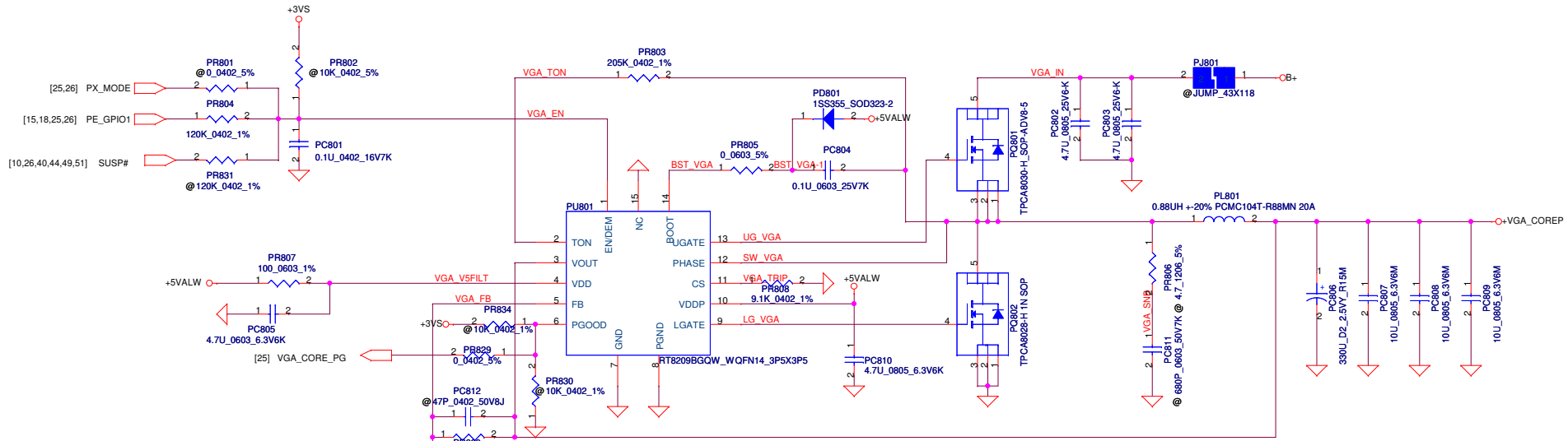
VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	Yes/Yes
0	1	0.8 V	Yes/Yes	Yes/Yes
1	1	0.75V	No/Yes	No/Yes
1	1	0.65V	No/Yes	No/Yes

Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

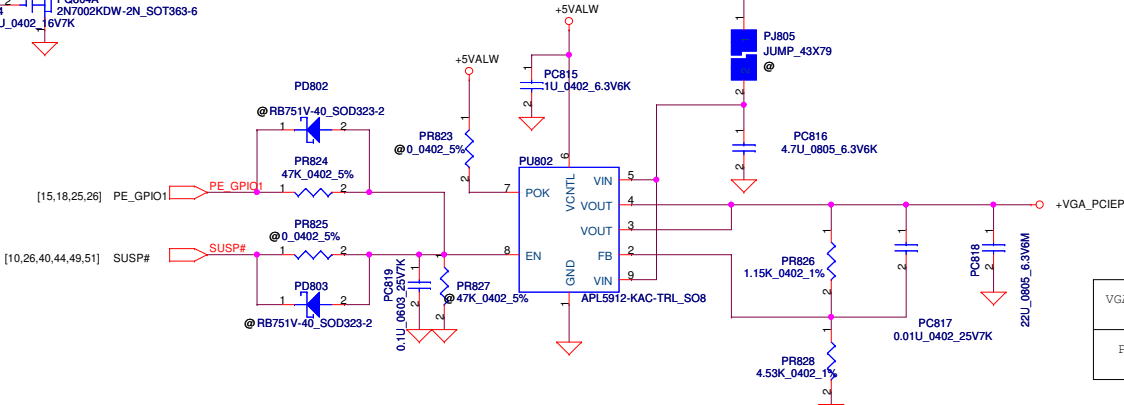
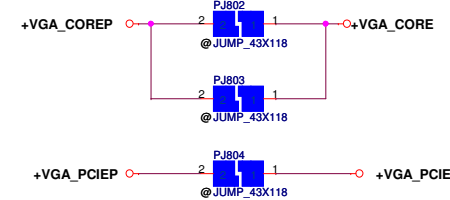


+1.05VS_VCCPP OCP (min)=20.75A

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Date:	Tuesday, August 17, 2010	Sheet	51	of	57



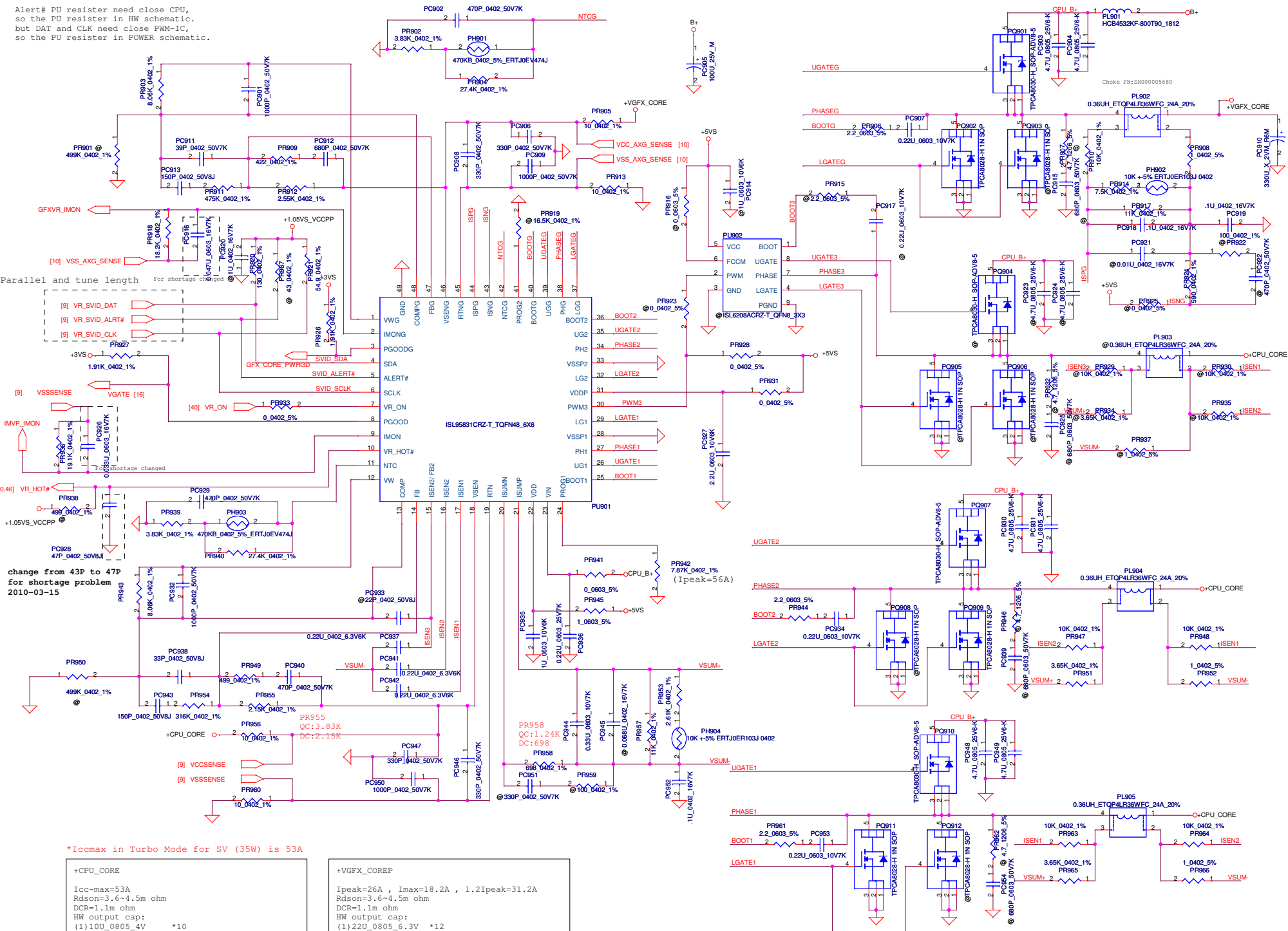
VGA_PWRSEL0	VGA_PWRSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V



VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K

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				VGA_CORE/PCIE
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Date:	Tuesday, August 17, 2010	Sheet	52	of 57

Alert# PU resistor need close CPU,
 so the PU resistor in HW schematic.
 but DAT and CLK need close PWM-IC,
 so the PU resistor in POWER schematic.



*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE
 Icc-max=53A
 Rds-on=3.6-4.5m ohm
 DCR=1.1m ohm
 HW output cap:
 (1) 10U_0805_4V *10
 (2) 22U_0805_6.3V *15
 (3) 470U_D2_2V *4 (ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP
 Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
 Rds-on=3.6-4.5m ohm
 DCR=1.1m ohm
 HW output cap:
 (1) 22U_0805_6.3V *12
 (2) 470U_D2_2V *2 (ESR=4.5m ohm)

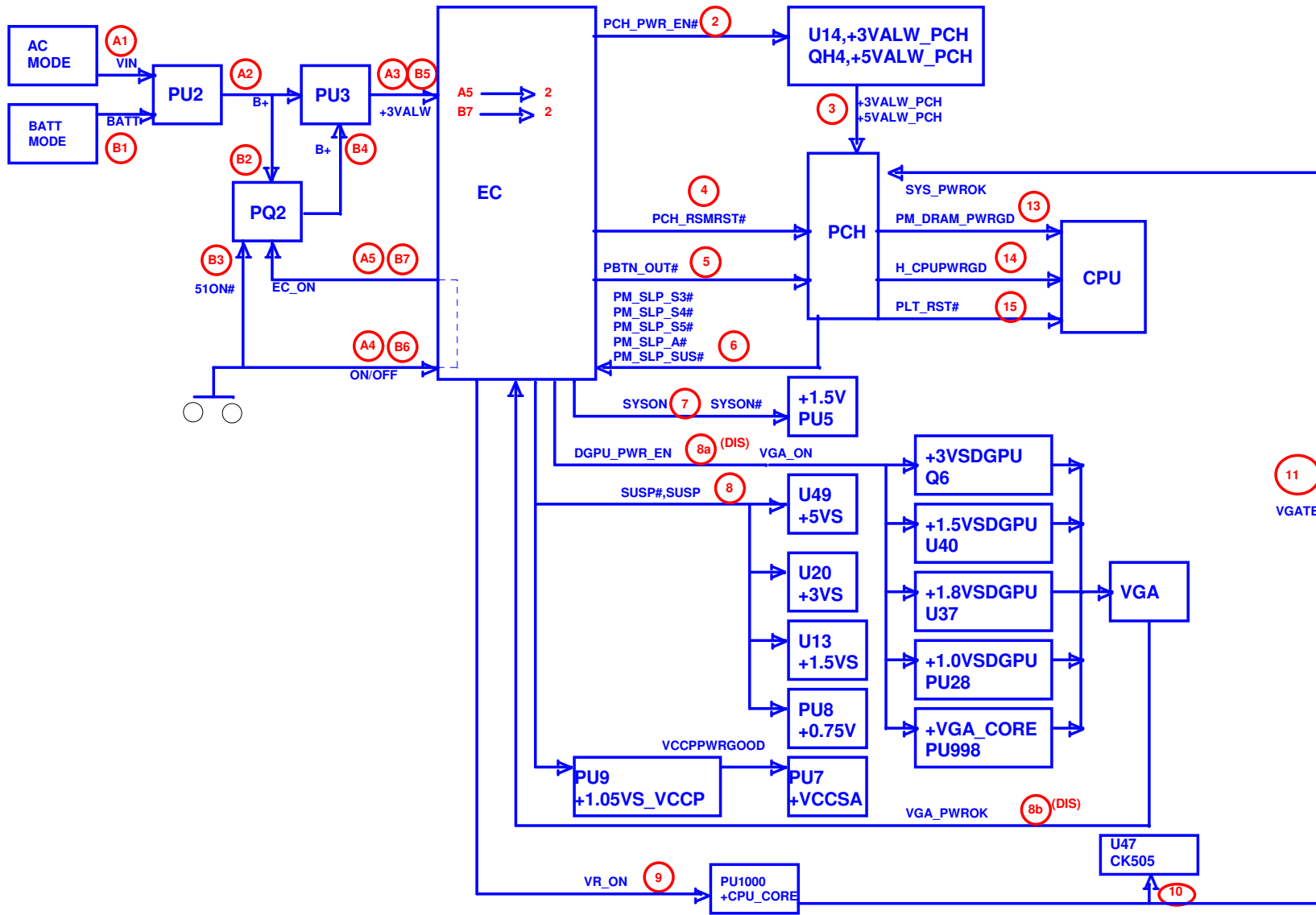
*OCP setting value=37A

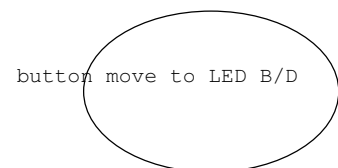
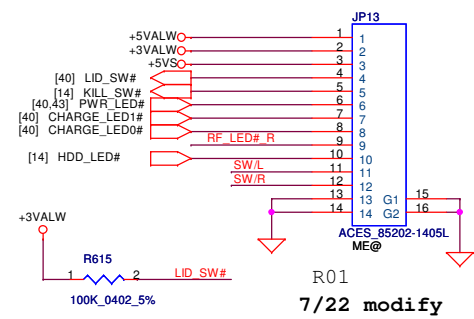
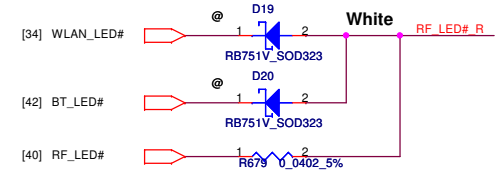
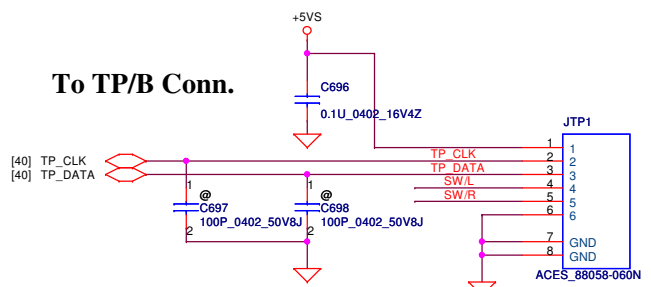
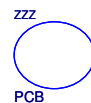
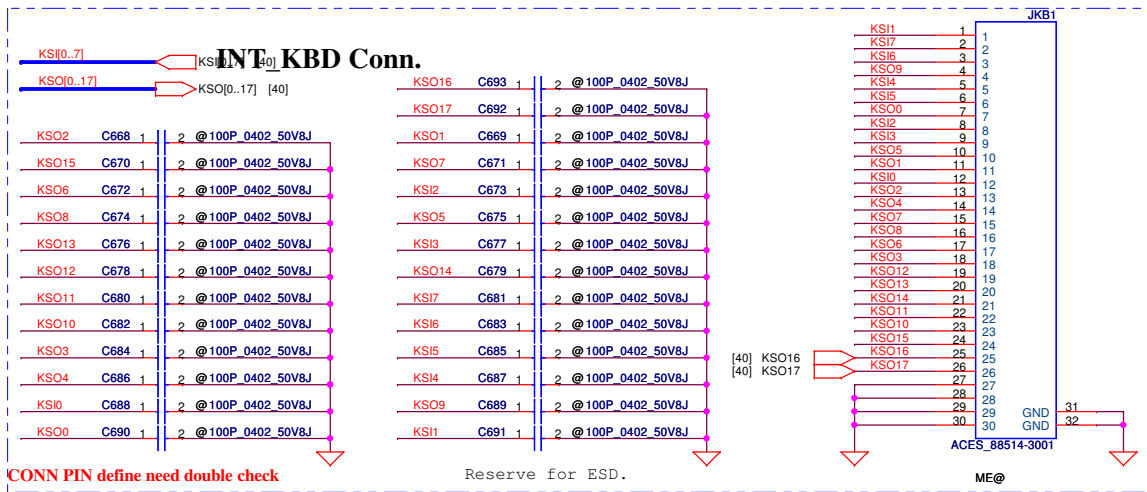
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PWR +CPU_CORE/+VGFX_CORE	
Document Number	PIWG4
Date:	Tuesday, August 17, 2010
Sheet	53 of 57

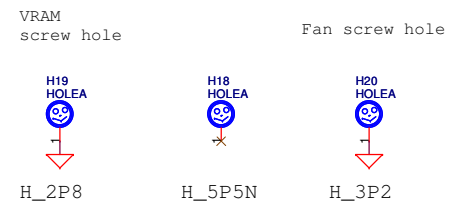
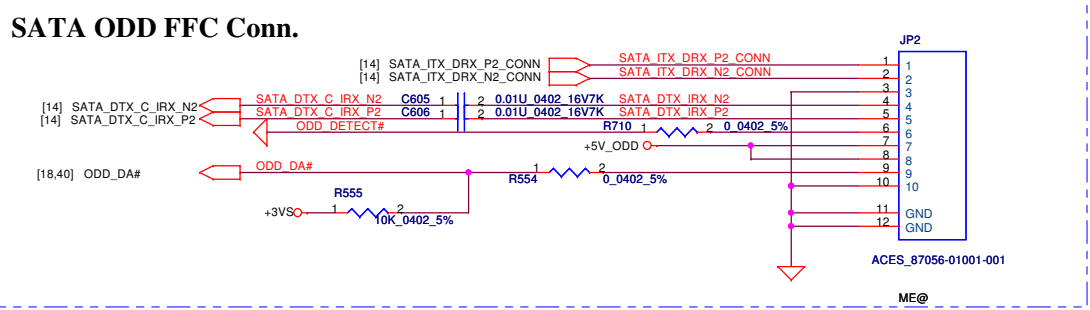
Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
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16					
17					

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Date:	Tuesday, August 17, 2010	Sheet	54	of	57
Rev	0.1				





CONN PIN define need double check



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Size	Document Number			Rev	
B	LA-6758P			0.1	
Date:	Tuesday, August 17, 2010	Sheet	56	of 57	

PHASE	PAGE	Modification list	PURPOSE
0.2	P31	Change CRT Symbol	For CRT footprint issue
0.2	P31	Del C510	For Non-used part
0.2	P39	change C610 pin 1 net name	change C610 pin 1 net name to correct
0.2	P35	U25 change to U26	For co-lay 10/100 and GIGA
0.2	P32	Add R735,R736	For DIS only SMBus pull high
0.2	P33	Add R738,R739	For DIS only SMBus pull high
0.2	P33	Change Q63 BOM structure to HDMI@	For DIS HDMI function
0.2	P40	Add R740, C93	For EC request
0.2	P18	Change R215 pin1 net name	Change R215 pin1 net name to correct
0.2	P18	Add R741	Add R741 for Reserved PE_GPIO0
0.2	P16	Add R742, R743	For PCH power sequence
0.2	P38	Del U28, R542-R551, J12	Del USB charger circuit
0.2	P40	Add EC pin 97,98,I03	Add EC pin 97 for SYS_PWROK_EC, pin 98 for CE_EN, pin 103 For BATT_SEL_EC
0.2	P24	Change R662 pin 2 net name	Change R662 pin 2 net name to correct
0.2	P28	Del C421,C422,C431,C432,C433, L27, Add R745, U8 pin N11,N12 change to NC	For AMD new document suggestion
0.2	P26	Add R744	Add R744 for control PE_GPIO1 from SUSP#
0.2	P39	Change J10 footprint and Add J13	Change J10 footprint by Dfx request and Add J13 by vendor suggestion
0.2	P39	Change PC_Beep circuit	Change PC_Beep circuit
0.2	P6	Add R161, R182, R192 BOM structure hange to @	Follow ORB circuit
0.2	P58/59	Add R615 in 15" and 17" page	Pull high LID_SW# at M/B side
0.2	P31	Add Q83 pin 1 power net name +CMOS_PW	For power trace net
0.2	P56/57/58	Change JP21 to JKBI	Change connector to standard name
0.2	P56/57/58	Change JP4 to JTP1	Change connector to standard name
0.2	P43/60	Change JP6 to JPPWRBI	Change connector to standard name
0.2	P34	Change JP1 to JWLNI	Change connector to standard name
0.2	P42	Change JP5 to JBTI	Change connector to standard name
0.2	P43/60	Change JP7 to JCRI	Change connector to standard name
0.2	P19	Add R542	For ESATA detect function
0.2	P42	Add R886, R887, C735	For ESATA detect function
0.2	P31	Add R543	For reserve EC control directly
0.2	P39	Change J10 footprint, Del C635, C636	Change J10 for Dfx and Del component for layout
0.2	P42	Add R877	For reserve EC control directly
0.2	P42	SW3 BOM structure change to @	For ME ASSY concern
0.2	P24	R324 BOM structure change, del @	For AMD update
0.2	P25	Change Q69,Q70,Q71,Q72 to BSS138, change Q66,Q67 pin 1 net name, D28 change to @	For Change BACO part follow AMD reference DATA ,D28 change to @ for leakage
0.2	P42	Change ESATA from port 5 to port 4	For intel risk
0.2	P15	Add R544,R545	For Pull high SMBus
0.2	P12/13	Del R74-R80,R82 R88-R94,R96	For DDR3 DM Bus to GND
0.2	P16	Add R182,R546	Add 186 for reserve sequence, Add R546 for follow CRB & ORB
0.2	P20	Del Add J12, R257 change to @	For voltage drop

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				Date	
				Sheet	57 of 57