

# KIWA5/A6

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM/PM+ICH9-M core logic

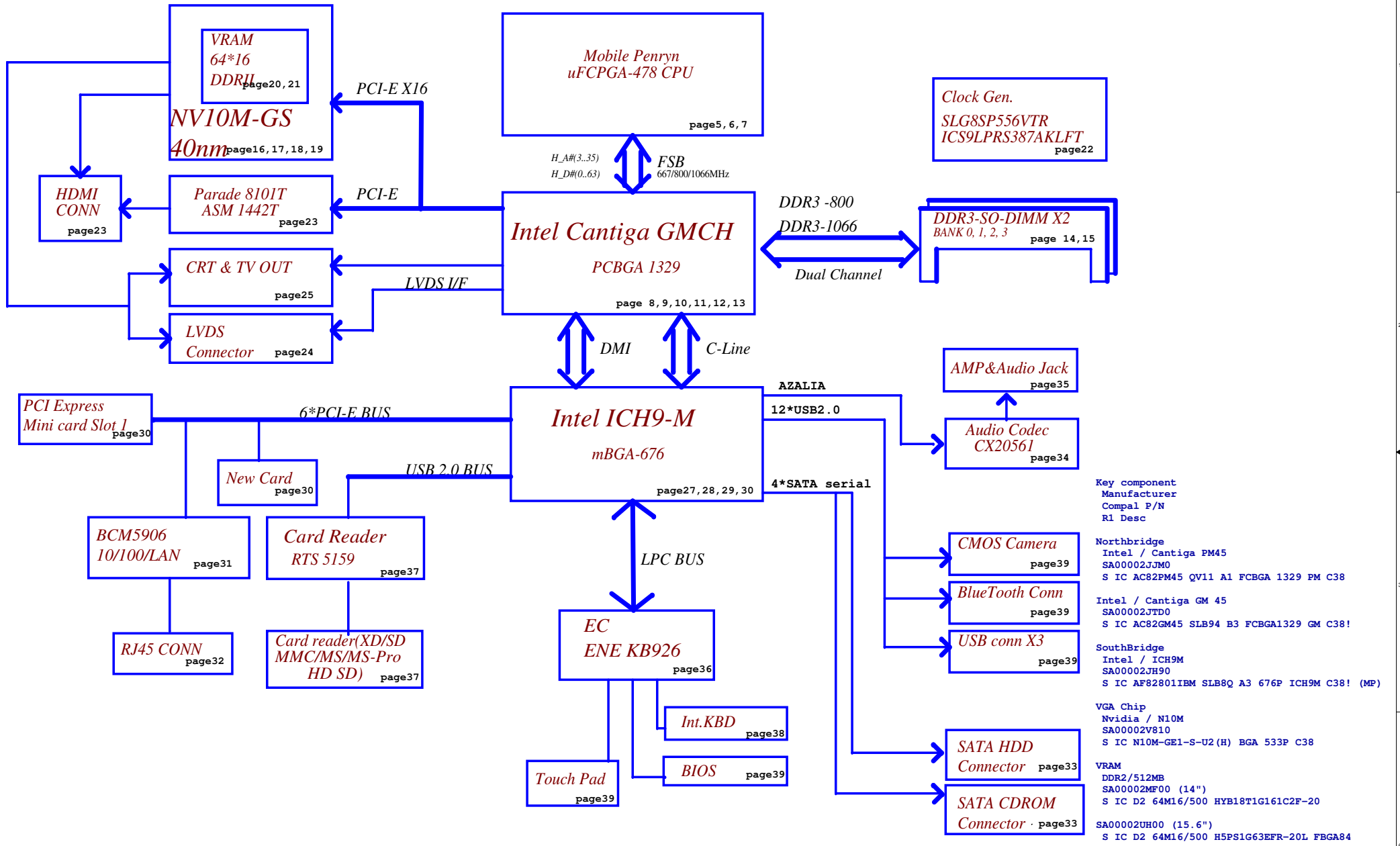
REV: 1.0

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**POWER Board**

**CAP SENSE LEDs Board**



- Key component  
 Manufacturer  
 Compal P/N  
 R1 Desc
- Northbridge  
 Intel / Cantiga PM45  
 SA00002JJM0  
 S IC AC82PM45 QV11 A1 FCBGA 1329 PM C38
  - Intel / Cantiga GM 45  
 SA00002JTD0  
 S IC AC82GM45 SLB94 B3 FCBGA1329 GM C38!
  - SouthBridge  
 Intel / ICH9M  
 SA00002JH90  
 S IC AF82801IBM SLB8Q A3 676P ICH9M C38! (MP)
  - VGA Chip  
 Nvidia / N10M  
 SA00002V810  
 S IC N10M-GE1-S-U2(H) BGA 533P C38
  - VRAM  
 DDR2/512MB  
 SA00002MF00 (14")  
 S IC D2 64M16/500 HYB18T1G161C2F-20  
 SA00002UH00 (15.6")  
 S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

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Custor	KIWAX_LA-5081P	1.0				

# DDR3 Voltage Rails

power plane State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS <b>+0.75VS</b> +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCLK VGA_DDCDATA	N10M	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	N10M	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT (55nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	N10M	X	X	X	V	X	X	X	X	X	X	X	X	X
IFPC_AUX IFPC_AUX_N (40nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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# VGA and DDR2 Voltage Rails (N10M)

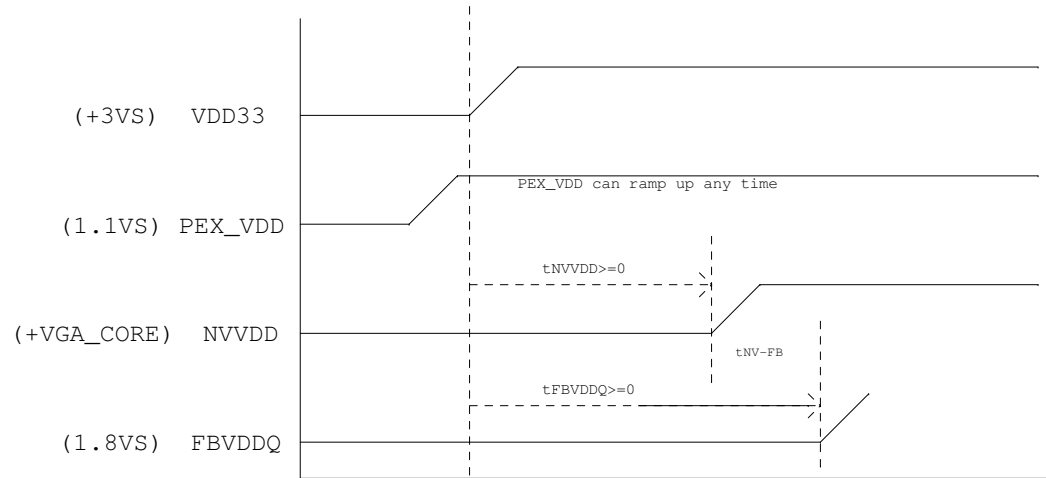
power plane	+3VS
	+VGA_CORE
State	+1.1VS
	+1.8VS
S0	○
S1	○
S3	✗
S5 S4/AC	✗
S5 S4/ Battery only	✗
S5 S4/AC & Battery don't exist	✗

# EDP at Tj = 97C\*

Power Supply Rail (V)		NB10M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
<b>TOTAL</b>	<b>1.1</b>	<b>3.425A</b>		<b>2.435A</b>	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
<b>TOTAL</b>	<b>1.8</b>	<b>2.76A</b>	<b>2.17A</b>	<b>2.575A</b>	<b>2.085A</b>
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
<b>TOTAL</b>	<b>3.3</b>	<b>0.445A</b>		<b>0.445A</b>	

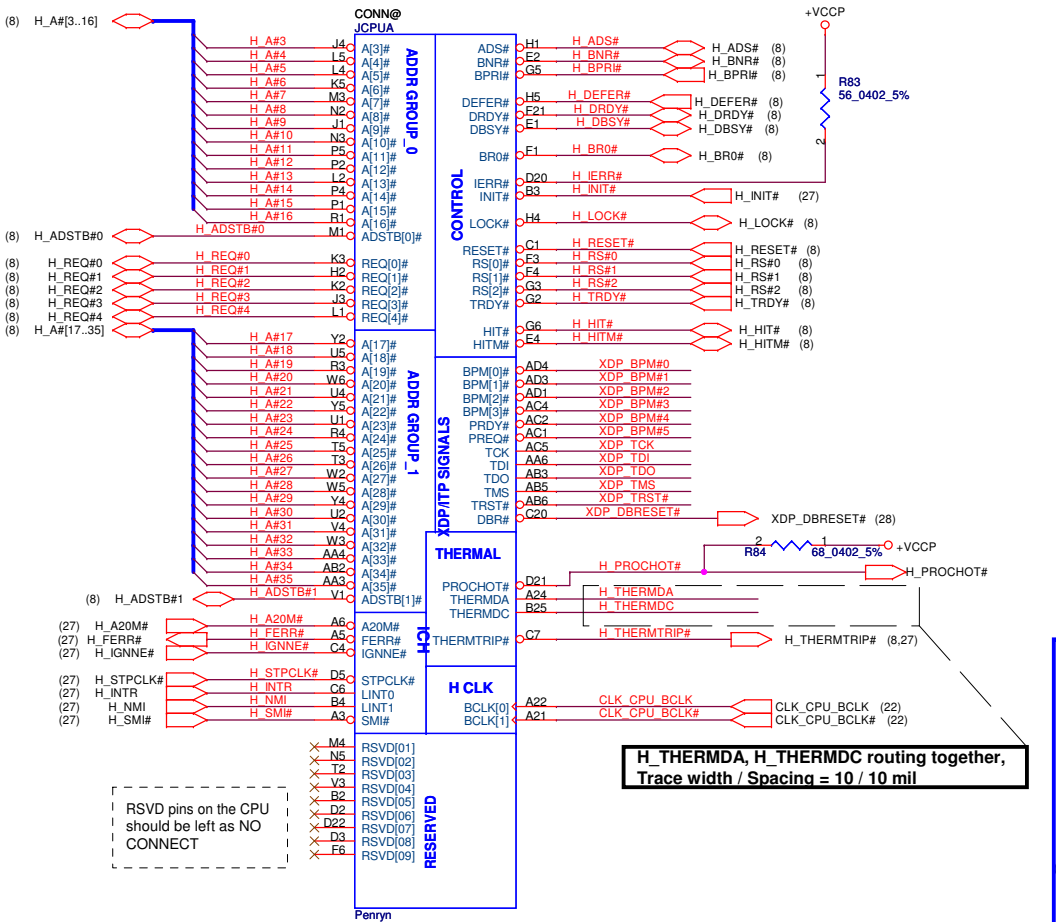
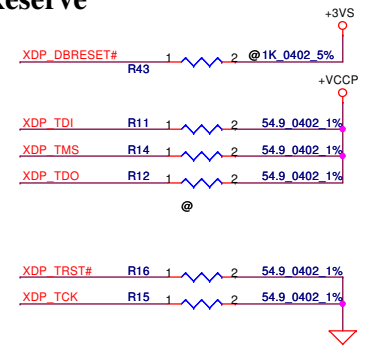
## POWER SEQUENCE

The ramp time for any rail must be more than 40us

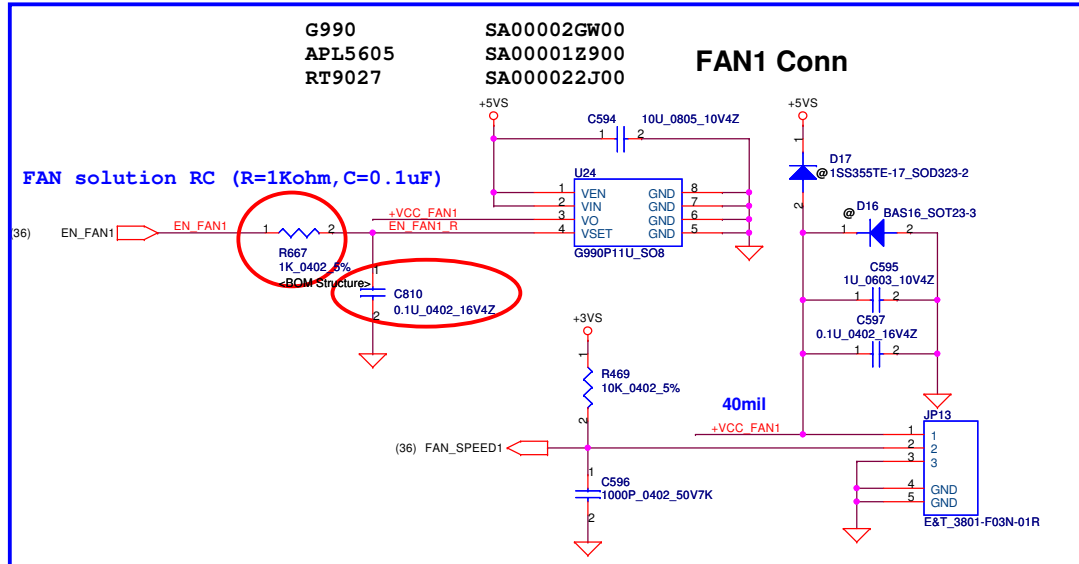
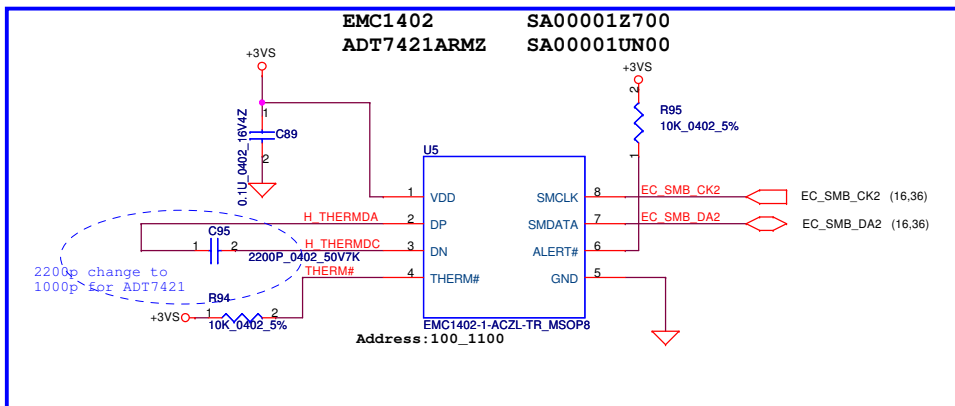


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# XDP Reserve

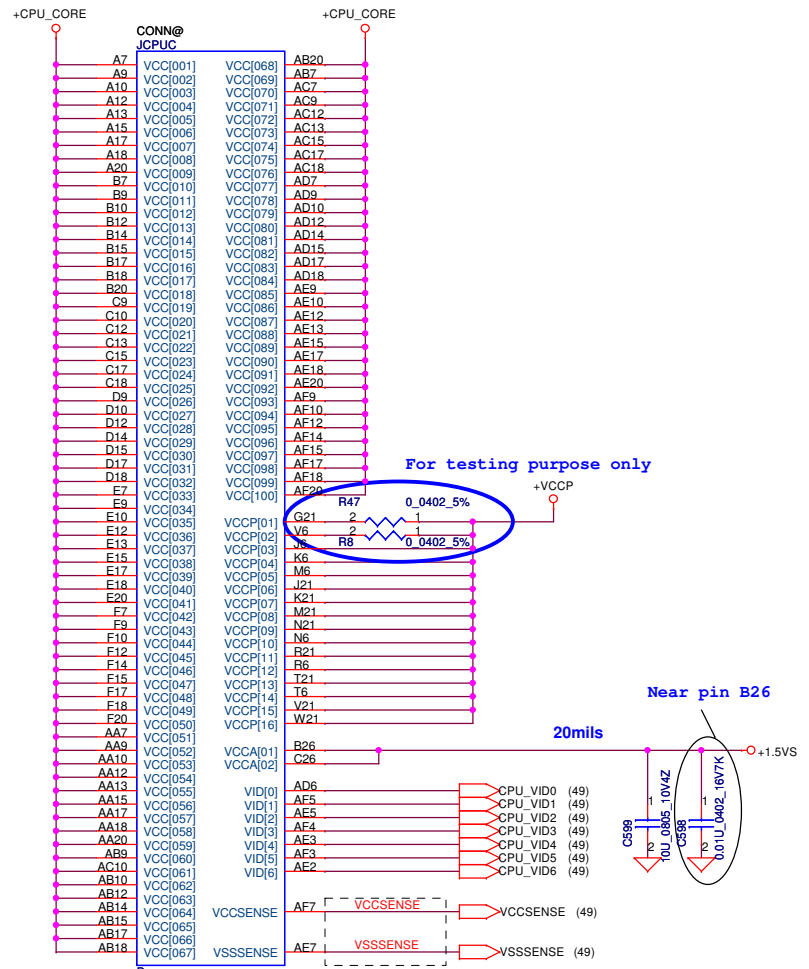
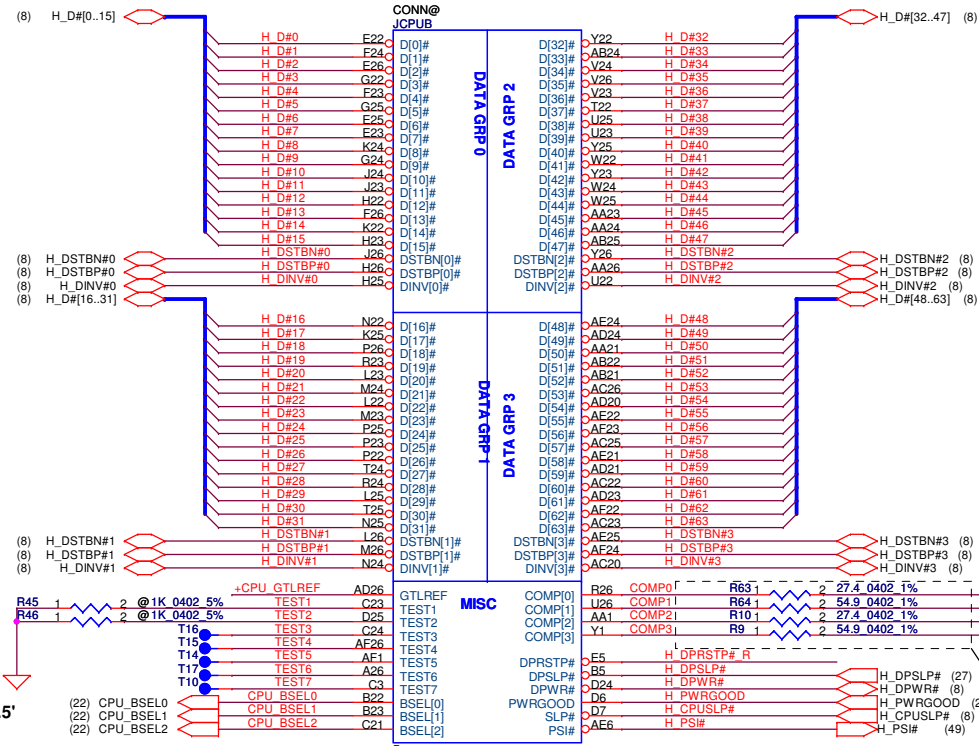


**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**



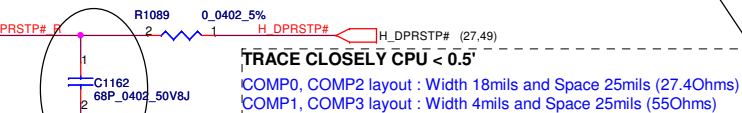
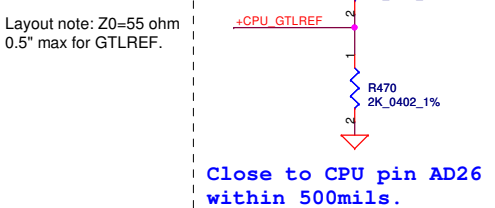
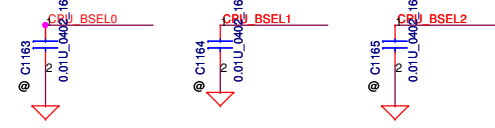
RSVD pins on the CPU should be left as NO CONNECT

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Trace Close CPU < 0.5'

Width=4 mil ,  
Spacing: 15mil  
(55Ohms)

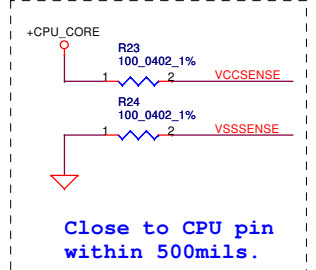


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

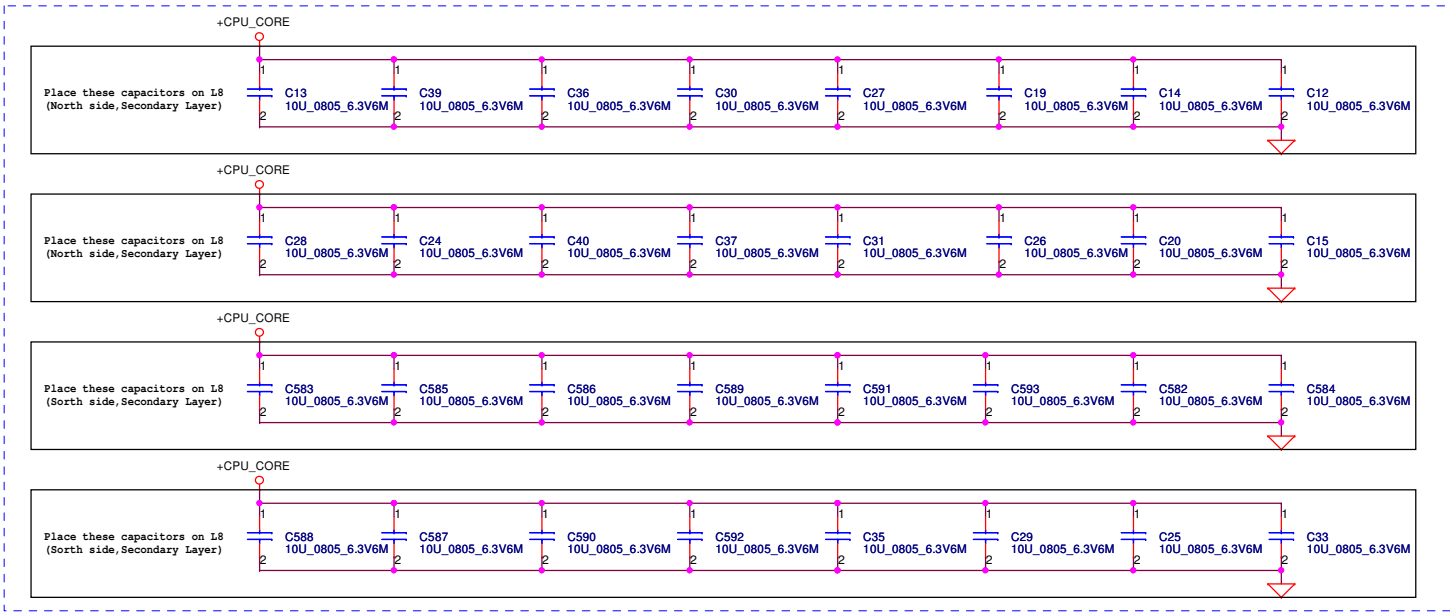
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.  
The trace width/space/other is 16/7/25.

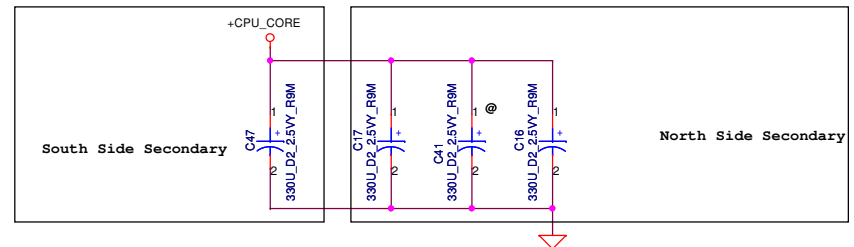
Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.



CONN@	JCPU@	VSS@	P6
A4	VSS001	VSS082	P6
A8	VSS002	VSS083	P21
A11	VSS003	VSS084	P24
A14	VSS004	VSS085	R2
A16	VSS005	VSS086	R5
A19	VSS006	VSS087	R22
A23	VSS007	VSS088	R25
AF2	VSS008	VSS089	T1
B8	VSS009	VSS090	T4
B11	VSS010	VSS091	T23
B13	VSS011	VSS092	T26
B16	VSS012	VSS093	U3
B19	VSS013	VSS094	U6
B21	VSS014	VSS095	U21
B24	VSS015	VSS096	U24
C5	VSS016	VSS097	V2
C8	VSS017	VSS098	V5
C11	VSS018	VSS099	V22
C14	VSS019	VSS100	V25
C16	VSS020	VSS101	W1
C19	VSS021	VSS102	W4
C2	VSS022	VSS103	W23
C22	VSS023	VSS104	W26
C25	VSS024	VSS105	Y3
D1	VSS025	VSS106	Y6
D4	VSS026	VSS107	Y21
D8	VSS027	VSS108	Y24
D11	VSS028	VSS109	AA2
D13	VSS029	VSS110	AA5
D16	VSS030	VSS111	AA8
D19	VSS031	VSS112	AA11
D23	VSS032	VSS113	AA14
D26	VSS033	VSS114	AA19
E3	VSS034	VSS115	AA22
E6	VSS035	VSS116	AA25
E8	VSS036	VSS117	AB1
E11	VSS037	VSS118	AB4
E14	VSS038	VSS119	AB8
E16	VSS039	VSS120	AB11
E19	VSS040	VSS121	AB13
E21	VSS041	VSS122	AB16
E24	VSS042	VSS123	AB19
F5	VSS043	VSS124	AB23
F8	VSS044	VSS125	AB26
F11	VSS045	VSS126	AC3
F13	VSS046	VSS127	AC6
F16	VSS047	VSS128	AC8
F19	VSS048	VSS129	AC11
F2	VSS049	VSS130	AC14
F22	VSS050	VSS131	AC16
F25	VSS051	VSS132	AC19
G4	VSS052	VSS133	AC21
G1	VSS053	VSS134	AC24
G23	VSS054	VSS135	AD2
G26	VSS055	VSS136	AD5
H3	VSS056	VSS137	AD8
H6	VSS057	VSS138	AD11
H21	VSS058	VSS139	AD13
H24	VSS059	VSS140	AD16
J2	VSS060	VSS141	AD19
J5	VSS061	VSS142	AD22
J22	VSS062	VSS143	AD25
J25	VSS063	VSS144	AE1
K1	VSS064	VSS145	AE4
K4	VSS065	VSS146	AE8
K23	VSS066	VSS147	AE11
K26	VSS067	VSS148	AE14
L3	VSS068	VSS149	AE16
L6	VSS069	VSS150	AE19
L21	VSS070	VSS151	AE23
L24	VSS071	VSS152	AE26
M2	VSS072	VSS153	A2
M5	VSS073	VSS154	AF6
M22	VSS074	VSS155	AF8
M25	VSS075	VSS156	AF11
N1	VSS076	VSS157	AF13
N4	VSS077	VSS158	AF16
N23	VSS078	VSS159	AF19
N26	VSS079	VSS160	AF21
P3	VSS080	VSS161	A25
	VSS081	VSS162	AF25
		VSS163	

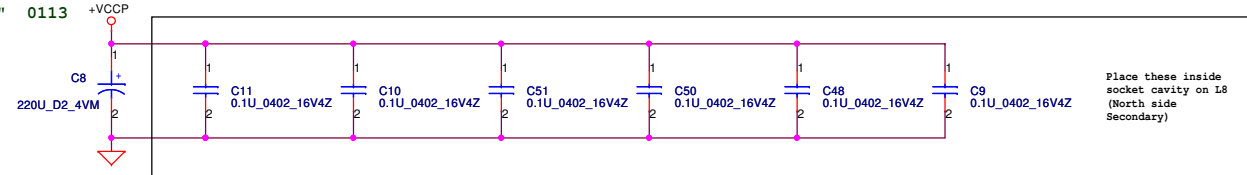


Mid Frequency Decoupling



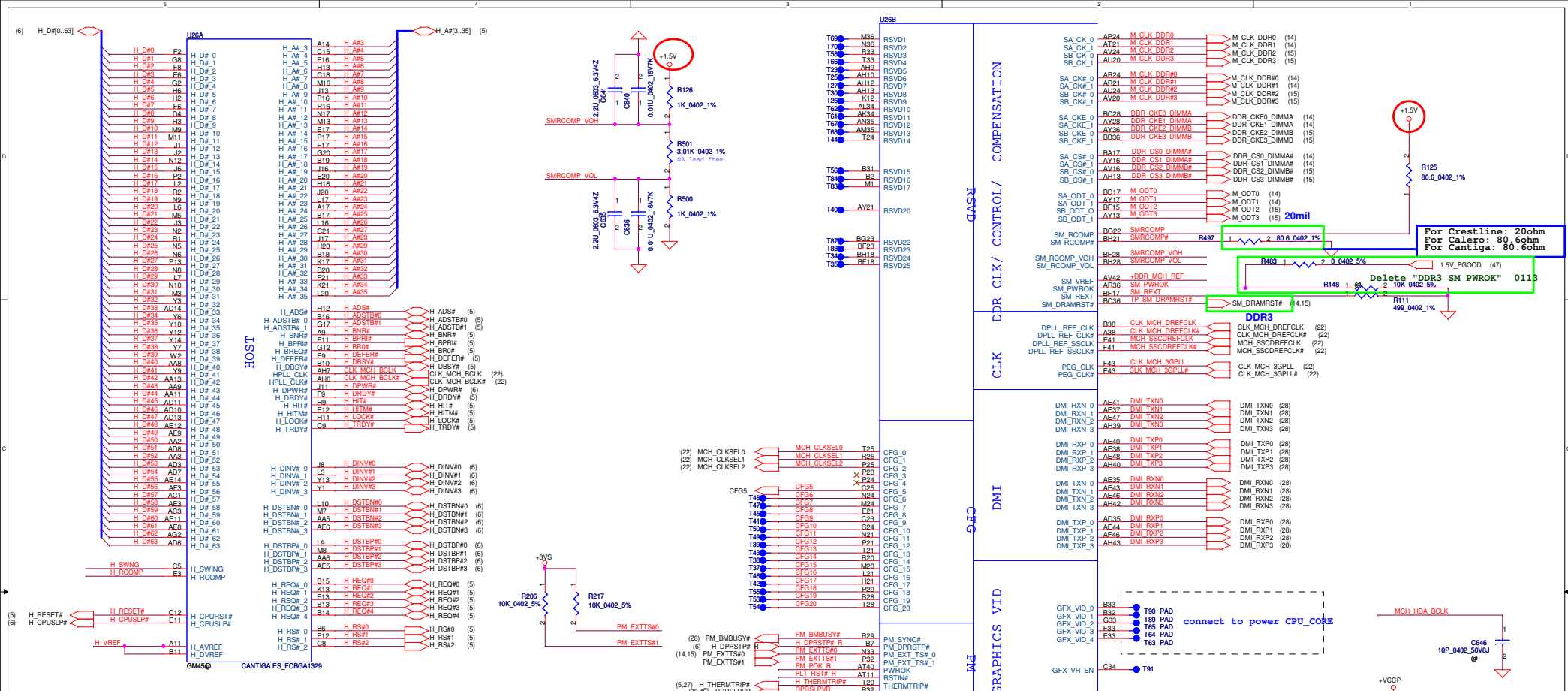
ESR <= 1.5m ohm  
Capacitor > 1980uF

Delete "REMOVE?" 0113



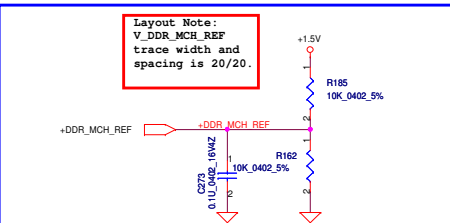
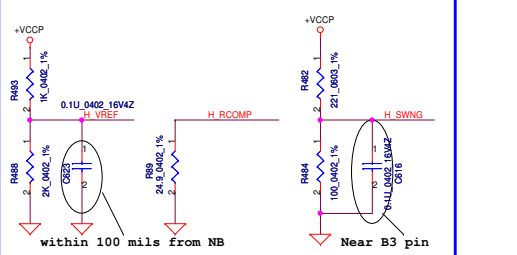
Place these inside  
socket cavity on L8  
(North side  
Secondary)

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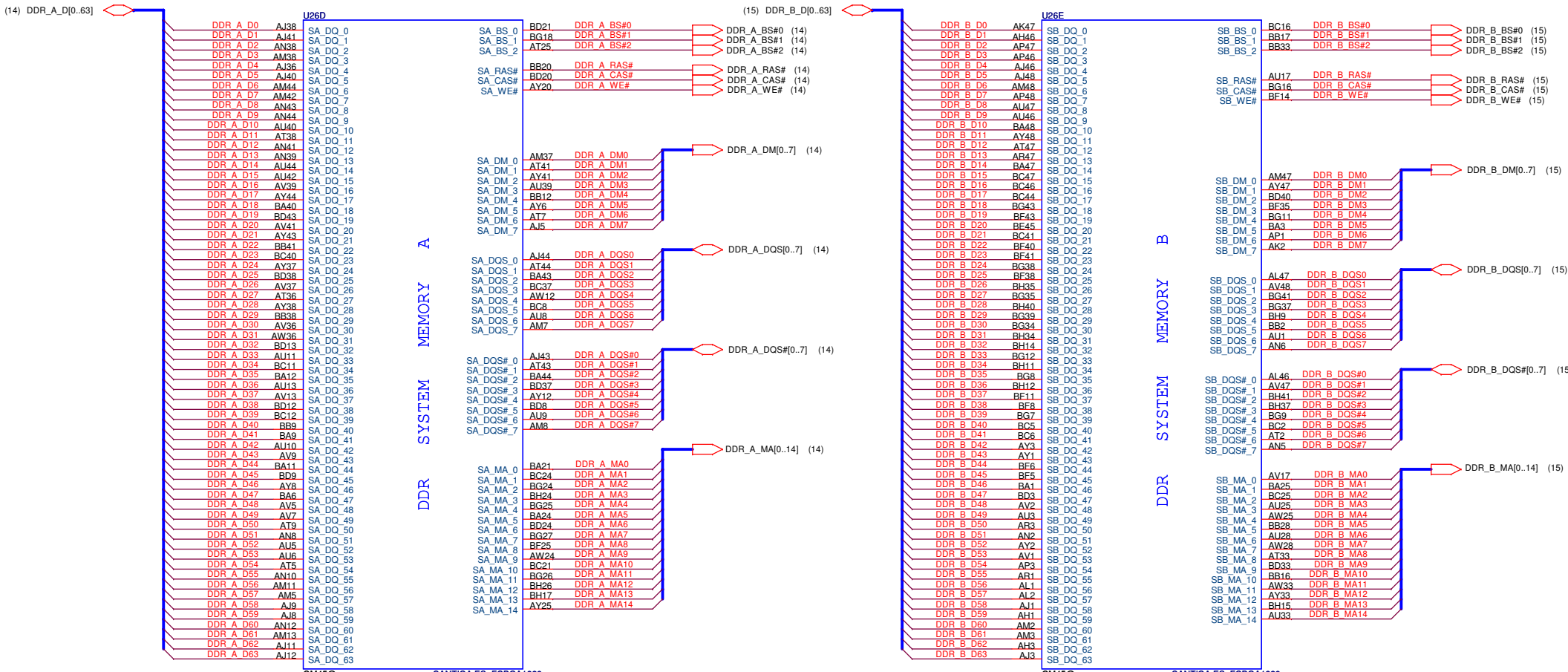


layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width and spacing (55 ohm) same as FSB data traces

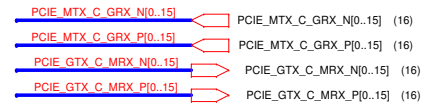
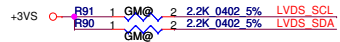
**Layout Note:**  
H\_RCOMP / H\_VREF / H\_SWING  
trace width and spacing is 10/20







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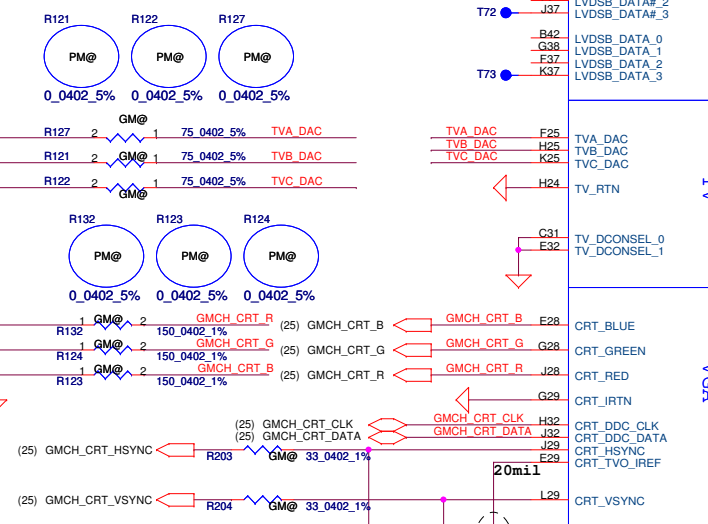


Place the resistor within 500mils (1.27mm) of the (GMCH)  
 PEGCOMP trace width and spacing is 20/25 mils.

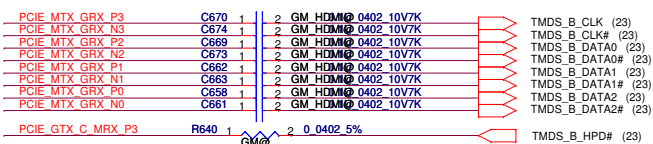
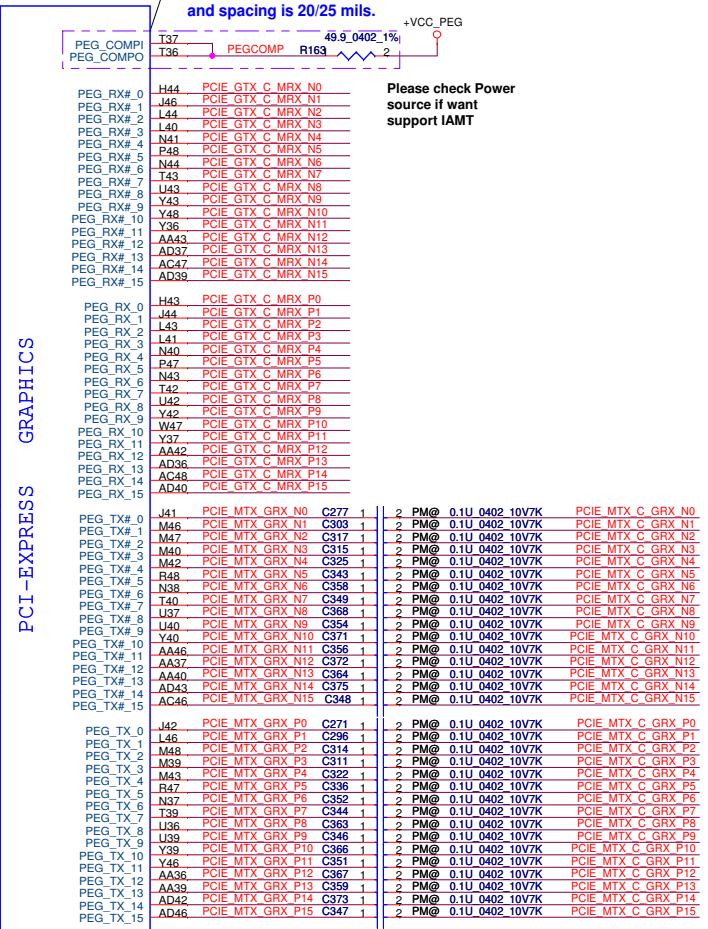
For Cantiga: 2.37kohm  
 For Crestline: 2.4kohm  
 For Calero: 1.5Kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

Layout Note: Place 150 Ohm termination resistors close to GMCH

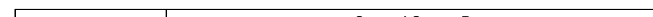


For Cantiga: 1.02kohm  
 For Crestline: 1.3kohm  
 For Calero: 255ohm

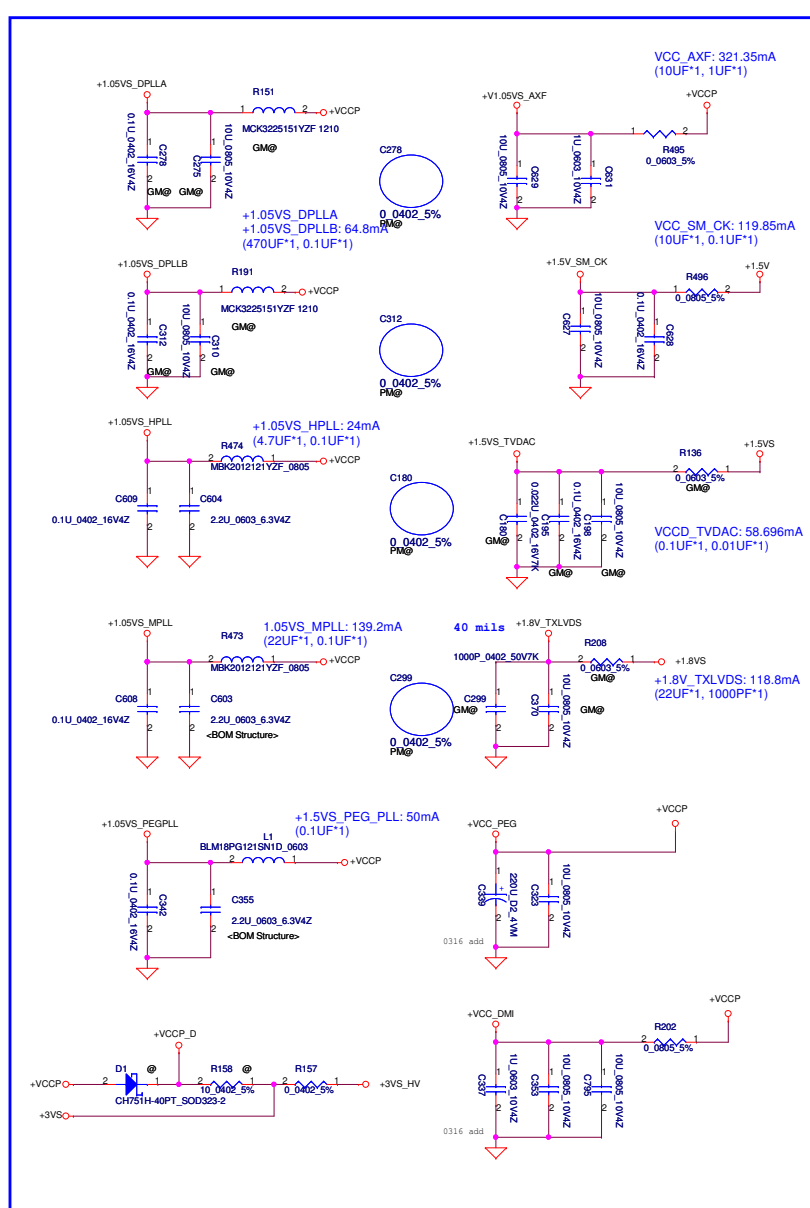
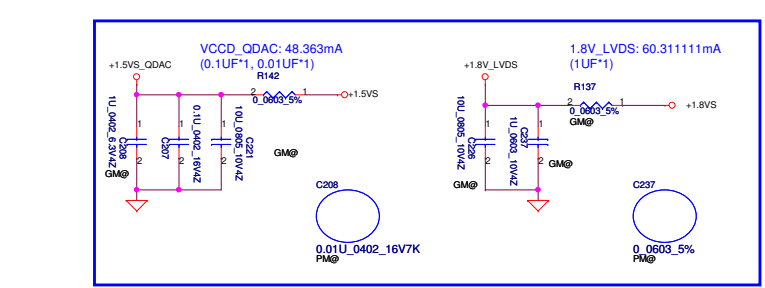
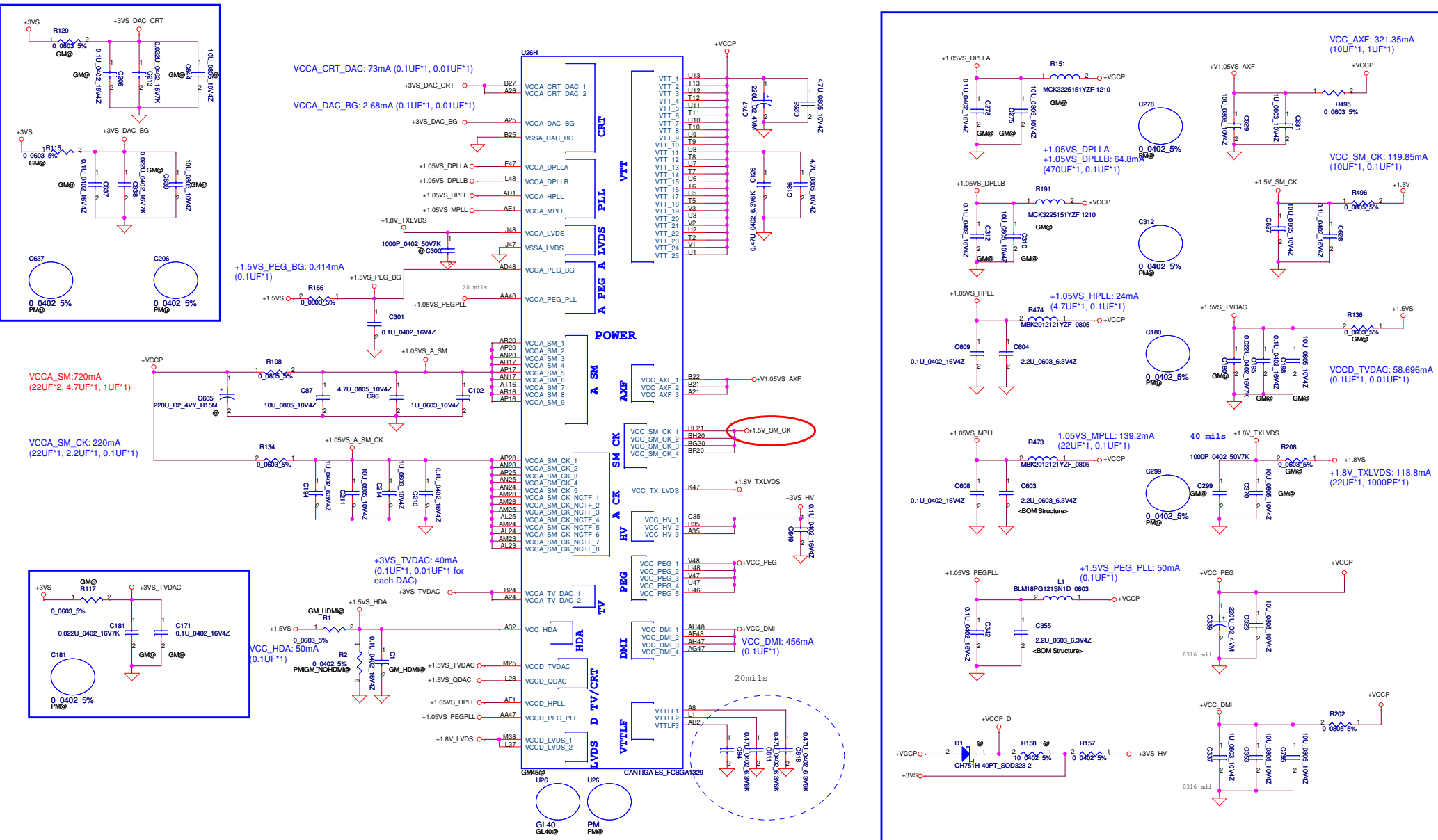


### Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *

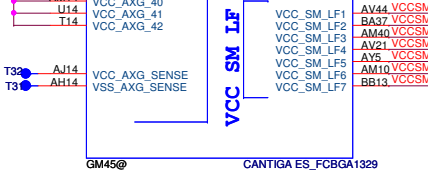
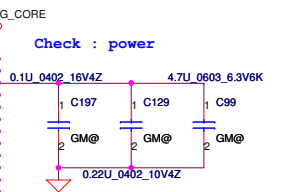
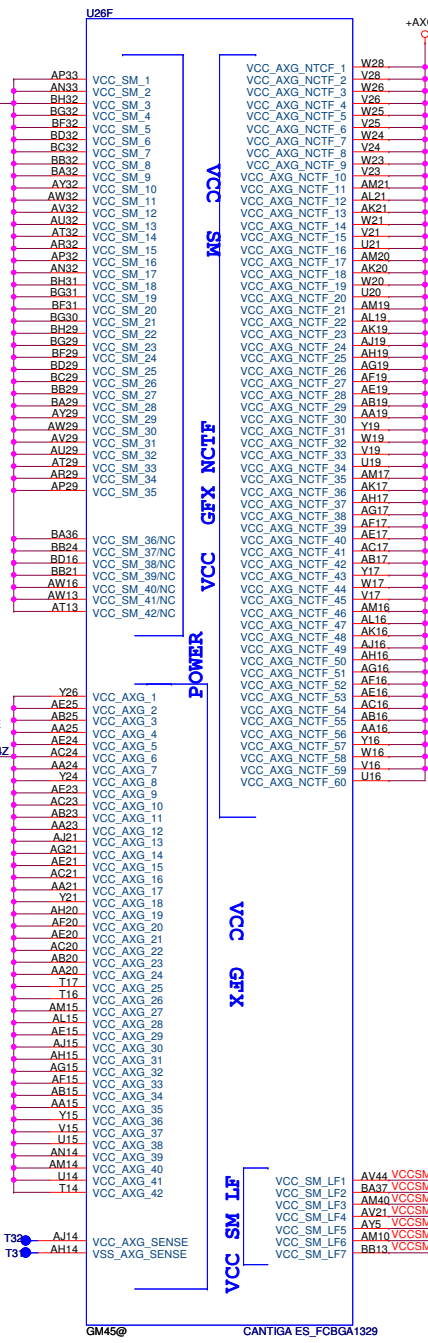
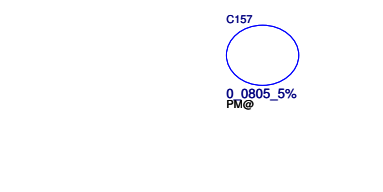
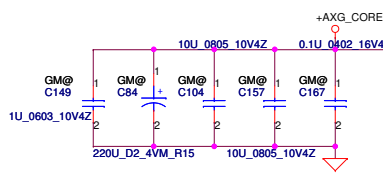
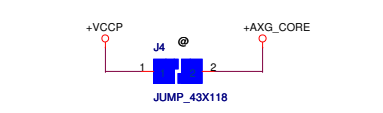
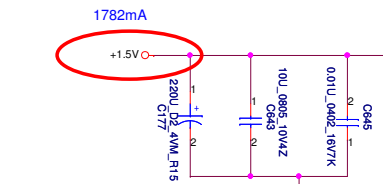
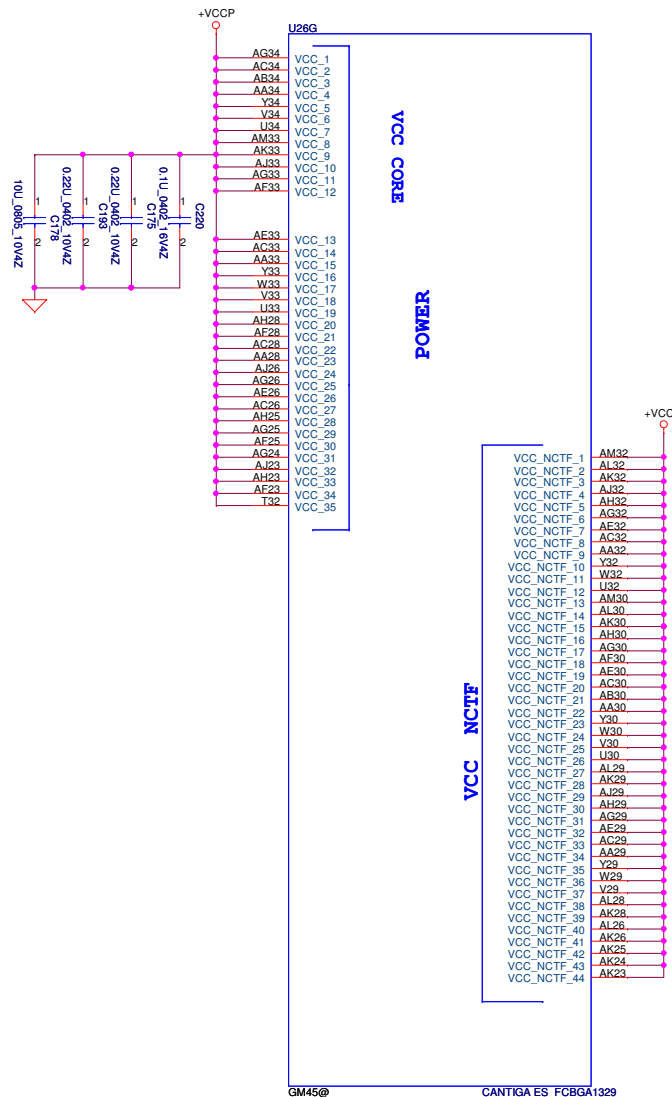


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Size	Document Number	Rev		1.0
Customer	KIWAX_LA-508IP			
Date:	Tuesday, April 28, 2009	Sheet	11	of 51

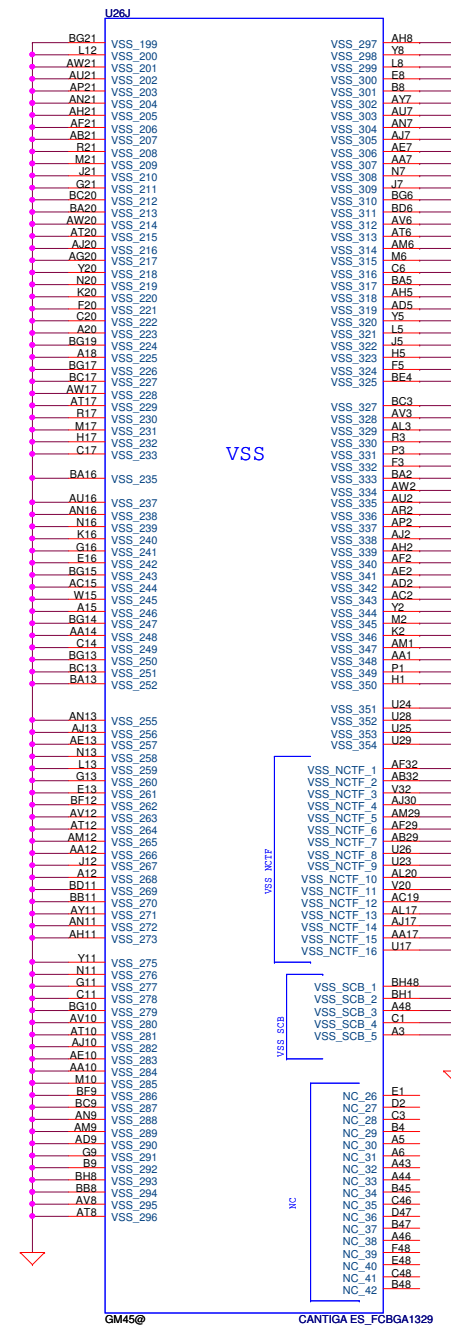
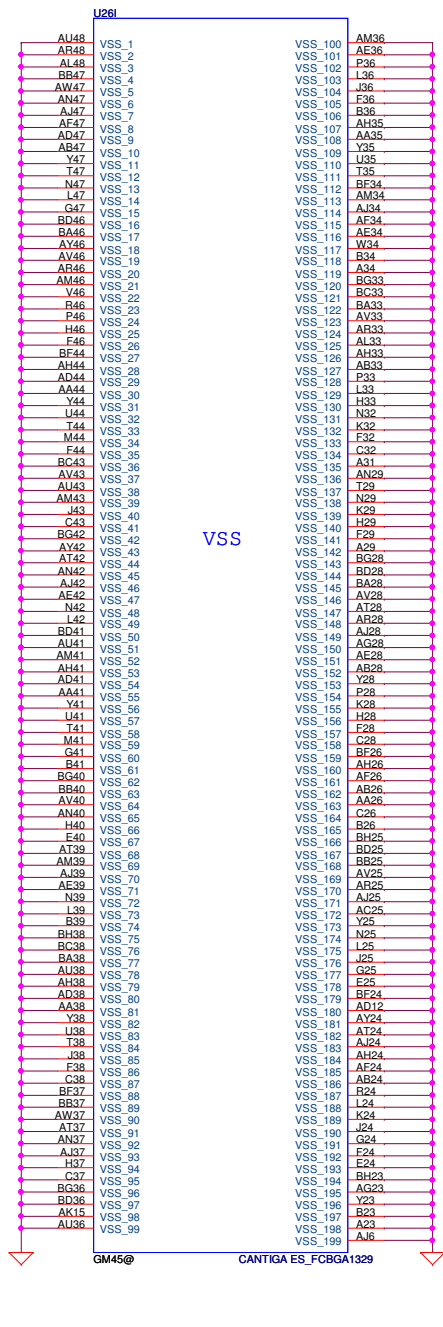
**Compal Electronics, Inc.**  
**Crestline GMCH (4/6)-VCC**



GM45@ CANTIGA ES\_FCBGA1329

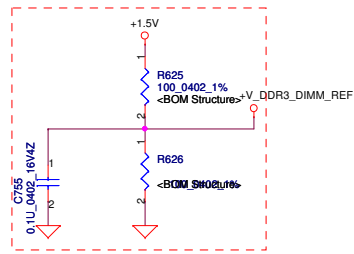
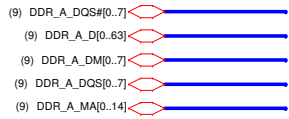
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Size	Document Number	K1WAX_LA-5081P		Rev	1.0
Customer	Date				Tuesday, April 28, 2009
Date				Sheet	12 of 51



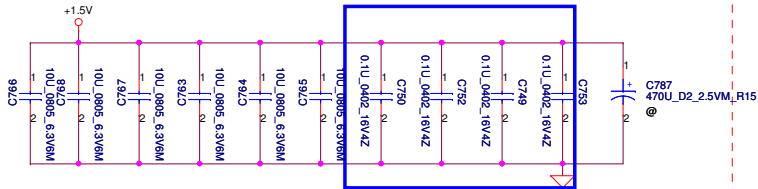
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Issued Date	2009/04/23	Deciphered Date	2010/05
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Compal Electronics, Inc.			
Title <b>Cantiga GMCH (6/6)-GND</b>			
Size	Document Number	Rev	
Custom	<b>KIWAX_LA-5081P</b>	1.0	
Date:	Tuesday, April 28, 2009	Sheet	13 of 51

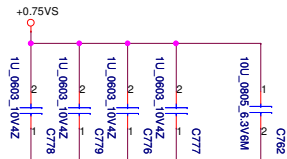


Layout Note:  
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:  
Place near JP4.203 & JP4.204



### DDR3 SO-DIMM A REVERSE

Security Classification	Compal Secret Data	
Issued Date	2009/04/23	Deciphered Date
		2010/05

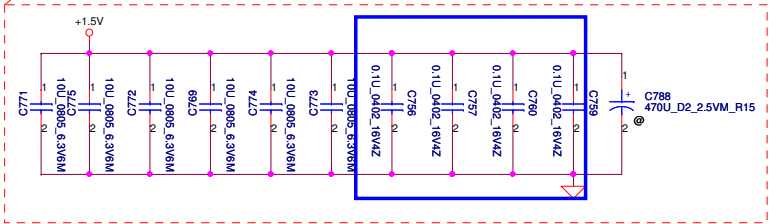
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Title		
Compal Electronics, Inc.		
DDRIII-SODIMM SLOT1		
Size	Document Number	Rev
Custort	KIWAX_LA-5081P	1.0
Date:	Tuesday, April 28, 2009	Sheet 14 of 51

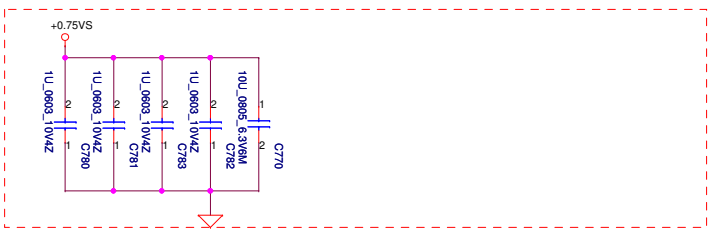
- (9) DDR\_B\_DQS#[0..7]
- (9) DDR\_B\_D[0..63]
- (9) DDR\_B\_DM[0..7]
- (9) DDR\_B\_DQS[0..7]
- (9) DDR\_B\_MA[0..14]

**Layout Note:**  
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



**Layout Note:**  
Place near JP5.203 & JP5.204

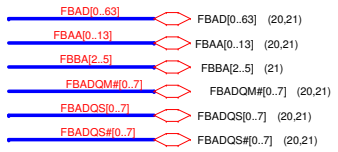


**DDR3 SO-DIMM B  
REVERSE**

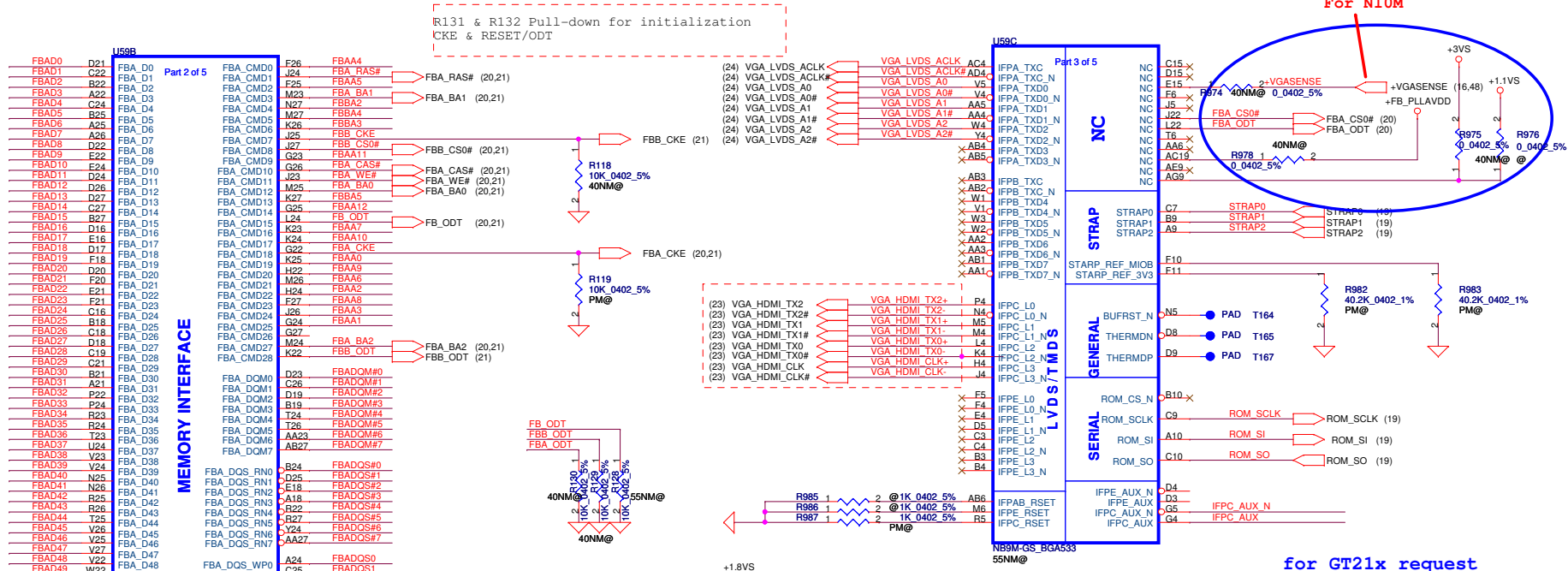
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				DDR3-SODIMM SLOT2	
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CKE.cs00DT



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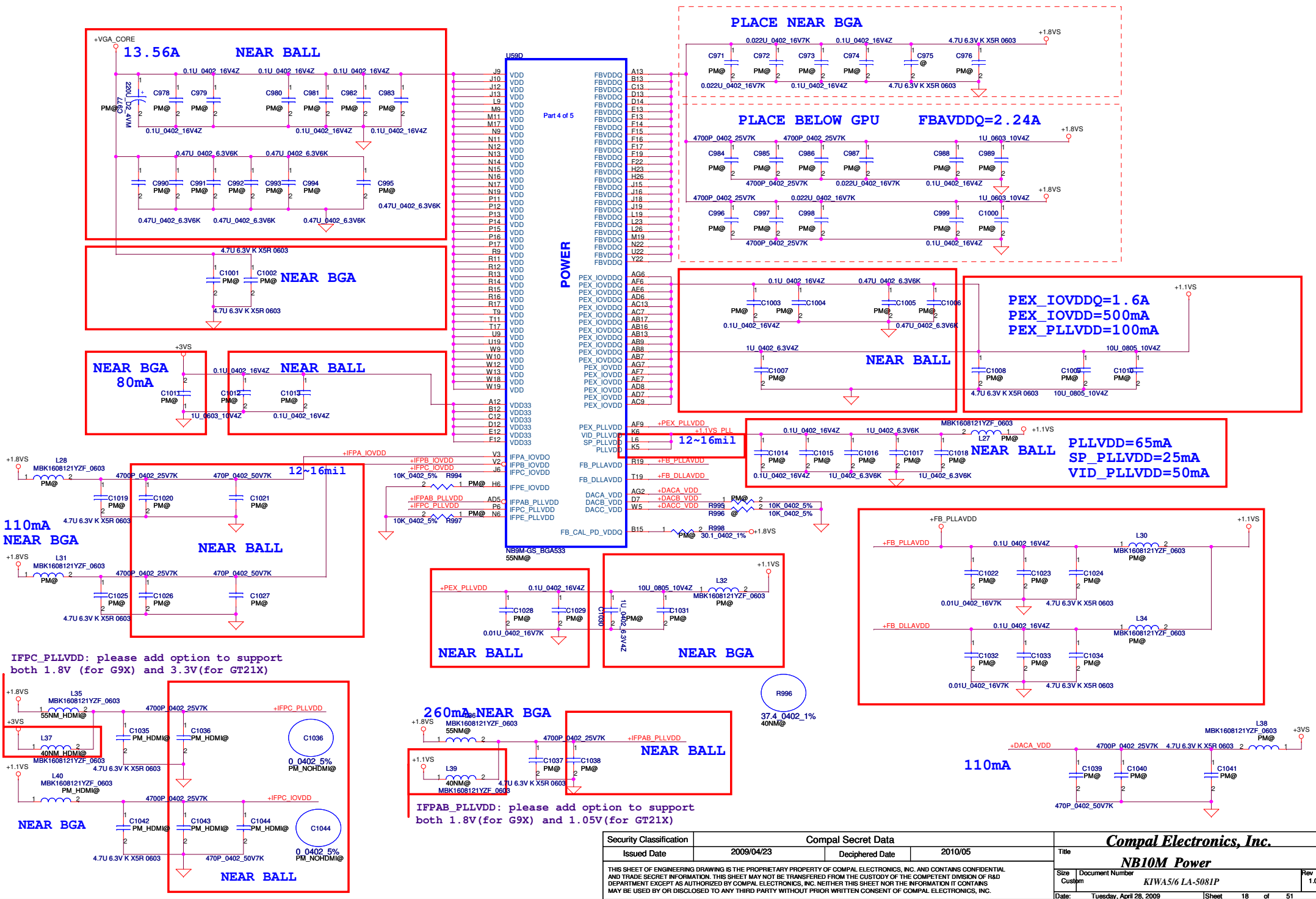
Compal Electronics, Inc.

N10M Memory

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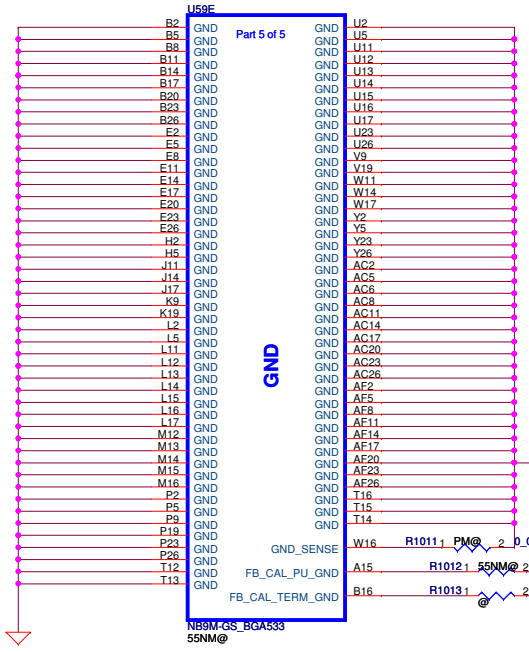
Title	N10M Memory		
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Date:	Tuesday, April 28, 2009	Sheet	17 of 51

FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS



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		Customer	KIWA5/6 LA-5081P	Date:	Tuesday, April 28, 2009
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A total of 8 signals are required for GB1 strapping this includes  
 2 reference signals  
 6 physical strapping pins  
 4 logical strapping bits  
 A total of 24 logical strapping bits are available



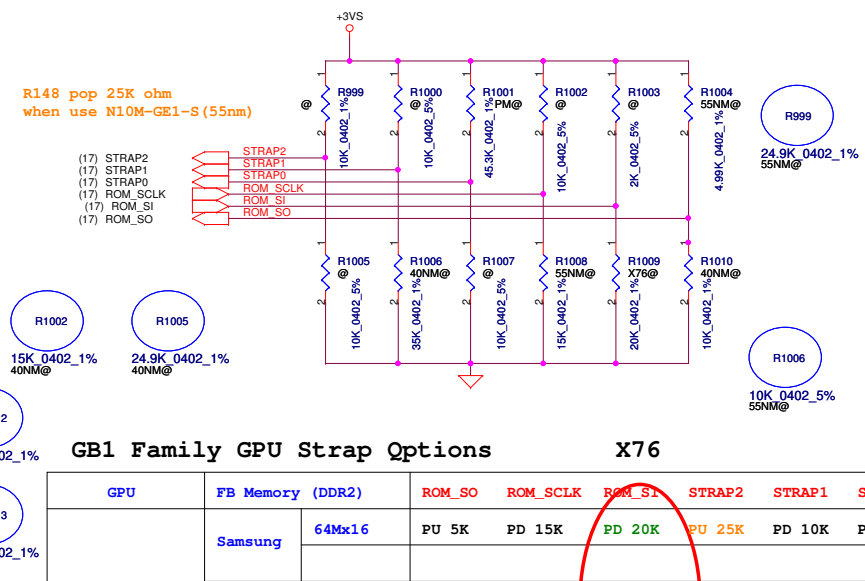
Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001\_V06 (2008/4/01)



R148 pop 25K ohm when use N10M-GE1-S (55nm)

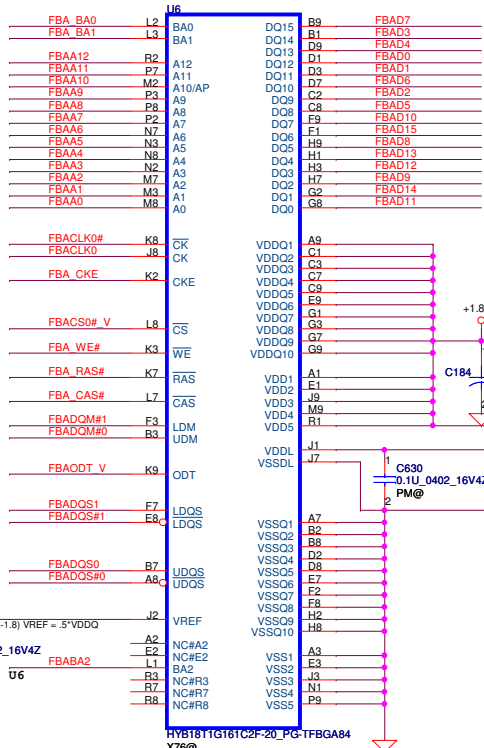
- (17) STRAP2
- (17) STRAP1
- (17) STRAP0
- (17) ROM\_SCLK
- (17) ROM\_SI
- (17) ROM\_SO



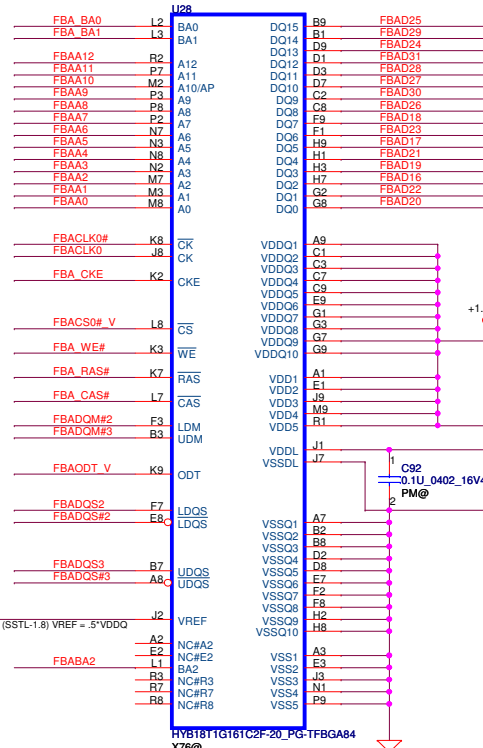
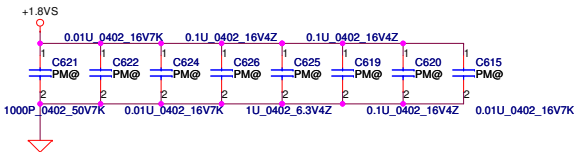
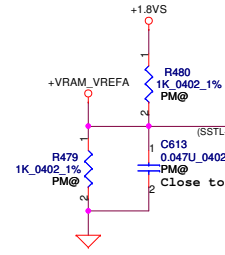
GB1 Family GPU Strap Options X76

GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung 64Mx16	PU 5K	PD 15K	PD 20K	PU 25K	PD 10K	PU 45K
	Hynix 64Mx16	PU 5K	PD 15K	PD 5K	PU 25K	PD 10K	PU 45K
	Qimonda 64Mx16	PU 5K	PD 15K	PD 15K	PU 25K	PD 10K	PU 45K
GPU	Samsung 64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 35K	PU 45K
	Hynix 64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 35K	PU 45K
	Qimonda 64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 35K	PU 45K

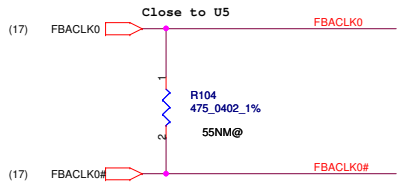
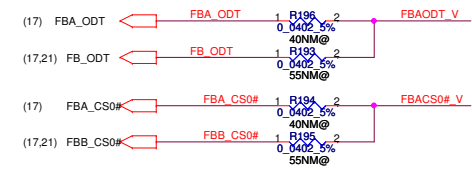
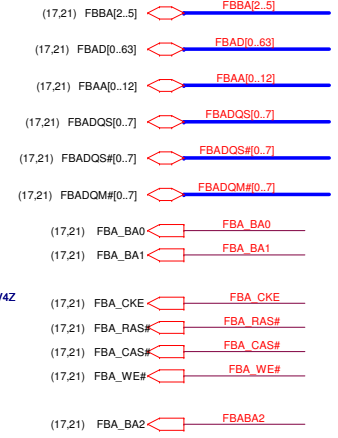
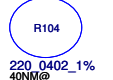
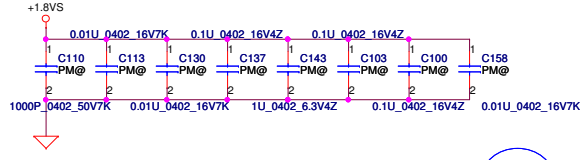
4/23 update strap1 10K to 35K according to N10M latest PUN



DDR2 BGA MEMORY

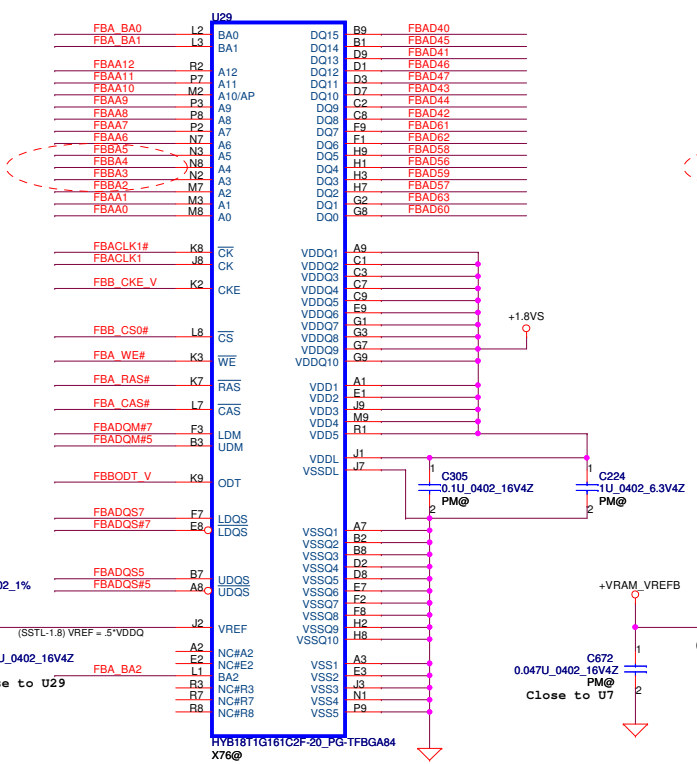


DDR2 BGA MEMORY

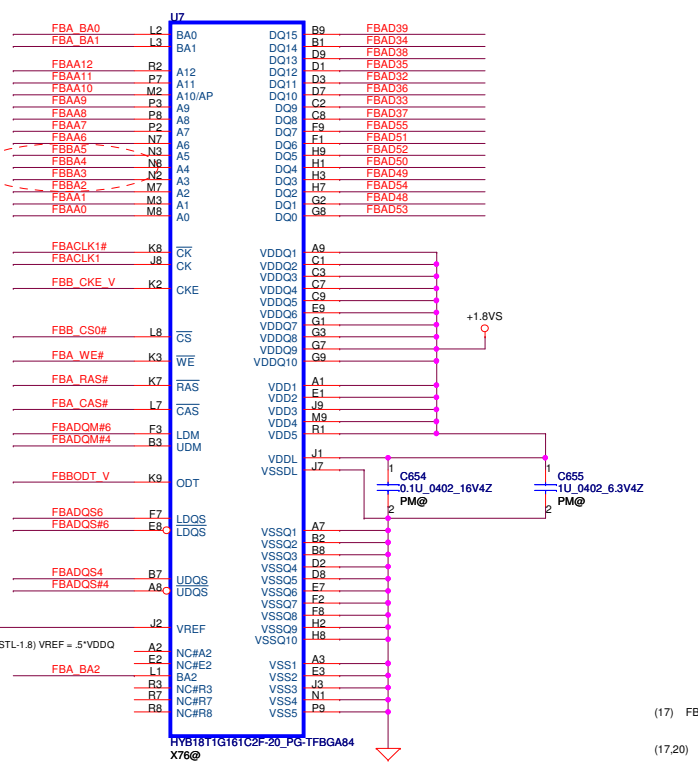


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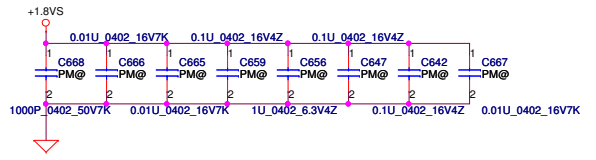
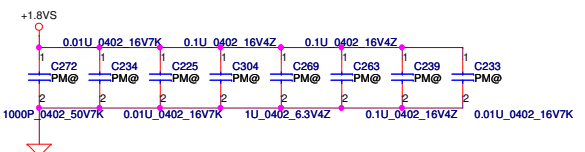
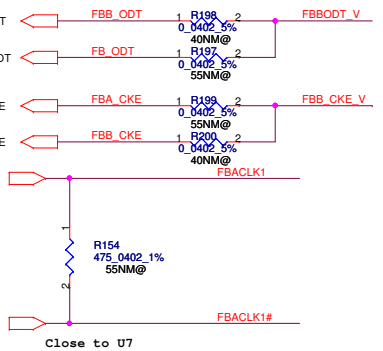
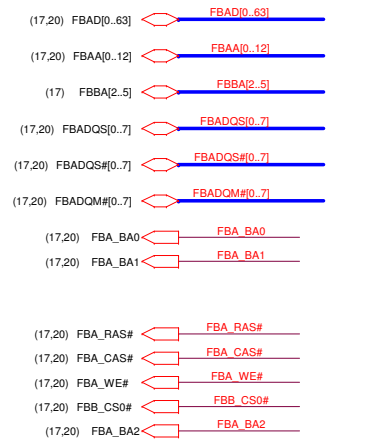
Title			
Compal Electronics, Inc.			
VRAM DDRA			
Size	Document Number	Rev	
Custom	KIWA5/6 LA-5081P	1.0	
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DDR2 BGA MEMORY



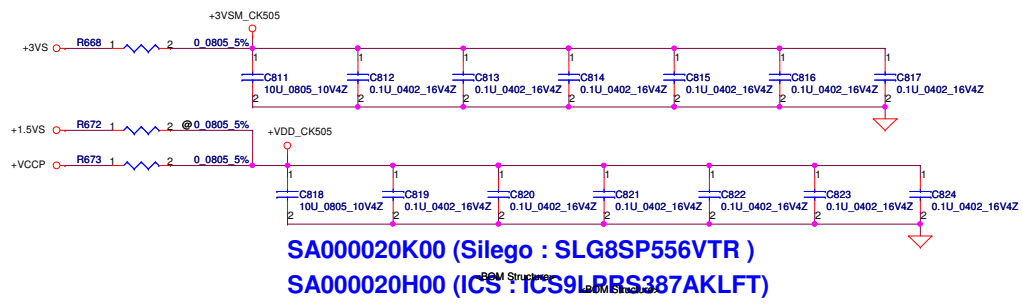
DDR2 BGA MEMORY



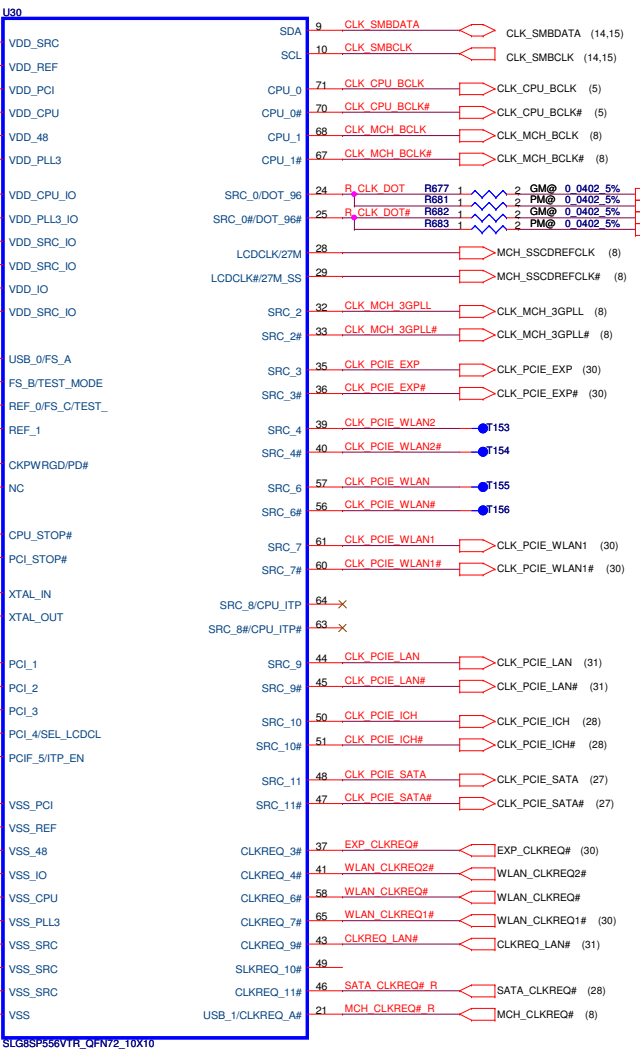
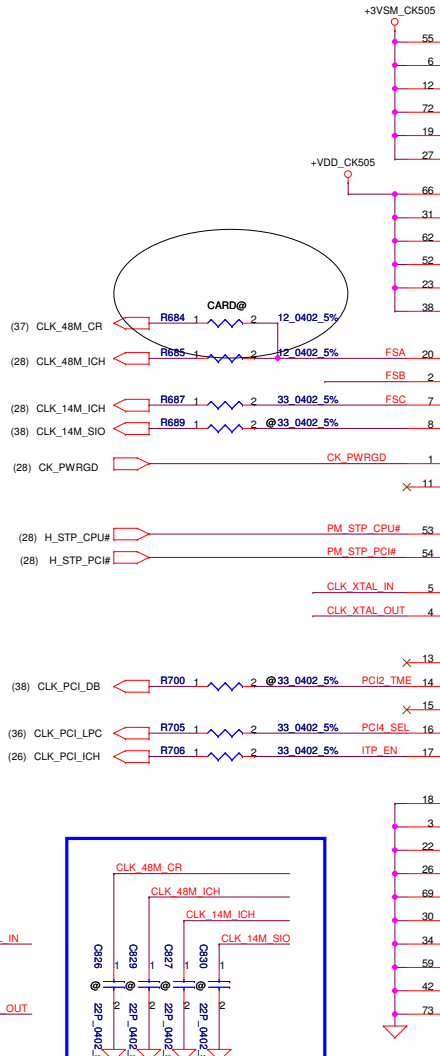
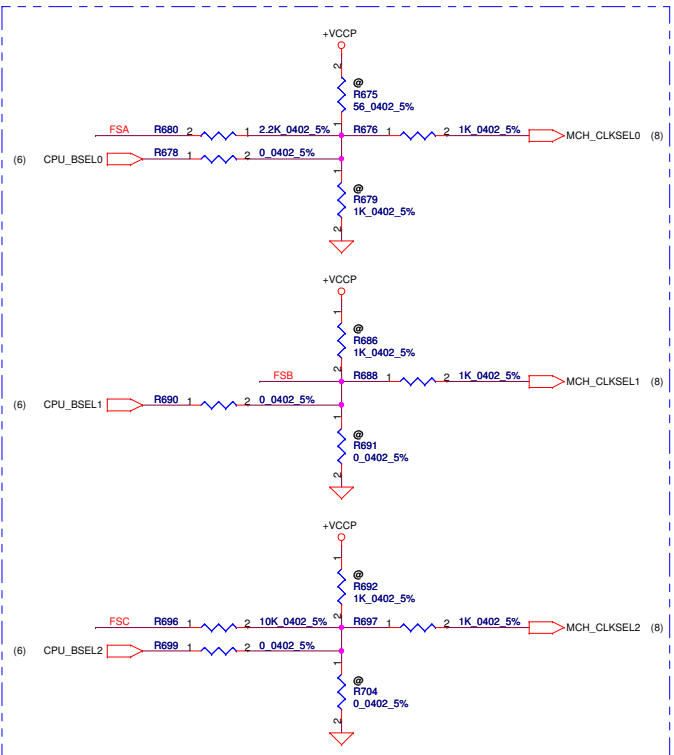
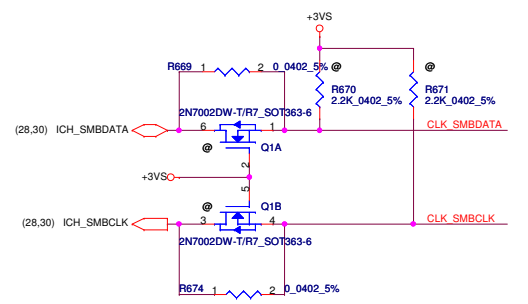
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Title			
Compal Electronics, Inc.			
VRAM DDRB			
Size	Document Number	Rev	
Custom	KIWA5/6 LA-5081P	1.0	
Date:	Tuesday, April 28, 2009	Sheet	21 of 51

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
<b>Reserved</b>								



**SA000020K00 (Silego : SLG8SP556VTR)**  
**SA000020H00 (ICS : ICS9LRS387AKLFT)**

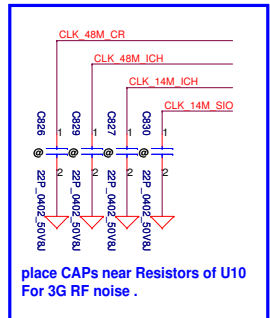
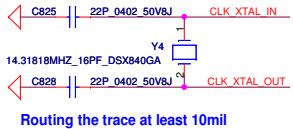
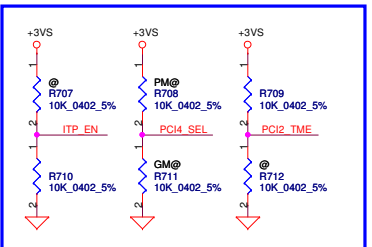


**SRC PORT LIST**

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN
SRC6	PCIE_WLAN1
SRC8	PCIE_WLAN
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

**REQ PORT LIST**

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	PCIE_LAN
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL



For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
 For PCI4\_SEL, 0 = Pin24/25 : DOT96 / DOT96#  
 Pin28/29 : LCDCLK / LCDCLK#  
 1 = Pin24/25 : SRC\_0 / SRC\_0#  
 Pin28/29 : 27M/27M\_SS

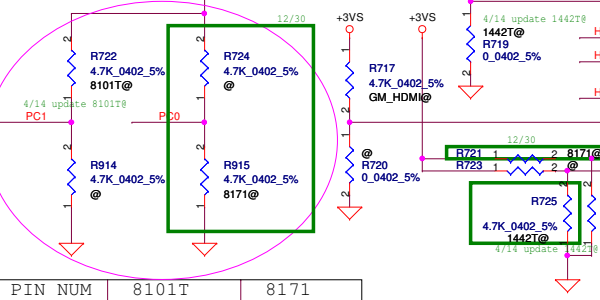
place CAPs near Resistors of U10  
 For 3G RF noise .

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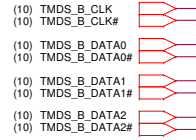
Compal Electronics, Inc.		
<b>Clock Generator CK505</b>		
Title	Document Number	Rev
	KIWA5/6 LA-5081P	1.0
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10/30 update PS8171 co-lay circuit  
4/14 update 1442T co-lay circuit

For 8171

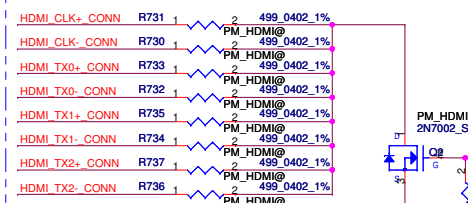


PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	P10
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	APD
PIN12	GND	ASQ1
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

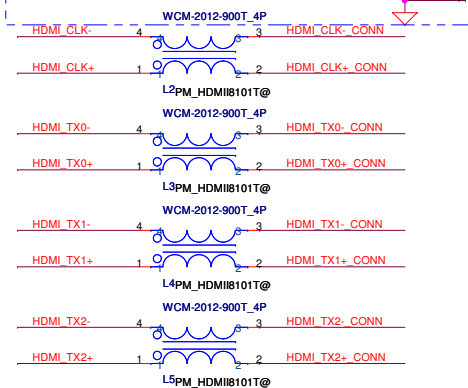


For 8171 net name:  
EMI0, EMI1  
ASQ0, ASQ1  
APD

**TMDS pull down (500ohm) resistors for ATI M92-S2 XT**

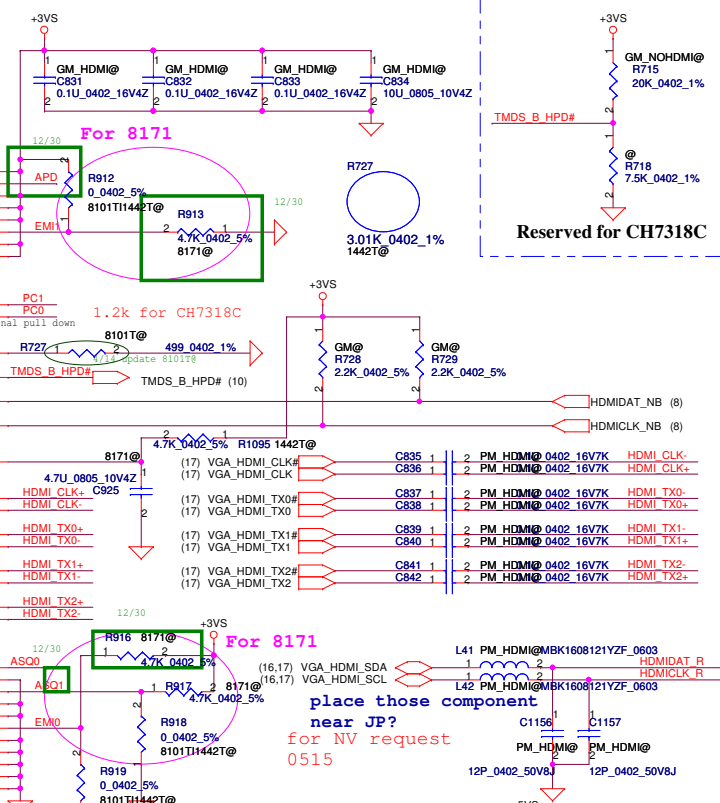
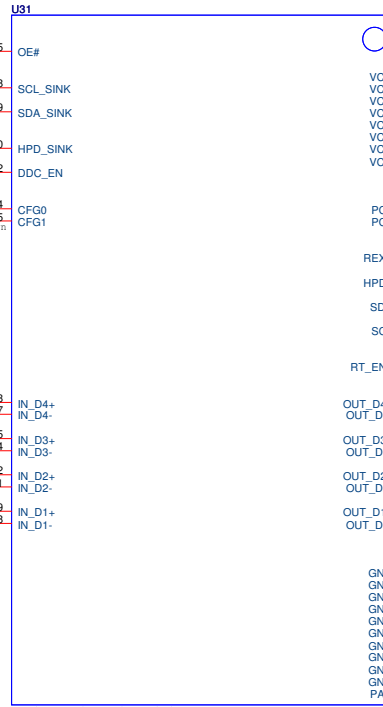


**NEAR CONNECTOR**



HDMI_CLK+	R751	1442T@	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_CLK-	R752	1442T@	2	0.0402_5%	HDMI_CLK- CONN
HDMI_TX0+	R753	1442T@	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_TX0-	R754	1442T@	2	0.0402_5%	HDMI_TX0- CONN
HDMI_TX1+	R755	1442T@	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_TX1-	R756	1442T@	2	0.0402_5%	HDMI_TX1- CONN
HDMI_TX2+	R757	1442T@	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_TX2-	R758	1442T@	2	0.0402_5%	HDMI_TX2- CONN

P/N:SA00002D700 (8101T)  
P/N:SA00001U920 (CH7318C)



place those component near JP?  
for NV request 0515

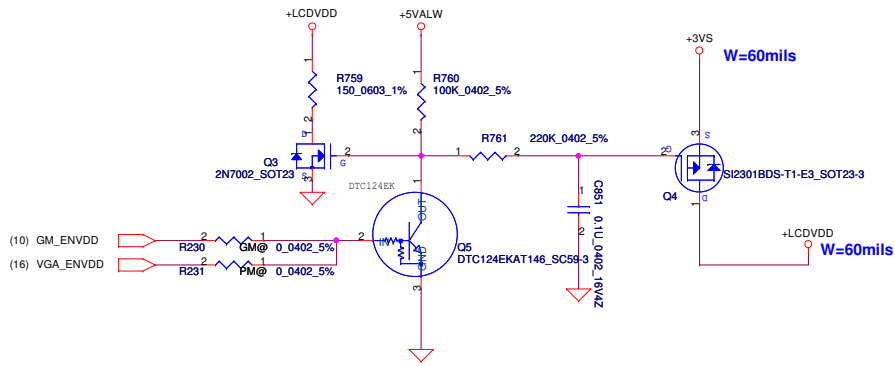
KIWB3/B4\_LA4551P

Security Classification	Compal Secret Data		2010/05
Issued Date	2009/04/23	Deciphered Date	

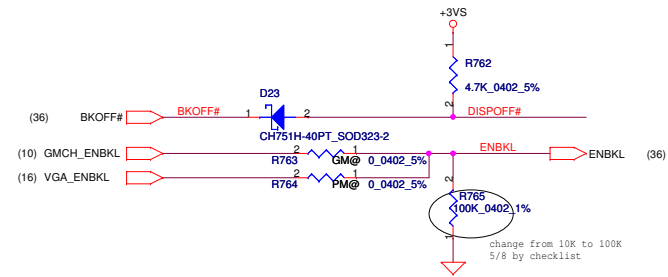
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Level Shifter_PS8101T			
Size	Document Number		Rev
Custom	KIWAX_LA-5081P		1.0
Date:	Tuesday, April 28, 2009	Sheet	23 of 51

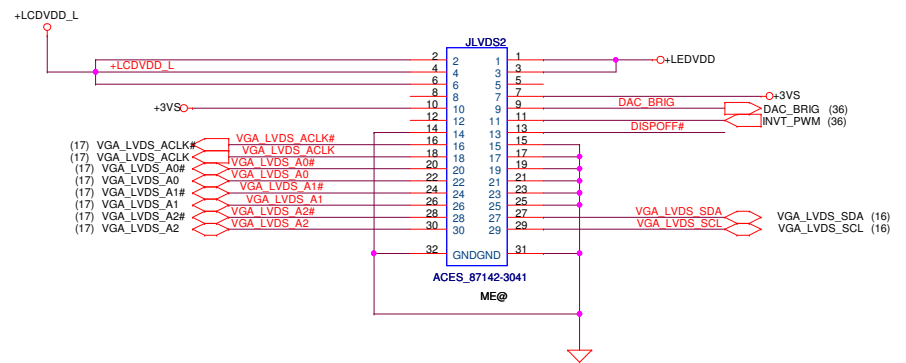
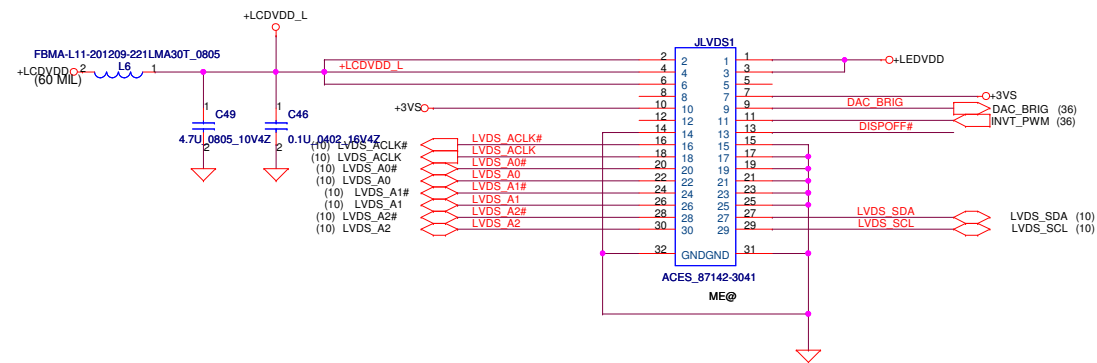
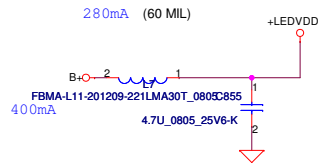
# LCD POWER CIRCUIT



LCD/PANEL BD. Conn. FOR UMA



LCD/PANEL BD. Conn. FOR DIS

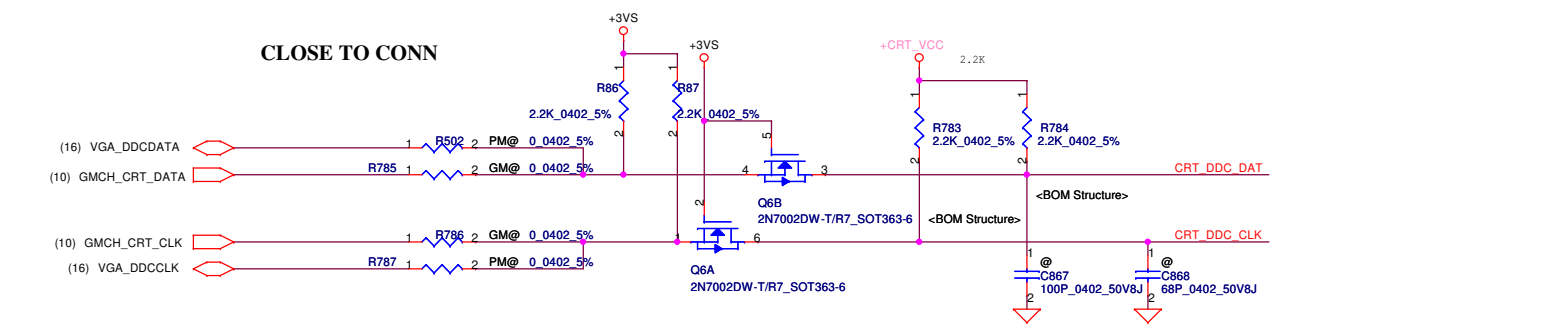
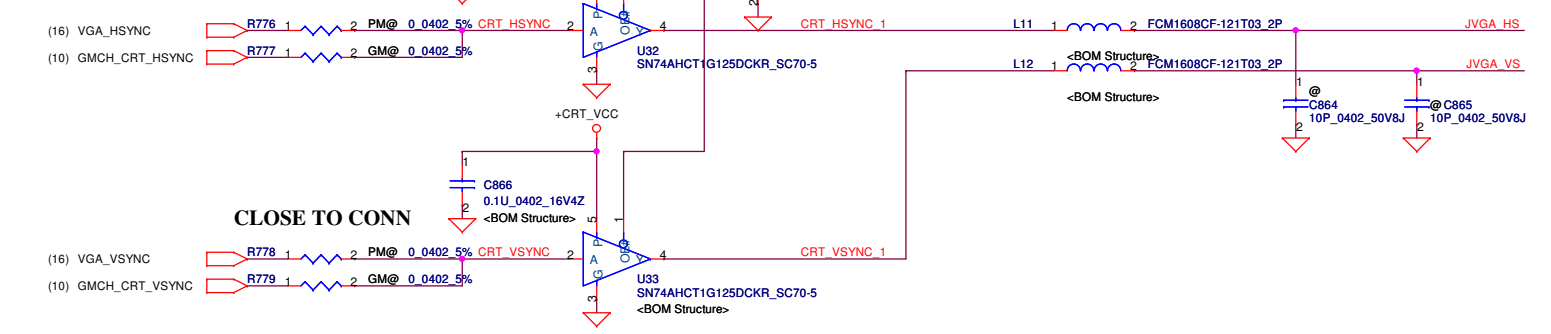
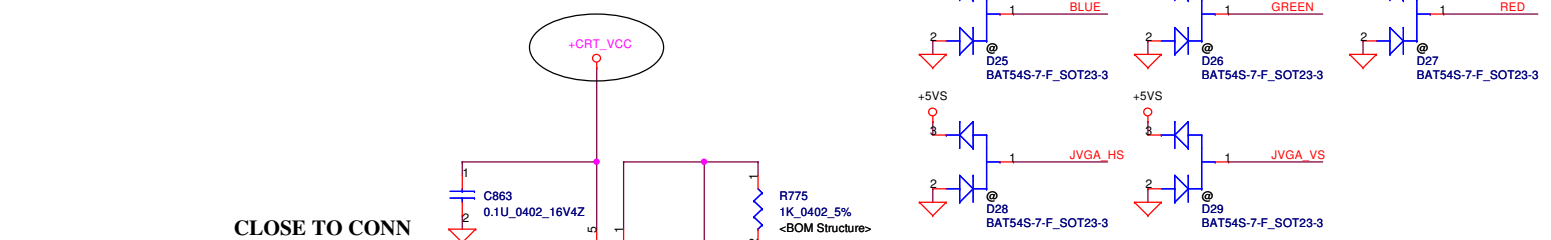
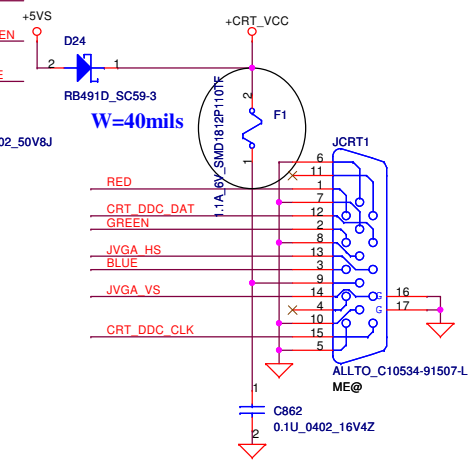
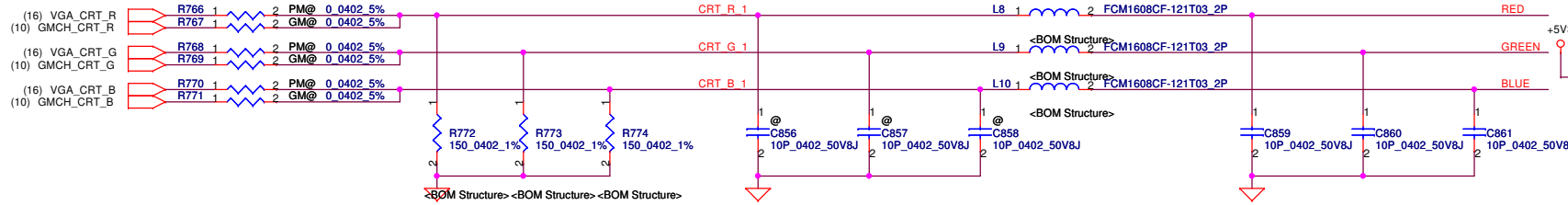


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# CRT Connector

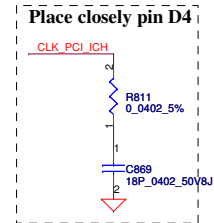
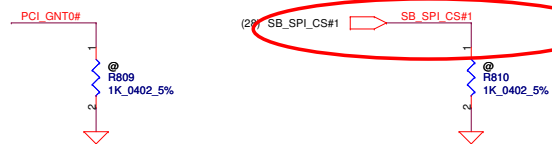
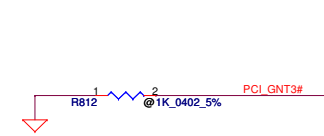
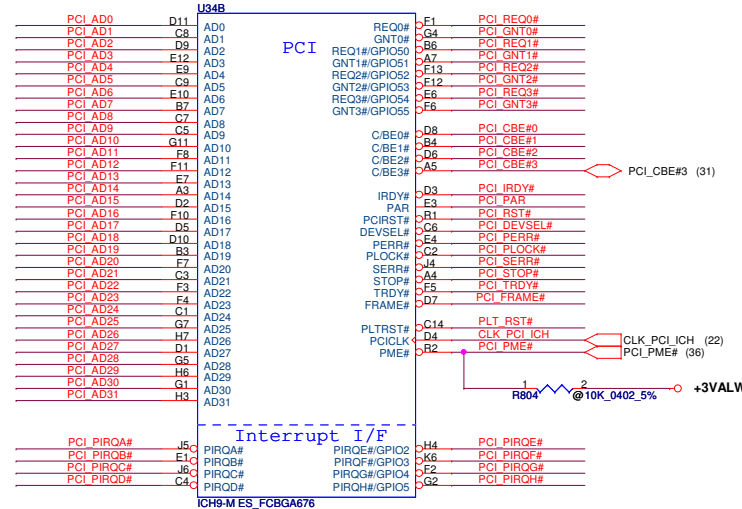
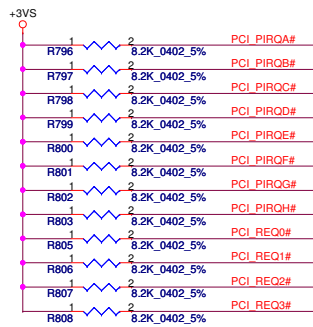
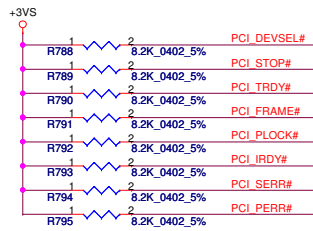
## CLOSE TO CONN



## PIN ASSIGMENT

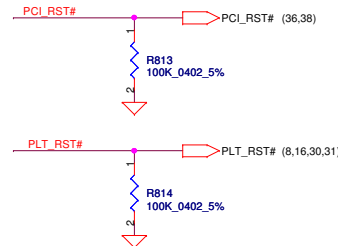
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

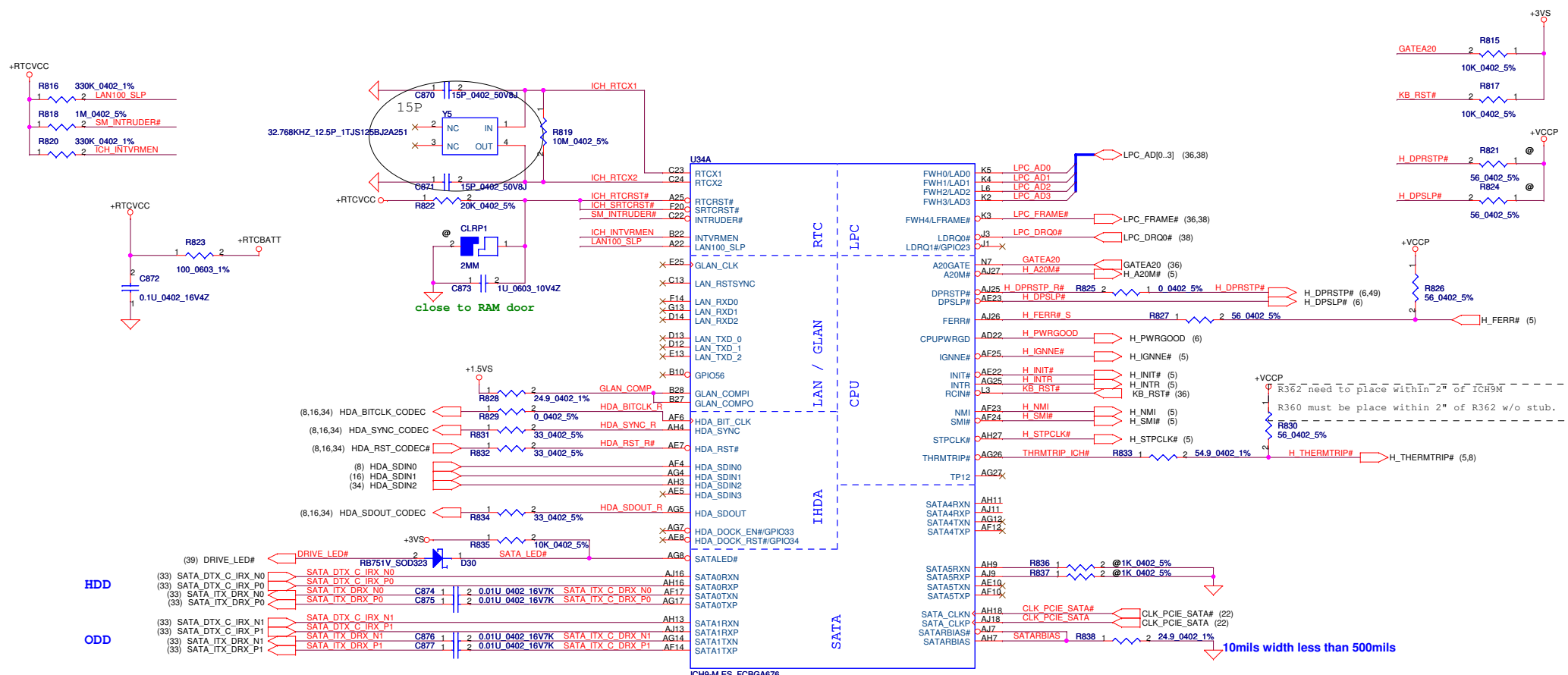
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Size	Custom	Rev	1.0		



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

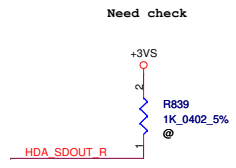
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

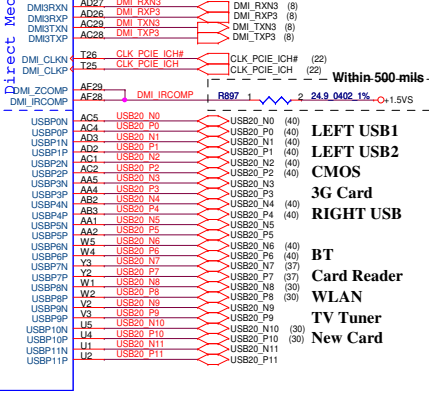
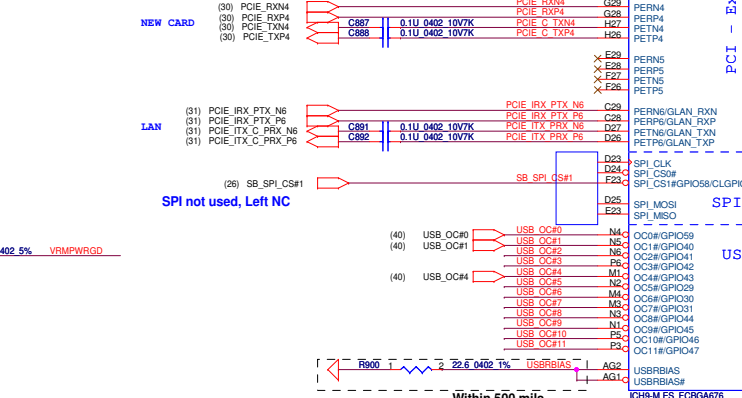
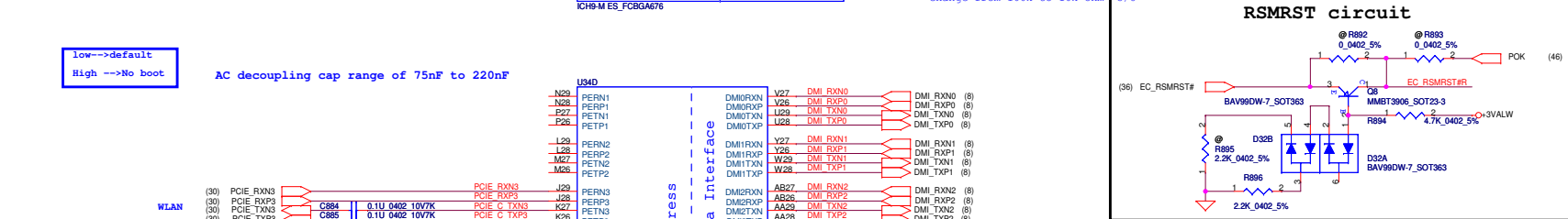
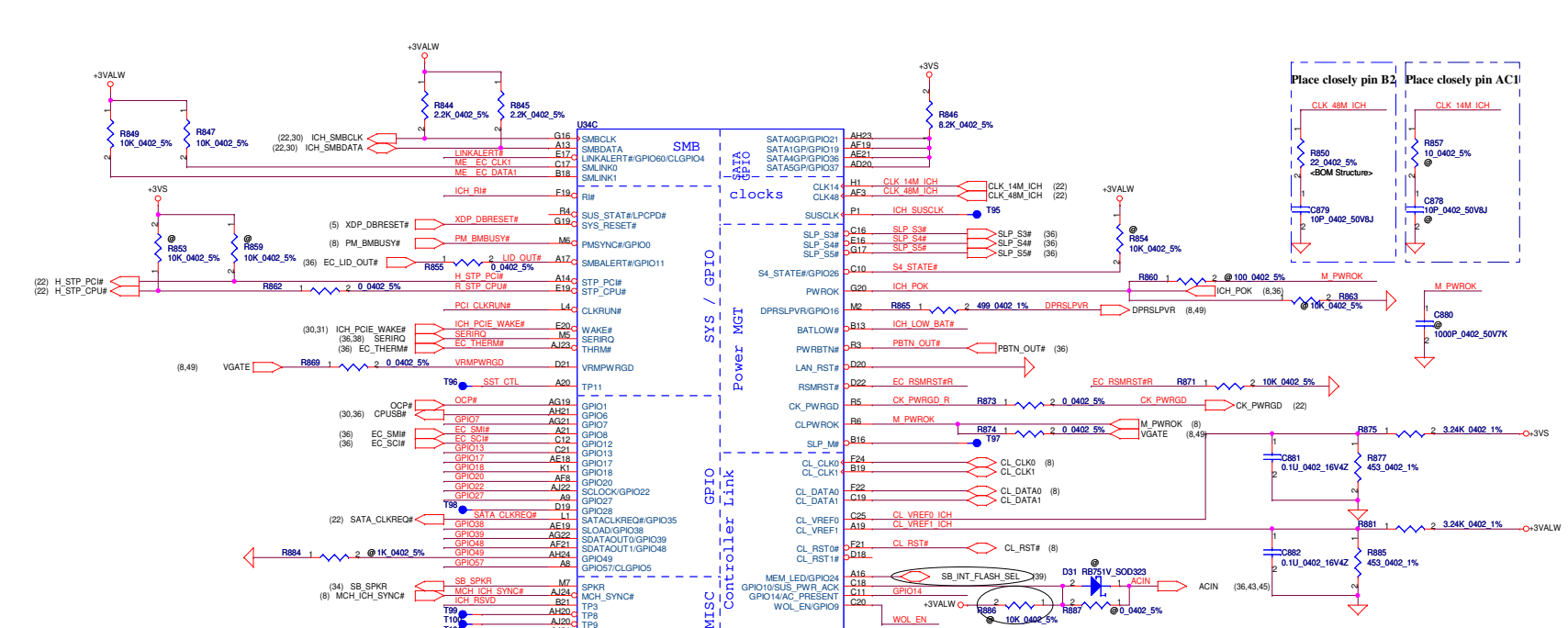
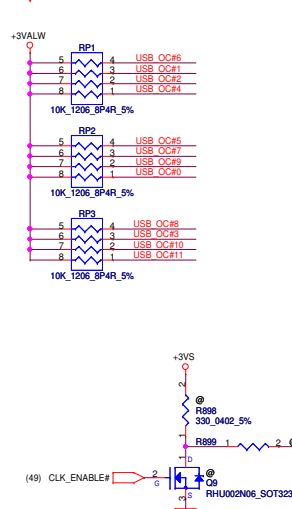
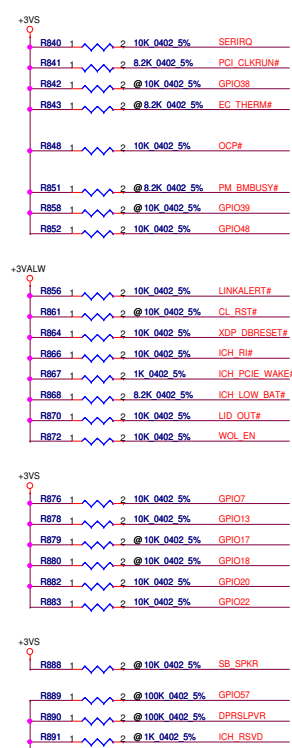




SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1





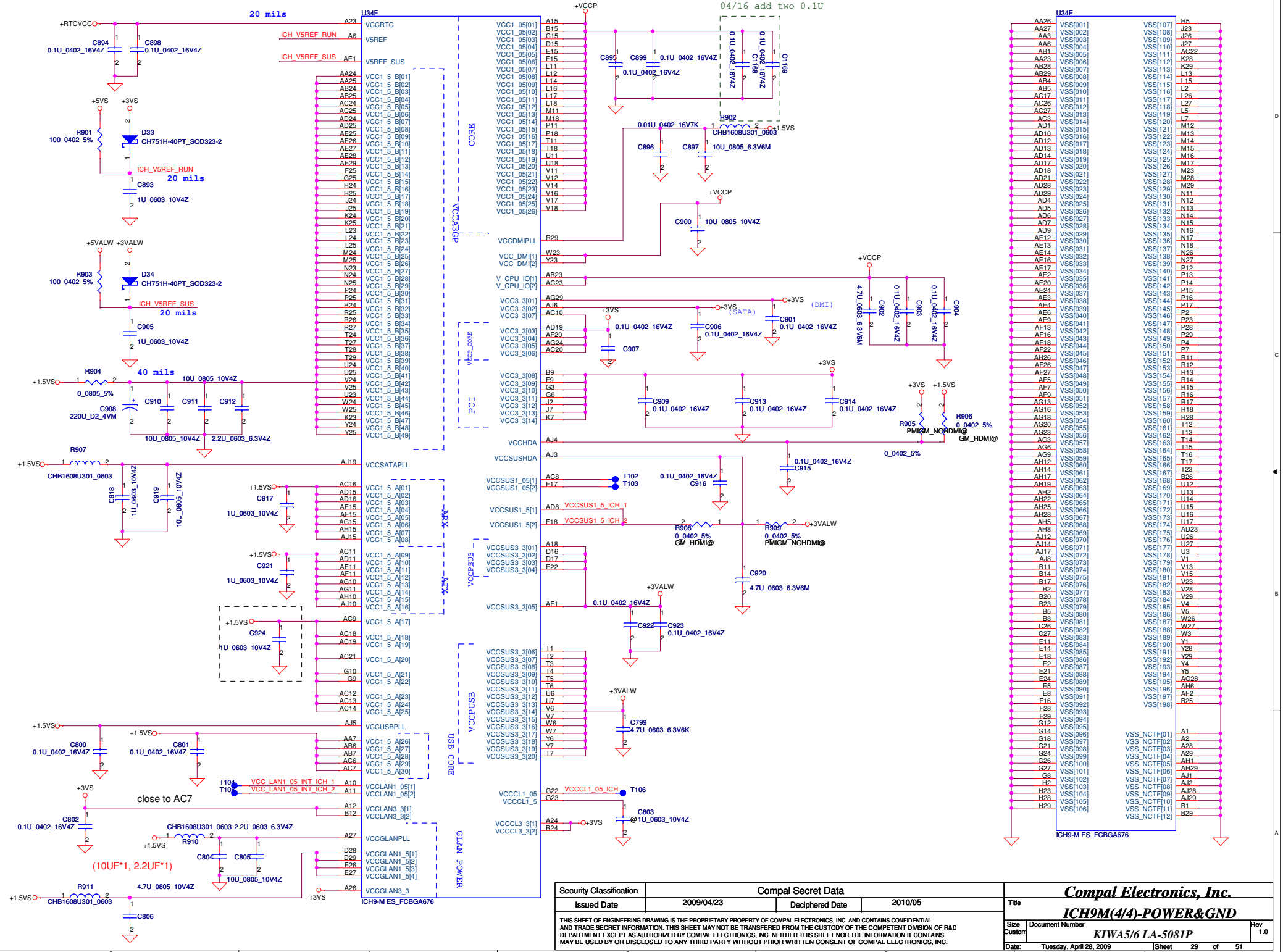
### PCI PORT LIST

PORT	DEVICE
1	
2	
3	WLAN
4	NEW CARD
5	
6	LAN

### USB PORT LIST

PORT	DEVICE
0	LEFT SIDE1
1	LEFT SIDE2
2	CMOS
3	3G
4	RIGHT SIDE
5	
6	BT
7	CARD READER
8	WIRELESS
9	
10	NEW CARD
11	

BT Card Reader  
WLAN  
TV Tuner  
New Card

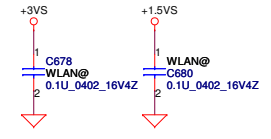
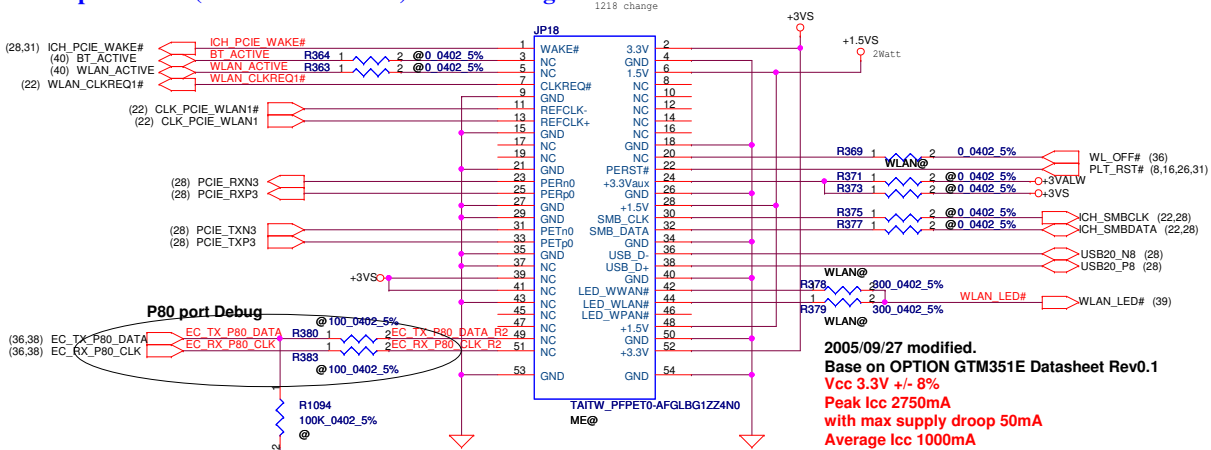


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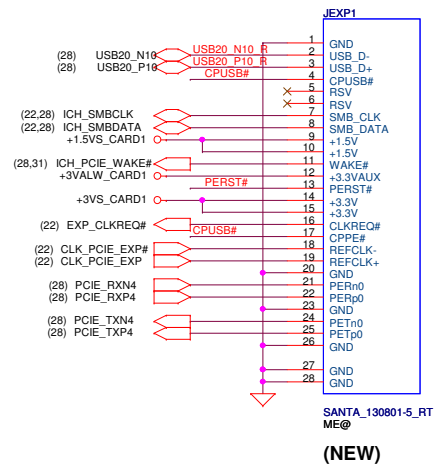
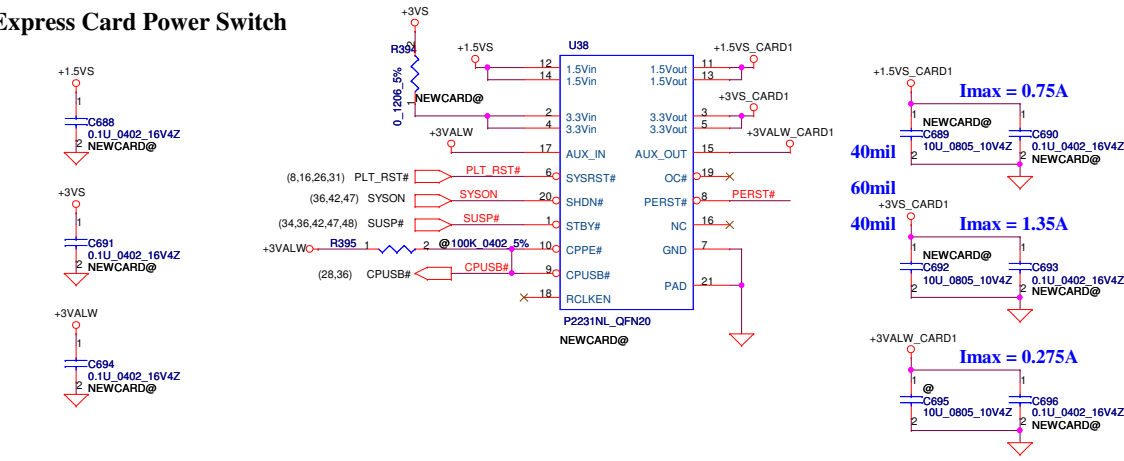
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Compal Electronics, Inc.			Title	
			<b>ICH9M(4/4)-POWER&amp;GND</b>	
Size	Document Number			Rev
Custom	KIWA5/6 LA-5081P			1.0
Date:	Tuesday, April 28, 2009	Sheet	29	of 51

# Mini-Express Card(Slot 2-WIRELESS) 5.2mm high

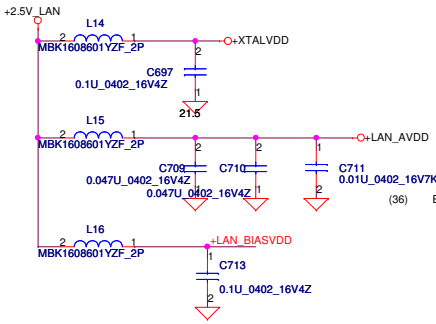


## Express Card Power Switch

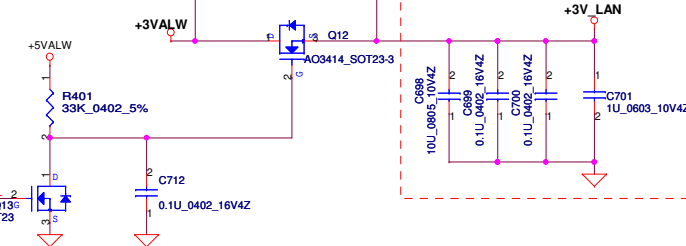


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				Mini-Card/3G/TV/BT		
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				Date:	Tuesday, April 28, 2009	Sheet 30 of 51

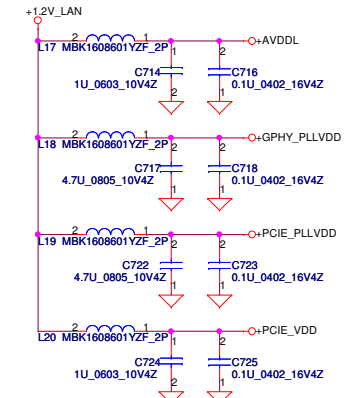
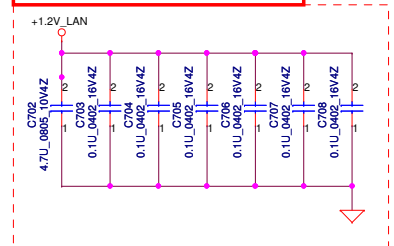
Layout Notice : Filter place as close chip as possible.



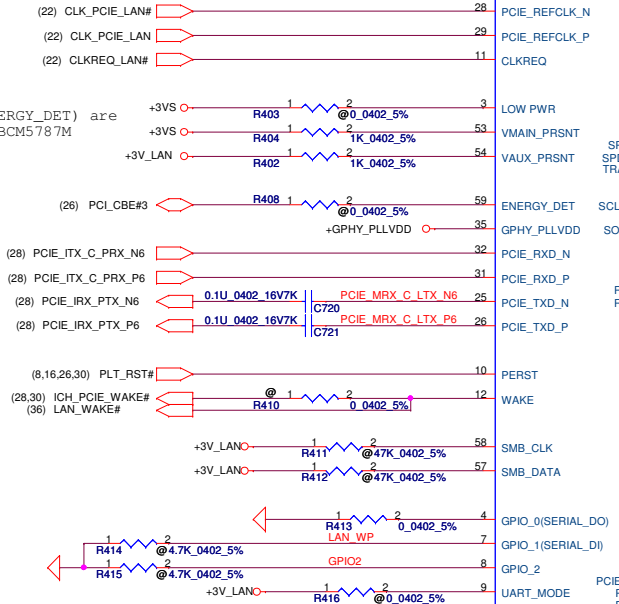
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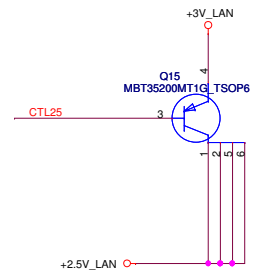
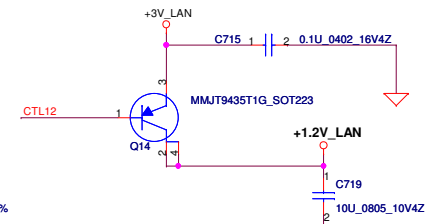
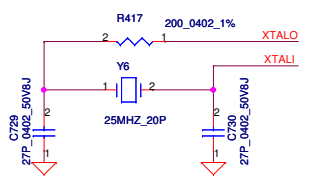
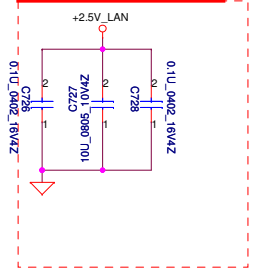
Layout Notice : 1.2V filter. Place as close chip as possible.



(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M

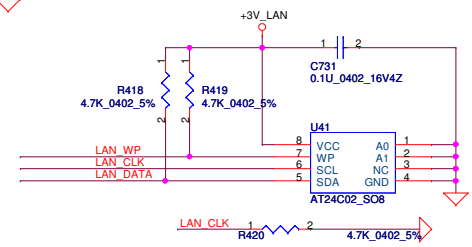


Layout Notice : Place as close chip as possible.

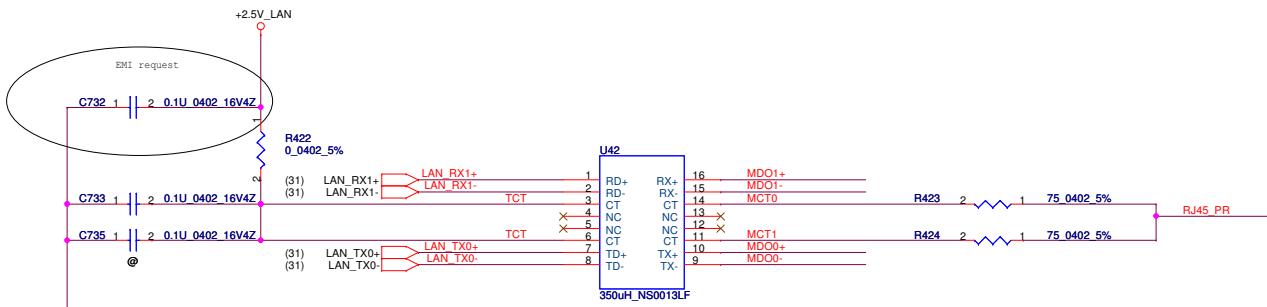


Notice : 4.7u 6.3V capacitor Thickness 1.25mm

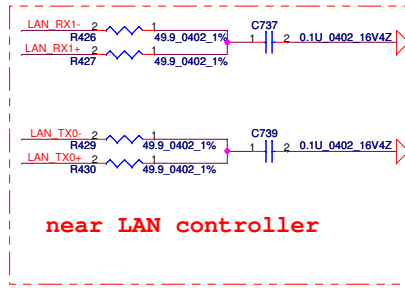
Layout Notice : Filter place as close chip as possible.



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Size	Document Number	Rev	Date: Tuesday, April 28, 2009   Sheet 31 of 51		
Customer	KIWA5/6 LA-5081P	1.0			

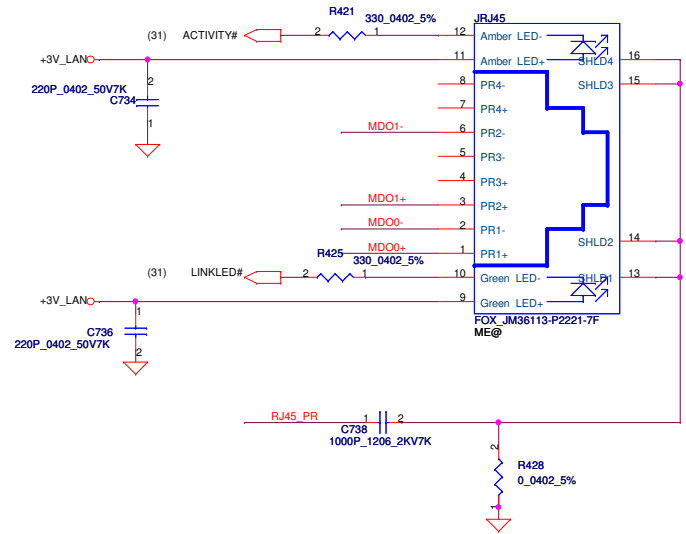


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



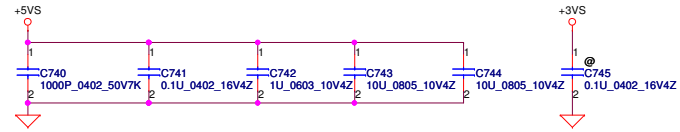
near LAN controller

## RJ45 CONN

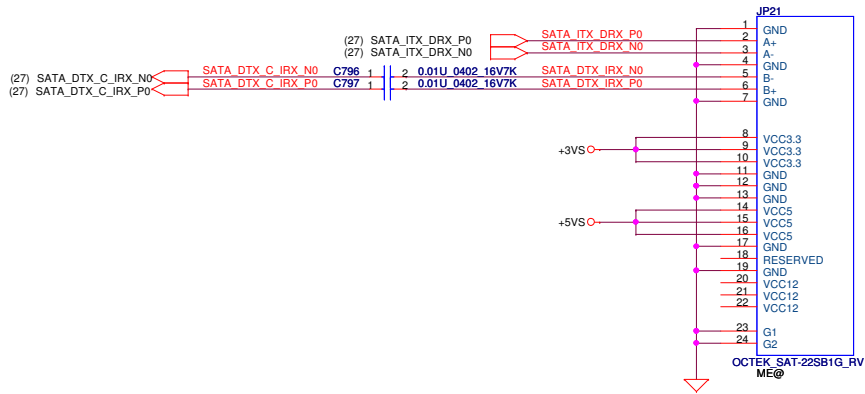


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Issued Date	2009/04/23	Deciphered Date	2010/05	LAN CONTROLLER	
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Date: Tuesday, April 28, 2009				Rev 1.0	Sheet 32 of 51

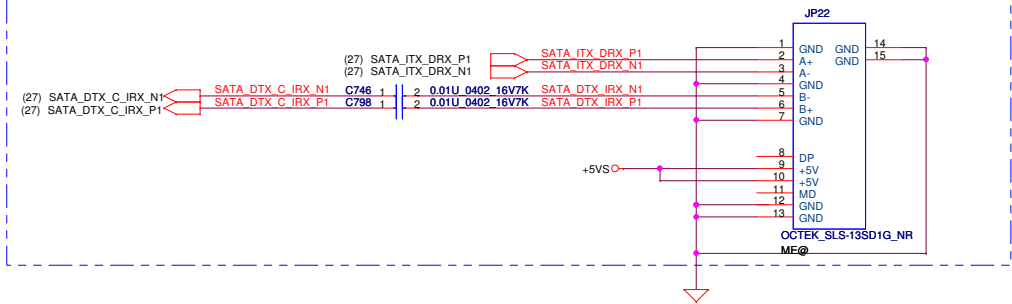




### SATA HDD Conn.



### SATA ODD Conn.



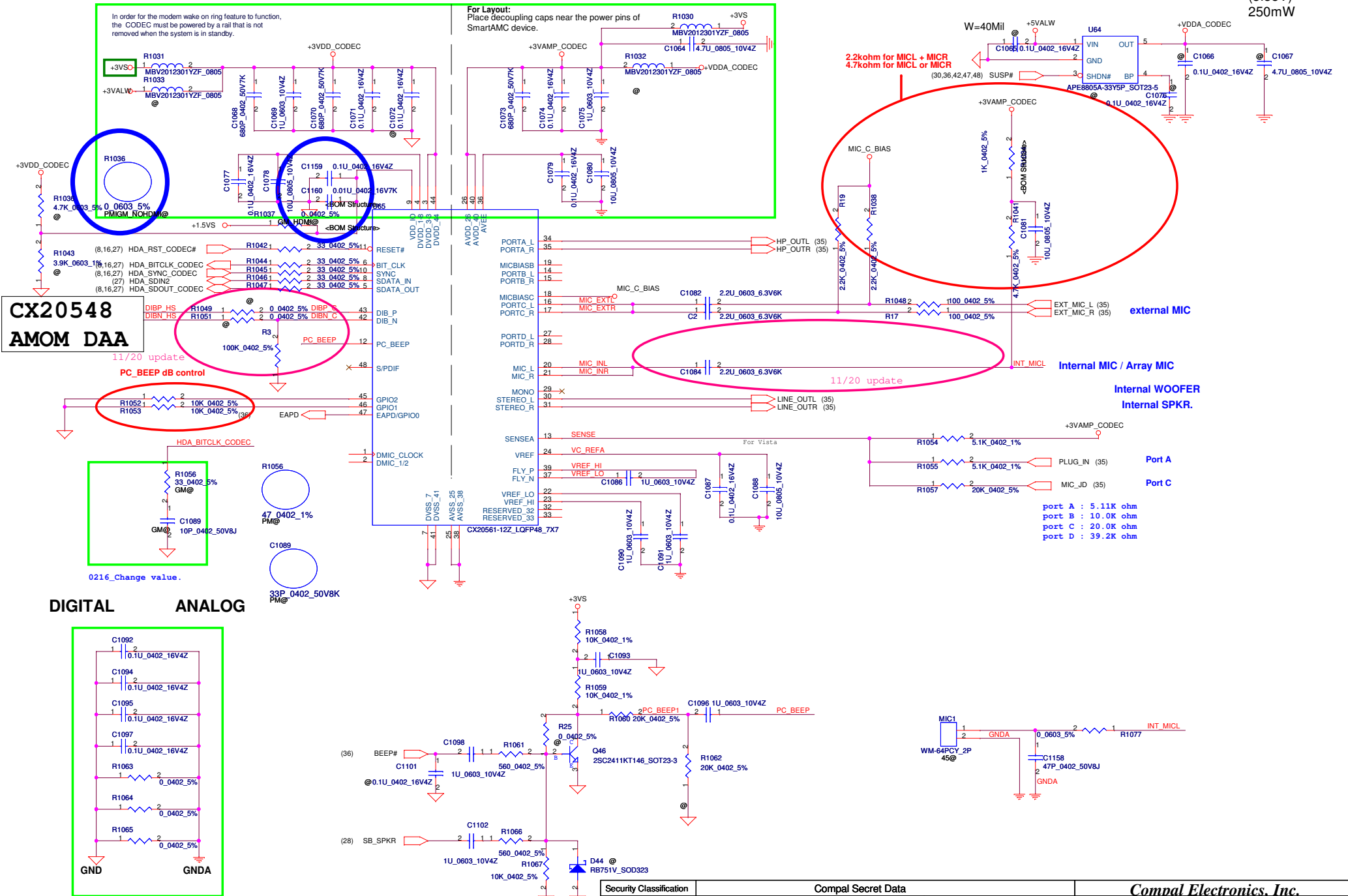
Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05	<b>Compal Electronics, Inc.</b> <b>HDD &amp; ODD Connector</b>	
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				<b>KIWA5/6 LA-5081P</b>	
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				Sheet 33	of 51

# AUDIO CODEC

0308\_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

# CODEC POWER

(3.33V)  
250mW



**CX20548  
AMOM DAA**

11/20 update  
PC\_BEEP dB control

100K\_0402\_5%  
R1052, R1053

HDA\_BITCLK\_CODEC  
R1056

0216\_Change value.  
C1089

47 0402\_1%  
R1056

33P 0402\_50V8K  
C1089

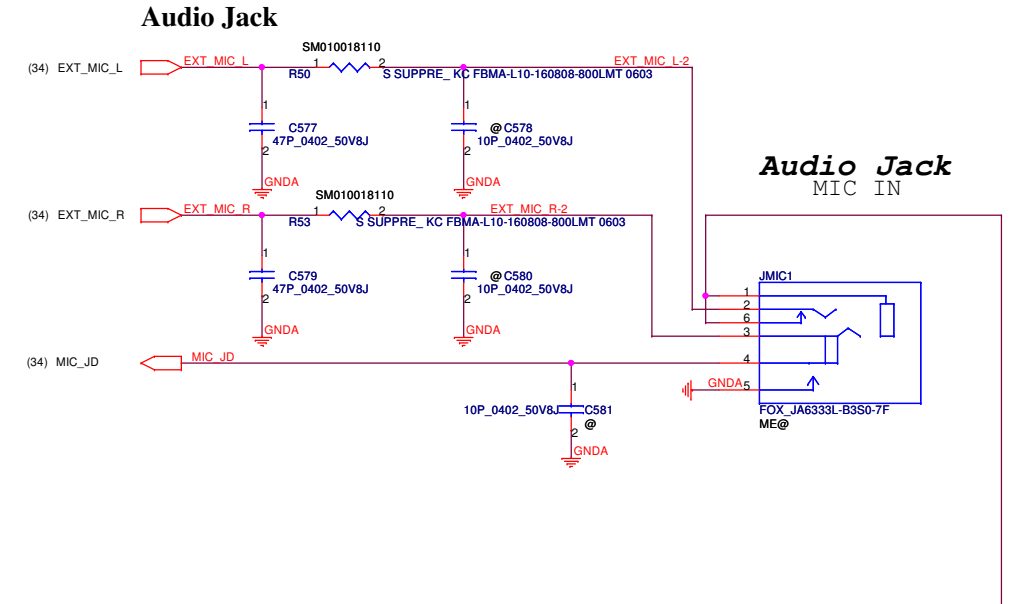
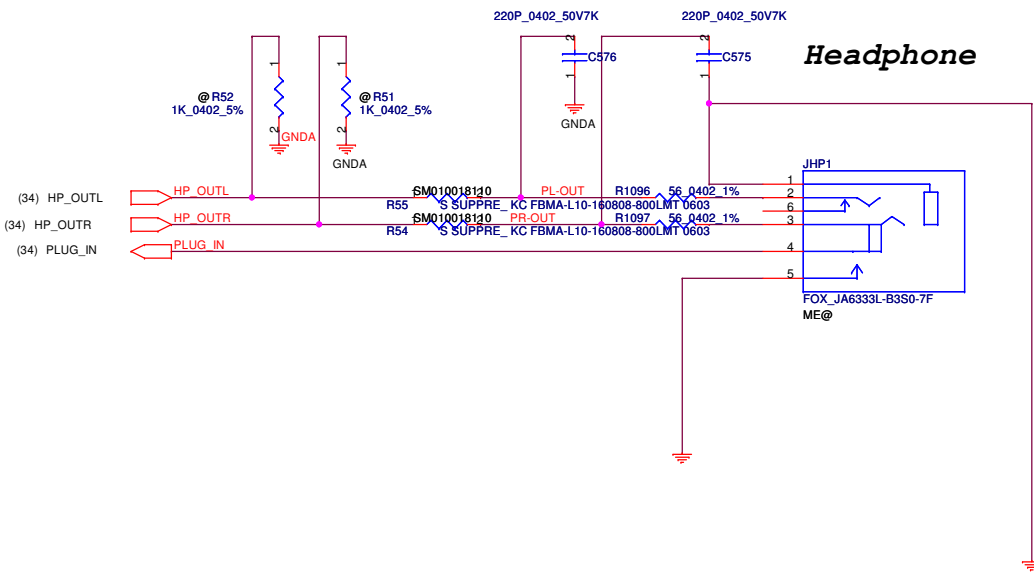
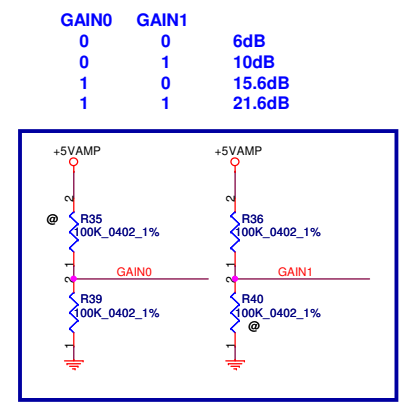
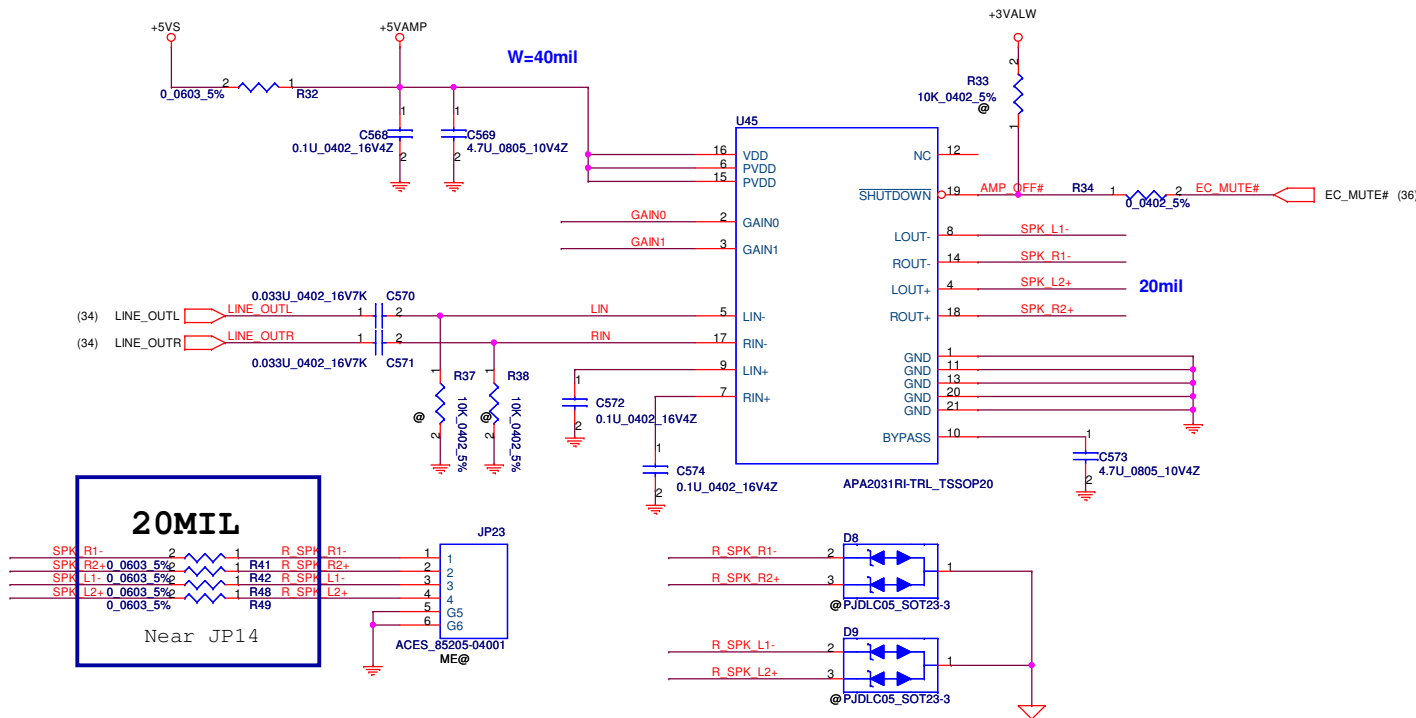
DIGITAL ANALOG

Place these C and R around AGND and DGND,  
then choose the one which is close to Codec  
to populate

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05
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Title <b>CX20561-AMOM Codec</b>			
Size	Document Number	Rev	
Custom	KIWA5/6 LA-5081P	1.0	
Date:	Tuesday, April 28, 2009	E/Sheet	34 of 51

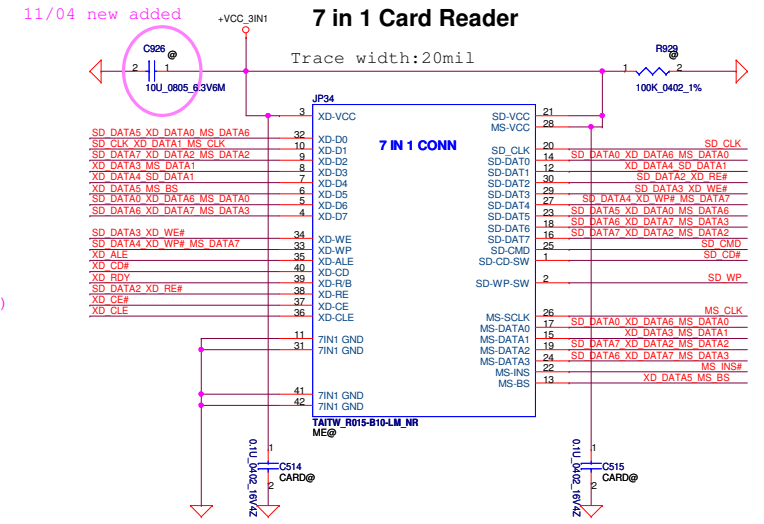
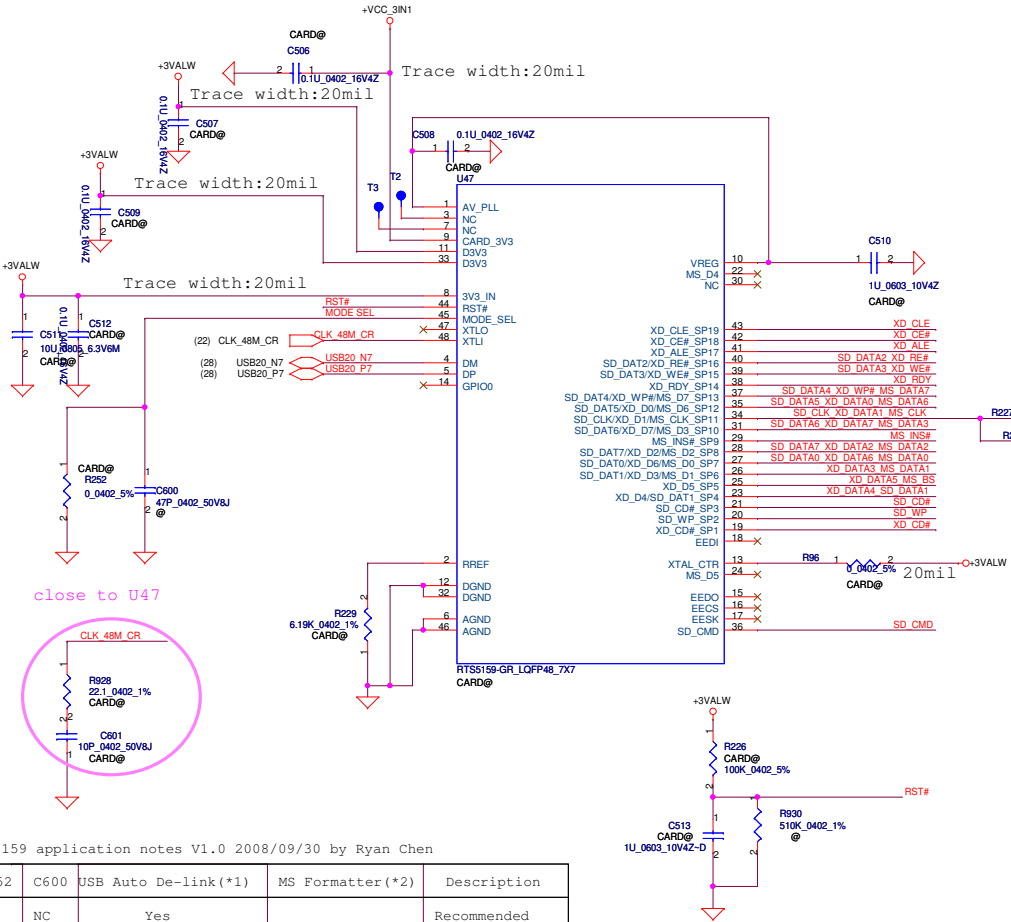
# Speaker Connector



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Issued Date	2009/04/23	Deciphered Date	2010/05	Title	AMP Audio speaker CONN
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# Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



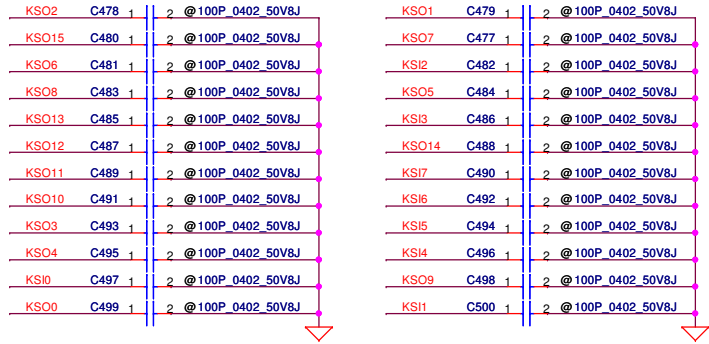
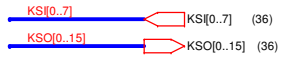
RTSS159 application notes V1.0 2008/09/30 by Ryan Chen

R252	C600	USB Auto De-link(*1)	MS Formatter(*2)	Description
0	NC	Yes		Recommended
NC	47pF	Yes	Yes	
NC	NC			Compatible with RTSS158E
NC	680pF	Yes		LED ON (*3)
10K	180pF			LED ON (*3)
10K	680pF		Yes	

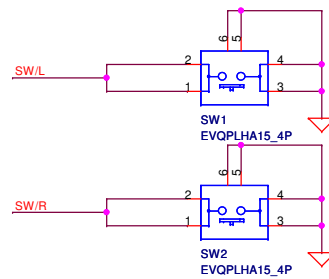
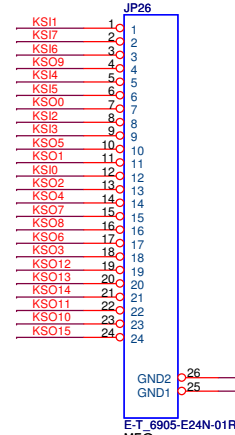
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2009/04/23	Deciphered Date	2010/05	USB_CR board			
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Source:SP01000IE00  
 2nd source:SP01000IF00  
 30 pin

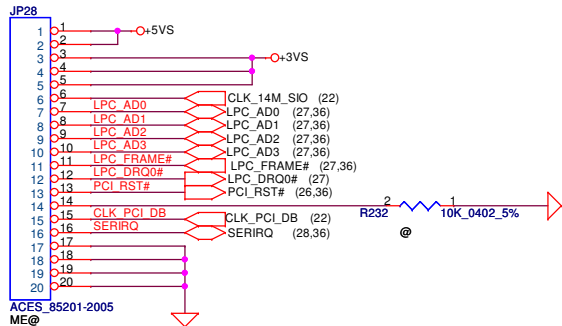
**INT\_KBD Conn.**



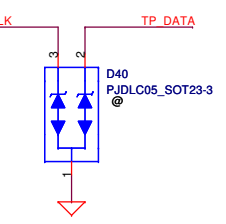
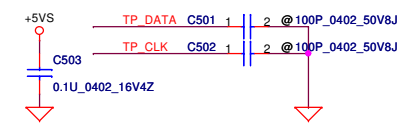
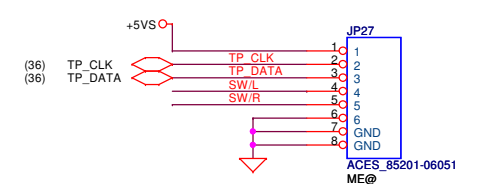
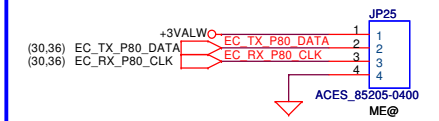
CONN PIN define need double check



**FOR LPC SIO DEBUG PORT**

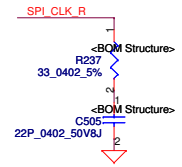
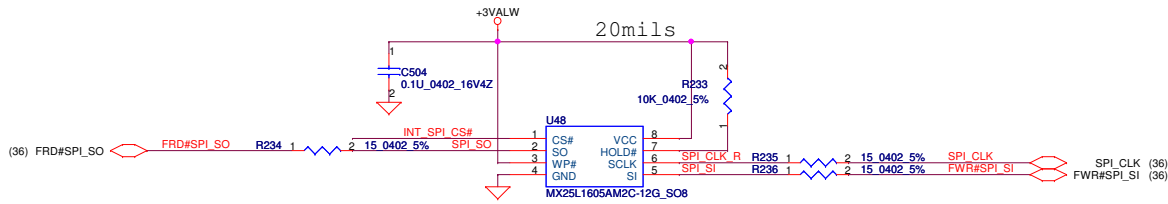


**EC DEBUG PORT**

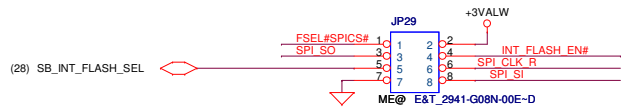
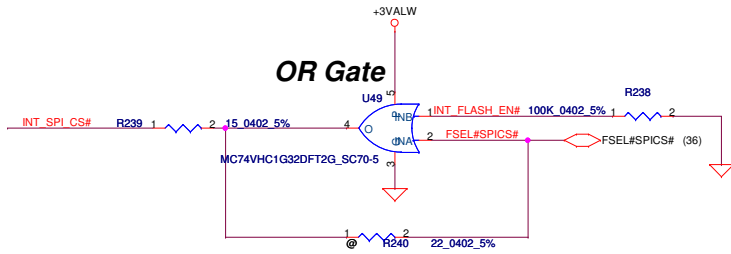


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Size	Document Number	Date		Rev	1.0
B	KIWA5/6 LA-5081P	Tuesday, April 28, 2009		Sheet	38 of 51

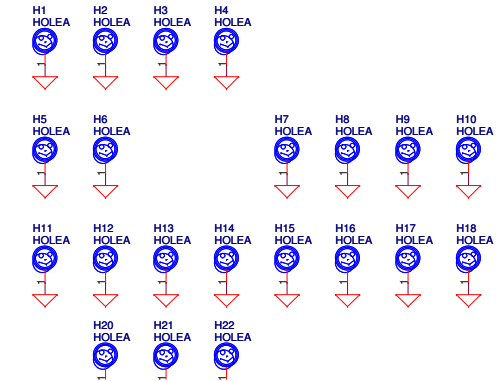
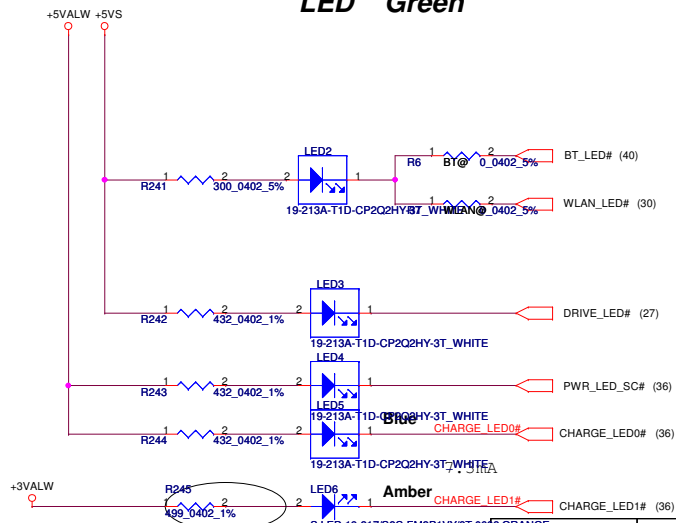
# FOR EC 16M SPI ROM



INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H



## LED Green

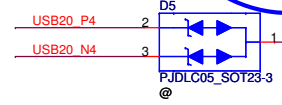
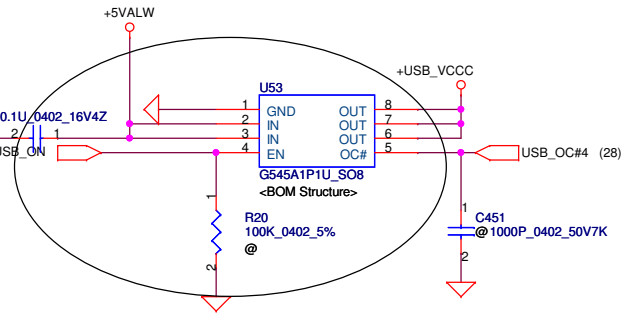
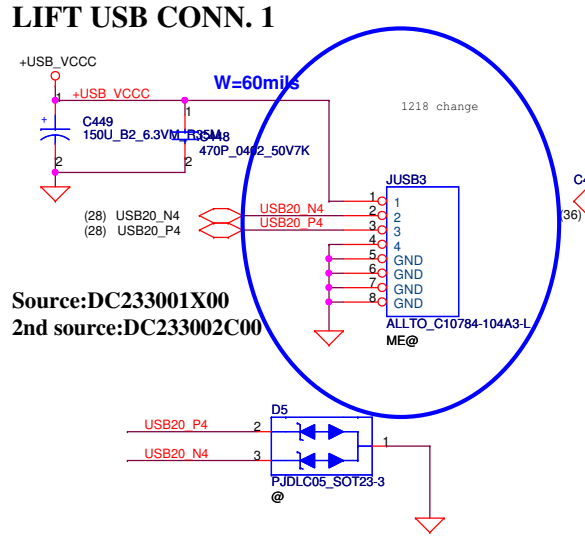
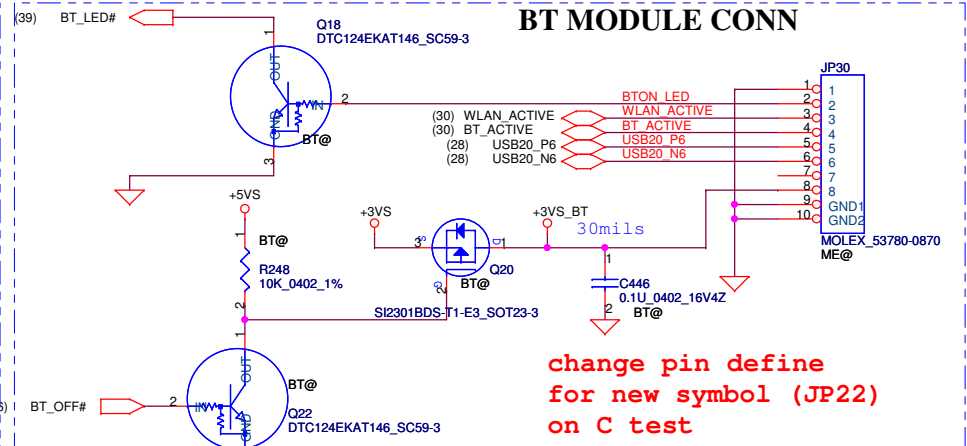
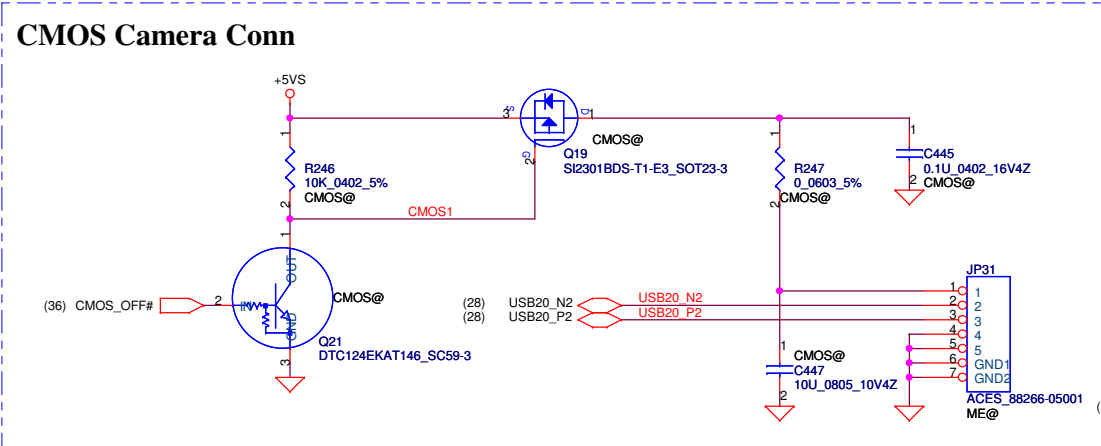
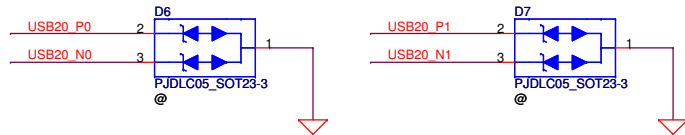
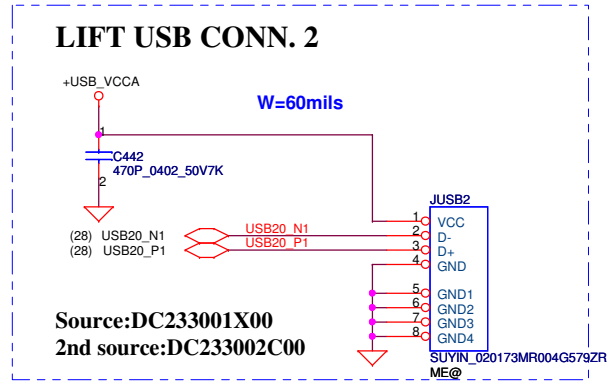
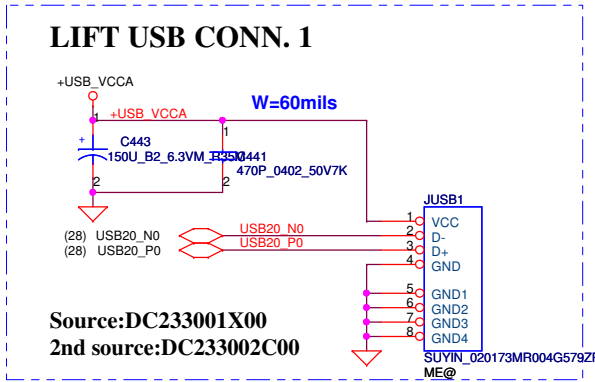
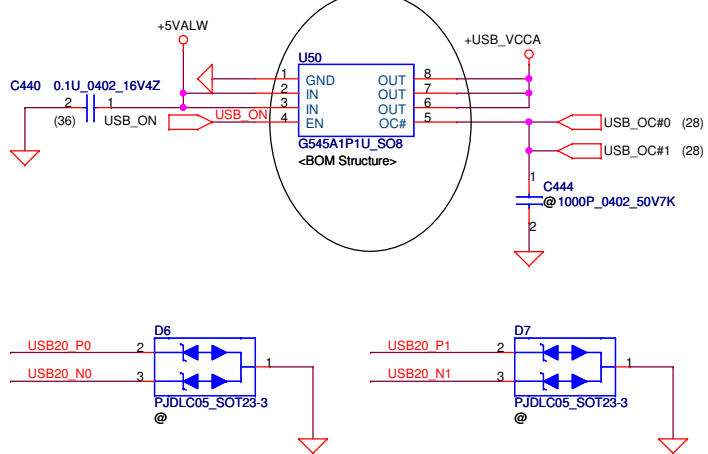


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Compal Electronics, Inc.

LED/EC SPI ROM

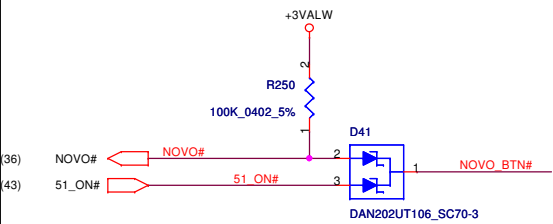
Date: Tuesday, April 28, 2009 Sheet 39 of 51



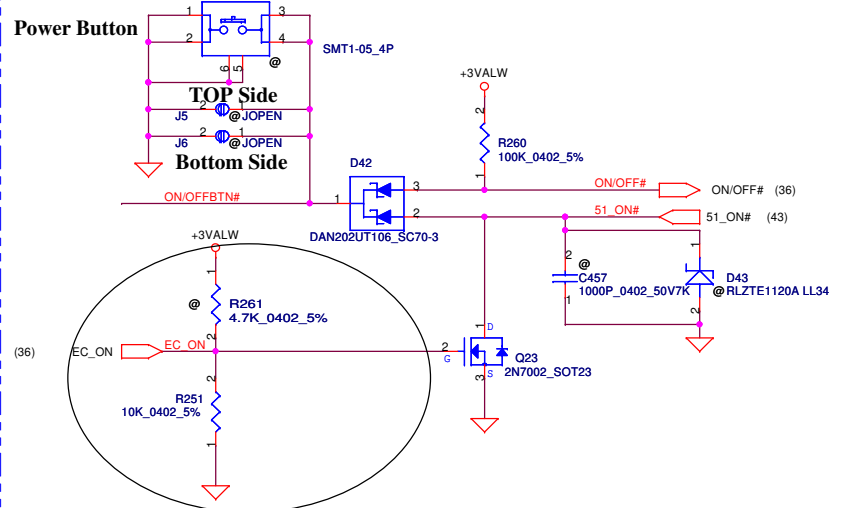
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Issued Date	2009/04/23	Deciphered Date
		2010/05
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Compal Electronics, Inc.		
Title Power OK, Reset and RTC Circuit, TP		
Size Custom	Document Number KIWA5/6 LA-5081P	Rev 1.0
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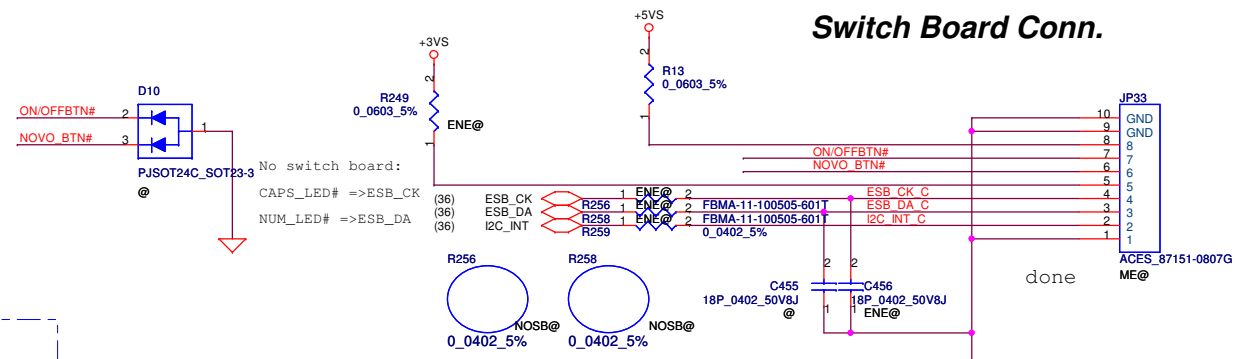
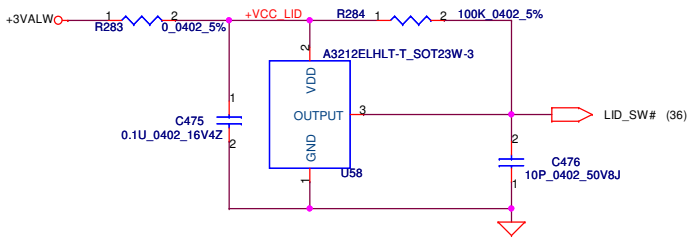




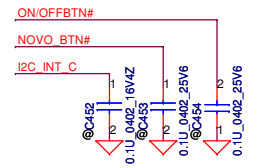
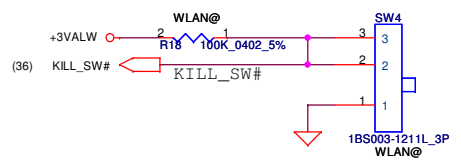
### ON/OFF switch



### Lid Switch

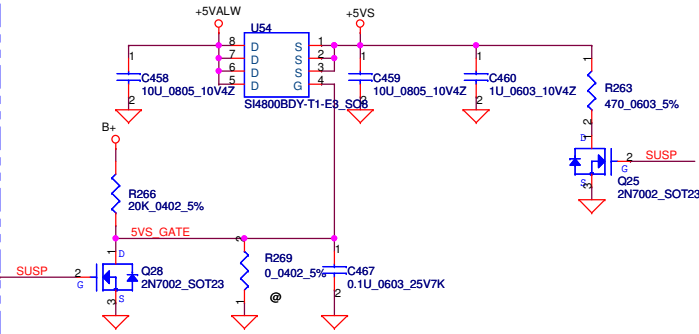


02/26 remove Smbus for CY  
Kill Switch

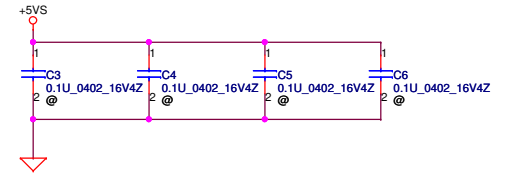
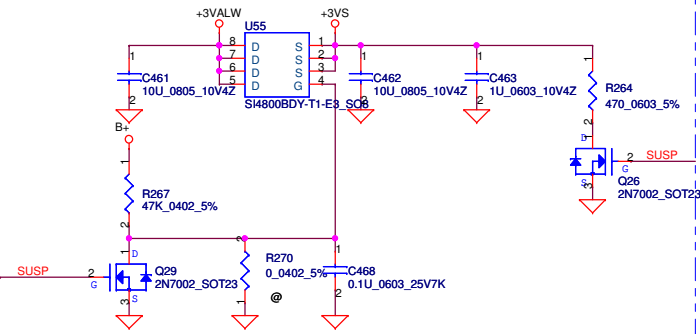


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Issued Date	2009/04/23	Deciphered Date	2010/05	Title
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Size Custom	Document Number	KIWA5/6 LA-5081P		Rev 1.0
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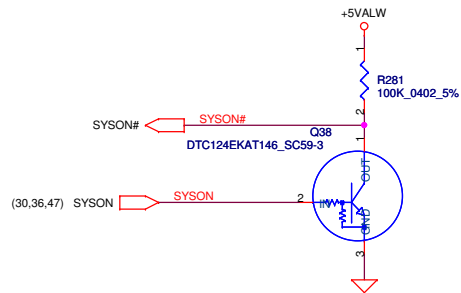
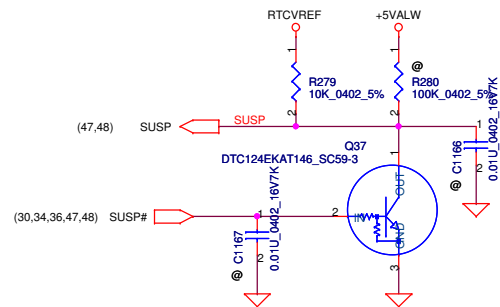
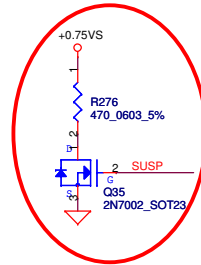
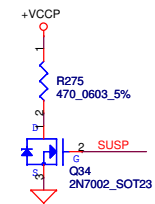
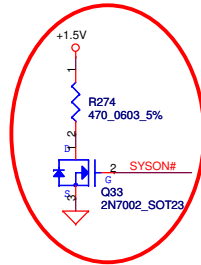
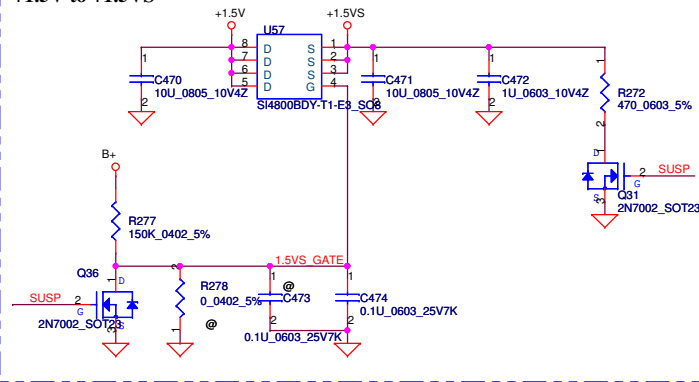
**+5VALW TO +5VS**



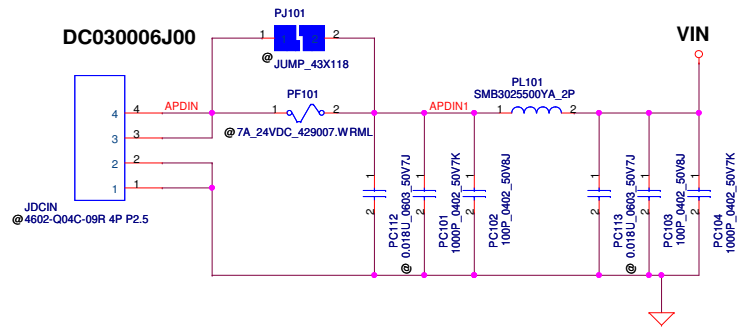
**+3VALW TO +3VS**



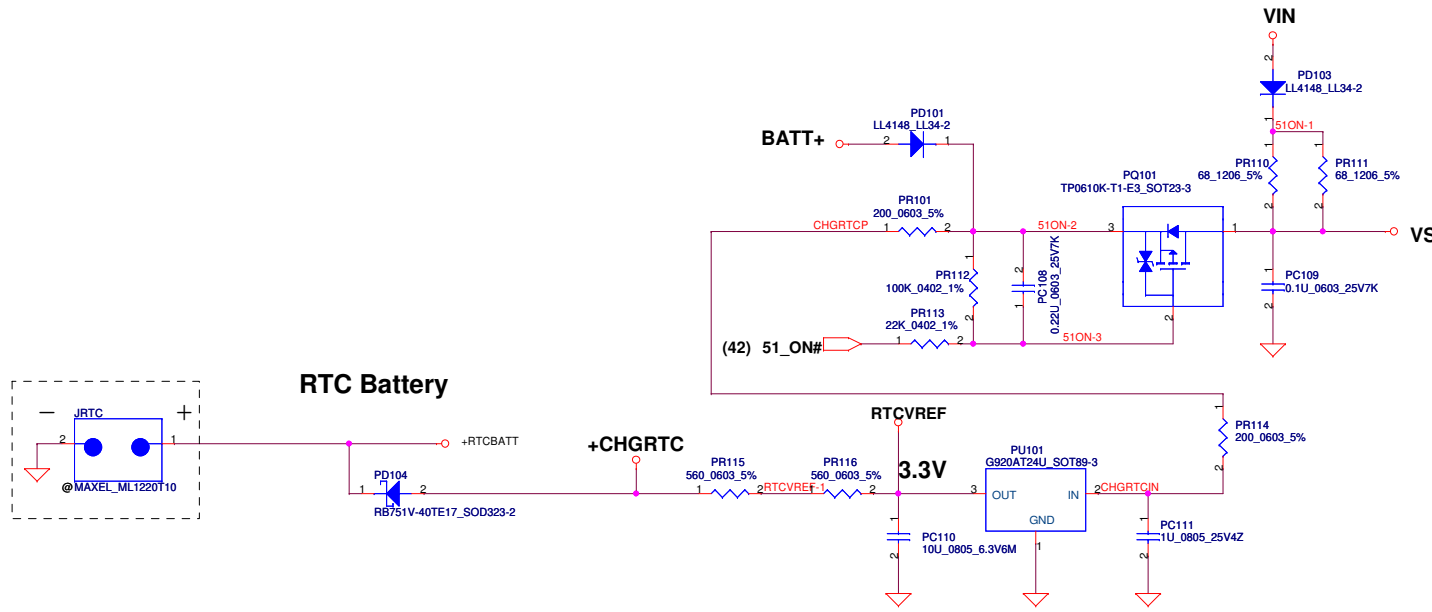
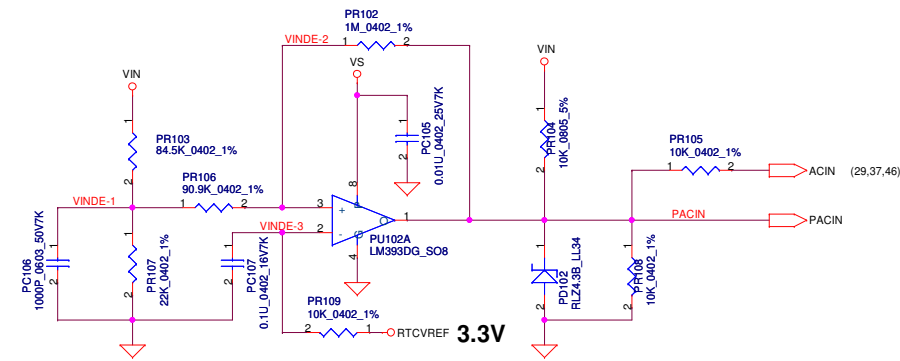
**+1.5V to +1.5VS**



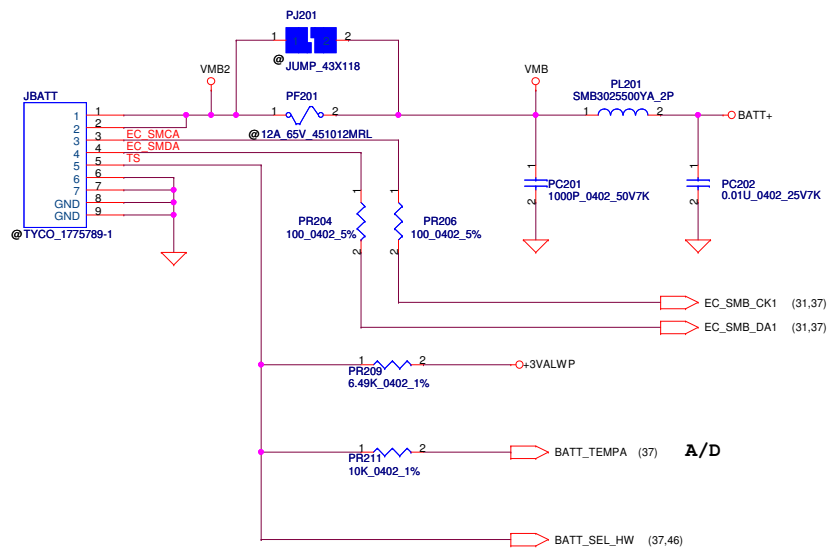
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Issued Date	2009/04/23	Deciphered Date	2010/05	Title	
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Size	Document Number	Rev		1.0	
Custom	KIWA5/6 LA-5081P				
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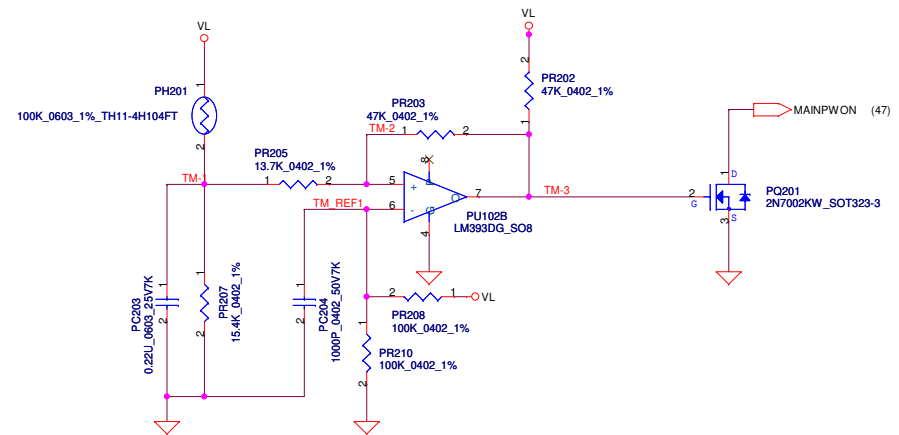
Vin Detector		
High	17.944	17.706
Low	16.242	16.027
	17.470	15.808



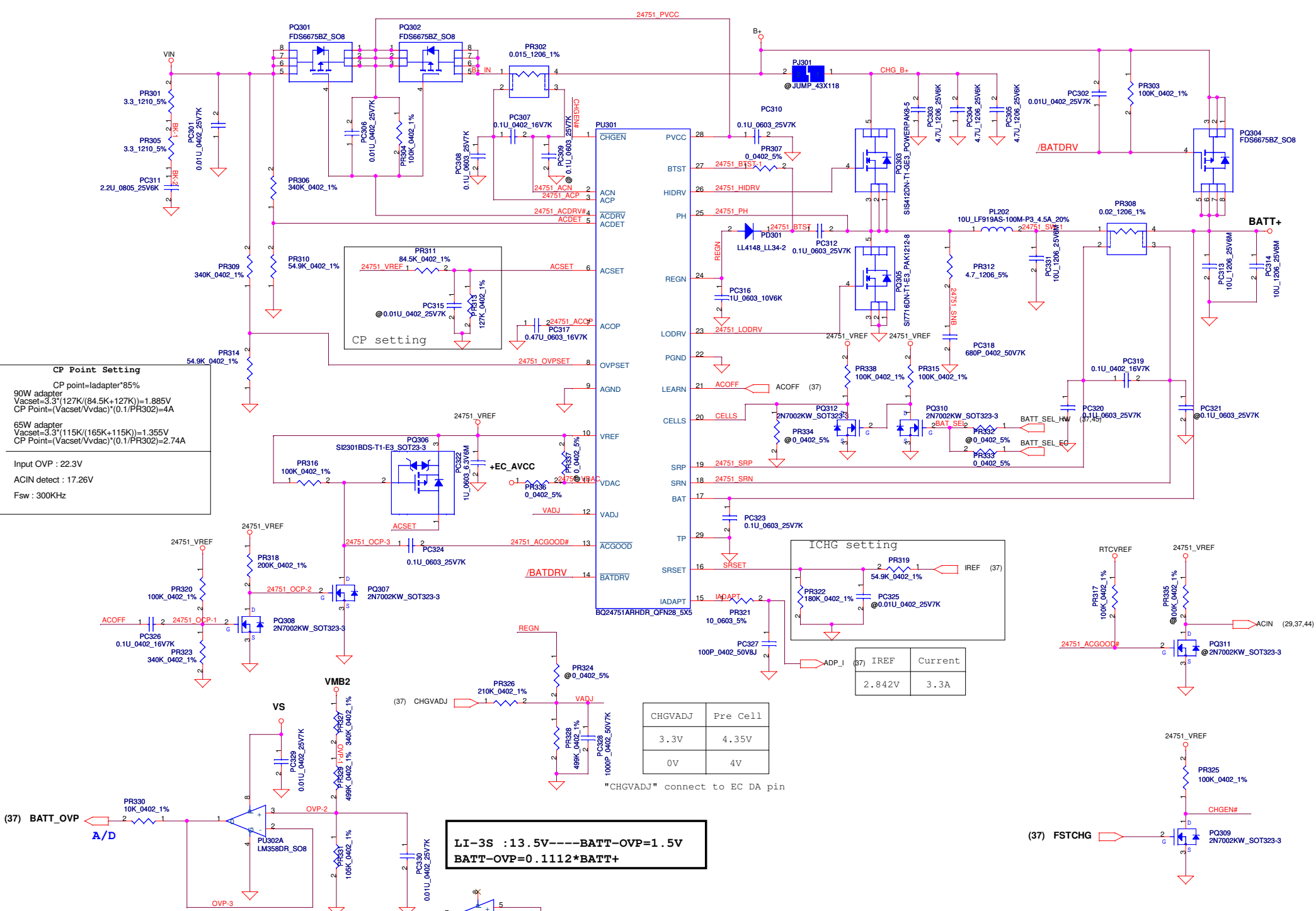
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**PH1 under CPU bottom side :**  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



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Size	Document Number			Rev	
				0.1	
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**CP Point Setting**

CP point=ladapler\*85%

90W adapter  
 $V_{acset}=3.3*(127K/(84.5K+127K))=1.885V$   
 $CP\ Point=(V_{acset}/V_{vdac})*(0.1/PR302)=4A$

65W adapter  
 $V_{acset}=3.3*(115K/(165K+115K))=1.355V$   
 $CP\ Point=(V_{acset}/V_{vdac})*(0.1/PR302)=2.74A$

Input OVP : 22.3V  
 ACIN detect : 17.26V  
 Fsw : 300KHz

**ICHG setting**

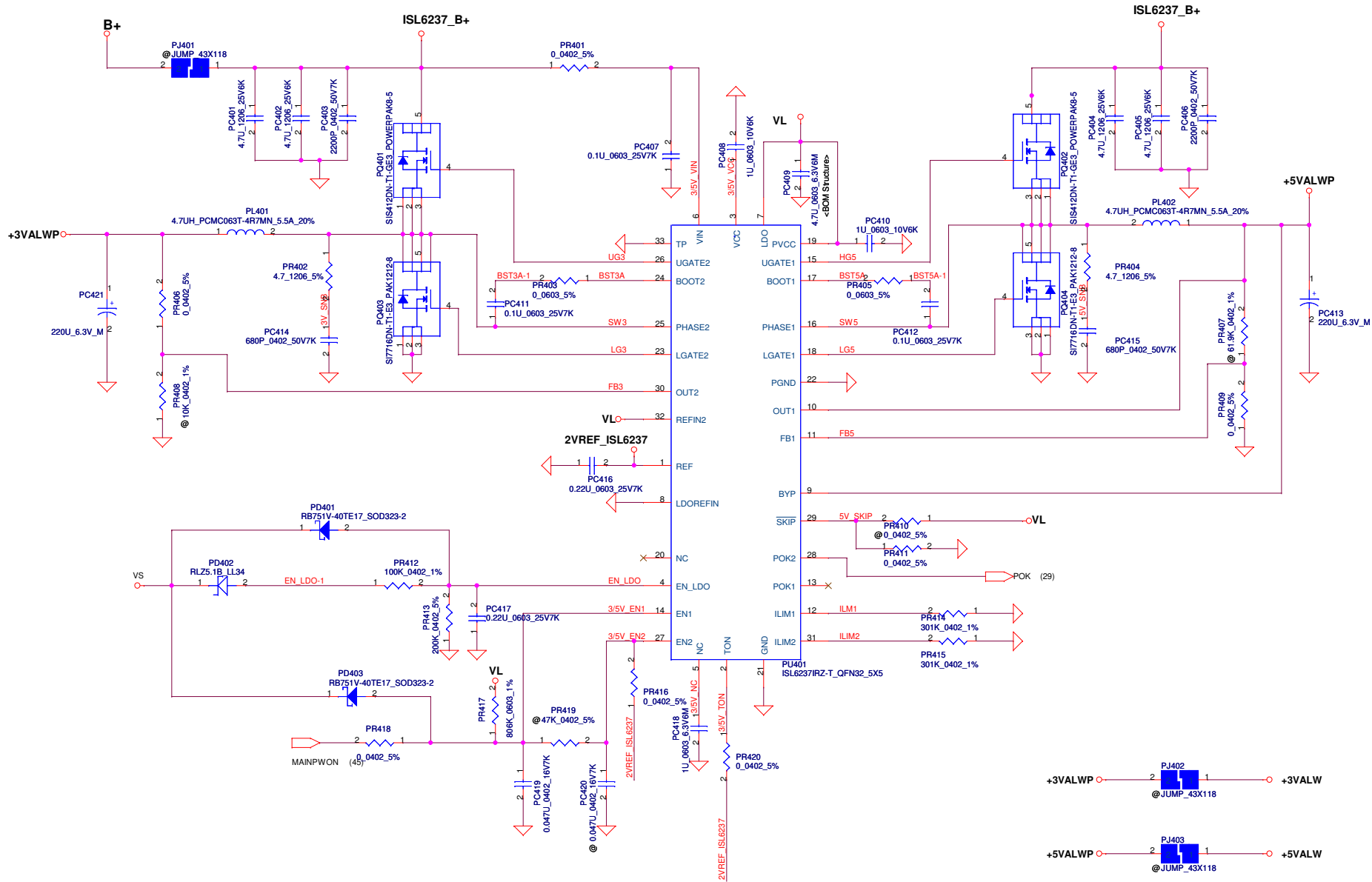
PR319 54.9K\_0402\_1% IREF (37)  
 PR322 180K\_0402\_1%  
 PC325 @0.01U\_0402\_25V7K

ADP_I (37) IREF	Current
2.842V	3.3A

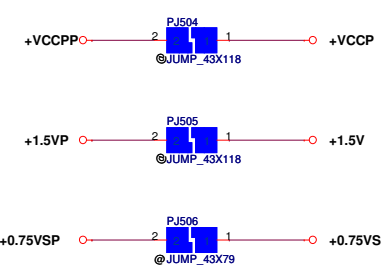
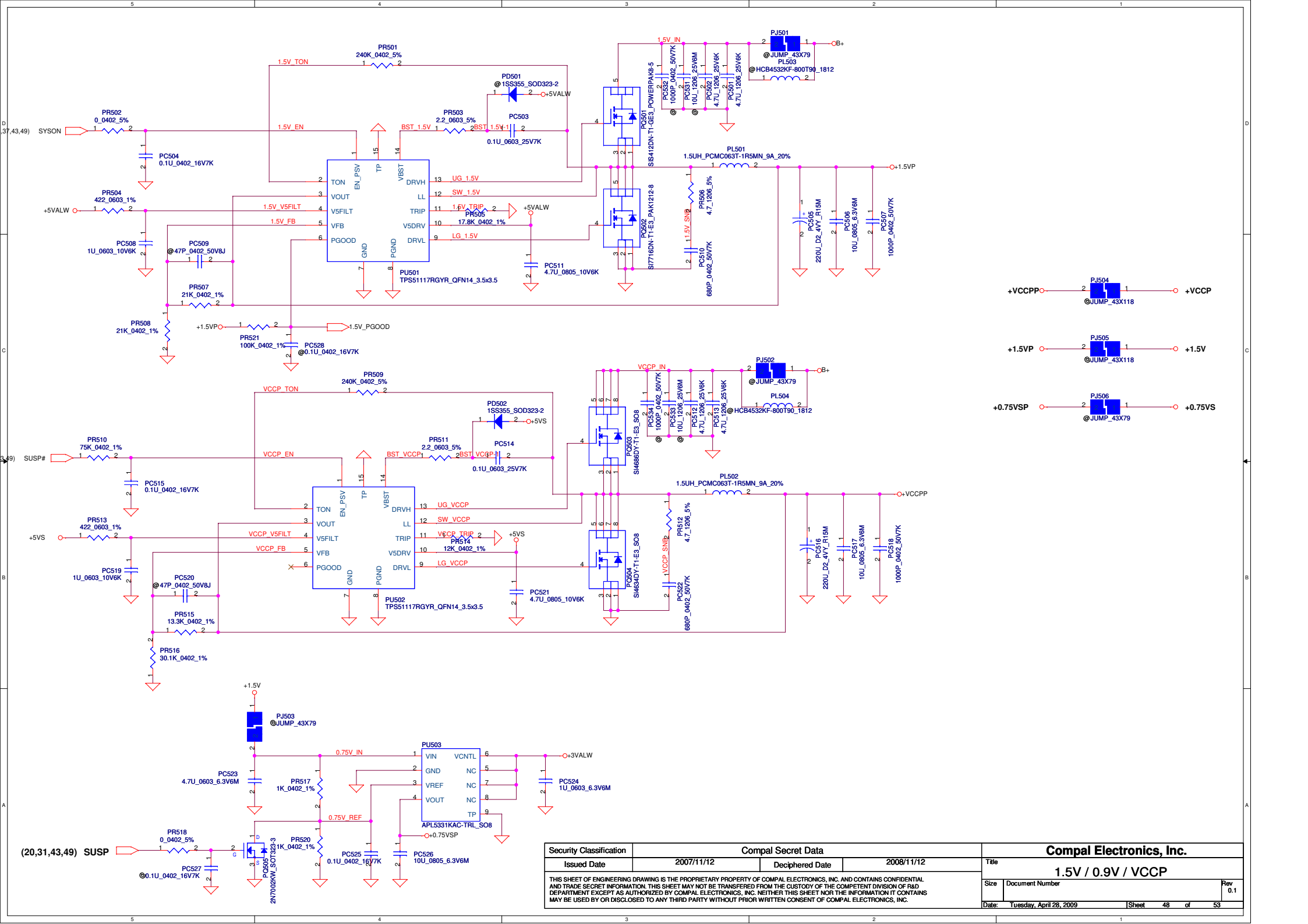
CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

"CHGVADJ" connect to EC DA pin

**LI-3S : 13.5V --- BATT-OVP=1.5V**  
**BATT-OVP=0.1112\*BATT+**

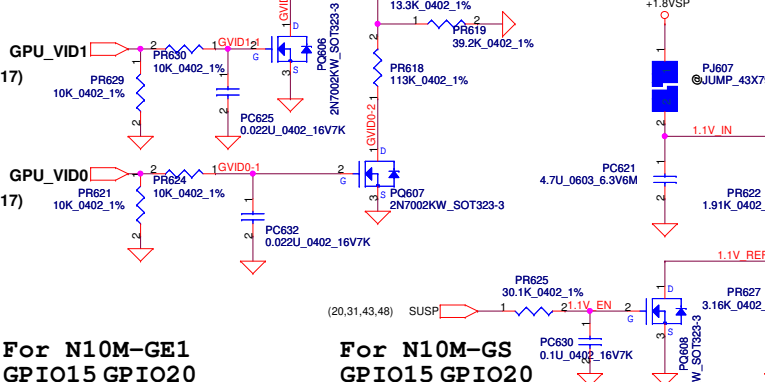
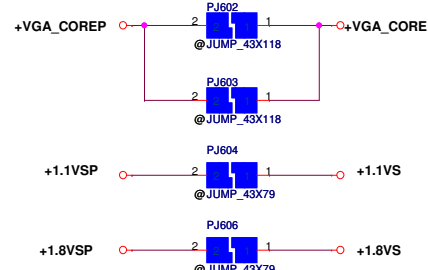
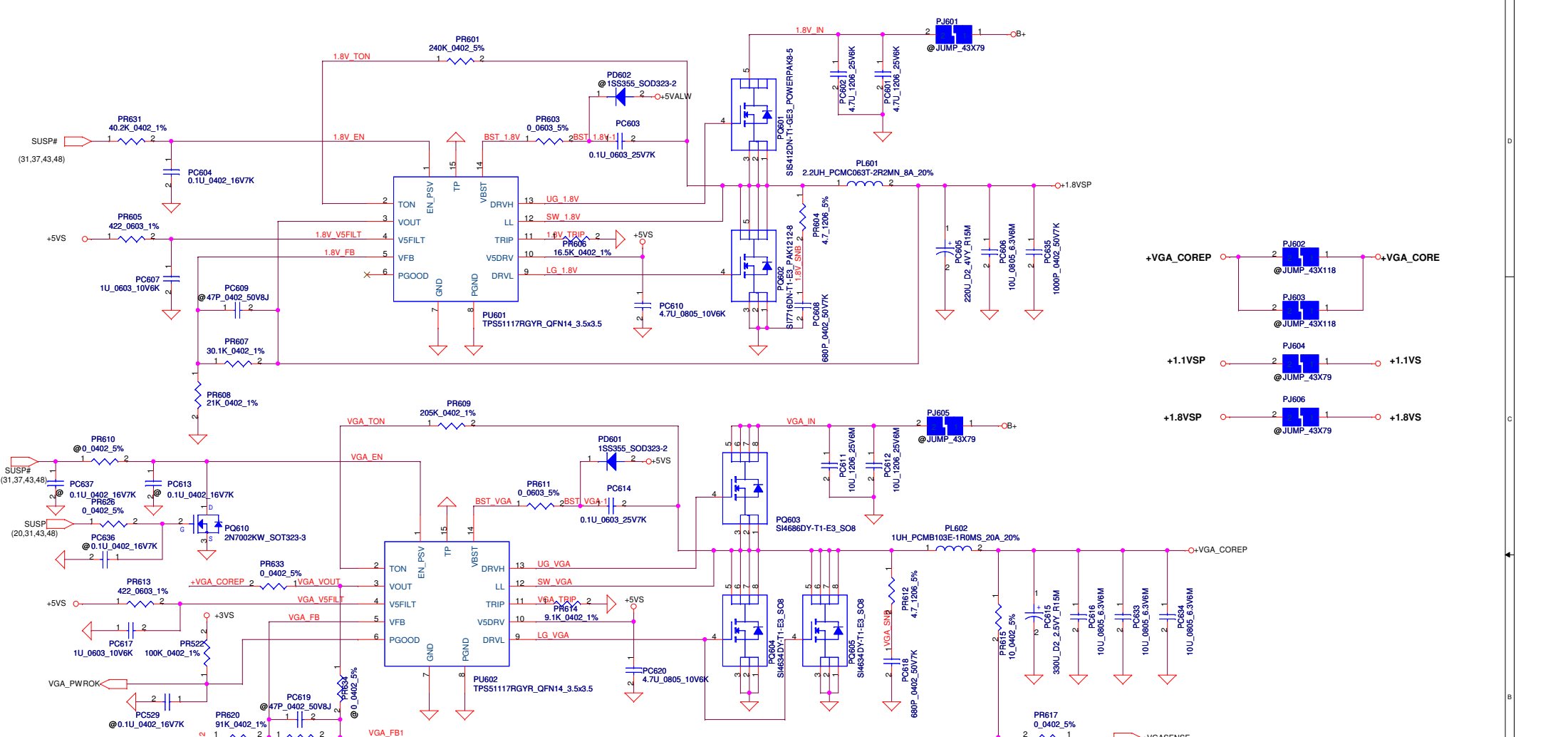


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(20,31,43,49) SUSP

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				1.5V / 0.9V / VCCP	
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PR616=>9.09K  
 PR622=>2.21K  
 PR629, PR630, PC625, PQ606, PR620=>un-pop  
 PR621, PR624, PC632, PQ607, PR618=>un-pop

For N10M-GE1  
 GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS  
 GPIO15 GPIO20

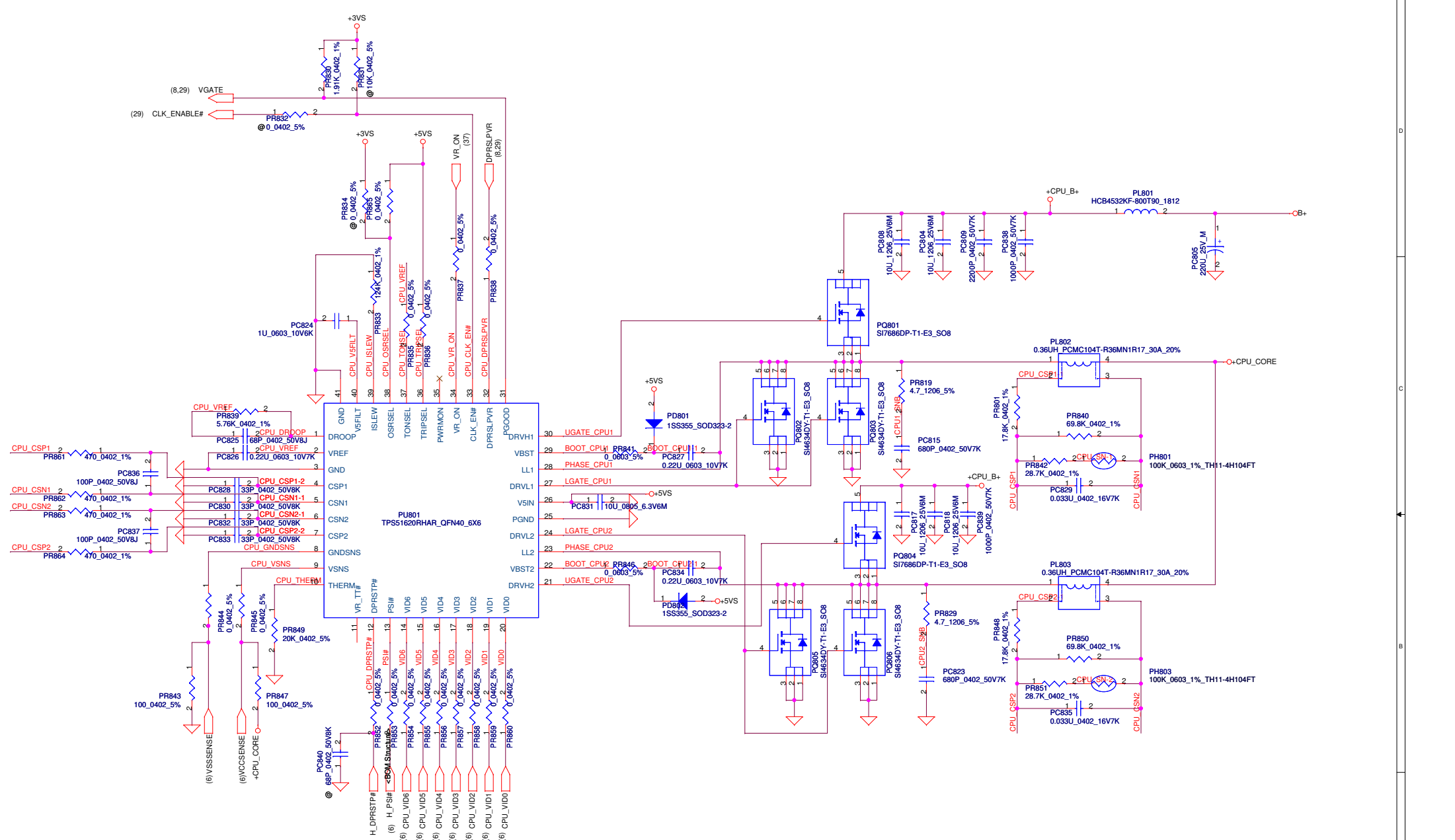
GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
0	1	0.9V
1	1	1.0V

Security Classification	Compal Secret Data	
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)	2009.01.14	
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MODIFICATION LIST

PURPOSE

1	12/10	39	Remove D11, and add R6, R7		
	12/10	36	change PWR_LED_SC# from U46.38 to U46.34		
2	1/15	39	modify H18 hold size, and change the H5、H6 and H18 hold type.		
		42	add 4 CAPs C3, C4, C5 and C6 for EMI.		
		35	change C572 and C574 footprint from 0603 to 0402.		
		34	add R25 for BEEP# test		
3	3/16	06	add R1089, C1162 and H_DPRSTP#_R add C1163, C1164, and C1165 for EMC request.		
		08	change H_DPRSTP# to H_DPRSTP#_R		
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU R999 change to 24.9K		
		23	add R1095 pull high		
		35	swap HP_OUTL and HP_OUTR		
		36	add R1090, R1091, R1092, R1093 CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R		
		41	add R256, R258 Bom configuration Remove CY SMBus		
		42	add C1166, C1167 for EMC request.		
		4	4/20	27	R829 changed to 0ohm.
				08	R80 changed to 33ohm
34	R1044 changed to 33ohm R1056 changed to 33ohm C1089 changed to 10P				

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