

JIWA1/A2

Compal Schematics Document **Confidential**

Mobile Penryn uFCPGA

Intel Cantiga_GM/PM+ICH9-M

Wednesday, May 14, 2008

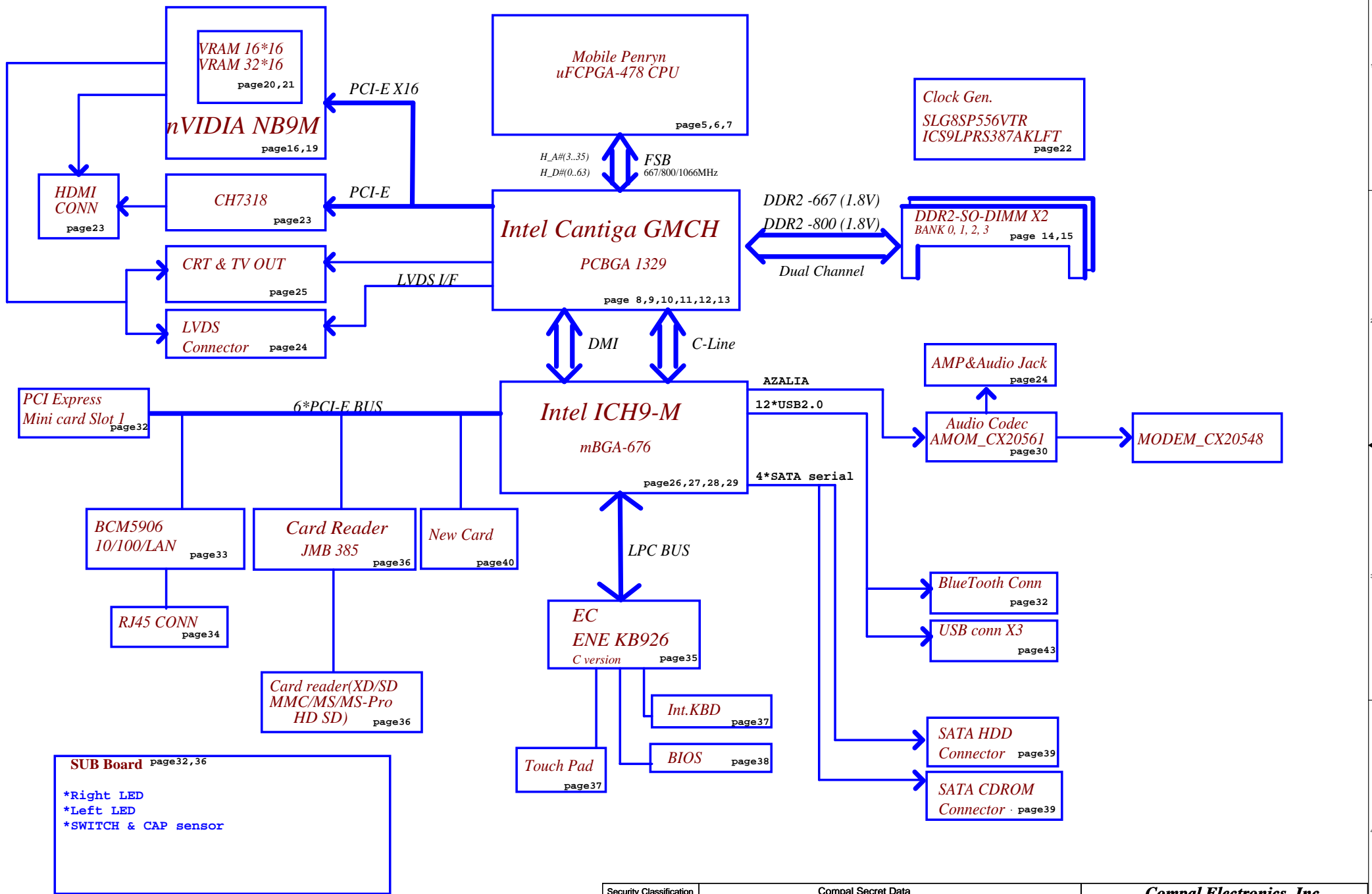
REV:1.0

Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Cover Sheet	
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Right LED Board

Switch & CAP SENSE LEDs Board

Left LED Board



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				MB Block Diagram		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

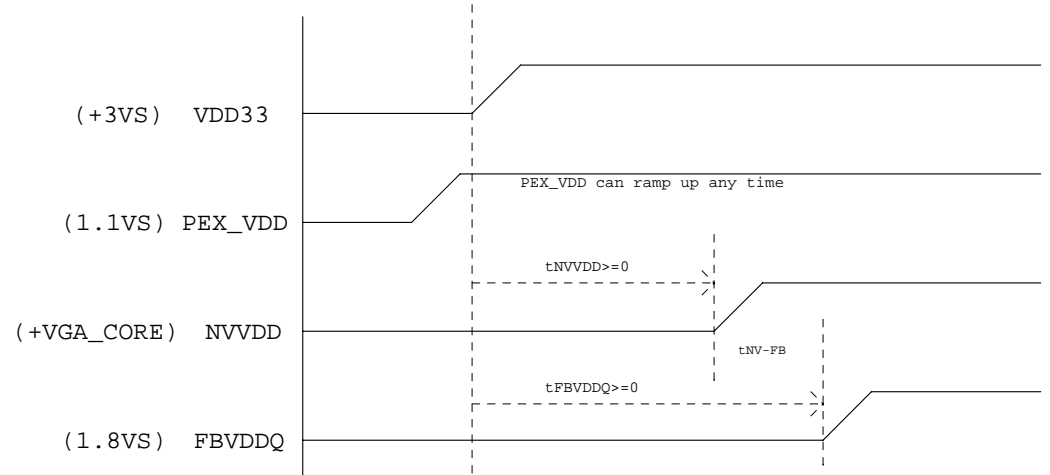
EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVDD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.225A			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
TOTAL	3.3	0.645A			

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

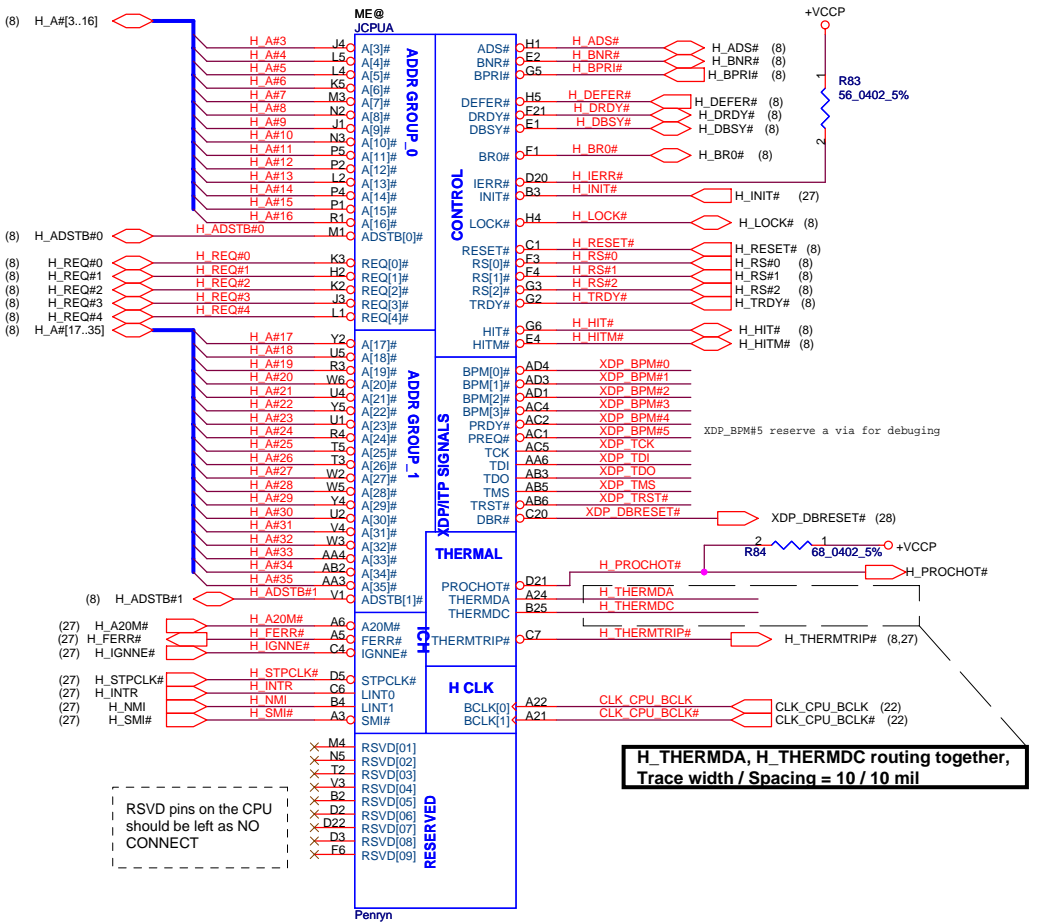
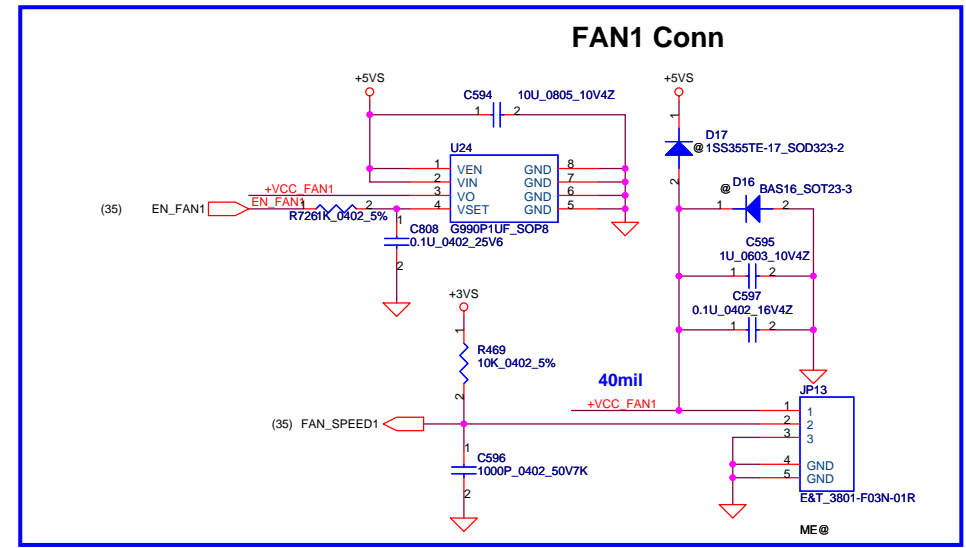
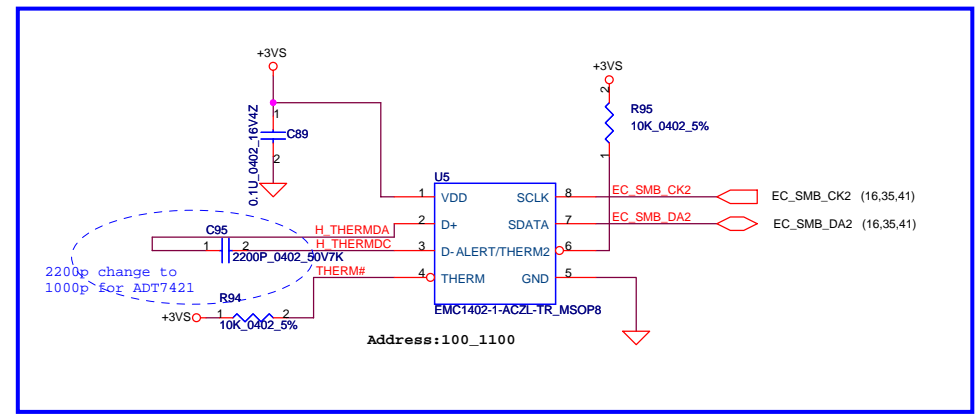
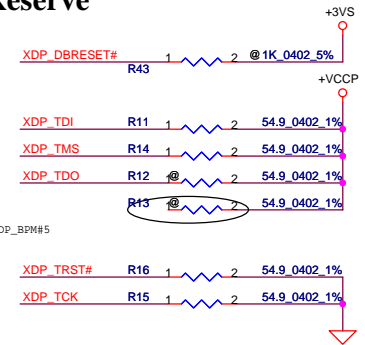
POWER SEQUENCE

The ramp time for any rail must be more than 40us



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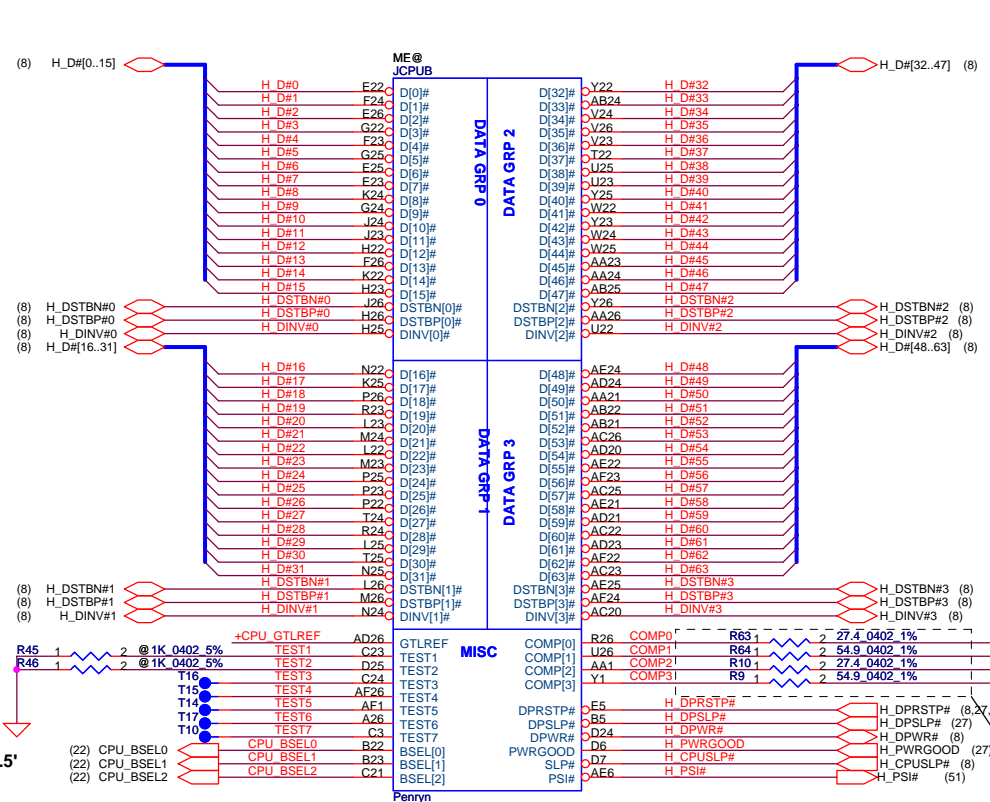
XDP Reserve



H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

RSVD pins on the CPU should be left as NO CONNECT

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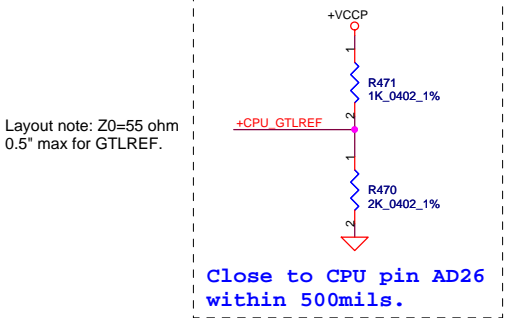


Trace Close CPU < 0.5'

Width=4 mil ,
Spacing: 15mil
(55Ohm)

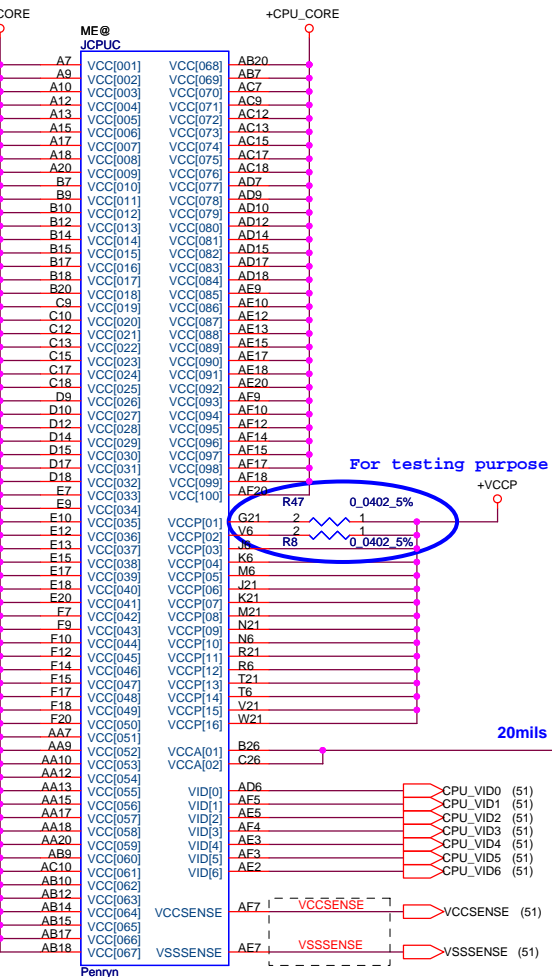
TRACE CLOSELY CPU < 0.5'
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs



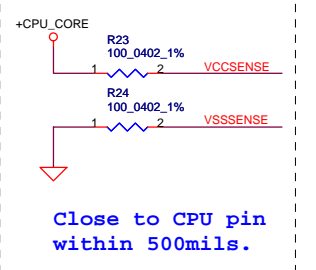
Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



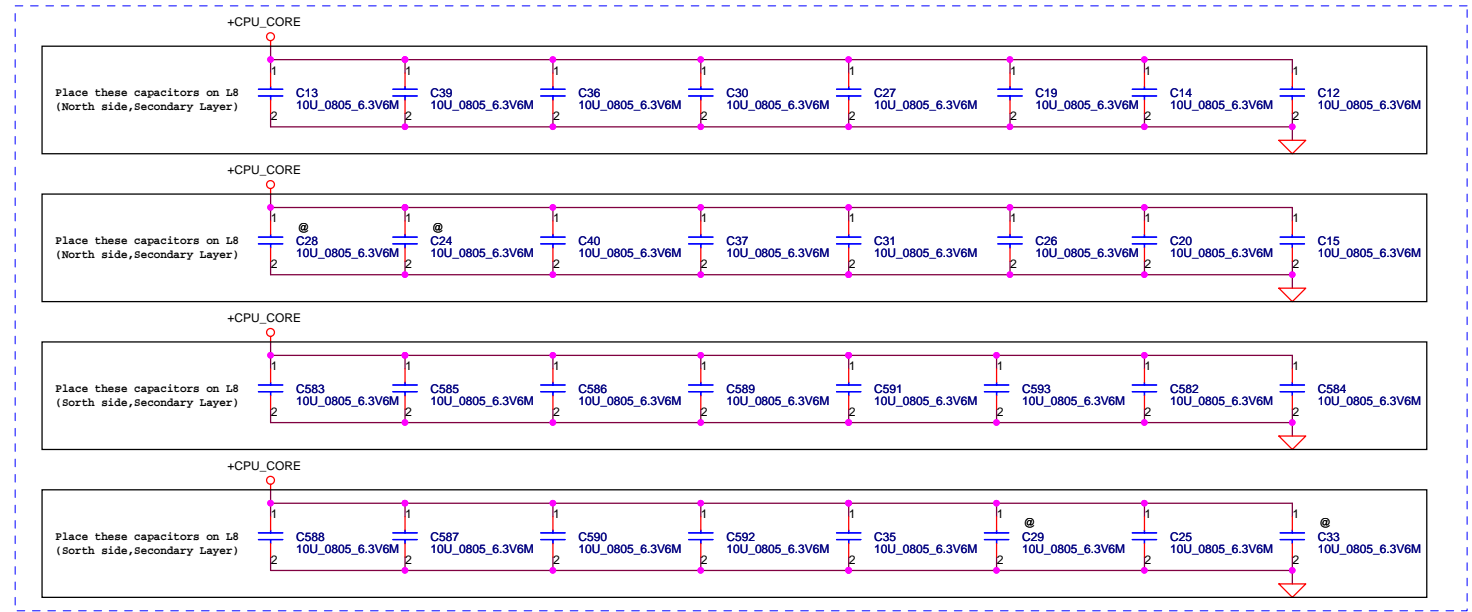
Length match within 25 mils.
The trace width/space/other is
16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

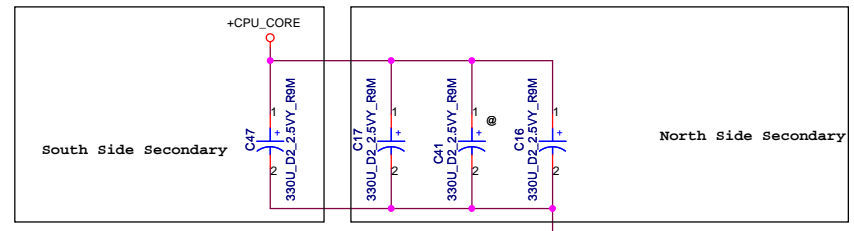


Close to CPU pin
within 500mils.

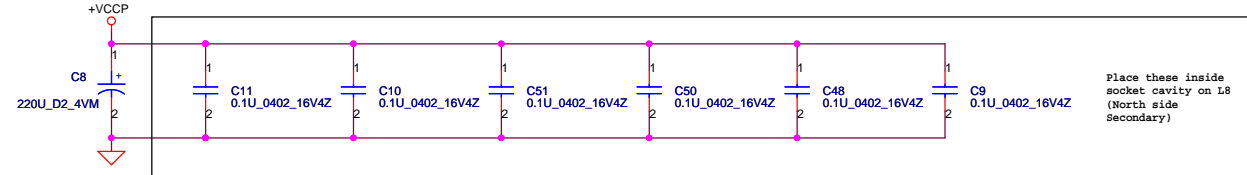
ME@	JCPU	VSS	Pin
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
H3	VSS[056]	VSS[137]	AD5
H6	VSS[057]	VSS[138]	AD8
H21	VSS[058]	VSS[139]	AD11
H24	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
	VSS[081]	VSS[163]	AF25



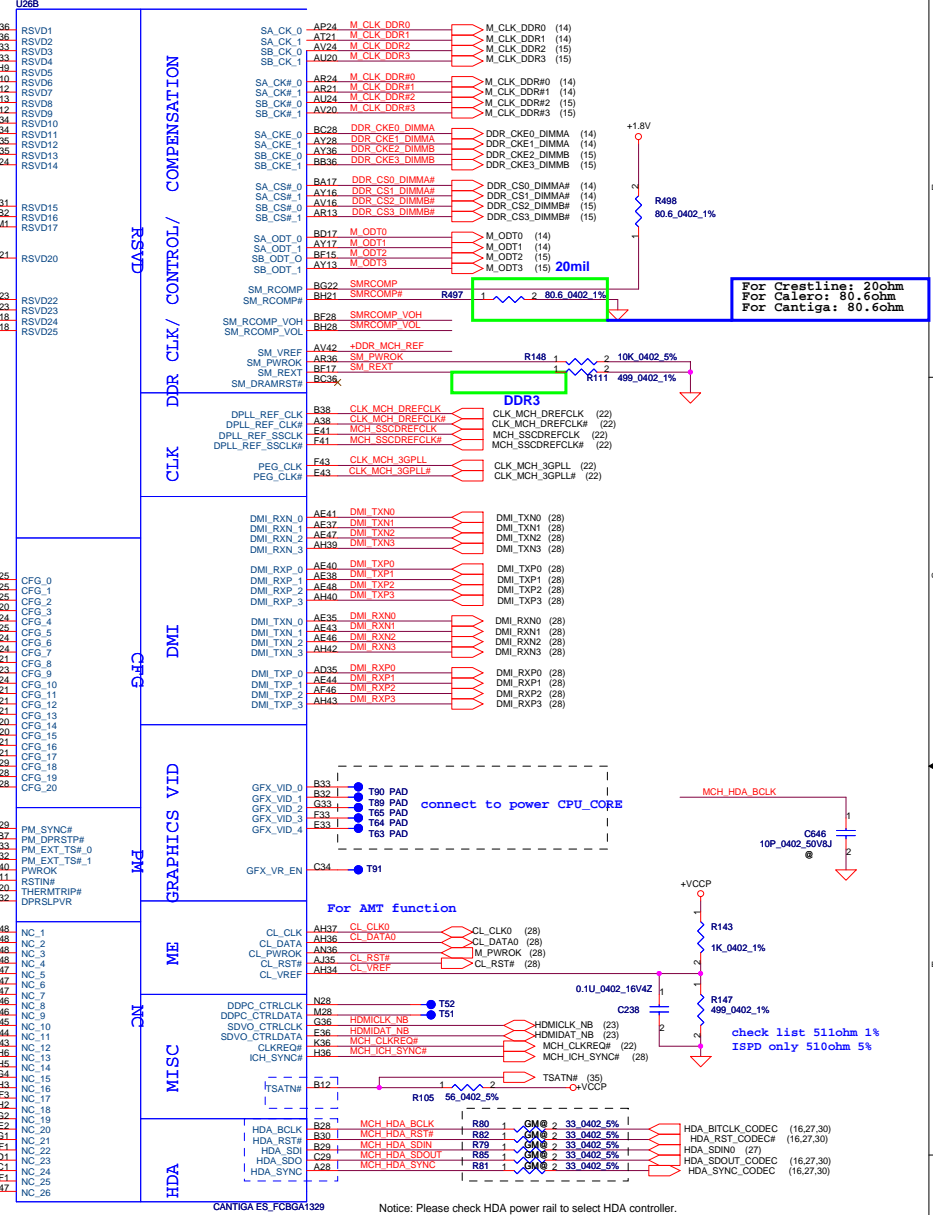
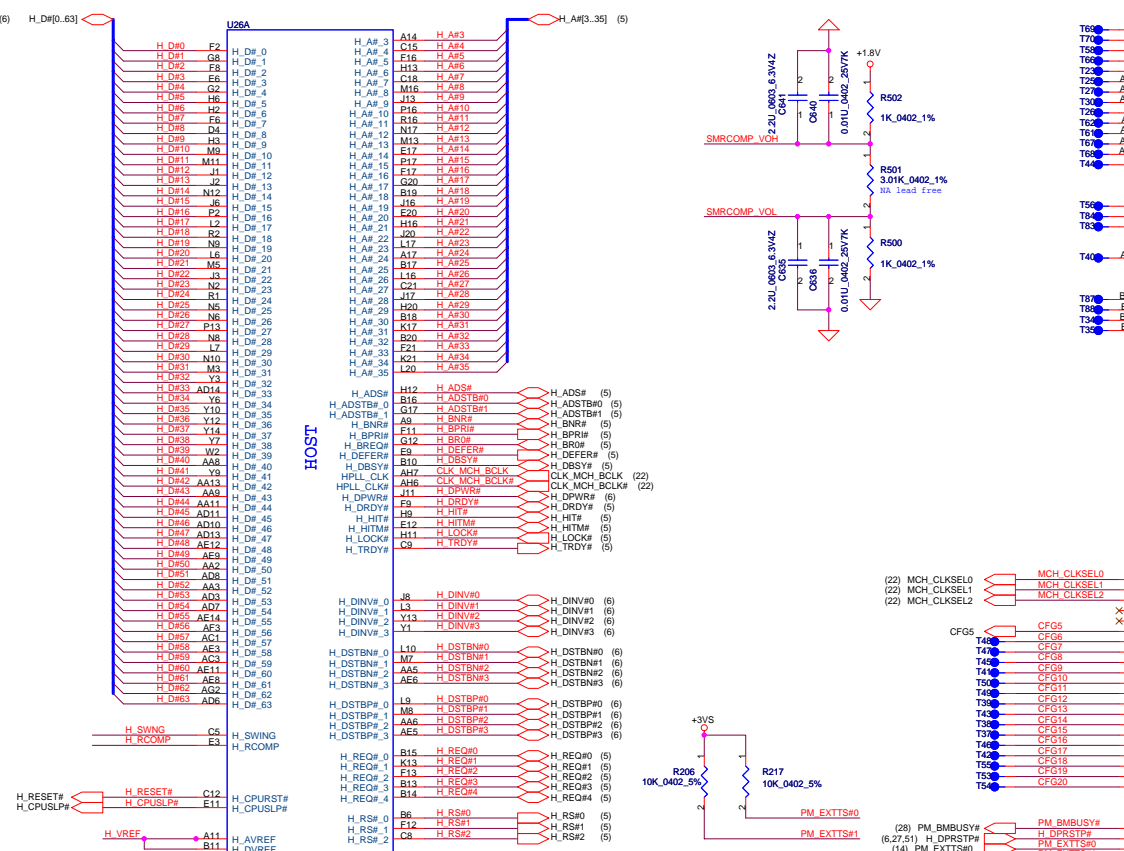
Mid Frequency Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

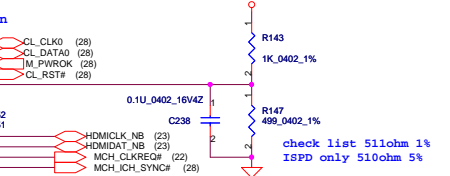
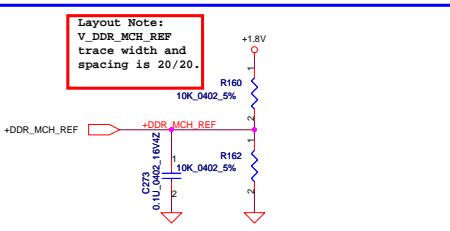
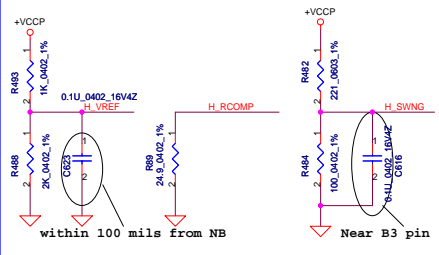


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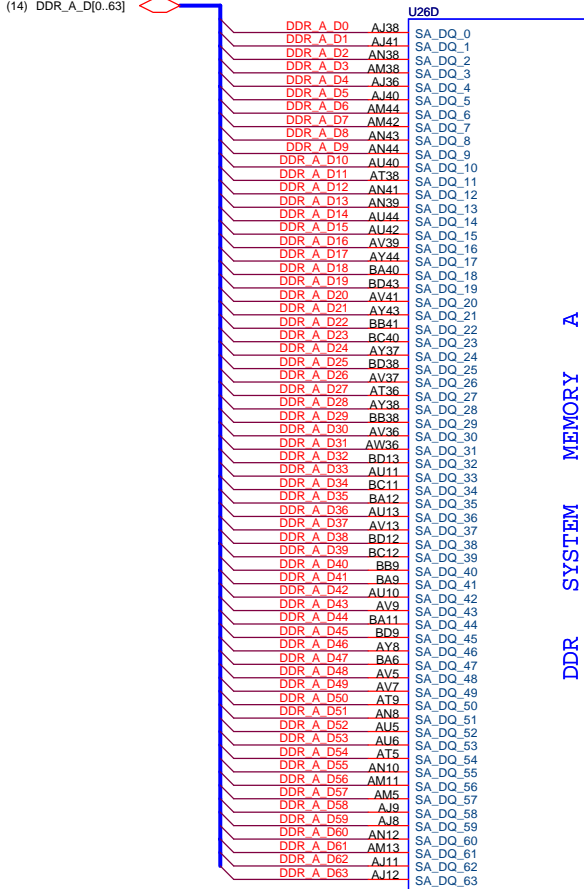
layout note:
Route H_SCOMP and H_SCOMP# with trace width spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCAMP / H_VREF / H_SWING
trace width and spacing is 10/20



Notice: Please check HDA power rail to select HDA controller.

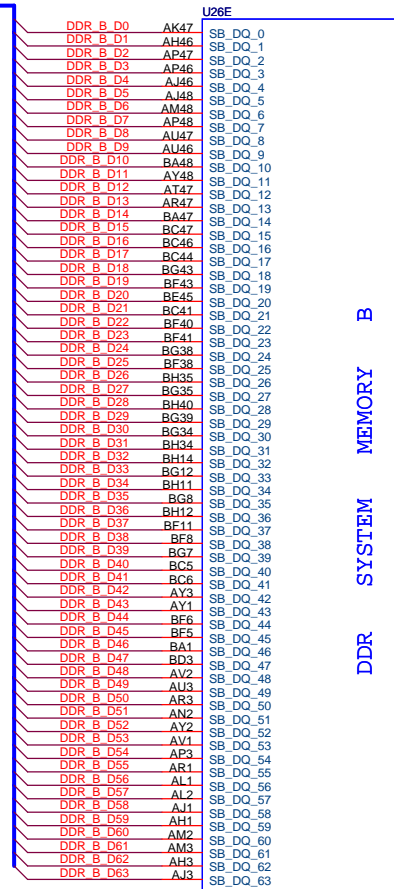
(14) DDR_A_D[0..63]



DDR SYSTEM MEMORY A

GM@

(15) DDR_B_D[0..63]



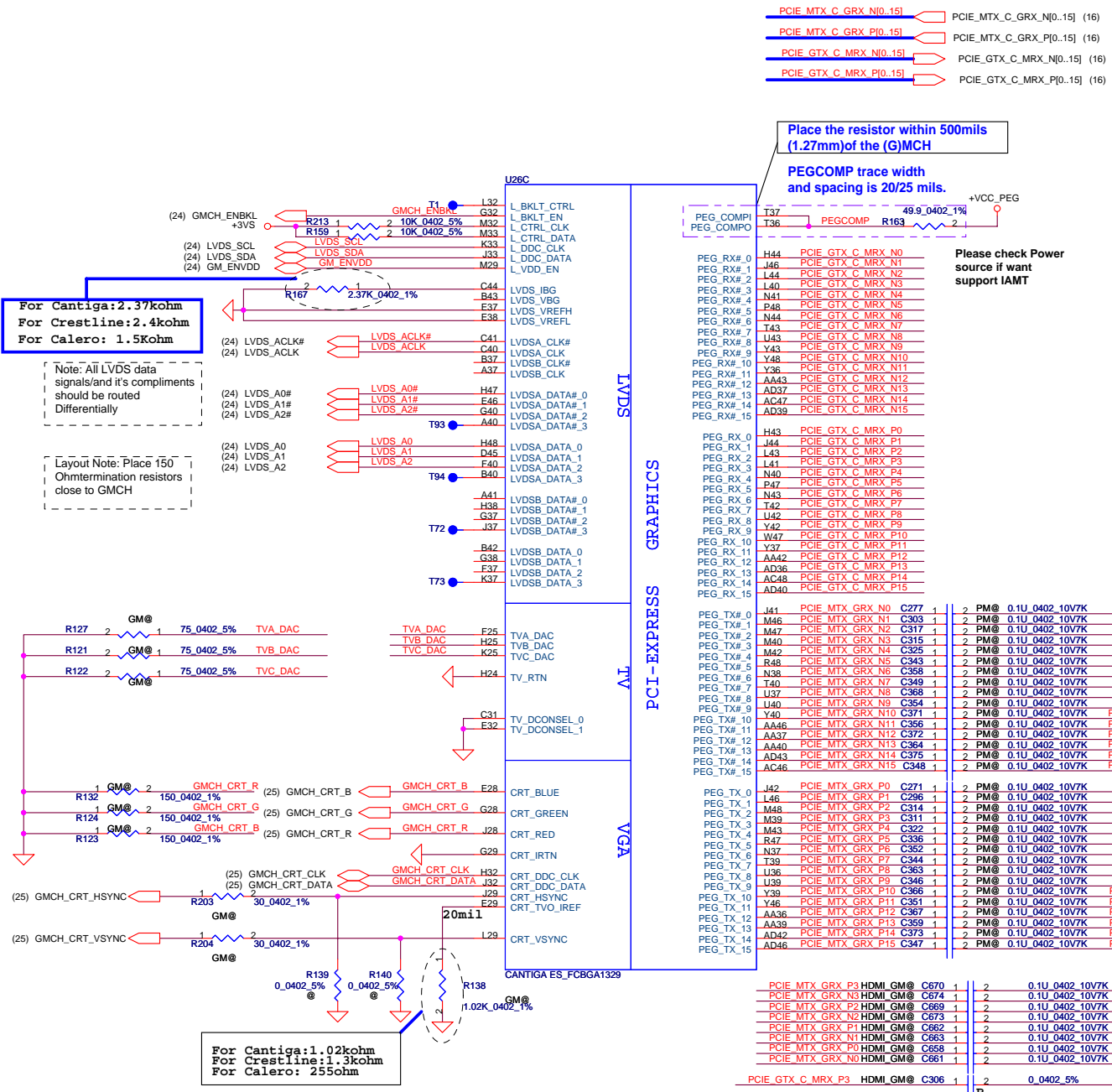
DDR SYSTEM MEMORY B

GM@

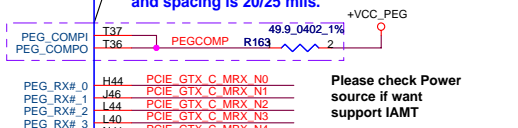
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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *



- PCIE_MTX_C_GRX_N0..15] (16)
- PCIE_MTX_C_GRX_P0..15] (16)
- PCIE_GTX_C_MRX_N0..15] (16)
- PCIE_GTX_C_MRX_P0..15] (16)



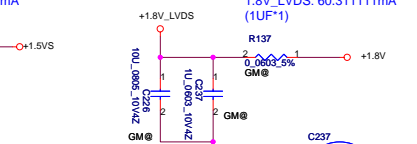
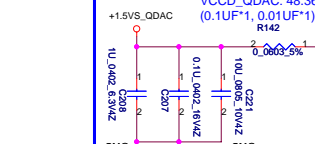
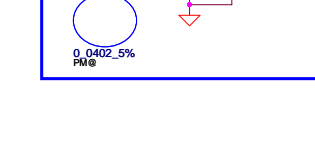
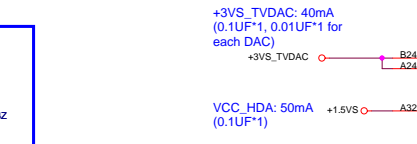
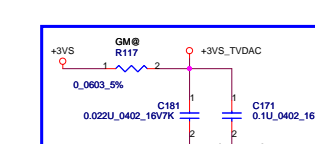
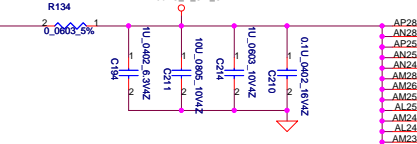
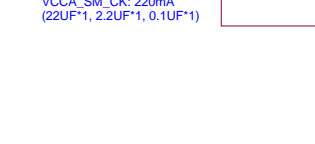
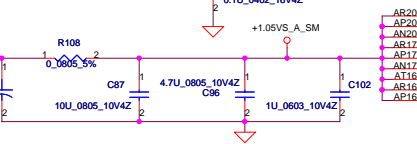
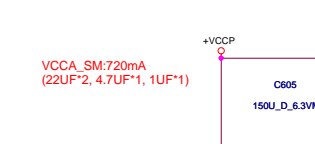
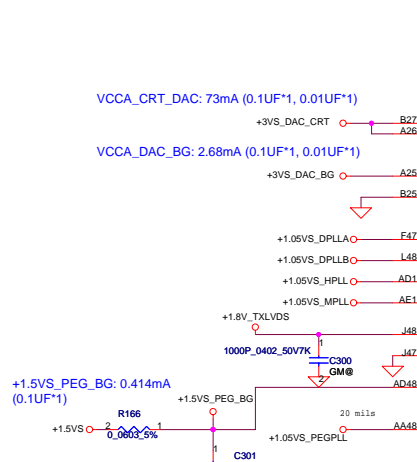
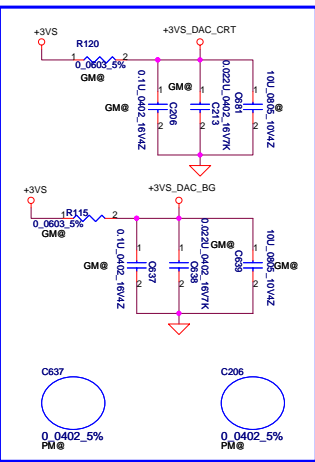
- H44 PCIE GTX C MRX N0
- L46 PCIE GTX C MRX N1
- L44 PCIE GTX C MRX N2
- L40 PCIE GTX C MRX N3
- N41 PCIE GTX C MRX N4
- P48 PCIE GTX C MRX N5
- N44 PCIE GTX C MRX N6
- T43 PCIE GTX C MRX N7
- U43 PCIE GTX C MRX N8
- Y43 PCIE GTX C MRX N9
- Y48 PCIE GTX C MRX N10
- Y36 PCIE GTX C MRX N11
- AA43 PCIE GTX C MRX N12
- AD37 PCIE GTX C MRX N13
- AC47 PCIE GTX C MRX N14
- AD39 PCIE GTX C MRX N15
- H43 PCIE GTX C MRX P0
- J44 PCIE GTX C MRX P1
- L43 PCIE GTX C MRX P2
- L41 PCIE GTX C MRX P3
- N40 PCIE GTX C MRX P4
- P47 PCIE GTX C MRX P5
- N43 PCIE GTX C MRX P6
- T42 PCIE GTX C MRX P7
- U42 PCIE GTX C MRX P8
- Y42 PCIE GTX C MRX P9
- U47 PCIE GTX C MRX P10
- Y37 PCIE GTX C MRX P11
- AA42 PCIE GTX C MRX P12
- AD36 PCIE GTX C MRX P13
- AC48 PCIE GTX C MRX P14
- AD40 PCIE GTX C MRX P15

- J41 PCIE MTX GRX N0 C277 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N0
- M46 PCIE MTX GRX N1 C303 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N1
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- M40 PCIE MTX GRX N3 C315 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N3
- M42 PCIE MTX GRX N4 C325 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N4
- R48 PCIE MTX GRX N5 C343 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N5
- N38 PCIE MTX GRX N6 C358 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N6
- T40 PCIE MTX GRX N7 C349 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N7
- U37 PCIE MTX GRX N8 C364 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N8
- U40 PCIE MTX GRX N9 C354 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N9
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- AA37 PCIE MTX GRX N12 C372 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N12
- AA40 PCIE MTX GRX N13 C364 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N13
- AD43 PCIE MTX GRX N14 C375 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N14
- AC46 PCIE MTX GRX N15 C348 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N15

- J42 PCIE MTX GRX P0 C271 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P0
- L46 PCIE MTX GRX P1 C296 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P1
- M48 PCIE MTX GRX P2 C314 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P2
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- R47 PCIE MTX GRX P5 C336 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P5
- N37 PCIE MTX GRX P6 C352 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P6
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- U36 PCIE MTX GRX P8 C363 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P8
- U39 PCIE MTX GRX P9 C346 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P9
- Y39 PCIE MTX GRX P10 C366 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P10
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- AD42 PCIE MTX GRX P14 C373 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P14
- AD46 PCIE MTX GRX P15 C347 1 2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P15

- PCIE_MTX_GRX_P3 HDMI_GM@ C670 1 2 0.1U 0402 10V7K TMDS_B_CLK (23)
- PCIE_MTX_GRX_N3 HDMI_GM@ C674 1 2 0.1U 0402 10V7K TMDS_B_CLK# (23)
- PCIE_MTX_GRX_P2 HDMI_GM@ C669 1 2 0.1U 0402 10V7K TMDS_B_DATA0 (23)
- PCIE_MTX_GRX_N2 HDMI_GM@ C673 1 2 0.1U 0402 10V7K TMDS_B_DATA0# (23)
- PCIE_MTX_GRX_P1 HDMI_GM@ C662 1 2 0.1U 0402 10V7K TMDS_B_DATA1 (23)
- PCIE_MTX_GRX_N1 HDMI_GM@ C663 1 2 0.1U 0402 10V7K TMDS_B_DATA1# (23)
- PCIE_MTX_GRX_P0 HDMI_GM@ C658 1 2 0.1U 0402 10V7K TMDS_B_DATA2 (23)
- PCIE_MTX_GRX_N0 HDMI_GM@ C661 1 2 0.1U 0402 10V7K TMDS_B_DATA2# (23)
- PCIE_GTX_C_MRX_P3 HDMI_GM@ C306 1 2 0.0402 5% TMDS_B_HPD# (23)

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VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)

VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)

+1.5VS_PEG_BG: 0.414mA (0.1UF*1)

VCCA_SM: 720mA (22UF*2, 4.7UF*1, 1UF*1)

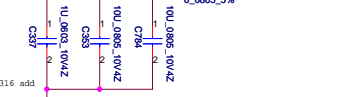
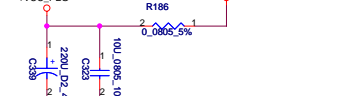
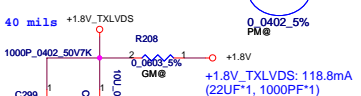
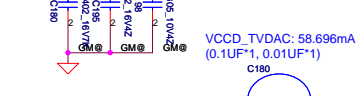
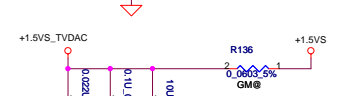
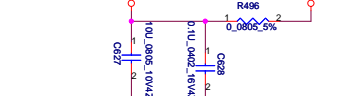
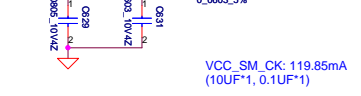
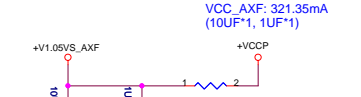
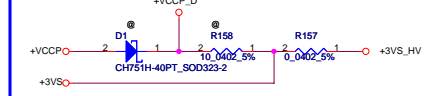
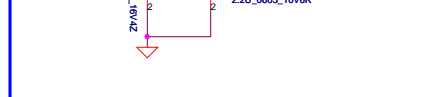
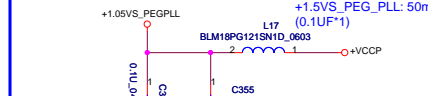
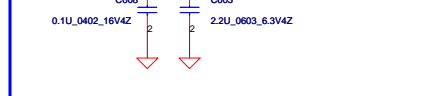
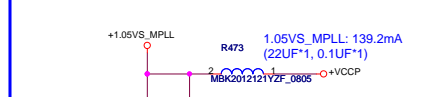
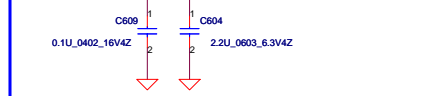
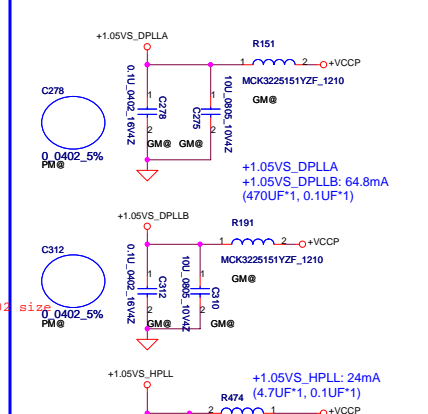
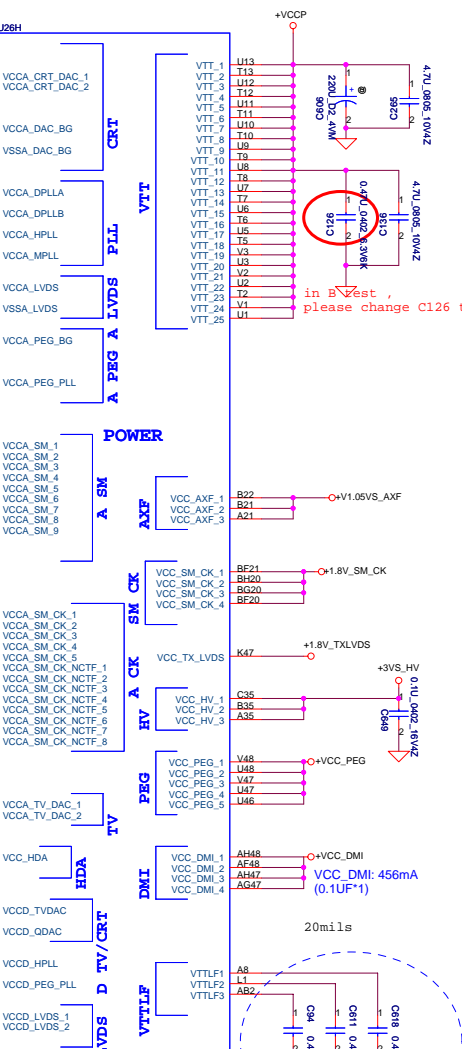
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)

+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)

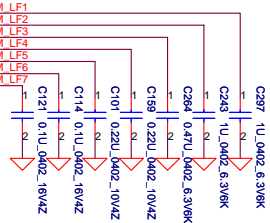
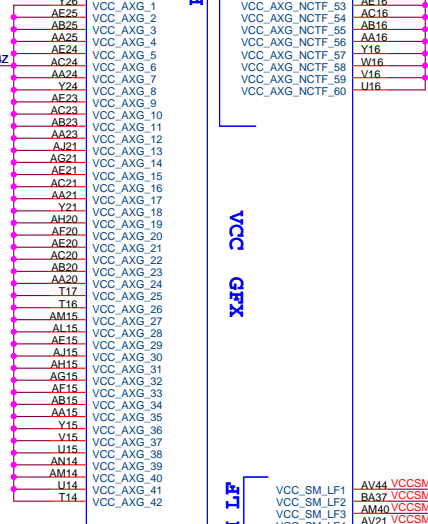
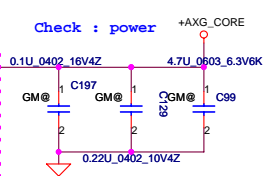
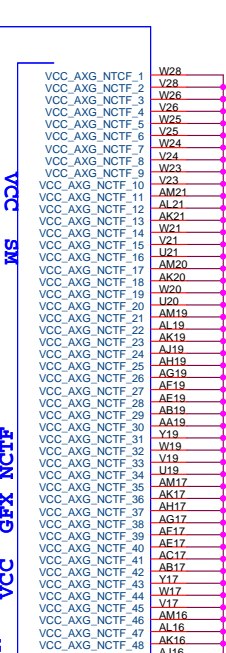
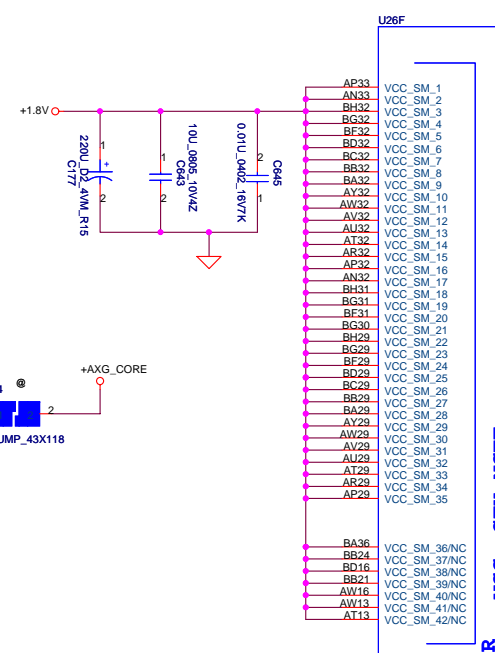
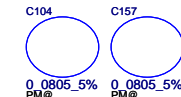
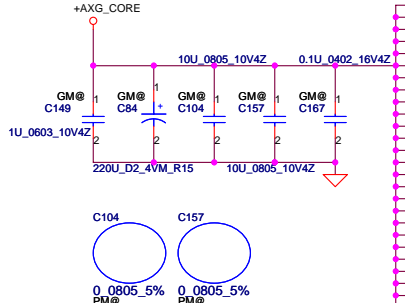
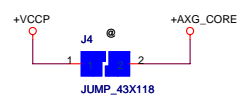
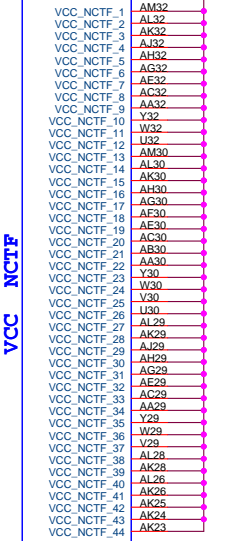
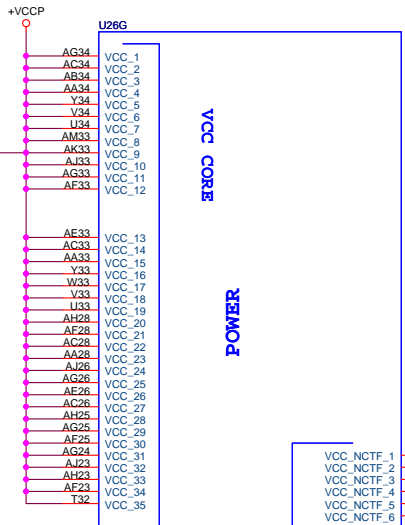
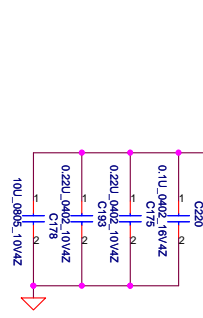
VCC_HDA: 50mA (0.1UF*1)

VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)

1.8V_TXLVD: 60.311111mA (1UF*1)



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Title Crestline GMCH (4/6)-VCC			Rev 1.0	
Date: Wednesday, May 14, 2008			Sheet 11 of 53	



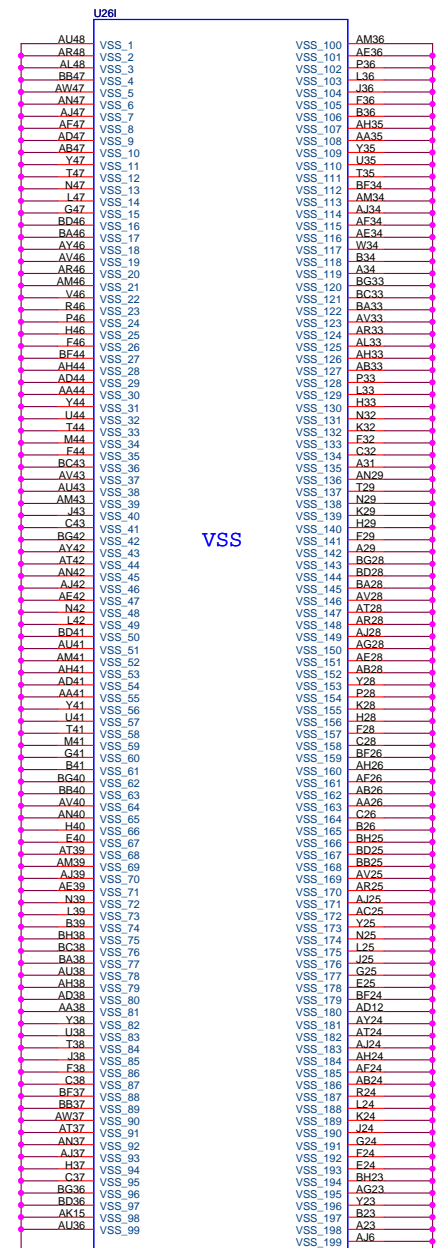
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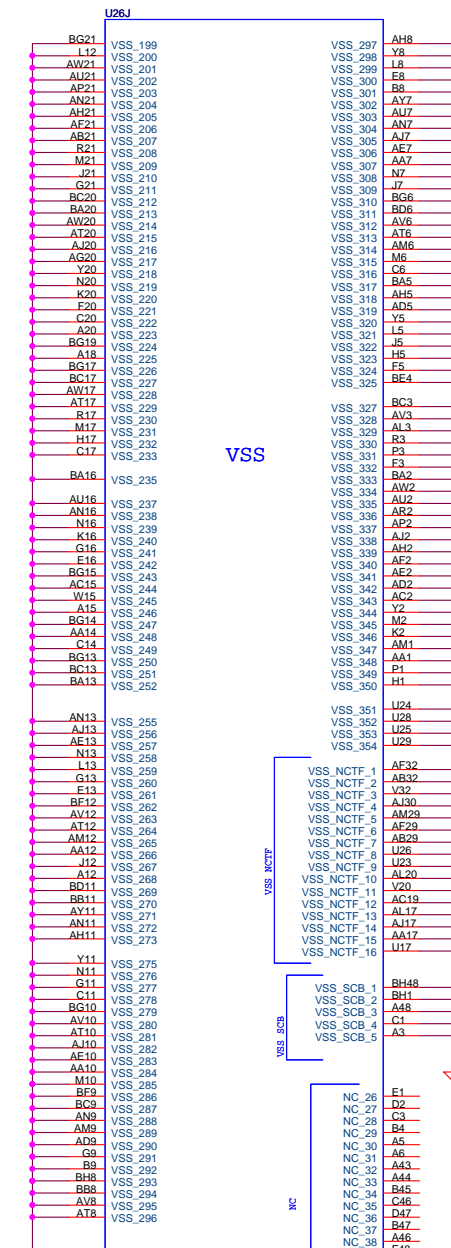
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Size	Document Number	J1WA1A2 JA-4211P		Rev	1.0
Date:	Wednesday, May 14, 2008	Sheet	12	of	53



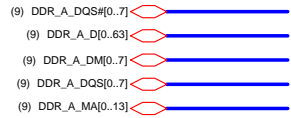
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Issued Date	2007/10/15	Deciphered Date	2008/10/15
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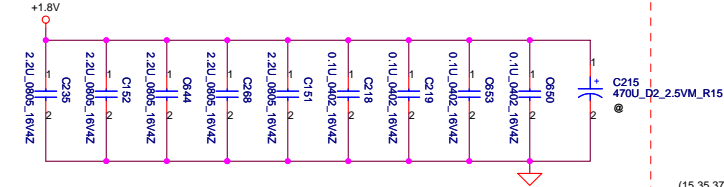
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Cantiga GMCH (6/6)-GND			
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Date:	Wednesday, May 14, 2008	Sheet	13 of 53



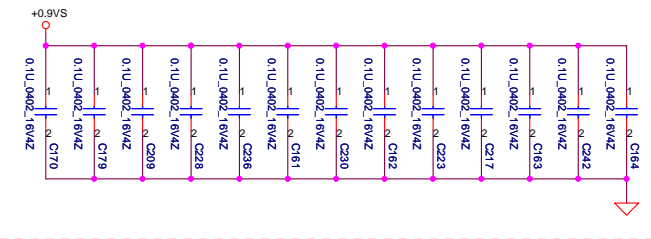
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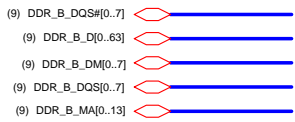


Layout Note:
Place near JP41

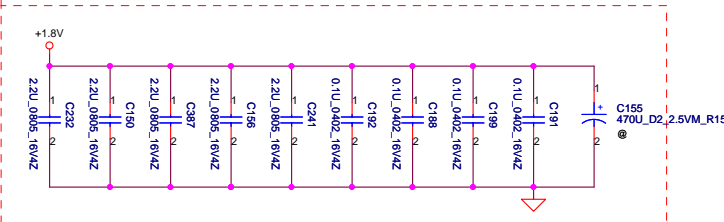


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

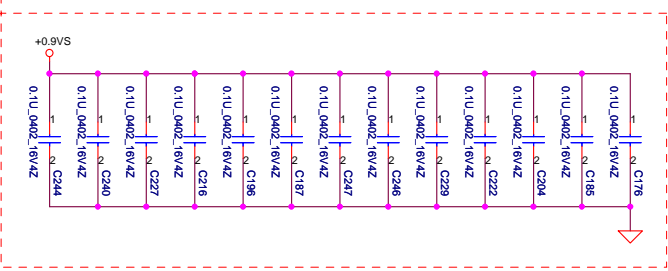




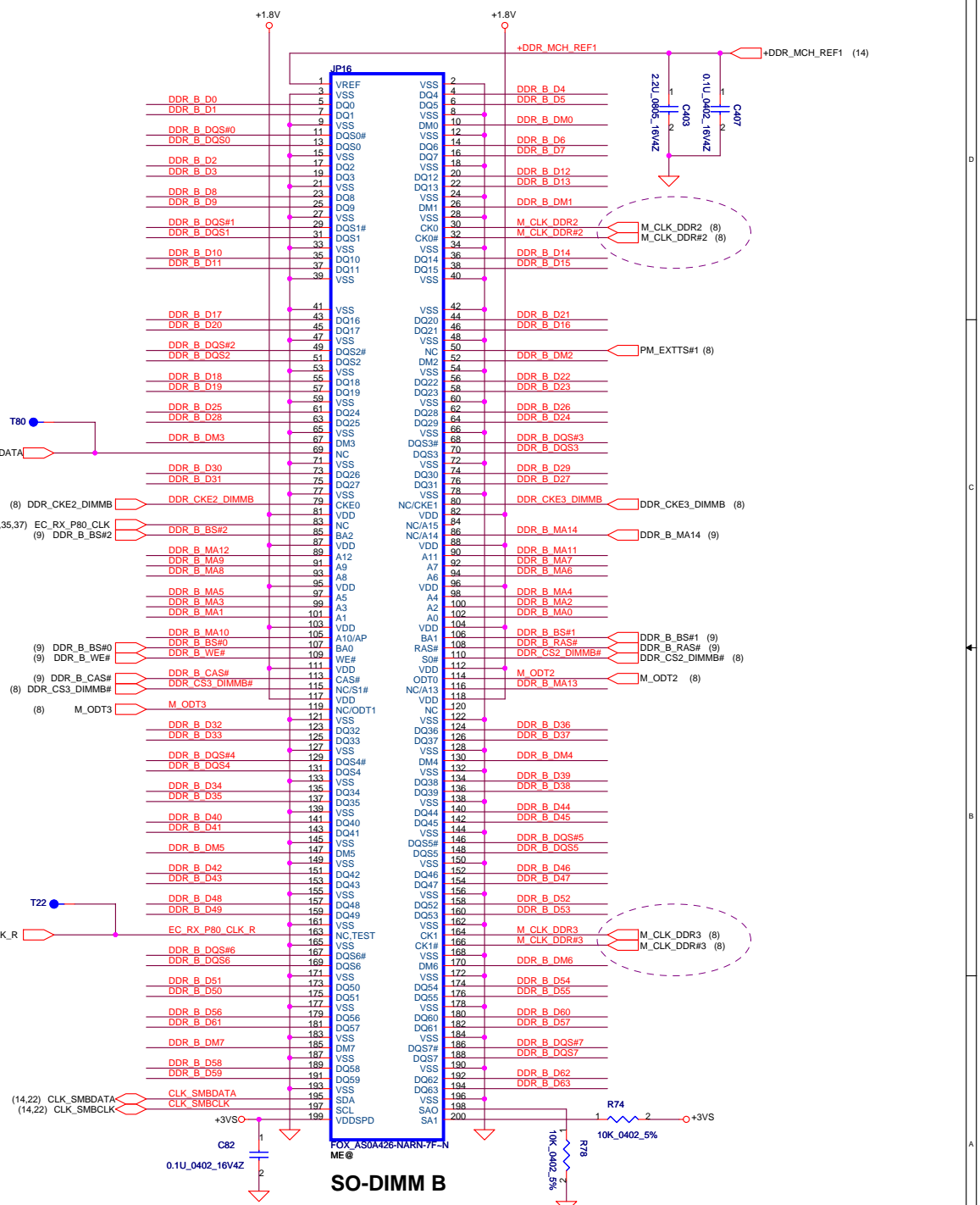
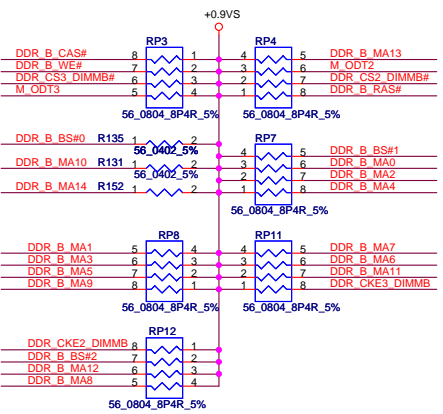
Layout Note:
Place near JP42



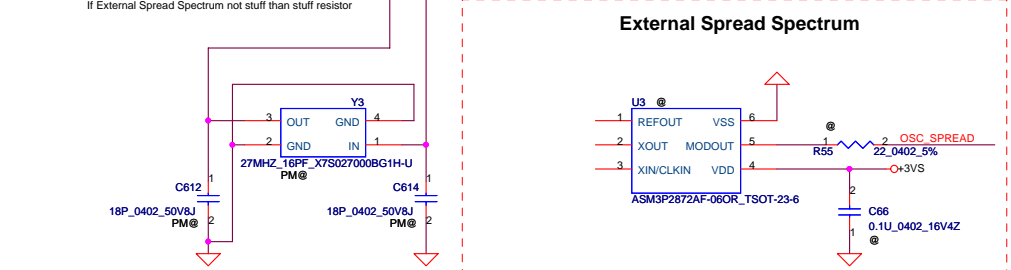
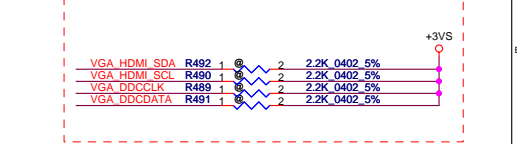
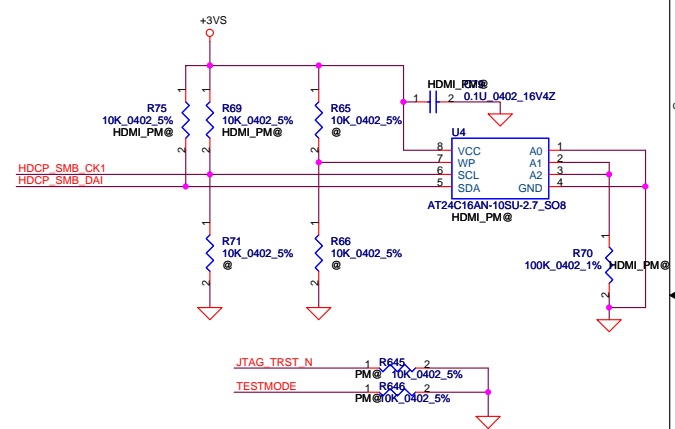
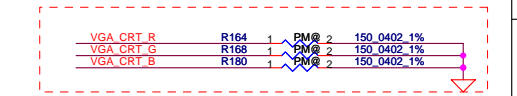
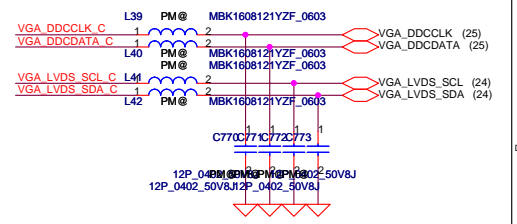
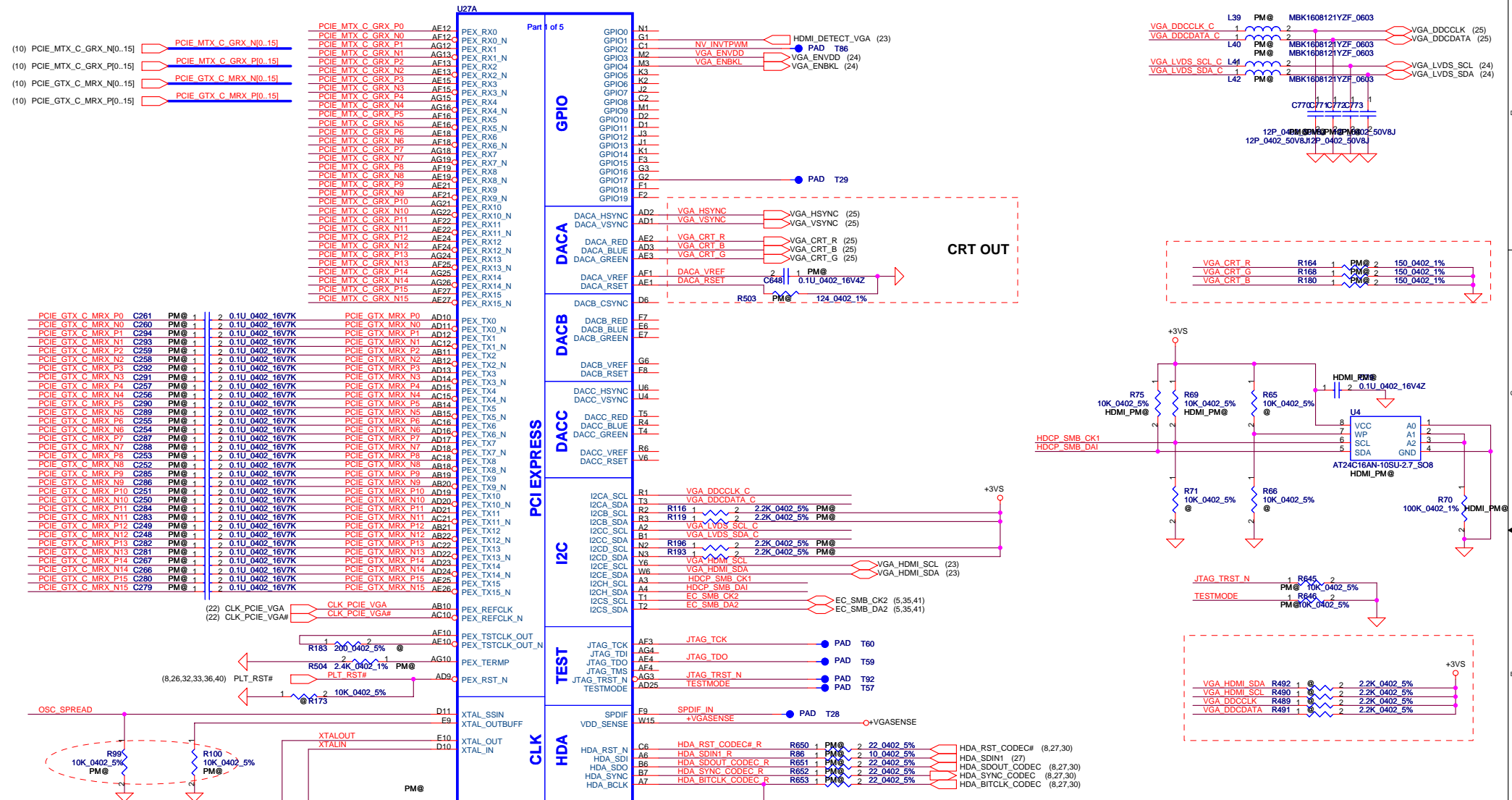
Layout Note:
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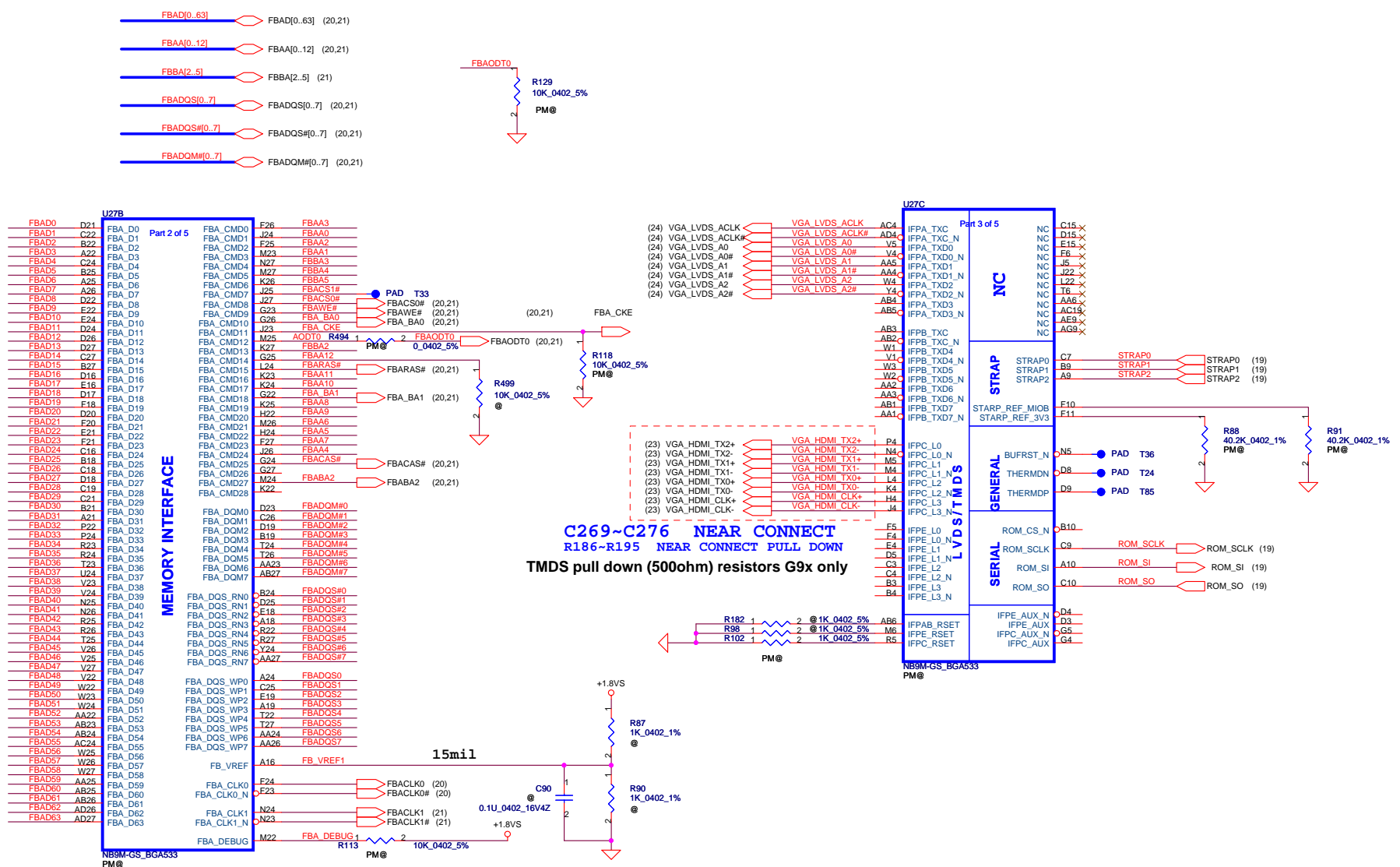
Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



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			Rev: 1.0
			Sheet 15 of 53

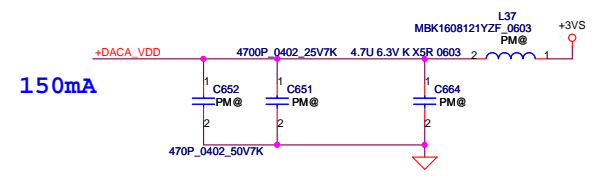
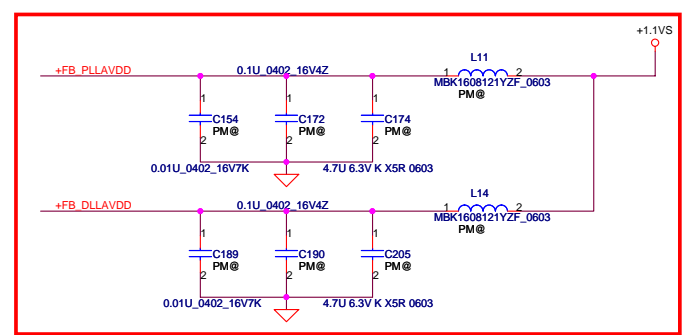
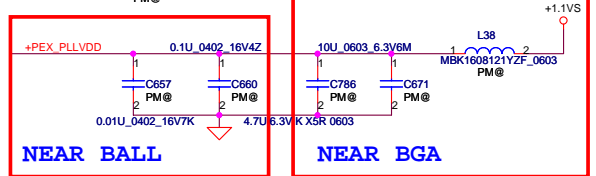
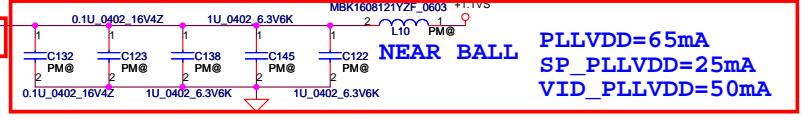
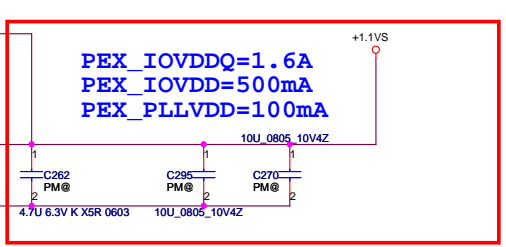
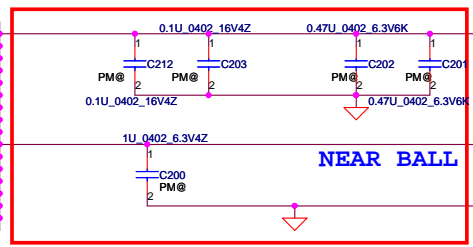
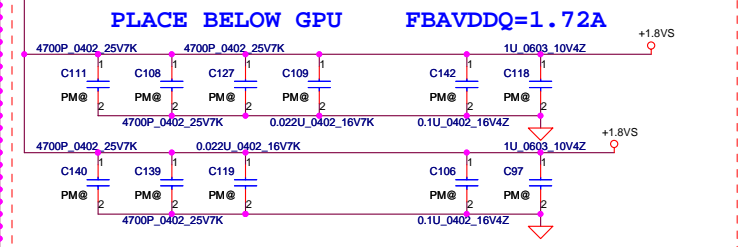
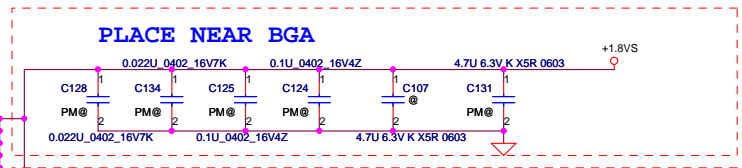
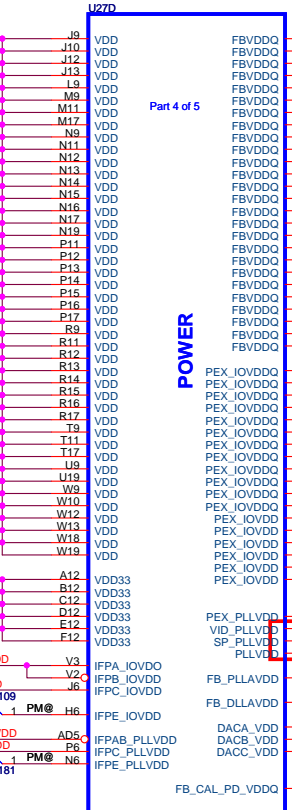
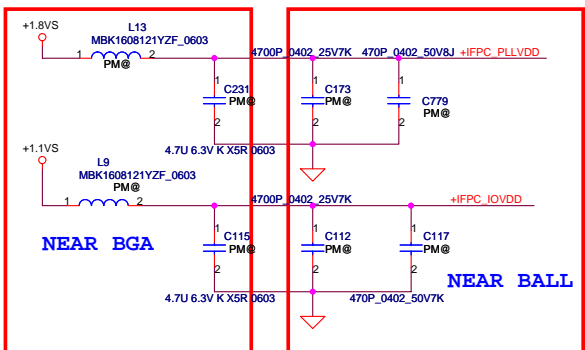
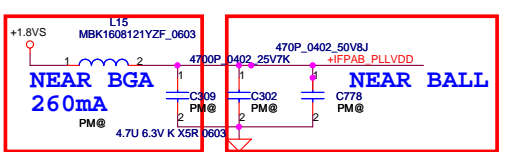
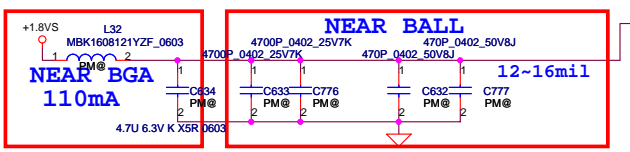
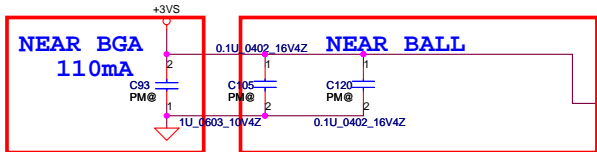
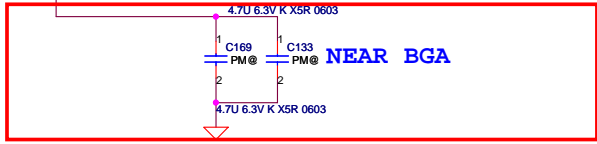
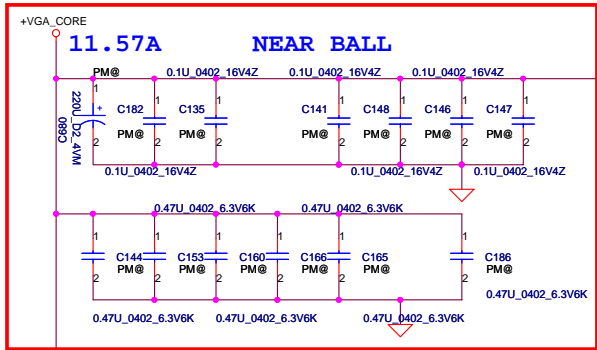


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Size	Document Number	JJWAI/A2_LA-4211P	Rev	1.0
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C269~C276 NEAR CONNECT
R186~R195 NEAR CONNECT PULL DOWN
TMDS pull down (500ohm) resistors G9x only

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Size B	Document Number	Rev 1.0		
	J1W1A1A2_LA-4211P			
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Date: Monday, May 12, 2008				Sheet 18	of 53

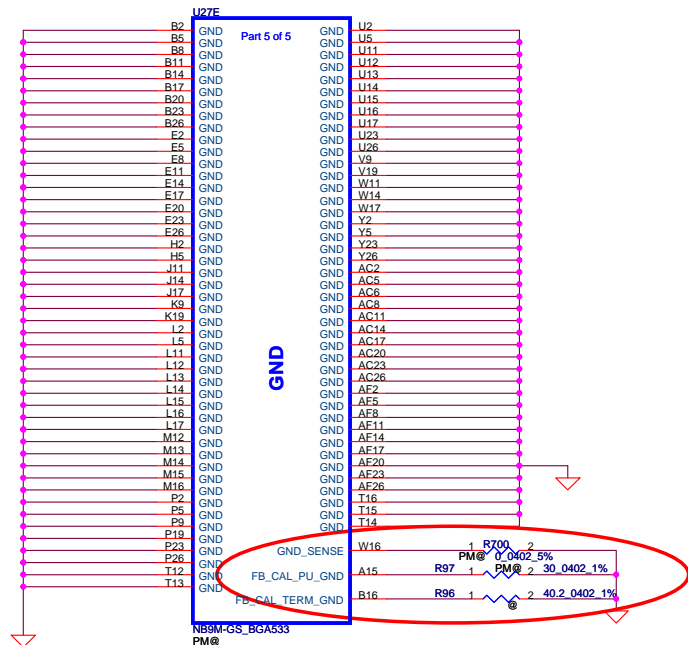
A total of 8 signals are required for GB1 strapping this includes

2 reference signals

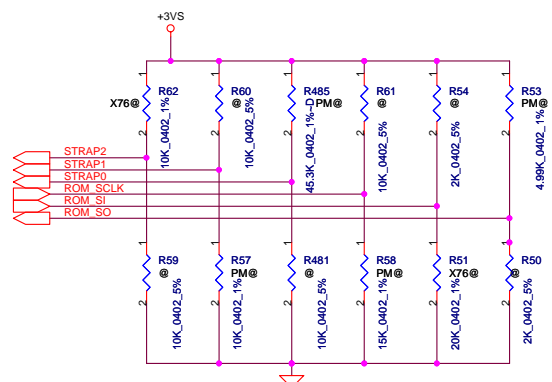
6 physical strapping pins

4 logical strapping bits

A total of 24 logical strapping bits are available



- (17) STRAP2
- (17) STRAP1
- (17) STRAP0
- (17) ROM_SCLK
- (17) ROM_SI
- (17) ROM_SO

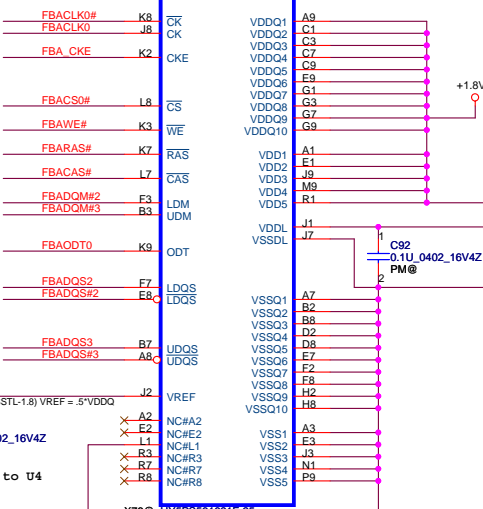
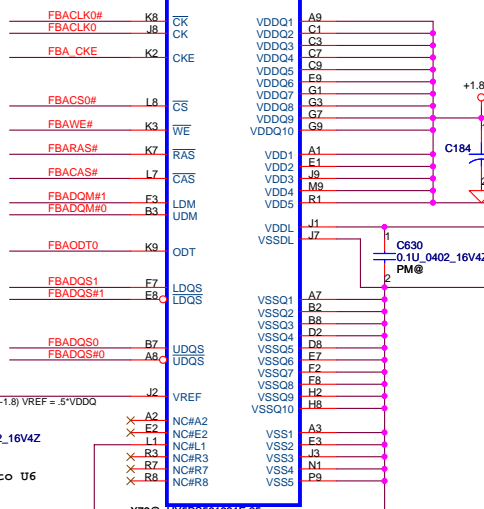
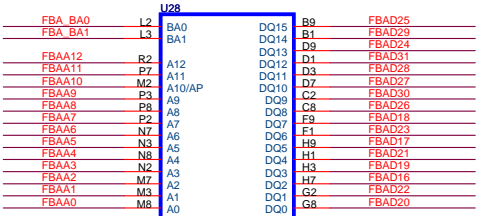
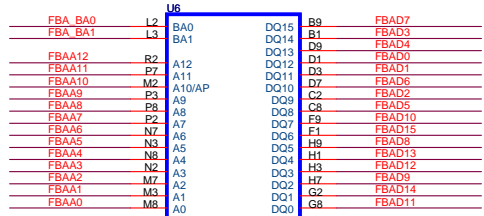


GB1 Family GPU Strap Options

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
NB9M-GE (0x06E8)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 5K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 5K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 5K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 5K	PD 10K	PU 45K

Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (16M*16)	Hynix	SA000012G30	X7611338L01
	Qimonda	SA00001YF10	X7611338L02
	Samsung	SA00001KH10	X7611338L03
DDR2 VRAM (32M*16)	Hynix	SA00000FP30	X7611338L04
	Qimonda	SA00000S820	X7611338L05
	Samsung	SA00001VX10	X7611338L06

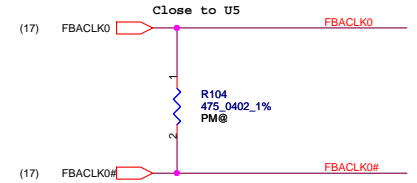
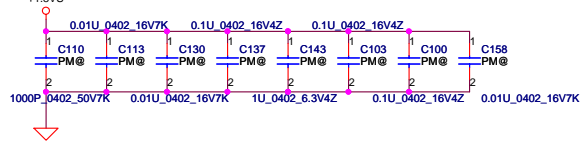
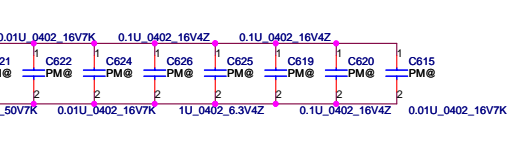
Security Classification	Compal Secret Data			Compal Electronics, Inc. NB9M-GE GND & STRAP		
Issued Date	2007/10/15	Deciphered Date	2008/10/15			
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				Date: Monday, May 12, 2008	Sheet 19	of 53



- (17.21) FBBA[2..5] FBBA[2..5]
- (17.21) FBAD[0..63] FBAD[0..63]
- (17.21) FBAA[0..12] FBAA[0..12]
- (17.21) FBADQS[0..7] FBADQS[0..7]
- (17.21) FBADQS#[0..7] FBADQS#[0..7]
- (17.21) FBADQM#[0..7] FBADQM#[0..7]
- (17.21) FBA_BA0 FBA_BA0
- (17.21) FBA_BA1 FBA_BA1
- (17.21) FBAODT0 FBAODT0
- (17.21) FBA_CKE FBA_CKE
- (17.21) FBARAS# FBARAS#
- (17.21) FBACAS# FBACAS#
- (17.21) FBAWE# FBAWE#
- (17.21) FBACS0# FBACS0#

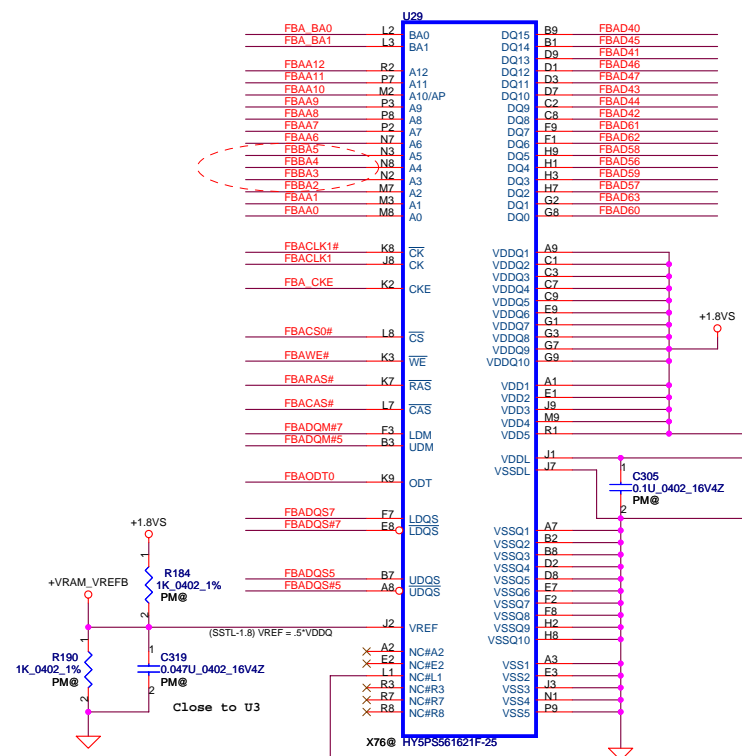
DDR2 BGA MEMORY

DDR2 BGA MEMORY

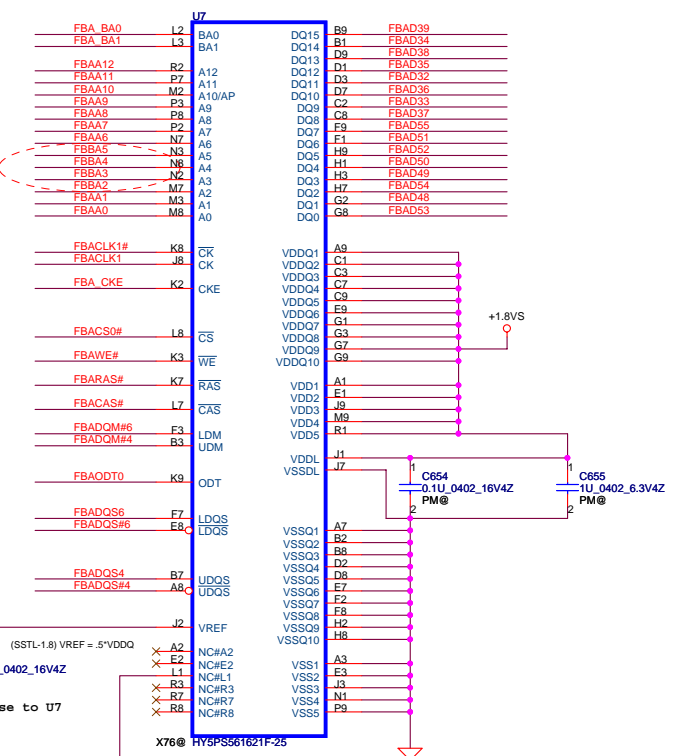


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Compal Electronics, Inc.		
VRAM DDRA		
Size	Document Number	Rev
Custom	J1WA1/A2_LA-4211P	1.0
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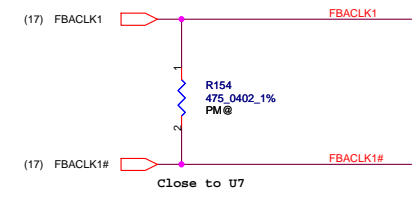
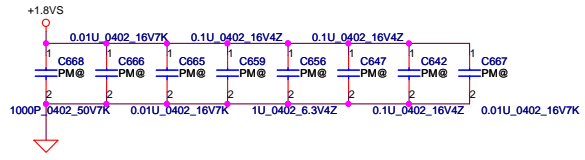
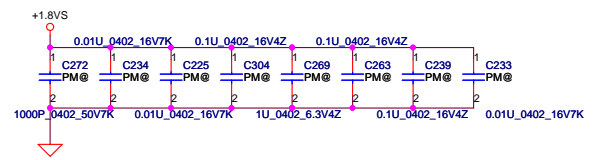


DDR2 BGA MEMORY



DDR2 BGA MEMORY

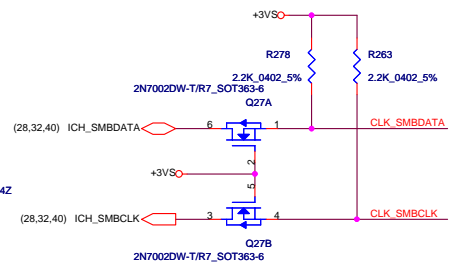
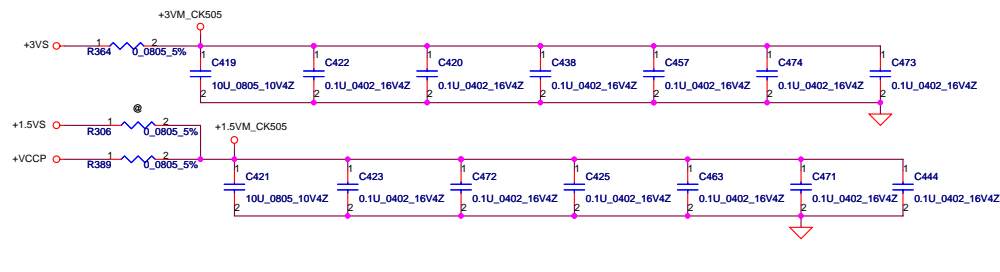
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- (17) FBBA[2..5] FBBA[2..5]
- (17,20) FBADQS[0..7] FBADQS[0..7]
- (17,20) FBADQS# [0..7] FBADQS#[0..7]
- (17,20) FBADQM# [0..7] FBADQM#[0..7]
- (17,20) FBA_BA0 FBA_BA0
- (17,20) FBA_BA1 FBA_BA1
- (17,20) FBAODT0 FBAODT0
- (17,20) FBA_CKE FBA_CKE
- (17,20) FBARAS# FBARAS#
- (17,20) FBACAS# FBACAS#
- (17,20) FBAAWE# FBAAWE#
- (17,20) FBACSO# FBACSO#



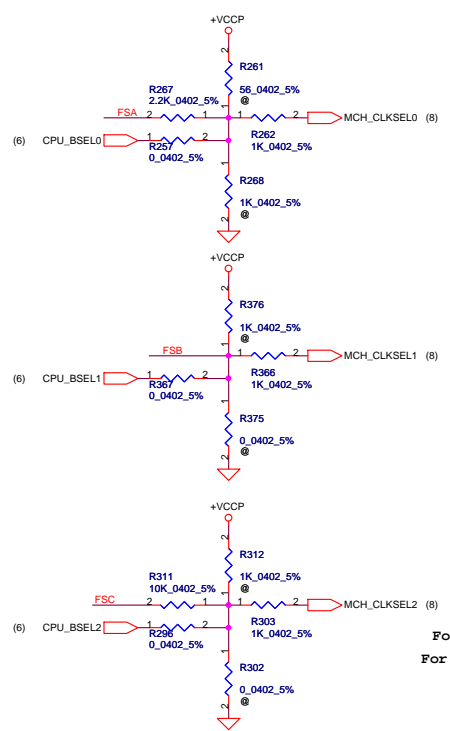
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Title			Compal Electronics, Inc.	
			VRAM DDRB	
Size	Document Number		Rev	
Custom	J1WA1/A2_LA-4211P		1.0	
Date:	Monday, May 12, 2008	Sheet	21	of 53

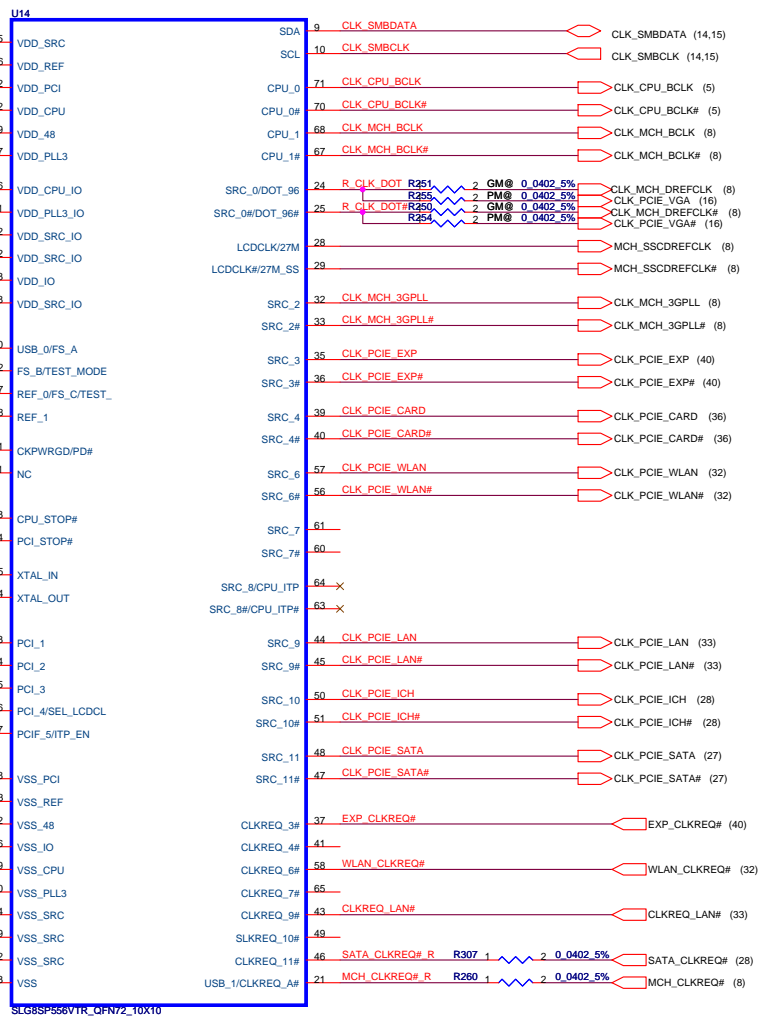
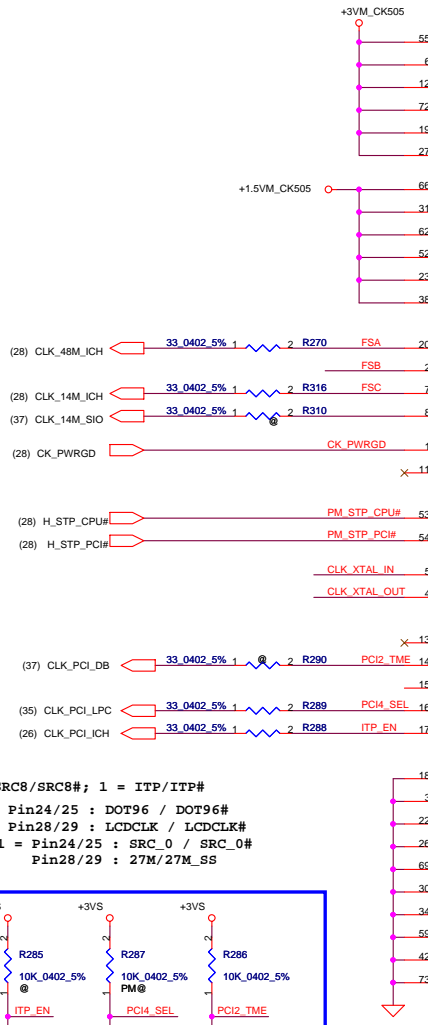
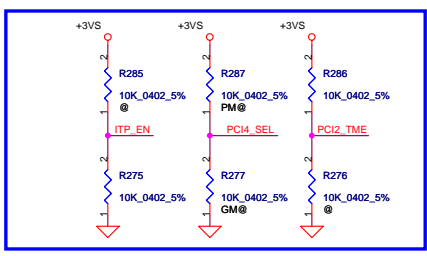
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
 For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
 Pin28/29 : LCDCLK / LCDCLK#
 1 = Pin24/25 : SRC_0 / SRC_0#
 Pin28/29 : 27M/27M_SS

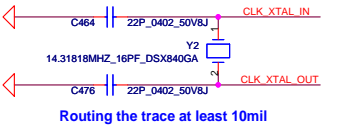


SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL



Routing the trace at least 10mil

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				JIWAI/A2_LA-4211P	1.0
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09/13 change pull low enable

09/13 change pull high enable

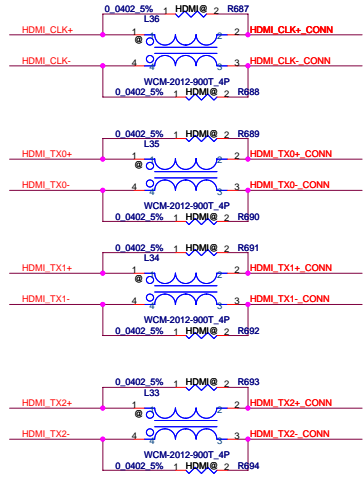
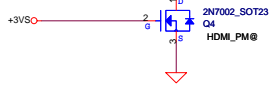
pull down for P88101T

P/N: SA00001U900

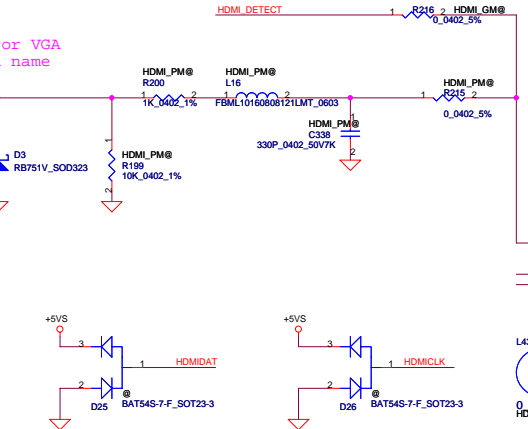
TMDS pull down (500ohm) resistors G9x only

- HDMI_CLK+ CONN R155 1 HDMI_PM# 499 0402 1%
- HDMI_CLK- CONN R156 1 HDMI_PM# 499 0402 1%
- HDMI_TX0+ CONN R150 1 HDMI_PM# 499 0402 1%
- HDMI_TX0- CONN R153 1 HDMI_PM# 499 0402 1%
- HDMI_TX1+ CONN R145 1 HDMI_PM# 499 0402 1%
- HDMI_TX1- CONN R149 1 HDMI_PM# 499 0402 1%
- HDMI_TX2+ CONN R141 1 HDMI_PM# 499 0402 1%
- HDMI_TX2- CONN R144 1 HDMI_PM# 499 0402 1%

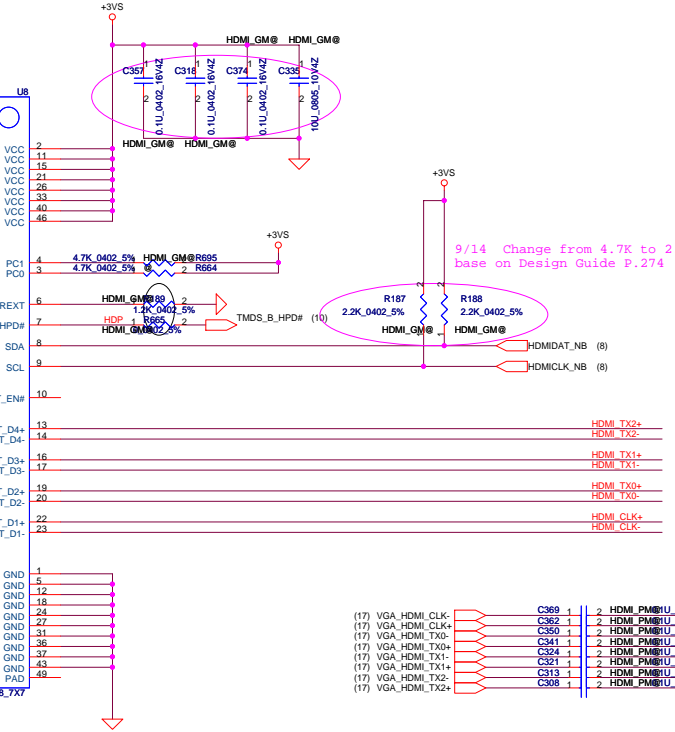
NEAR CONNECT



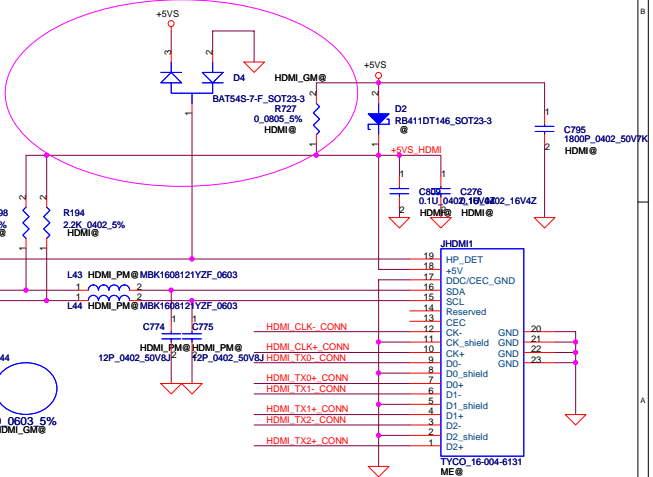
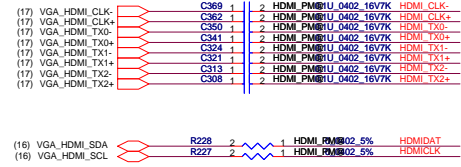
9/14 Reserve for VGA used; check pin name



9/14 Modify for UMA used

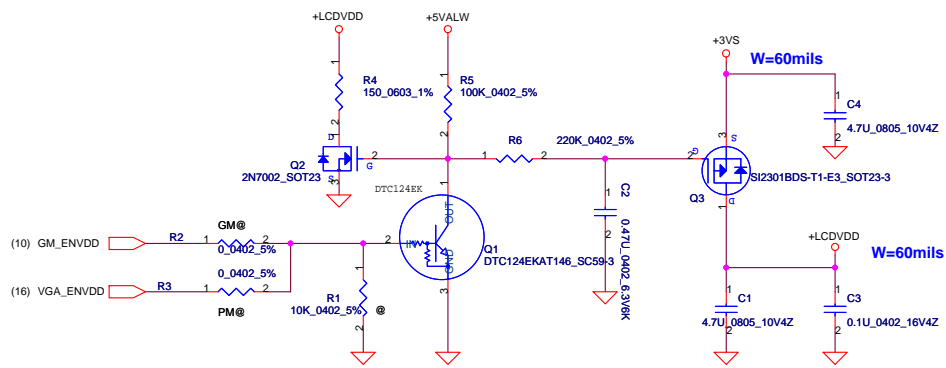


9/14 Change from 4.7K to 2.2K base on Design Guide P.274

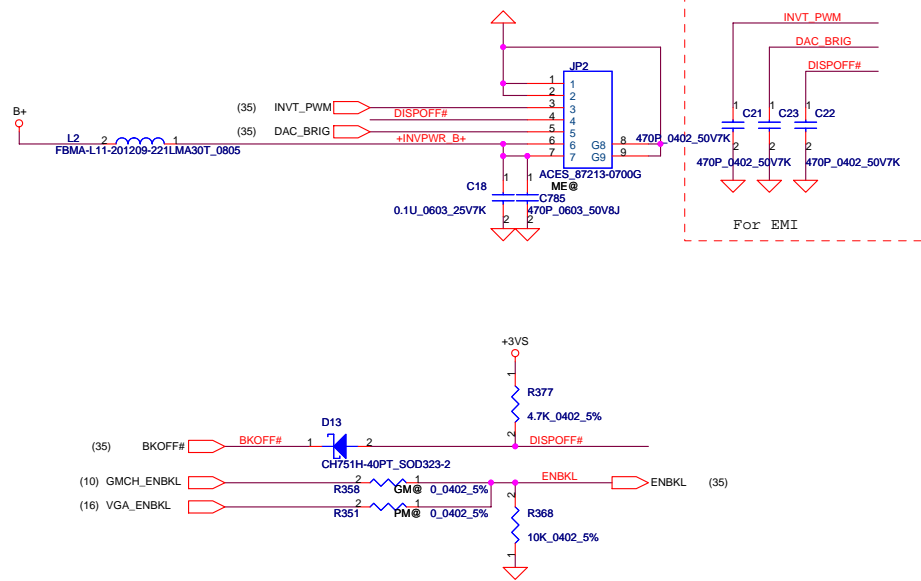


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Size	Document Number	J1WAI/A2_LA-4211P		Rev 1.0
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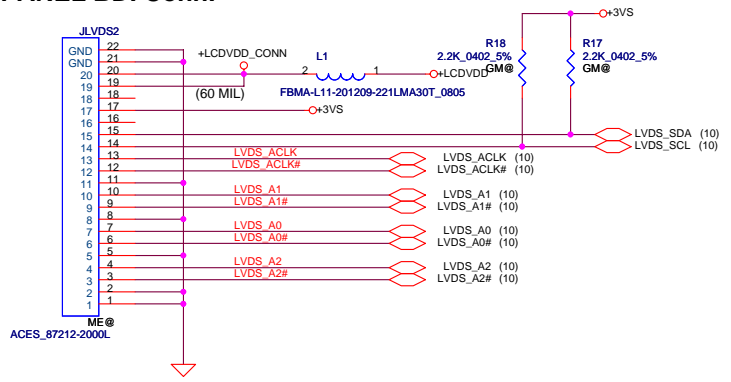
LCD POWER CIRCUIT



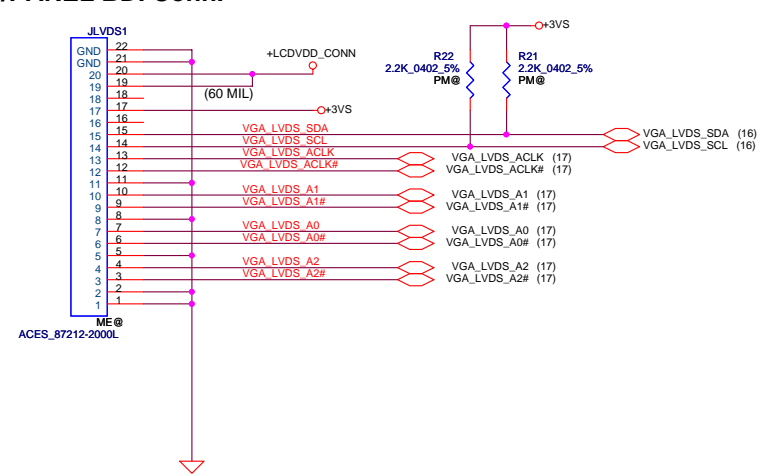
INVERTER Conn.



LCD/PANEL BD. Conn.



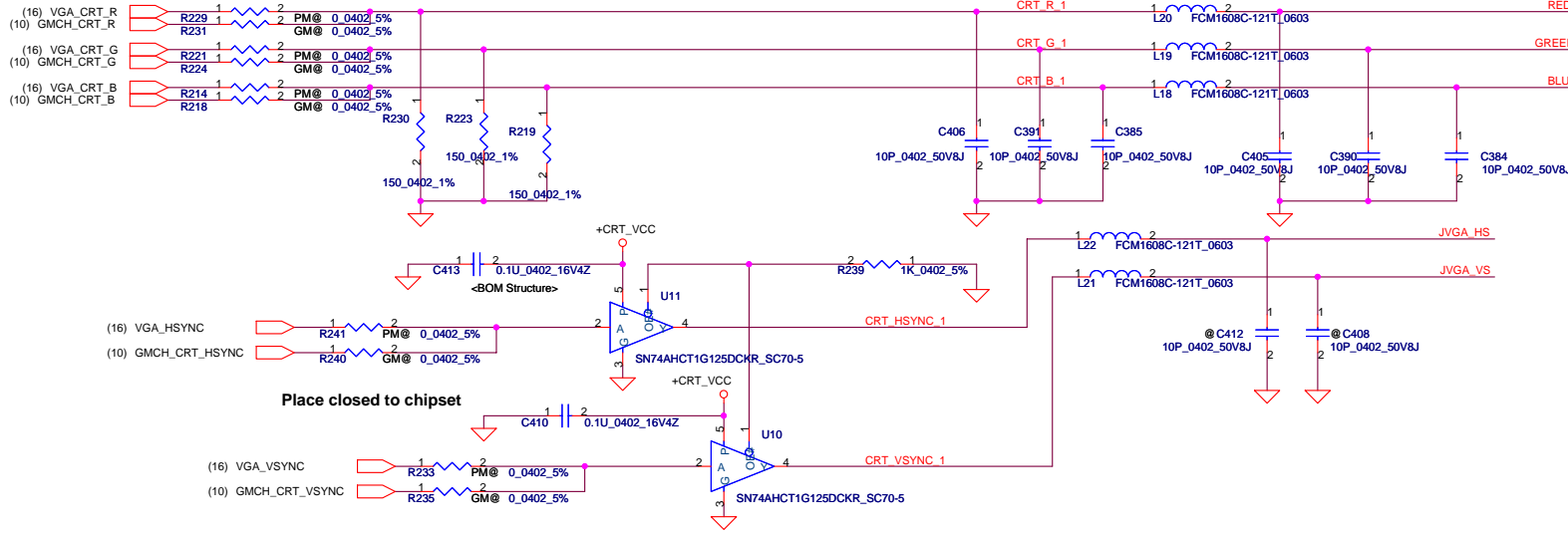
LCD/PANEL BD. Conn.



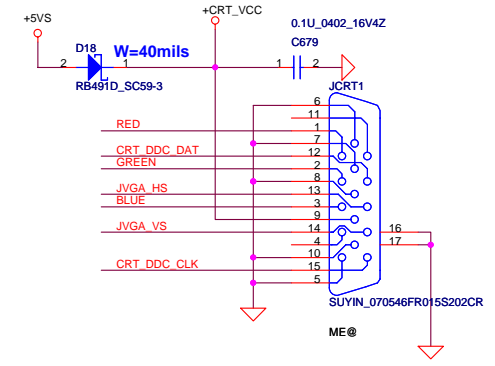
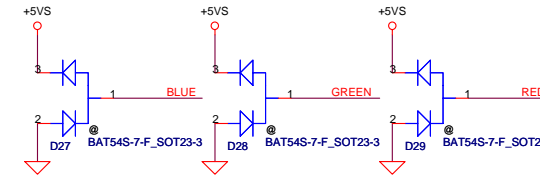
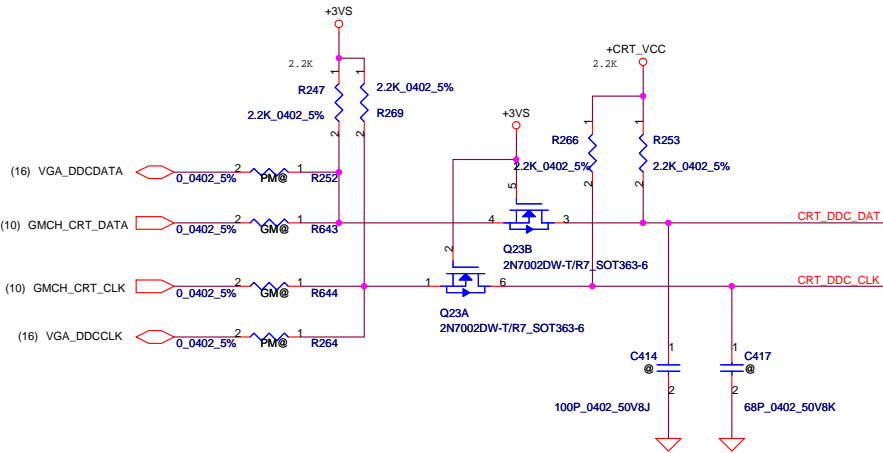
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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Size B	Document Number	JIWA1/A2_LA-4211P		Rev	1.0
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CRT Connector

Place closed to chipset



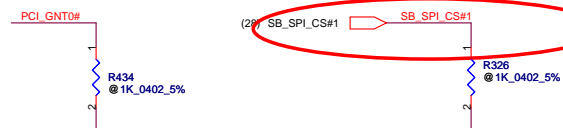
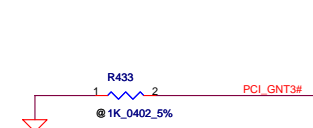
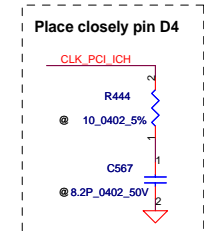
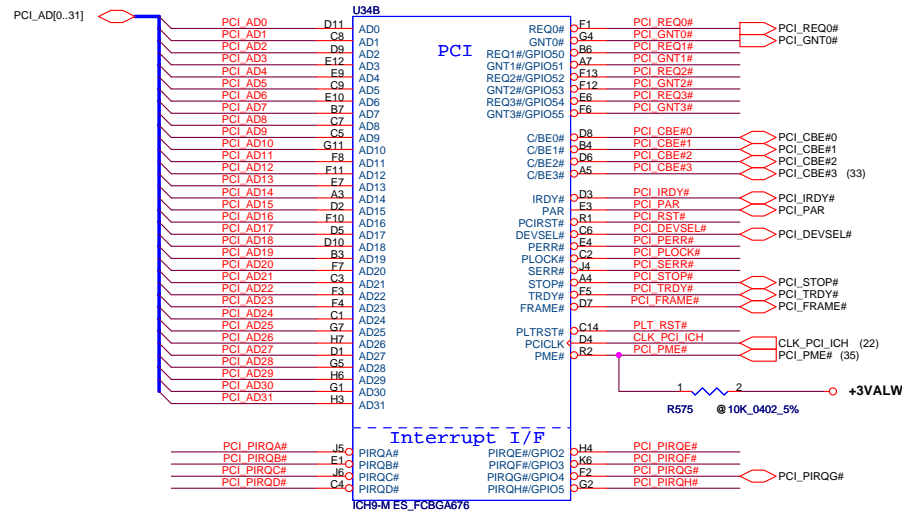
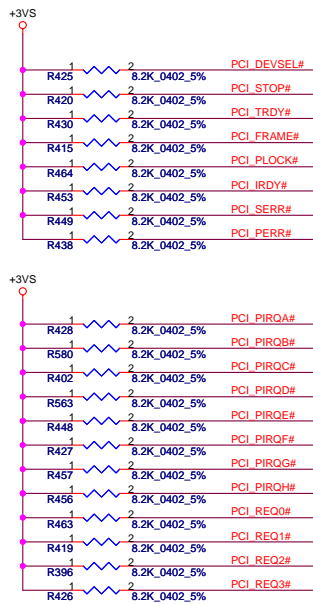
Place closed to chipset



PIN ASSIGNMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

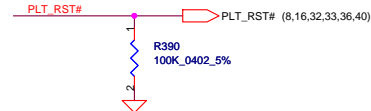
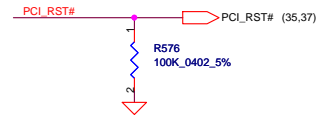
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	
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Size	Document Number	Rev		1.0
Custom	JJWAI/A2_LA-4211P	Date:		Monday, May 12, 2008
Date:		Monday, May 12, 2008	Sheet	25 of 53

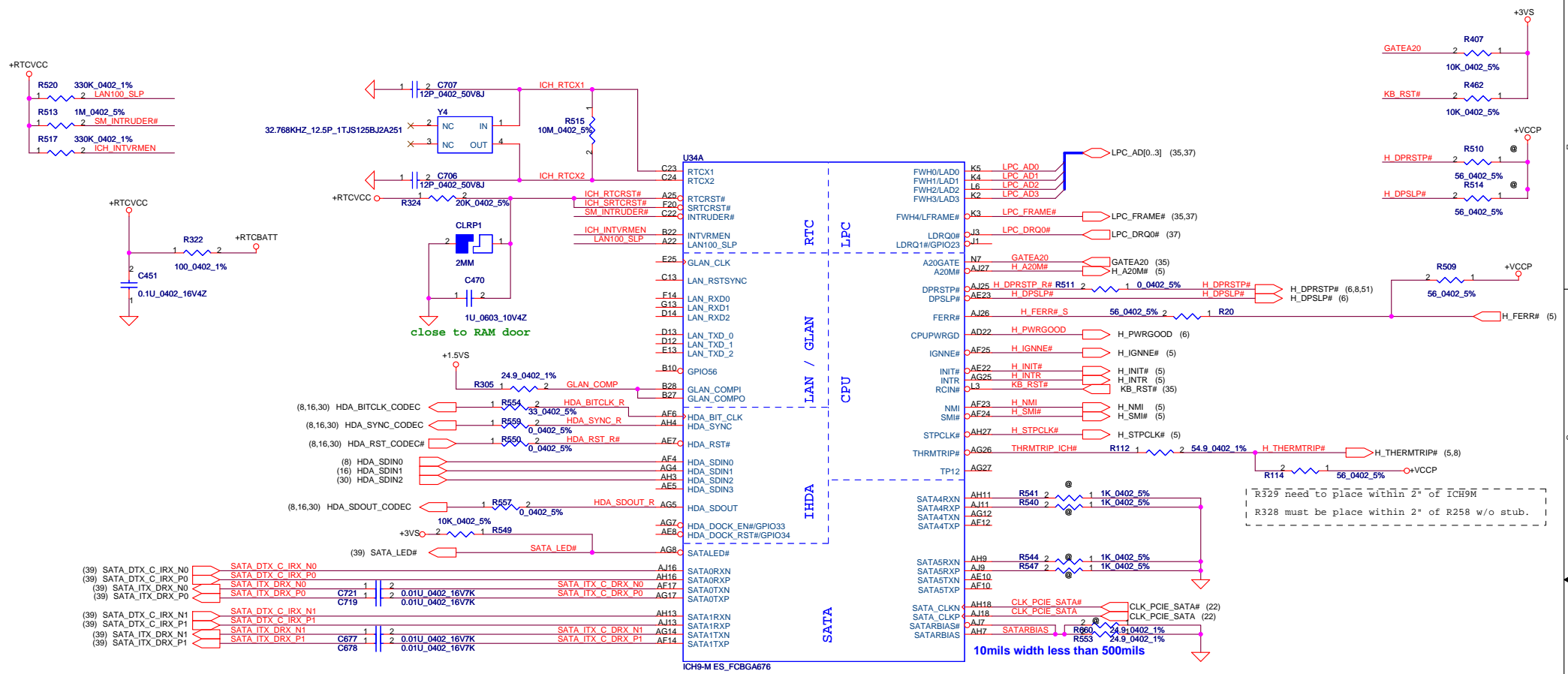


Pull high?

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

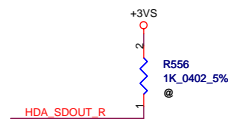
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*





R329 need to place within 2" of ICH9M
 R328 must be place within 2" of R258 w/o stub.

Need check



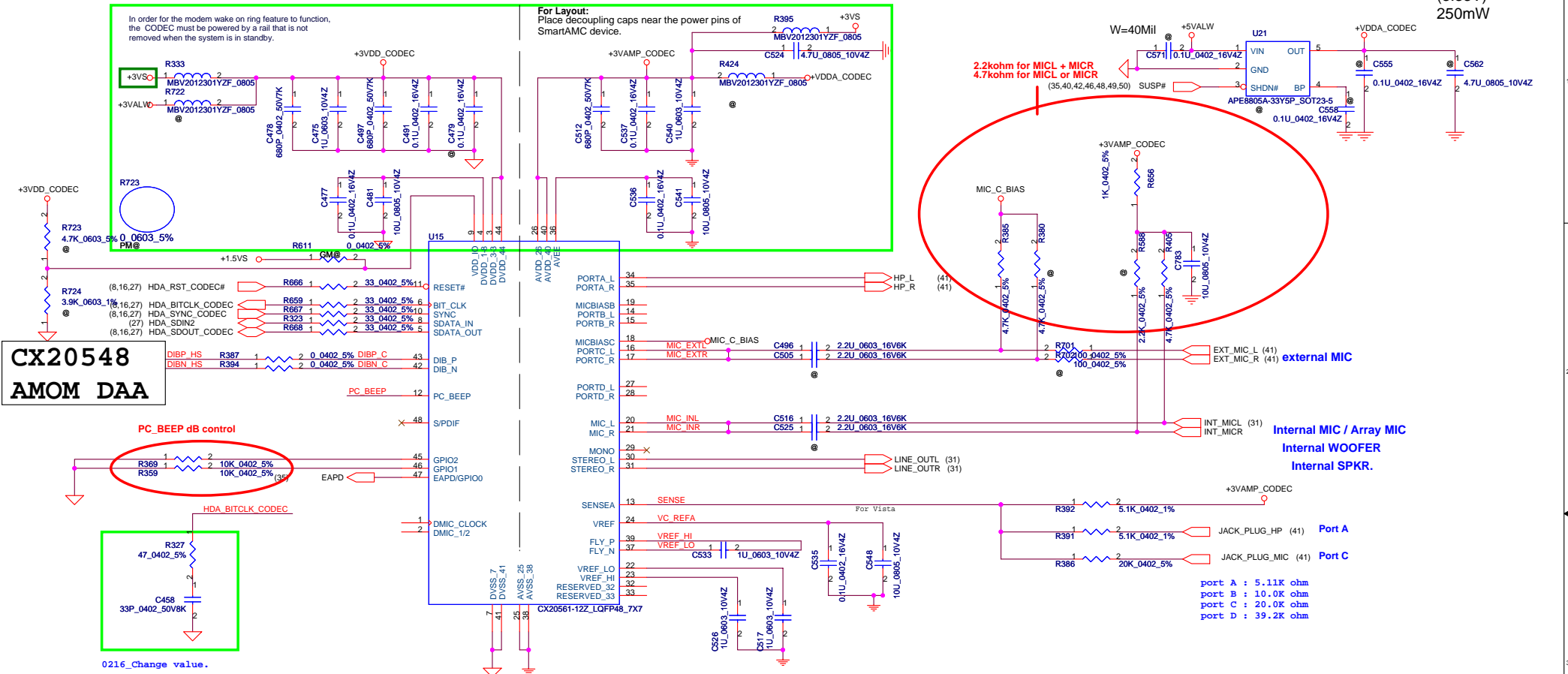
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

CODEC POWER

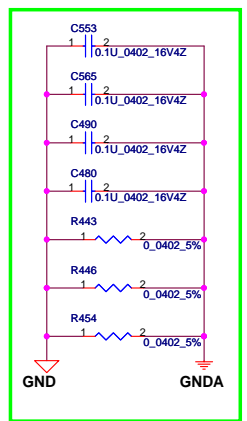
(3.33V)
250mW



**CX20548
AMOM DAA**

**CX20548
AMOM DAA**

DIGITAL ANALOG

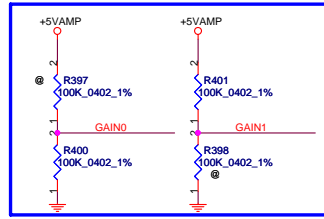


Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

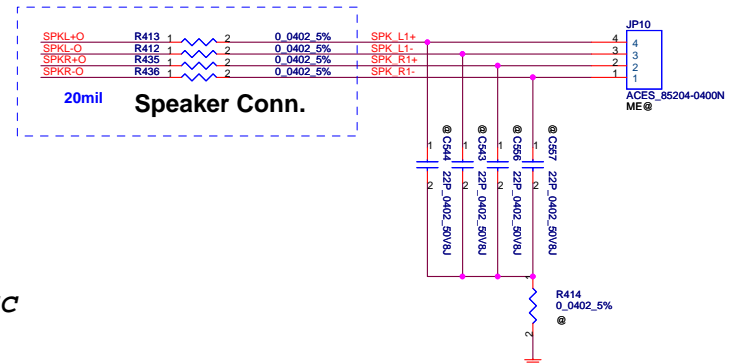
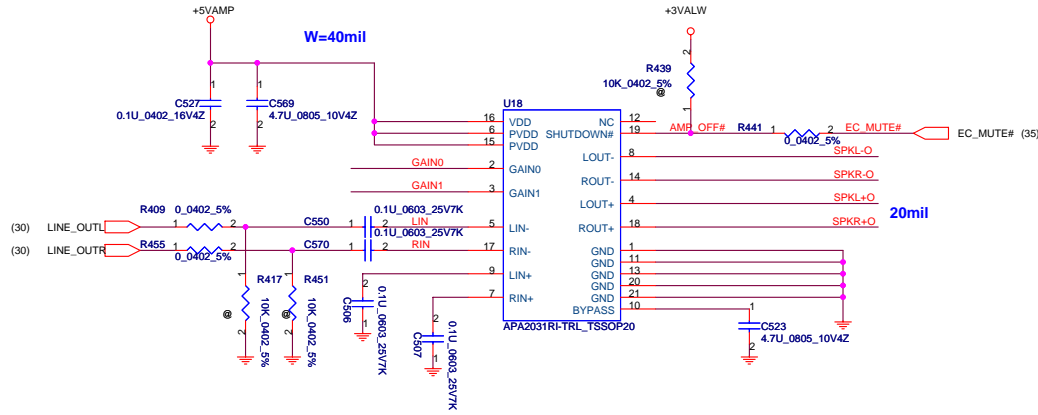
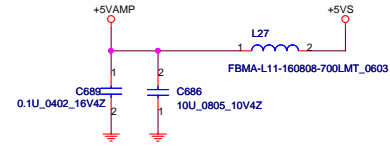
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				Document Number JIWA1/A2_LA-42LIP	
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				Date: Monday, May 12, 2008	
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Speaker Amplifier

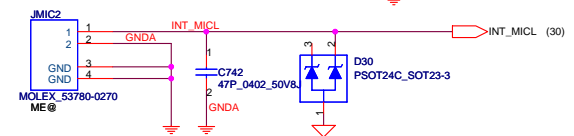
1nd = TPA6017 (SA601720010)
 2nd = APA2031 (SA00001RZ00)



GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

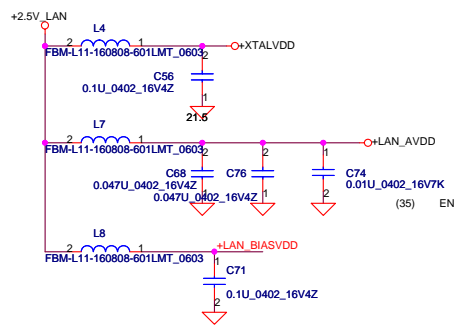


INT MIC

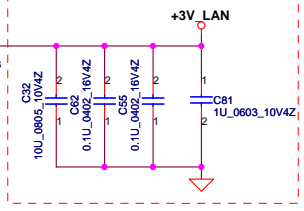


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Compal Electronics, Inc. AMP/VR/Audio Jack/MIC			Size	Rev
Document Number Custom JIWA1/A2_LA-4211P			1.0	
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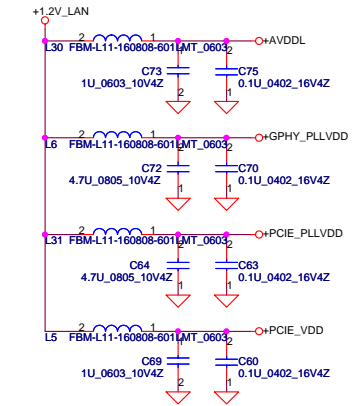
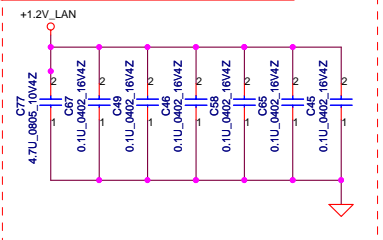
Layout Notice : Filter place as close chip as possible.



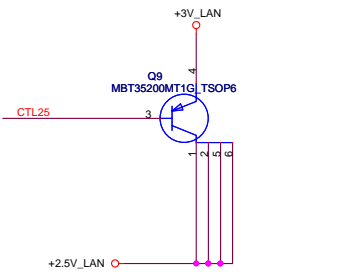
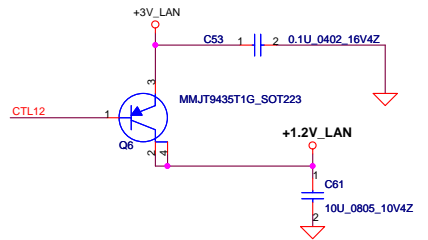
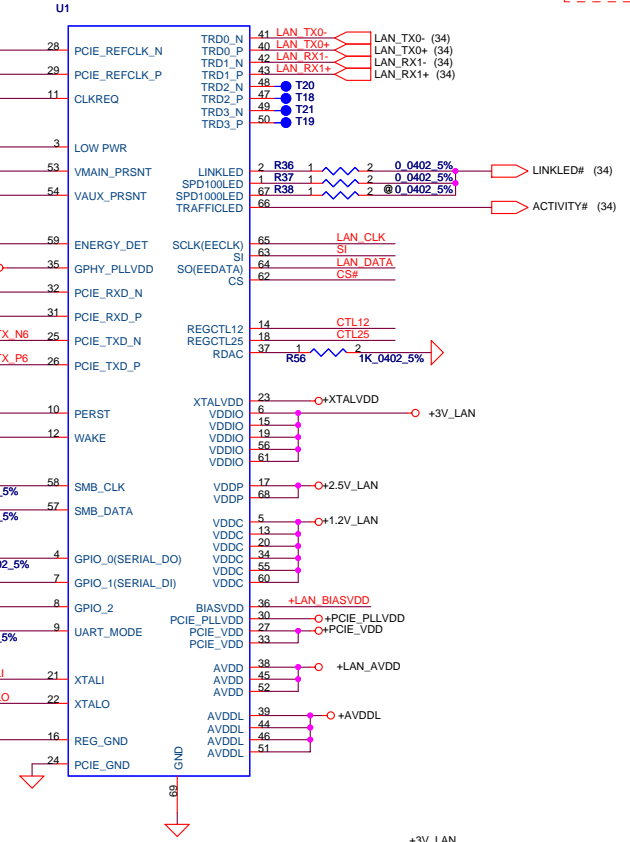
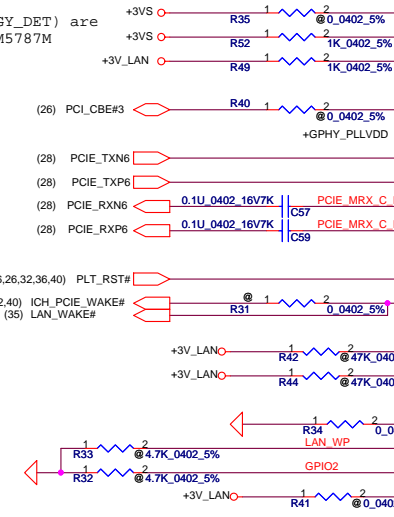
Layout Notice : Place as close chip as possible.



Layout Notice : 1.2V filter. Place as close chip as possible.



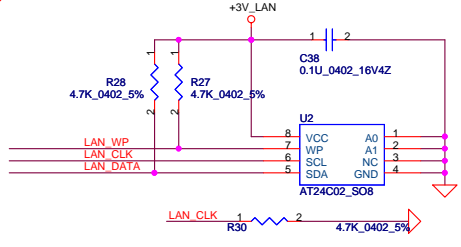
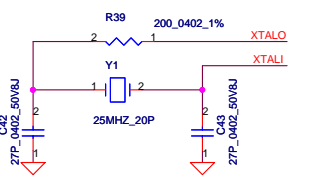
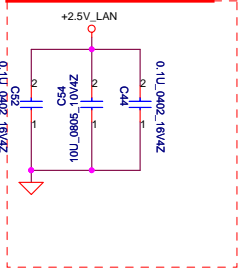
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



Notice : 4.7u 6.3V capacitor Thickness 1.25mm

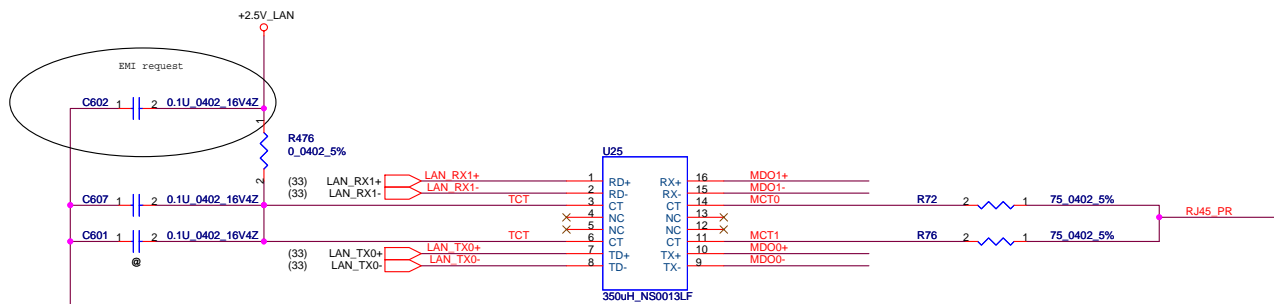
Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

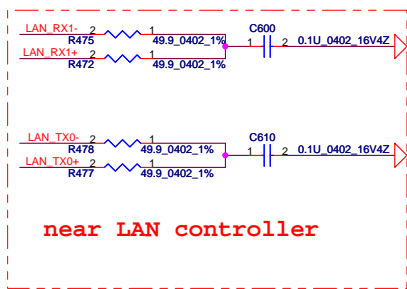


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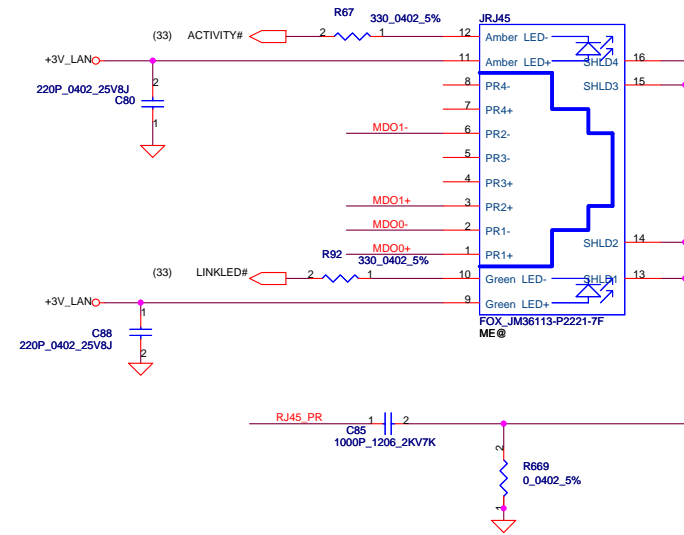
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			BCM5787MKML	
Size	Document Number			Rev
Custom	J1WA1/A2_LA-4211P			1.0
Date:	Monday, May 12, 2008	Sheet	33	of 53



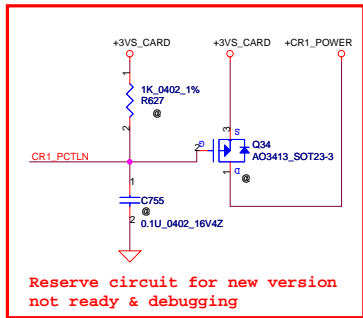
Change C468, C470, C473, C474, C475, C476 from 0.01uF to 0.1uF



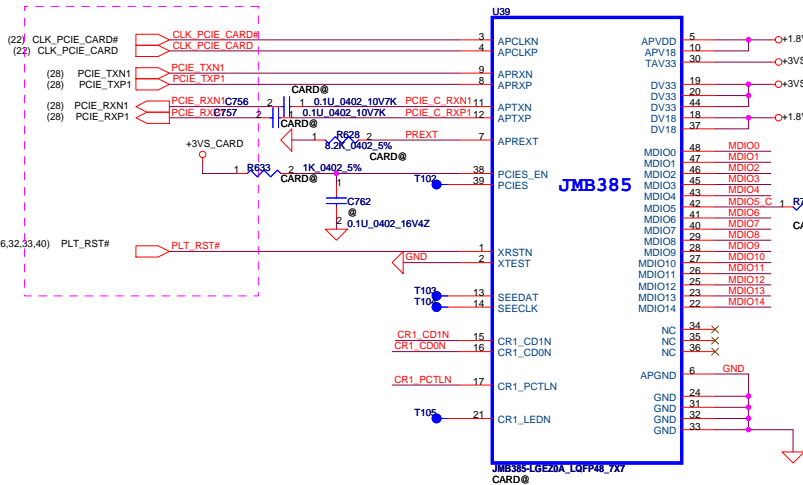
RJ45 CONN



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				JJWA1/A2_LA-421IP	
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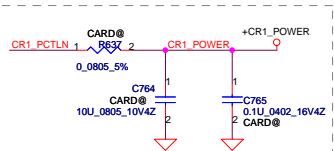
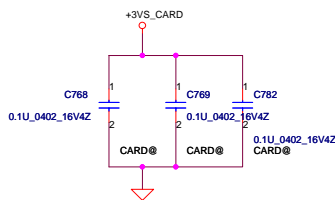
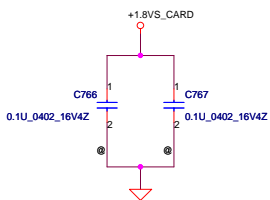
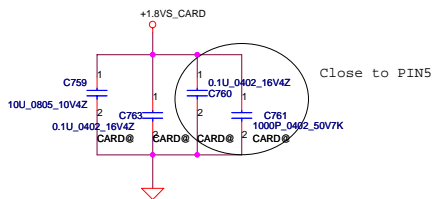
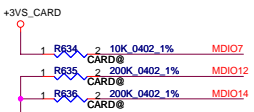
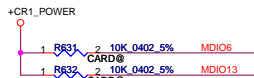


Need check CLK GEN & SB select pin & page



JMB385 Operation Modes

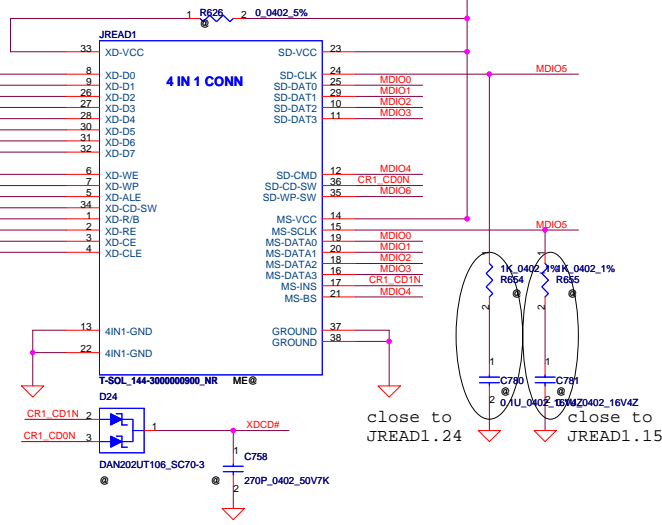
	Normal
XTEST	0
CR1_CD0N	X
CR1_CD1N	X



Use 0805 type and over 20 mils trace width on both side

Card Reader power circuit

- MDIO0 @: R671 2 0.0402 5%
- MDIO1 @: R672 2 0.0402 5%
- MDIO2 @: R673 2 0.0402 5%
- MDIO3 @: R674 2 0.0402 5%
- MDIO4 @: R675 2 0.0402 5%
- MDIO5 @: R676 2 0.0402 5%
- MDIO6 @: R677 2 0.0402 5%
- MDIO7 @: R678 2 0.0402 5%
- MDIO8 @: R679 2 0.0402 5%
- MDIO9 @: R680 2 0.0402 5%
- MDIO10 @: R681 2 0.0402 5%
- MDIO11 @: R682 2 0.0402 5%
- MDIO12 @: R683 2 0.0402 5%
- MDIO13 @: R684 2 0.0402 5%
- MDIO14 @: R685 2 0.0402 5%

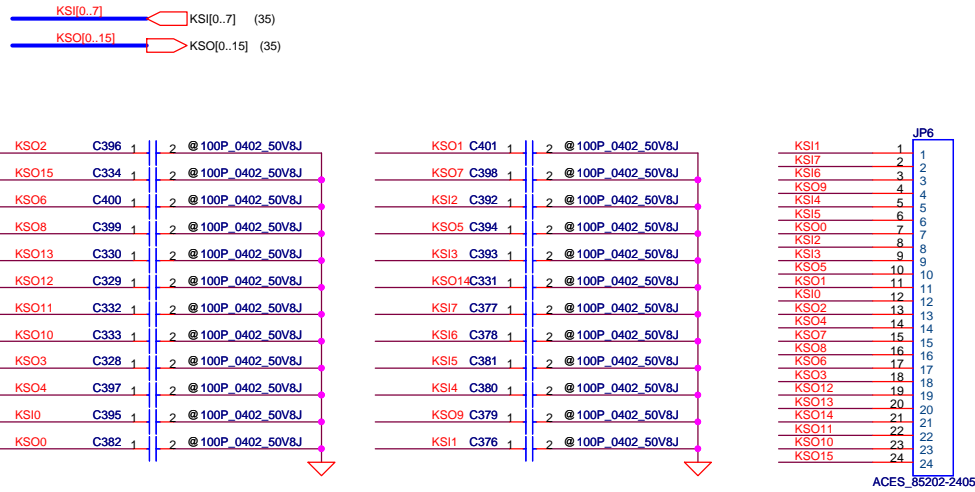


SD,MMC,MS,XD multi-function pin define

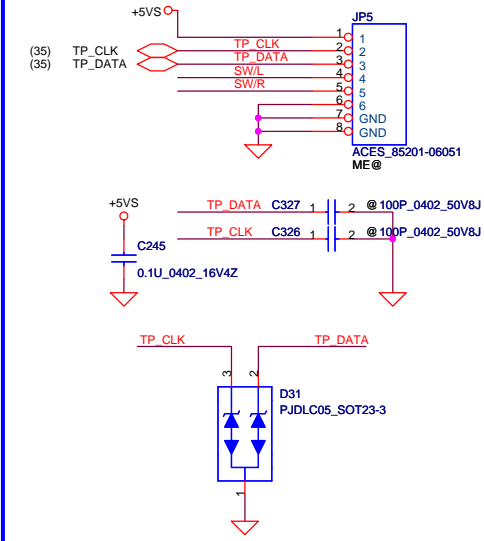
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

Cardreader contactor not support MMC & MS Bit 4~7

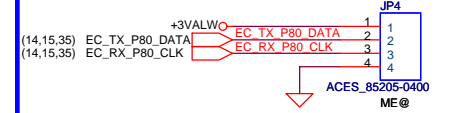
INT_KBD Conn.



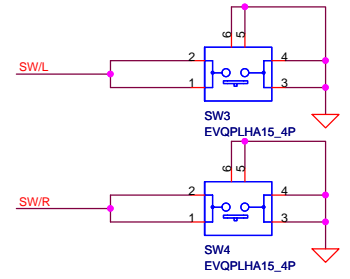
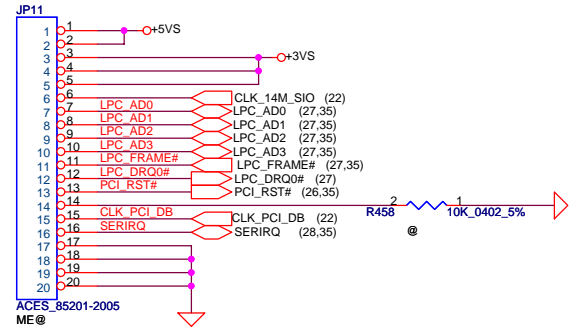
To TP/B Conn.



EC DEBUG PORT

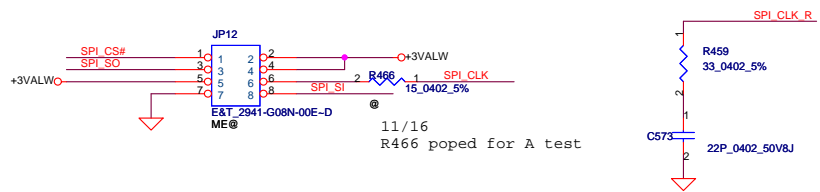
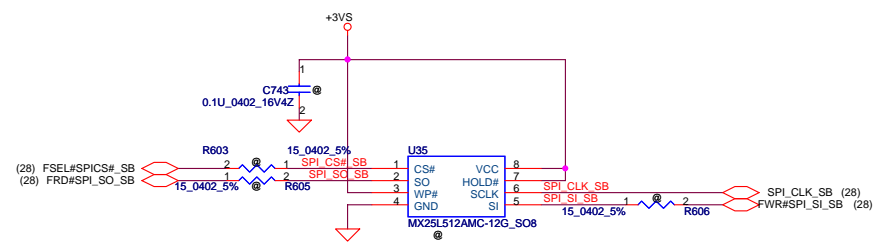
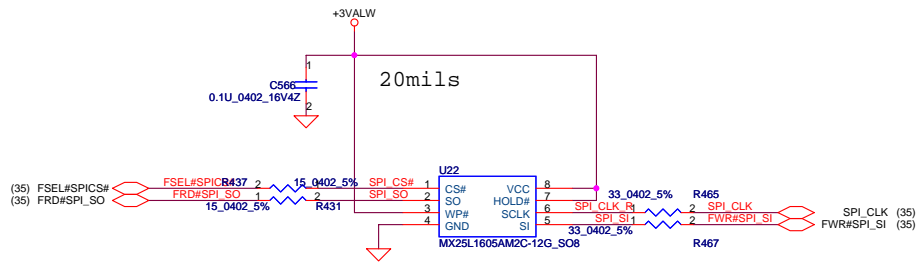


FOR LPC SIO DEBUG PORT

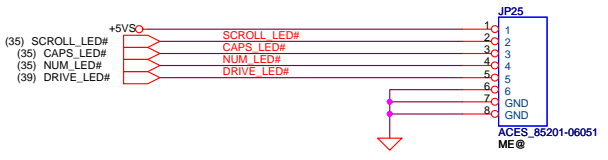
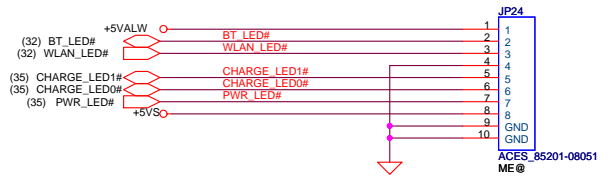
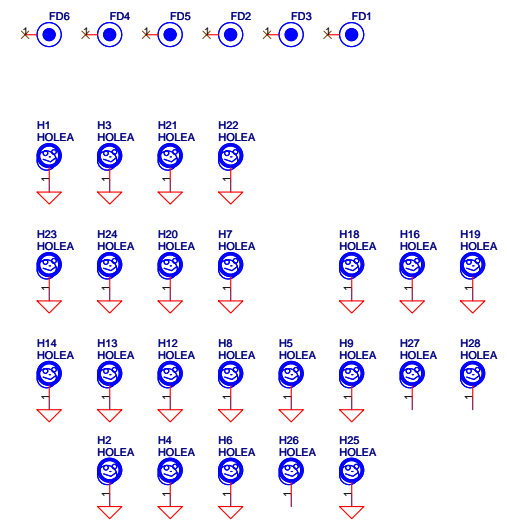
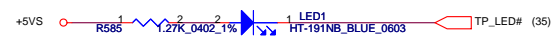


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				B	JJWA1/A2_LA-4211P
				Date:	Monday, May 12, 2008
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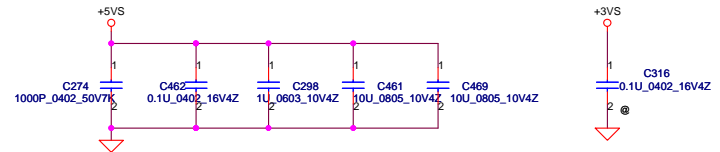
FOR EC 8M SPI ROM



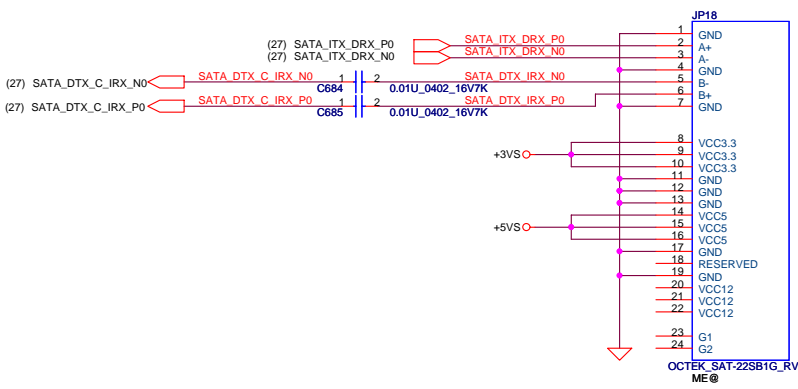
LED



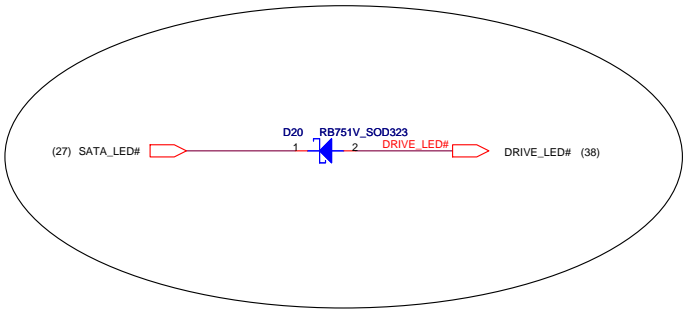
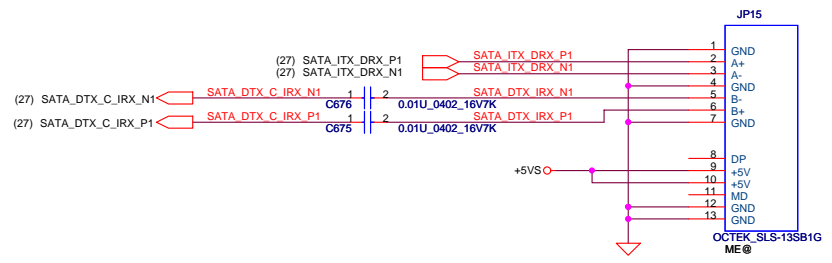
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Issued Date	2007/10/15	Deciphered Date	2008/10/15		
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				Date: Wednesday, May 14, 2008	Rev 1.0
				Sheet 38	of 53



SATA HDD Conn.



SATA ODD Conn.

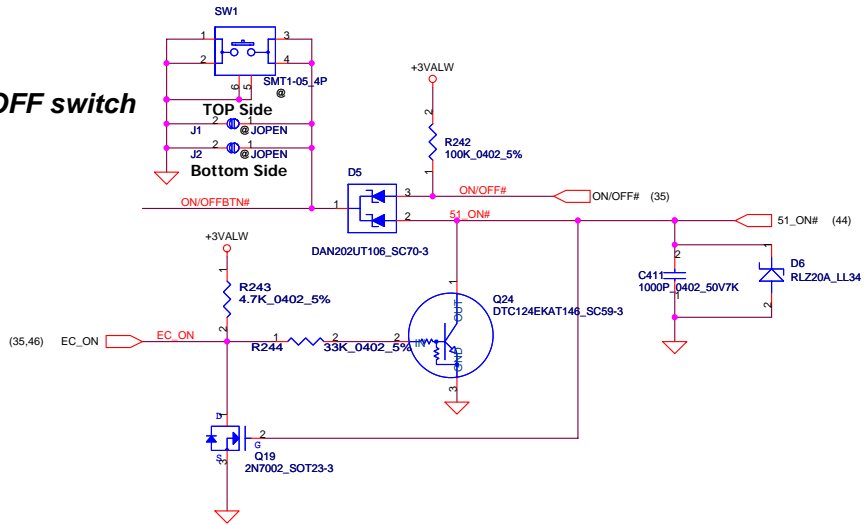


Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15		
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			Date:	Monday, May 12, 2008	Sheet 39 of 53

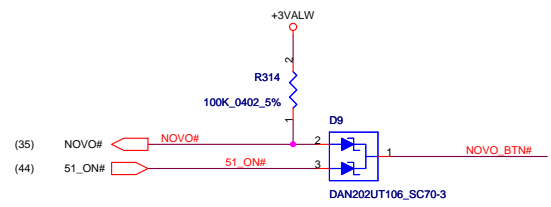
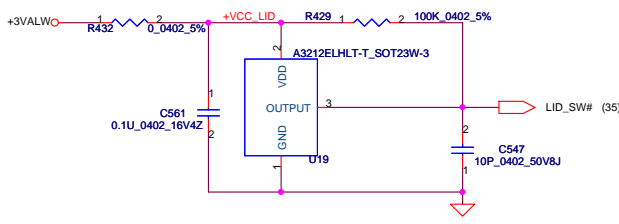
HDD & ODD Connector
 JIWA1/A2_LA-4211P

Power Button

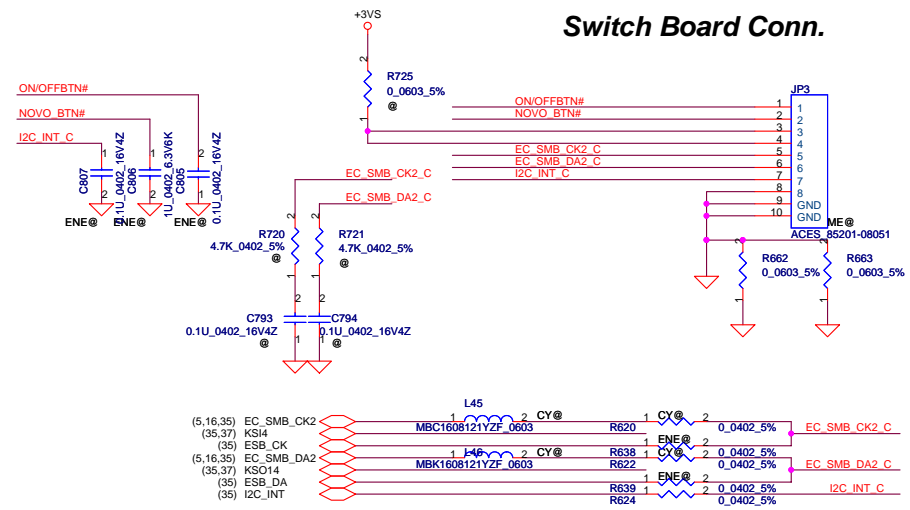
ON/OFF switch



Lid Switch

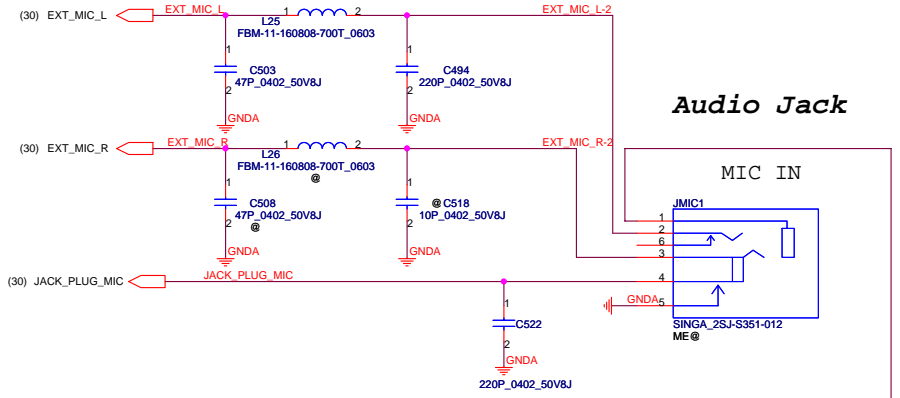


Switch Board Conn.

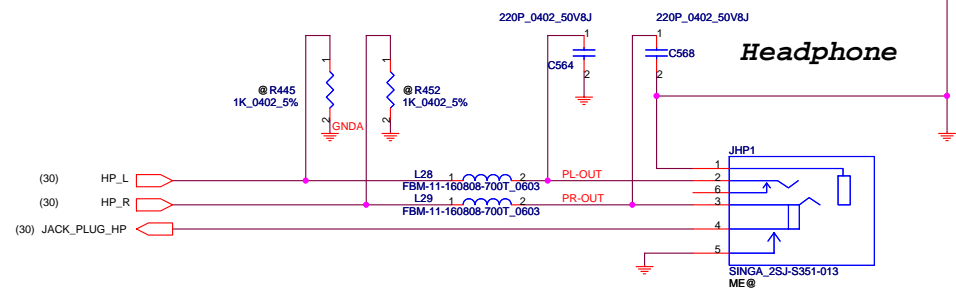


8 mil

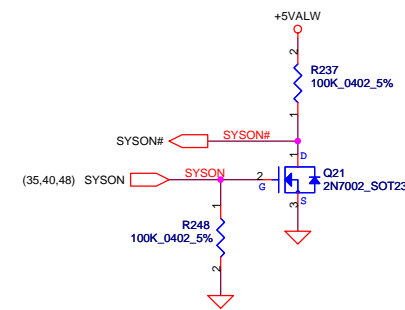
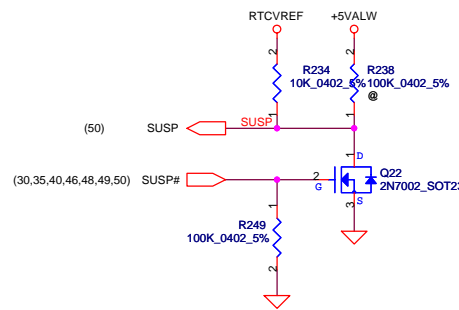
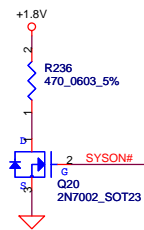
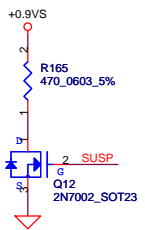
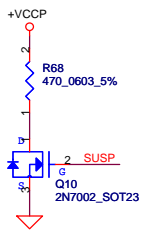
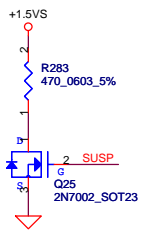
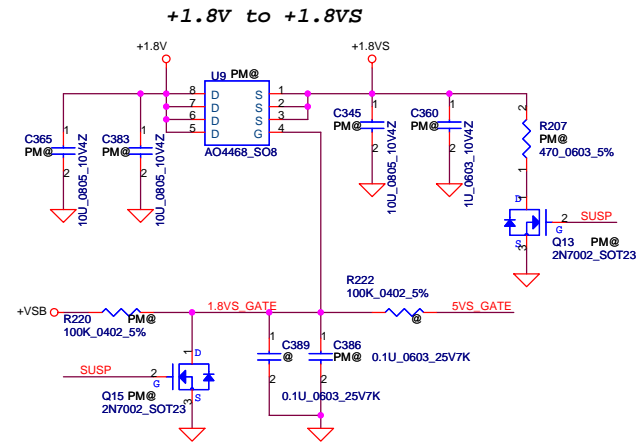
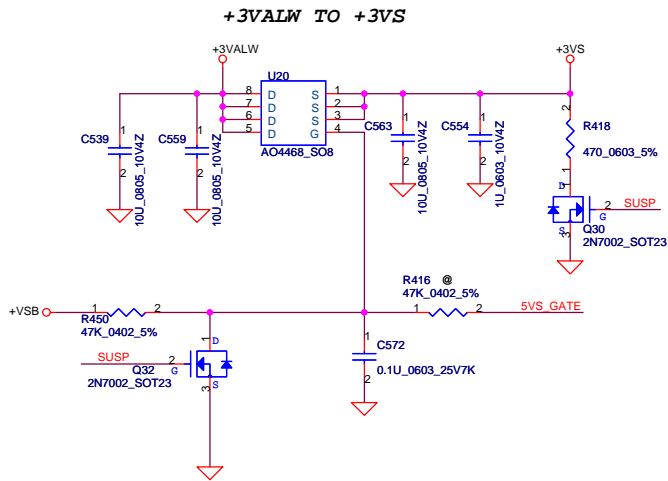
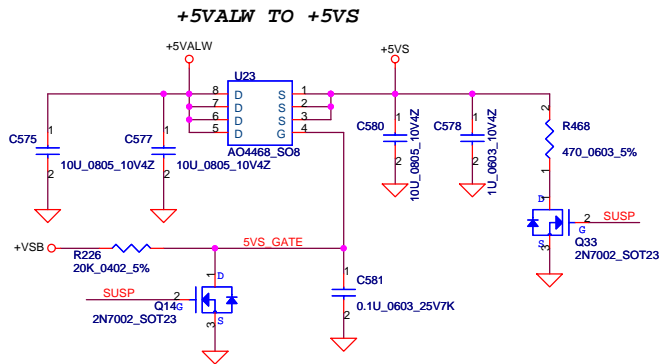
Audio Jack



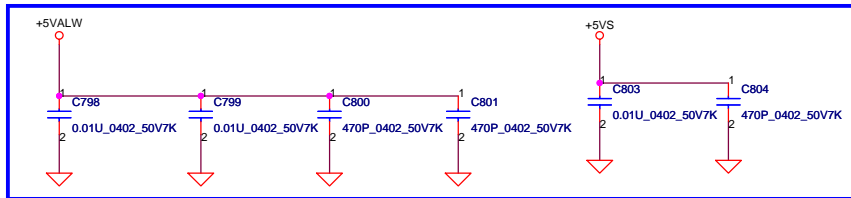
Headphone



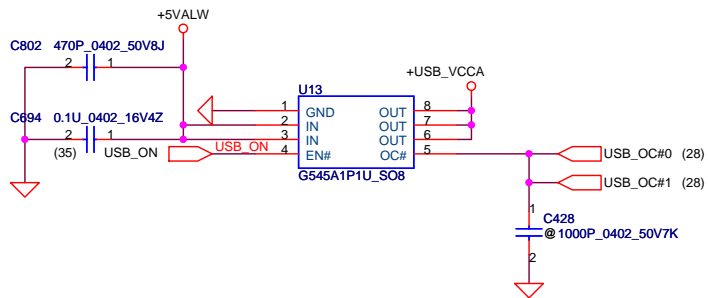
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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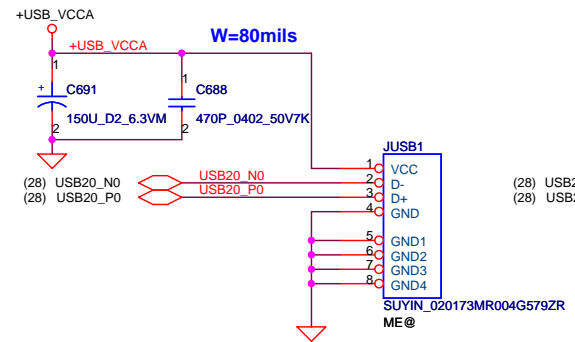
for EMI



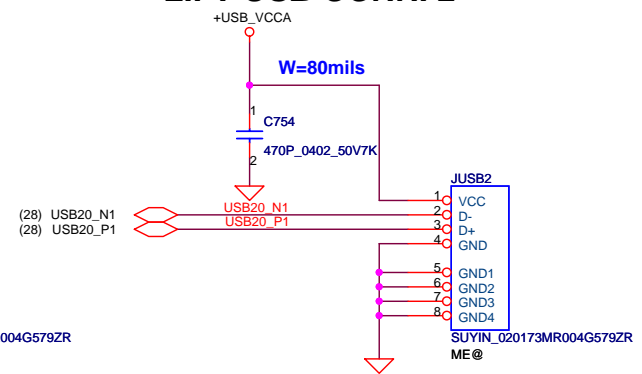
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number			Rev	1.0
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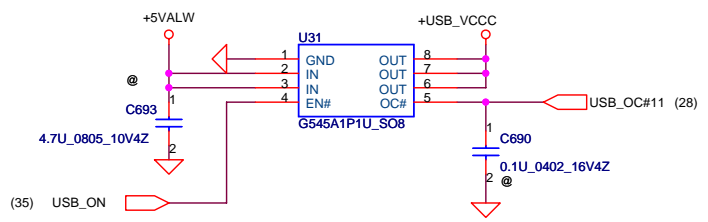
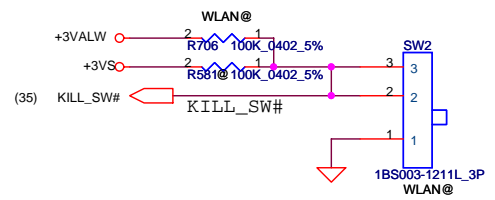
LIFT USB CONN. 1



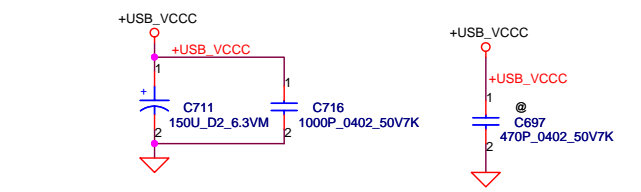
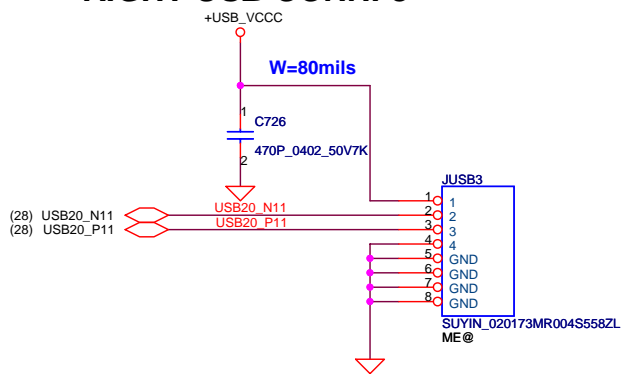
LIFT USB CONN. 2



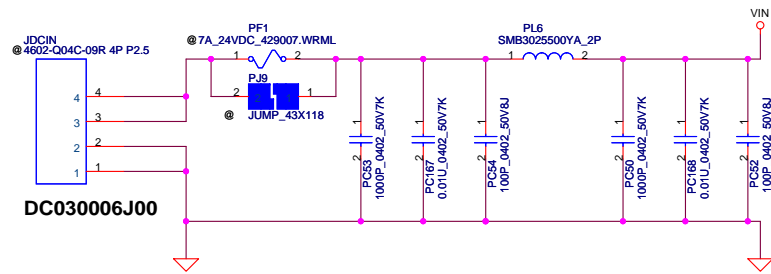
Kill Switch



RIGHT USB CONN. 3



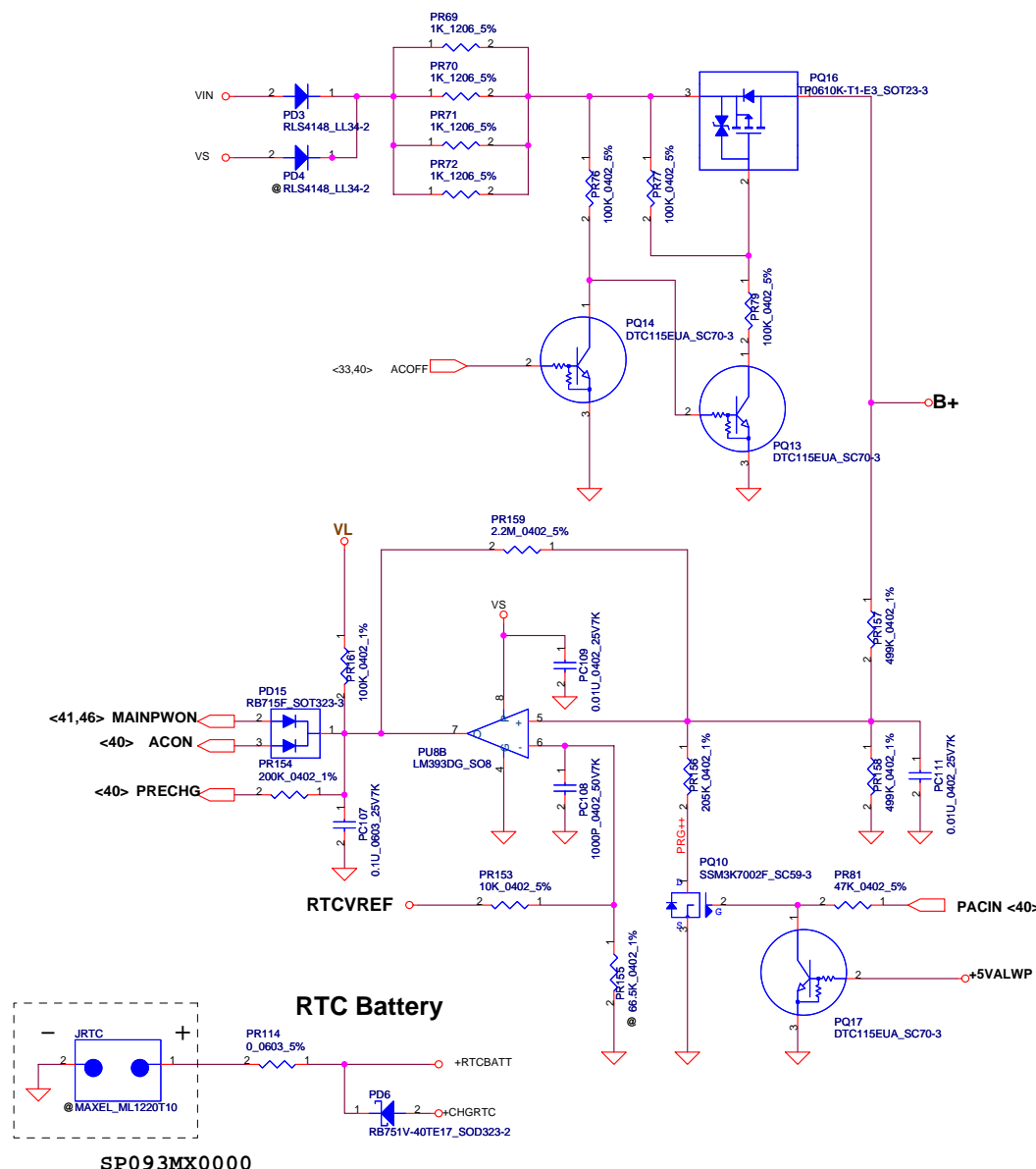
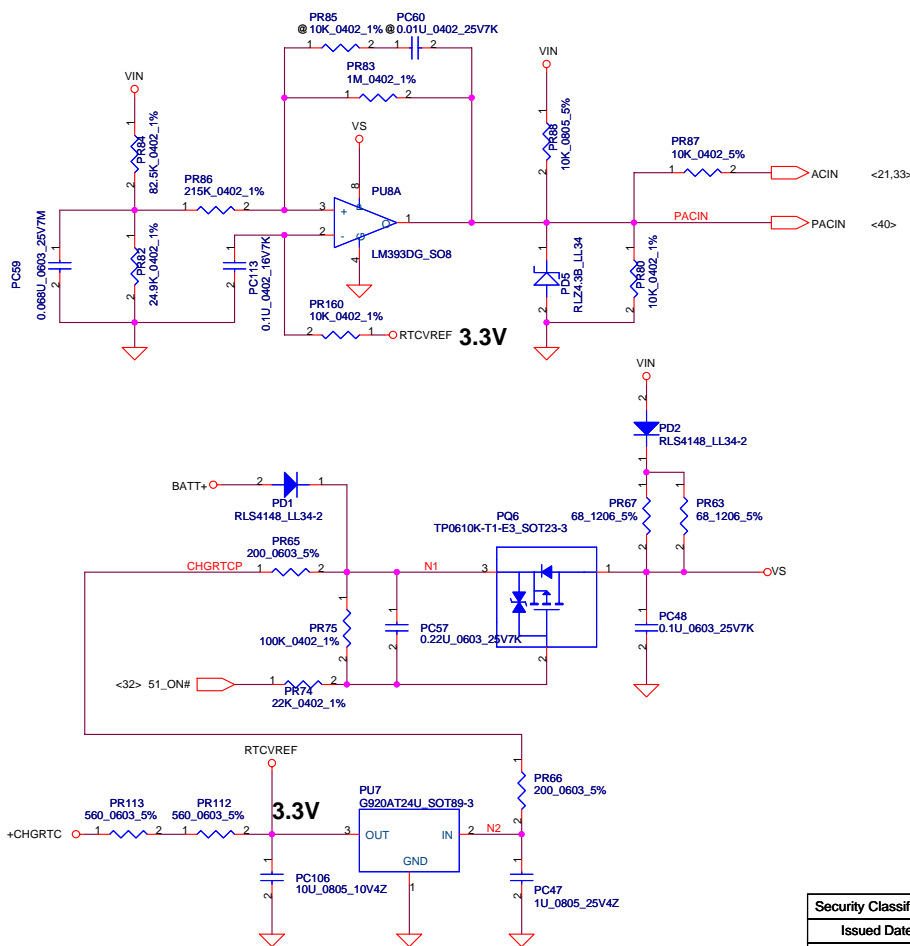
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Power OK, Reset and RTC Circuit, TP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	J1WA1/A2_LA-4211P
				Date:	Tuesday, May 13, 2008
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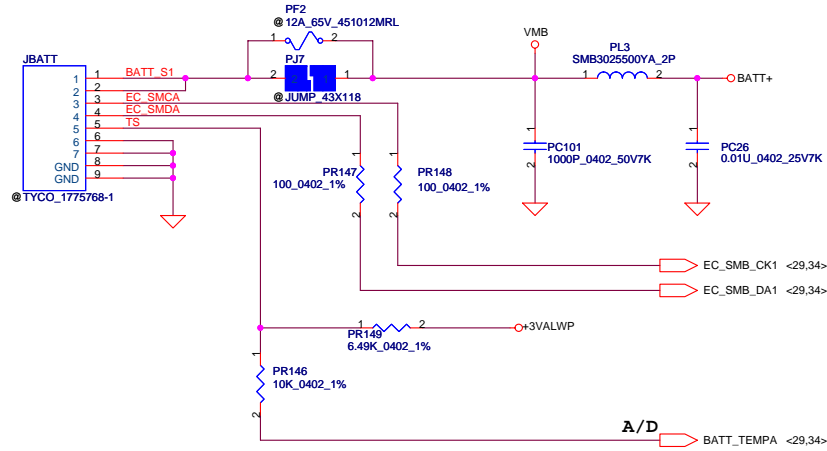
Vin Detector		
High	18.135	17.566
Low	14.866	14.355
	17.011	14.063

ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	13.843V	14.247V	14.636V
L->H	14.936V	15.381V	15.814V

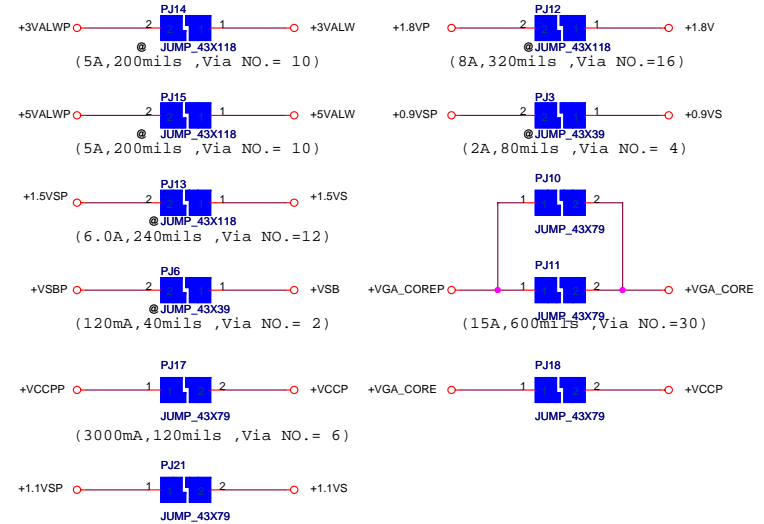
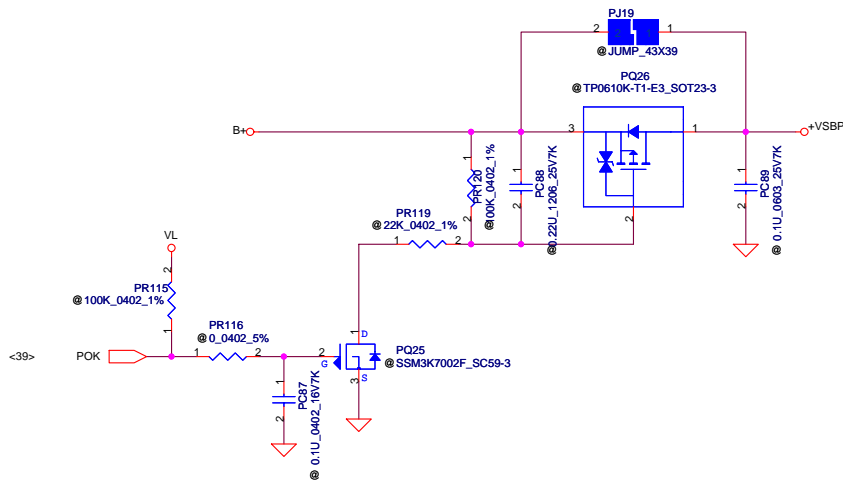
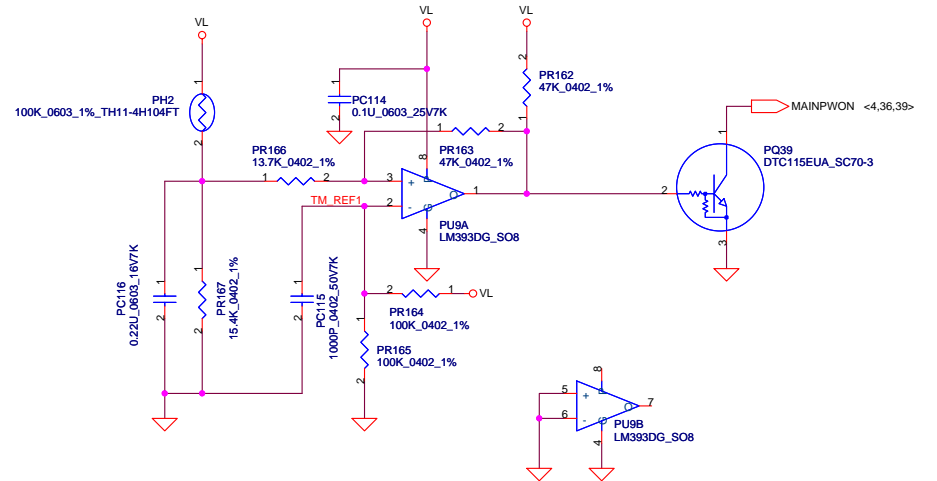
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



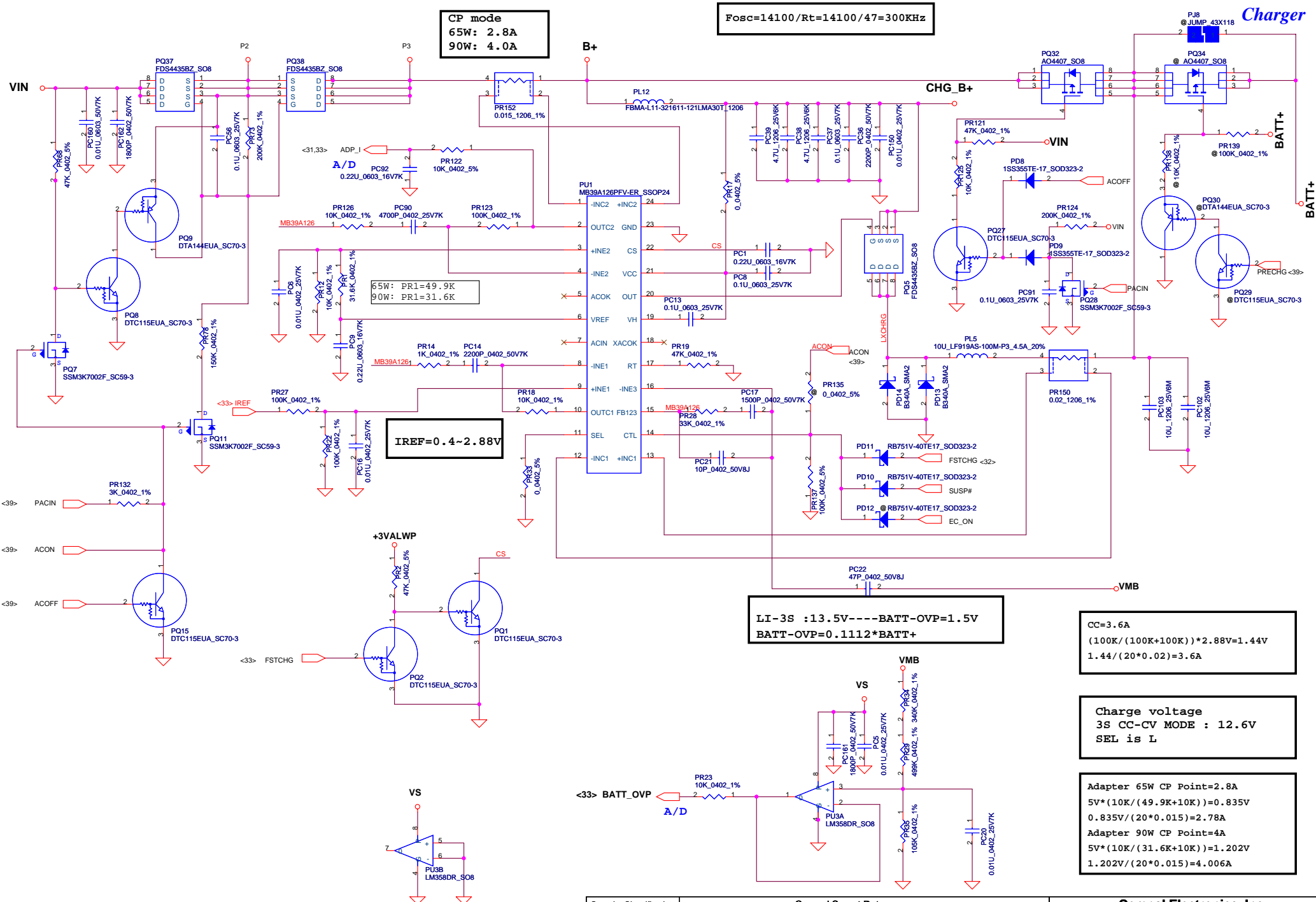
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/06/22	Deciphered Date	2008/06/22	Title	
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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CP mode
 65W: 2.8A
 90W: 4.0A

$F_{osc}=14100/Rt=14100/47=300KHz$

Charger

IREF=0.4~2.88V

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

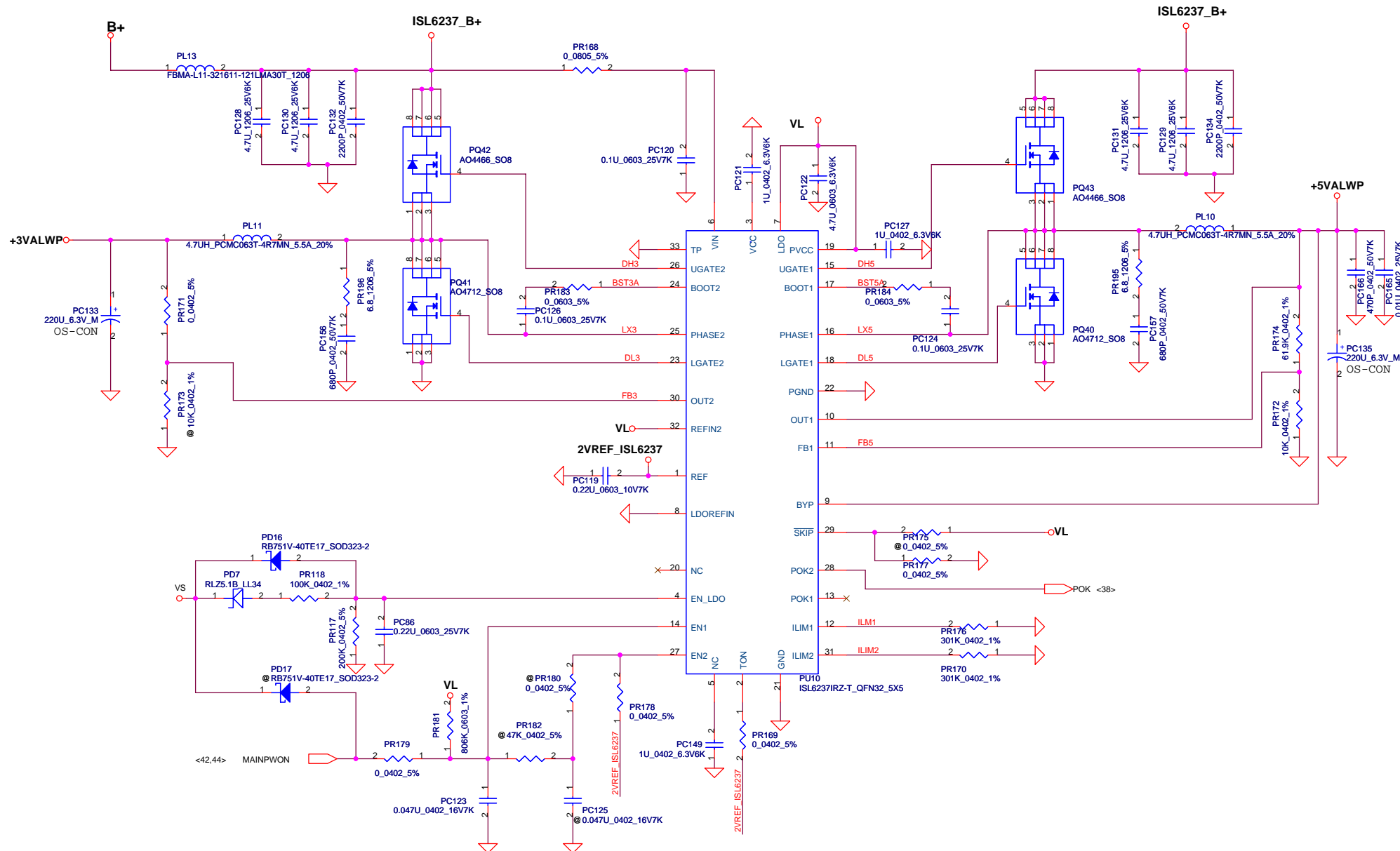
CC=3.6A
 $(100K/(100K+100K))*2.88V=1.44V$
 $1.44V/(20*0.02)=3.6A$

Charge voltage
 3S CC-CV MODE : 12.6V
 SEL is L

Adapter 65W CP Point=2.8A
 $5V*(10K/(49.9K+10K))=0.835V$
 $0.835V/(20*0.015)=2.78A$
 Adapter 90W CP Point=4A
 $5V*(10K/(31.6K+10K))=1.202V$
 $1.202V/(20*0.015)=4.006A$

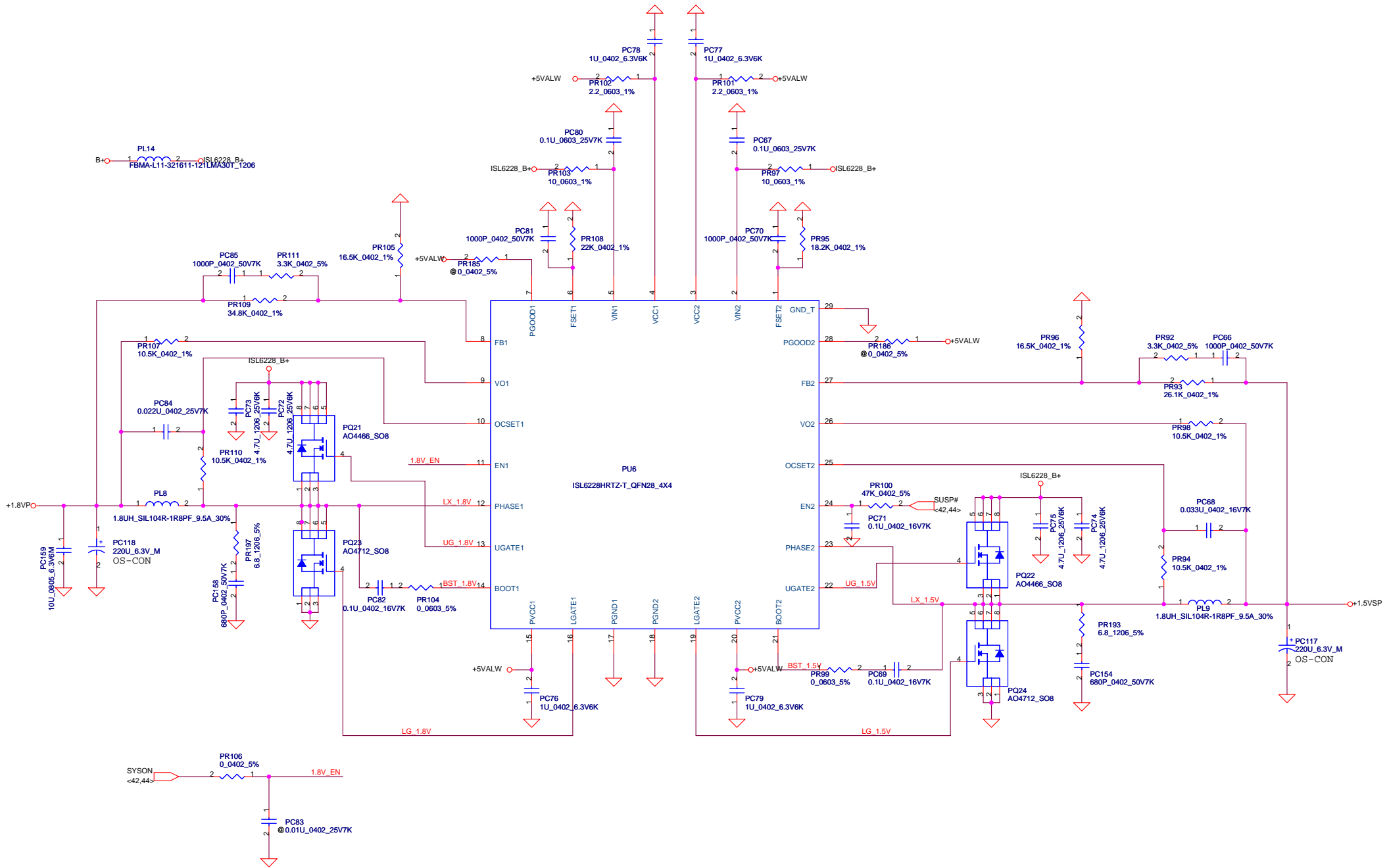
Security Classification	Compal Secret Data		Title
Issued Date	2006/08/04	Deciphered Date	2006/10/06
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Compal Electronics, Inc.		
CHARGER		
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Date:	Monday, May 12, 2008	Sheet 46 of 53

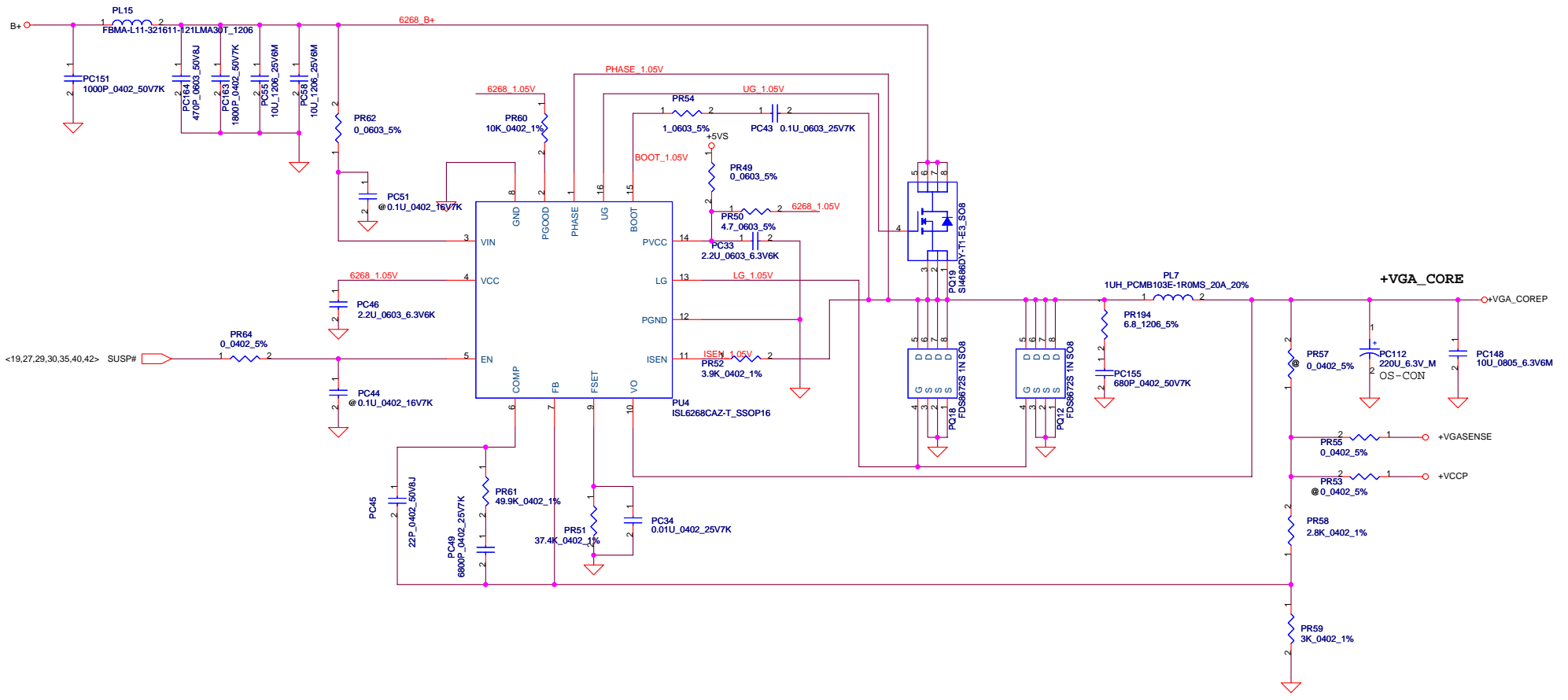


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Issued Date	2007/06/22	Deciphered Date	2008/06/22	+5V/+3V	
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Size	Document Number	Date		Sheet	Rev
Custom		Monday, May 12, 2008		47 of 53	1.0

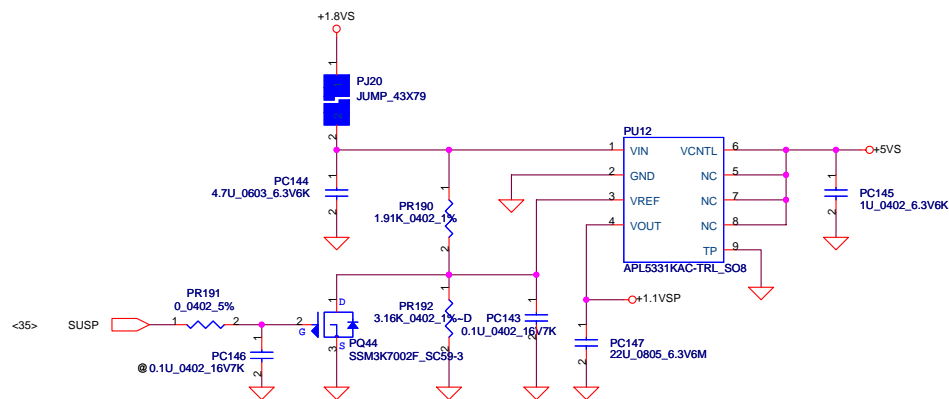
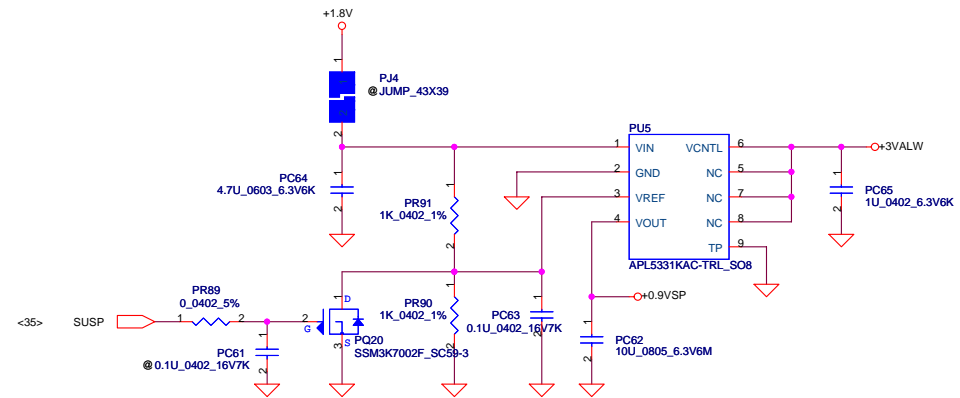
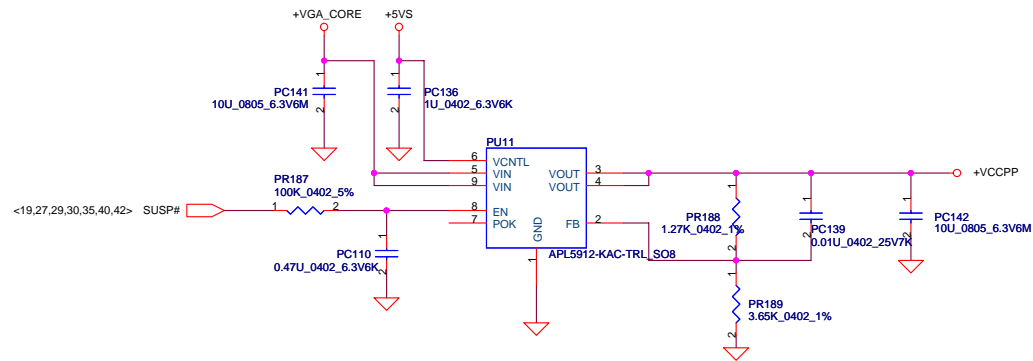
Compal Electronics, Inc.



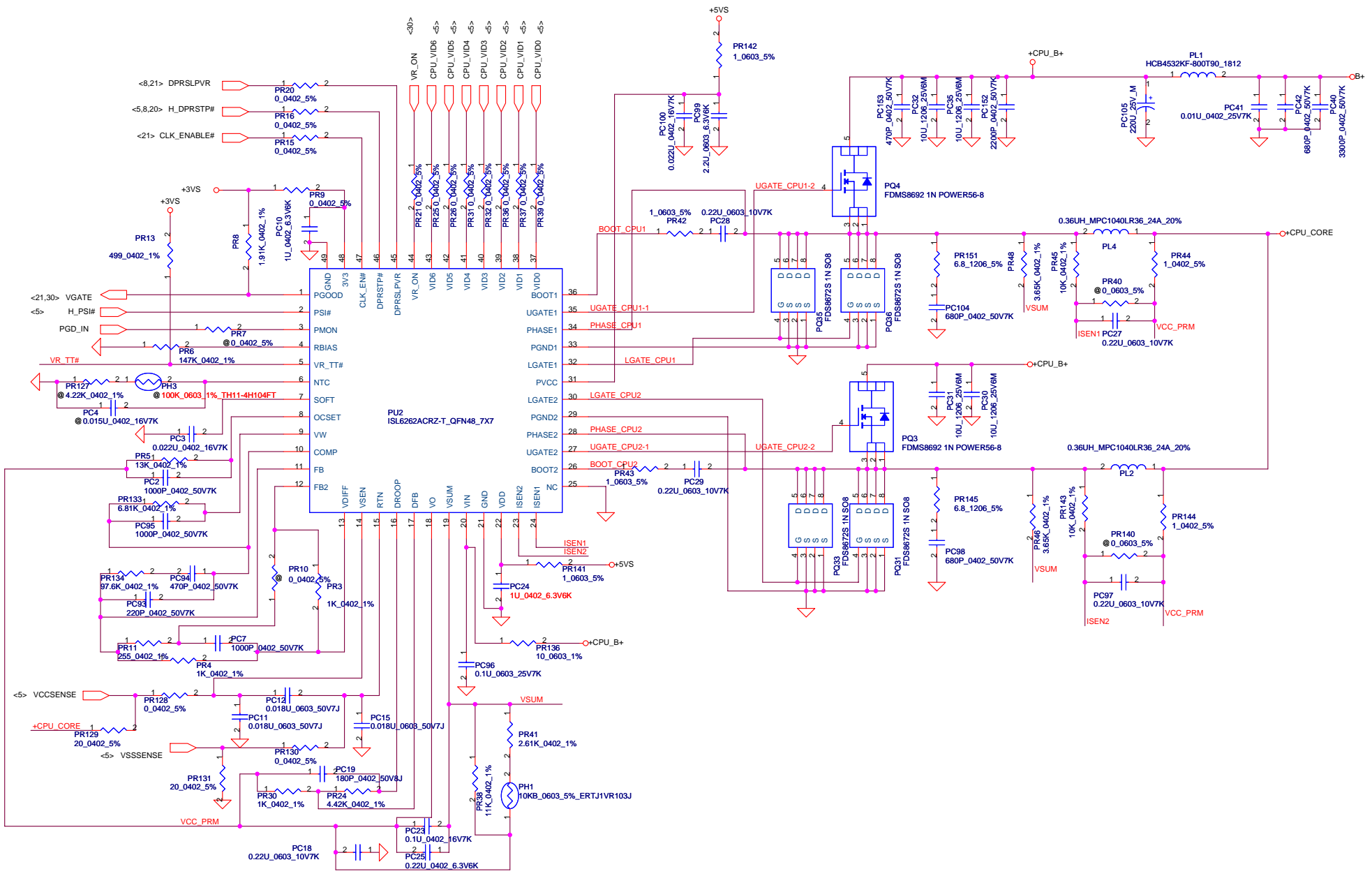
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/06/22	Deciphered Date	2008/06/22	Title	1.8V / 1.5V
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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title	
				VCCP/0.9V/1.1V	
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Security Classification	Compal Secret Data		Title	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	+CPU_CORE
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

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				Document Number	
Date: Monday, May 12, 2008				Sheet 51 of 51	
				Power PIR	
				J1W1A2_LA-421P	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	P29	C615 change to R615 and BOM Structure change to PM@	Fix DIS Audio issue
2	12/10	P20, P21	R104 & R154 BOM Structure change to PM@	Reduce cost
3	12/10	P16	R86, R645, R646, R650, R651, R652 & R653 BOM Structure change to PM@	Reduce cost
4	12/10	P29	R614 change from 10K to 45.3ohm R615 change from 12K to 54.9ohm	Fix UMA Audio issue
5	12/10	P08	R79 change from 33 to 10ohm R80, R81, R82 & R85 change from 0 to 22 ohm	Fix UMA Audio issue
6	12/10	P30	The C783 links to GND	Fix Internal MIC issue
7	12/10	P41	Add L45 & L46 MBC1608121YZF Bead	Fix F/B issue
8	01/02	P11	Change C126 package	
9	01/02	P28	Add R704 to connect VGATE to M_PWROK	Modify power sequence
10	01/02	P16	Add R699 to connect +VGASENSE	
11	01/02	P16	Remove U3.P1	
12	01/02	P16	Add R700 to connect GND	
13	02/15	P08	Change R147 from 511 ohm 1% to 499 ohm 1%	
14	02/15	P23	Change D4 location	
15	02/15	P23	Add D25 & D26 for ESD	
16	02/15	P25	Add D27, D28 & D29 for ESD	
17	02/15	P29	Add R713 connect to 1.5V	
18	05/08	P05	Add R726 1k ohm & C808 0.1uF to fix issue.	
19	05/08	P16	Remove R48 for EMI request.	
20	05/08	P23	Remove HDMI function.	
21	05/08	P27	Change R554 from 0 ohm to 33 ohm for EMI request.	
22	05/08	P28	Add R566 10 ohm & C733 10pF for EMI request.	
23	05/08	P30	Add R327 47 ohm & C458 33pF for EMI request.	
24	05/08	P35	Change C501 & C514 from 15pF to 12pF	
25	05/08	P37	Add D31 (PJDLCO5_SOT23-3) for ESD request.	
26	05/08	P41	Add C494, C522, C564 & C568 220pF for EMI request	

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