

Compal Confidential

UMA M/B Schematics Document Haswell with DDRIII + Lynx Point PCH

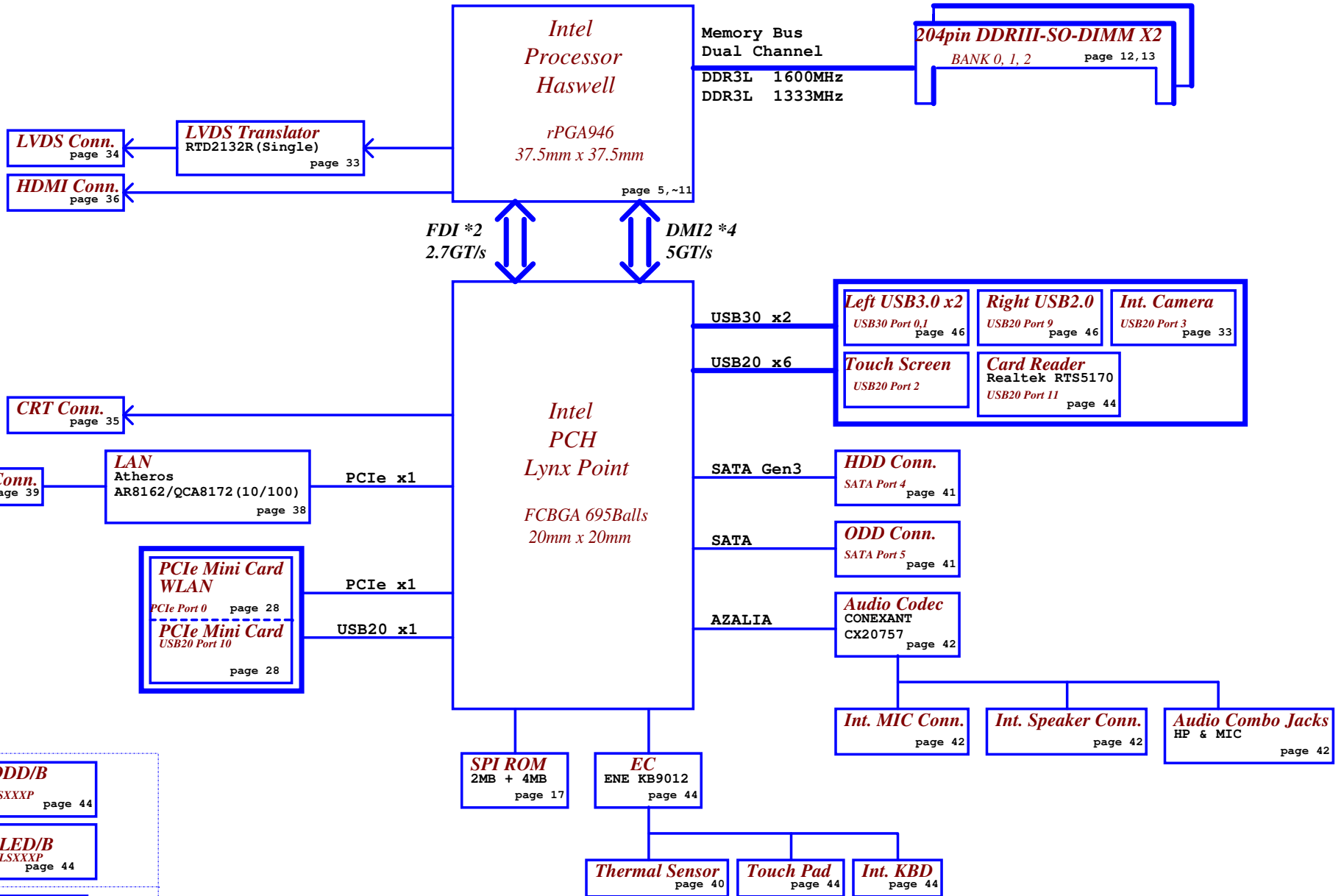
2013-04-18

LA-9642P

REV: 1.0

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				Document Number	LA-9642P
				Date:	Friday, April 19, 2013
				Sheet	1 of 49

Shark Bay



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				Block Diagram
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Document Number			Rev	
LA-9642P			%	

Voltage Rails

power plane	+B	+5VALW	+1.35V	+3VS	+VCC_CORE +VGA_CORE
State					
S0	○	○	○	○	
S3	○	○	○	○	X
S5 S4/AC	○	○	X	X	X
S5 S4/ Battery only	○	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	Ra/Rc/Re	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
3.3V +/- 5%	100K +/- 5%						
Board ID							
0	0		0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%		0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%		0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%		0.712 V	0.819 V	0.875 V	G-series	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
		4	
	UHCI2	5	
		6	
7			
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
		12	
		13	

BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Camera	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
Right side USB	RUSB@
Zero ODD circuit	ZODD@
Share ROM	SROM@
Non-share ROM	NOSROM@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

VRAM BOM STRUCTURE Refer P4. VGA NOTE

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b

Device	Address
Thermal Sensor	1001_100xb

PCH SM Bus address

AMD-GPU SM Bus address

Device	Address
DDR DIMM1 ChannelA	0xA0
DDR DIMM2 ChannelB	0xA4

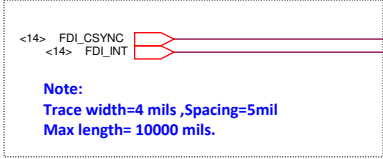
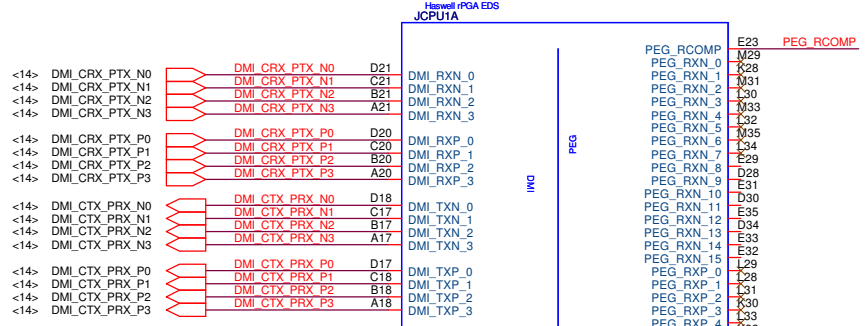
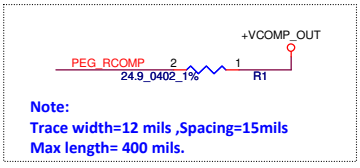
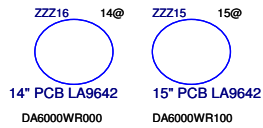
Device	Address
Internal thermal sensor	1000_001xb

Device	Address
RTD2132R	1101 010Xb

SMBUS Control Table

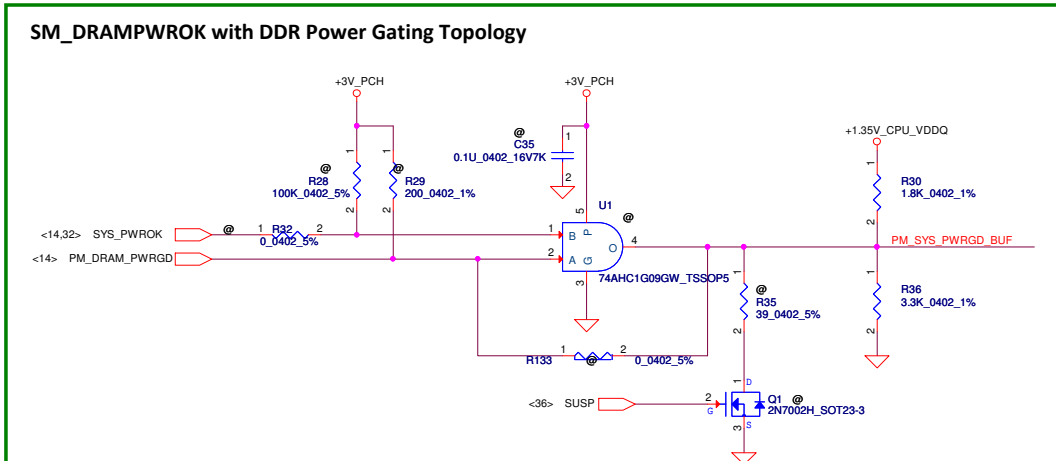
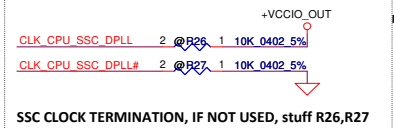
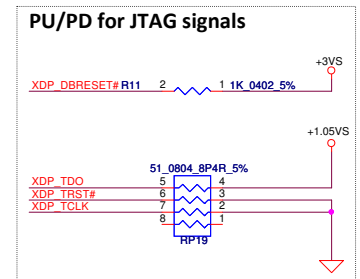
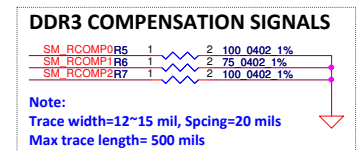
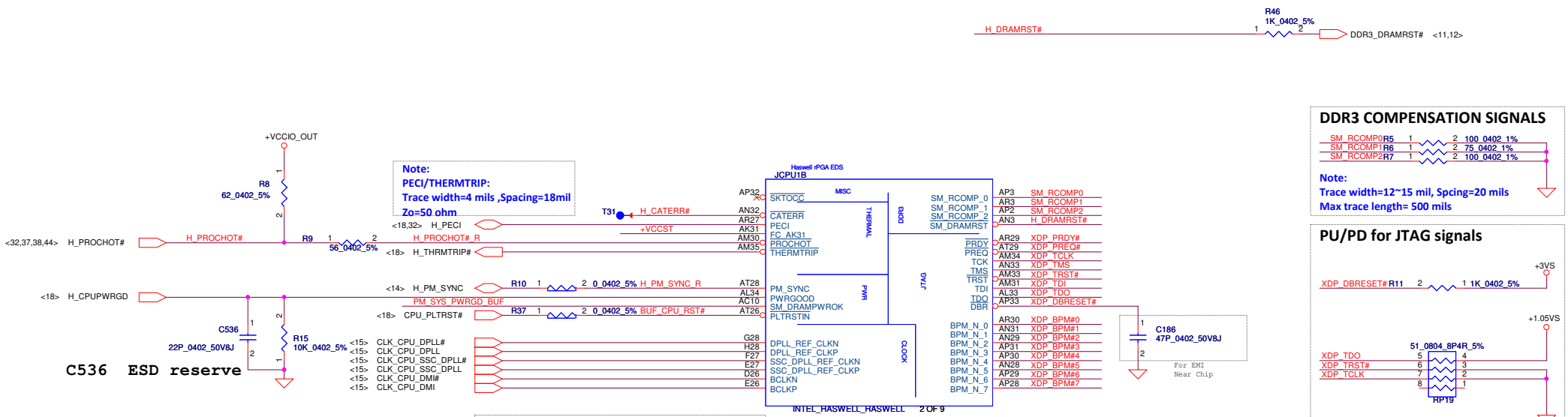
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	+3VS	+3VS
SMB_EC_DA2	+3VALW								
SMBCLK	PCH	X	X	X	V	V	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	V	X	V	X	X	V	X	V
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

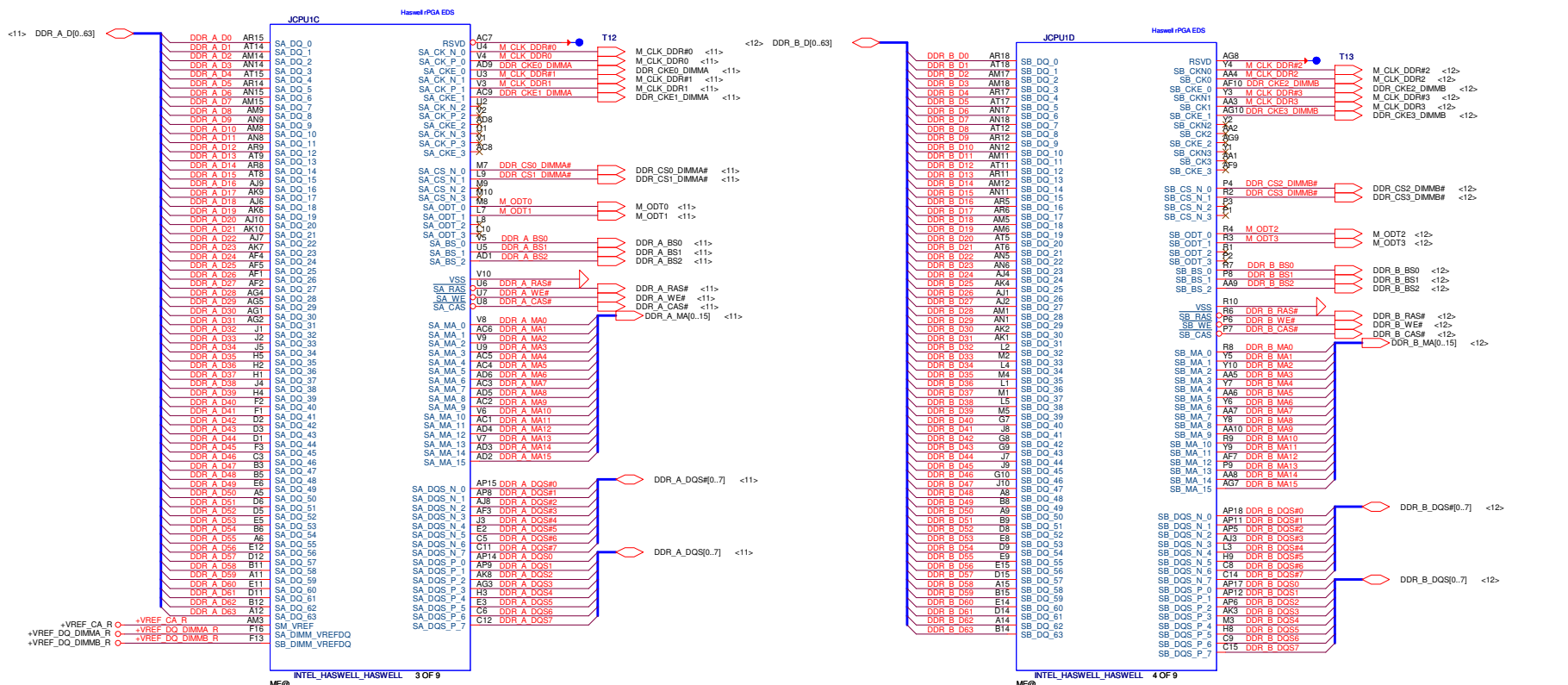
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				Sheet	3	of 49	



INTEL_HASWELL_HASWELL 1 OF 9
ME@

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Date:	Friday, April 19, 2013	Sheet	4 of 49		



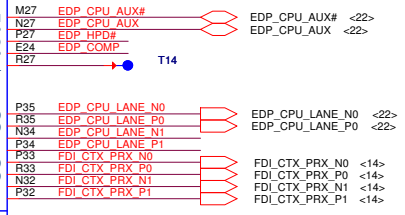
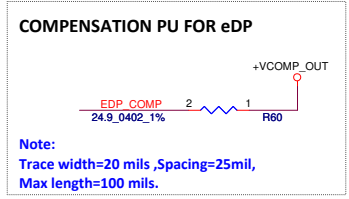
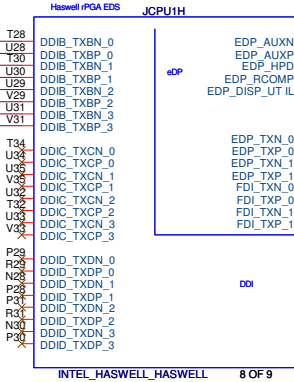
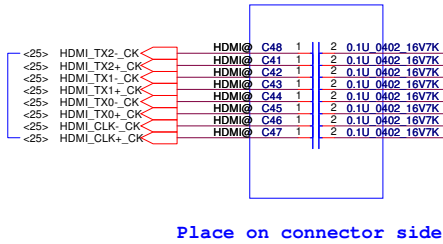


CPI DRIVER VREF PATH IS DEFAULT

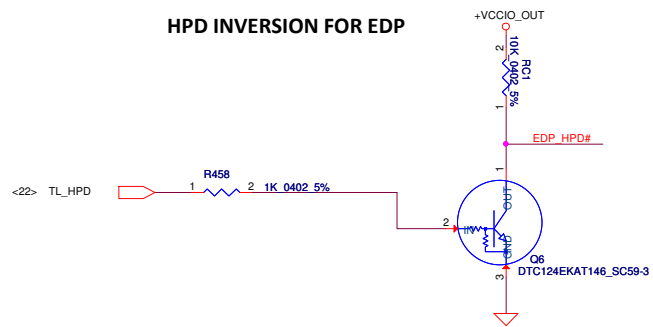
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Document Number	LA-9642P	Revision	(%)	Date	Friday, April 19, 2013
Sheet			6 of 49		

HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI



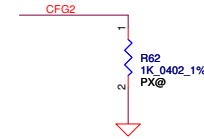
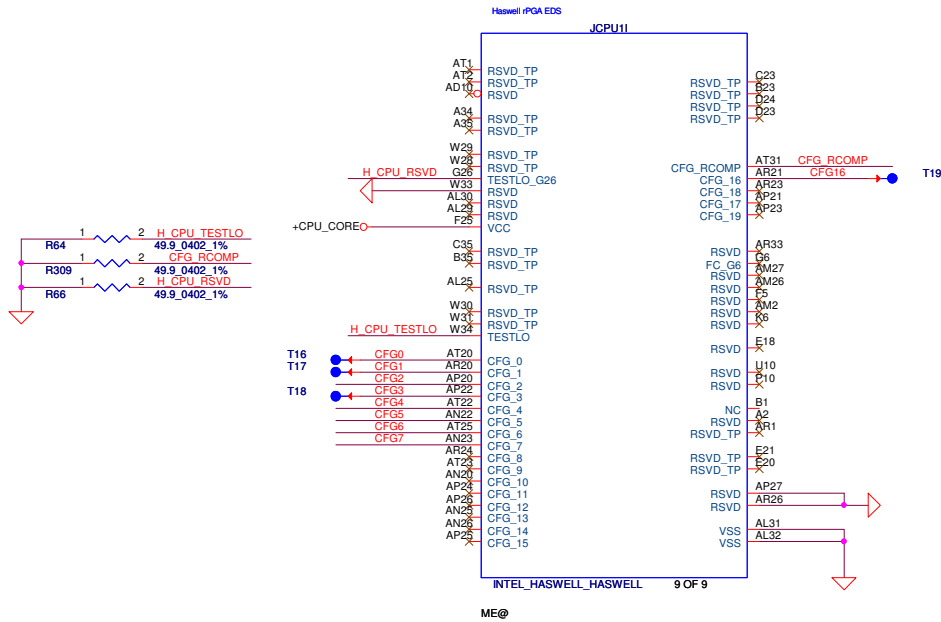
HPD INVERSION FOR EDP



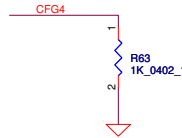
HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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				LA-9642P	(%)
				Date: Friday, April 19, 2013	Sheet 7 of 49

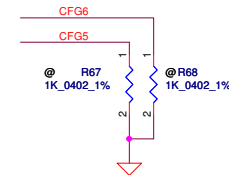
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



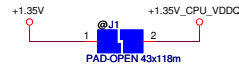
Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

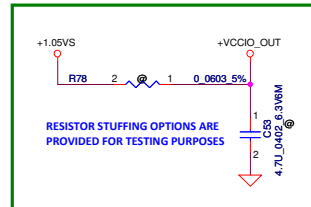
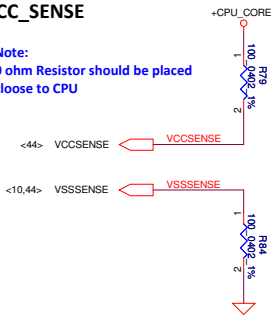
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

+1.35V_CPU_VDDQ Source

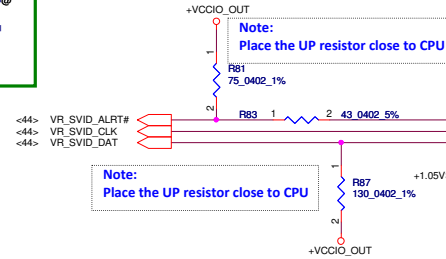


VCC_SENSE

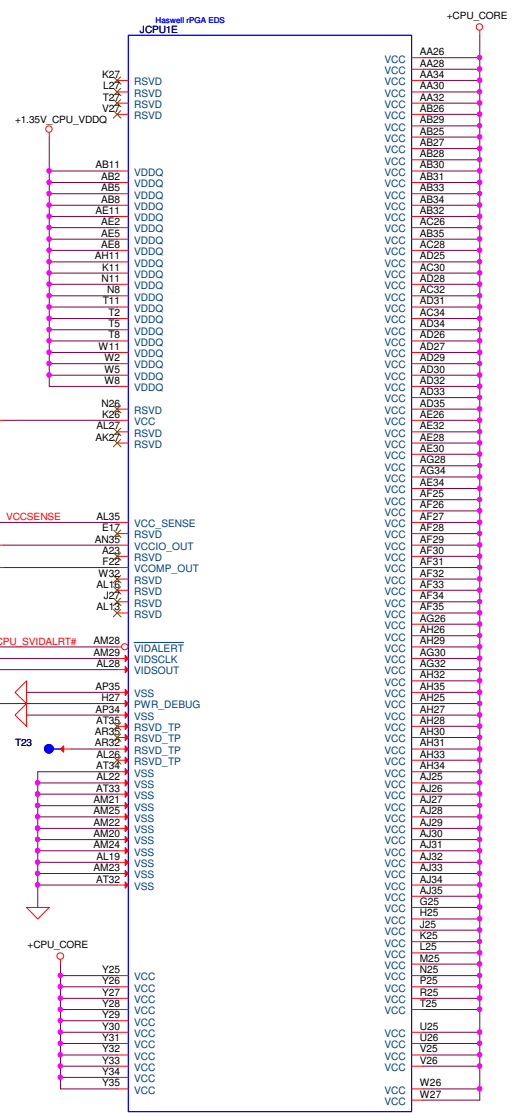
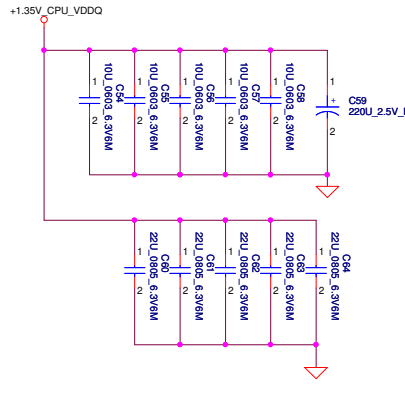
Note:
0 ohm Resistor should be placed close to CPU



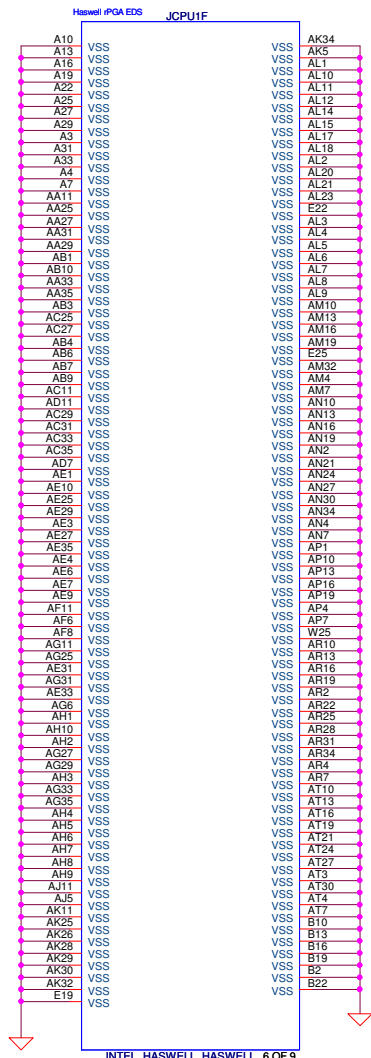
Note:
Place the UP resistor close to CPU



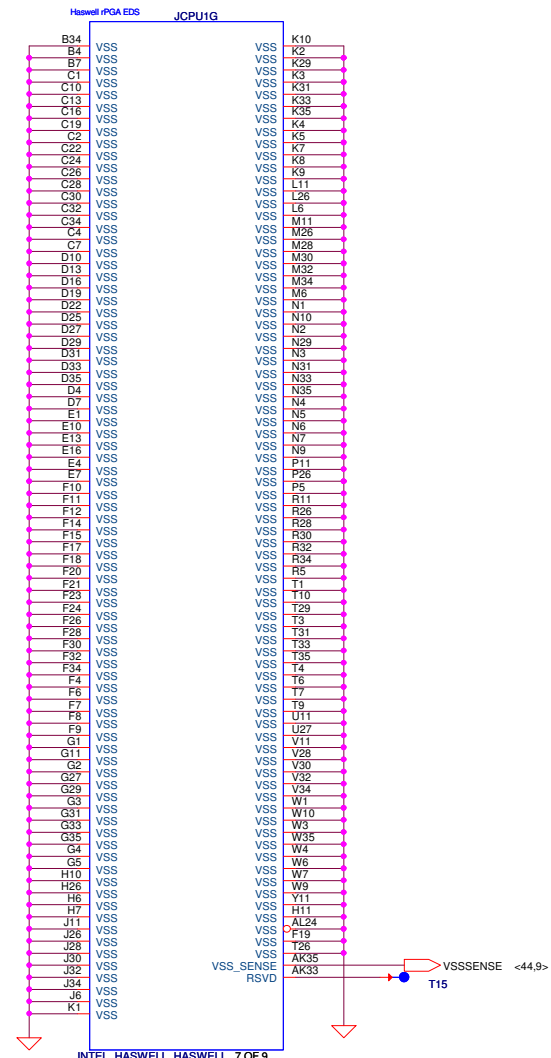
VDDQ DECOUPLING



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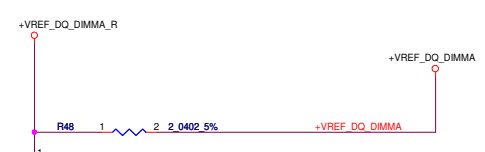
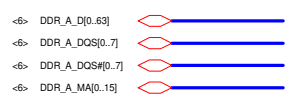
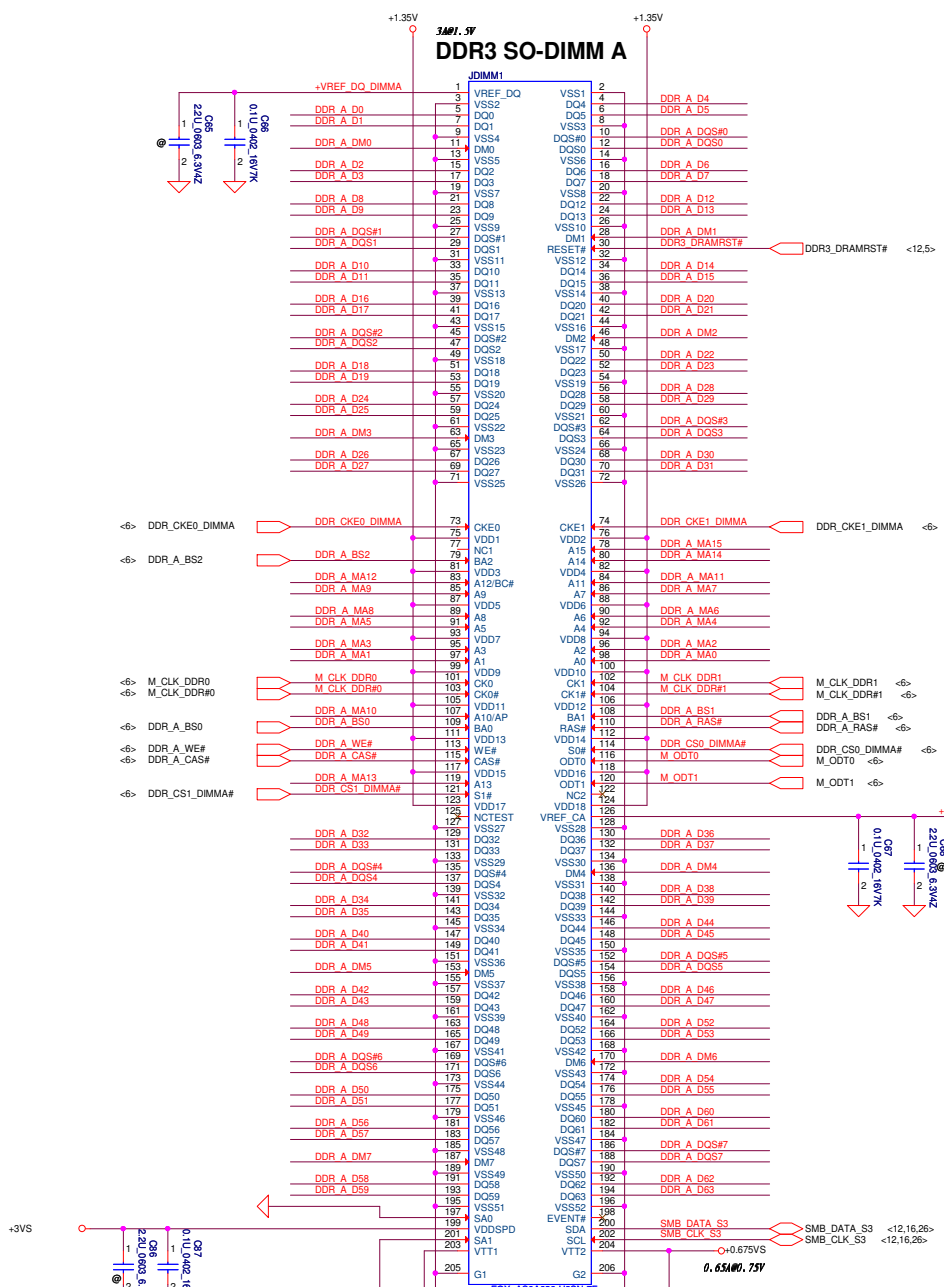
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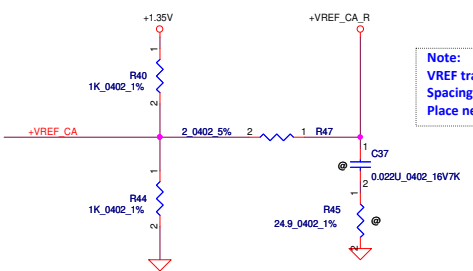
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Date: Friday, April 19, 2013				Sheet	10 of 49

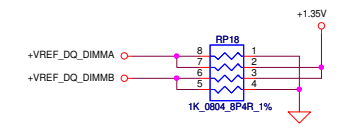
PROCESSOR(7/7) VSS
 Document Number
LA-9642P
 Date: Friday, April 19, 2013 | Sheet 10 of 49



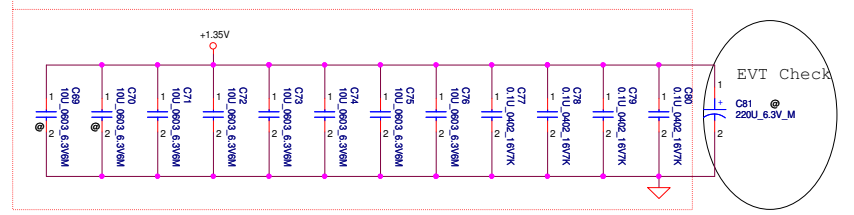
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket



Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

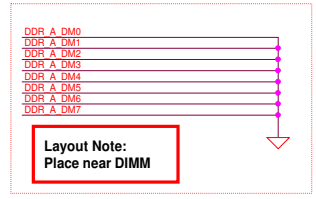
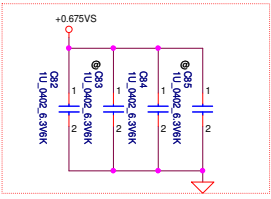


Layout Note:
Place near DIMM



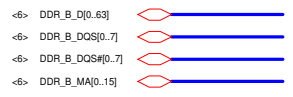
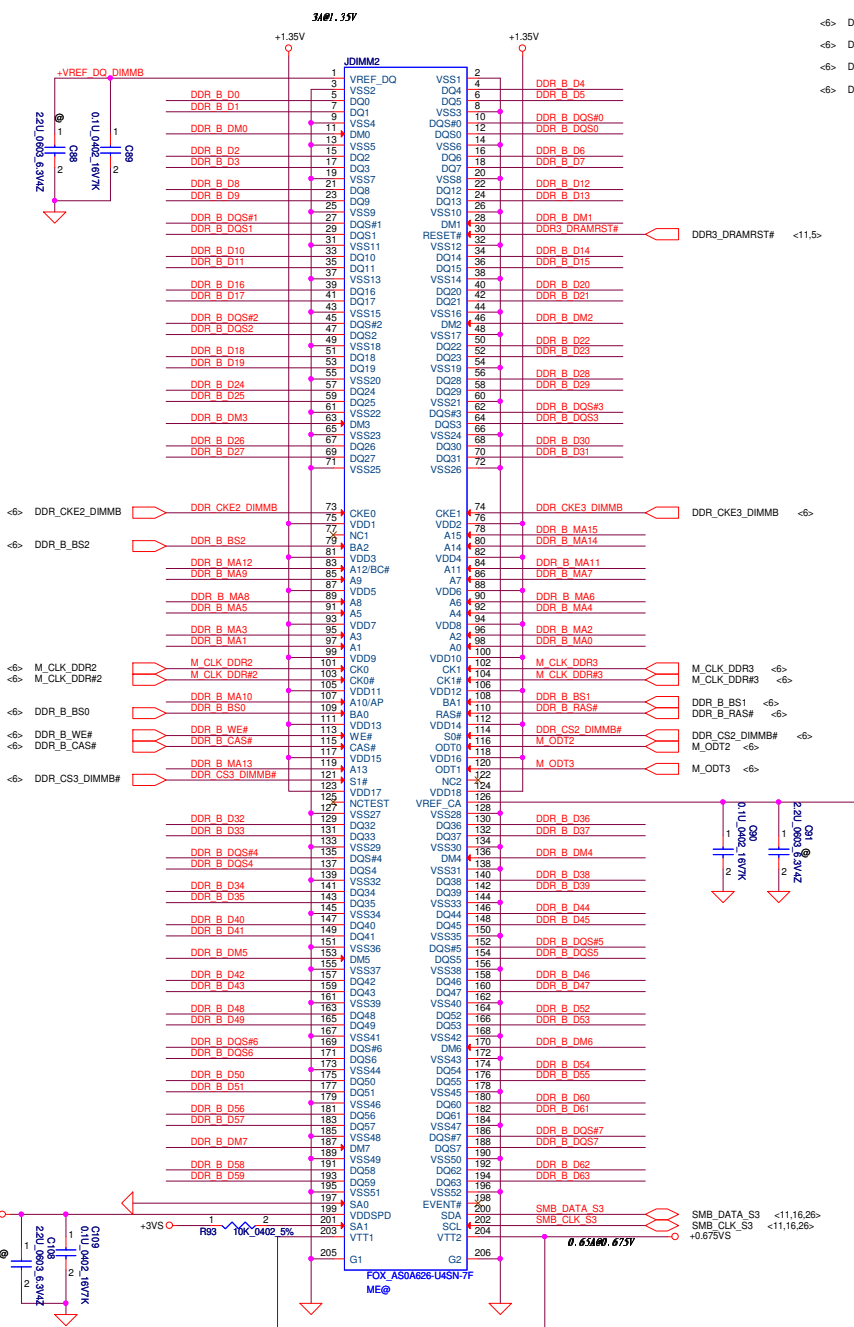
EVT Check
C81 220u_6.3V_M

Layout Note:
Place near DIMM

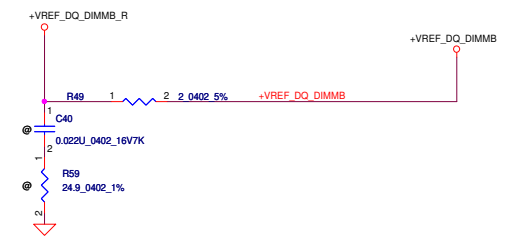


Layout Note:
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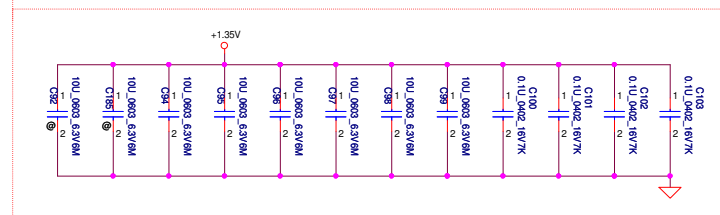
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Customer	Document Number	LA-9642P			
Date:	Friday, April 19, 2013	ISheet	11	of 49	



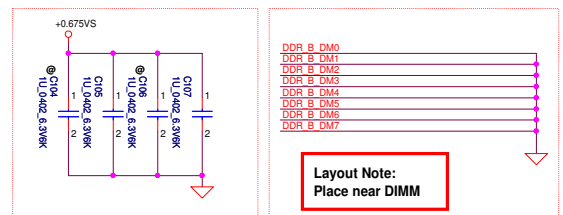
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes



Layout Note:
Place near DIMM

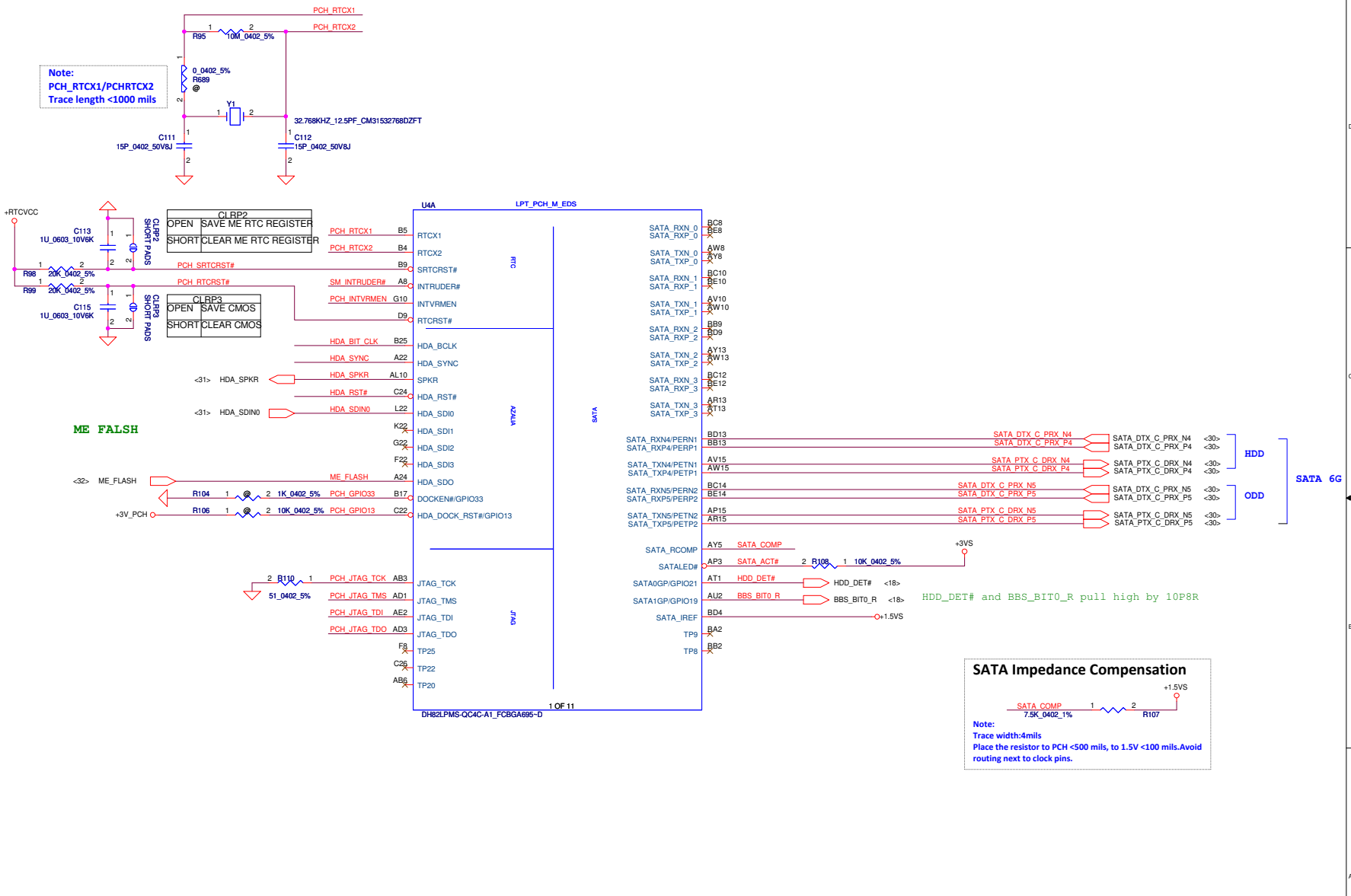
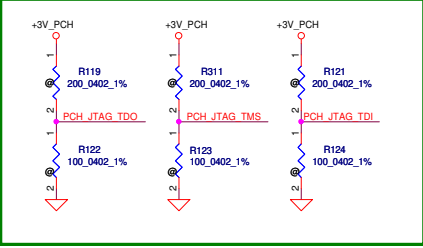
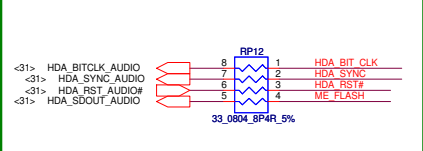
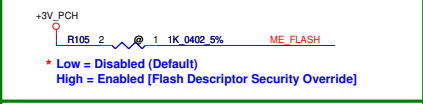
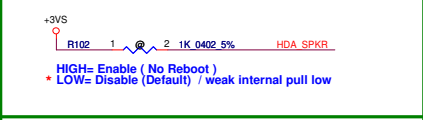
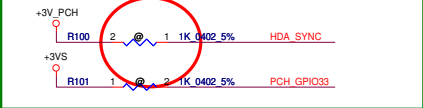
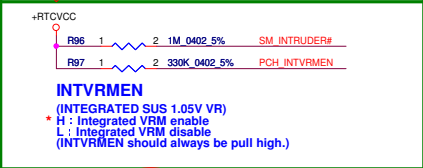
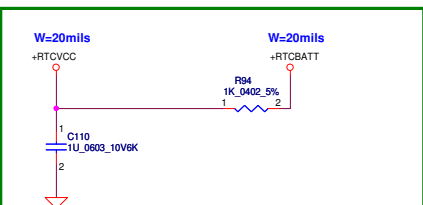


Layout Note:
Place near DIMM

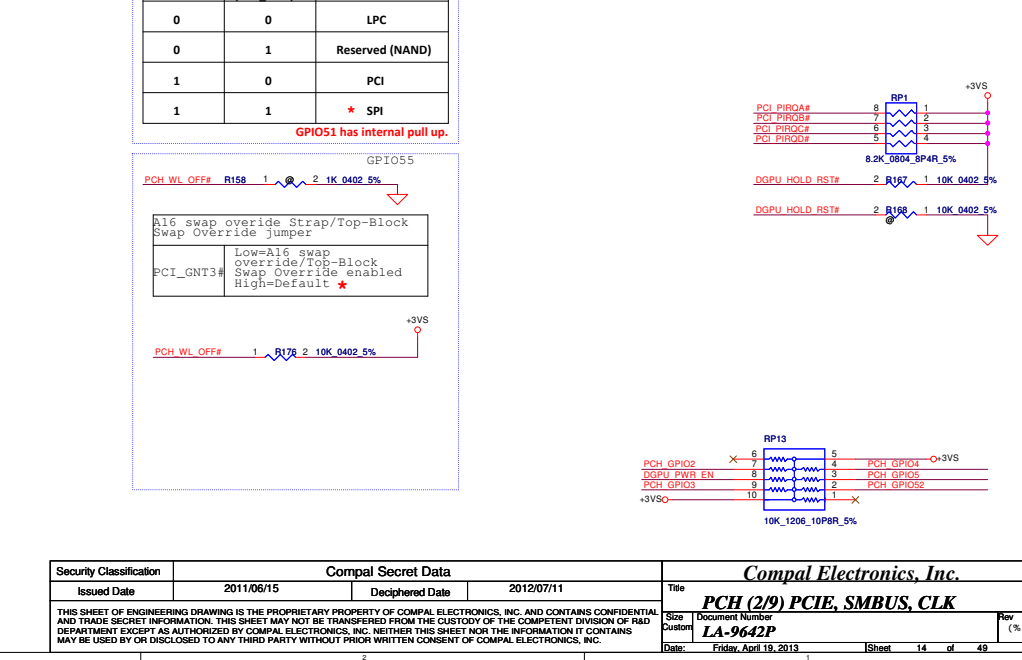
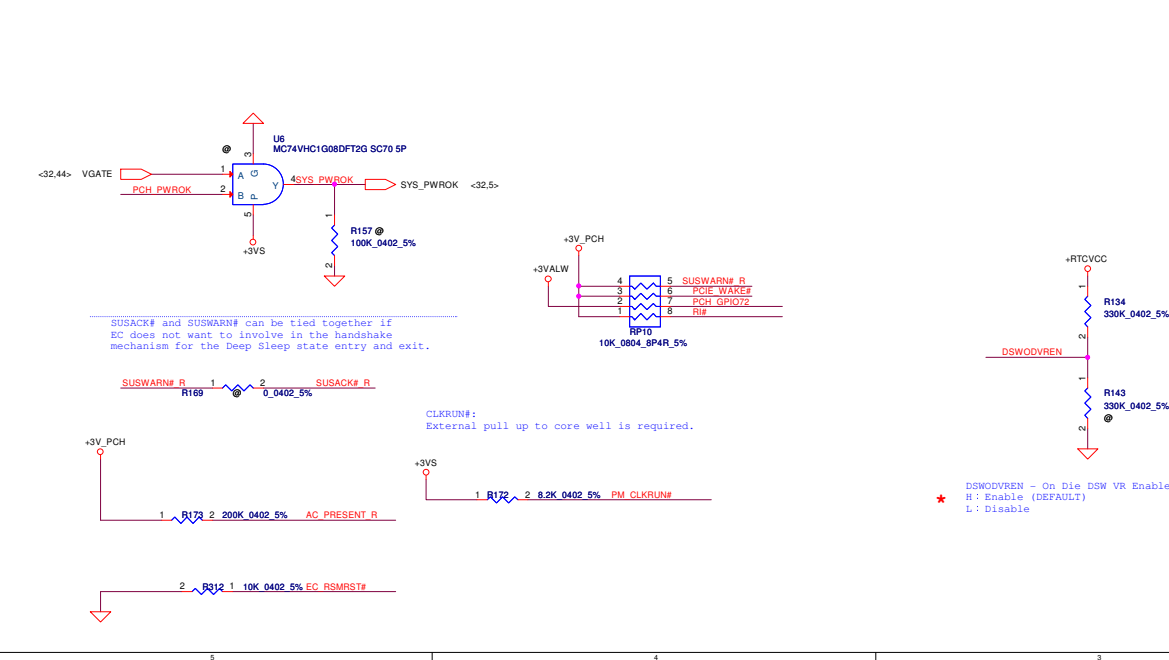
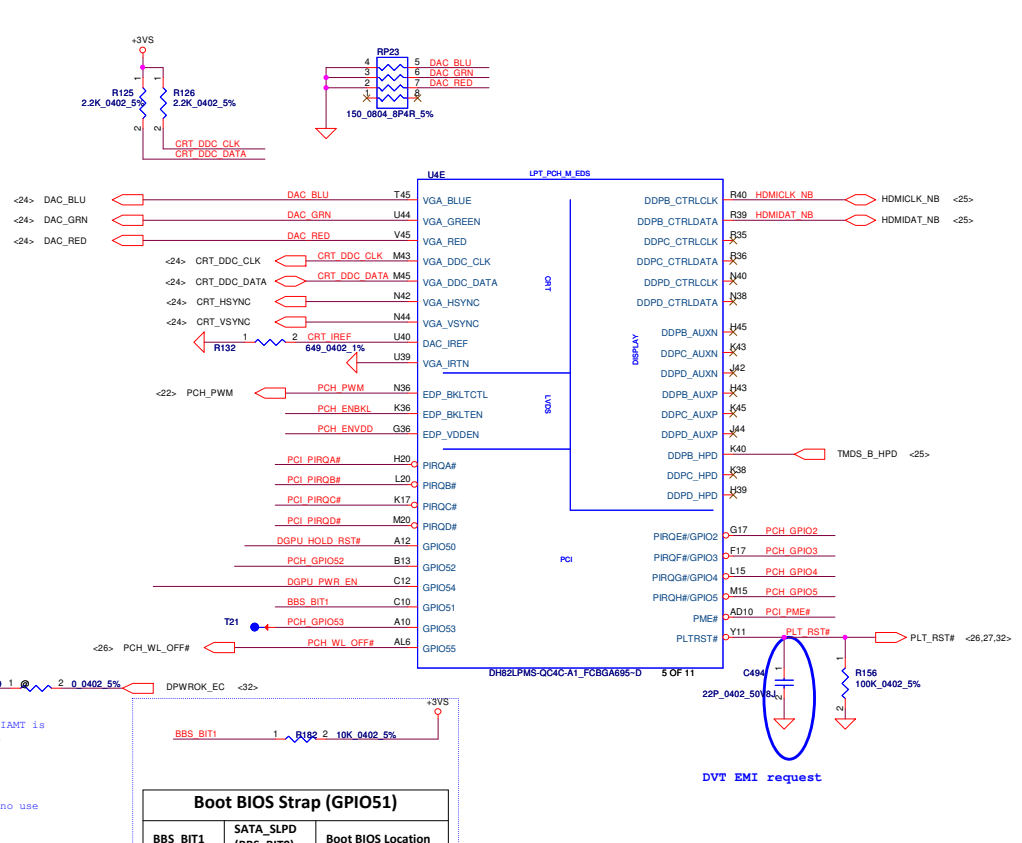
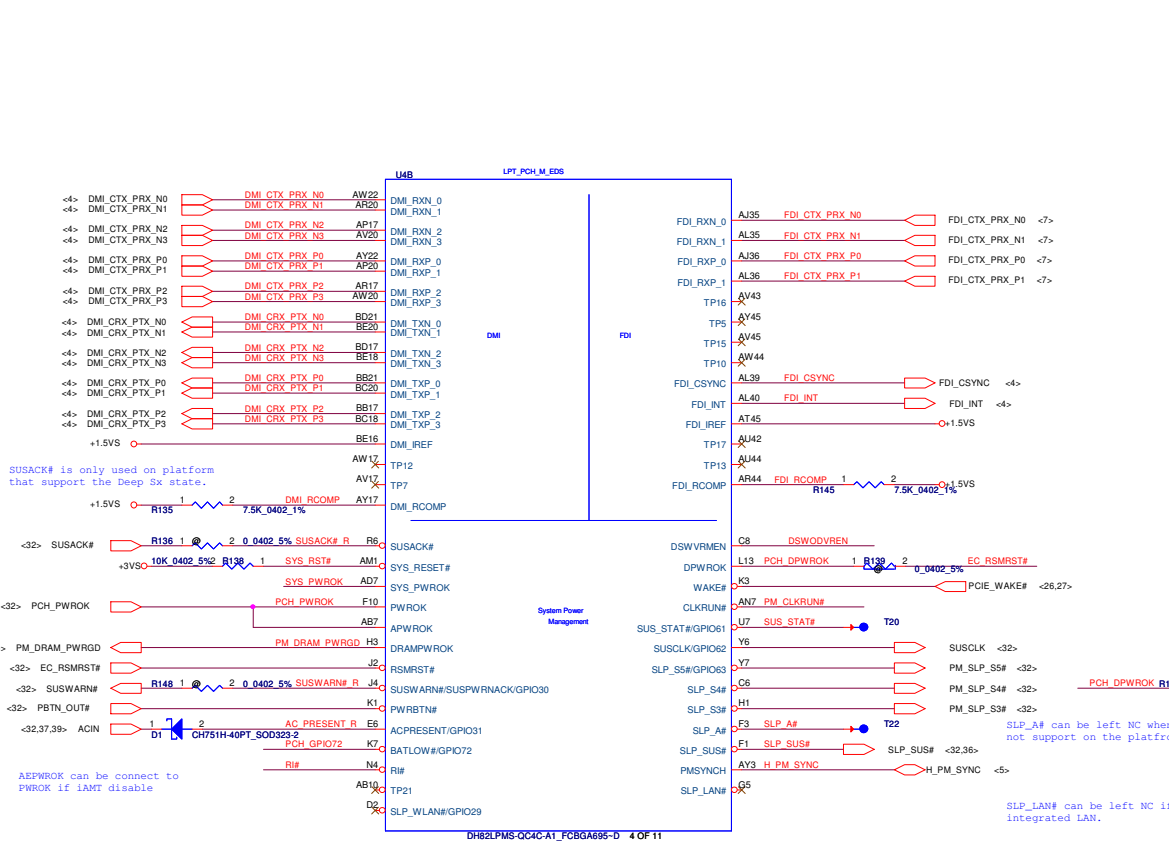


Layout Note:
Place near DIMM

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Issued Date	2011/06/15	Deciphered Date	
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (1/9) SATA, HDA, SPI, LPC, XDP
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Sheet 13 of 49				Rev (%)



Boot BIOS Strap (GPIO51)

BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	* SPI

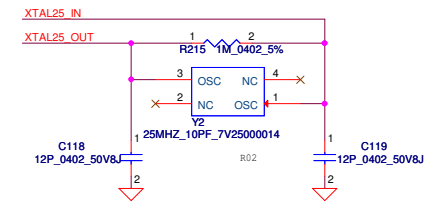
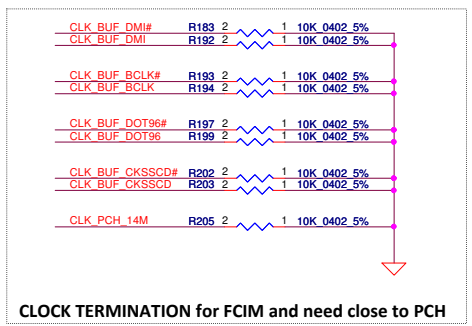
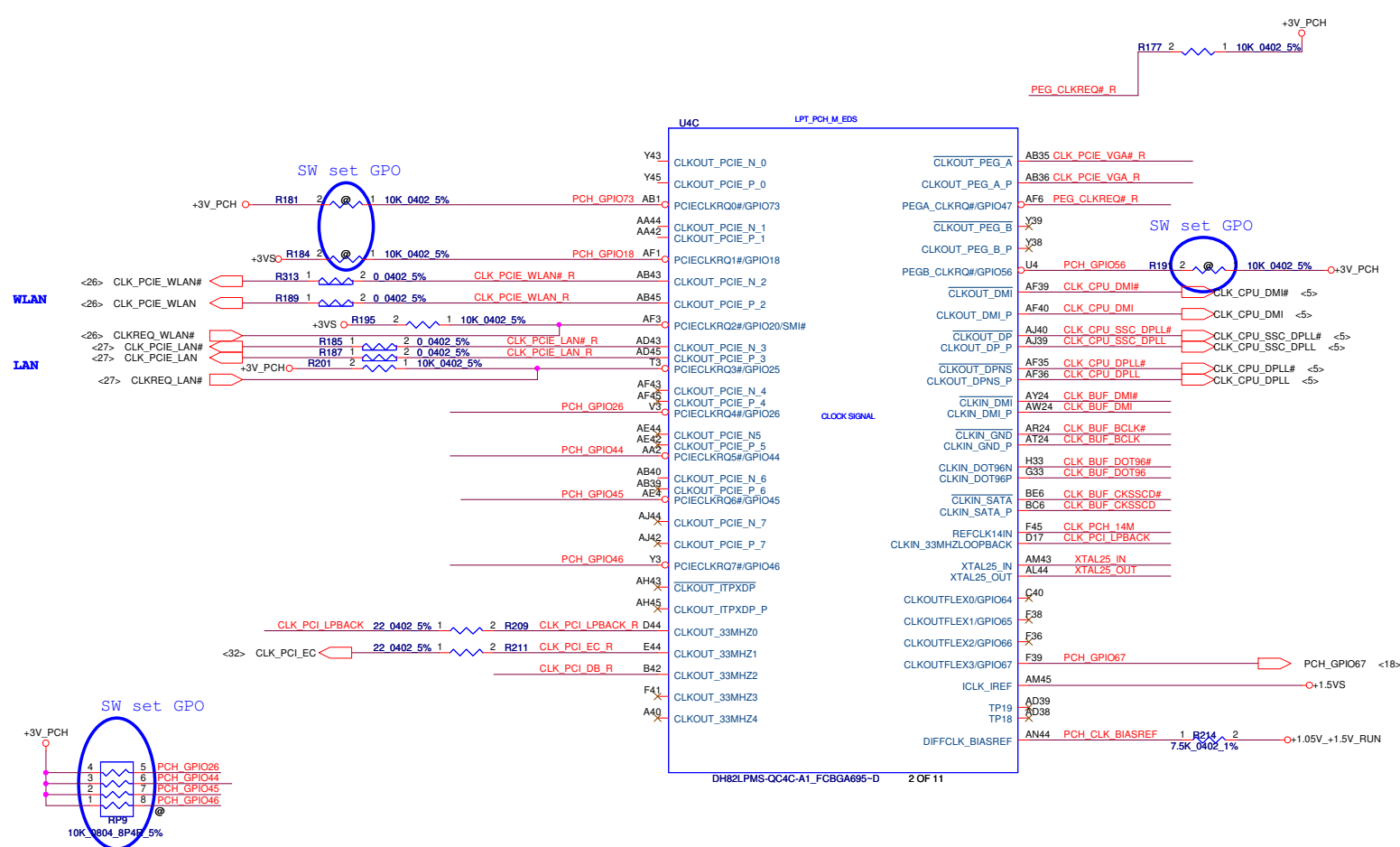
GPIO51 has internal pull up.

GPIO55

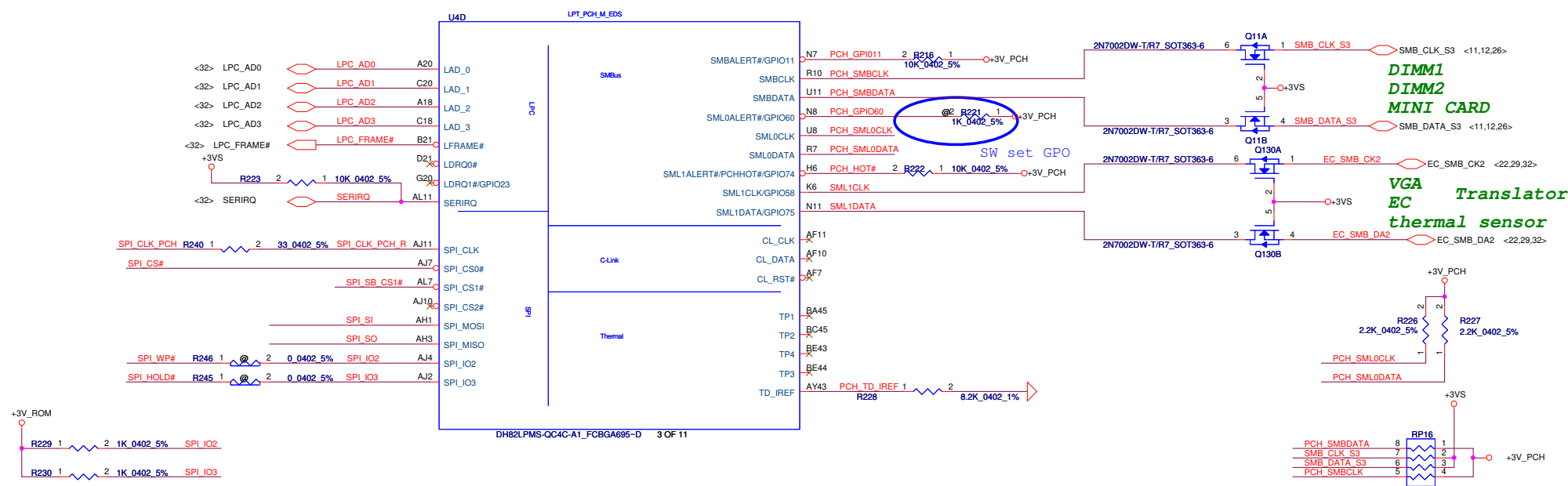
A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled
High=Default *

PCH_WL_OFF#	R158	1	2	1K 0402 5%
PCH_WL_OFF#	R178	2	10K 0402 5%	



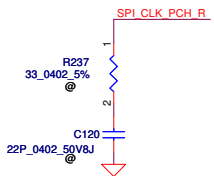
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (3/9) DMI,FDI,PM,	
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			LA-9642P	Rev (%)	
			Date: Friday, April 19, 2013	Sheet 15	of 49



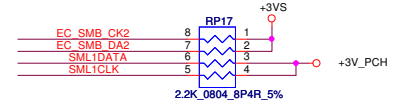
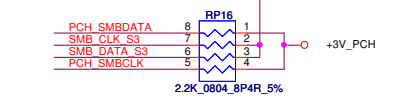
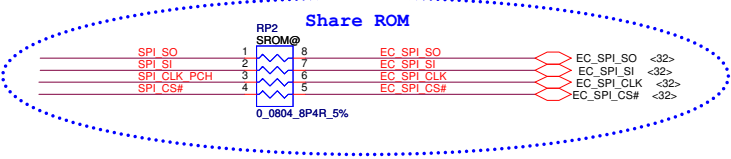
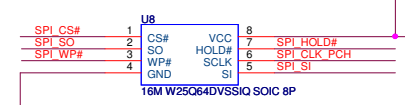
**DIMM1
DIMM2
MINI CARD**

**VGA
EC Translator
thermal sensor**

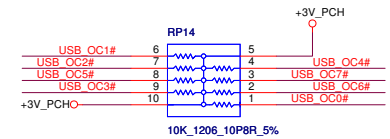
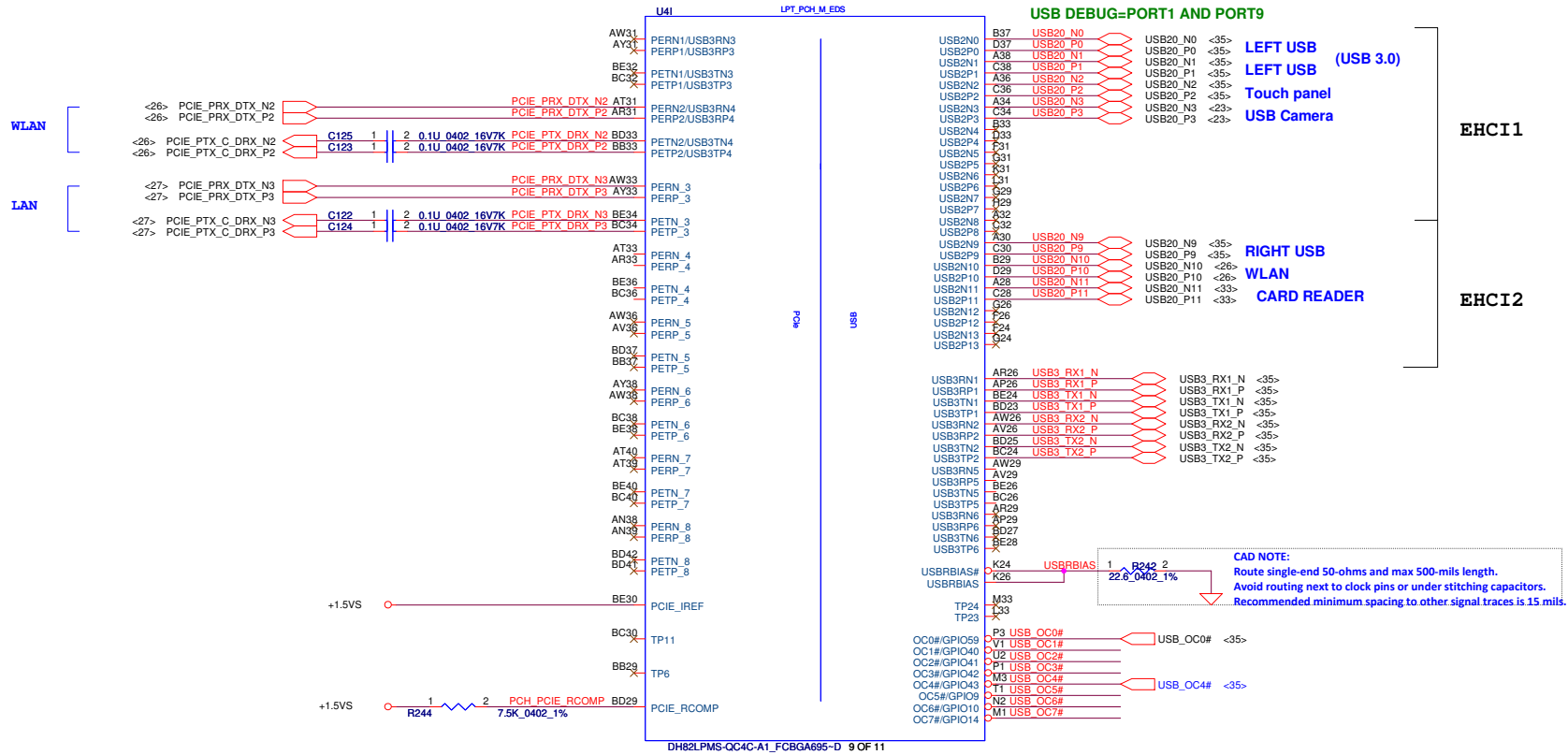
8MB SPI ROM FOR ME & Non-share ROM.



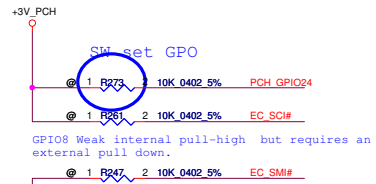
R124;c190 close to U4.T3 pin



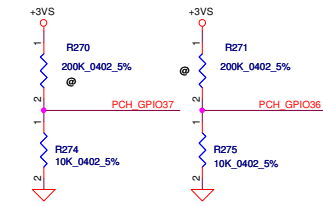
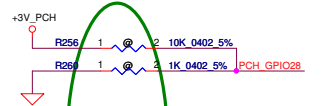
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Date: Friday, April 19, 2013				Sheet 16 of 49



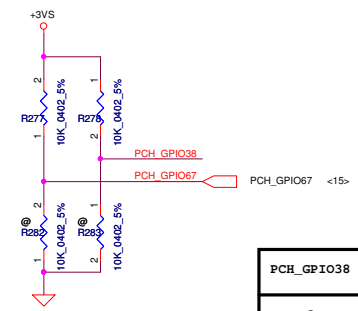
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				LA-9642P	
				Document Number	Sheet 17 of 49
				Friday, April 19, 2013	



Remove strap description inform SW set GPO

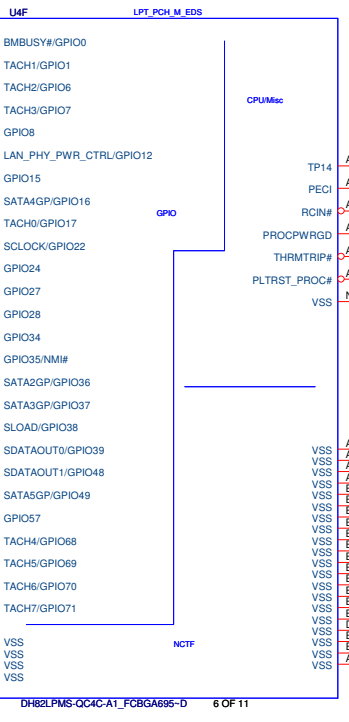
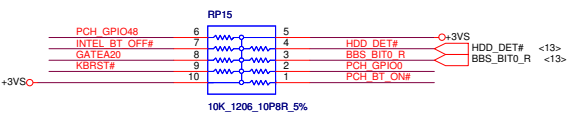
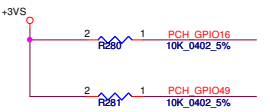
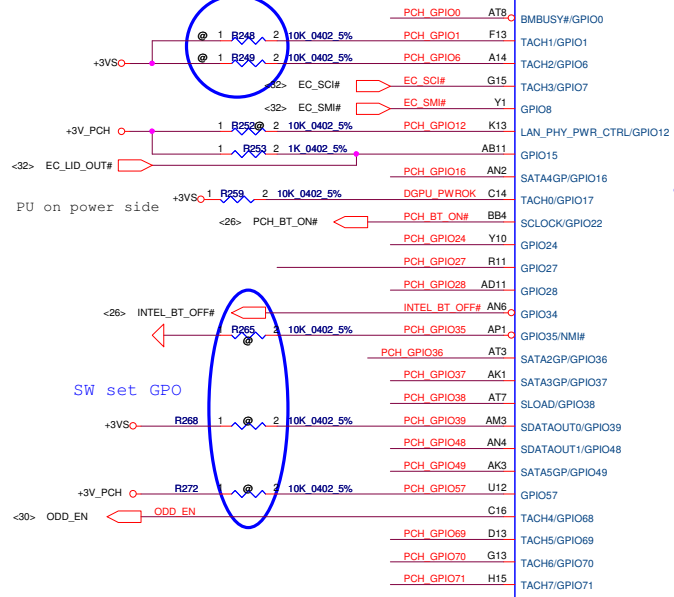


BIOS Request SKU ID

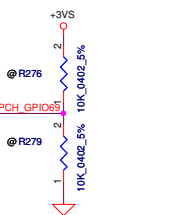


PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	DIS
1	1	UMA

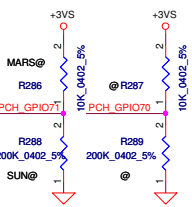
SW set GPO



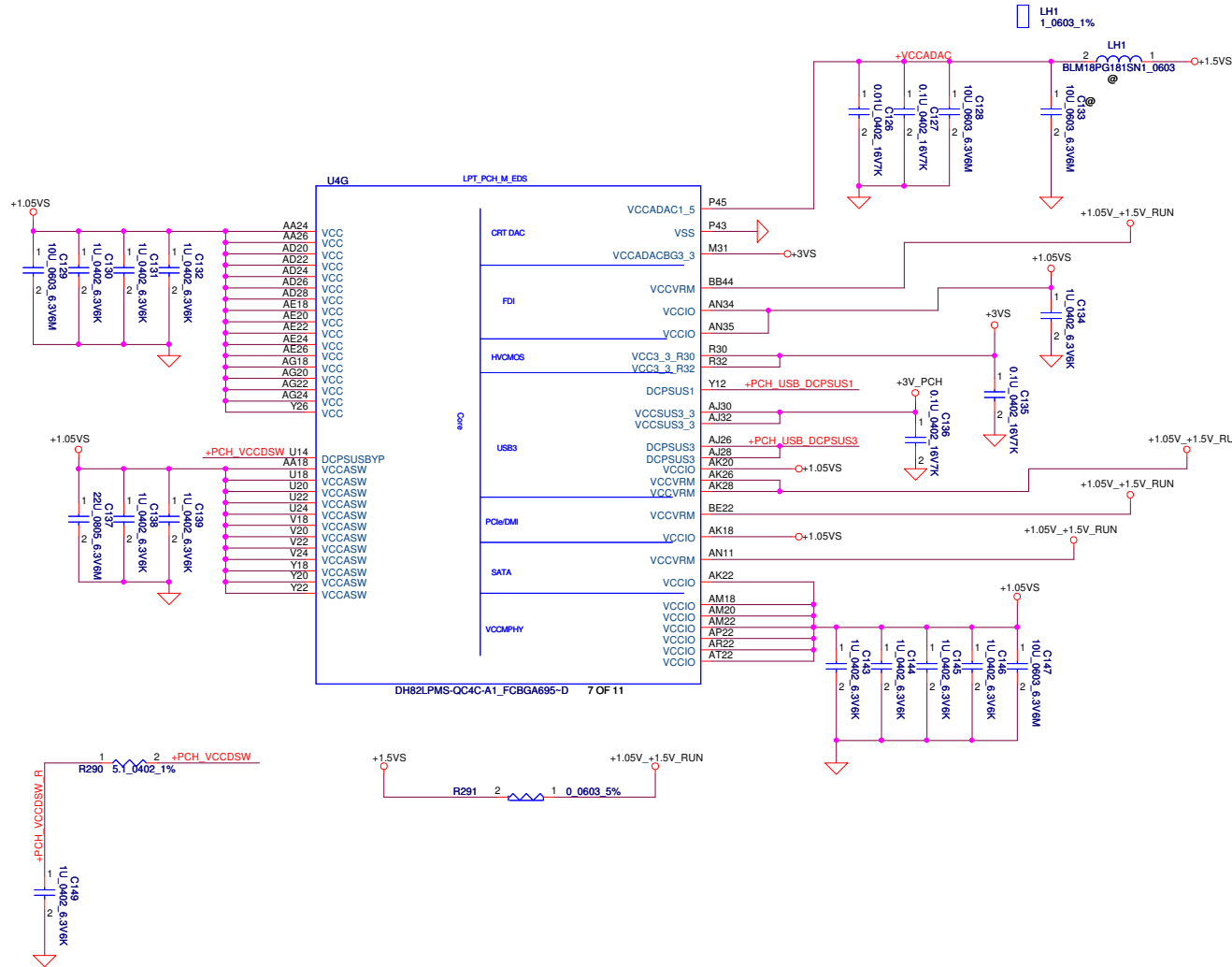
PCH_GPIO69	Function
0	
1	



PCH_GPIO70	Function
0	
1	
PCH_GPIO71	Function
0	SUN PRO
1	Mars XT

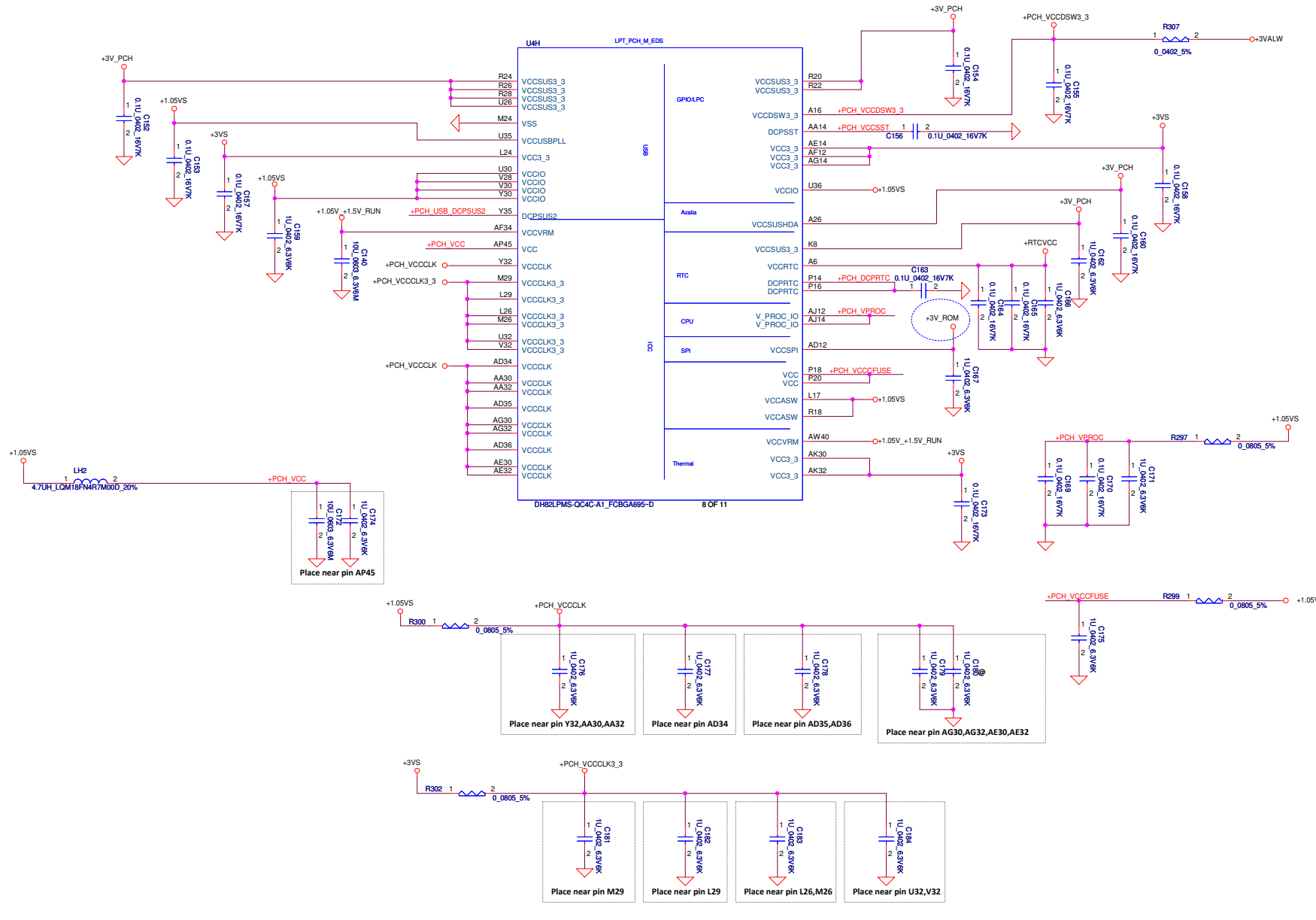


Need Update



PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Date:	Friday, April 19, 2013	Sheet	19	of 49



PCH Power Rail Table

Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROG_IO	1.05V	0.004 A

Place near pin AP45

Place near pin Y32,AA30,AA32

Place near pin AD34

Place near pin AD35,AD36

Place near pin AG30,AG32,AE30,AE32

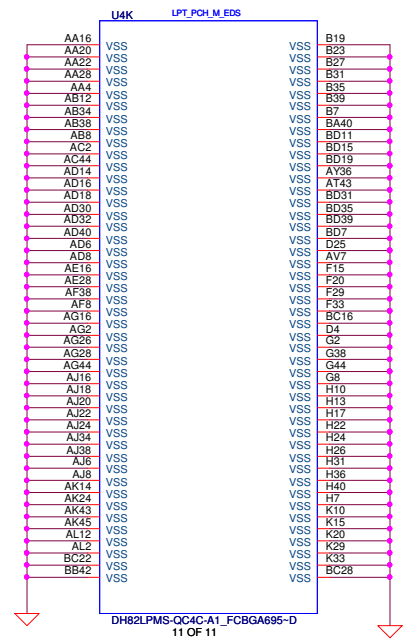
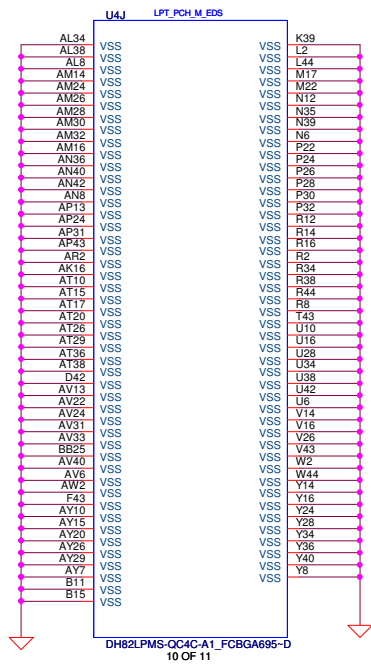
Place near pin M29

Place near pin L29

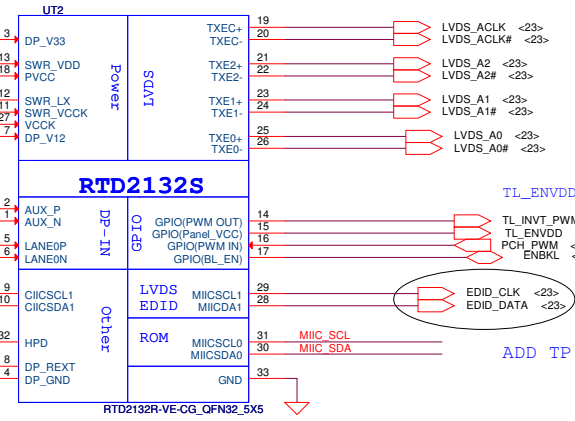
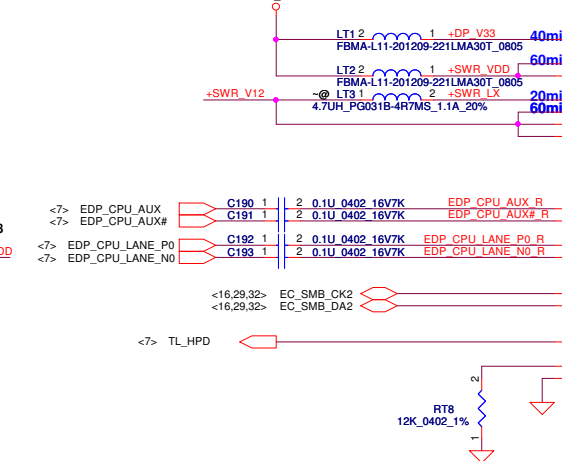
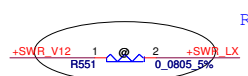
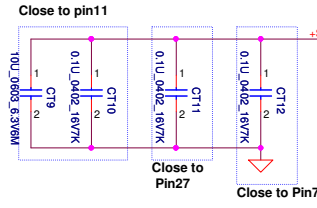
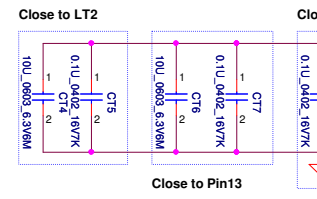
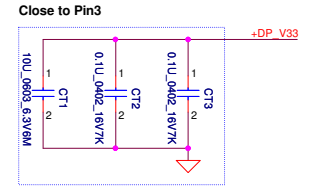
Place near pin L26,M26

Place near pin U32,V32

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Customer	LA-9642P	Date	Friday, April 19, 2013	Sheet	20 of 49

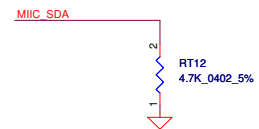
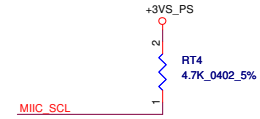
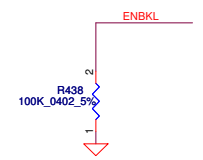
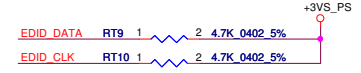


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				LA-9642P	(%)
				Date: Friday, April 19, 2013	Sheet 21 of 49



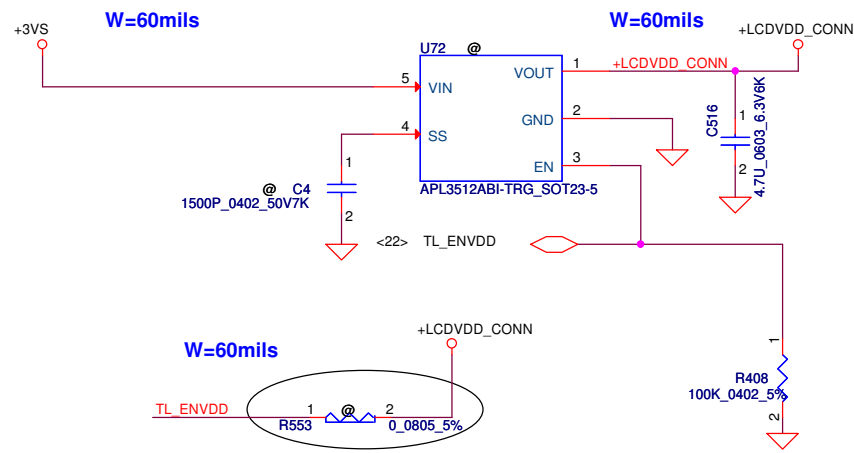
TL_ENVDD need 60 mil if use for LVDS power on R version

ADD TP on trace or via

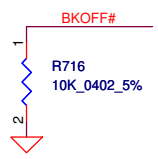


	MIIC_SDA	0	1
MIIC_SCL		X	EC CODE
		1	Internal ROM

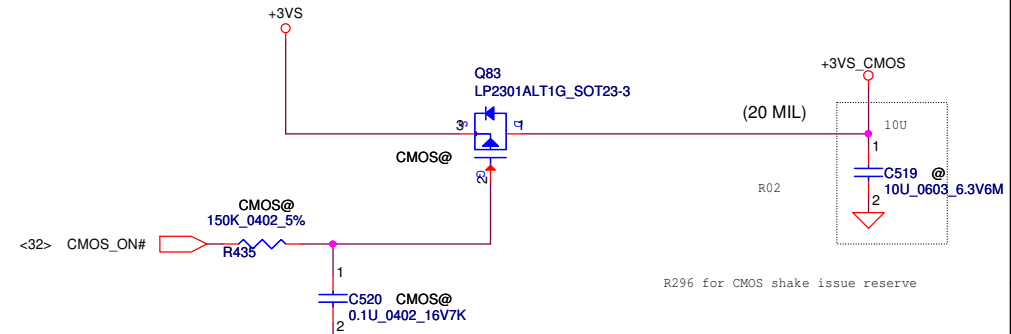
LCD POWER CIRCUIT



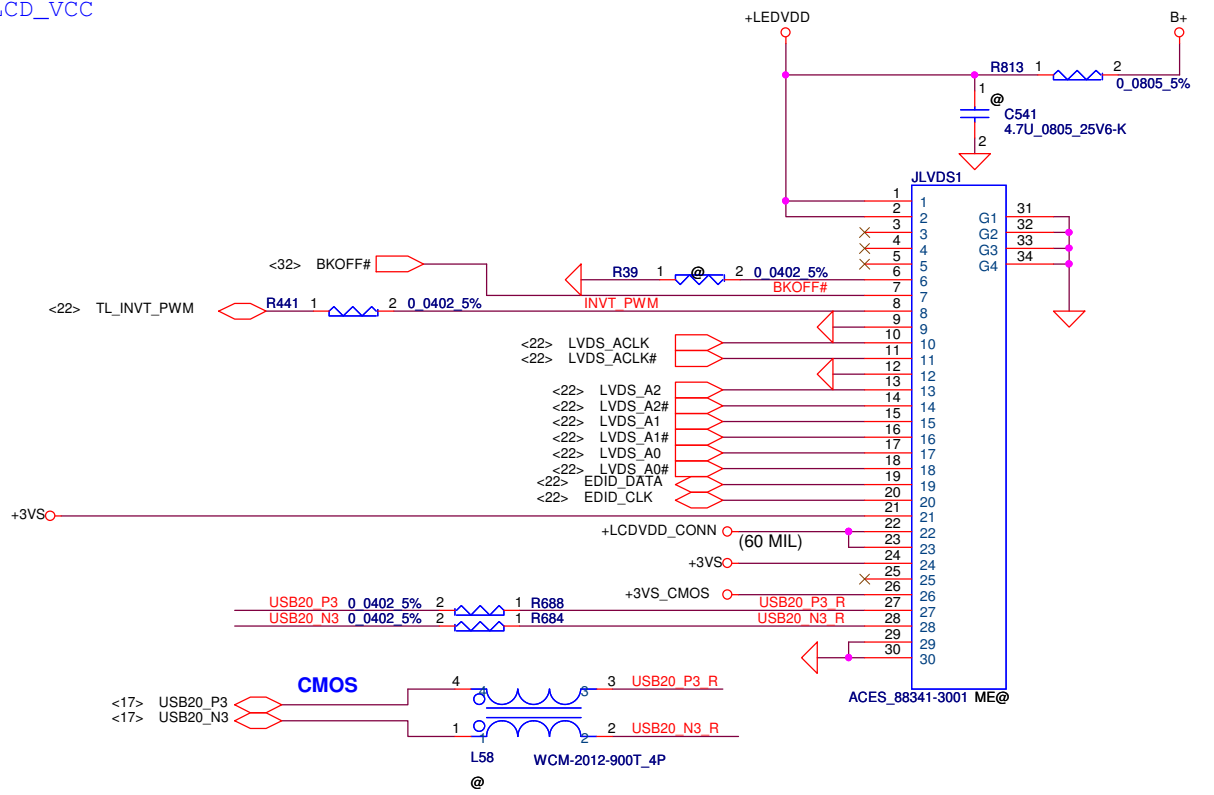
RTD2132R Internal load switch for +LCD_VCC



CMOS Camera

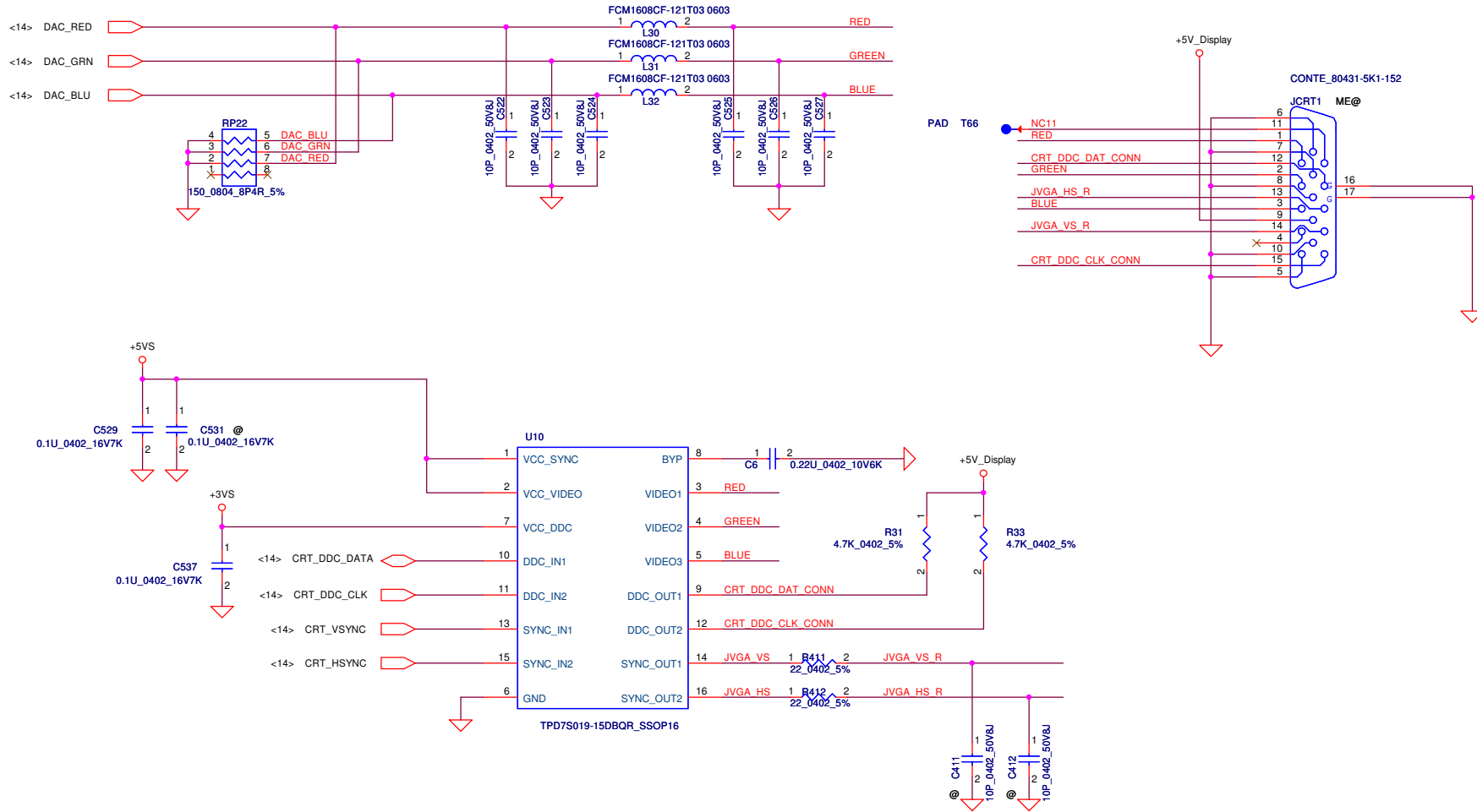


VGA LCD/PANEL BD. Conn.

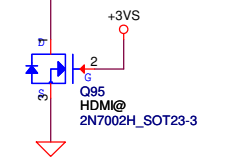
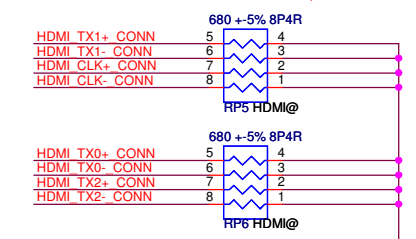
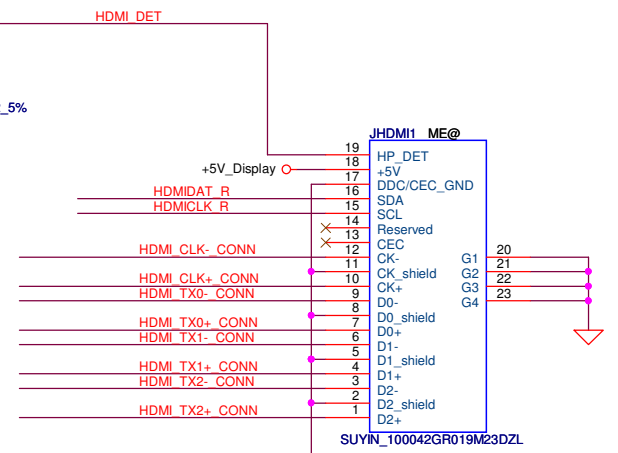
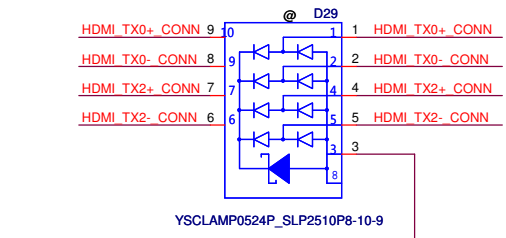
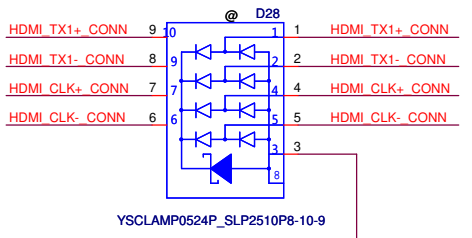
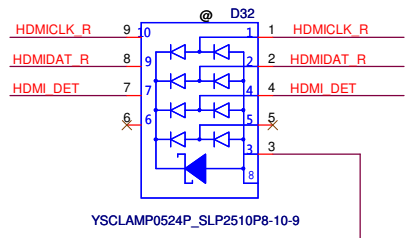
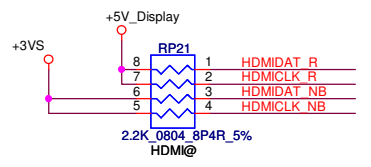
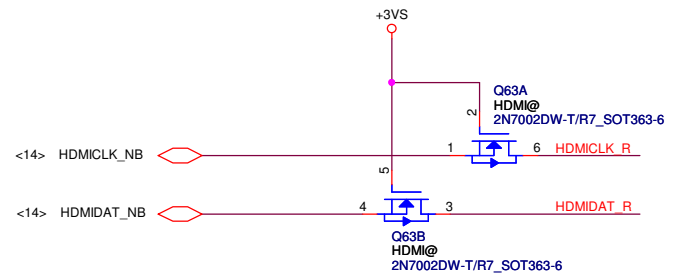
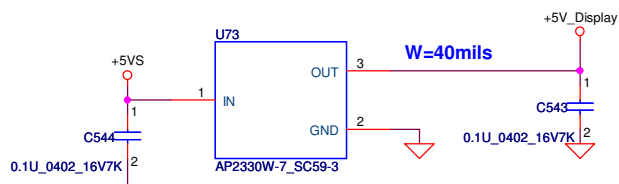
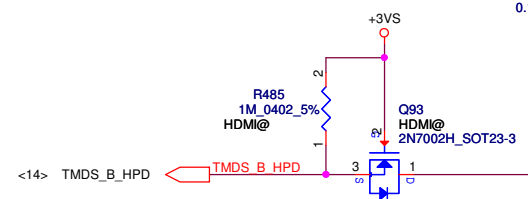
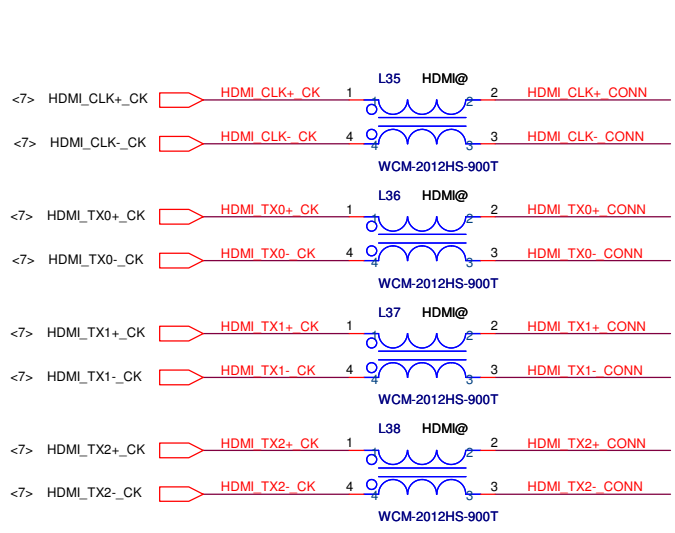


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				LA-9642P
Date: Friday, April 19, 2013				Sheet 23 of 49

CRT Connector

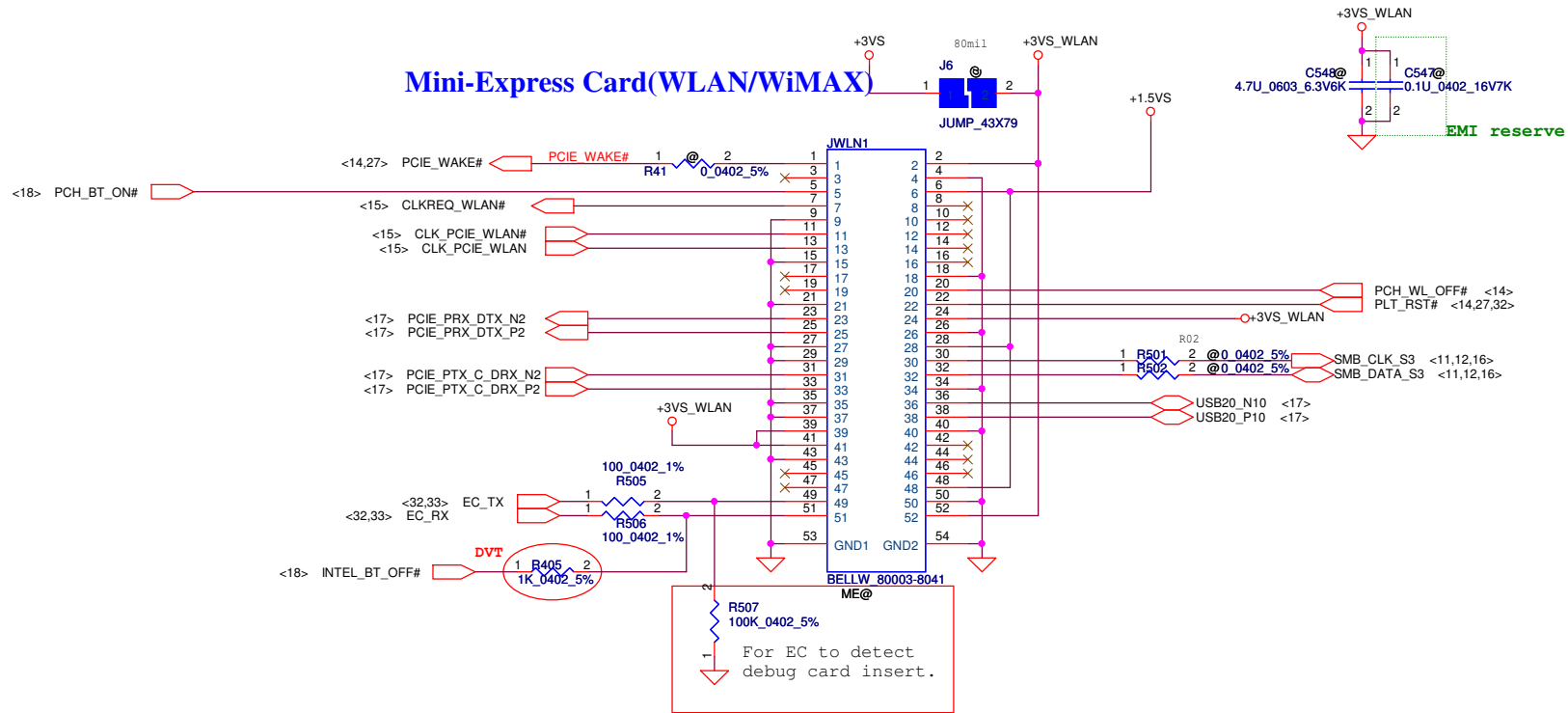


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Size	Custom	Document Number	LA-9642P	Rev	(%)
Date:	Friday, April 19, 2013	Sheet	24	of	49

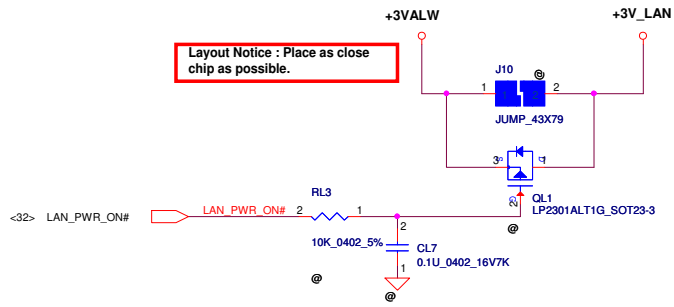


Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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				Size	Document Number
				LA-9642P	
				Date: Friday, April 19, 2013	Sheet 25 of 49

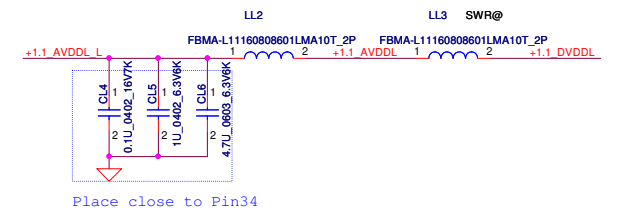
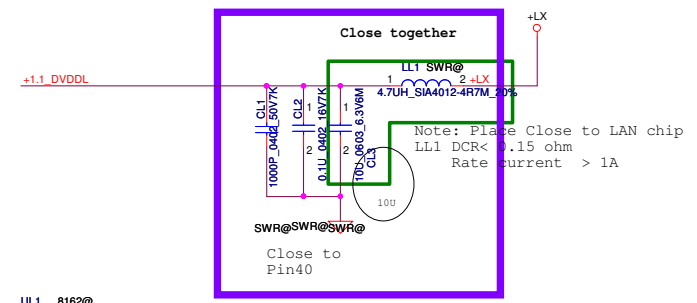
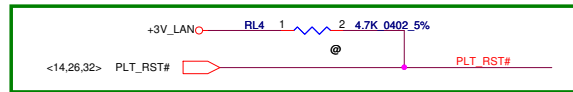
Mini-Express Card for WLAN/WiMAX(Half)



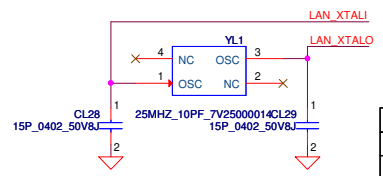
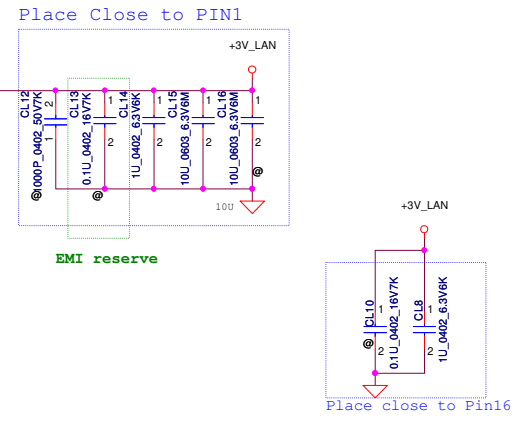
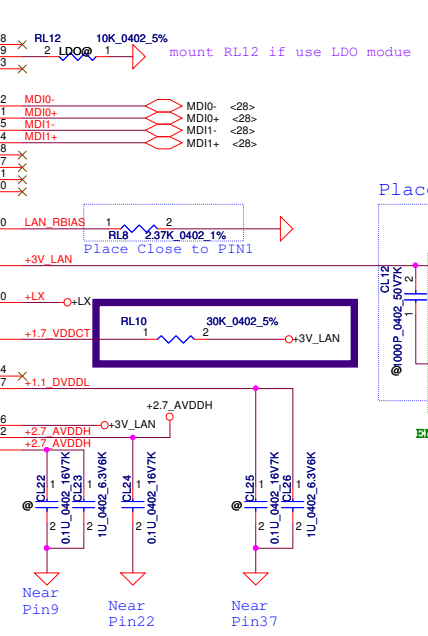
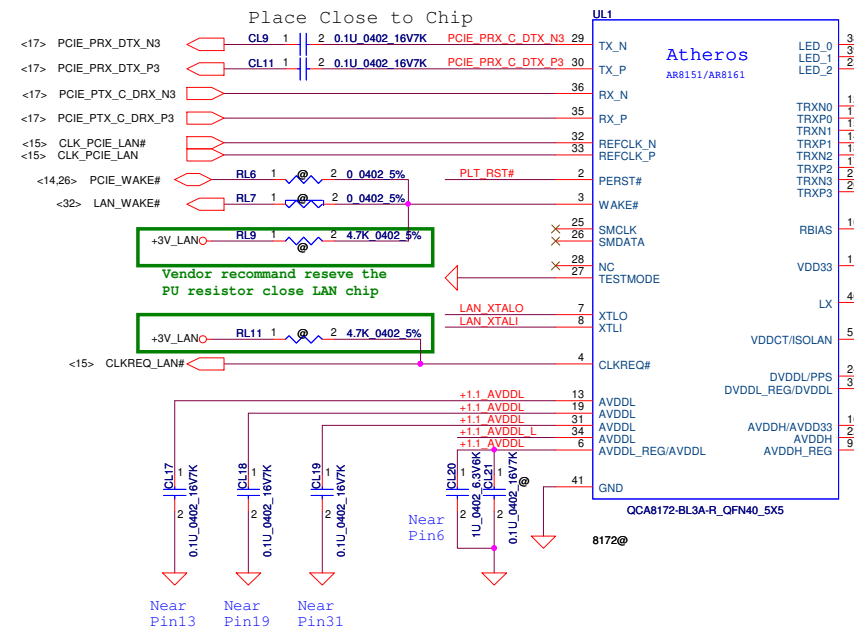
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title Mini-Card/NEW Card/SIM	
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				Date	Friday, April 19, 2013



Vendor recommend reseve the PU resistor close LAN chip



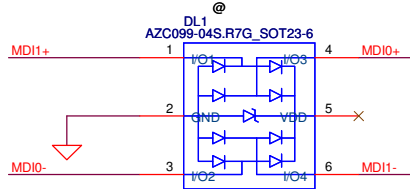
UL1 8162@
AR8162-AL3A-R
SA000065410 S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL
SA000052J10 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL



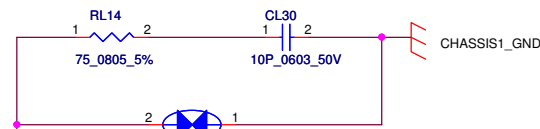
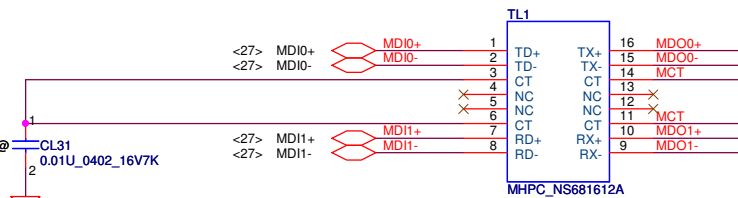
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
				LAN-AR8162/8172	
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Size	Document Number	Date	Friday, April 19, 2013	Sheet	27 of 49
Rev	LA-9642P				(%)

DL1
 1'S PN:SC300001G00
 2'S PN:SC300002E00

Place Close to TL1



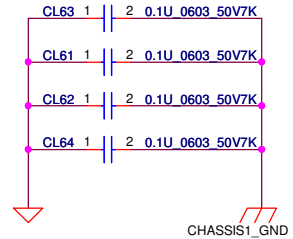
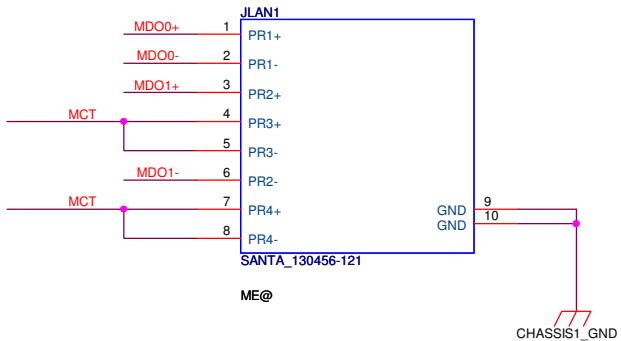
Reserve gas tube for EMI go rural solution



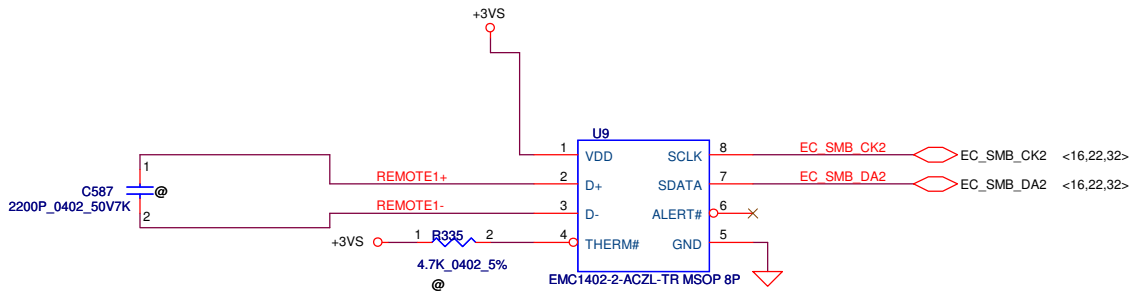
Place Close to TL1

DL11
 BS4200N-C-LV_SMB-F2
 GAS@

Need check Symbol

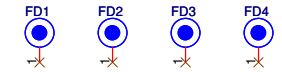
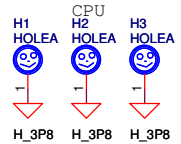


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title LAN_Transformer	
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				Date: Friday, April 19, 2013	Sheet 28 of 49

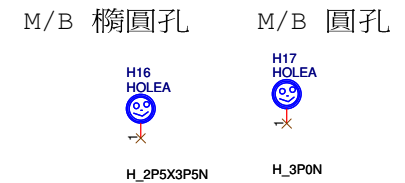
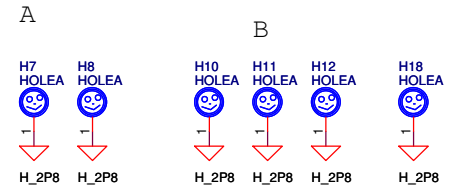
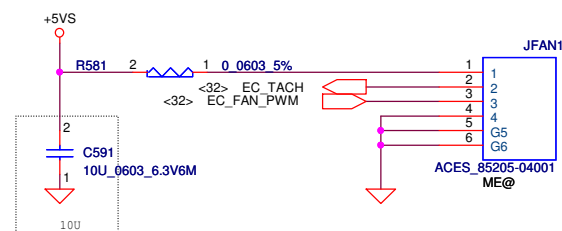


EMC1412-A (SA00003YA00)
 Address 1111_100xb
 S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1, 2+/-:
 Trace width/space: 10/10 mil
 Trace length: <8"



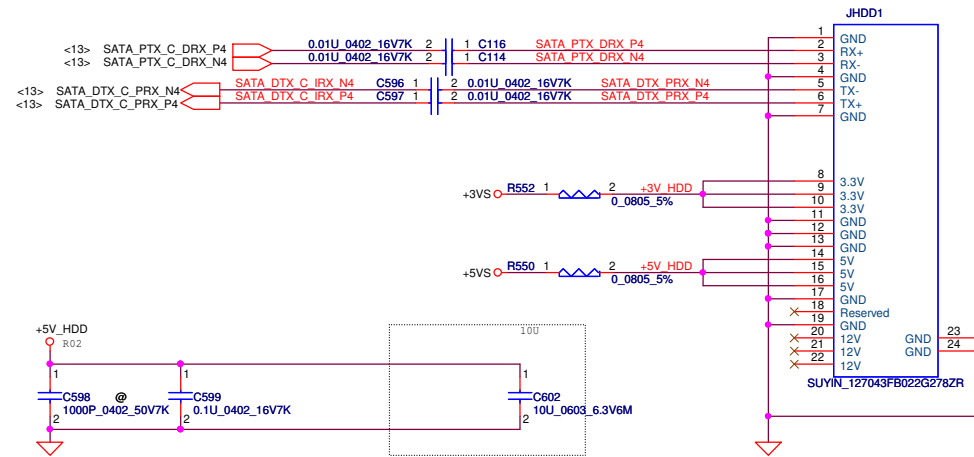
FAN1 Conn



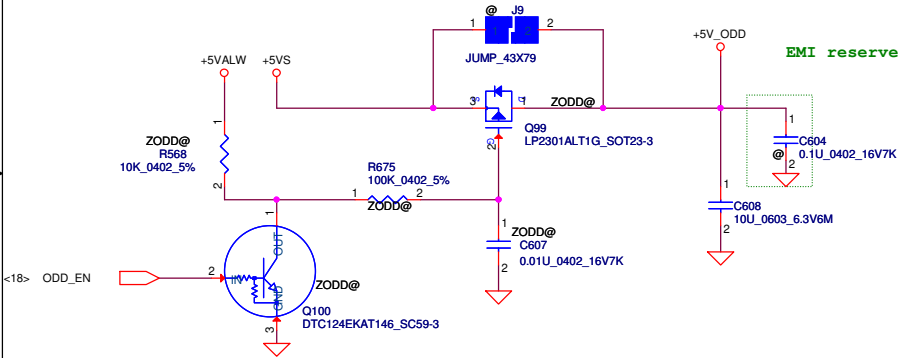
2P8 * 7 pcd

Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Fintek-Thermal IC/FAN/screw
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				Date:	Friday, April 19, 2013
				Sheet	29 of 49

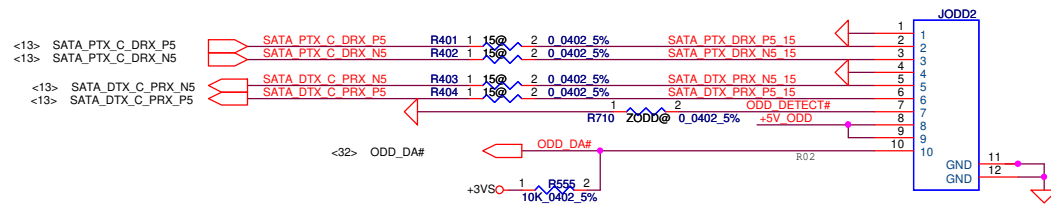
SATA HDD Conn.



ODD Power Control

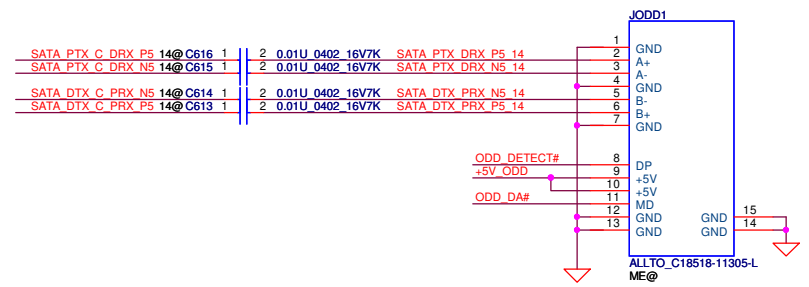


FOR 15" SATA ODD FFC Conn.



Co-lay

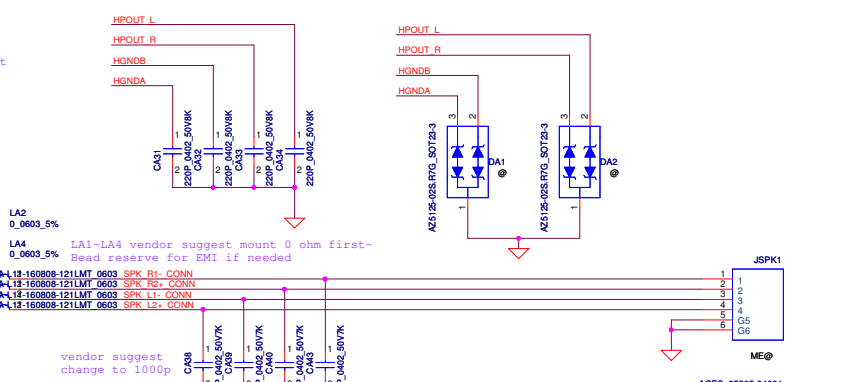
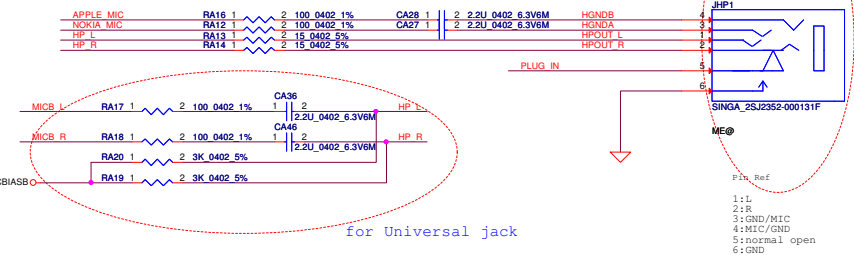
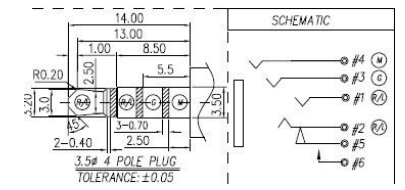
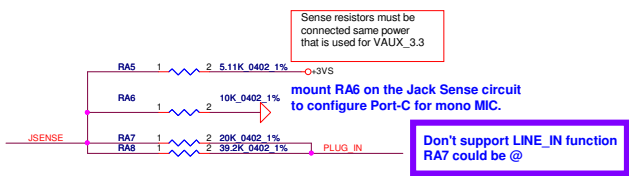
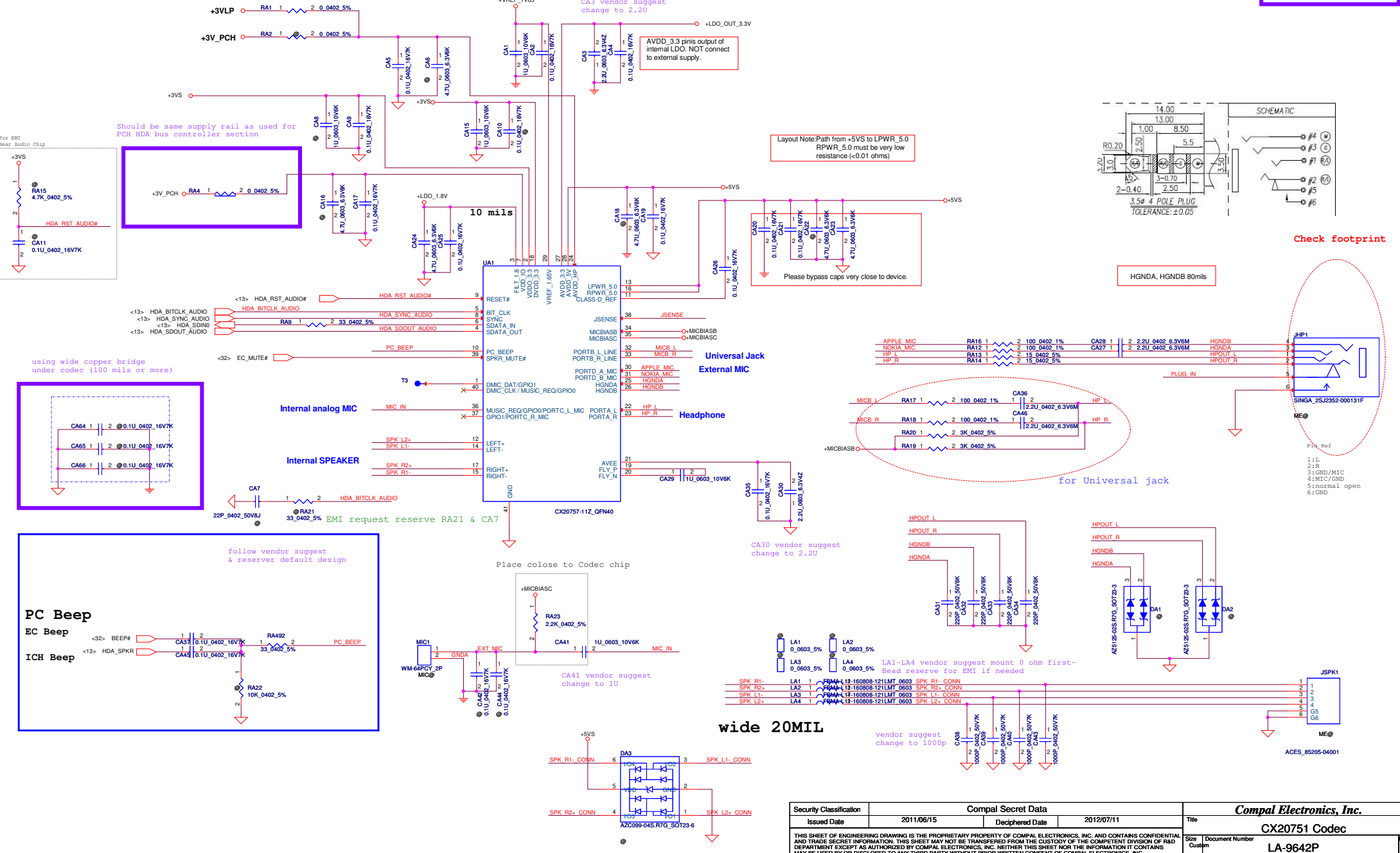
FOR 14" SATA ODD Conn.



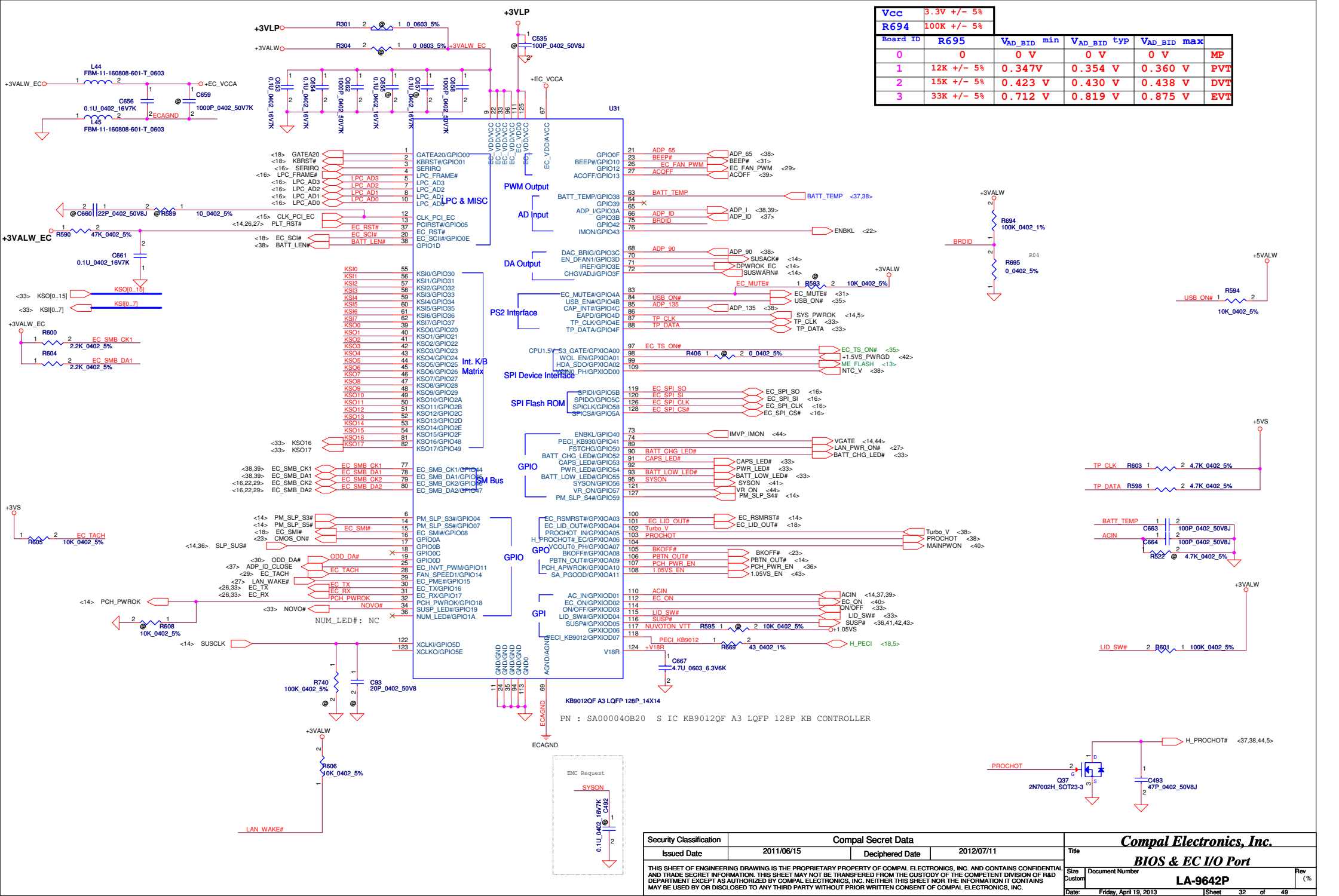
Security Classification	Compal Secret Data	
Issued Date	2011/06/15	Deciphered Date
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Compal Electronics, Inc.	
HDD/ODD/BT Connector	
Title	
Size	Document Number
Custom	LA-9642P
Date:	Friday, April 19, 2013
Sheet	30 of 49

CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).



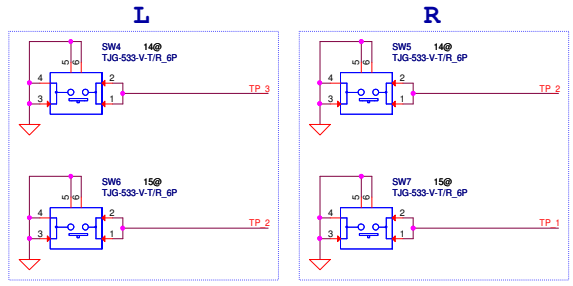
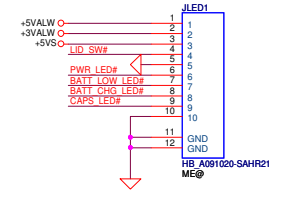
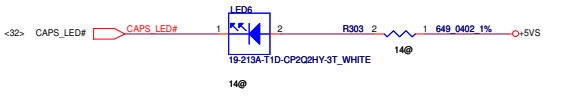
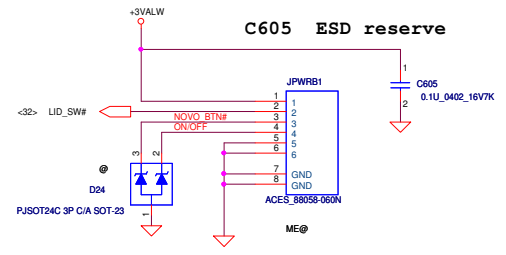
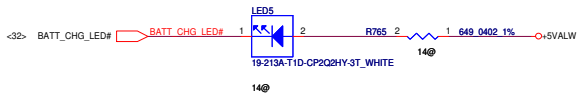
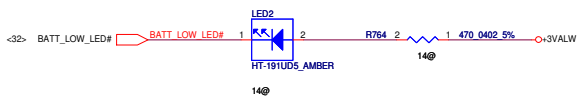
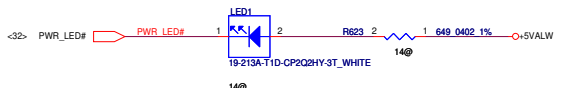
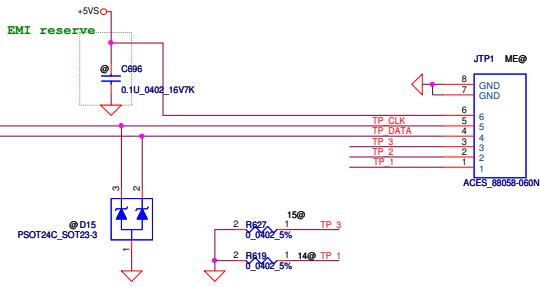
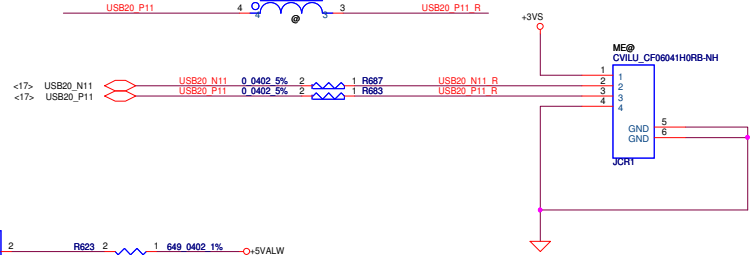
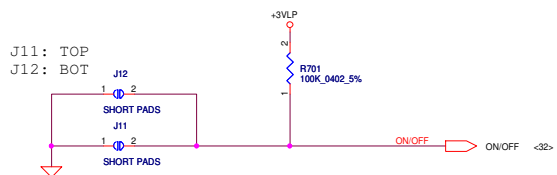
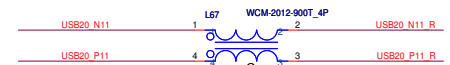
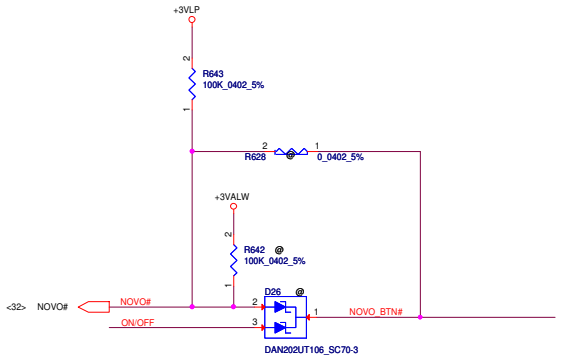
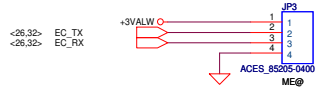
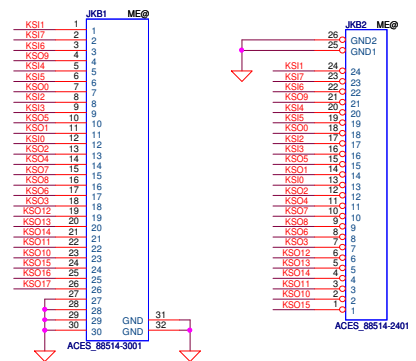
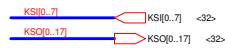
Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	CX20751 Codec
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Size	Document Number	Rev	%	
Custom	LA-9642P			
Date:	Friday, April 19, 2013	Sheet	31	of 49



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Issued Date	2011/06/15	Deciphered Date
		2012/07/11

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Title		
Compal Electronics, Inc.		
BIOS & EC I/O Port		
Size	Document Number	Rev
Custom	LA-9642P	(%)
Date:	Friday, April 19, 2013	Sheet 32 of 49



15"	14"
1 VCC	1 VCC
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 L
5 L	5 R
6 R	6 GND

A

B

C

D

E

1

1

2

2

3

3

4

4

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	USB ext. ports
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				Date: Friday, April 19, 2013	Rev (%) Sheet 34 of 49

A

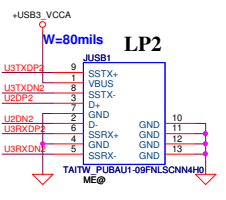
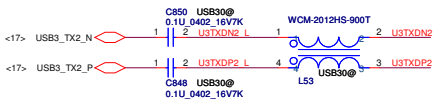
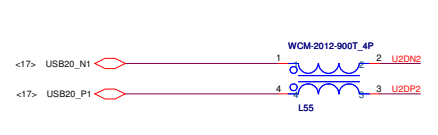
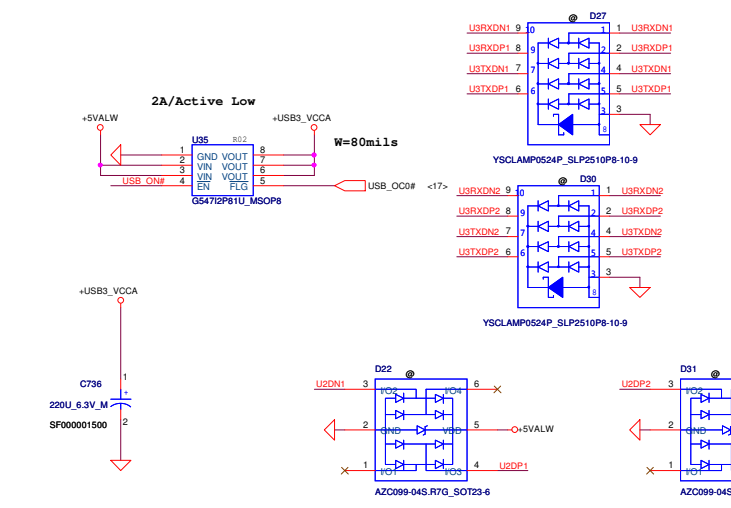
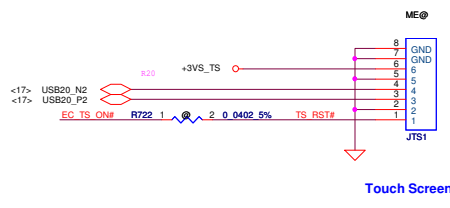
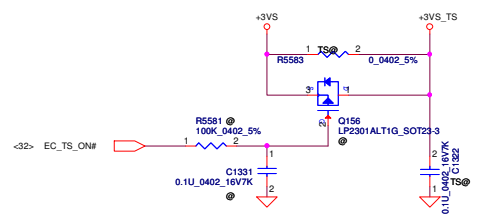
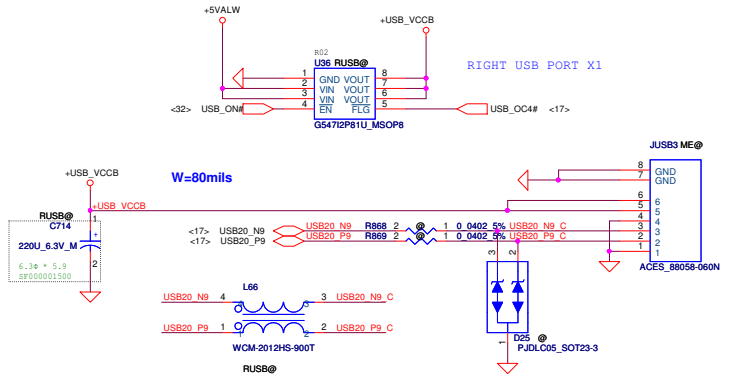
B

C

D

E

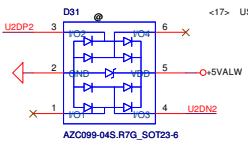
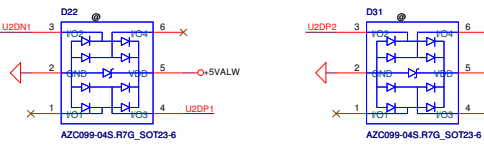
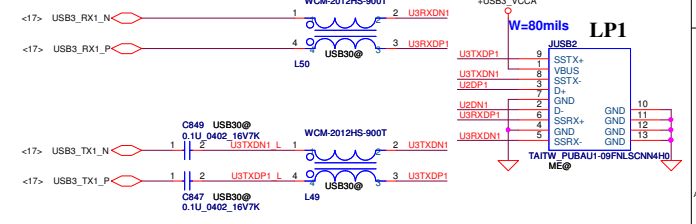
Right Ext.USB Conn.



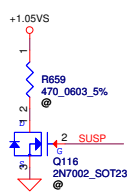
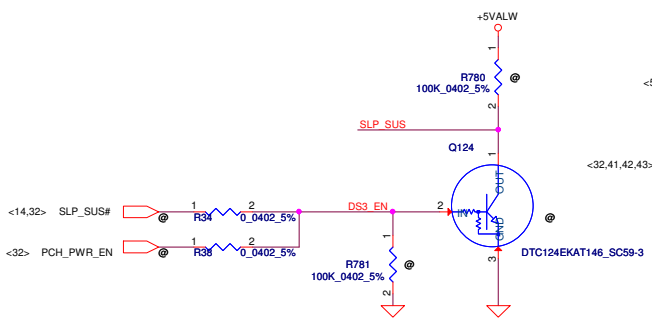
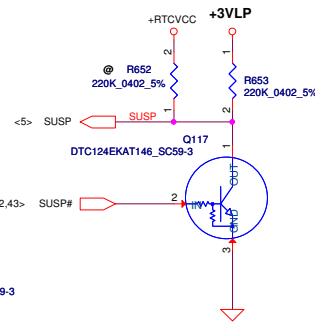
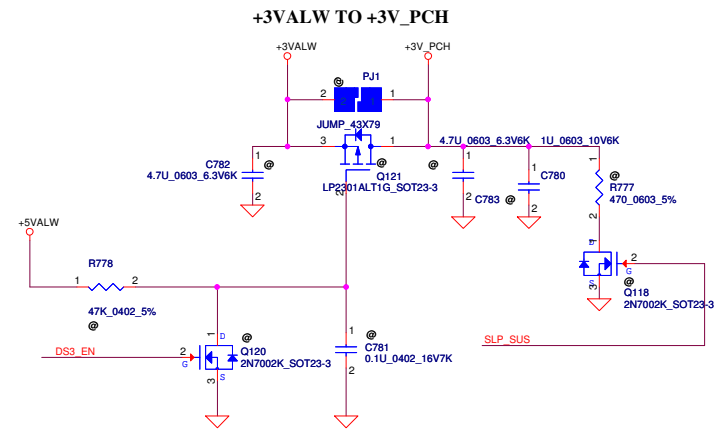
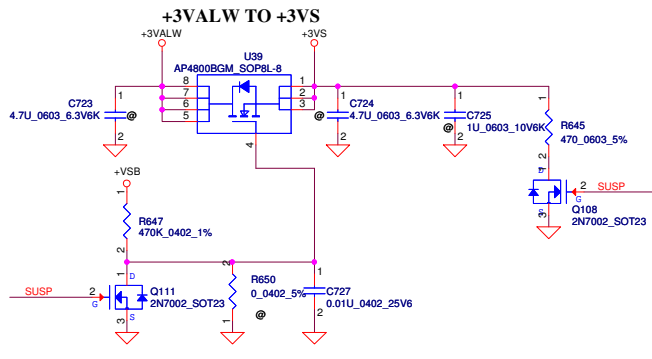
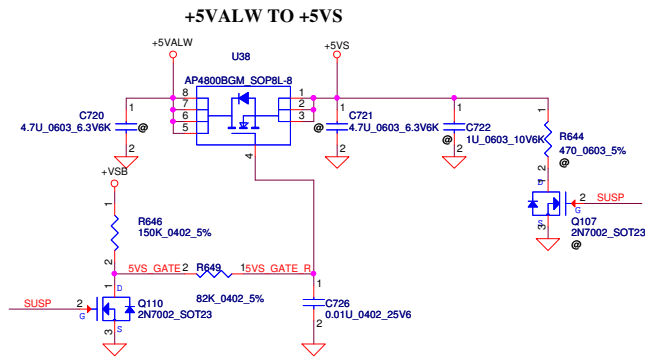
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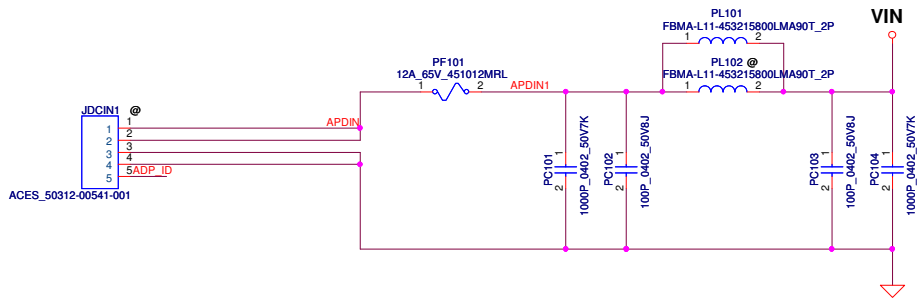
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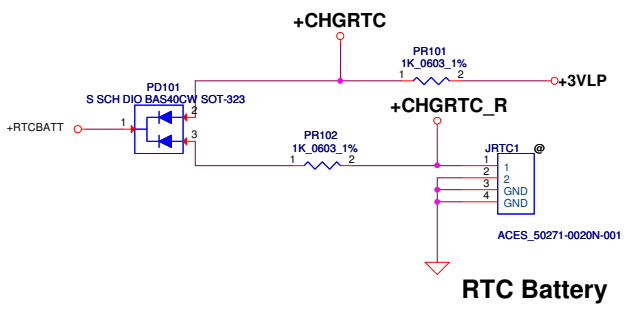
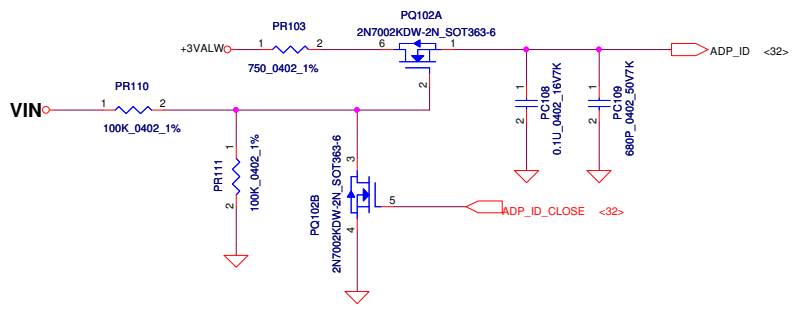
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Size	Custom	Document Number	LA-9642P		Rev
Date:	Friday, April 19, 2013	Sheet	36	of	49

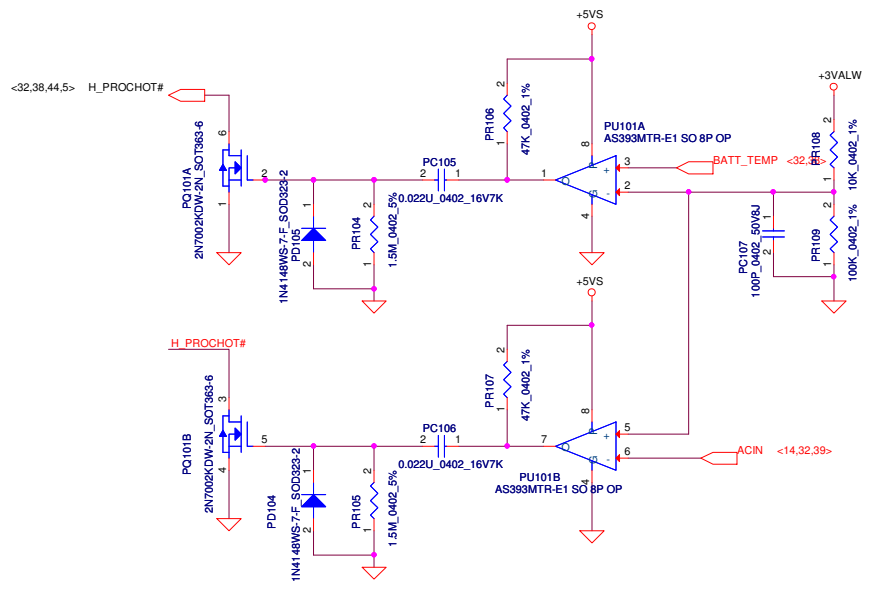


ACES_50312-00541-001



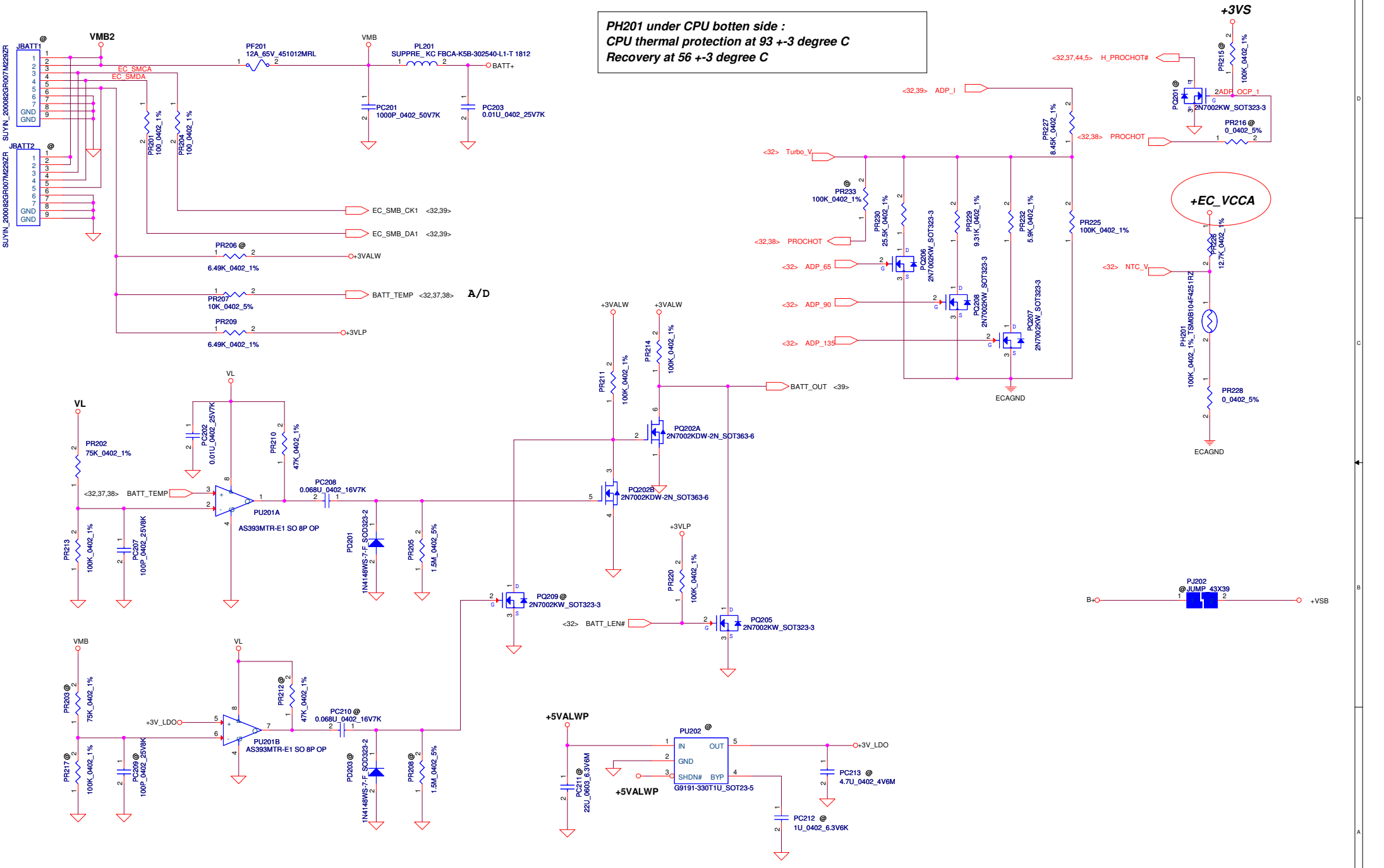
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RTC Battery



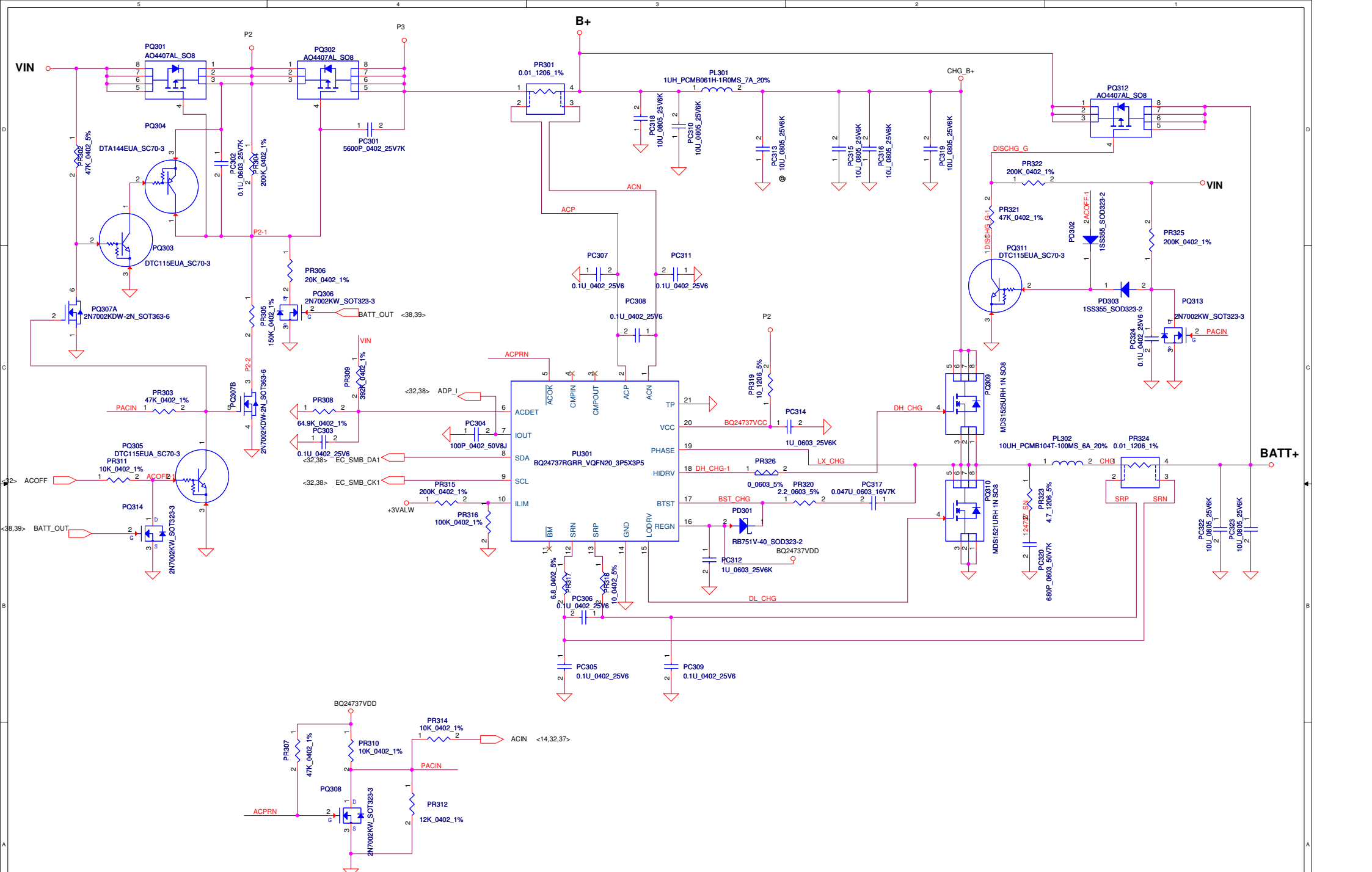
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				LA-9642P	(%)
				Date: Friday, April 19, 2013	Sheet 37 of 47

PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

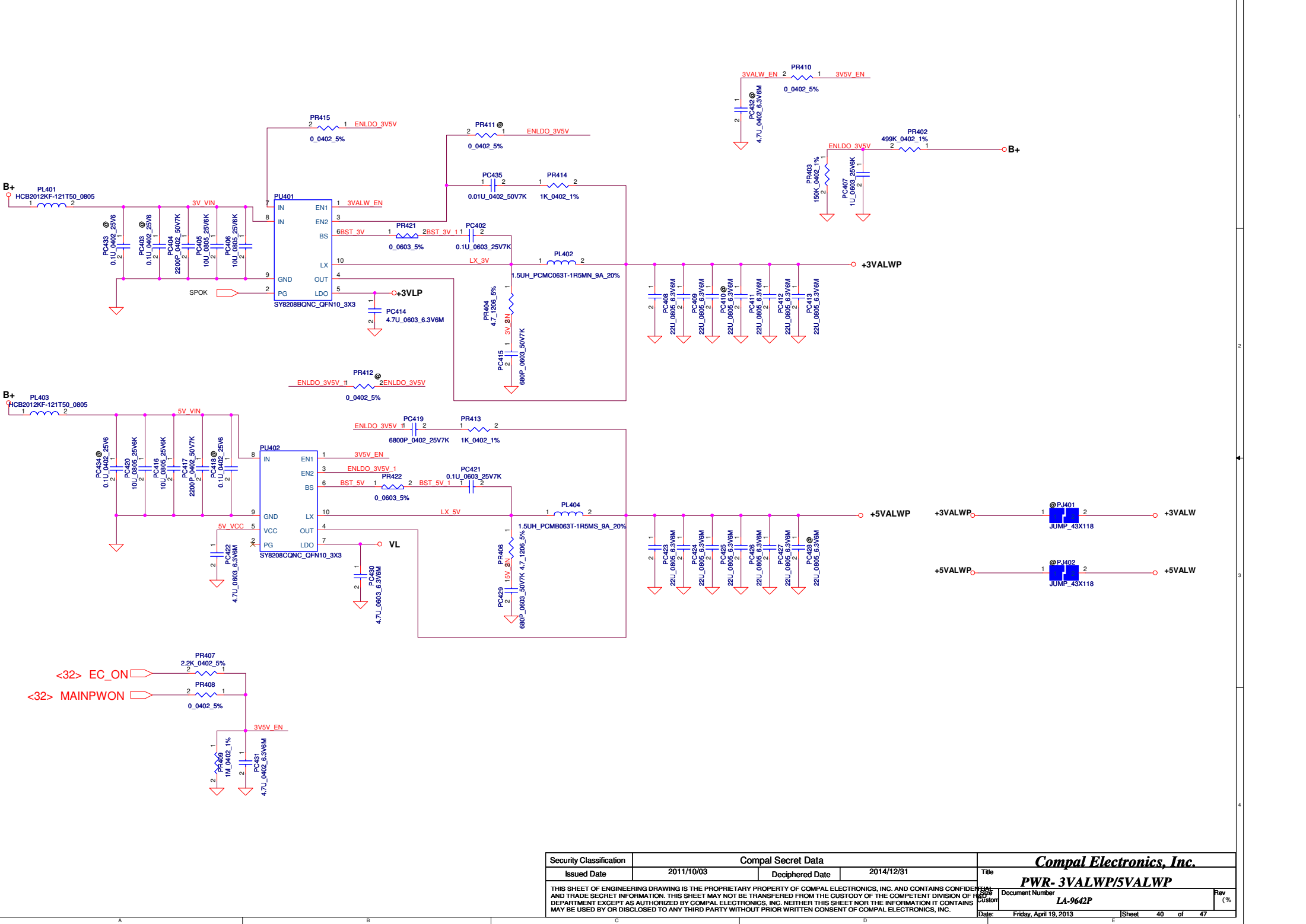


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Compal Electronics, Inc.	
PWR-BATTERY CONN/OTP	
Document Number	Rev
LA-9642P	(%)
Date: Friday, April 19, 2013	Sheet 38 of 47



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Size	Document Number			Rev	(%)
	LA-9642P				
Date:	Friday, April 19, 2013	Sheet	39	of	47

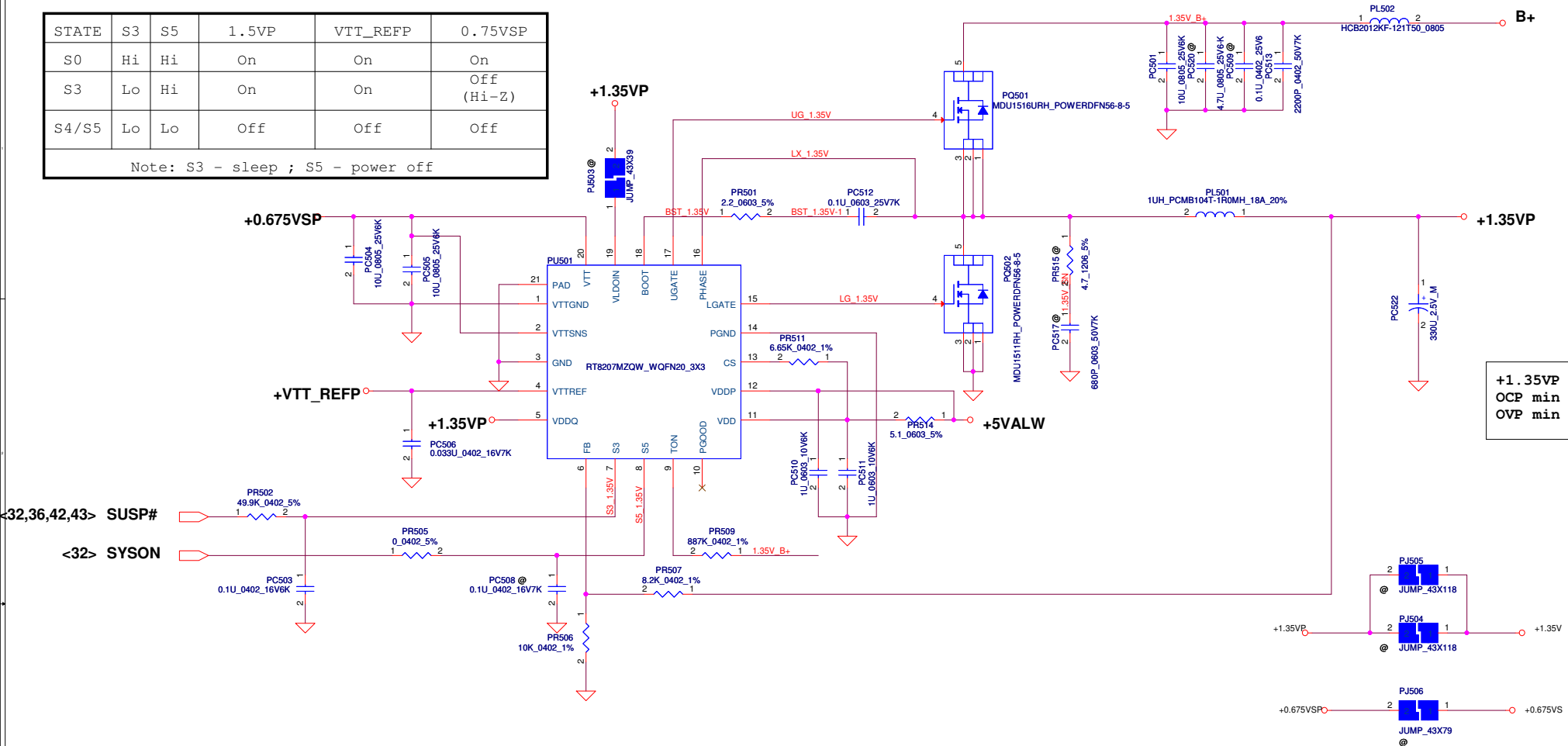


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		2014/12/31
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Title		Compal Electronics, Inc.	
Document Number		PWR- 3VALWP/5VALWP	
Date:	Friday, April 19, 2013	Sheet	40 of 47
Rev	(%)	LA-9642P	

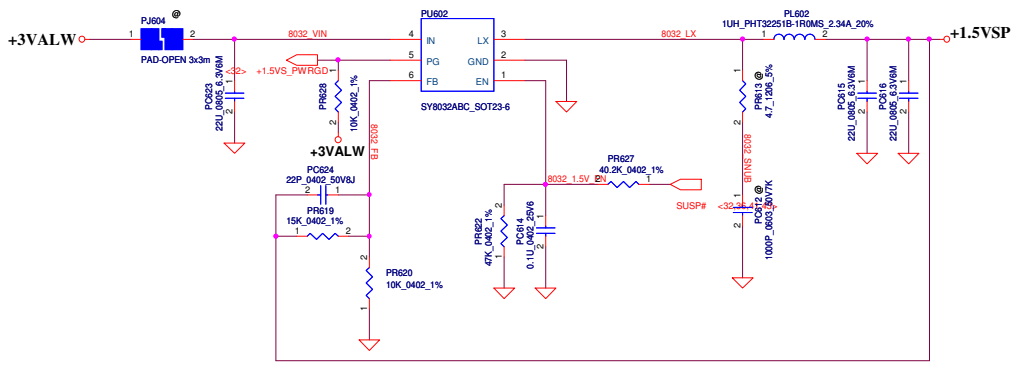
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

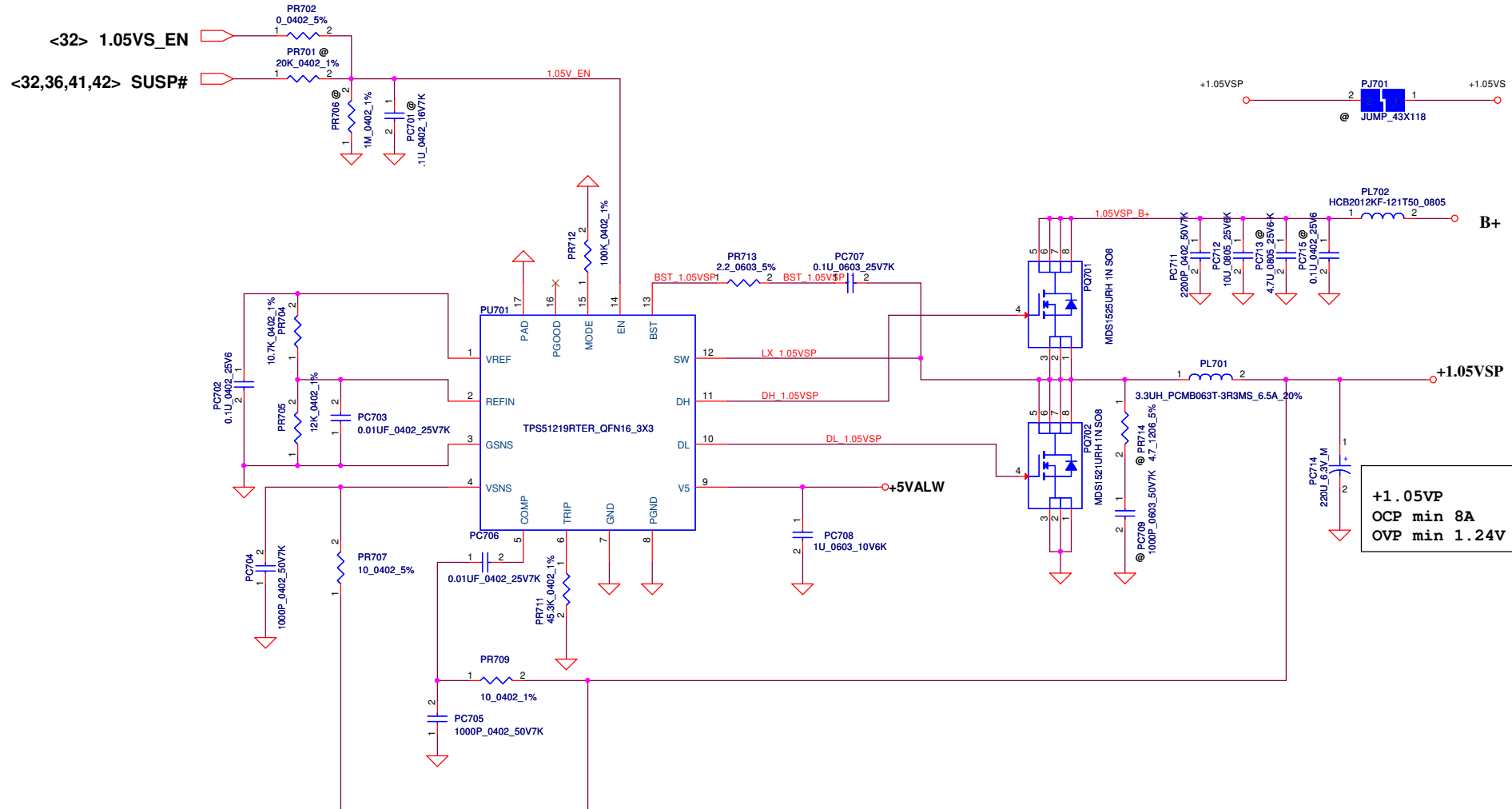


+1.35VP
 OCP min 20A
 OVP min 1.485V

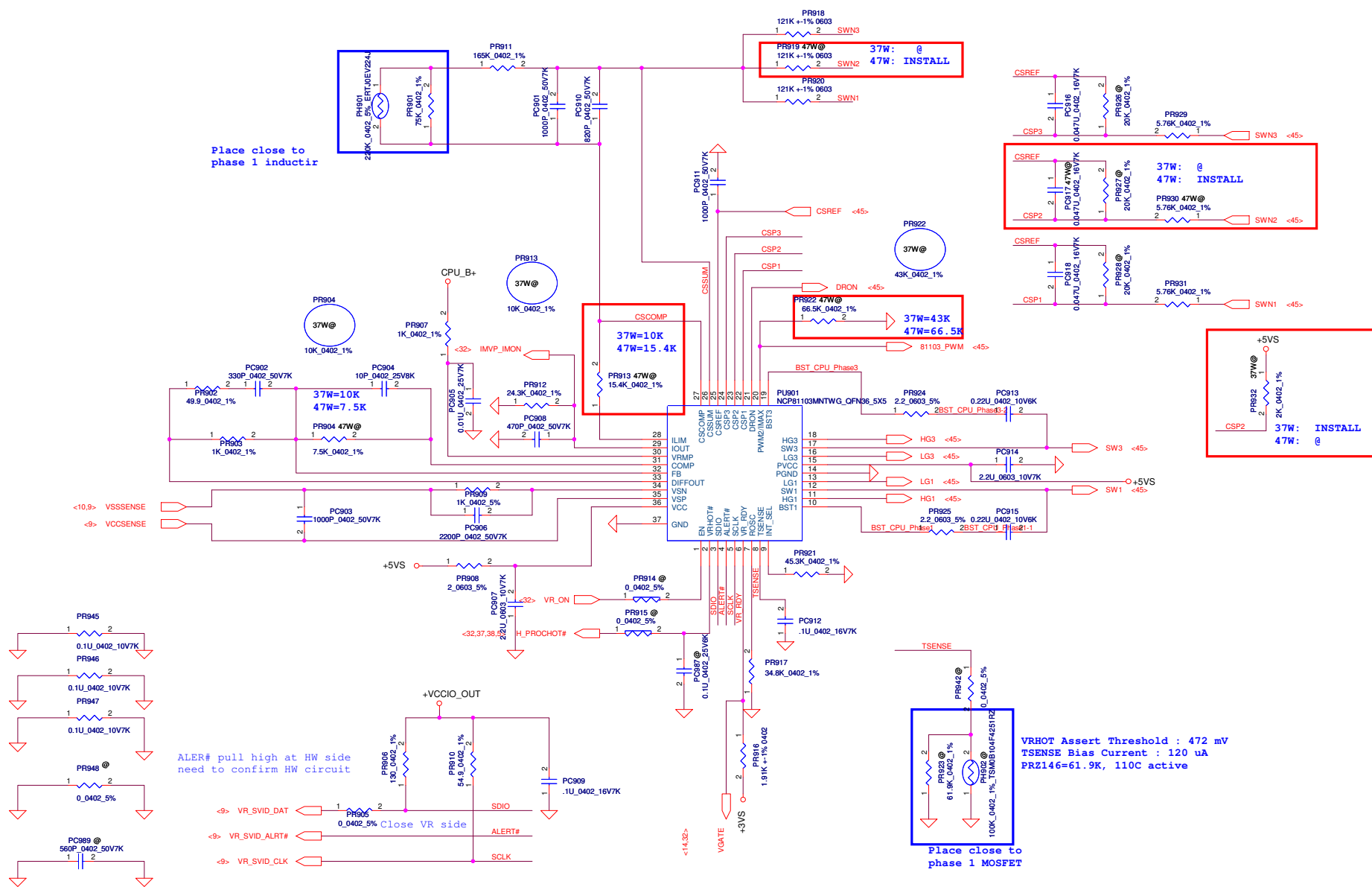
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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	+1.35V DDR
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				Custom	LA-9642P
				Date:	Friday, April 19, 2013
				Sheet	41 of 47



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Size	Document Number	Rev		
C	LA-9642P	(%)		
Date:	Friday, April 18, 2013	Sheet	42	of 47



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				Date:	Friday, April 19, 2013
				Sheet	43 of 47



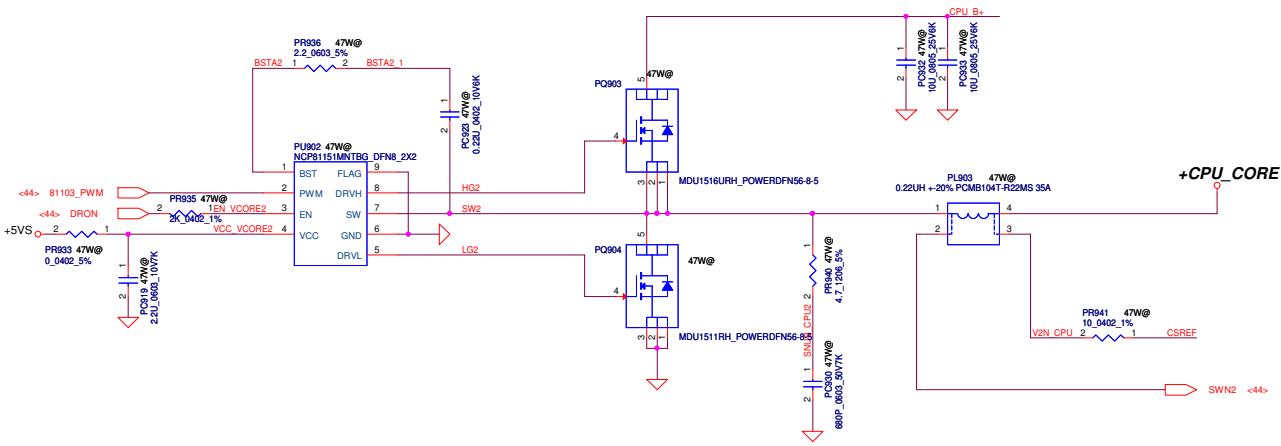
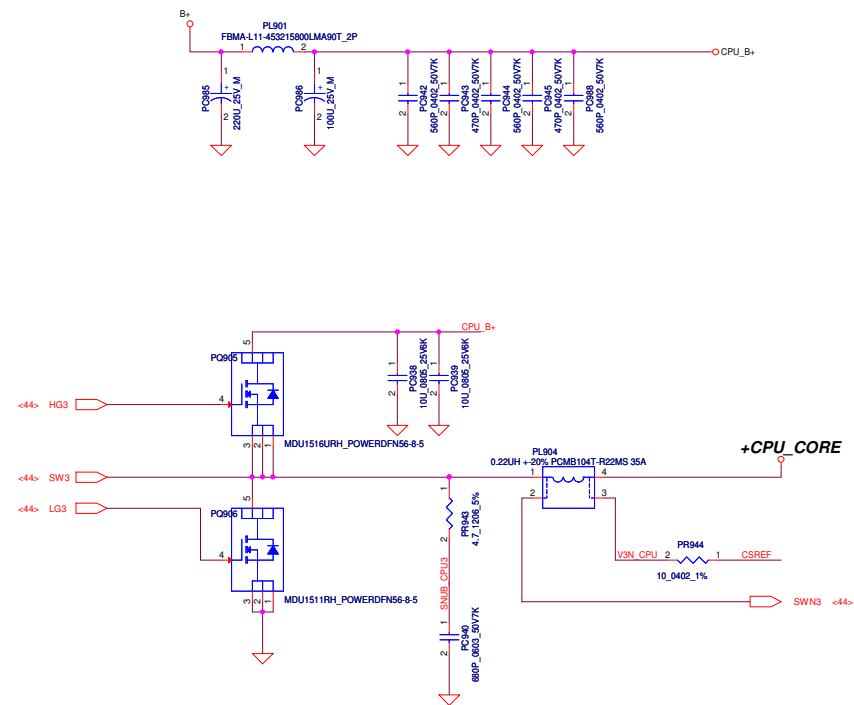
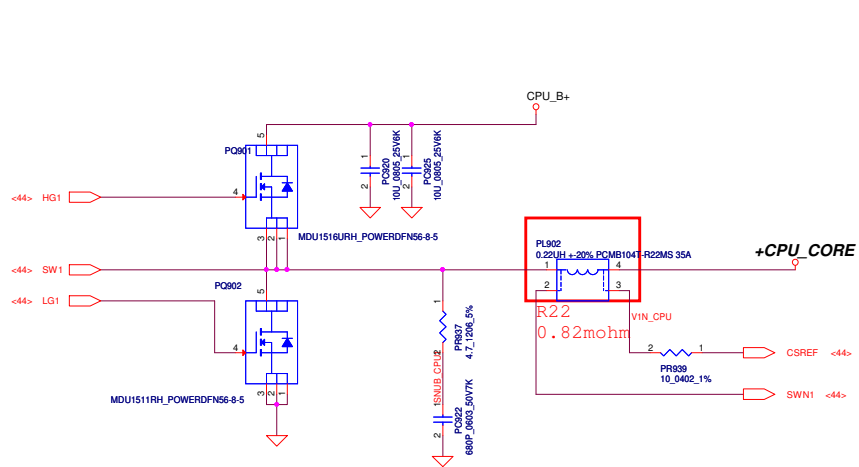
Place close to phase 1 inductor

ALERT# pull high at HW side need to confirm HW circuit

Place close to phase 1 MOSFET

VRHOT Assert Threshold : 472 mV
TSENSE Bias Current : 120 uA
PRZ146=61.9K, 110C active

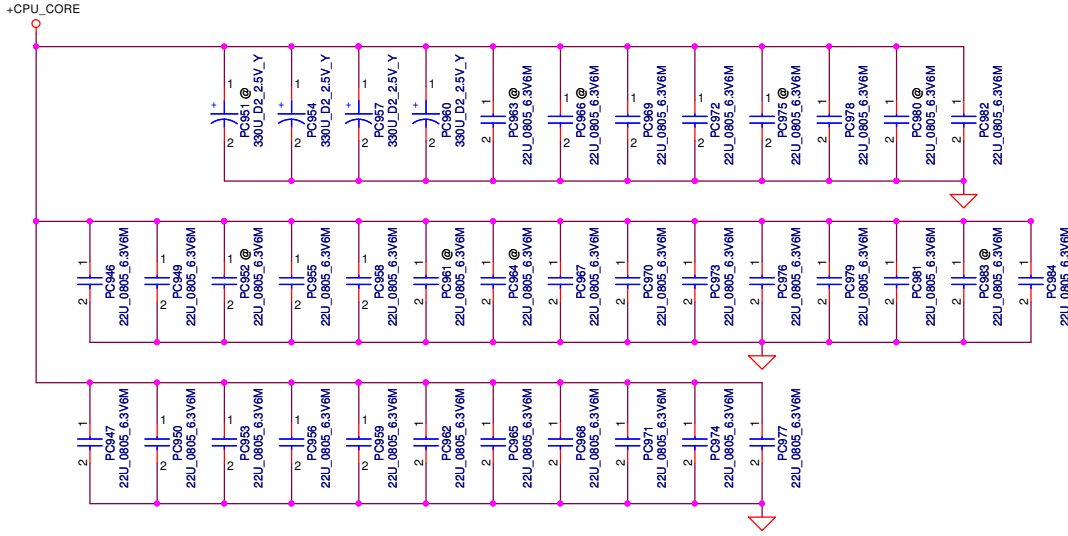
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				Customer
				LA-9642P
				Date: Friday, April 19, 2013
				Sheet 44 of 47



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+CPU_CORE

3 X 330u/9m (47W) 2X330u/9m (37W)
 34 X 22u/0805 34 X 22u/0805



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Title				PROCESSOR DECOUPLING	
Size				Document Number	
				LA-9642P	
Date				Friday, April 19, 2013	
Sheet				46 of 47	

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adapter ID selection circuit	37 38	Add PR103,PR110,PR111,PQ102,PC108,PC109 Add PR227,PR230,PR229,PR232,PR225,PQ206,PQ208,PQ207	2012.11.28	DVT
2	Delete reserve circuit B+ to VSB	38	Delete PR217,PR218,PR219,PC204,PQ203,PR223,PR224,PC205,PQ204,PC206	2012.11.28	DVT
3	Pop Snubber by EMI request	39	PR323,PC320	2012.11.28	DVT
4	To reduce ripple	40	PC411,PC426 and change PL404 to 3.3uH	2012.11.28	DVT
5	Reserve enable signal by HW request	40	Add PR410,PC432	2012.11.28	DVT
6	Add boost resistor by EMI request	40	Add PR421,PR422	2012.11.28	DVT
7	Reserve feedback signal for IC application	40	Add PR413,PC419	2012.11.28	DVT
8	To reduce ripple	43	Change PL701 to 3.3uH	2012.11.28	DVT
9	Reserve enable signal by HW request	43	Add PR702	2012.11.28	DVT
10	Add input MLCC by EMI request	44	Add PC943,PC944,PC945,PC988	2012.11.28	DVT
11	Reserve battery detective circuit	38 39	Add PR203,PR217,PC209,PR212,PC210,PD203,PR208,PQ209,PC211,PU202,PC212,PC213 Add PQ314,PR311(Pop)	2013.03.03	PVT
12	Reserve capacitor by EMI request	39	Add PC318,PC319	2013.03.03	PVT
13	Reduce component	40	Delete PD401	2013.03.03	PVT
14	Reserve 1.5VSP Power Good by HW request	42	Add PR628	2013.03.03	PVT
15	Reserve bridge resistor by EMI request	44	Add PR948,PC989		
16					

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Size	Custom	Document Number	LA-9642P	Rev	(%)
Date:	Friday, April 19, 2013	Sheet	47	of	47

Item	Reason for change	PG#	Modify List	Date	Phase
1	USE singal 8M ROM for BIOS		Change U8 to SA000039A30 8MB ROM Del U7, R239, R234, R235, R233, R236	12/25	DVT
2	POWER NEW AC Connector		U31.21--> ADP_65 U31.68 change from EC_WL_OFF# to ADP_90 U31.85 change from EC_TS_ON#to ADP_135 U31.66 change from BRDID_1 to ADP_ID	12/25	DVT
3	Change XDP pull down Resistor to R pack		Del R18, R21, R23 / Add RP19	12/25	DVT
4	Update Lenovo BGA footprint		UV1, U4, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	12/25	DVT
5	Move 15" ODD CAP to Small Board		ChangeC605 to R401/ChangeC606 to R402/ ChangeC618 to R403/ChangeC617 to R404	12/25	DVT
6	WLAN Control change to PCH		PCH_GPIO55--> PCH_WL_OFF# PCH_GPIO22-->PCH_BT_ON# PCH_GPIO34-->INTEL_BT_OFF#	12/25	DVT
7	POP TL_ENVDD PULL DOWN		POP R408	12/25	DVT
8	Change HDMI LV from 10P8R to 8R4R X2		Del RP19 ADD RP5, RP6	12/25	DVT
9	Update EC GPIO		NOVO# change form pin 26 to 34 EC_FAN_PWM change form pin 34 to 26 ENBKL change form pin 73 to 76 IMVP_IMON change form pin 76 to 73 DGPU_PWR_EN change form pin 107 to 123	12/25	DVT
10	VGA sequence		+1.5VGS : RV41 --> 240K / CV53 --> 0.1U	12/25	DVT
11	EC Board ID		Change R695 to 15K	12/25	DVT
12	Change ODD connector symbol		JODD1->ALLTO_C18518-11305-L_13P-T	12/25	DVT
13	Update Crystal cap Value by vendor suggestion		C111/ C112 --> 15p CV36/CV37-->8.2p	12/25	DVT
14	Reserve for EMI		ADD R411, R412, C411, C412	12/25	DVT
15	Change PCIE port and clock connection by SW request		LAN-->Port 3 / WLAN--> Port2	12/25	DVT
16	Reserve R301		Reserve +3VLP power rail to EC	12/25	DVT
17	Change EC_RST# power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
18	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
19					
20					
21					
22					

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Size	Custom	Document Number	VIWGG/GS		Rev (%)
Date:	Friday, April 19, 2013	Sheet	48	of	49

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add resistor to switch audio power from +3VS to +3VLP and +3VALW.		Add RA1,RA2	02/18	PVT
2	Reconnect HDD +3VS power rail.		Add R-short R552.	02/18	PVT
3	Modify LED current limiting resistor value.		Modify : R623,R765,R303	02/18	PVT
4	Add parallel resistor to separate BIOS and EC.		Add RP2	02/18	PVT
5	Add a Capacitor to connect CHASSIS_GND and GND by EMI request.		Add CL64	02/18	PVT
6					
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Size	Custom	Document Number	VIWGG/GS	Rev	(%)
Date:	Friday, April 19, 2013	Sheet	49	of	49

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