

Compal Confidential

UMA M/B Schematics Document Haswell with DDRIII + Lynx Point PCH

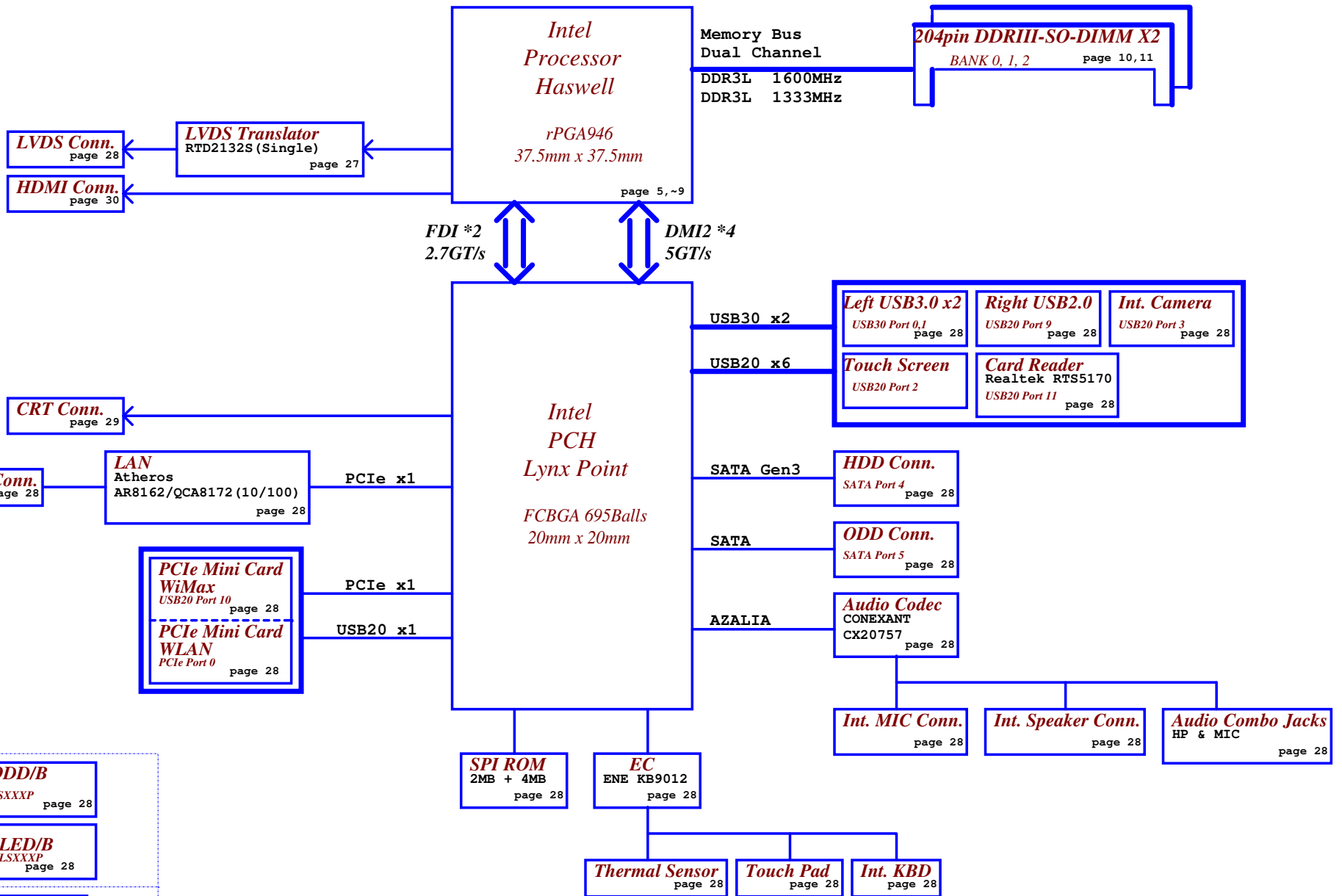
2012-10-03

LA-9642P

REV: 0.1

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page		
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Shark Bay



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				Block Diagram
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Voltage Rails

power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS
				+VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
		2	Touch screen
	UHCI1	3	Camera
		4	
		5	
		6	
7			
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
		12	
		13	

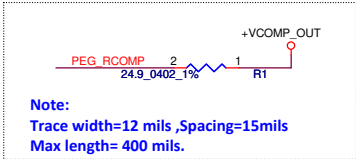
BOM Structure Table

BTO Item	BOM Structure
HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Camera	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@

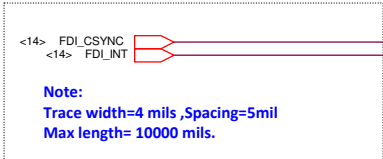
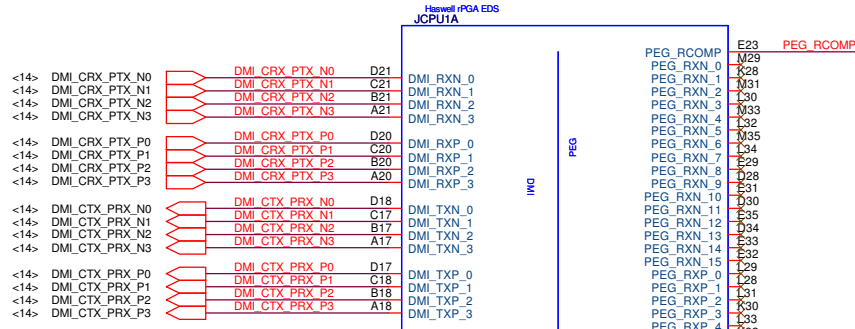
SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	√	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	+3VS	+3VS
SMB_EC_DA2	+3VALW								
SMBCLK	PCH	X	X	X	√	√	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	√	X	√	X	X	√	X	√
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

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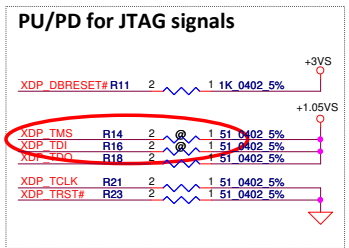
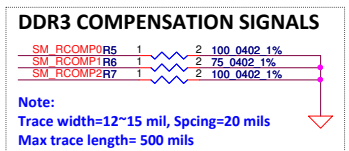
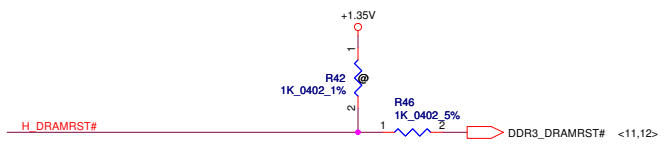
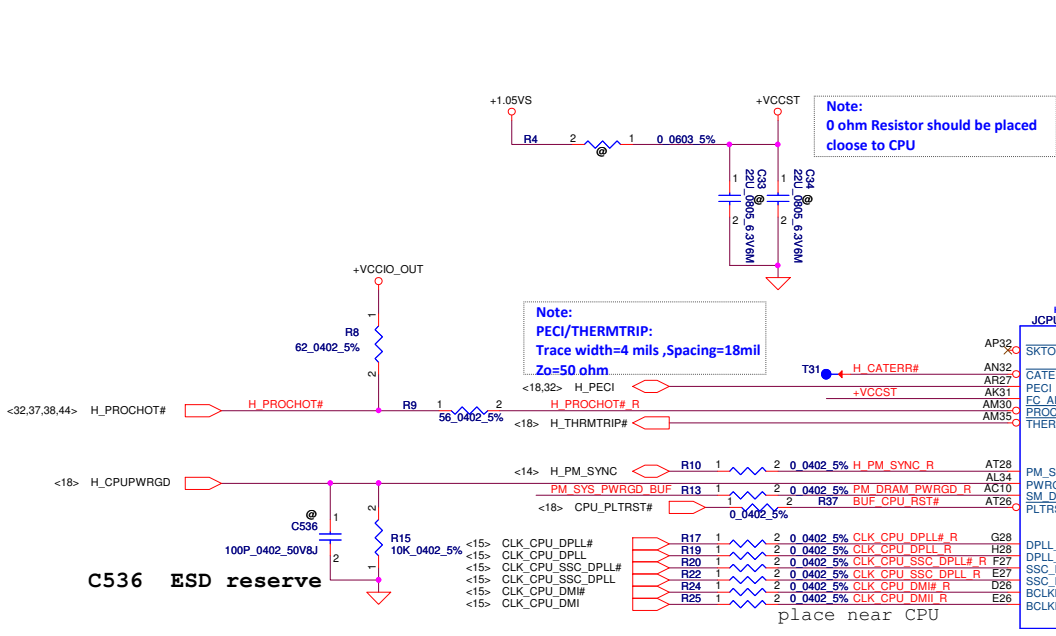
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Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.



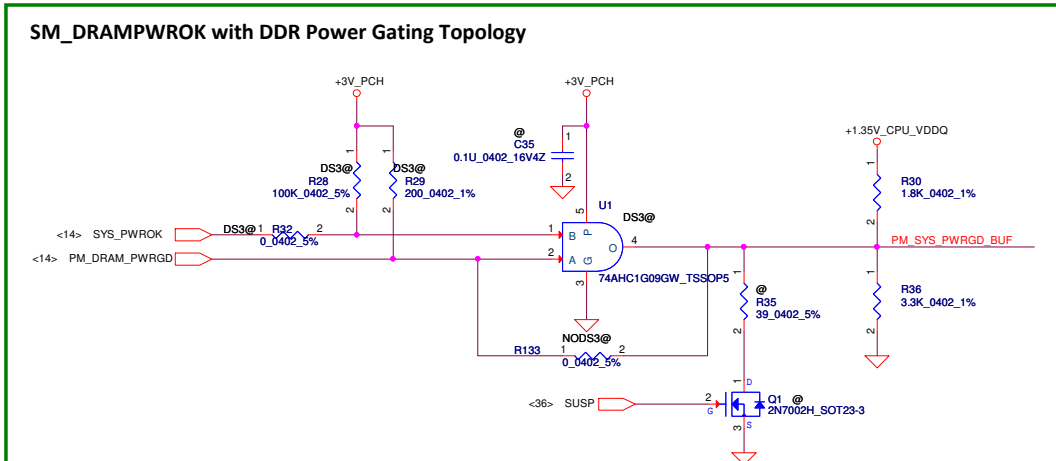
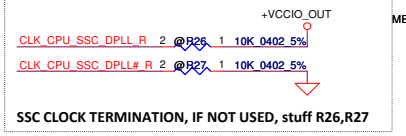
Note:
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Max length= 10000 mils.

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ME@

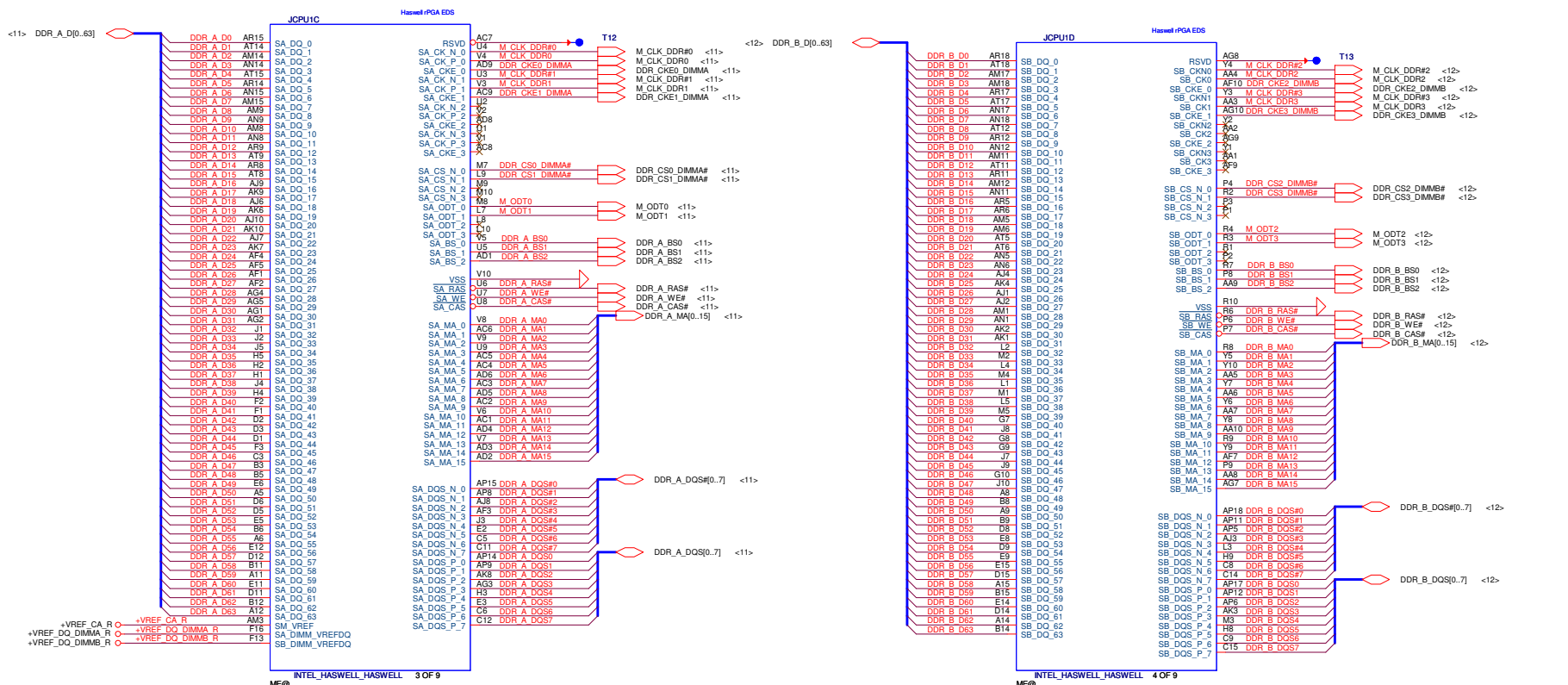
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PROCESSOR(1/7) DMI,FDI,PEG	
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C536 ESD reserve



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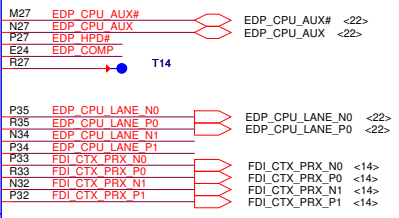
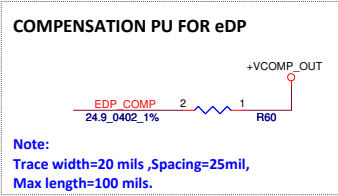
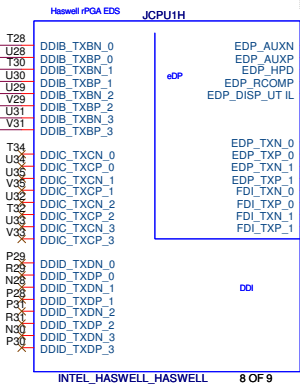
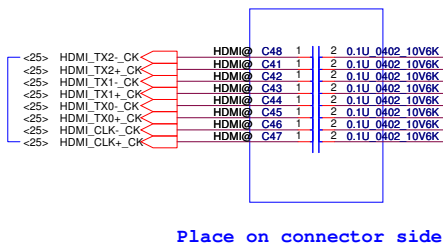
CPI DRIVER VREF PATH IS DEFAULT

*M3-M1:Default Recommendation
 M1:VREF_DQ driven by a voltage Divider Network during Processor power-off state.
 M3:VREF_DQ driven by Processor.

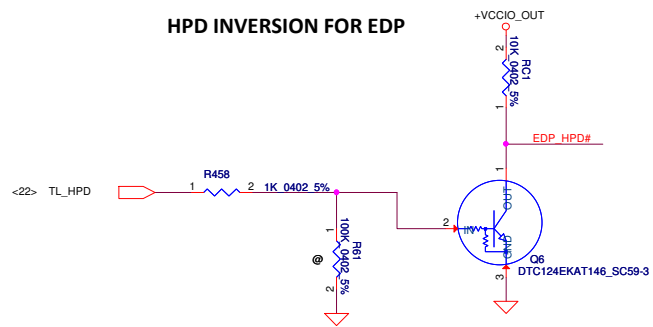
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI



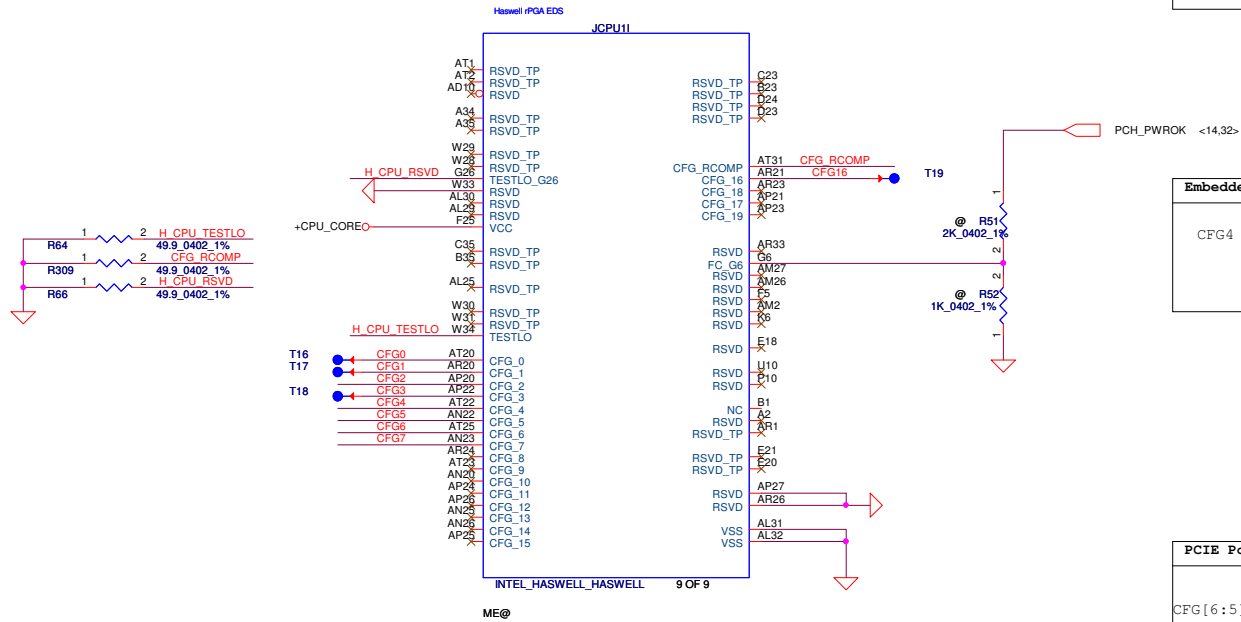
HPD INVERSION FOR EDP



HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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CFG Straps for Processor



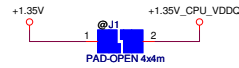
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

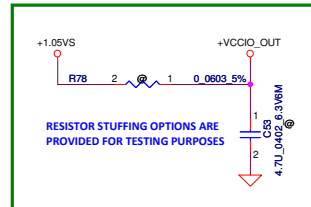
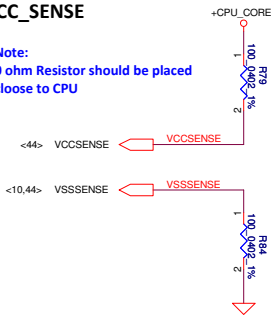
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

+1.35V_CPU_VDDQ Source



VCC_SENSE

Note:
0 ohm Resistor should be placed close to CPU



RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES



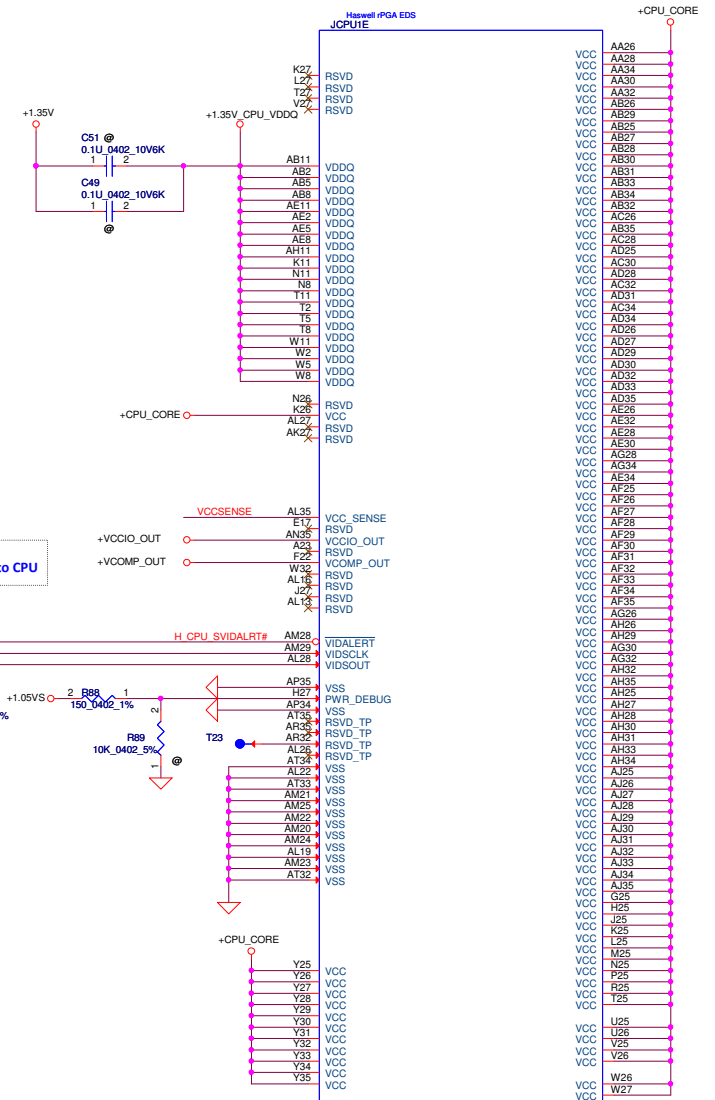
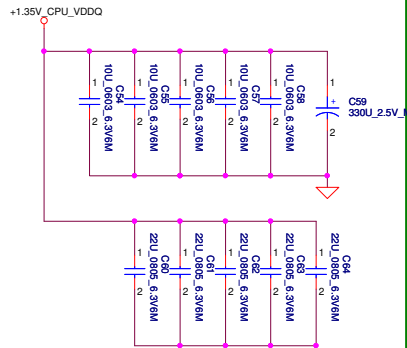
Note:
Place the UP resistor close to CPU



Note:
Place the UP resistor close to CPU



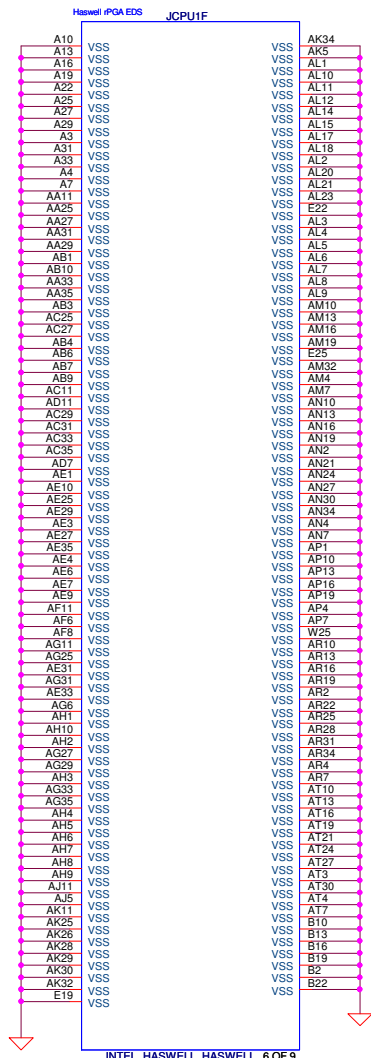
VDDQ DECOUPLING



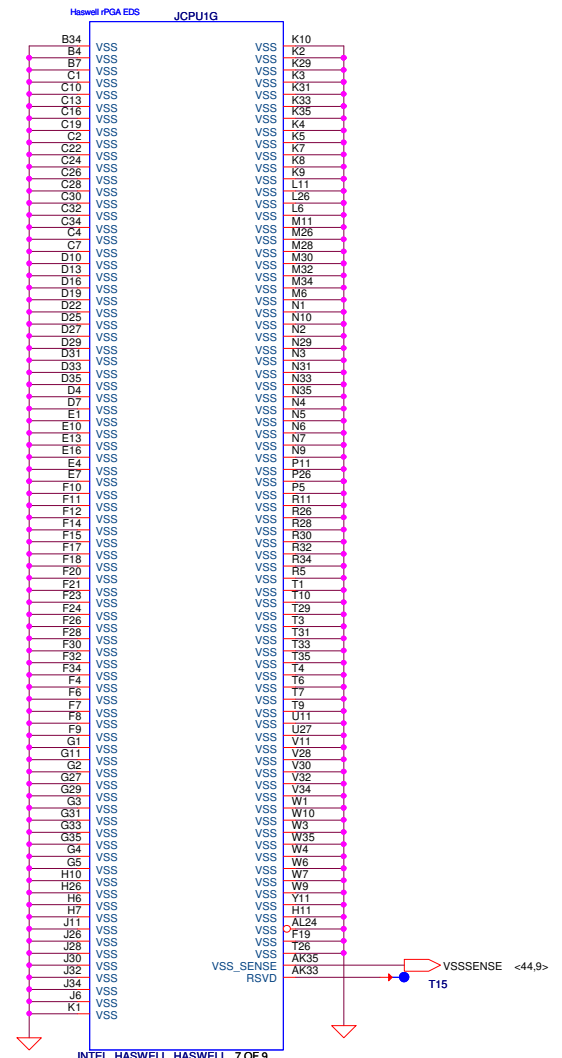
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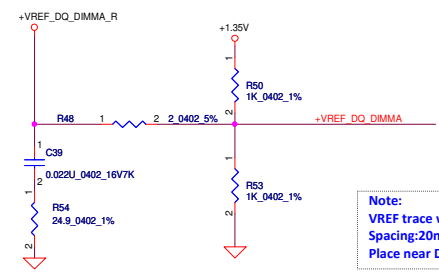
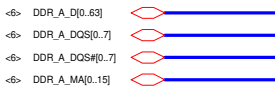


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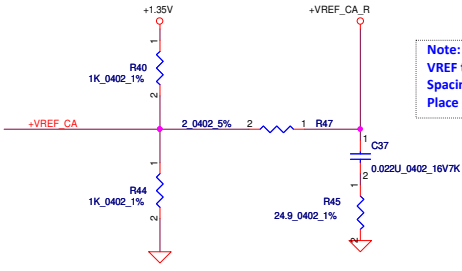


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Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

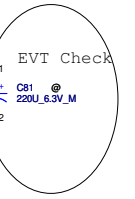
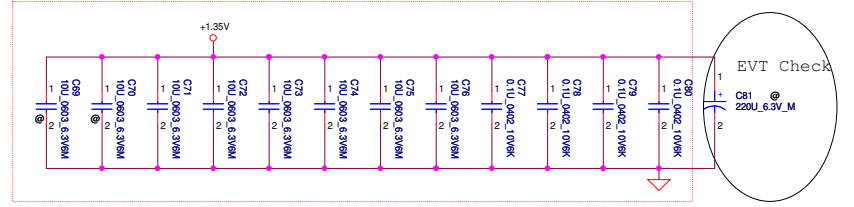


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Place near DIMM socket

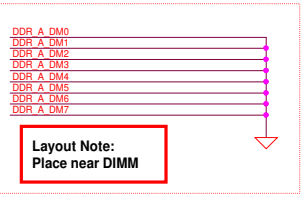
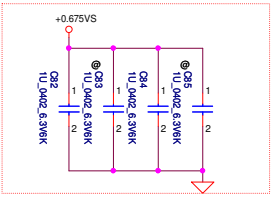
Layout Note:
Place near DIMM

$OSCAN (220uF_6.3V_4.2L_ESR17m) *1 = (SF00002Y00)$
 $(10uF_0603_6.3V) *8$
 $(0.1uF_402_10V) *4$

Layout Note:
Place near DIMM

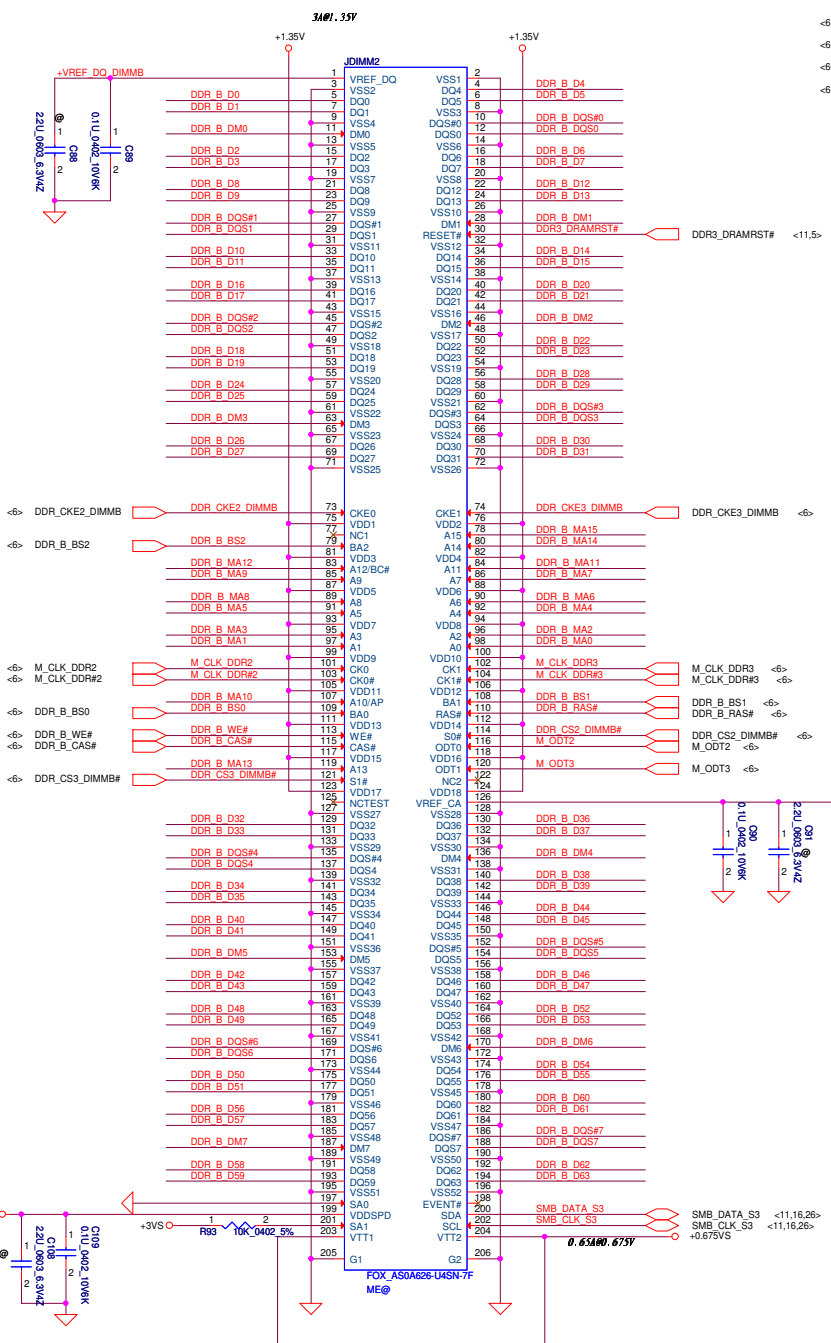


Layout Note:
Place near DIMM

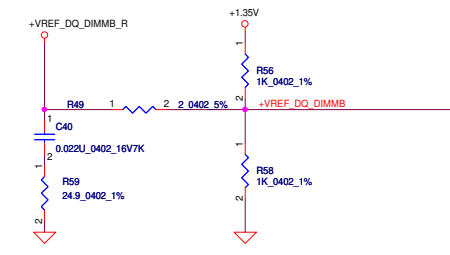


Layout Note:
Place near DIMM

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Rev	Document Number	Date	Wednesday, October 03, 2012	LA-7981P
R01	2201_0603_6.3V_M	11	11	of 60

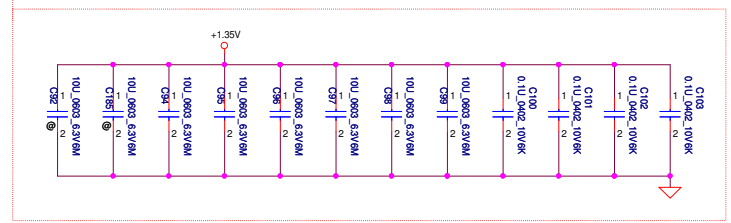


Note:
VREF trace width: 20 mils at least
Spacing: 20mils to other signal/planes

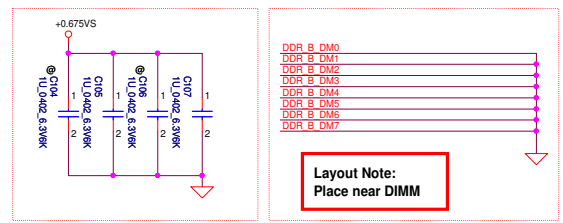


Layout Note:
Place near DIMM

(10uF_0603_6.3V) * 8
(0.1uF_402_10V) * 4

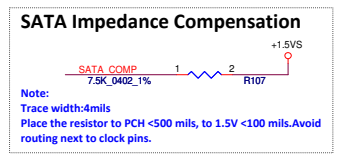
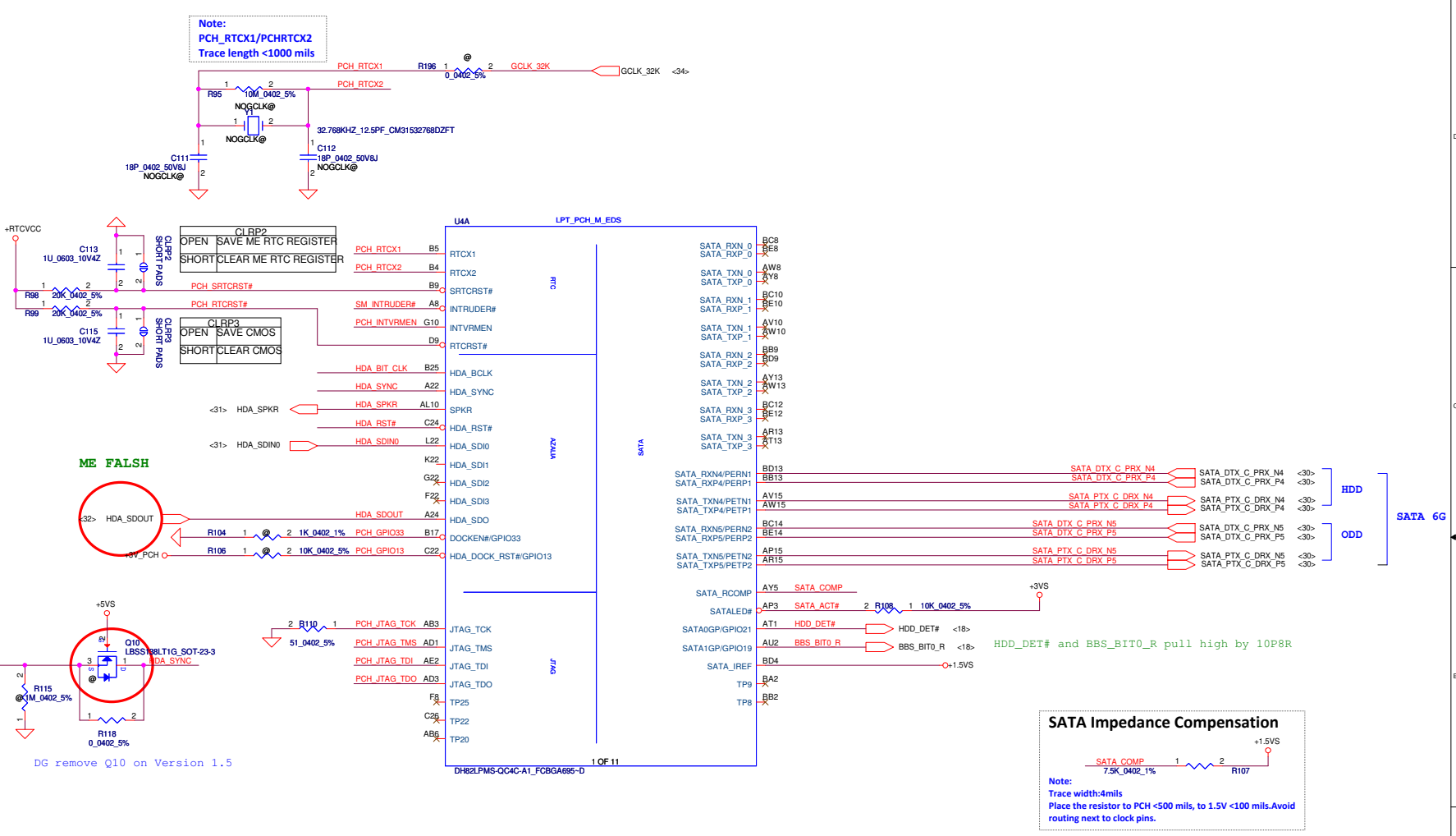
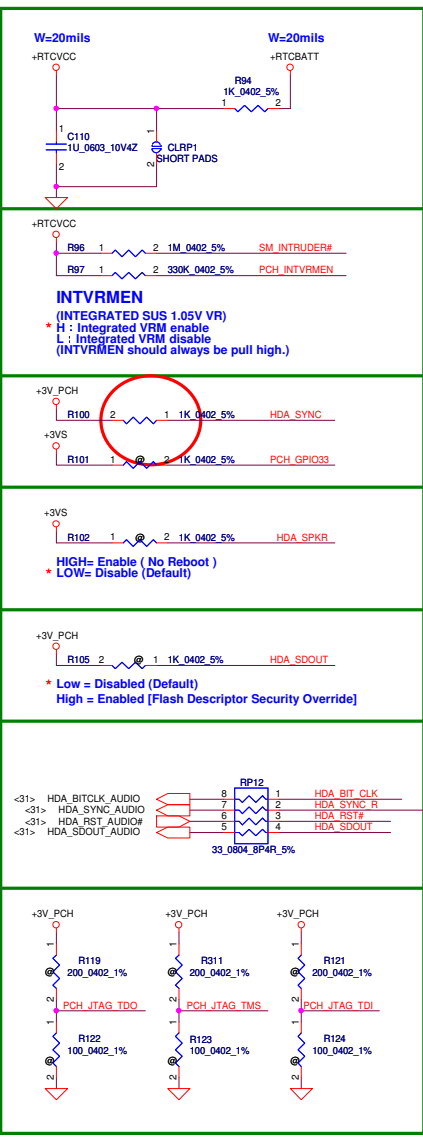


Layout Note:
Place near DIMM

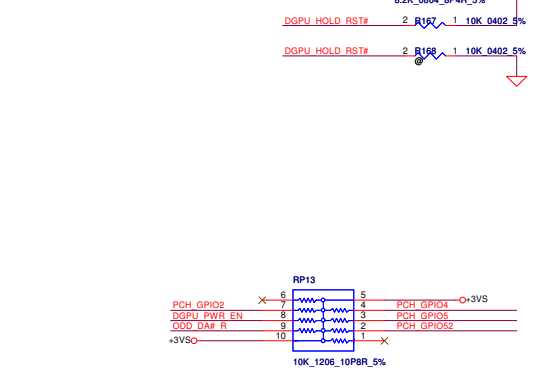
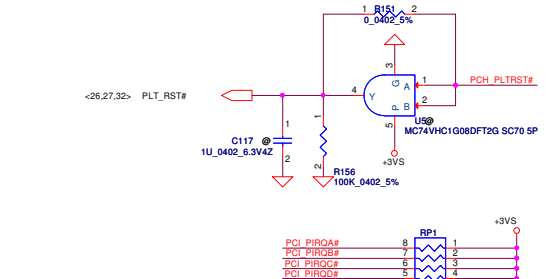
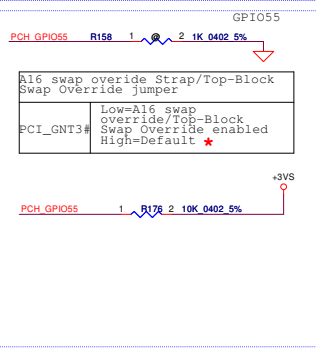
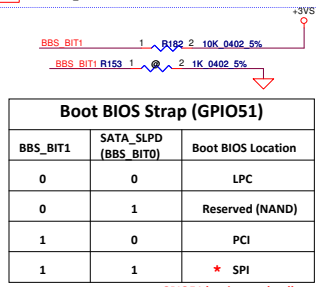
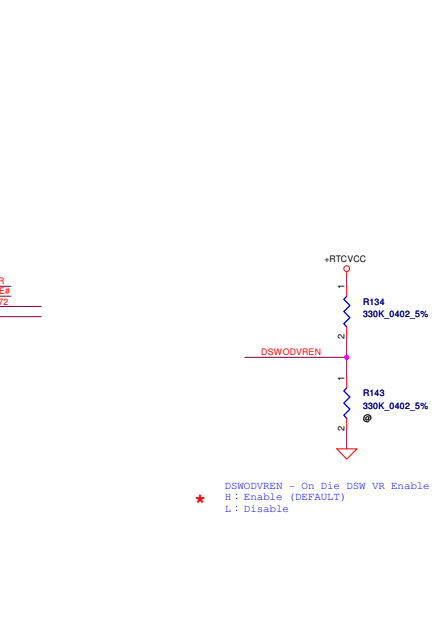
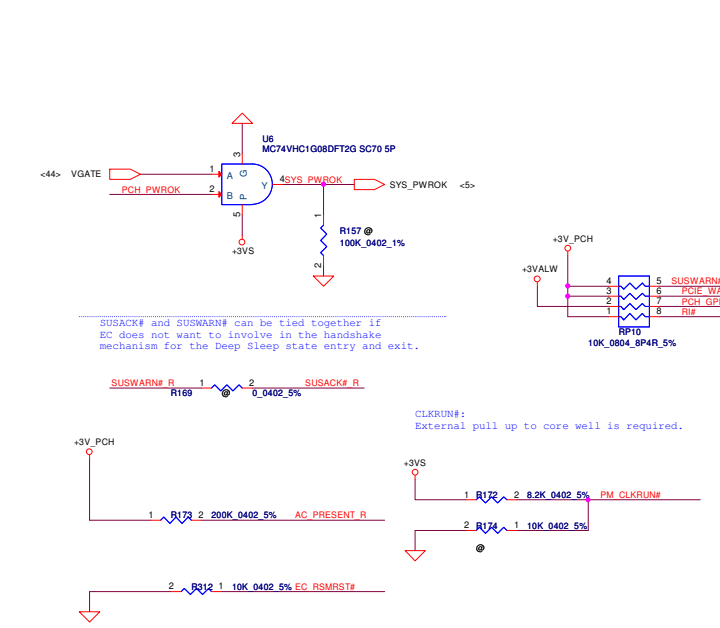
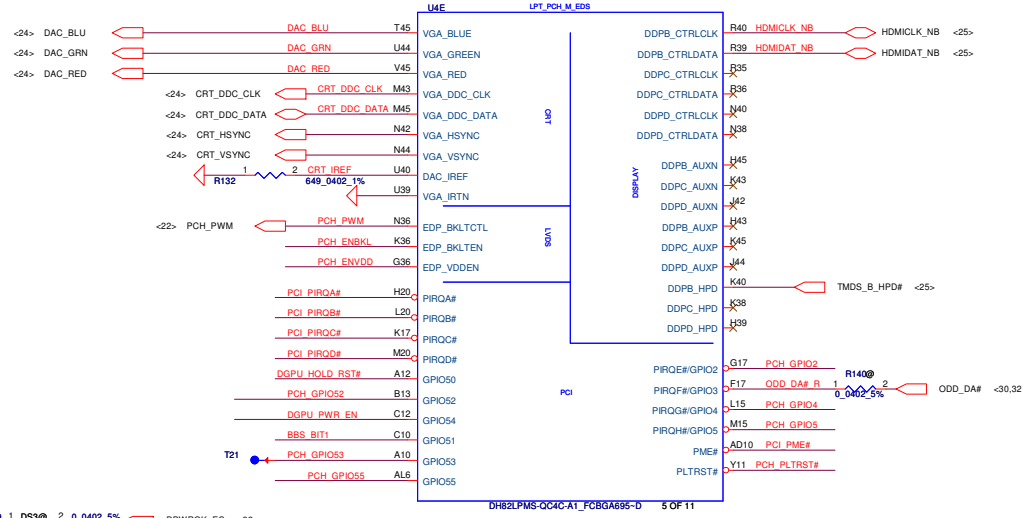
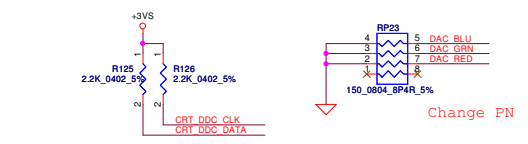
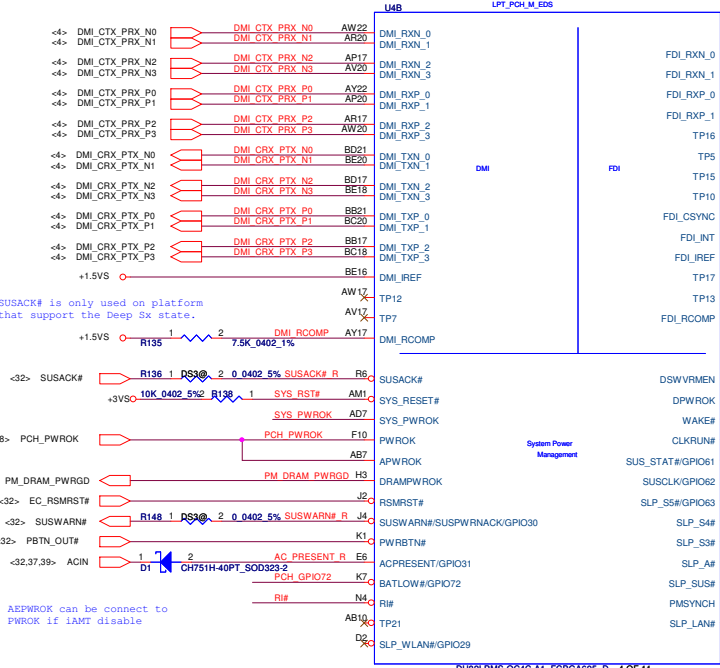


Layout Note:
Place near DIMM

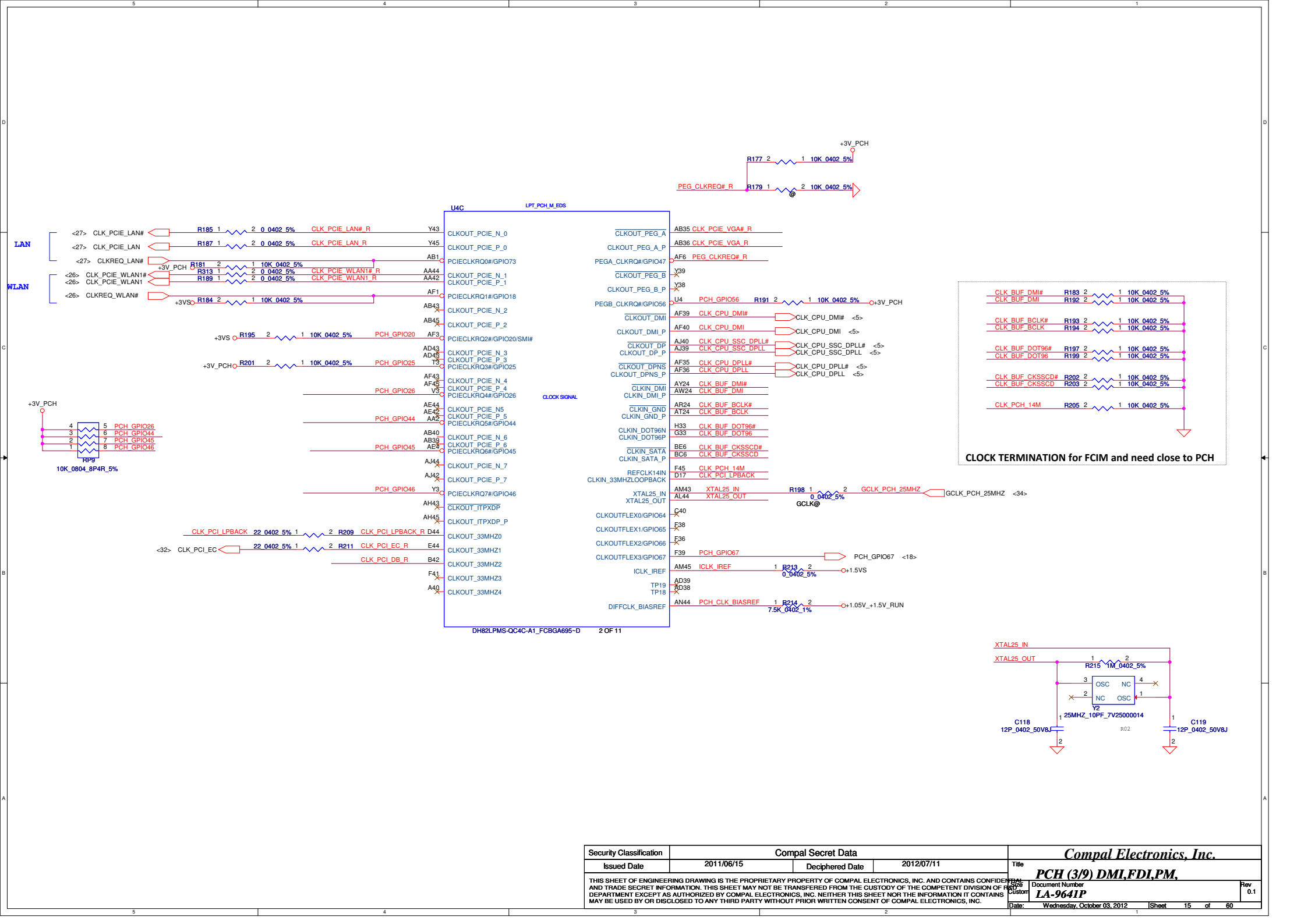
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	DDR III-SODIMM SLOT2	
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Sheet		of 60		

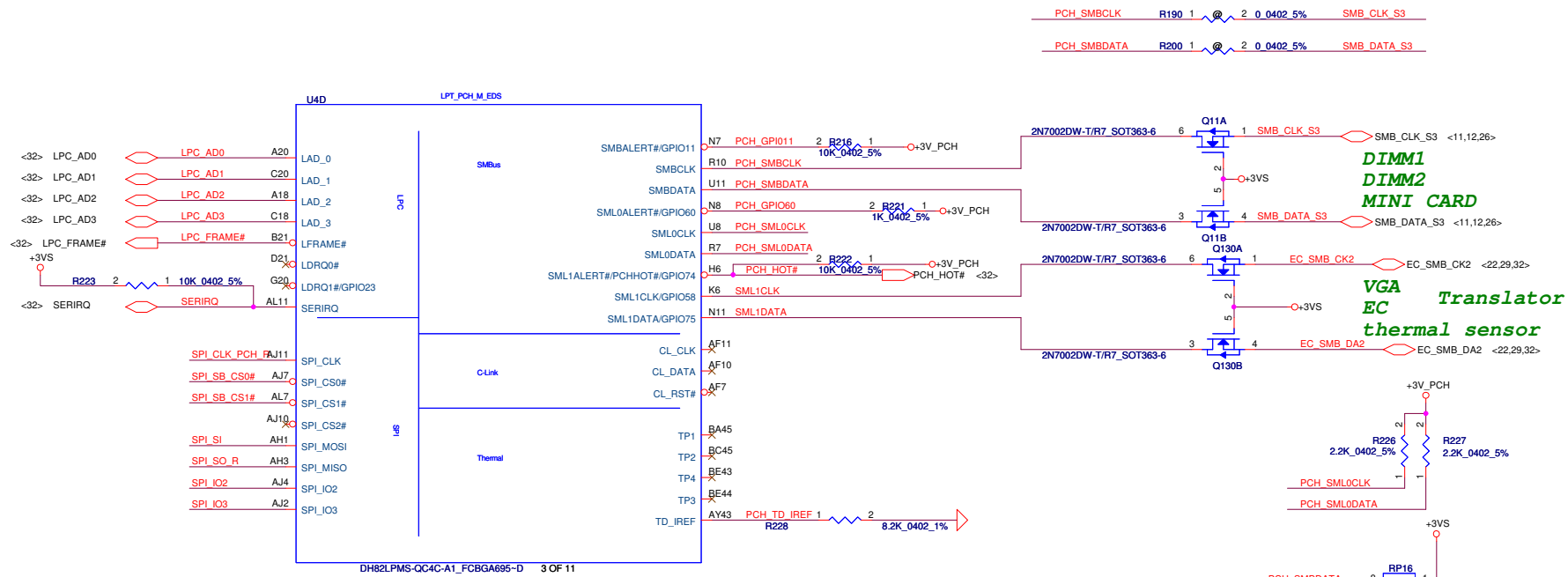


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<p>Company: Compal Electronics, Inc. Title: PCIE (2/9) PCIE, SMBUS, CLK</p>			<p>Document Number: LA-9641P Date: Wednesday, October 03, 2012 Sheet: 14 of 60</p>	



CLOCK TERMINATION for FCIM and need close to PCH

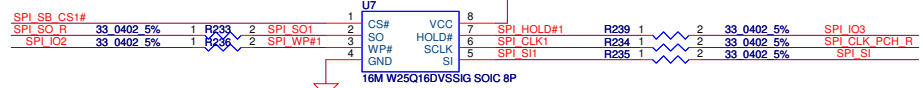
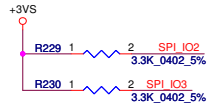
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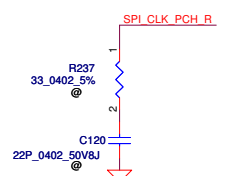
**DIMM1
DIMM2
MINI CARD**

**VGA
EC Translator
thermal sensor**

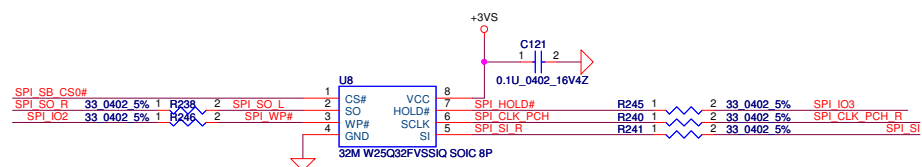
8MB SPI ROM FOR ME & Non-share ROM.



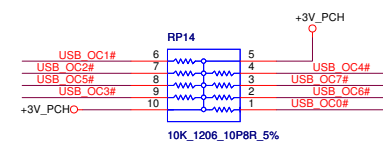
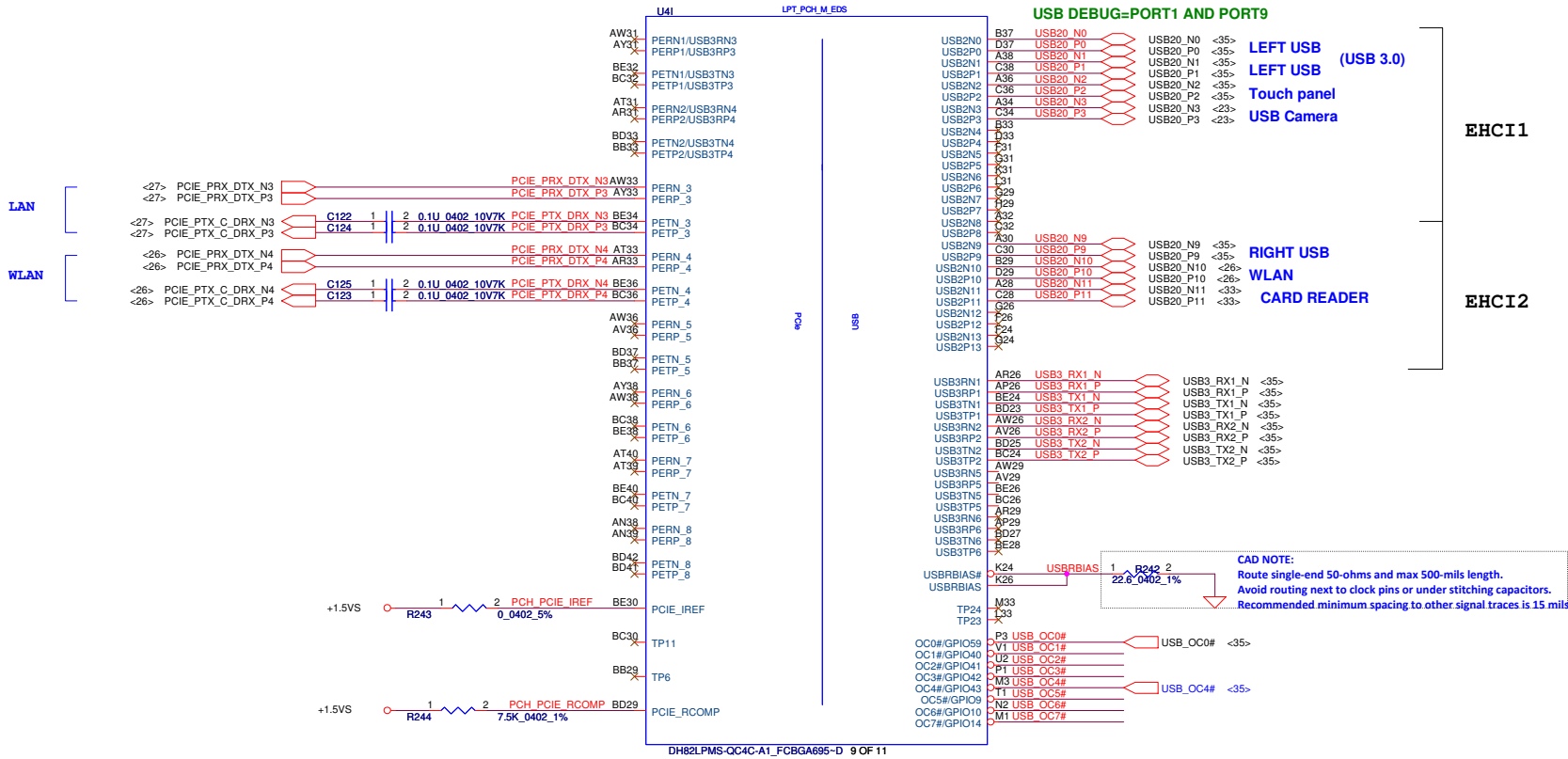
U7 Rersver 4M+2M Solution



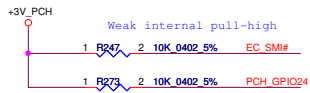
R124;c190 close to U4.T3 pin



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (4/9) LVDS,CRT,DP,HDMI	
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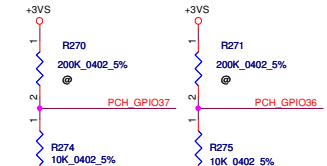
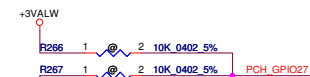
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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				Date: Wednesday, October 03, 2012	Sheet 17 of 60



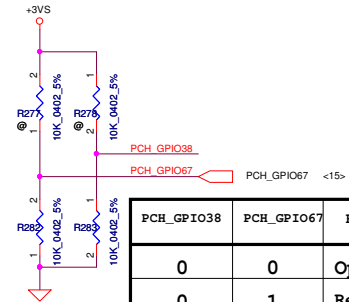
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable (Default)
L : On-Die PLL Voltage Regulator disable



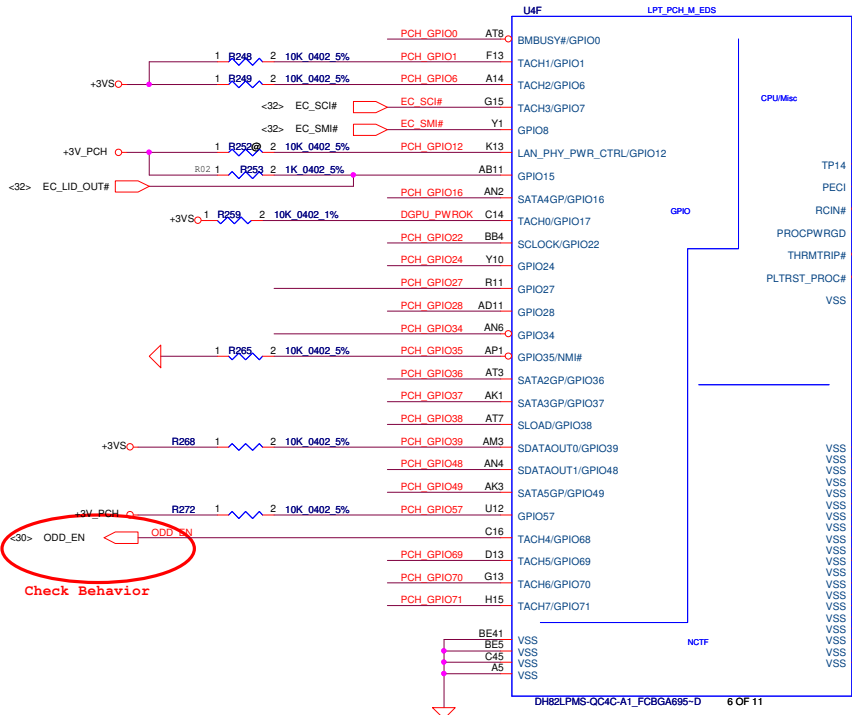
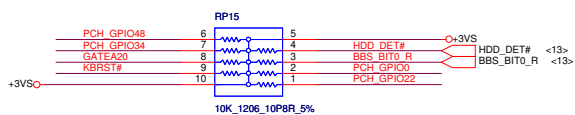
★ **PCH_GPIO27** (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA



Check Behavior

Check list require 1K pull high, CRB 100 ohm!

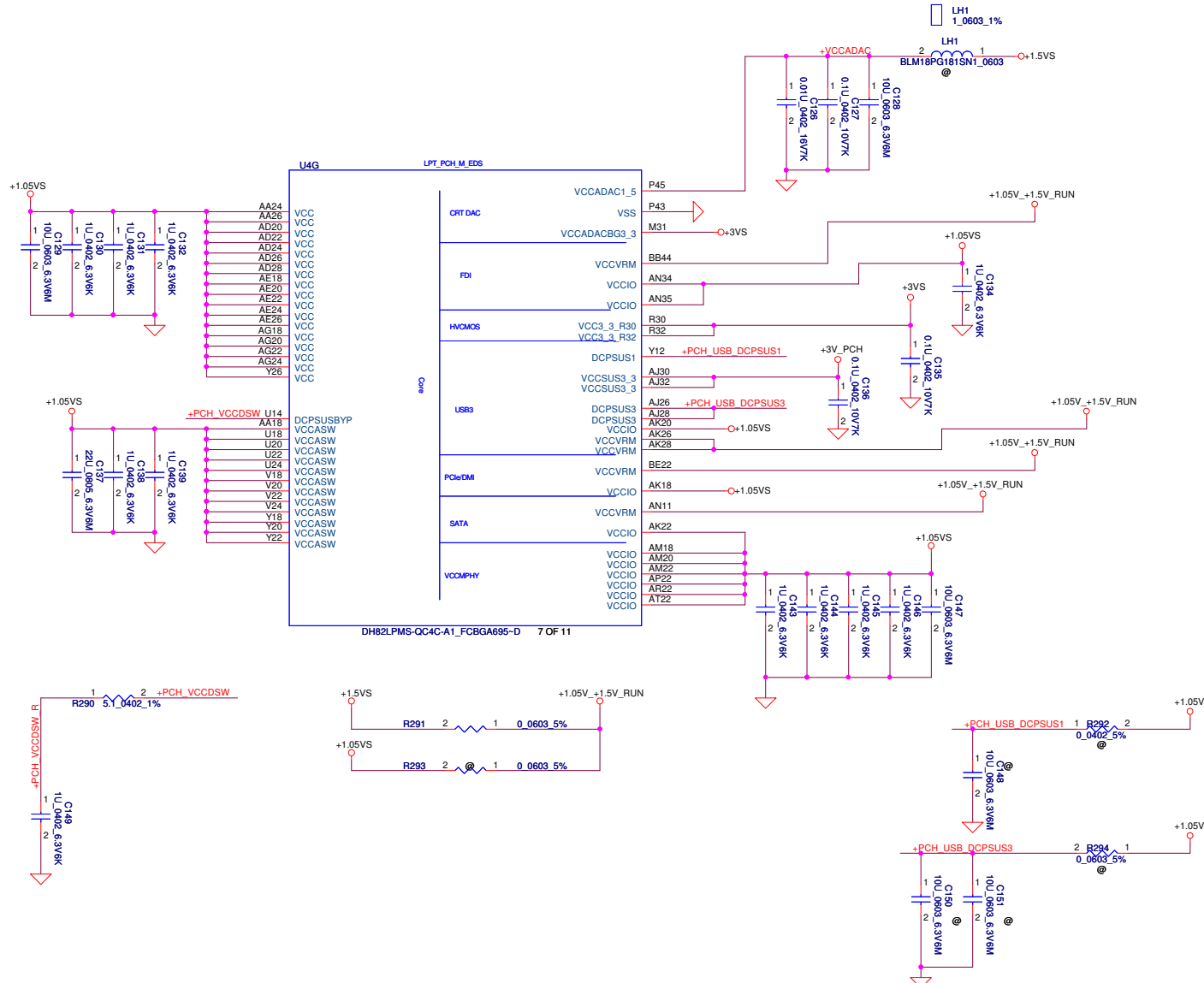
Need Update

Config	GPIO16 & 49
USB3.0 x4, PCIe x8, SATA x6	11
★ USB3.0 x6, PCIe x8, SATA x4	01

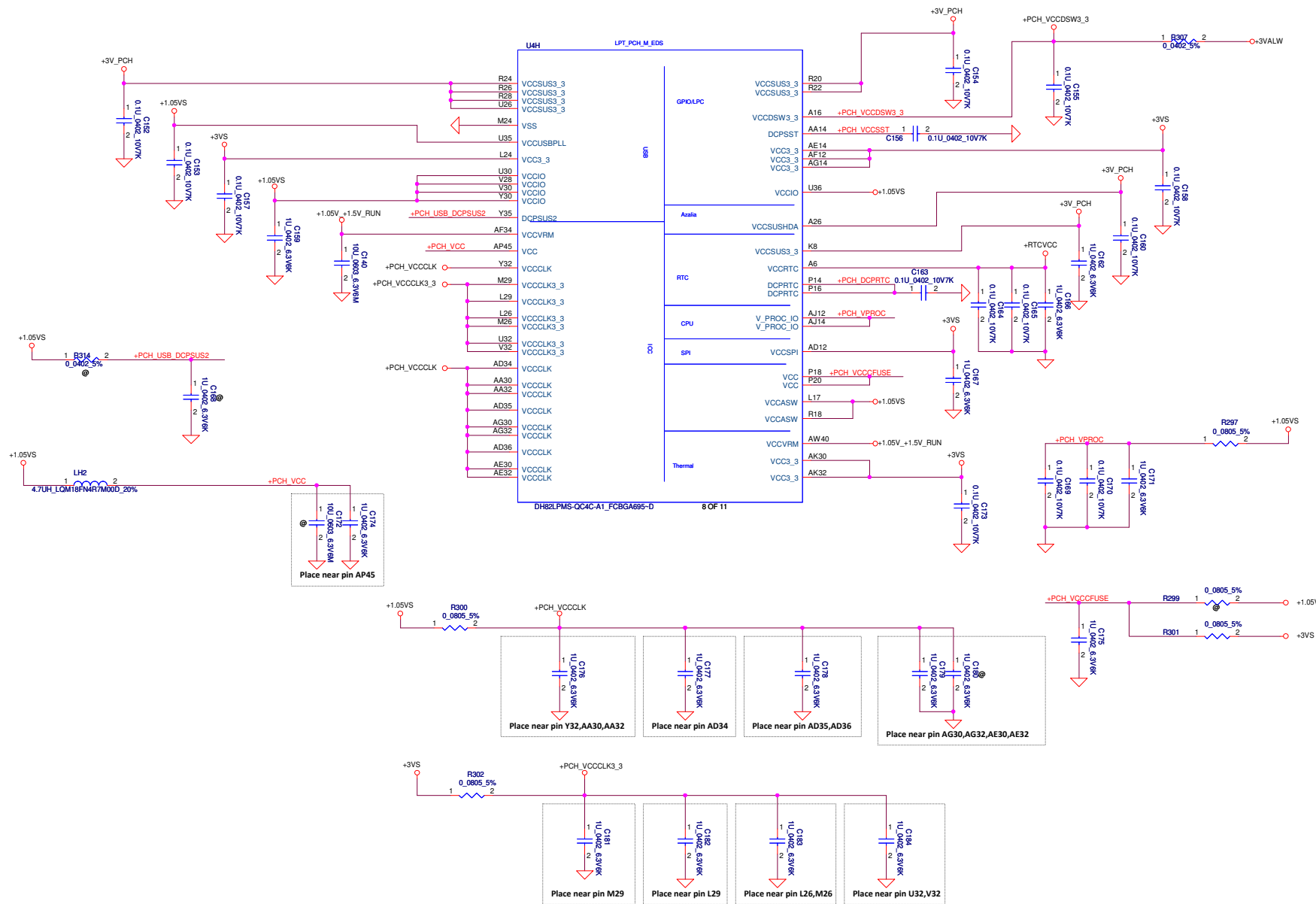
Fixed Signals			Muxed Signals		Fixed Signals			Muxed Signals		Fixed Signals						
USB3_1	USB3_2	USB3_5	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_9	SATA_1	SATA_2	SATA_3
(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)

PCH_GPIO69	Function
0	
1	

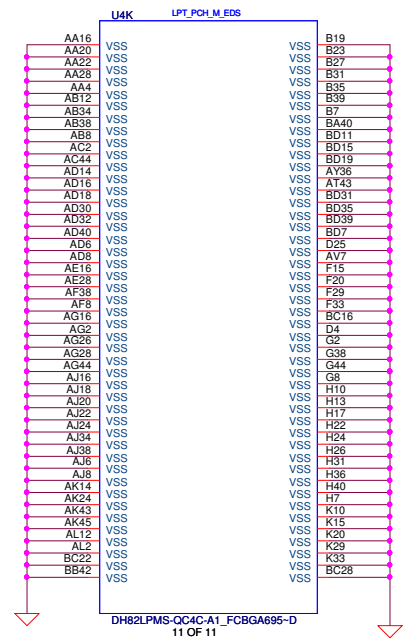
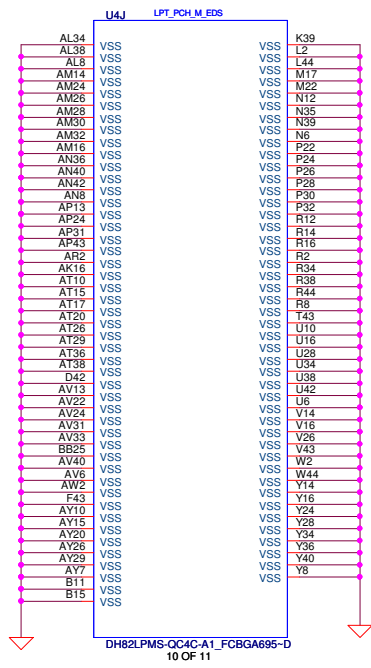
PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	
1	



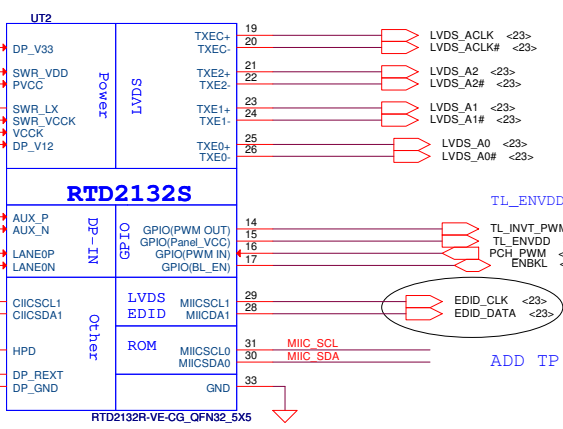
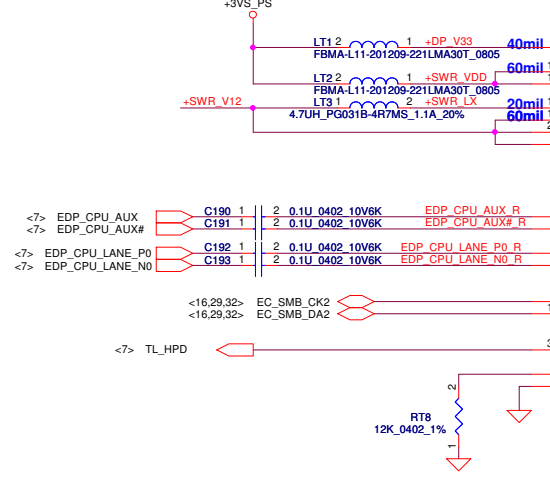
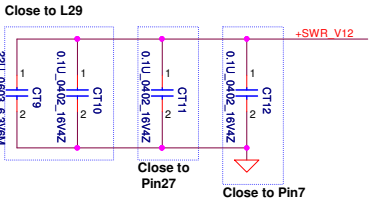
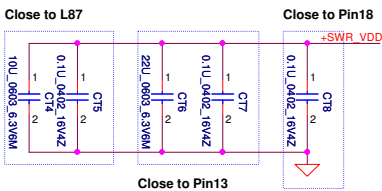
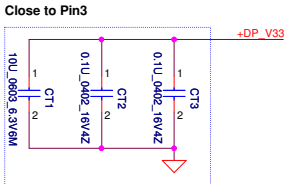
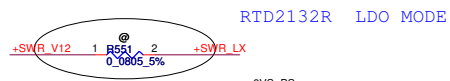
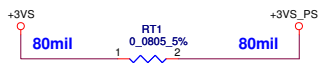
PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVCRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

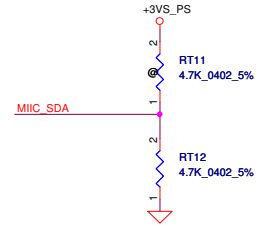
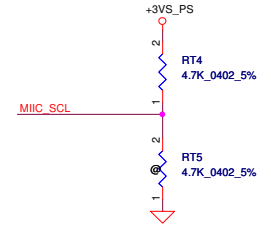
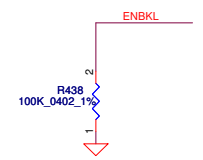
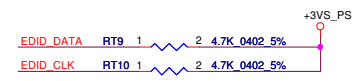


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Date: Wednesday, October 03, 2012				Sheet	21 of 60



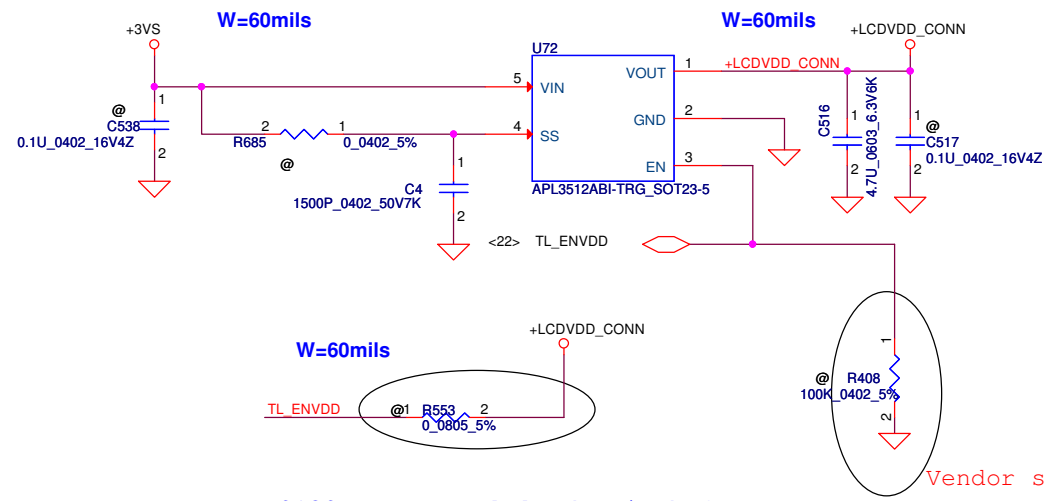
TL_ENVDD need 40 mil if use for LVDS power on R version

ADD TP on trace or via

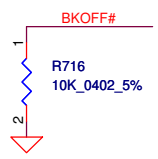


	MIIC_SDA	0	1
MIIC_SCL		X	EC CODE
		Internal ROM	EEPROM

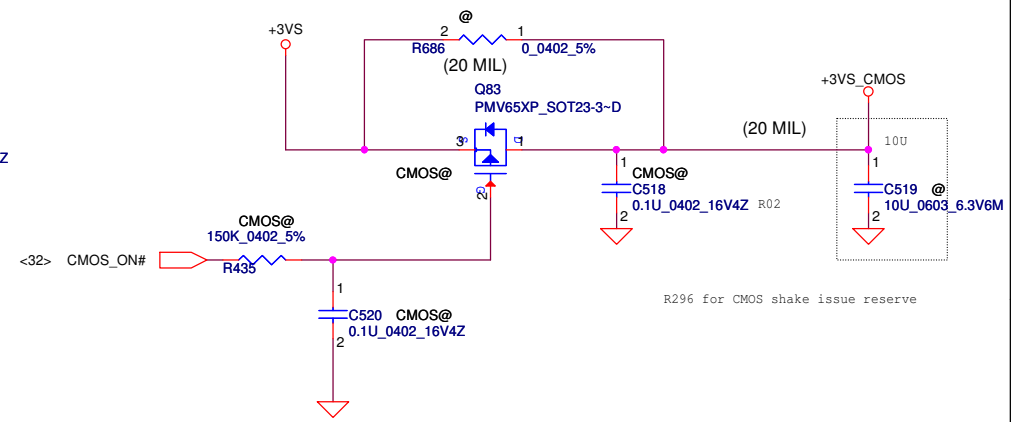
LCD POWER CIRCUIT



RTD2132R Internal load switch for +LCD_VCC

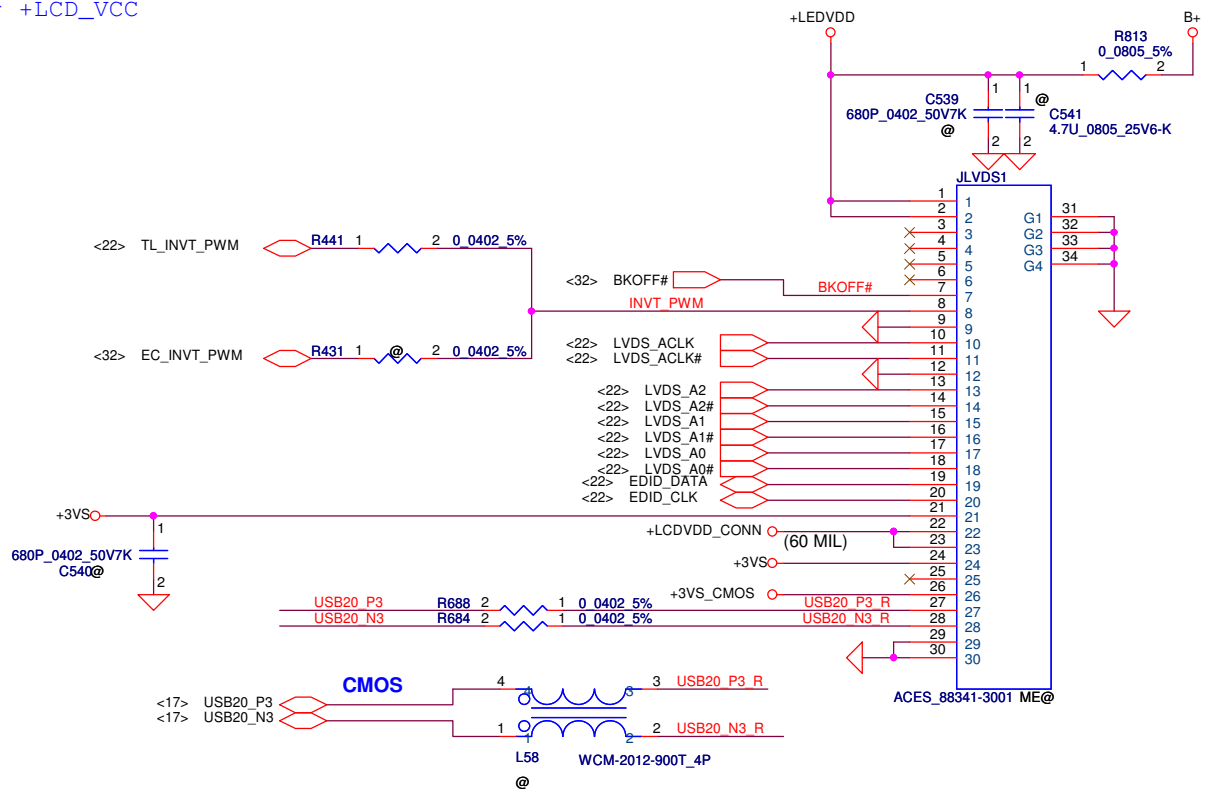


CMOS Camera



R296 for CMOS shake issue reserve

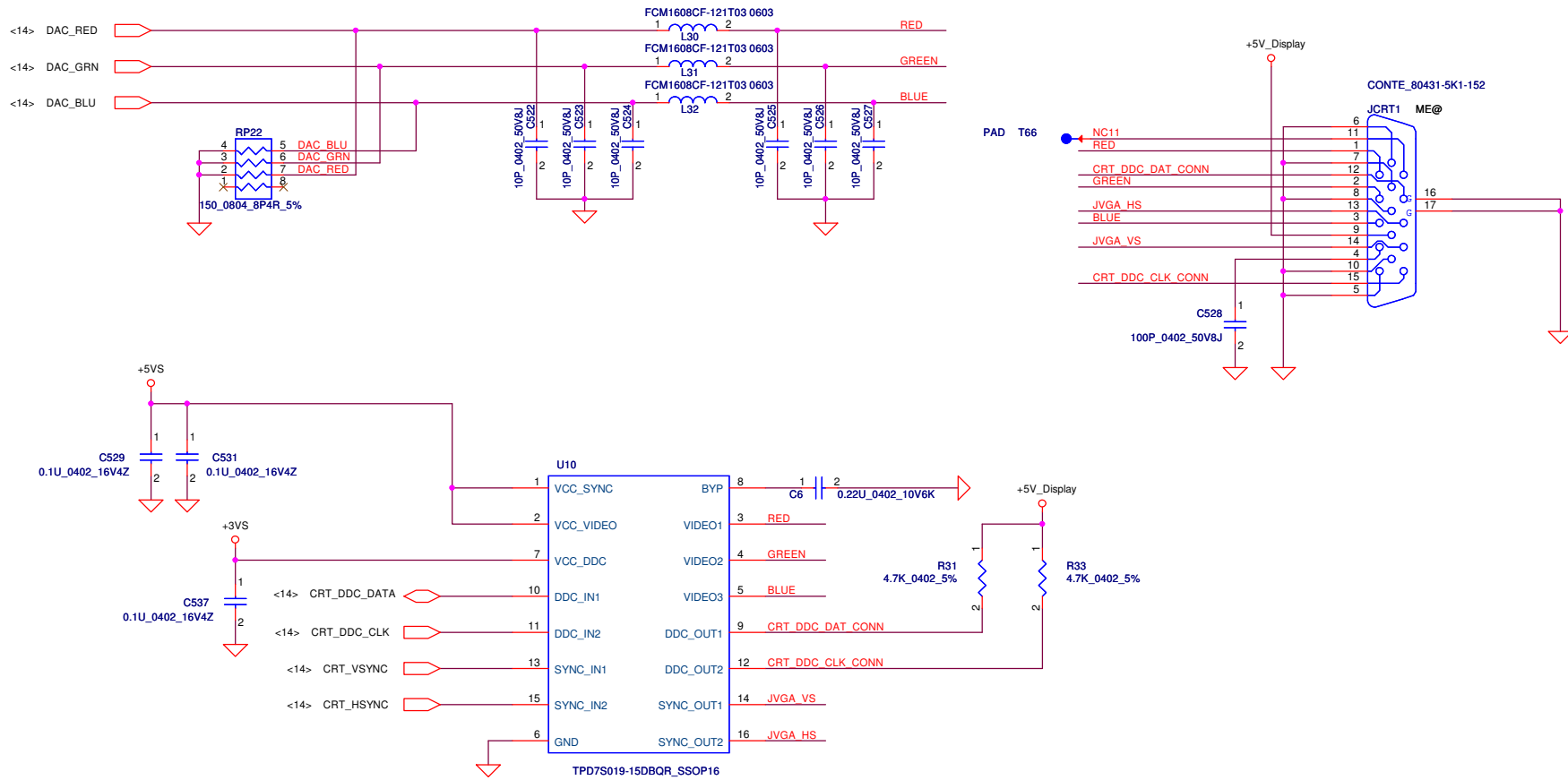
VGA LCD/PANEL BD. Conn.



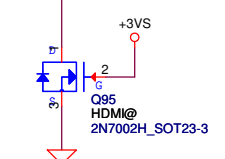
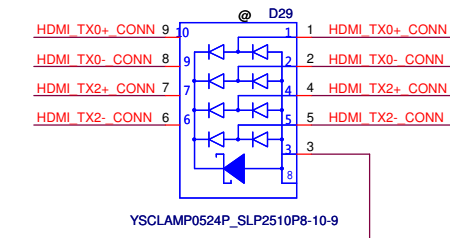
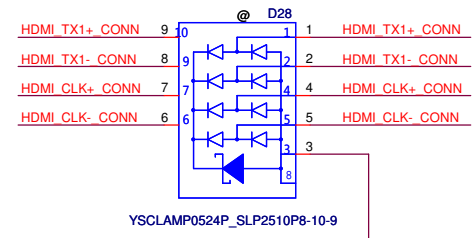
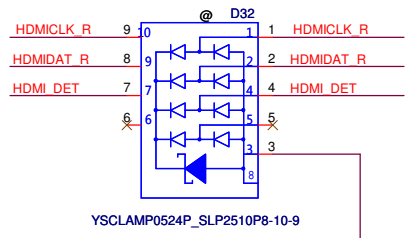
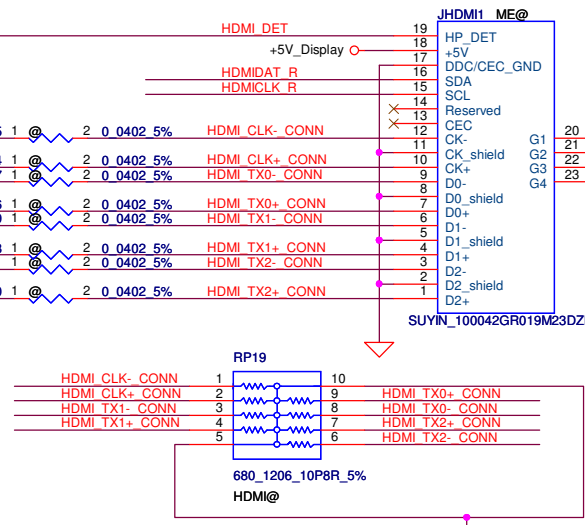
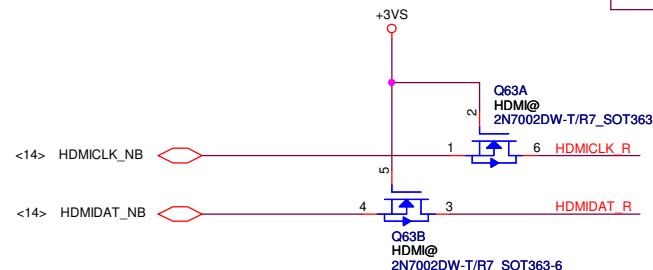
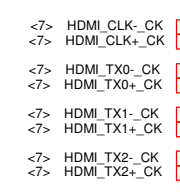
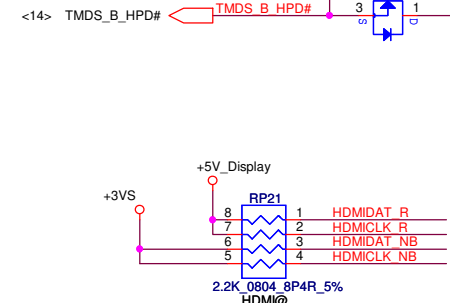
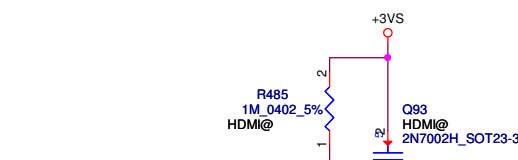
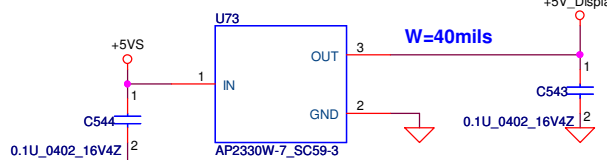
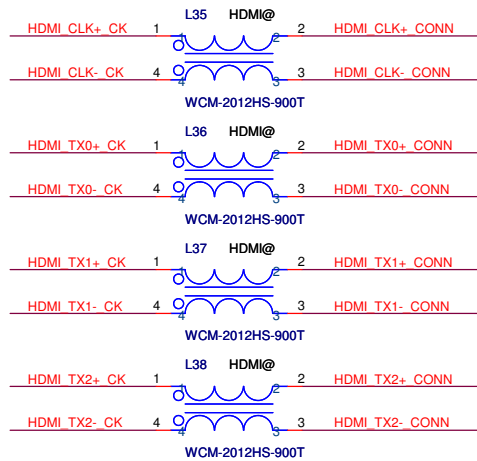
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		2012/07/11
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		LVDS/CAMERA	
Size	Document Number	Rev	
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CRT Connector

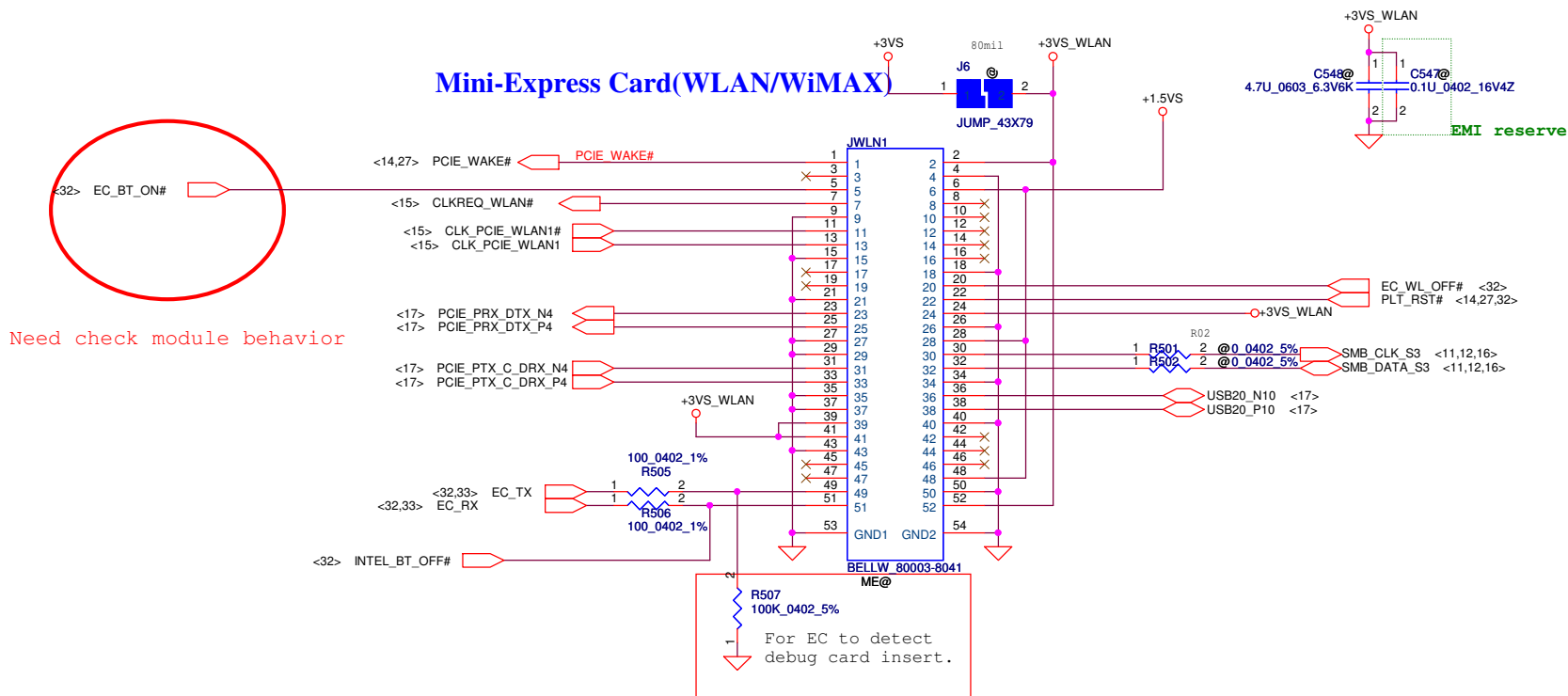


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Size	Custom	Document Number	LA-9641P	Rev	2.0
Date:	Wednesday, October 03, 2012	Sheet	24	of	60

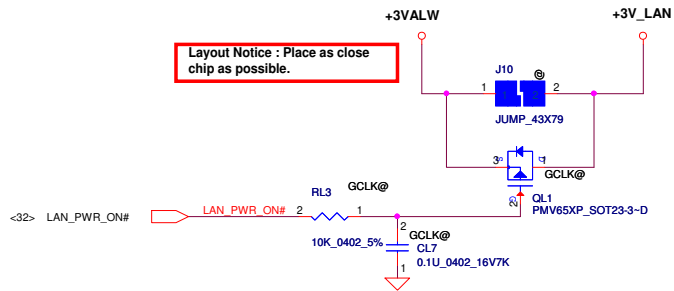


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				Date: Wednesday, October 03, 2012	Sheet 25 of 60

Mini-Express Card for WLAN/WiMAX(Half)

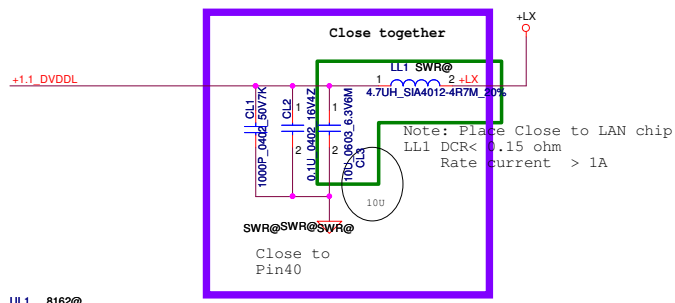
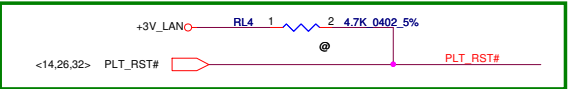


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title Mini-Card/NEW Card/SIM	
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				LA-9641P	
Date: Wednesday, October 03, 2012				Sheet	26 of 60



Layout Notice : Place as close chip as possible.

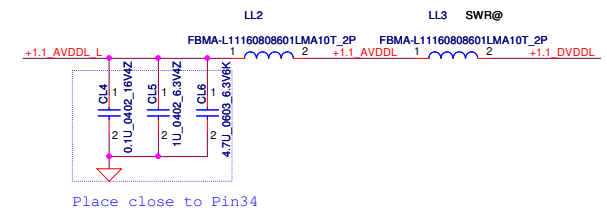
Vendor recommend reseve the PU resistor close LAN chip



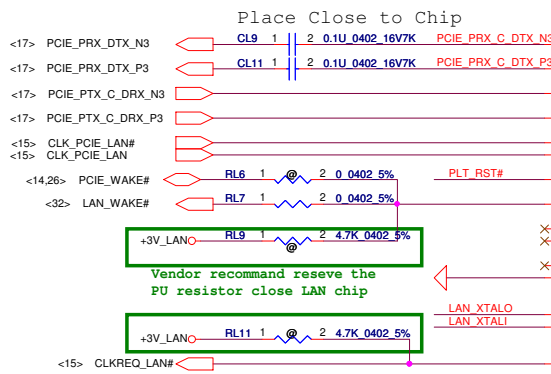
Note: Place Close to LAN chip
LL1 DCR < 0.15 ohm
Rate current > 1A



SA000065400 S IC QCA8172-AL3A-R QFN 40P E-LAN CTRL
SA000052J10 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL

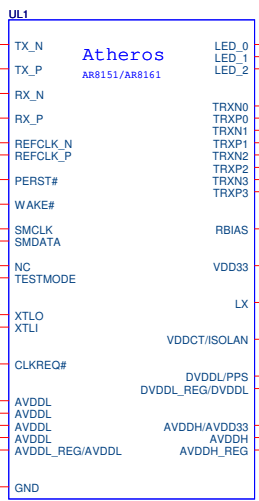


Place close to Pin34



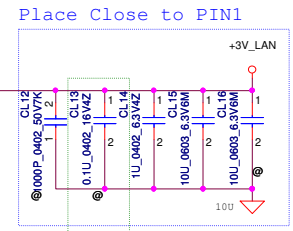
Place Close to Chip

Vendor recommend reseve the PU resistor close LAN chip

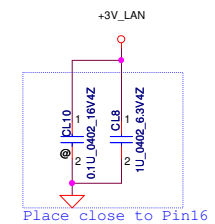


mount RL12 if use LDO modue

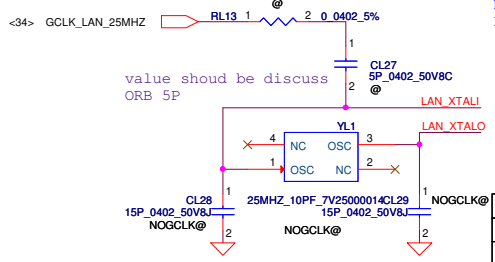
Place Close to PIN1



EMI reserve



Place close to Pin16

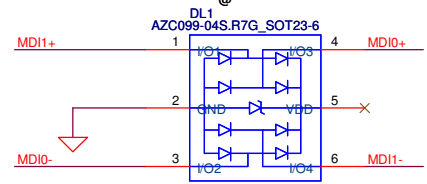


value should be discuss ORB 5P

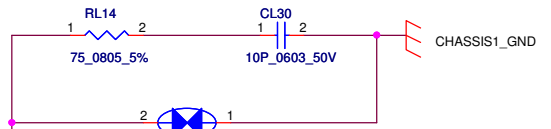
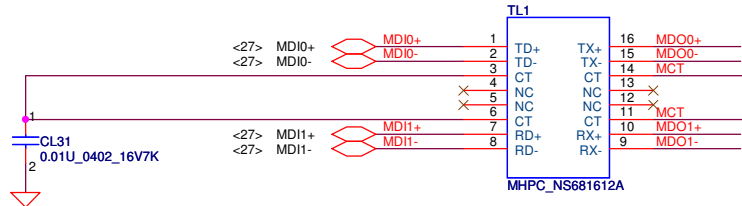
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	LAN-AR8162/8172	
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Date:	Wednesday, October 03, 2012	Sheet	27	of	60

DL1
 1'S PN:SC300001G00
 2'S PN:SC300002E00

Place Close to TL1

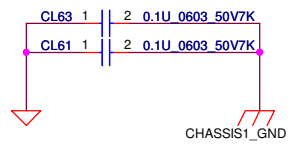


Reserve gas tube for EMI go rural solution

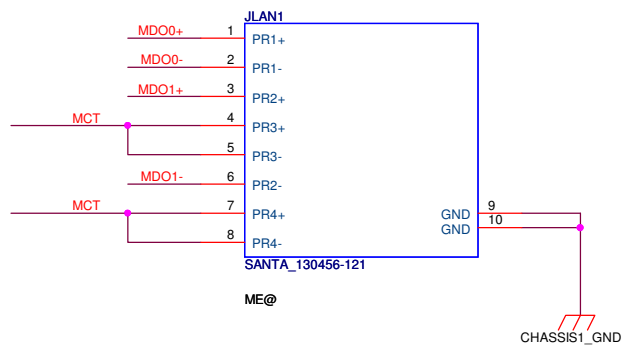


Place Close to TL1

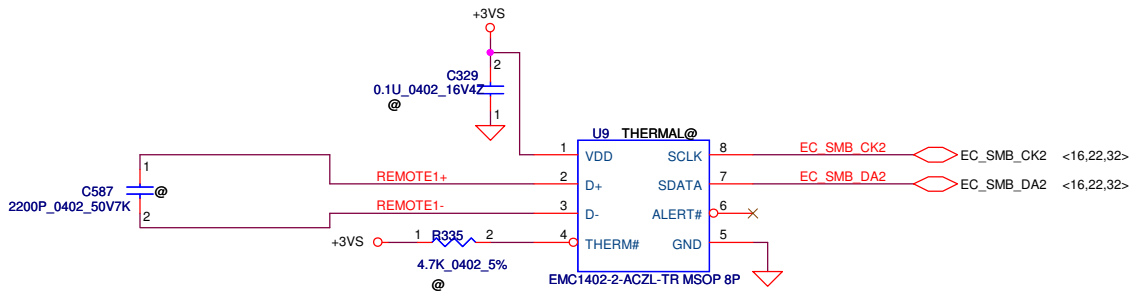
DLL1
 BS4200N-C-LV_SMB-F2
 GAS@



Need check Symbol

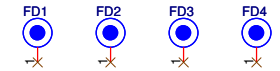
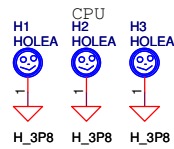


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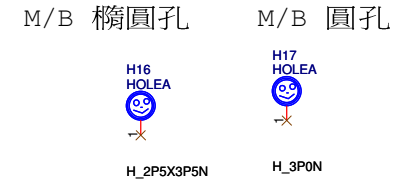
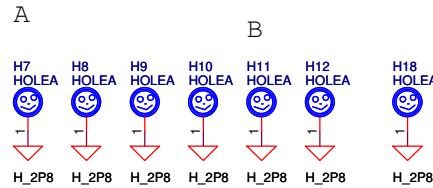
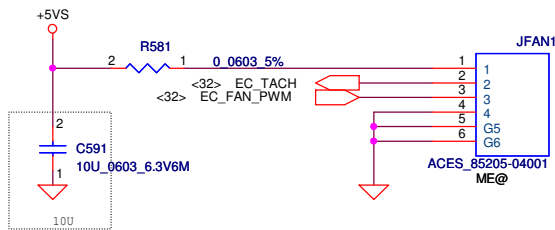


EMC1412-A (SA00003YA00)
 Address 1111_100xb
 SIC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1, 2+/-:
 Trace width/space: 10/10 mil
 Trace length: <8"



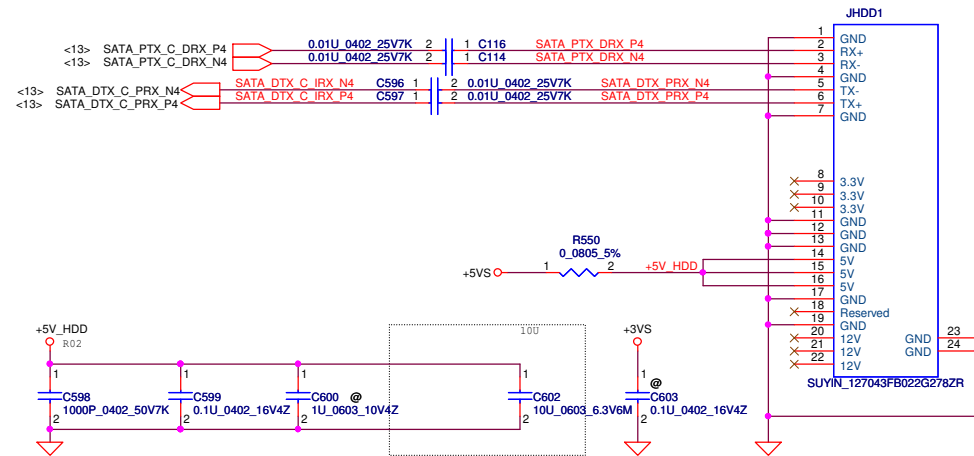
FAN1 Conn



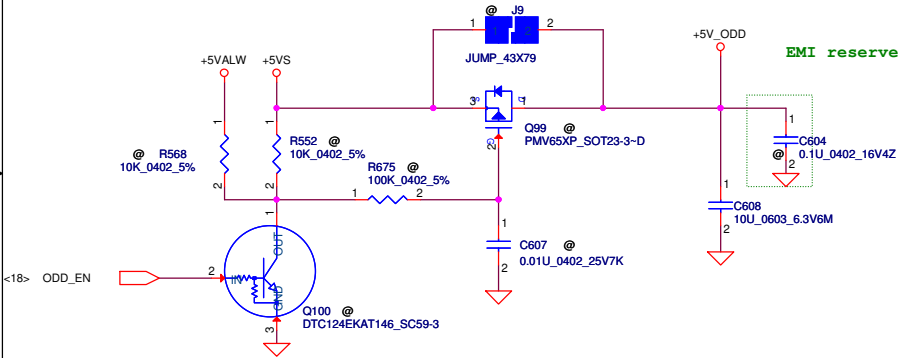
2P8 * 7 pcd

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				Date:	Wednesday, October 03, 2012
				Sheet	29 of 60
				Rev	2.0

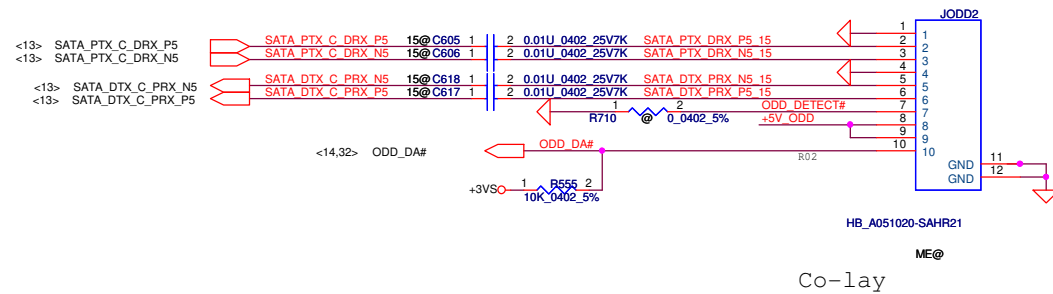
SATA HDD Conn.



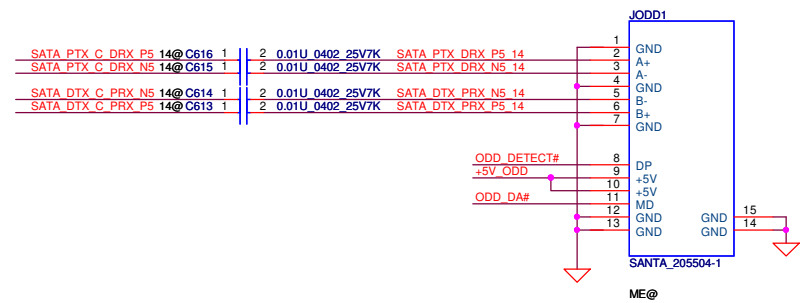
ODD Power Control



FOR 15" SATA ODD FFC Conn.

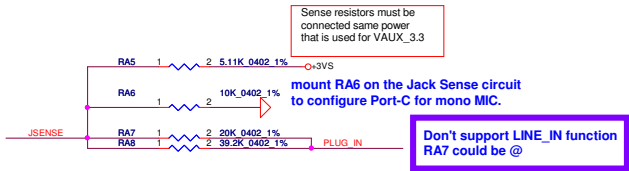


FOR 14" SATA ODD Conn.

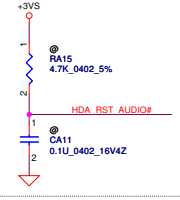


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Size	Document Number	LA-9641P		Filev	2.0	
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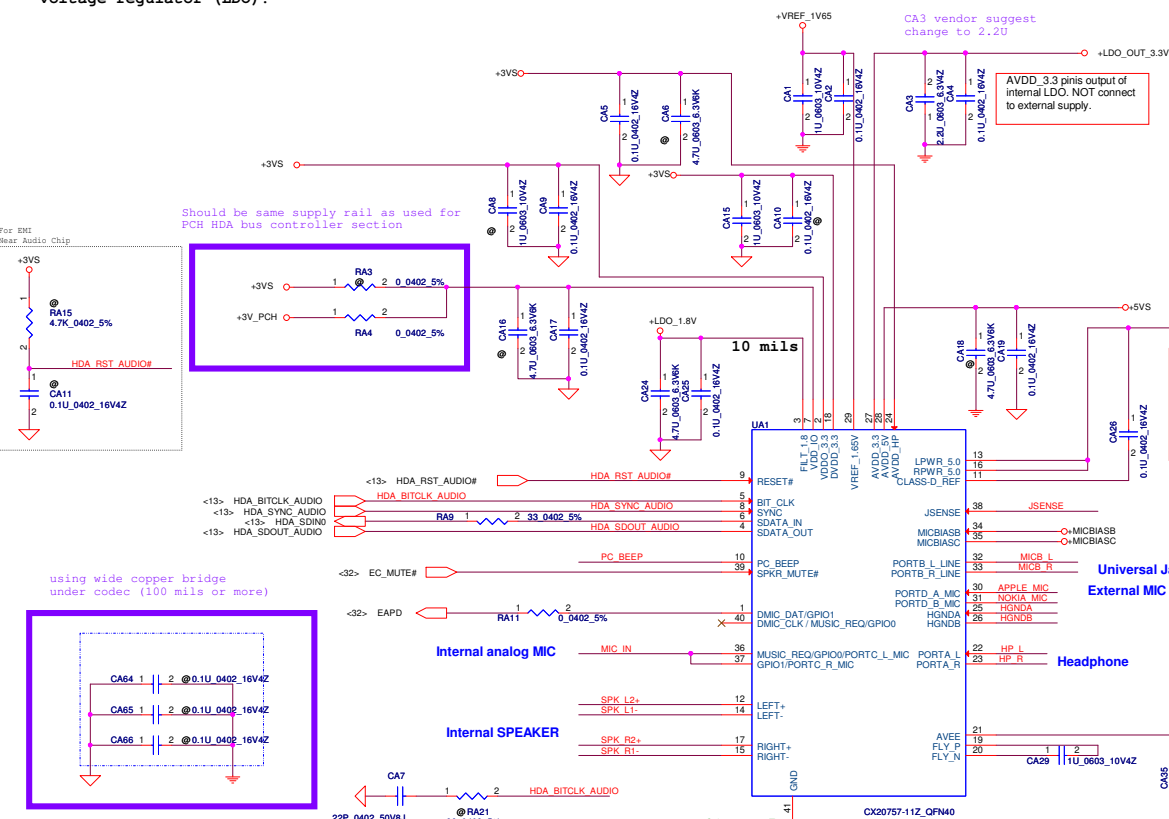
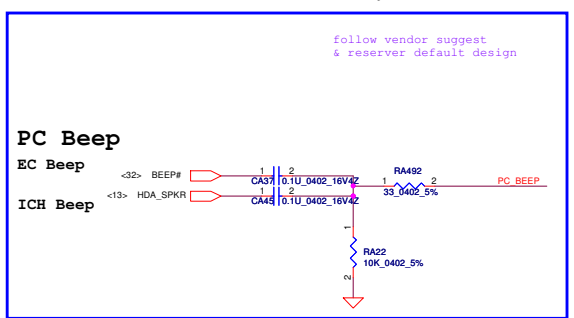
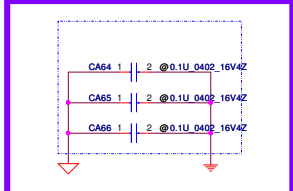
CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



For EMI
 Near Audio Chip

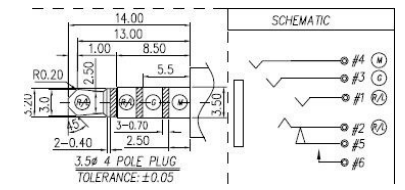


using wide copper bridge
 under codec (100 mils or more)



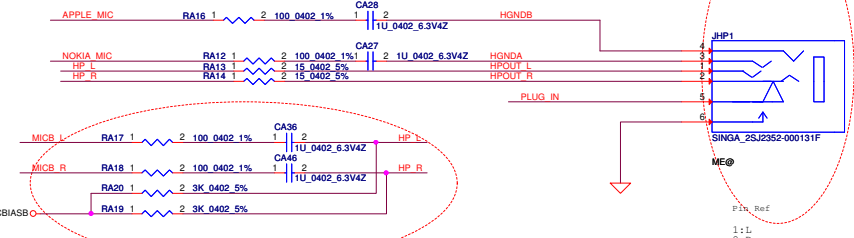
Layout Note: Path from +5VS to LPWR_5.0
 RPWR_5.0 must be very low
 resistance (<0.01 ohms)

Please bypass caps very close to device.



Check footprint

HGND, HGND 80mils



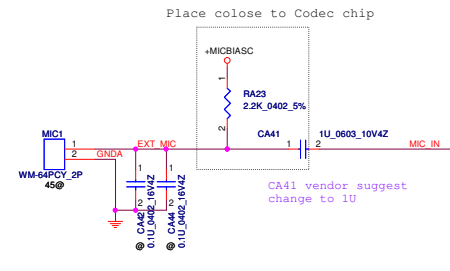
for Universal jack

CA30 vendor suggest
 change to 2.2U

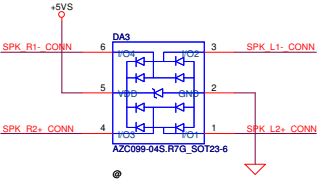
LA1-LA4 vendor suggest mount 0 ohm first-
 Bead reserve for EMI if needed

wide 20MIL

vendor suggest
 change to 1000p



Place colose to Codec chip



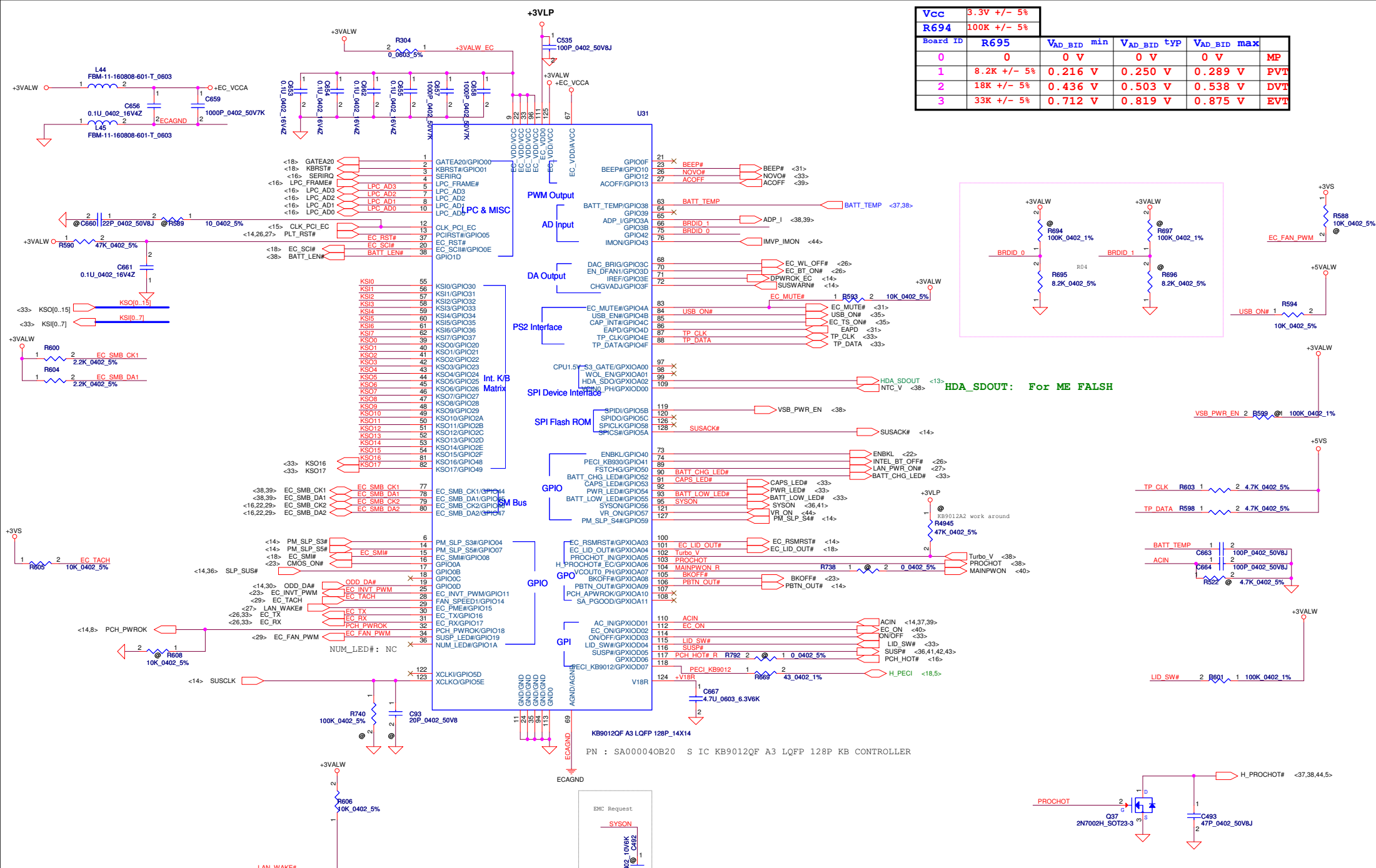
Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	CX20751 Codec
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Compal Electronics, Inc.

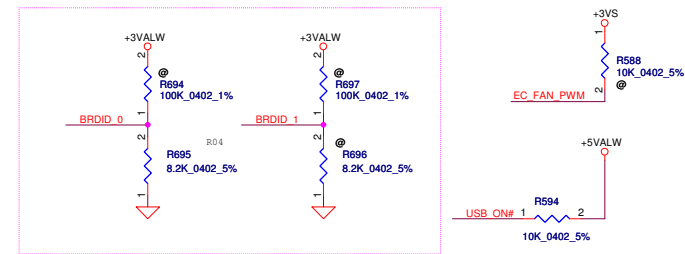
CX20751 Codec

LA-7982P

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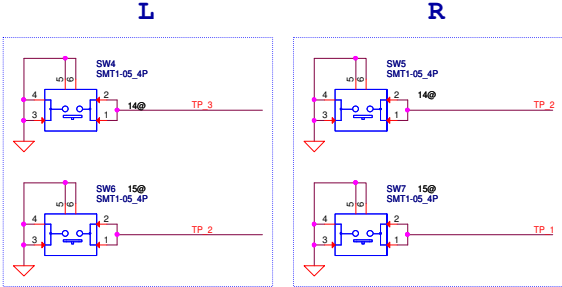
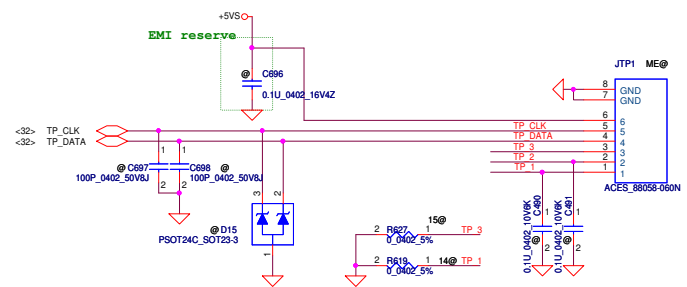
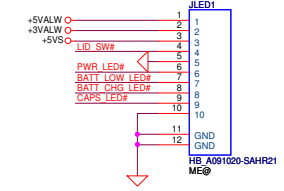
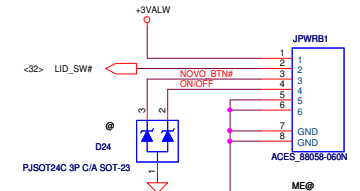
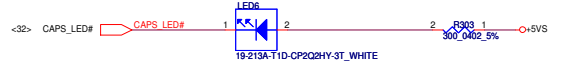
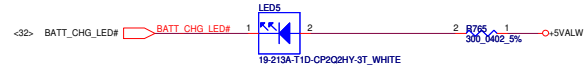
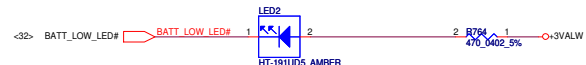
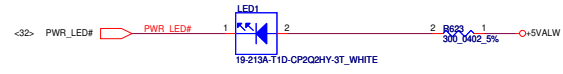
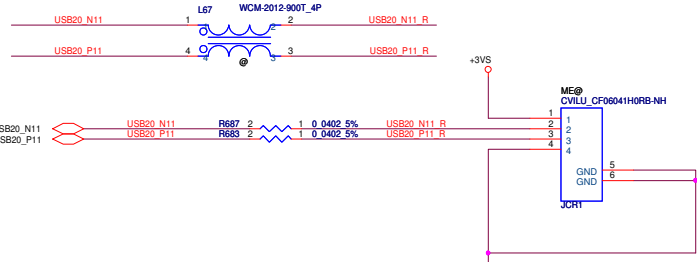
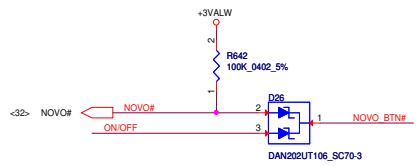
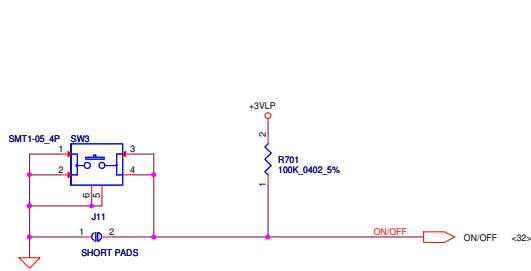
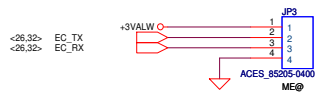
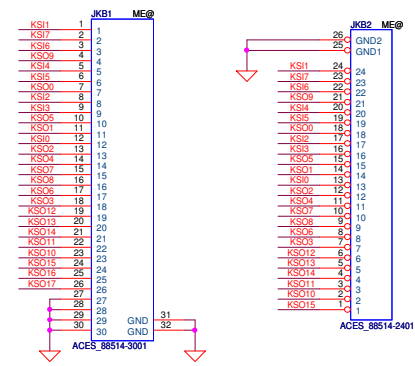
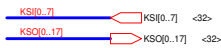
Vcc	3.3V +/- 5%							
R694	100K +/- 5%							
Board ID	R695	VAD_BID min	0 V	VAD_BID typ	0 V	VAD_BID max	0 V	MP
0	0	0.216 V	0.250 V	0.289 V	PVT			
1	8.2K +/- 5%	0.436 V	0.503 V	0.538 V	DVT			
2	18K +/- 5%	0.712 V	0.819 V	0.875 V	EVT			
3	33K +/- 5%							



HDA_SDOUT: For ME FALSH

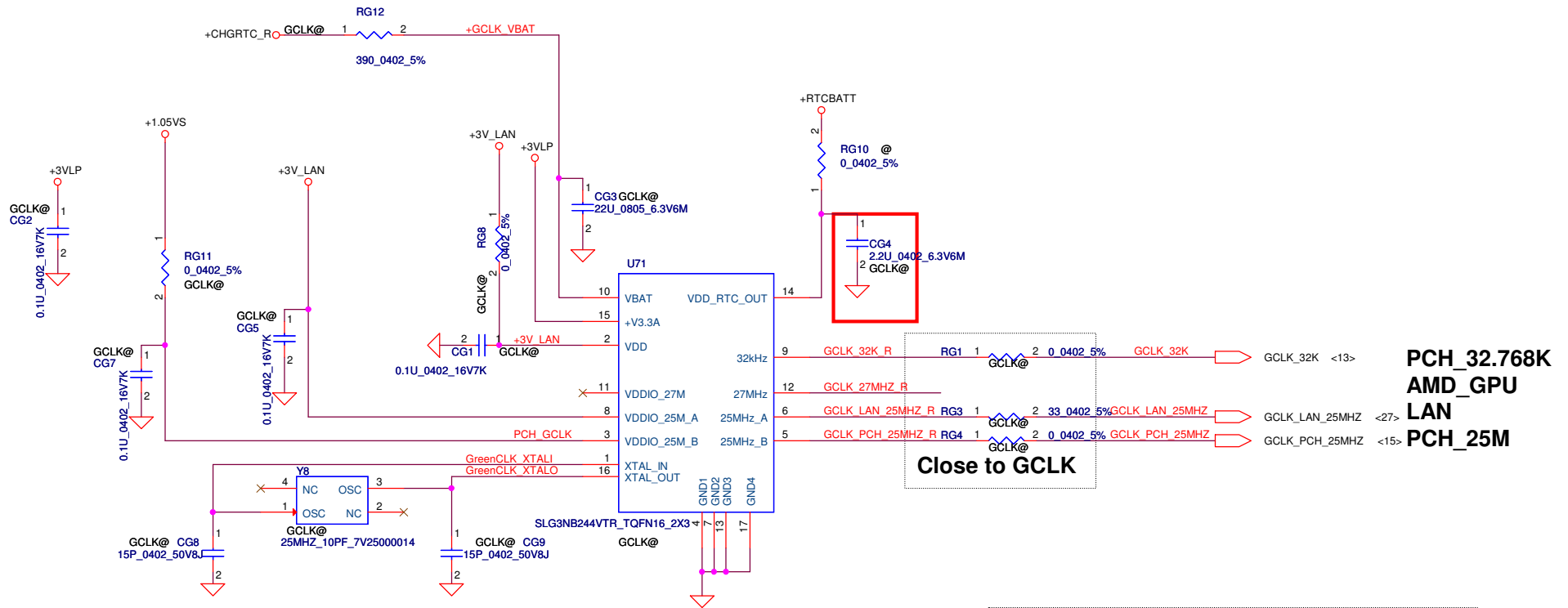
VSB_PWR_EN 2 R590 @ 100K 0.402 1%

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15"	14"
1 VCC	1 VCC
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 L
5 L	5 R
6 R	6 GND

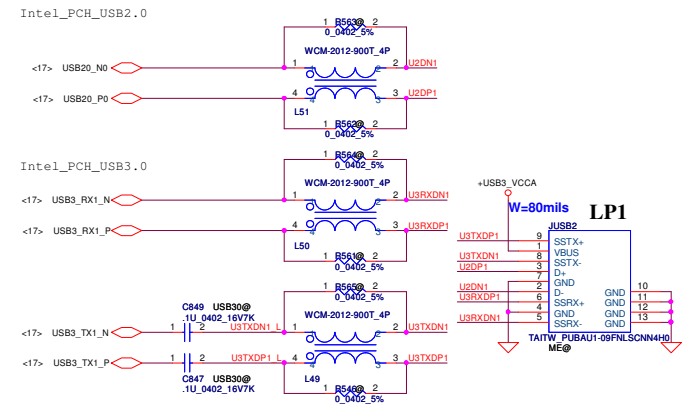
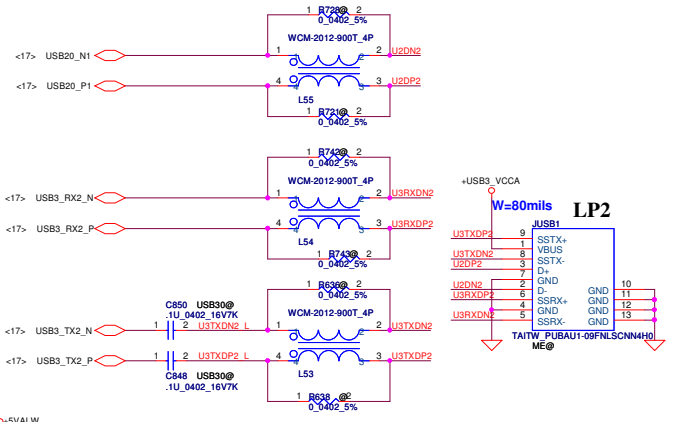
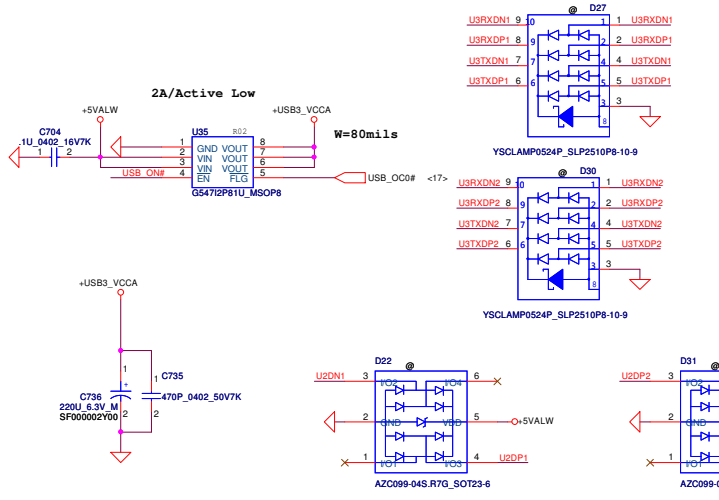
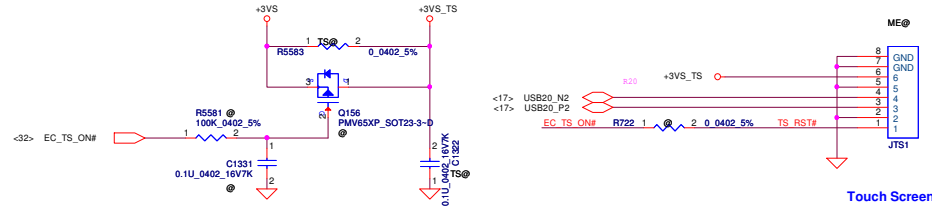
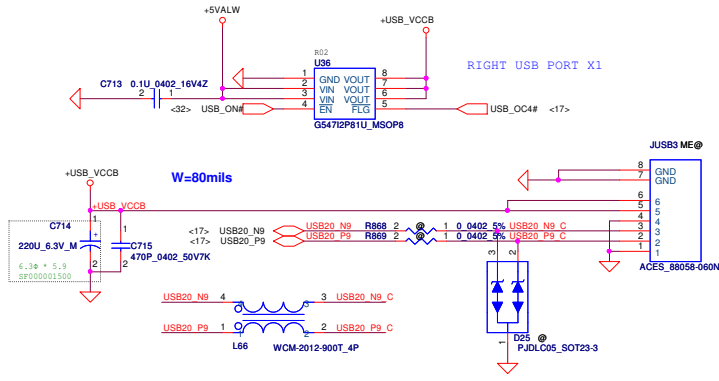
Green Clock



PCH_32.768K
AMD_GPU
LAN
PCH_25M

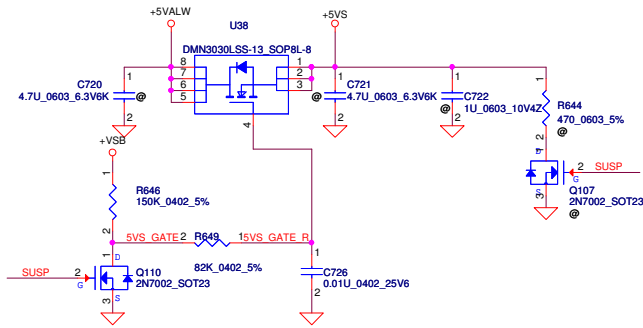
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title USB ext. ports		
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Right Ext.USB Conn.

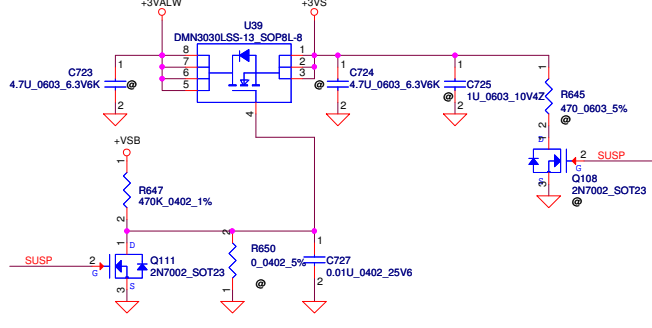


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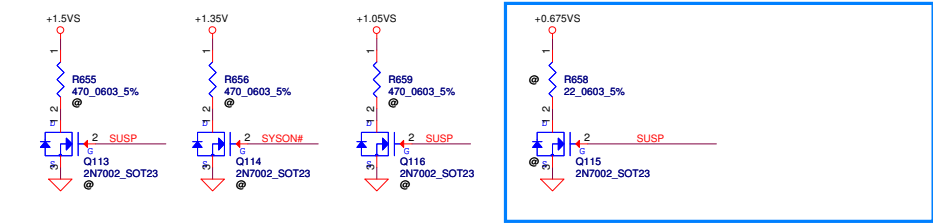
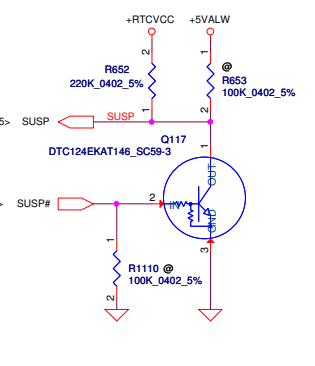
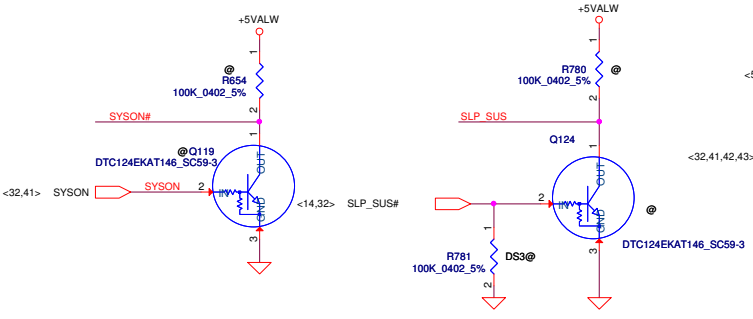
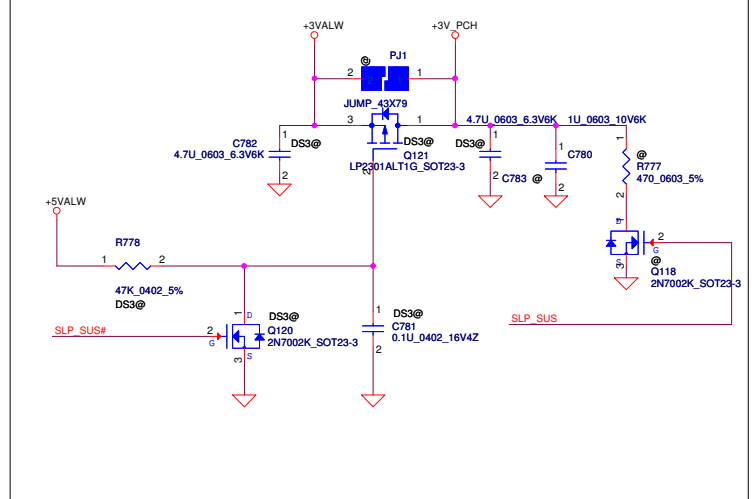
+5VALW TO +5VS



+3VALW TO +3VS



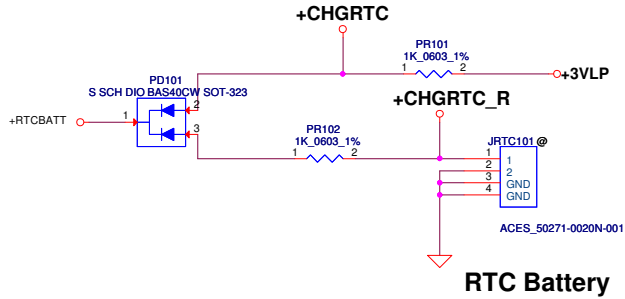
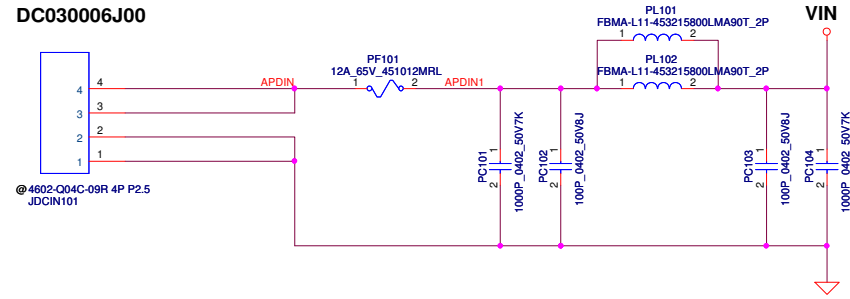
+3VALW TO +3VALW(PCH AUX Power)



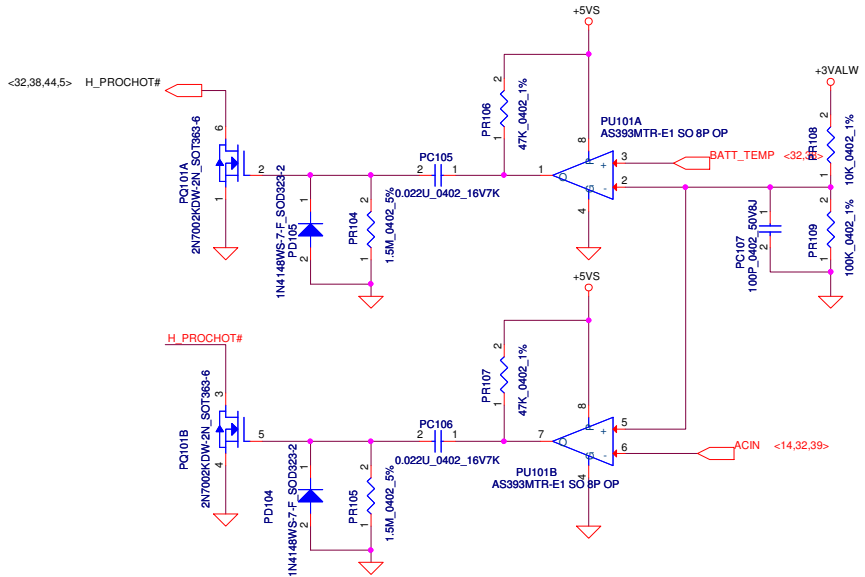
For Intel S3 Power Reduction.

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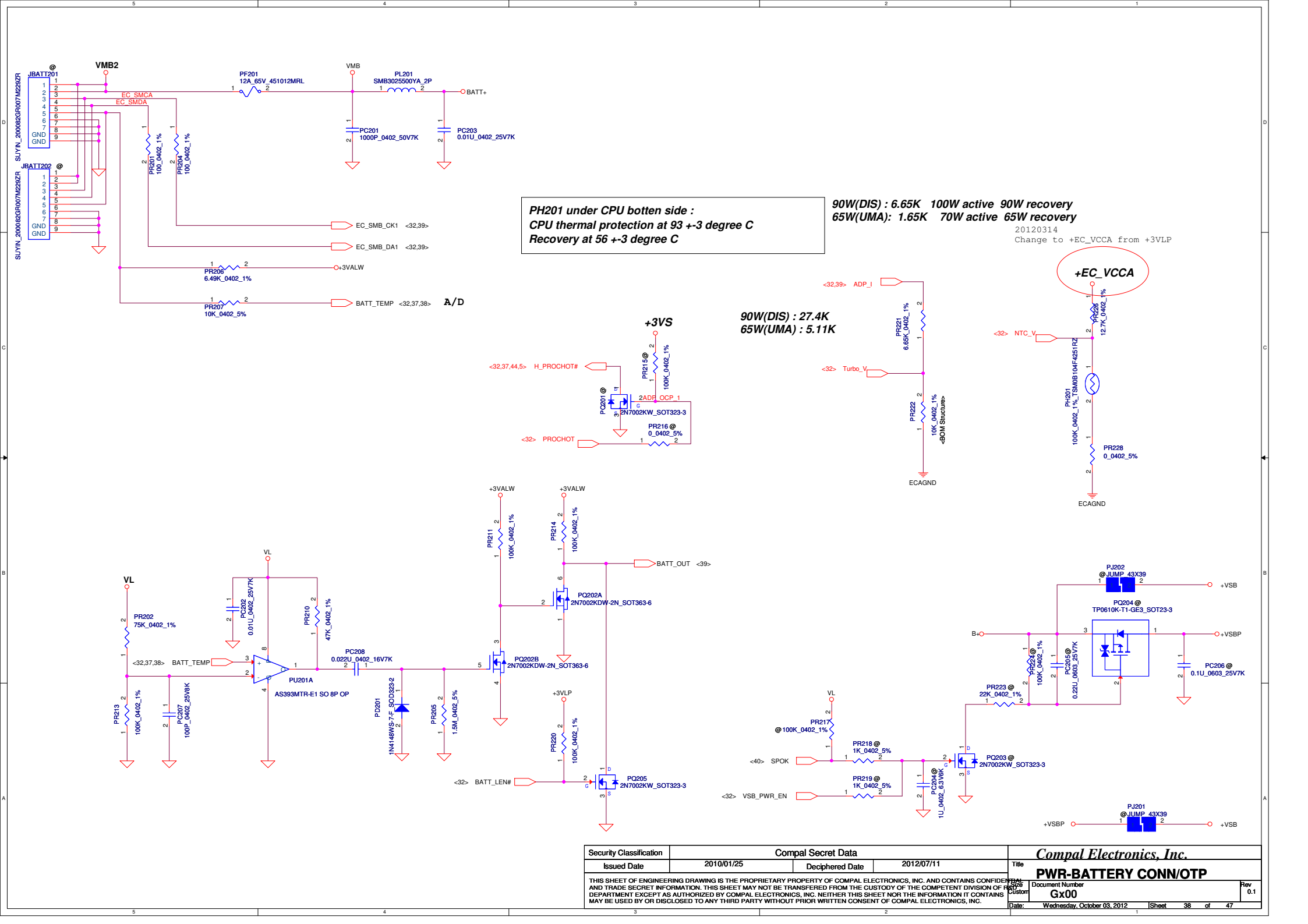
DC030006J00



RTC Battery



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PH201 under CPU bottom side :
CPU thermal protection at 93 +/- 3 degree C
Recovery at 56 +/- 3 degree C

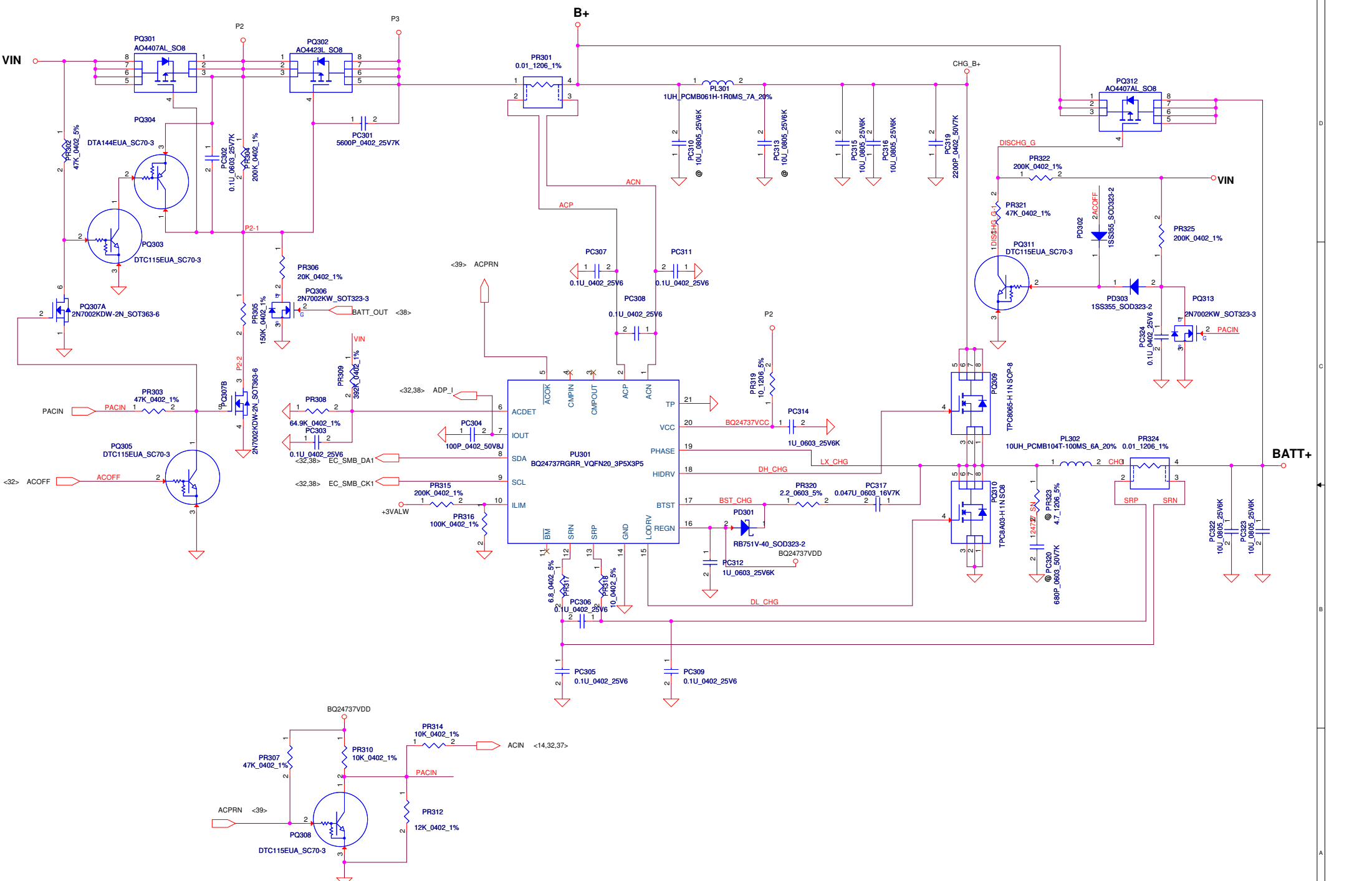
90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA) : 1.65K 70W active 65W recovery

20120314
 Change to +EC_VCCA from +3VLP

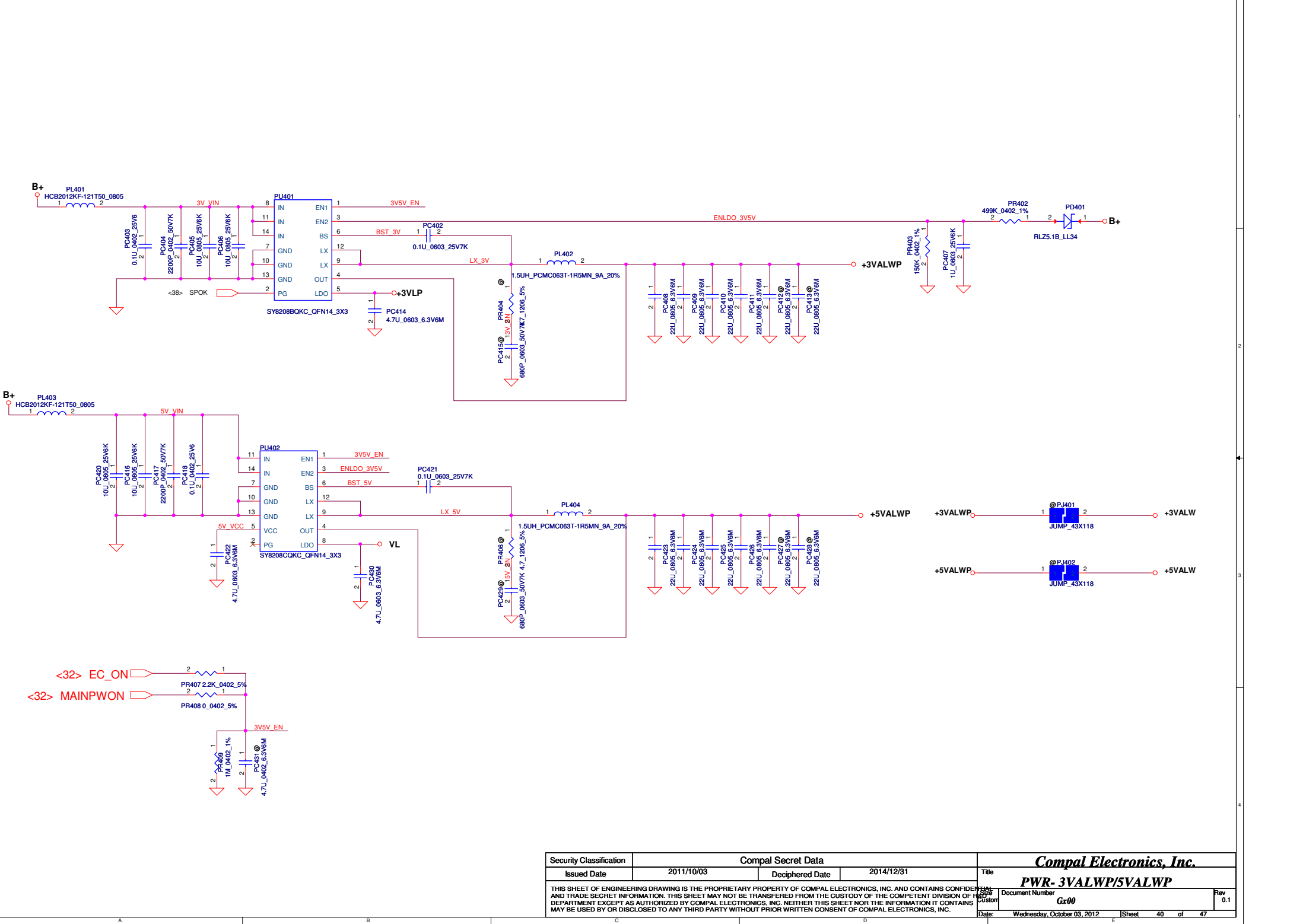
90W(DIS) : 27.4K
65W(UMA) : 5.11K

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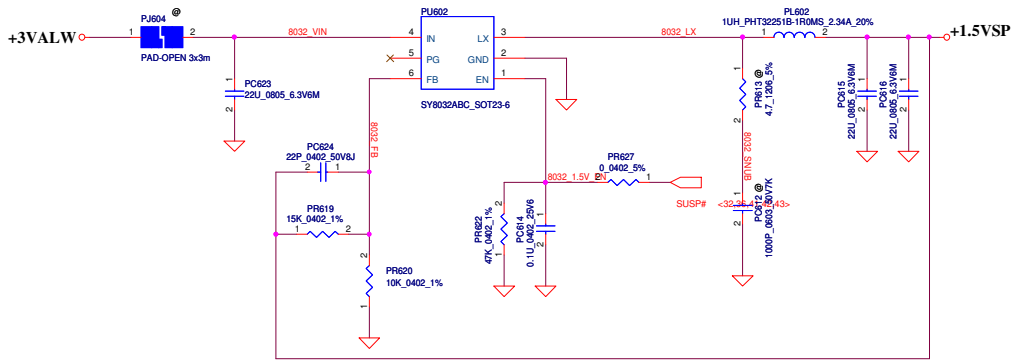
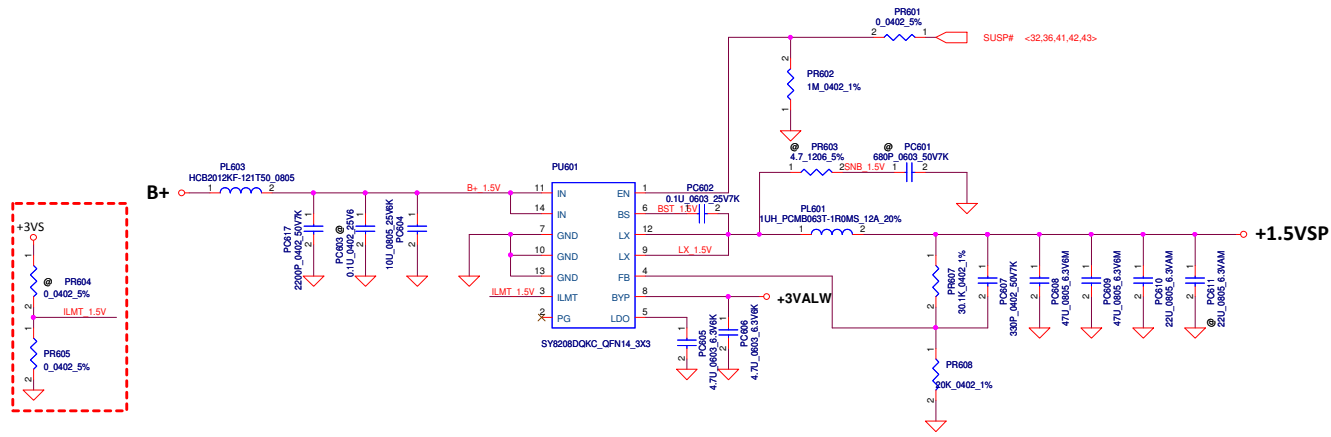
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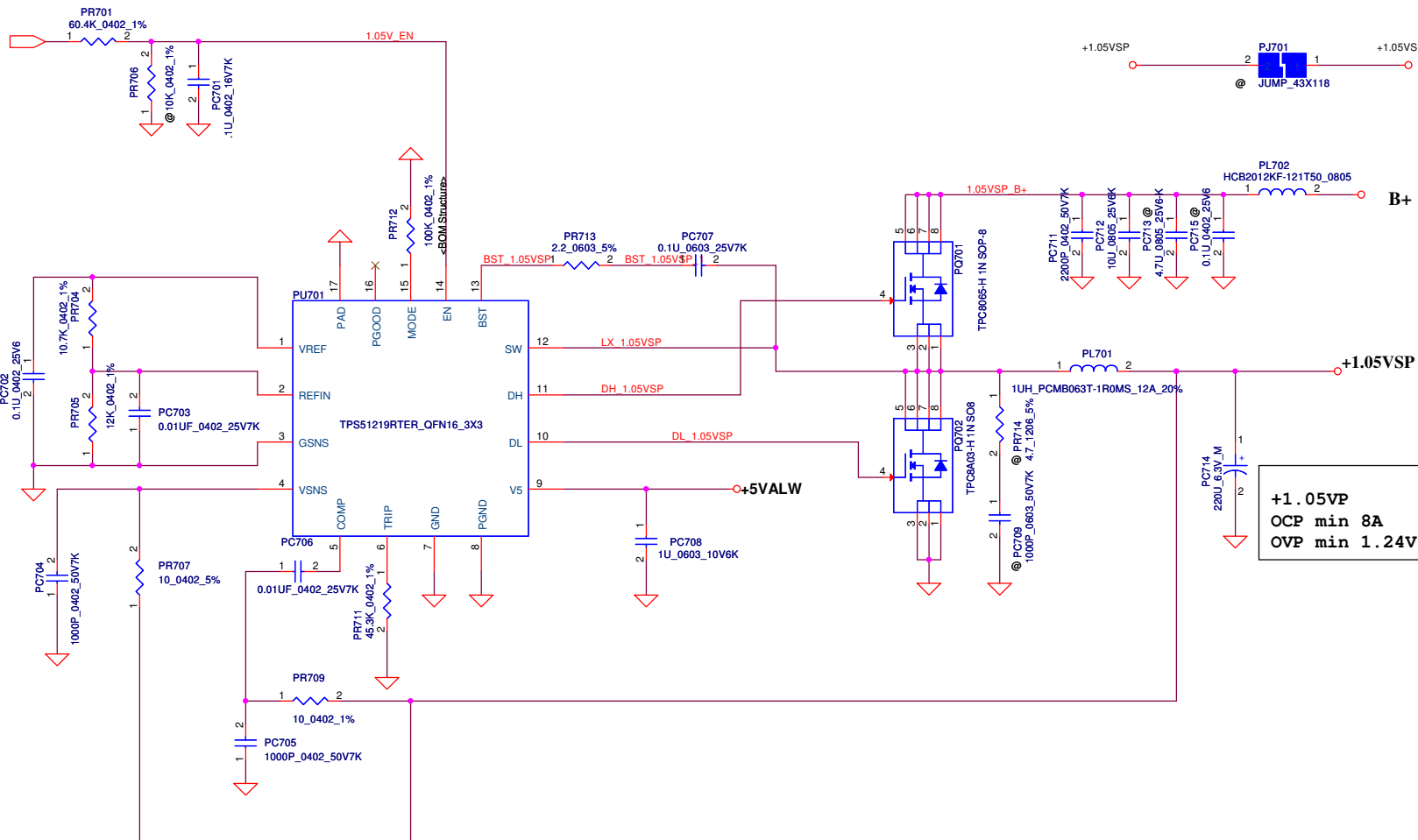


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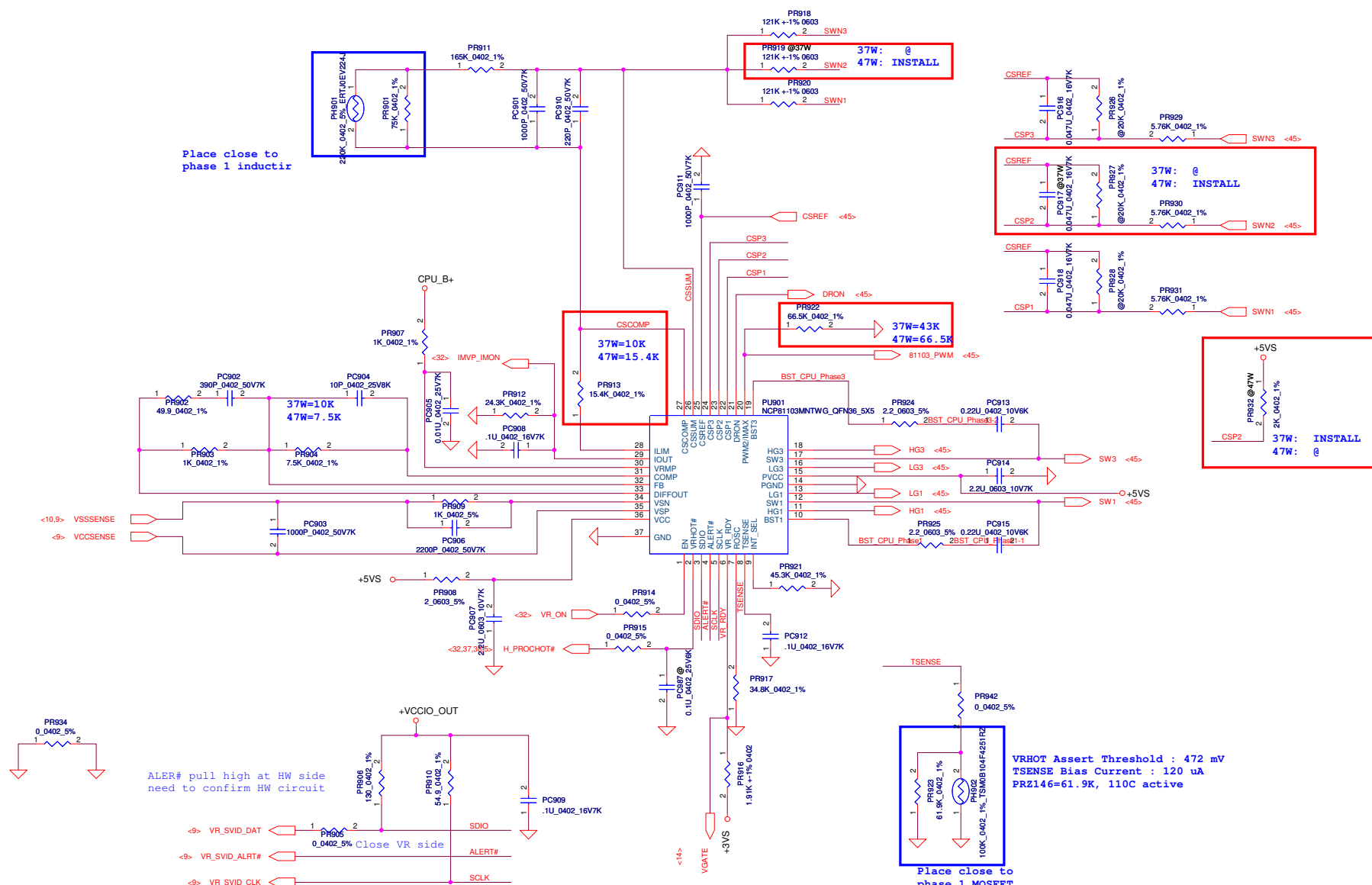


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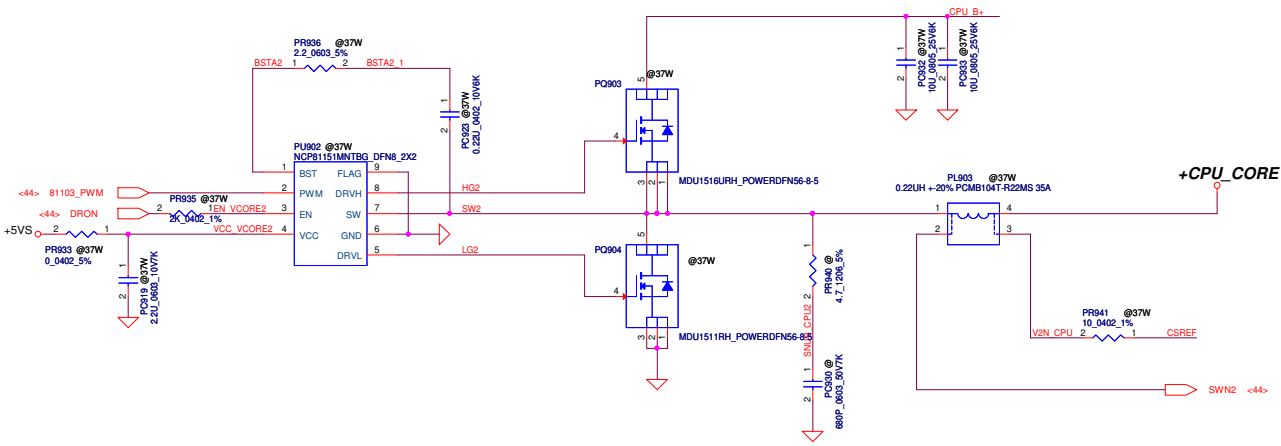
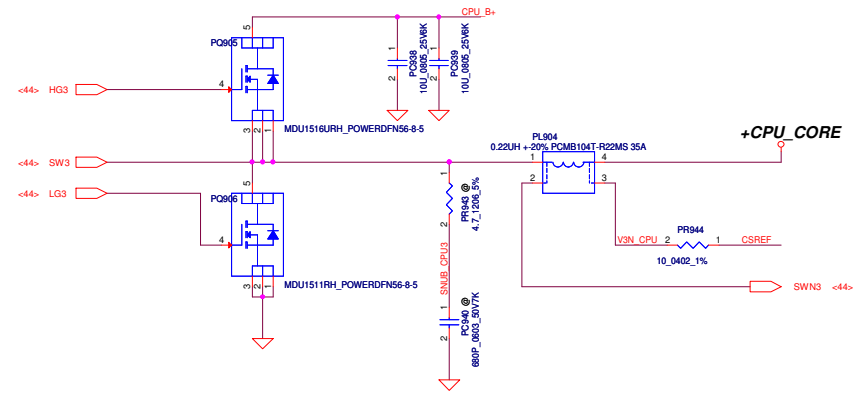
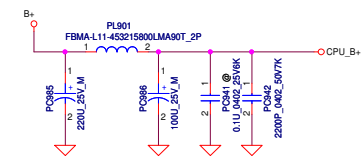
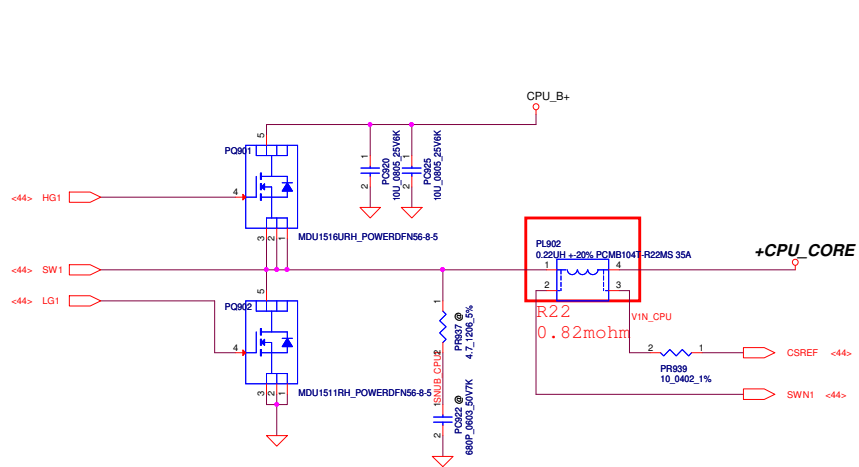
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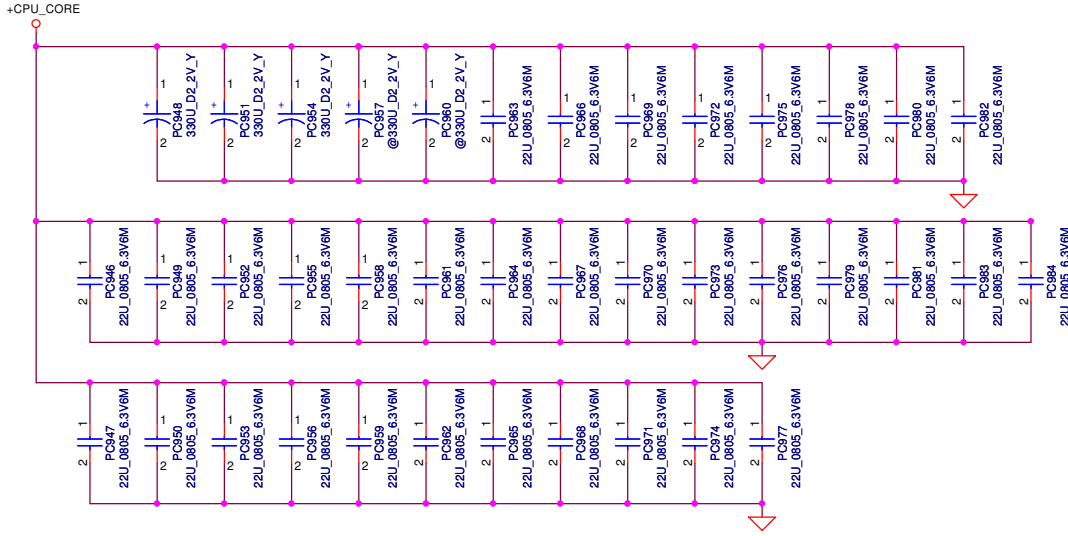


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+CPU_CORE

3 X 330u/9m (47W)
34 X 22u/0805

2X330u/9m (37W)
34 X 22u/0805



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