

Compal Confidential

DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2013-04-18

LA-9641P

REV: 1.0

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page
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Shark Bay

AMD MARS XT M2 128 bits / SUN PRO M2 64 bits

VRAM 512MB/1GB/2GB
MARS XT : DDR3 x 8
SUN PRO : DDR3 x 4

page 23~32

PEG 8x
Gen2 / Gen3

Intel Processor Haswell

rPGA946
37.5mm x 37.5mm

page 5,~11

Memory Bus
Dual Channel

DDR3L 1600MHz
DDR3L 1333MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2

page 12,13

LVDS Conn.
page 34

LVDS Translator
RTD2132R(Single)

page 33

HDMI Conn.
page 36

FDI *2
2.7GT/s

DMI2 *4
5GT/s

Intel PCH Lynx Point

FCBGA 695Balls
20mm x 20mm

USB30 x2

Left USB3.0 x2
USB30 Port 0,1
page 46

Right USB2.0
USB20 Port 9
page 46

Int. Camera
USB20 Port 3
page 33

Touch Screen
USB20 Port 2

Card Reader
Realtek RTS5170
USB20 Port 11
page 44

USB20 x6

CRT Conn.
page 35

RJ45 Conn.
page 39

LAN
Atheros AR8162/QCA8172 (10/100)

PCIe x1
page 38

SATA Gen3

HDD Conn.
SATA Port 4
page 41

SATA

ODD Conn.
SATA Port 5
page 41

PCIe Mini Card WLAN
PCIe Port 0
page 28

PCIe Mini Card
USB20 Port 10
page 28

PCIe x1

AZALIA

Audio Codec
CONEXANT CX20757
page 42

USB20 x1

Int. MIC Conn.
page 42

Int. Speaker Conn.
page 42

Audio Combo Jacks
HP & MIC
page 42

SPI ROM
2MB + 4MB
page 17

EC
ENE KB9012
page 44

Thermal Sensor
page 40

Touch Pad
page 44

Int. KBD
page 44

Sub-board

15"

14"

Power/B LSXXXP
page 44

LED/B LSXXXP
page 44

USB/B LSXXXP
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CR/B LSXXXP
page 44

ODD/B LSXXXP
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				Block Diagram
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Voltage Rails

power plane	+B	+5VALW	+1.35V	+5VS
		+3VALW		+3VS
State				+VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b

Device	Address
Thermal Sensor	1001_100xb

PCH SM Bus address

AMD-GPU SM Bus address

Device	Address
DDR DIMM1 ChannelA	0xA0
DDR DIMM2 ChannelB	0xA4

Device	Address
Internal thermal sensor	1000_001xb

Device	Address
RTD2132R	1101 010Xb

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Project	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
		2	Touch screen
	UHCI2	3	Camera
		4	
		5	
		6	
EHCI2	UHCI3	7	
		8	
	UHCI4	9	Right USB2.0
		10	WLAN
		11	Card reader
	UHCI5	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Camera	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
Right side USB	RUSB@
Zero ODD circuit	ZODD@
Share ROM	SROM@
Non-share ROM	NOSROM@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

R_USB@

SMBUS Control Table

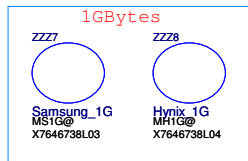
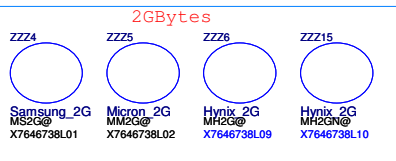
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	√	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	+3VS	+3VS
SMB_EC_DA2	+3VALW								
SMBCLK	PCH	X	X	X	√	√	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			X
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	√	X	√	X	X	√	X	√
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

VRAM BOM STRUCTURE Refer P4. VGA NOTE

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Mars XT VRAM STRAP

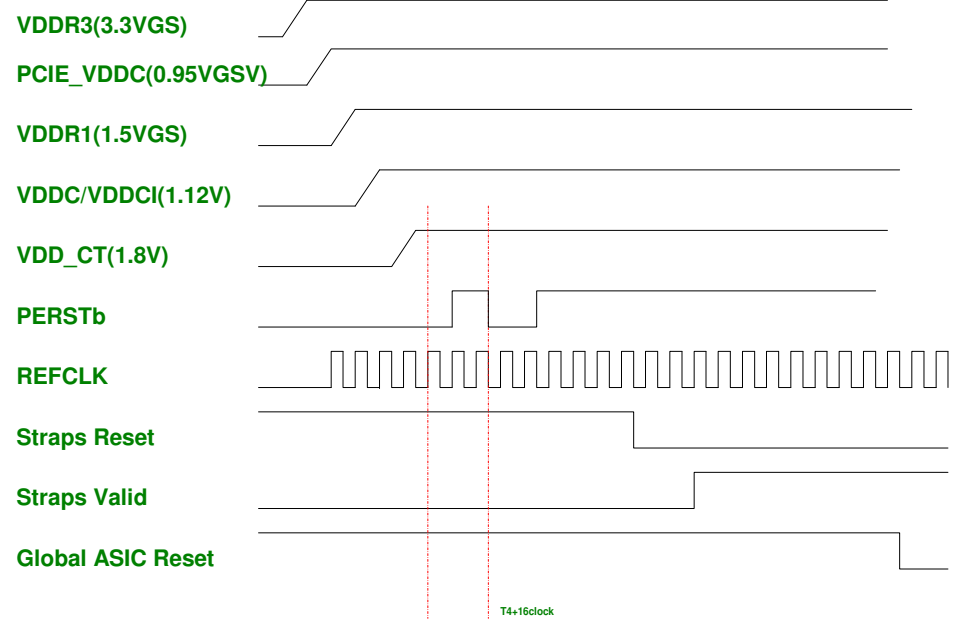
	x76@	x76@					
	Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27	
2GBytes ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K	
2GBytes ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K	
1GBytes ZZZ6 MH2G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	0	1	0	4.53K	2K	
1GBytes ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K	
1GBytes ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC	
2GBytes ZZZ15 MH2GN@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K	



Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

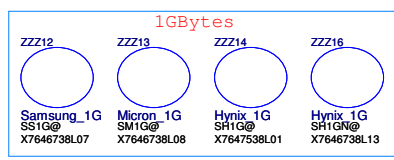
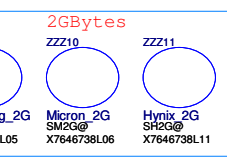


R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

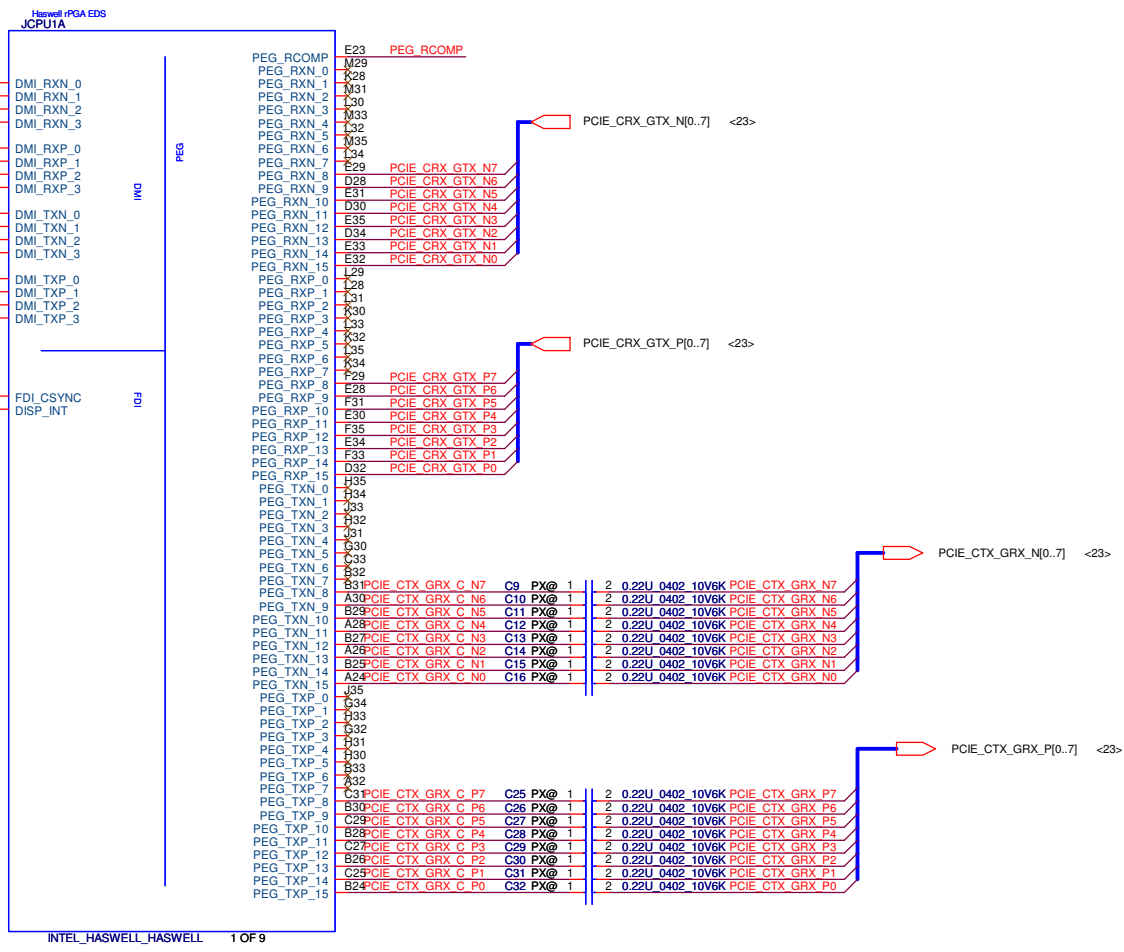
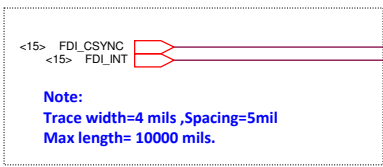
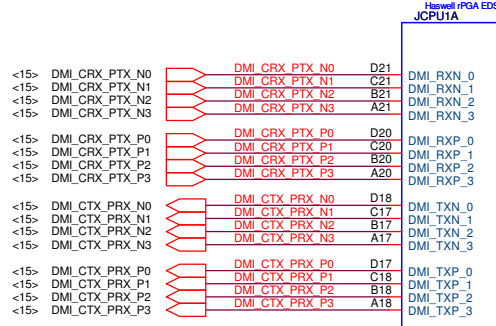
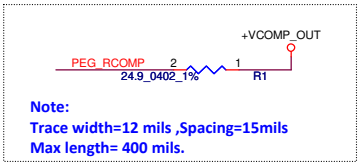
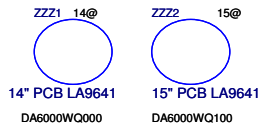
Note: 0402 1% resistors are required.

Sun PRO VRAM STRAP

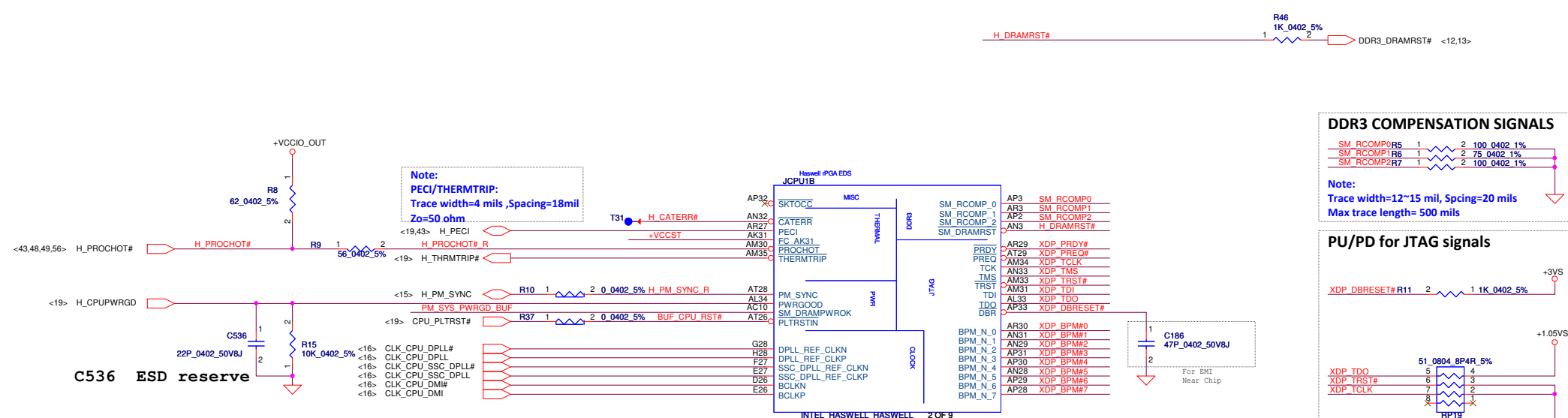
	x76@	x76@					
	Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27	
2GBytes ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-BC11	0	0	0	NC	4.75K	
2GBytes ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-109G:E	0	0	1	8.45K	2K	
1GBytes ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K	
1GBytes ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K	
1GBytes ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K	
1GBytes ZZZ14 SH1G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	1	1	1	4.75K	NC	
1GBytes ZZZ16 SH1GN@	Hynix 2048Mbits SA00006H400 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K	



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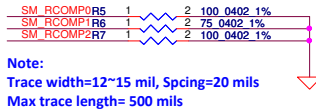


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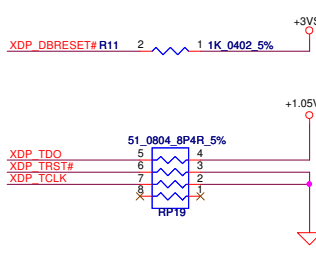


Note:
 PECCI/THERMTRIP:
 Trace width=4 mils, Spacing=18mil
 Zo=50 ohm

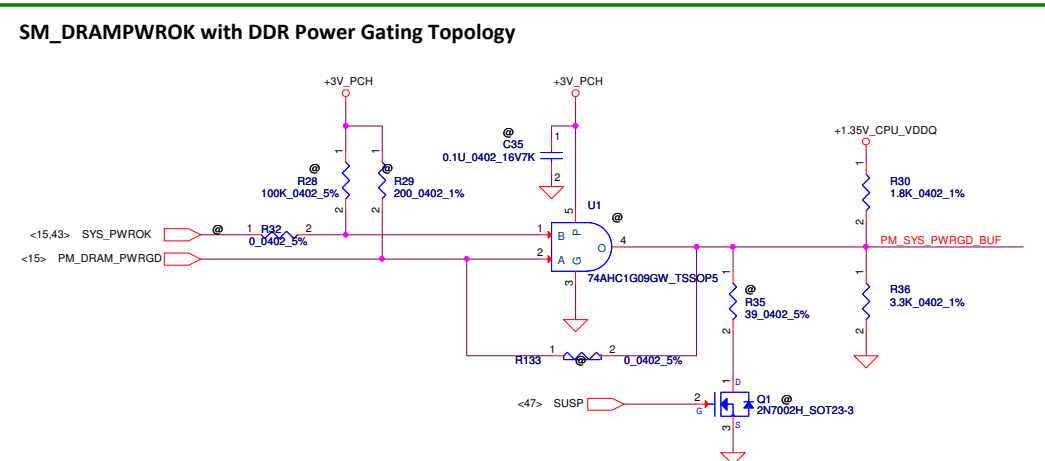
DDR3 COMPENSATION SIGNALS



PU/PD for JTAG signals



+VCCIO_OUT
 CLK_CPU_SSC_DPLL# 2 @R26 1 10K 0402 5%
 CLK_CPU_SSC_DPLL# 2 @R27 1 10K 0402 5%
SSC CLOCK TERMINATION, IF NOT USED, stuff R26,R27



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<12> DDR_A_D[0..63]

JCPUIC

Haswell iPGA EDS

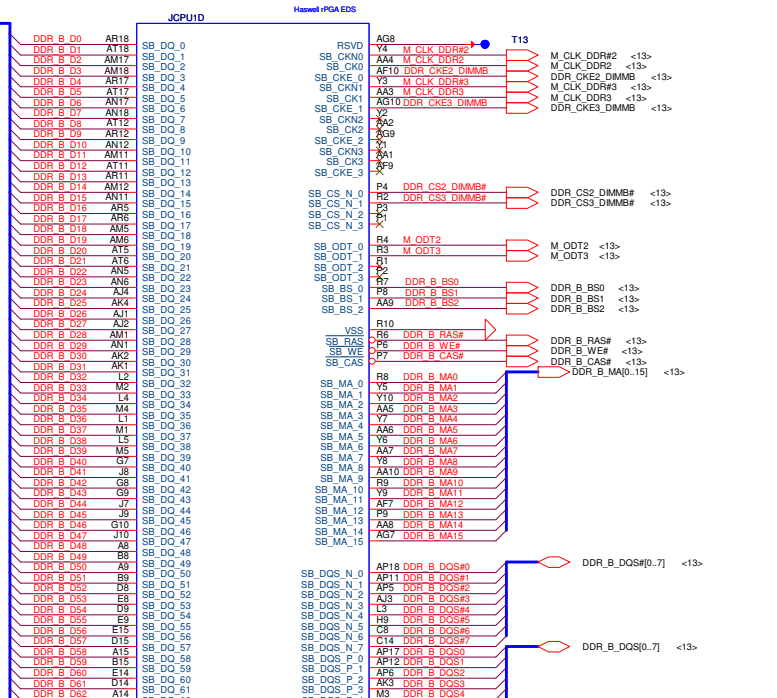


INTEL_HASWELL_HASWELL 3 OF 9

<13> DDR_B_D[0..63]

JCPUID

Haswell iPGA EDS



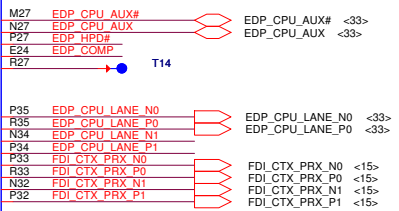
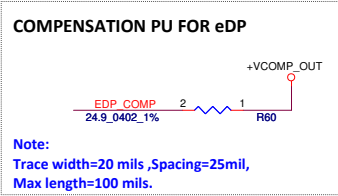
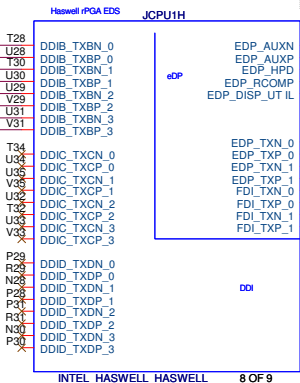
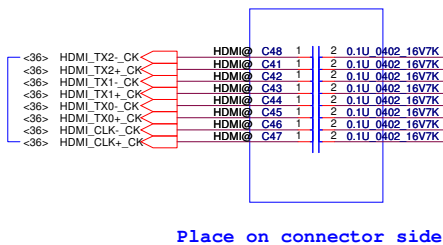
INTEL_HASWELL_HASWELL 4 OF 9

CPI DRIVER VREF PATH IS DEFAULT

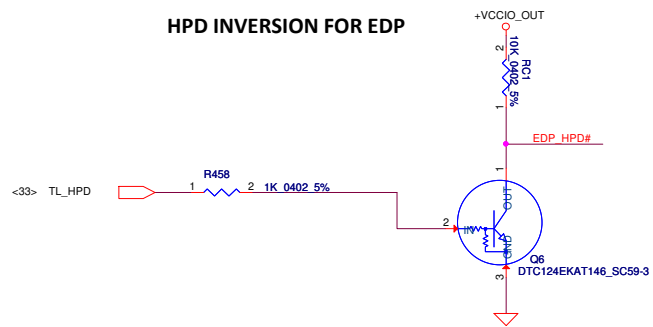
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

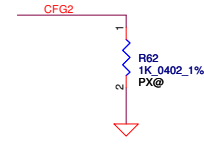
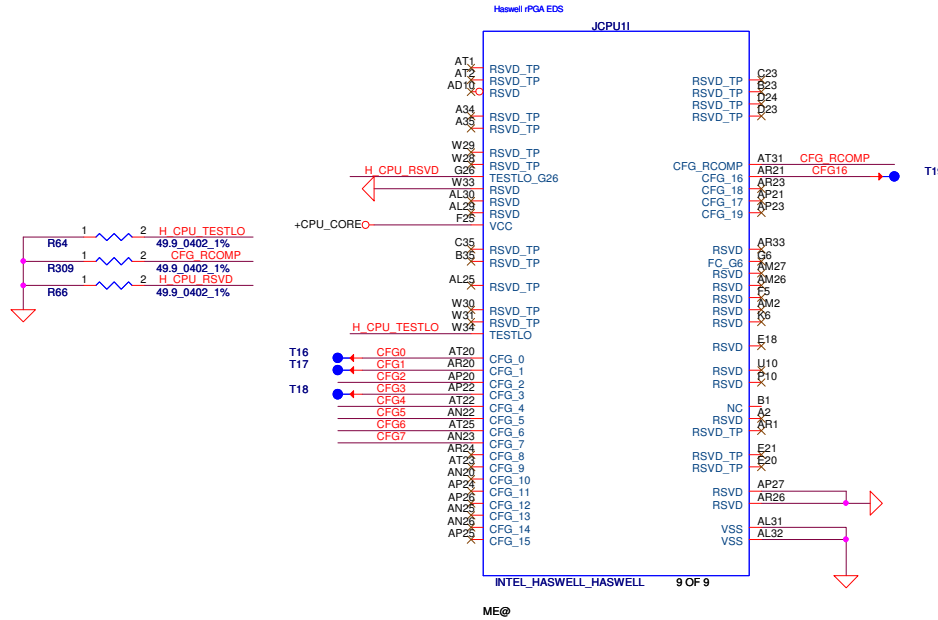


HPD INVERSION FOR EDP

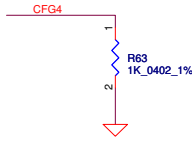


HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

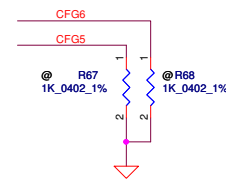
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

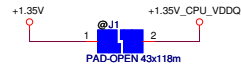


PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

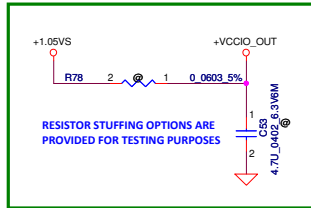
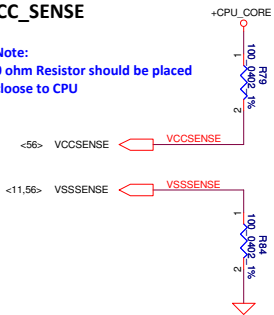
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+1.35V_CPU_VDDQ Source



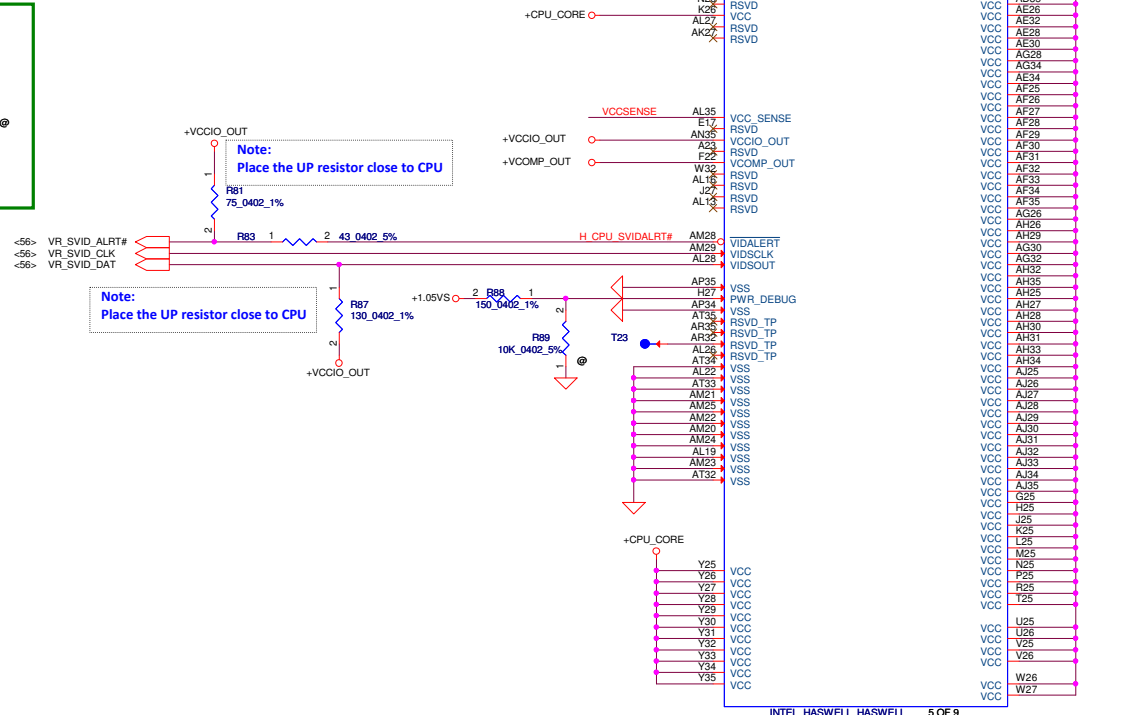
VCC_SENSE

Note:
0 ohm Resistor should be placed close to CPU

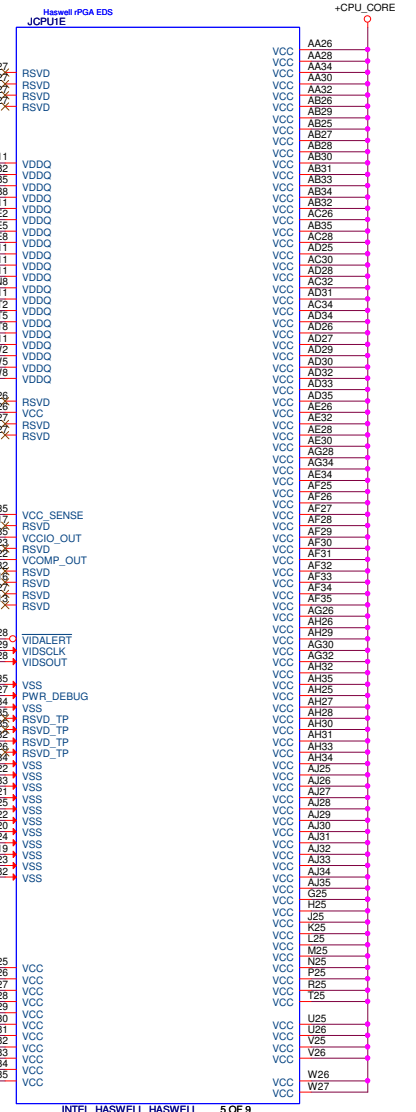
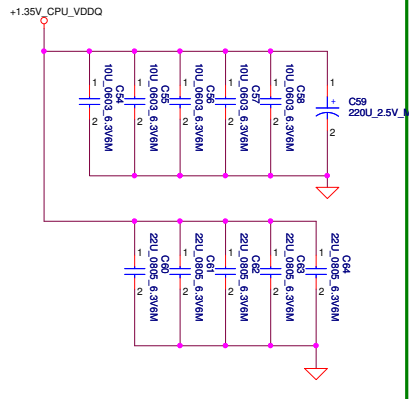


Note:
Place the UP resistor close to CPU

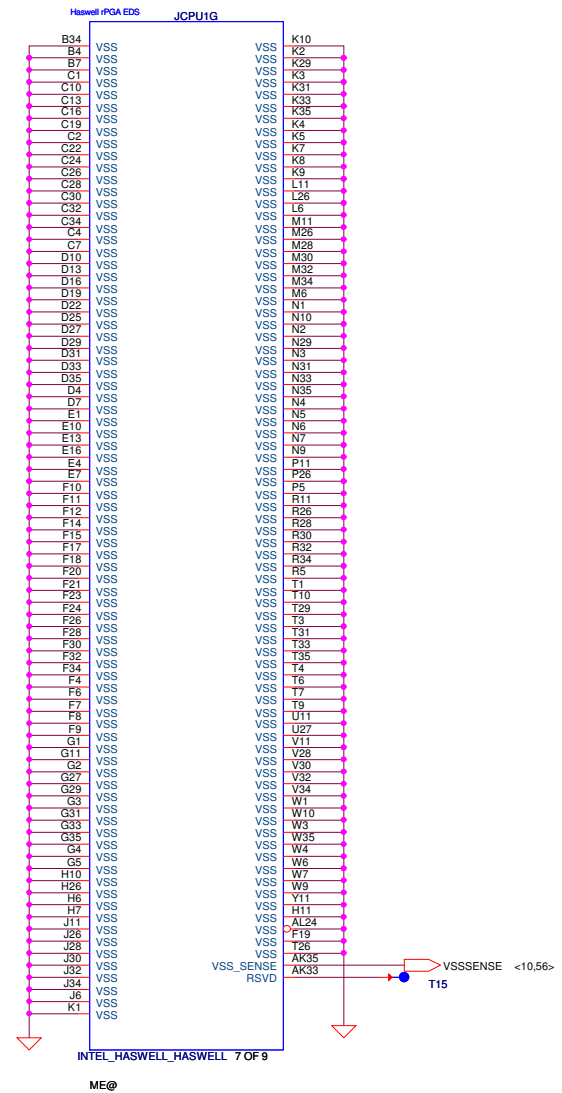
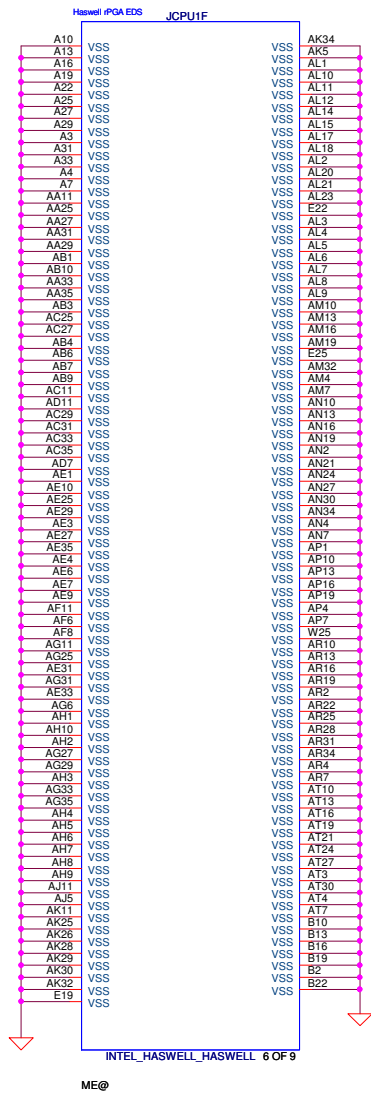
Note:
Place the UP resistor close to CPU



VDDQ DECOUPLING



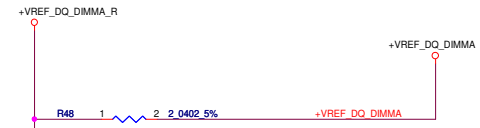
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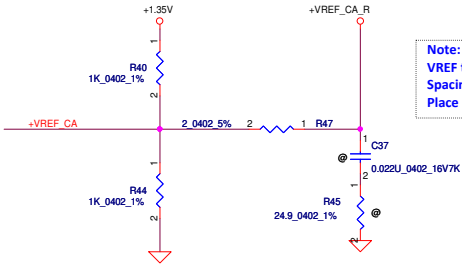
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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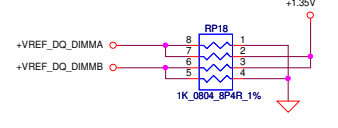
<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#0..7
<7> DDR_A_MA[0..15]



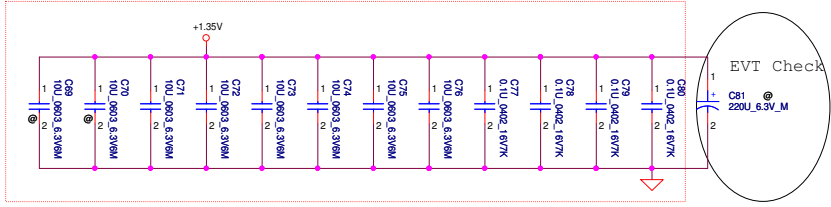
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket



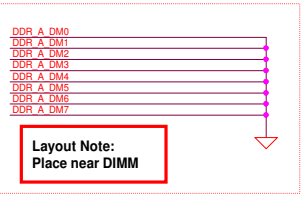
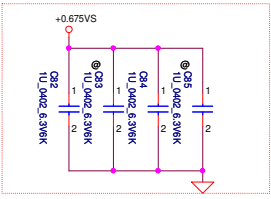
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket



Layout Note:
Place near DIMM

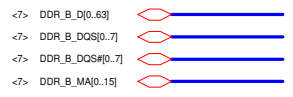
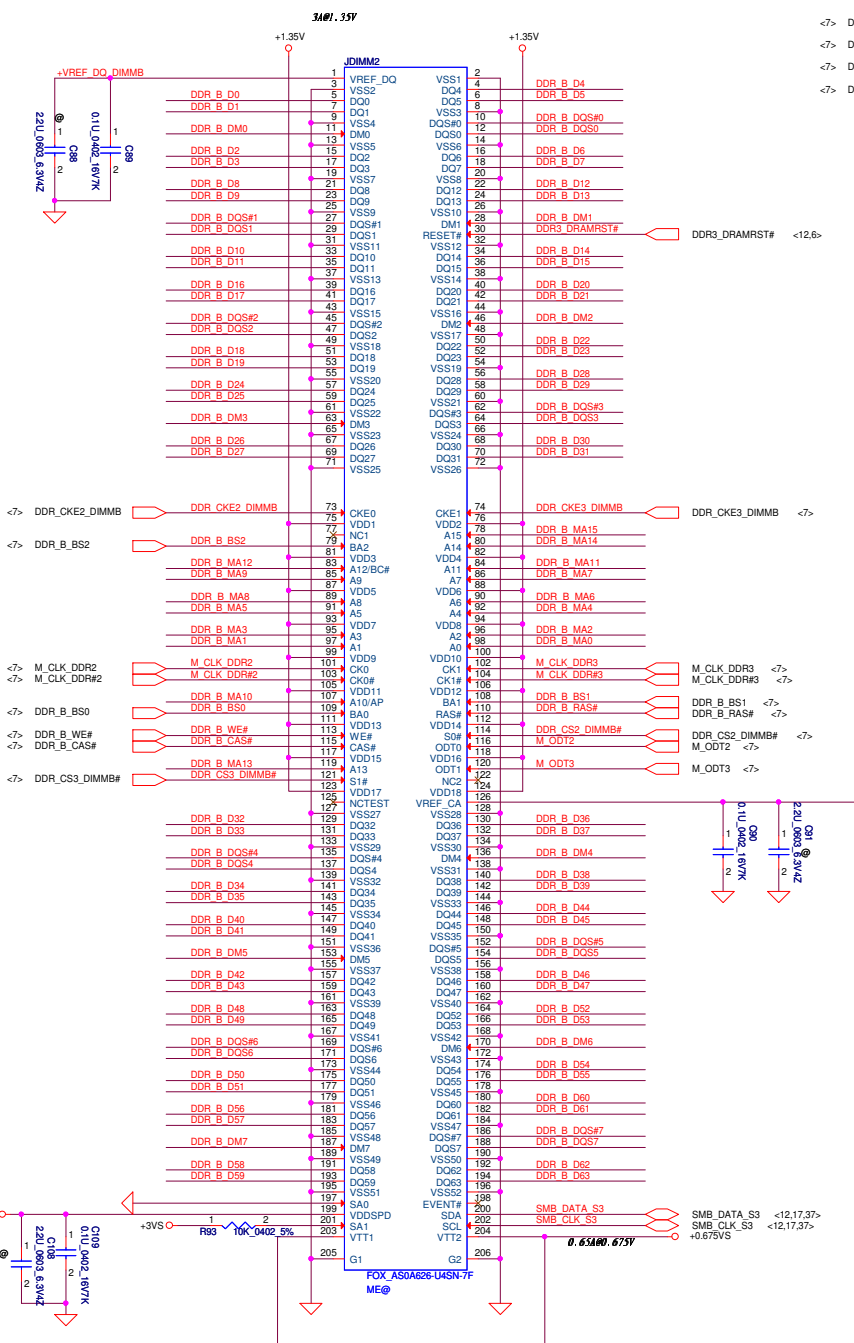


Layout Note:
Place near DIMM

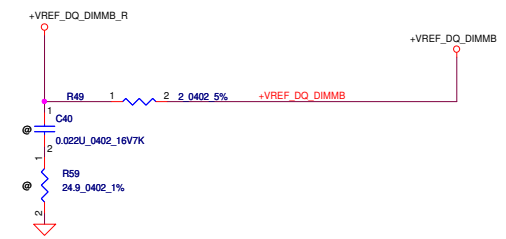


Layout Note:
Place near DIMM

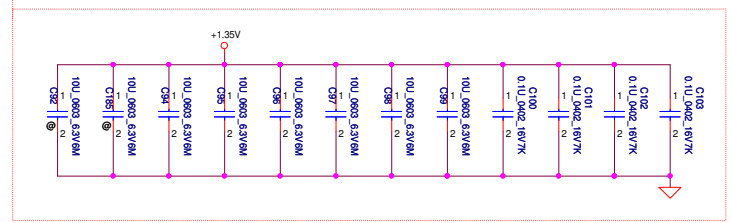
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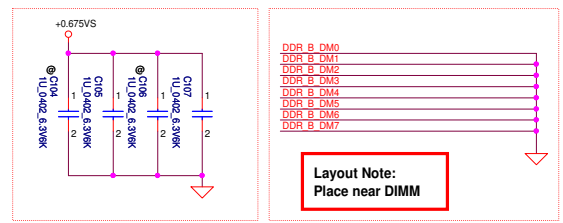
Note:
VREF trace width: 20 mils at least
Spacing: 20mils to other signal/planes



Layout Note:
Place near DIMM

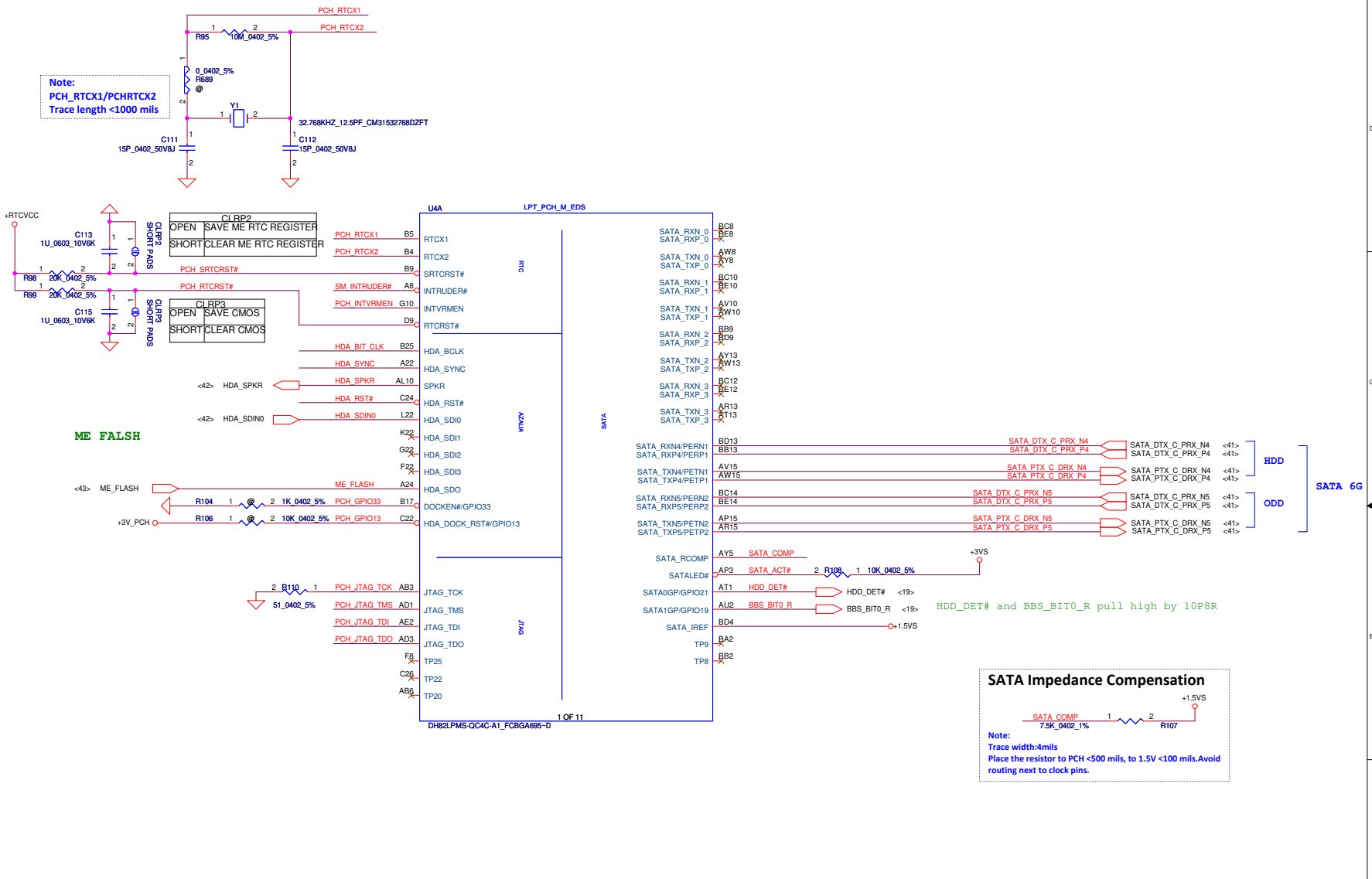
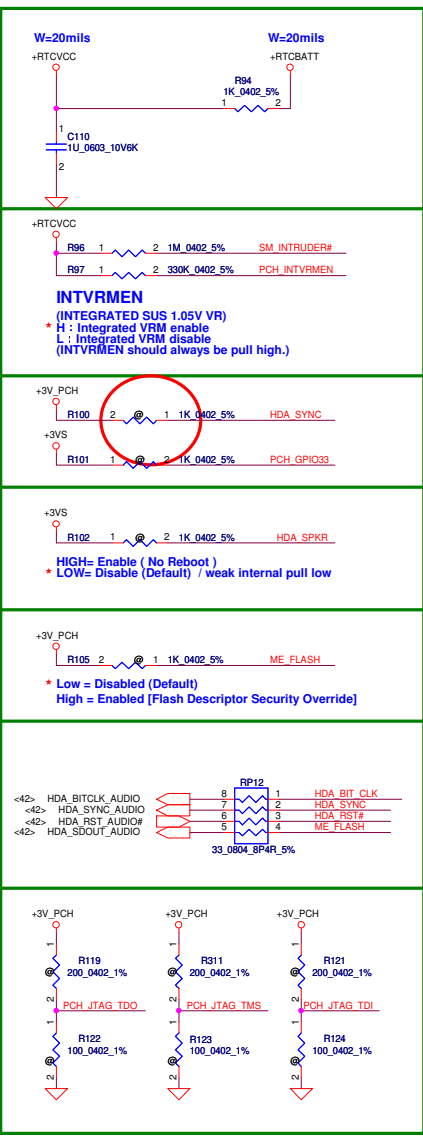


Layout Note:
Place near DIMM

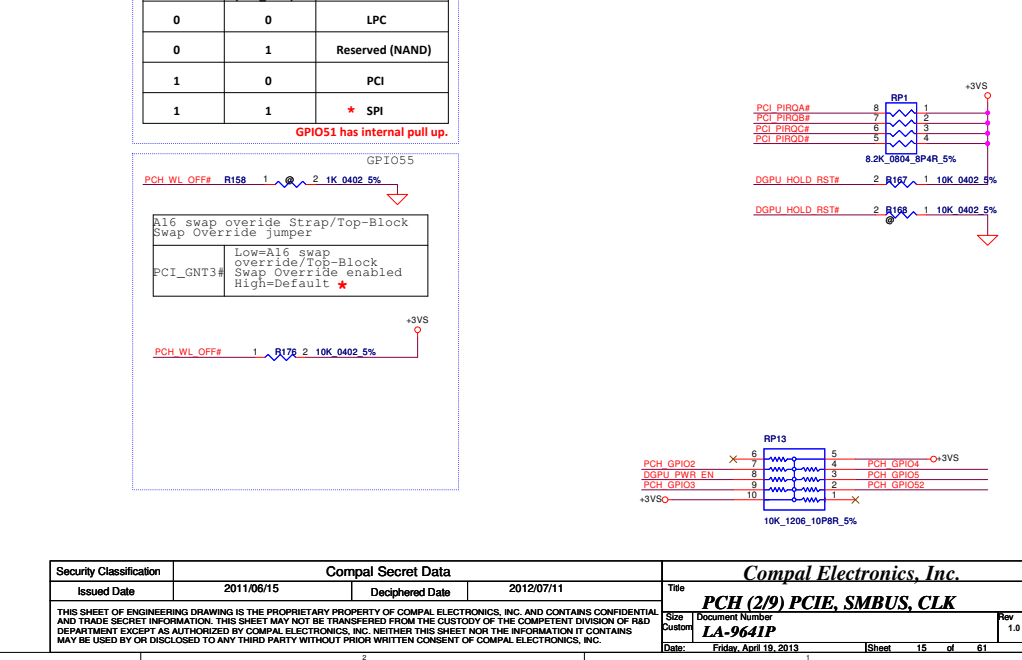
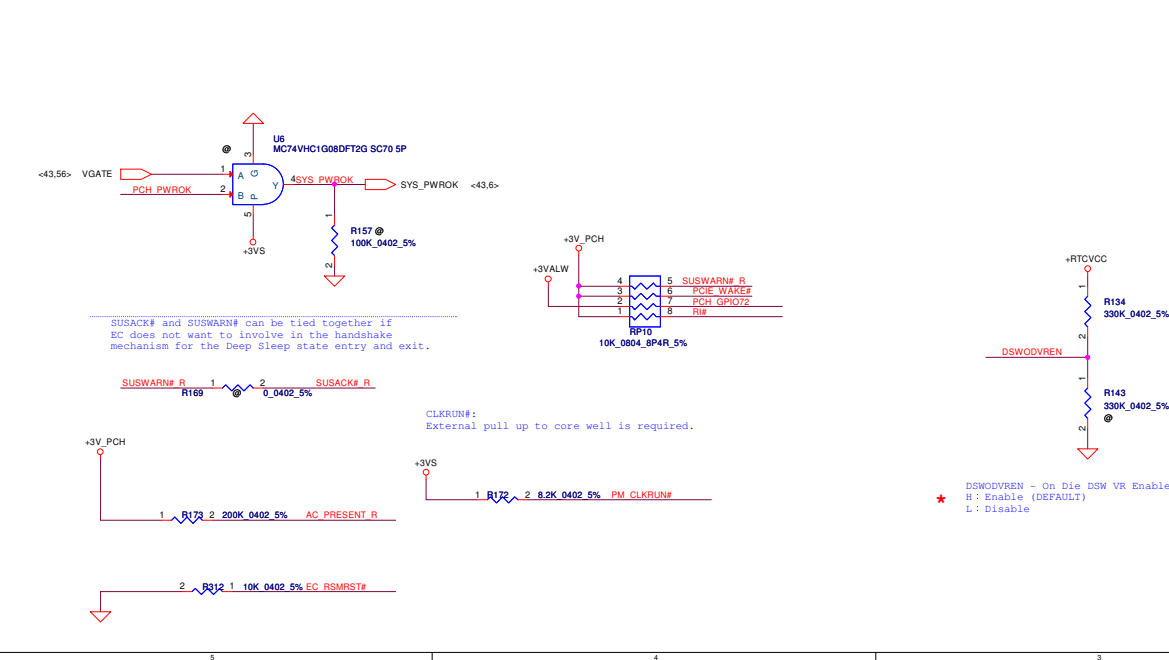
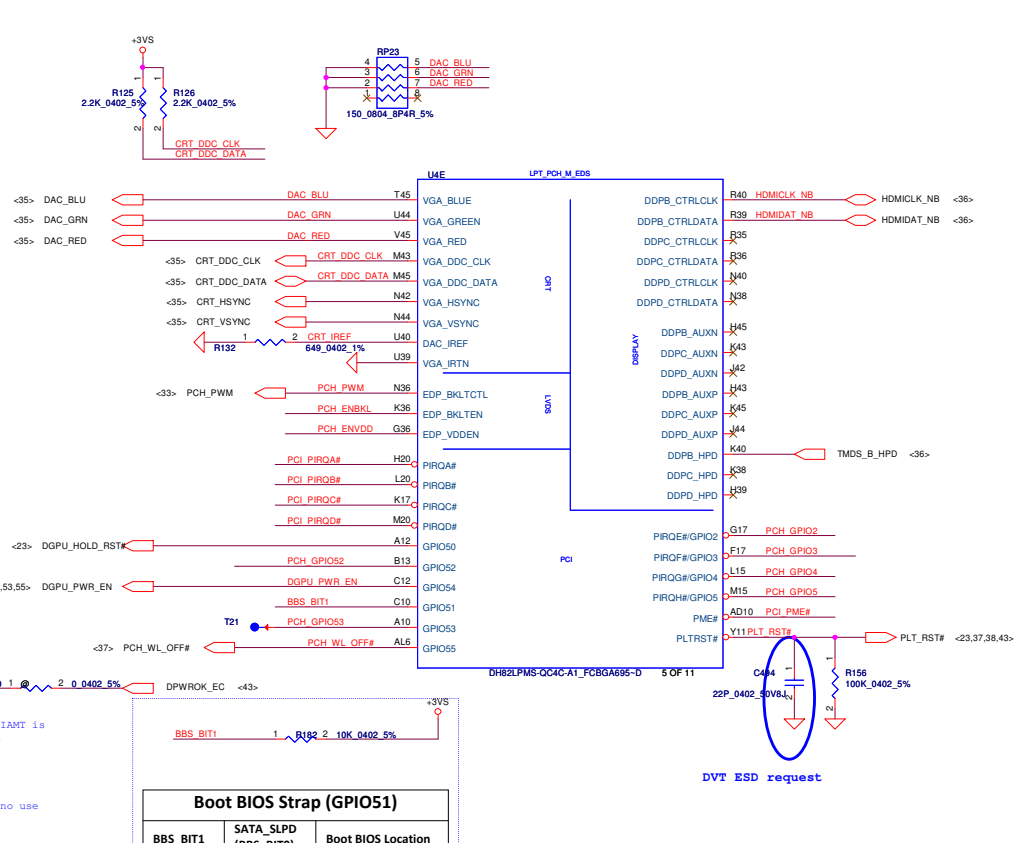
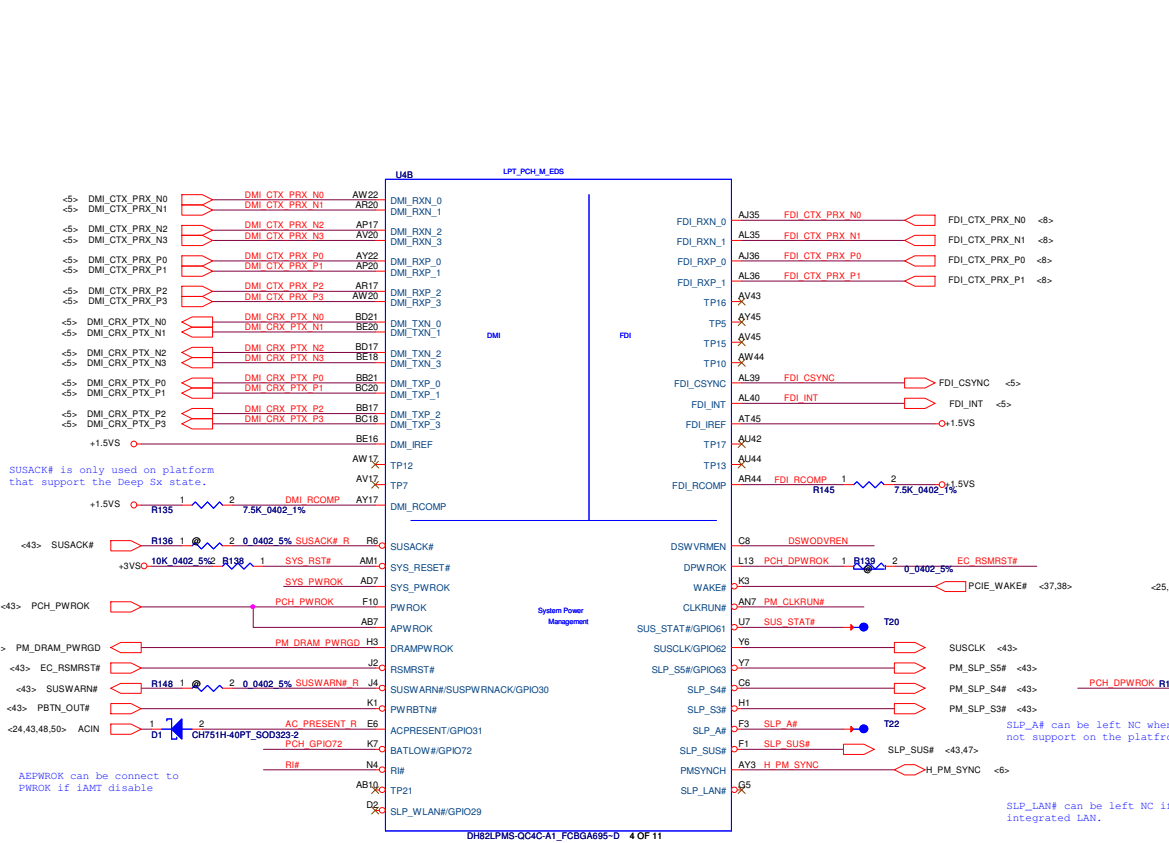


Layout Note:
Place near DIMM

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Boot BIOS Strap (GPIO51)

BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	* SPI

GPIO51 has internal pull up.

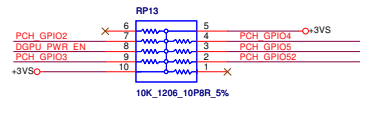
GPIO55

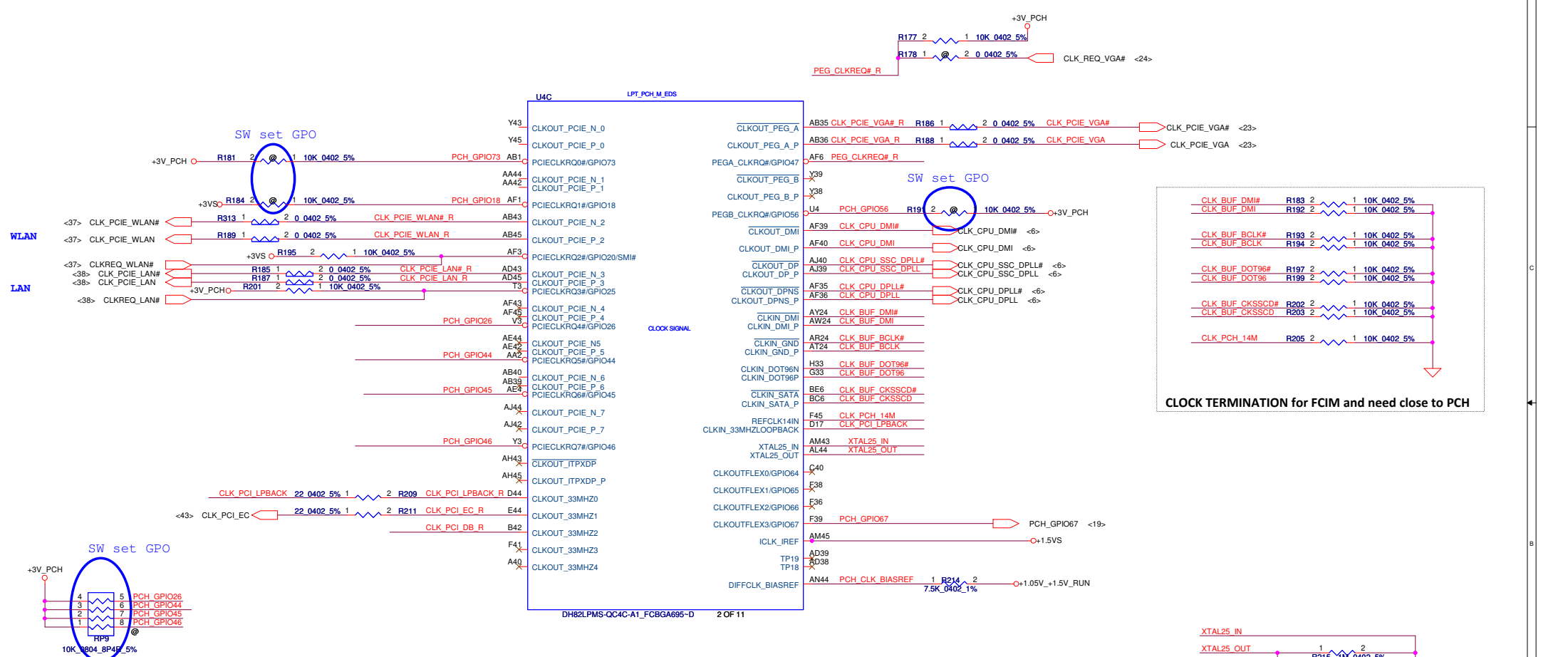
A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled
High=Default *

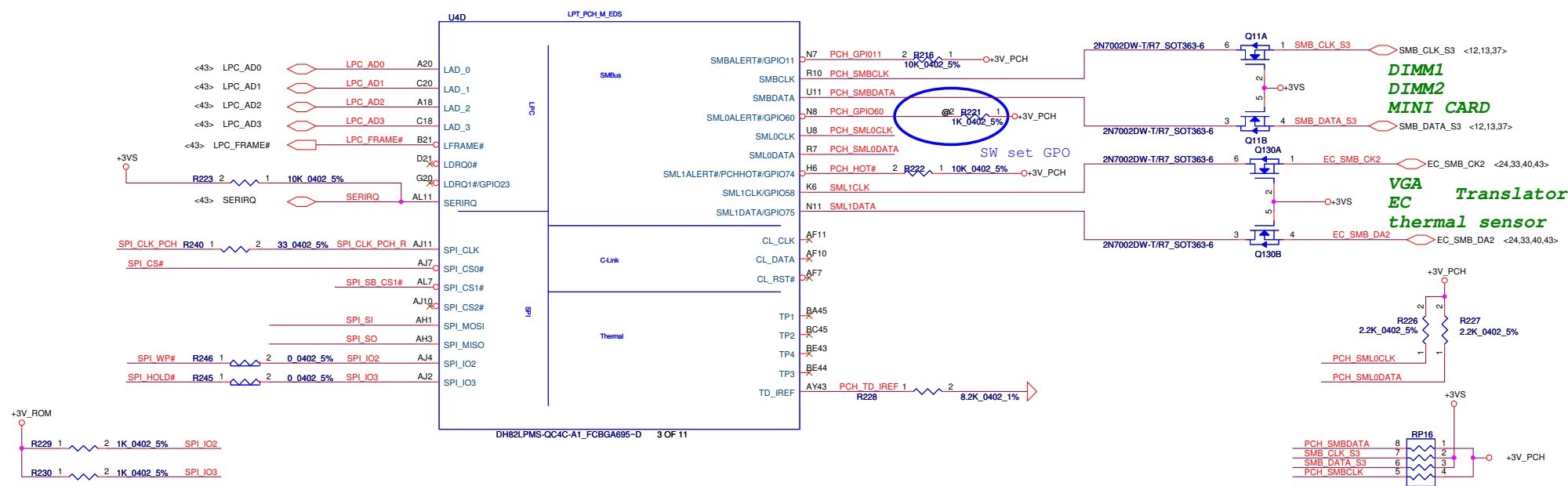
PCH_WL_OFF# R158 1 @ 2 1K 0402 5%

PCH_WL_OFF# 1 R178 2 10K 0402 5%



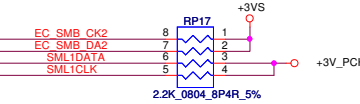
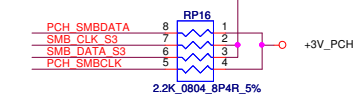
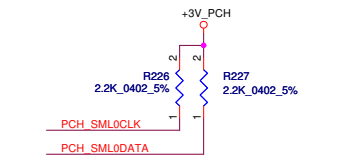


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			LA-9641P	1.0	
			Date: Friday, April 19, 2013	Sheet 16	of 61

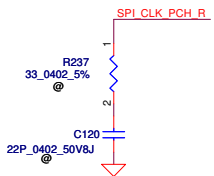


**DIMM1
DIMM2
MINI CARD**

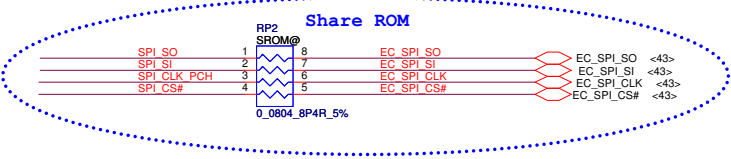
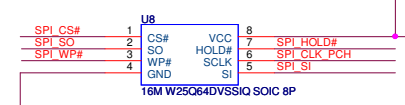
**VGA
EC Translator
thermal sensor**



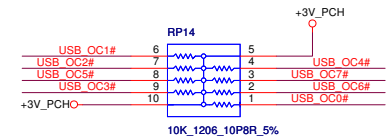
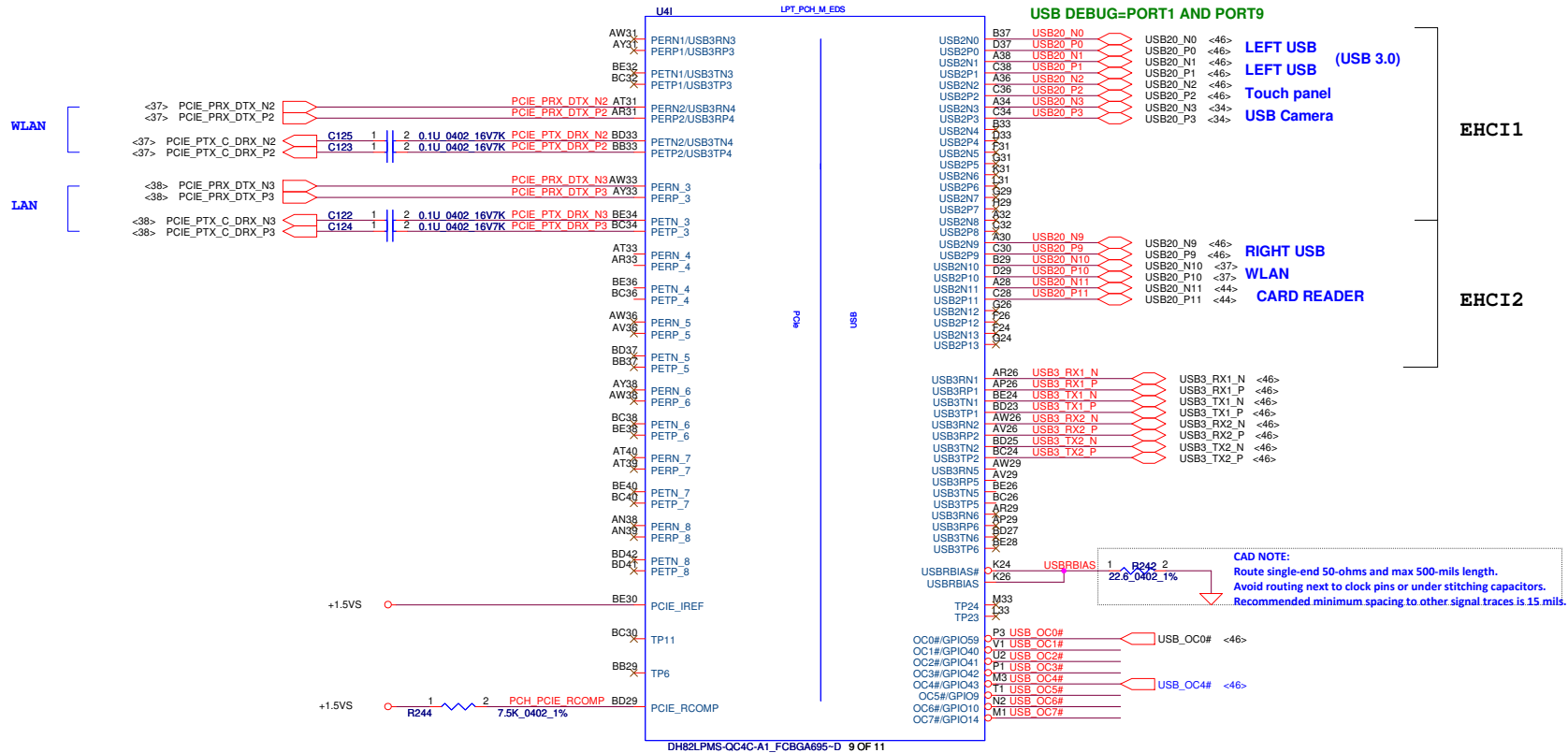
8MB SPI ROM FOR ME & Non-share ROM.



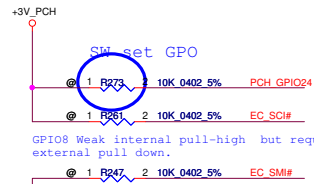
R124;c190 close to U4.T3 pin



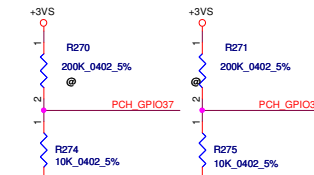
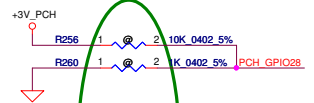
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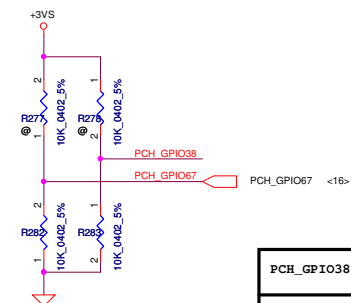
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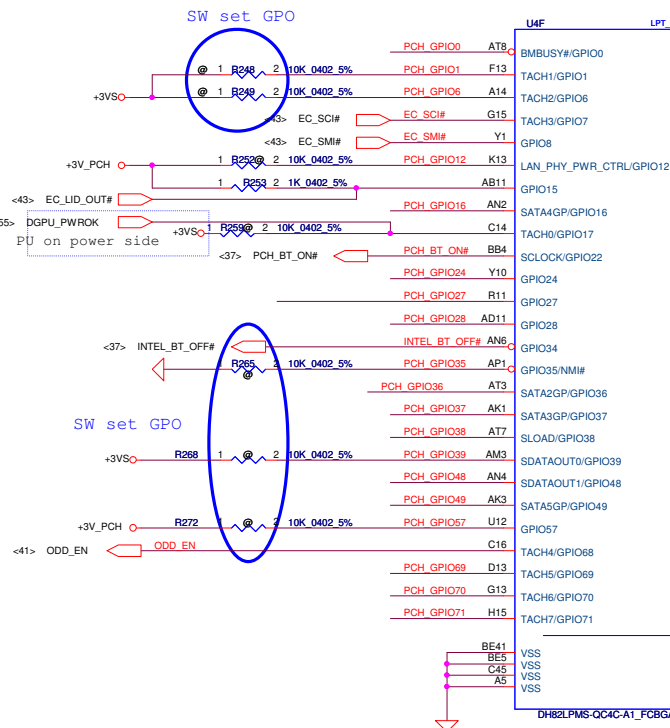
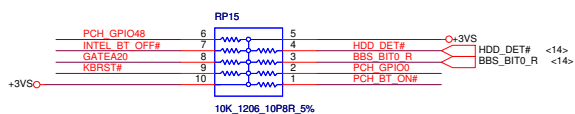
Remove strap description
inform SW set GPIO



BIOS Request SKU ID

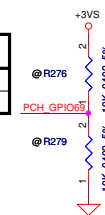


PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	DIS
1	1	UMA

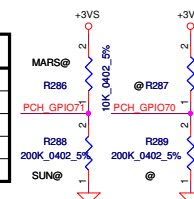


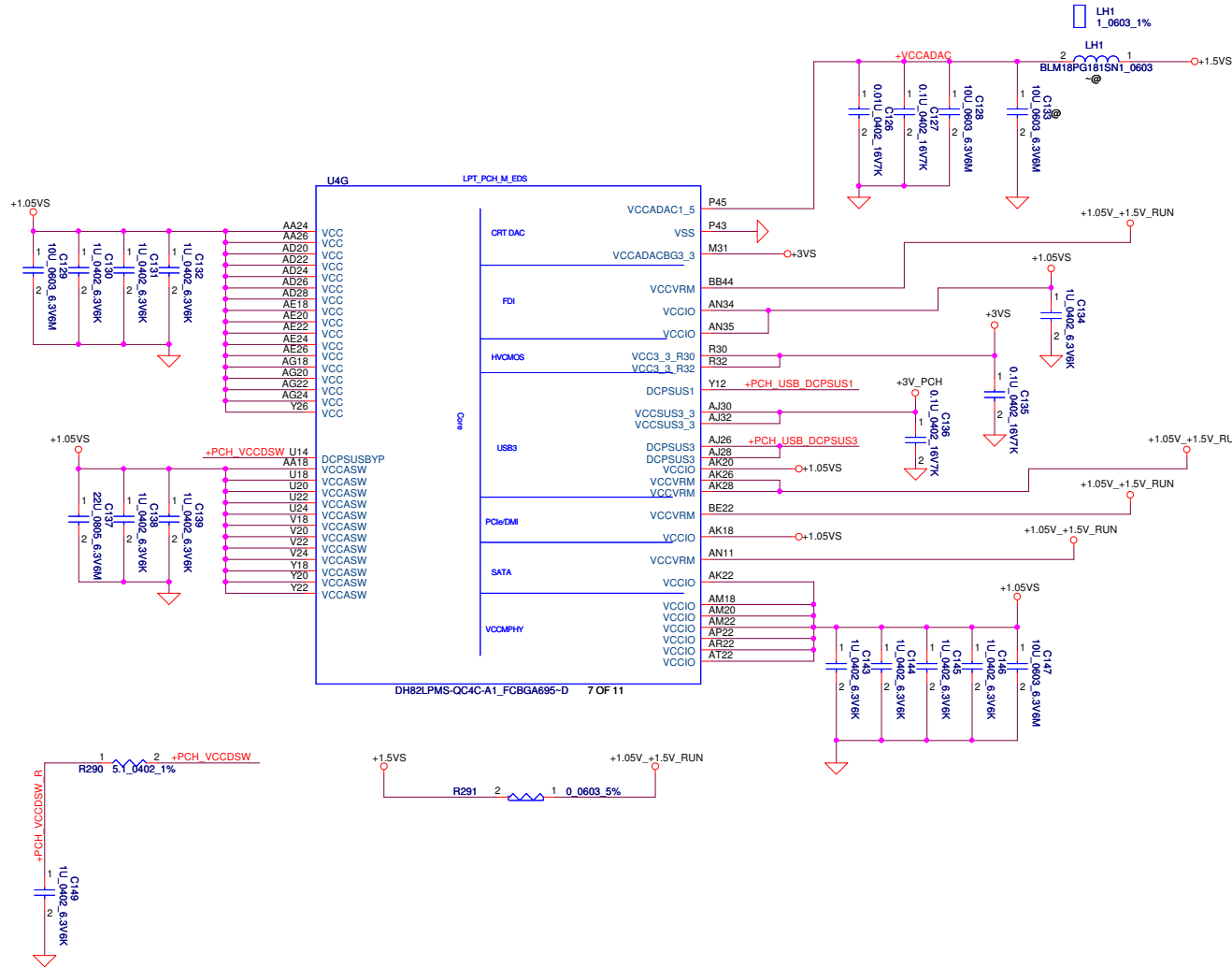
Need Update

PCH_GPIO69	Function
0	
1	

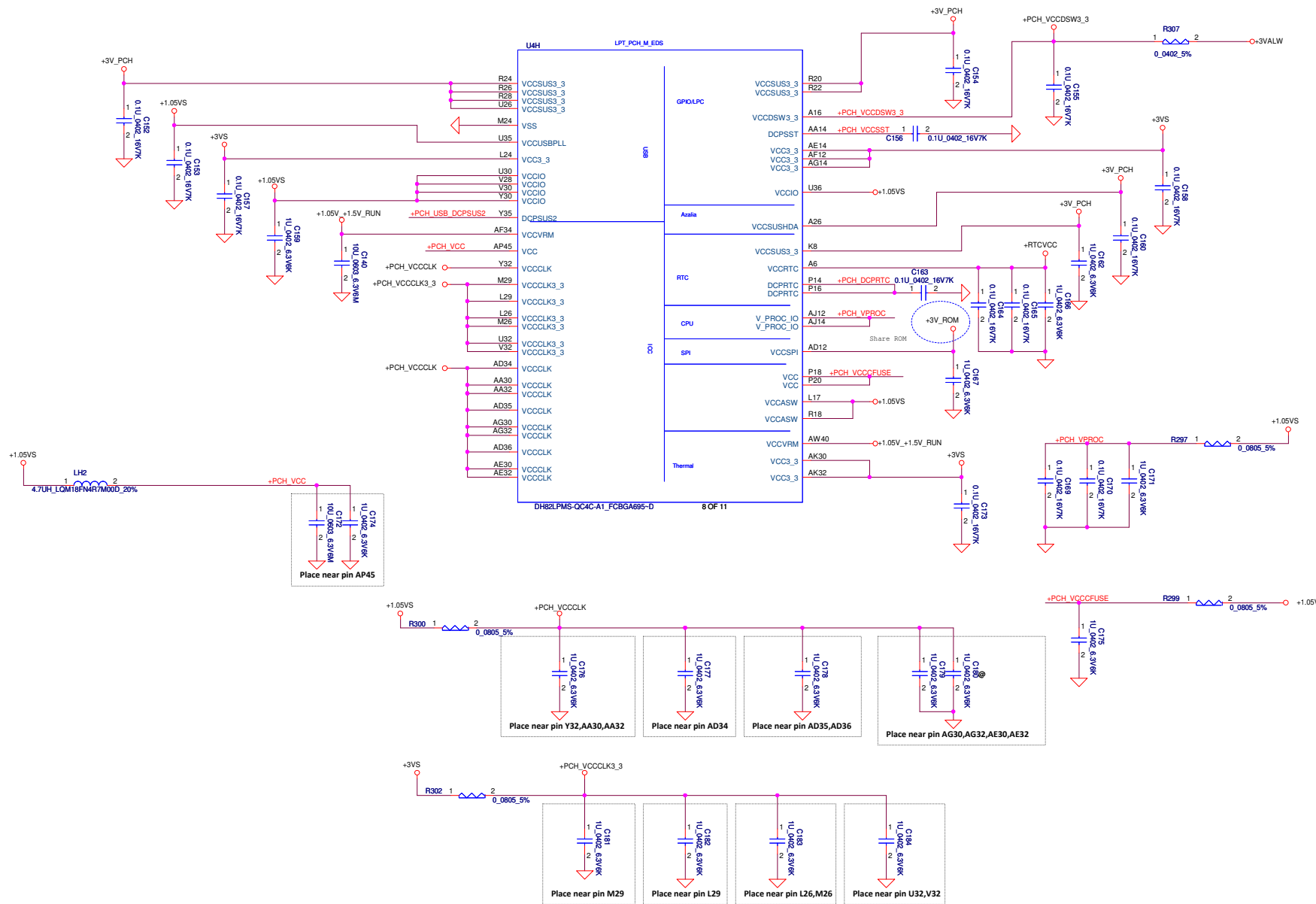


PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	SUN PRO
1	Mars XT





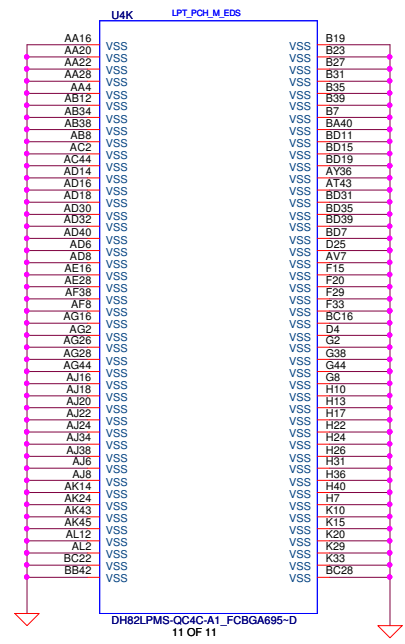
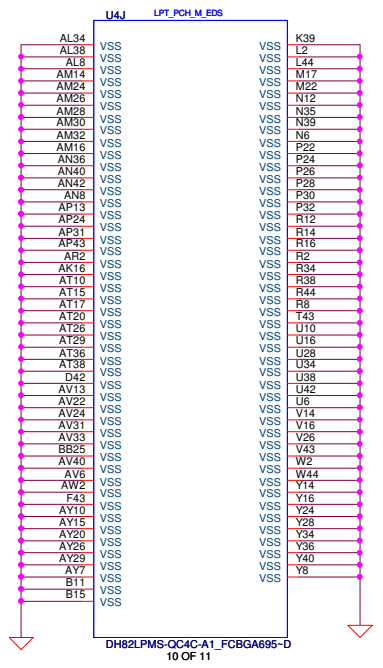
PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



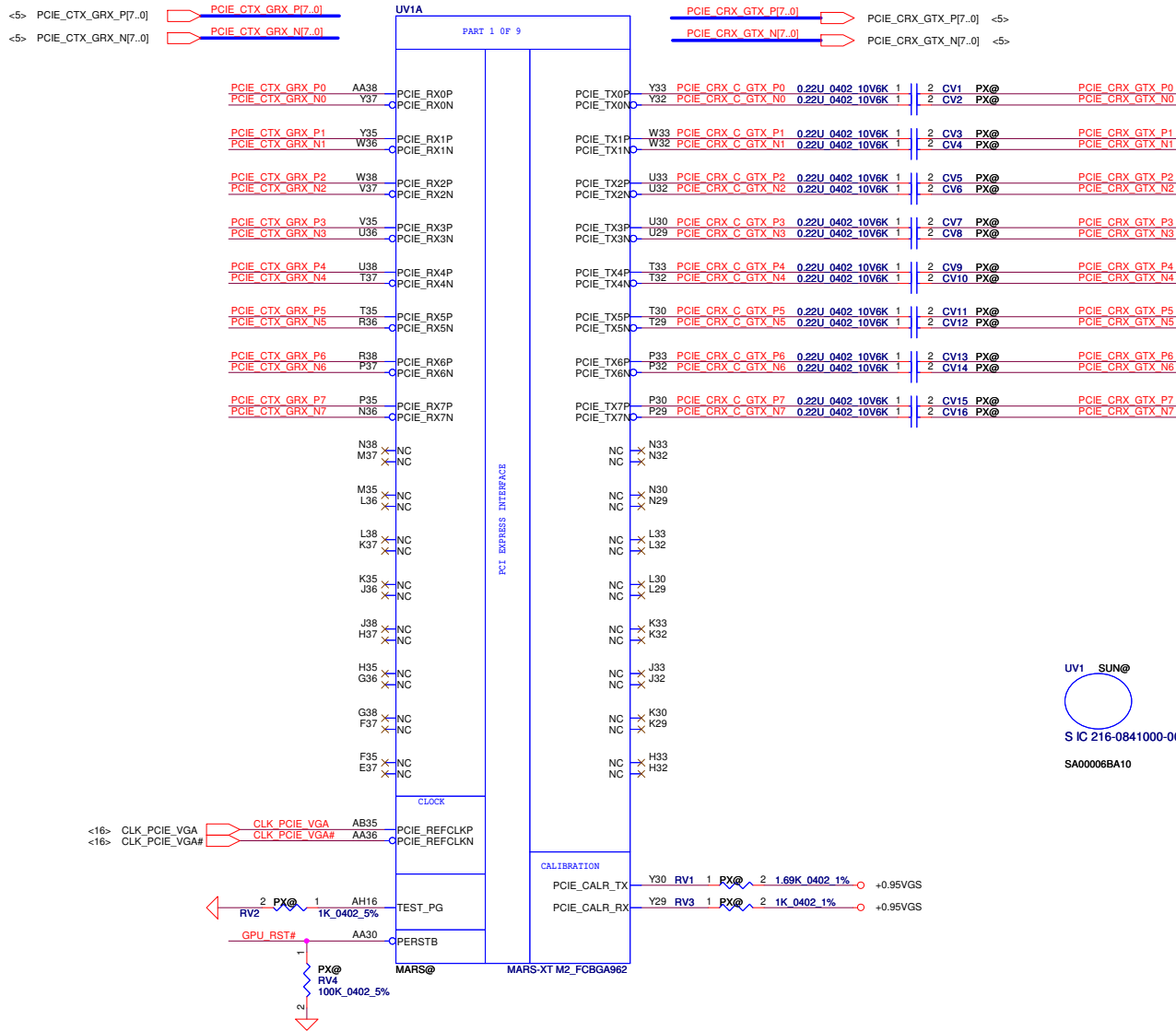
PCH Power Rail Table

Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

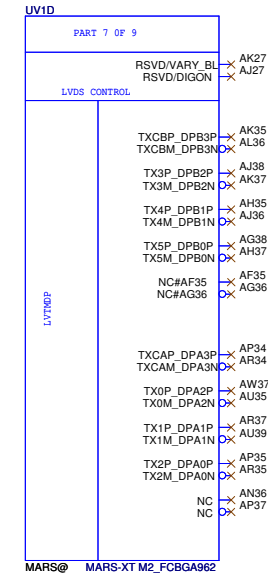
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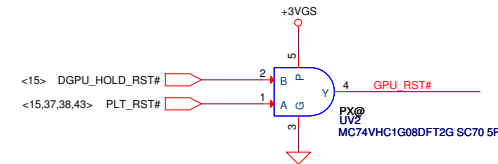
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LVDS Interface

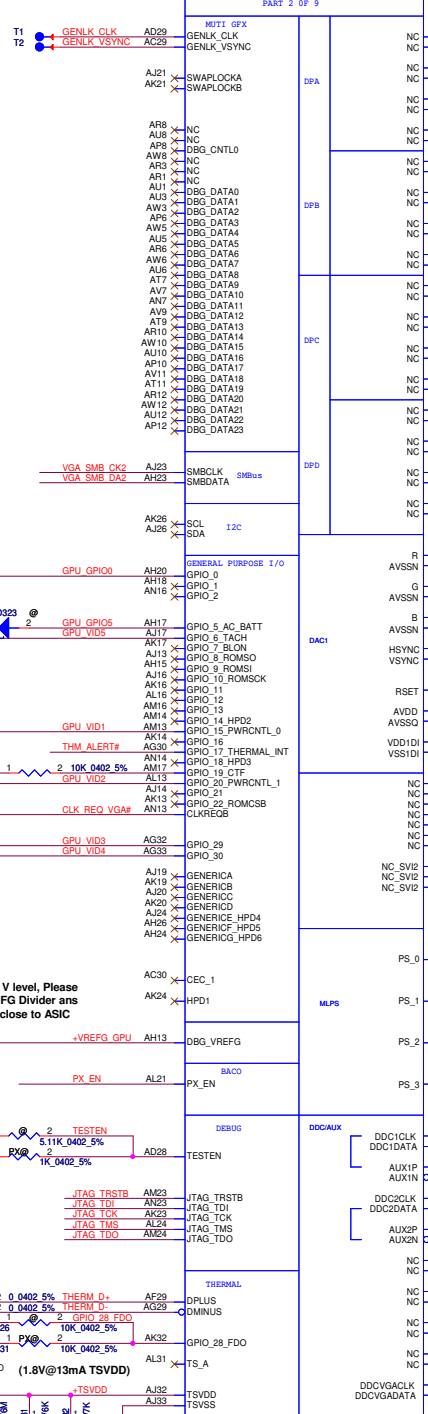


UV1 SUN@
 S IC 216-0841000-00 A0 SUN PRO M2 FCBGA 962P C38
 SA00006BA10

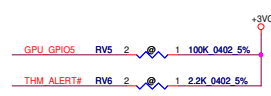


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UV1B PART 2 OF 9



STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

0.60 V level, Please VREFG Divider ans cap close to ASIC

GPIO 28 FDO MLPS

GPIO	FDO	MLPS
H	Disable	
L	Enable	

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

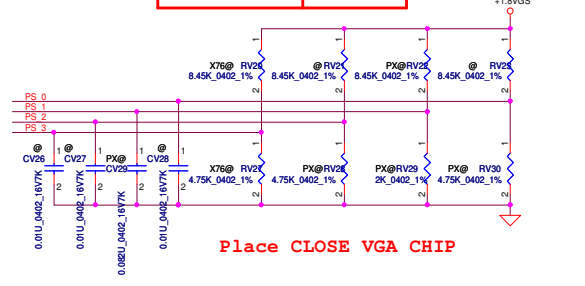
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRs_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select if PS_2[3]=0, defines memory aperture size if PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1]	NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

MLPS Strap

Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd	
PS_0[5:1]	1 1	000	NC	NC	4.75K
PS_1[5:1]	01	0 0 1	82 nF	8.45K	2K
PS_2[5:1]	10	0 0 0	NC	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 4

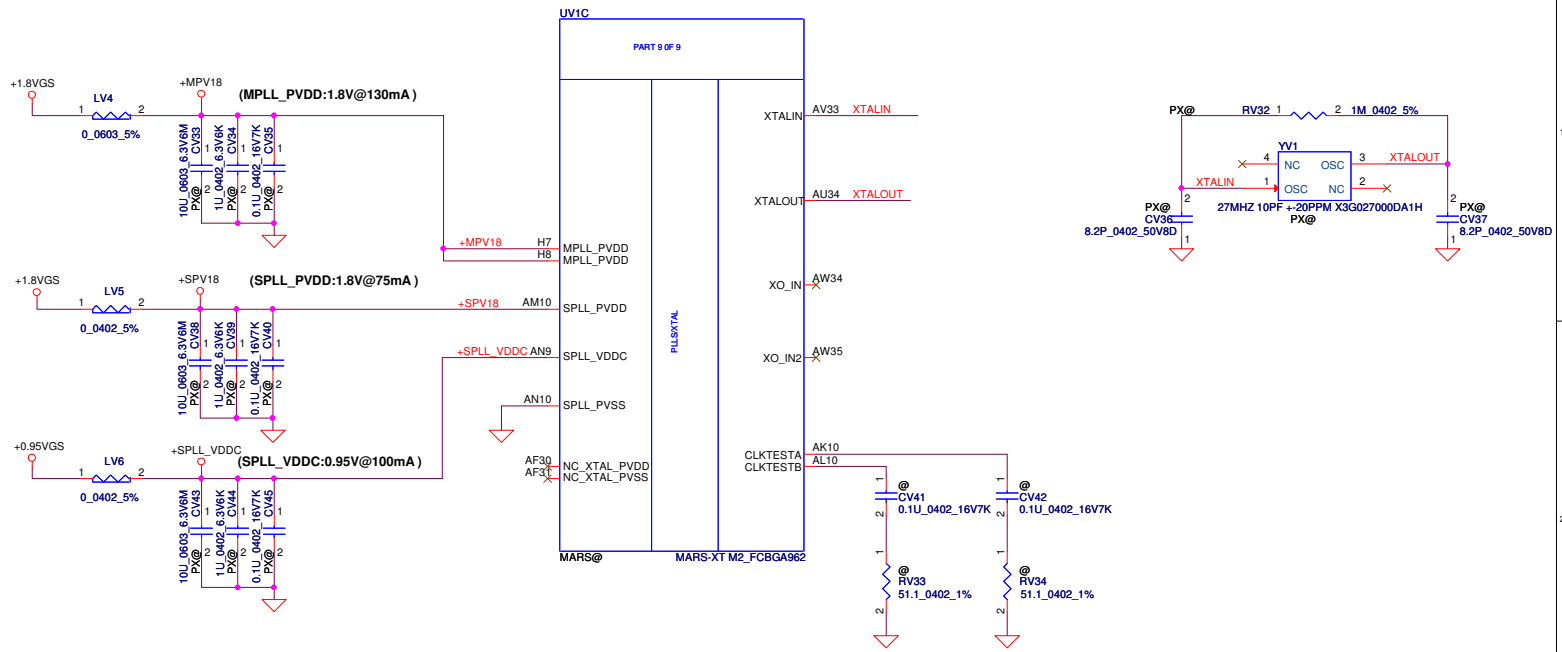


Place CLOSE VGA CHIP

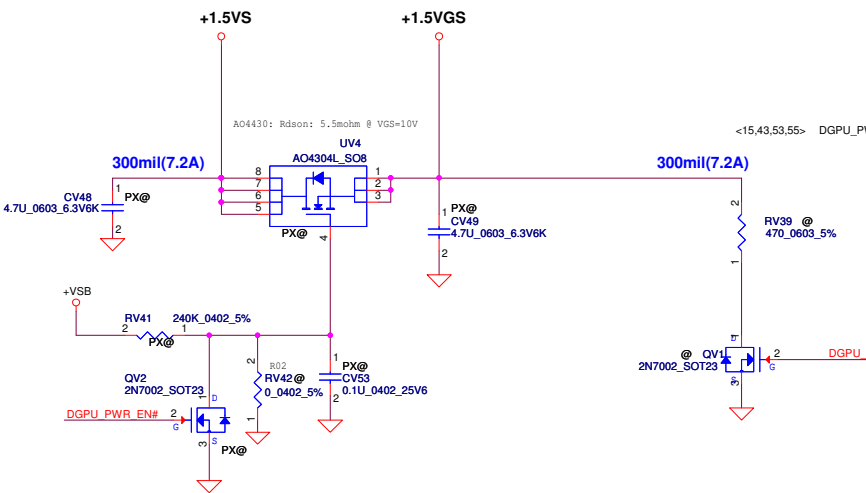
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

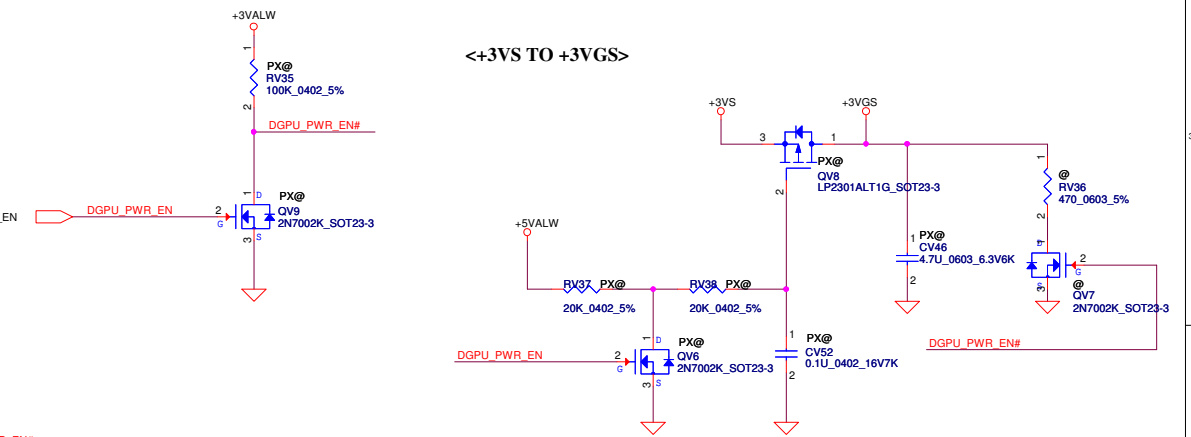
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



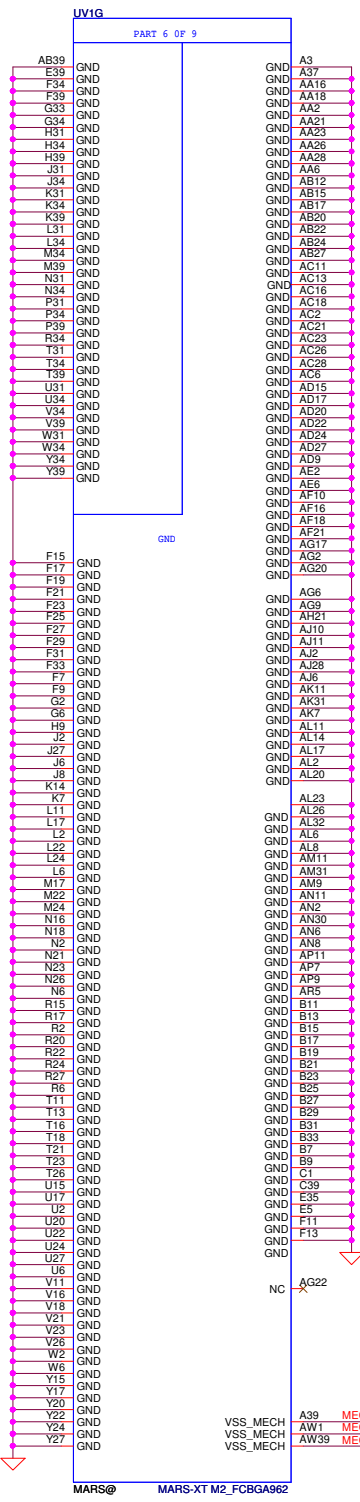
+1.5VS to +1.5VGS Transfer



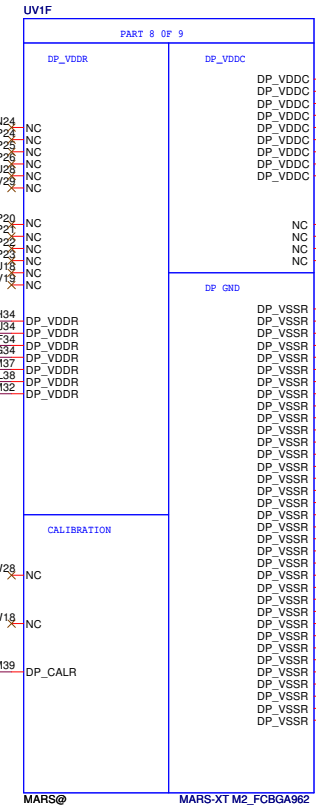
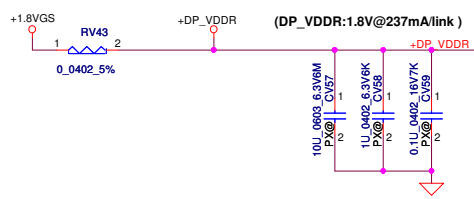
<+3VS TO +3VGS>



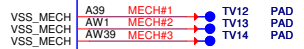
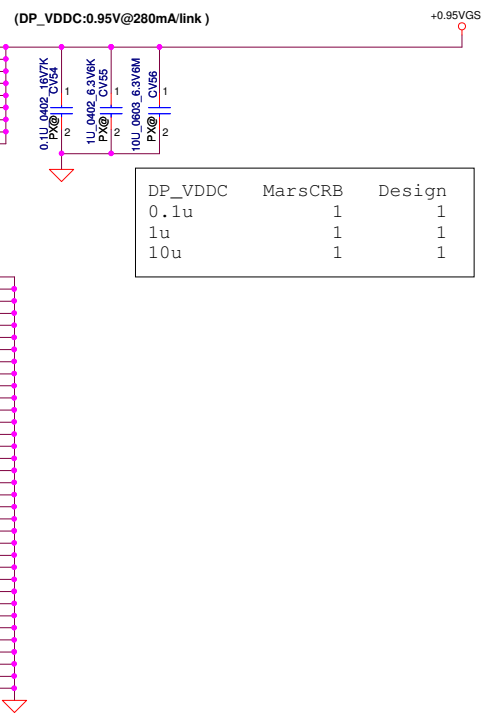
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Issued Date	2012/07/03	Deciphered Date	2013/07/03	Title
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				LA-9641P
				Rev 1.0
				Date: Friday, April 19, 2013 Sheet 25 of 61



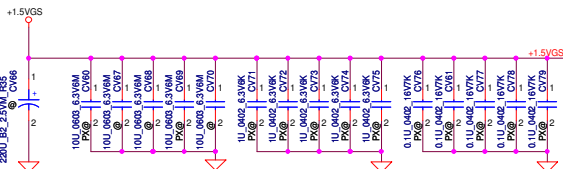
DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



Security Classification				Compal Secret Data				Compal Electronics, Inc.				
Issued Date	2012/07/03	Deciphered Date	2013/07/03	Title				AT1 MarsXTX M2 PWR GND				
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Date:								Friday, April 19, 2013	Sheet	26	of	61

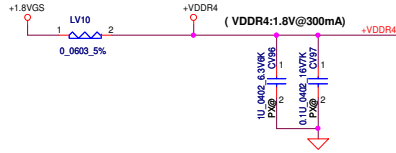
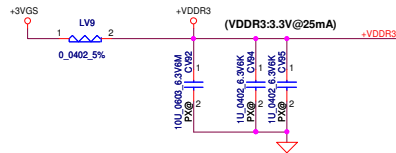
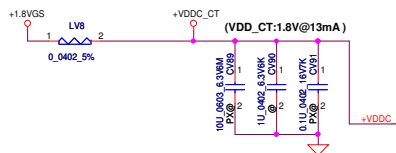


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

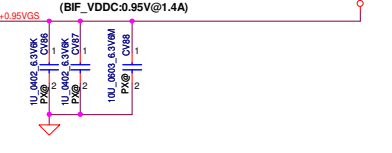
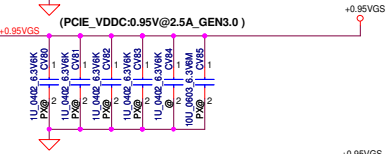
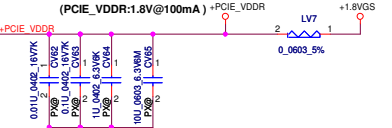
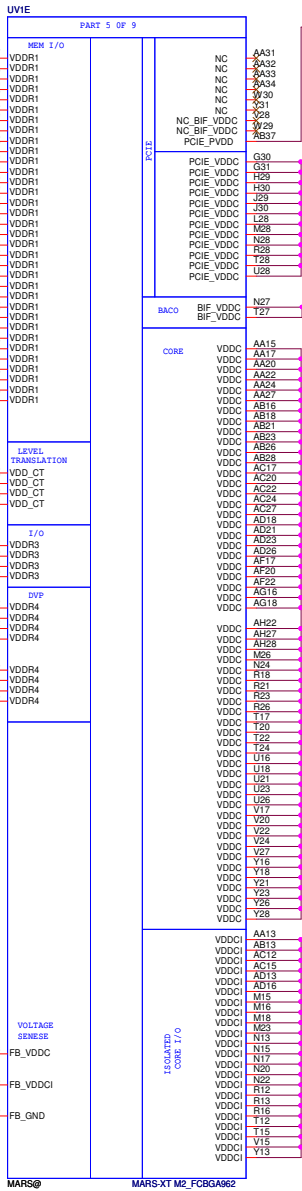
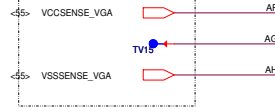
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



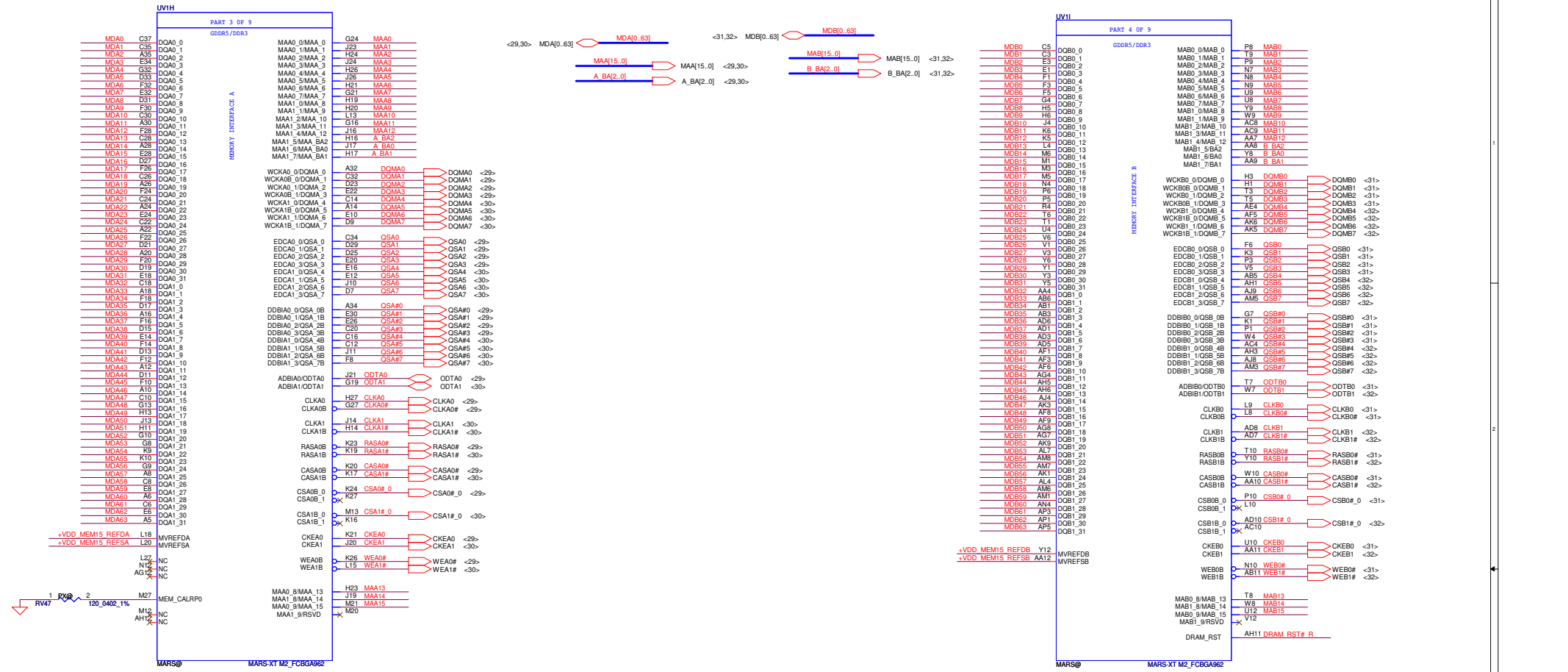
Route as differential pair



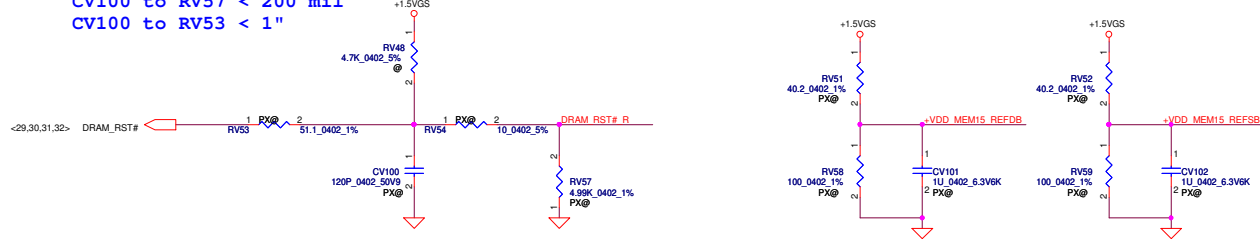
PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

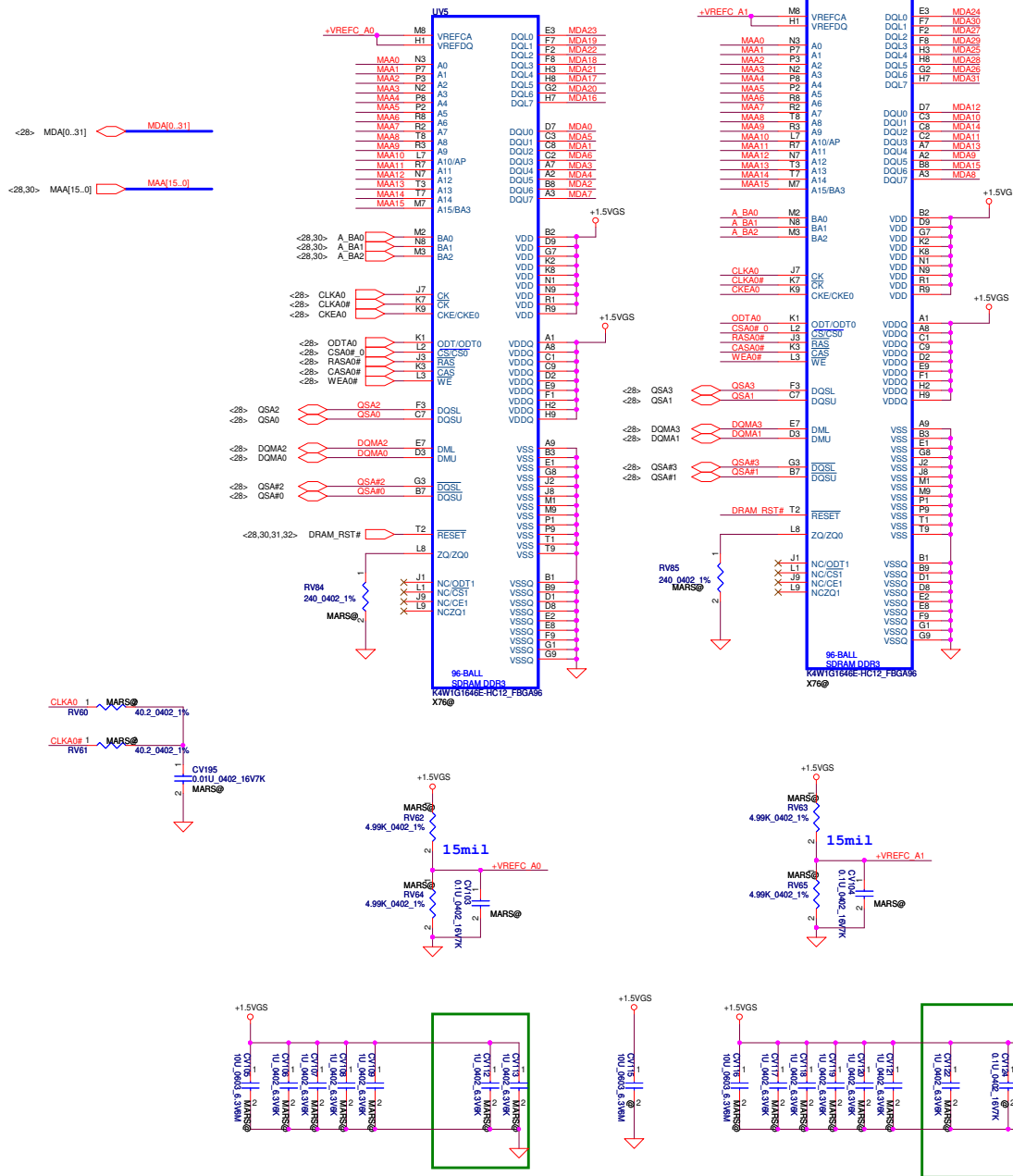
VGA_CORE Cap in power side sheet

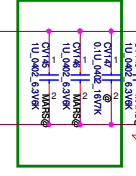
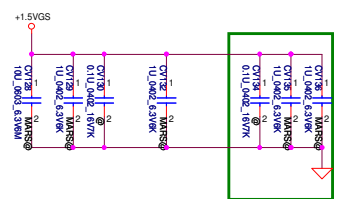
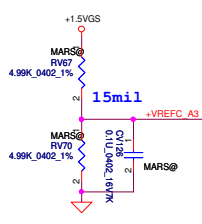
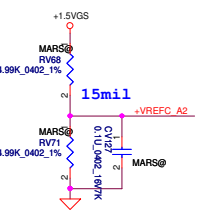
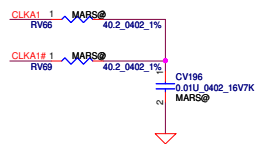
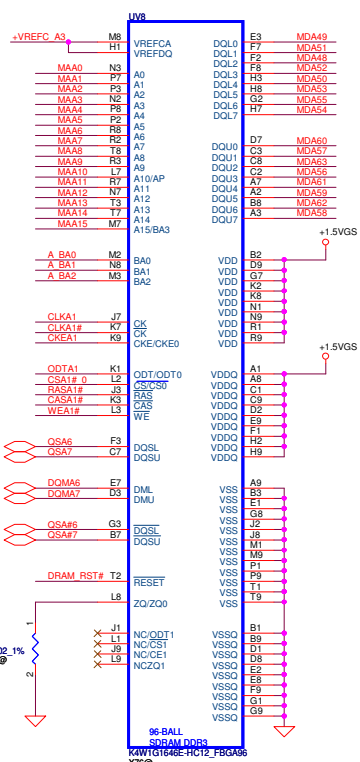
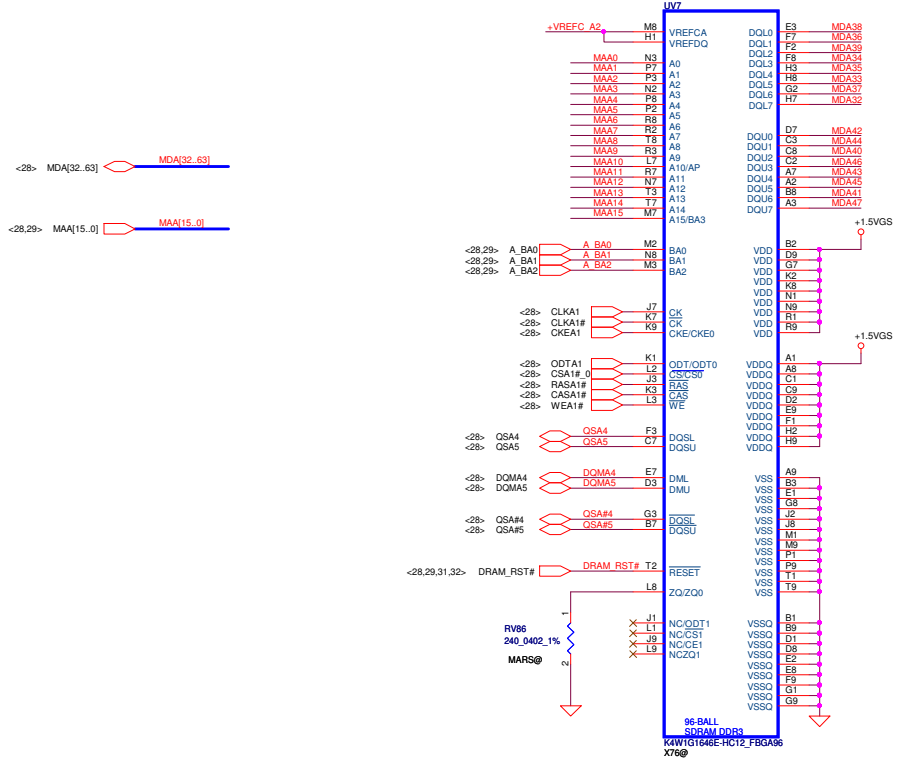


Ball to RV57 < 1"
 CV100 to RV57 < 200 mil
 CV100 to RV53 < 1"

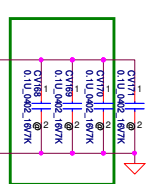
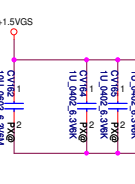
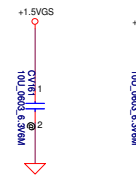
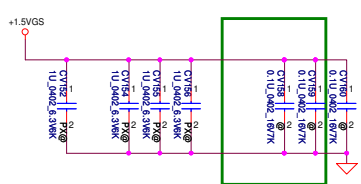
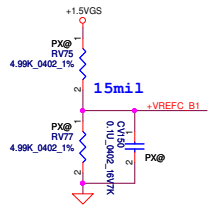
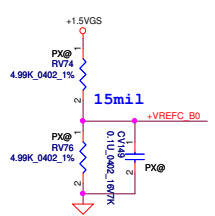
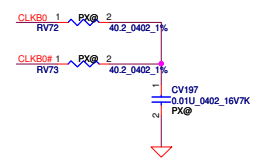
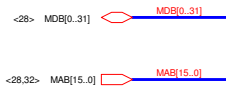
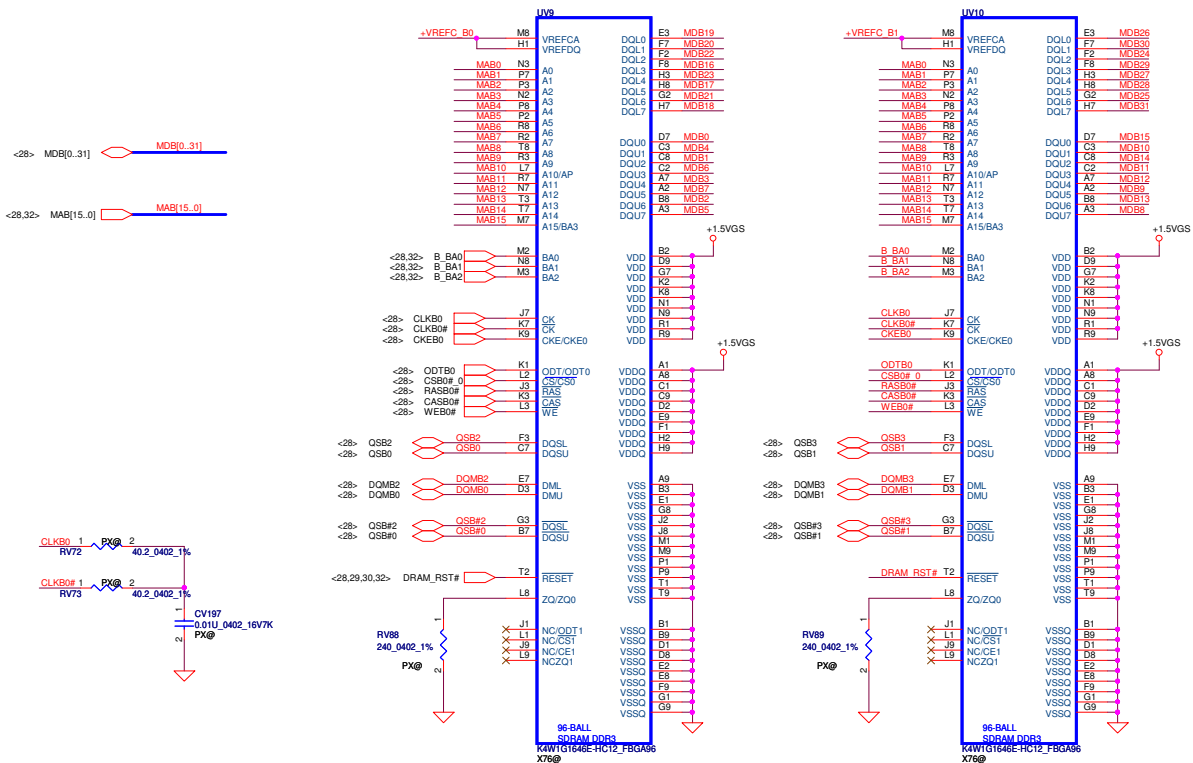


DRAM_RST# is a daisy-chain net that connects to all VRAM
 This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and |I Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
 Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

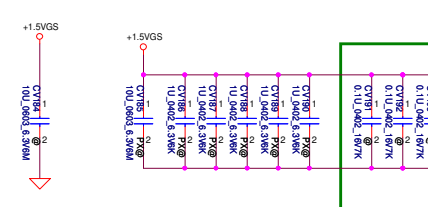
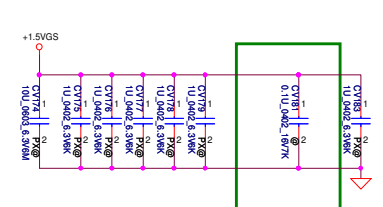
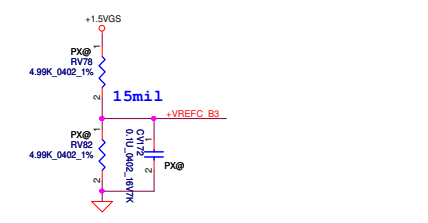
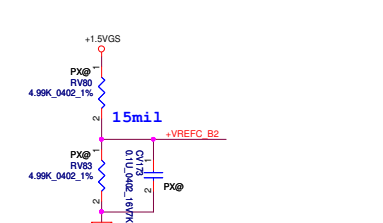
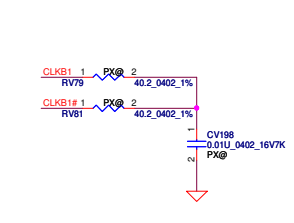
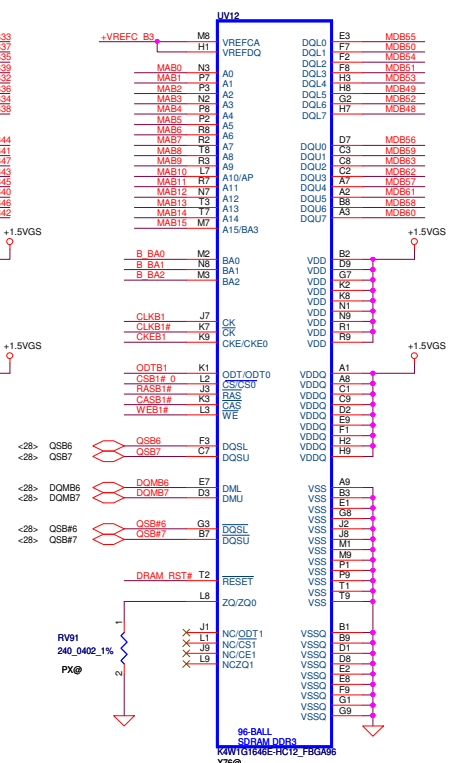
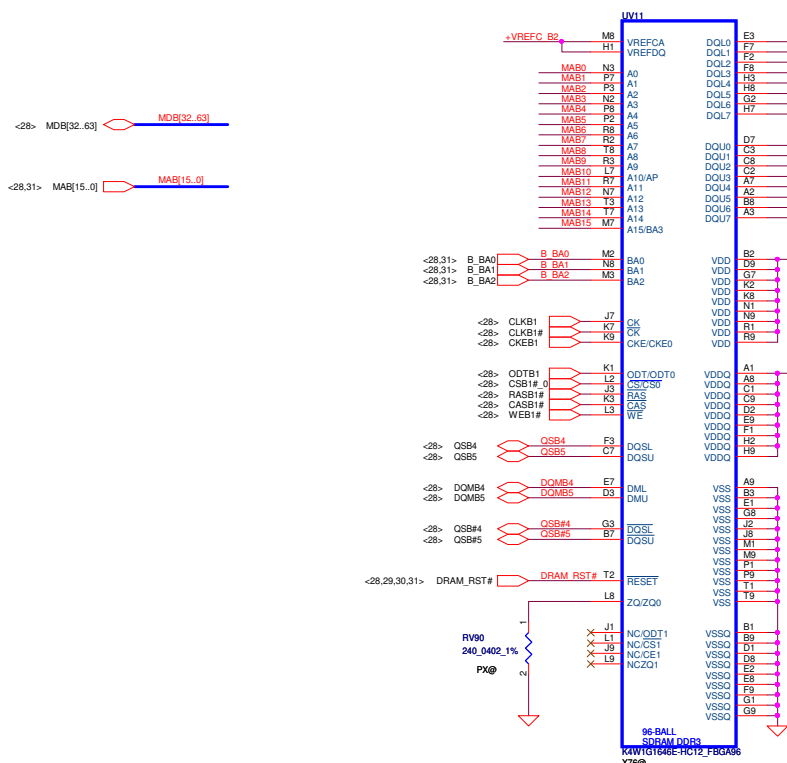




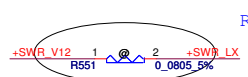
Security Classification	Compal Secret Data		2012/08/25		Title	
Issued Date	2010/08/25	Deciphered Date	2012/08/25	ATI Whistler M2 VRAM A		
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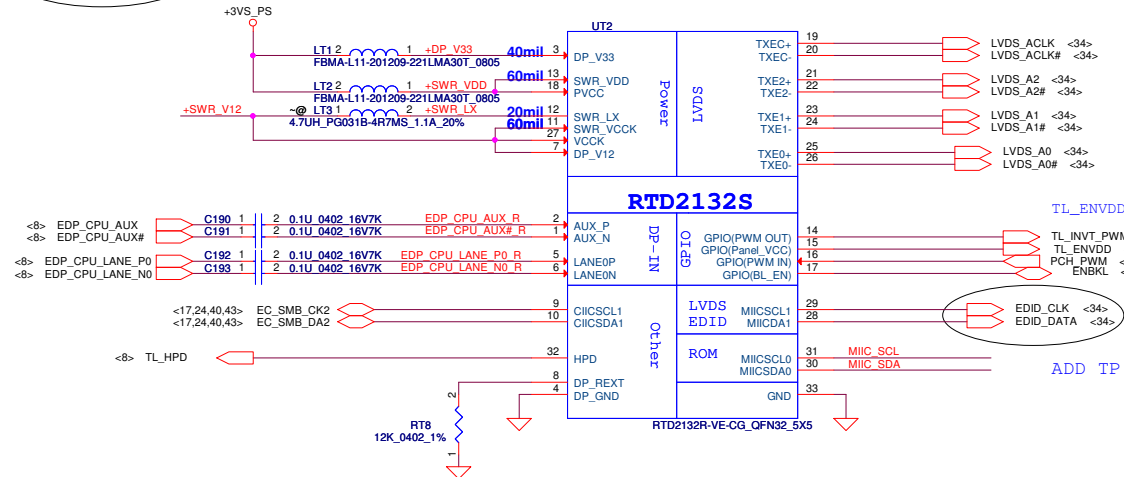
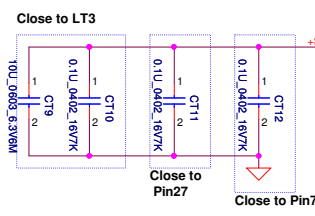
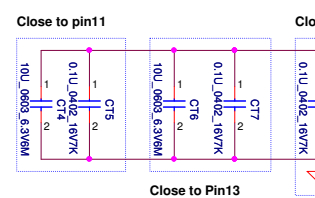
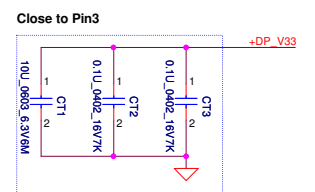
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Issued Date	2010/08/25	Deciphered Date	2012/08/25	ATI Whistler M2 VRAM B
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Size	C	Document Number	LA-9641P	Rev
Date:	Friday, April 18, 2013	Sheet	32	of 61

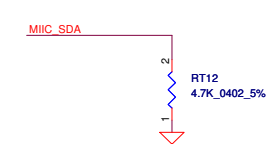
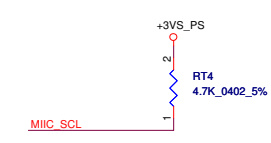
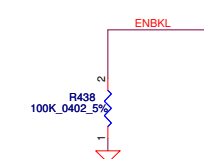


RTD2132R LDO MODE



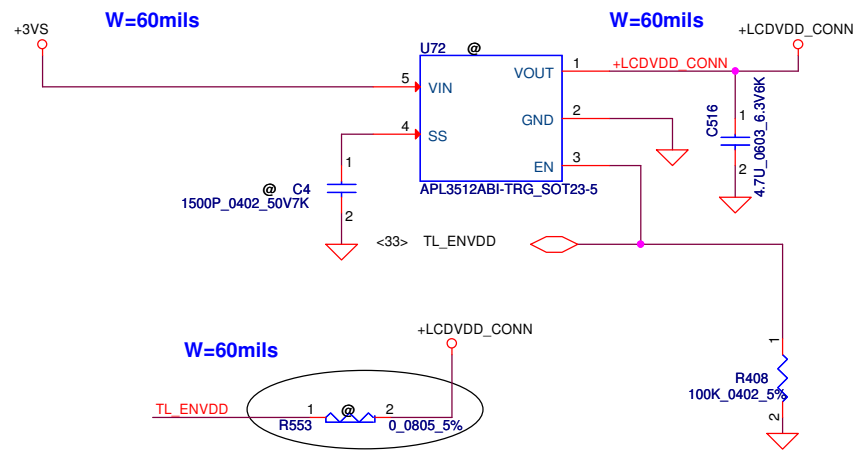
TL_ENVDD need 60 mil if use for LVDS power on R version

ADD TP on trace or via

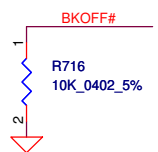
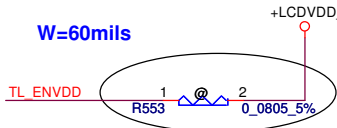


	MIIC_SDA	0	1
MIIC_SCL		X	EC CODE
		1	Internal ROM

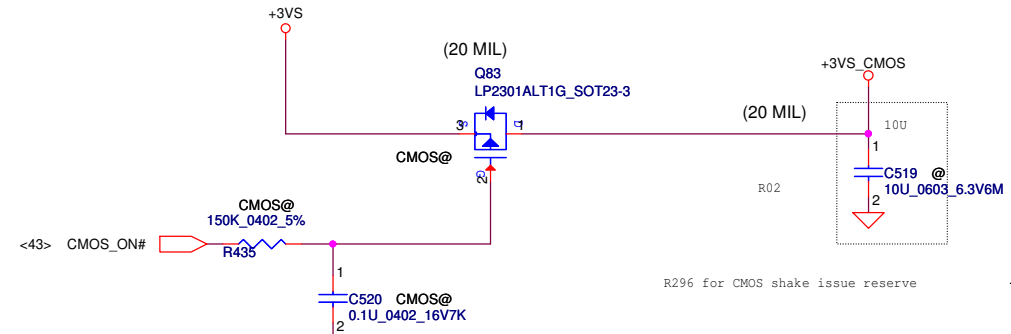
LCD POWER CIRCUIT



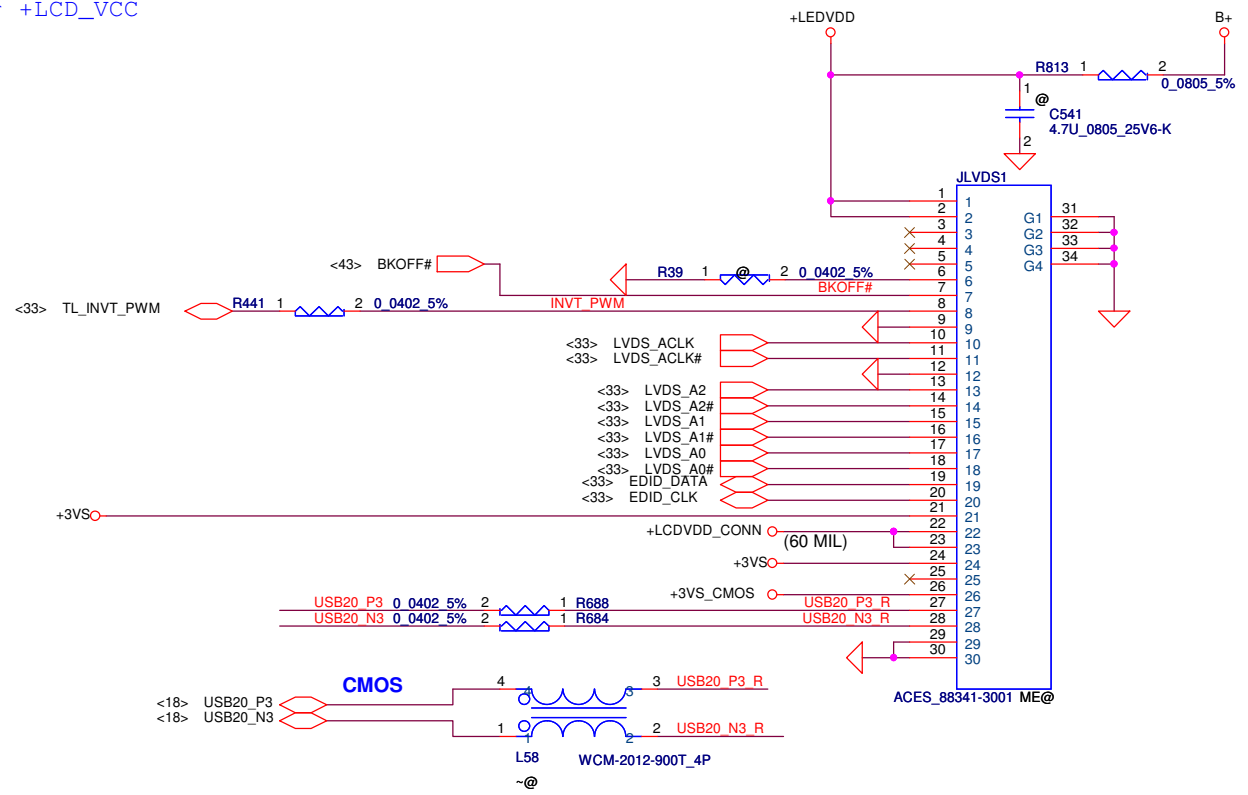
RTD2132R Internal load switch for +LCD_VCC



CMOS Camera

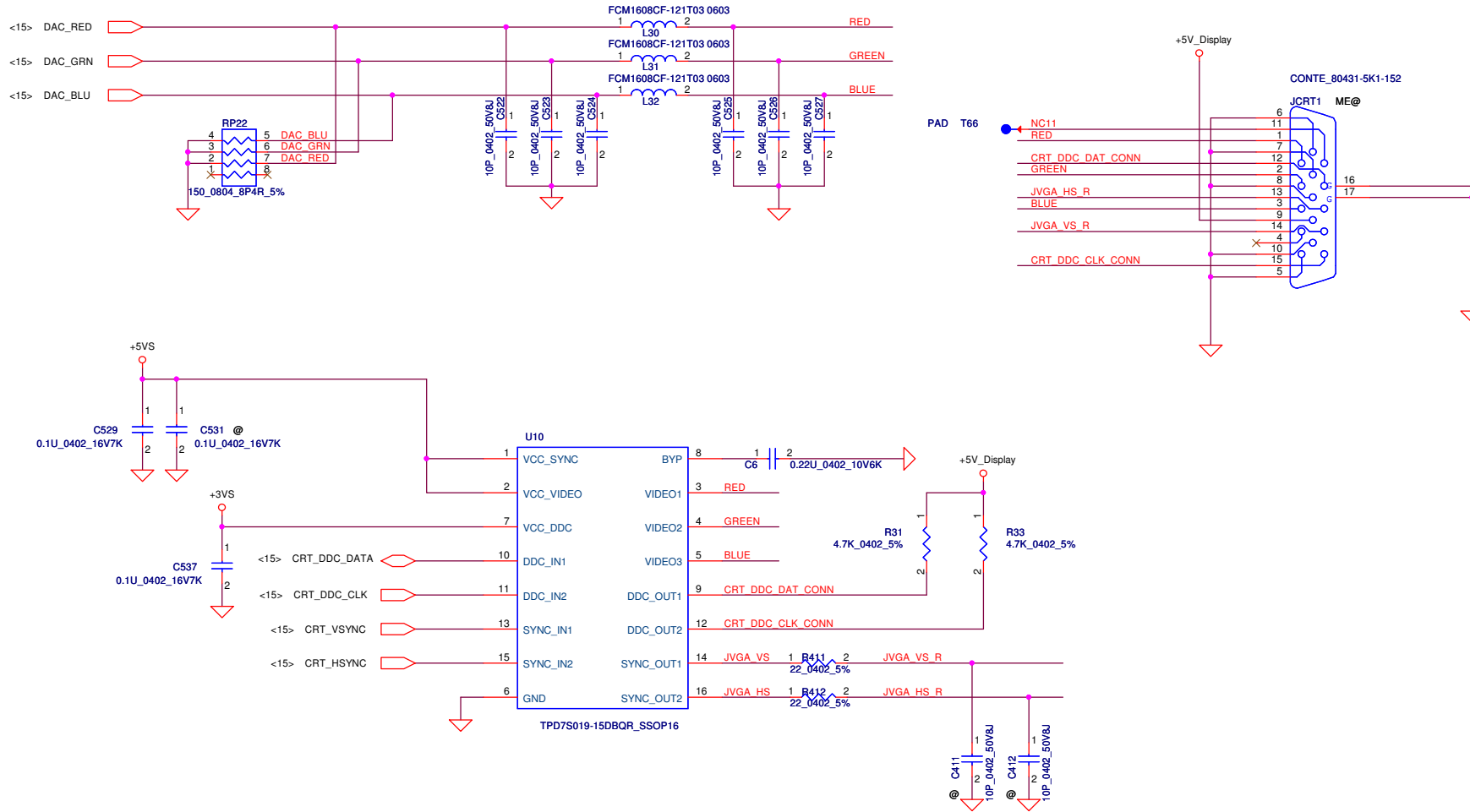


VGA LCD/PANEL BD. Conn.

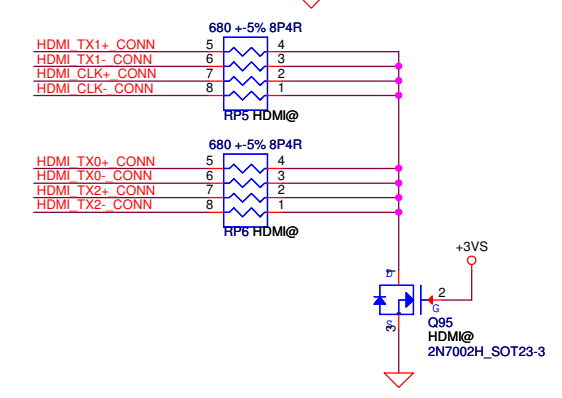
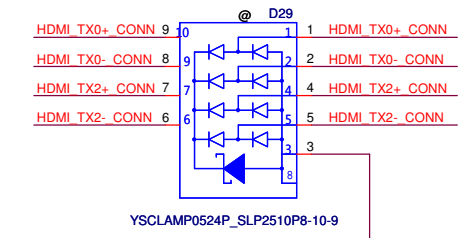
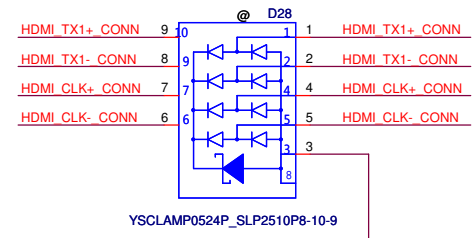
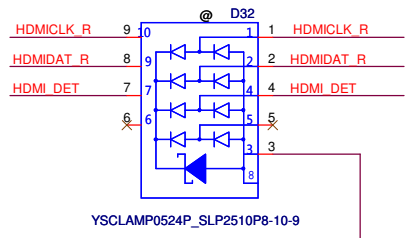
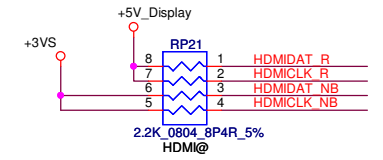
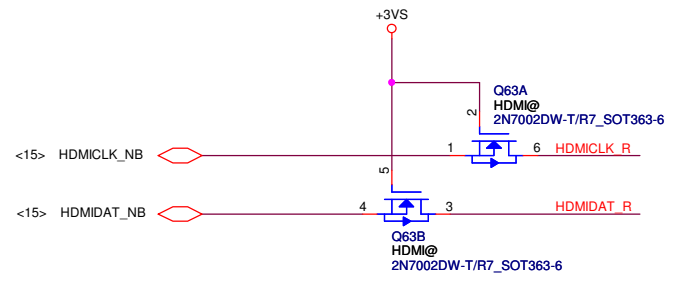
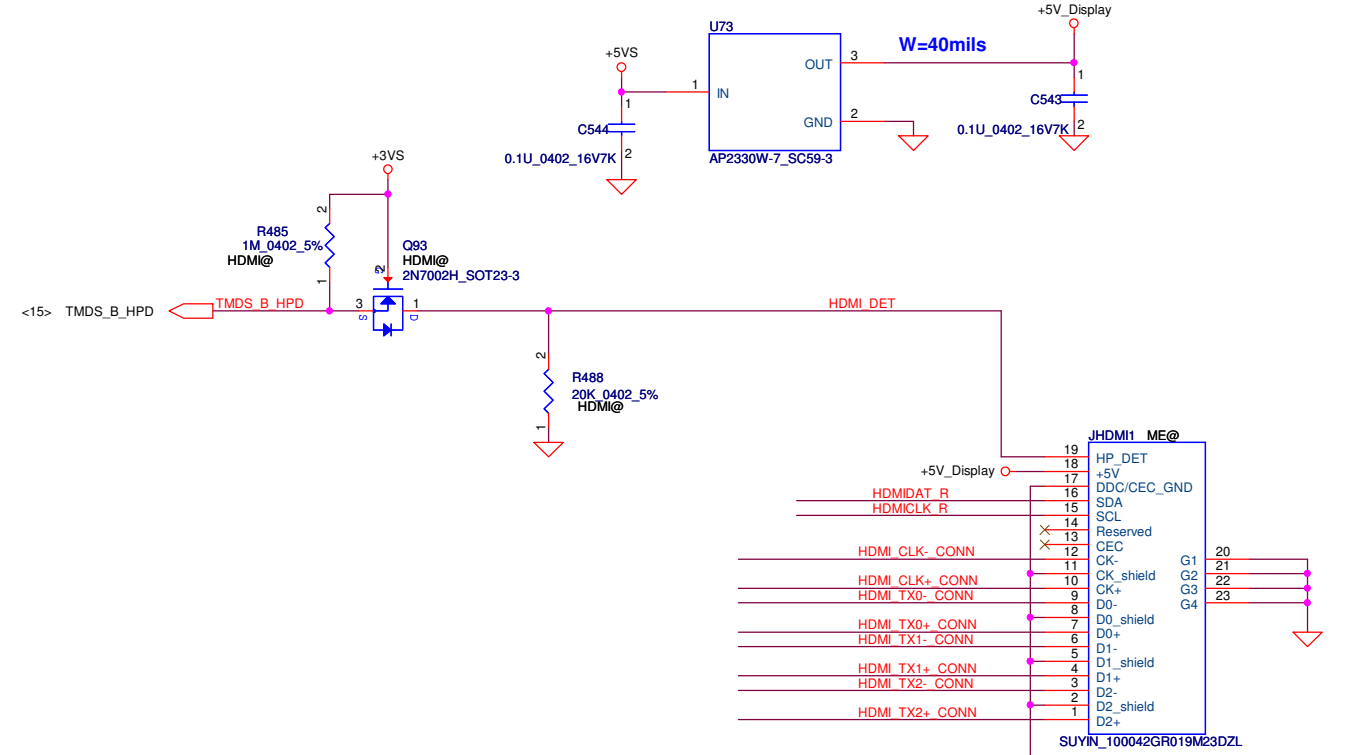
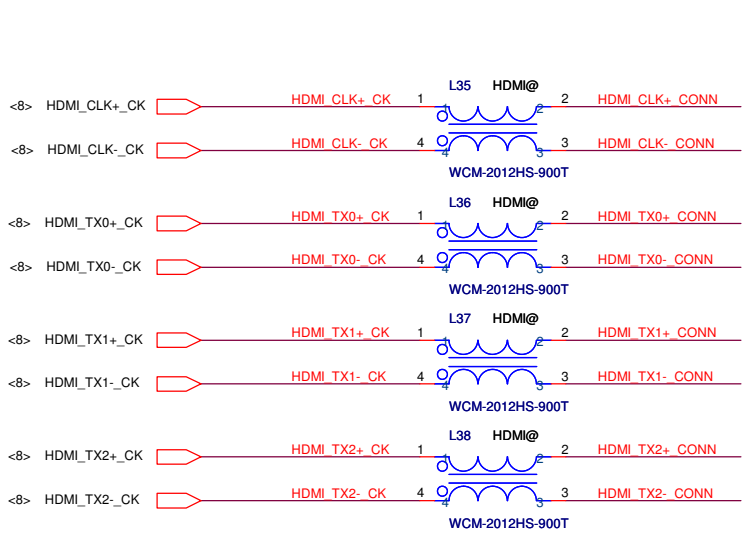


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Size	Document Number	Date:		Friday, April 19, 2013
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CRT Connector

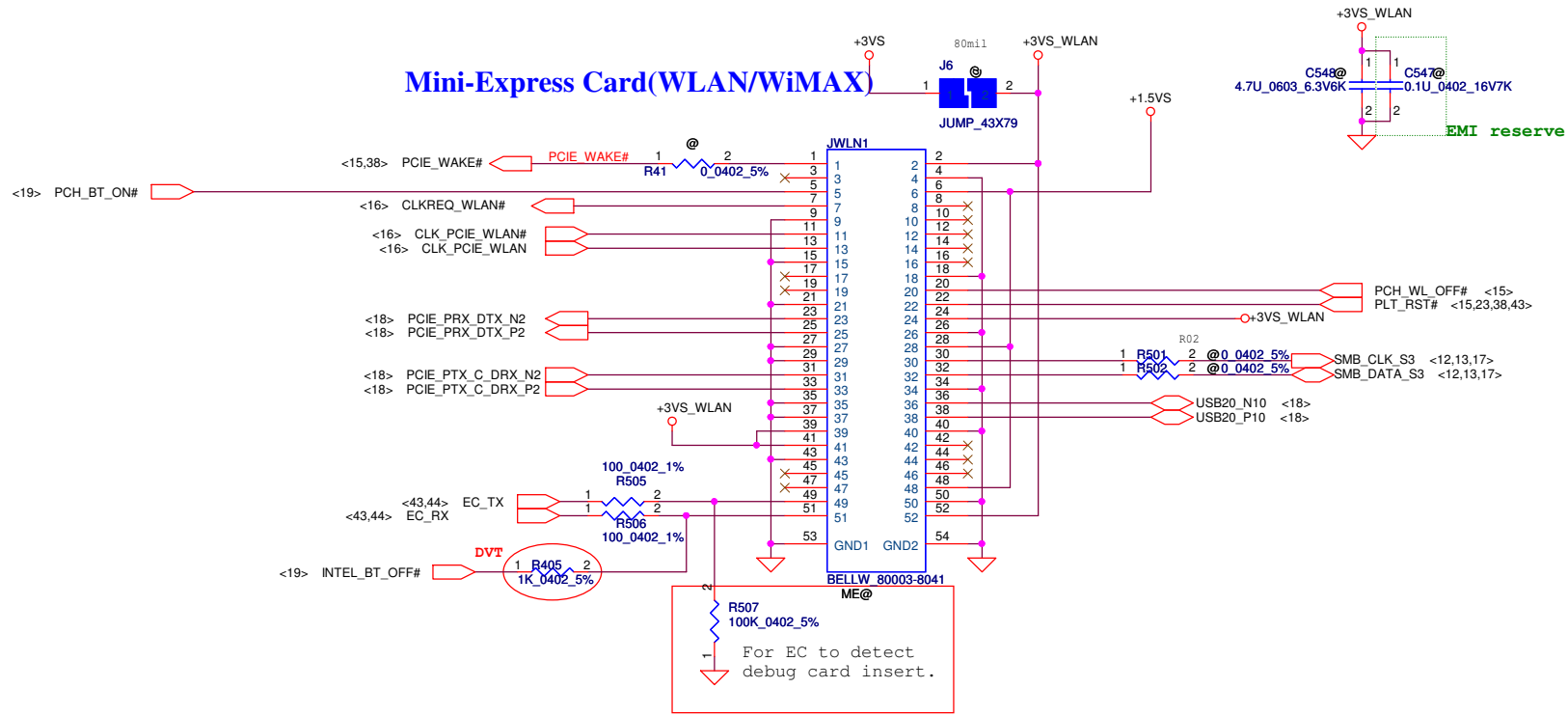


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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Size	Custom	Document Number	LA-9641P	Rev	1.0
Date:	Friday, April 19, 2013	Sheet	35	of	61

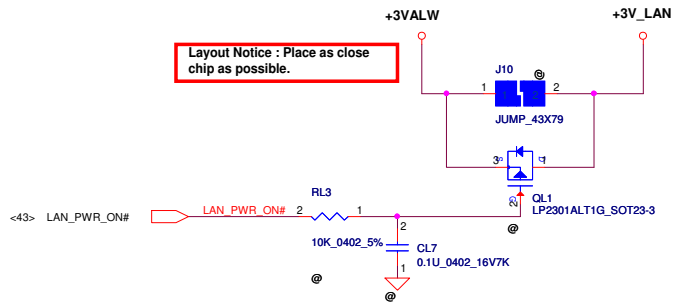


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				Date: Friday, April 19, 2013	Sheet 36 of 61

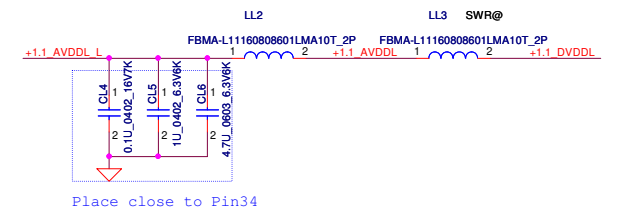
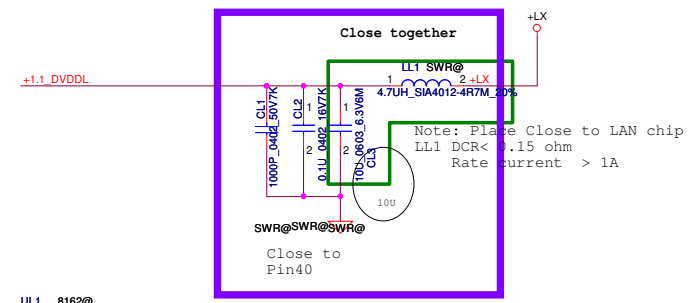
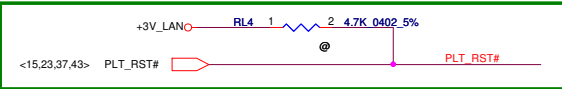
Mini-Express Card for WLAN/WiMAX(Half)



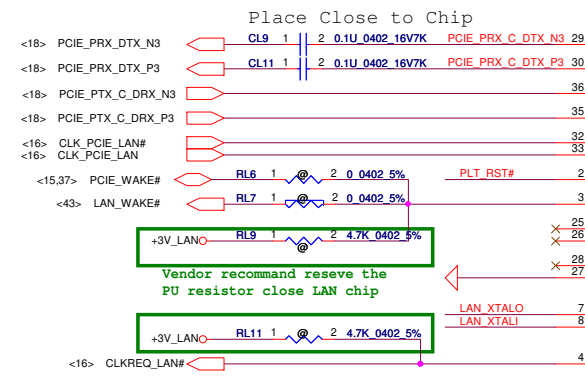
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title Mini-Card/NEW Card/SIM	
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Vendor recommend reseve the PU resistor close LAN chip



SA000065410 S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL
 SA000052J20 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL



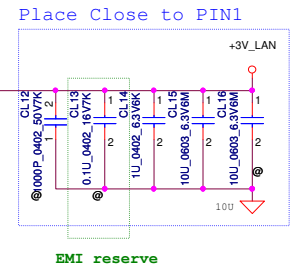
Vendor recommend reseve the PU resistor close LAN chip

Near Pin13
Near Pin19
Near Pin31

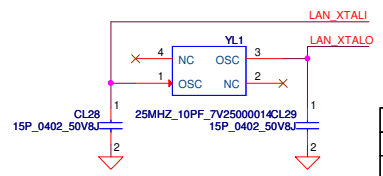
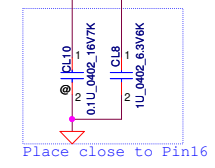
Near Pin6

mount RL12 if use LDO modue

Place Close to PIN1



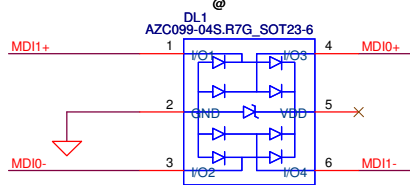
EMI reserve



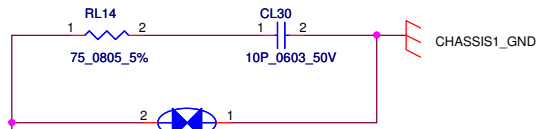
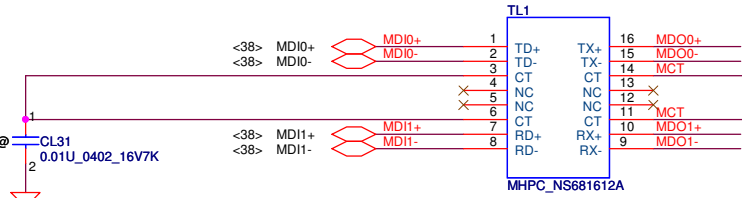
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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DL1
 1'S PN:SC300001G00
 2'S PN:SC300002E00

Place Close to TL1



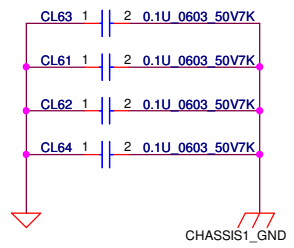
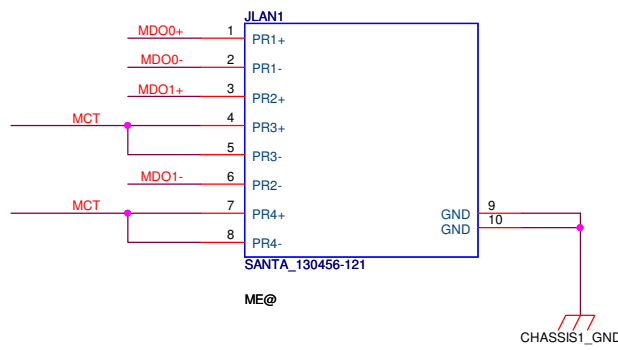
Reserve gas tube for EMI go rural solution



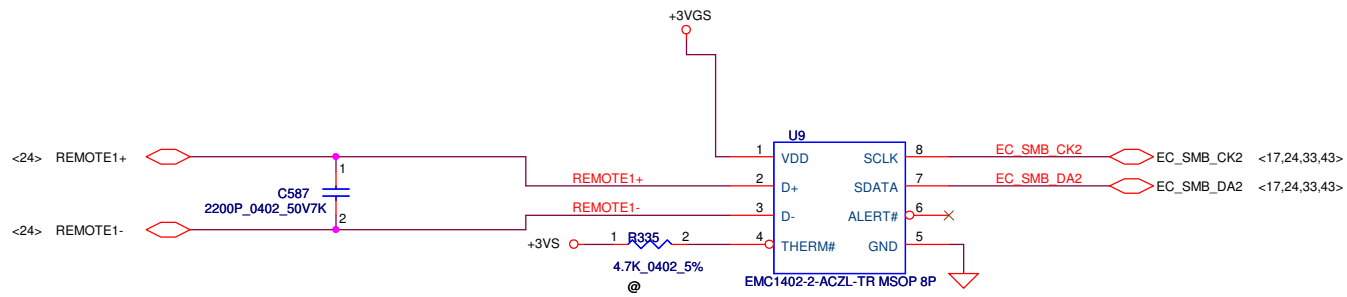
Place Close to TL1

DLL1
 BS4200N-C-LV_SMB-F2
 GAS@

Need check Symbol



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				LA-9641P	1.0
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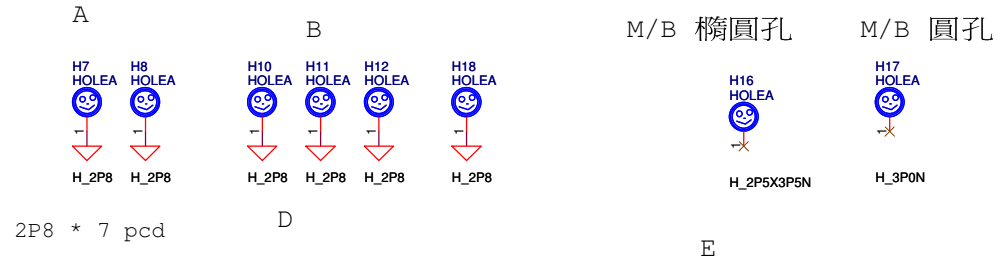
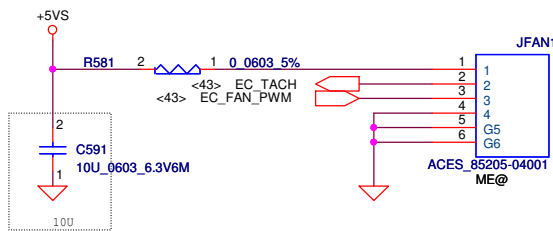


EMC1412-A (SA00003YA00)
 Address 1111_100xb
 SIC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1, 2+/-:
 Trace width/space: 10/10 mil
 Trace length: <8"

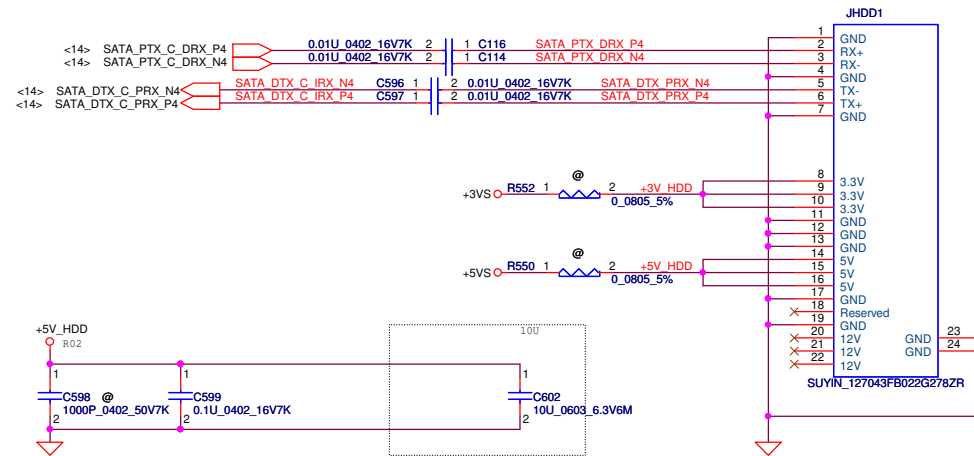


FAN1 Conn

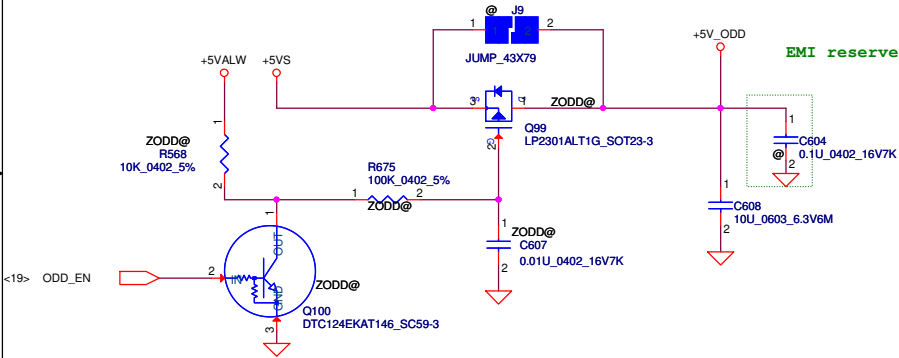


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Fintek-Thermal IC/FAN/screw
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				Date: Friday, April 19, 2013	Sheet 40 of 61

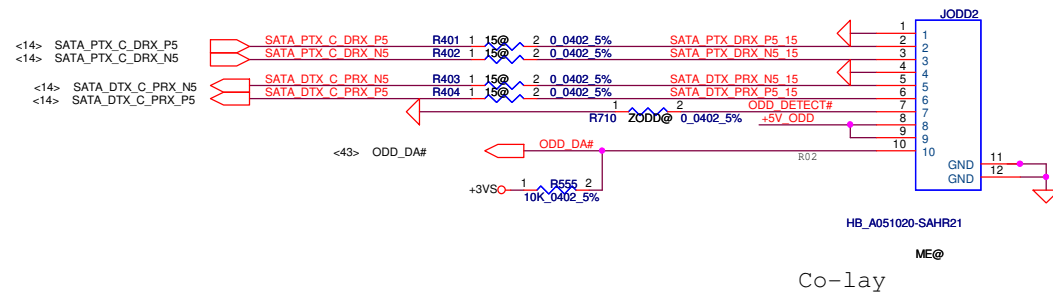
SATA HDD Conn.



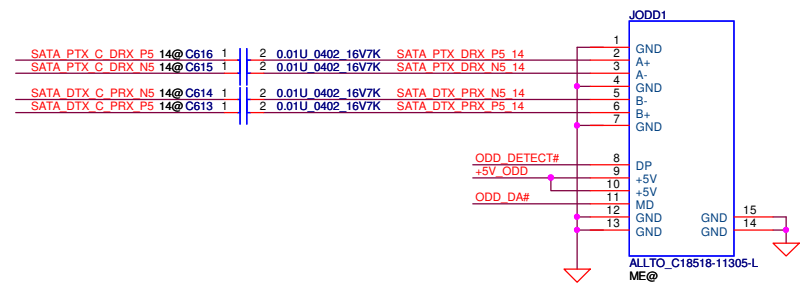
ODD Power Control



FOR 15" SATA ODD FFC Conn.

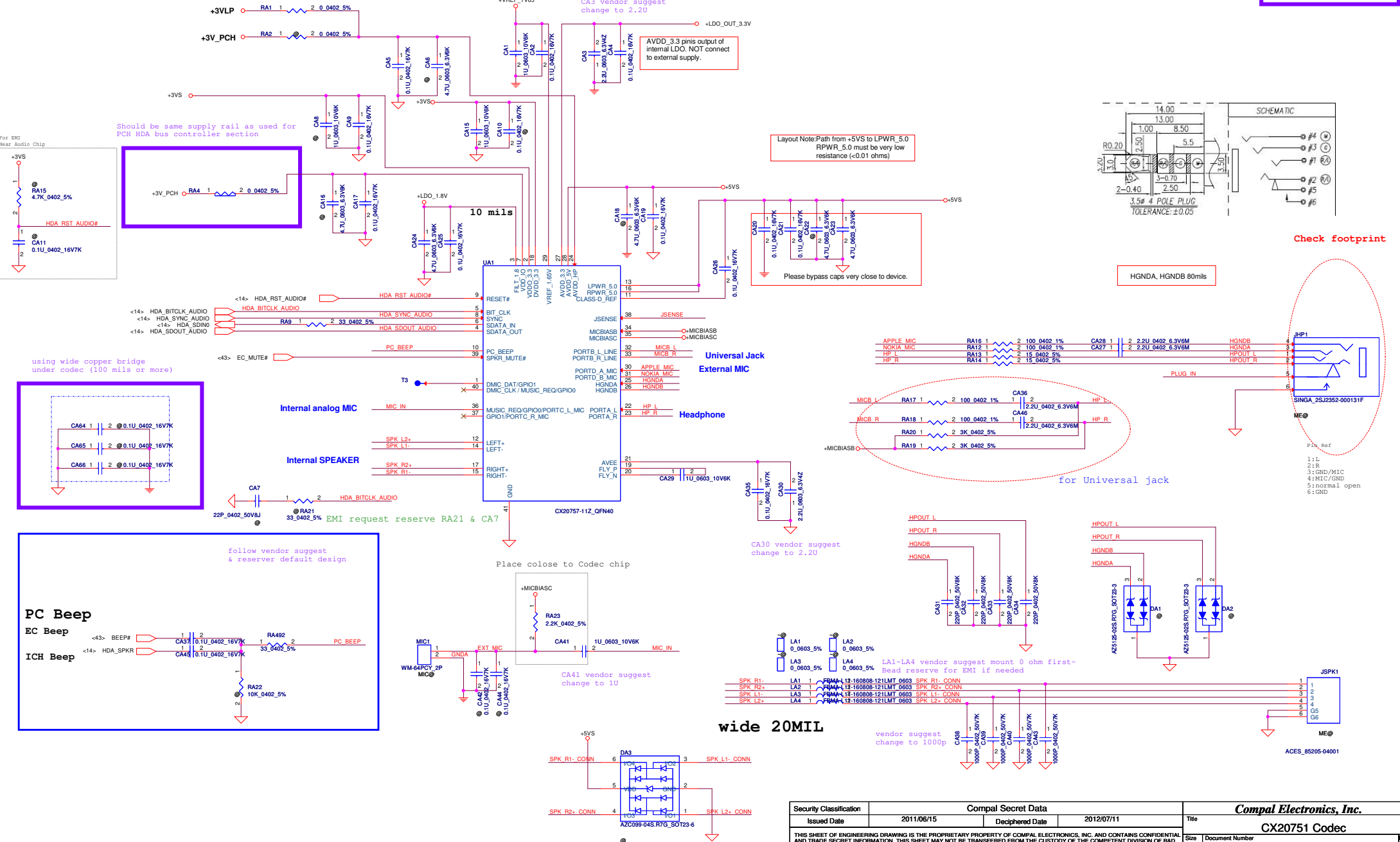


FOR 14" SATA ODD Conn.



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CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Sense resistors must be connected same power that is used for VAUX_3.3

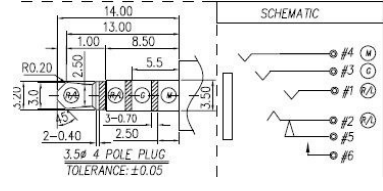
mount RA6 on the Jack Sense circuit to configure Port-C for mono MIC.

Don't support LINE_IN function RA7 could be @

AVDD_3.3 pins output of internal LDO. NOT connect to external supply.

Layout Note: Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

Please bypass caps very close to device.



Check footprint

HGNDA, HGNCB 80mils

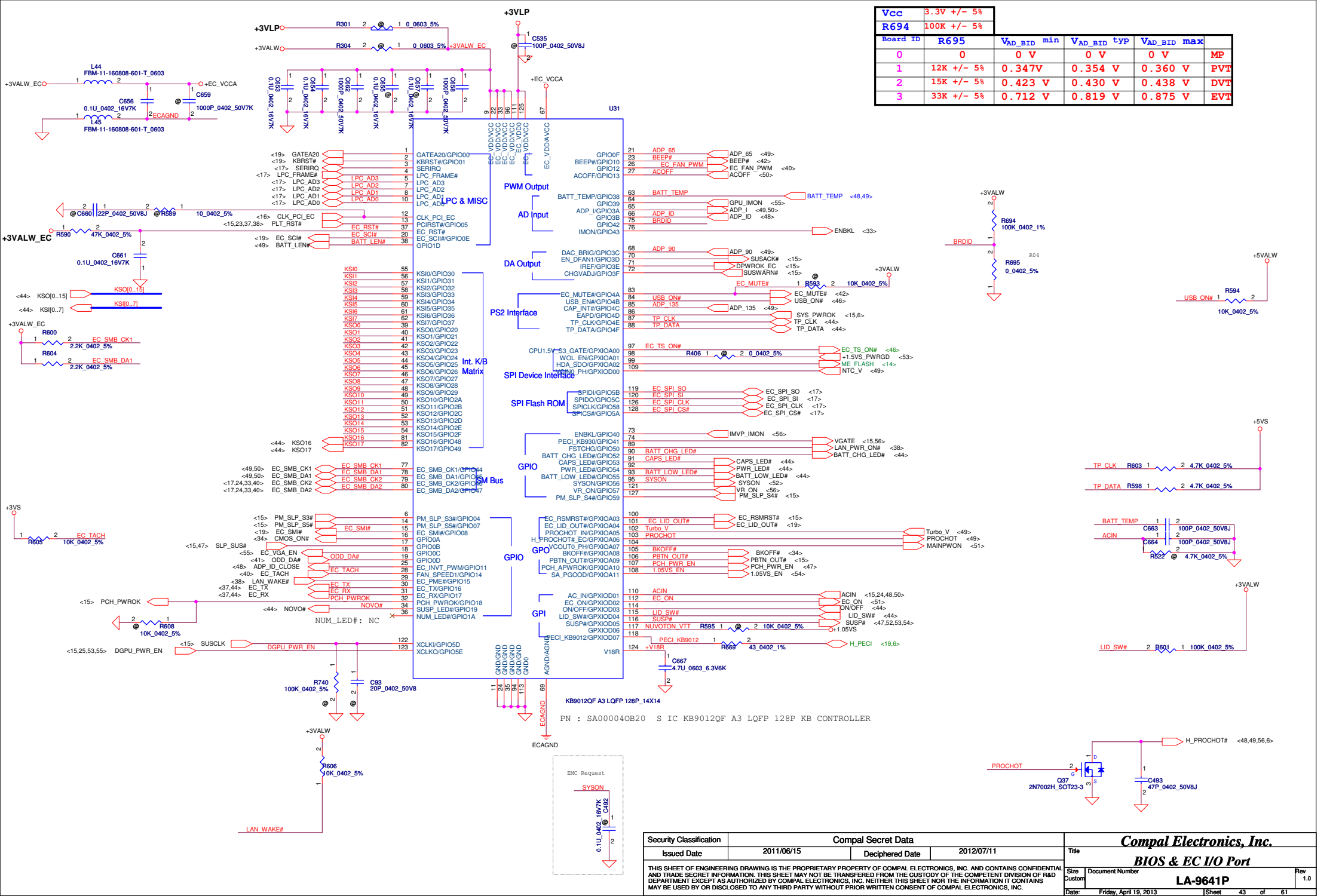


for Universal jack

wide 20MIL

vendor suggest change to 1000p

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Size	Document Number	Rev	LA-9641P		
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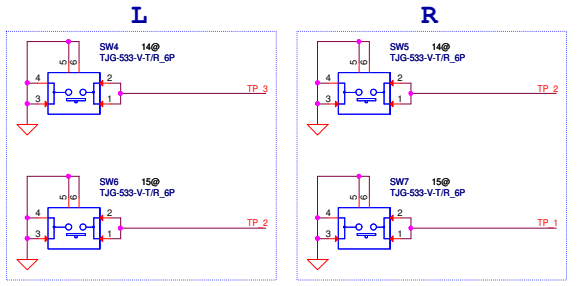
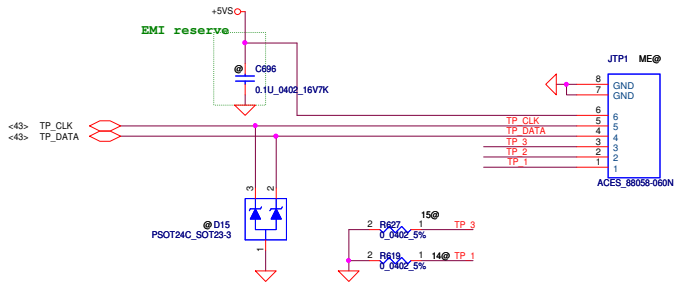
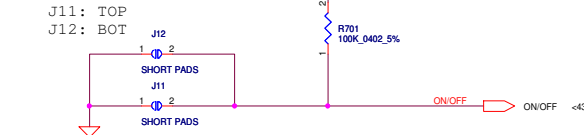
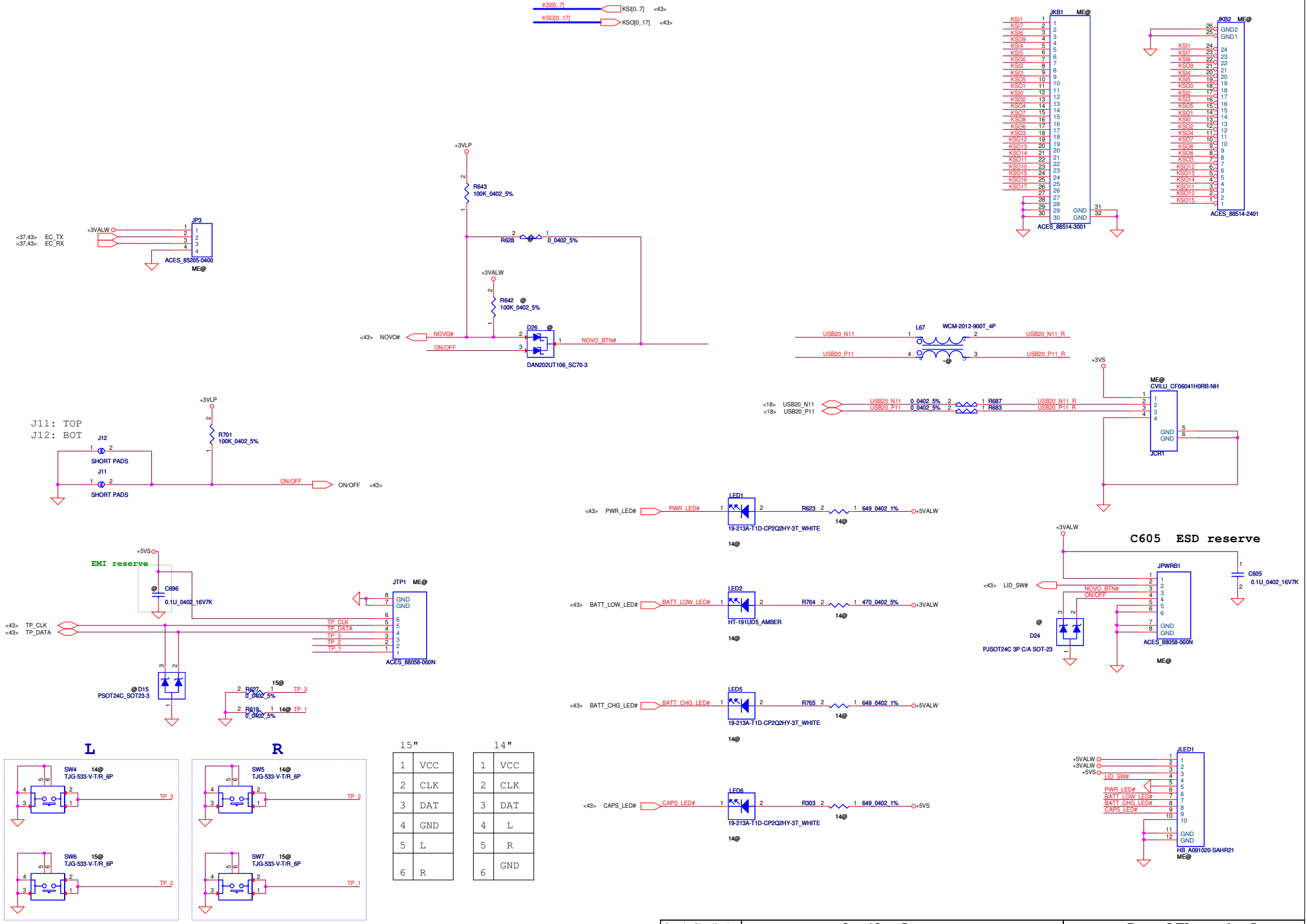


Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	VAD_BID min	VAD_BID typ	VAD_BID max	MP
0	0	0 V	0 V	0 V	MP
1	12K +/- 5%	0.347V	0.354 V	0.360 V	PVT
2	15K +/- 5%	0.423 V	0.430 V	0.438 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

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Compal Electronics, Inc.		
BIOS & EC I/O Port		
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15"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND

A

B

C

D

E

1

1

2

2

3

3

4

4

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				Sheet 45 of 61	

A

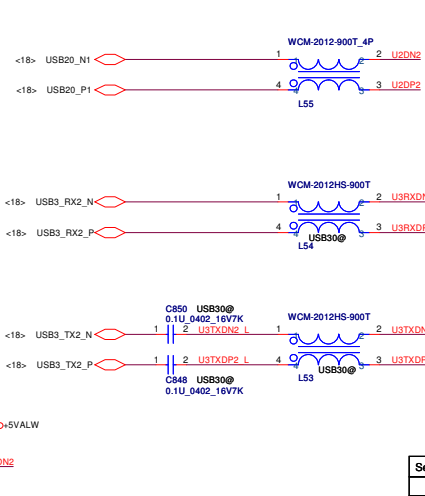
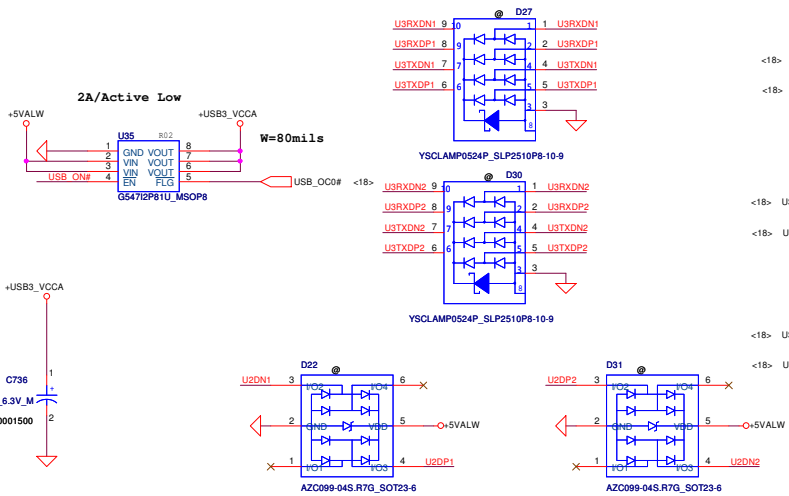
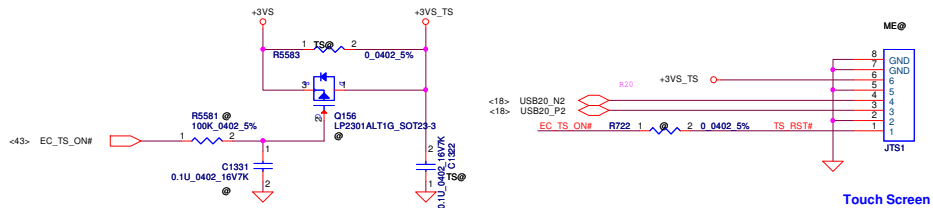
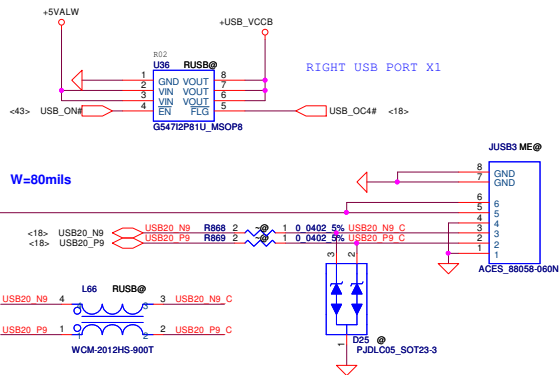
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C

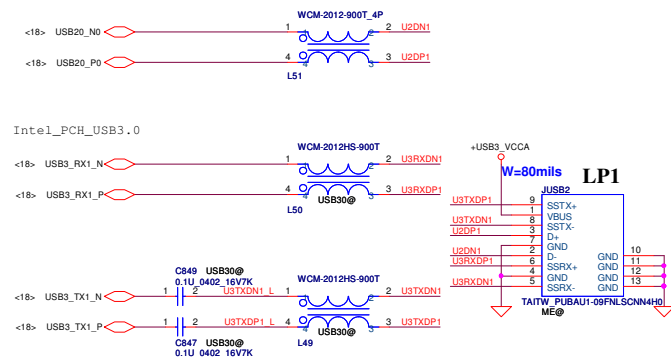
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E

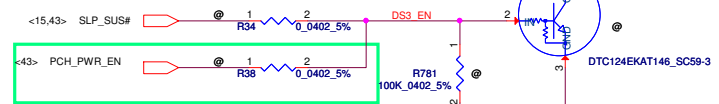
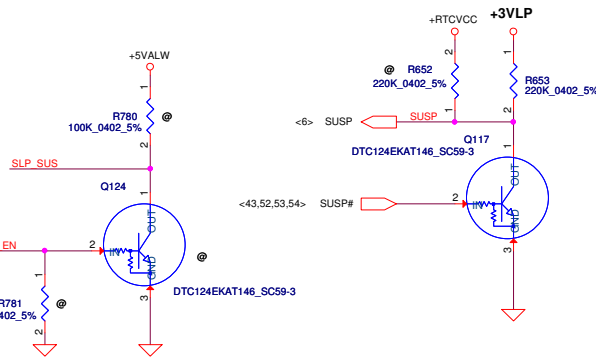
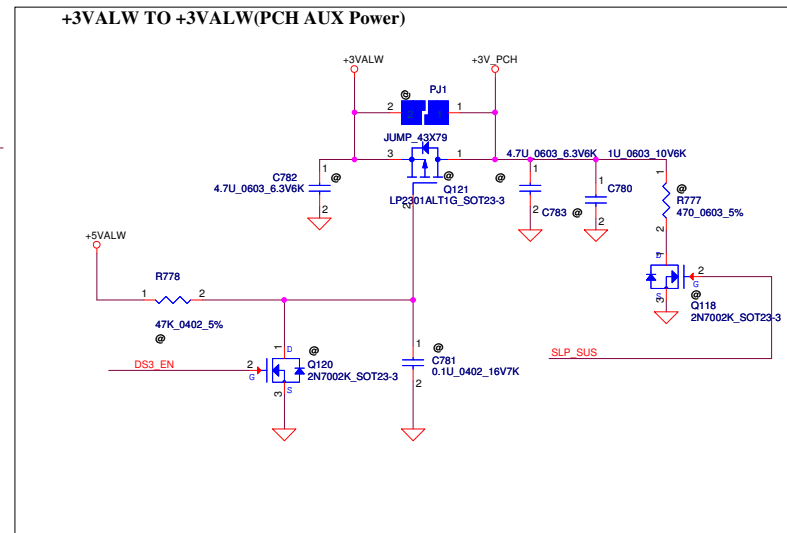
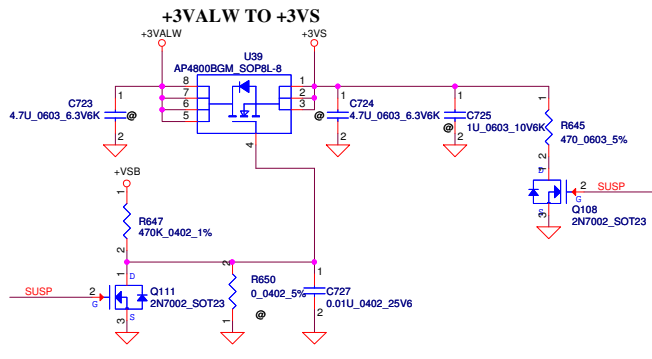
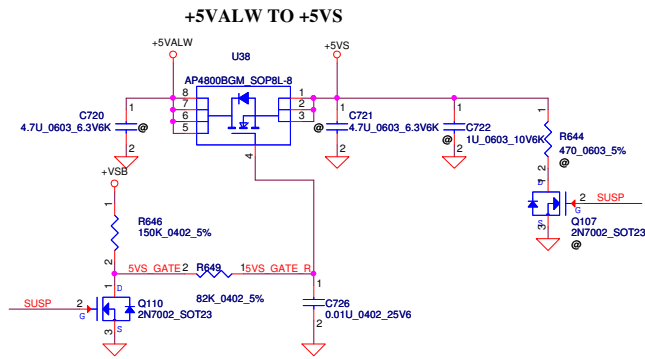
Right Ext.USB Conn.



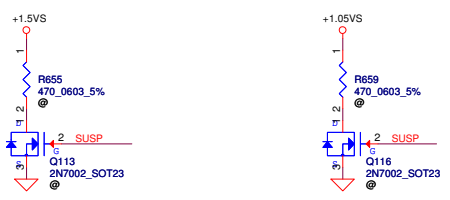
Intel_PCH_USB2.0



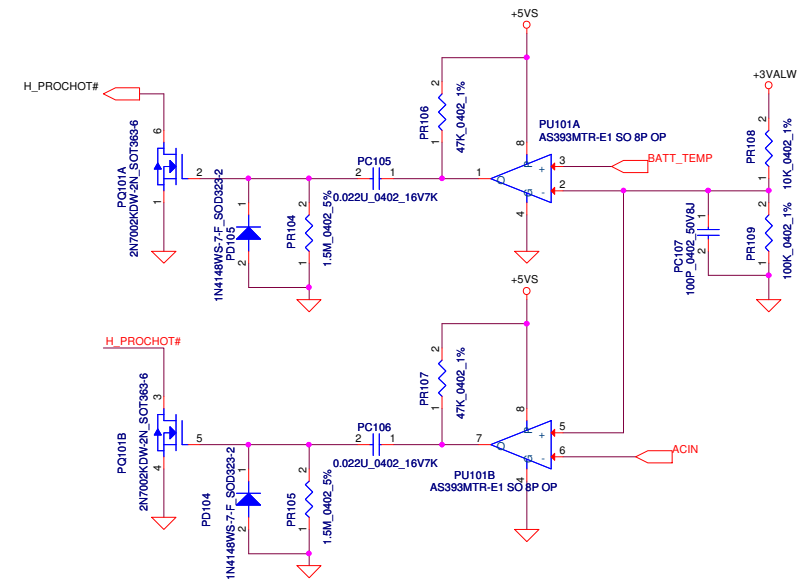
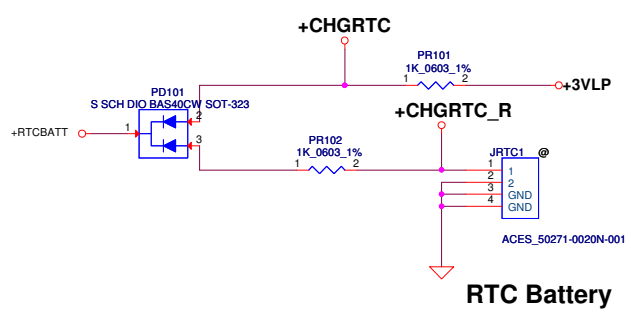
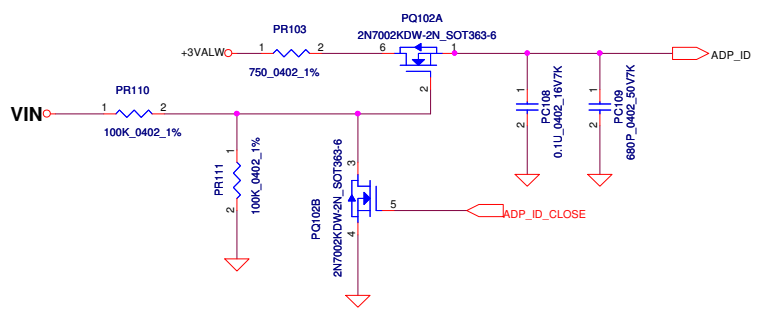
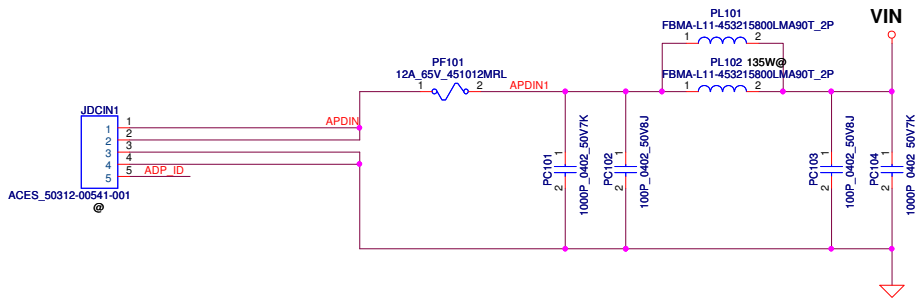
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				USB3.0/Left USB Ports
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先預留,C phase再決定



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Size	Custom	Document Number	LA-9641P	Rev	1.0
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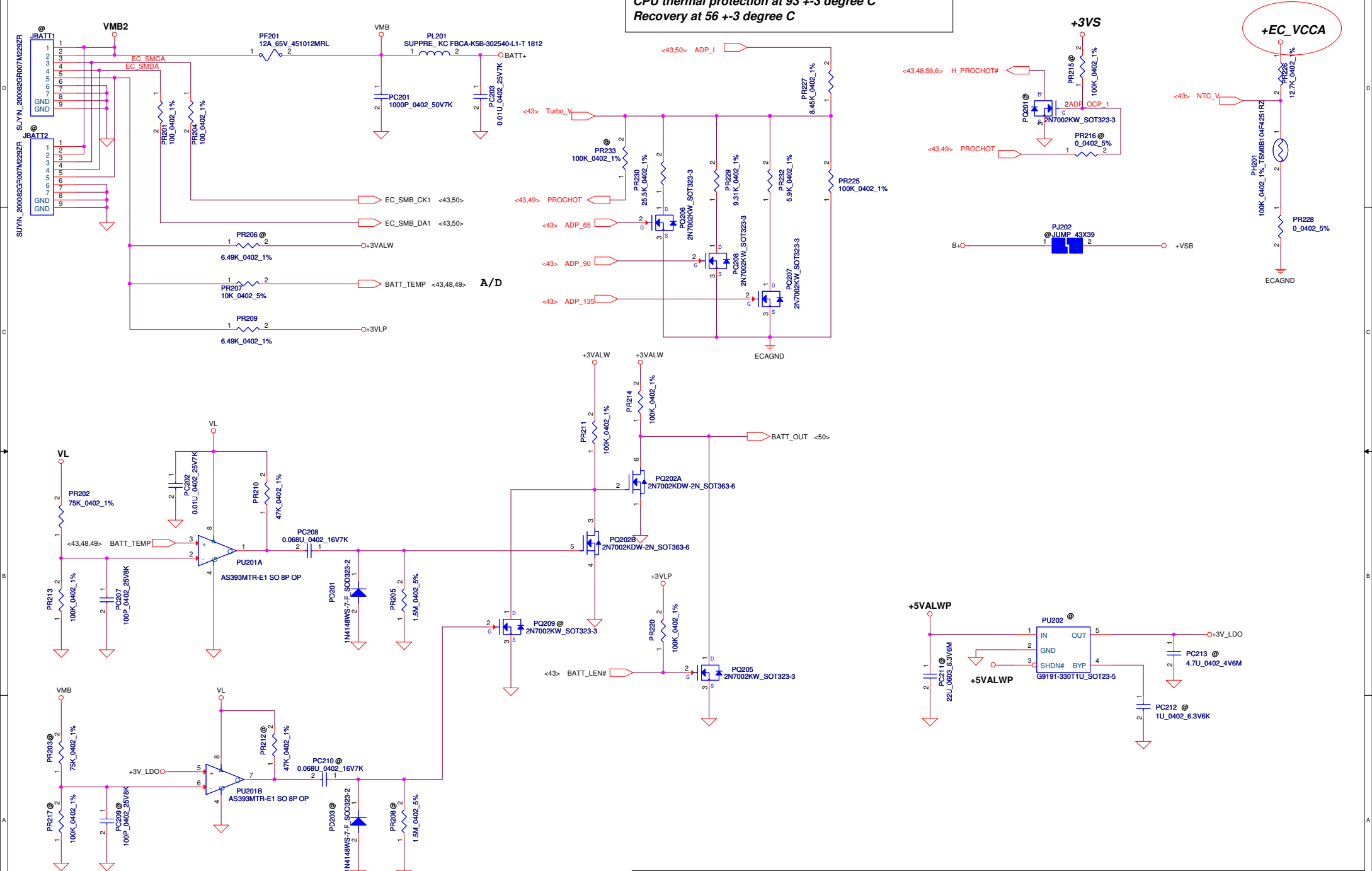


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PWR DCIN / RTC Battery	
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JBATT1 -15" JBATT2 -14"

PH201 under CPU bottom side :
 CPU thermal protection at 93 +3 degree C
 Recovery at 56 +3 degree C

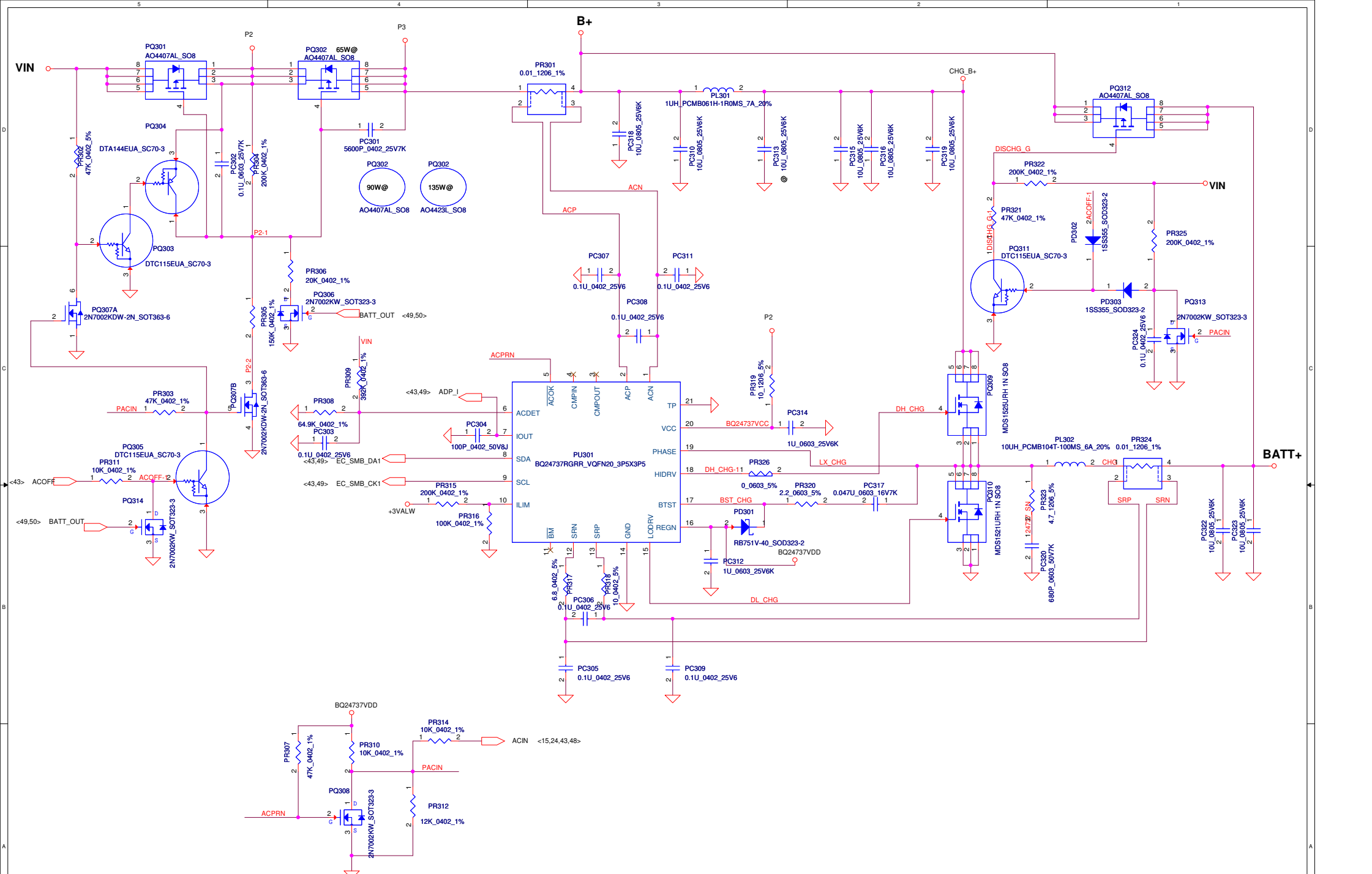


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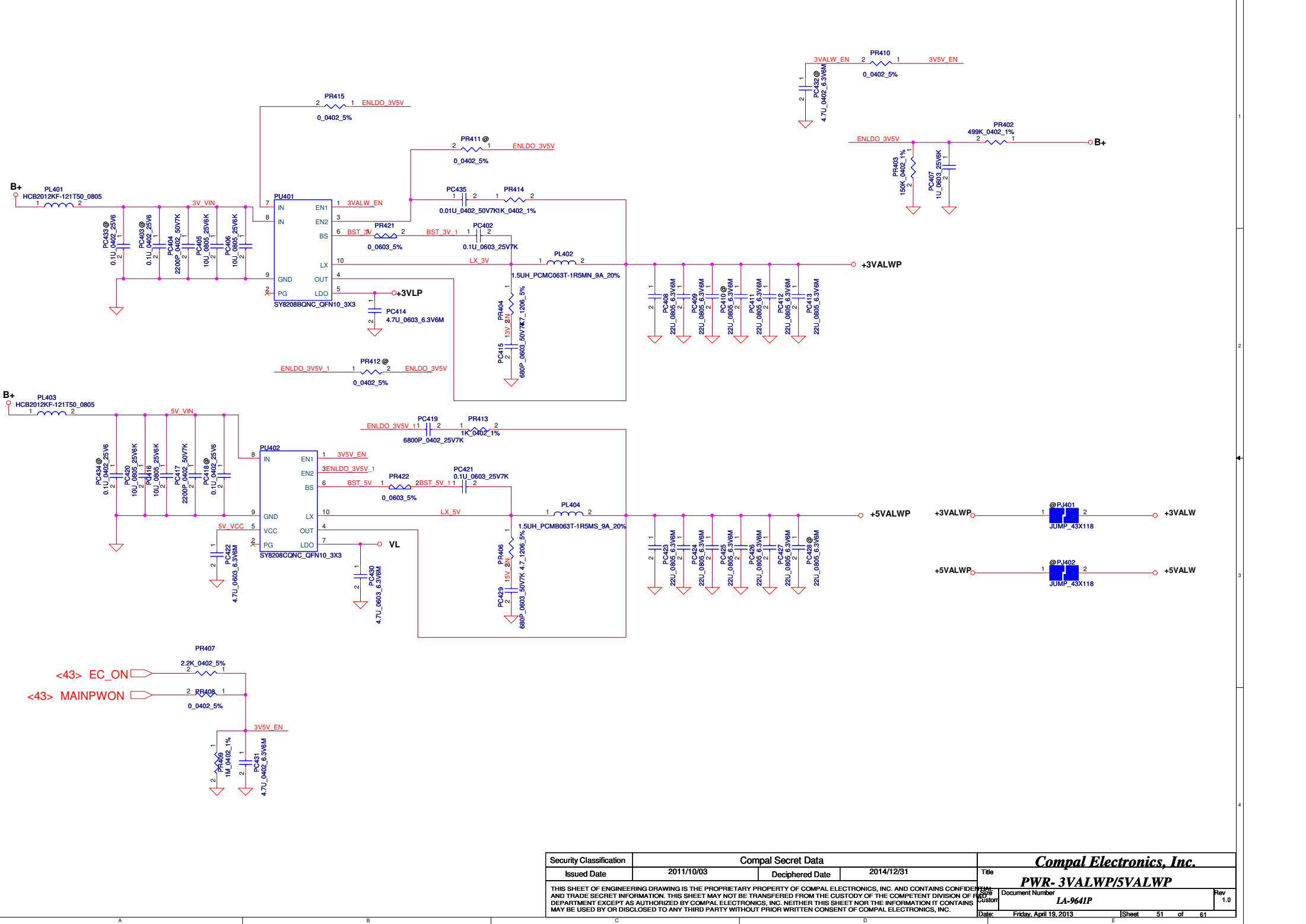
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PWR-BATTERY CONN/OTP

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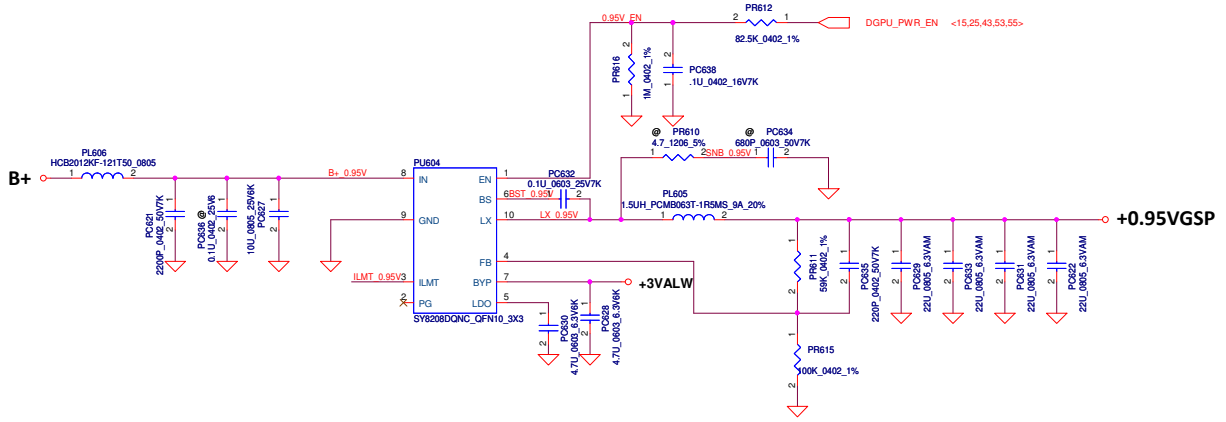
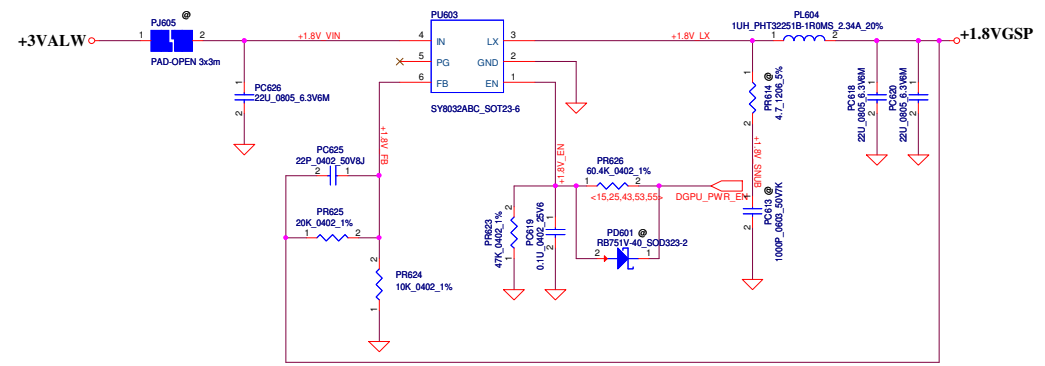
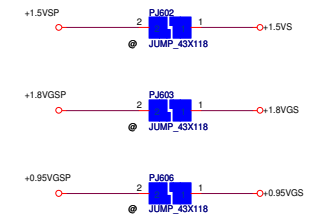
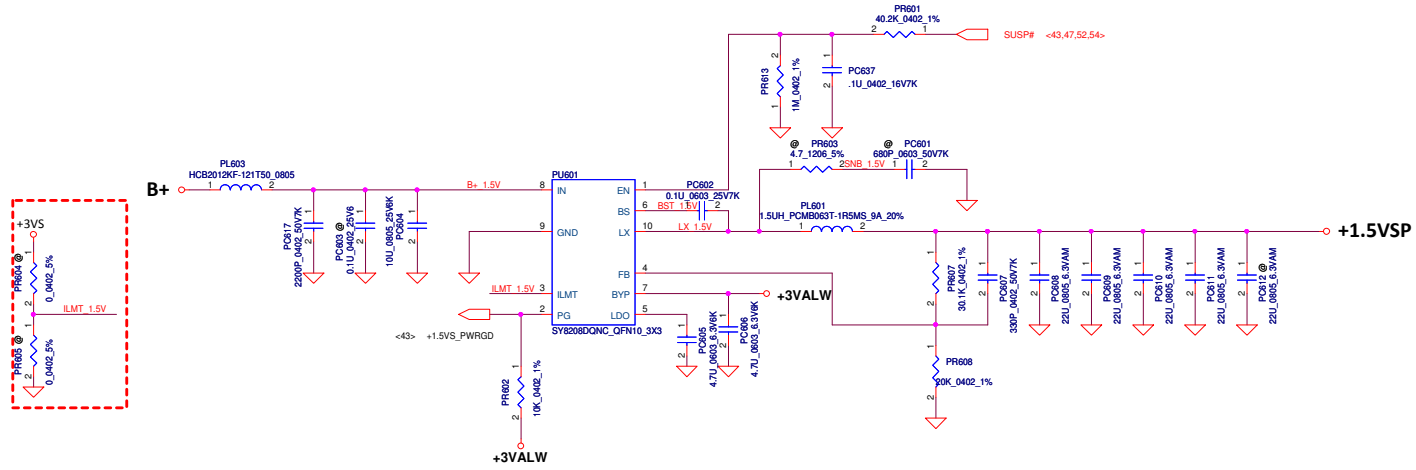


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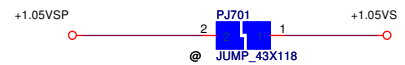
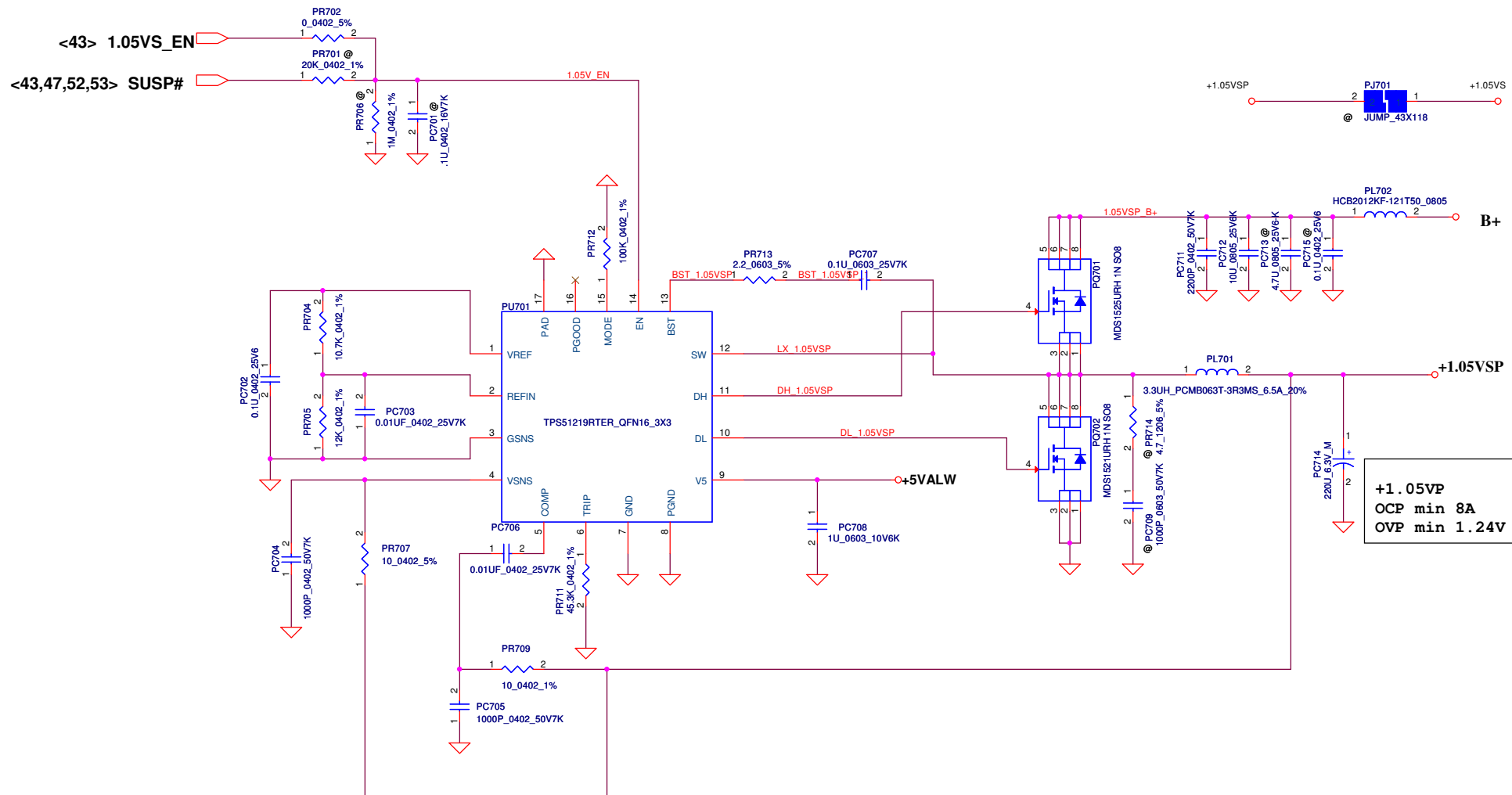


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Compal Electronics, Inc.	
PWR- 3VALWP/5VALWP	
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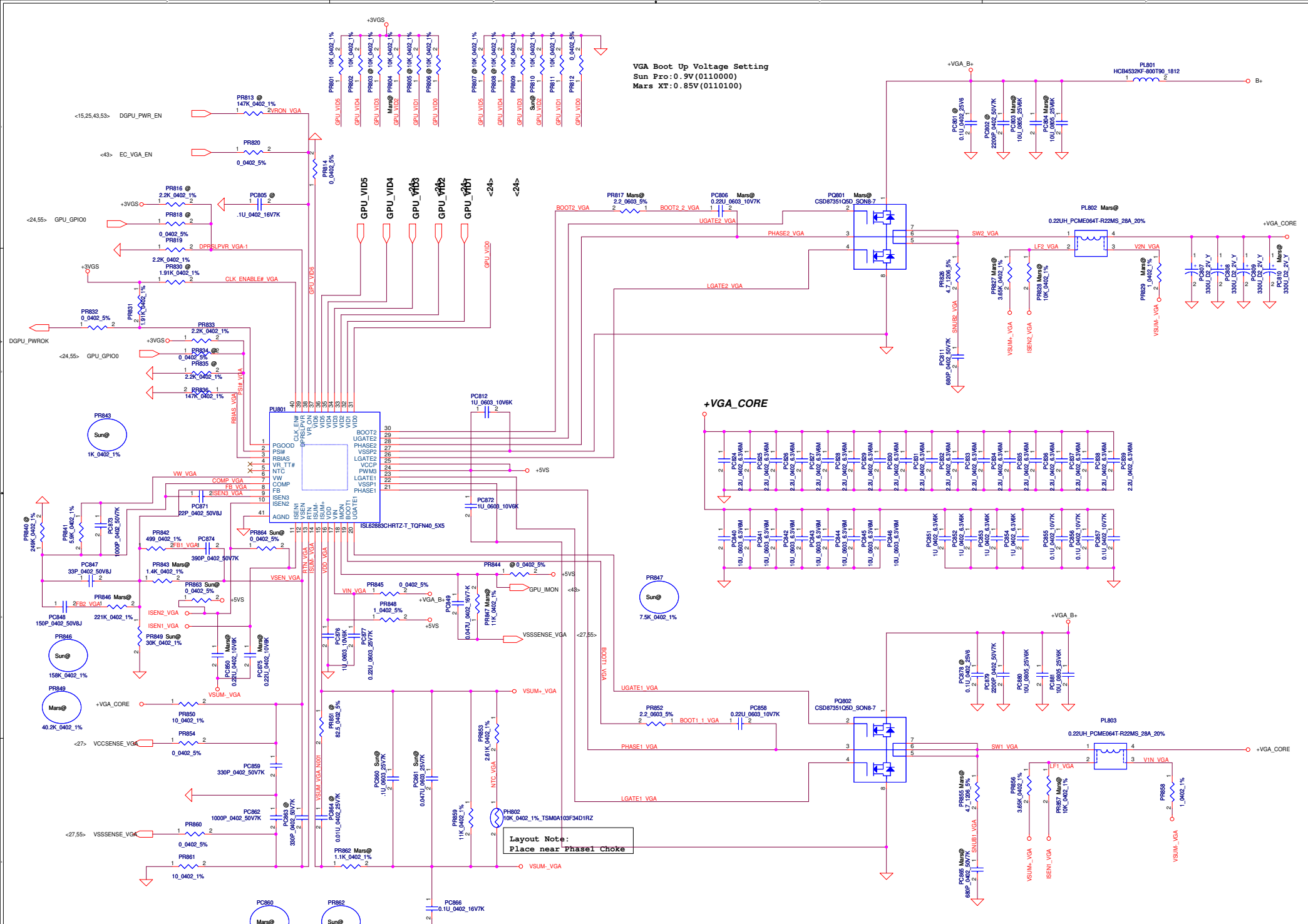
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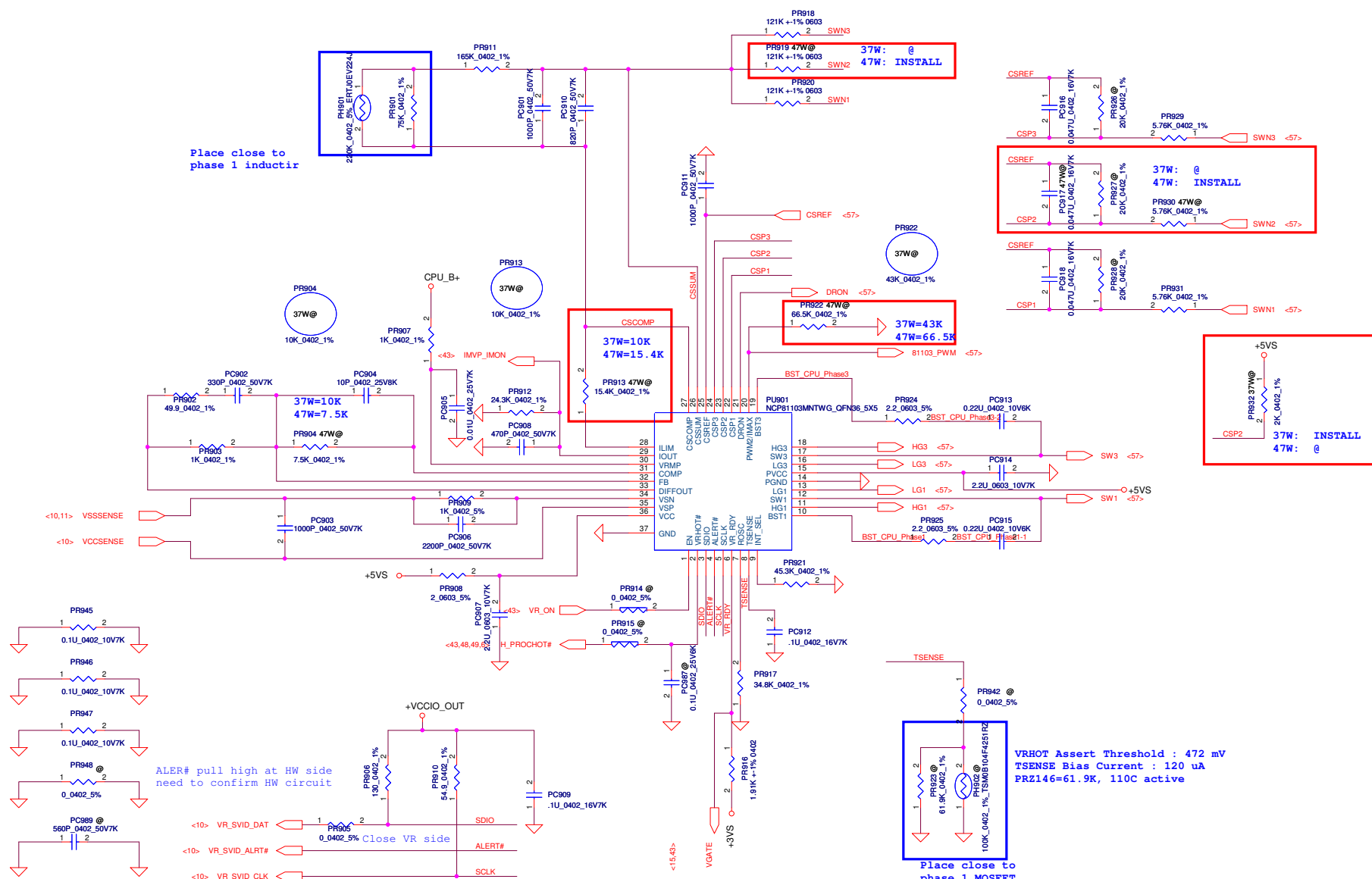
+1.05VP
 OCP min 8A
 OVP min 1.24V

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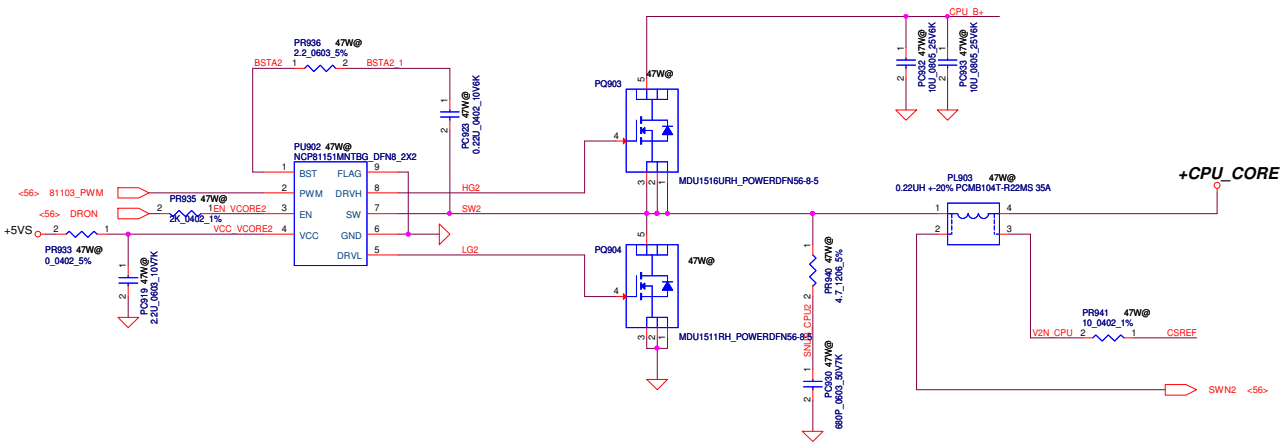
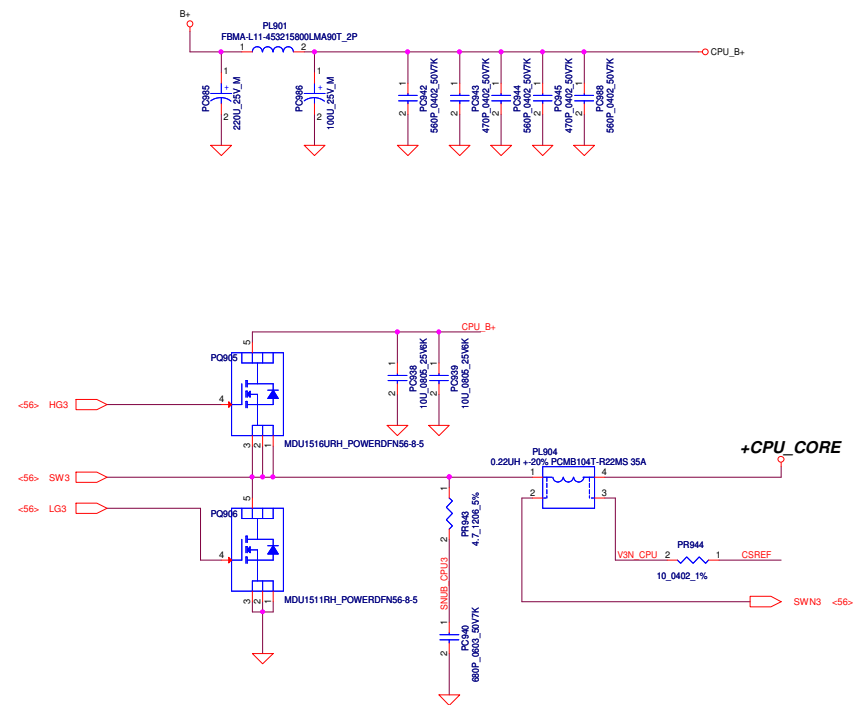
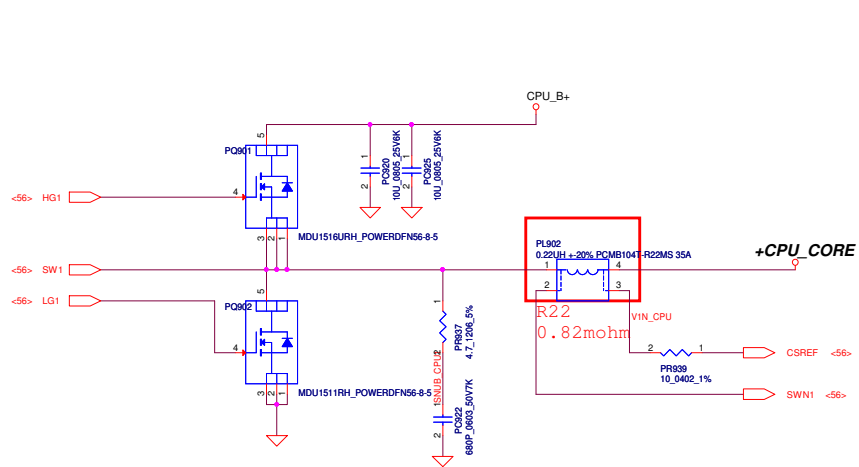
VGA Boot Up Voltage Setting
 Sun Pro: 0.9V (0110000)
 Mars XT: 0.85V (0110100)



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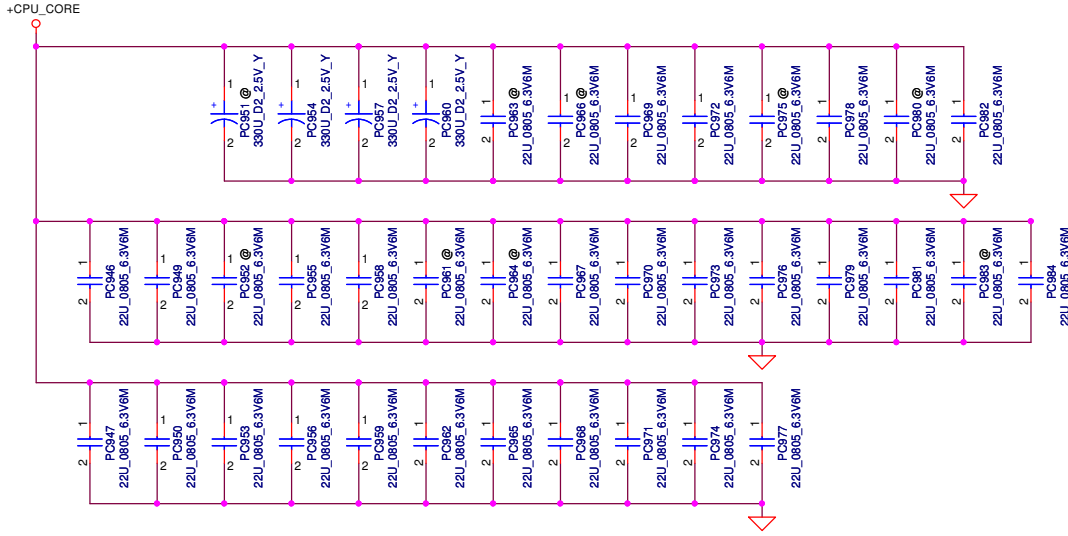
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+CPU_CORE

3 X 330u/9m (47W) 2X330u/9m (37W)
 34 X 22u/0805 34 X 22u/0805



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adapter ID selection circuit	48 49	Add PR103,PR110,PR111,PQ102,PC108,PC109 Add PR227,PR230,PR229,PR232,PR225,PQ206,PQ208,PQ207	2012.11.28	DVT
2	Delete reserve circuit B+ to VSB	49	Delete PR217,PR218,PR219,PC204,PQ203,PR223,PR224,PC205,PQ204,PC206	2012.11.28	DVT
3	Pop Snubber by EMI request	50	PR323,PC320	2012.11.28	DVT
4	To reduce Ripple	51	PC411,PC426 and change PL404 to 3.3uH	2012.11.28	DVT
5	Reserve enable signal by HW request	51	Add PR410,PC432	2012.11.28	DVT
6	Add boost resistor by EMI request	51	Add PR421,PR422	2012.11.28	DVT
7	Reserve feedback signal for IC application	51	Add PR413,PC419	2012.11.28	DVT
8	To reduce Ripple	53	Change PL601and PL605 to 1.5uH	2012.11.28	DVT
9	Delete reserve circuit	53	Delete PC623,PU602,PC624,PR619,PR620,PR622,PC614,PR627,PL602,PR613,PC612,PC615,PC616	2012.11.28	DVT
10	To reduce Ripple	54	Change PL601and PL701 to 3.3uH	2012.11.28	DVT
11	Reserve enable signal by HW request	54	Add PR702	2012.11.28	DVT
12	Pop Snubber by EMI request	55	PR826,PC811,PR855,PC865	2012.11.28	DVT
13	Add input MLCC by EMI request	57	Add PC943,PC944,PC945,PC988	2012.11.28	DVT
14	Reserve battery detective circuit	49 50	Add PR2003,PR217,PC209,PR212,PC210,PD203,PR208,PQ209,PC211,PU202,PC212,PC213 Add PQ314,PR311(Pop)	2013.03.03	PVT
15	Reserve capacitor by EMI request	50	Add PC318,PC319	2013.03.03	PVT
16	Reduce Component	51	Delete PD401	2013.03.03	PVT
17	Reserve 1.5VSP Power Good by HW request	53	Add PR602	2013.03.03	PVT
18	Reserve bridge resistor by EMI request	55	Add PR948,PC989		

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Item	Reason for change	PG#	Modify List	Date	Phase
1	USE singal 8M ROM for BIOS		Change U8 to SA000039A30 8MB ROM Del U7, R239, R234, R235, R233, R236	12/25	DVT
2	POWER NEW AC Connector		U31.21--> ADP_65 U31.68 change from EC_WL_OFF# to ADP_90 U31.85 change from EC_TS_ON#to ADP_135 U31.66 change from BRDID_1 to ADP_ID	12/25	DVT
3	Change XDP pull down Resistor to R pack		Del R18, R21, R23 / Add RP19	12/25	DVT
4	Update Lenovo BGA footprint		UV1, U4, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	12/25	DVT
5	Move 15" ODD CAP to Small Board		ChangeC605 to R401/ChangeC606 to R402/ ChangeC618 to R403/ChangeC617 to R404	12/25	DVT
6	WLAN Control change to PCH		PCH_GPIO55--> PCH_WL_OFF# PCH_GPIO22-->PCH_BT_ON# PCH_GPIO34-->INTEL_BT_OFF#	12/25	DVT
7	POP TL_ENVDD PULL DOWN		POP R408	12/25	DVT
8	Change HDMI LV from 10P8R to 8R4R X2		Del RP19 ADD RP5, RP6	12/25	DVT
9	Update EC GPIO		NOVO# change form pin 26 to 34 EC_FAN_PWM change form pin 34 to 26 ENBKL change form pin 73 to 76 IMVP_IMON change form pin 76 to 73 DGPU_PWR_EN change form pin 107 to 123	12/25	DVT
10	VGA sequence		+1.5VGS : RV41 --> 240K / CV53 --> 0.1U	12/25	DVT
11	EC Board ID		Change R695 to 15K	12/25	DVT
12	Change ODD connector symbol		JODD1->ALLTO_C18518-11305-L_13P-T	12/25	DVT
13	Update Crystal cap Value by vendor suggestion		C111/ C112 --> 15p CV36/CV37-->8.2p	12/25	DVT
14	Reserve for EMI		ADD R411, R412, C411, C412	12/25	DVT
15	Change PCIE port and clock connection by SW request		LAN-->Port 3 / WLAN--> Port2	12/25	DVT
16	Reserve R301		Reserve +3VLP power rail to EC	12/25	DVT
17	Change EC_RST# power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
18	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
19					
20					
21					
22					

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Add resistor to switch audio power from +3VS to +3VLP and +3VALW.		Add RA1,RA2	02/18	PVT
2	Reconnect HDD +3VS power rail.		Add R-short R552.	02/18	PVT
3	Modify LED current limiting resistor value.		Modify : R623,R765,R303	02/18	PVT
4	Add parallel resistor to separate BIOS and EC.		Add RP2	02/18	PVT
5	Add a Capacitor to connect CHASSIS_GND and GND by EMI request.		Add CL64	02/18	PVT
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