

# Compal Confidential

## DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2013-02-27

LA-9641P

REV: 0.3

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# Shark Bay

**AMD MARS XT M2 128 bits / SUN PRO M2 64 bits**

VRAM 512MB/1GB/2GB  
MARS XT : DDR3 x 8  
SUN PRO : DDR3 x 4

page 23~32

PEG 8x  
Gen2 / Gen3

**Intel Processor Haswell**

rPGA946  
37.5mm x 37.5mm

page 5,~11

Memory Bus  
Dual Channel

DDR3L 1600MHz  
DDR3L 1333MHz

**204pin DDRIII-SO-DIMM X2**

BANK 0, 1, 2

page 12,13

**LVDS Conn.**  
page 34

**LVDS Translator**  
RTD2132R(Single)

page 33

**HDMI Conn.**  
page 36

FDI \*2  
2.7GT/s

DMI2 \*4  
5GT/s

**Intel PCH Lynx Point**

FCBGA 695Balls  
20mm x 20mm

USB30 x2

**Left USB3.0 x2**  
USB30 Port 0,1  
page 46

**Right USB2.0**  
USB20 Port 9  
page 46

**Int. Camera**  
USB20 Port 3  
page 33

**Touch Screen**  
USB20 Port 2

**Card Reader**  
Realtek RTS5170  
USB20 Port 11  
page 44

USB20 x6

**CRT Conn.**  
page 35

**RJ45 Conn.**  
page 39

**LAN**  
Atheros AR8162/QCA8172 (10/100)

PCIe x1  
page 38

SATA Gen3

**HDD Conn.**  
SATA Port 4  
page 41

SATA

**ODD Conn.**  
SATA Port 5  
page 41

**PCIe Mini Card WLAN**  
PCIe Port 0  
page 28

**PCIe Mini Card**  
USB20 Port 10  
page 28

PCIe x1

AZALIA

**Audio Codec**  
CONEXANT CX20757  
page 42

USB20 x1

**Int. MIC Conn.**  
page 42

**Int. Speaker Conn.**  
page 42

**Audio Combo Jacks**  
HP & MIC  
page 42

Sub-board

**15"**  
**Power/B**  
LSXXXP  
page 44

**14"**  
**LED/B**  
LSXXXP  
page 44

**USB/B**  
LSXXXP  
page 44

**CR/B**  
LSXXXP  
page 44

**ODD/B**  
LSXXXP  
page 44

**SPI ROM**  
2MB + 4MB  
page 17

**EC**  
ENE KB9012  
page 44

**Thermal Sensor**  
page 40

**Touch Pad**  
page 44

**Int. KBD**  
page 44

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				Block Diagram
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### Voltage Rails

power plane	+B	+5VALW	+1.35V	+5VS
				+3VS
State		+3VALW		+VCC_CORE
				+VGA_CORE
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b

Device	Address
Thermal Sensor	1001_100xb

### PCH SM Bus address

### AMD-GPU SM Bus address

Device	Address
DDR DIMM1 ChannelA	0xA0
DDR DIMM2 ChannelB	0xA4

Device	Address
Internal thermal sensor	1000_001xb

Device	Address
RTD2132R	1101 010Xb

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

### Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	Project	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

### USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
		2	Touch screen
	UHCI2	3	Camera
		4	
		5	
		6	
7			
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
		12	
		13	

### BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Camera	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
Righ side USB	RUSB@
Zero ODD circuit	ZODD@
Share ROM	SROM@
Non-share ROM	NOSROM@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

R\_USB@

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	+3VS	+3VS
SMB_EC_DA2	+3VALW								
SMBCLK	PCH	X	X	X	V	V	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SMLCLK	PCH	X	X	X	X	X	X	X	X
SMLDATA	+3VALW								
SML1CLK	PCH	V	X	V	X	X	V	X	V
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

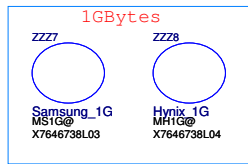
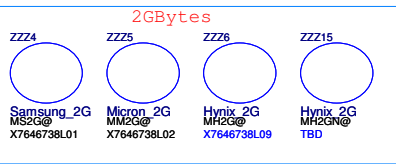
VRAM BOM STRUCTURE Refer P4. VGA NOTE

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### Mars XT VRAM STRAP

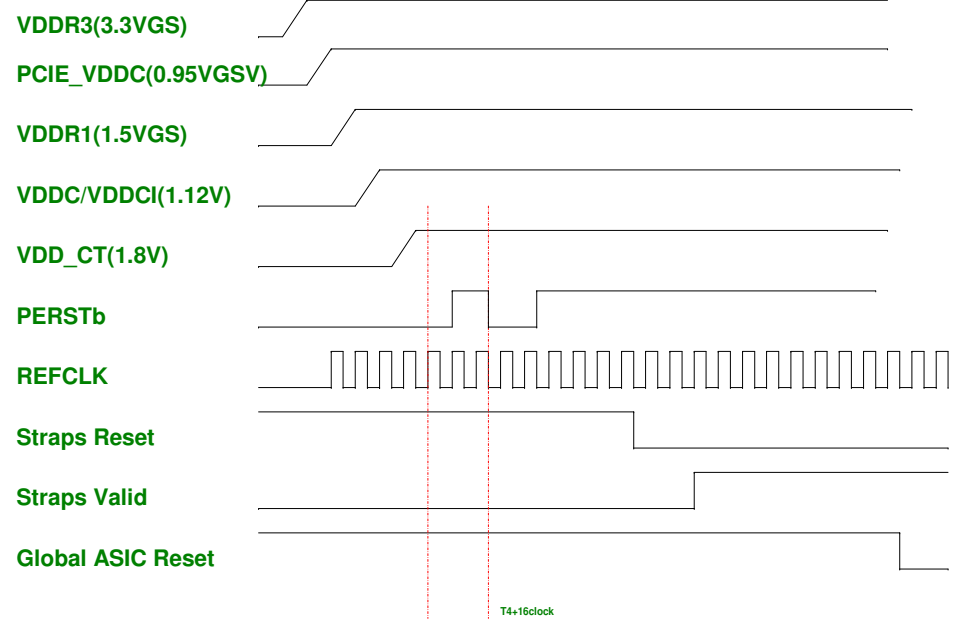
	x76@		x76@			
	Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC
ZZZ15 MH2GN@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K



### Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

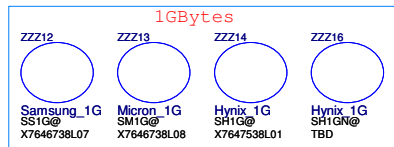
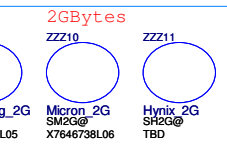


R_pu ( $\Omega$ )	R_pd ( $\Omega$ )	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

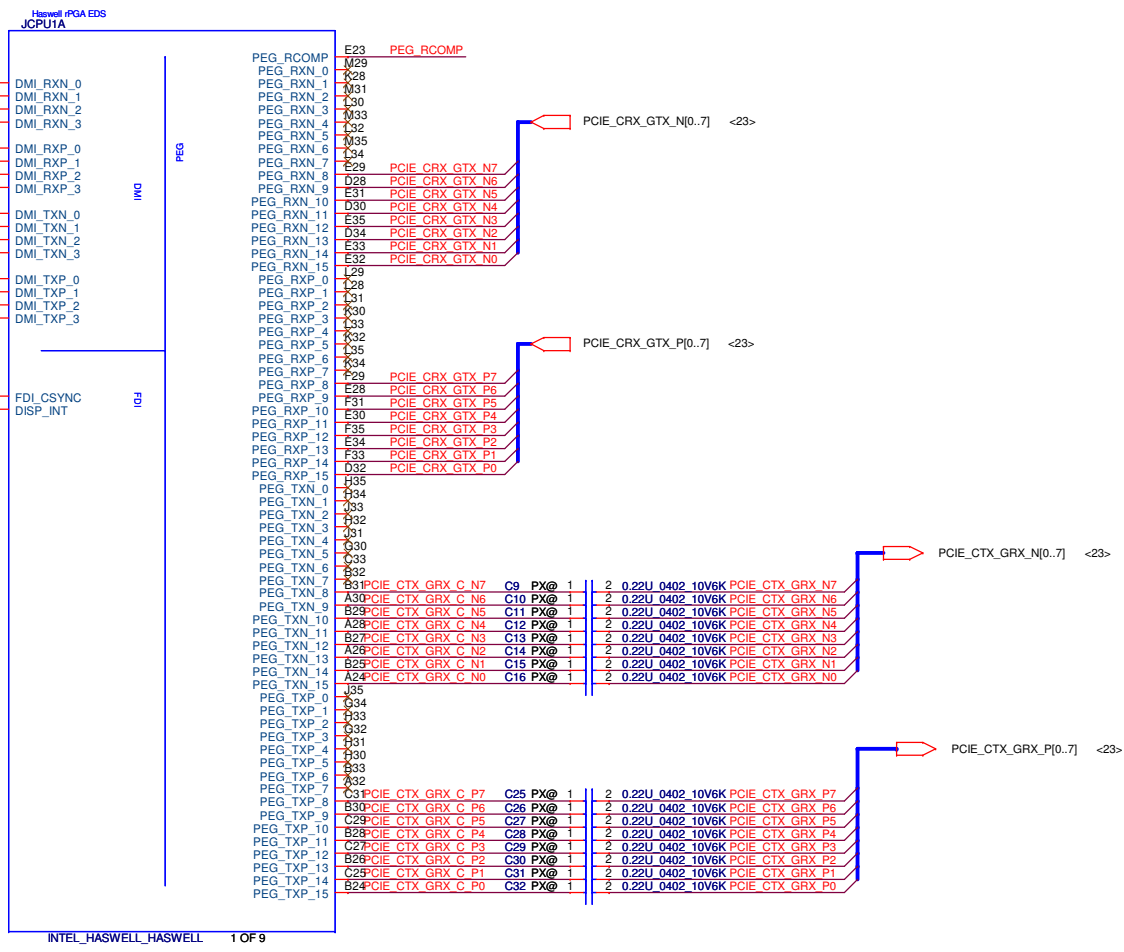
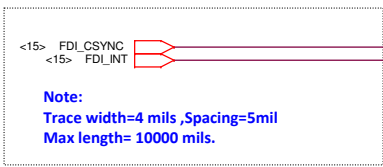
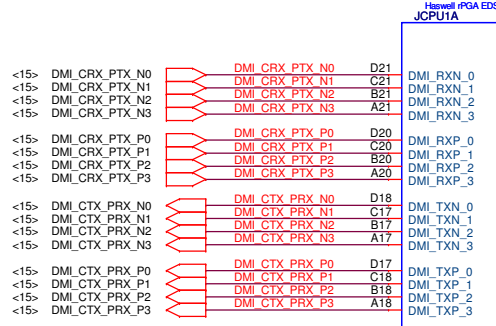
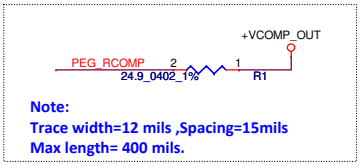
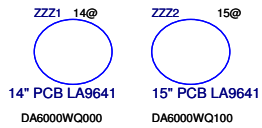
Note: 0402 1% resistors are required.

### Sun PRO VRAM STRAP

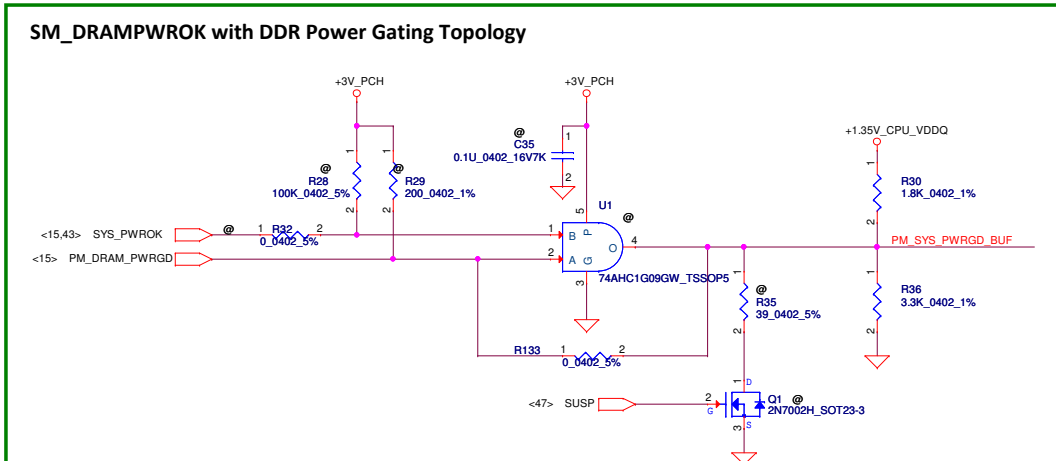
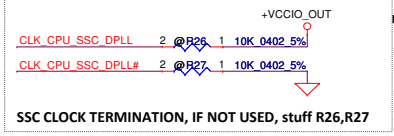
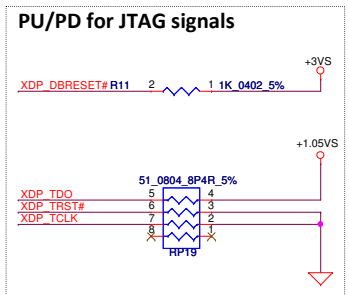
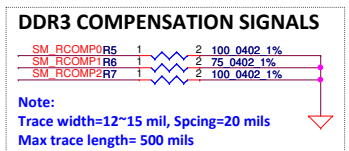
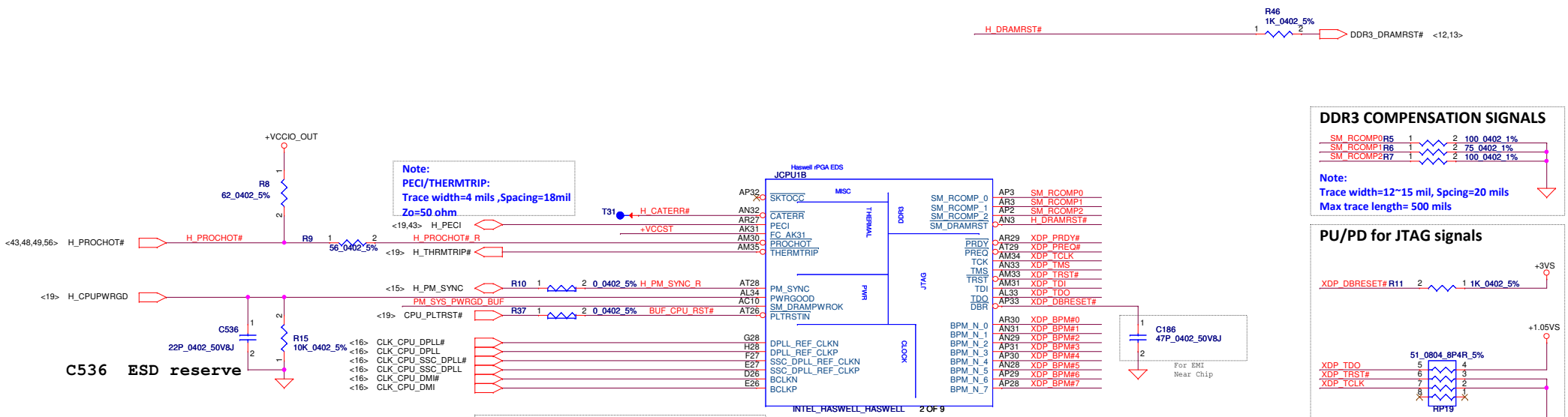
	x76@		x76@			
	Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-109G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	1	1	1	4.75K	NC
	Hynix 2048Mbits SA00006H400 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K



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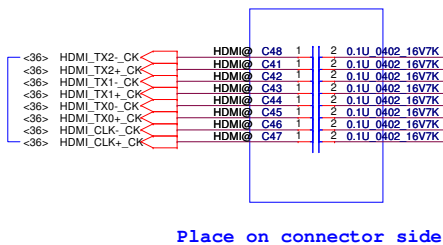


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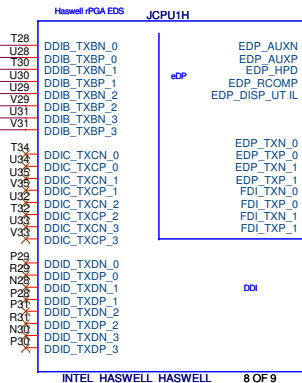


HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

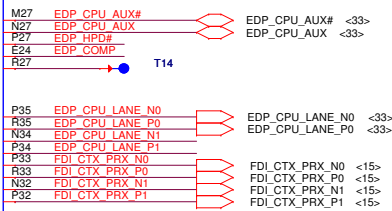
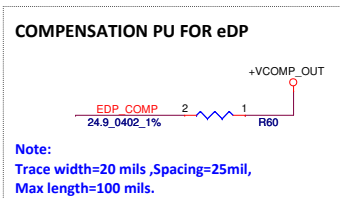
HDMI



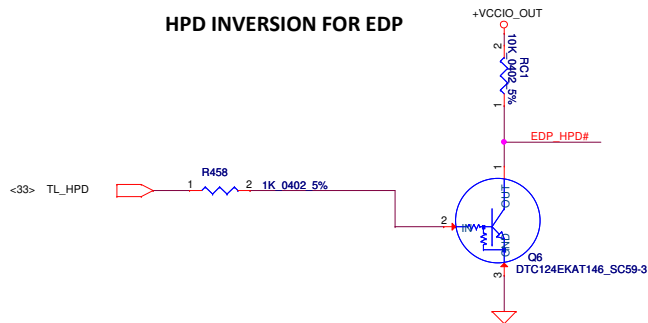
Place on connector side



ME@



**HPD INVERSION FOR EDP**



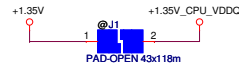
HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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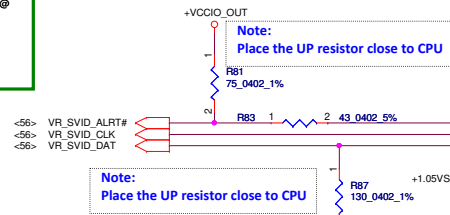
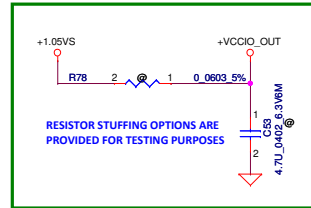
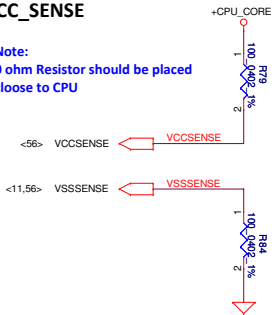


### +1.35V\_CPU\_VDDQ Source

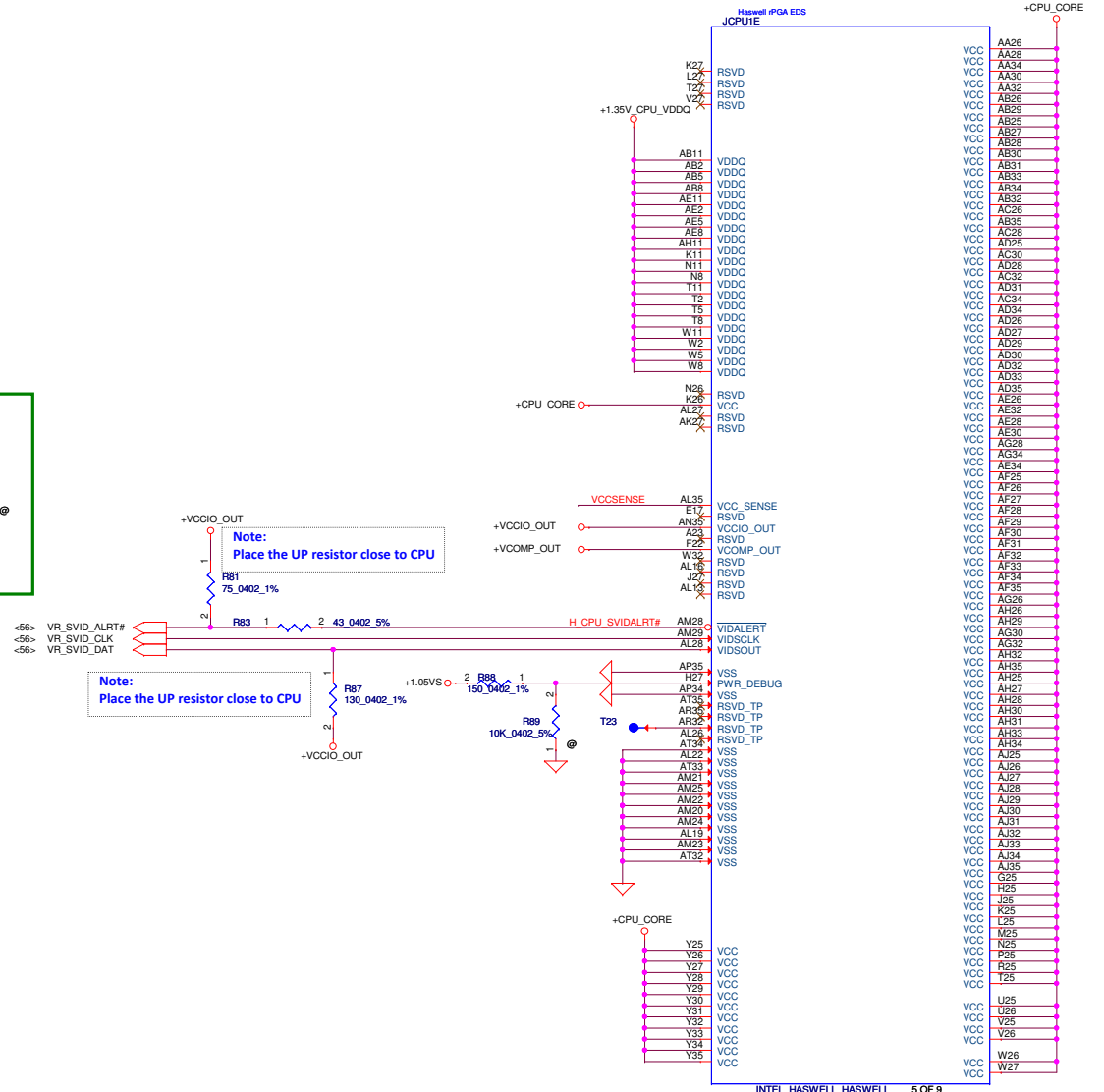
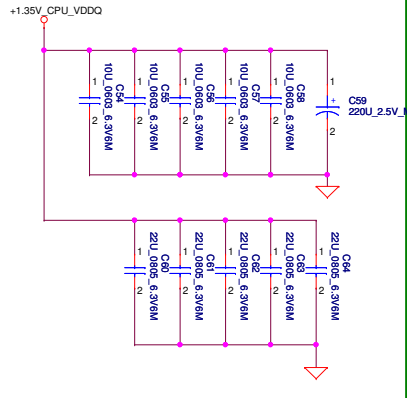


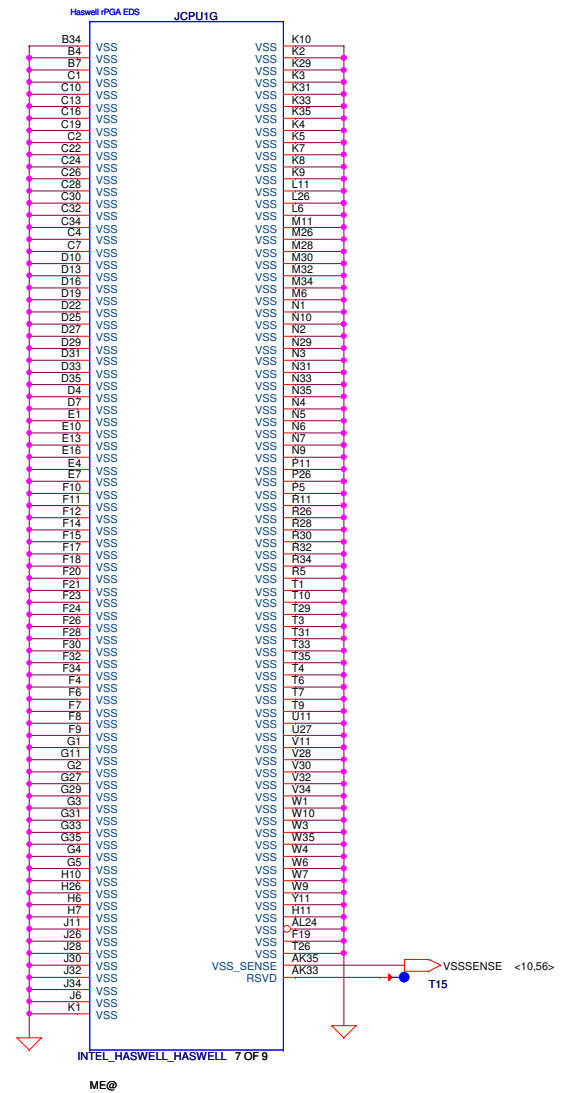
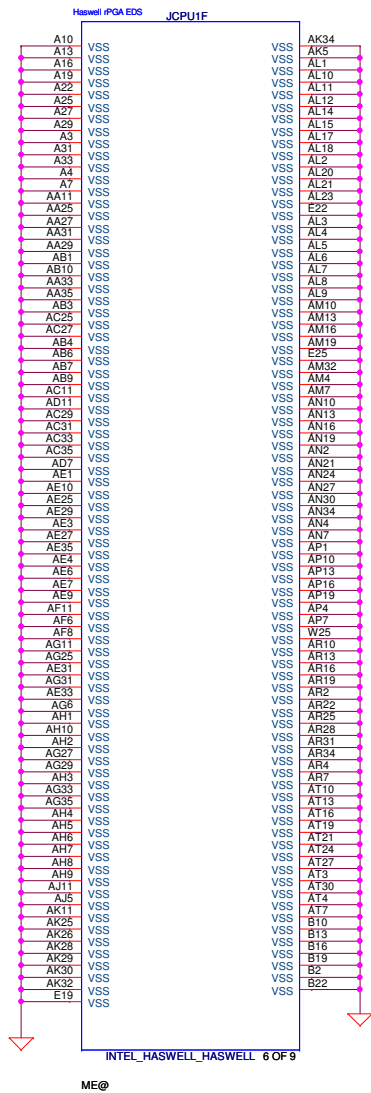
### VCC\_SENSE

Note:  
0 ohm Resistor should be placed close to CPU



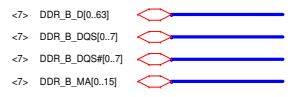
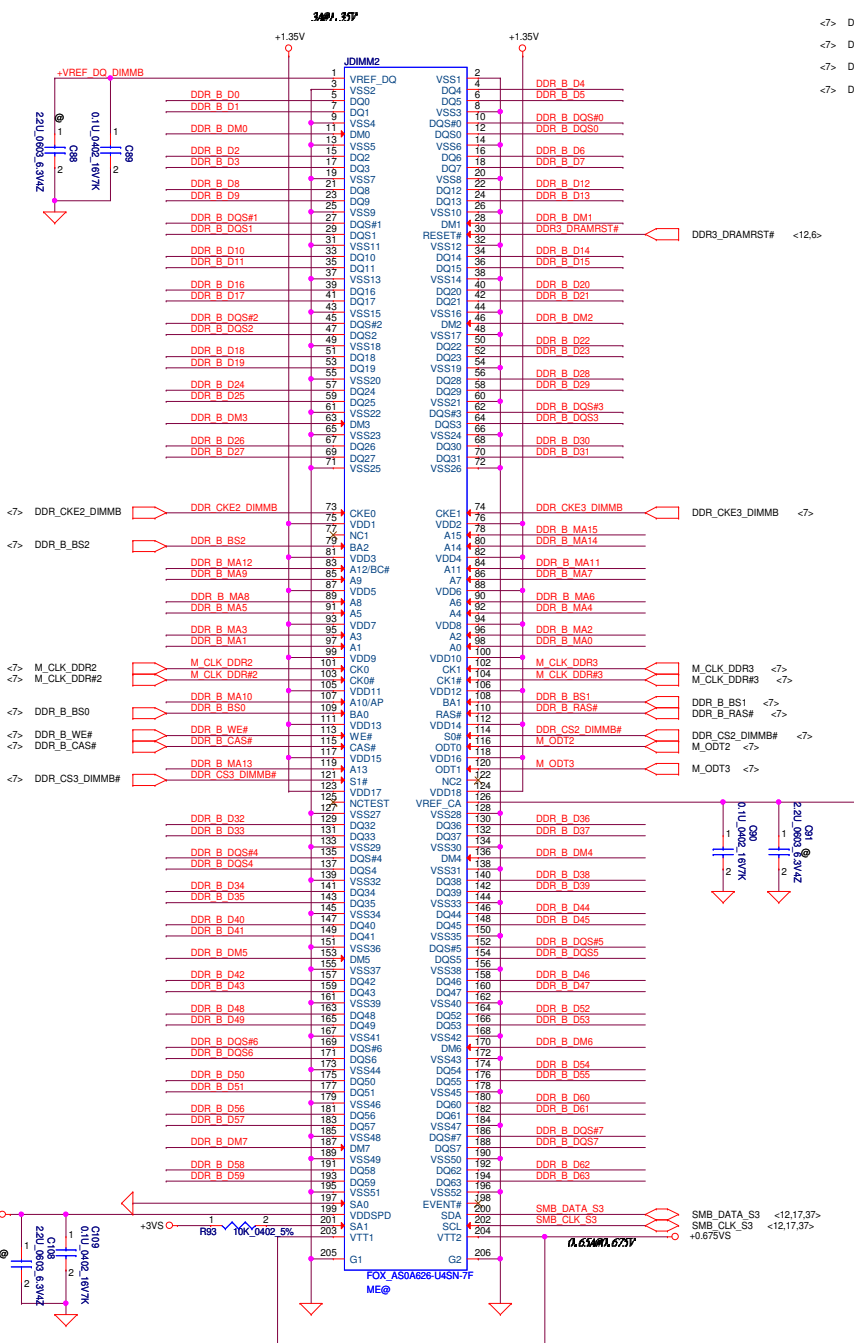
### VDDQ DECOUPLING



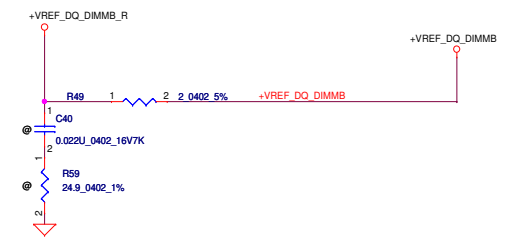


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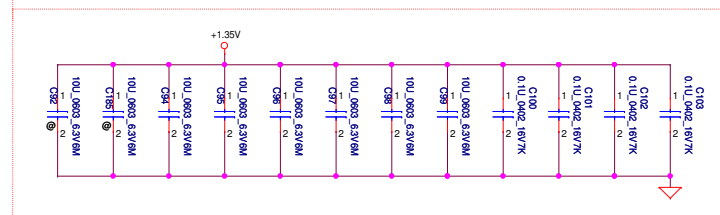




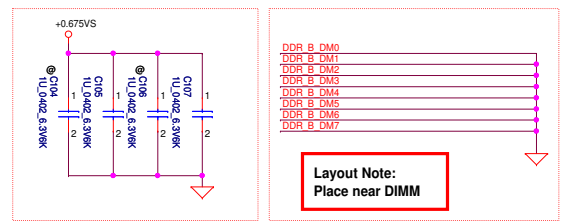
Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes



Layout Note:  
Place near DIMM

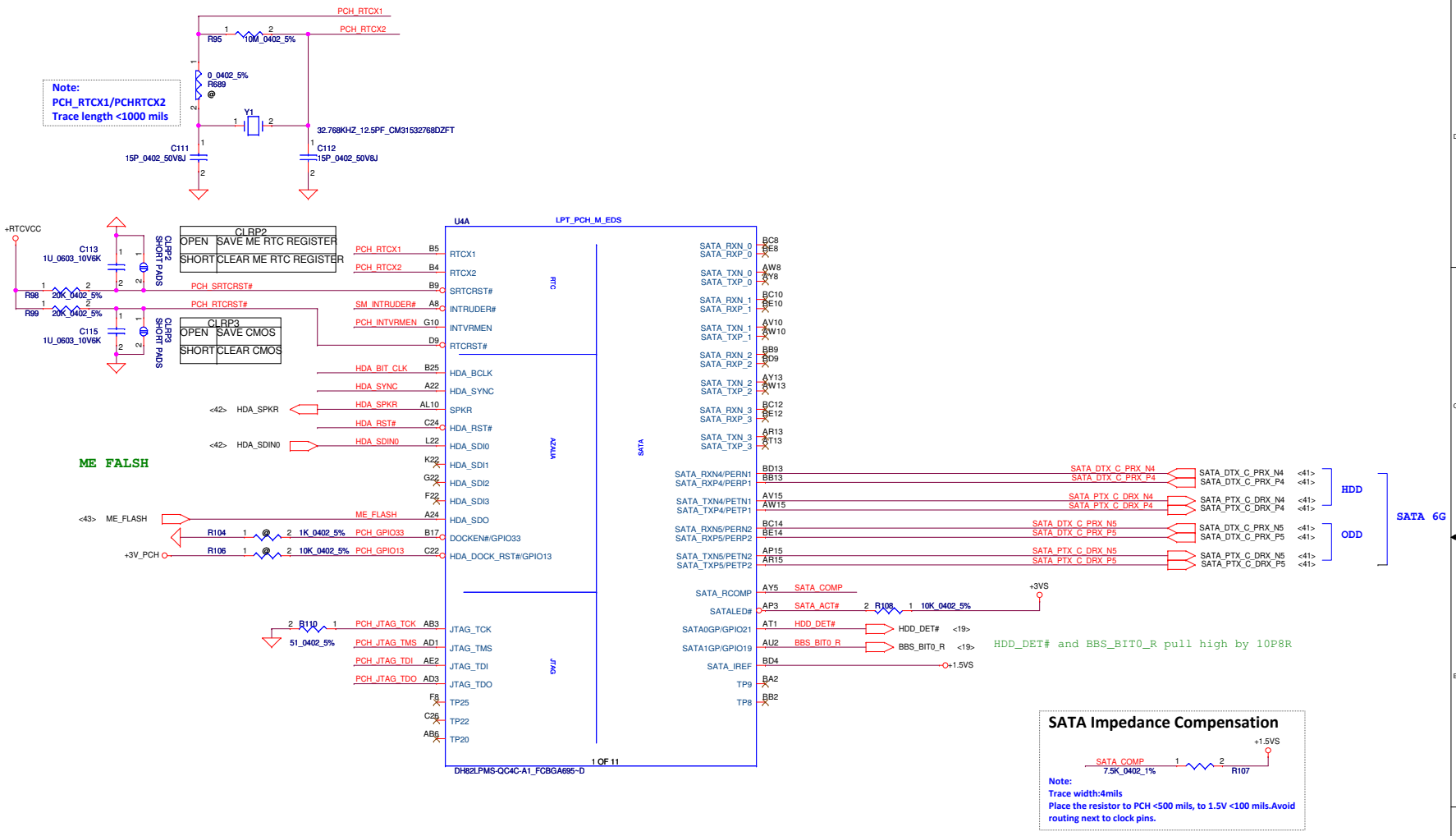
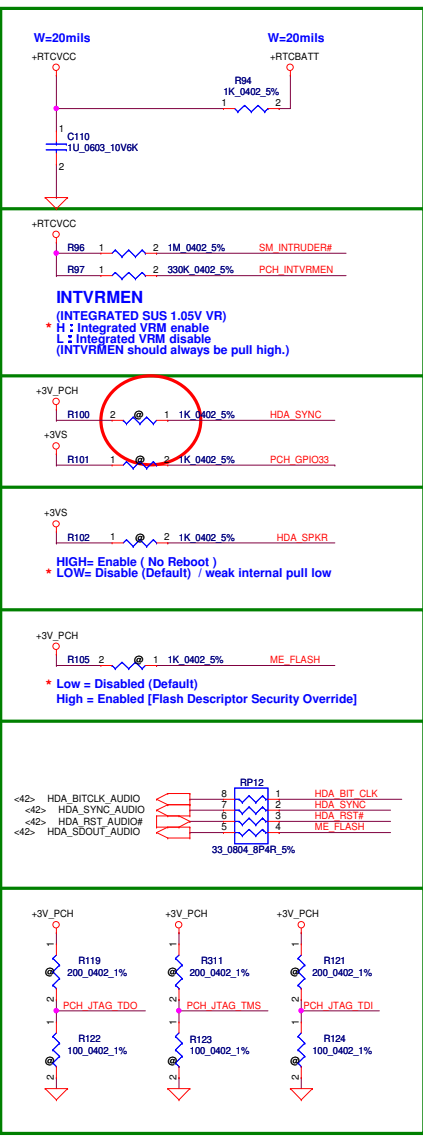


Layout Note:  
Place near DIMM



Layout Note:  
Place near DIMM

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Issued Date	2011/06/15	Deciphered Date	
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Date:	Wednesday, March 08, 2013	Sheet	13 of 61

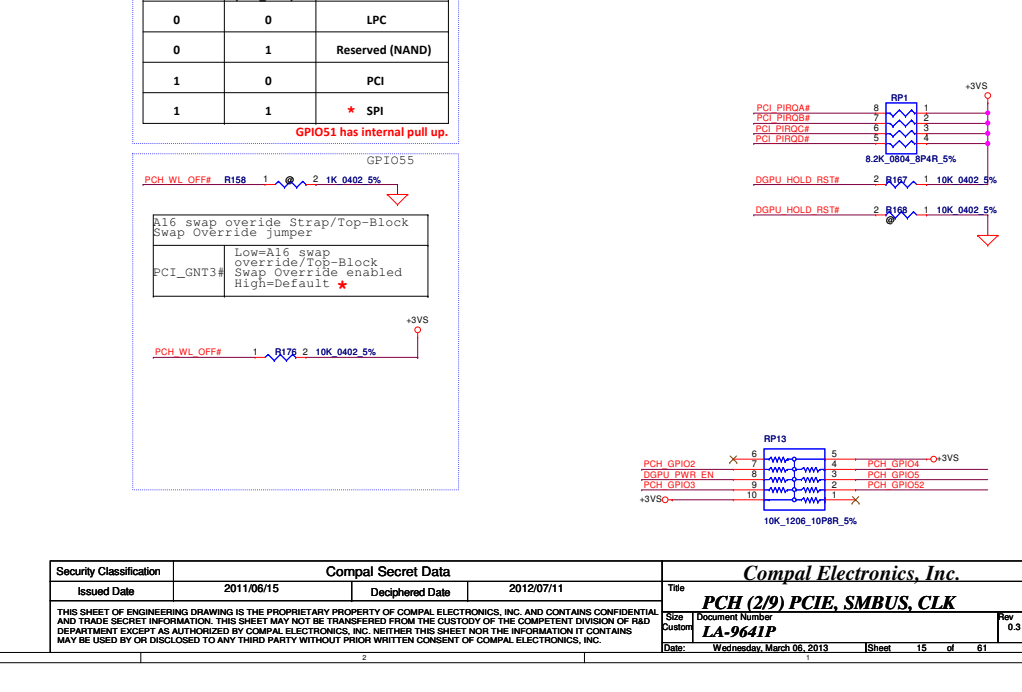
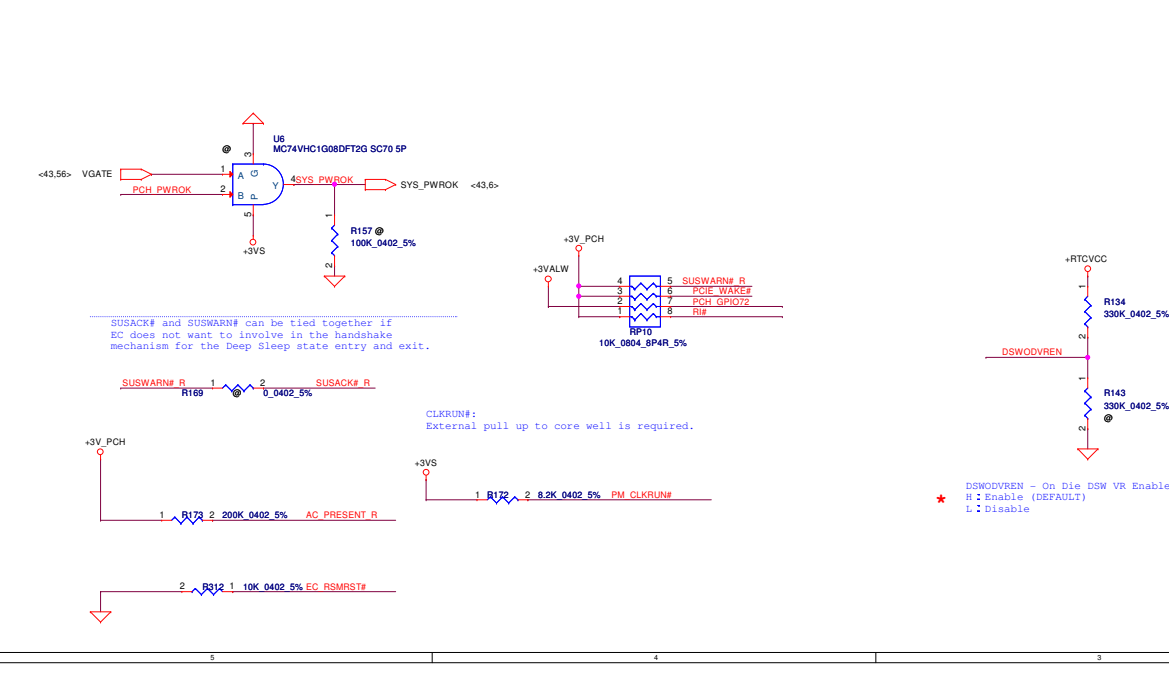
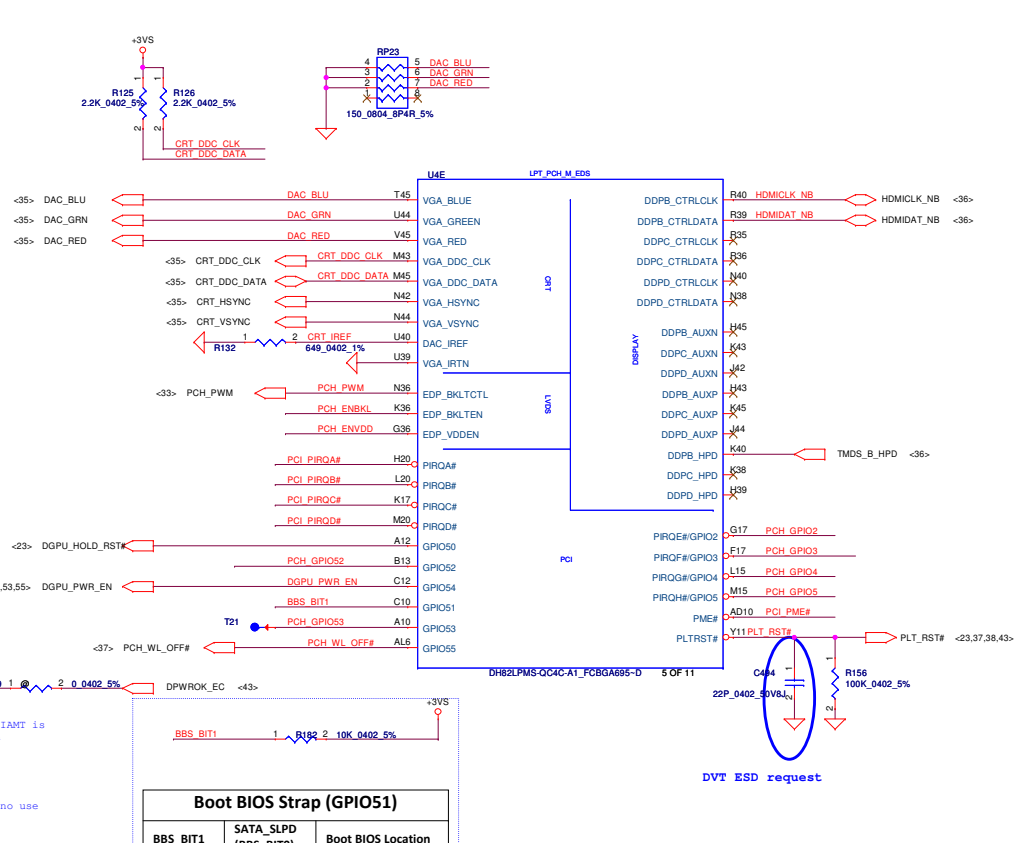
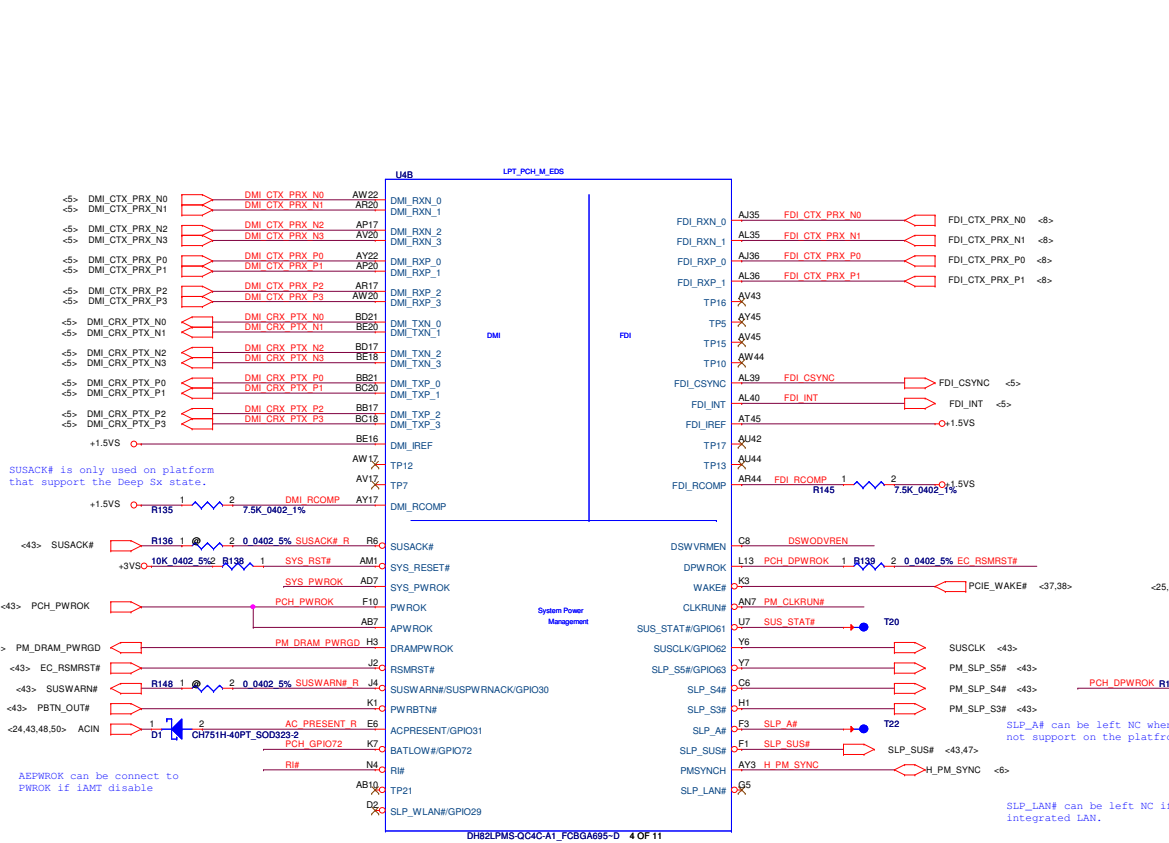


**SATA Impedance Compensation**

SATA\_COMP → R107 7.5K\_0402\_1% → +1.5V

**Note:**  
Trace width: 4mils  
Place the resistor to PCH <500 mils, to 1.5V <100 mils. Avoid routing next to clock pins.

Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	<b>PCH (1/9) SATA, HDA, SPI, LPC, XDP</b>
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Date: Wednesday, March 06, 2013				Sheet 14 of 61



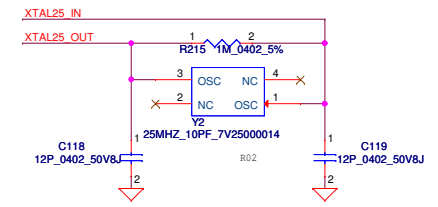
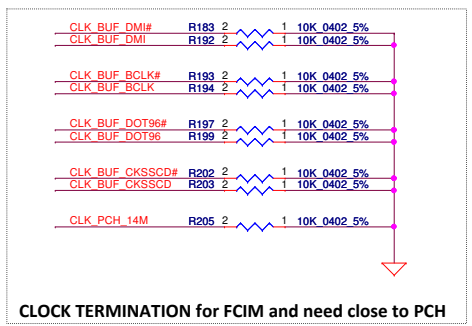
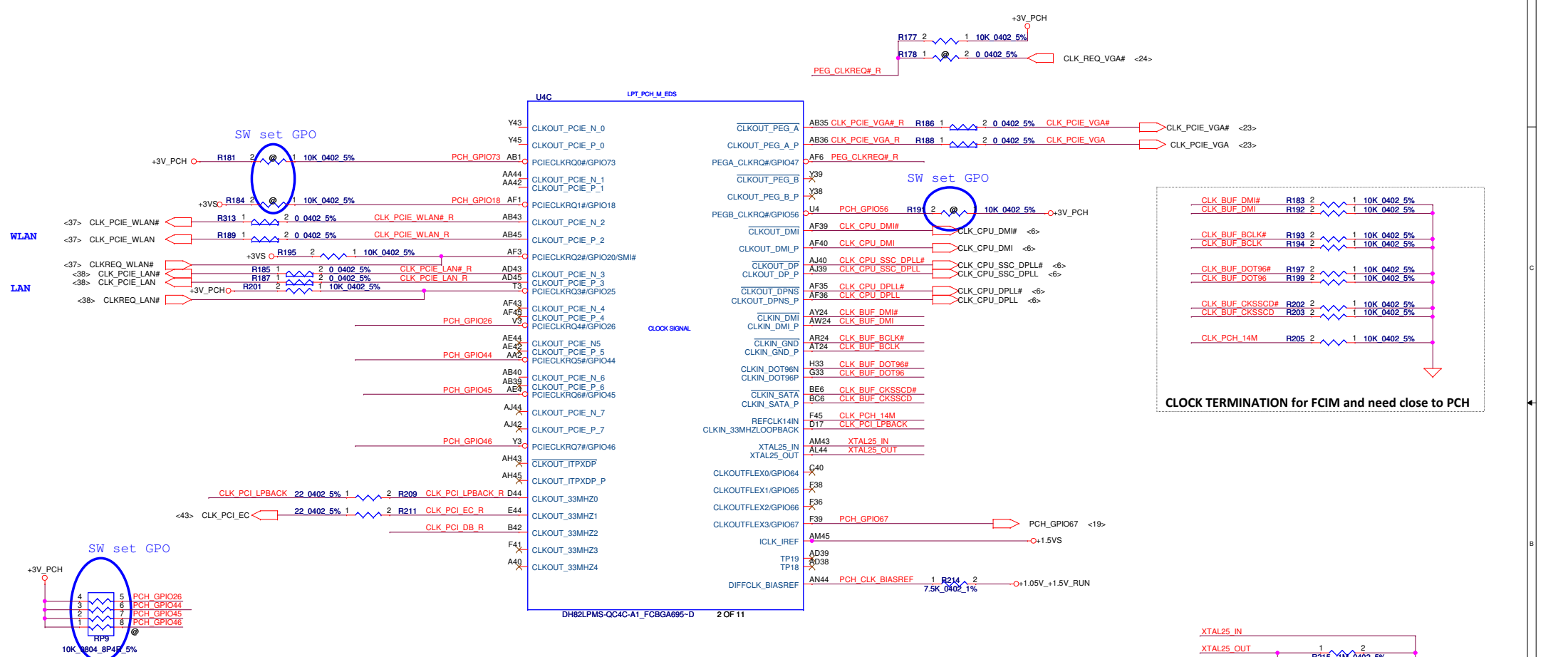
### Boot BIOS Strap (GPIO51)

BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	* SPI

GPIO51 has internal pull up.

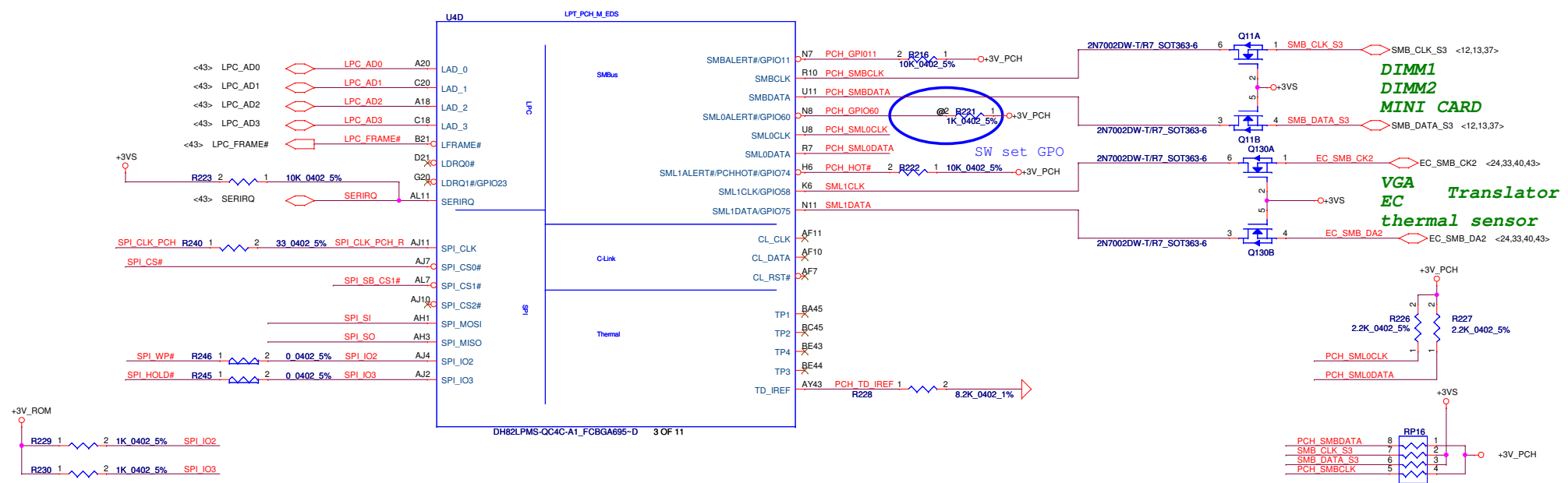
### GPIO55

GPIO55	Function
PCH_WL_OFF#	Low= A16 swap override/Top-Block Swap Override jumper
PCI_GNT3#	Low= A16 swap override/Top-Block Swap Override enabled
	High= Default *



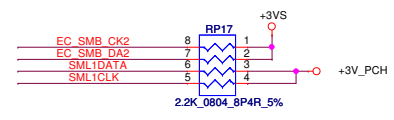
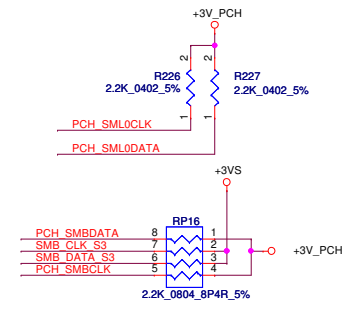
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Issued Date	2011/06/15	Deciphered Date	2012/07/11
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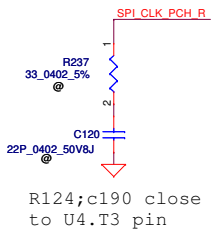
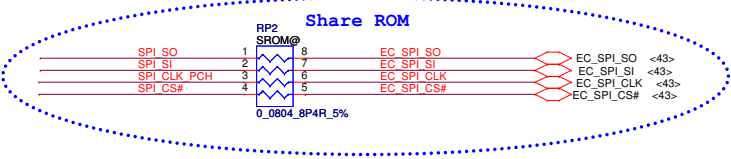
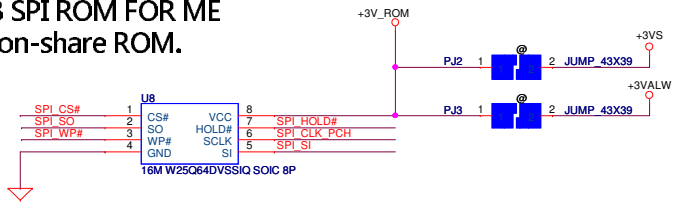


**DIMM1  
DIMM2  
MINI CARD**

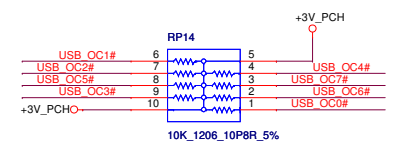
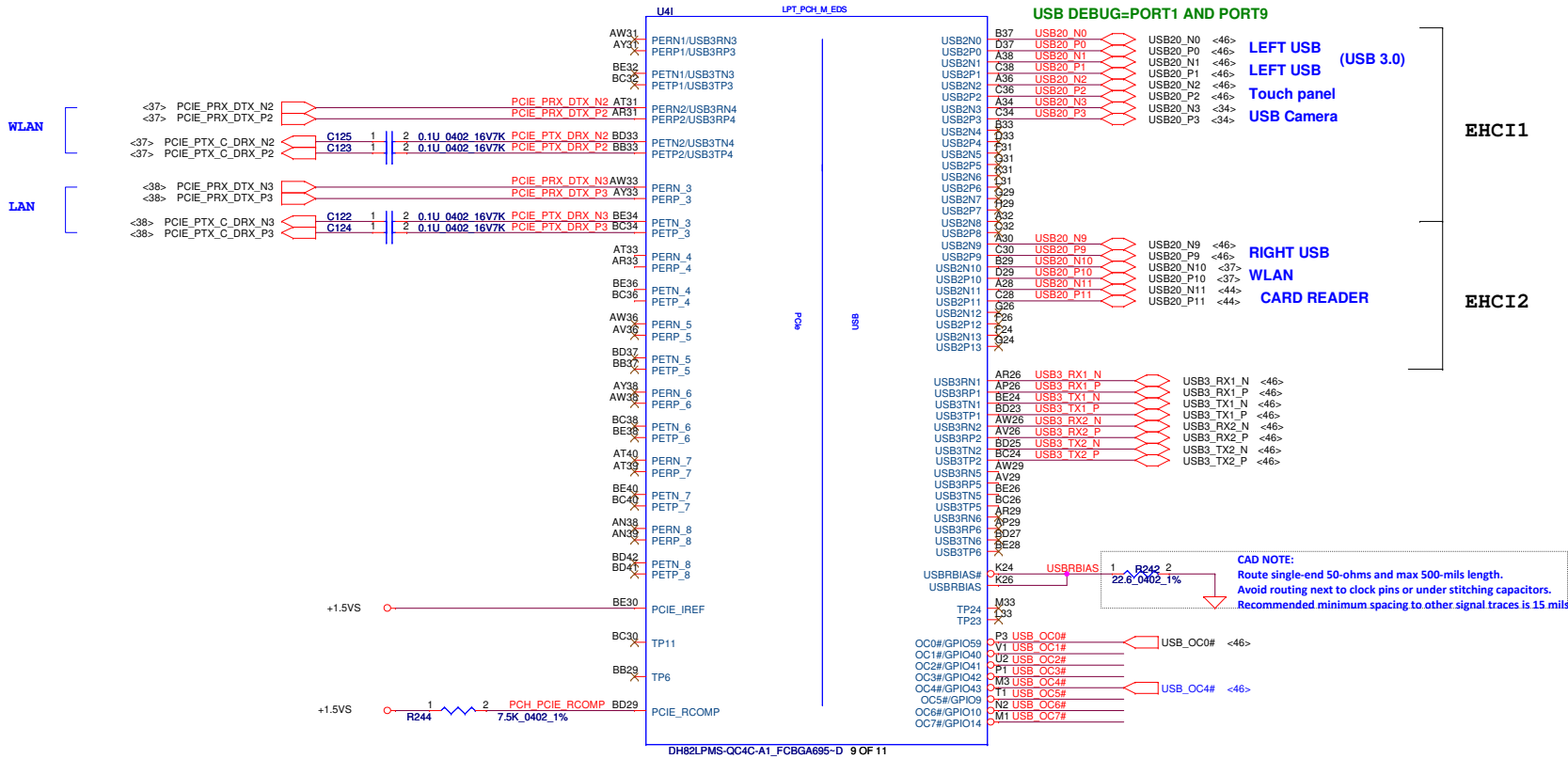
**VGA  
EC Translator  
thermal sensor**



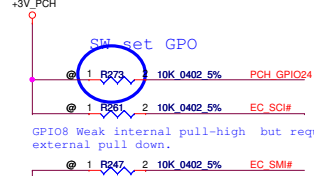
**8MB SPI ROM FOR ME & Non-share ROM.**



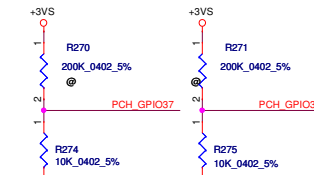
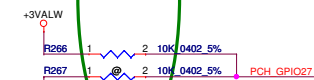
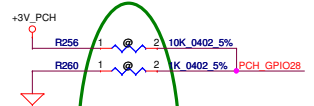
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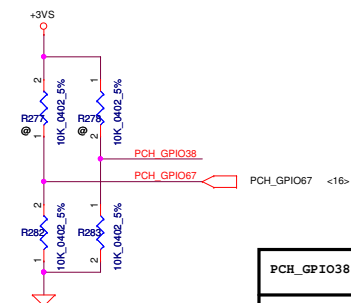
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				LA-9641P	0.3
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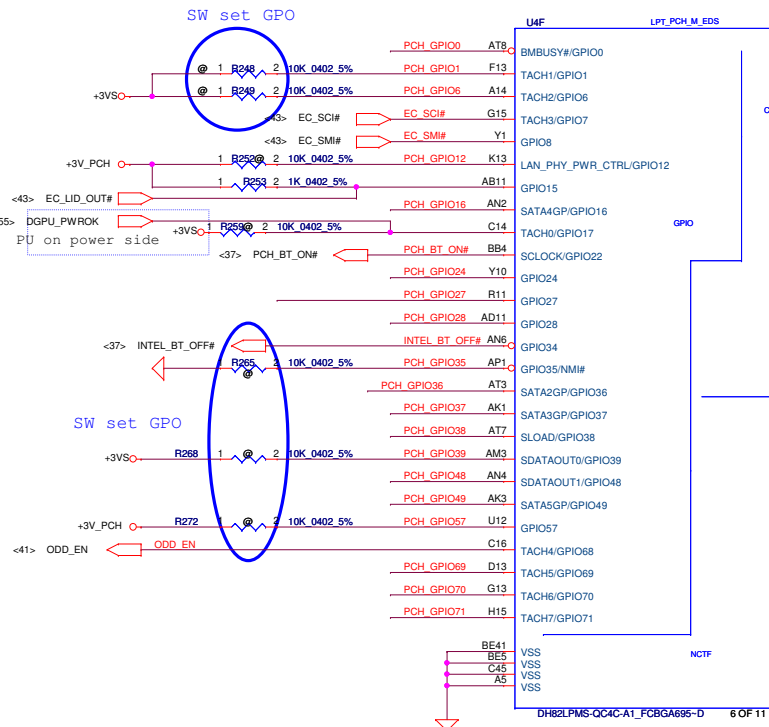
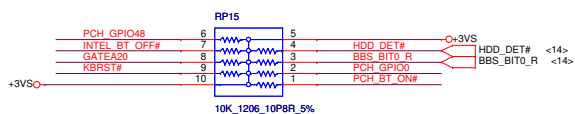
Remove strap description inform SW set GPIO



BIOS Request SKU ID

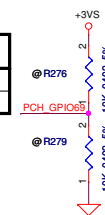


PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	DIS
1	1	UMA

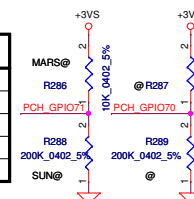


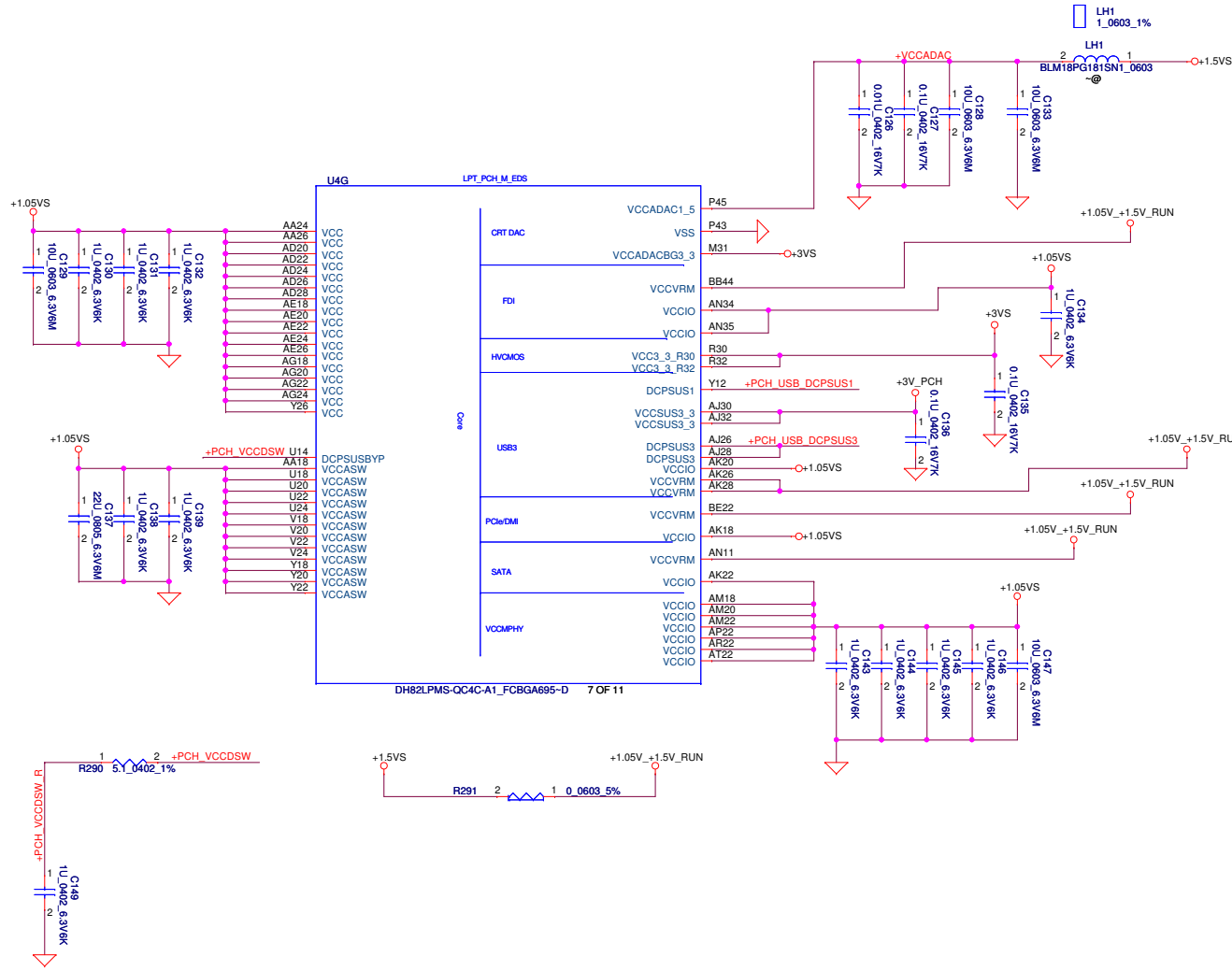
Need Update

PCH_GPIO69	Function
0	
1	



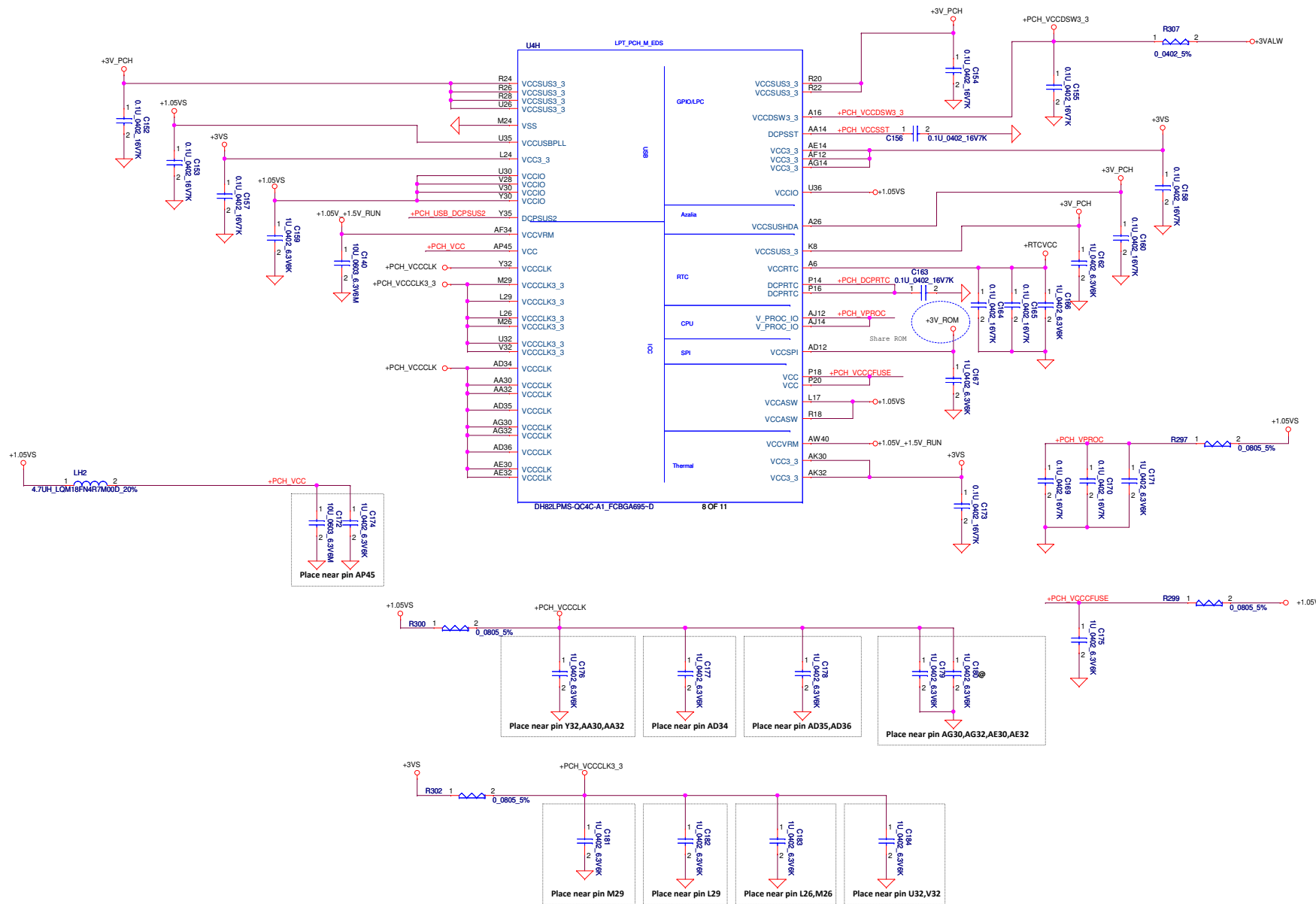
PCH_GPIO70	Function
0	
1	
PCH_GPIO71	Function
0	SUN PRO
1	Mars XT





PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Date: Wednesday, March 06, 2013				Sheet	20 of 61



PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Place near pin AP45

Place near pin Y32,AA30,AA32

Place near pin AD34

Place near pin AD35,AD36

Place near pin AG30,AG32,AE30,AE32

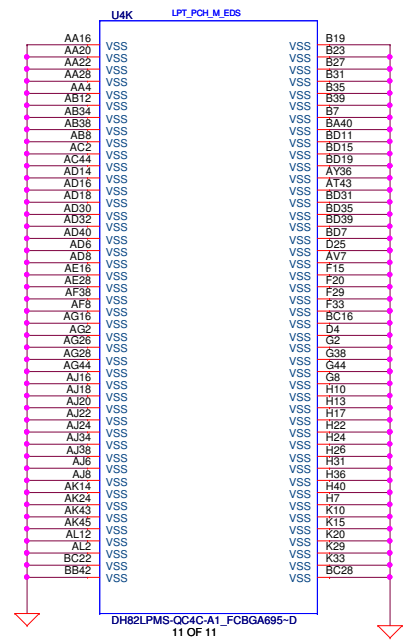
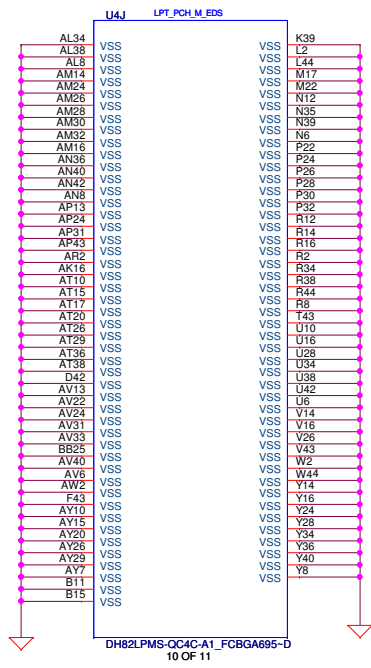
Place near pin M29

Place near pin L29

Place near pin L26,M26

Place near pin U32,V32

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Date: Wednesday, March 08, 2012				Sheet	61



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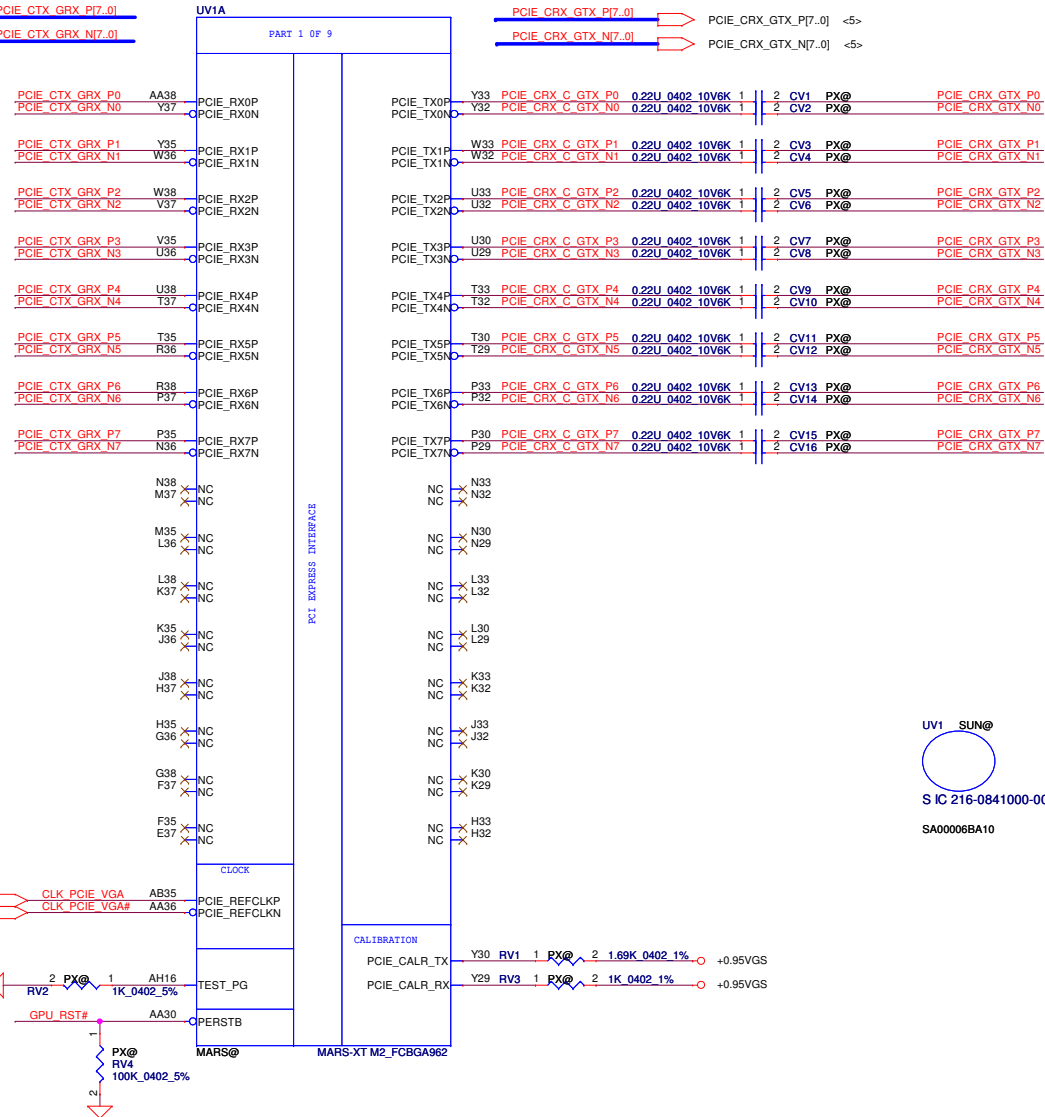
**PCH (9/9) VSS**  
Document Number  
**LA-9641P**

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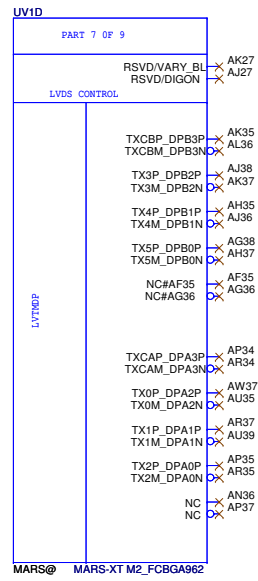
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PCIe\_CRX\_GTX\_P[7..0] PCIe\_CRX\_GTX\_P[7..0] <5>

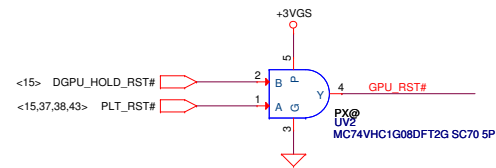
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### LVDS Interface

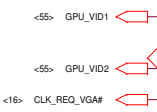
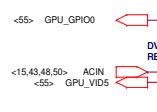
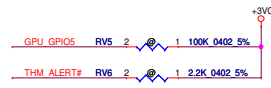
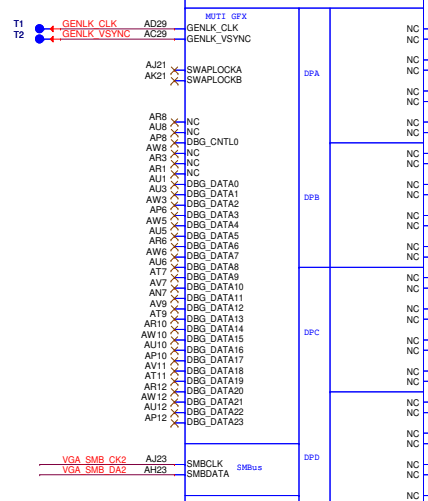


UV1 SUN@  
  
 S IC 216-0841000-00 A0 SUN PRO M2 FCBGA 962P C38  
 SA00006BA10

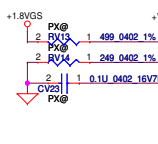


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				Rev <b>0.3</b> Sheet 23 of 61

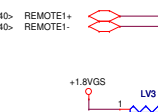
### STRAPS



0.60 V level, Please VREFG Divider and cap close to ASIC

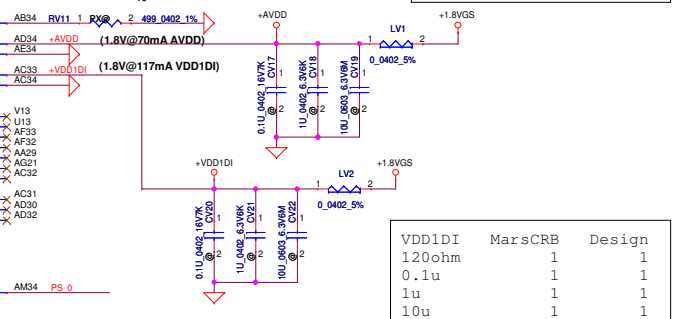


GPIO 28 FDO	MLPS
H	Disable
L	Enable



TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

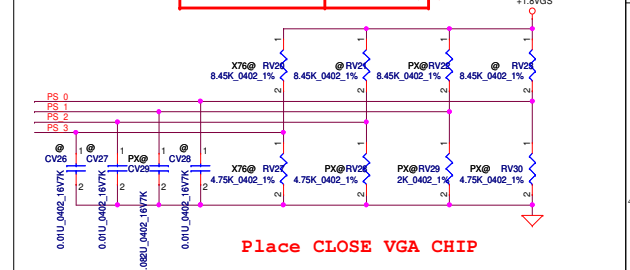
RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 10K RESISTOR  
 X= DESIGN DEPENDANT  
 NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRs_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100-512Kbit M2SP05A (ST) 101-1Mbit M2SP10A (ST) 101-2Mbit M2SP20 (ST) 101-4Mbit M2SP40 (ST) 101-8Mbit M2SP80 (ST) 100-512Kbit Pm2SLV010 (Chingis) 101-1Mbit Pm2SLV010 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1]	NA	00- No audio function 01- Audio for DP only 10- Audio for DP and HDMI if dongle is detected 11- Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111- 0 usable endpoints 110- 1 usable endpoints 101- 2 usable endpoints 100- 3 usable endpoints 011- 4 usable endpoints 010- 5 usable endpoints 001- 6 usable endpoints 000- all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

### MLPS Strap

Bits[5:1]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1 000	NC	NC	4.75K
PS_1[5:1]	01 0 0 1	82 nF	8.45K	2K
PS_2[5:1]	10 0 0 0	10 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	X	X

Mapping to VRAM type please refer to page 4



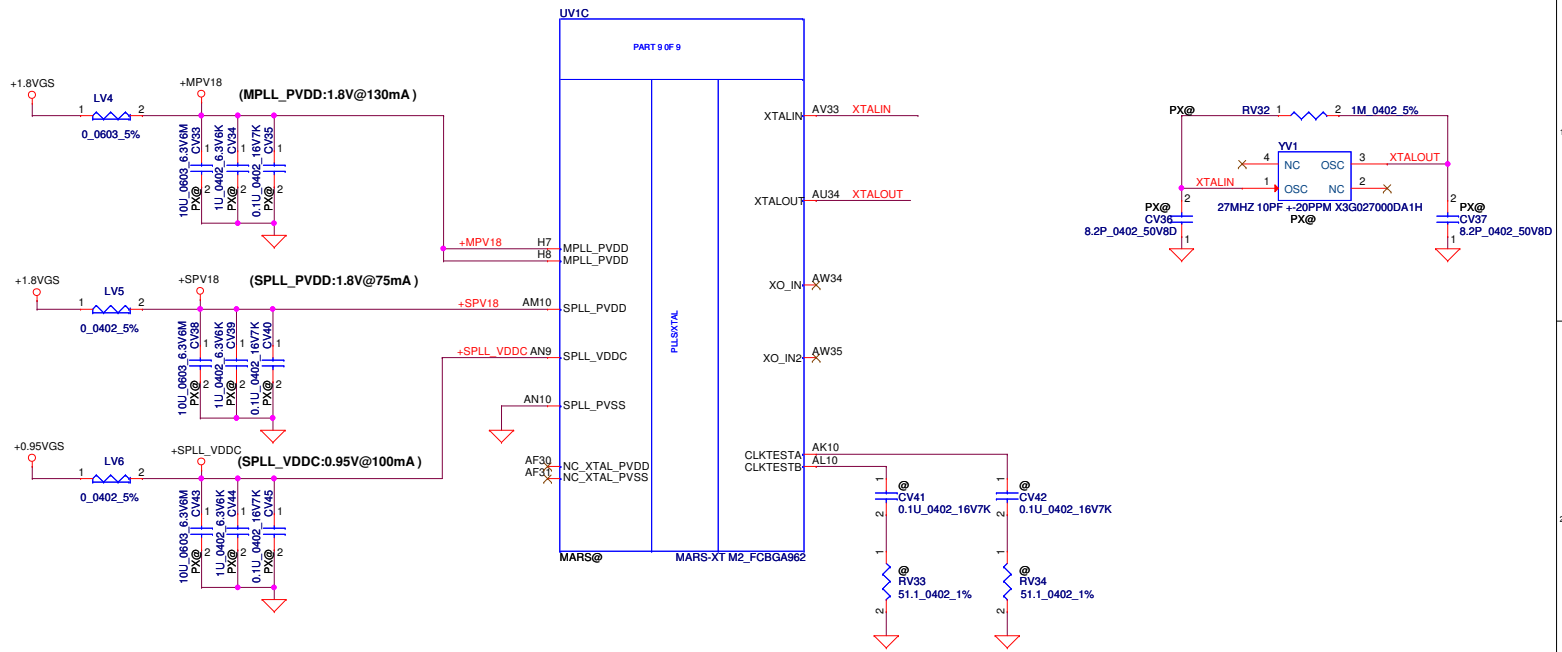
Place CLOSE VGA CHIP



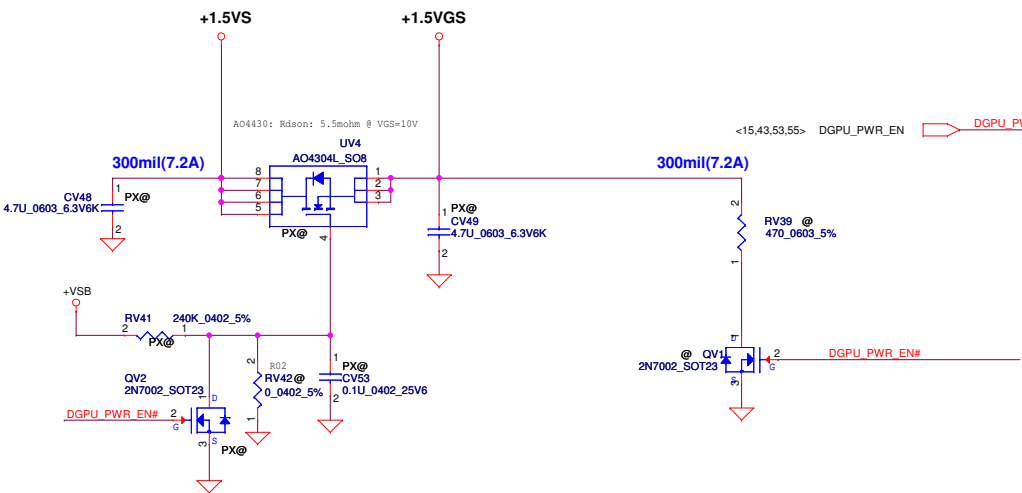
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

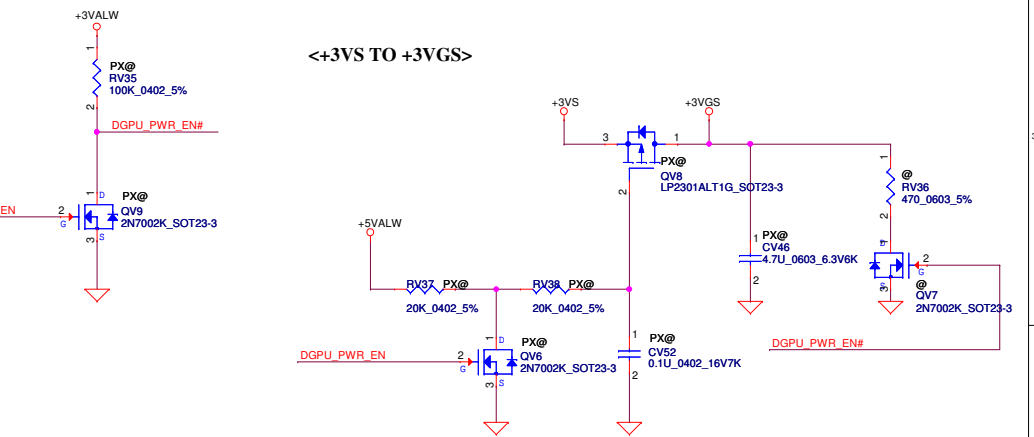
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



**+1.5VS to +1.5VGS Transfer**

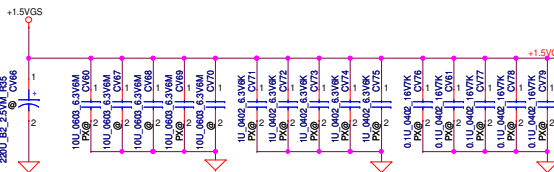


**<+3VS TO +3VGS>**



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				Rev 0.3



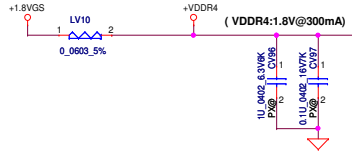
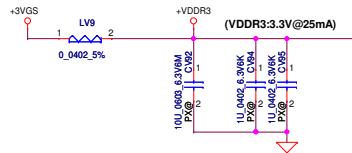
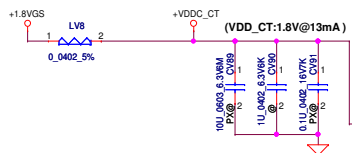


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

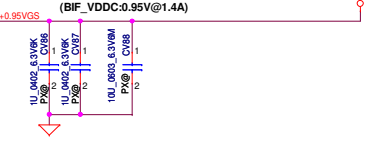
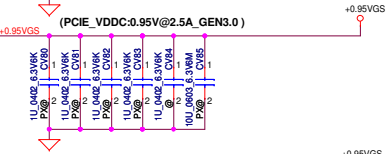
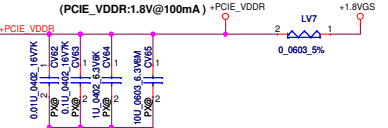
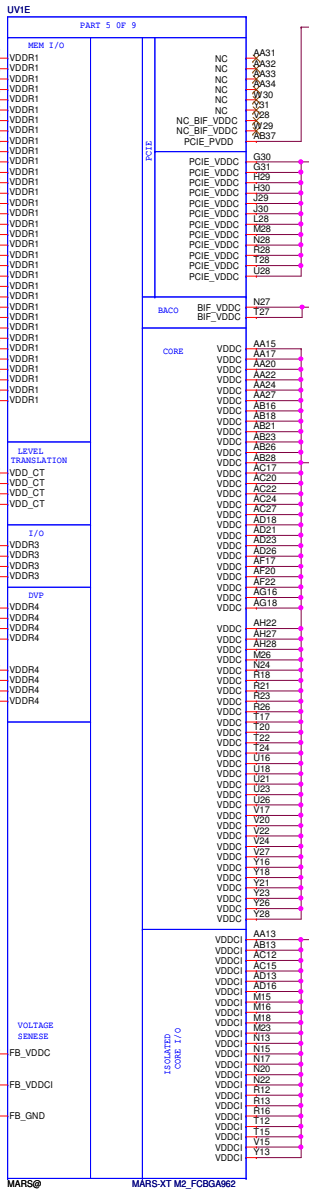
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



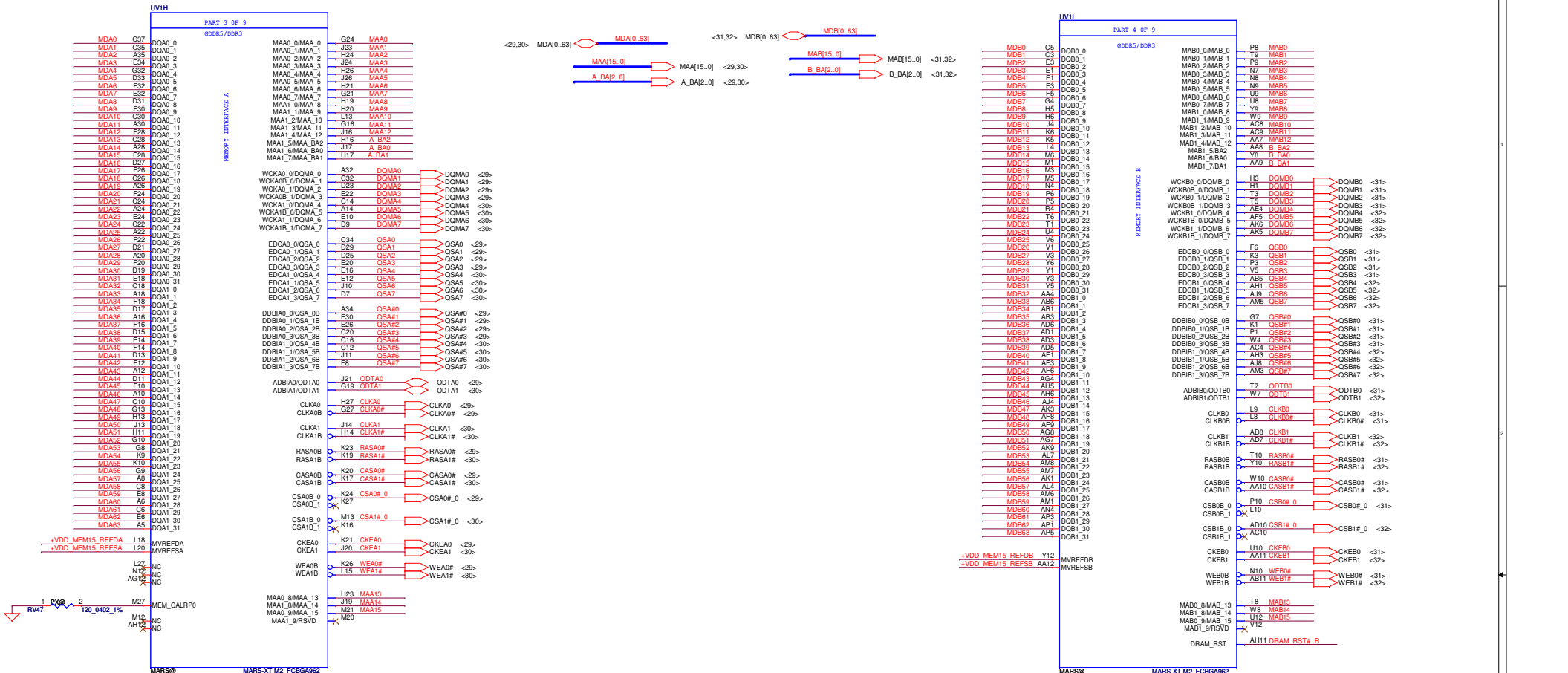
Route as differential pair

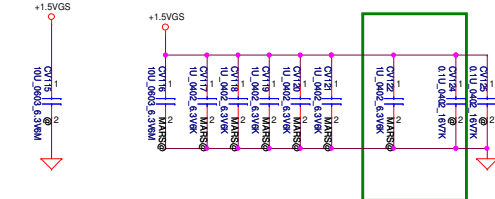
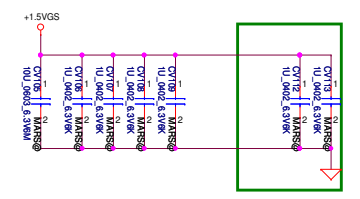
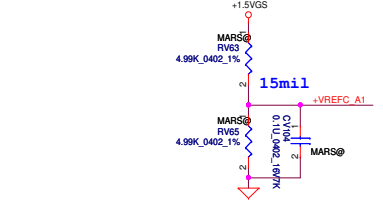
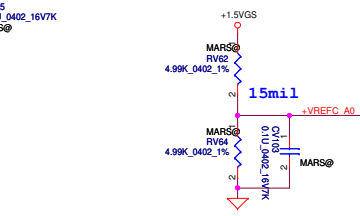
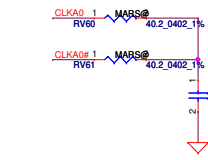
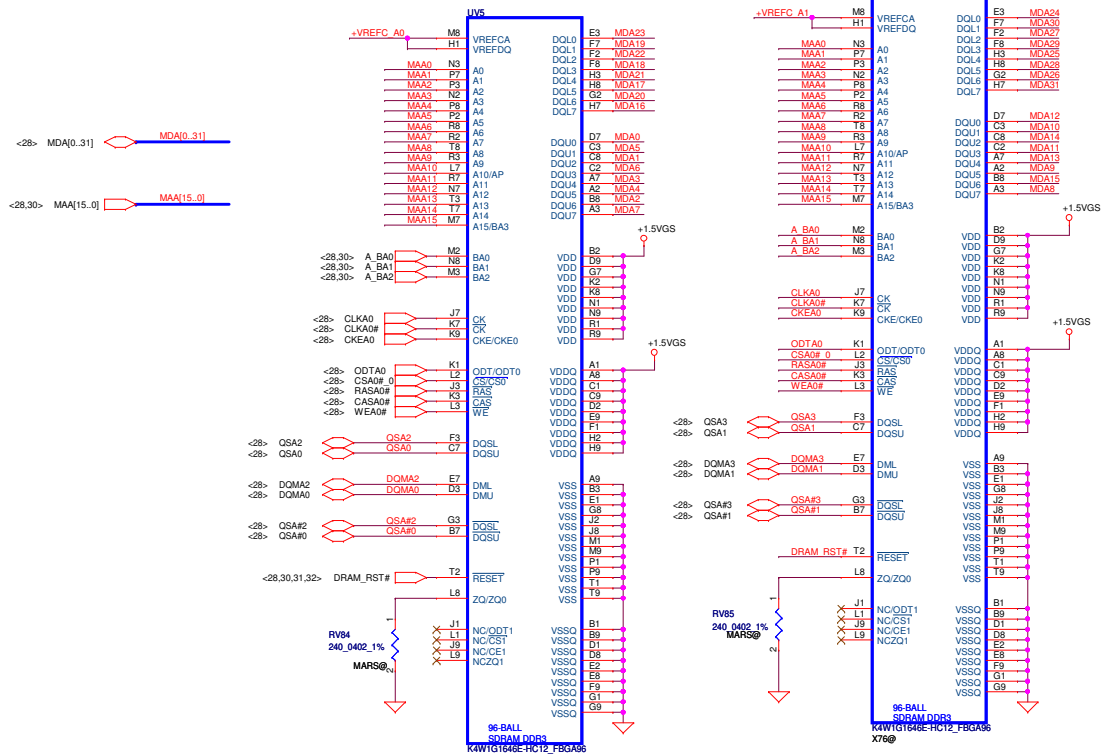


PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

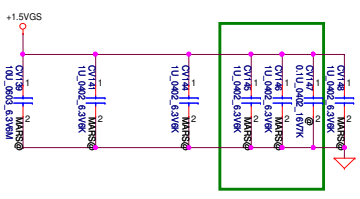
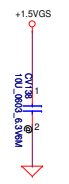
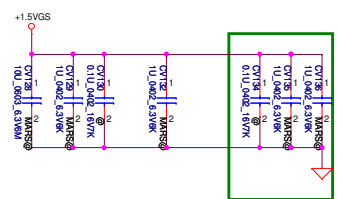
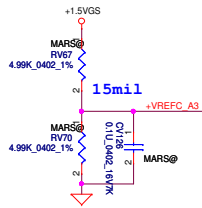
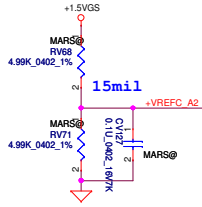
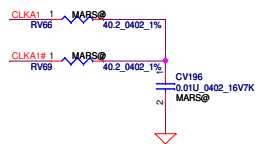
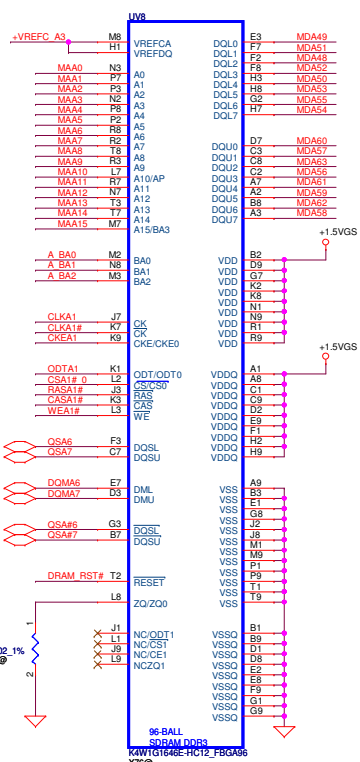
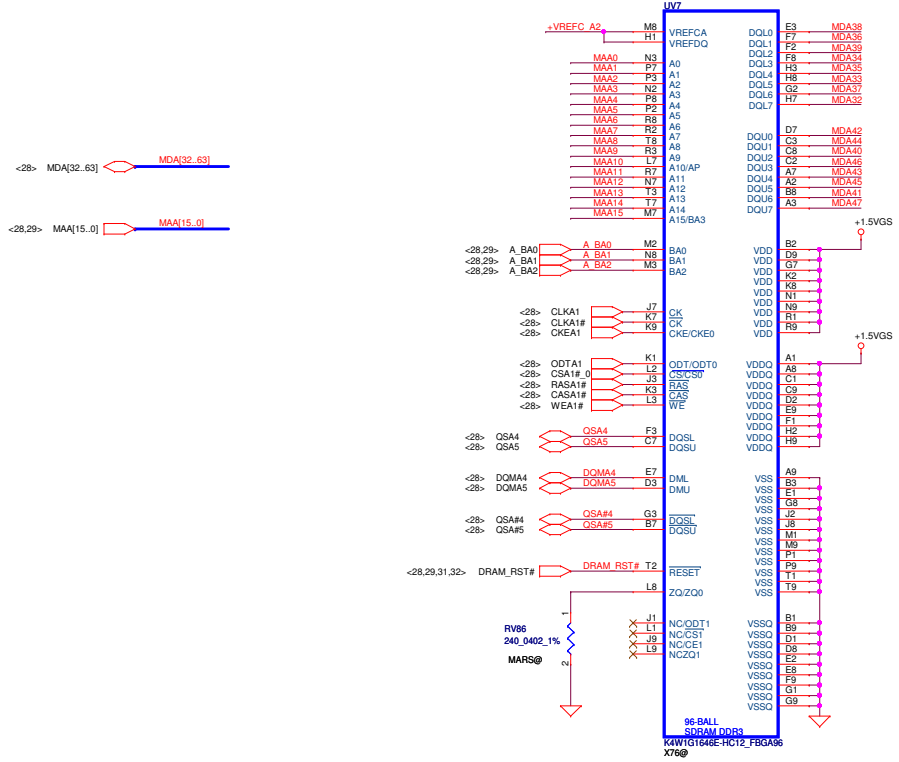
PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA\_CORE Cap in power side sheet

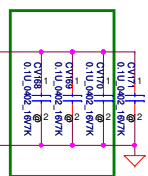
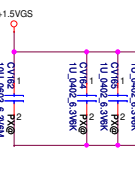
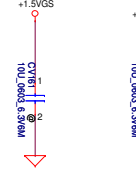
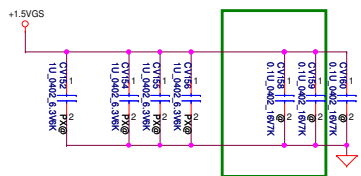
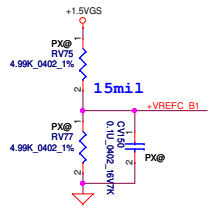
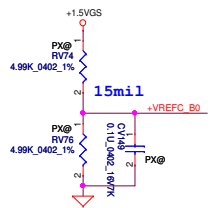
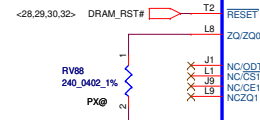
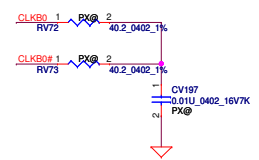
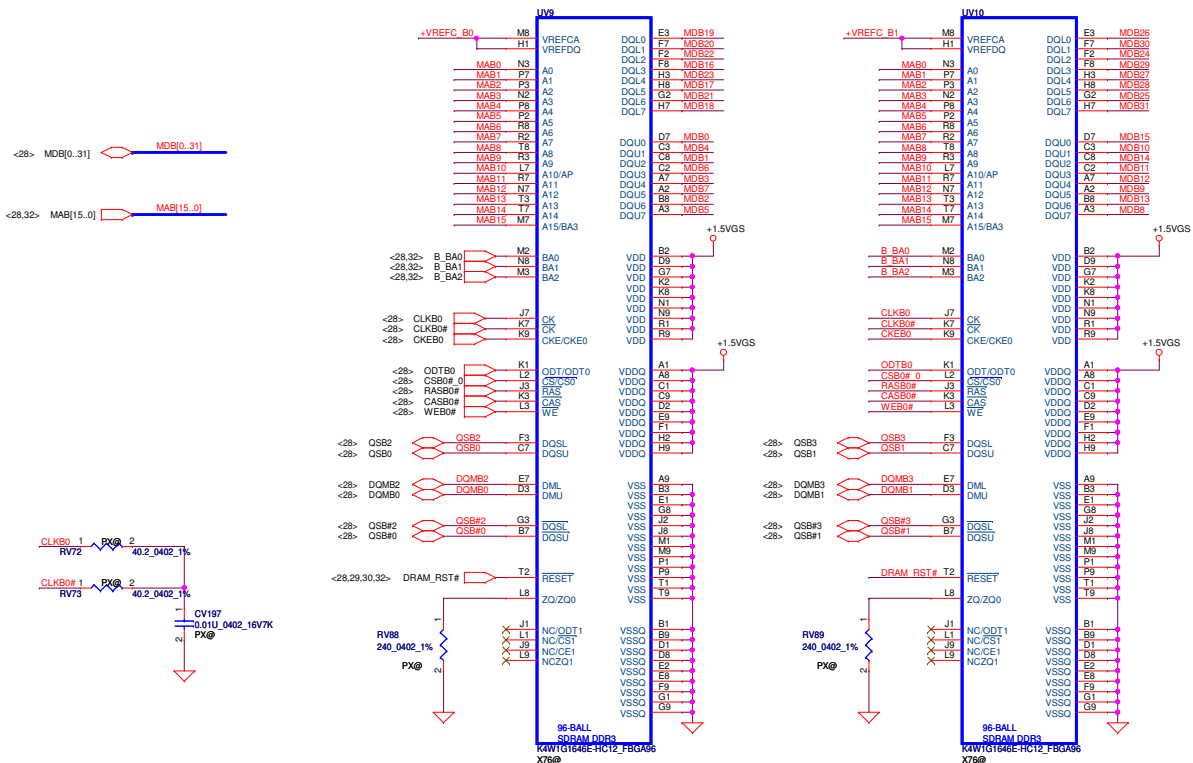




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C	QIY2 LA6884P	0.3		Wednesday, March 06, 2013   Sheet 29 of 61		



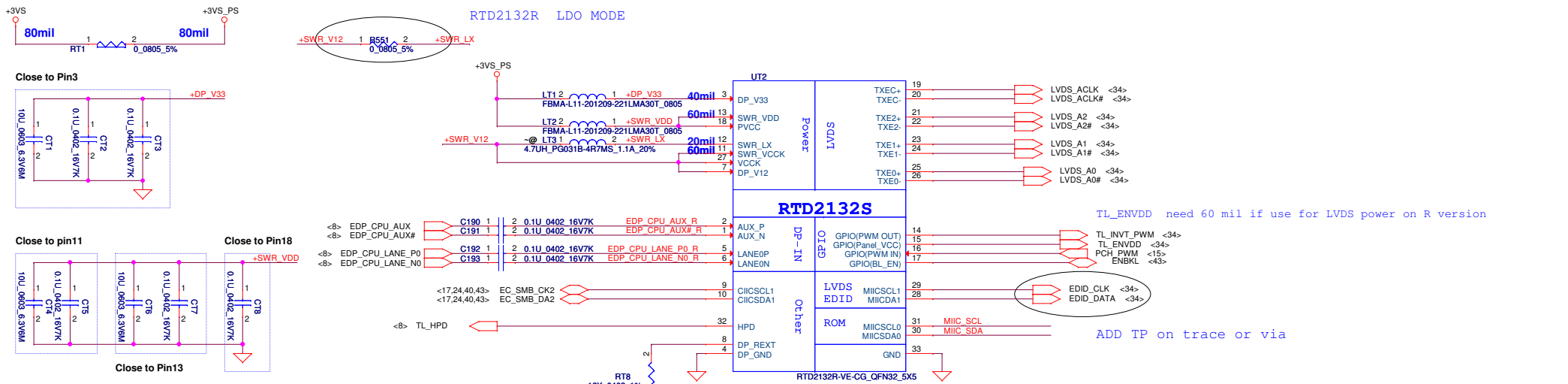
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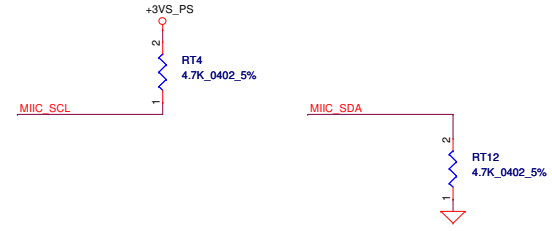
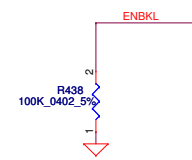
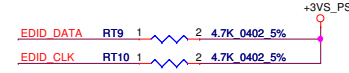






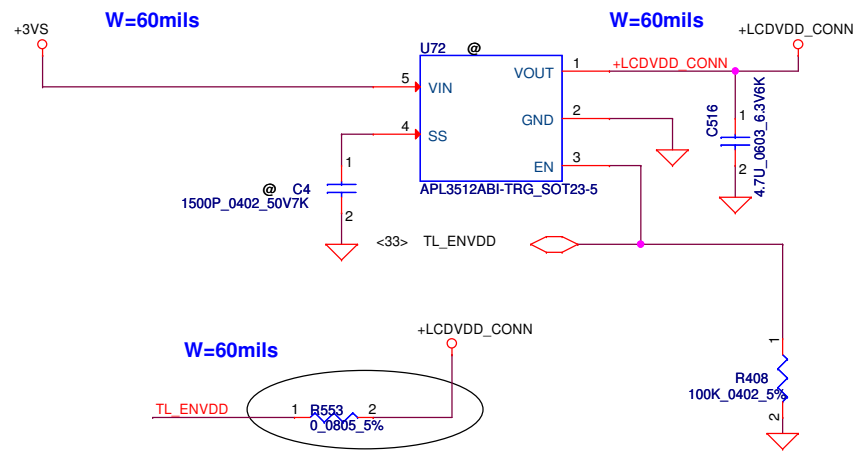
TL\_ENVDD need 60 mil if use for LVDS power on R version

ADD TP on trace or via

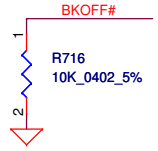


	MIIC_SDA	0	1
MIIC_SCL		X	EC CODE
		1	Internal ROM
			EEPROM

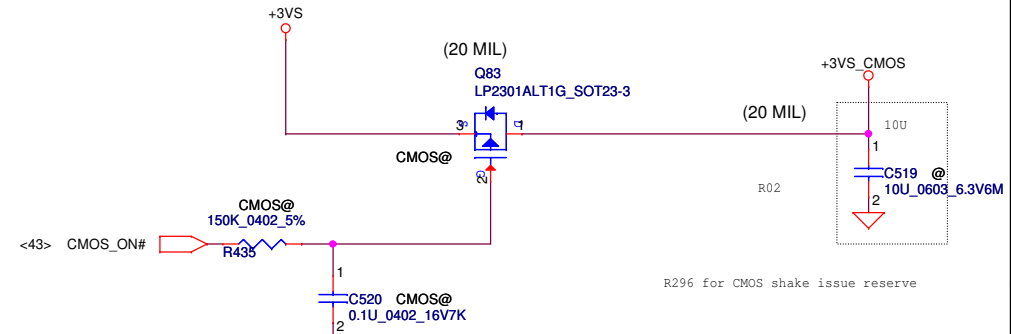
# LCD POWER CIRCUIT



RTD2132R Internal load switch for +LCD\_VCC

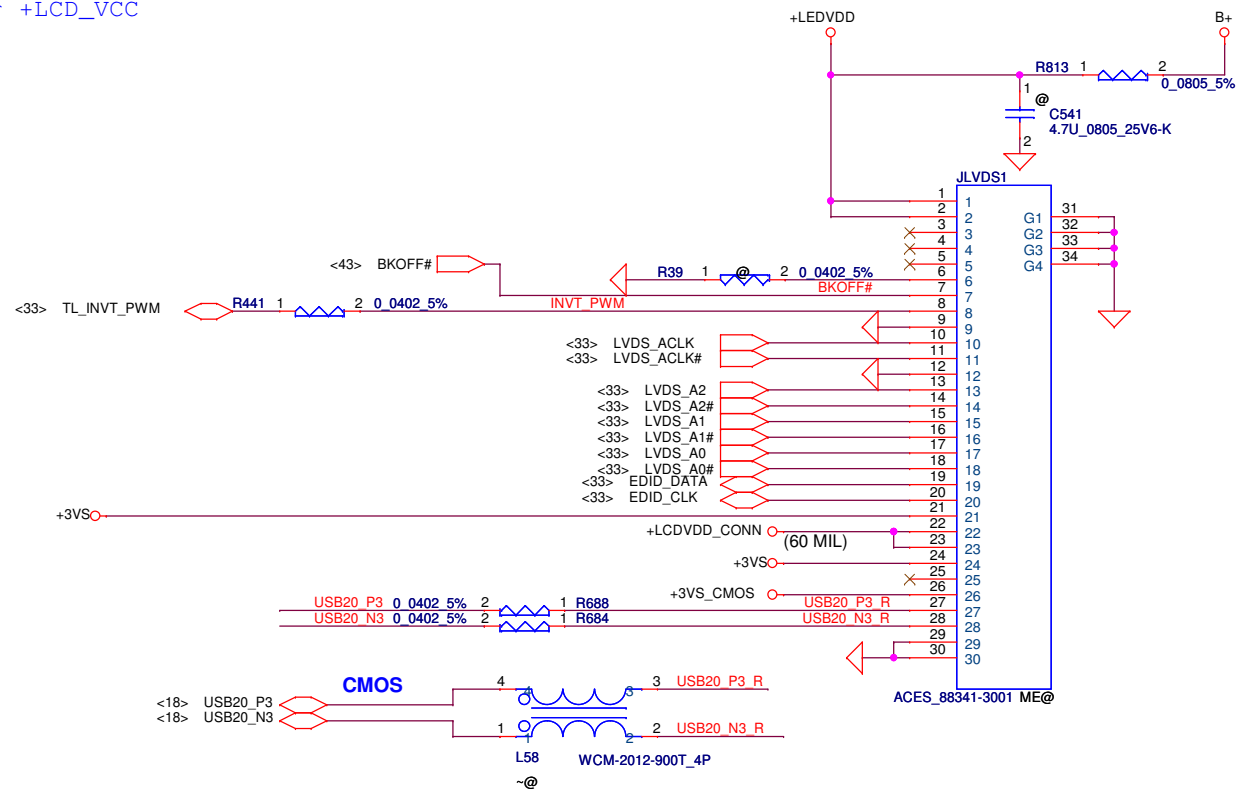


# CMOS Camera



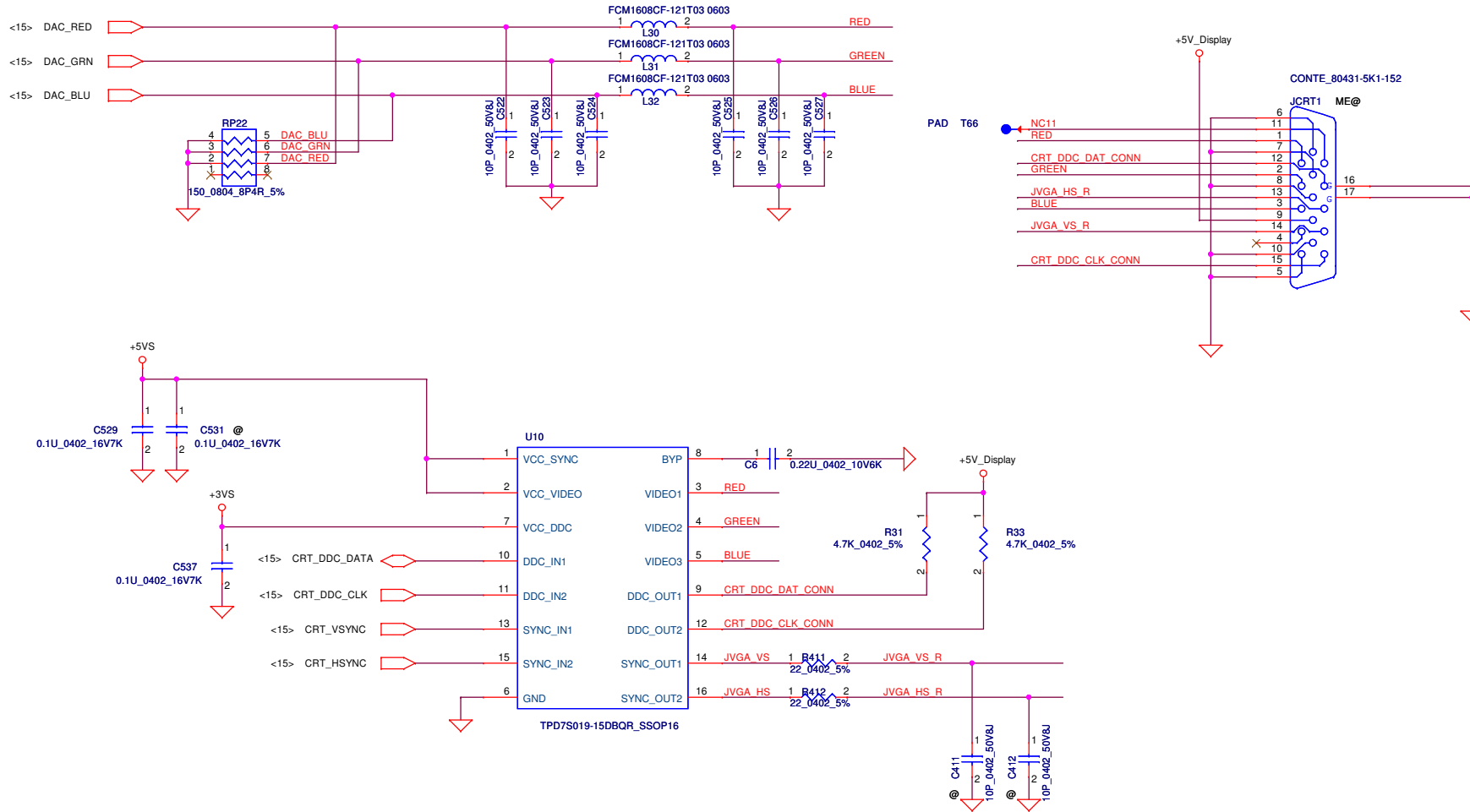
R296 for CMOS shake issue reserve

# VGA LCD/PANEL BD. Conn.

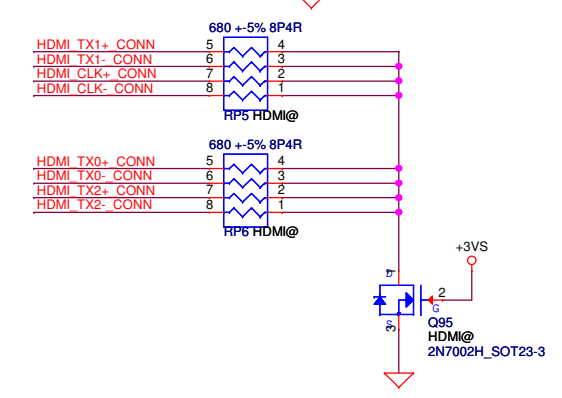
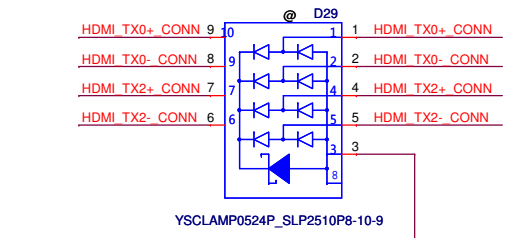
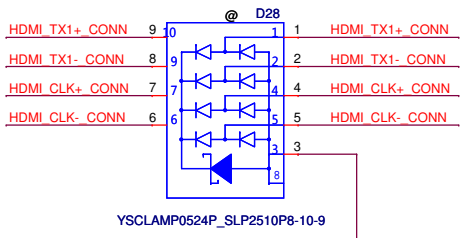
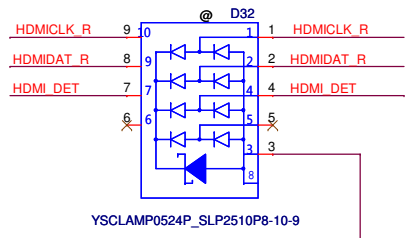
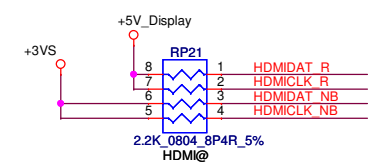
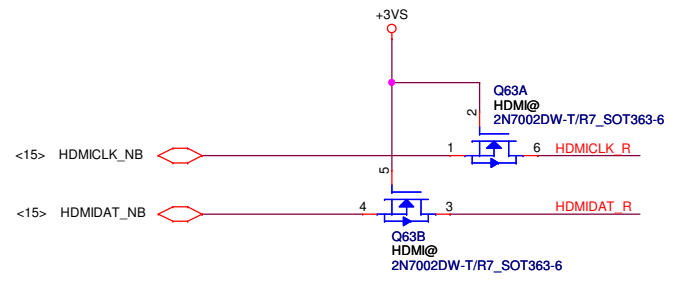
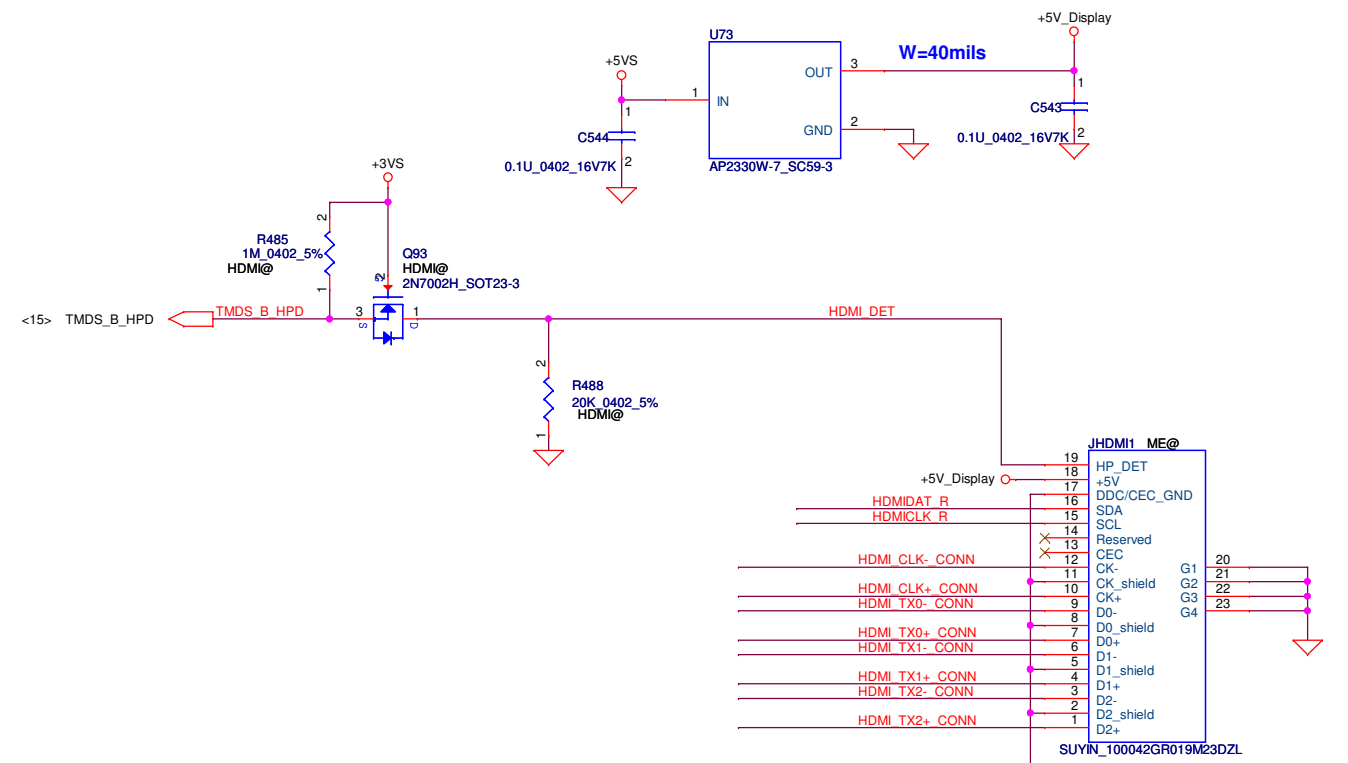
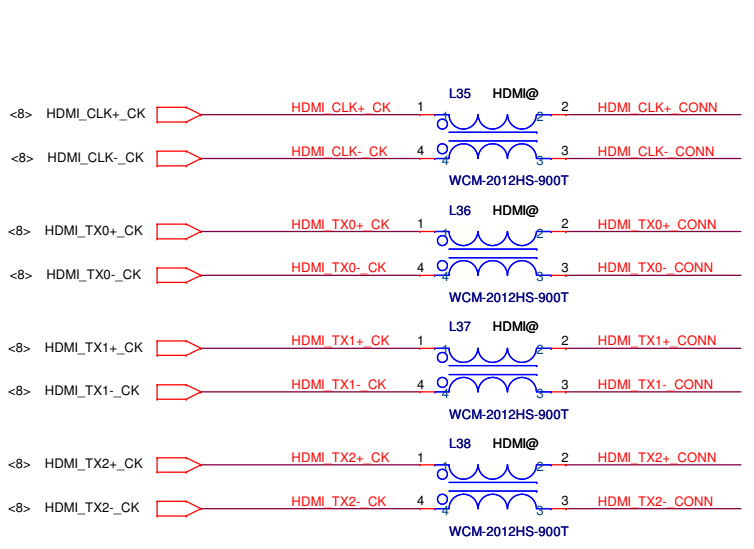


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				LA-9641P
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# CRT Connector

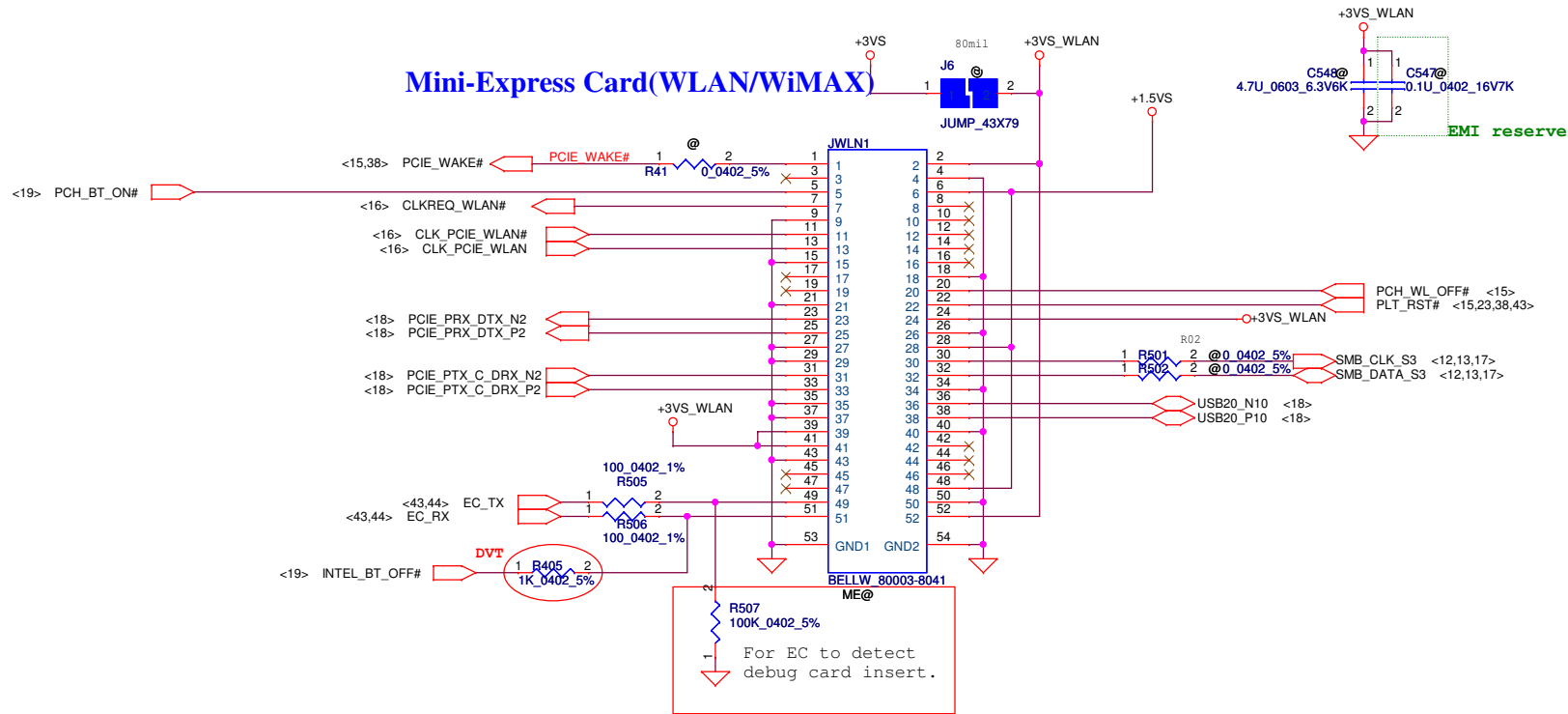


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Date:	Wednesday, March 06, 2013	Sheet	35	of	61

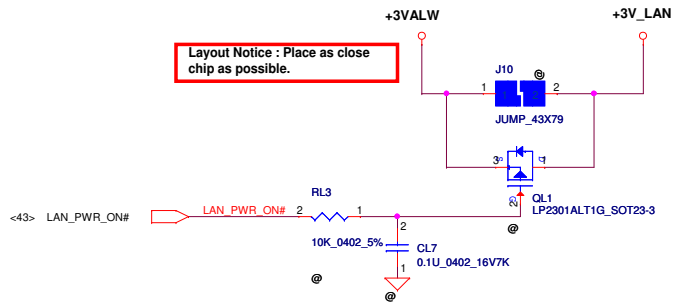


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				HDMI CONN	
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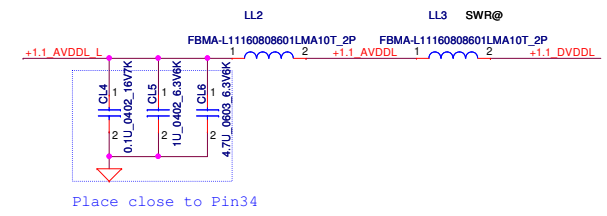
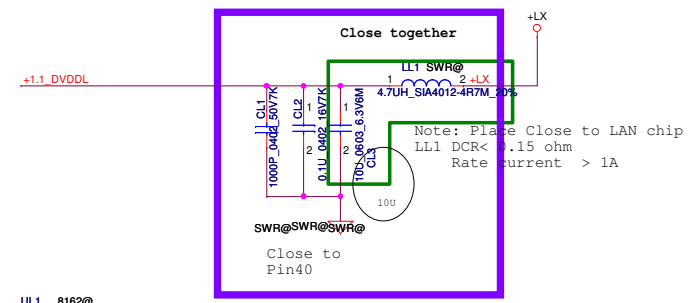
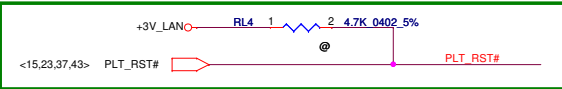
# Mini-Express Card for WLAN/WiMAX(Half)



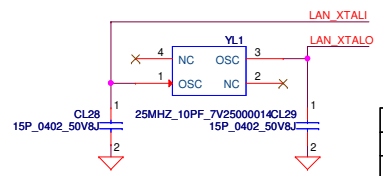
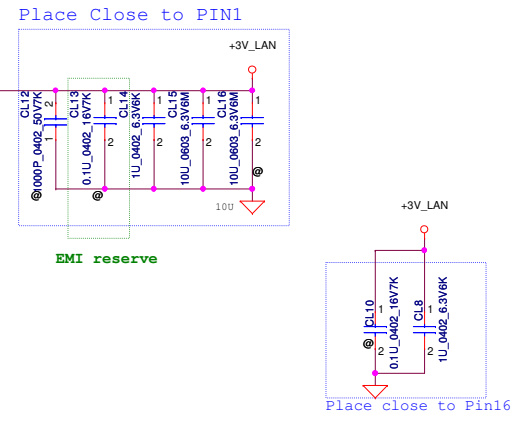
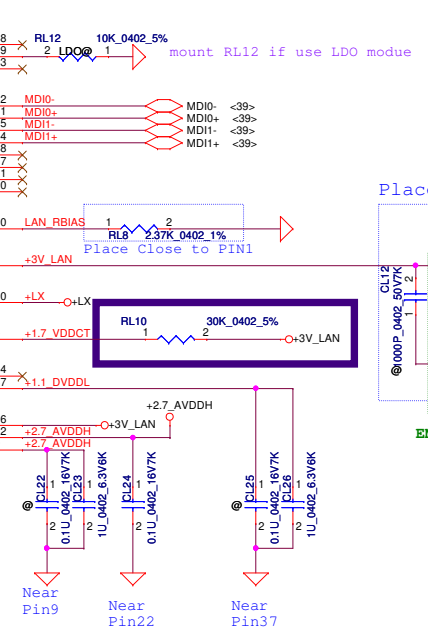
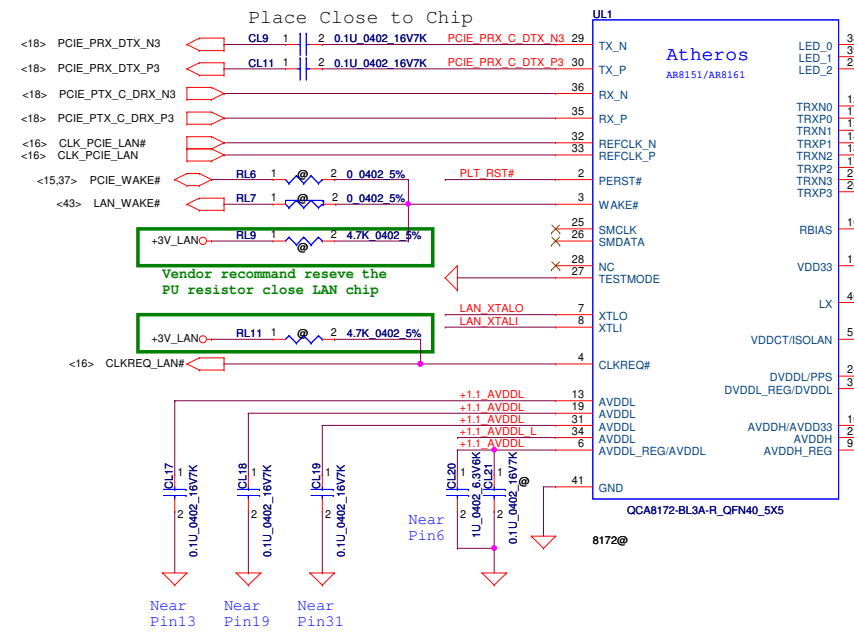
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title <b>Mini-Card/NEW Card/SIM</b>	
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				Document Number <b>LA-9641P</b>	Date: Wednesday, March 06, 2013



Vendor recommend reseve the PU resistor close LAN chip



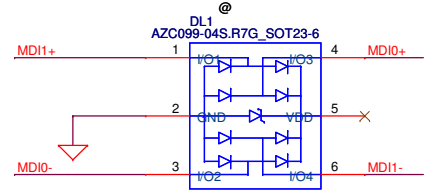
SA000065410 S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL  
 SA000052J20 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL



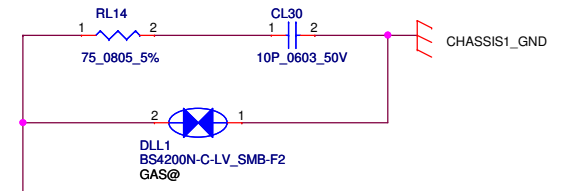
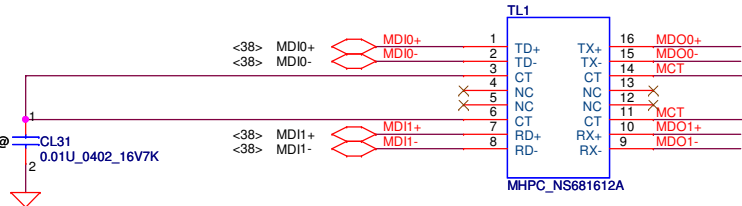
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Custom	LA-7982P	Rev	0.3		

**DL1**  
 1'S PN:SC300001G00  
 2'S PN:SC300002E00

Place Close to TL1

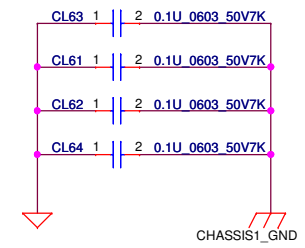
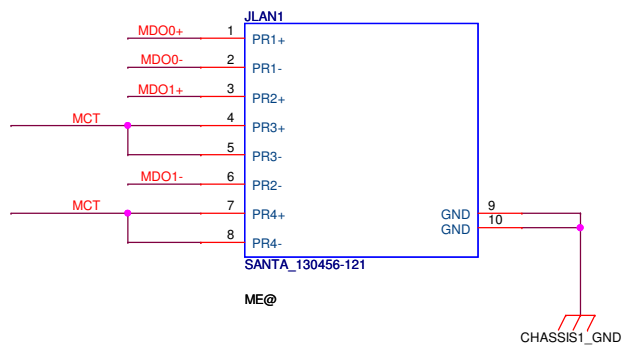


Reserve gas tube for EMI go rural solution

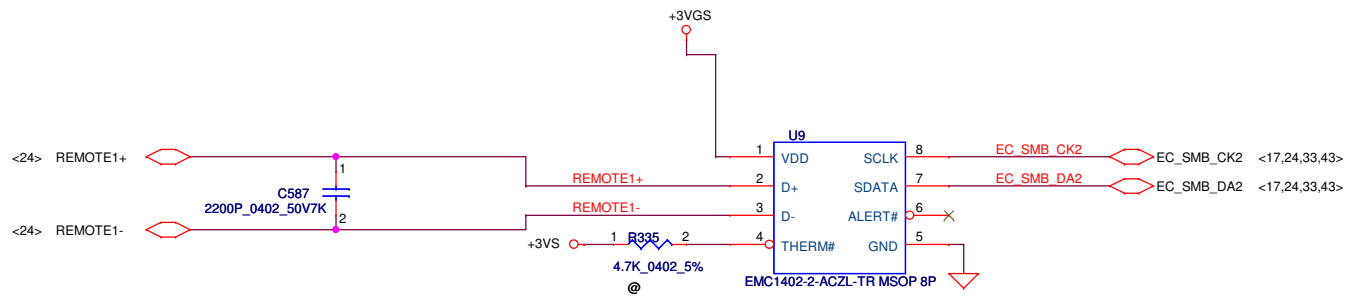


Place Close to TL1

Need check Symbol

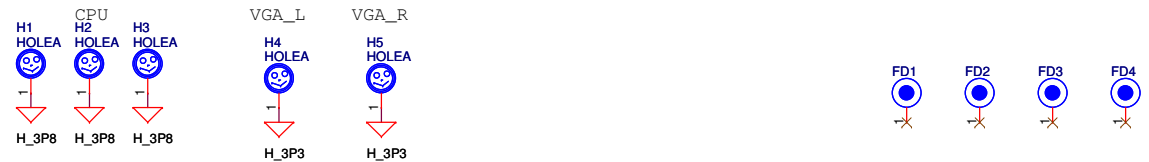


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				LA-7982P	0.3
				Date:	Wednesday, March 06, 2013
				Sheet	39 of 61

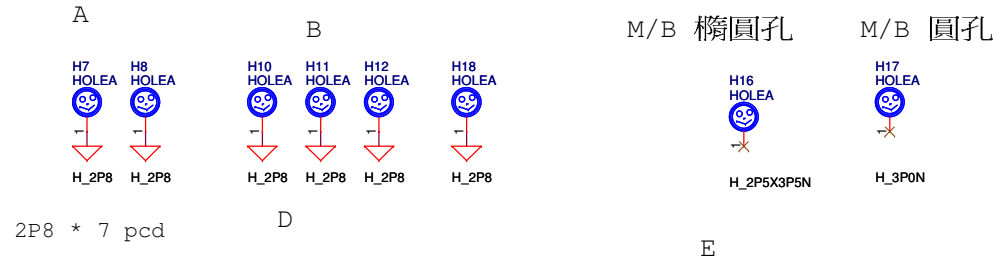
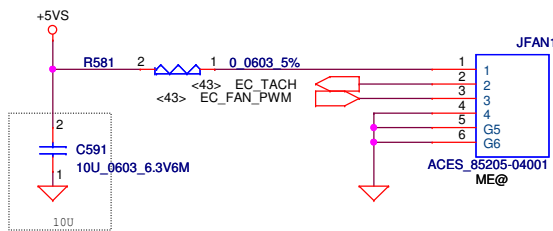


EMC1412-A (SA00003YA00)  
 Address 1111\_100xb  
 SIC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1, 2+/-:  
 Trace width/space: 10/10 mil  
 Trace length: <8"



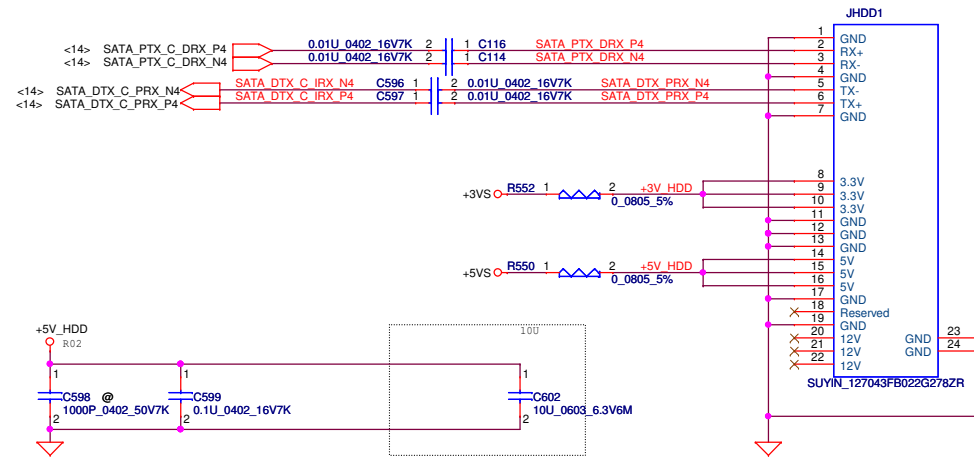
### FAN1 Conn



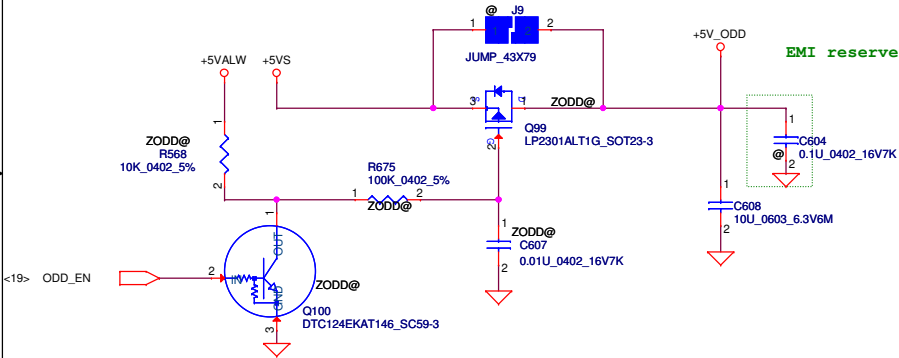
Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Fintek-Thermal IC/FAN/screw
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				Date: Wednesday, March 06, 2013	Sheet



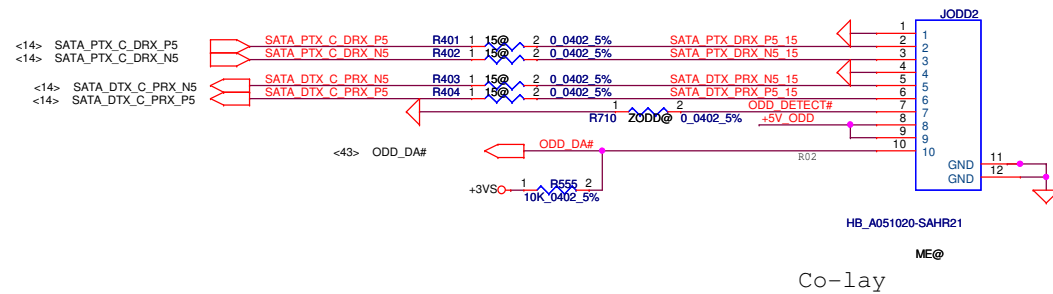
### SATA HDD Conn.



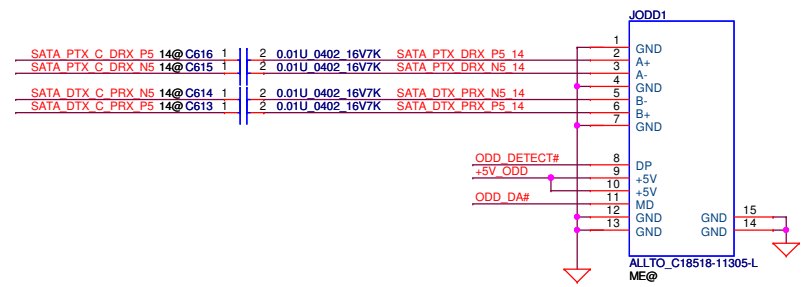
### ODD Power Control



### FOR 15" SATA ODD FFC Conn.

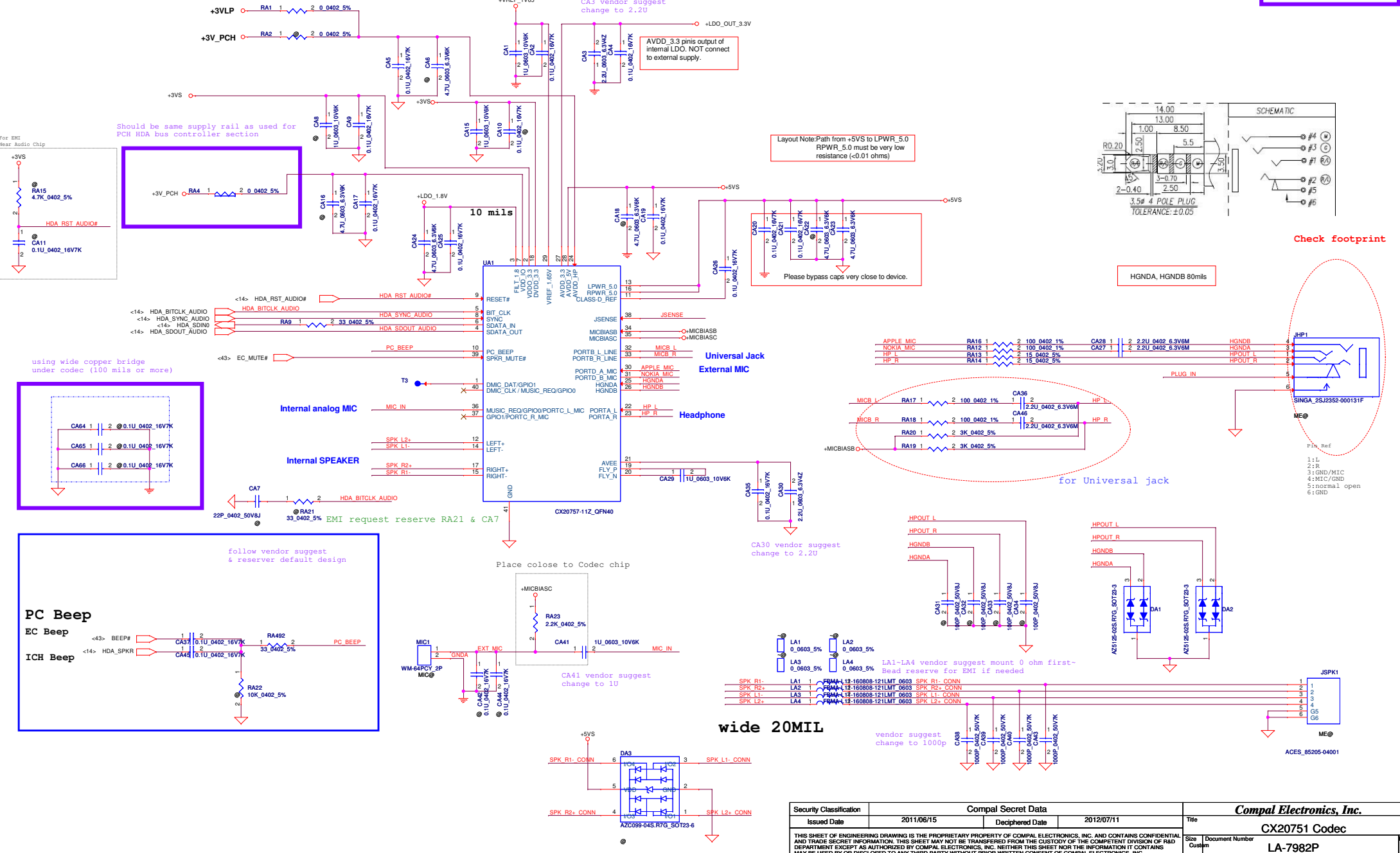


### FOR 14" SATA ODD Conn.



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Compal Electronics, Inc. <b>HDD/ODD/BT Connector</b>			Document Number <b>LA-9641P</b>	Revision 0.3
Date: Wednesday, March 06, 2013			Sheet 41	of 61

**CX20751**  
**High Definition Audio Codec SoC**  
**With Integrated Class-D Stereo**  
**Amplifier.**  
**An integrated 5 V to 3.3 V Low-dropout**  
**voltage regulator (LDO).**  
**An integrated 3.3 V to 1.8V Low-dropout**  
**voltage regulator (LDO).**



Sense resistors must be connected same power that is used for VAUX\_3.3

mount RA6 on the Jack Sense circuit to configure Port-C for mono MIC.

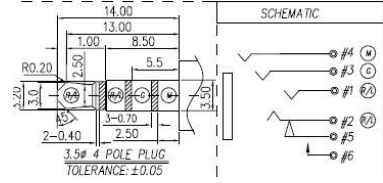
Don't support LINE\_IN function RA7 could be @

CA3 vendor suggest change to 2.2U

AVDD\_3.3 pins output of internal LDO. NOT connect to external supply.

Layout Note: Path from +5VS to LPWR\_5.0 RPWR\_5.0 must be very low resistance (<0.01 ohms)

Please bypass caps very close to device.



Check footprint

HGNDA, HGNDB 80mils

for Universal jack

CA30 vendor suggest change to 2.2U

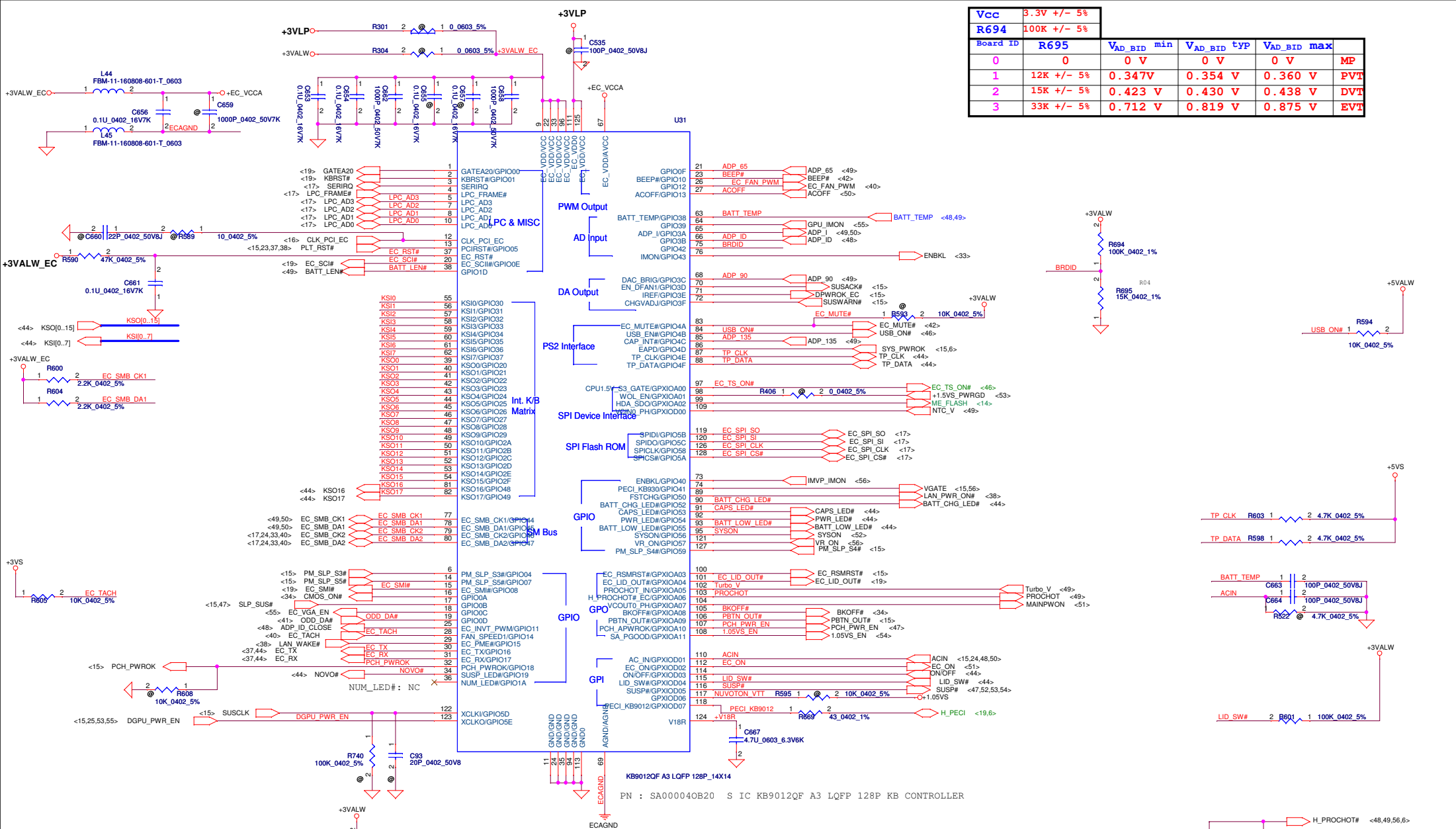
Place colose to Codec chip

CA41 vendor suggest change to 1U

wide 20MIL

vendor suggest change to 1000p

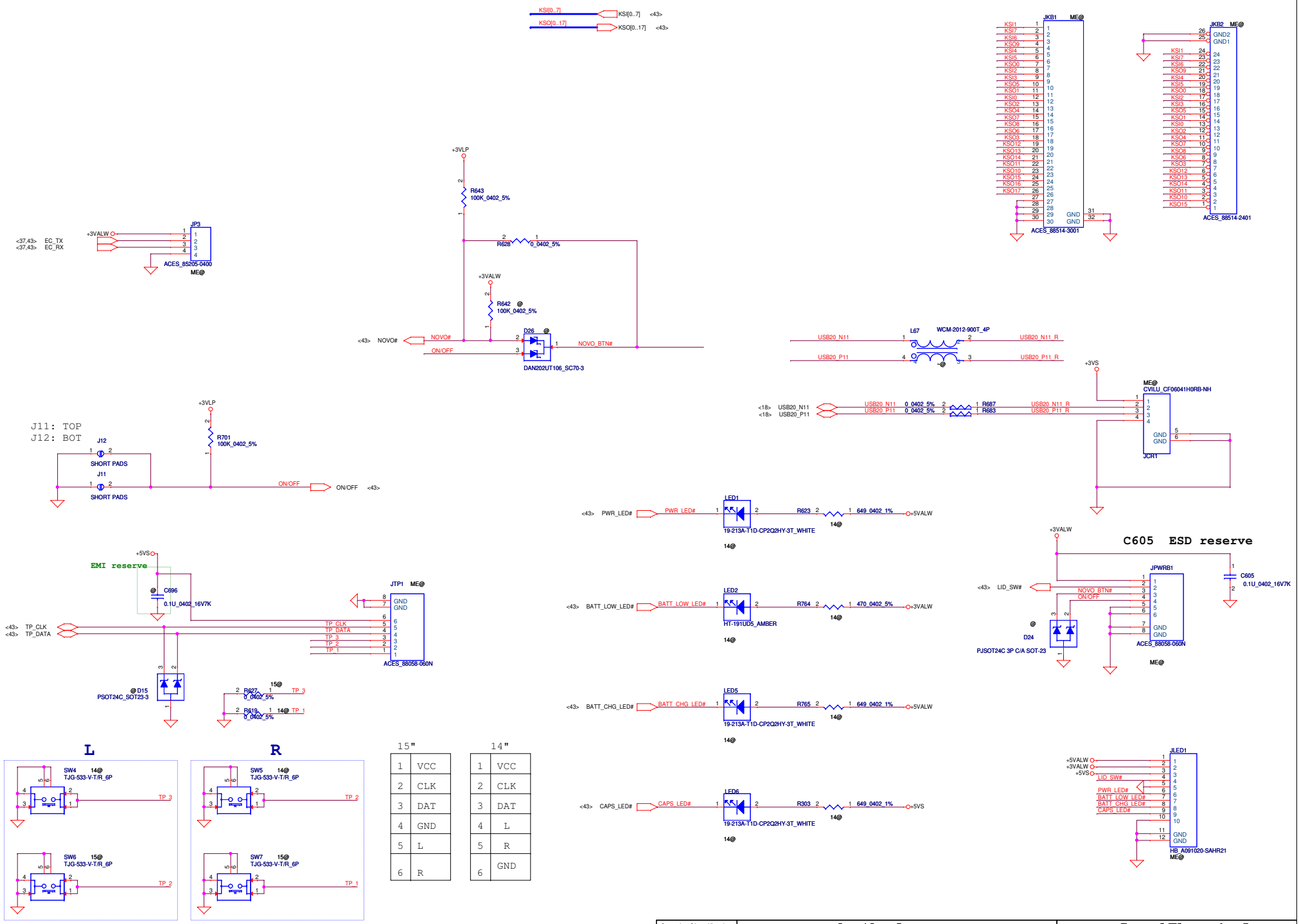
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	CX20751 Codec
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Custom	LA-7982P	0.3			
Date:	Wednesday, March 06, 2013	Sheet	42	of	61



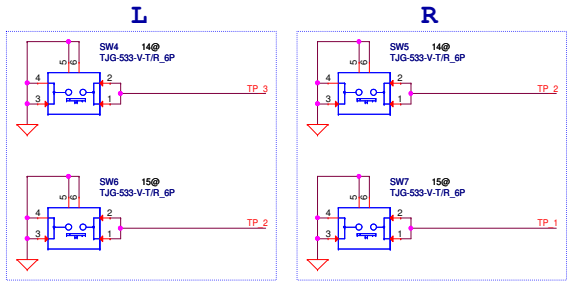
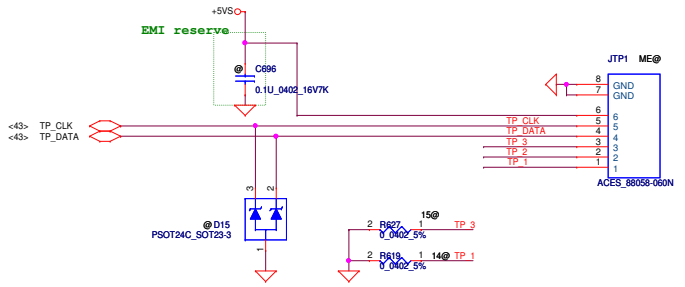
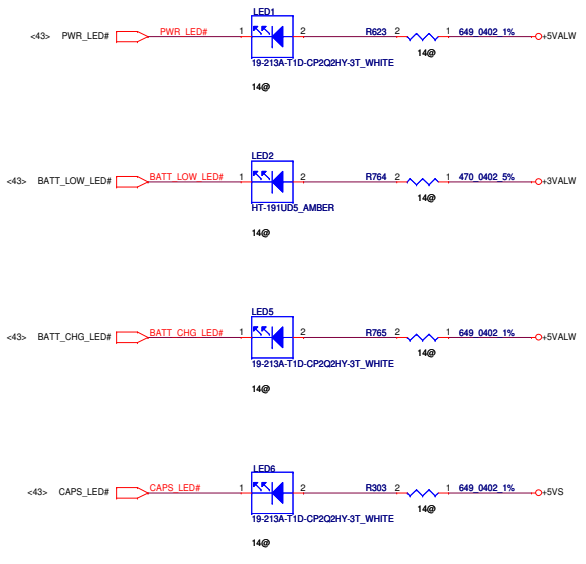
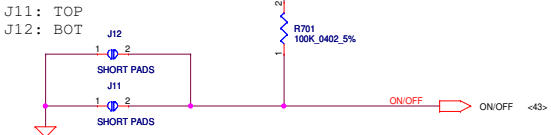
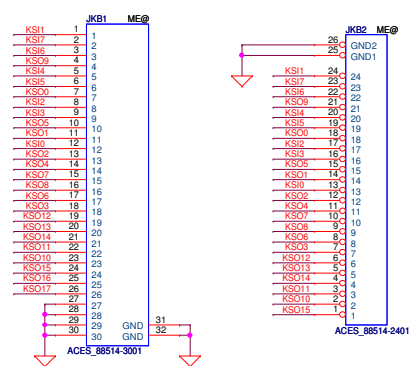
Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	MP
0	0	0 V	0 V	0 V	
1	12K +/- 5%	0.347V	0.354 V	0.360 V	PVT
2	15K +/- 5%	0.423 V	0.430 V	0.438 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

PN : SA000040B20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

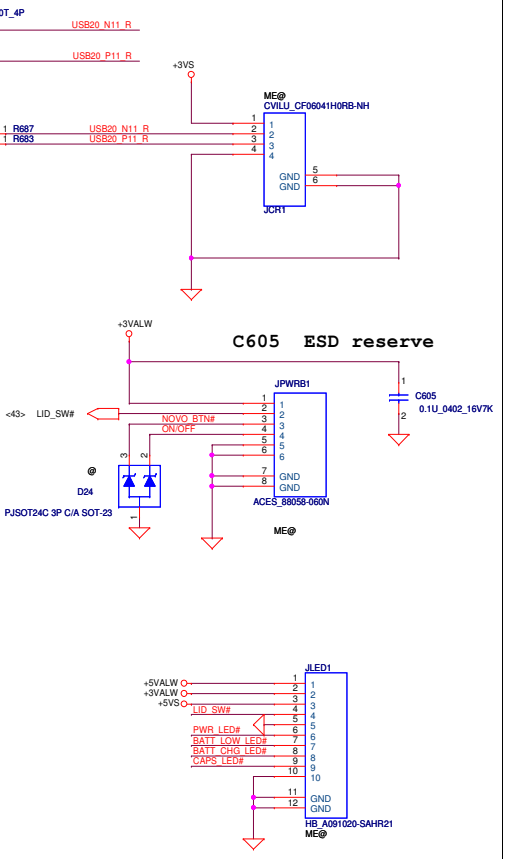
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Issued Date	2011/06/15	Deciphered Date			
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Size	Document Number	Rev	Date: Wednesday, March 06, 2013   Sheet 43 of 61		
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KSIO[.7] <43>  
KSQ[0..17] <43>



15"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND



A

B

C

D

E

1

1

2

2

3

3

4

4

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				Date Wednesday, March 06, 2013	Sheet 45	of 61

A

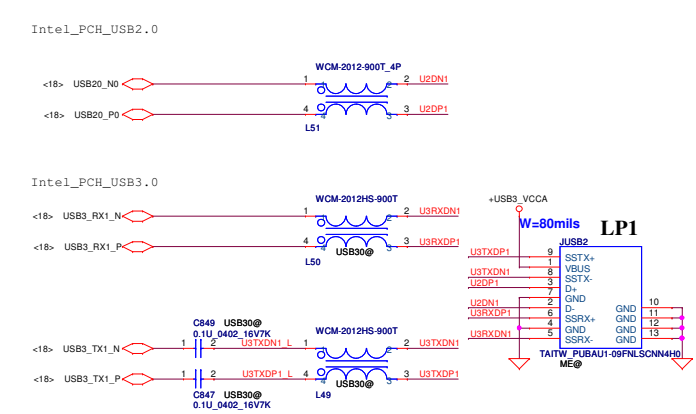
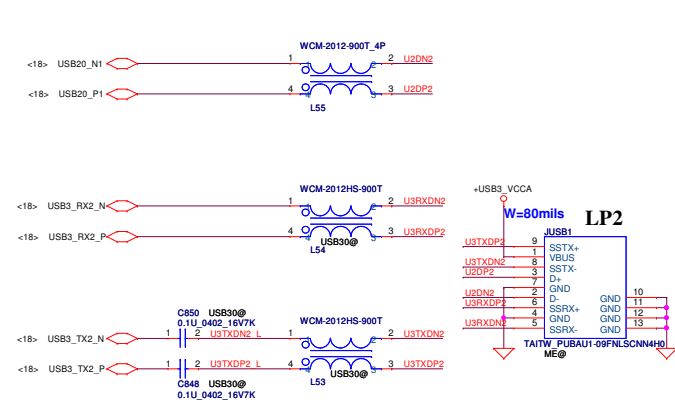
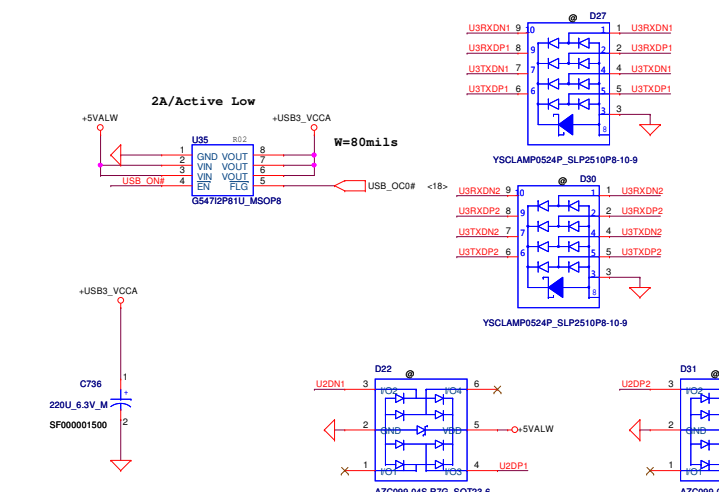
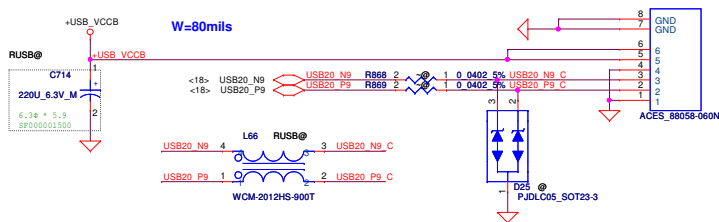
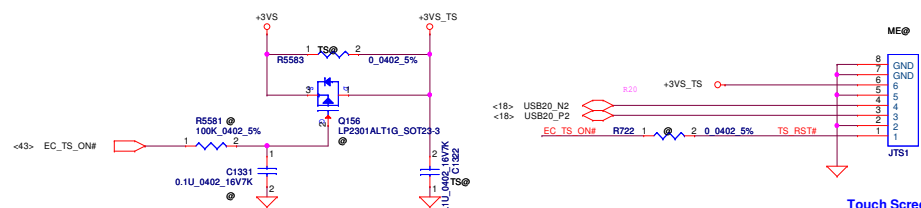
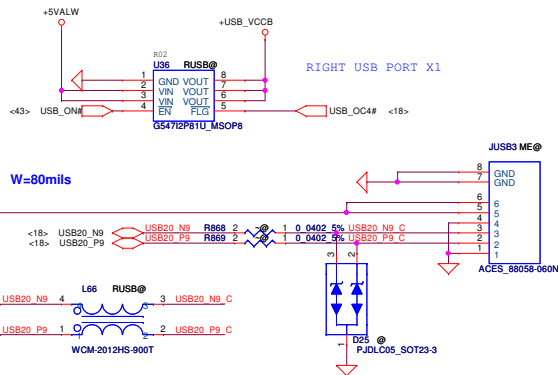
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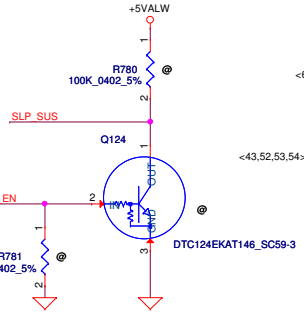
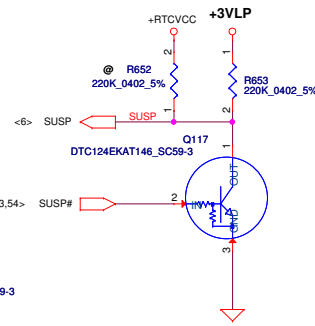
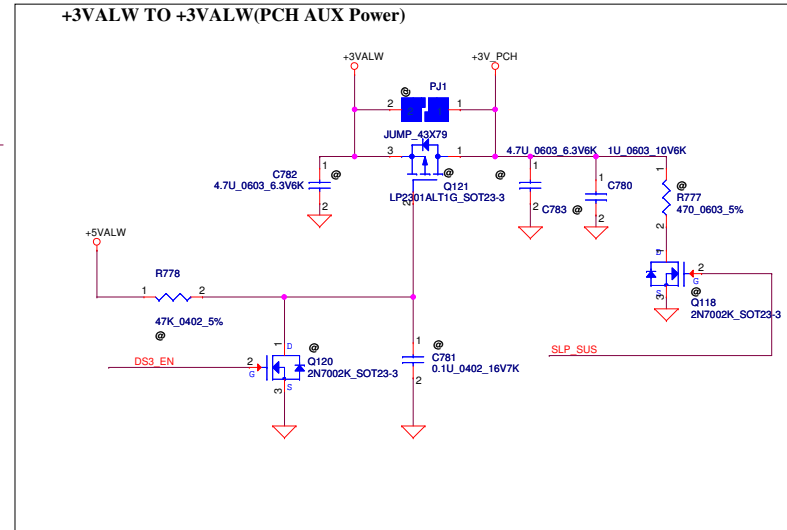
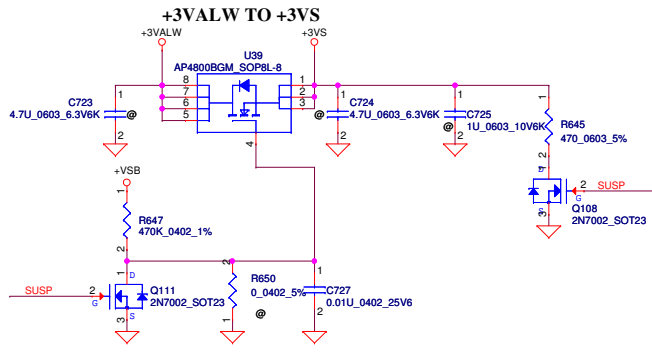
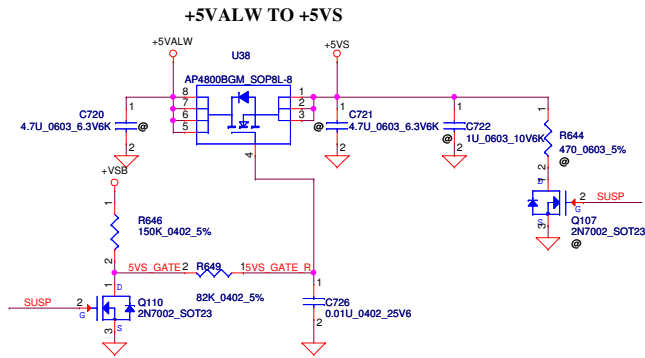
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D

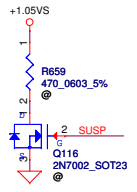
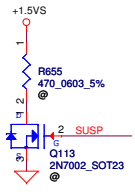
E

**Right Ext.USB Conn.**

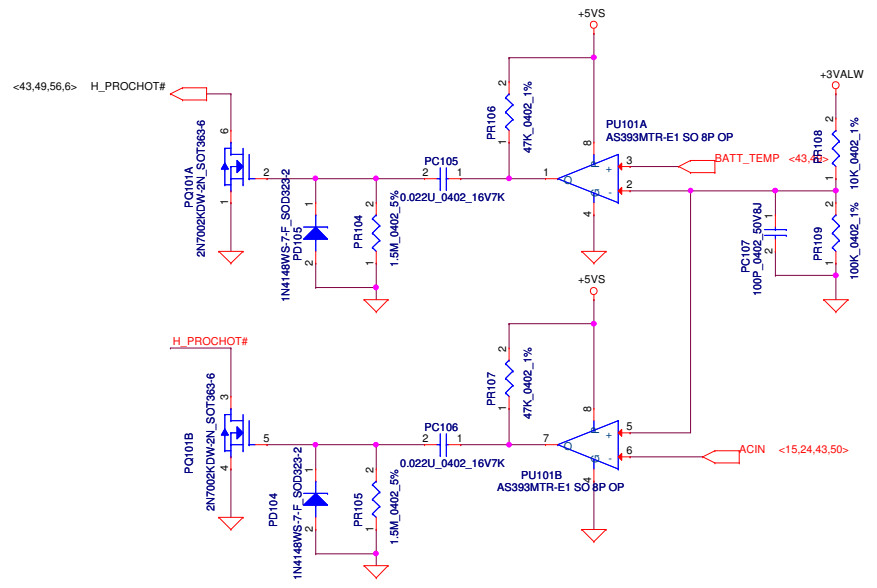
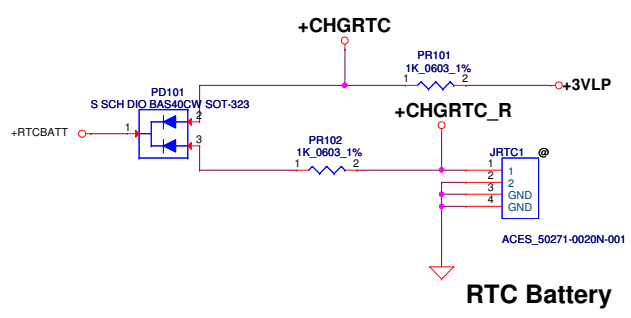
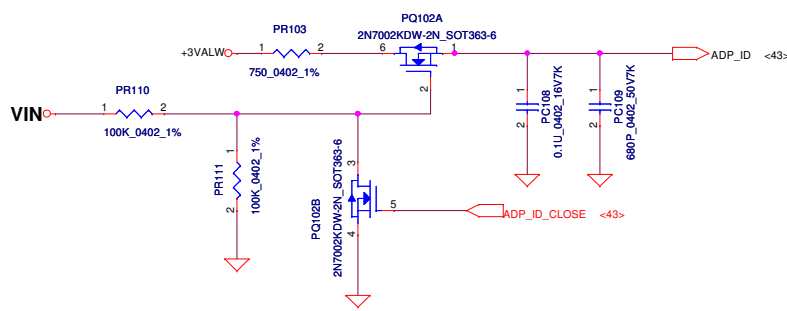
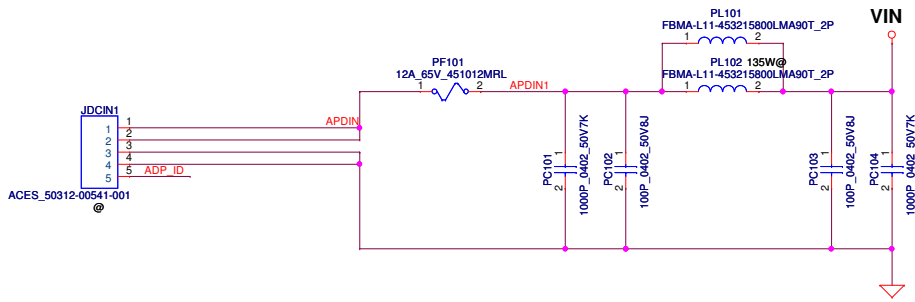




先預留,C phase再決定



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Size	Document Number	Rev		0.3	
Custom	LA-9641P	Date:		Wednesday, March 06, 2013   Sheet 47 of 61	

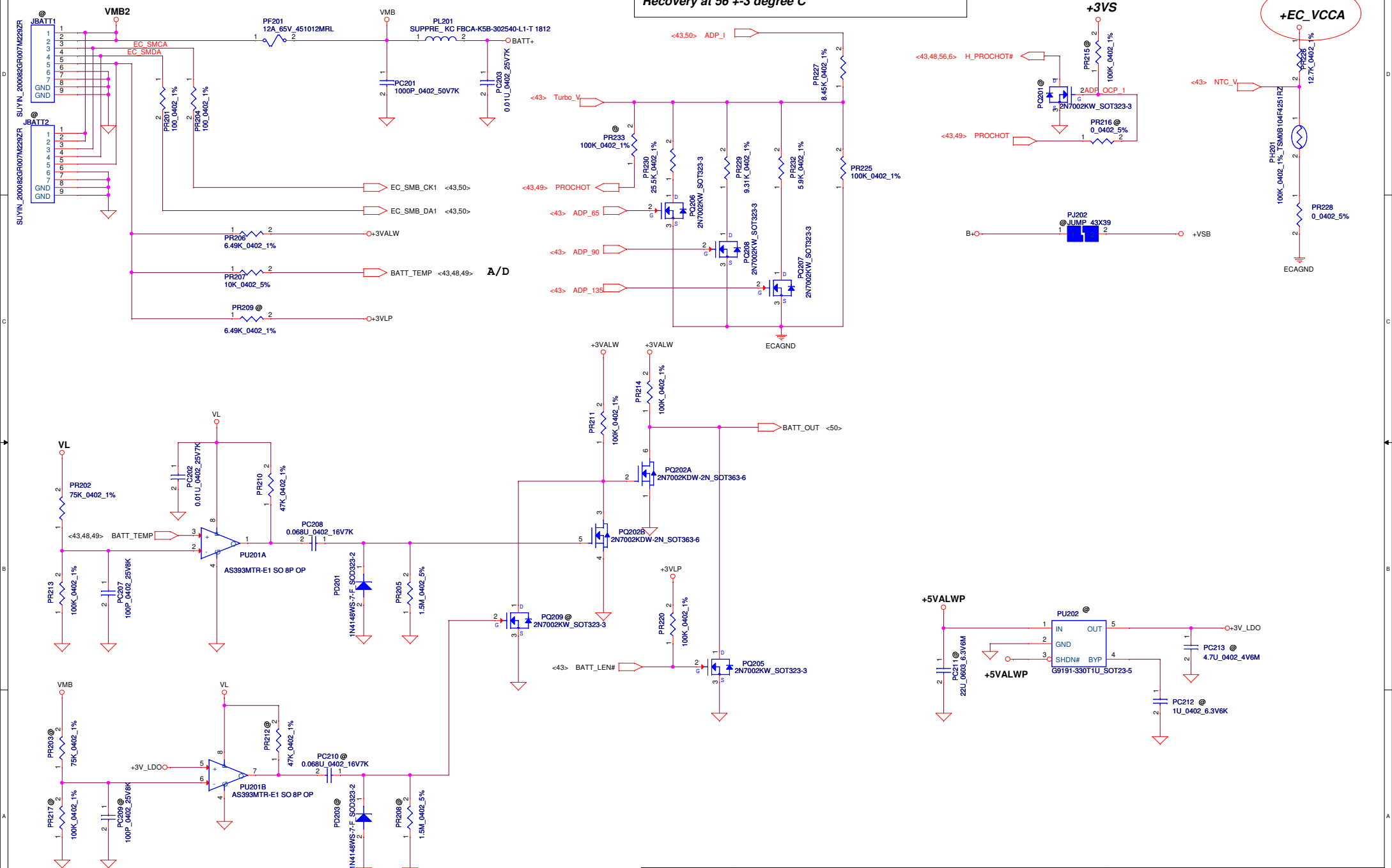


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				Document Number	Rev
				LA-9641P	0.2
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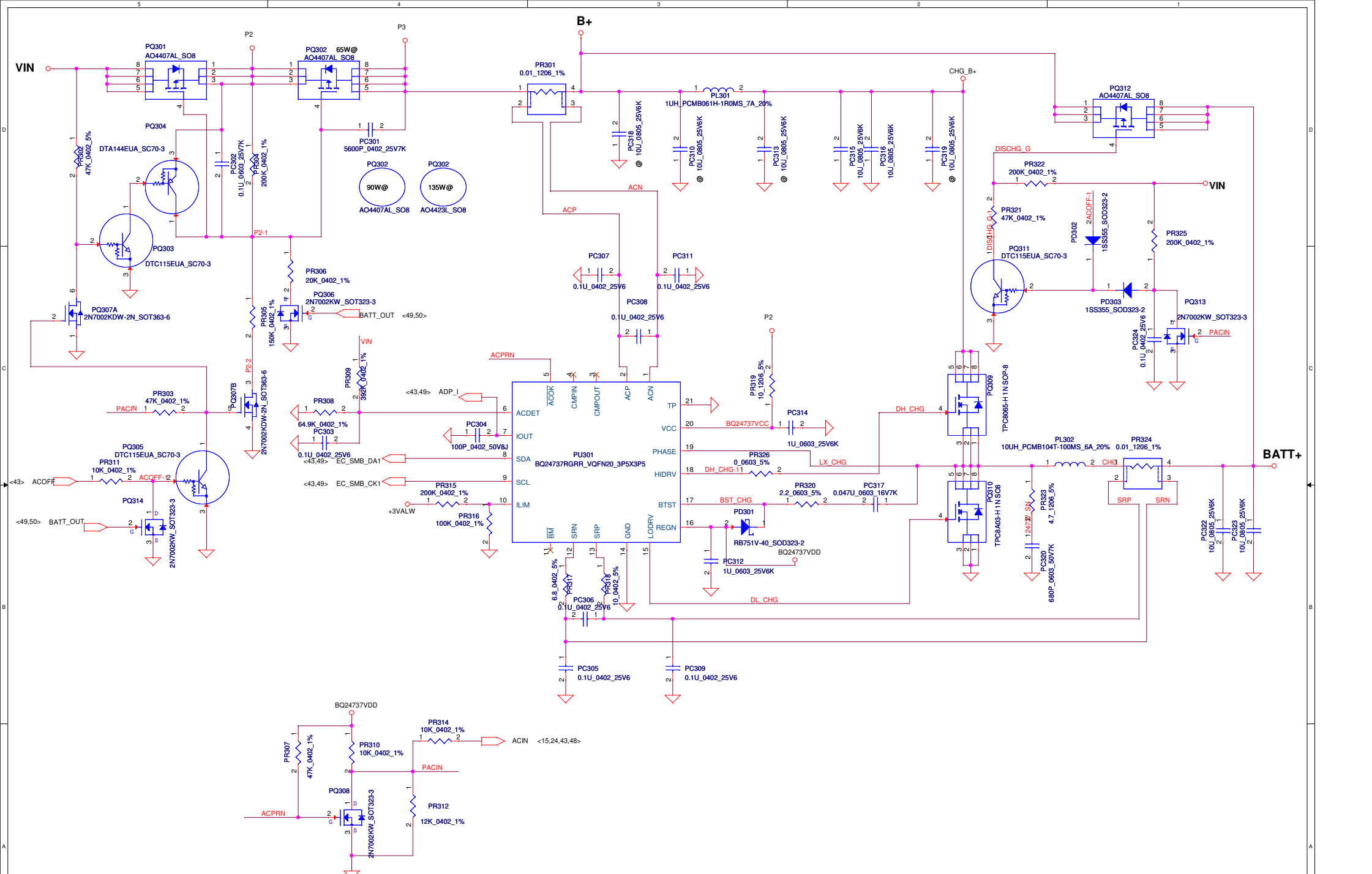
JBATT1 -15" JBATT2 -14"

PH201 under CPU bottom side :  
 CPU thermal protection at 93 +3 degree C  
 Recovery at 56 +3 degree C

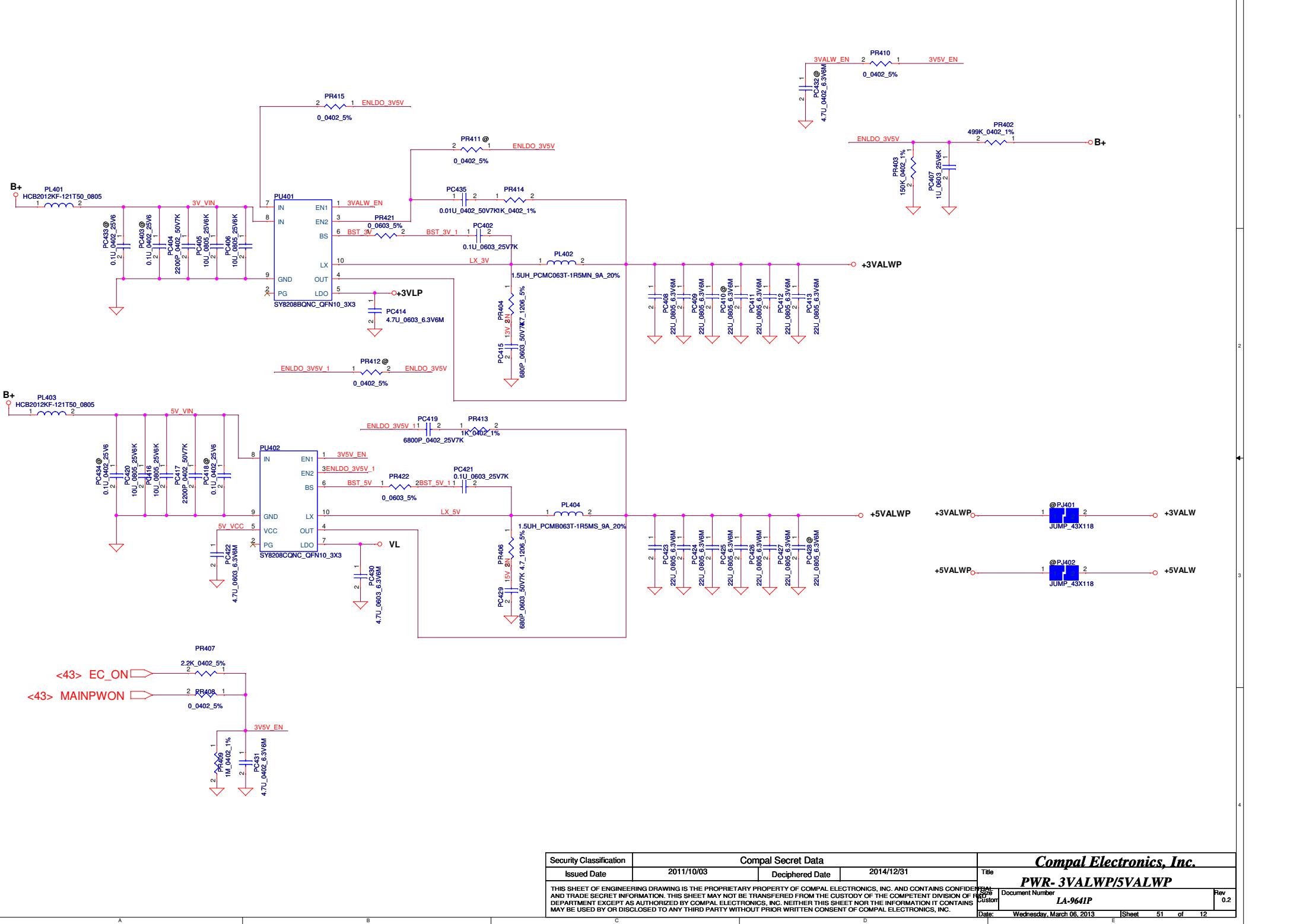


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<b>Compal Electronics, Inc.</b>	
<b>PWR-BATTERY CONN/OTP</b>	
Title PWR-BATTERY CONN/OTP Document Number LA-9641P Date: Wednesday, March 06, 2013	Rev 0.2 Sheet 49 of 59



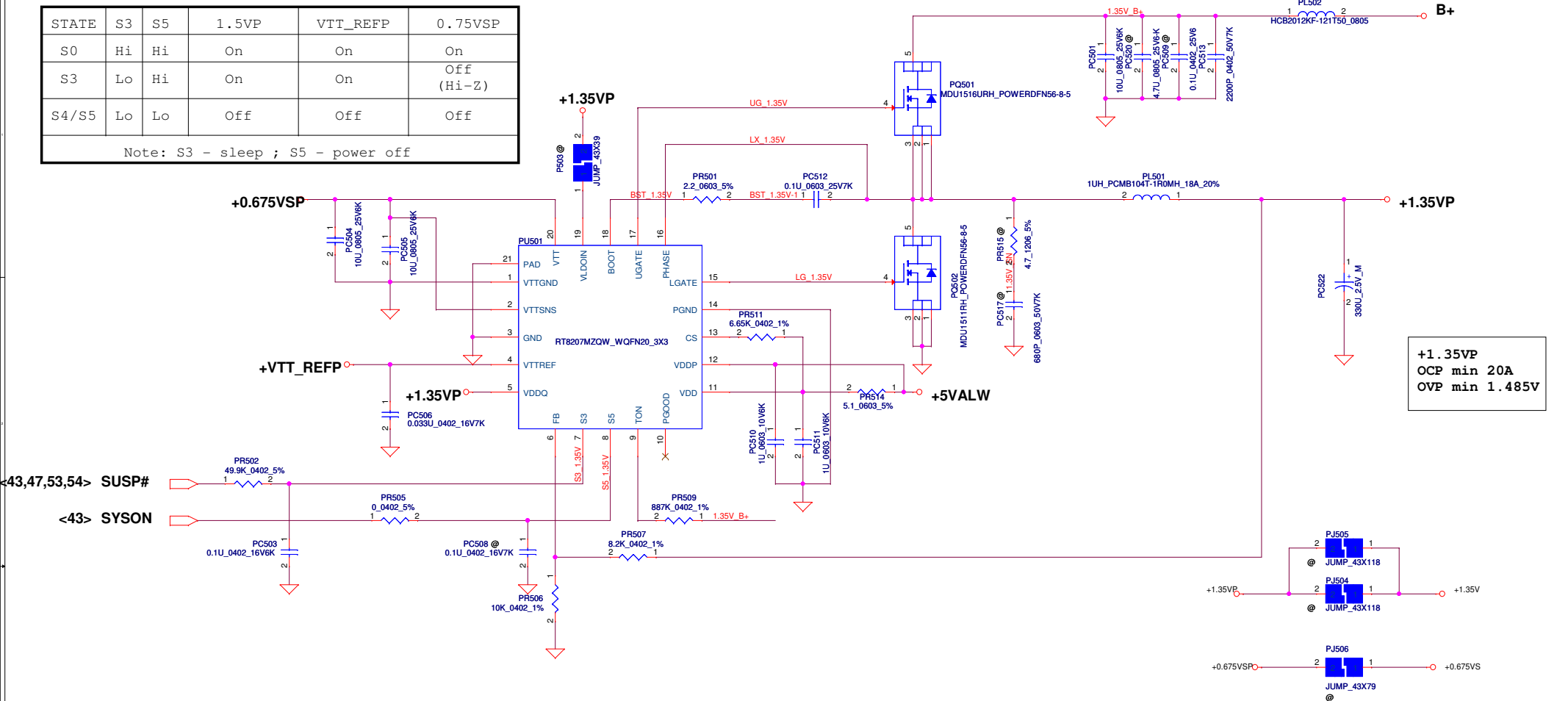
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Issued Date	2010/01/13	Deciphered Date	2012/07/11	Title	
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				Document Number	0.2
				LA-9641P	
Date: Wednesday, March 06, 2013		Sheet 50 of 59			



Security Classification	Compal Secret Data			Title	
Issued Date	2011/10/03	Deciphered Date	2014/12/31	PWR- 3VALWP/5VALWP	
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				LA-964IP	0.2
				Date: Wednesday, March 06, 2013	Sheet 51 of 12

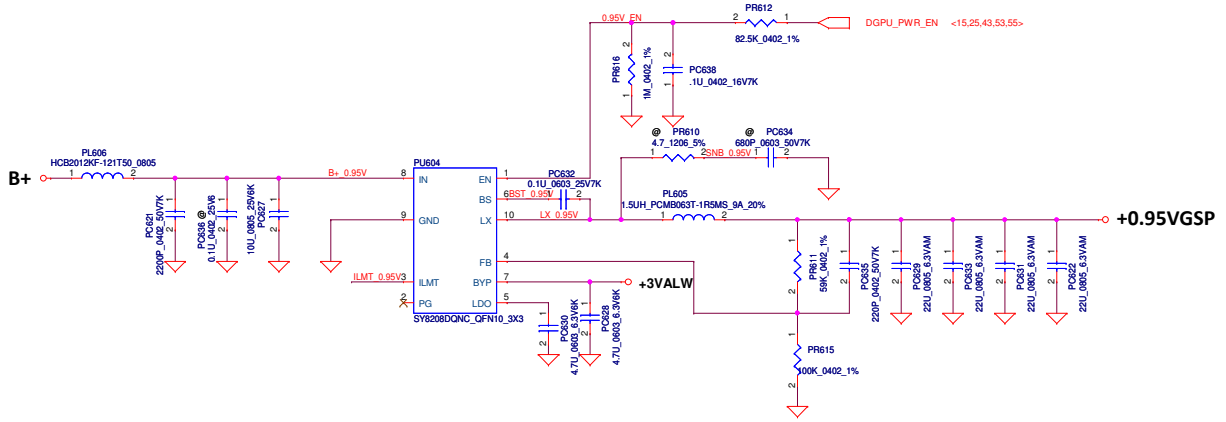
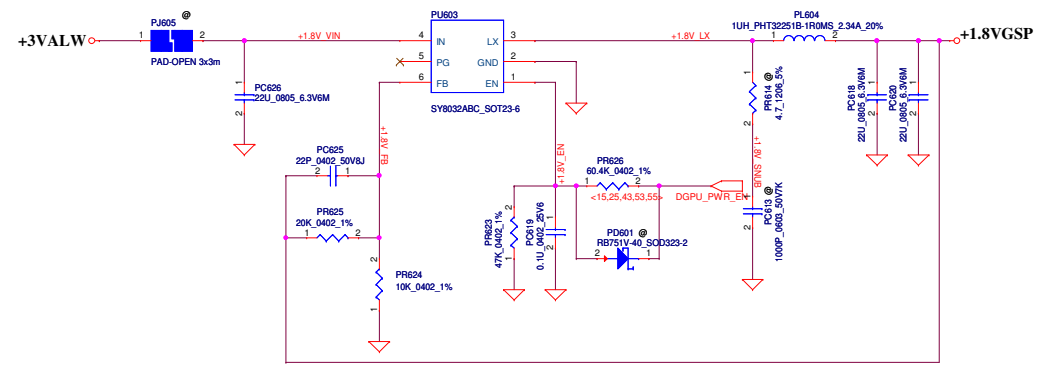
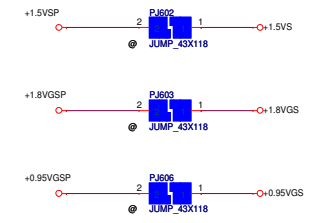
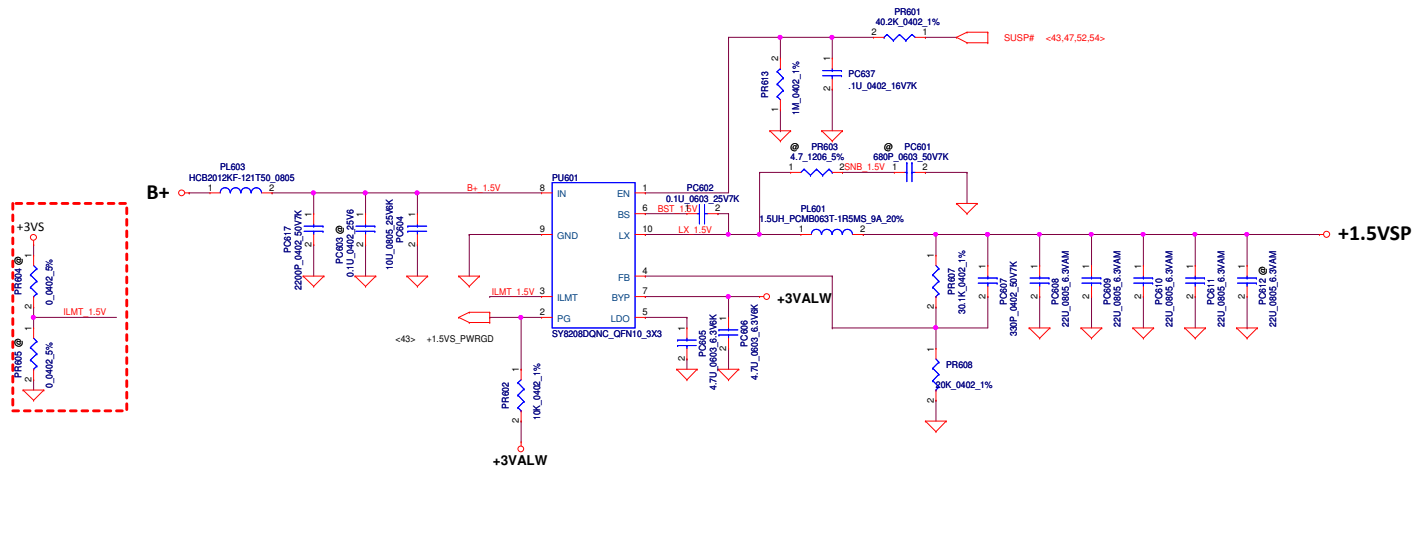
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

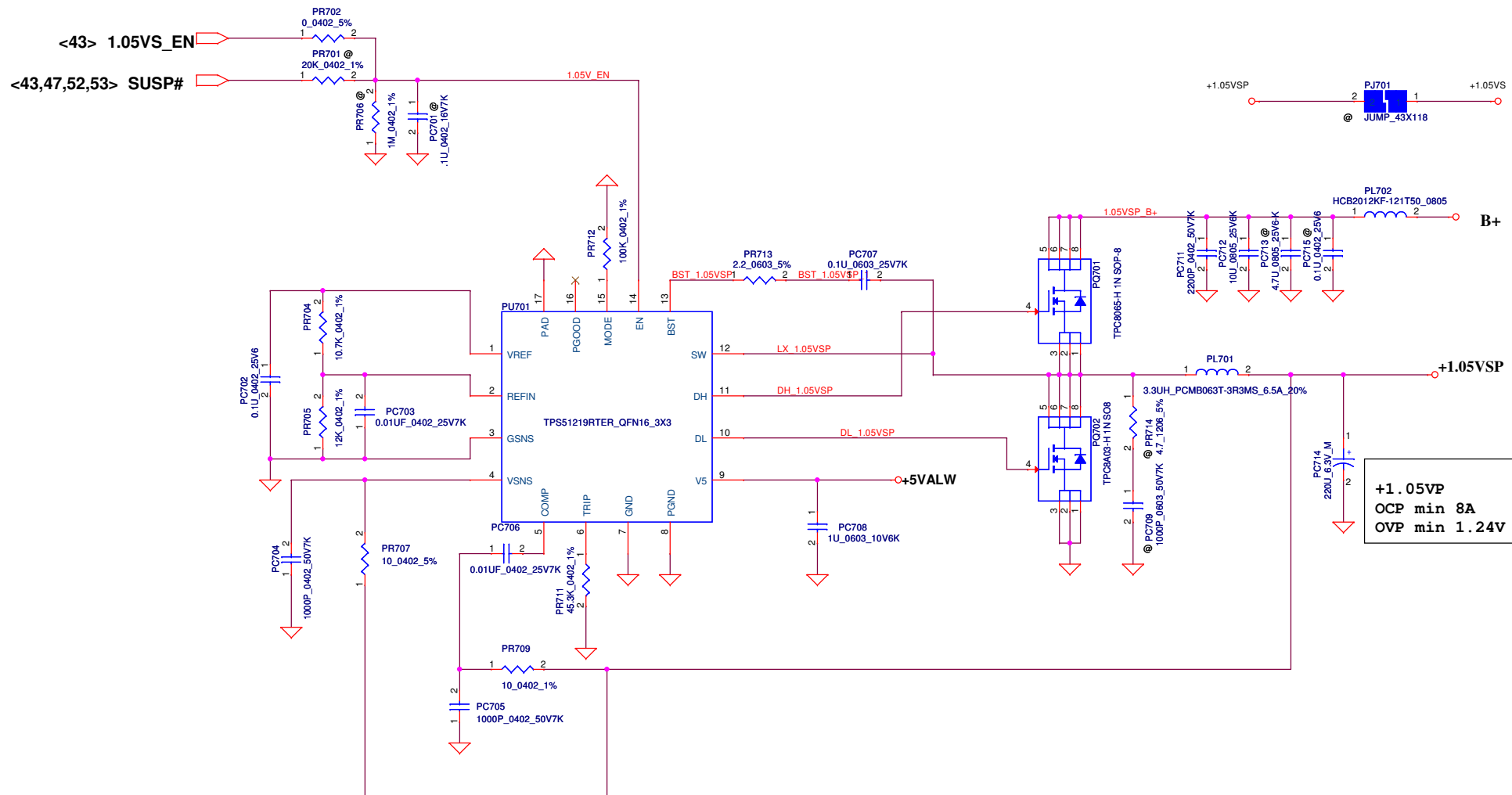


**+1.35VP**  
 OCP min 20A  
 OVP min 1.485V

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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	<b>+1.35V DDR</b>
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				Custom	<b>LA-9641P</b>
				Date:	Wednesday, March 06, 2013
				Sheet	52 of 59
				Rev	0.2

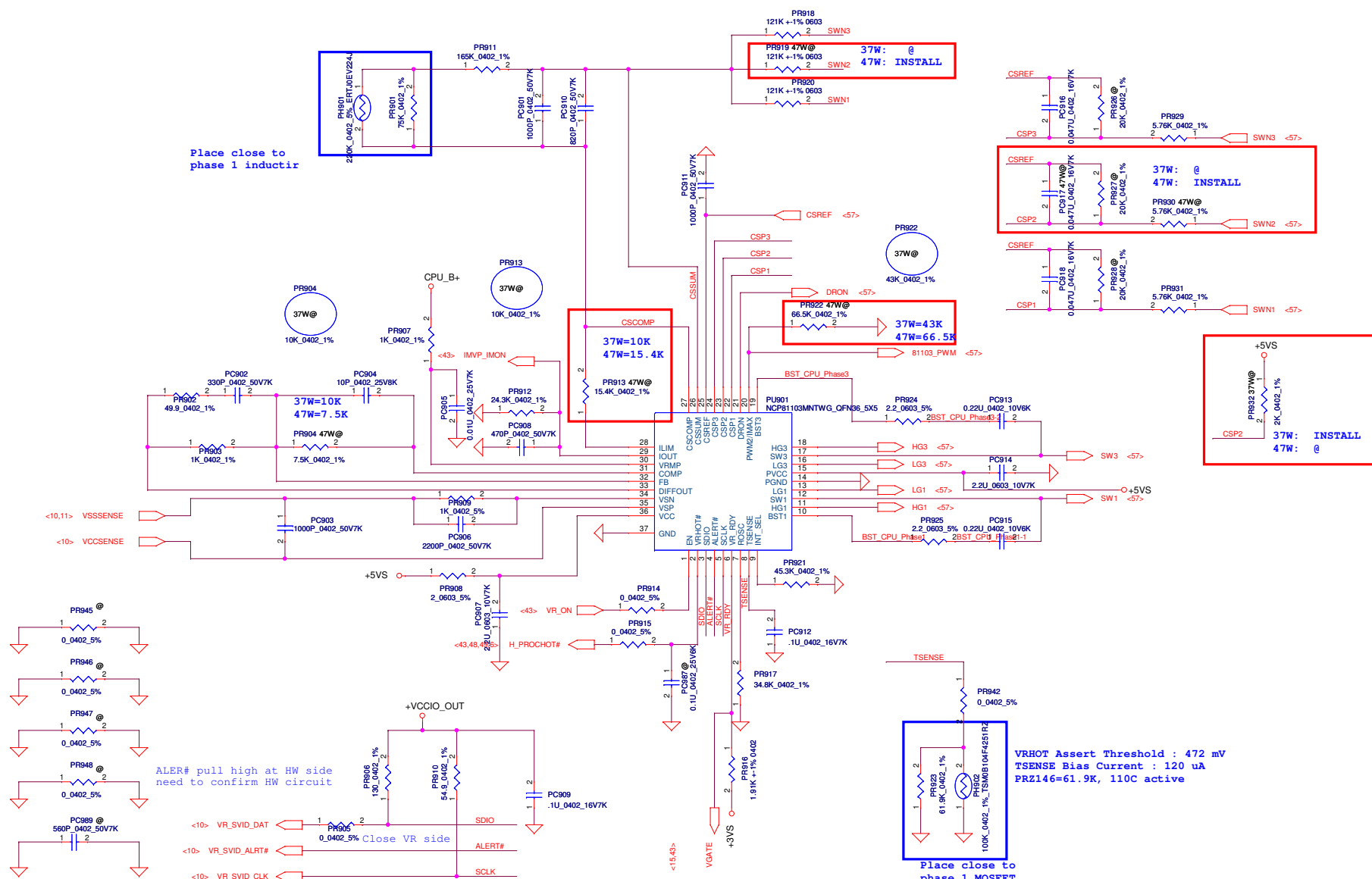


Security Classification	Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>1.5V_VRAM1.8V/0.95V</b> Document Number <b>LA-9641P</b>	Rev 0.2
Issued Date	2010/01/25	Deciphered Date		
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Date:	Wednesday, March 06, 2013	Sheet	54	of	59
				Rev	0.2





Place close to phase 1 inductor

ALER# pull high at HW side need to confirm HW circuit

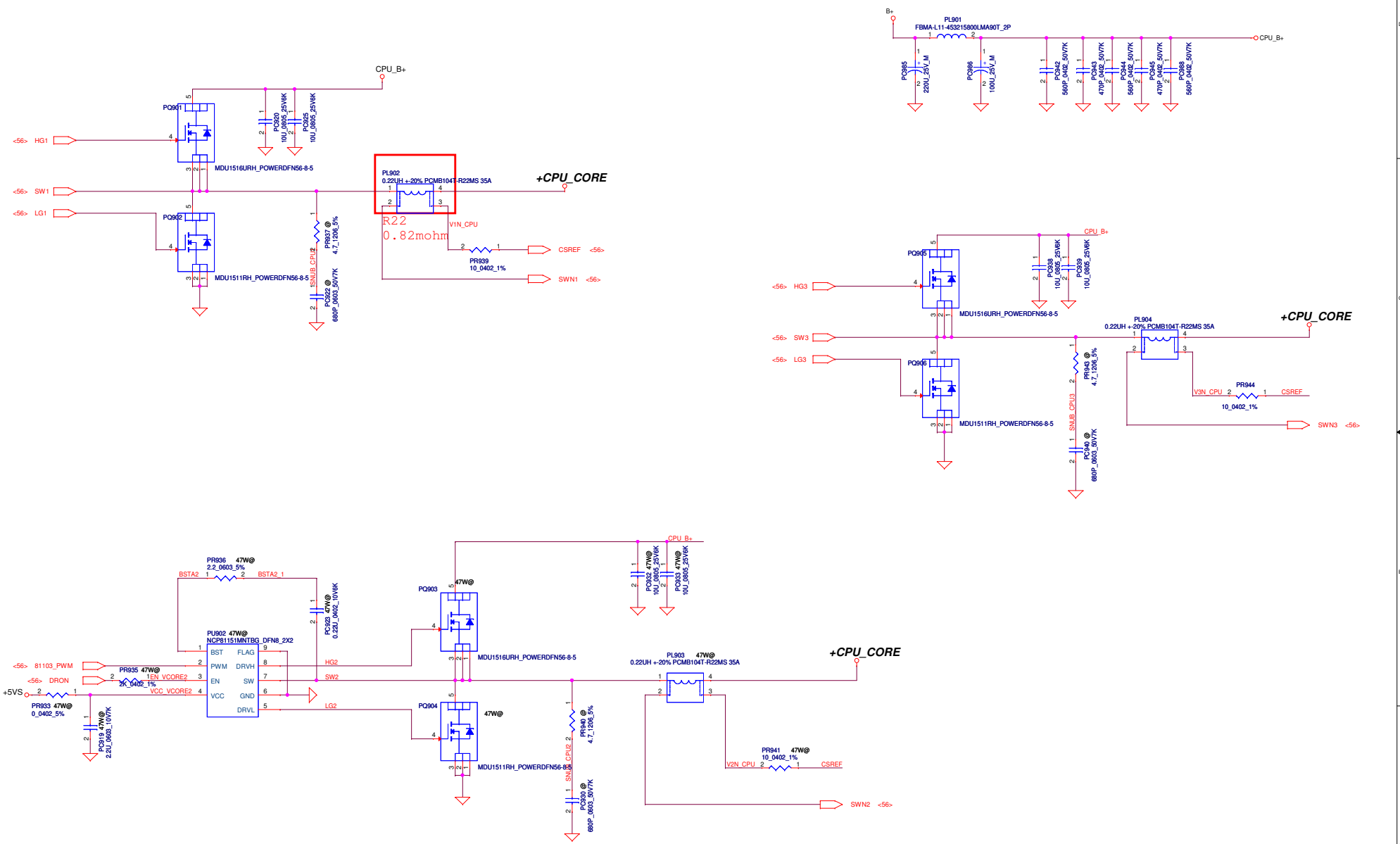
Close VR side

Place close to phase 1 MOSFET

VRHOT Assert Threshold : 472 mV  
TSENSE Bias Current : 120 uA  
PRZ146=61.9K, 110C active

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Issued Date	2011/12/14	Deciphered Date	2012/12/31	Title	CPU CORE1
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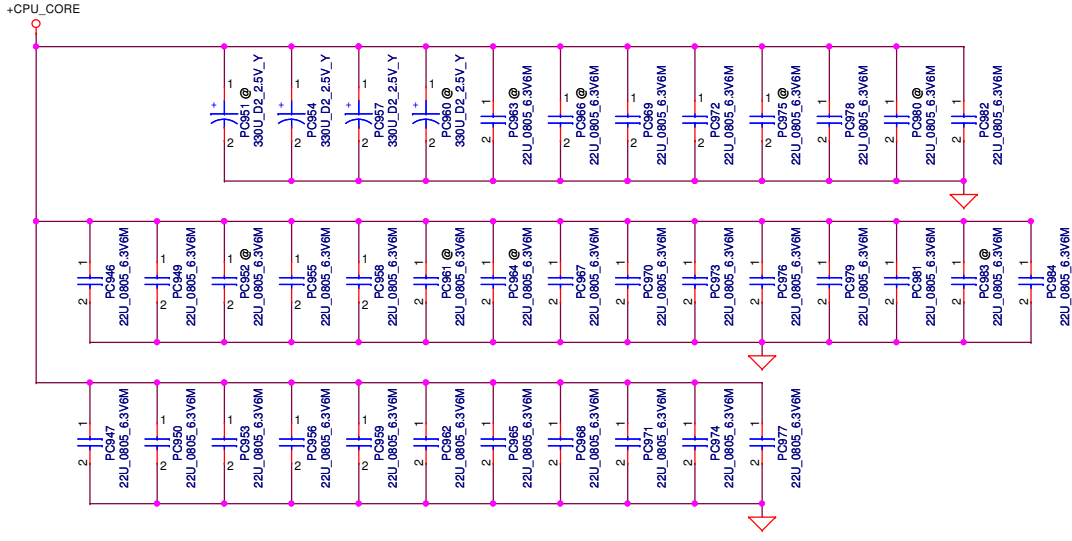


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**+CPU\_CORE**

3 X 330u/9m(47W)  
34 X 22u/0805

2X330u/9m(37W)  
34 X 22u/0805



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adapter ID selection circuit	48 49	Add PR103,PR110,PR111,PQ102,PC108,PC109 Add PR227,PR230,PR229,PR232,PR225,PQ206,PQ208,PQ207	2012.11.28	DVT
2	Delete reserve circuit B+ to VSB	49	Delete PR217,PR218,PR219,PC204,PQ203,PR223,PR224,PC205,PQ204,PC206	2012.11.28	DVT
3	Pop Snubber by EMI request	50	PR323,PC320	2012.11.28	DVT
4	To reduce Ripple	51	PC411,PC426 and change PL404 to 3.3uH	2012.11.28	DVT
5	Reserve enable signal by HW request	51	Add PR410,PC432	2012.11.28	DVT
6	Add boost resistor by EMI request	51	Add PR421,PR422	2012.11.28	DVT
7	Reserve feedback signal for IC application	51	Add PR413,PC419	2012.11.28	DVT
8	To reduce Ripple	53	Change PL601and PL605 to 1.5uH	2012.11.28	DVT
9	Delete reserve circuit	53	Delete PC623,PU602,PC624,PR619,PR620,PR622,PC614,PR627,PL602,PR613,PC612,PC615,PC616	2012.11.28	DVT
10	To reduce Ripple	54	Change PL601and PL701 to 3.3uH	2012.11.28	DVT
11	Reserve enable signal by HW request	54	Add PR702	2012.11.28	DVT
12	Pop Snubber by EMI request	55	PR826,PC811,PR855,PC865	2012.11.28	DVT
13	Add input MLCC by EMI request	57	Add PC943,PC944,PC945,PC988	2012.11.28	DVT
14	Reserve battery detective circuit	49 50	Add PR2003,PR217,PC209,PR212,PC210,PD203,PR208,PQ209,PC211,PU202,PC212,PC213 Add PQ314,PR311(Pop)	2013.03.03	PVT
15	Reserve capacitor by EMI request	50	Add PC318,PC319	2013.03.03	PVT
16	Reduce Component	51	Delete PD401	2013.03.03	PVT
17	Reserve 1.5VSP Power Good by HW request	53	Add PR602	2013.03.03	PVT
18	Reserve bridge resistor by EMI request	55	Add PR948,PC989		

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Item	Reason for change	PG#	Modify List	Date	Phase
1	USE singal 8M ROM for BIOS		Change U8 to SA000039A30 8MB ROM Del U7, R239, R234, R235, R233, R236	12/25	DVT
2	POWER NEW AC Connector		U31.21--> ADP_65 U31.68 change from EC_WL_OFF# to ADP_90 U31.85 change from EC_TS_ON#to ADP_135 U31.66 change from BRDID_1 to ADP_ID	12/25	DVT
3	Change XDP pull down Resistor to R pack		Del R18, R21, R23 / Add RP19	12/25	DVT
4	Update Lenovo BGA footprint		UV1, U4, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	12/25	DVT
5	Move 15" ODD CAP to Small Board		ChangeC605 to R401/ChangeC606 to R402/ ChangeC618 to R403/ChangeC617 to R404	12/25	DVT
6	WLAN Control change to PCH		PCH_GPIO55--> PCH_WL_OFF# PCH_GPIO22-->PCH_BT_ON# PCH_GPIO34-->INTEL_BT_OFF#	12/25	DVT
7	POP TL_ENVDD PULL DOWN		POP R408	12/25	DVT
8	Change HDMI LV from 10P8R to 8R4R X2		Del RP19 ADD RP5, RP6	12/25	DVT
9	Update EC GPIO		NOVO# change form pin 26 to 34 EC_FAN_PWM change form pin 34 to 26 ENBKL change form pin 73 to 76 IMVP_IMON change form pin 76 to 73 DGPU_PWR_EN change form pin 107 to 123	12/25	DVT
10	VGA sequence		+1.5VGS : RV41 --> 240K / CV53 --> 0.1U	12/25	DVT
11	EC Board ID		Change R695 to 15K	12/25	DVT
12	Change ODD connector symbol		JODD1->ALLTO_C18518-11305-L_13P-T	12/25	DVT
13	Update Crystal cap Value by vendor suggestion		C111/ C112 --> 15p CV36/CV37-->8.2p	12/25	DVT
14	Reserve for EMI		ADD R411, R412, C411, C412	12/25	DVT
15	Change PCIE port and clock connection by SW request		LAN-->Port 3 / WLAN--> Port2	12/25	DVT
16	Reserve R301		Reserve +3VLP power rail to EC	12/25	DVT
17	Change EC_RST# power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
18	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
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Item	Reason for change	PG#	Modify List	Date	Phase
1	Add resistor to switch audio power from +3VS to +3VLP and +3VALW.		Add RA1,RA2	02/18	PVT
2	Reconnect HDD +3VS power rail.		Add R-short R552.	02/18	PVT
3	Modify LED current limiting resistor value.		Modify : R623,R765,R303	02/18	PVT
4	Add parallel resistor to separate BIOS and EC.		Add RP2	02/18	PVT
5	Add a Capacitor to connect CHASSIS_GND and GND by EMI request.		Add CL64	02/18	PVT
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