Compal Confidential

DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2012-08-06

LA-9641P

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: Cover Page		
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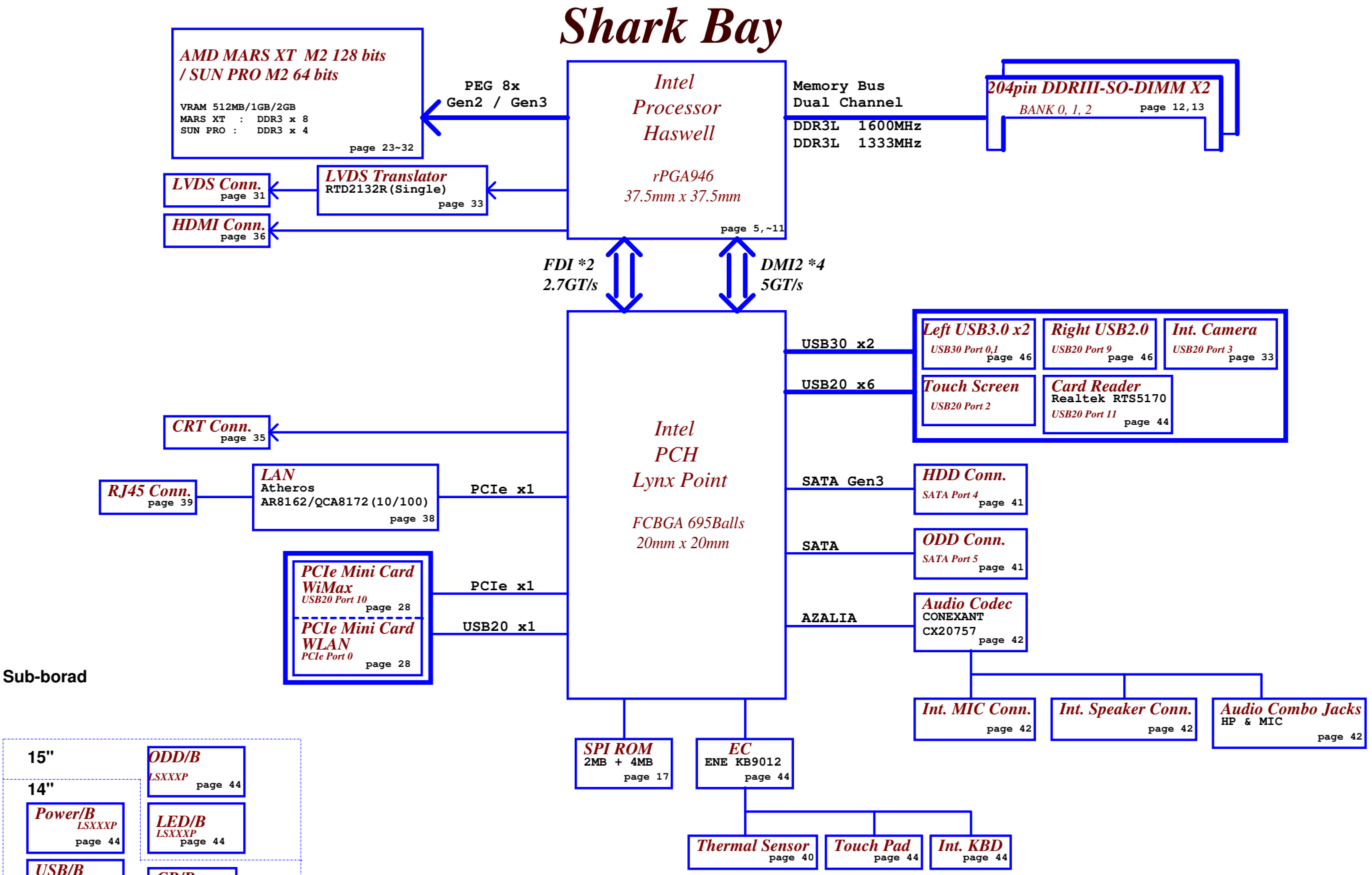
Compal confidential
File Name :

Shark Bay



Sub-borad

15"

14"

ODD/B
LSXXXP
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Power/B
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LED/B
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USB/B
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Title	Block Diagram		
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USb30@
Cameara	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
GREEN CLOCK	GCLK@
DIS GREEN CLOCK	GCLK304@
UMA GREEN CLOCK	GCLK244@
NO GREEN CLOCK	NOGCLK@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

VRAM BOM STRUCTURE Refer P4. VGA NOTE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Device	Address
RTD2132R	1101 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1000_001xb

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	V +3VS

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Compal Electronics, Inc.

Title: Notes List

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Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

Mars XT VRAM STRAP

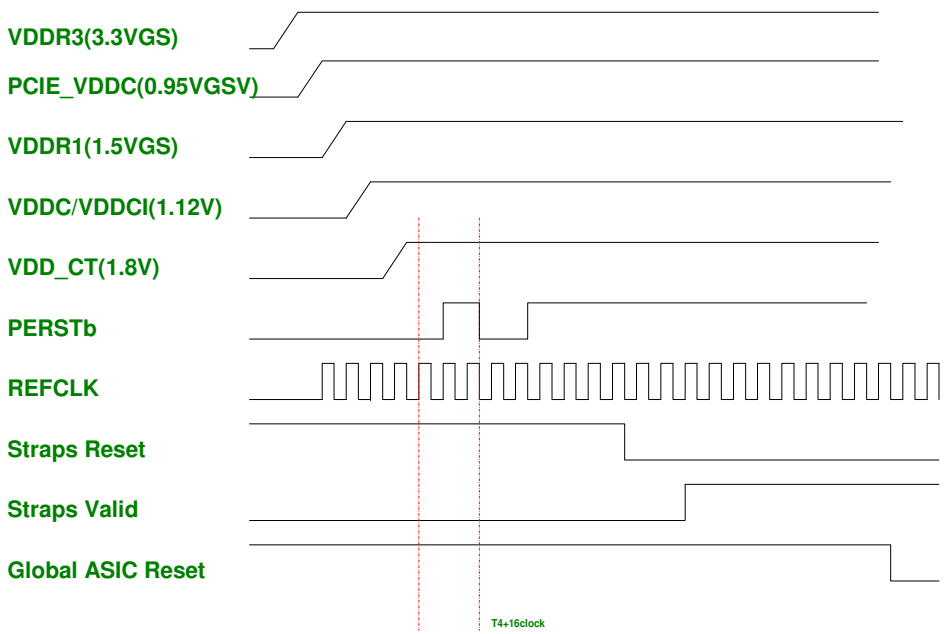
	X76@ Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	X76@ R_pd RV27
ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
2GBytes ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@	Hynix 2048Mbits TBD H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
1GBytes ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC

ZZZ4 Samsung_2G MS2G@ X7646738L01
ZZZ5 Micron_2G MM2G@ X7646738L02
ZZZ6 Hynix_2G MH2G@ TBD
ZZZ7 Samsung_1G MS1G@ X7646738L03
ZZZ8 Hynix_1G MH1G@ X7646738L04

Sun PRO VRAM STRAP

	X76@ Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	X76@ R_pd RV27
ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
2GBytes ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-107G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
1GBytes ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@	Hynix 2048Mbits TBD H5TQ2G63DFR-N0C	1	1	1	4.75K	NC

ZZZ9 Samsung_2G SS2G@ X7646738L05
ZZZ10 Micron_2G SM2G@ X7646738L06
ZZZ11 Hynix_2G SH2G@ TBD
ZZZ12 Samsung_1G SS1G@ X7646738L07
ZZZ13 Micron_1G SM1G@ X7646738L08
ZZZ14 Hynix_1G SH1G@ TBD



ZZZ1 14_DIS@

14" PCB LA9641

DA6000WQ000

ZZZ2 15_DIS@

15" PCB LA9641

DA6000WQ100

ZZZ3 45@

HDMI Logo

RO0000003HM

ZZZ16 14_UMA@

14" PCB LA9641

DA6000WR000

ZZZ15 15_UMA@

15" PCB LA9641

DA6000WR100

+VCOMP_OUT

PEG_RCOMP 2 — 24.9_0402_1% — 1 R1

Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.

Haswell rPGA EDS

JCPU1A

<15> DMI_CRX_PTX_N0 — DMI_CRX_PTX_N0 D21 — DMI_RXN_0
<15> DMI_CRX_PTX_N1 — DMI_CRX_PTX_N1 C21 — DMI_RXN_1
<15> DMI_CRX_PTX_N2 — DMI_CRX_PTX_N2 B21 — DMI_RXN_2
<15> DMI_CRX_PTX_N3 — DMI_CRX_PTX_N3 A21 — DMI_RXN_3

<15> DMI_CRX_PTX_P0 — DMI_CRX_PTX_P0 D20 — DMI_RXP_0
<15> DMI_CRX_PTX_P1 — DMI_CRX_PTX_P1 C20 — DMI_RXP_1
<15> DMI_CRX_PTX_P2 — DMI_CRX_PTX_P2 B20 — DMI_RXP_2
<15> DMI_CRX_PTX_P3 — DMI_CRX_PTX_P3 A20 — DMI_RXP_3

<15> DMI_CTX_PRX_N0 — DMI_CTX_PRX_N0 D18 — DMI_TXN_0
<15> DMI_CTX_PRX_N1 — DMI_CTX_PRX_N1 C17 — DMI_TXN_1
<15> DMI_CTX_PRX_N2 — DMI_CTX_PRX_N2 B17 — DMI_TXN_2
<15> DMI_CTX_PRX_N3 — DMI_CTX_PRX_N3 A17 — DMI_TXN_3

<15> DMI_CTX_PRX_P0 — DMI_CTX_PRX_P0 D17 — DMI_TXP_0
<15> DMI_CTX_PRX_P1 — DMI_CTX_PRX_P1 C18 — DMI_TXP_1
<15> DMI_CTX_PRX_P2 — DMI_CTX_PRX_P2 B18 — DMI_TXP_2
<15> DMI_CTX_PRX_P3 — DMI_CTX_PRX_P3 A18 — DMI_TXP_3

DMI

<15> FDI_CSYNC — H29 — FDI_CSYNC
<15> FDI_INT — J29 — DISP_INT

FDI

Note:
Trace width=4 mils ,Spacing=5mil
Max length= 10000 mils.

PEG

PEG_RCOMP — E23 PEG_RCOMP

PEG_RXN_0 M29
PEG_RXN_1 K28
PEG_RXN_2 M31
PEG_RXN_3 L30
PEG_RXN_4 M33
PEG_RXN_5 L32
PEG_RXN_6 M35
PEG_RXN_7 L34
PEG_RXN_8 E29 PCIE_CRX_GTX_N7
PEG_RXN_9 D28 PCIE_CRX_GTX_N6
PEG_RXN_10 E31 PCIE_CRX_GTX_N5
PEG_RXN_11 D30 PCIE_CRX_GTX_N4
PEG_RXN_12 E35 PCIE_CRX_GTX_N3
PEG_RXN_13 D34 PCIE_CRX_GTX_N2
PEG_RXN_14 E33 PCIE_CRX_GTX_N1
PEG_RXN_15 E32 PCIE_CRX_GTX_N0

PCIE_CRX_GTX_N[0..7] <23>

PEG_RXP_0 L29
PEG_RXP_1 L28
PEG_RXP_2 L31
PEG_RXP_3 K30
PEG_RXP_4 L33
PEG_RXP_5 K32
PEG_RXP_6 L35
PEG_RXP_7 K34
PEG_RXP_8 F29 PCIE_CRX_GTX_P7
PEG_RXP_9 E28 PCIE_CRX_GTX_P6
PEG_RXP_10 F31 PCIE_CRX_GTX_P5
PEG_RXP_11 E30 PCIE_CRX_GTX_P4
PEG_RXP_12 F35 PCIE_CRX_GTX_P3
PEG_RXP_13 E34 PCIE_CRX_GTX_P2
PEG_RXP_14 F33 PCIE_CRX_GTX_P1
PEG_RXP_15 D32 PCIE_CRX_GTX_P0

PCIE_CRX_GTX_P[0..7] <23>

PEG_TXN_0 H35
PEG_TXN_1 H34
PEG_TXN_2 J33
PEG_TXN_3 H32
PEG_TXN_4 J31
PEG_TXN_5 G30
PEG_TXN_6 G33
PEG_TXN_7 B32
PEG_TXN_8 B31 PCIE_CTX_GRX_C_N7 C9 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N7
PEG_TXN_9 A30 PCIE_CTX_GRX_C_N6 C10 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N6
PEG_TXN_10 B29 PCIE_CTX_GRX_C_N5 C11 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N5
PEG_TXN_11 A28 PCIE_CTX_GRX_C_N4 C12 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N4
PEG_TXN_12 B27 PCIE_CTX_GRX_C_N3 C13 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N3
PEG_TXN_13 A26 PCIE_CTX_GRX_C_N2 C14 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N2
PEG_TXN_14 B25 PCIE_CTX_GRX_C_N1 C15 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N1
PEG_TXN_15 A24 PCIE_CTX_GRX_C_N0 C16 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N0

PCIE_CTX_GRX_N[0..7] <23>

PEG_TXP_0 J35
PEG_TXP_1 G34
PEG_TXP_2 H33
PEG_TXP_3 G32
PEG_TXP_4 J31
PEG_TXP_5 D30
PEG_TXP_6 B33
PEG_TXP_7 A32
PEG_TXP_8 C31 PCIE_CTX_GRX_C_P7 C25 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P7
PEG_TXP_9 B30 PCIE_CTX_GRX_C_P6 C26 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P6
PEG_TXP_10 C29 PCIE_CTX_GRX_C_P5 C27 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P5
PEG_TXP_11 B28 PCIE_CTX_GRX_C_P4 C28 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P4
PEG_TXP_12 C27 PCIE_CTX_GRX_C_P3 C29 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P3
PEG_TXP_13 B26 PCIE_CTX_GRX_C_P2 C30 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P2
PEG_TXP_14 C25 PCIE_CTX_GRX_C_P1 C31 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P1
PEG_TXP_15 B24 PCIE_CTX_GRX_C_P0 C32 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P0

PCIE_CTX_GRX_P[0..7] <23>

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ME@

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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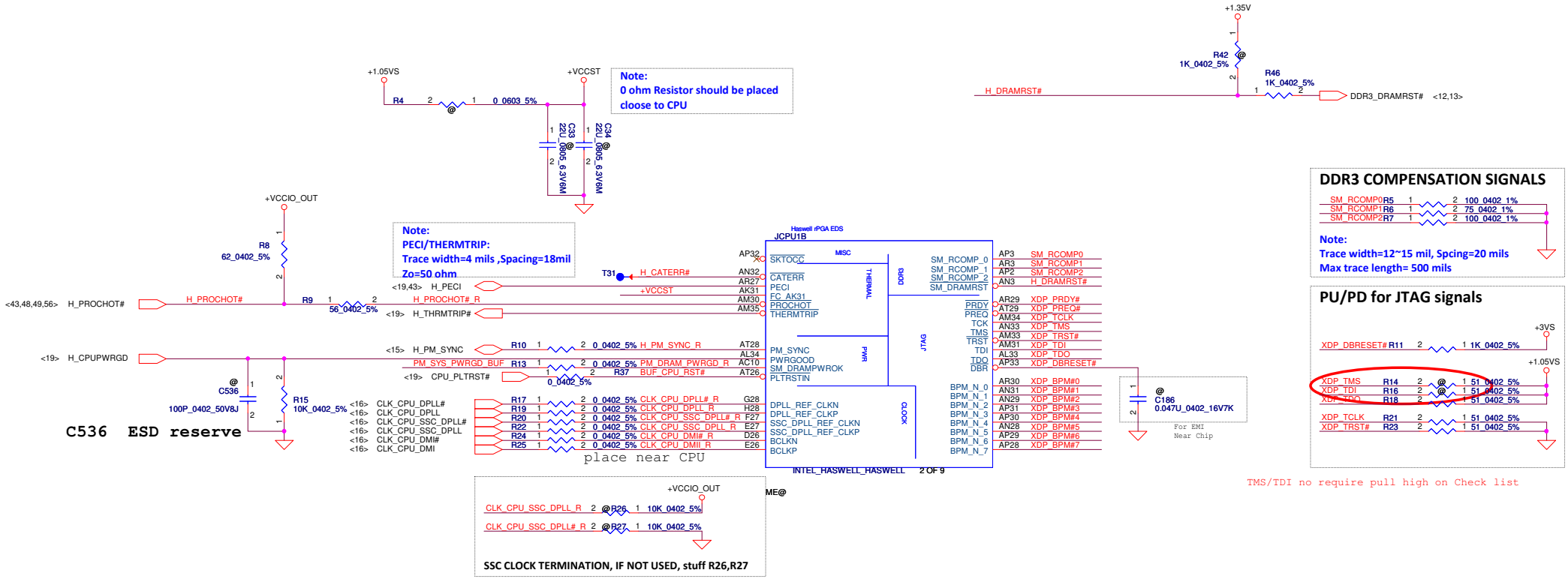
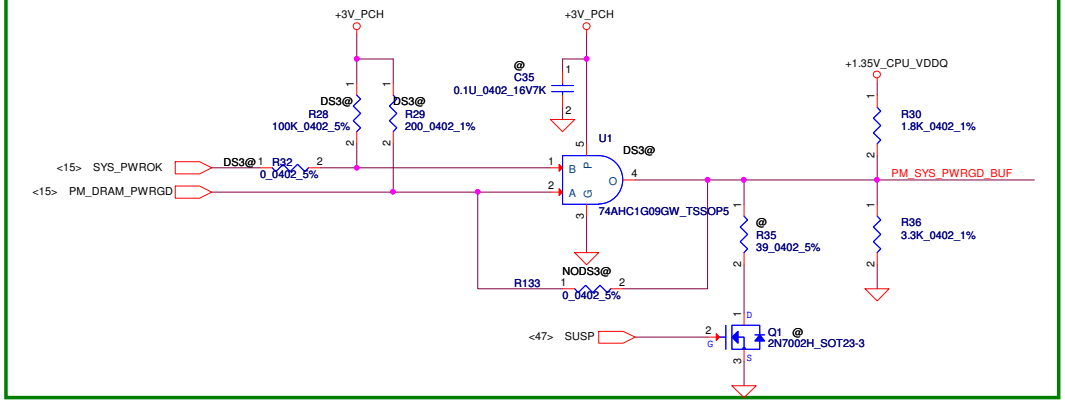


SM_DRAMPWROK with DDR Power Gating Topology



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Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: LA-9641P | Rev: 0.1

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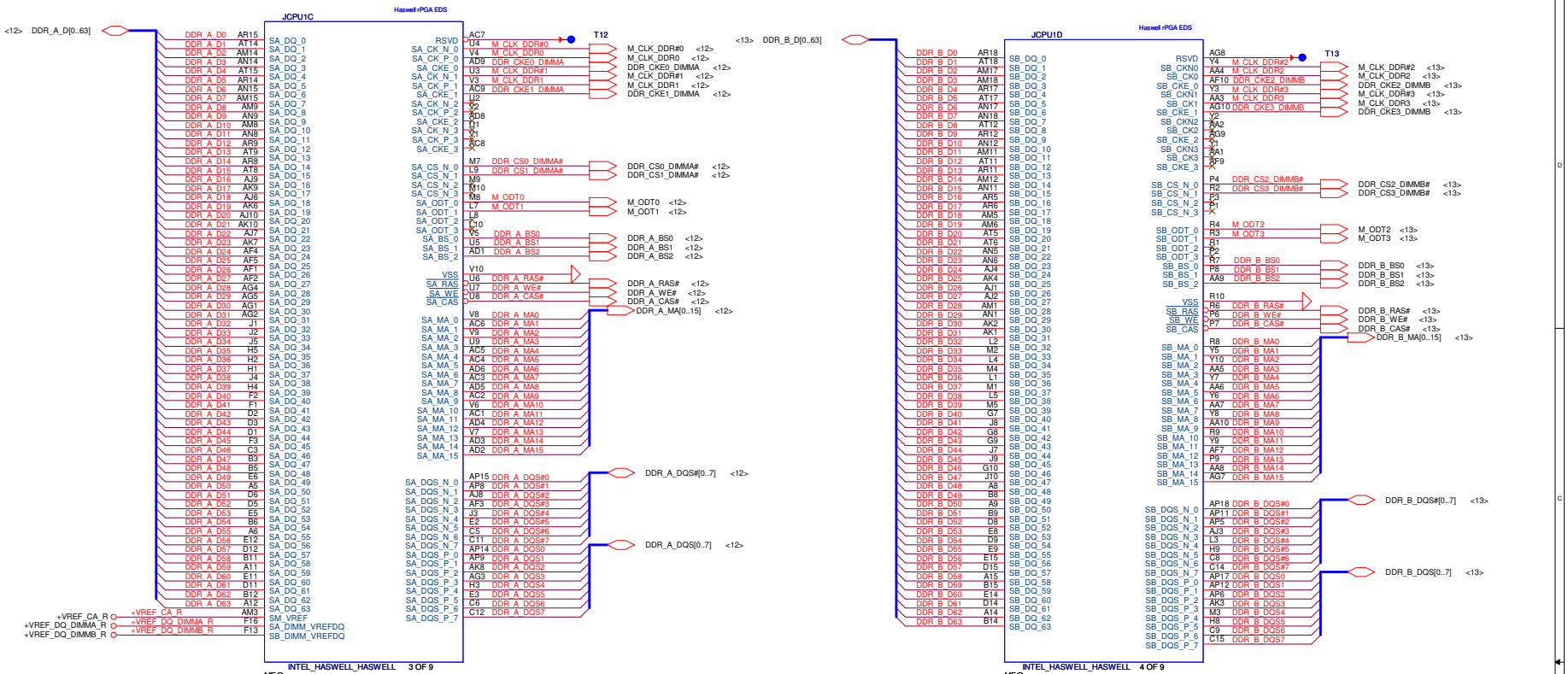

CPI DRIVER VREF PATH IS DEFAULT

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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

<36> HDMI_TX2-_CK — HDMI@ C48 1 — 2 0.1U_0402_16V7K — TMDS_B_DATA2#_PCH — T28
<36> HDMI_TX2+_CK — HDMI@ C41 1 — 2 0.1U_0402_16V7K — TMDS_B_DATA2_PCH — U28
<36> HDMI_TX1-_CK — HDMI@ C42 1 — 2 0.1U_0402_16V7K — TMDS_B_DATA1#_PCH — T30
<36> HDMI_TX1+_CK — HDMI@ C43 1 — 2 0.1U_0402_16V7K — TMDS_B_DATA1_PCH — U30
<36> HDMI_TX0-_CK — HDMI@ C44 1 — 2 0.1U_0402_16V7K — TMDS_B_DATA0#_PCH — U29
<36> HDMI_TX0+_CK — HDMI@ C45 1 — 2 0.1U_0402_16V7K — TMDS_B_DATA0_PCH — V29
<36> HDMI_CLK-_CK — HDMI@ C46 1 — 2 0.1U_0402_16V7K — TMDS_B_CLK#_PCH — V31
<36> HDMI_CLK+_CK — HDMI@ C47 1 — 2 0.1U_0402_16V7K — TMDS_B_CLK_PCH — V31

Place on connector side

Haswell rPGA EDS — JCPU1H

DDIB_TXBN_0 T34
DDIB_TXBP_0 U34
DDIB_TXBN_1 U35
DDIB_TXBP_1 V35
DDIB_TXBN_2 U32
DDIB_TXBP_2 T32
DDIB_TXBN_3 U33
DDIB_TXBP_3 V33

DDIC_TXCN_0 P29
DDIC_TXCP_0 R29
DDIC_TXCN_1 N28
DDIC_TXCP_1 P28
DDIC_TXCN_2 P31
DDIC_TXCP_2 R31
DDIC_TXCN_3 N30
DDIC_TXCP_3 P30

DDI

eDP:
EDP_AUXN M27 — EDP_CPU_AUX# — EDP_CPU_AUX# <33>
EDP_AUXP N27 — EDP_CPU_AUX — EDP_CPU_AUX <33>
EDP_HPD P27 — EDP_HPD#
EDP_RCOMP E24 — EDP_COMP
EDP_DISP_UT IL R27 — T14

EDP_TXN_0 P35 — EDP_CPU_LANE_N0 — EDP_CPU_LANE_N0 <33>
EDP_TXP_0 R35 — EDP_CPU_LANE_P0 — EDP_CPU_LANE_P0 <33>
EDP_TXN_1 N34 — EDP_CPU_LANE_N1
EDP_TXP_1 P34 — EDP_CPU_LANE_P1

FDI_TXN_0 P33 — FDI_CTX_PRX_N0 — FDI_CTX_PRX_N0 <15>
FDI_TXP_0 R33 — FDI_CTX_PRX_P0 — FDI_CTX_PRX_P0 <15>
FDI_TXN_1 N32 — FDI_CTX_PRX_N1 — FDI_CTX_PRX_N1 <15>
FDI_TXP_1 P32 — FDI_CTX_PRX_P1 — FDI_CTX_PRX_P1 <15>

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ME@

COMPENSATION PU FOR eDP

+VCOMP_OUT
EDP_COMP — 2 — 24.9_0402_1% — 1 — R60

Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP

+VCCIO_OUT
10K_0402_5% RC1 (2 / 1)
EDP_HPD#
<33> TL_HPD — R458 (1) — 1K_0402_5% (2)
100K_0402_5% R861 (@) (1 / 2)
Q6 DTC124EKAT146_SC59-3 (IN / GND / OUT)

HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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Title: PROCESSOR(2/7) PM,XDP,CLK
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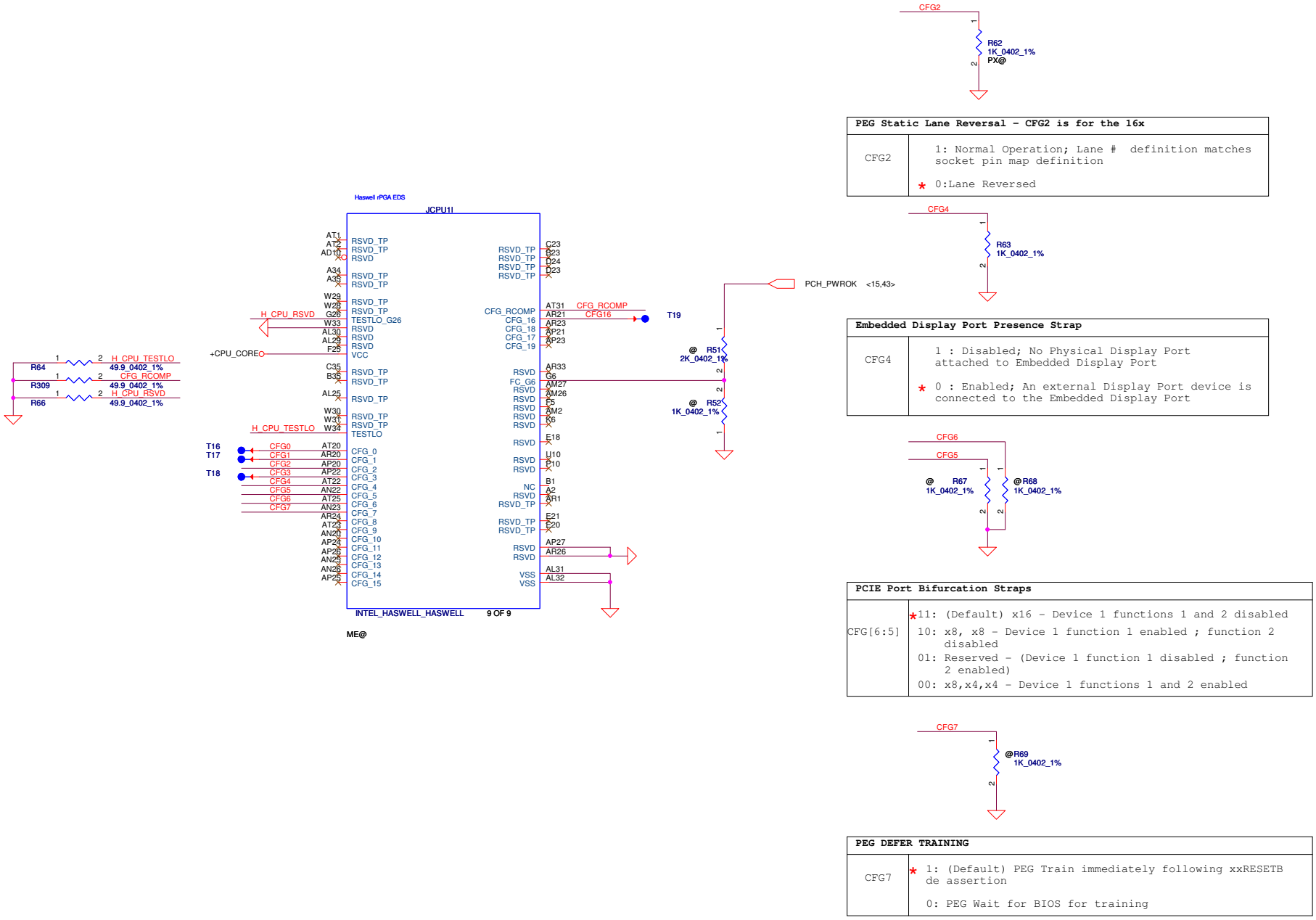
CFG Straps for Processor



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

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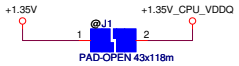
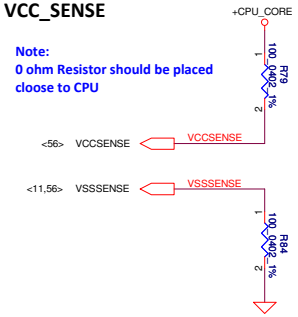
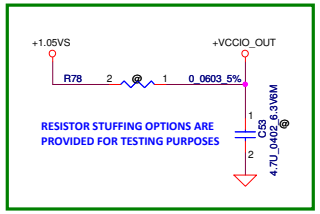
+1.35V_CPU_VDDQ Source

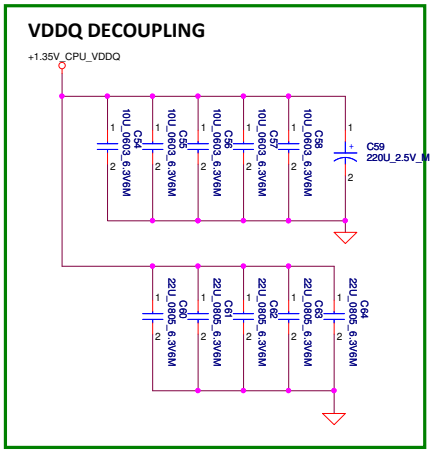


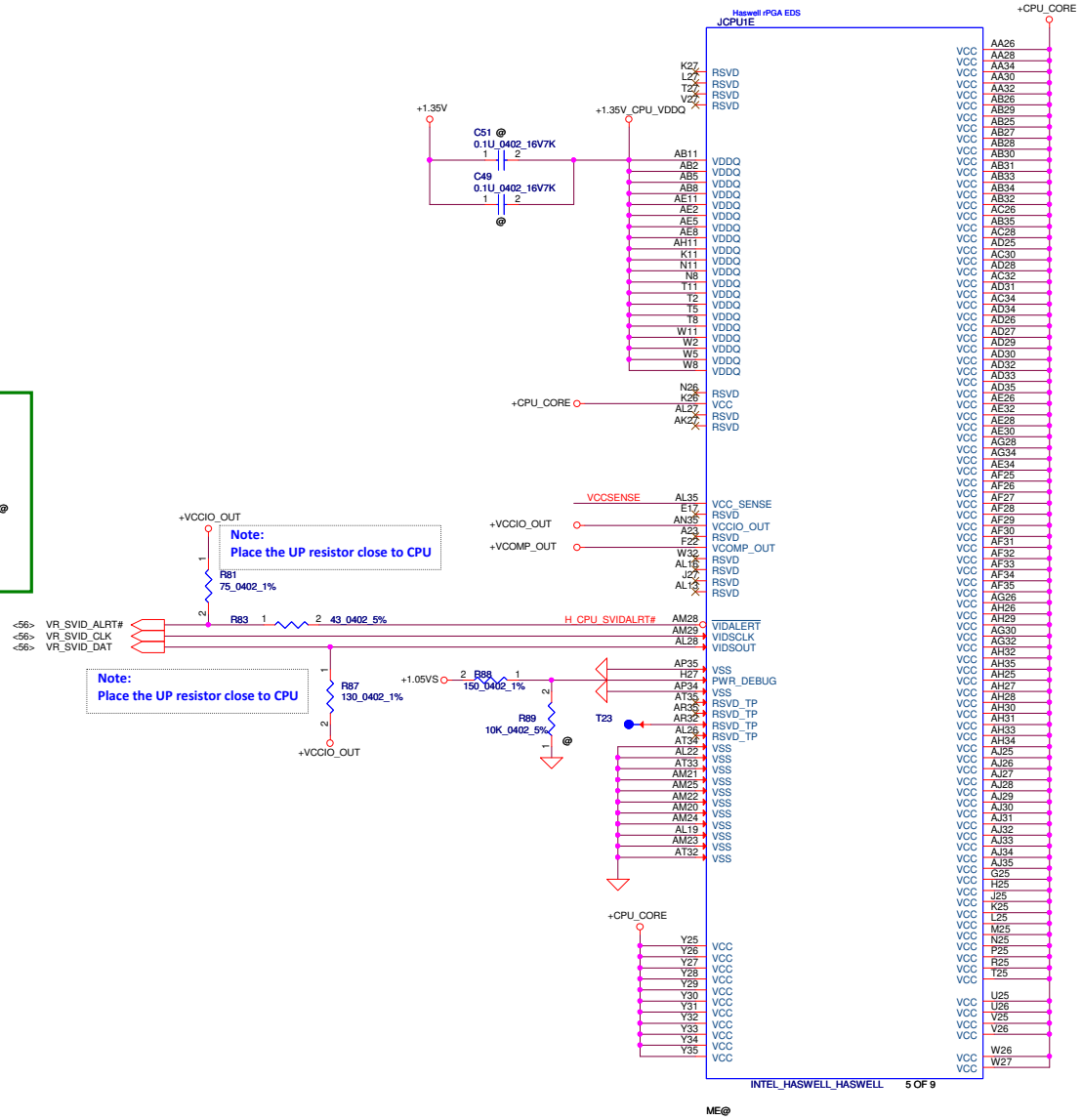
VCC_SENSE





VDDQ DECOUPLING



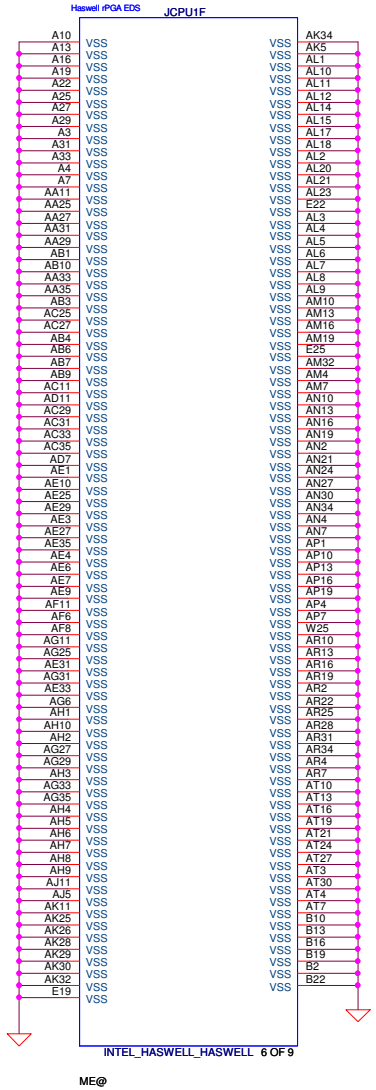


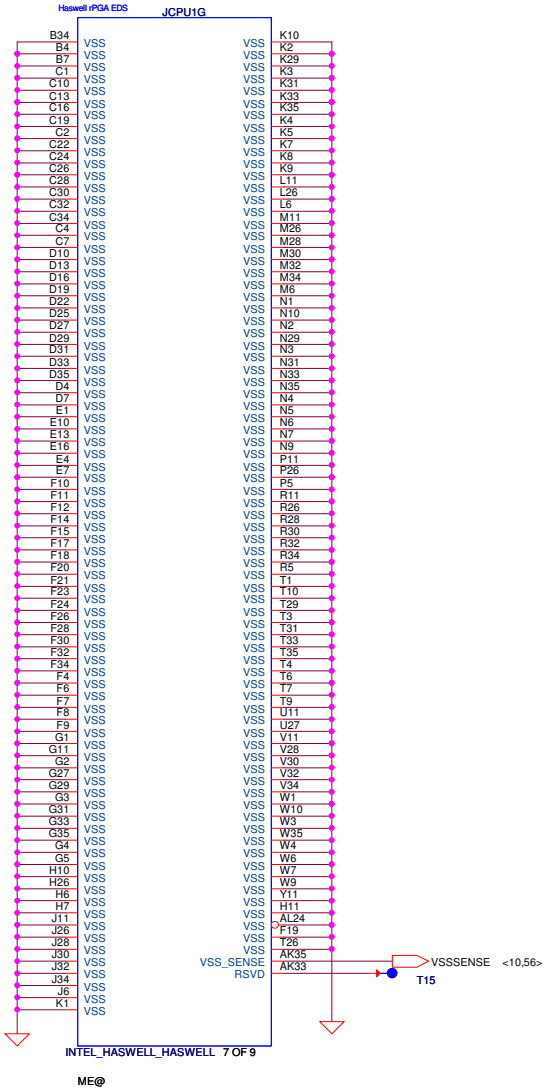
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: **PROCESSOR(6/7) PWR**

Size: Custom | Document Number: **LA-9641P** | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 10 of 60





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

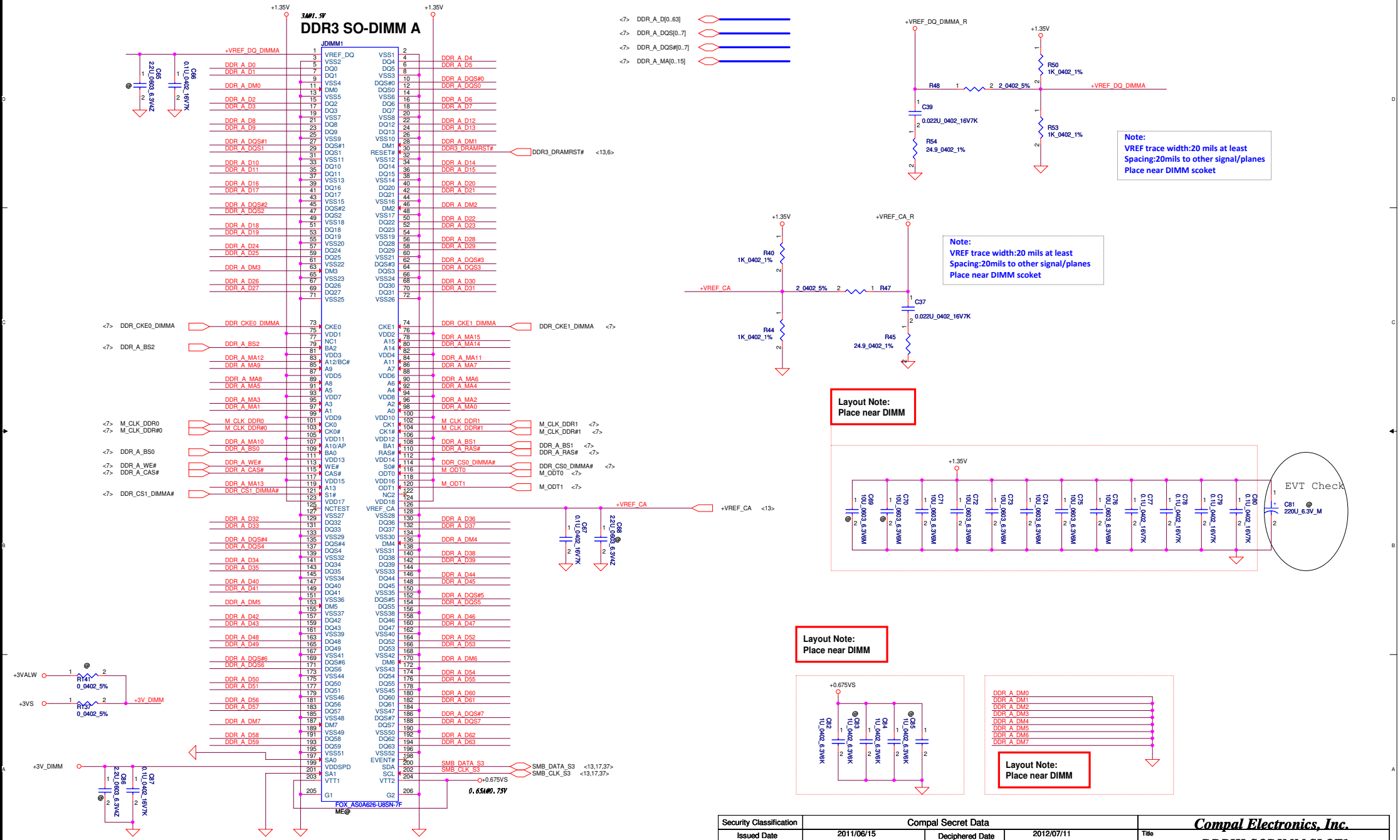
Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 11 of 60

DDR3 SO-DIMM A



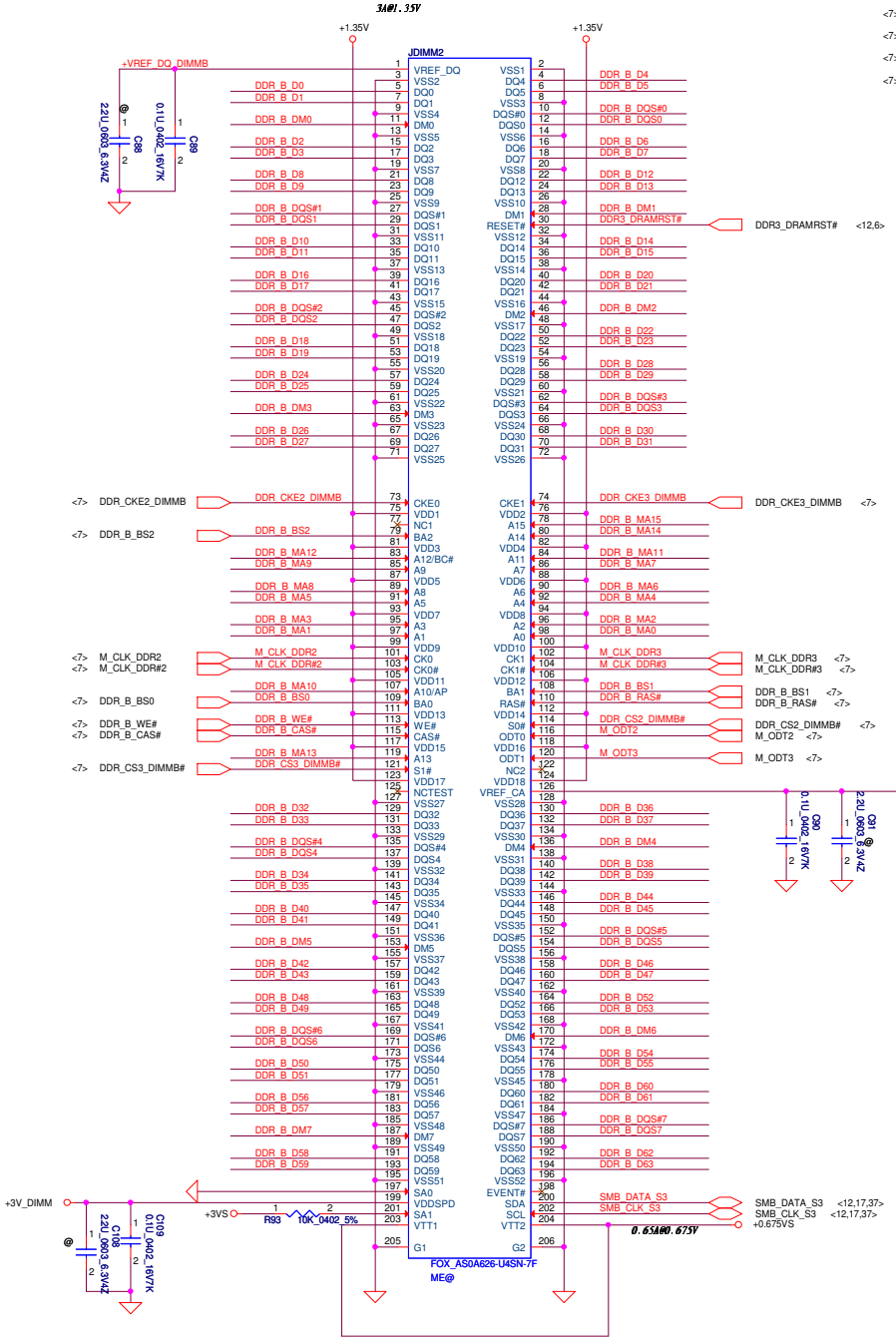
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

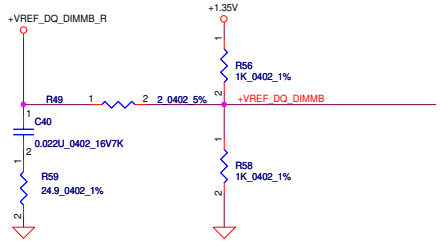
Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LA-9641P	0.1

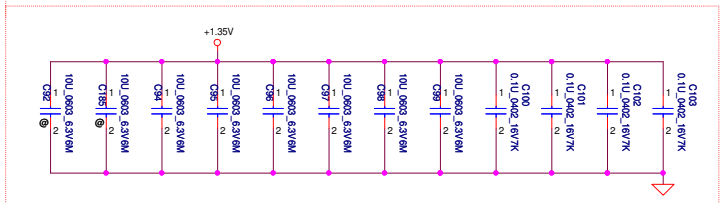
Date: Thursday, October 11, 2012 | Sheet 12 of 60



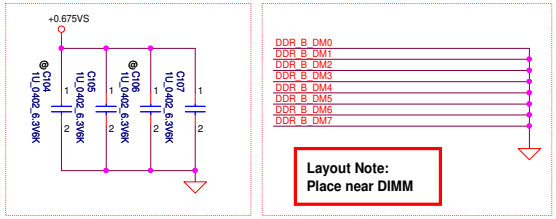
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes



Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



Layout Note:
Place near DIMM

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 13 of 60

W=20mils +RTCVCC — R94 1K_0402_5% — W=20mils +RTCBATT
C110 1U_0603_10V6K — CLRP1 SHORT PADS

+RTCVCC
R96 1M_0402_5% SM_INTRUDER#
R97 330K_0402_5% PCH_INTVRMEN

INTVRMEN
(INTEGRATED SUS 1.05V VR)
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3V_PCH R100 1K_0402_5% HDA_SYNC
+3VS R101 1K_0402_5% PCH_GPIO33

+3VS R102 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)
* LOW= Disable (Default) / weak internal pull low

+3V_PCH R105 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]

RP12 33_0804_8P4R_5%
<42> HDA_BITCLK_AUDIO — HDA_BIT_CLK
<42> HDA_SYNC_AUDIO — HDA_SYNC_R
<42> HDA_RST_AUDIO# — HDA_RST#
<42> HDA_SDOUT_AUDIO — HDA_SDOUT

+3V_PCH R119 200_0402_1% PCH_JTAG_TDO — R122 100_0402_1%
+3V_PCH R311 200_0402_1% PCH_JTAG_TMS — R123 100_0402_1%
+3V_PCH R121 200_0402_1% PCH_JTAG_TDI — R124 100_0402_1%

Note:
PCH_RTCX1/PCHRTCX2
Trace length <1000 mils

PCH_RTCX1 — R196 0_0402_5% — GCLK_32K — GCLK_32K <45>
PCH_RTCX2 — R95 10M_0402_5% NOGCLK@ — Y1 32.768KHZ_12.5PF_CM31532768DZFT NOGCLK@
C111 18P_0402_50V8J NOGCLK@ — C112 18P_0402_50V8J NOGCLK@

+RTCVCC
C113 1U_0603_10V6K — CLRP2 SHORT PADS
CLRP2: OPEN — SAVE ME RTC REGISTER; SHORT — CLEAR ME RTC REGISTER
R98 20K_0402_5% PCH_SRTCRST#
R99 20K_0402_5% PCH_RTCRST#
C115 1U_0603_10V6K — CLRP3 SHORT PADS
CLRP3: OPEN — SAVE CMOS; SHORT — CLEAR CMOS

ME FALSH
<43> HDA_SDOUT — R104 1K_0402_5% PCH_GPIO33 — R106 10K_0402_5% PCH_GPIO13 — +3V_PCH

+5VS — Q10 LBSS138LT1G_SOT-23-3 — HDA_SYNC
R115 1M_0402_5% — R118 0_0402_5%

DG remove Q10 on Version 1.5

R110 51_0402_5% — PCH_JTAG_TCK, PCH_JTAG_TMS, PCH_JTAG_TDI, PCH_JTAG_TDO

U4A LPT_PCH_M_EDS

PCH_RTCX1	B5	RTCX1	RTC
PCH_RTCX2	B4	RTCX2	
PCH_SRTCRST#	B9	SRTCRST#	
SM_INTRUDER#	A8	INTRUDER#	
PCH_INTVRMEN	G10	INTVRMEN	
	D9	RTCRST#	
HDA_BIT_CLK	B25	HDA_BCLK	AZALIA
HDA_SYNC	A22	HDA_SYNC	
HDA_SPKR	AL10	SPKR	
HDA_RST#	C24	HDA_RST#	
HDA_SDIN0	L22	HDA_SDI0	
	K22	HDA_SDI1	
	G22	HDA_SDI2	
	F22	HDA_SDI3	
HDA_SDOUT	A24	HDA_SDO	
PCH_GPIO33	B17	DOCKEN#/GPIO33	
PCH_GPIO13	C22	HDA_DOCK_RST#/GPIO13	
PCH_JTAG_TCK	AB3	JTAG_TCK	JTAG
PCH_JTAG_TMS	AD1	JTAG_TMS	
PCH_JTAG_TDI	AE2	JTAG_TDI	
PCH_JTAG_TDO	AD3	JTAG_TDO	
	F8	TP25	
	C26	TP22	
	AB6	TP20	

1 OF 11
DH82LPMS-QC4C-A1_FCBGA695-D

SATA

SATA_RXN_0 / SATA_RXP_0	BC8 / BE8	
SATA_TXN_0 / SATA_TXP_0	AW8 / AY8	
SATA_RXN_1 / SATA_RXP_1	BC10 / BE10	
SATA_TXN_1 / SATA_TXP_1	AV10 / AW10	
SATA_RXN_2 / SATA_RXP_2	BB9 / BD9	
SATA_TXN_2 / SATA_TXP_2	AY13 / AW13	
SATA_RXN_3 / SATA_RXP_3	BC12 / BE12	
SATA_TXN_3 / SATA_TXP_3	AR13 / AT13	
SATA_RXN4/PERN1 / SATA_RXP4/PERP1	BD13 / BB13	SATA_DTX_C_PRX_N4 / SATA_DTX_C_PRX_P4
SATA_TXN4/PETN1 / SATA_TXP4/PETP1	AV15 / AW15	SATA_PTX_C_DRX_N4 / SATA_PTX_C_DRX_P4
SATA_RXN5/PERN2 / SATA_RXP5/PERP2	BC14 / BE14	SATA_DTX_C_PRX_N5 / SATA_DTX_C_PRX_P5
SATA_TXN5/PETN2 / SATA_TXP5/PETP2	AP15 / AR15	SATA_PTX_C_DRX_N5 / SATA_PTX_C_DRX_P5
SATA_RCOMP	AY5	SATA_COMP
SATALED#	AP3	SATA_ACT# — R108 10K_0402_5% — +3VS
SATA0GP/GPIO21	AT1	HDD_DET# — HDD_DET# <19>
SATA1GP/GPIO19	AU2	BBS_BIT0_R — BBS_BIT0_R <19>
SATA_IREF	BD4	+1.5VS
TP9	BA2	
TP8	BB2	

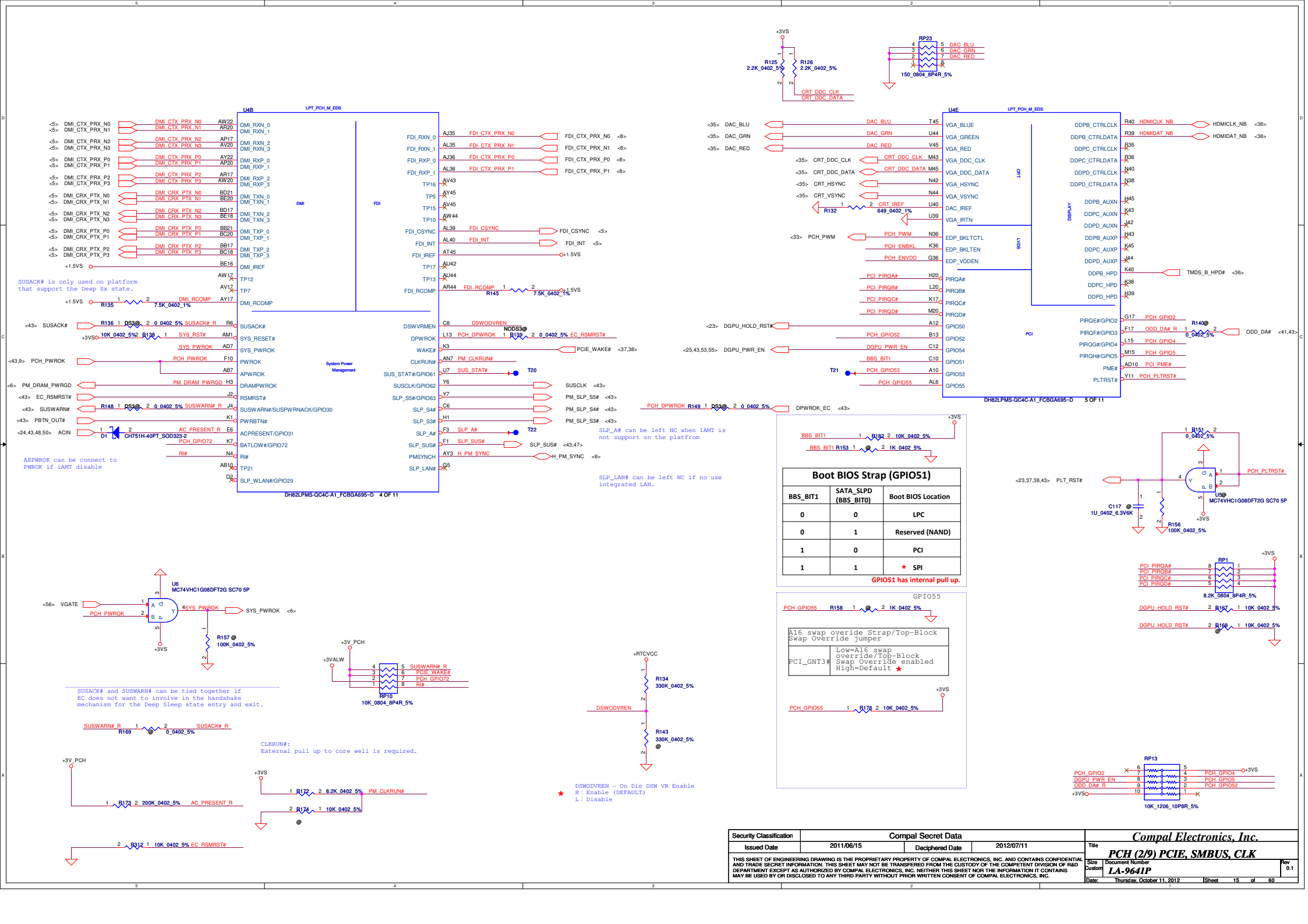
HDD_DET# and BBS_BIT0_R pull high by 10P8R

HDD: SATA_DTX_C_PRX_N4 <41> / SATA_DTX_C_PRX_P4 <41>; SATA_PTX_C_DRX_N4 <41> / SATA_PTX_C_DRX_P4 <41>
ODD: SATA_DTX_C_PRX_N5 <41> / SATA_DTX_C_PRX_P5 <41>; SATA_PTX_C_DRX_N5 <41> / SATA_PTX_C_DRX_P5 <41>
SATA 6G

SATA Impedance Compensation
SATA_COMP — R107 7.5K_0402_1% — +1.5VS
Note:
Trace width:4mils
Place the resistor to PCH <500 mils, to 1.5V <100 mils.Avoid routing next to clock pins.

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: LA-9641P | Rev: 0.1
Date: Thursday, October 11, 2012 | Sheet 14 of 60



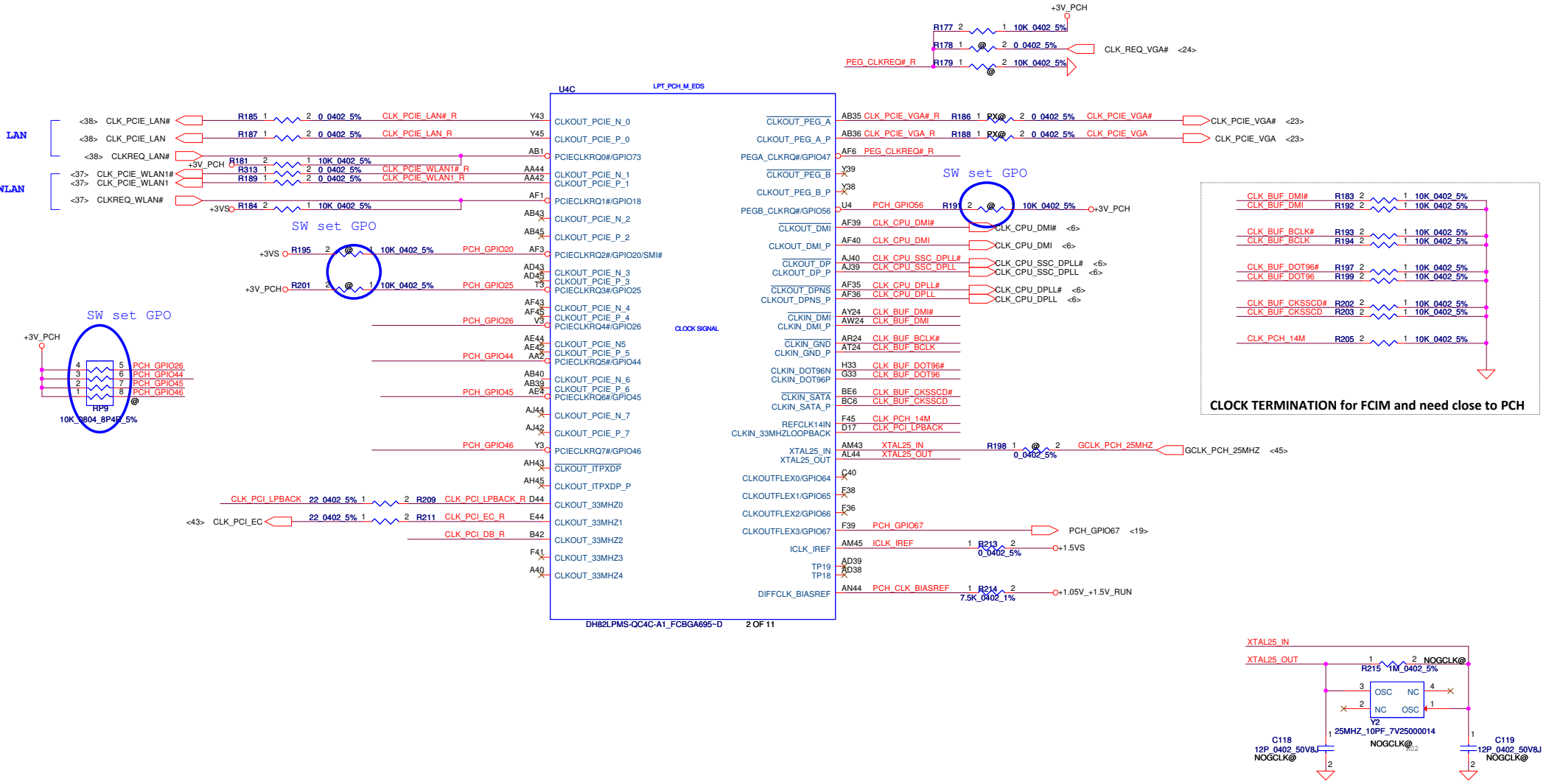
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 15 of 60



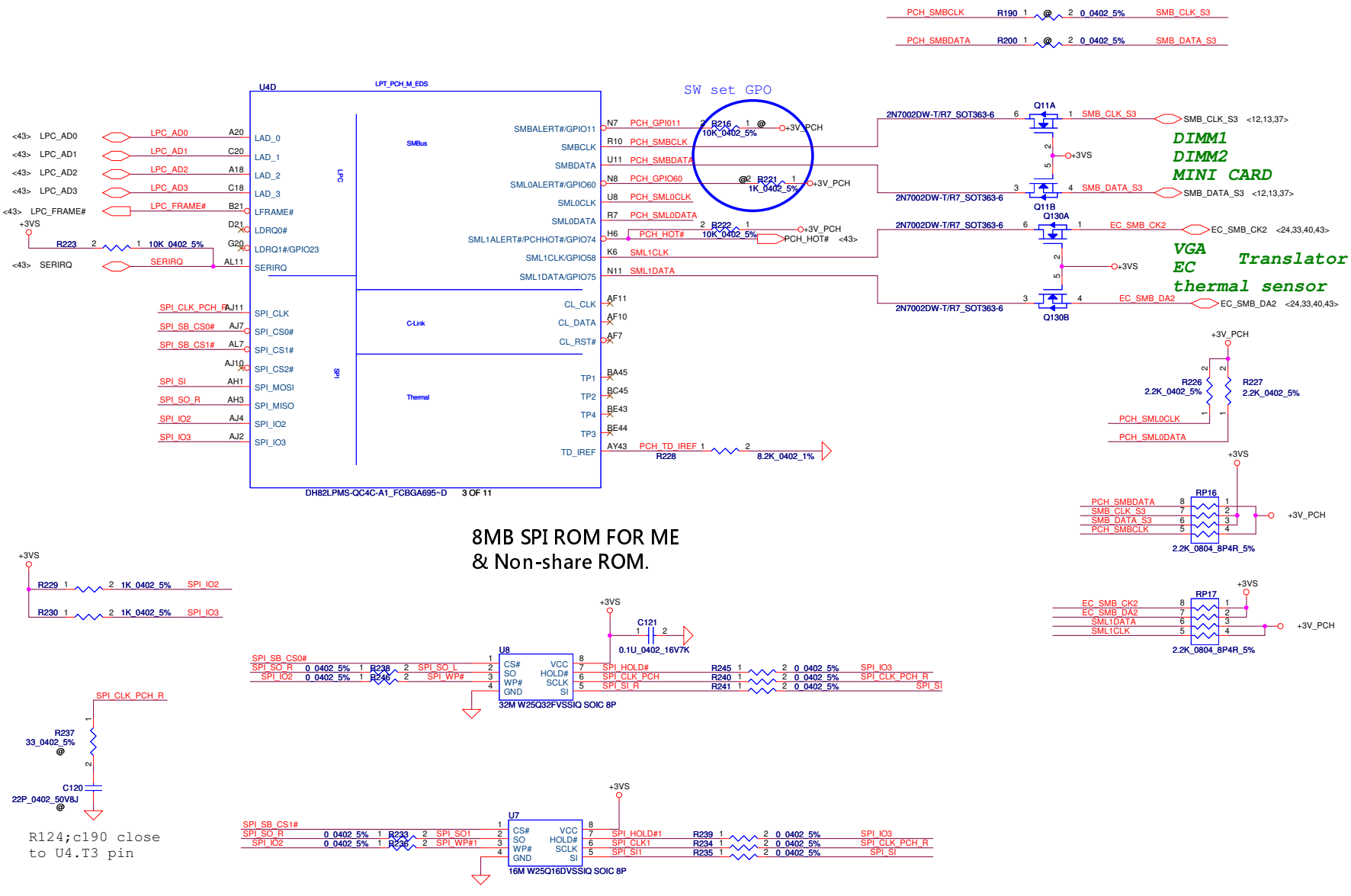
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 16 of 60



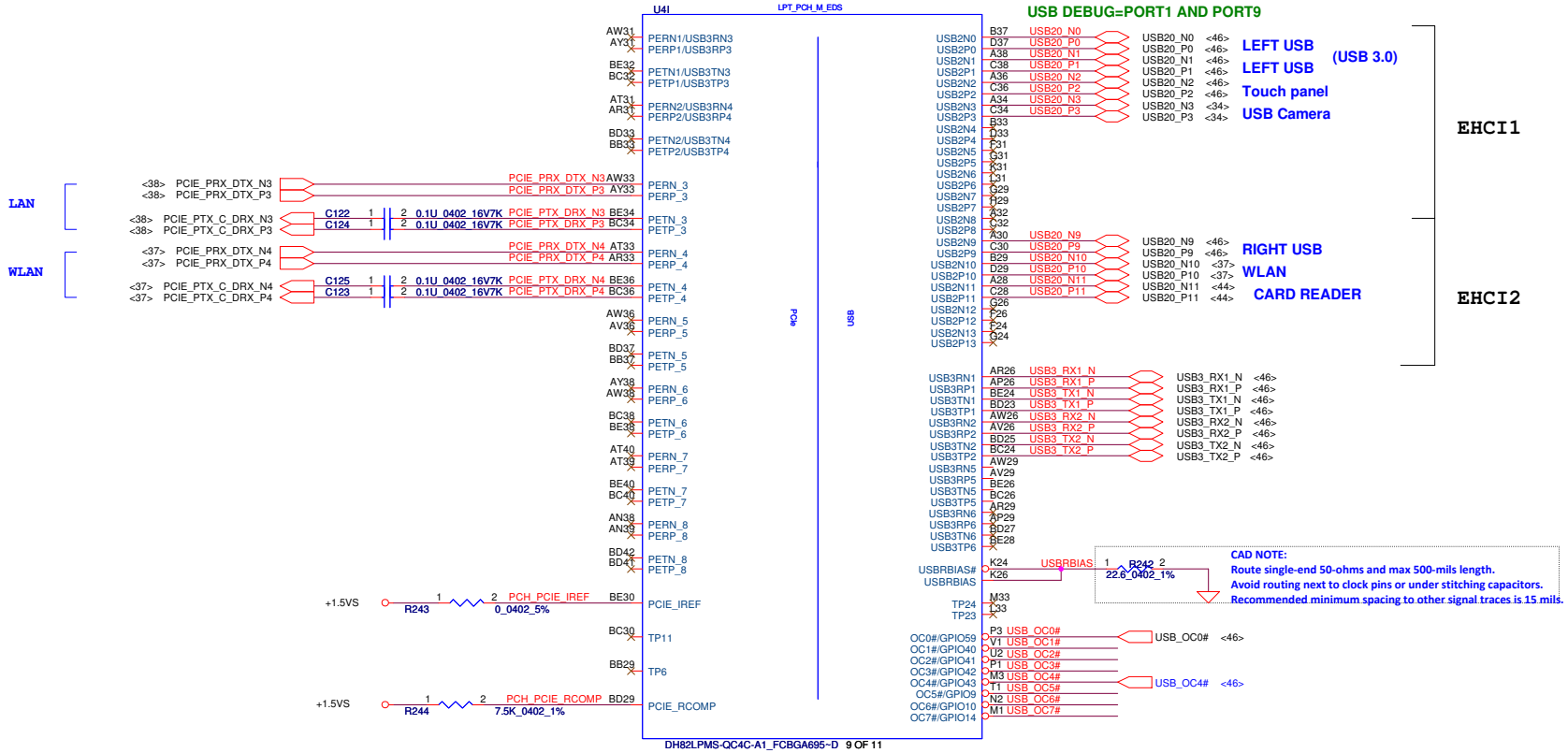
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

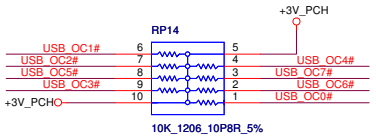
Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 17 of 60





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 18 of 60

Weak internal pull-high

SW set GPO

Remove strap description
inform SW set GPO

BIOS Request SKU ID

SW set GPO

PU on power side

Check Behavior

Need Update

PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	UMA
1	1	DIS

PCH_GPIO69	Function
0	
1	

PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	SUN PRO
1	Mars XT

Config	GPIO16 & 49
USB3.0 x4, PCIE x8, SATA x6	11
USB3.0 x6, PCIE x8, SATA x4	01

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

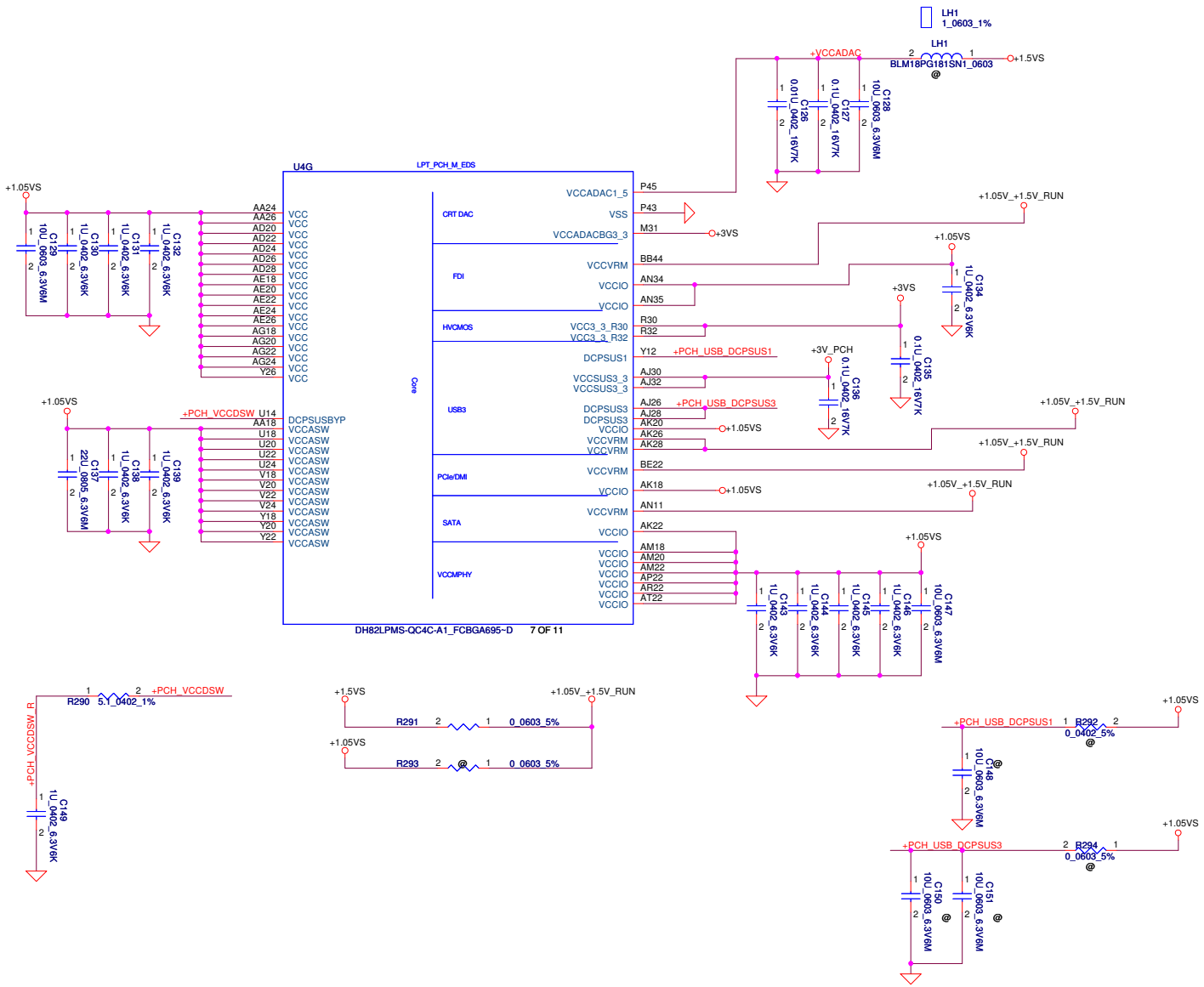
Security Classification: Compal Secret Data
Issued Date: 2011/06/15 | Deciphered Date: 2012/07/11

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 19 of 60



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

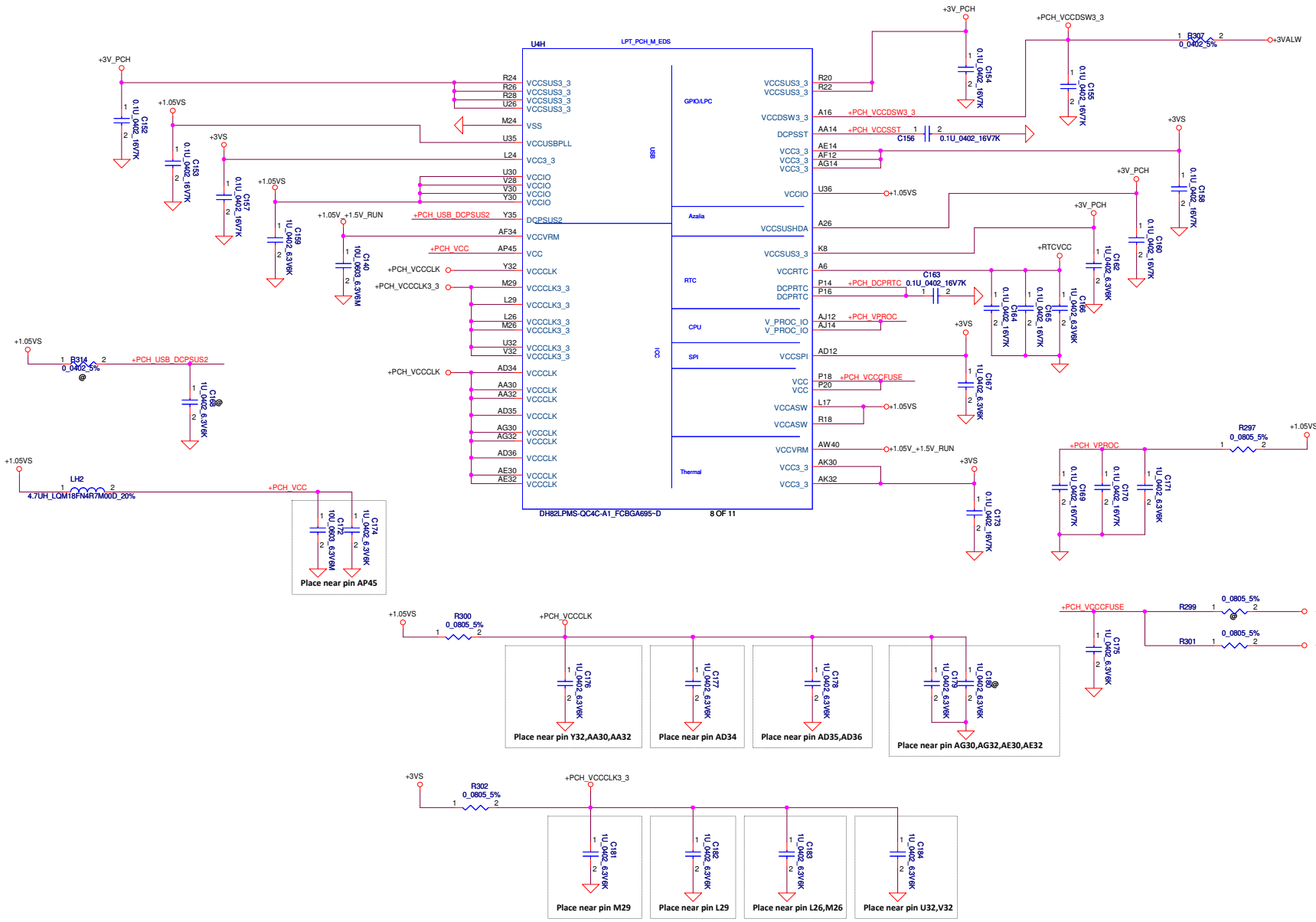
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 20 of 60



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

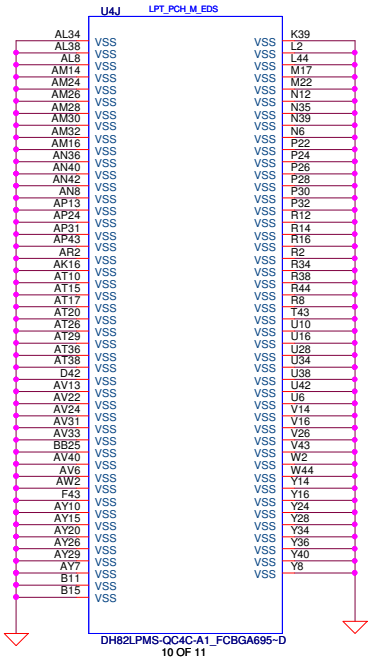
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

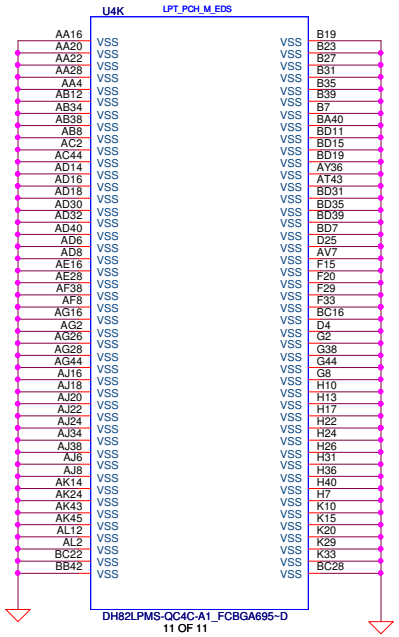
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 21 of 60





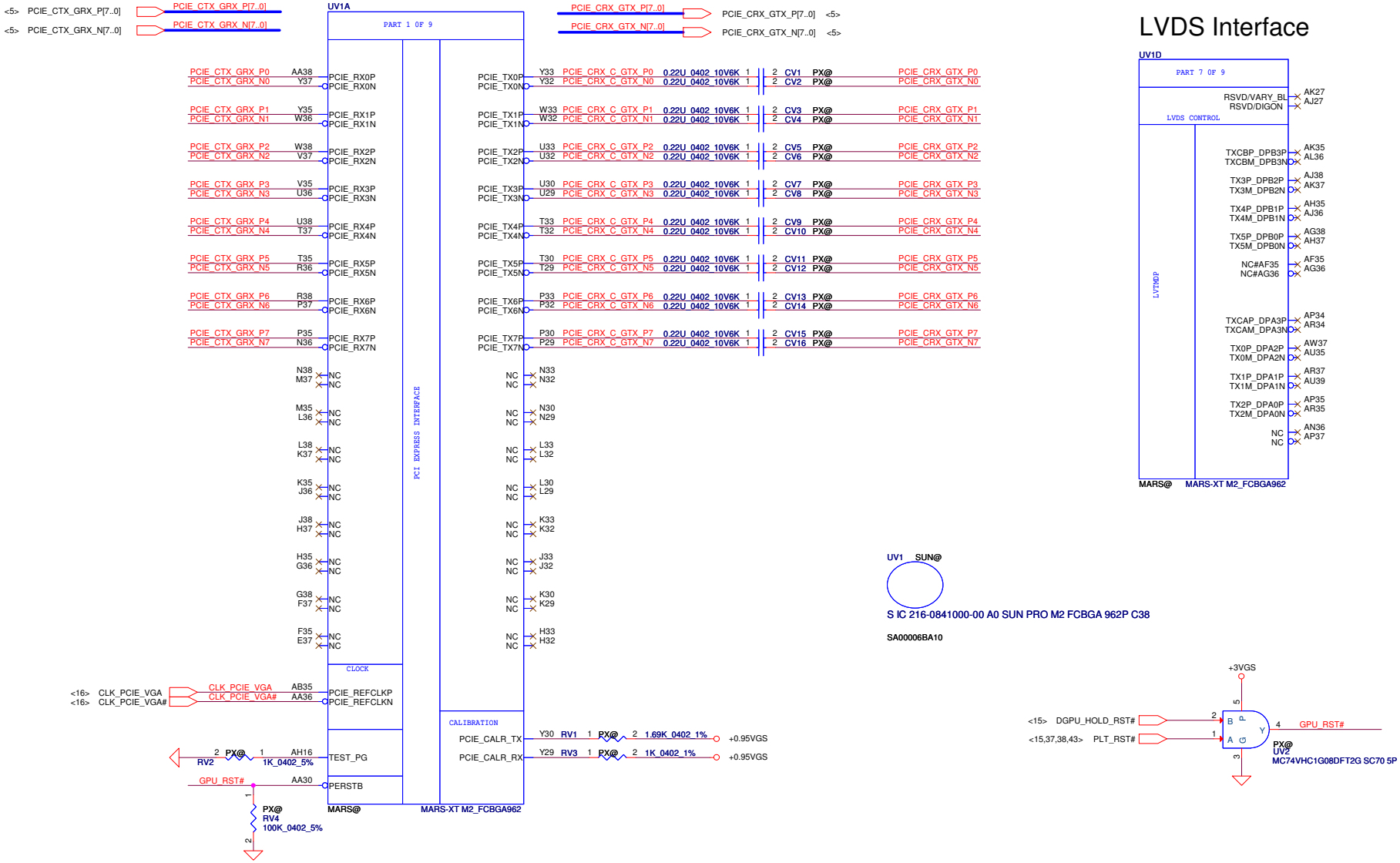
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

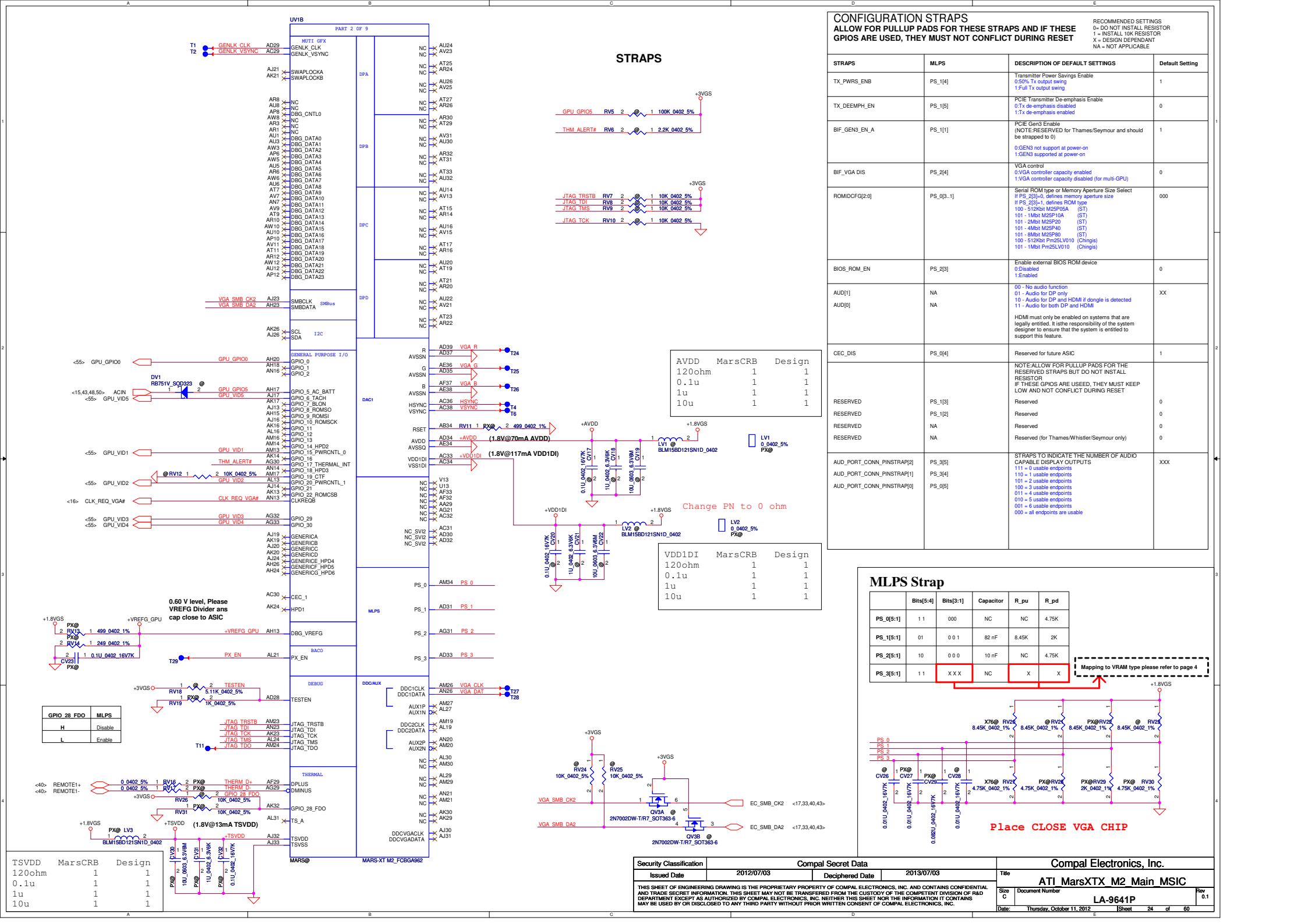
Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 22 of 60



LVDS Interface

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/03	Deciphered Date 2013/07/03	Title: ATI_MarsXTX_M2_PCIE/LVDS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Custom; Document Number: LA-9641P; Rev: 0.1
			Date: Thursday, October 11, 2012; Sheet 23 of 60



STRAPS

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

GPIO_28_FDO	MLPS
H	Disable
L	Enable

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	000	NC	NC	4.75K
PS_1[5:1]	01	0 0 1	82 nF	8.45K	2K
PS_2[5:1]	10	0 0 0	10 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 4

Place CLOSE VGA CHIP

Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_Main_MSIC

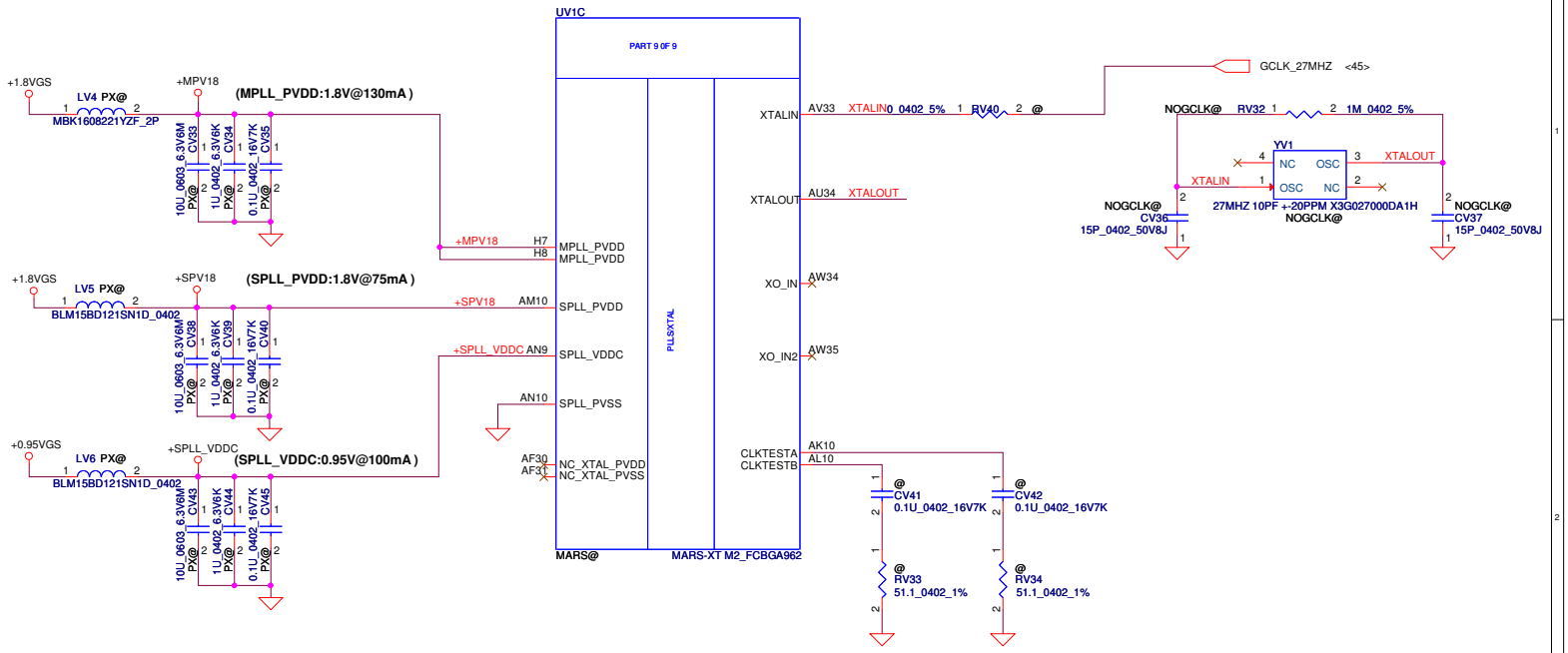
Size	Document Number	Rev
C	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 24 of 60

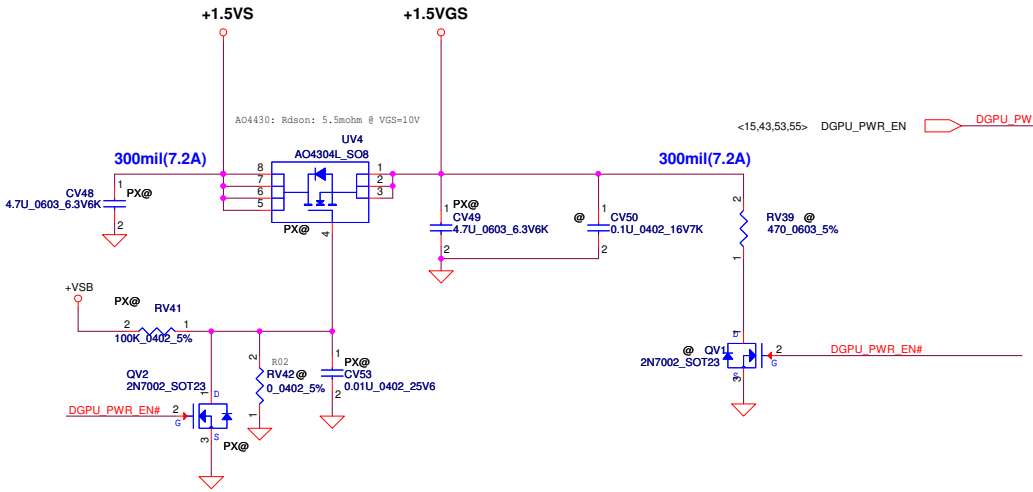
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

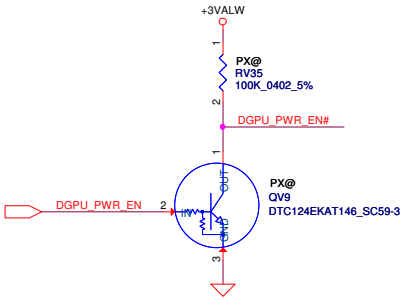
SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

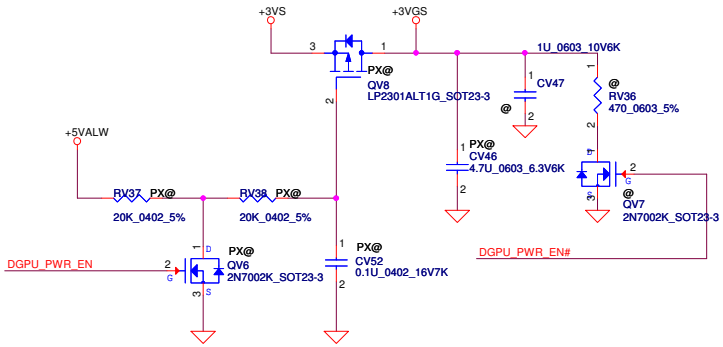


+1.5VS to +1.5VGS Transfer





<+3VS TO +3VGS> **Need OPEN**



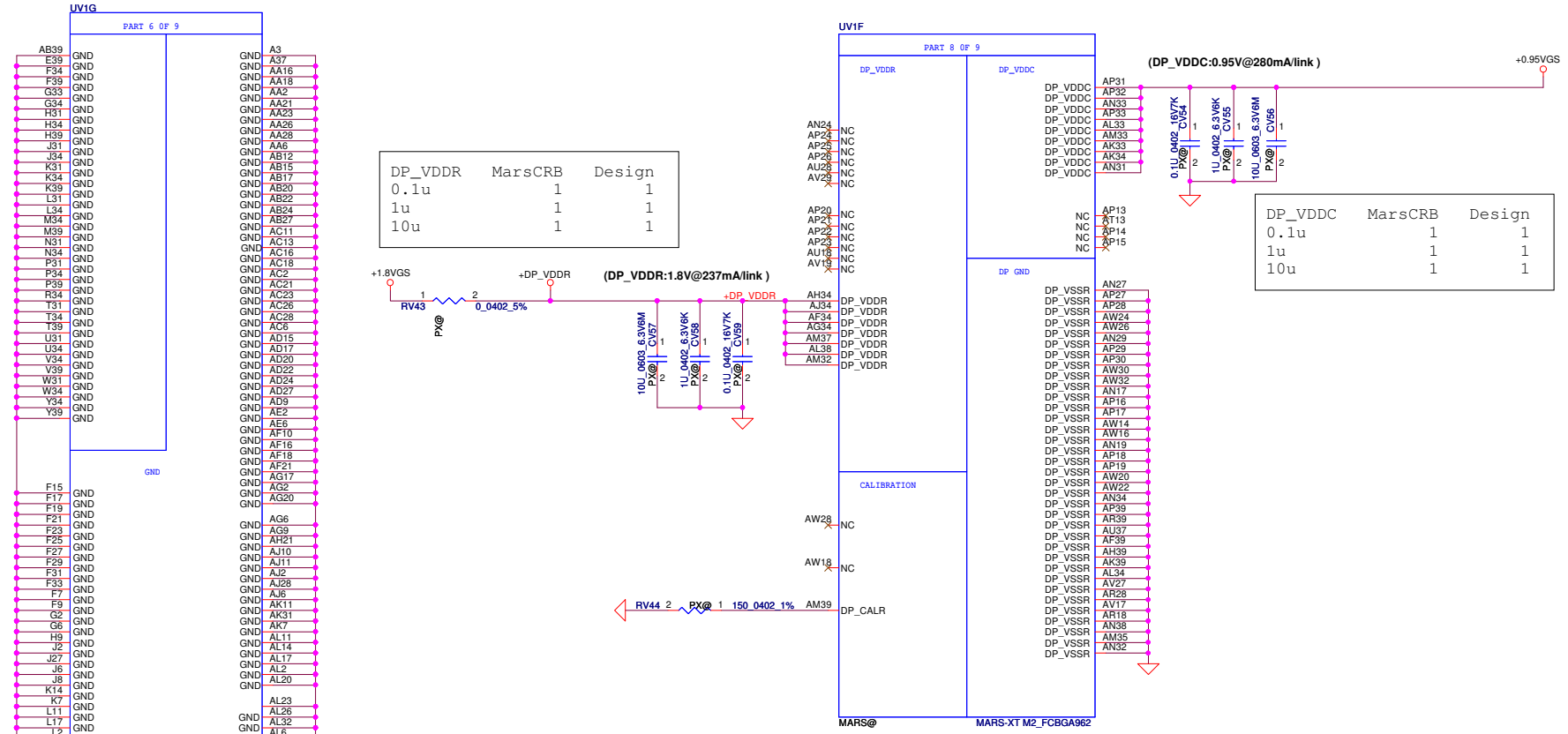
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_BACO POWER

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 25 of 60



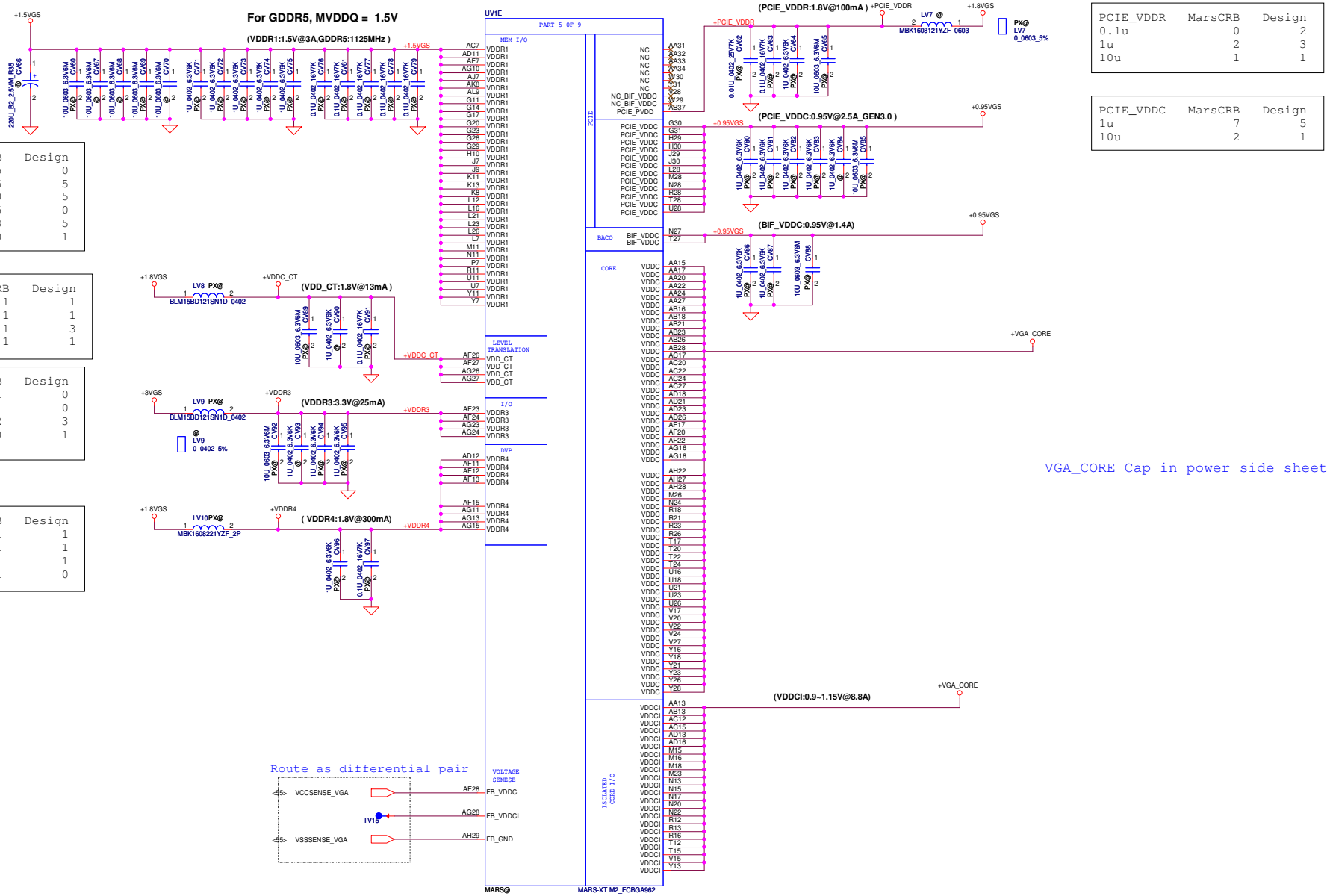
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_PWR_GND

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 26 of 60



VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

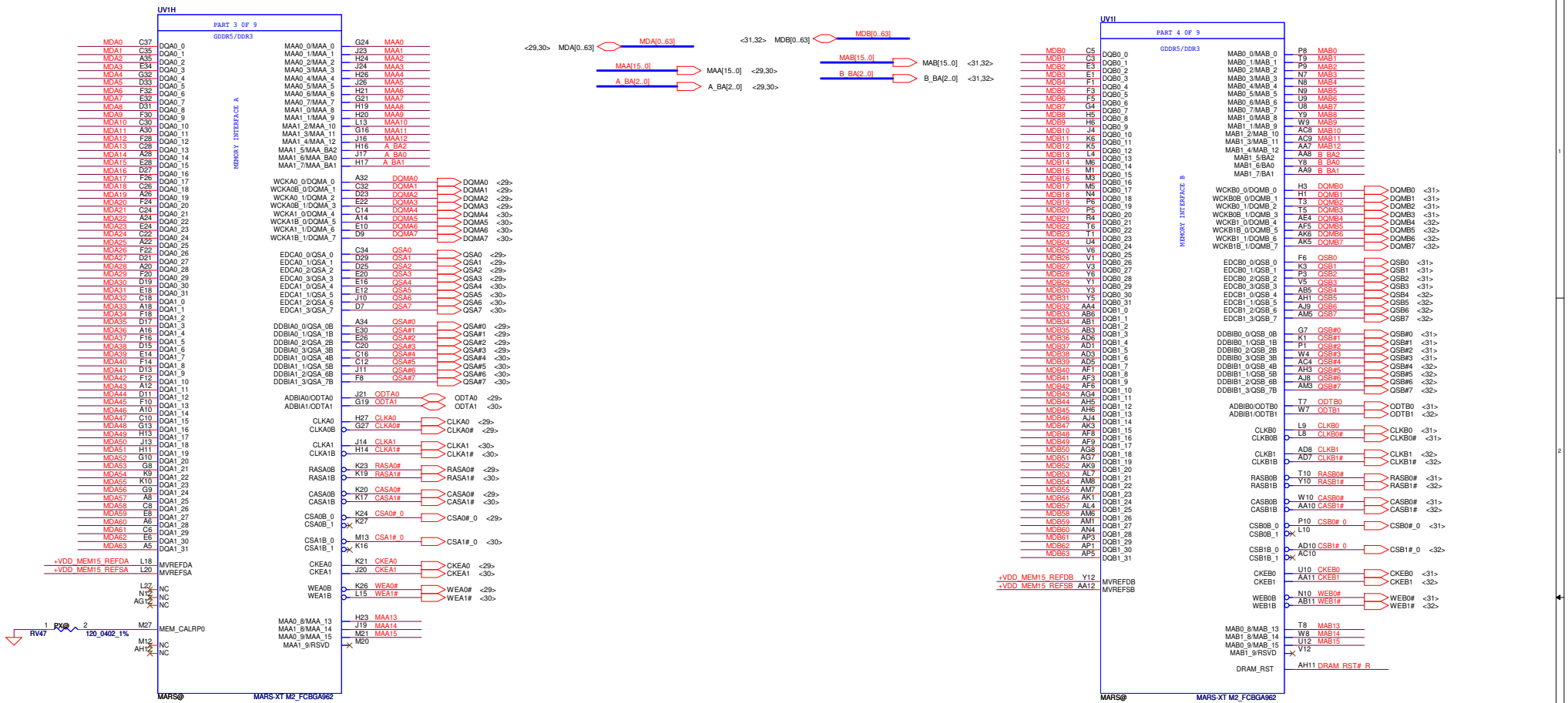
Security Classification	Compal Secret Data	
Issued Date	2012/07/03	Deciphered Date 2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_Power

Size	Document Number	Rev
C	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 27 of 60



Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"

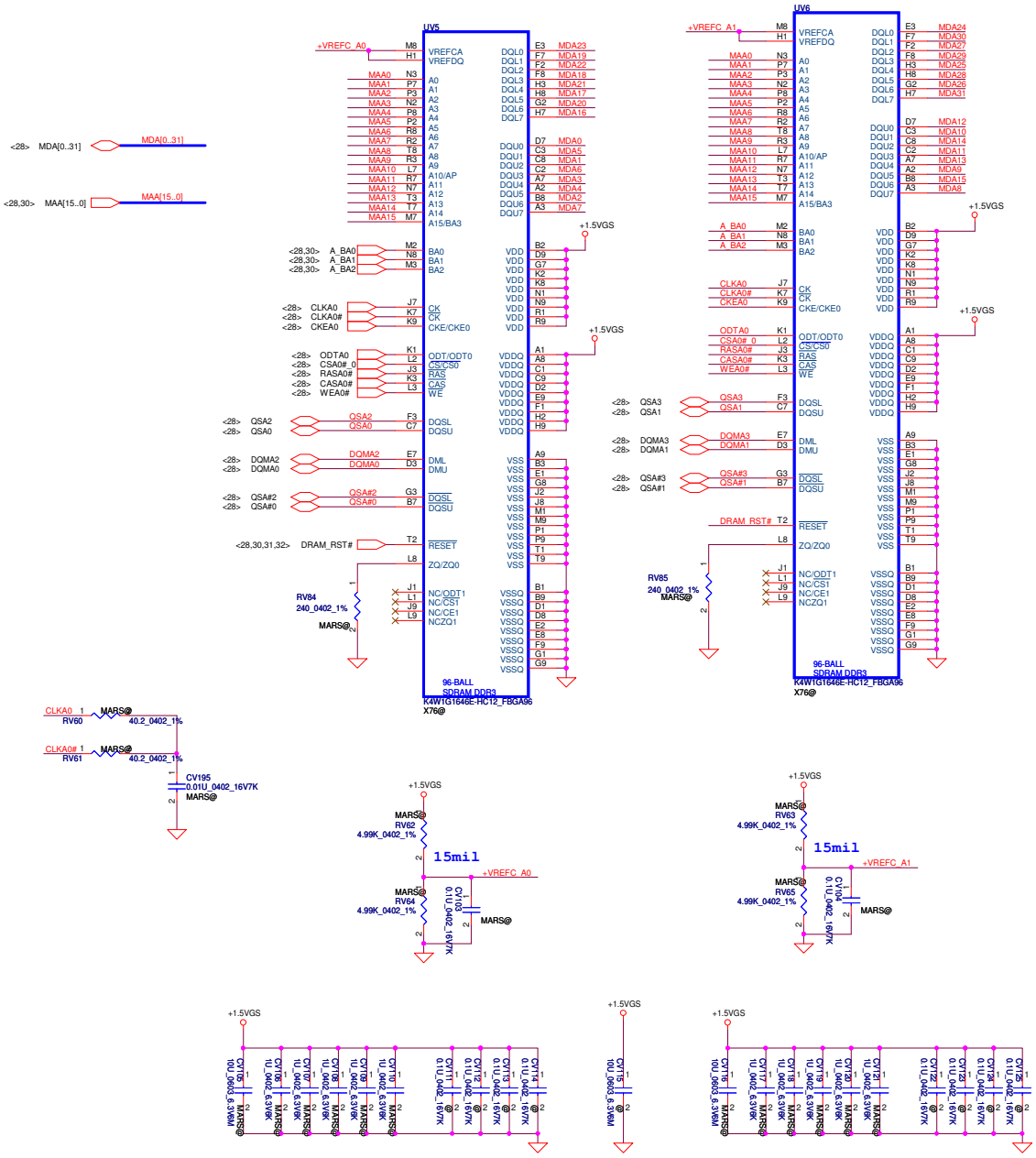
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_MEM IF

Size	Document Number	Rev
C	LA-9641P	0.1

Date: Thursday, October11, 2012 Sheet 28 of 60



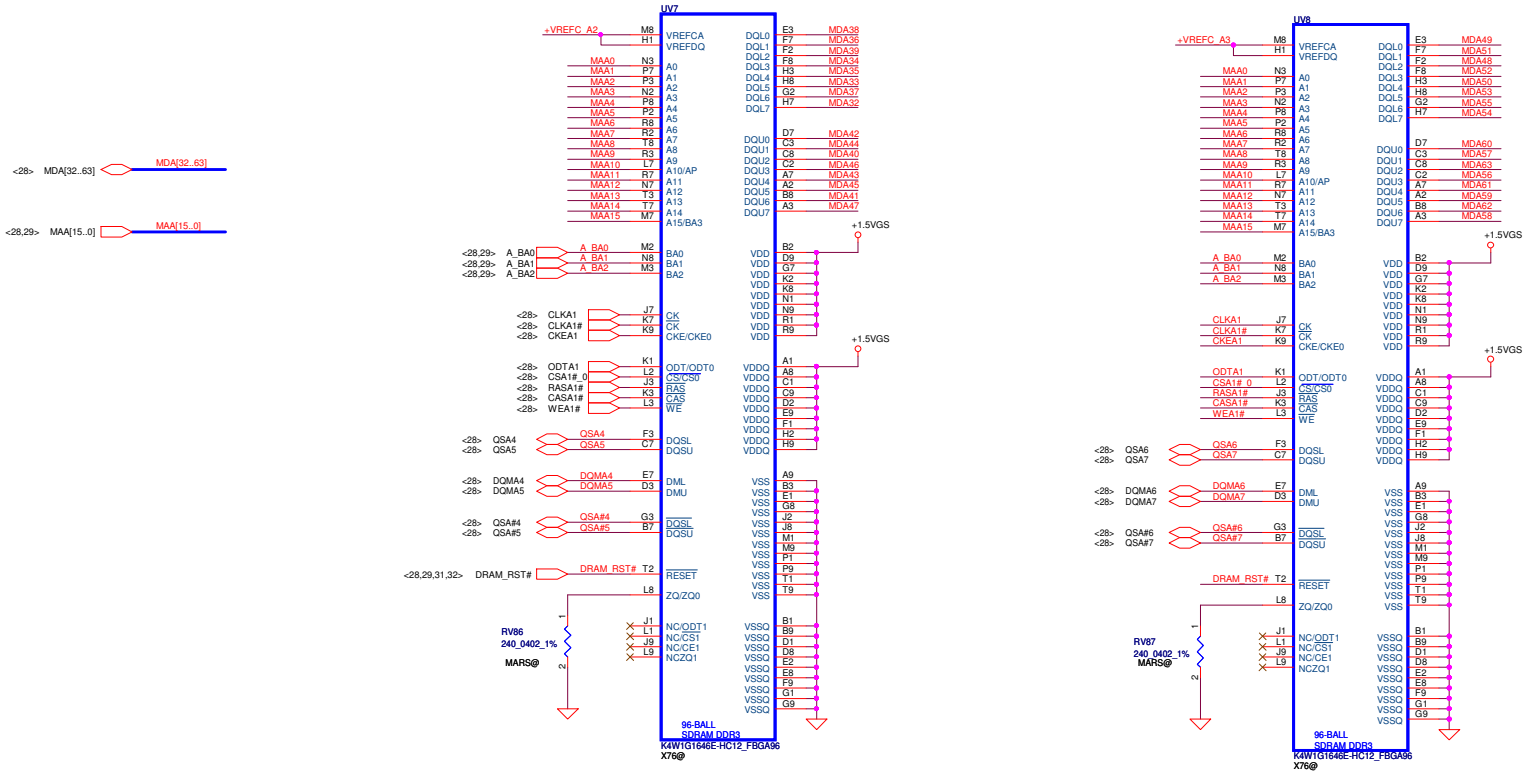
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

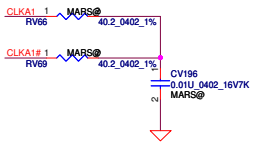
Compal Electronics, Inc.

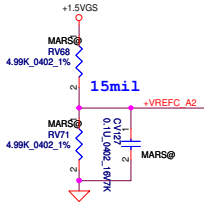
Title: ATI_Whistler_M2_VRAM_A

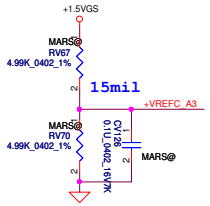
Size	Document Number	Rev
C	0D0<974S	0.1

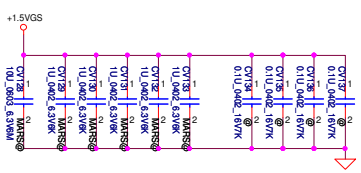
Date: Thursday, October 11, 2012 | Sheet 29 of 60

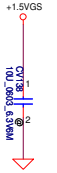


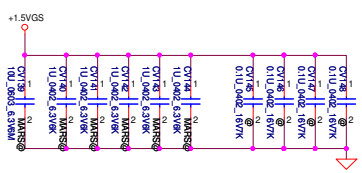












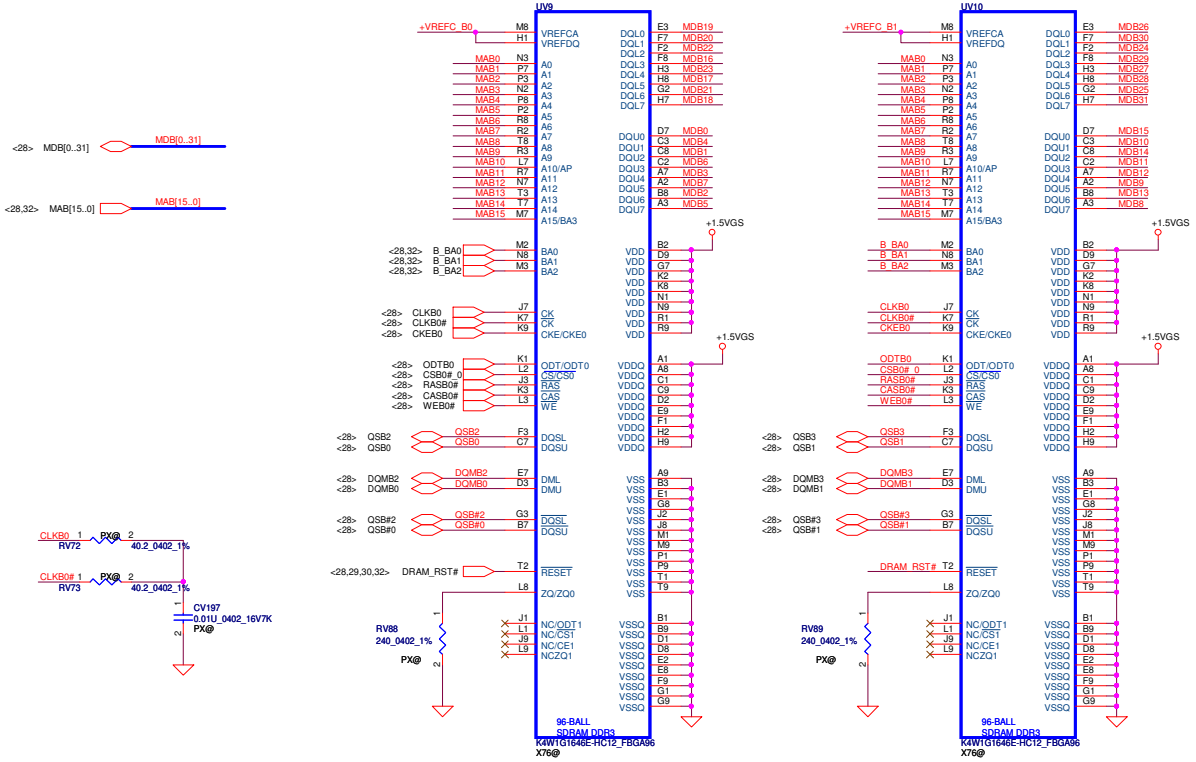
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

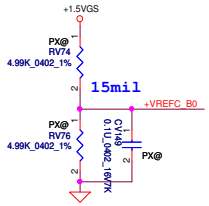
Compal Electronics, Inc.

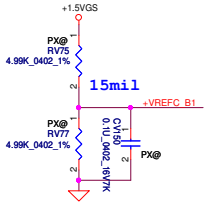
Title: ATI_Whistler_M2_VRAM_A

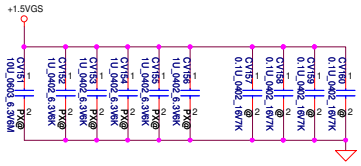
Size	Document Number	Rev
C	LA-9641P	0.1

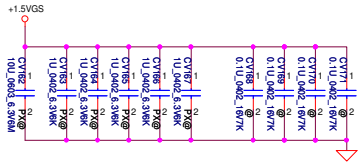
Date: Thursday, October 11, 2012 | Sheet 30 of 60











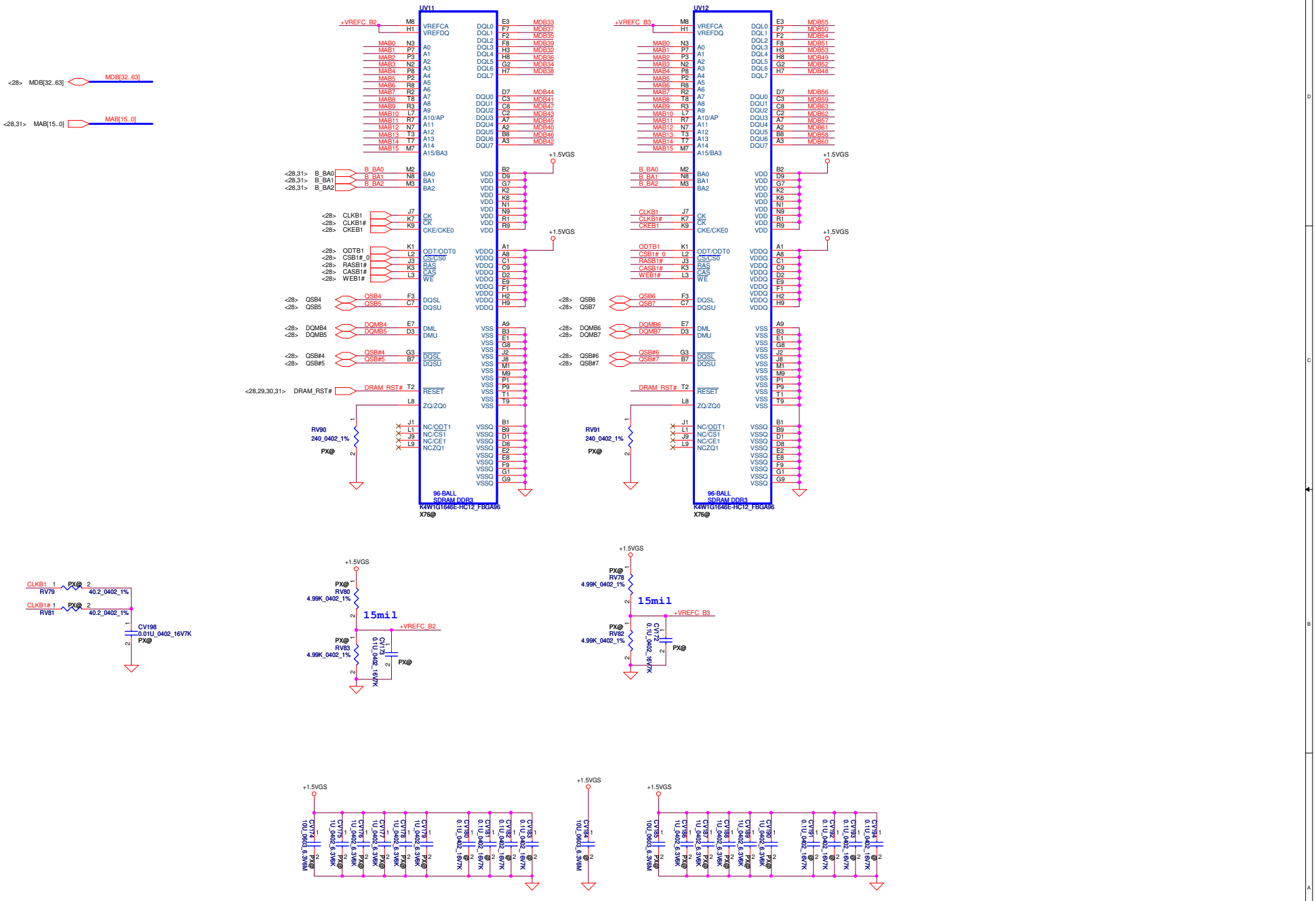
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B

Size	Document Number	Rev
C	0D0<974S	0.1

Date: Thursday, October 11, 2012 | Sheet 31 of 60



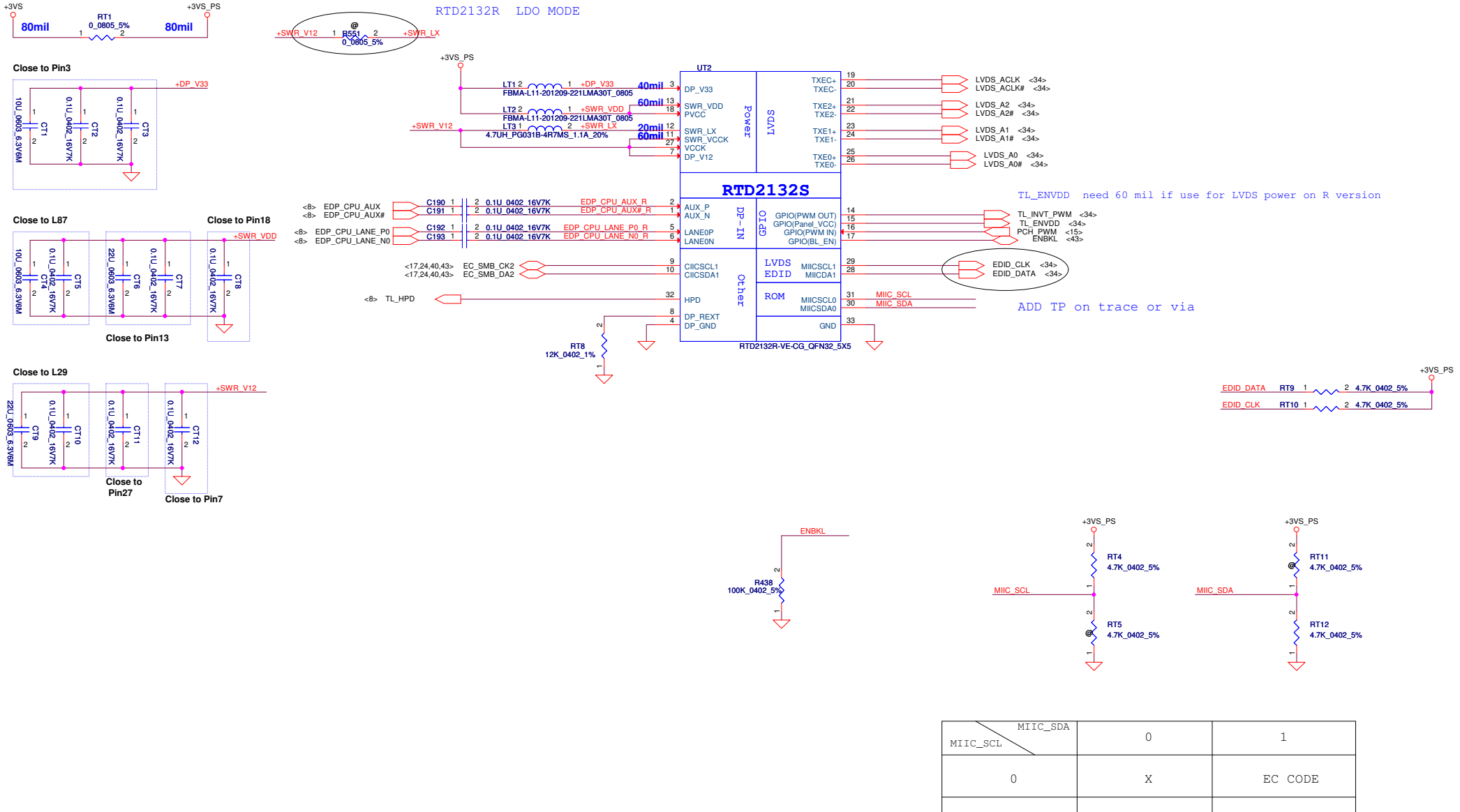
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	0D0<974S	0.1

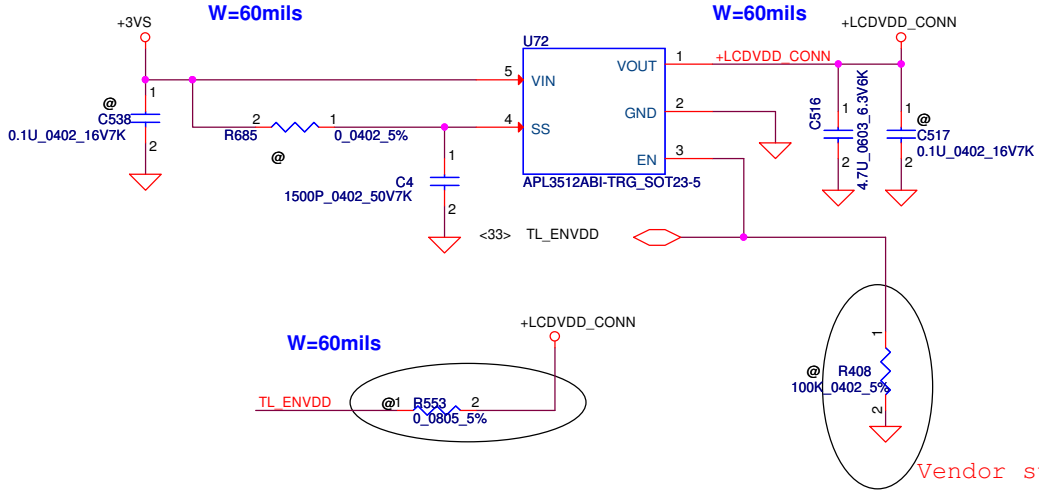
Date: Thursday, October 11, 2012 | Sheet 32 of 60



MIIC_SDA / MIIC_SCL	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date 2013/06/30	Title: LVDS Translator - RTD2132S
			Size: Custom; Document Number: LA-9641P; Rev: 0.1
			Date: Thursday, October 11, 2012; Sheet 33 of 60

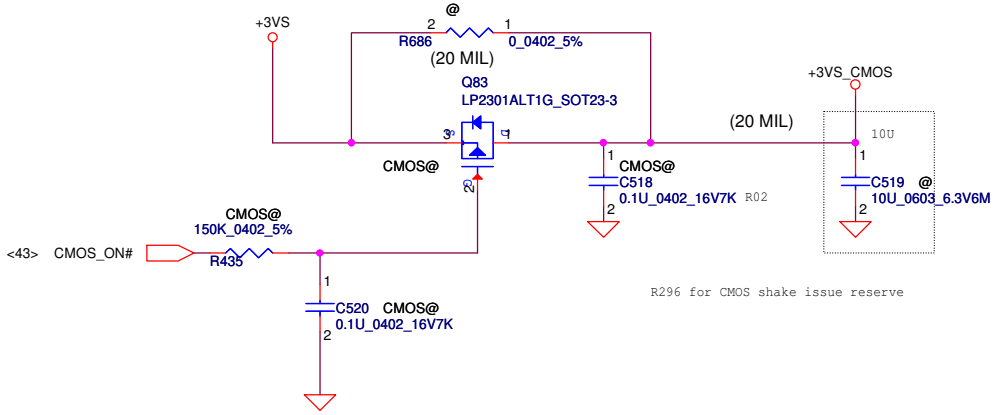
LCD POWER CIRCUIT



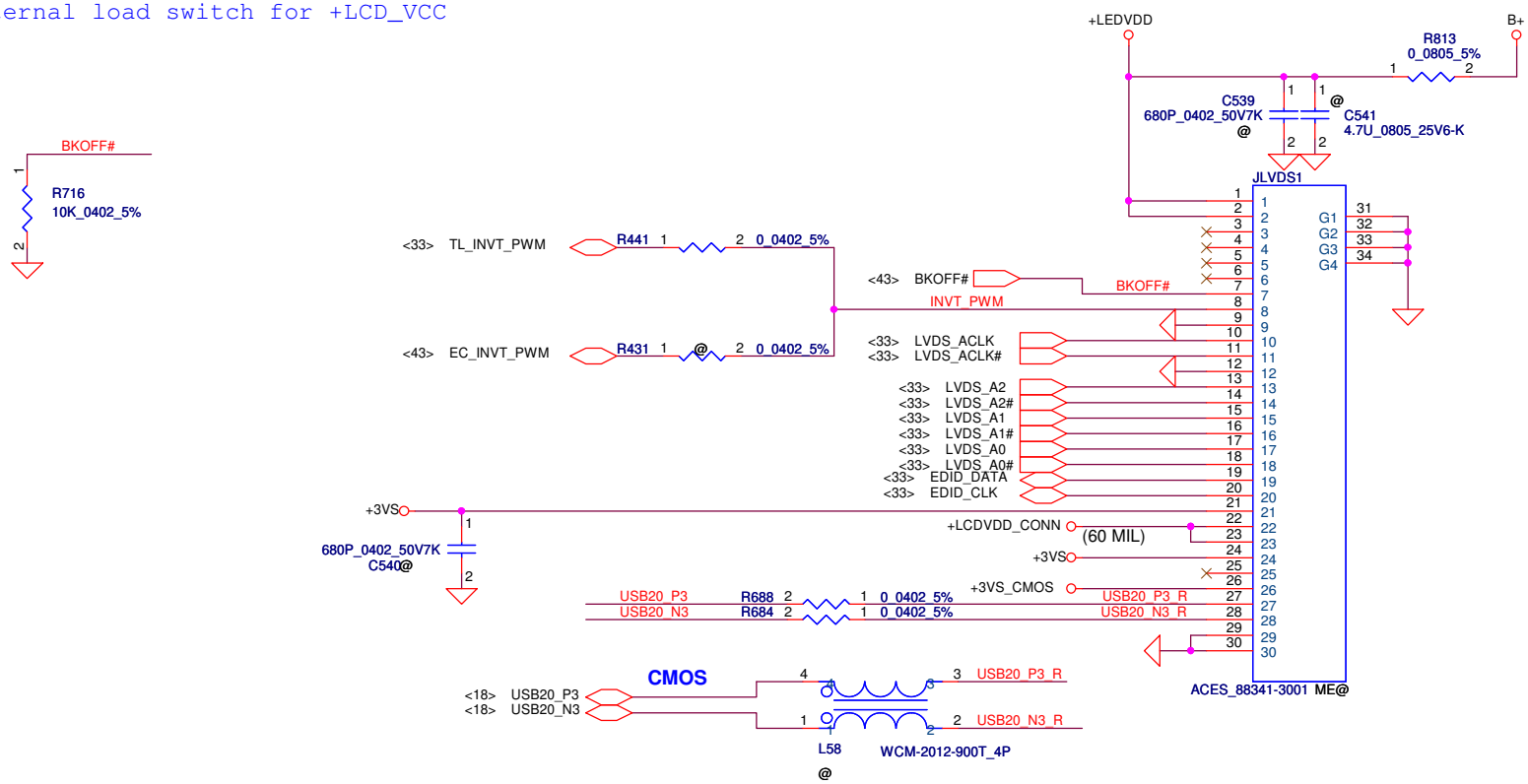
Vendor suggest reserve

RTD2132R Internal load switch for +LCD_VCC

CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

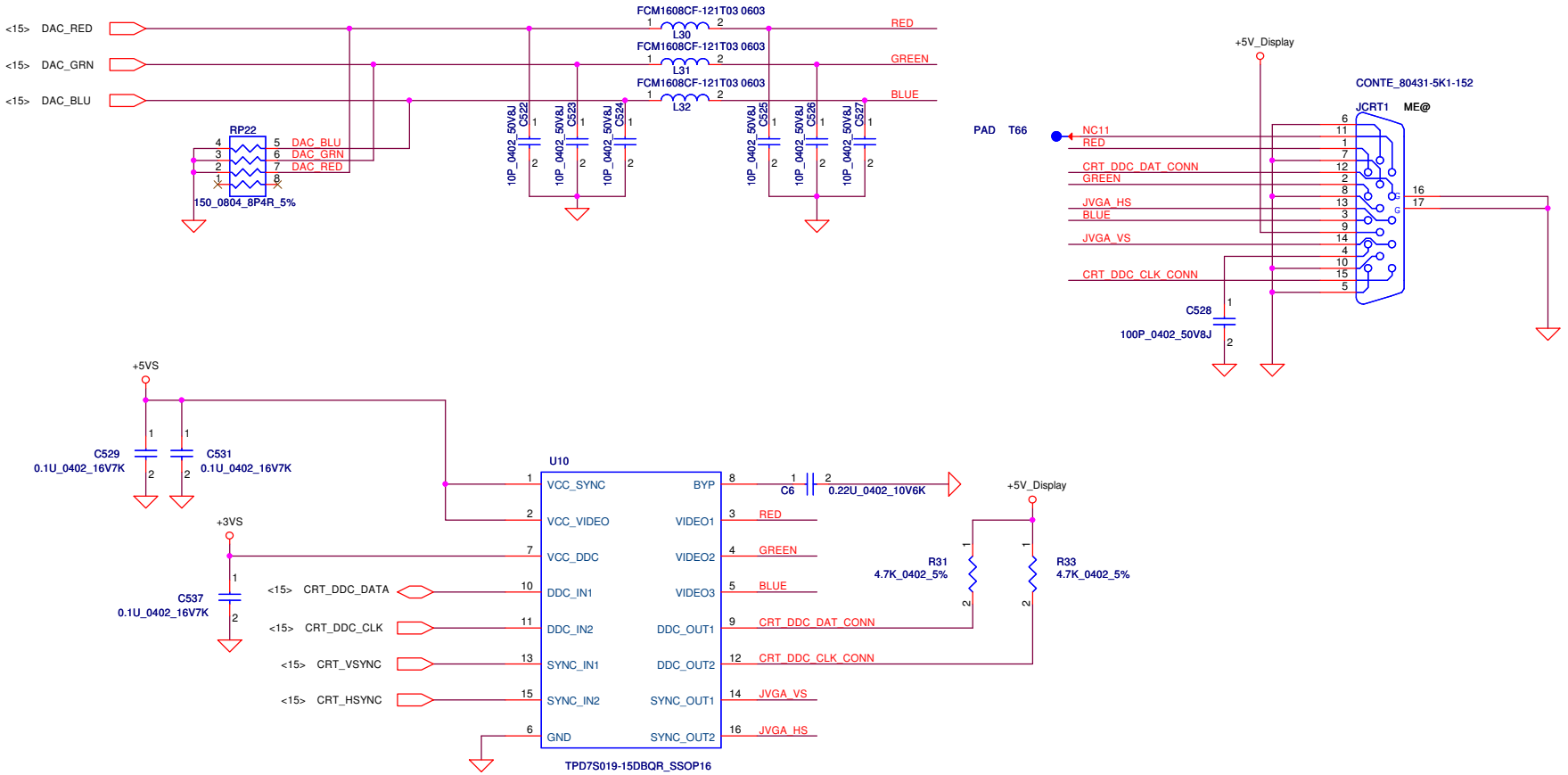
Compal Electronics, Inc.

Title: LVDS/CAMERA

Size	Document Number	Rev
Custom	LA-9641P	0.1

Date: Thursday, October 11, 2012 Sheet 34 of 60

CRT Connector



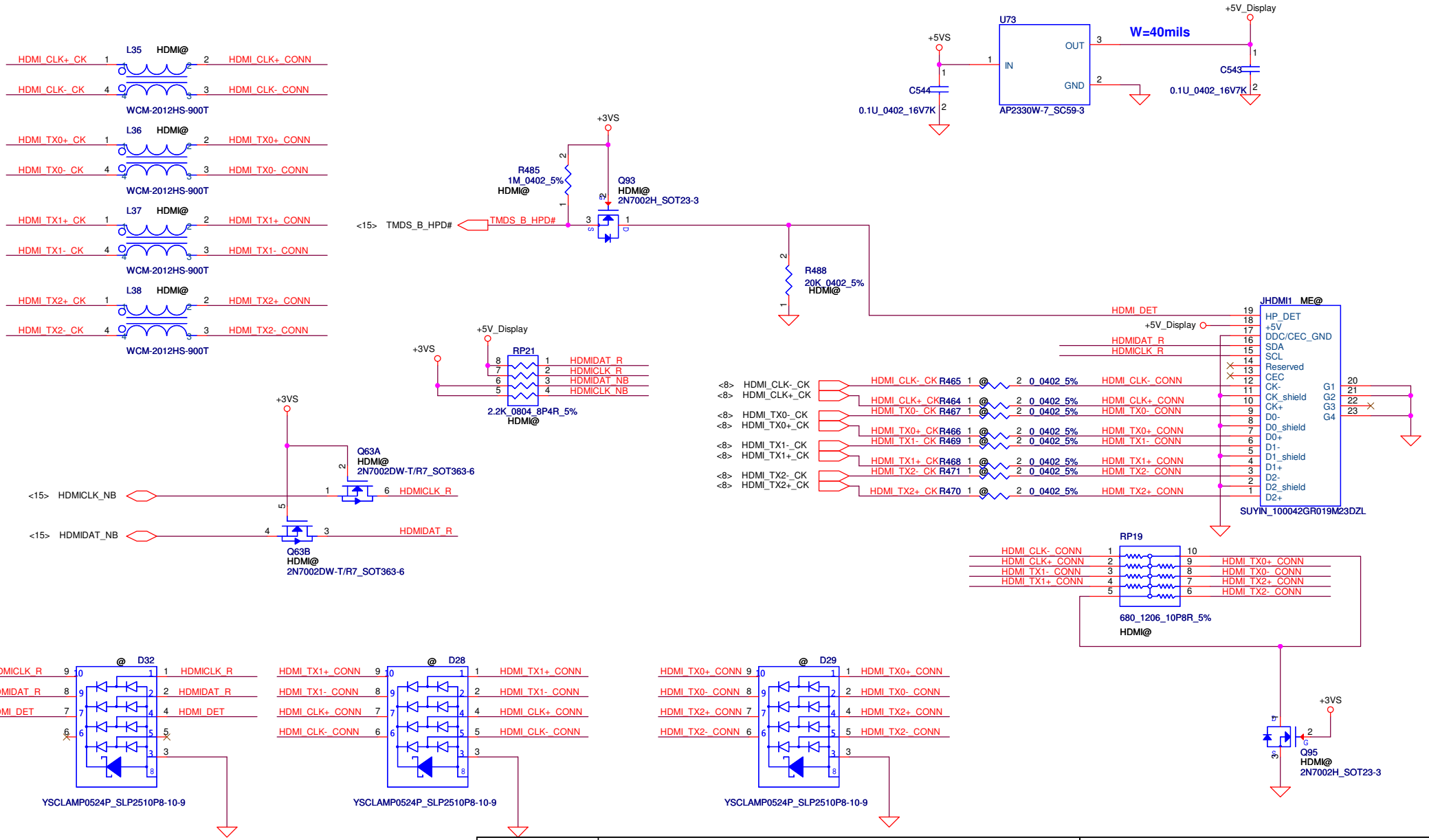
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 35 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

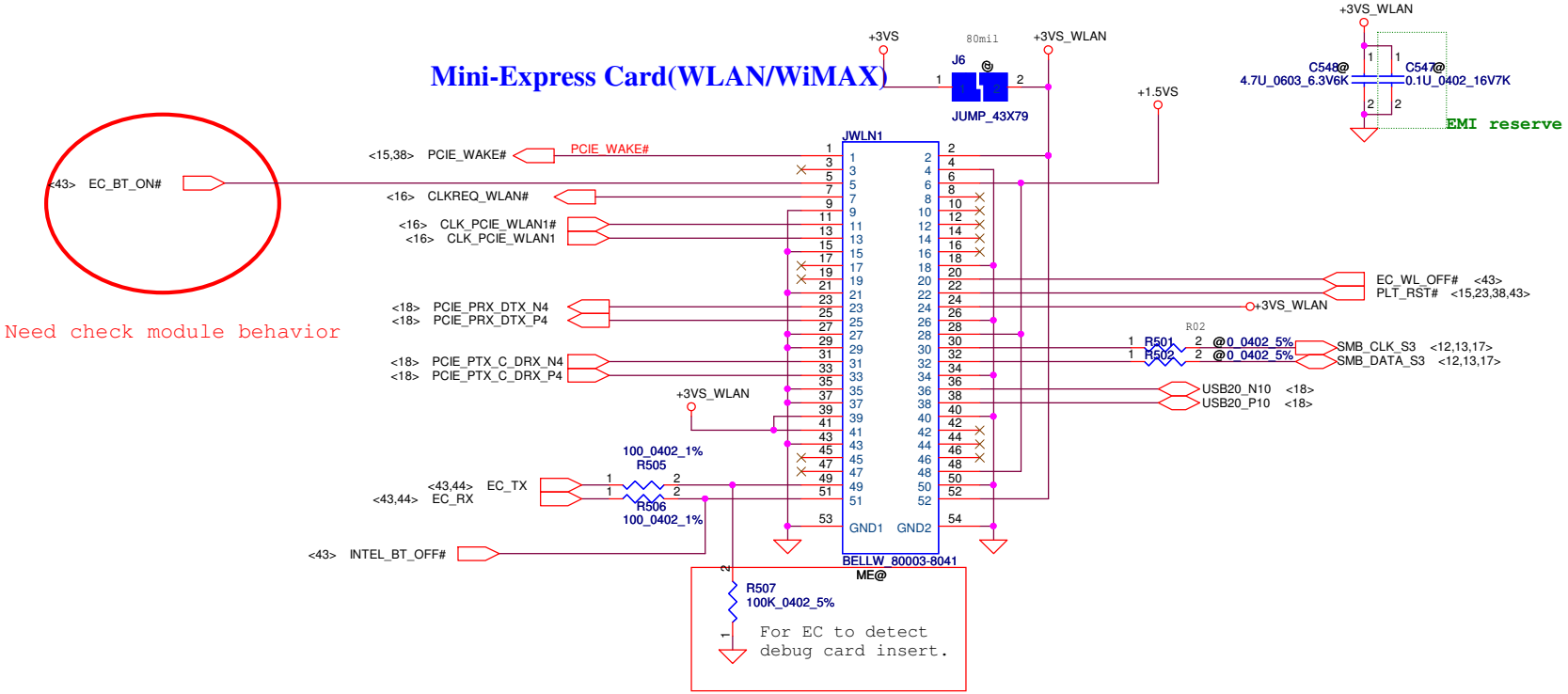
Compal Electronics, Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-9641P	0.1

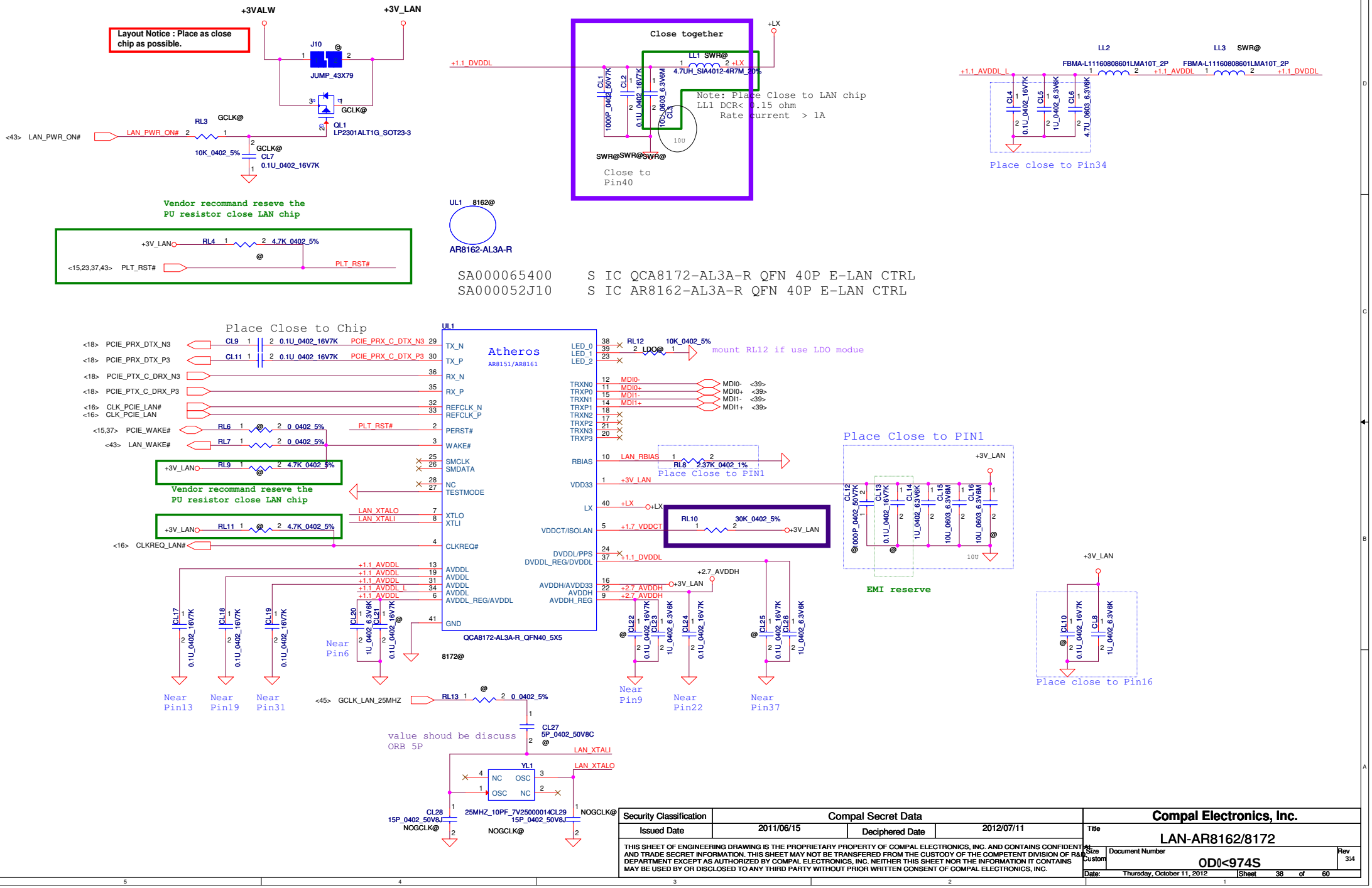
Date: Thursday, October 11, 2012 Sheet 36 of 60

Mini-Express Card for WLAN/WiMAX(Half)



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	Mini-Card/NEW Card/SIM		
Size	Document Number	LA-9641P	Rev 3|4
Date: Thursday, October 11, 2012	Sheet 37 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-AR8162/8172

Size: Custom | Document Number: 0D0<974S | Rev: 3I4

Date: Thursday, October 11, 2012 | Sheet 38 of 60

Place Close to TL1

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

@
DL1
AZC099-04S.R7G_SOT23-6

Reserve gas tube for EMI go rural solution

RL14 75_0805_5%
CL30 10P_0603_50V
CHASSIS1_GND
DLL1
BS4200N-C-LV_SMB-F2
GAS@

Place Close to TL1

TL1
MHPC_NS681612A
CL31 0.01U_0402_16V7K

CL63 0.1U_0603_50V7K
CL61 0.1U_0603_50V7K
CHASSIS1_GND

Need check Symbol

JLAN1
SANTA_130456-121
ME@
CHASSIS1_GND

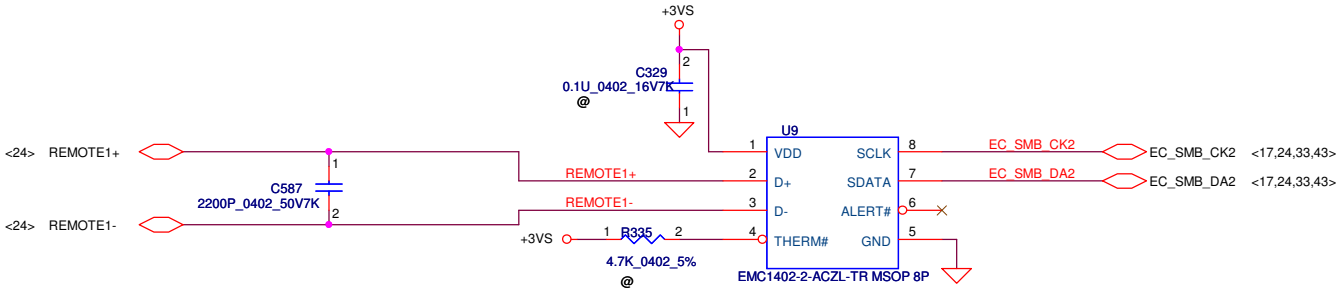
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN_Transformer

Size: B | Document Number: 0D0<974S | Rev: 3l4

Date: Thursday, October 11, 2012 | Sheet 39 of 60



EMC1412-A (SA00003YA00)
Address 1111_100xb
S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

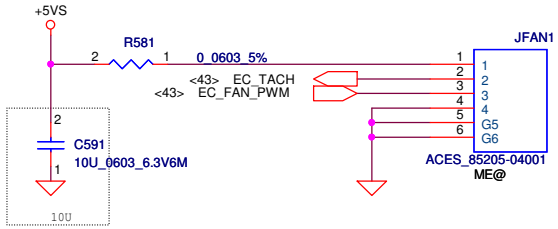
A B M/B 橢圓孔 M/B 圓孔

2P8 * 7 pcd

D

E

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

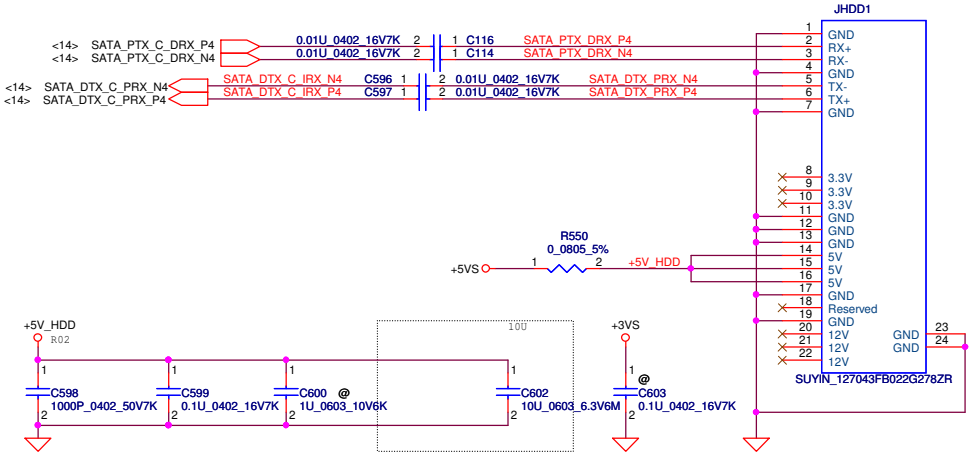
Compal Electronics,Ltd.

Title: Fintek-Thermal IC/FAN/screw

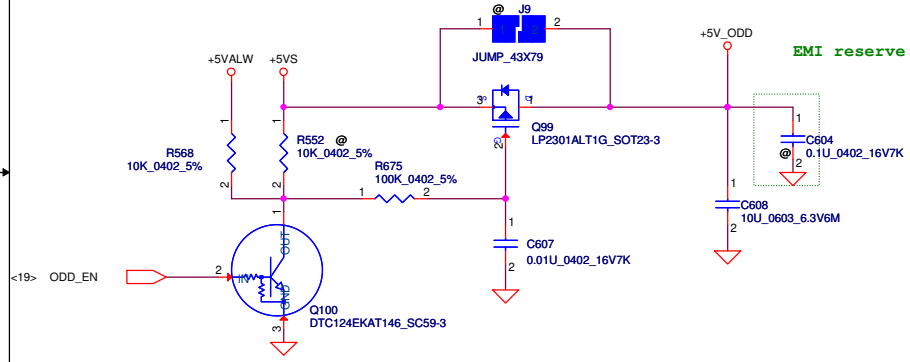
Size: B | Document Number: LA-9641P | Rev: 3\4

Date: Thursday, October 11, 2012 | Sheet 40 of 60

SATA HDD Conn.

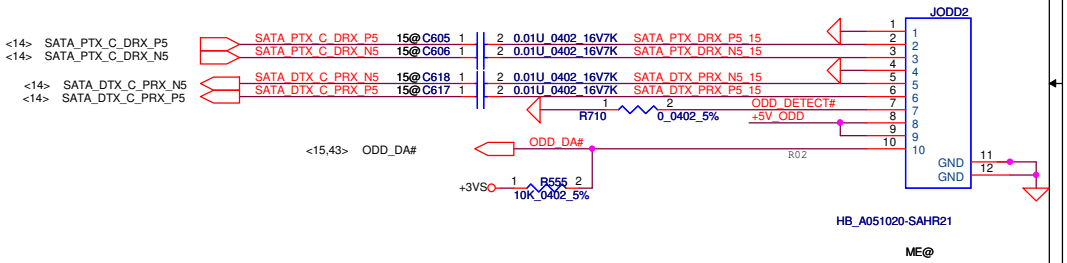


ODD Power Control



FOR 15"

SATA ODD FFC Conn.

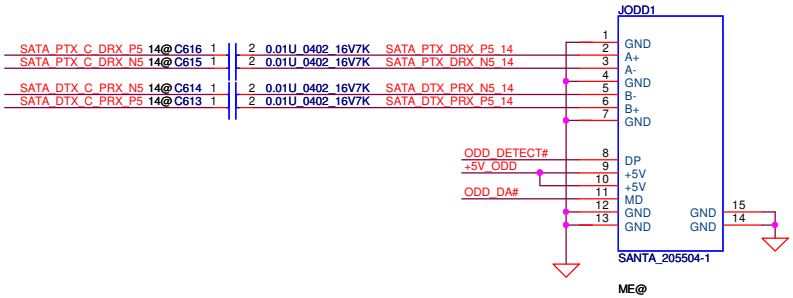


ME@

Co-lay

FOR 14"

SATA ODD Conn.



ME@

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-9641P	3I4

Date: Thursday, October 11, 2012 | Sheet 41 of 60

CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Sense resistors must be connected same power that is used for VAUX_3.3

mount RA6 on the Jack Sense circuit to configure Port-C for mono MIC.

Don't support LINE_IN function RA7 could be @

CA3 vendor suggest change to 2.2U

AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.

Should be same supply rail as used for PCH HDA bus controller section

Layout Note:Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

Please bypass caps very close to device.

10 mils

Check footprint

HGNDA, HGNDB 80mils

Universal Jack
External MIC

Internal analog MIC

Headphone

Internal SPEAKER

using wide copper bridge under codec (100 mils or more)

EMI request reserve RA21 & CA7

for Universal jack

CA30 vendor suggest change to 2.2U

follow vendor suggest & reserver default design

Place colose to Codec chip

CA41 vendor suggest change to 1U

LA1~LA4 vendor suggest mount 0 ohm first~ Bead reserve for EMI if needed

wide 20MIL

vendor suggest change to 1000p

PC Beep

EC Beep

ICH Beep

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: CX20751 Codec

Size: Custom | Document Number: 0D0<974S | Rev: 3A4

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Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

HDA_SDOUT: For ME FALSH

PN : SA000040B20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

KB9012QF A3 LQFP 128P_14X14

NUM_LED#: NC

EMC Request

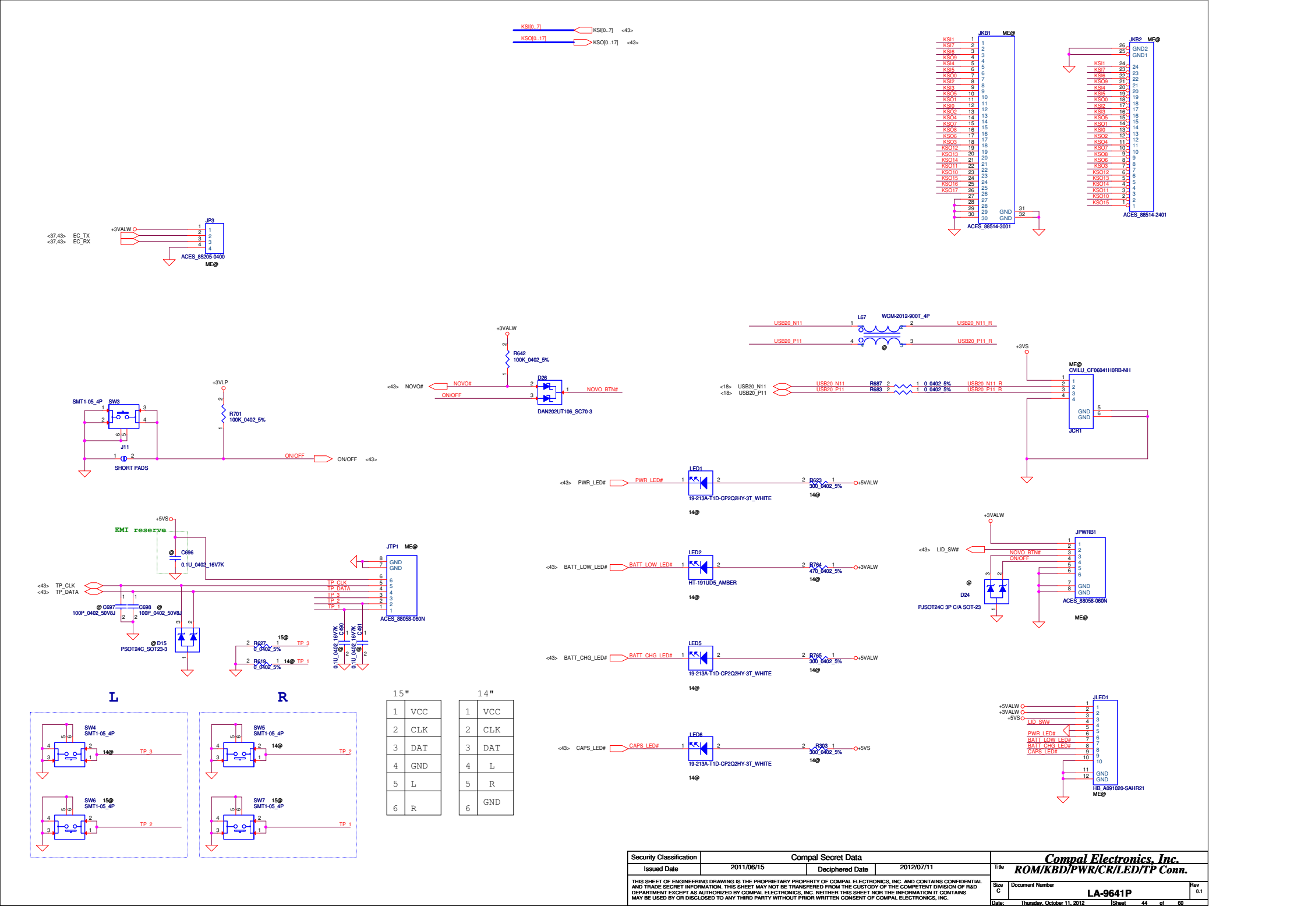
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size: Custom | Document Number: LA-9641P | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 43 of 60



15"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

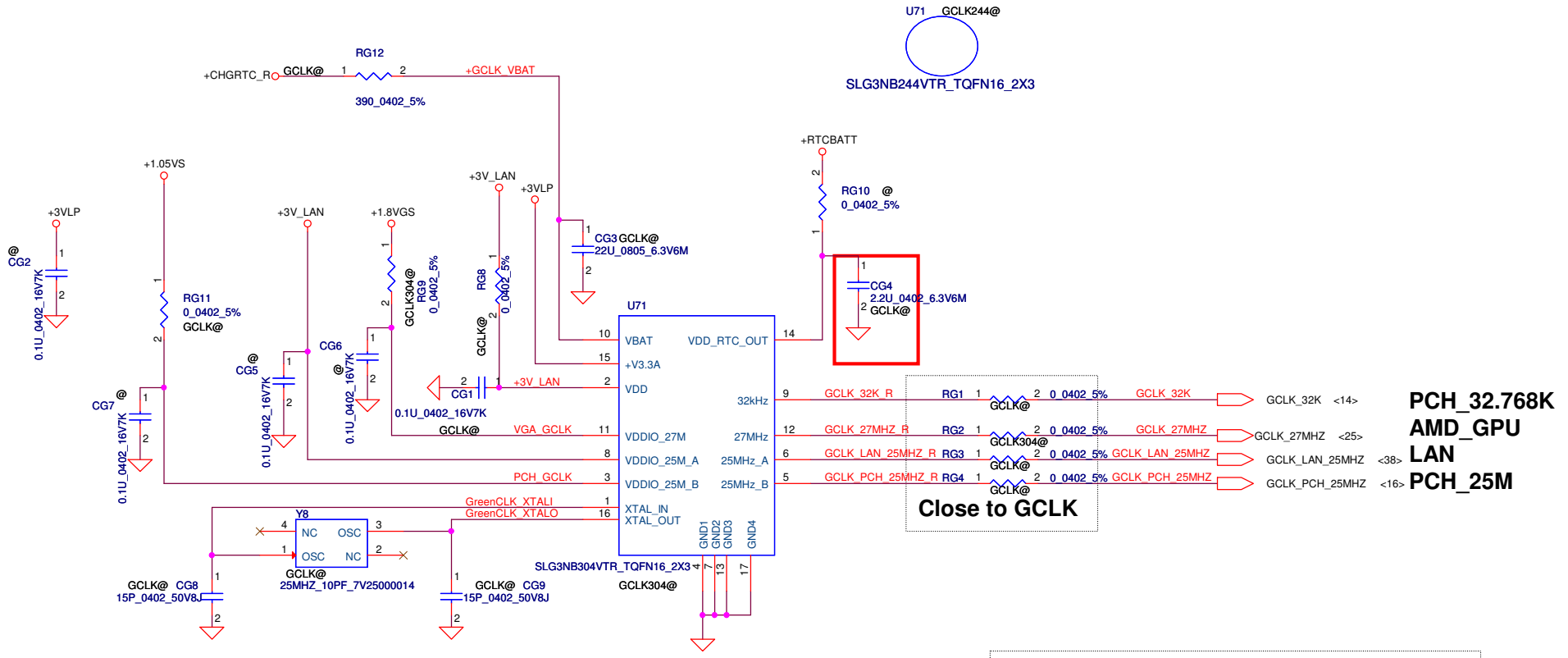
14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA-9641P		Rev 0.1
Date: Thursday, October 11, 2012	Sheet 44 of 60		

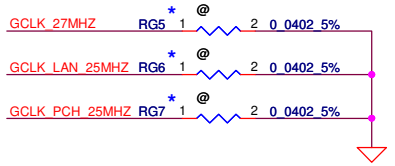
Green Clock

Every power trace need:
W=20mils



PCH_32.768K
AMD_GPU
LAN
PCH_25M

Reserved for Swing Level adjustment (Close GCLK side)



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

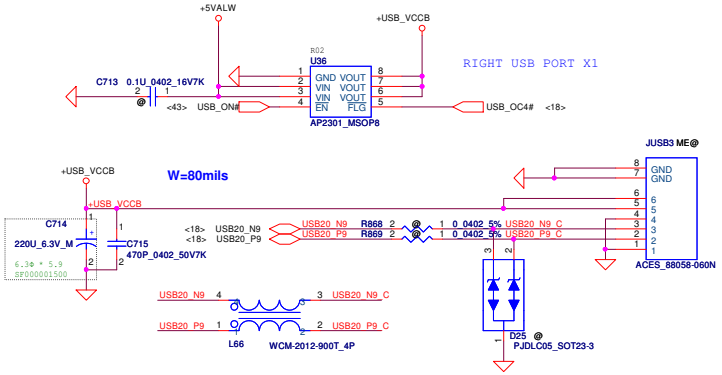
Compal Electronics, Inc.

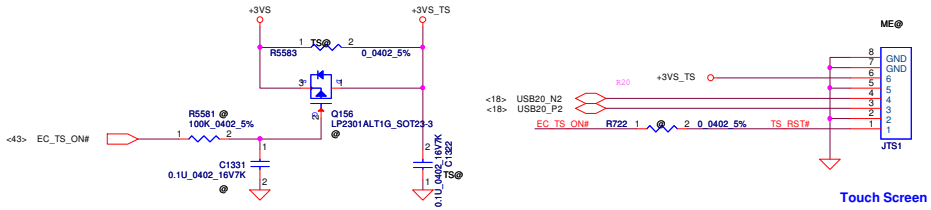
Title: USB ext. ports

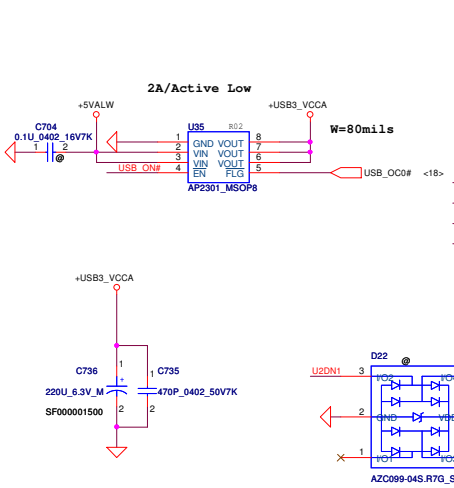
Size	Document Number	Rev
B	LA-9641P	0.1

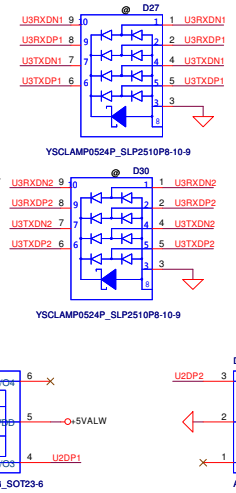
Date: Thursday, October 11, 2012 Sheet 45 of 60

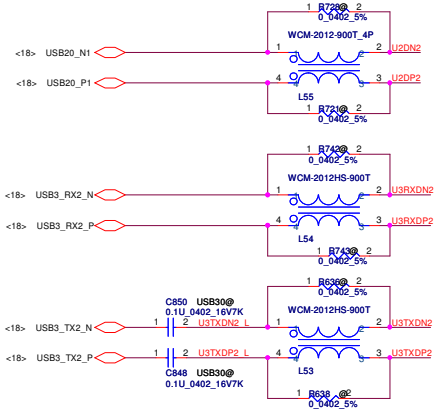
Right Ext.USB Conn.

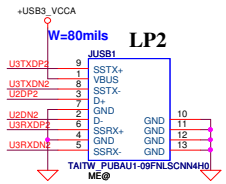


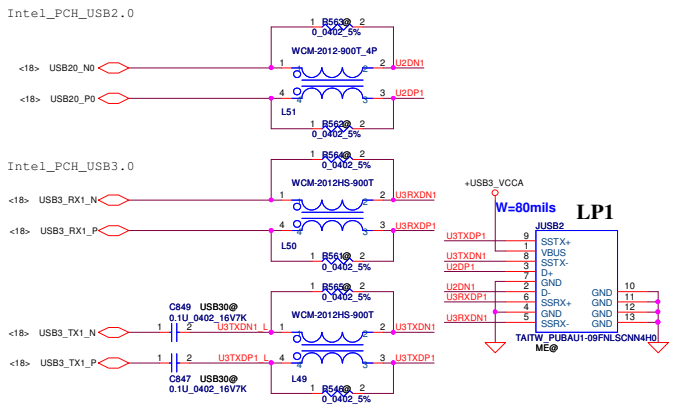












Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

Size	Document Number	Rev
Custom		0.1

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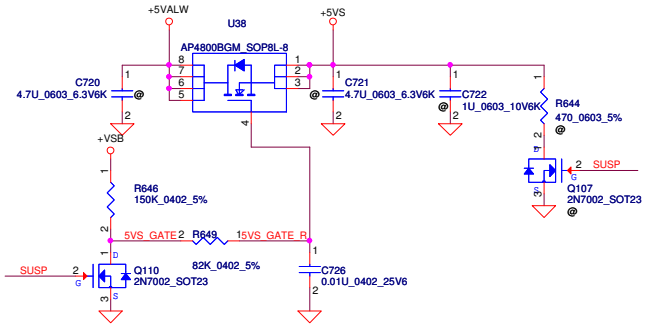
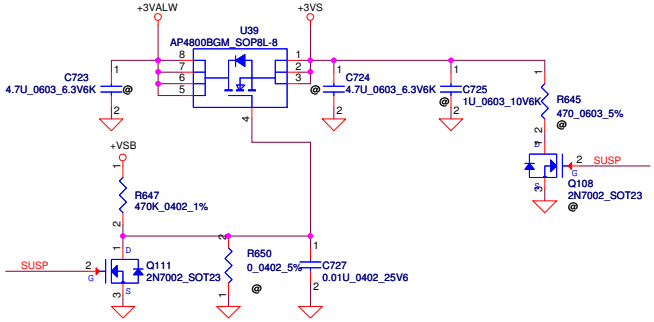
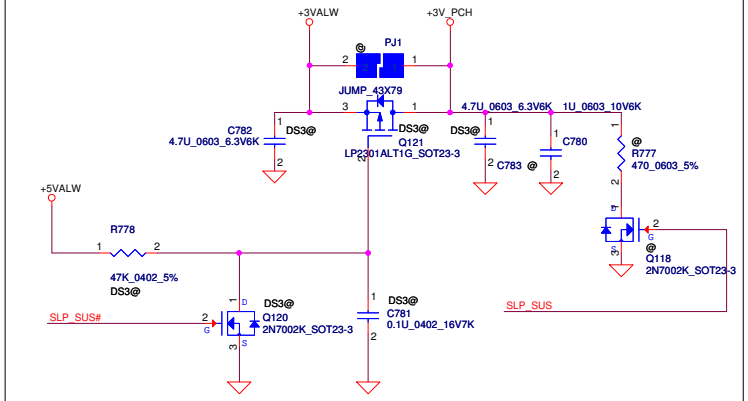
+5VALW TO +5VS

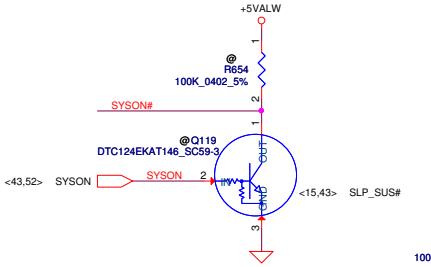


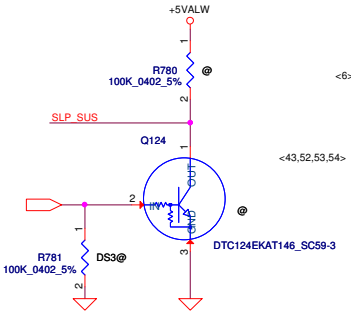
+3VALW TO +3VS

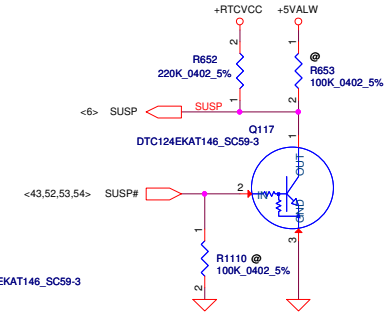


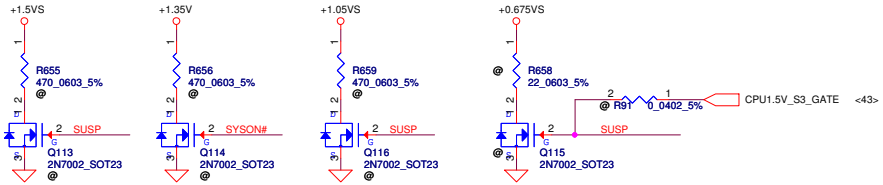
+3VALW TO +3VALW(PCH AUX Power)











Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-9641P	0.1

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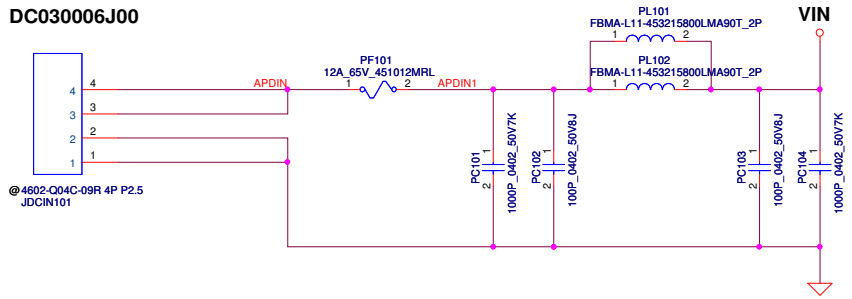
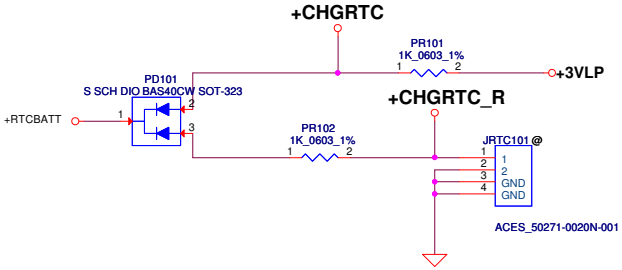
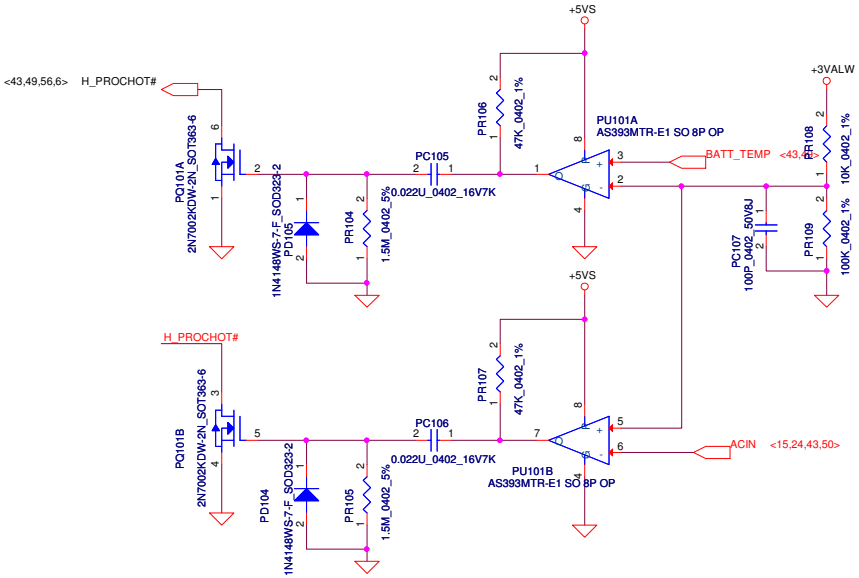




RTC Battery



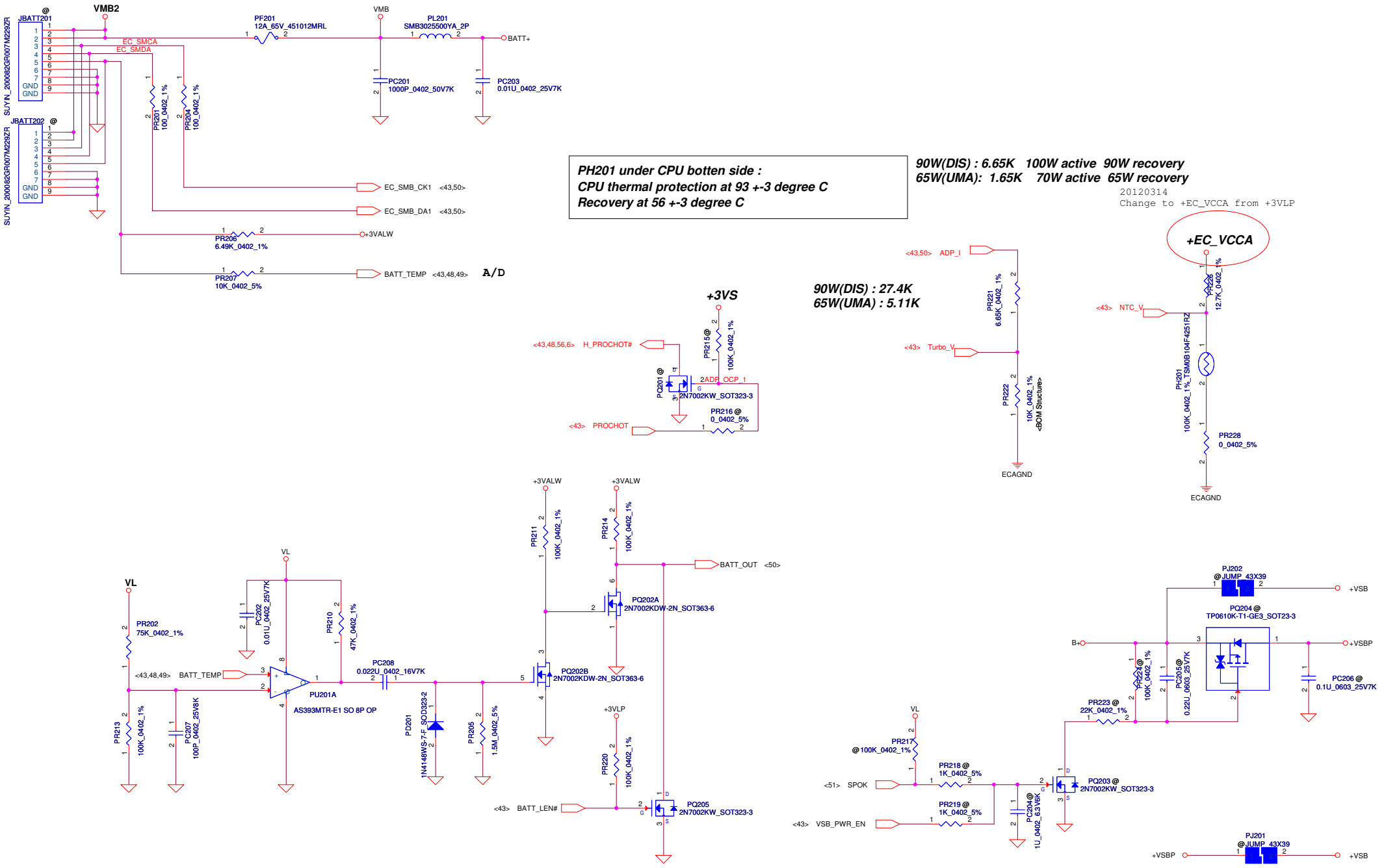
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: Gx00 | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 48 of 59



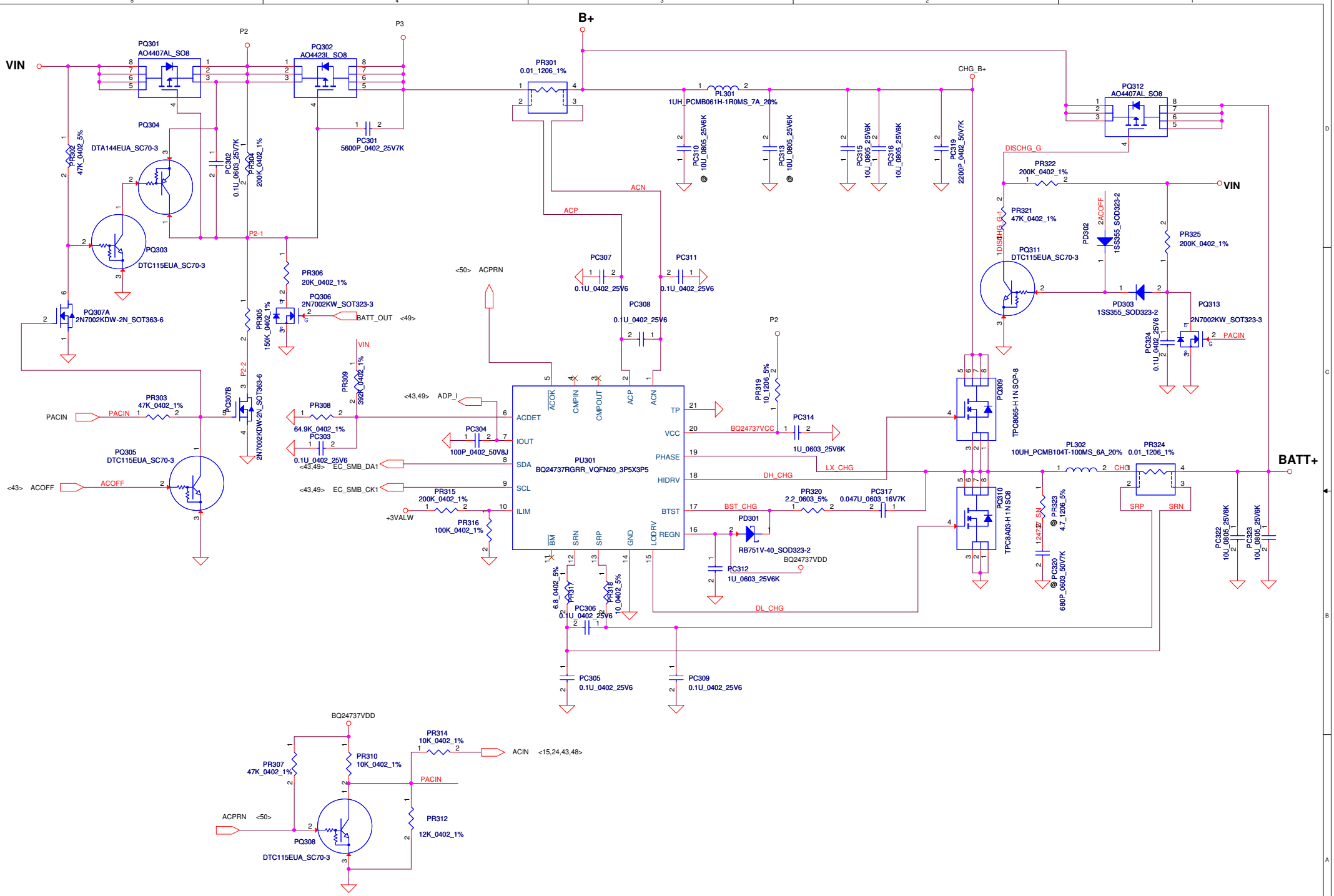
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	Gx00	0.1

Date: Thursday, October 11, 2012 Sheet 49 of 59



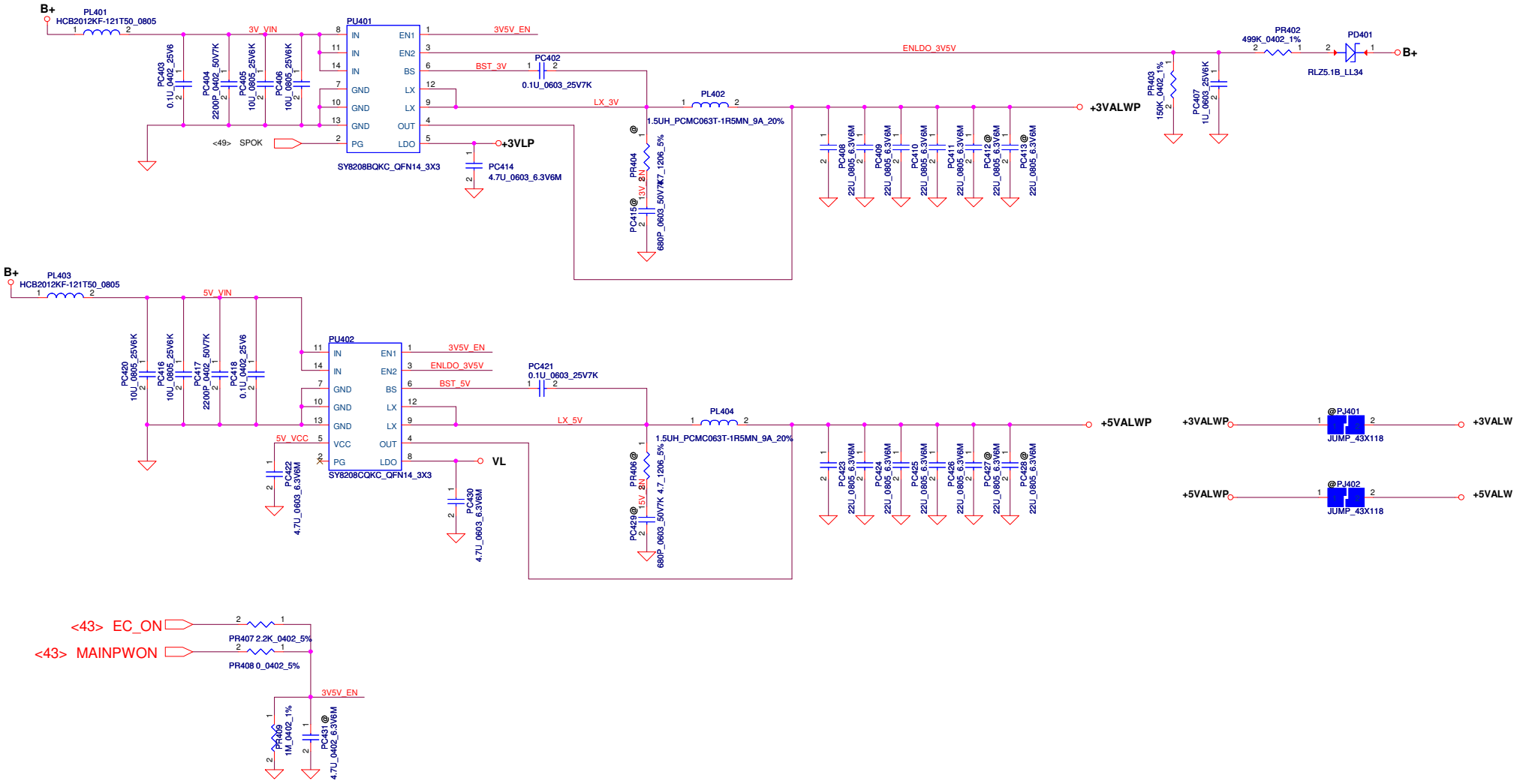
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CHARGER-BQ24737

Size	Document Number	Rev
	Gx00	0.1

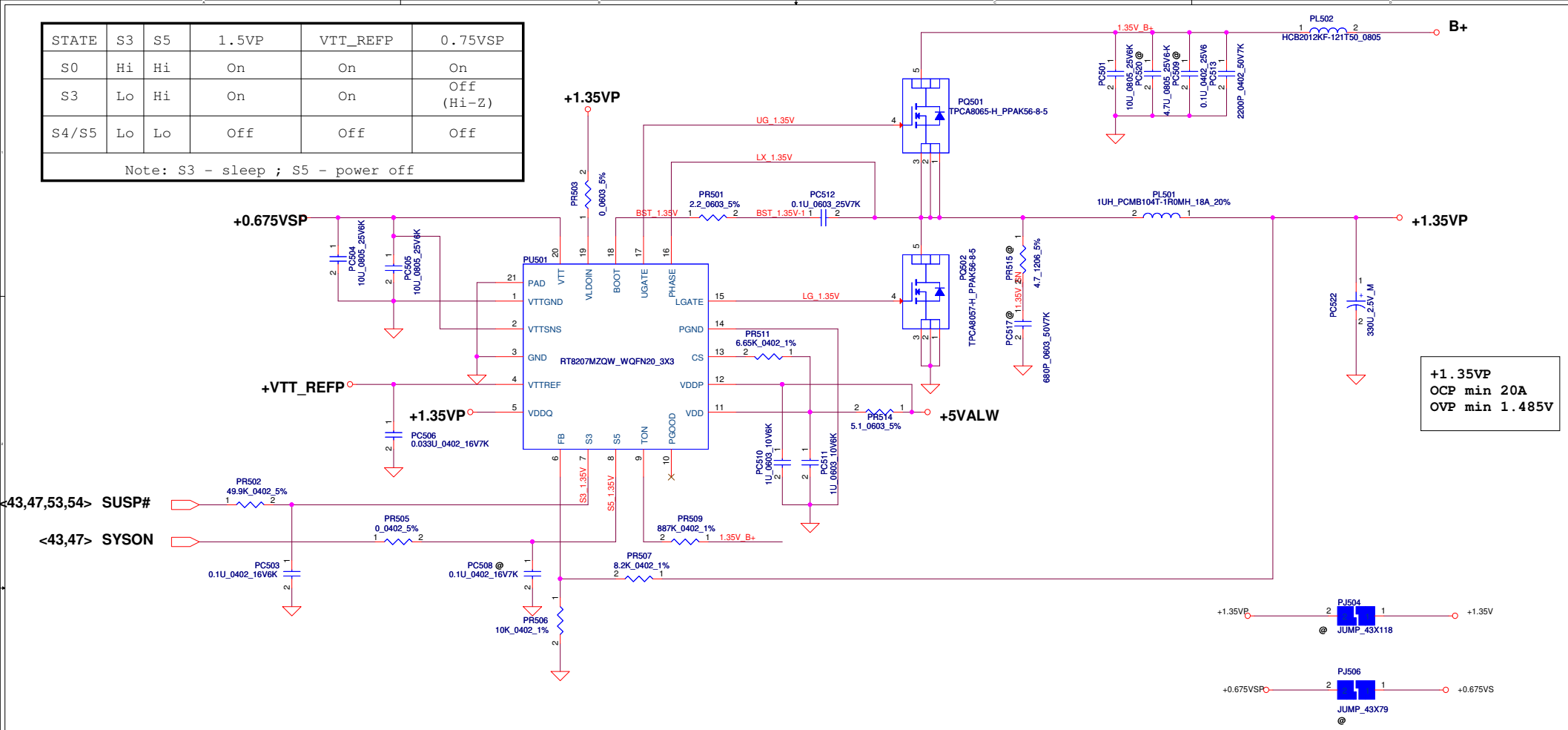
Date: Thursday, October 11, 2012 | Sheet 50 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title: PWR- 3VALWP/5VALWP			
Size: Custom	Document Number: Gx00		Rev: 0.1
Date: Thursday, October 11, 2012	Sheet 51 of 12		

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



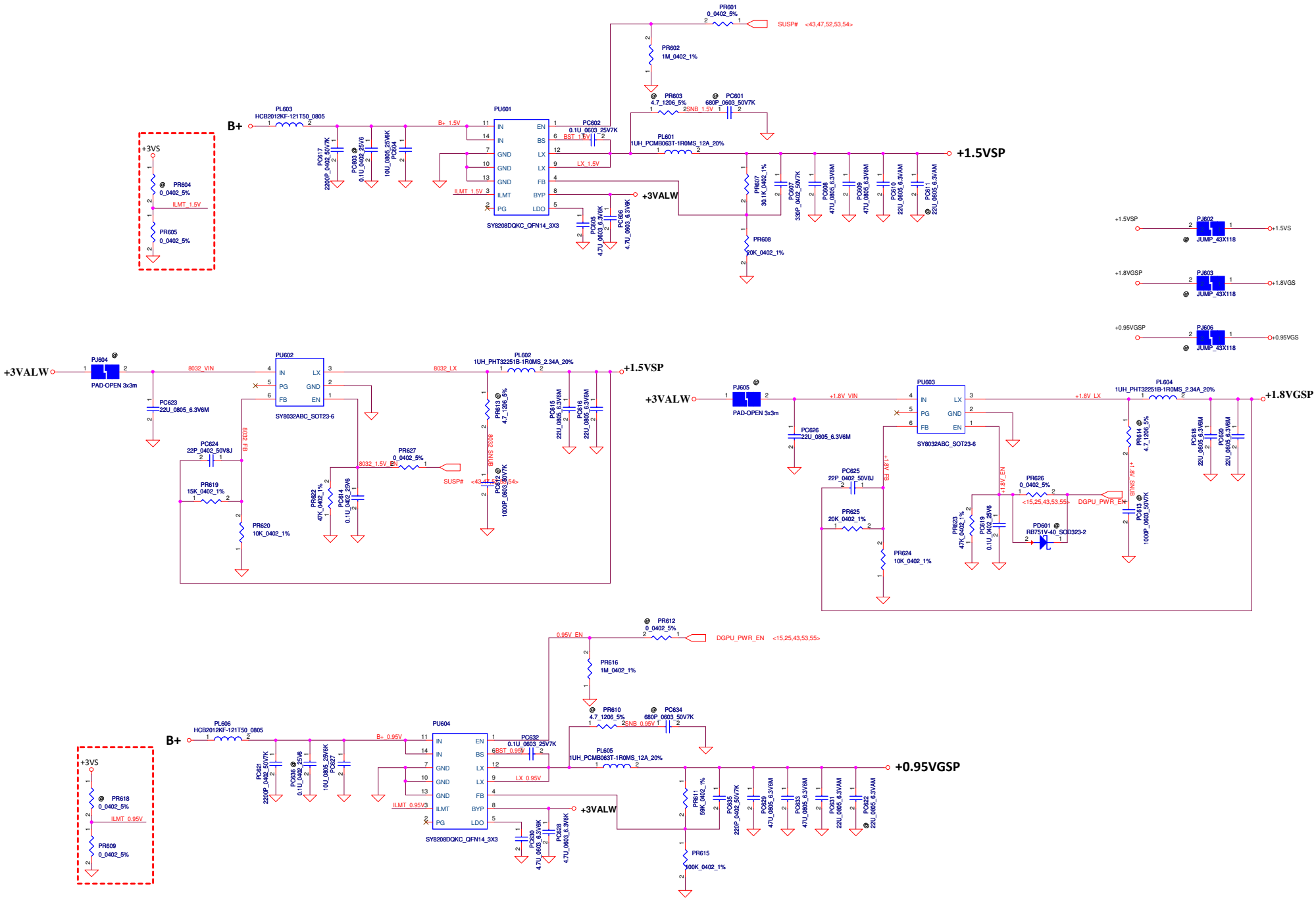
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.35V_DDR

Size: Custom | Document Number: Gx00 | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 52 of 59



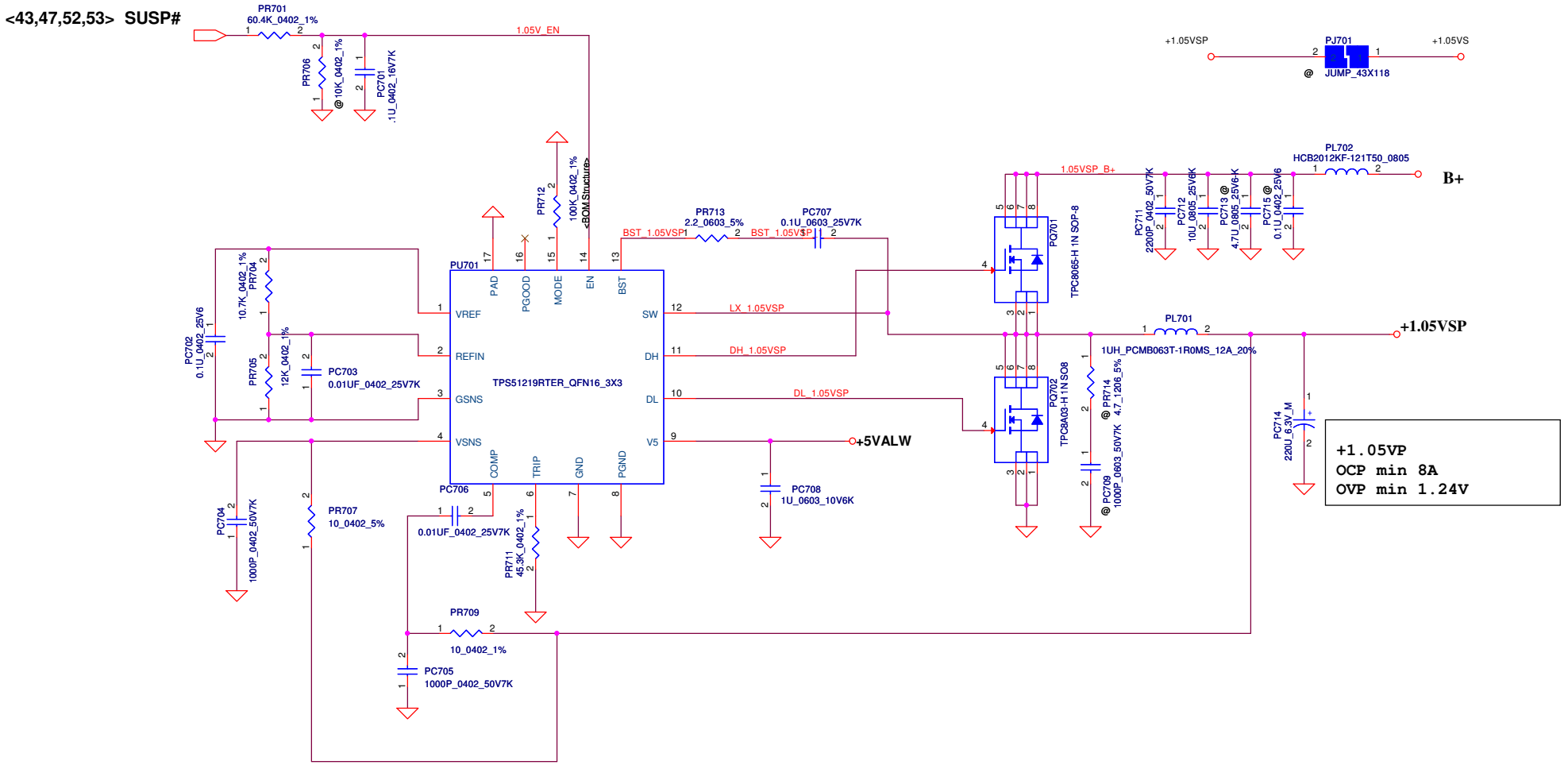
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: 1.5V_VRAM/1.8V/0.95V

Size	Document Number	Rev
C	Gx00	0.1

Date: Thursday, October 11, 2012 Sheet 53 of 59



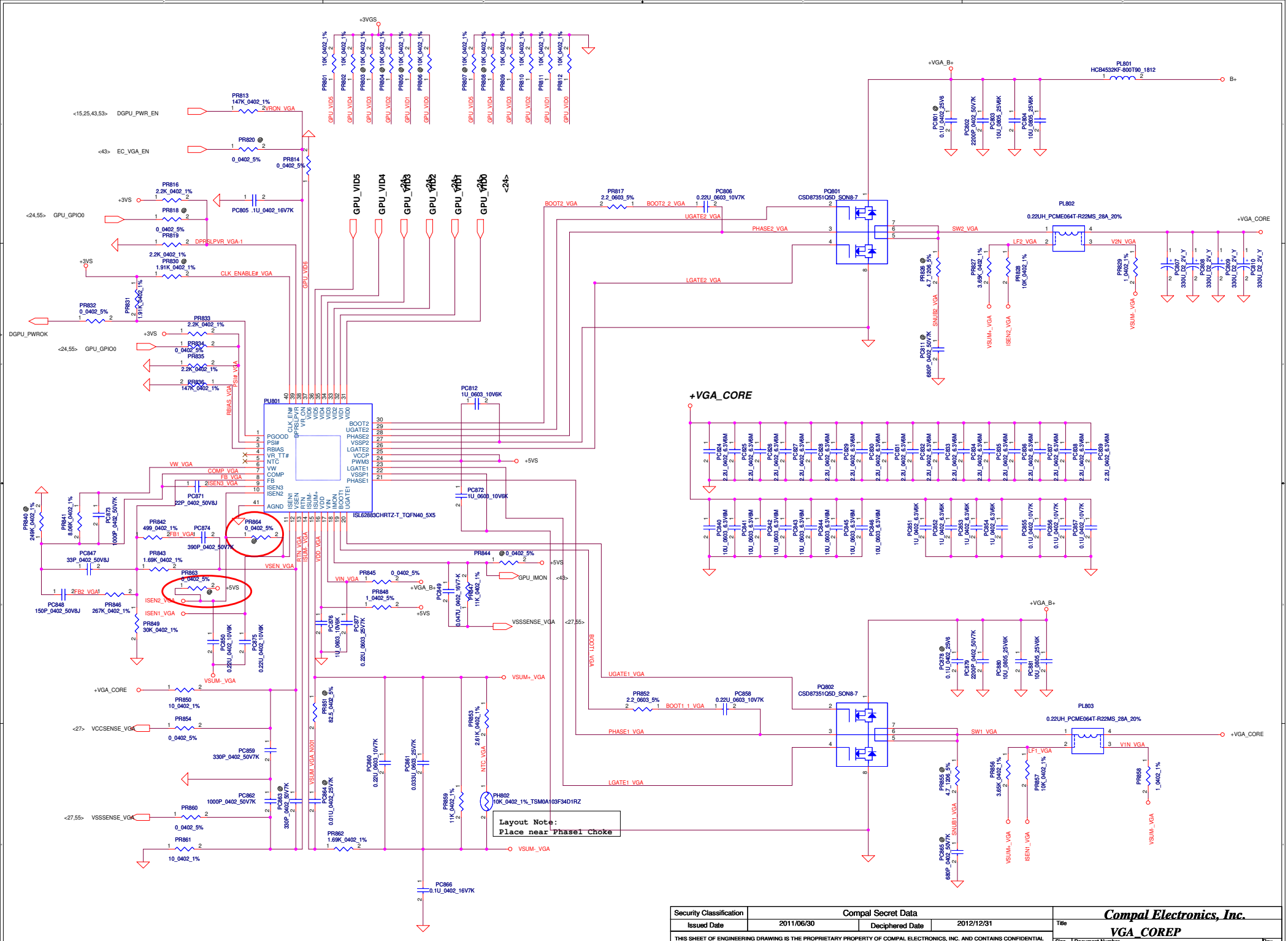
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.05VS

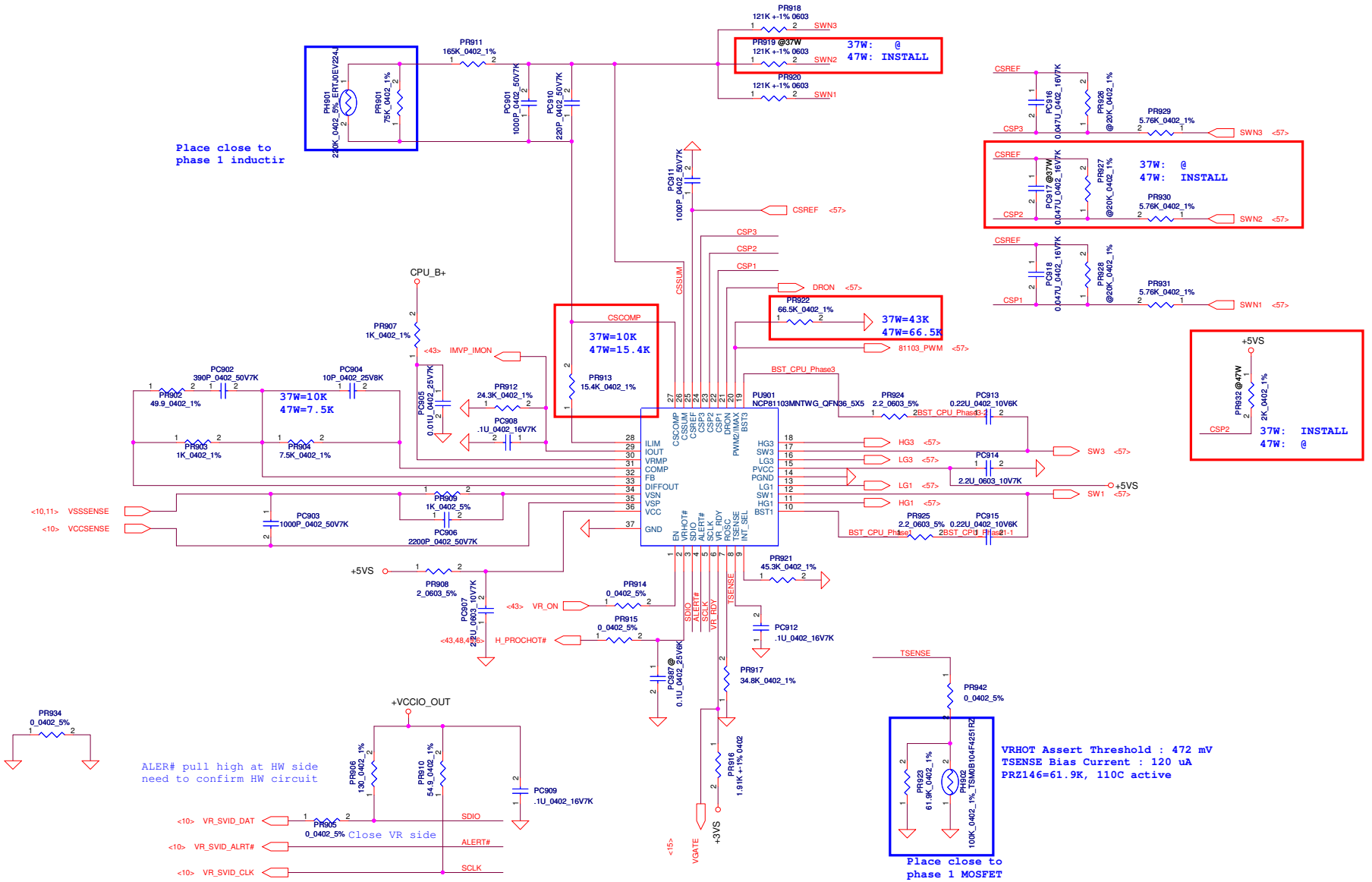
Size	Document Number	Rev
Custom	Gx00	0.1

Date: Thursday, October 11, 2012 Sheet 54 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: VGA_COREP			
Size	Document Number: Gx00		Rev: 0.1
Date: Thursday, October 11, 2012		Sheet 55 of 59	



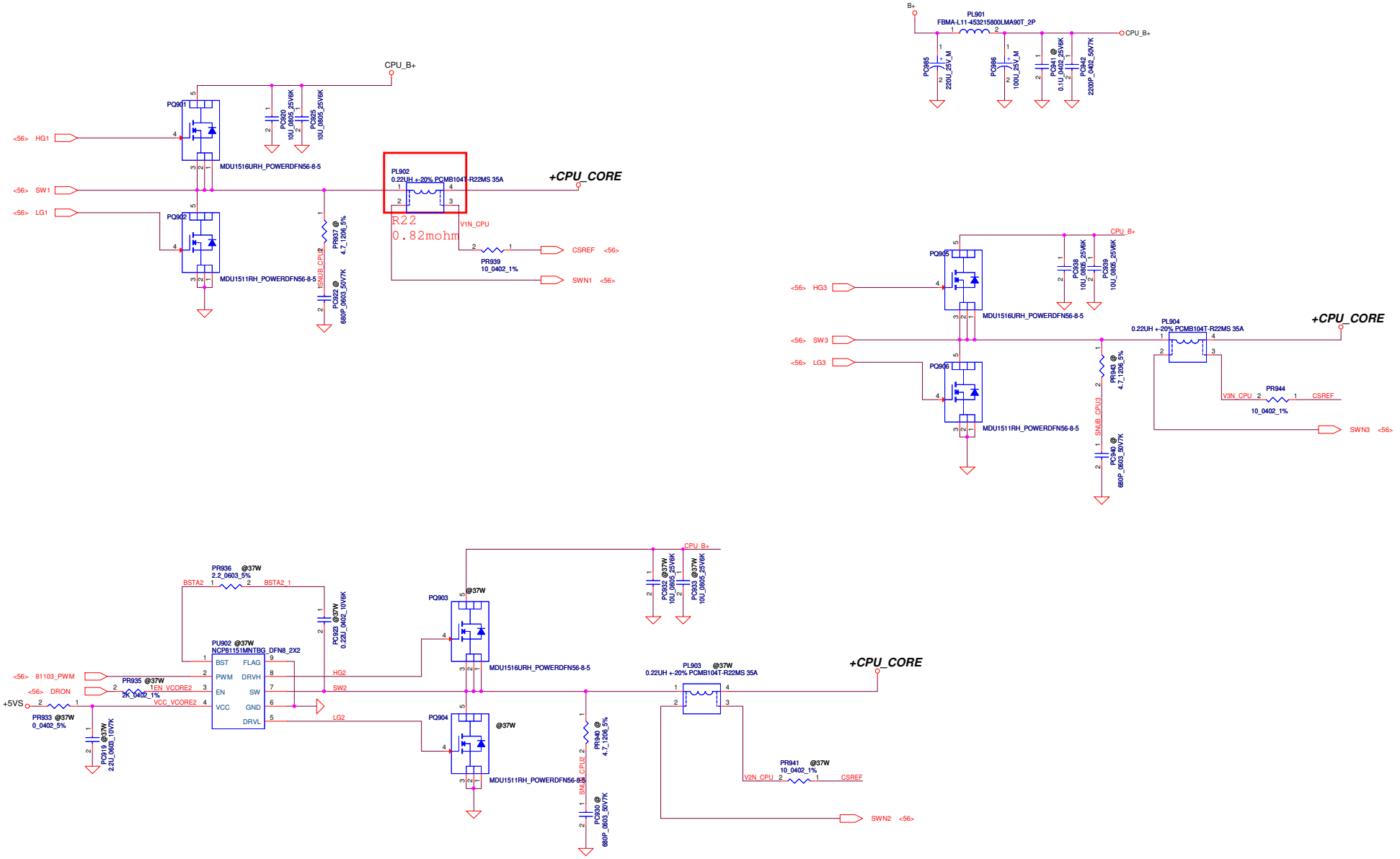
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE1

Size	Document Number	Rev
Custom	Gx00	0.1

Date: Thursday, October 11, 2012 Sheet 56 of 59

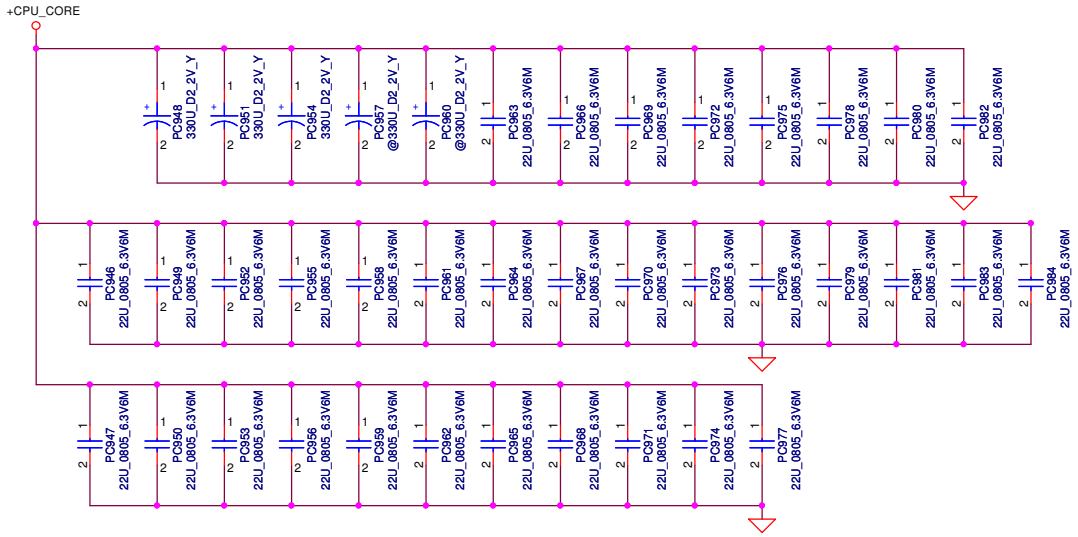


Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	CPU_CORE2		
Size C	Document Number Gx00		Rev 0.1
Date: Thursday, October 11, 2012		Sheet 57 of 59	

+CPU_CORE

3 X 330u/9m(47W)　　2X330u/9m(37W)
34 X 22u/0805　　34 X 22u/0805



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: **Gx00** | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 58 of 59

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: Zx90 | Rev: 0.1

Date: Thursday, October 11, 2012 | Sheet 59 of 12