Intel BayTrail-D Platform

Date : 2013/12/27
Version 1.0

Compal Confidential

ZAA00(C260) LA-B001P Schematics Document

Intel BayTrail-D Platform

AIO M/B

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/01/03	Deciphered Date	2014/01/03	Title: Cover Page

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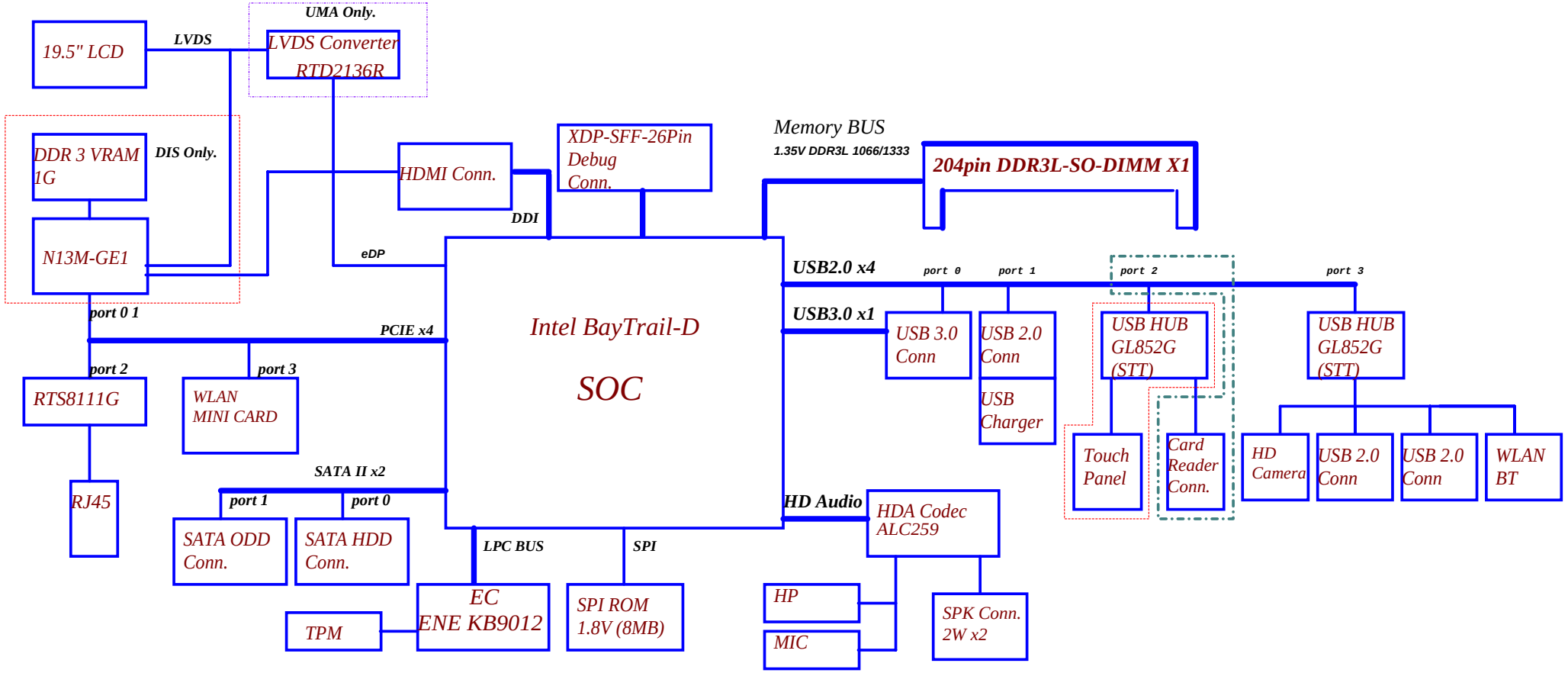

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Title	Block Diagrams		
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1) SO-DIMM B (JDIMM2)	A0h A2h

Board ID / SKU ID Table for AD channel

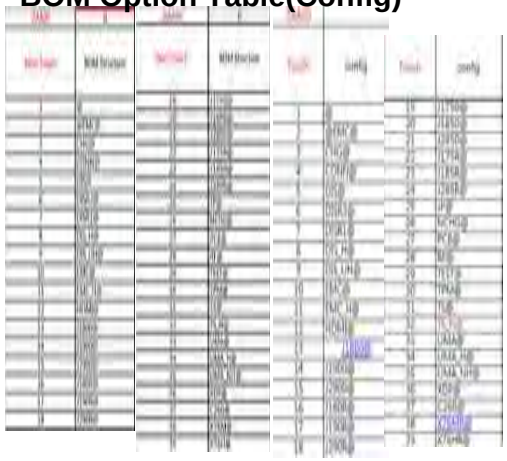
Vcc	3.3V +/- 5%
R280	100K +/- 5%

Board ID	R281	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0.1	0	0 V	0 V	0 V
0.2	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
0.3	18K +/- 5%	0.436 V	0.503 V	0.538 V
1.0	33K +/- 5%	0.712 V	0.819 V	0.875 V
	56K +/- 5%	1.036 V	1.185 V	1.264 V
	100K +/- 5%	1.453 V	1.650 V	1.759 V
	200K +/- 5%	1.935 V	2.200 V	2.341 V
	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0.1	R281=0 Ohm; R280 open
0.2	R281=8.2K Ohm; R280 100K Ohm
0.3	R281=18K Ohm; R280 100K Ohm
1.0	R281=33K Ohm; R280 100K Ohm

BOM Option Table(Config)



UMA/DIS ID Table

	0(DIS)	1(UMA)	
AD_PID1	R297=10K Ohm ; R298 open	R297 open ; R298=10K Ohm	
UD	R330 = 10K Ohm; R299 open	R330 open ; R299 10K Ohm	

43 level BOM table

43 Level	Description	BOM Structure
4319RF38L01~20	ZAA00	None Touch SKU
4319RF38L30~50	ZAA20	Touch SKU

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Title: Notes List

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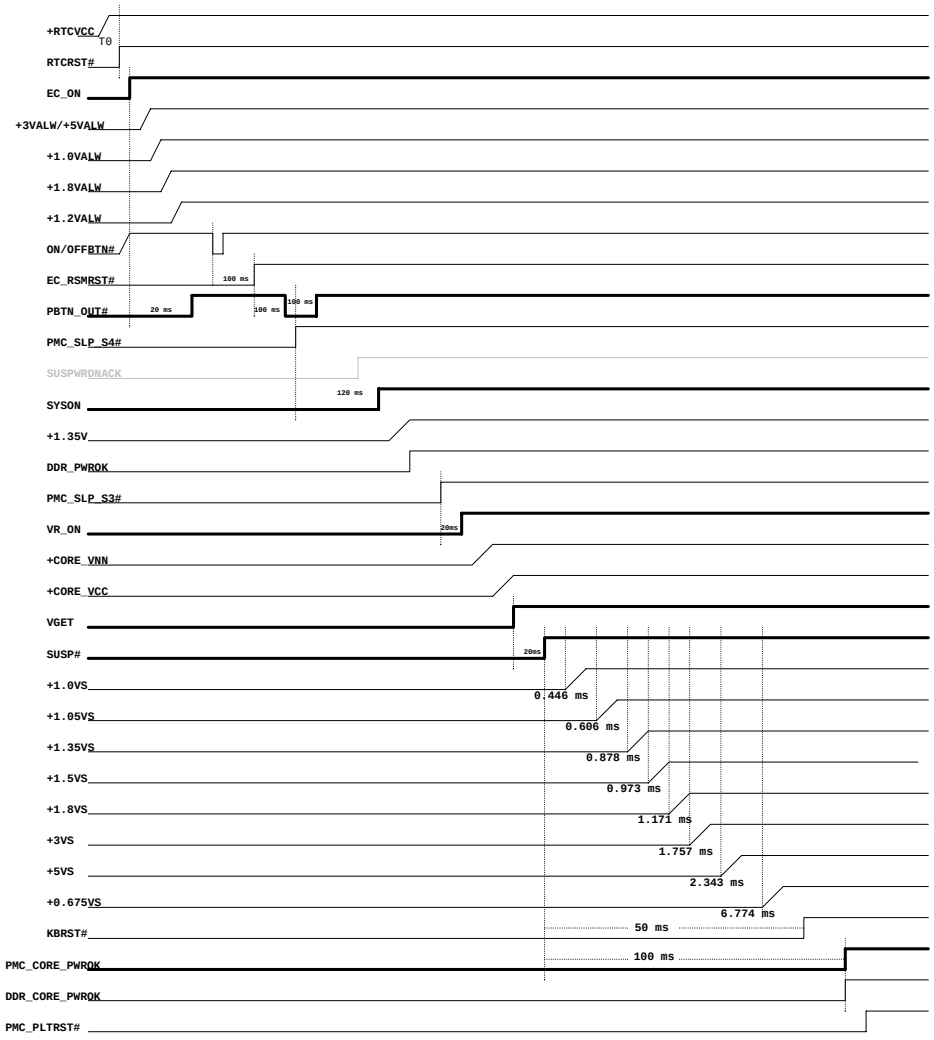
Power ON



T0: +RTCVCC stable to RTCRST# high > 9ms
T1: VR ramp up time from 10% to 90% voltage level < 2ms
T2 :Rail to subsequent rail turn on delay < 2ms
T3 :+VALWAS stable to EC_RSMRST# high > 10ms
T4 :+VS rails stable to PMC_CORE_PWROK > TBD

NOTE:
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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Title = Power Sequence	Title: Power Sequence	
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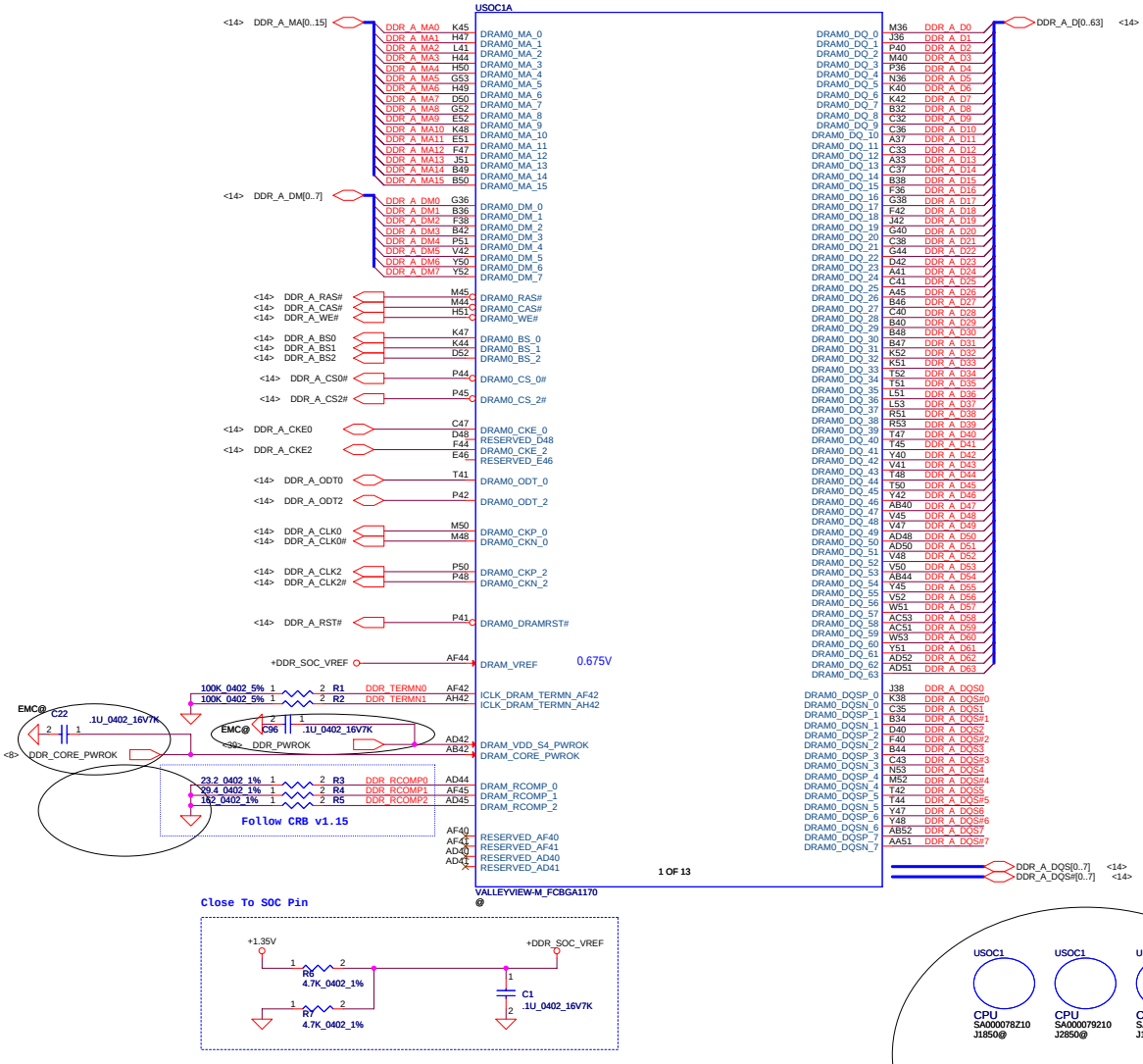
PCB

ZZZ1

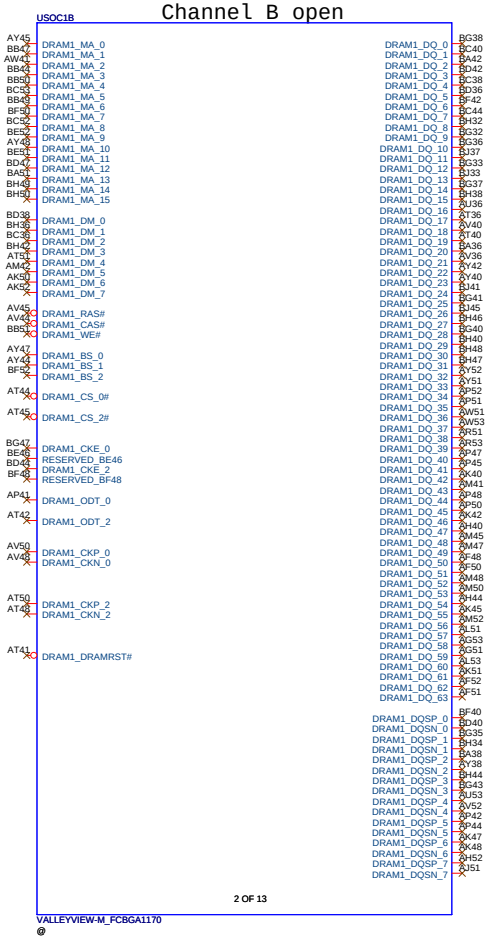
LA-B001P
DAZ14000101
PCB@

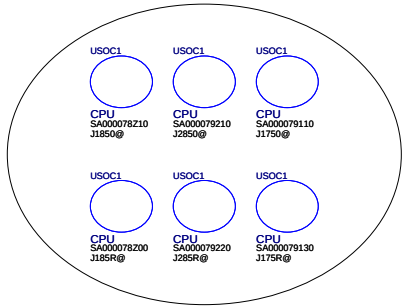
Channel A Only

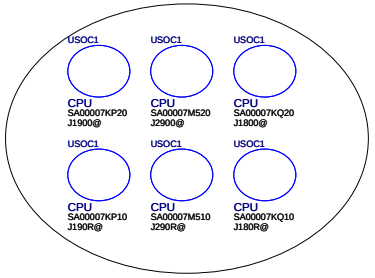


Close To SOC Pin

Channel B open







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Compal Electronics, Inc.			
Title	BayTrail-D Memory DDR3L		
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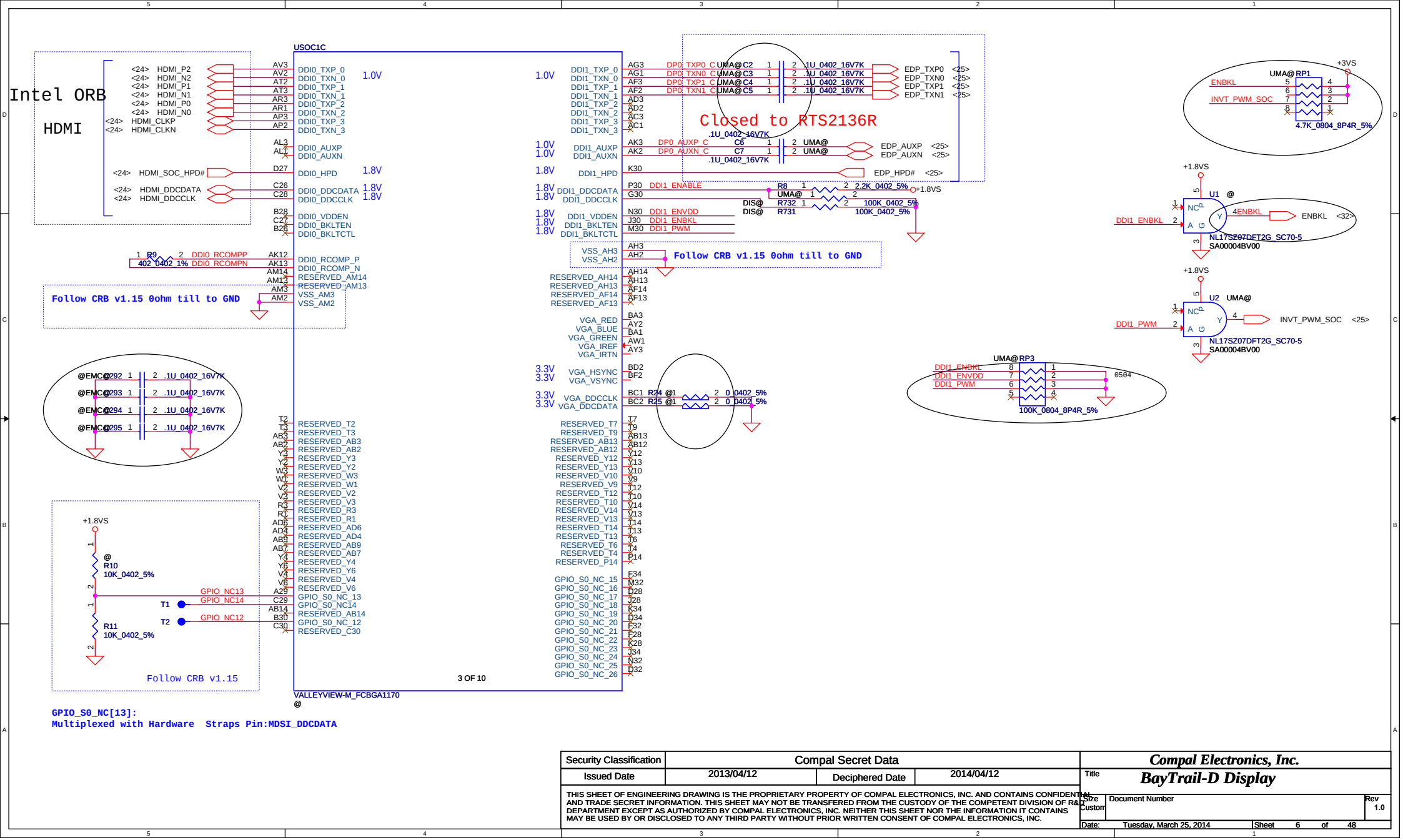

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Compal Electronics, Inc.			
Title: BayTrail-D Display			
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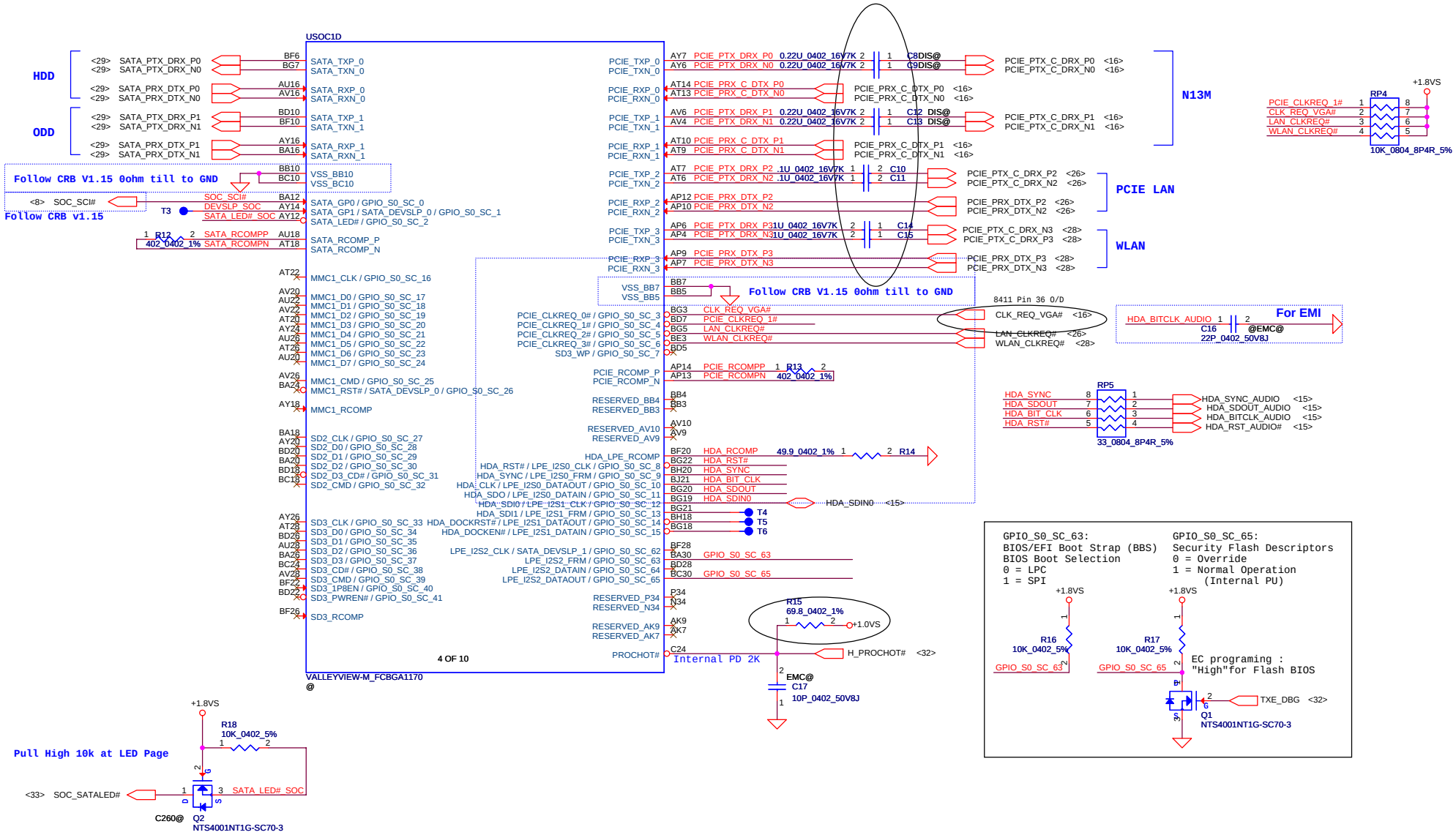

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Compal Electronics, Inc.

Title: **BayTrail-D SATA/PCI-E/HDA**

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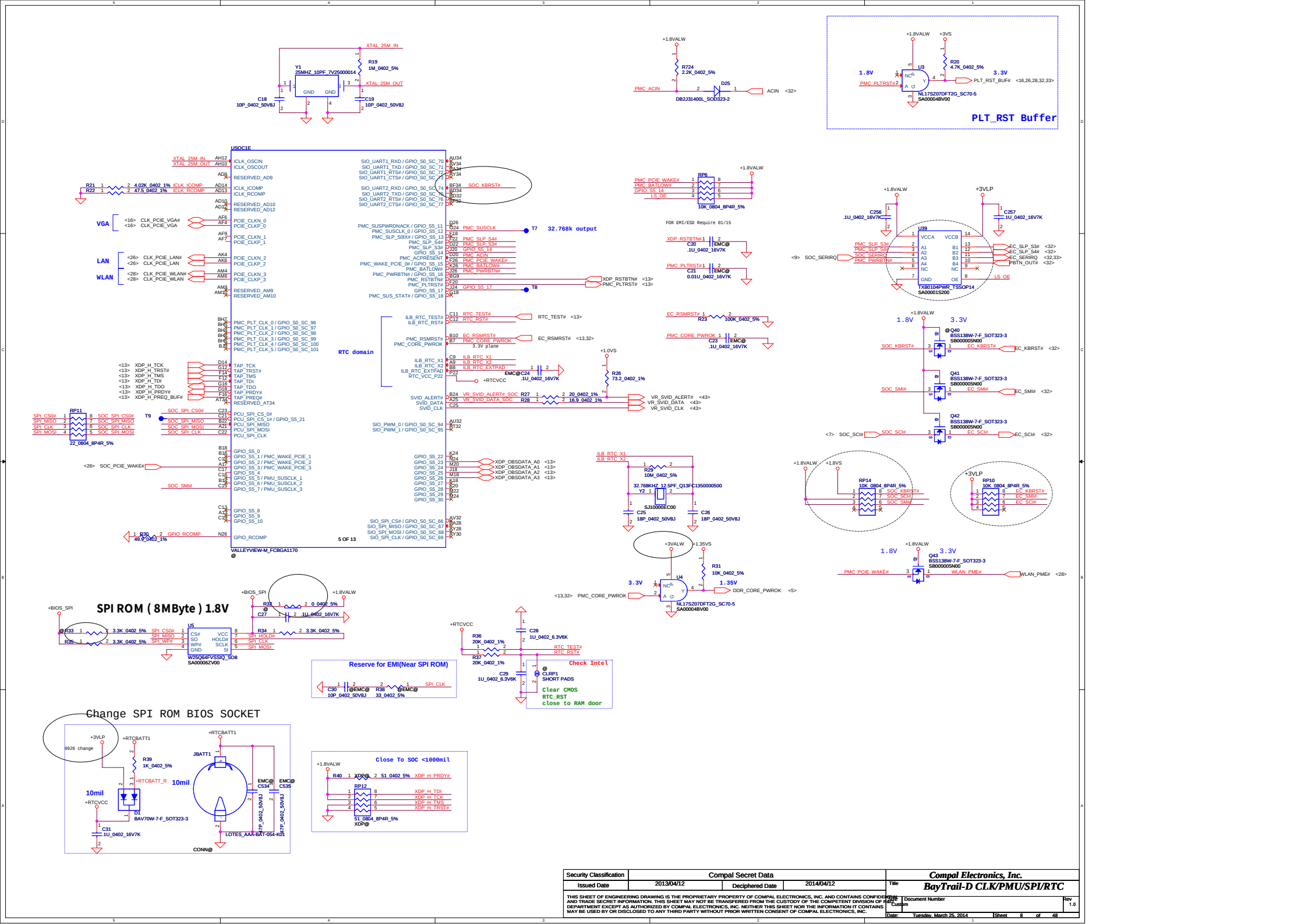
PLT_RST Buffer
SPI ROM (8MByte) 1.8V
Change SPI ROM BIOS SOCKET
Reserve for EMI(Near SPI ROM)
Close To SOC <1000mil
Check Intel
Clear CMOS
RTC_RST
close to RAM door
32.768k output
VALLEYVIEW-M_FCBGA1170
RTC domain
5 OF 13
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BayTrail-D CLK/PMU/SPI/RTC
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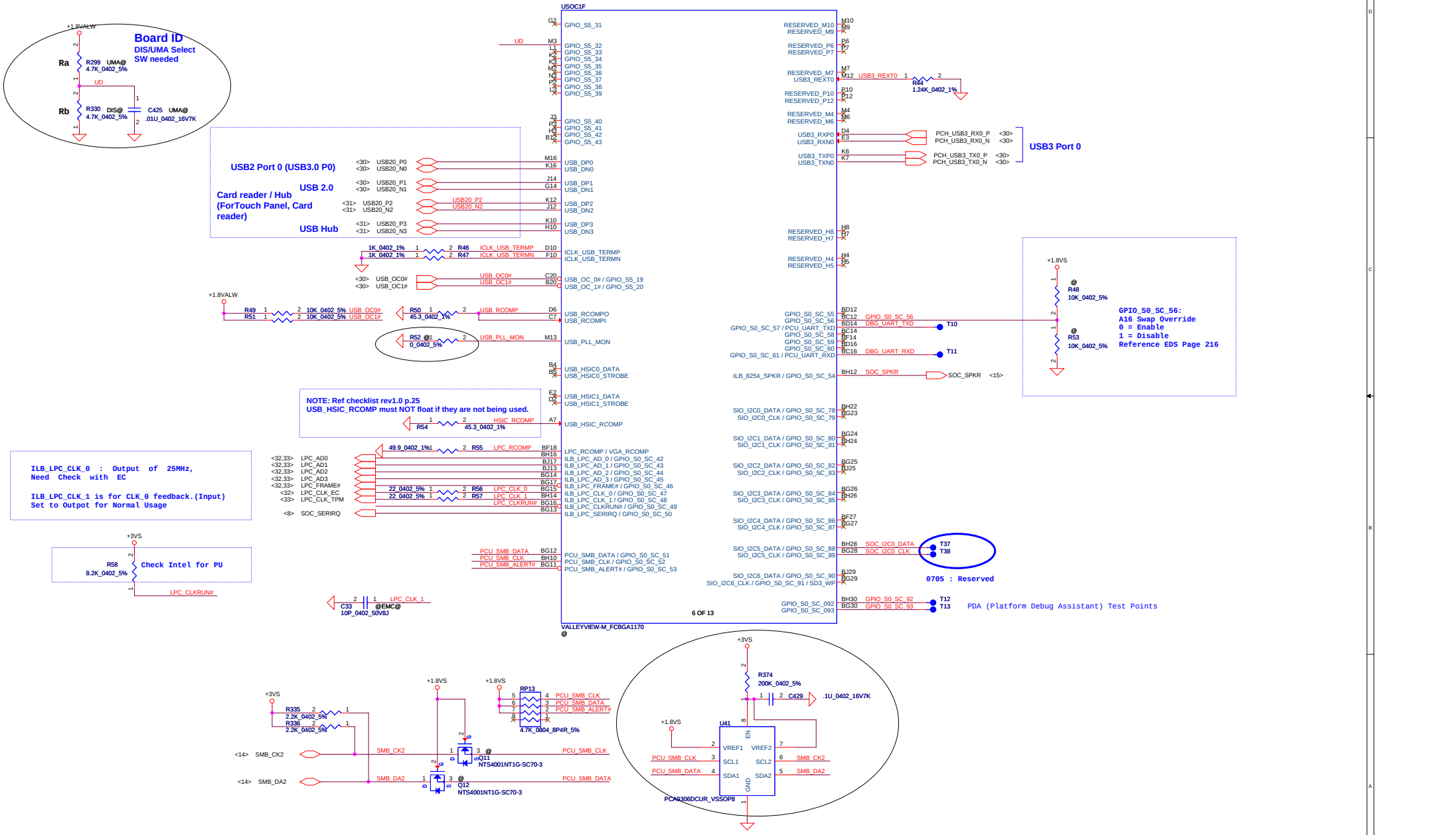

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Title	BayTrail-D USB/LPC/SMBus		
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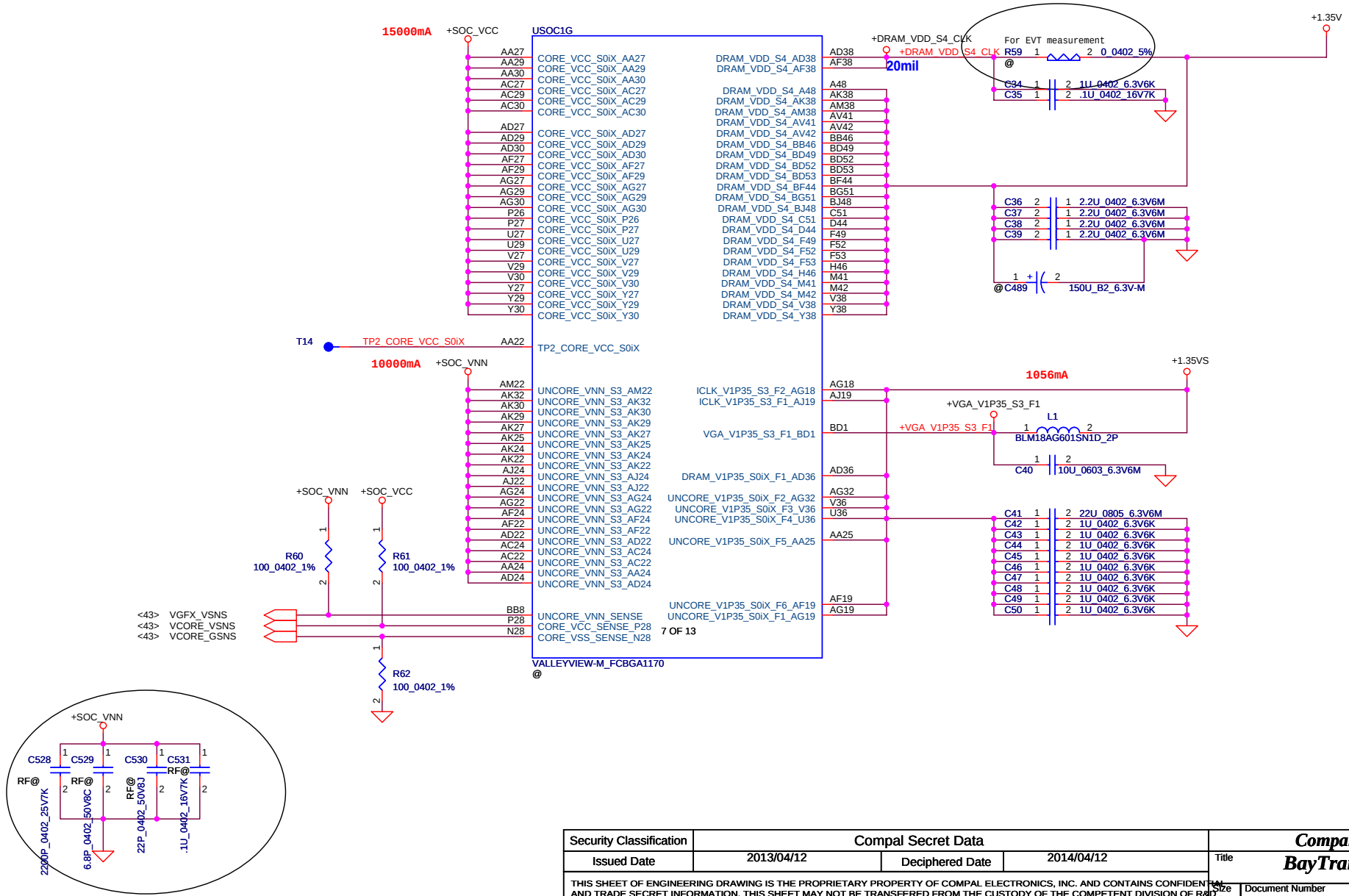

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Compal Electronics, Inc.

Title: **BayTrail-D Power1**

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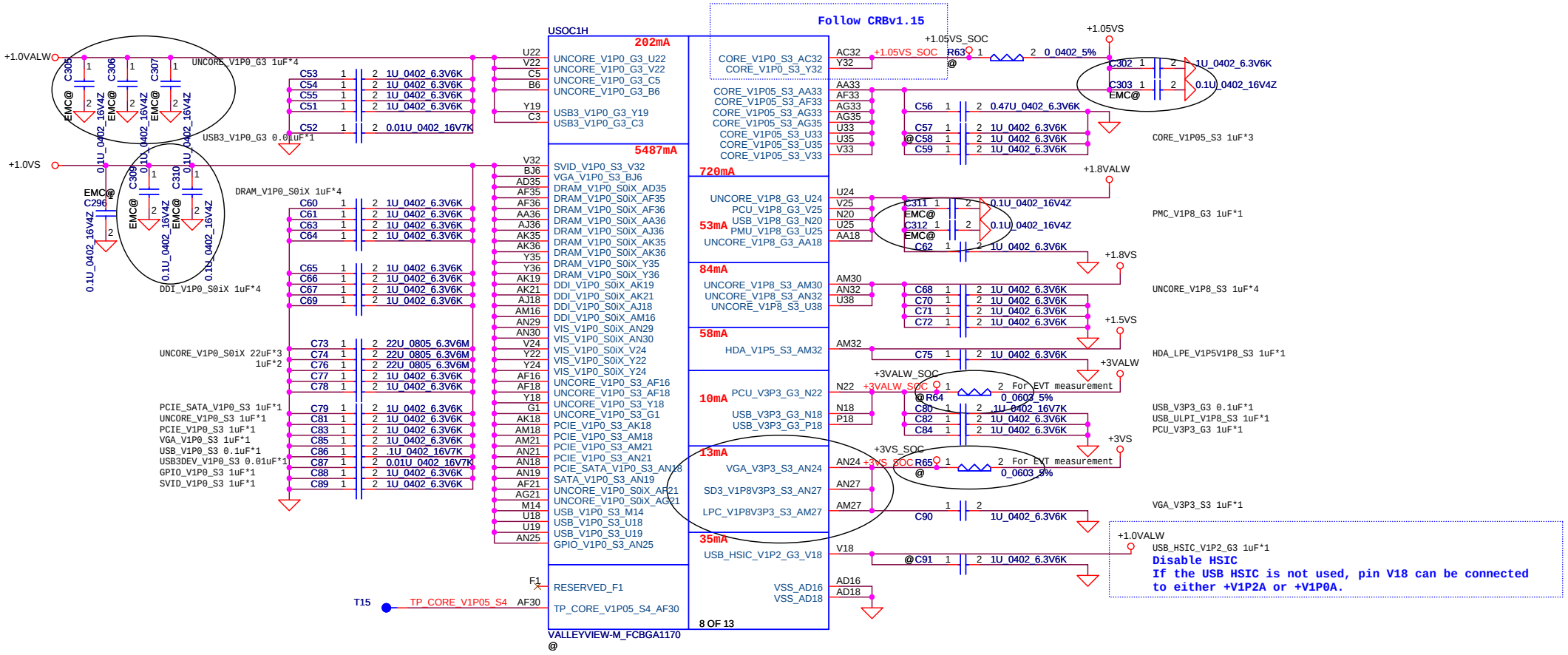

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Title: **BayTrail-D Power2**

Size	Document Number	Rev
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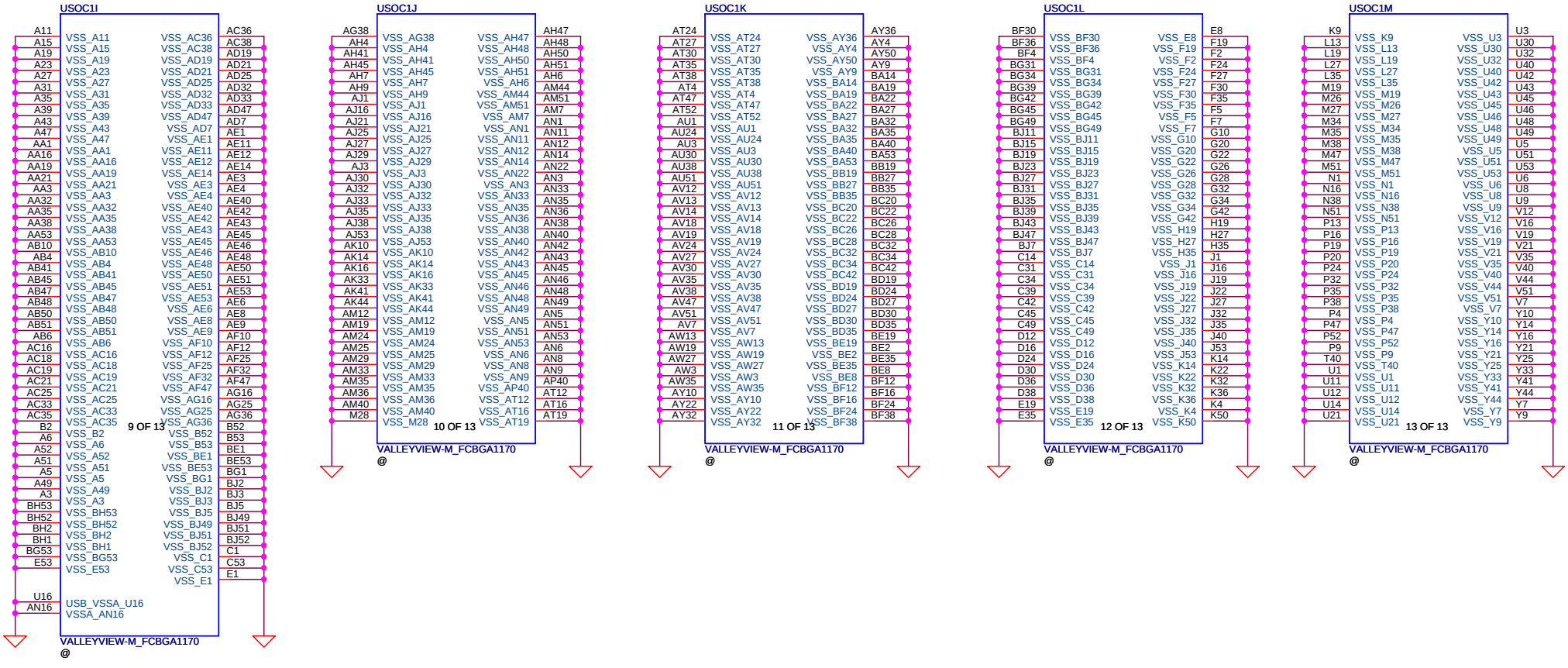

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Title: **BayTrail-D GND**

Size: B	Document Number	Rev: 1.0
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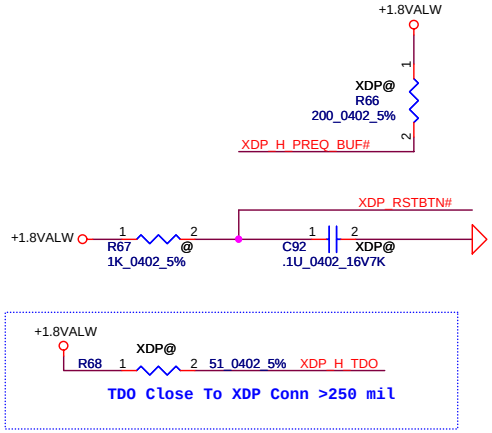
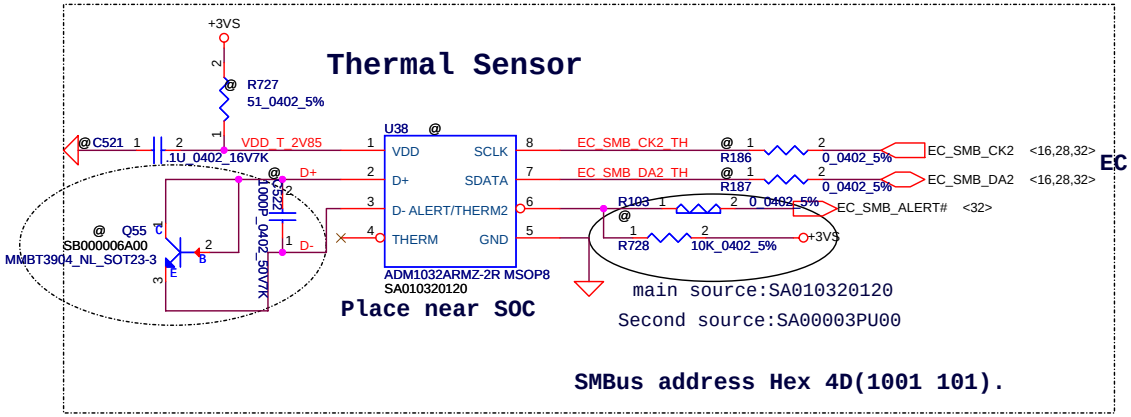
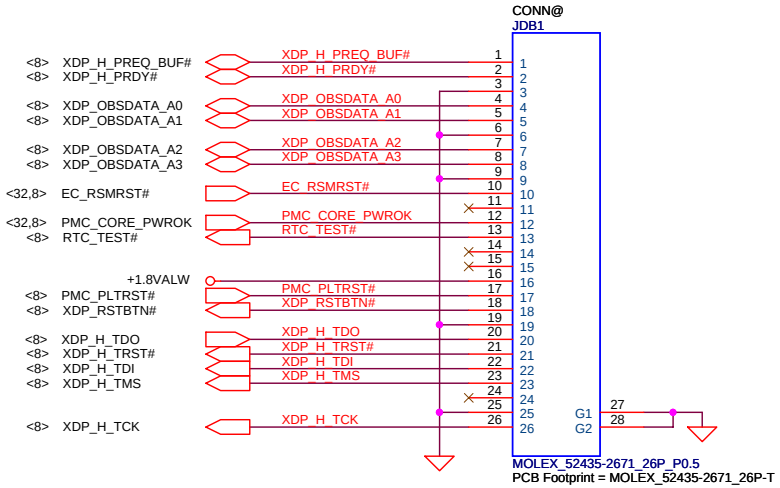




XDP-SFF-26Pin



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Title: BayTrail-D Debug			
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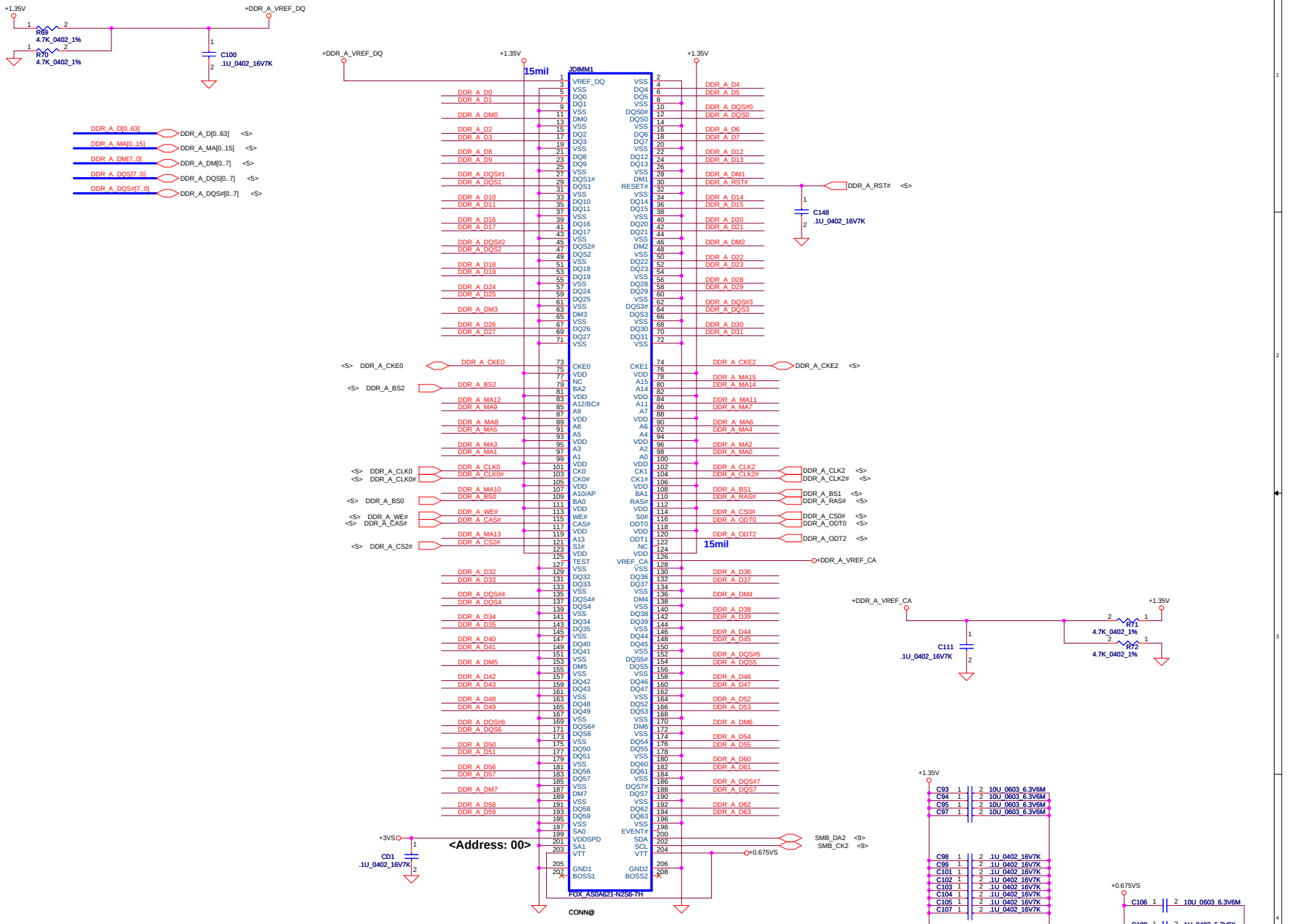
Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.



DIMM_A H:4mm Reverse--> STD 0809

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Title: DDR3L DIMMA			
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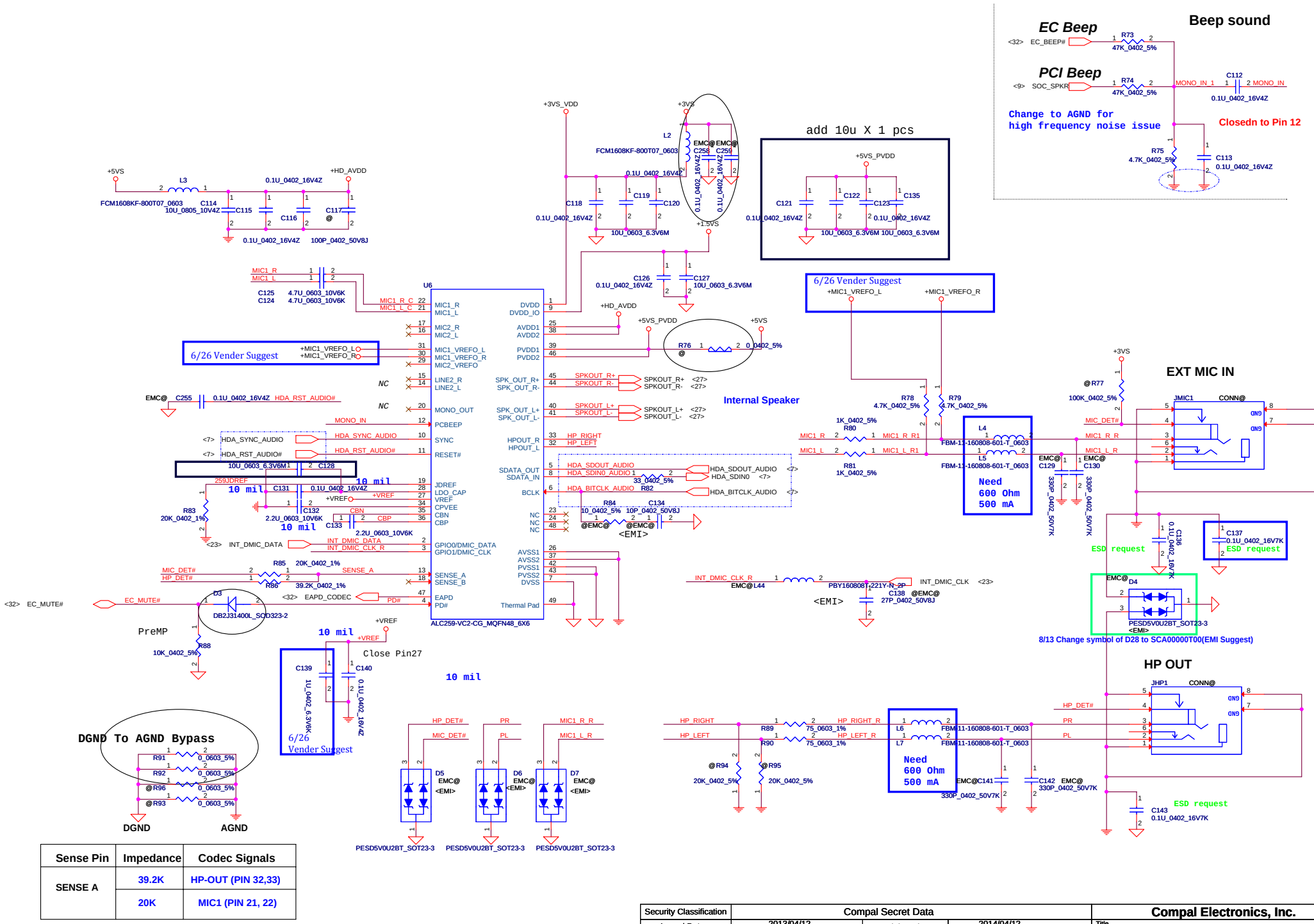

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	HP-OUT (PIN 32,33)
	20K	MIC1 (PIN 21, 22)

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Title: HDA-ALC259/HP/MIC

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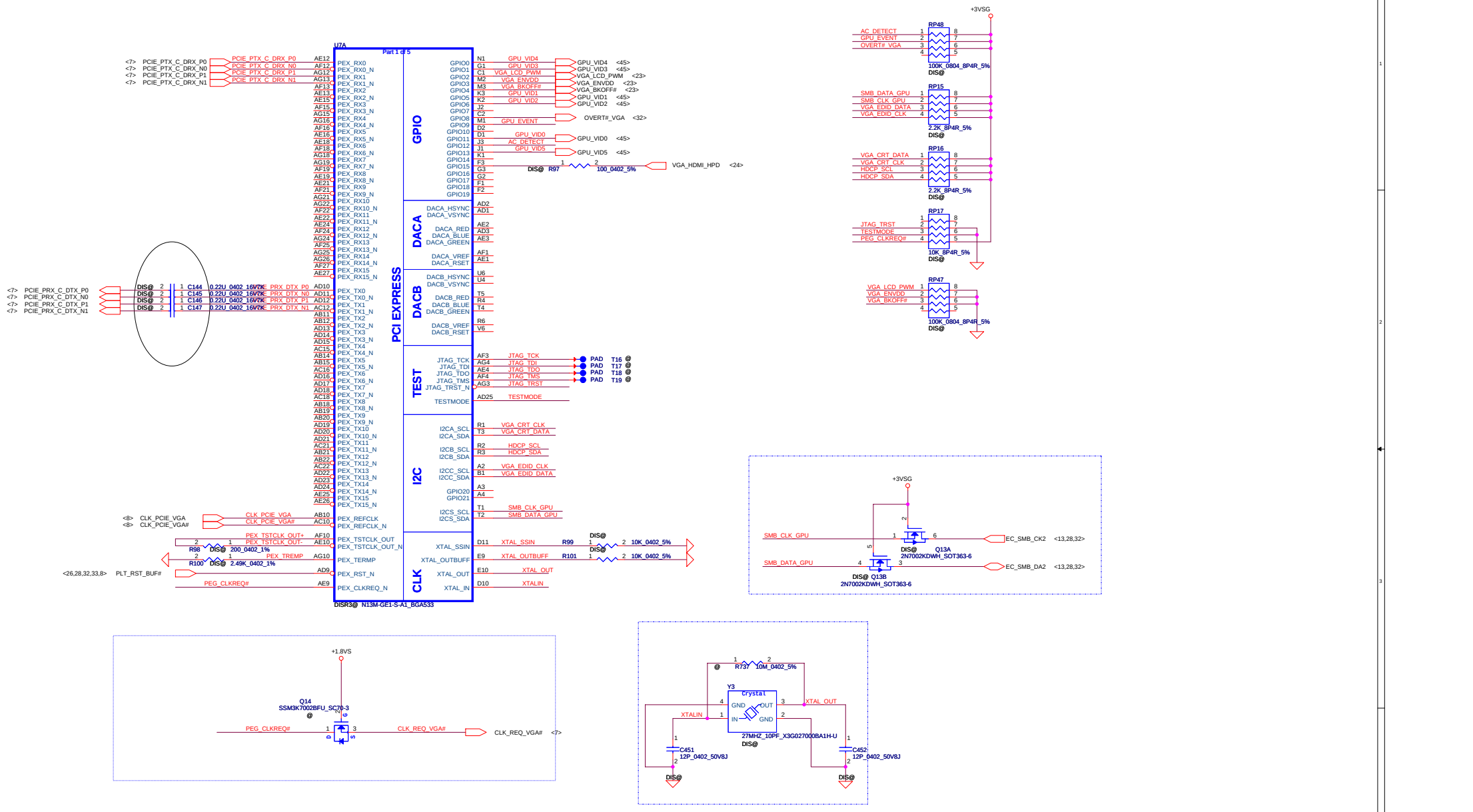

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: N13M PEG & DAC			
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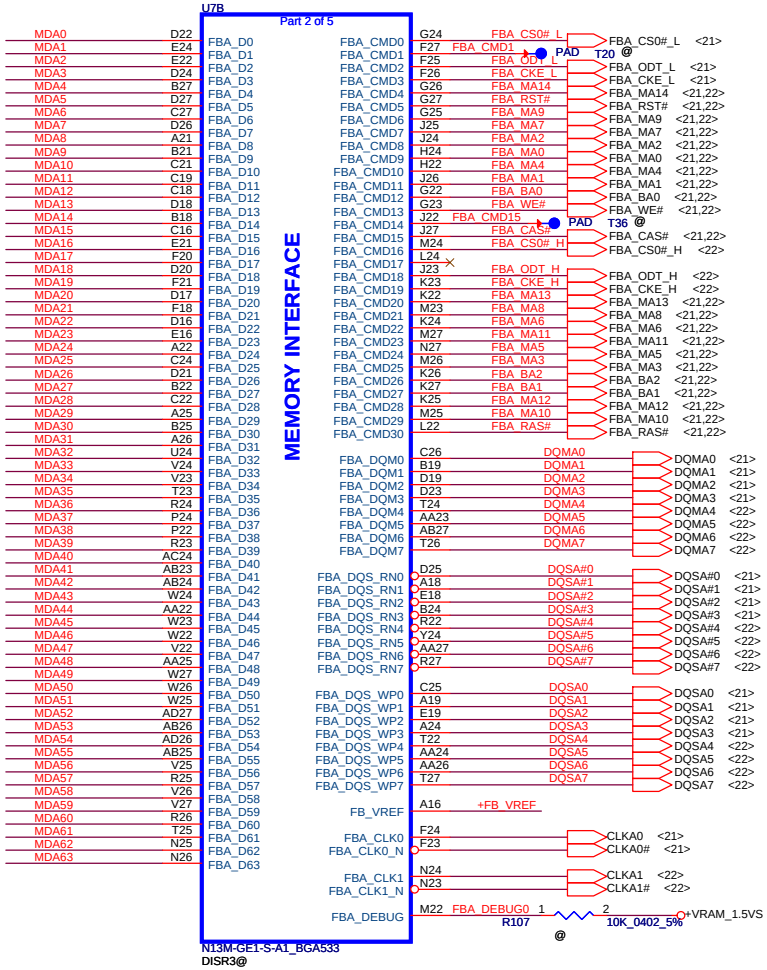
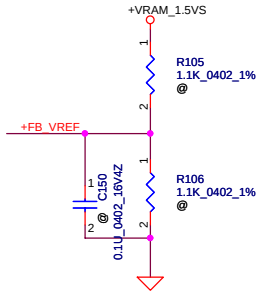
VRAM Interface

<21> MDA[31..0] — MDA[31..0]

<22> MDA[63..32] — MDA[63..32]





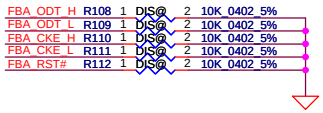
Mode D Address	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

* A15 is not required for any x16 device, even up to 4Gb density

* A15 is only needed if we support x8 configurations, and only at 4Gb

Place close to the first T point

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



Security Classification	Compal Secret Data		
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Title: N13M VRAM Interface

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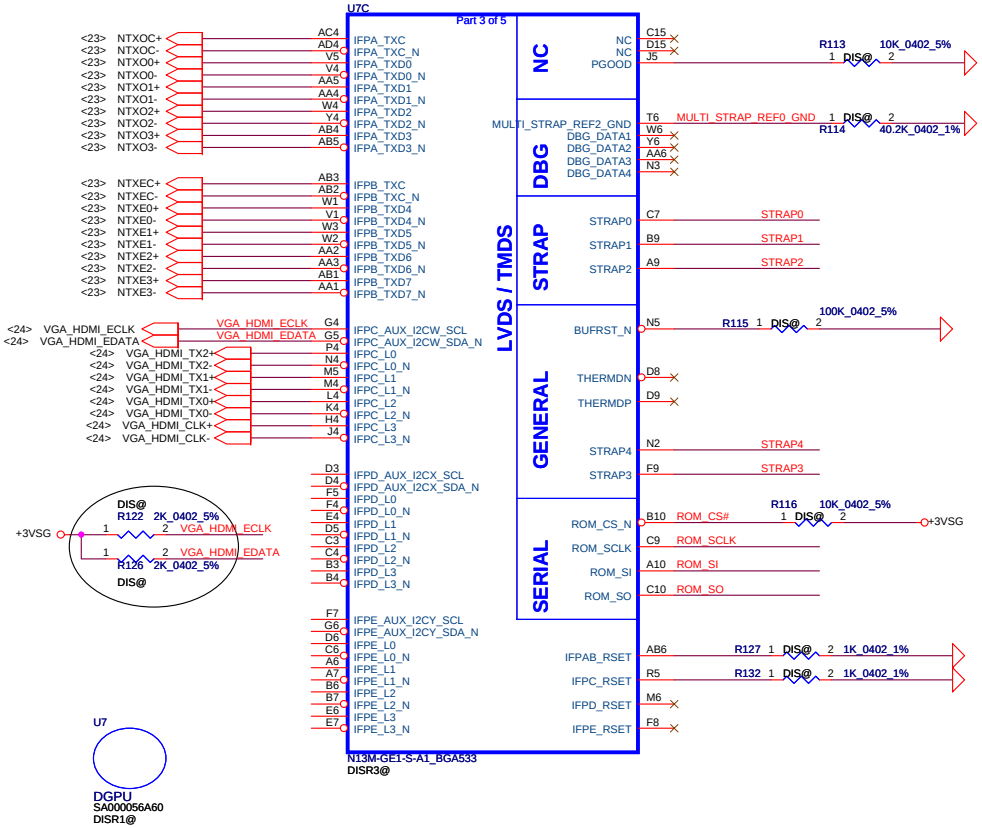
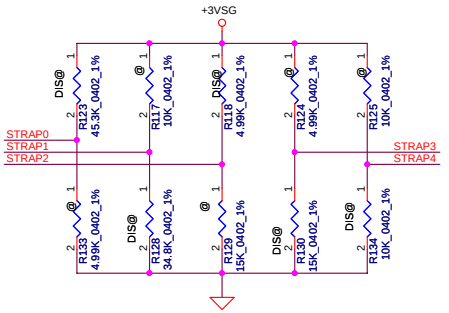
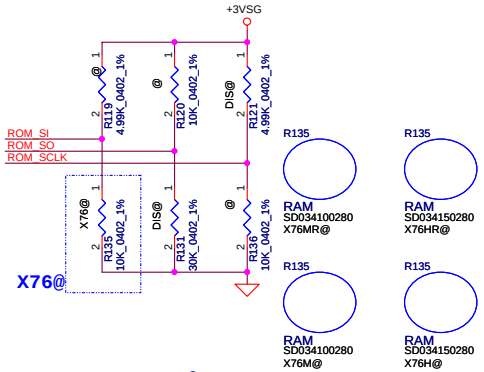


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**PCI_DEVID[5]**	PEX_PLL_EN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

SKU	Device ID	biit5 to bit0
N13M-GE1-S	0x1058	011000

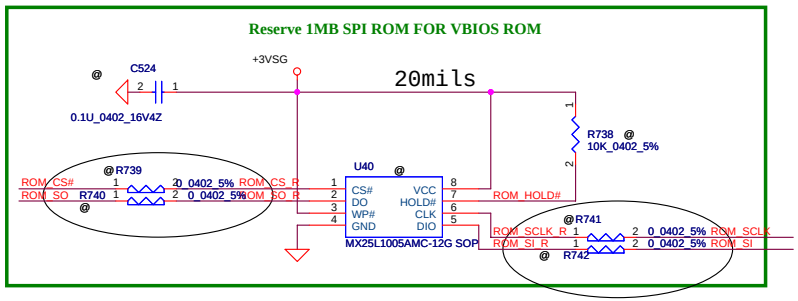
Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111





X76@

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	128M* 16* 4 1GB	Micron MT41J128M16JT-107G:K	1111 R123 PU 45K	0110 R128 PD 35K	1000 R118 PU 5K	0010 R130 PD 15K	0001 R134 PD 10K	0000 R135 PD 10K	0101 R120 PD 30K	1000 R121 PU 5K
	900 MHz	128M* 16* 4 1GB	Hynix H5TC2G63FFR-11C	1111 R123 PU 45K	0110 R128 PD 35K	1000 R118 PU 5K	0010 R130 PD 15K	0001 R134 PD 10K	0101 R135 PD 15K	0101 R120 PD 30K	1000 R121 PU 5K



Security Classification	Compal Secret Data		
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Title: N13M LVDS&TMDS

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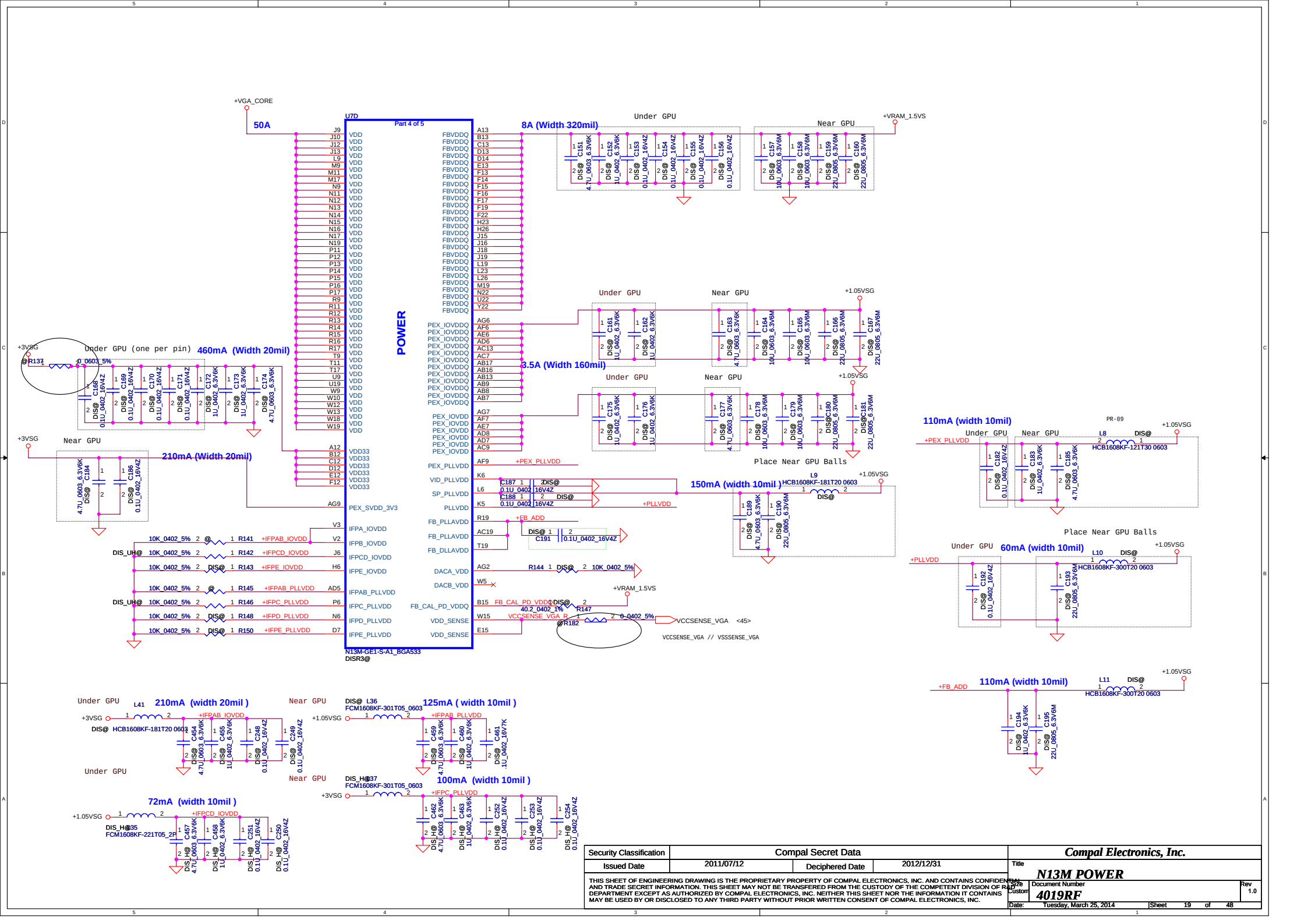

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13M POWER**

Size: Custom | Document Number: **4019RF** | Rev: 1.0

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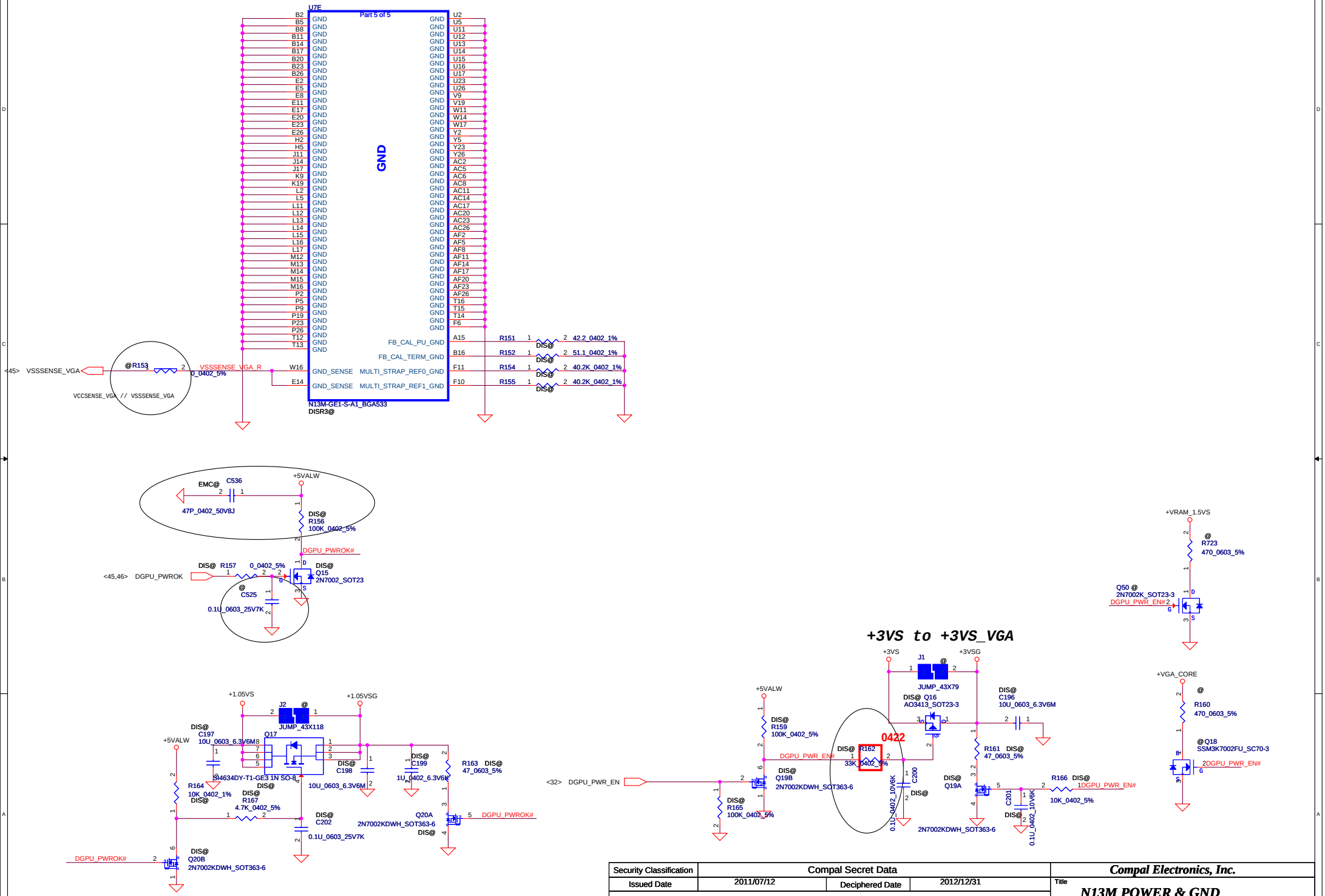


Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13M POWER & GND**

Size	Document Number	Rev
Custom	4019RF	1.0

Date: Tuesday, March 25, 2014 Sheet 20 of 48

RANK 0 [31...0]

VRAM DDR3 Chips

<17> MDA[31..0] MDA[31..0]

+VRAM_1.5VS

R168 1.33K_0402_1% DIS@

+MEM_VREF_CA0 +MEM_VREF_CA0

R169 1.33K_0402_1% DIS@

C203 0.01U_0402_16V7K DIS@

+VRAM_1.5VS

R170 1.33K_0402_1% DIS@

+MEM_VREF_DQ0 +MEM_VREF_DQ0

R171 1.33K_0402_1% DIS@

C204 0.01U_0402_16V7K DIS@

Place close to the first T point

<17> CLKA0

DIS@ R174 160_0402_1%

<17> CLKA0#

U8

+MEM_VREF_CA0 M8 VREFCA
+MEM_VREF_DQ0 H1 VREFDQ

<17,22> FBA_MA0 N3 A0
<17,22> FBA_MA1 P7 A1
<17,22> FBA_MA2 P3 A2
<17,22> FBA_MA3 N2 A3
<17,22> FBA_MA4 P8 A4
<17,22> FBA_MA5 P2 A5
<17,22> FBA_MA6 R8 A6
<17,22> FBA_MA7 R2 A7
<17,22> FBA_MA8 T8 A8
<17,22> FBA_MA9 R3 A9
<17,22> FBA_MA10 L7 A10/AP
<17,22> FBA_MA11 R7 A11
<17,22> FBA_MA12 N7 A12
<17,22> FBA_MA13 T3 A13
<17,22> FBA_MA14 T7 NC/A14
M7 NC/A15/BA3

<17,22> FBA_BA0 M2 BA0
<17,22> FBA_BA1 N8 BA1
<17,22> FBA_BA2 M3 BA2

CLKA0 J7 CK
CLKA0# K7 CK
<17> FBA_CKE_L K9 CKE/CKE0

<17> FBA_ODT_L K1 ODT/ODT0
<17> FBA_CS0#_L L2 CS/CS0
<17,22> FBA_RAS# J3 RAS
<17,22> FBA_CAS# K3 CAS
<17,22> FBA_WE# L3 WE

<17> DQSA1 F3 DQSL
<17> DQSA2 C7 DQSU

<17> DQMA1 E7 DML
<17> DQMA2 D3 DMU

<17> DQSA#1 G3 DQSL
<17> DQSA#2 B7 DQSU

<17,22> FBA_RST# T2 RESET
ZQ0 L8 ZQ/ZQ0

DIS@ R172 243_0402_1%

J1 NC/ODT1
L1 NC/CS1
J9 NC/CE1
L9 NCZQ1

DQU0 C3 DQU1 C8 DQU2 C2 DQU3 A7 DQU4 A2 DQU5 B8 DQU6 A3 DQU7

DQL0 E3 DQL1 F7 DQL2 F2 DQL3 H3 DQL4 H8 DQL5 G2 DQL6 H7 DQL7

Group1: MDA11 MDA14 MDA9 MDA13 MDA10 MDA12 MDA8 MDA15
Group2: MDA19 MDA18 MDA21 MDA22 MDA16 MDA23 MDA17 MDA20

+VRAM_1.5VS

VDD B2 VDD D9 VDD G7 VDD K2 VDD K8 VDD N1 VDD N9 VDD R1 VDD R9

VDDQ A1 VDDQ A8 VDDQ C1 VDDQ C9 VDDQ D2 VDDQ E9 VDDQ F1 VDDQ H2 VDDQ H9

VSS A9 VSS B3 VSS E1 VSS G8 VSS J2 VSS J8 VSS M1 VSS M9 VSS P1 VSS P9 VSS T1 VSS T9

VSSQ B1 VSSQ B9 VSSQ D1 VSSQ D8 VSSQ E2 VSSQ E8 VSSQ F9 VSSQ G1 VSSQ G9

96-BALL SDRAM DDR3

X76M@

SA00005SM80

U9

+MEM_VREF_CA0 M8 VREFCA
+MEM_VREF_DQ0 H1 VREFDQ

FBA_MA0 N3 A0
FBA_MA1 P7 A1
FBA_MA2 P3 A2
FBA_MA3 N2 A3
FBA_MA4 P8 A4
FBA_MA5 P2 A5
FBA_MA6 R8 A6
FBA_MA7 R2 A7
FBA_MA8 T8 A8
FBA_MA9 R3 A9
FBA_MA10 L7 A10/AP
FBA_MA11 R7 A11
FBA_MA12 N7 A12
FBA_MA13 T3 A13
FBA_MA14 T7 NC/A14
M7 NC/A15/BA3

FBA_BA0 M2 BA0
FBA_BA1 N8 BA1
FBA_BA2 M3 BA2

CLKA0 J7 CK
CLKA0# K7 CK
FBA_CKE_L K9 CKE/CKE0

FBA_ODT_L K1 ODT/ODT0
FBA_CS0#_L L2 CS/CS0
FBA_RAS# J3 RAS
FBA_CAS# K3 CAS
FBA_WE# L3 WE

<17> DQSA0 F3 DQSL
<17> DQSA3 C7 DQSU

<17> DQMA0 E7 DML
<17> DQMA3 D3 DMU

<17> DQSA#0 G3 DQSL
<17> DQSA#3 B7 DQSU

FBA_RST# T2 RESET
ZQ1 L8 ZQ/ZQ0

DIS@ R173 243_0402_1%

J1 NC/ODT1
L1 NC/CS1
J9 NC/CE1
L9 NCZQ1

DQU0 C3 DQU1 C8 DQU2 C2 DQU3 A7 DQU4 A2 DQU5 B8 DQU6 A3 DQU7

DQL0 E3 DQL1 F7 DQL2 F2 DQL3 H3 DQL4 H8 DQL5 G2 DQL6 H7 DQL7

Group0: MDA4 MDA3 MDA7 MDA0 MDA5 MDA2 MDA6 MDA1
Group3: MDA28 MDA29 MDA26 MDA31 MDA27 MDA25 MDA24 MDA30

+VRAM_1.5VS

VDD B2 VDD D9 VDD G7 VDD K2 VDD K8 VDD N1 VDD N9 VDD R1 VDD R9

VDDQ A1 VDDQ A8 VDDQ C1 VDDQ C9 VDDQ D2 VDDQ E9 VDDQ F1 VDDQ H2 VDDQ H9

VSS A9 VSS B3 VSS E1 VSS G8 VSS J2 VSS J8 VSS M1 VSS M9 VSS P1 VSS P9 VSS T1 VSS T9

VSSQ B1 VSSQ B9 VSSQ D1 VSSQ D8 VSSQ E2 VSSQ E8 VSSQ F9 VSSQ G1 VSSQ G9

96-BALL SDRAM DDR3

X76M@

SA00005SM80

310mA

310mA

U8 U9 U10 U11

RAM SA00006H420 X76H@

R1

RAM SA00006H400 X76HR@

RAM SA00005SM00 X76MR@

+VRAM_1.5VS

C205 1U_0402_6.3V6K DIS@
C206 1U_0402_6.3V6K DIS@
C207 1U_0402_6.3V6K DIS@
C208 1U_0402_6.3V6K DIS@
C209 1U_0402_6.3V6K DIS@
C210 1U_0402_16V7K DIS@
C211 1U_0402_16V7K DIS@
C212 1U_0402_16V7K DIS@
C213 1U_0402_16V7K DIS@
C214 1U_0402_16V7K DIS@

+VRAM_1.5VS

C215 1U_0402_6.3V6K DIS@
C216 1U_0402_6.3V6K DIS@
C217 1U_0402_6.3V6K DIS@
C218 1U_0402_6.3V6K DIS@
C219 1U_0402_6.3V6K DIS@
C220 1U_0402_16V7K DIS@
C221 1U_0402_16V7K DIS@
C222 1U_0402_16V7K DIS@
C223 1U_0402_16V7K DIS@
C224 1U_0402_16V7K DIS@

Place close to RANK0 VRAM

+VRAM_1.5VS

C225 22U_0805_6.3V6M DIS@

Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

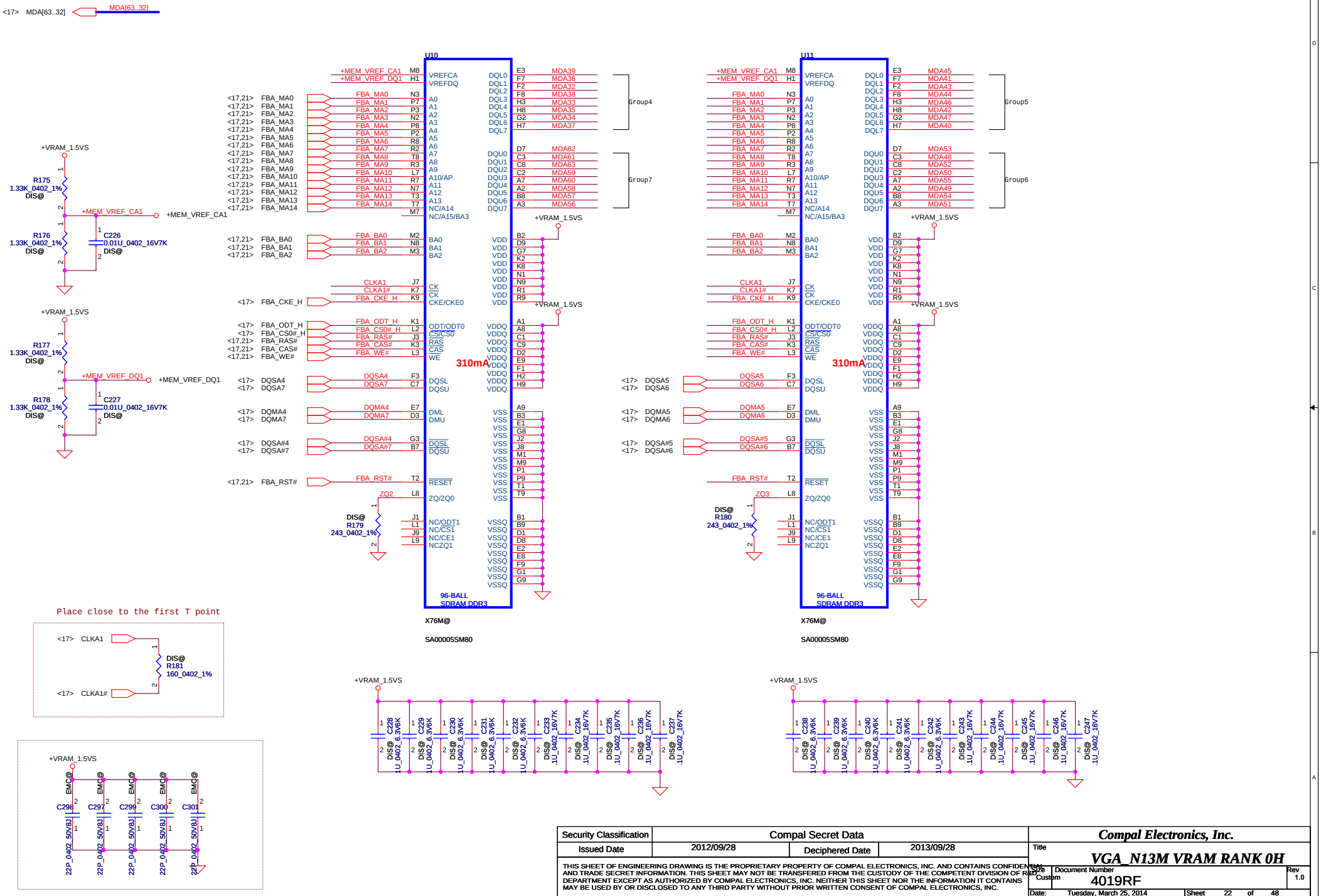
Title: VGA_N13M VRAM RANK 0L

Size: Custom | Document Number: 4019RF | Rev: 1.0

Date: Tuesday, March 25, 2014 | Sheet 21 of 48

RANK 0 [63...32]

VRAM DDR3 Chips



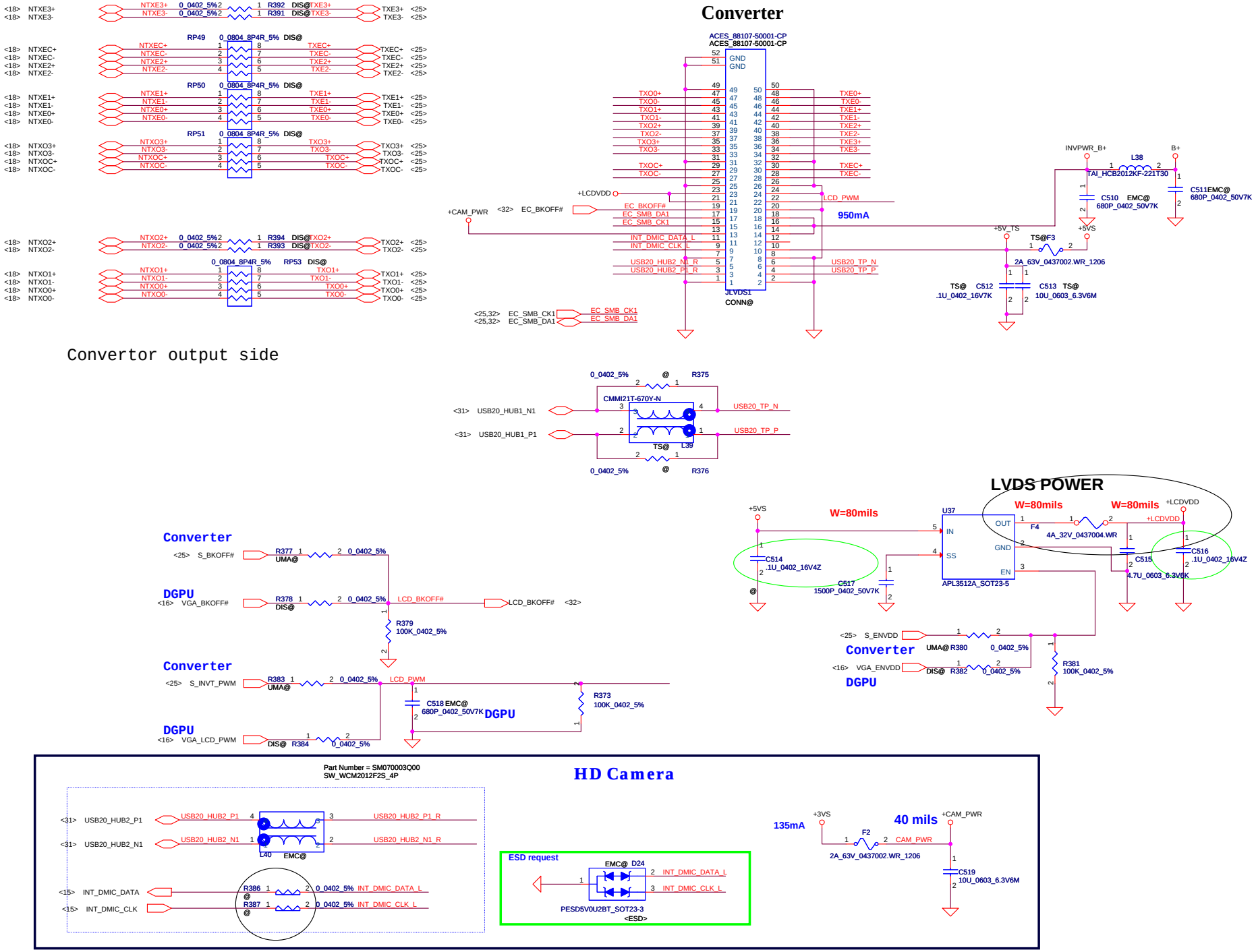
Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N13M VRAM RANK 0H

Size	Document Number	Rev
Custom	4019RF	1.0

Date: Tuesday, March 25, 2014 | Sheet 22 of 48



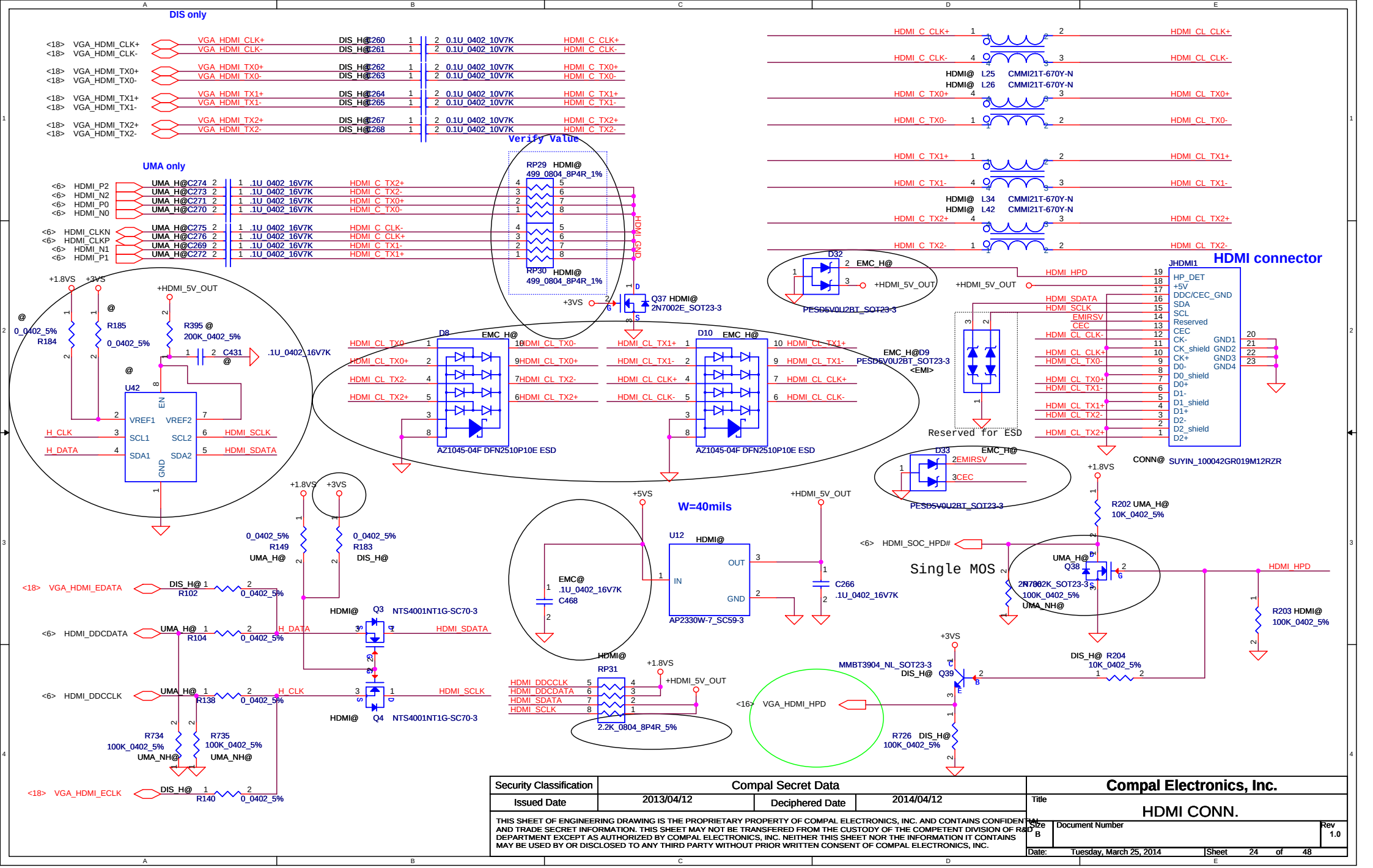
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: LVDS/CAM

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 25, 2014 | Sheet 23 of 48


DIS only
UMA only
Verify Value
HDMI connector
JHDMI1
CONN@ SUYIN_100042GR019M12RZR
Reserved for ESD
Single MOS
W=40mils
AZ1045-04F DFN2510P10E ESD
PESD5V0U2BT_SOT23-3
AP2330W-7_SC59-3
NTS4001NT1G-SC70-3
MMBT3904_NL_SOT23-3
2N7002E_SOT23-3
CMMI21T-670Y-N
Compal Secret Data
Issued Date 2013/04/12
Deciphered Date 2014/04/12
Compal Electronics, Inc.
Title HDMI CONN.
Size B
Document Number
Rev 1.0
Date: Tuesday, March 25, 2014
Sheet 24 of 48
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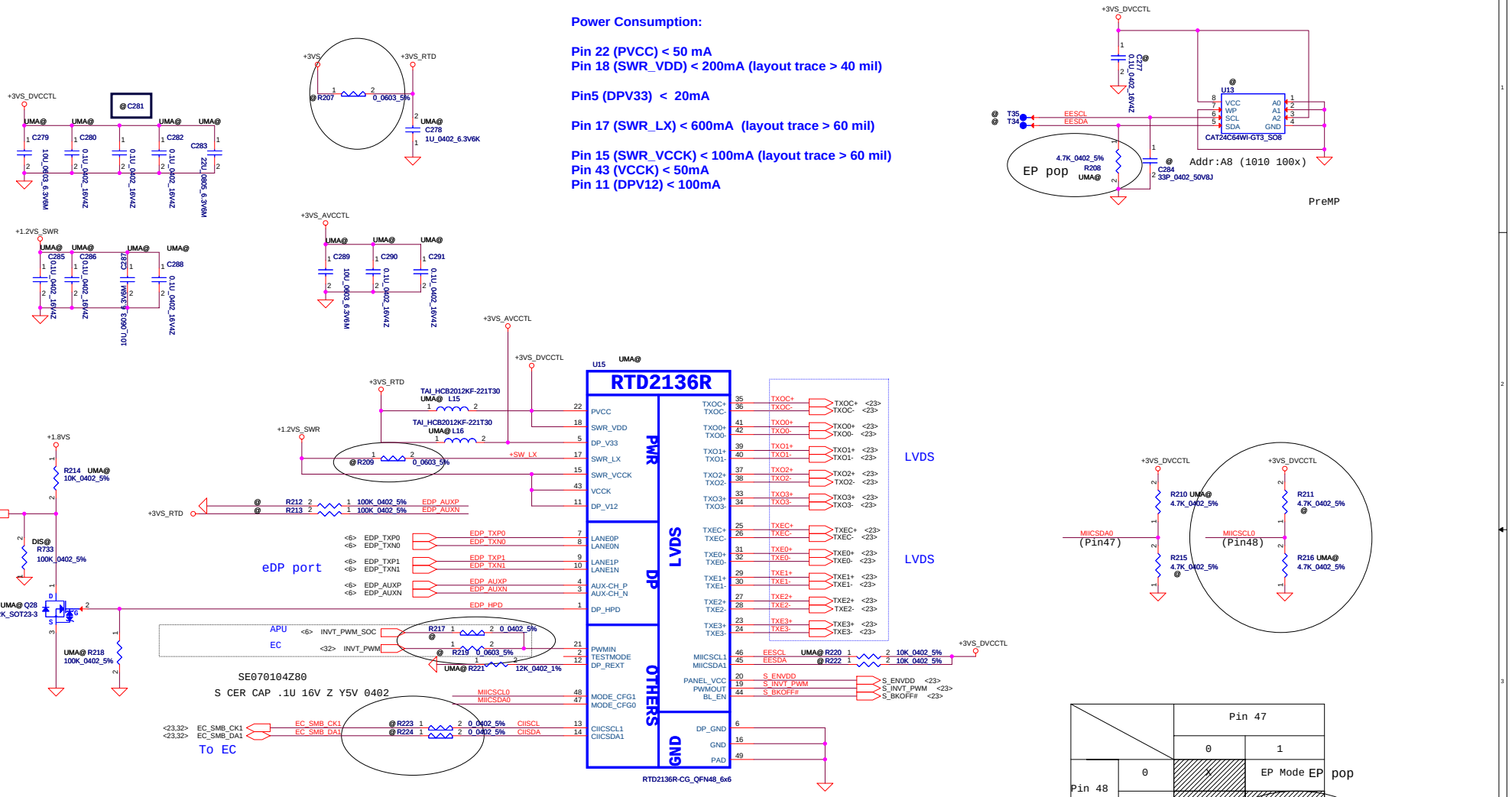
Power Consumption:

Pin 22 (PVCC) < 50 mA
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)

Pin5 (DPV33) < 20mA

Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)

Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 43 (VCCK) < 50mA
Pin 11 (DPV12) < 100mA

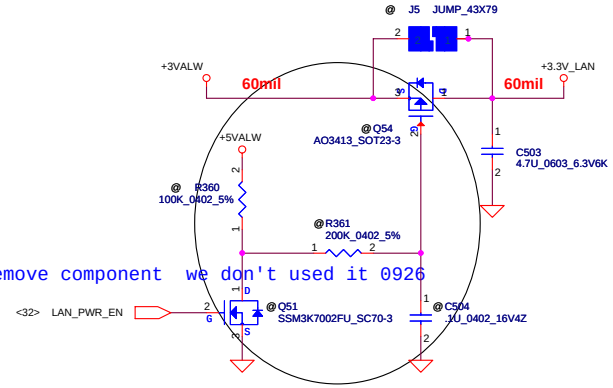


RTD2136R

S IC RTD2136R-CG QFN 48P DP/LVDS CTRL

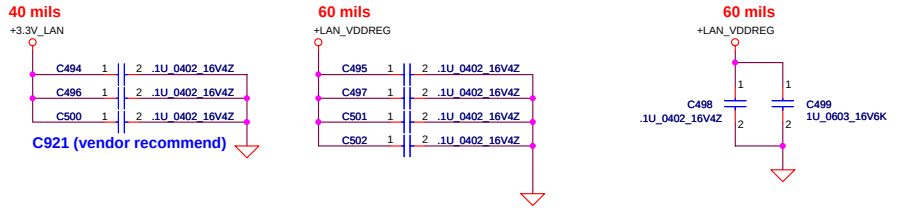
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/12	Deciphered Date	2014/04/12
Title	LVDS Converter RTD2136R		
Size C	Document Number		Rev 1.0
Date: Tuesday, March 25, 2014	Sheet 25 of 48		

WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

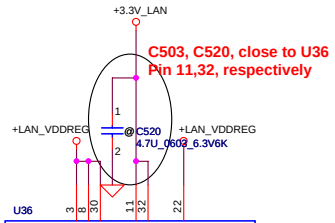
Power (Decoupling Cap.)



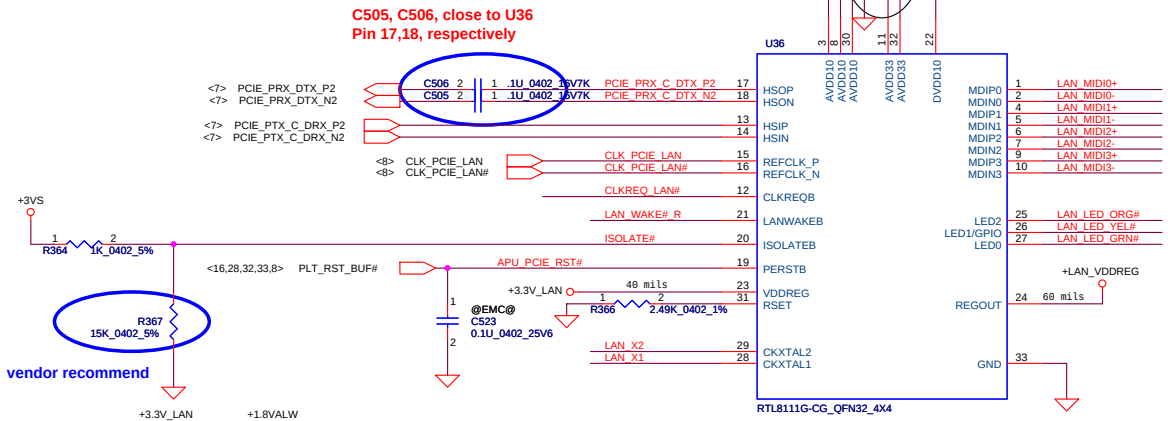
C494, C496, C500 close to U36 Pin 11,32 ,23, respectively

C495, C497, C501, C502, close to U36 Pin 3,8,24,30, respectively

C498, C499 close to U36 Pin22

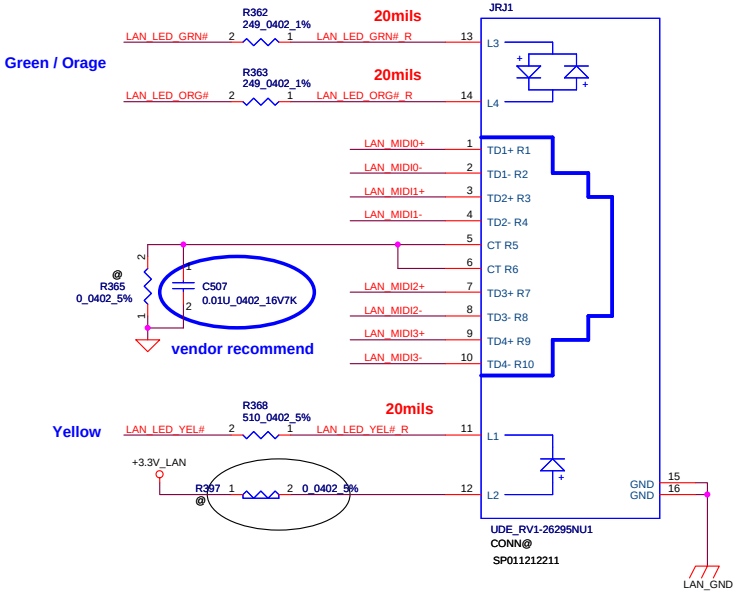


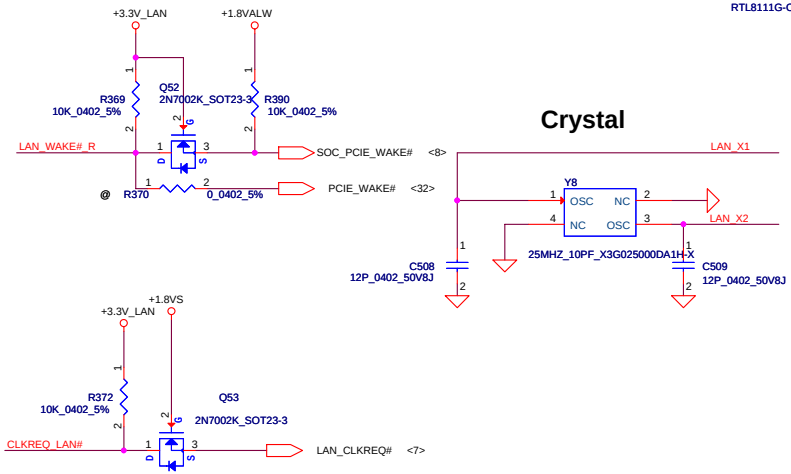
C505, C506, close to U36 Pin 17,18, respectively

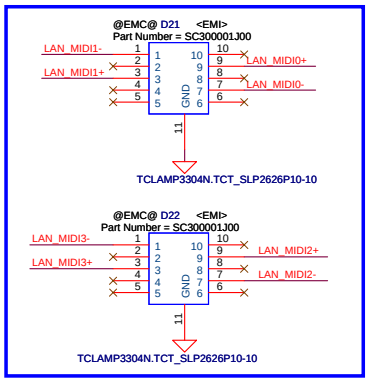


Green / Orage

Yellow







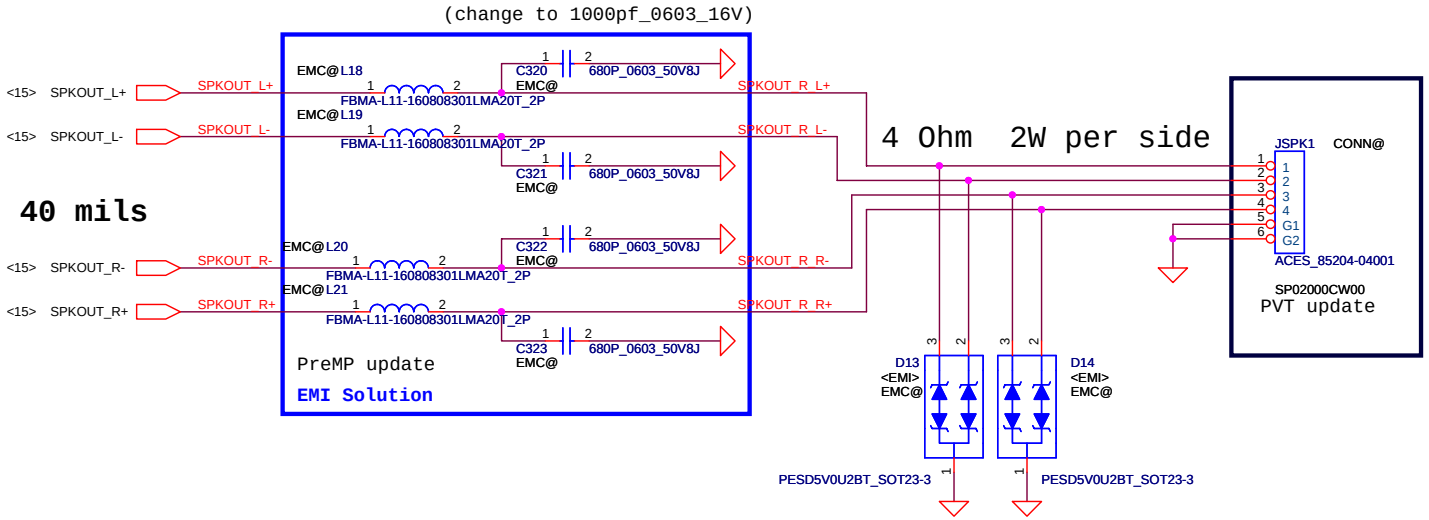
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: LAN RTL8111

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, March 25, 2014 Sheet 26 of 48



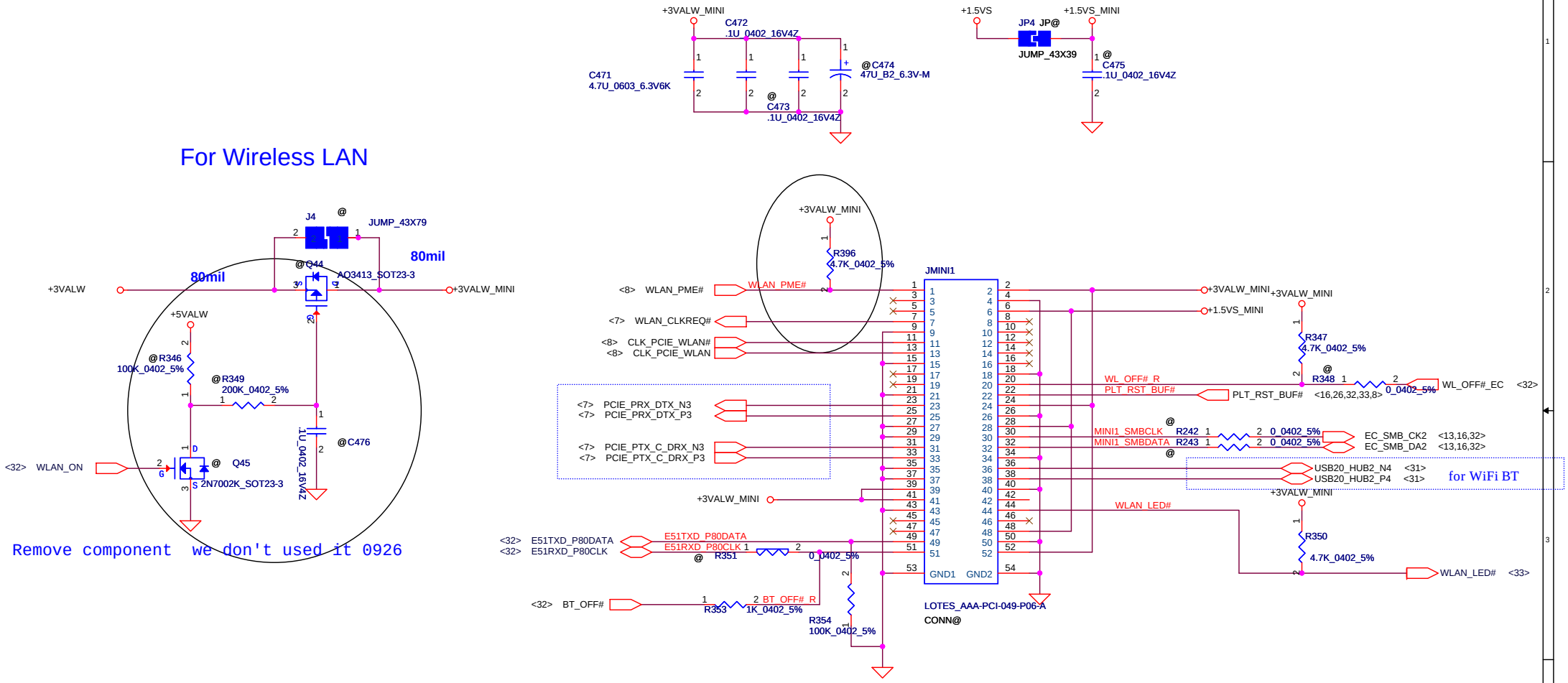
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: RJ45 / Speaker conn

Size	Document Number	Rev
B		1.0

Date: Tuesday, March 25, 2014 Sheet 27 of 48



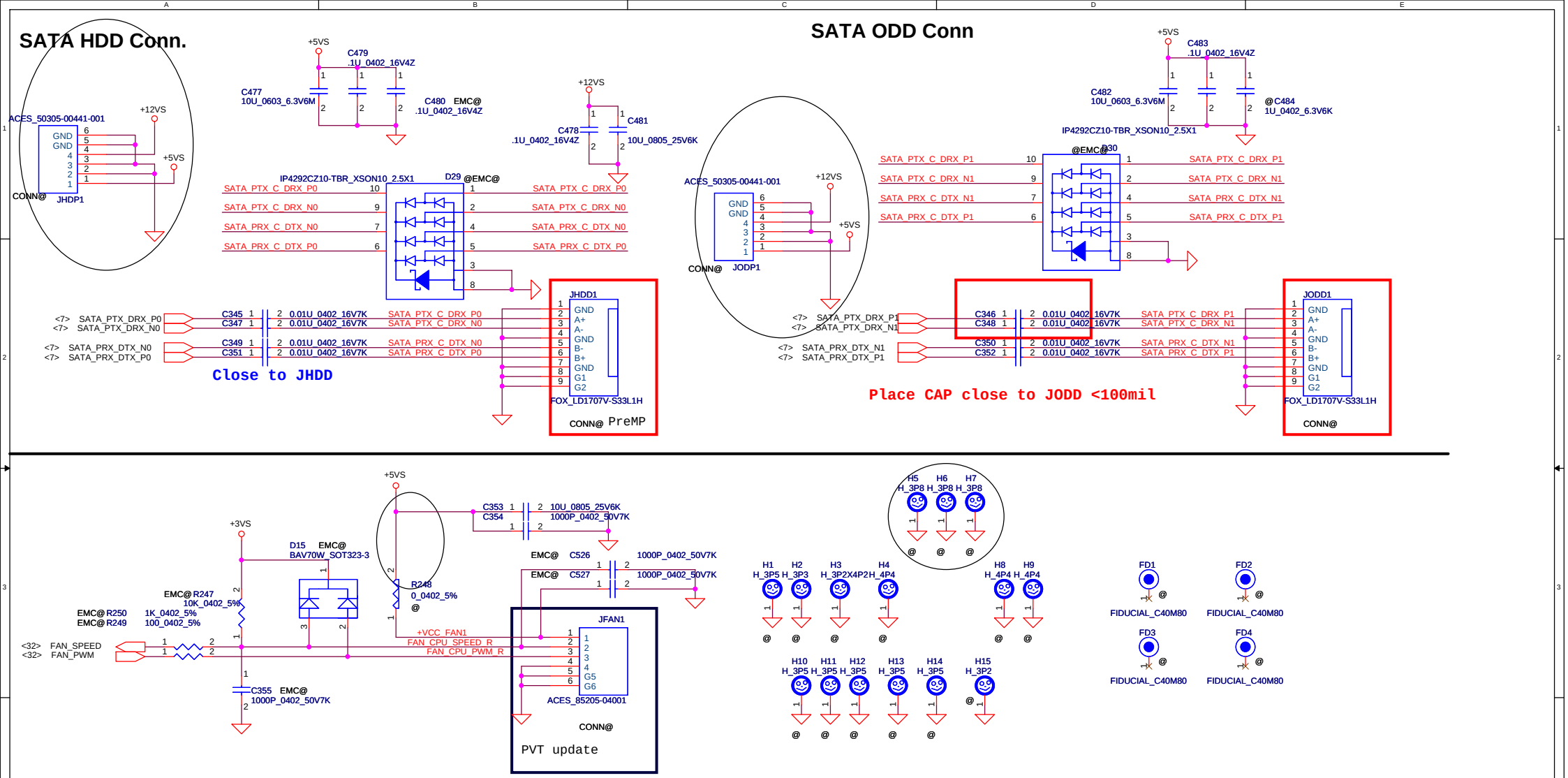
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: **Mini PCIE(WLAN)**

Size	Document Number	Rev
B		1.0

Date: Tuesday, March 25, 2014 Sheet 28 of 48



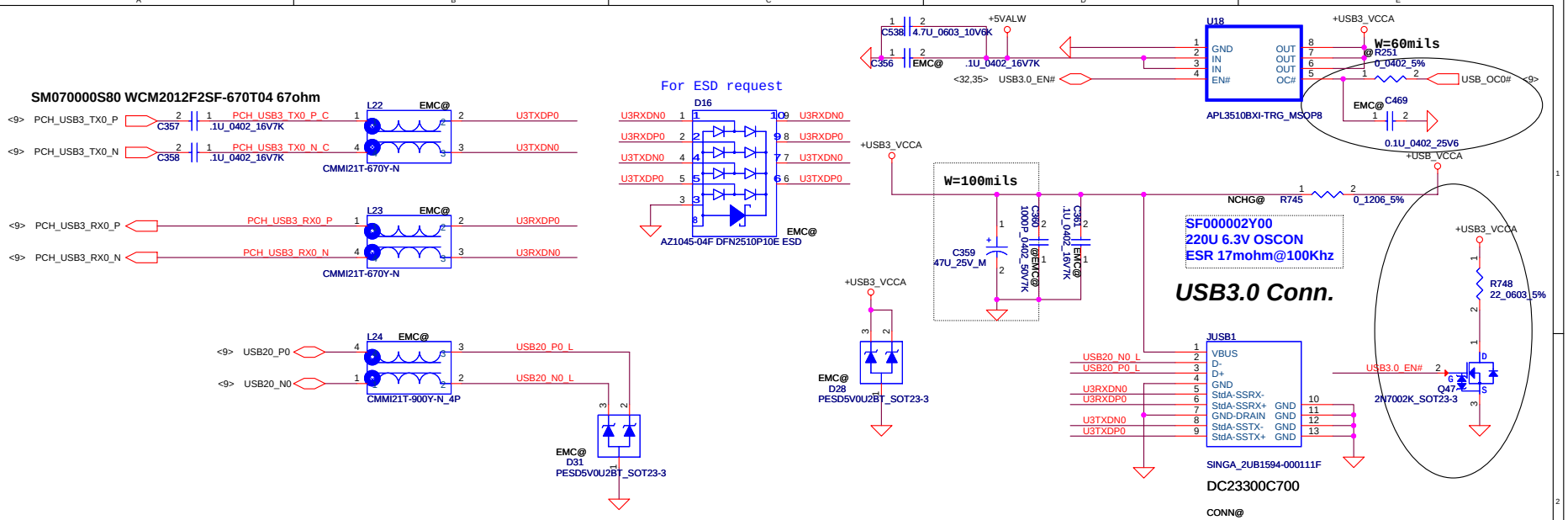
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

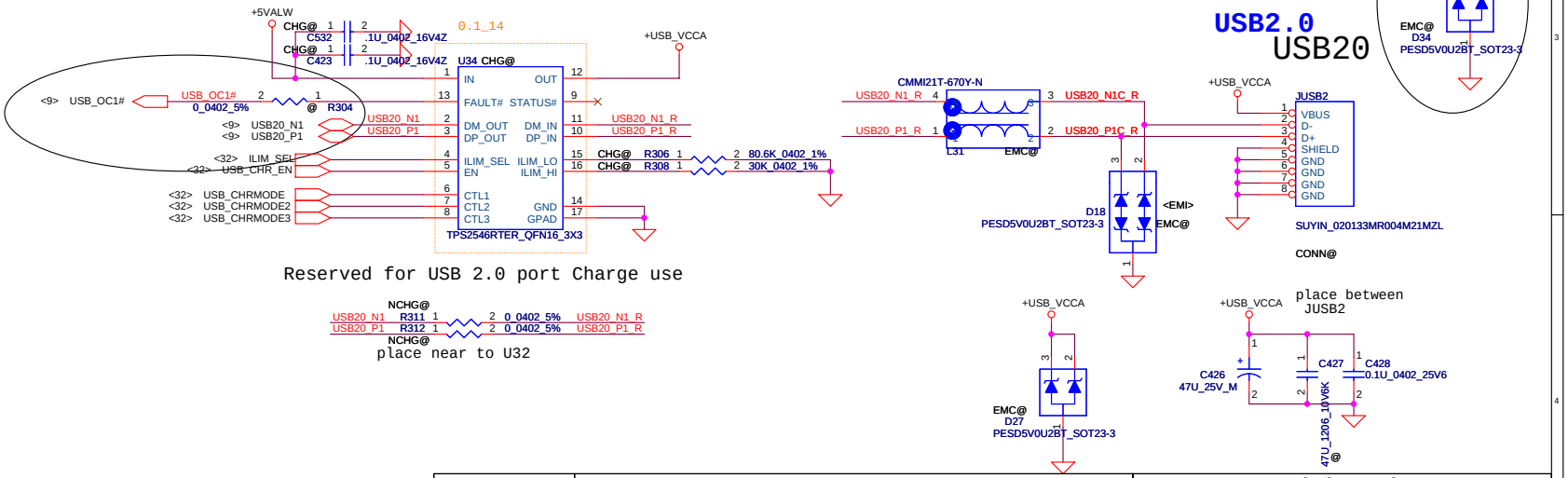
Title: HDD/ODD/FAN&Screw Hole

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 25, 2014 | Sheet 29 of 48



System Global Power State	TPS2546/TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake	0	0	1	1	ILIM_HI



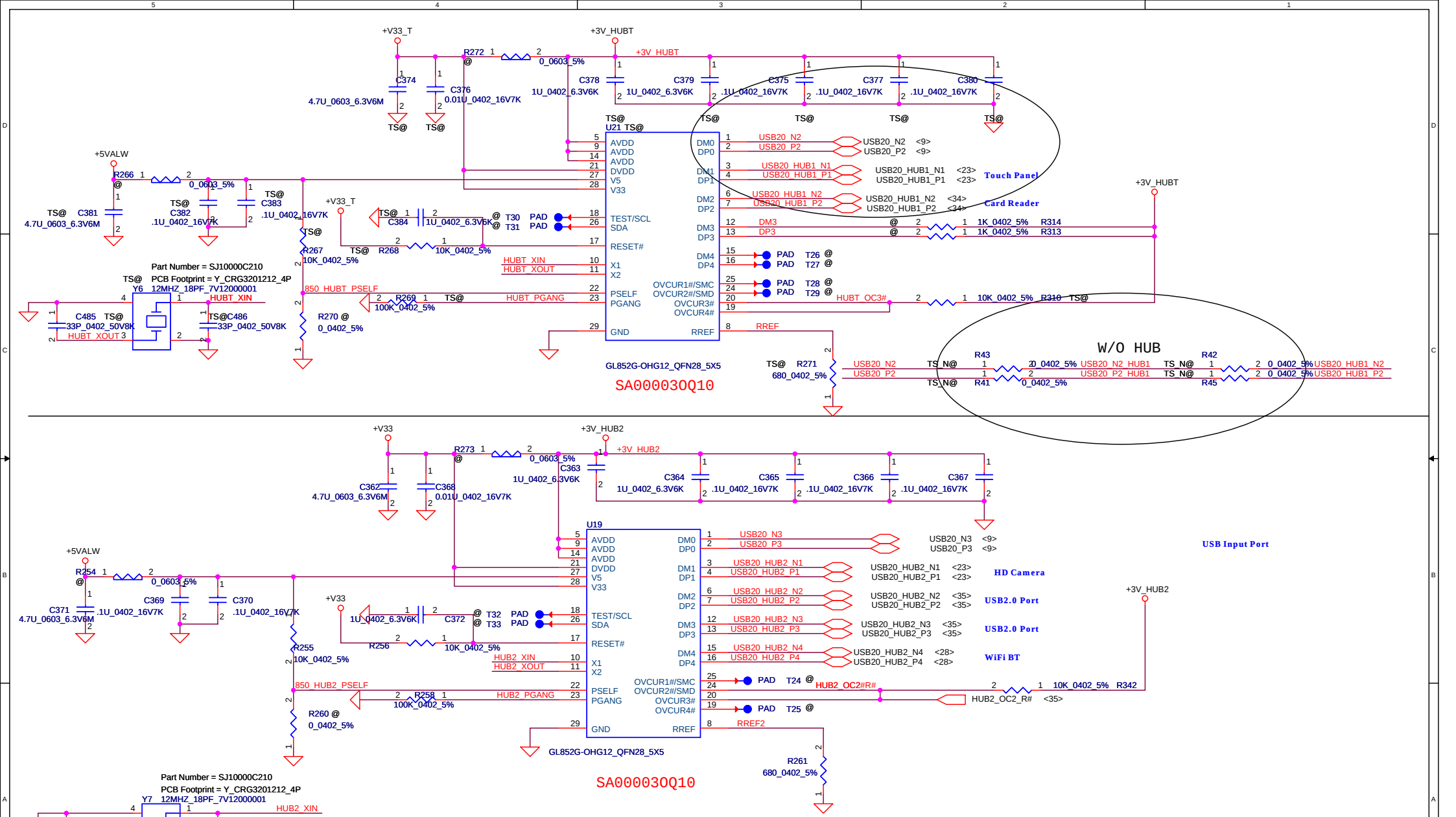
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: USB3.0 Conn & Hub

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, March 25, 2014 | Sheet 30 of 48



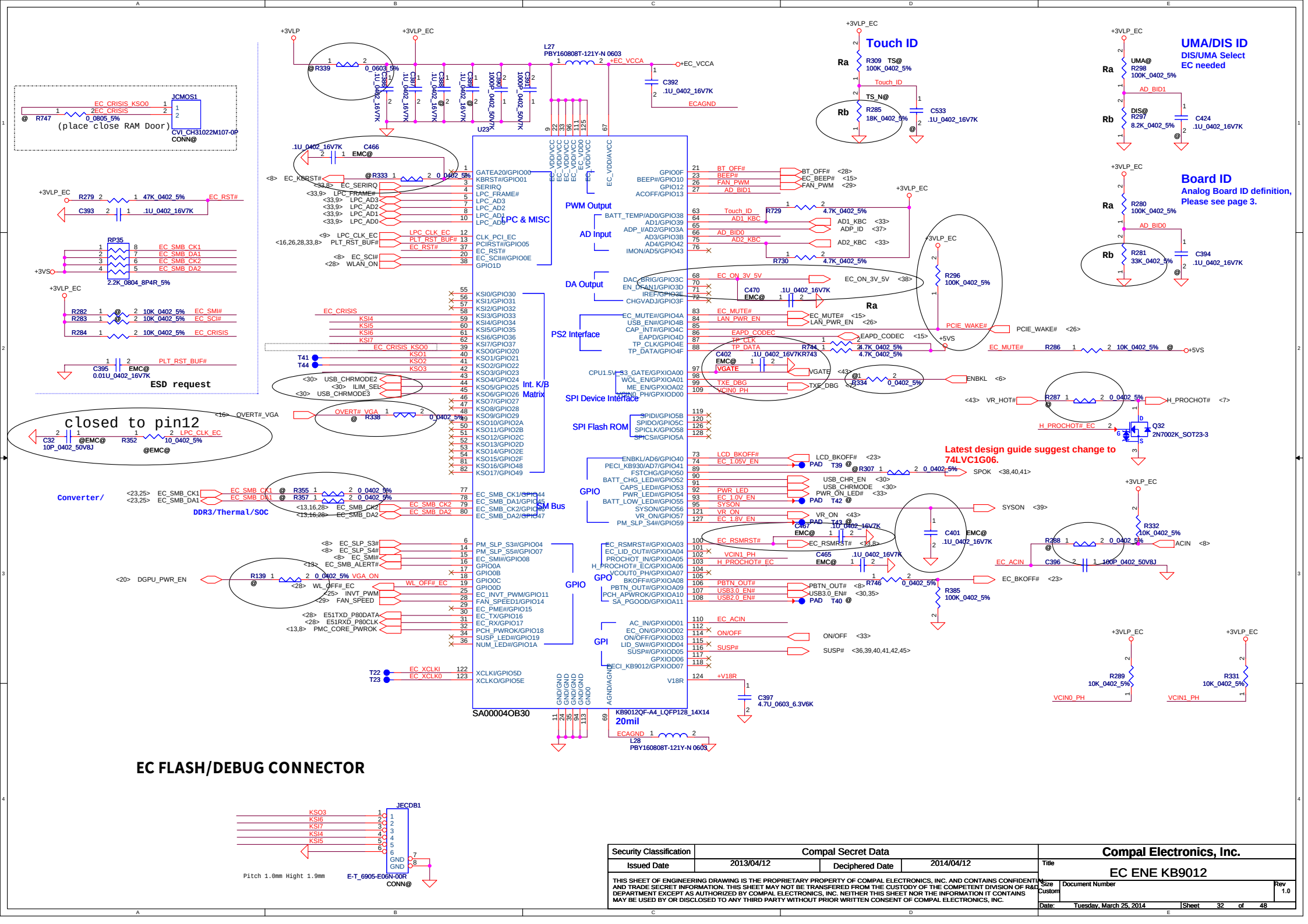
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: USB Hub for Touch

Size	Document Number	Rev
B		1.0

Date: Tuesday, March 25, 2014 | Sheet 31 of 48


Touch ID
UMA/DIS ID
DIS/UMA Select
EC needed
Board ID
Analog Board ID definition,
Please see page 3.
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus
Converter/
DDR3/Thermal/SOC
ESD request
closed to pin12
Latest design guide suggest change to 74LVC1G06.
EC FLASH/DEBUG CONNECTOR
SA00004OB30
KB9012QF-A4_LQFP128_14X14
20mil
Pitch 1.0mm Hight 1.9mm
E-T_6905-E06N-00R
CONN@
Security Classification
Compal Secret Data
Issued Date
2013/04/12
Deciphered Date
2014/04/12
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Compal Electronics, Inc.
Title
EC ENE KB9012
Size
Custom
Document Number
Rev
1.0
Date:
Tuesday, March 25, 2014
Sheet
32
of
48

TOP side
For debug

@ SW1
SMT1-05-A_4P
ON/OFFBTN#
R290 100K_0402_5%
R340 100_0402_5%
+3VLP
ON/OFF <32>
C398 0.1U_0402_25V6
For EMI request

Power Brd Connector

PU 4.7K on EC side

<32> AD1_KBC
<32> AD2_KBC
AD1_KBC
AD2_KBC
ON/OFFBTN#
JSW1 CONN@
ACES_85201-0405N
EMC@ C456 270P_0402_50V7K
C464 EMC@ 270P_0402_50V7K

TPM(Reserve)

+3VS
20 mils
TPM@ C399 0.1U_0402_16V4Z
TPM@ C400 10U_0603_6.3V6M
TPM@ U24
ST33ZP24AR28PVSP_TSSOP28
<32,9> LPC_FRAME#
LPC_FRAME# R292 0_0402_5%
LPC_FRAME# R
<32,8> EC_SERIRQ
EC_SERIRQ R291 0_0402_5%
RP36
<32,9> LPC_AD0
<32,9> LPC_AD1
<32,9> LPC_AD2
<32,9> LPC_AD3
TPM@ 0_0804_8P4R_5%
<9> LPC_CLK_TPM
TPM@ R293 33_0402_5%
C149 10P_0402_50V8J
@EMC@ @EMC@
R356 10_0402_5%
<16,26,28,32,8> PLT_RST_BUF#
R294 0_0402_5% TPM@
@ C403 0.1U_0402_16V4Z

LED Brd Connector

+3VS_LED +3VALW_LED
JLED1
ACES_85201-06051
CONN@
<32> PWR_ON_LED#
<7> SOC_SATALED#
<28> WLAN_LED#
PWR_ON_LED#
WLAN_LED#
C260@ R303 0_0402_5%
ON/OFFBTN#
S330@ R305 0_0402_5%
GND
GND

PWR_ON_LED# EMC@ C404 1000P_0402_50V7K
SOC_SATALED# EMC@ C405 470P_0402_50V7K
WLAN_LED# EMC@ C406 470P_0402_50V7K
Reserve for EMI.

+3VS
R341 1_0603_5%
+3VS_LED
C407 C408 C409 0.1U_0402_25V6
C412 0.1U_0402_25V6
For EMI request

EMI Request

+3VALW
R343 1_0603_5%
+3VALW_LED
C410 0.1U_0402_25V6
C411 0.1U_0402_25V6

Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: TP/LED/TPM

Size	Document Number	Rev
Custom		1.0

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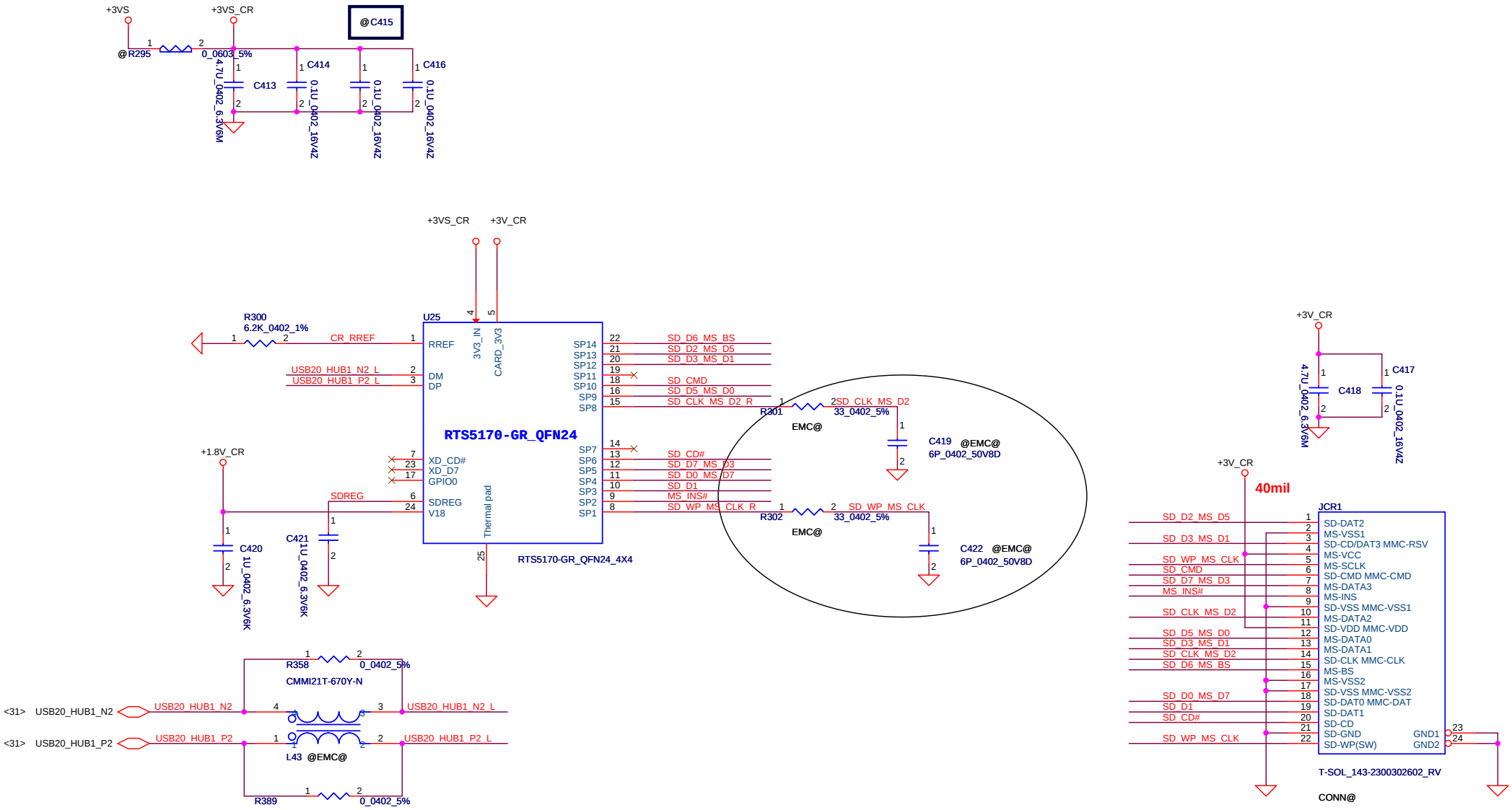

Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: USB Cardreader

Size	Document Number	Rev
B		1.0

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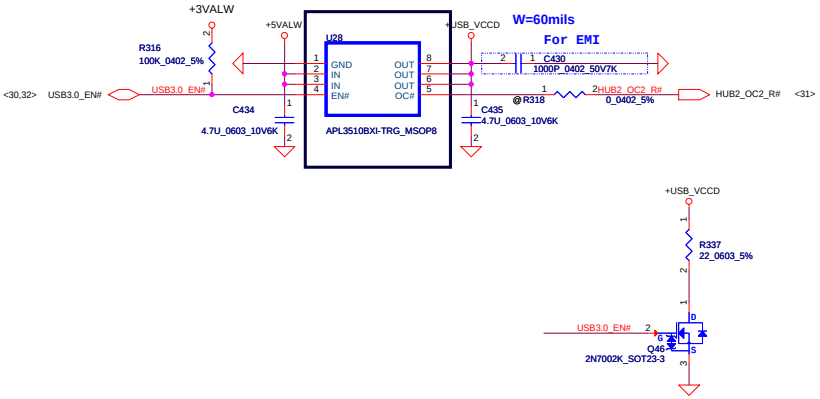
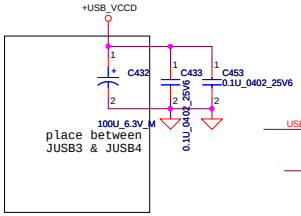
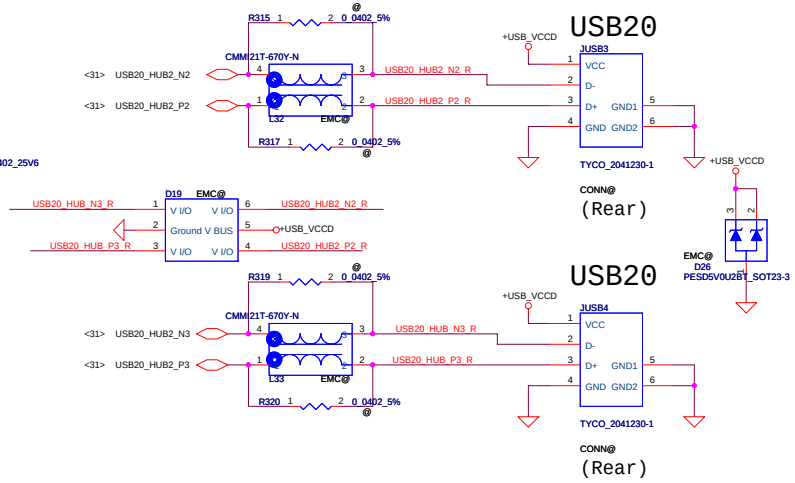
USB2.0 Power



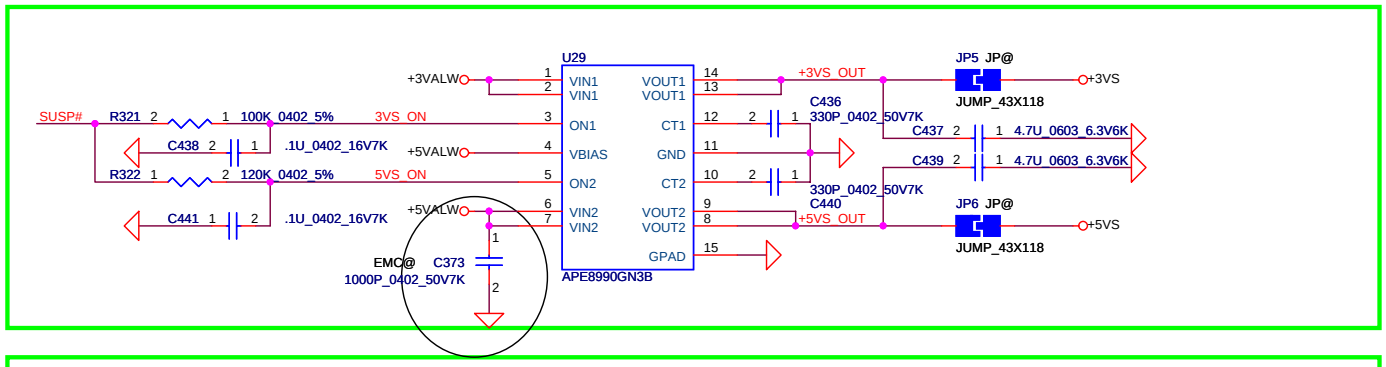


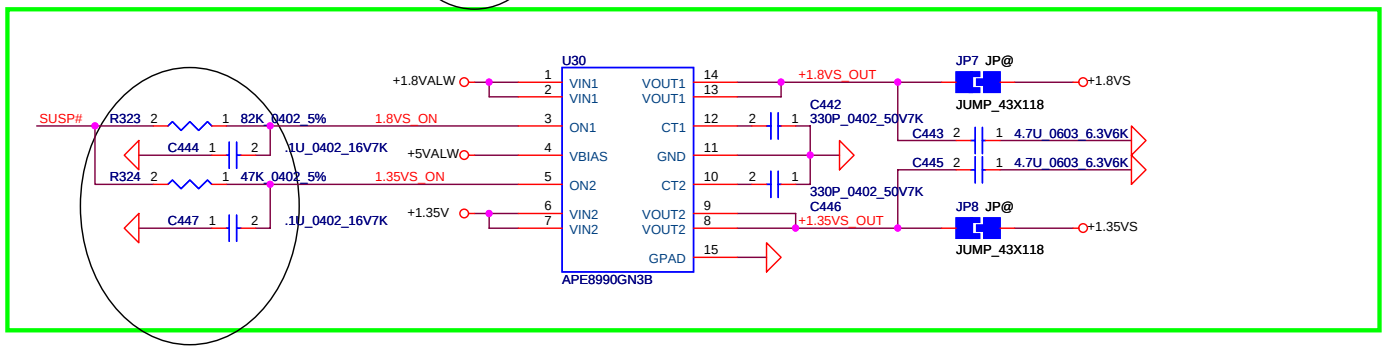


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/12	Deciphered Date	2014/04/12

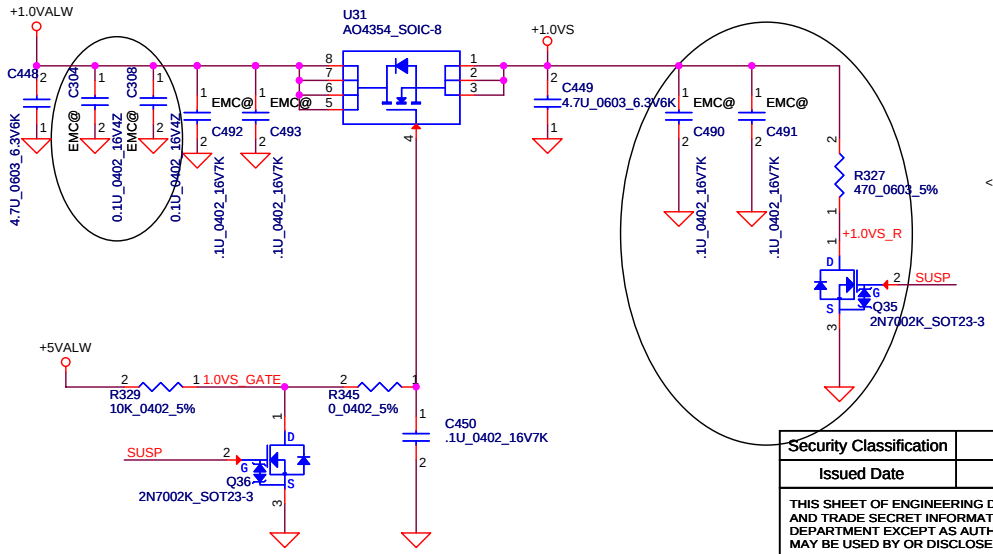
Title	USB connector		
Size C	Document Number		Rev 1.0
Date: Tuesday, March 25, 2014	Sheet 35 of 48		

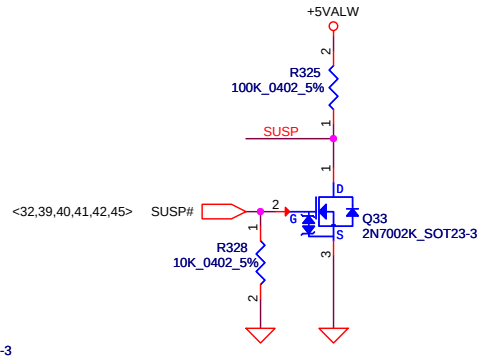
Normall Platform (Not support M-STATE and Deep Sleep)

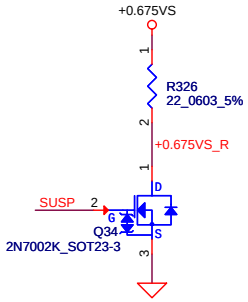




+1.0VALW TO +1.0VS







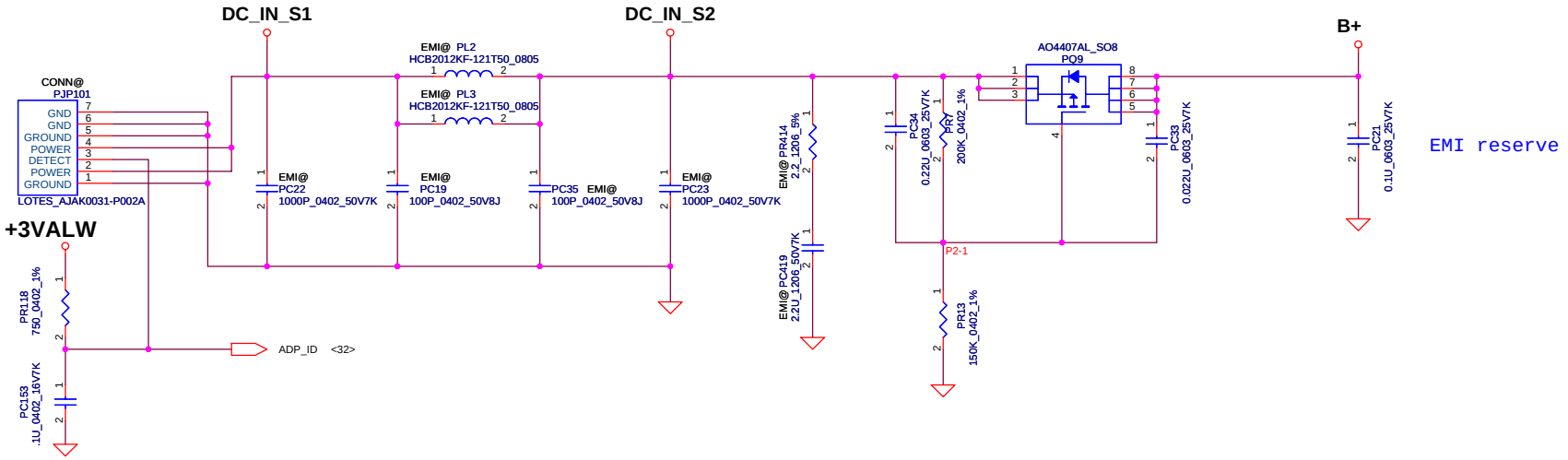
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: DC DC

Size: B | Document Number | Rev: 1.0

Date: Tuesday, March 25, 2014 | Sheet 36 of 48



Security Classification	Compal Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/08/15

Compal Electronics, Inc.

Title: **DCIN / CONN**

Size	Document Number	Rev
Custom	4019RF	1.0

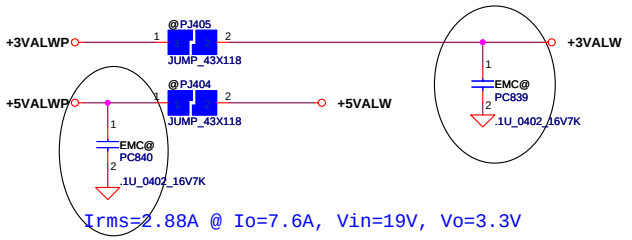
Date: Tuesday, March 25, 2014 | Sheet 37 of 48

Module model information

RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

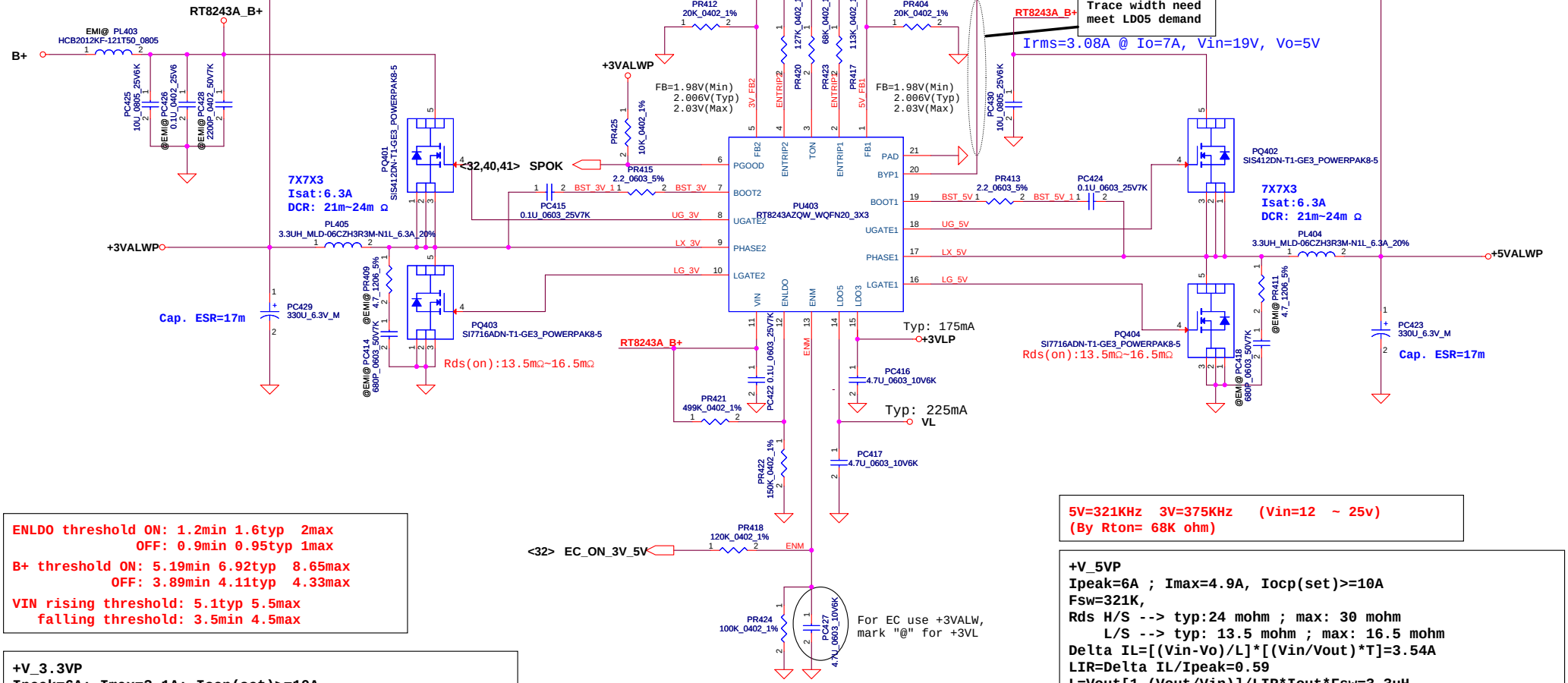
ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.



Irms=2.88A @ Io=7.6A, Vin=19V, Vo=3.3V

Irms=3.08A @ Io=7A, Vin=19V, Vo=5V

Trace width need meet LDO5 demand



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max
B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max
VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

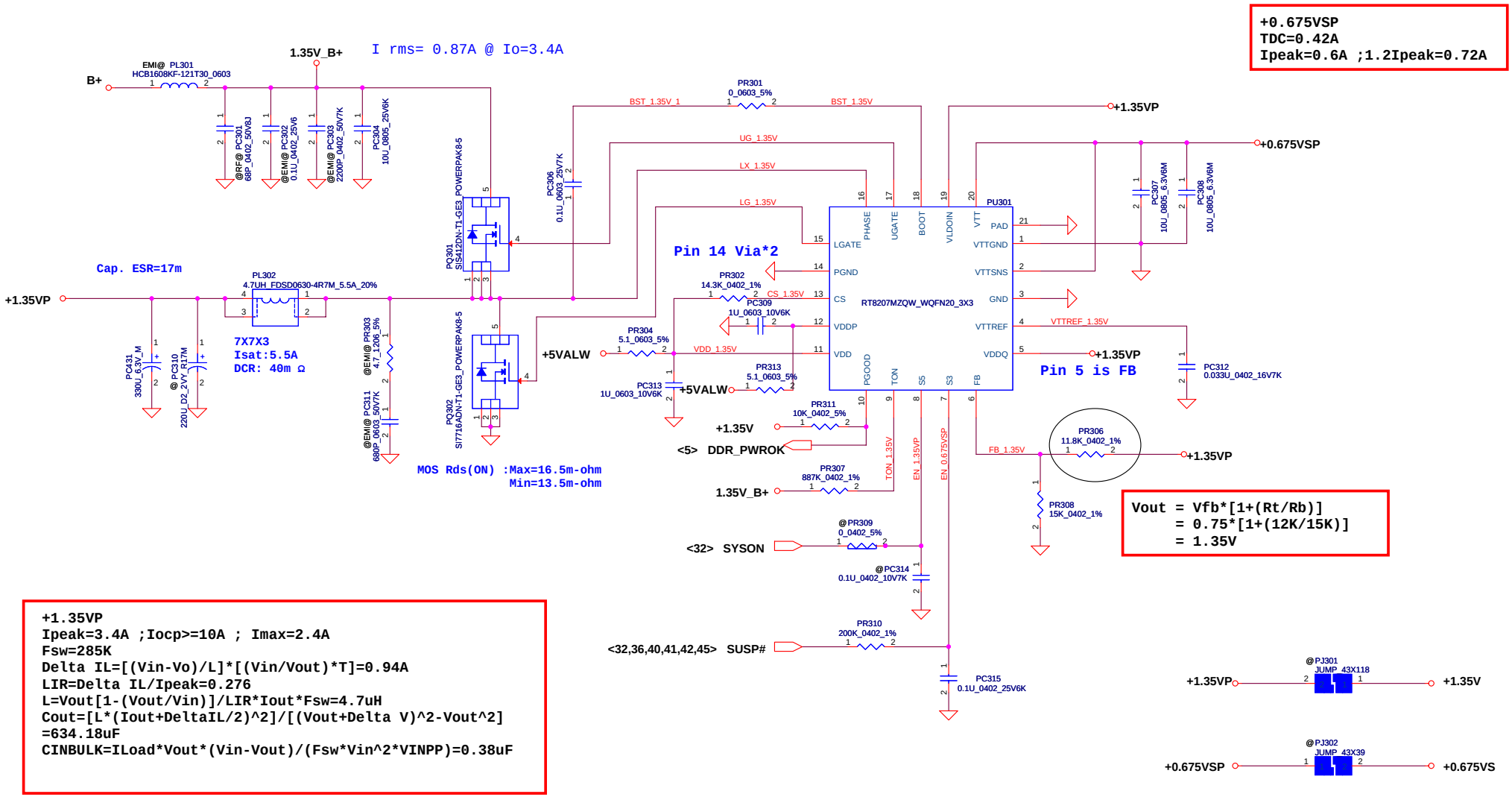
5V=321KHz 3V=375KHz (Vin=12 ~ 25v)
(By Rton= 68K ohm)

+V_3.3VP
Ipeak=6A; Imax=3.1A; Iocp(set)>=10A
Fsw=300K
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=2.22A
LIR=Delta IL/Ipeak=0.37
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=3.3uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=379.53uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.1uF

+V_5VP
Ipeak=6A ; Imax=4.9A, Iocp(set)>=10A
Fsw=321K,
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=3.54A
LIR=Delta IL/Ipeak=0.59
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=3.3uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=197.26uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.75uF

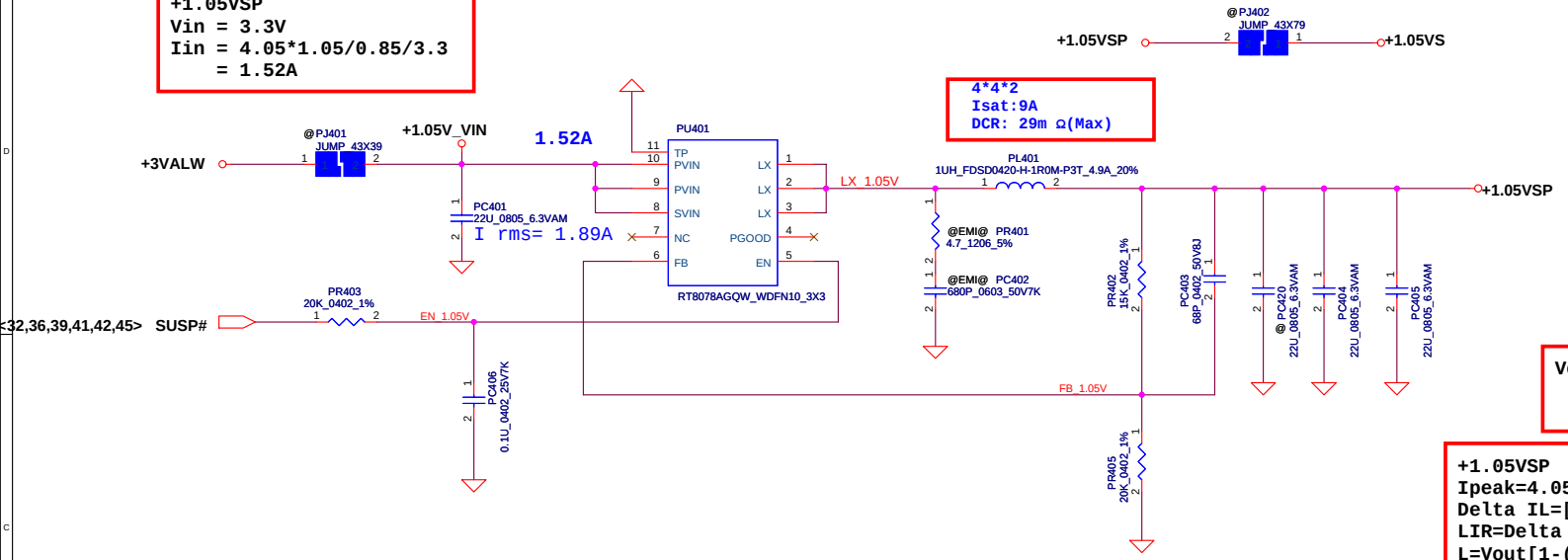
Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	2014/08/31

Title	3VALW/5VALW		
	ZAA00 MB		
Size: Custom	Document Number		Rev: 1.0
Date: Tuesday, March 25, 2014	Sheet 38 of 48		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/12	Deciphered Date	2014/08/12
Title	+1.35VP / +0.675VSP		
Size: Custom	Document Number: 4019RF		Rev: 1.0
Date: Tuesday, March 25, 2014	Sheet 39 of 48		

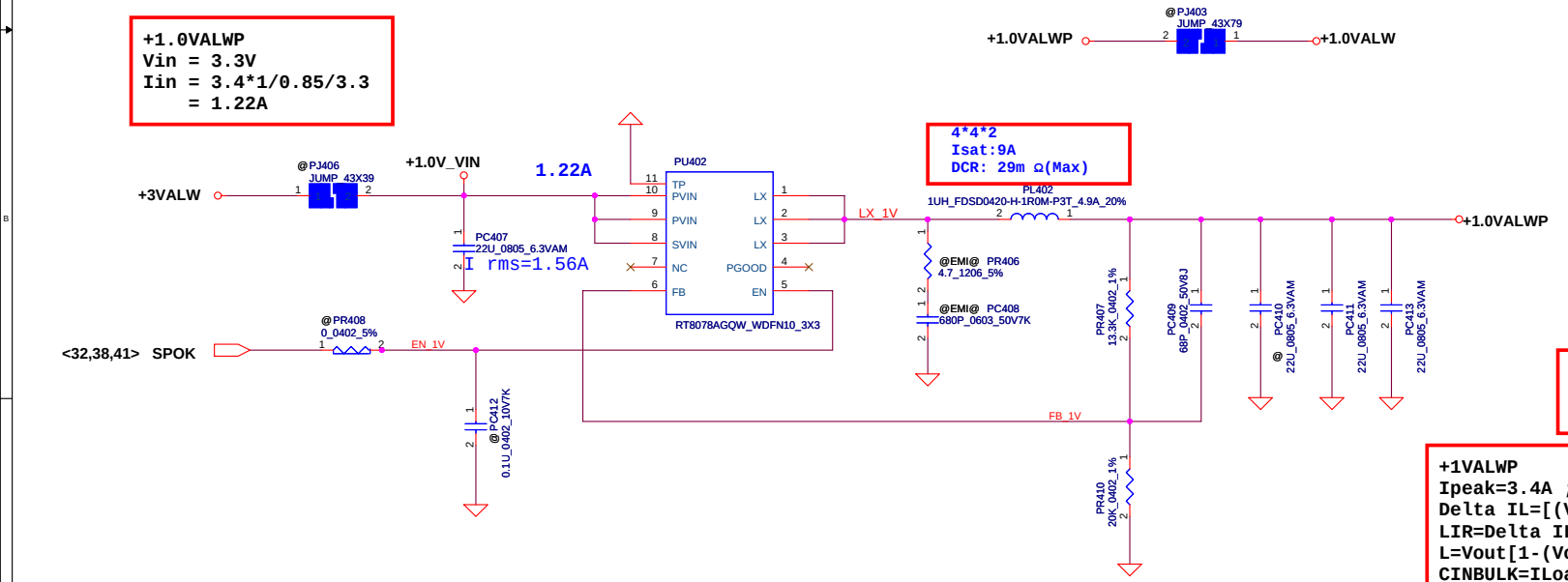
+1.05VSP
Vin = 3.3V
Iin = 4.05*1.05/0.85/3.3
= 1.52A



Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(15K/20K)]
= 1.05V

+1.05VSP
Ipeak=4.05A; CL(min)>=4.4A; Fsw=1MHz
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=0.716A
LIR=Delta IL/Ipeak=0.177
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=1.0uH
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=2.66uF

+1.0VALWP
Vin = 3.3V
Iin = 3.4*1/0.85/3.3
= 1.22A



Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(9.76K/14.7K)]
= 1V

+1VALWP
Ipeak=3.4A ;CL(min)>=4.4A; Fsw=1MHz
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=0.697A
LIR=Delta IL/Ipeak=0.205
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=1.0uH
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=2.18uF

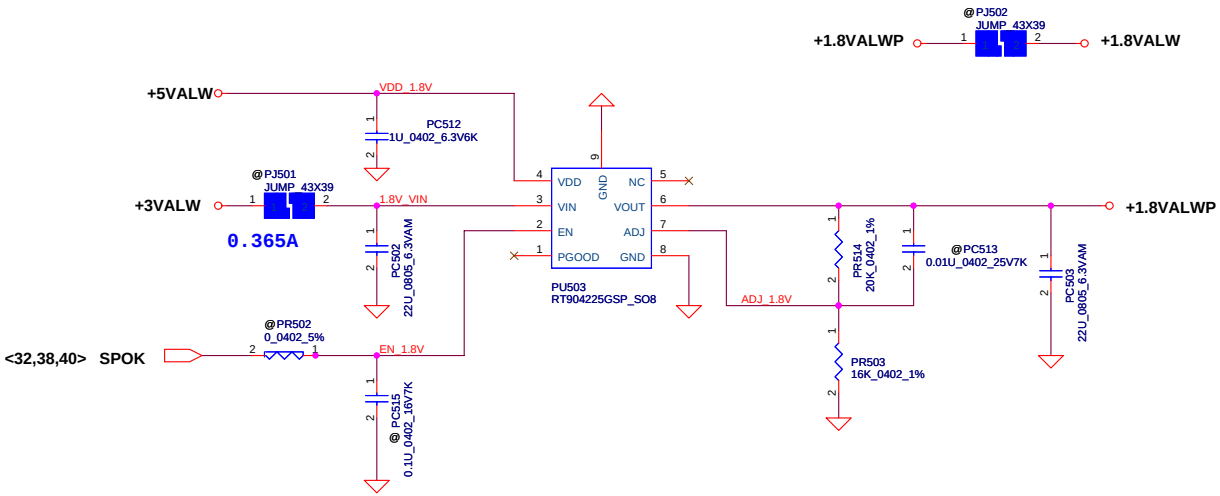
Security Classification	Compal Secret Data		
Issued Date	2013/08/12	Deciphered Date	2014/08/12

Compal Electronics, Inc.

Title: +1.05VSP / +1.0VALWP

Size: Custom | Document Number: 4019RF | Rev: 1.0

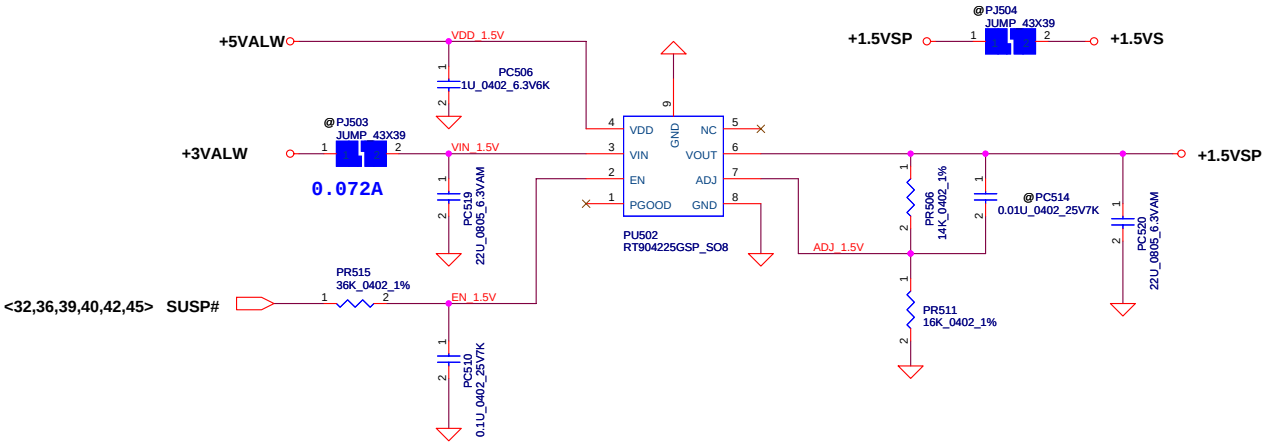
Date: Tuesday, March 25, 2014 | Sheet 40 of 48




```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.8*[1+(20K/16K)]
     = 1.8V
```

```
+1.8VALWP
Ipeak=0.365A ;
Iocp>=3.1A


RT9042:
Quiescent Current (GND Current)
IQ(typ)=0.6mA,IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.551W
θ JA= 75°C/W*0.551=41.35°C
```




```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.8*[1+(14K/16K)]
     = 1.5V
```

```
+1.5VSP
Ipeak=0.072A
Iocp>=3.1A
```

```
RT9042:
Quiescent Current (GND Current)
IQ(typ)=0.6mA,IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.133W
θ JA= 75°C/W*0.551=10.01°C
```

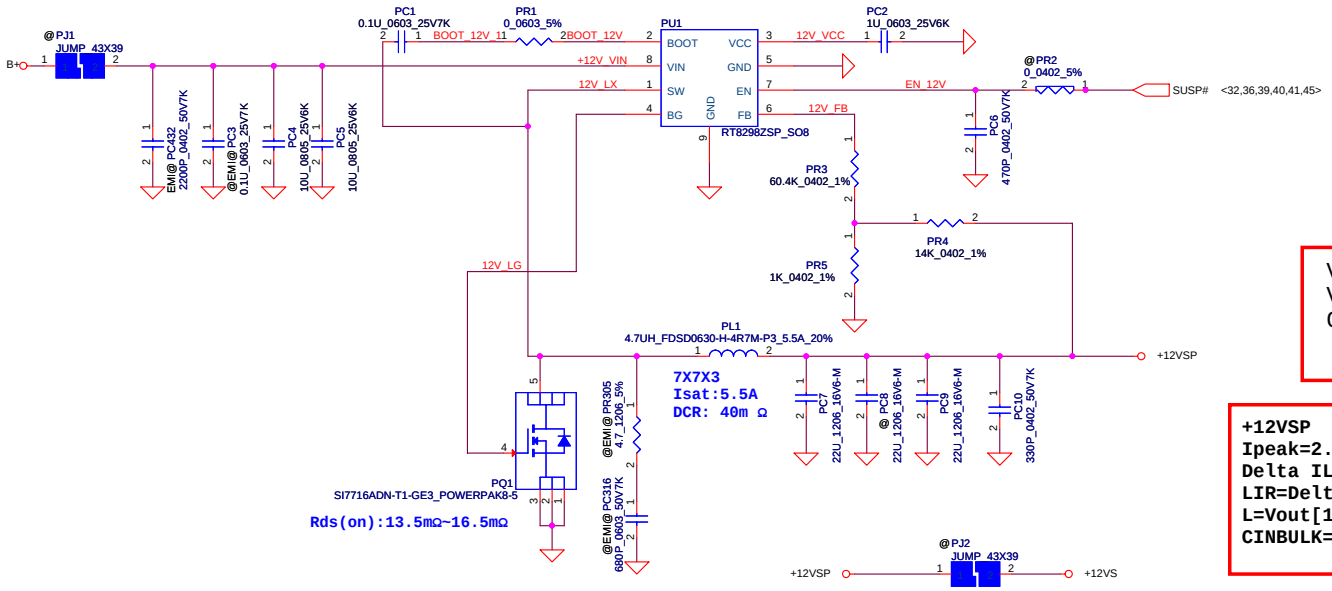
Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	2014/08/15

Compal Electronics, Inc.

Title: **+1.8VALWP / +1.5VSP**

Size	Document Number	Rev
Custom	4019RF	1.0

Date: Tuesday, March 25, 2014 | Sheet 41 of 48



VFB=0.8V
Vo=0.8(1+Rt/Rb)=0.8(1+14k/1k)=12V
CL(min)=8A; CL(min)=10A; CL(min)=12A

+12VSP
Ipeak=2.5A; Fsw=600KHz
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=1.702A
LIR=Delta IL/Ipeak=0.851
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=4.7uH
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=2.59uF

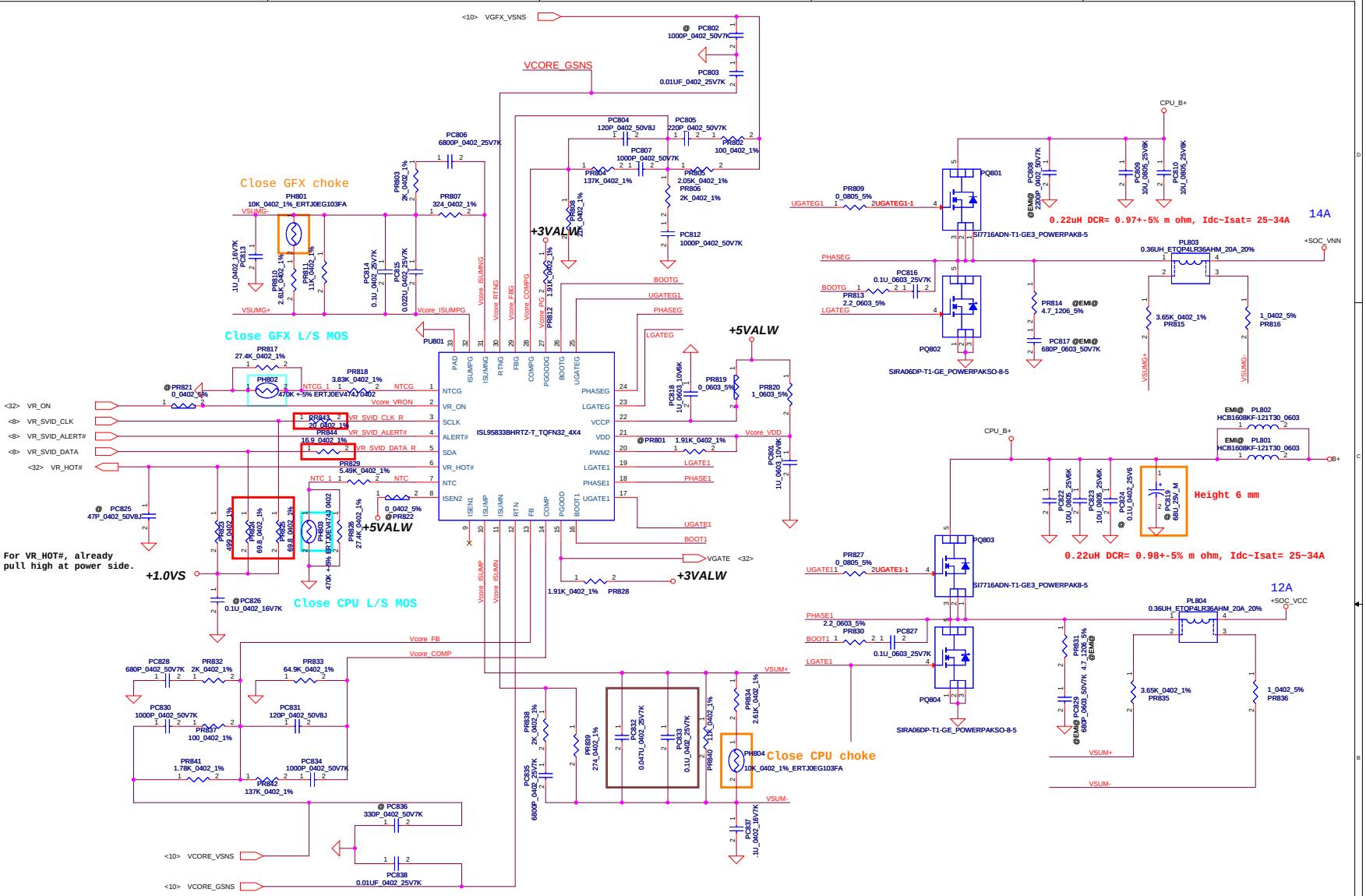
Security Classification	Compal Secret Data		
Issued Date	2012/04/27	Deciphered Date	2013/04/27

Compal Electronics, Inc.

Title: PWR- 12VSP

Size: Custom | Document Number: 4019RF | Rev: 1.0

Date: Tuesday, March 25, 2014 | Sheet 42 of 48



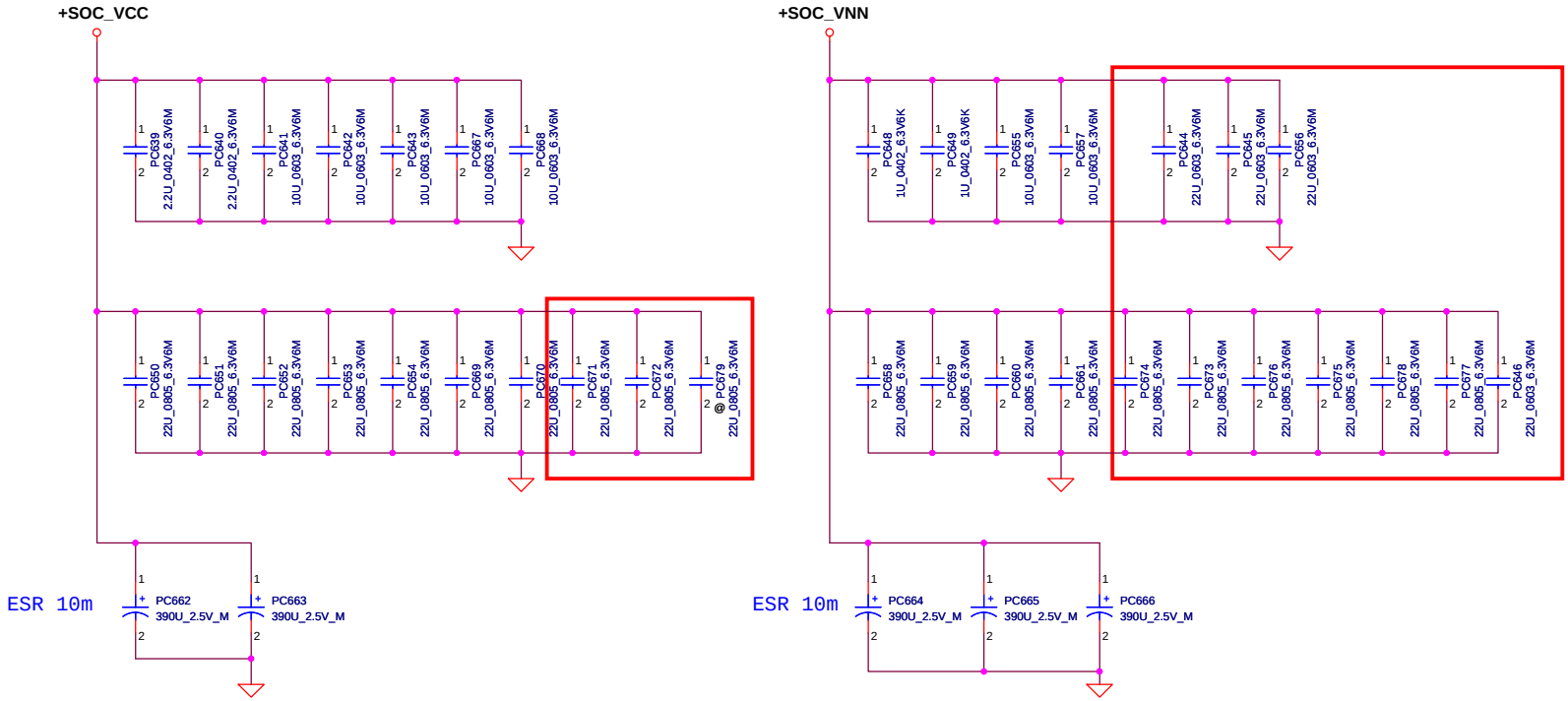
OCP:
+SO.C_VCC: 18A
+SOC_VNN: 21A
OTP:
VR_HOT at 110 deg.
VR_ALERT at 107 deg

+SOC_VCC:
Ipeak=12A; Fsw=450KHz; Vboot=1.1V
Iocp>=18A
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=10.5A
LIR=Delta IL/Ipeak=0.875
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=0.22uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1339.17uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

+SOC_VNN:
Ipeak=14A; Fsw=450KHz; Vboot=1.1V
Iocp>=21A
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=10.5A
LIR=Delta IL/Ipeak=0.75
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=0.22uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1667.7uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.81uF

Security Classification	Compal Secret Data		
Issued Date	2012/12/01	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	+SOC_VCC/+SOC_VNN
Size: Custom	Document Number: 4019RF
Rev: 1.0	
Date:	Sheet 43 of 48



Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: **CPU Capacitor**

Size	Document Number	Rev
Custom	4019RF	1.0

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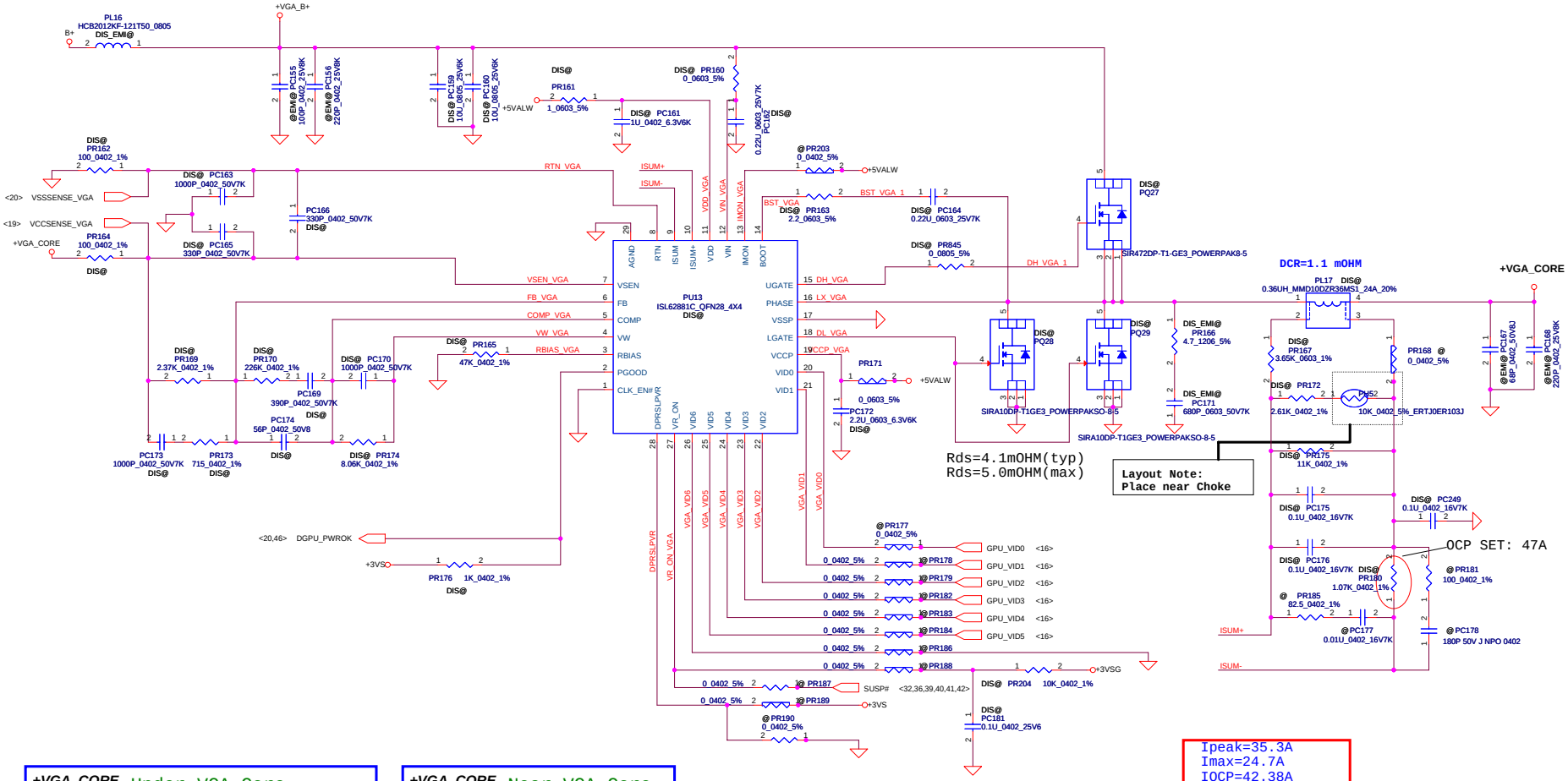


+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

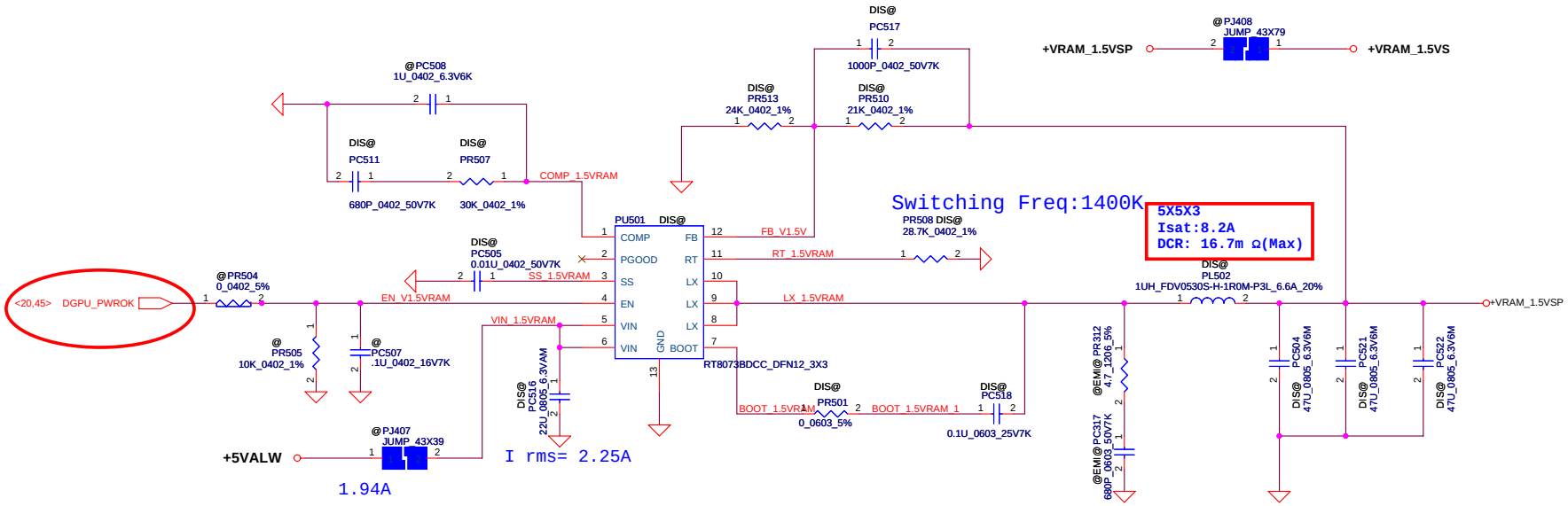
Ipeak=35.3A
Imax=24.7A
IOCP=42.38A
F=300kHZ
Total capacitor
1460u
ESR=1.8m ohm

+VGA_CORE:
Ipeak=35.3A;Imax=24.7A; Fsw=300KHz; Vboot=1.1V
Iocp(set)>=47A
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=9.625A
LIR=Delta IL/Ipeak=0.273
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=0.36uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11849uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=3.06uF

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title	VGA_CORE		
Size C	Document Number 4019RF		Rev 1.0
Date: Tuesday, March 25, 2014		Sheet 45 of 48	



Ipeak=5.5A, Imax=3.84A, Fsw=1400KHz
CL(min)=7A, CL(typ)=9A
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=0.75A
LIR=Delta IL/Ipeak=0.136
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=1.0uH
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.65uF

Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR-VRAM_1.5VSP

Size	Document Number	Rev
Custom	4019RF	1.0

Date: Tuesday, March 25, 2014 | Sheet 46 of 48

POWER PIR (Product Improve Record)

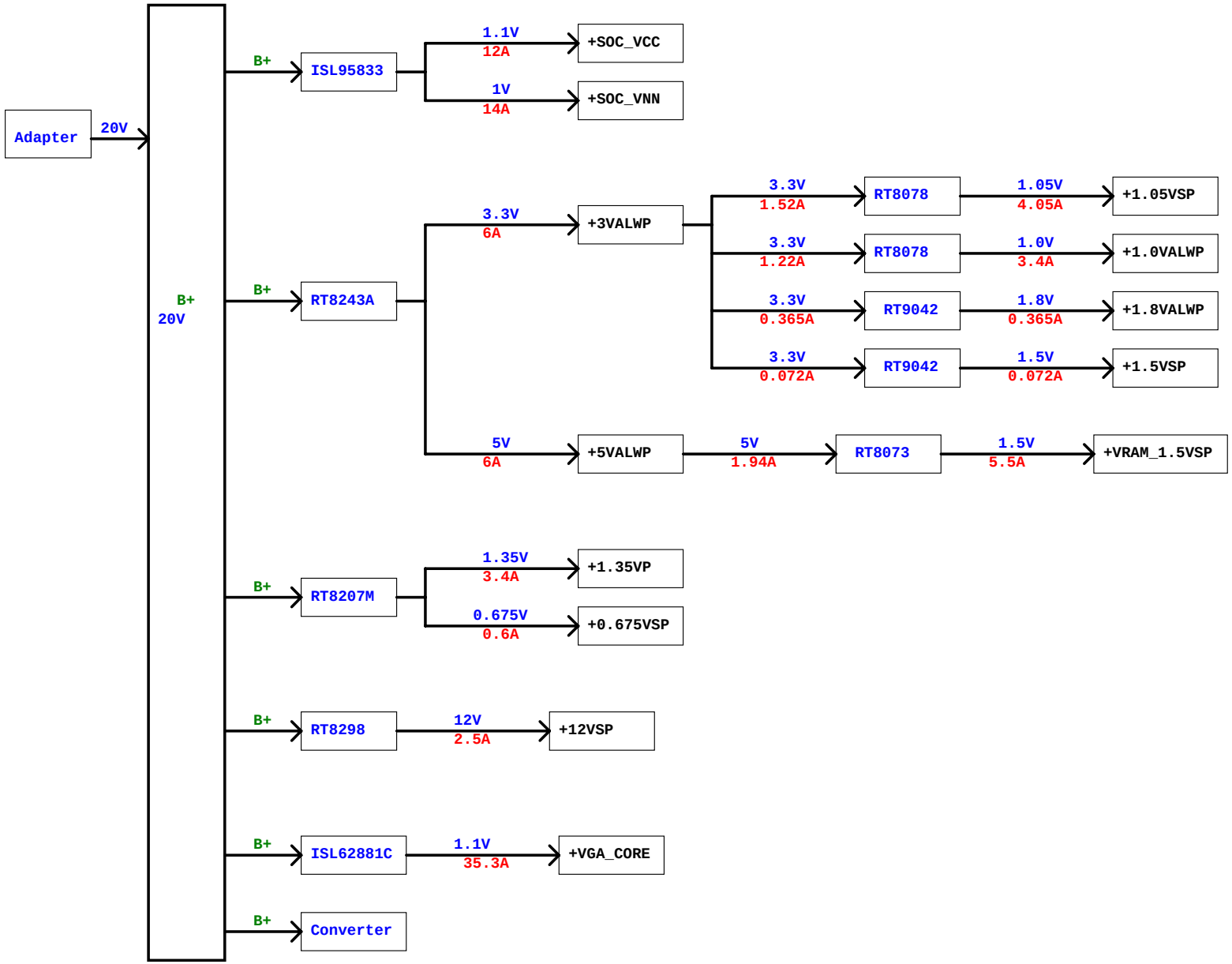
ZAA00 LA-XXXX SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/08/xx

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2013/08/12	43	PR814, PR833 change to 0402	module layout

NO	DATE	PAGE	MODIFICATION LIST(DVT)	PURPOSE
2	2013/09/14	39	change PR311 to 10K and pull high to +1.35V	design change
3	2013/09/17	43	change PC829 and PC817 to 0603 size	meet C38 MB design guide
4	2013/09/23	39	change PR306=12K, PR308=15K	meet voltage level
5	2013/09/23	44	add PC671,PC672,PC673,PC674,PC675,PC676, reserve PC677,PC678, PC679,PC646	meet Intel spec
6	2013/09/23	38	change PR418=12K, PR424=10K, PC417=un-pop	meet C38 MB design guide, light load Switching freq. >22KHz
7	2013/09/24	43	change PR807=324, PC815=0.022uF, PR839=274, PR837=100,PC830=1000pF, PL803=0.36uF, PL804=0.36uF, PC819= un-pop	meet Intel spec
8	2013/09/26	40,41	change PR403=20K, PR515=36K, PC406=0.1uF, PC510=0.1uF	meet Power sequence
9	2013/10/04	43	change PR802=100, PC805=220pF, PC812=1000pF	meet Intel spec
10	2013/10/04	37	change PC34=0.22uF, PC33=0.022uF	meet inrush spec
11	2013/10/08	46	change PC504=47uF, PC521=47uF, PC522=47uF, PR507=30k	meet Vram spec
12	2013/10/09	39	PC310=SGA00008S00	meet design spec

NO	DATE	PAGE	MODIFICATION LIST(PVT)	PURPOSE
13	2013/10/14	46	add PC517=1000pF	meet Vram spec
14	2013/10/29	43	1. Change the PC831 from 68pF to 120pF. 2. Change the PC834 from 150pF to 1000pF. 3. Change the PR838 from 649 Ohm to 2kOhm. 4. Change the PC804 from 68pF to 120pF. 5. Change the PC807 from 150pF to 1000pF. 6. Change the PR803 from 649 Ohm to 2kOhm.	solve can't boot issue
15	2013/11/12	38	1.PR418=120K 2.P424=100K	reduce current sink
16	2013/11/13	44	PC644,PC645,PC646,PC656= 22uF(0603 size) PU801= ISL95833B(SA00007IG00)	meet Intel spec
17	2013/11/18	38,39	PR425=10K PR306=11.8K	HW request
18	2013/11/21	38	PC839, PC840=0.1uF	EMC request

NO	DATE	PAGE	MODIFICATION LIST(Pre MP)	PURPOSE
1	2013/12/20	ALL	Change to short pad PR171,PR819 PR2,PR168,PR177,PR178,PR179, PR182,PR183,PR184,PR186,PR188, PR189,PR203,PR309,PR502,PR504, PR822,PR821,PR408	cost down



Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: **Power Rail**

Size	Document Number	Rev
Custom	4019RF	1.0

Date: Tuesday, March 25, 2014 Sheet 48 of 48