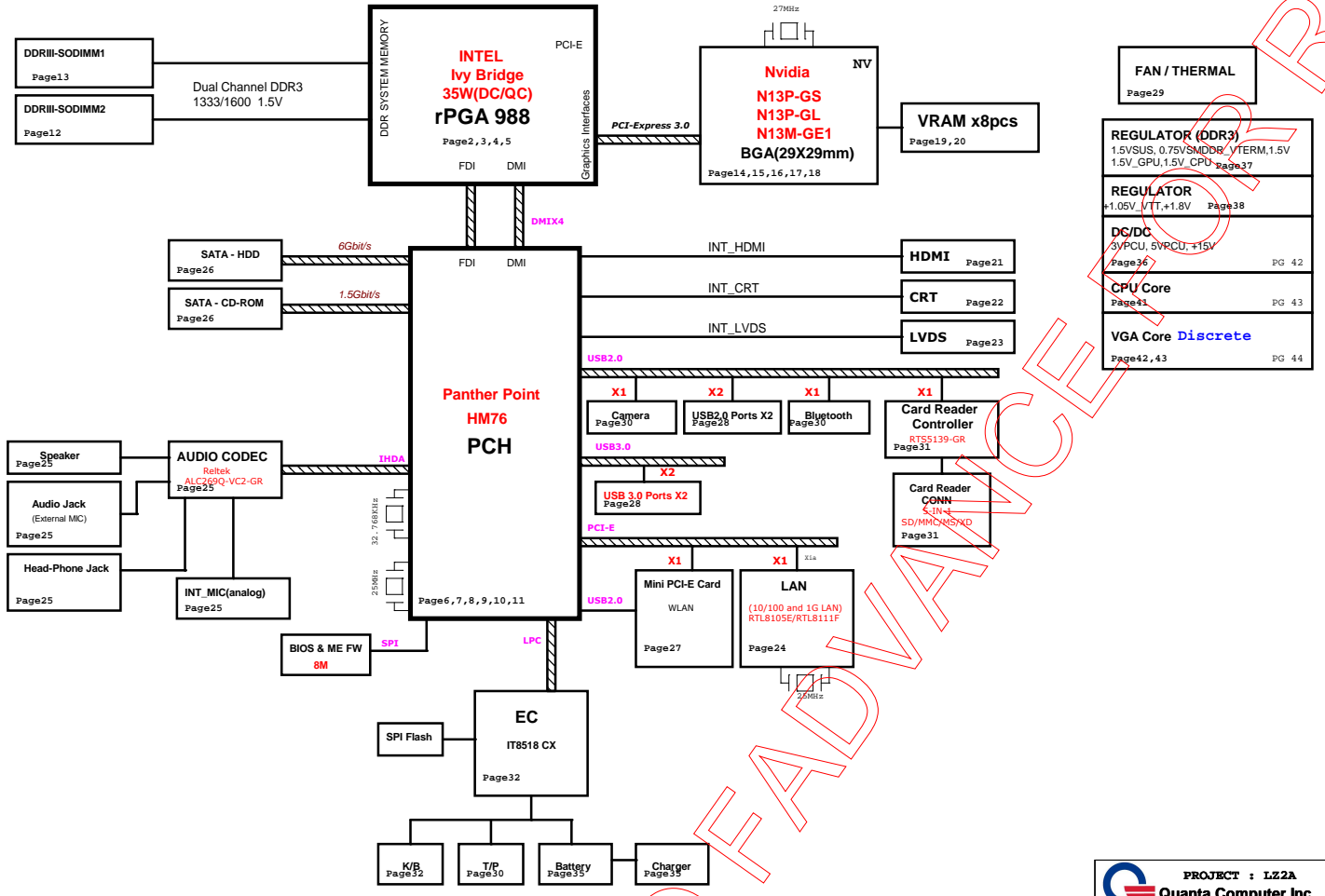


LZ3/LZ3A (Z580) Intel Chief River Platform (Optimus) Block Diagram

01



PROJECT : LZ2A
Quanta Computer Inc.

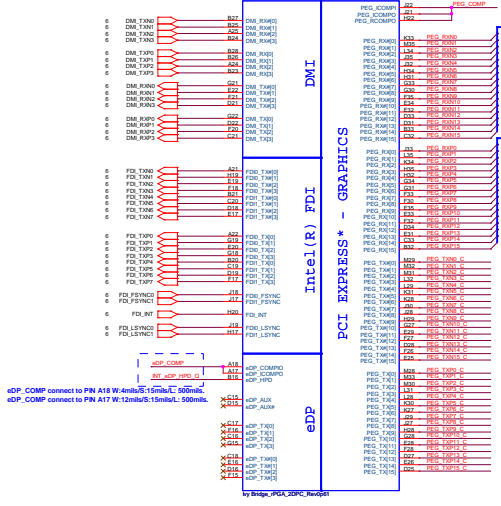
Size	Document Number	Rev
Custom	Front page	1A
Date:	Thursday, December 01, 2011	Sheet 1 of 43

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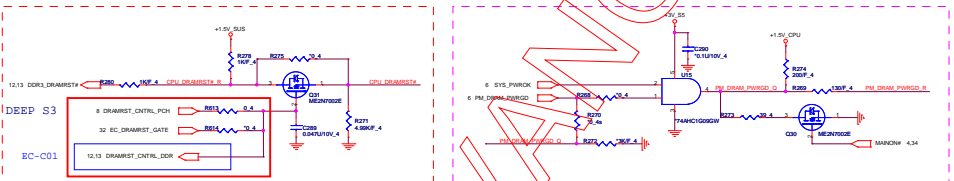
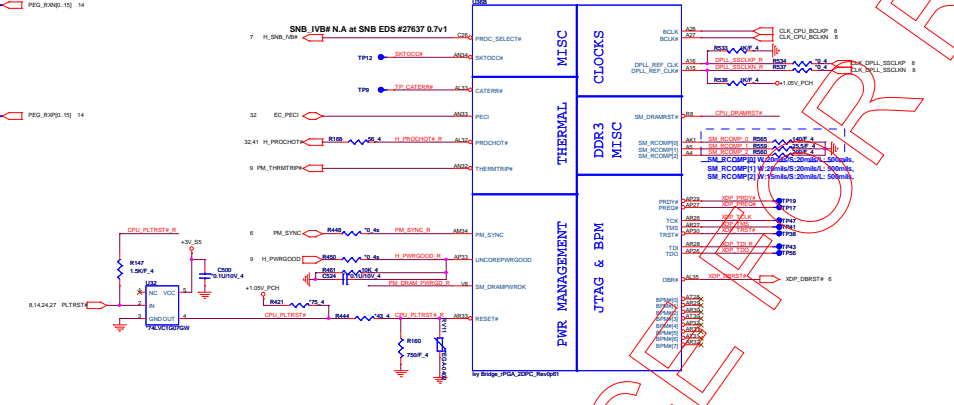
PEG_COMP connect to PIN H22&J22 W:4mb/s; 15mb/s; 500mb/s.
PEG_COMP connect to PIN J21 W:12mb/s; 15mb/s; 500mb/s.

467.8103343545 +1.0V_PCH
4.91021033335745 +1.0V_BUS
6.75102103335745 +1V_CPU
4.28 -1.0V_CPU

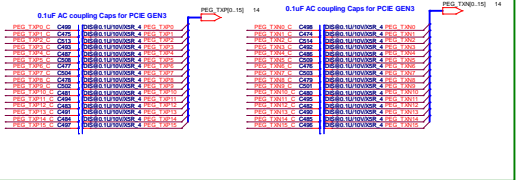
Ivy Bridge Processor (DMI, PEG, FDI)



Ivy Bridge Processor (CLK, MISC, JTAG)



PEG x16 (UMA Non-stuff)



DP & PEG Compensation

+1.0V_PCH -> [Circuit Diagram]
 PEG, ICOMPO and ICOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG, ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

+1.0V_PCH -> [Circuit Diagram]
 +1.0V_PCH -> [Circuit Diagram]
 eDP, COMPIO and ICOMPO signals should be routed near ball grid routed with typical impedance < 20 mohms

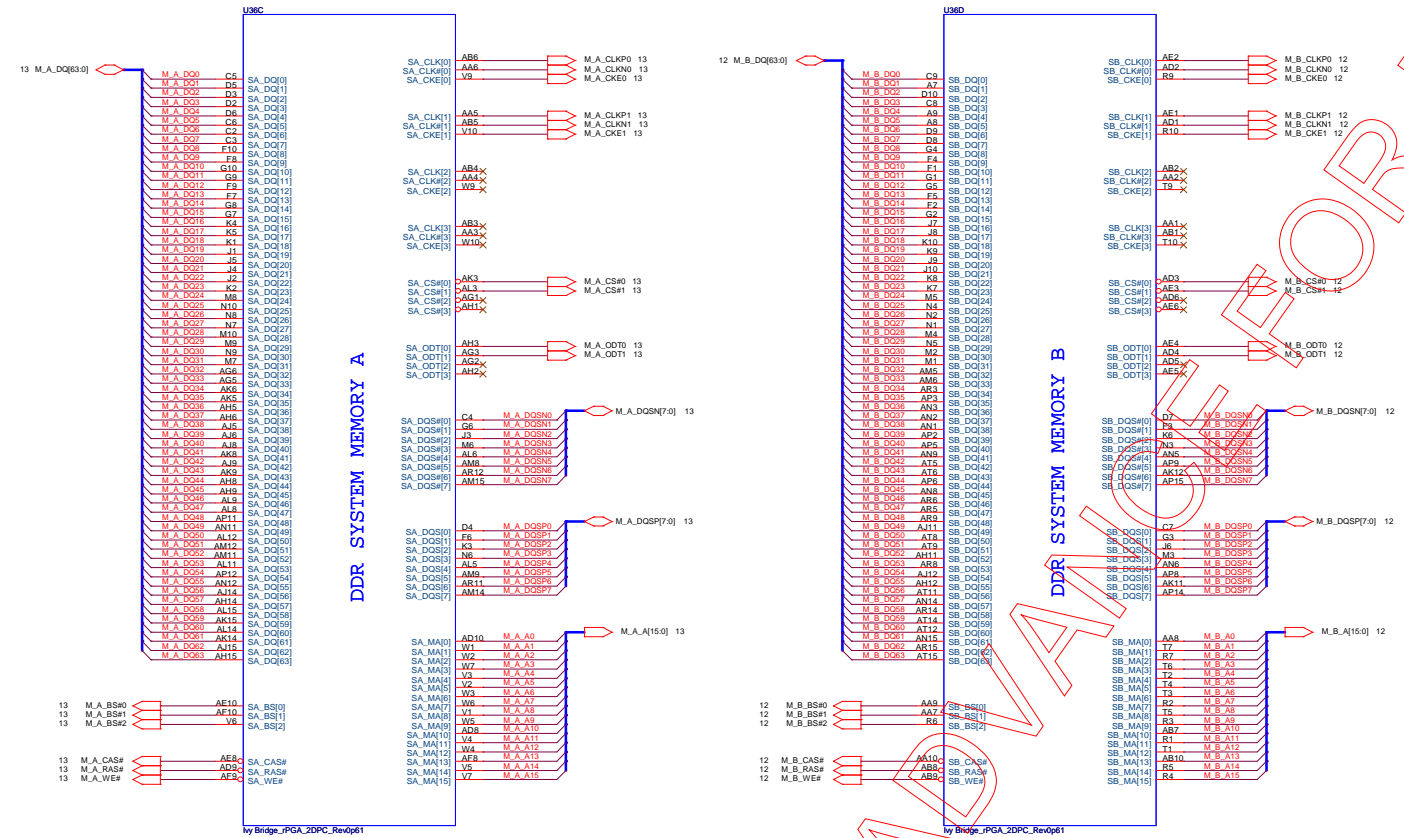
Processor pull-up(CPU)



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Ivy Bridge Processor (DDR3)

03



Ivy Bridge_PGA_ZDPC_Rev0p61

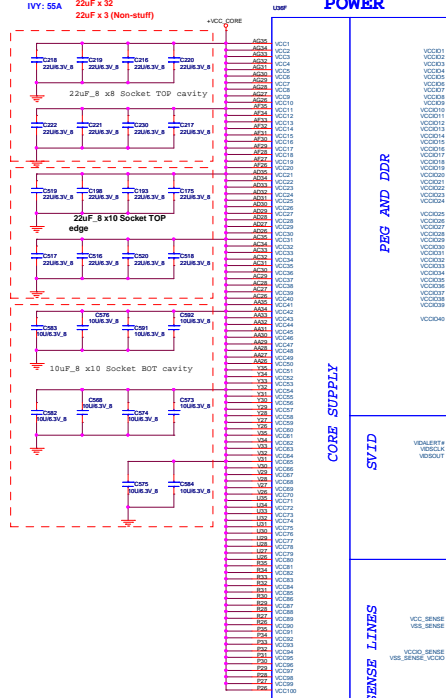
Ivy Bridge_PGA_ZDPC_Rev0p61

PROJECT : IZ2A
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Doc	Document Number	Rev
	IVY Bridge 2/4	1A
Date:	Thursday, December 01, 2011	Sheet 3 of 43

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CPU Core Power
SNB 55A
IVY: 55A



POWER

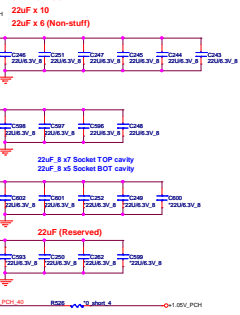
PEG AND DDR

CORE SUPPLY

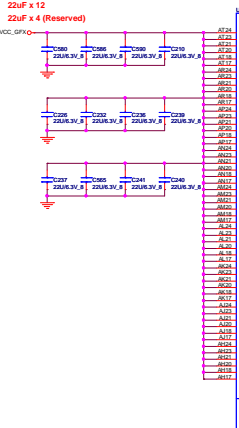
SVID

SENSE LINES

CPU VTT
SNB 45W: 6.5A
22uF x 10
22uF x 6 (Non-stuff)



CPU VGT
SNB 45W: 33A
22uF x 12
22uF x 4 (Reserved)



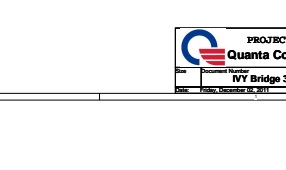
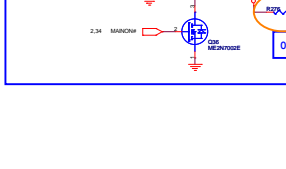
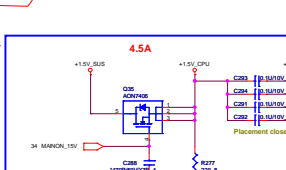
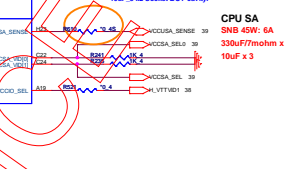
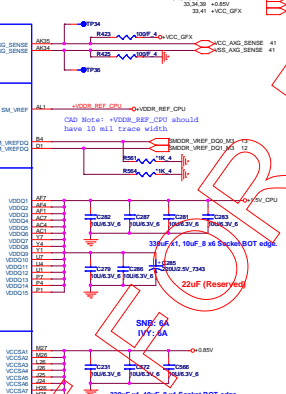
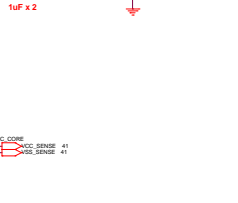
POWER

GRAPHICS

1.5V RAIL

MISC

CPU VCCPL
SNB 45W: 1.5A
330uF/6mohm x 1
10uF x 1
1uF x 2



CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6
SNB: 5A
IVY: 5A

CPU SA
SNB 45W: 6A
330uF/6mohm x 1
10uF x 3

Layout note: need routing together and ALERT need between CLK and DATA

Place PU resistor close to CPU

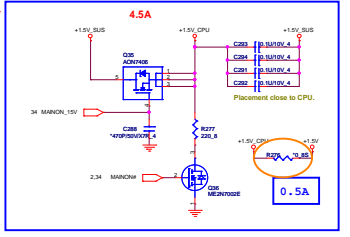
SVID CLK

SVID DATA

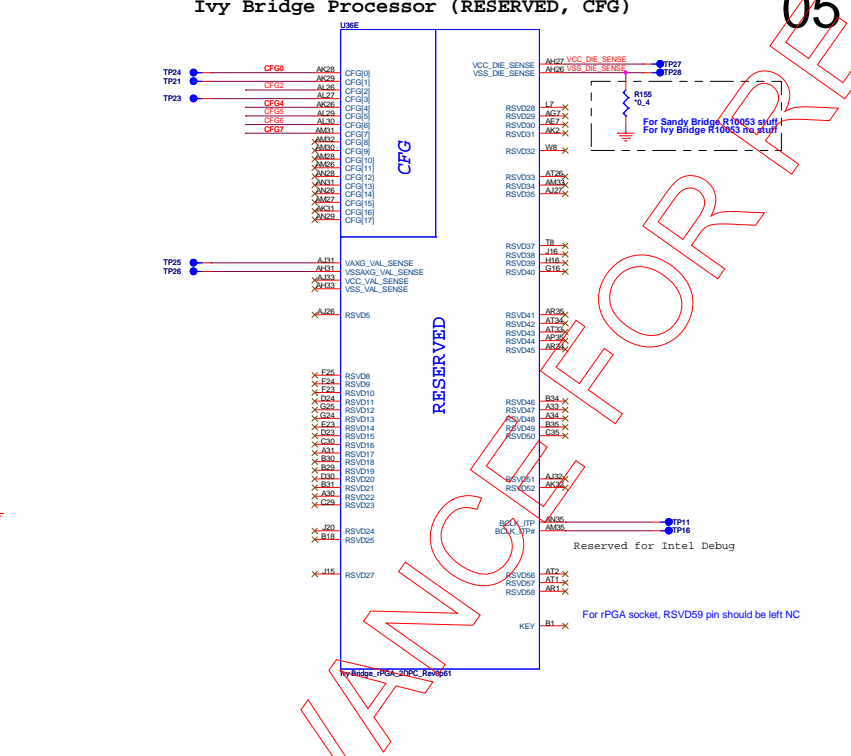
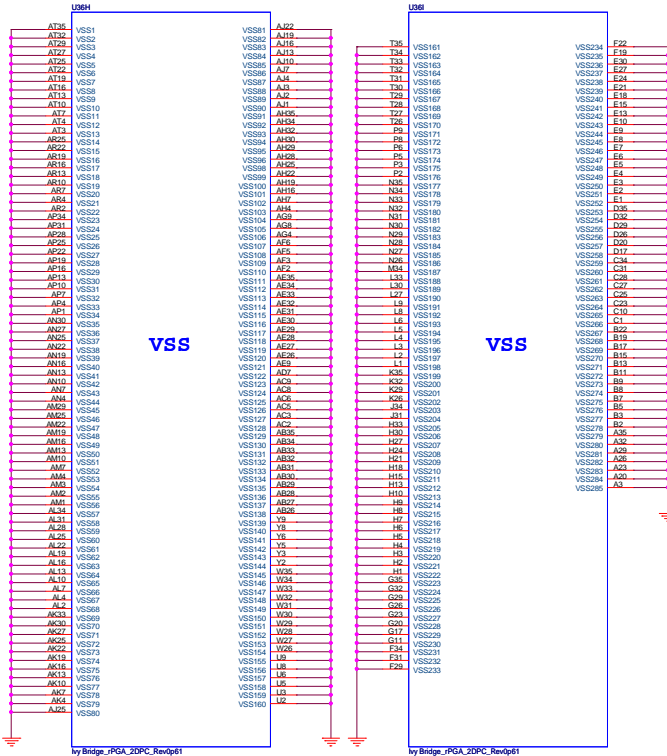
SVID ALERT

Close to VR

Close to VR

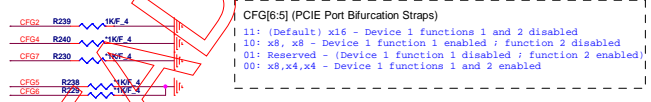


CONFIDENTIAL



Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xRESETB de assertion	PEG wait for BIOS training

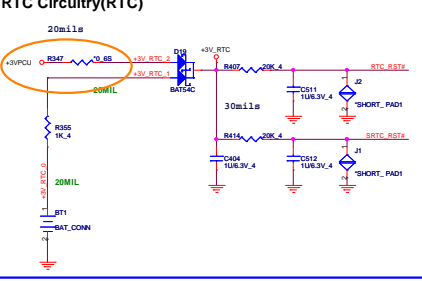


CFG6.5 (PCIe Port Bifurcation Straps)

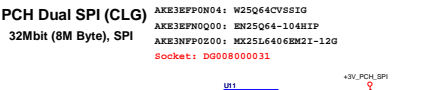
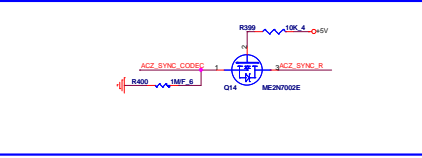
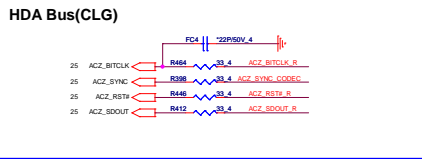
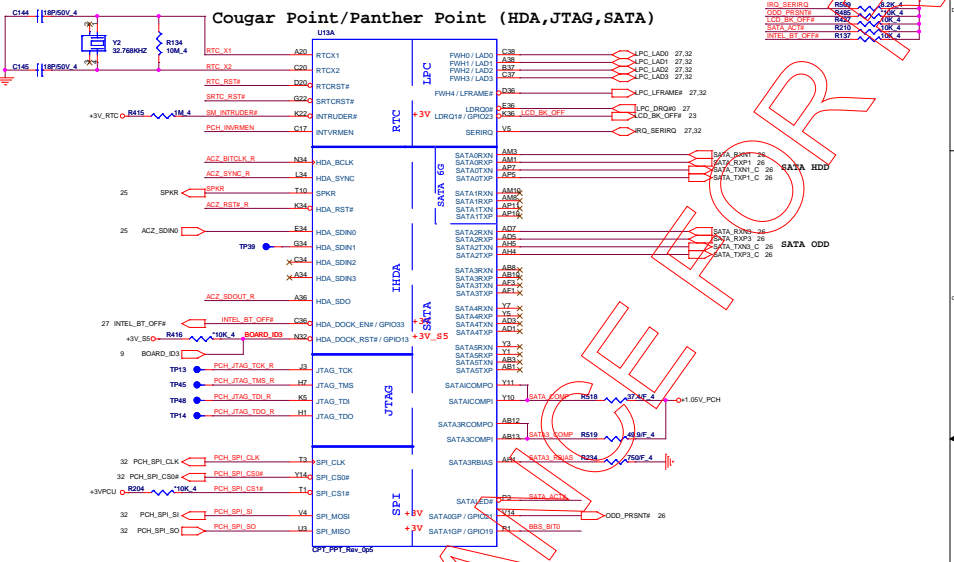
- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
- 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PROJECT : L2.2A
Quanta Computer Inc.
 Document Number
IVY Bridge 4/4
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PCH2 (CLG)



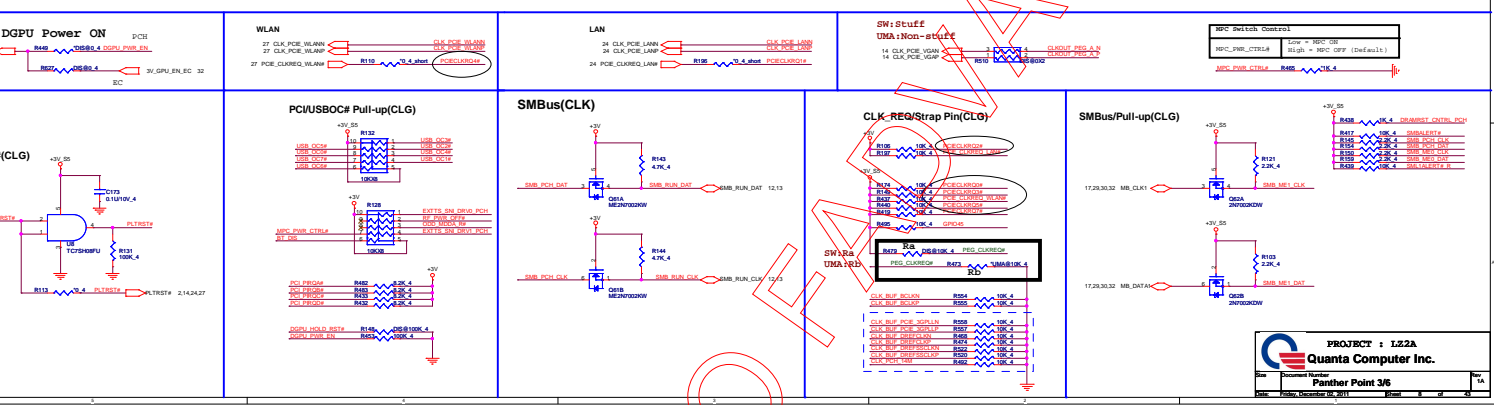
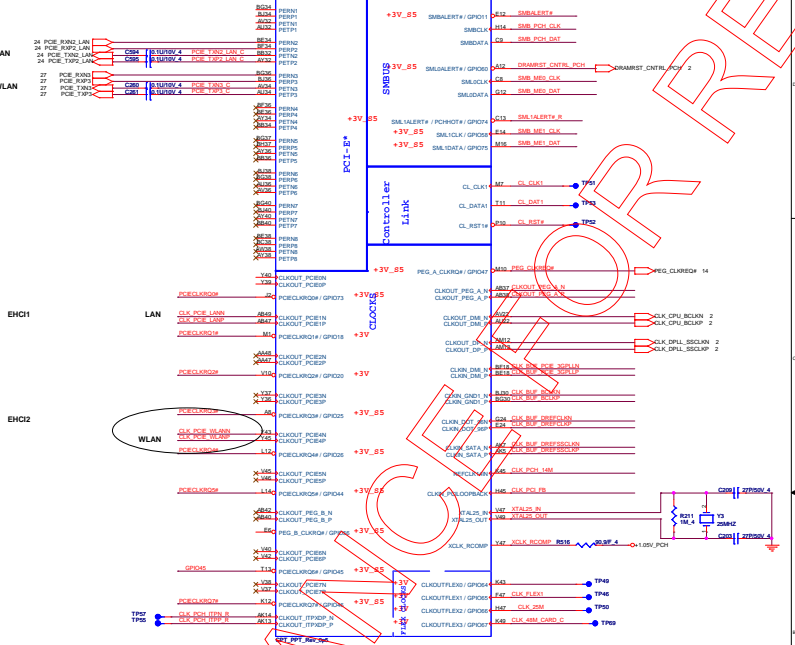
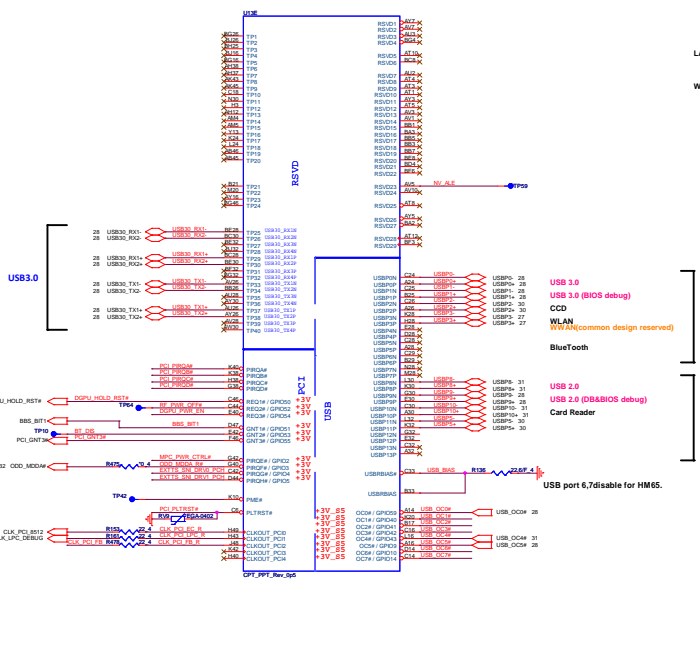
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	0	0	LPC
GNT1#	GNT0#	Boot Location										
1	1	SPI										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vcc 1 = Set to Vcc (weak pull-down 20K)									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.5V (weak pull-down) 1 = Support by 1.5V									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K) 1 = Enable									
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable									
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)									

PROJECT : I.22A
Quanta Computer Inc.
 Document Number: Panther Point 2/6
 Date: Thursday, December 17, 2015

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Cougar Point-M/Panther Point (PCI,USB,NVRAM)

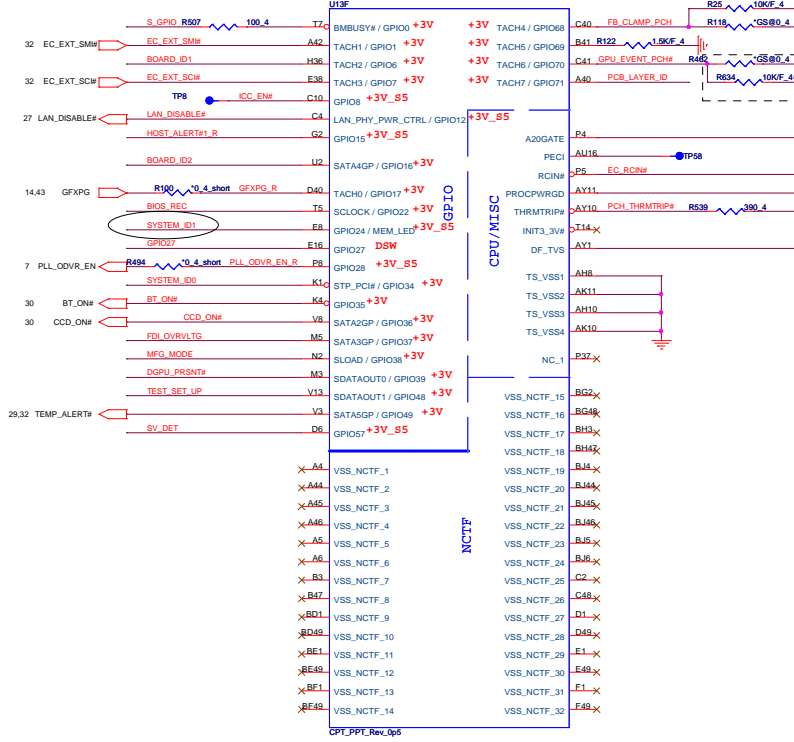


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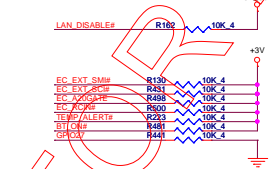
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

6.7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 2.6,7,8,10,27,31,34 +3V_SS +3V

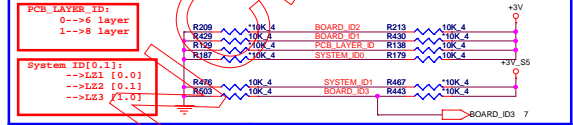
09



GPIO Pull-up/Pull-down(CLG)



Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVF	0	1	1
SOVP	1	0	0



PCB_LAYER ID:
0-->6 layer
1-->8 layer

System ID[0:1]:
-->L21 [0.0]
-->L22 [0.1]
-->L23 [1.0]

Arvin Wang update table on 9/19 14:12

L22	BOARD ID0 GPIO 71	SYSTEM ID0 GPIO 34	SYSTEM ID1 GPIO 24
6 Layer	0	0	1
8 Layer	1	0	1



TEST SET UP
High = Floating (Default)

MFG-TEST
MFG_MODE
High = Enable

SGPIO
S_GPIO
High = Enable

FDI TERMINATION VOLTAGE OVERRIDE
LOW - Tx, Rx terminated to same voltage

DMT TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

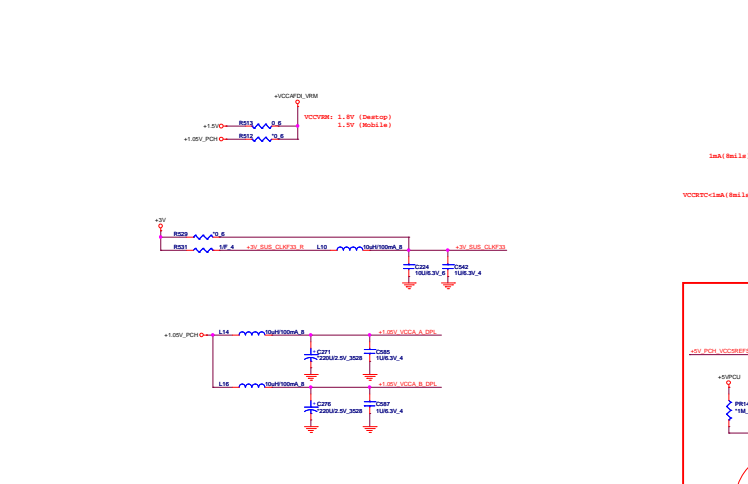
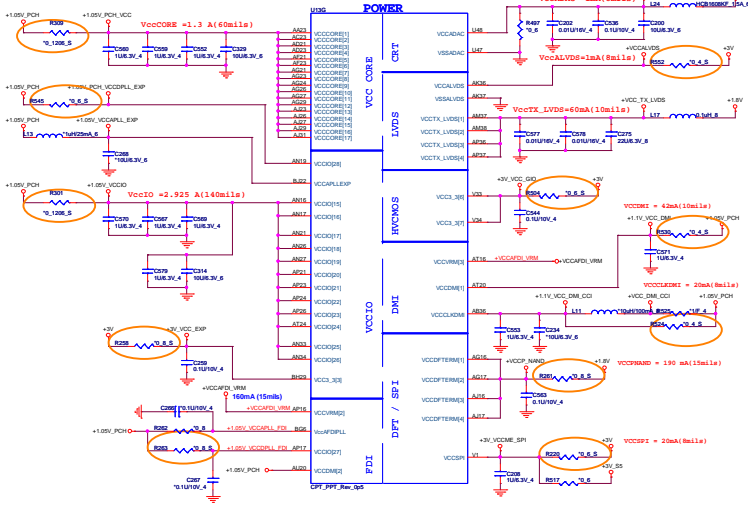
BIOS RECOVERY
High = Disable (Default)
Low = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

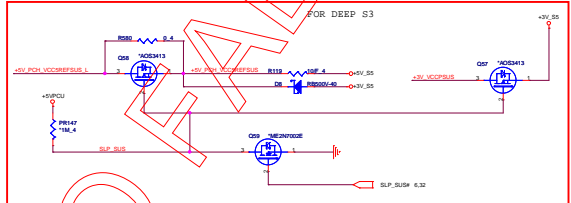
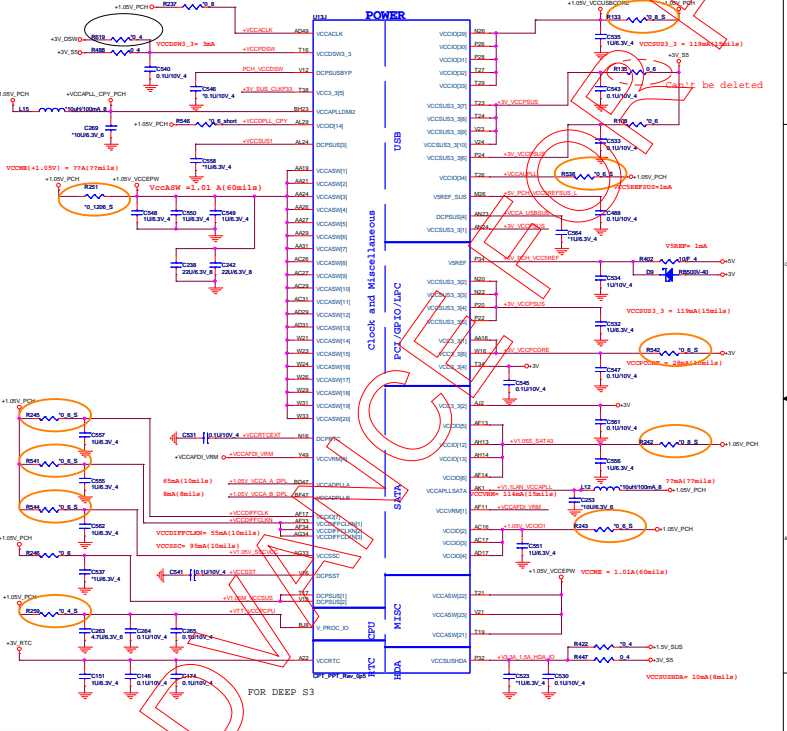
PROJECT : L22A
Quanta Computer Inc.
Panther Point 4/6

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Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (POWER)



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Quanta Computer Inc.
Panther Point S/E
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Cougar Point/Panther Point (GND)

U191

HE	VSS0	
AA17	VSS11	
AA2	VSS21	
AA3	VSS3	
AA3A	VSS4	
AA34	VSS5	
AB11	VSS6	
AB14	VSS7	
AB3	VSS8	
AB4	VSS9	
AB5	VSS10	
AB6	VSS11	
AB7	VSS12	
AC19	VSS14	
AC2	VSS15	
AC3	VSS16	
AC4	VSS17	
AC34	VSS18	
AC48	VSS19	
AD10	VSS20	
AD11	VSS21	
AD12	VSS22	
AD13	VSS23	
AD19	VSS24	
AD24	VSS25	
AD28	VSS26	
AD27	VSS27	
AD33	VSS28	
AD34	VSS29	
AD36	VSS30	
AD37	VSS31	
AD38	VSS32	
AD39	VSS33	
AD4	VSS34	
AD42	VSS35	
AD43	VSS36	
AD45	VSS37	
AD46	VSS38	
AD8	VSS39	
AE2	VSS40	
AE3	VSS41	
AF10	VSS42	
AF12	VSS43	
AF14	VSS44	
AF16	VSS45	
AF18	VSS46	
AF19	VSS47	
AF24	VSS48	
AF26	VSS49	
AF27	VSS50	
AF29	VSS51	
AF31	VSS52	
AF38	VSS53	
AF4	VSS54	
AF42	VSS55	
AF46	VSS56	
AF5	VSS57	
AF7	VSS58	
AF8	VSS59	
AG19	VSS60	
AG2	VSS61	
AG31	VSS62	
AG48	VSS63	
AG49	VSS64	
AH11	VSS65	
AH3	VSS66	
AH38	VSS67	
AH39	VSS68	
AH40	VSS69	
AH42	VSS70	
AH46	VSS71	
AH7	VSS72	
AJ19	VSS73	
AJ21	VSS74	
AJ24	VSS75	
AJ33	VSS76	
AJ34	VSS77	
AK12	VSS78	
AK3	VSS79	

DPT_PPT_Rev.1p5

U198

AY4	VSS159	
AY42	VSS160	
AY46	VSS161	
AY7A	VSS162	
B11	VSS163	
B15	VSS164	
B15A	VSS165	
B27	VSS166	
B31	VSS167	
B35	VSS168	
B39	VSS169	
B7	VSS170	
F4C	VSS171	
F4C	VSS172	
BB0	VSS173	
BB16	VSS174	
BB20	VSS175	
BB22	VSS176	
BB24	VSS177	
BB26	VSS178	
BB30	VSS179	
BB4	VSS180	
BB6	VSS181	
BC14	VSS182	
BC18	VSS183	
BC2	VSS184	
BC22	VSS185	
BC26	VSS186	
BC32	VSS187	
BC36	VSS188	
BC38	VSS189	
BC40	VSS190	
BC42	VSS191	
BC46	VSS192	
BC50	VSS193	
BC54	VSS194	
BC58	VSS195	
BD22	VSS196	
BD26	VSS197	
BD40	VSS198	
BF10	VSS199	
BF12	VSS200	
BF16	VSS201	
BF20	VSS202	
BF22	VSS203	
BF24	VSS204	
BF26	VSS205	
BF28	VSS206	
BF30	VSS207	
BF32	VSS208	
BF34	VSS209	
BF36	VSS210	
BF38	VSS211	
BF42	VSS212	
BF46	VSS213	
BF48	VSS214	
BF54	VSS215	
BH11	VSS216	
BH14	VSS217	
BH15	VSS218	
BH17	VSS219	
BH20	VSS220	
BH22	VSS221	
BH31	VSS222	
BH35	VSS223	
BH39	VSS224	
BH43	VSS225	
BH47	VSS226	
BH7	VSS227	
D3	VSS228	
D12	VSS229	
D16	VSS230	
D18	VSS231	
D22	VSS232	
D24	VSS233	
D26	VSS234	
D30	VSS235	
D34	VSS236	
D38	VSS237	
D42	VSS238	
D46	VSS239	
D48	VSS240	
D52	VSS241	
D56	VSS242	
D60	VSS243	
D64	VSS244	
G20	VSS245	
G24	VSS246	
G28	VSS247	
G36	VSS248	
G48	VSS249	
H12	VSS250	
H16	VSS251	
H22	VSS252	
H26	VSS253	
H30	VSS254	
H32	VSS255	
H34	VSS256	
H4	VSS257	
F4	VSS258	

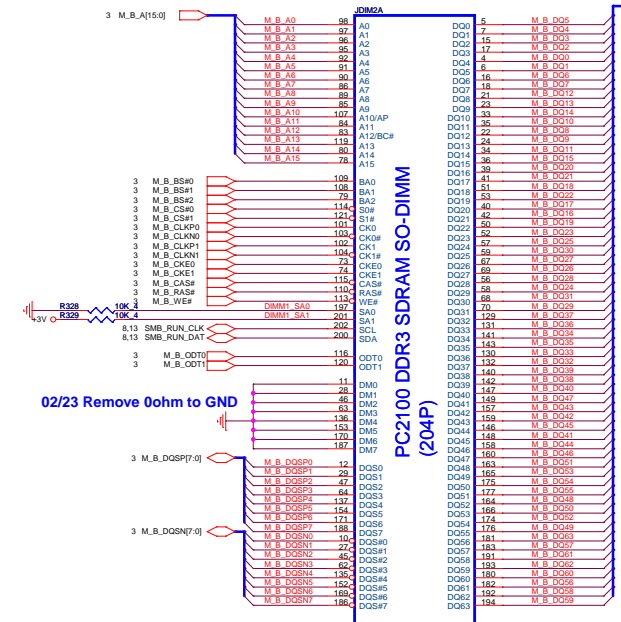
DPT_PPT_Rev.1p5

H46	VSS259	
K18	VSS260	
K28	VSS261	
K30	VSS262	
K36	VSS263	
K7	VSS264	
L18	VSS265	
L20	VSS266	
L26	VSS267	
L28	VSS268	
L36	VSS269	
L48	VSS270	
M12	VSS271	
M16	VSS272	
M18	VSS273	
M22	VSS274	
M24	VSS275	
M30	VSS276	
M32	VSS277	
M34	VSS278	
M38	VSS279	
M4	VSS280	
M42	VSS281	
M46	VSS282	
M6	VSS283	
M8	VSS284	
M18	VSS285	
P30	VSS286	
P11	VSS287	
P16	VSS288	
T33	VSS289	
T40	VSS290	
P40	VSS291	
P42	VSS292	
P47	VSS293	
R2	VSS294	
R48	VSS295	
T31	VSS296	
T31	VSS297	
T4	VSS298	
T4	VSS299	
U24	VSS300	
T46	VSS301	
V26	VSS302	
V27	VSS303	
V28	VSS304	
V11	VSS305	
V17	VSS306	
V22	VSS307	
V31	VSS308	
V36	VSS309	
V38	VSS310	
V43	VSS311	
V7	VSS312	
V17	VSS313	
V17	VSS314	
V19	VSS315	
W2	VSS316	
W27	VSS317	
W48	VSS318	
Y12	VSS319	
Y38	VSS320	
Y4	VSS321	
Y42	VSS322	
Y46	VSS323	
Y8	VSS324	
BC29	VSS325	
N24	VSS326	
A3	VSS327	
BE7	VSS328	
B43	VSS329	
BE10	VSS330	
BE41	VSS331	
G14	VSS332	
H16	VSS333	
T36	VSS334	
BC22	VSS335	
C22	VSS336	
AP15	VSS337	
M14	VSS338	
AP3	VSS339	
AP1	VSS340	
BE16	VSS341	
BE16	VSS342	
BC28	VSS343	
BC28	VSS344	
BC28	VSS345	
BC28	VSS346	
BC28	VSS347	
BC28	VSS348	
BC28	VSS349	
BC28	VSS350	
BC28	VSS351	
BC28	VSS352	

PROJECT : IZ2A
 Quanta Computer Inc.
 Panther Point 6/6
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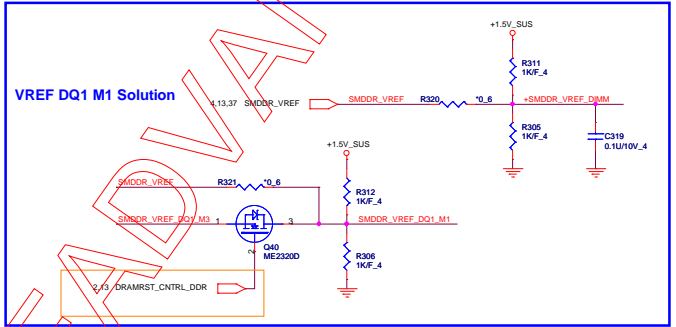
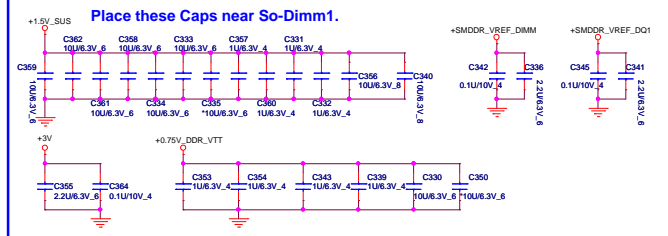
DDR_RVS (DDR)



	STD 4H	STD 8H
FOX		
LTK	DGKM4000004	DGKM4000097
SUY		
MLX	DGKM4000011	DGKM4000080

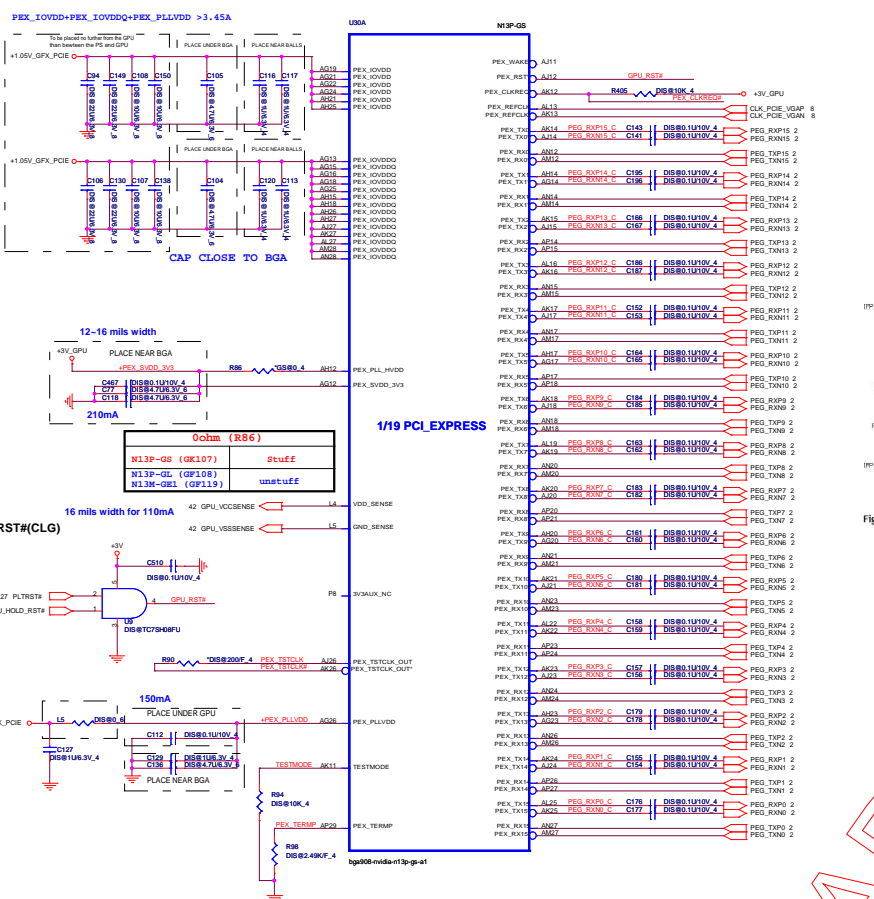
Standard 8H type:DDR-C-2013310-204p-1

DDR3 DIMM0_1H=4.0_RVS
DDR-78279-001_RVS-204P
DGKM0000100
SOCKET DDR3 SO-DIMM(204P,H4.0,REV1)



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12



All GPU power rails must ramp up after VDD33. The following conditions must be met:

- ▶ INVDD0 > 0
- ▶ IFBVDDQ > 0
- ▶ IFVDD > 0
- ▶ IFPx_JOVDD > 0
- ▶ IFPy_JOVDD > 0
- ▶ The ramp time for any rail must be more than 40 ns.

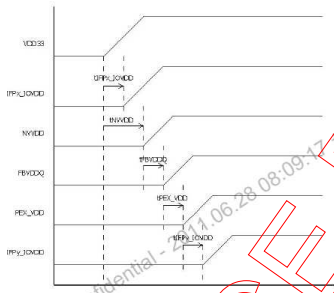


Figure 17. Recommended Power On Sequencing Order

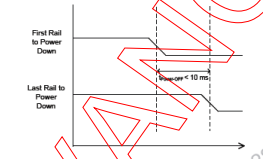
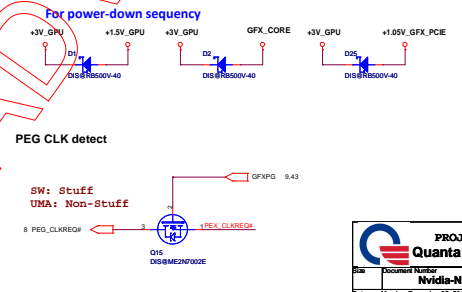


Figure 18. Recommended Power Off Sequencing Order



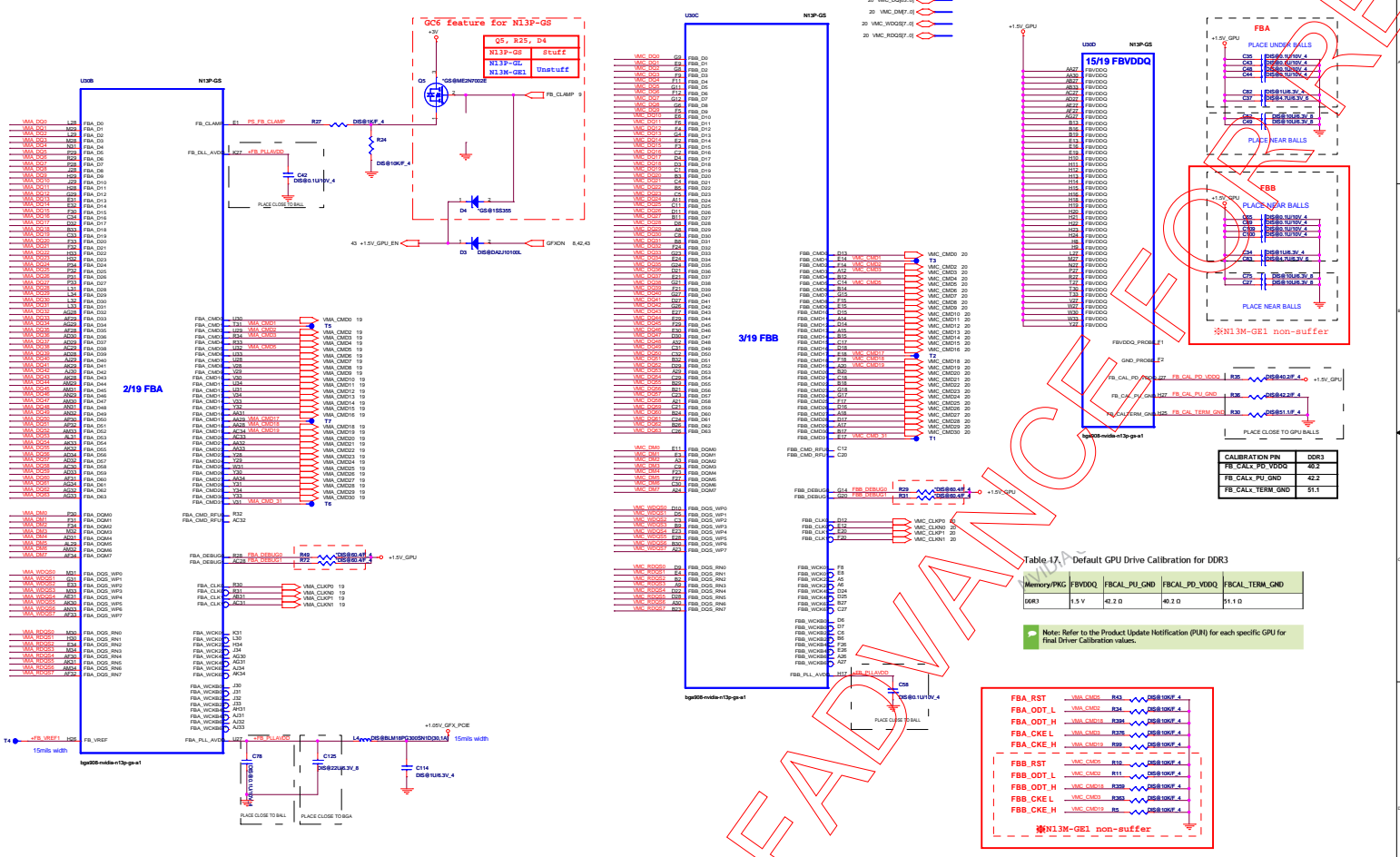
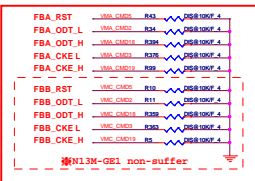


Table 17. Default GPU Drive Calibration for DDR3

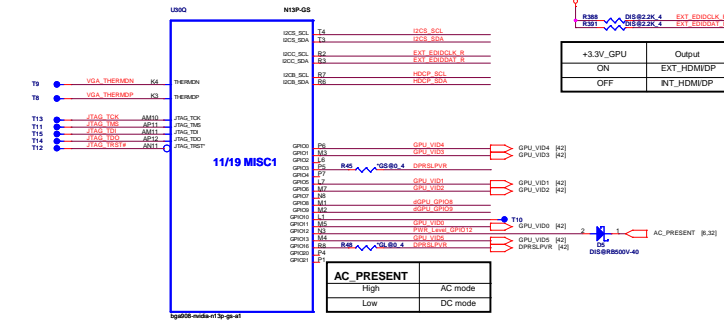
Memory/PKG	FBVDDQ	FBCL_PU_GND	FBCL_PD_VDDQ	FBCL_TERM_GND
DDR3	1.5 V	42.0 Ω	40.2 Ω	51.1 Ω

Note: Refer to the Product Update Notification (PUN) for each specific GPU for final Driver Calibration values.

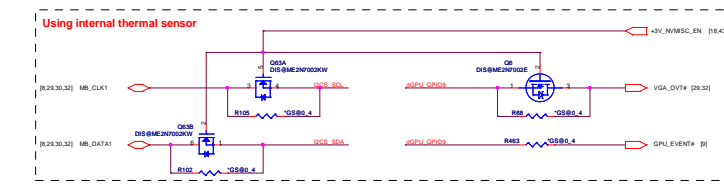


PROJECT : I.32A
Quanta Computer Inc.
 Infile-N13P GB4-12R(MEM IF)
 Rev: 1.0
 Date: 2011-08-10

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 NO



Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FS_B_SDR_SIZE	VGA_DEVICE
ROM_SCLK	PCI_DEVIO[4]	S0B_VINDOR	SLOTT_CLK_CFG
ROM_SI	RAMCFG[0]	RAMCFG[1]	RAMCFG[0]
STRAP0	USER[3]	USER[2]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP2	PCI_DEVIO[3]	PCI_DEVIO[2]	PCI_DEVIO[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCI_MAX_SPEED

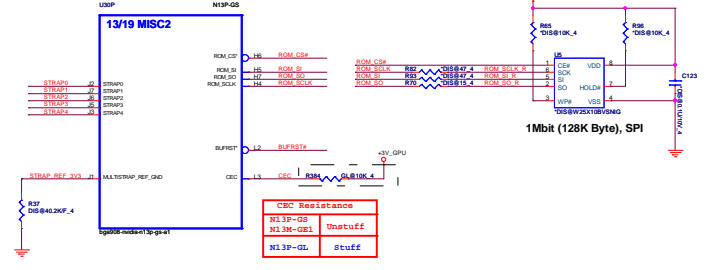
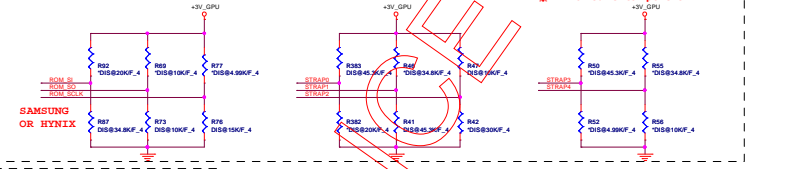


VRAM Configuration Table

VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG (3:0)	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646G-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWT500		H5TQ2638FR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGWT502		K4W1G1646G-B11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5L2WT502		H5TQ1G43DFR-11C	0x2(0010)	R87 (15K ohm)

Table 5. Stuffing Options

GPU	Signal/Trail	Stuffing Option
N13P-GT/GS-LP, N14P-Q1-Q3	IDC and GPIO	No stuff FET Stuff 0Ω bypass resistor
Other N13P and N13M	IDC and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor



NVDD Table

	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
GPU_VB0	0 (R66)	0 (R66)	0 (R66)
GPU_VB1	0 (R62)	0 (R62)	0 (R62)
GPU_VB2	0 (R58)	1 (R59)	0 (R58)
GPU_VB3	0 (R57)	1 (R54)	0 (R57)
GPU_VB4	1 (R71)	0 (R49)	1 (R71)
GPU_VB5	1 (R385)	1 (R385)	1 (R385)

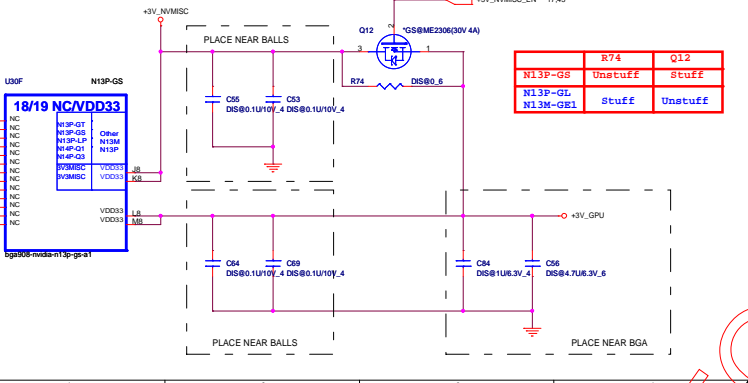
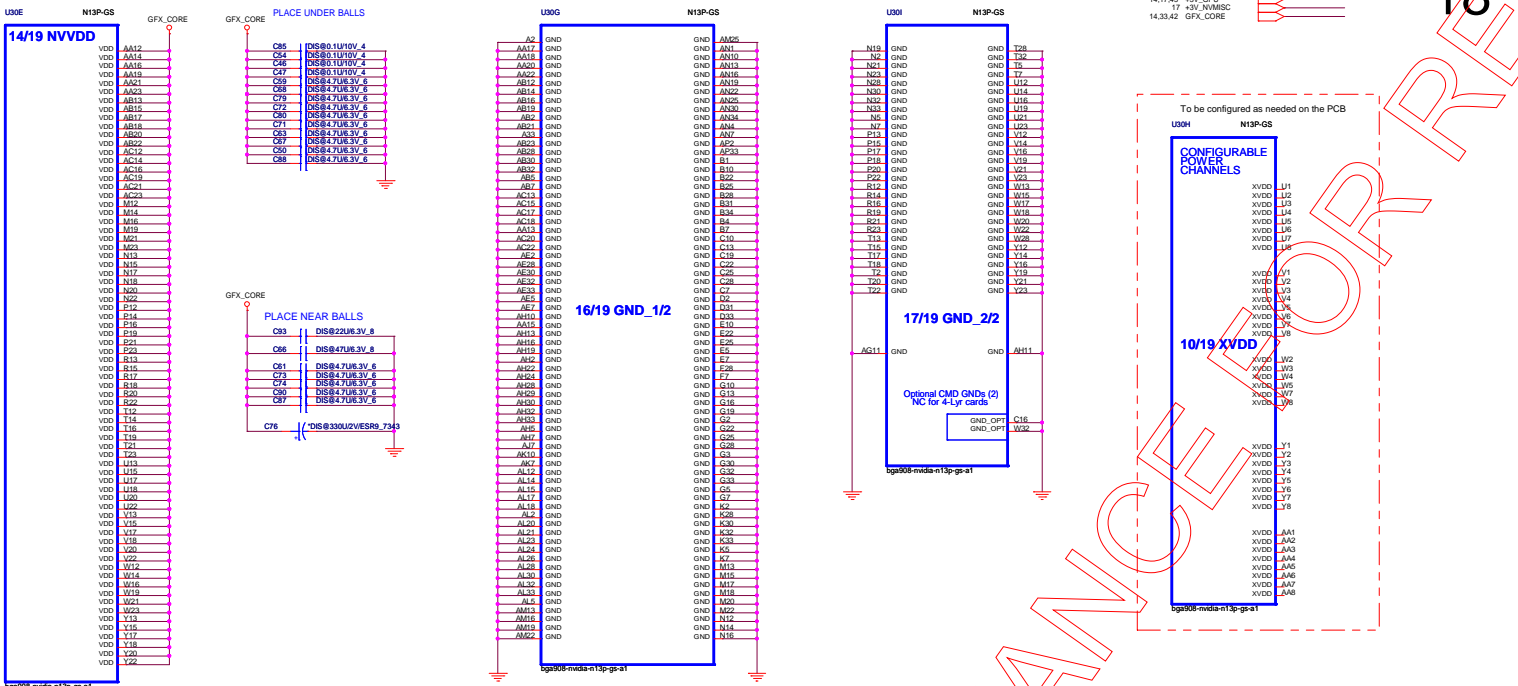
Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PE5-GL-N51 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/GS-LP and N14P-Q1-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PE5-GL/H51.

GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VB0	O	GPU Core VDD VB0
GPIO1	GPU_VB1	O	GPU Core VDD VB1
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase-Shedding
GPIO4	LCD_BL_EN	O	Panel Backlight Enable
GPIO5	GPU_VB1	O	GPU Core VDD VB1
GPIO6	GPU_VB2	O	GPU Core VDD VB2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERST	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VDD0	O	GPU Core VDD VDD0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overload input
GPIO13	GPU_VB5	O	GPU Core VDD VB5
GPIO14	HPD_AB	I	Hot Plug Detect for HPAB
GPIO15	HPD_C	I	Hot Plug Detect for HPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VDD
GPIO17	HPD_D	I	Hot Plug Detect for HPD
GPIO18	HPD_E	I	Hot Plug Detect for HPE
GPIO19	HPD_F	I	Hot Plug Detect for HPF
GPIO20	Reserved		
GPIO21	Reserved		

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N13P-GS	R74	Q12
N13P-GL	Unstuff	Stuff
N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

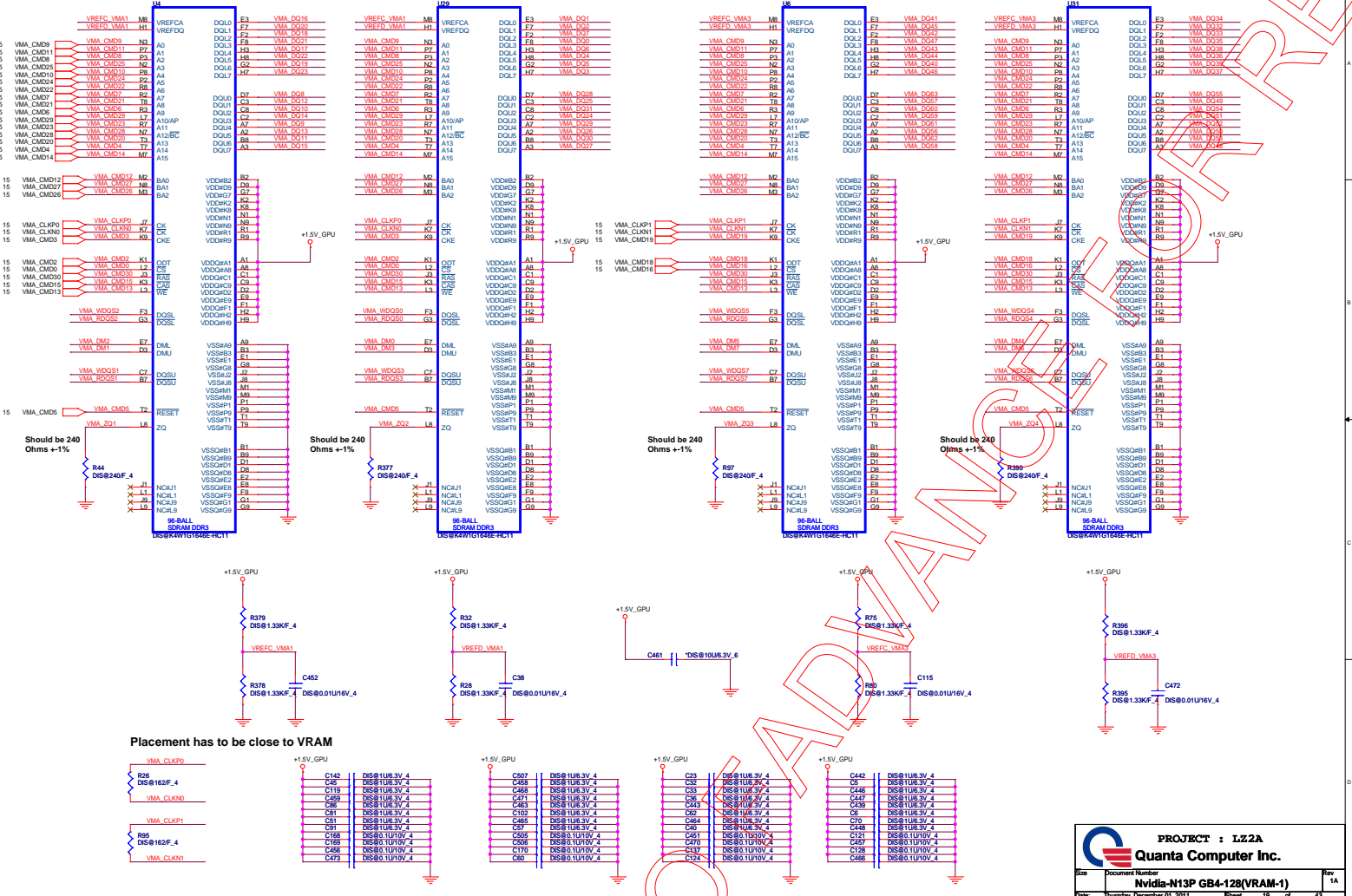
GPU	Signal/Rail	Stuffing Option
H13P-GT/-GS-LP, H14P-Q11-Q3	I2C and GPIO	No stuff FET
	3V3MISC	Stuff 00 bypass resistor
Other H13P and H13M	I2C and GPIO	Stuff FET
	3V3MISC	No stuff 00 bypass resistor

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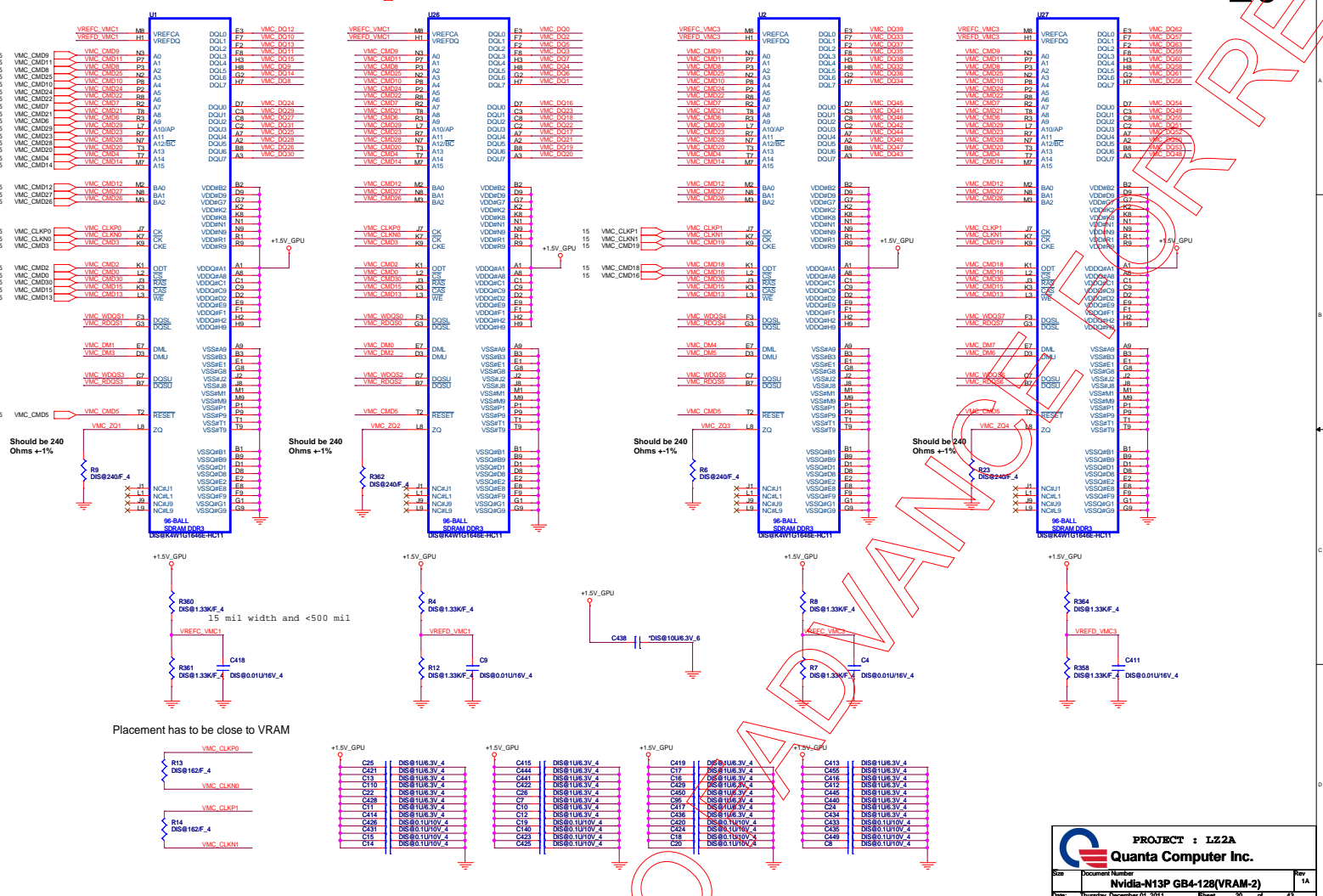
Rev 1A

Thursday, December 01, 2011

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PROJECT : L2.2A
Quanta Computer Inc.
 Document Number: **Nvidia-N13P GB4-128(VRAM-1)**
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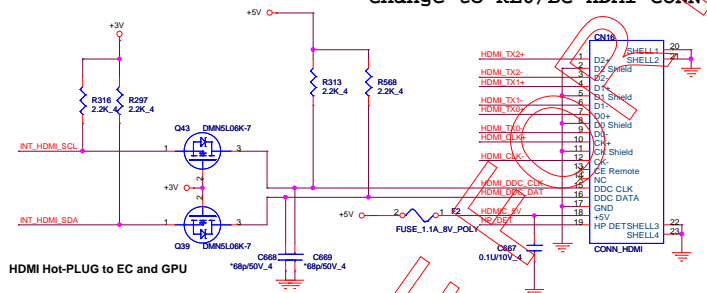
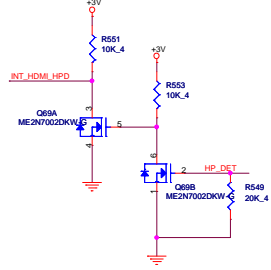


Placement has to be close to VRAM

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Quanta Computer Inc.
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 Nvidia-N13P GB4-128(VRAM-2)
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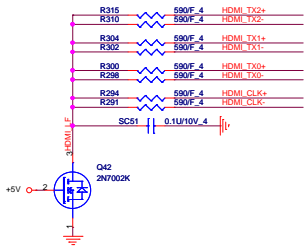
6	INT_HDMI_TXDP2	C820	0.1u/10V_4	HDMI_TX2+
6	INT_HDMI_TXDN2	C819	0.1u/10V_4	HDMI_TX2-
6	INT_HDMI_TXDP1	C818	0.1u/10V_4	HDMI_TX1+
6	INT_HDMI_TXDN1	C817	0.1u/10V_4	HDMI_TX1-
6	INT_HDMI_TXDP0	C816	0.1u/10V_4	HDMI_TX0+
6	INT_HDMI_TXDN0	C815	0.1u/10V_4	HDMI_TX0-
6	INT_HDMI_TXCP	C813	0.1u/10V_4	HDMI_CLK+
6	INT_HDMI_TXCN	C811	0.1u/10V_4	HDMI_CLK-

6 INT_HDMI_SCL INT_HDMI_SCL
6 INT_HDMI_SDA INT_HDMI_SDA
6 INT_HDMI_HPD INT_HDMI_HPD

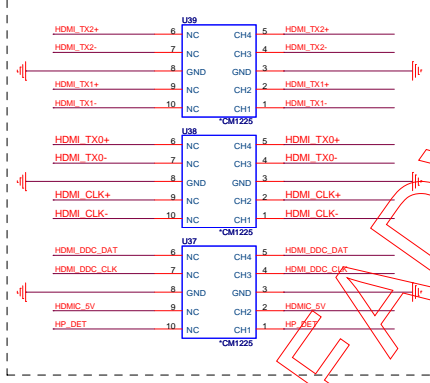


HDMI Hot-PLUG to EC and GPU

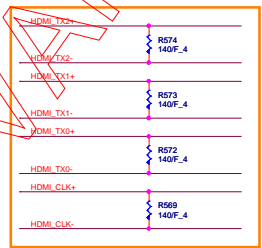
Change to KL6/BC HDMI CONN



For ESD



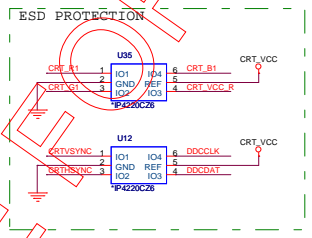
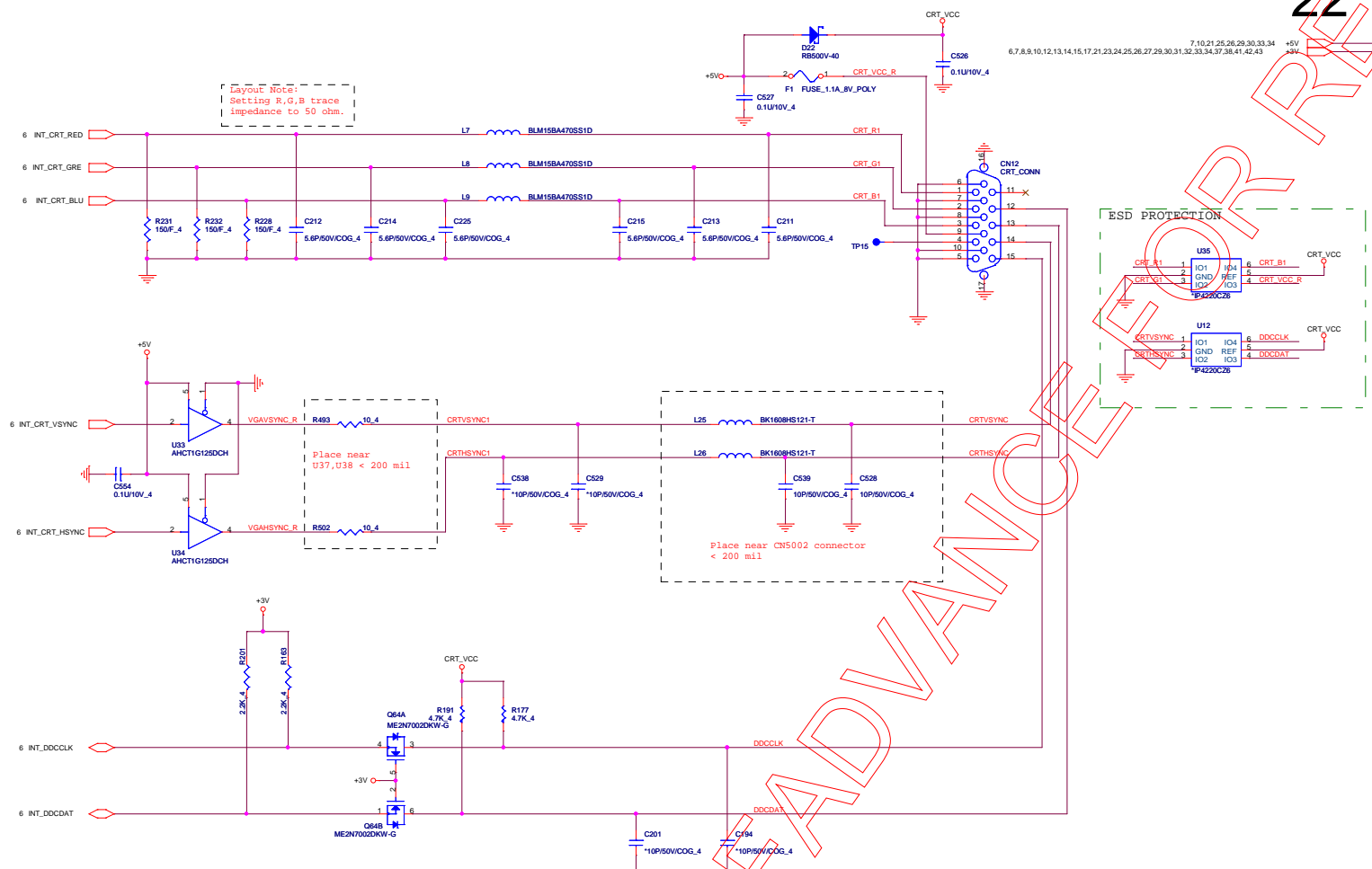
EMI reserve for HDMI



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Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

7,10,21,25,26,29,30,33,34
6,7,8,9,10,12,13,14,15,17,21,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43

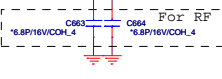
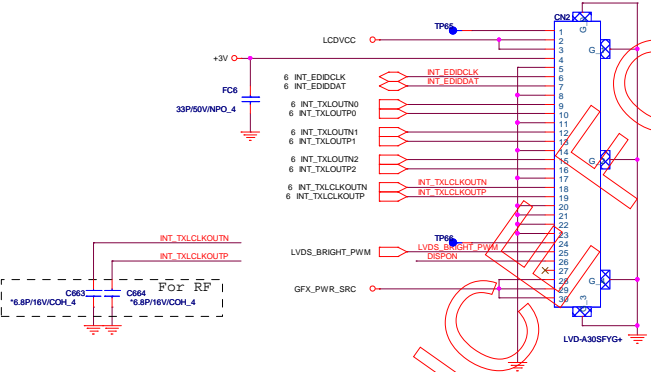
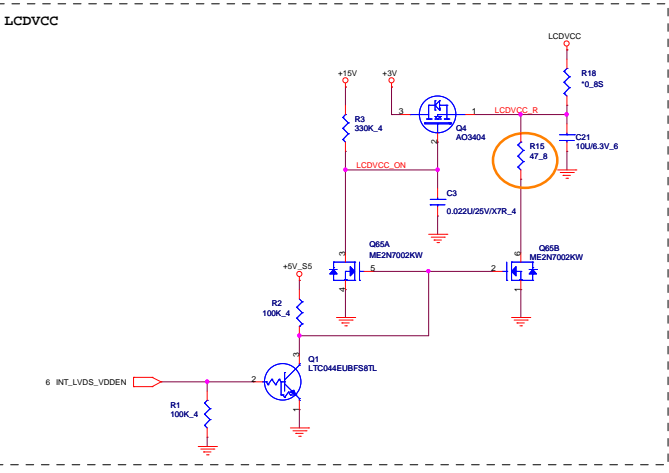
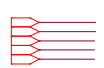


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Quanta Computer Inc.

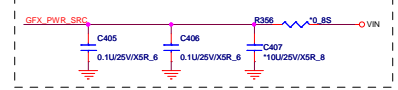
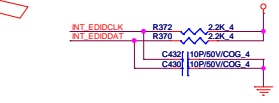
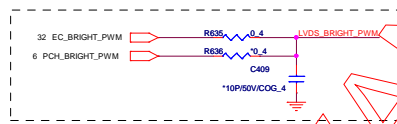
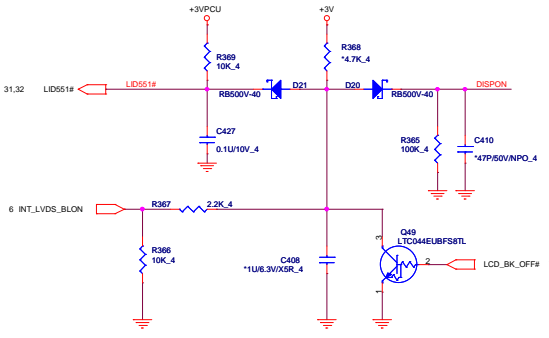
Size	Account Number	Rev
Custom	CRT_CONN	1A
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26,30,34,36,43 +1V
37,38,41,42,43 +3V
10,26,28,31,33,34 +5V_S5
6,7,24,26,27,31,32,34,35,36,40 +3VPCU
33,35,36,37,38,39,41,42 VIN



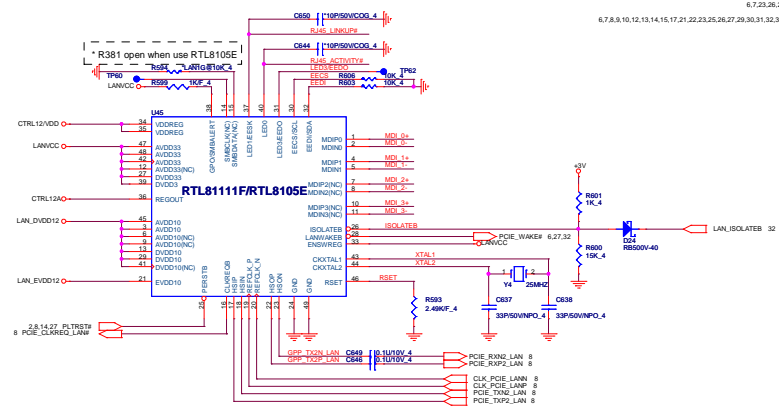
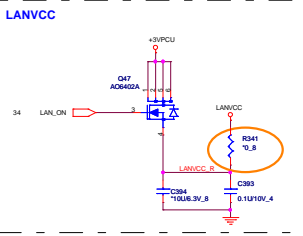
back light



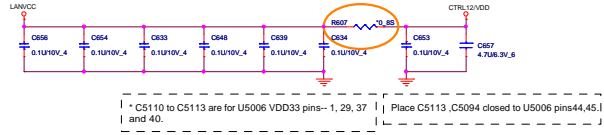
PROJECT : LZ2A
Quanta Computer Inc.

Size	Account Number	Rev
Custom	LCD CONN	1A
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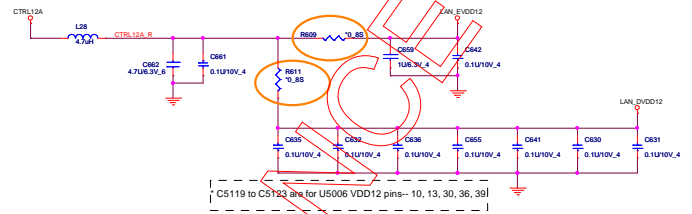


* C476 and C472 are for U24 LAN_VDDIO2 pin 21.



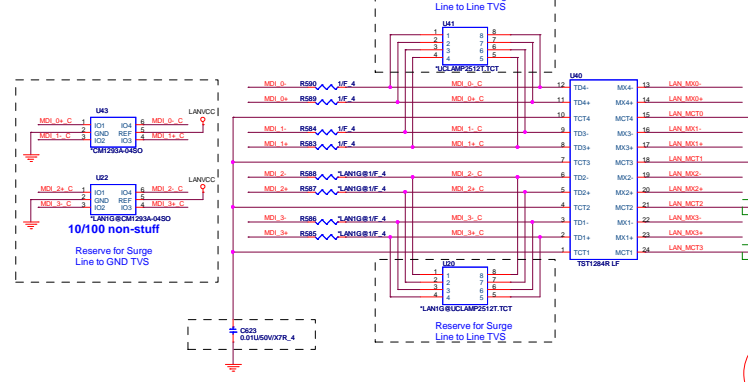
C510 to C513 are for U5006 VDD33 pins-- 1, 29, 37 | Place C513, C5094 closed to U5006 pins44,45,1 and 40.

1. Layout: All termination signal should have 20 mil trace
2. Del U1000 group for 10/100

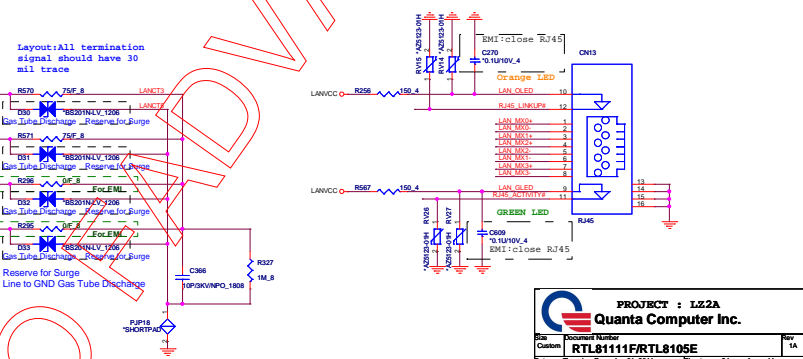


C519 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39, 41

Transformer

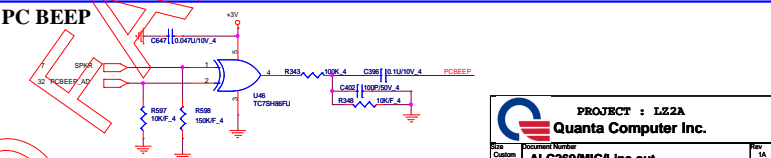
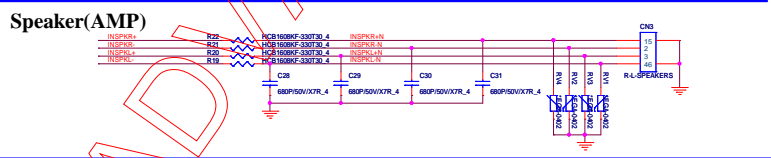
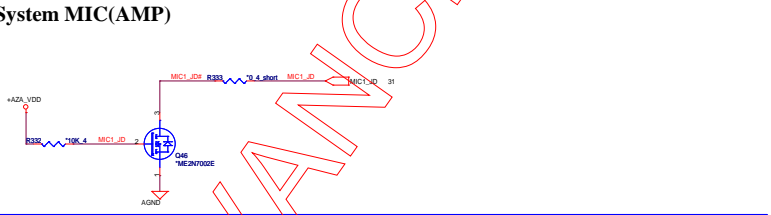
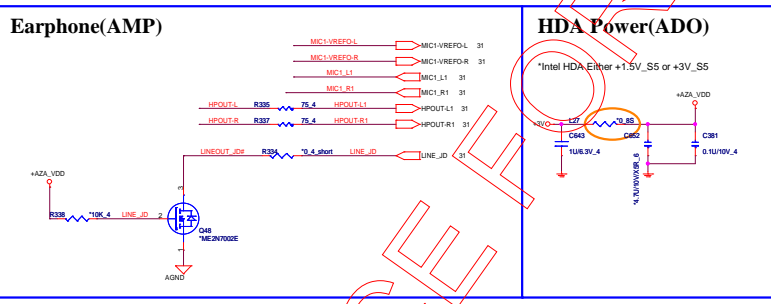
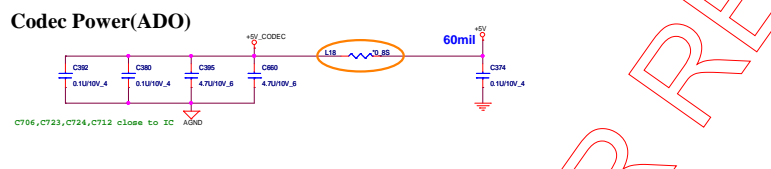
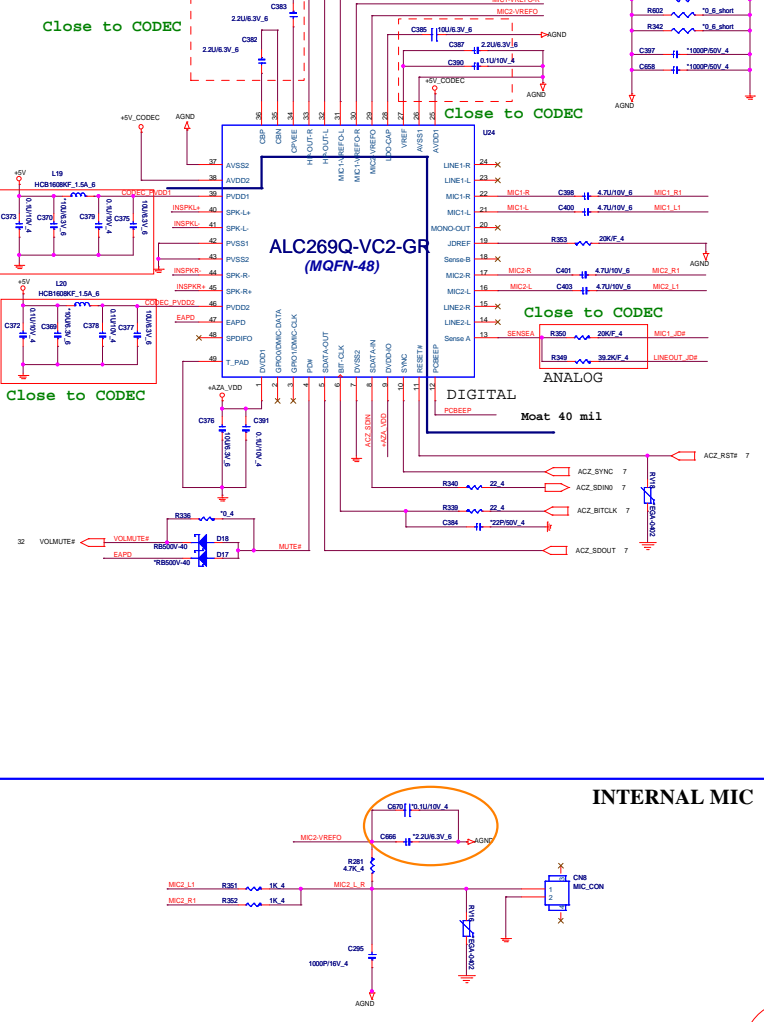


RJ45 Connector



PROJECT : I.2.2A
 Quanta Computer Inc.
 Part Number: RTL8111F/RTL8105E
 Rev: 1A
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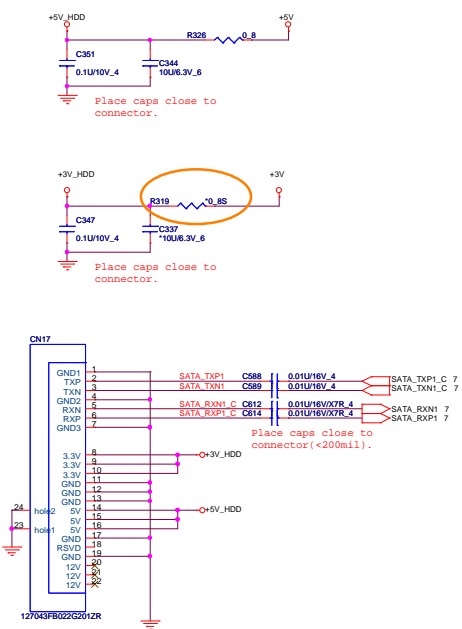


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Quanta Computer Inc.

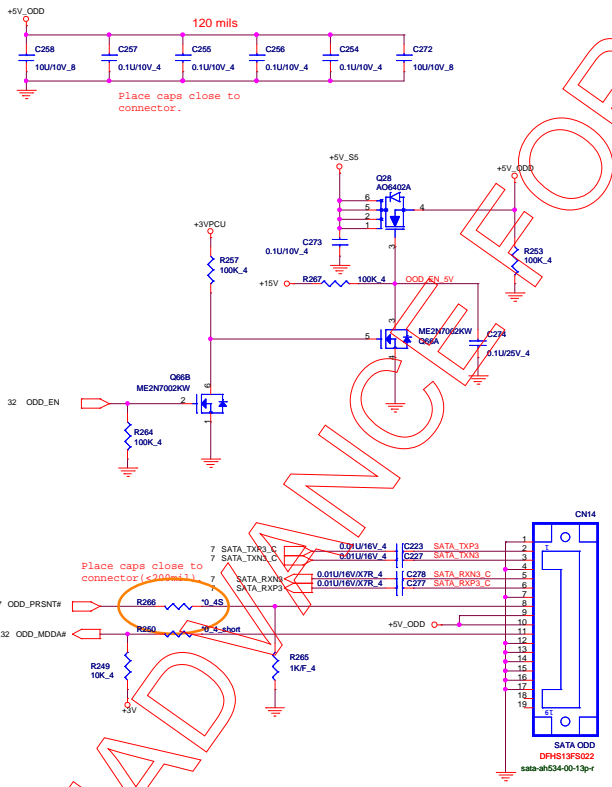
Rev: 1.0
Customer: ALC269/MIC/Line out
Date: 2008.09.10

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SATA HDD Connector.



SATA ODD Connector.



PROJECT : LZ2A

Quanta Computer Inc.

Account Number

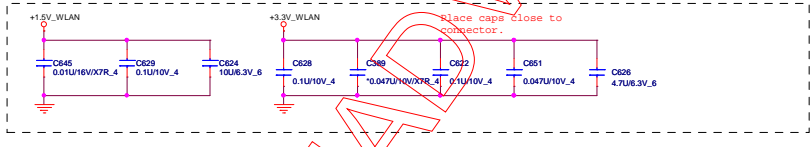
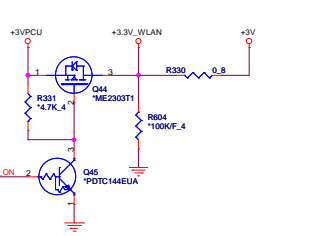
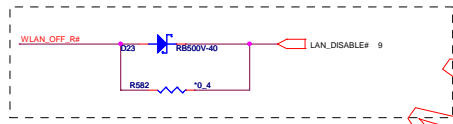
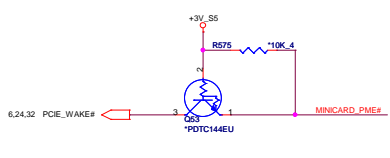
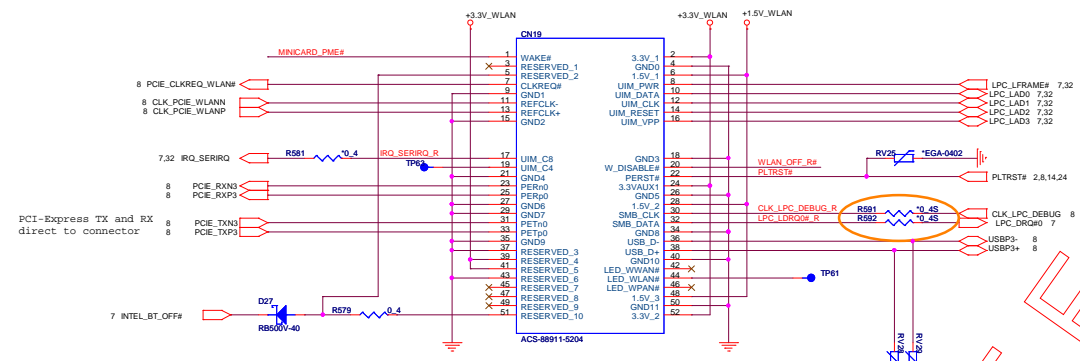
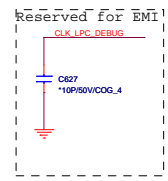
SATA HDD/CD-ROM

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Rev 1A

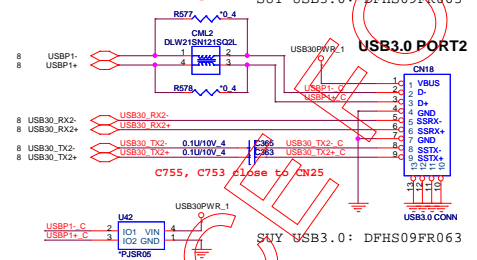
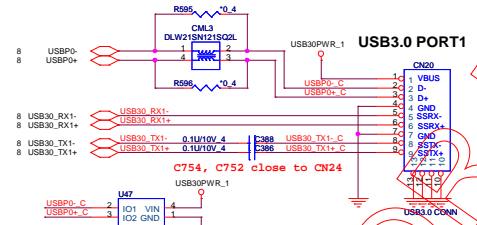
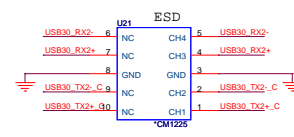
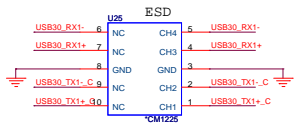
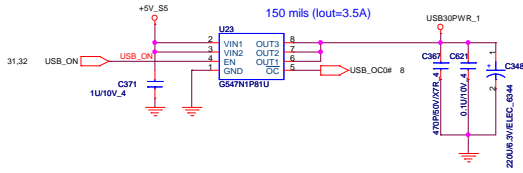
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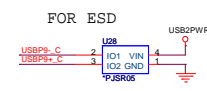
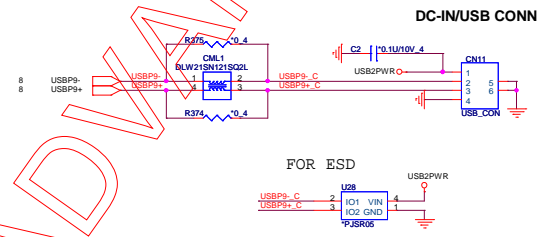
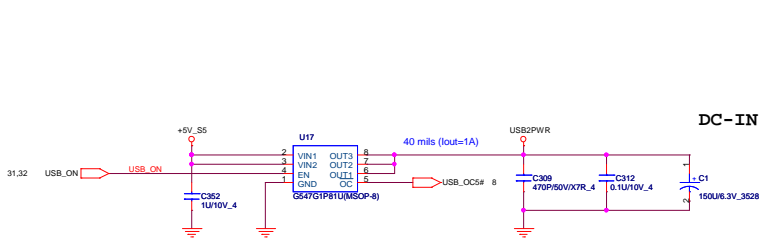
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Quanta Computer Inc.		Account Number	
Site Custom	USB2.0*2/WLAN/BT	Date: Thursday, December 01, 2011	
Sheet 27 of 43		Rev 1A	

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USB3.0*2



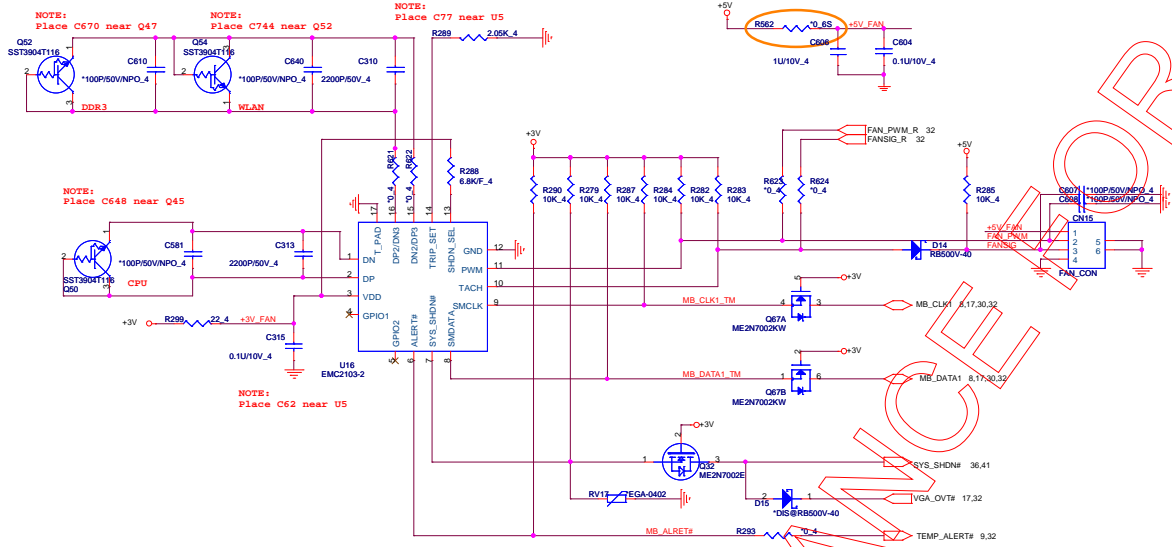
USB2.0*1



PROJECT : LZ2A
 Quanta Computer Inc.
 Rev 1A
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 Date: Thursday, December 01, 2011 Sheet 28 of 43

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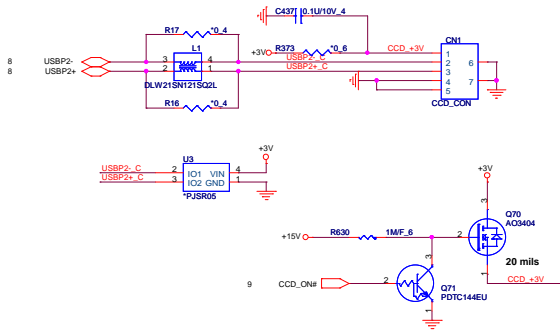
FAN CONTROL



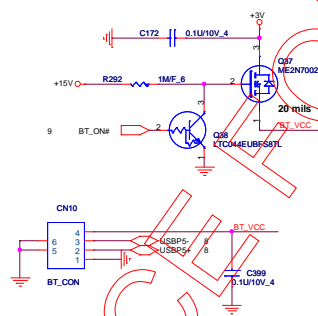
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Quantum Computer Inc.			
Site	Account Number		
Custom	FAN/THERMAL		
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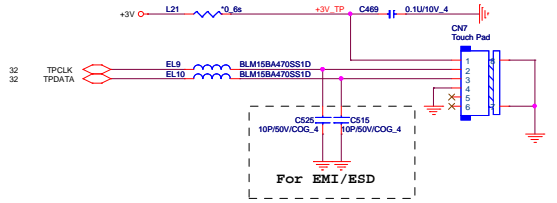
CCD BOARD



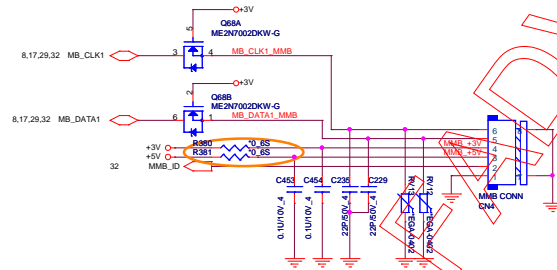
BLUETOOTH



Touch pad

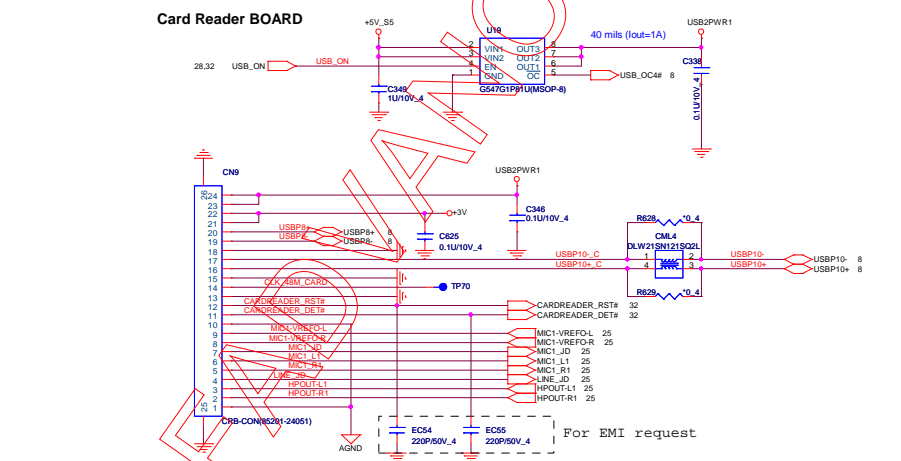
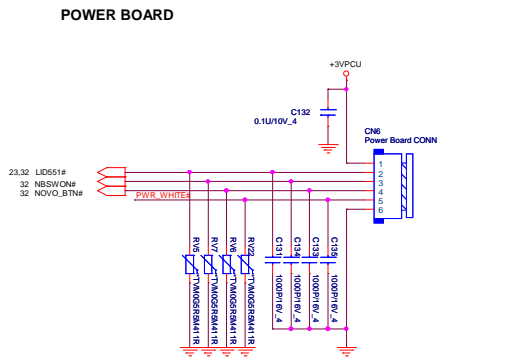
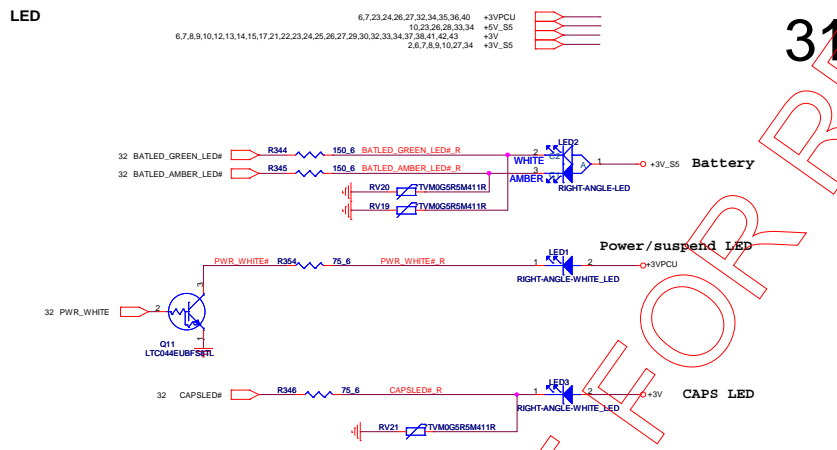
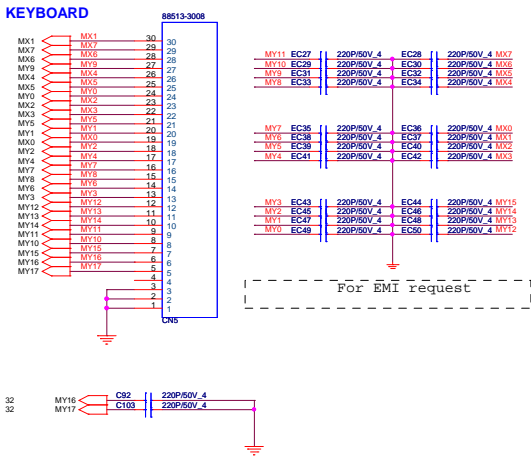


MMB



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Quanta Computer Inc.		Account Number	
CCD/TP/BT/MMB		Date	
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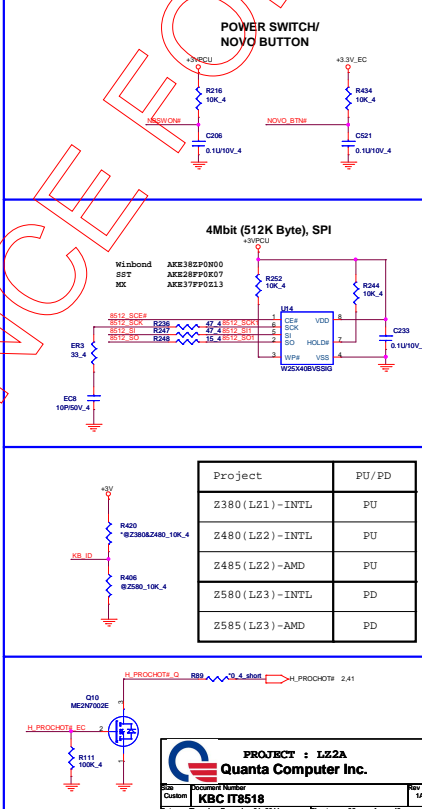
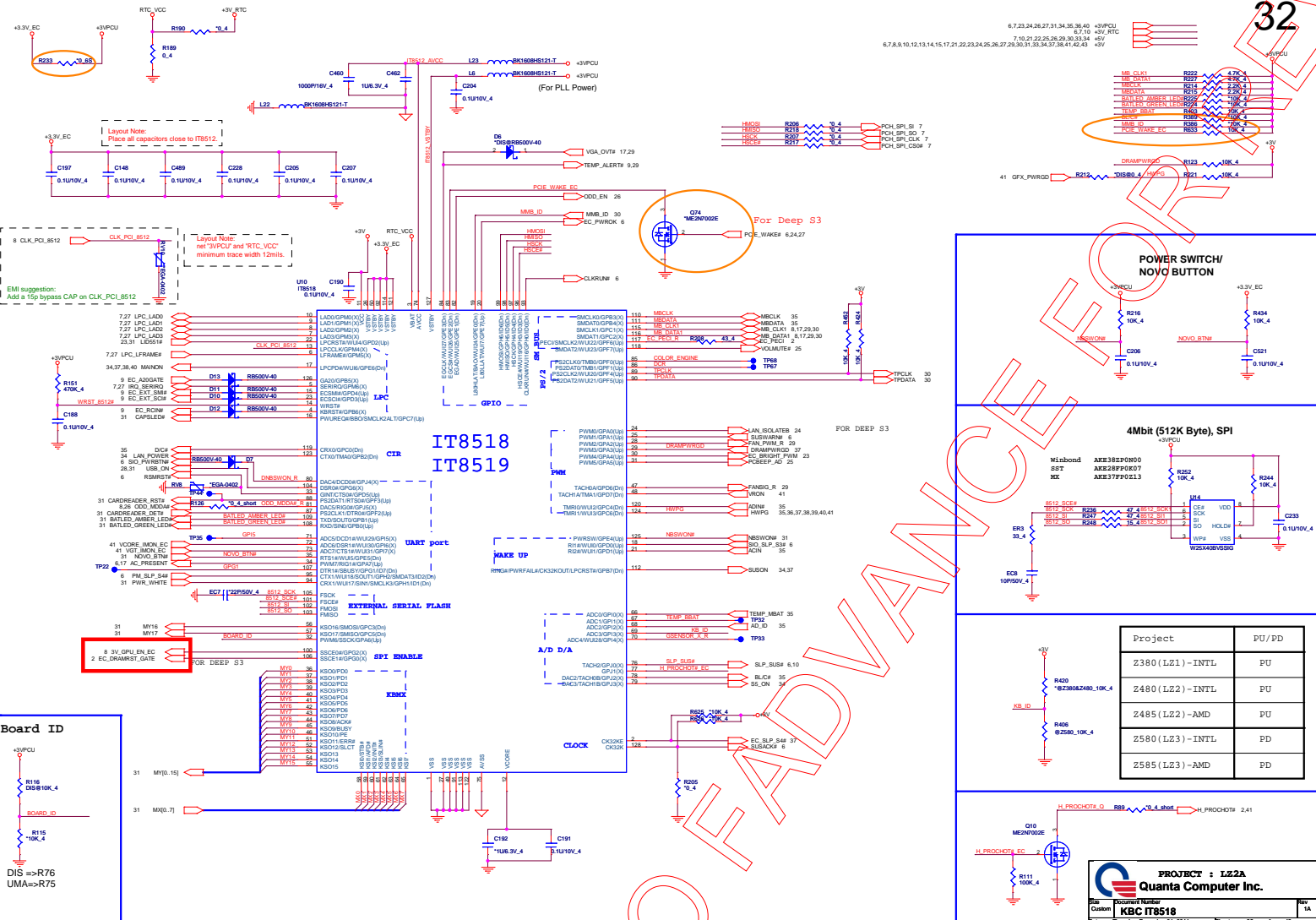


PROJECT : LZ2A
Quanta Computer Inc.

Rev	Account Number	Rev
Custom	KB/PB/LED/CRB	1A
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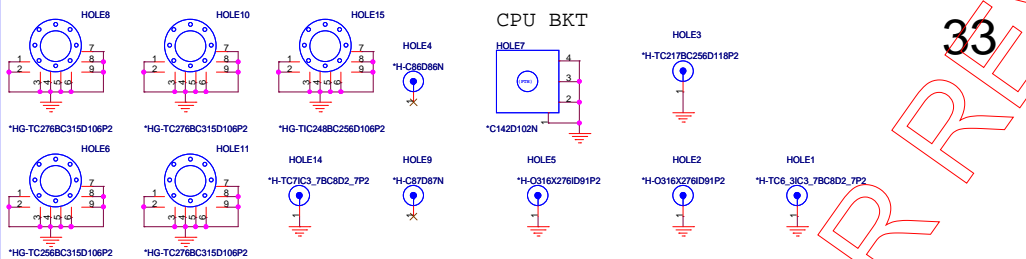
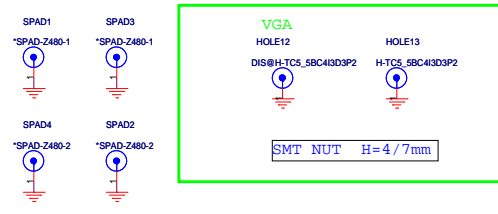
CONFIDENTIAL

6.7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,34,35,36,40,43,45
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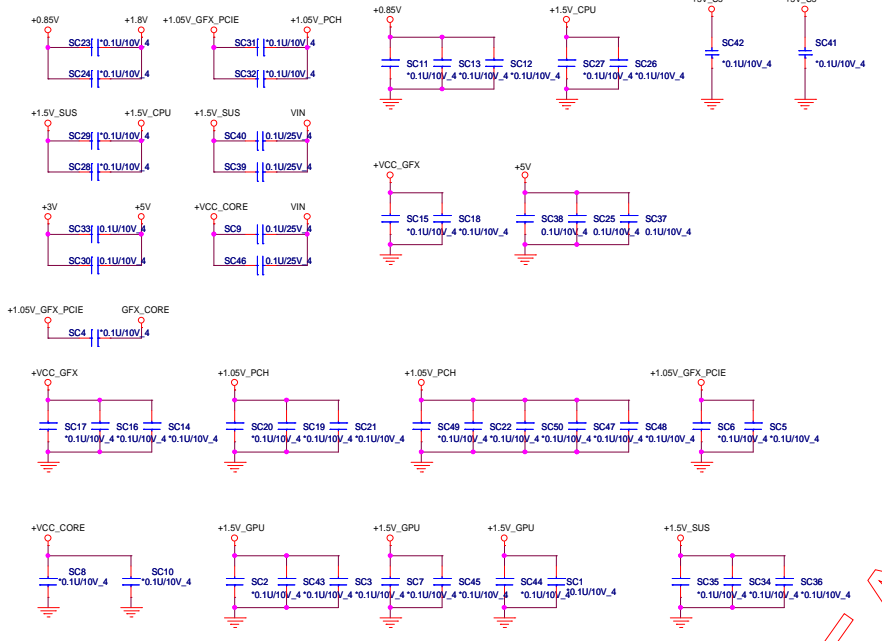


CONFIDENTIAL TO

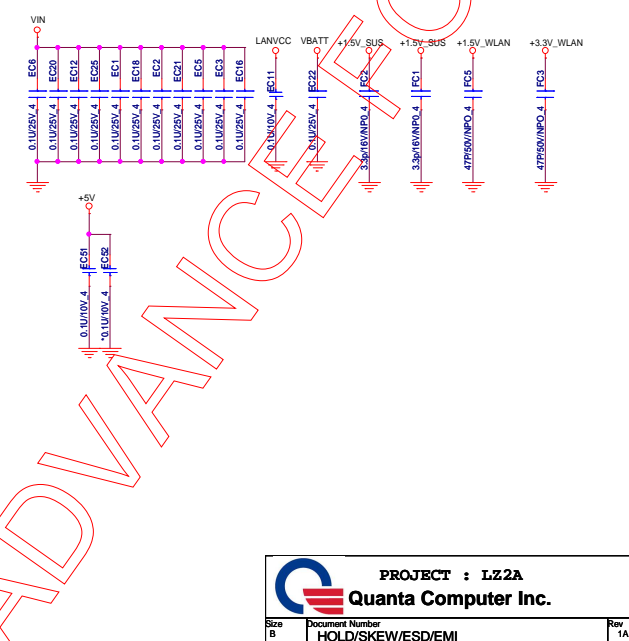
Screw for ME



For ESD



For EMI

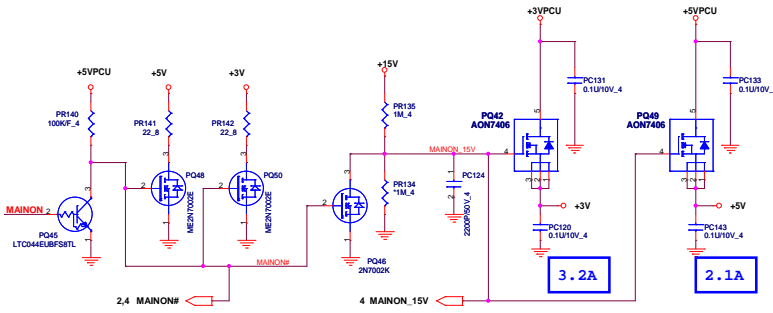


PROJECT : LZ2A
Quanta Computer Inc.

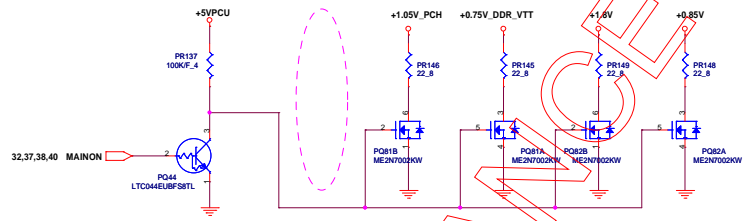
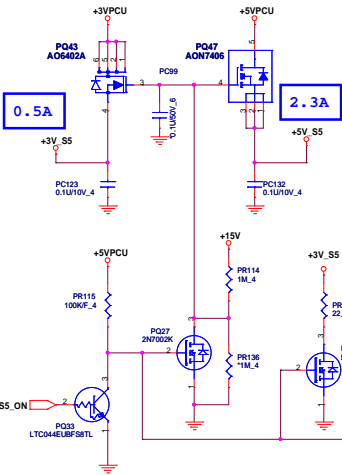
Size B	Document Number	Rev
	HOLD/SKEW/ESD/EMI	1A
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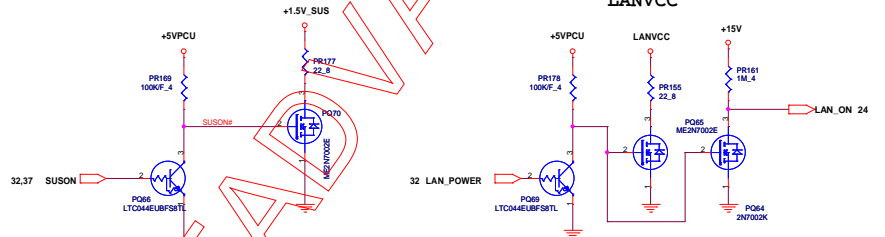
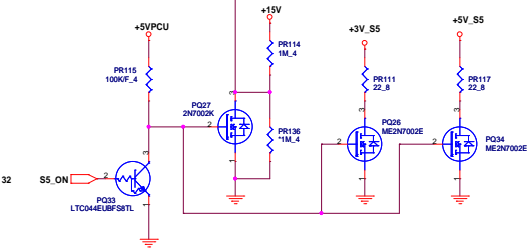
- 10,35,36,37,38,39,40,41,42,43 +5VPCU
- 7,10,21,22,25,26,29,30,33 +5V
- 6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,37,38,41,42,43 +3V
- 23,26,30,36,43 +15V
- 3,4,5,6,7,8,9,10,27,31 +3VPCU
- 2,6,7,8,9,10,27,31 +3V_S5
- 10,23,26,28,31,33 +5V_S5
- 2,4,10,12,13,33,35,45 +1.85V_SUS
- 2,4,6,7,8,10,33,35,45 +1.85V_PCH
- 2,4,33 LANVCC
- 12,13,37 +0.75V_DDR_VTT
- 47,110,33,40 +1.8V
- 4,33,39 +0.85V



3V_S5, 5V_S5

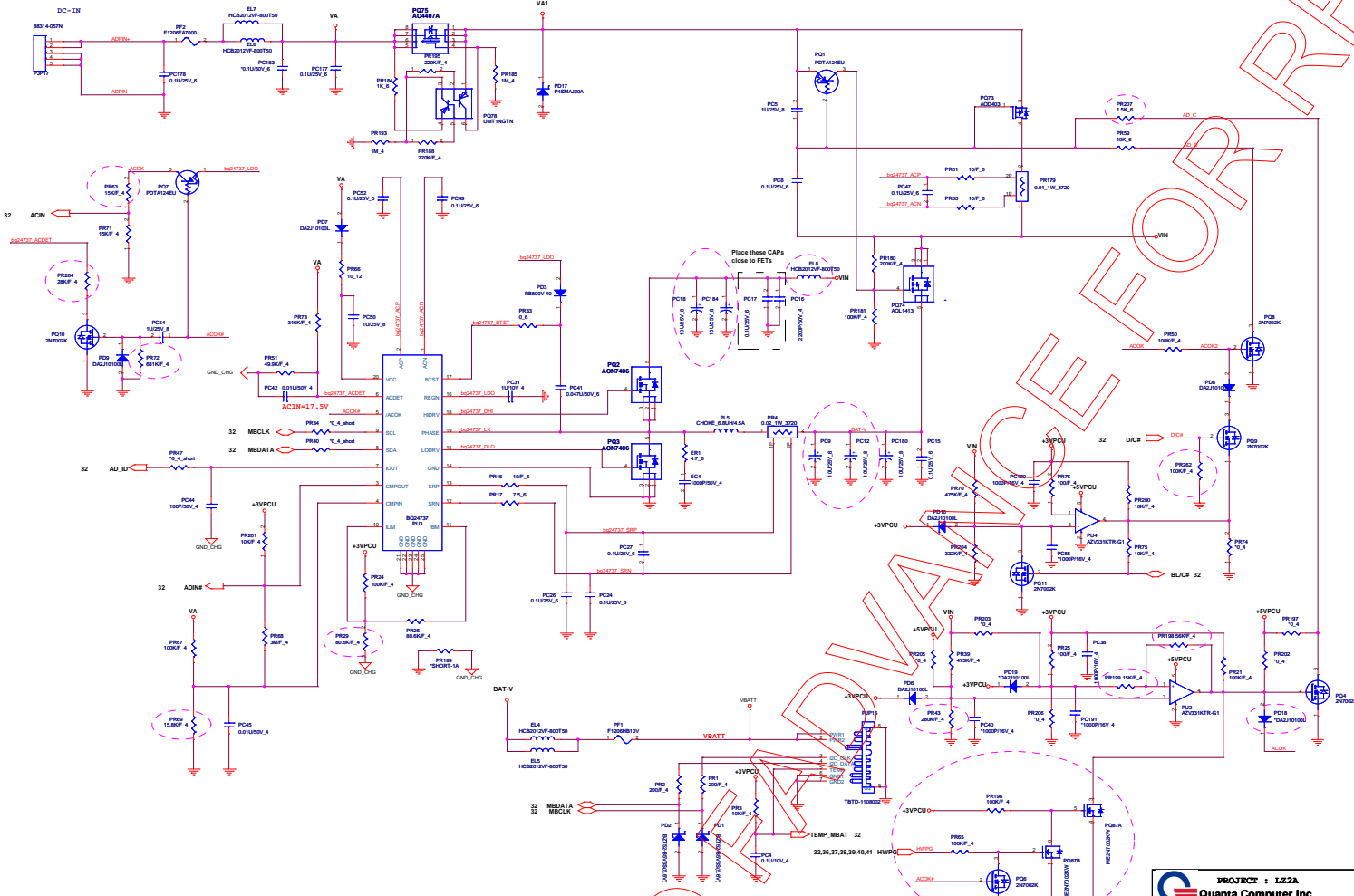


LANVCC



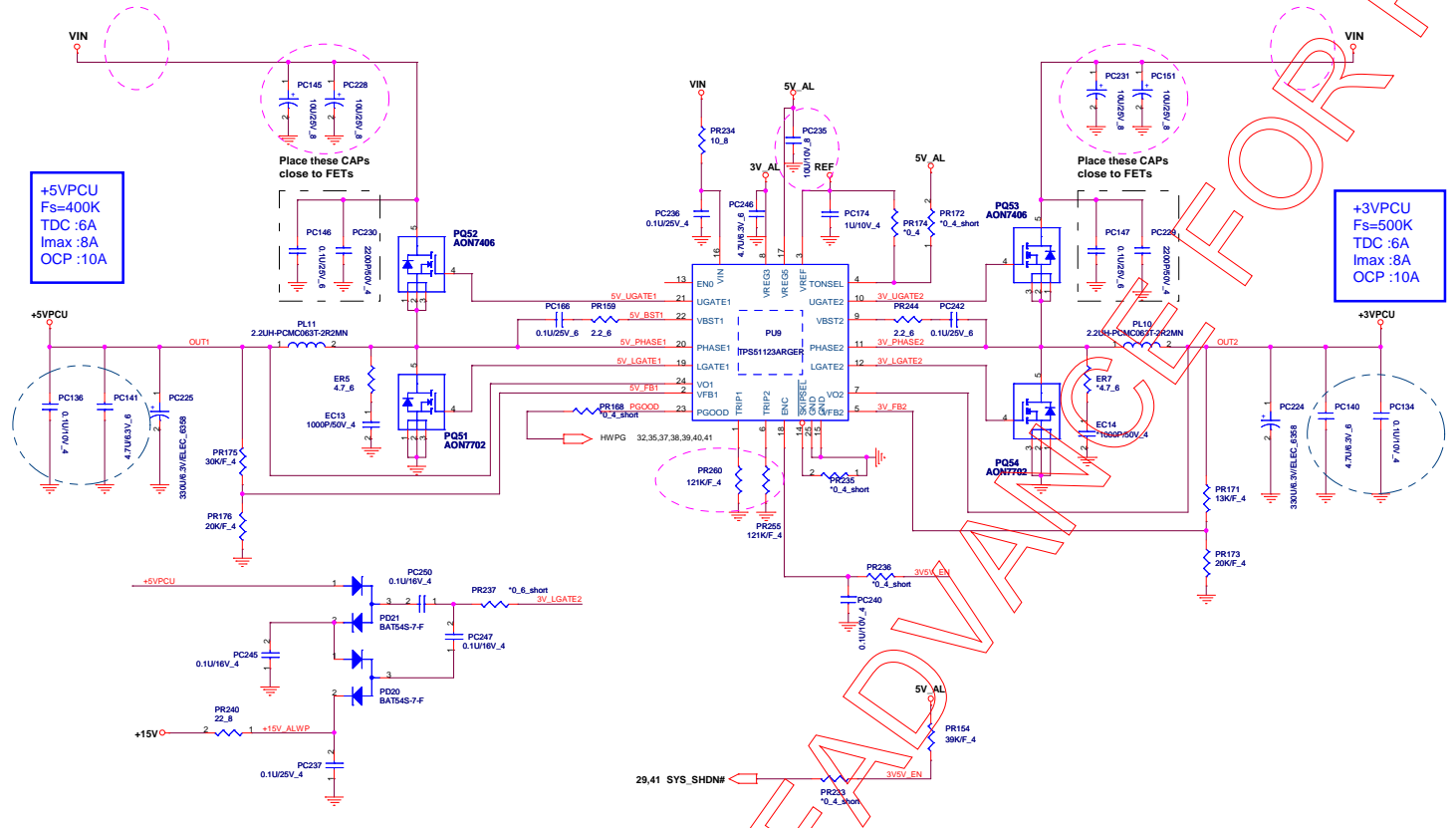
PROJECT : LZ2A	
Quanta Computer Inc.	
Doc	Document Number
Discharge	
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PROJECT : I.32A Quanta Computer Inc. 3F, Sec 2, No. 100, Zhongxing Rd., Hsinchu City, Taiwan, R.O.C.	
Design: [Blank] Check: [Blank]	Designer: [Blank] Checker: [Blank]
Date: [Blank]	File: [Blank]

23,33,35,37,38,39,41,42	VIN
	5V_AL
	3V_AL
	REF
10,34,35,37,38,39,40,41,42,43	+5VPCU
23,26,30,34,43	+15V
6,7,23,24,28,27,31,32,34,38,40	+3VPCU



+5VPCU
Fs=400K
TDC :6A
Imax :8A
OCP :10A

+3VPCU
Fs=500K
TDC :6A
Imax :8A
OCP :10A

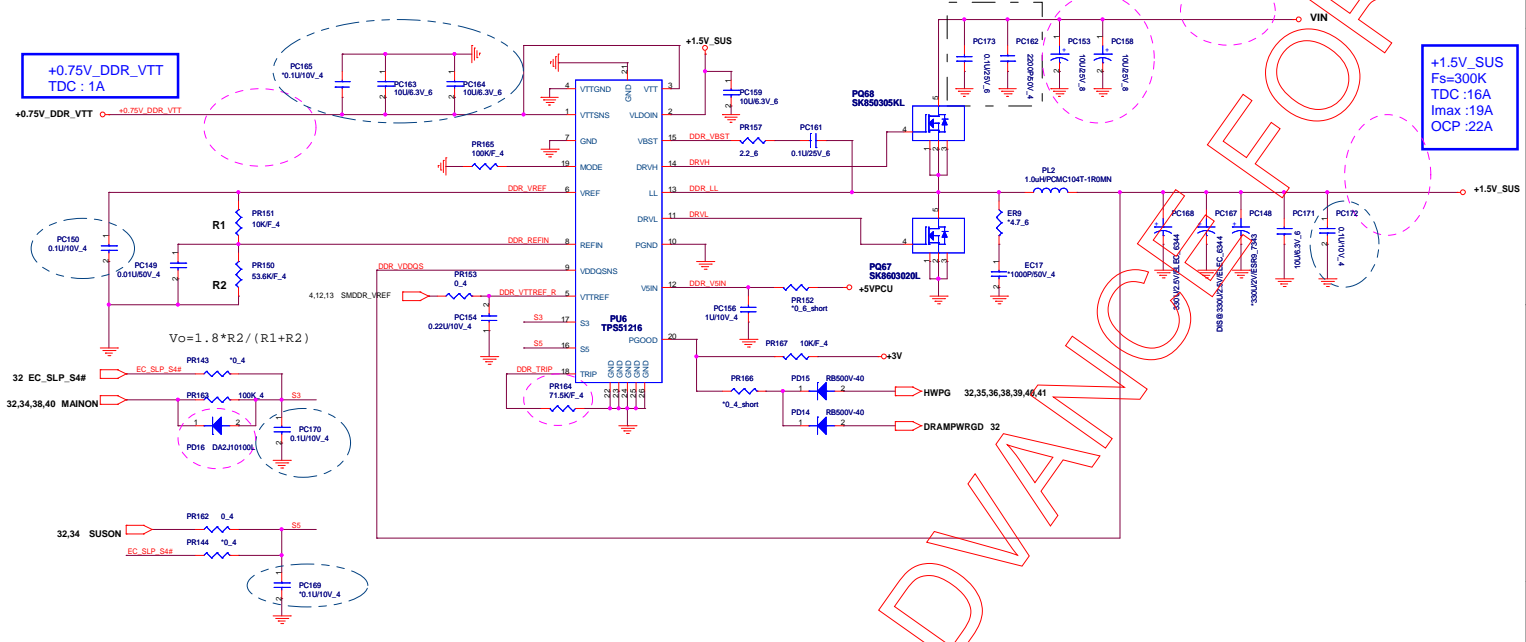
PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Account Number	Rev
	3V/5V (TPS51123ARGER)	
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12,13,34 +0.75V_DDR_VTT
23,33,35,36,38,39,41,42 VIN
2,4,10,12,13,33,34,43 +1.5V_SUS

+0.75V_DDR_VTT
TDC : 1A

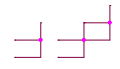
+1.5V_SUS
Fs=300K
TDC :16A
Imax :19A
OCP :22A

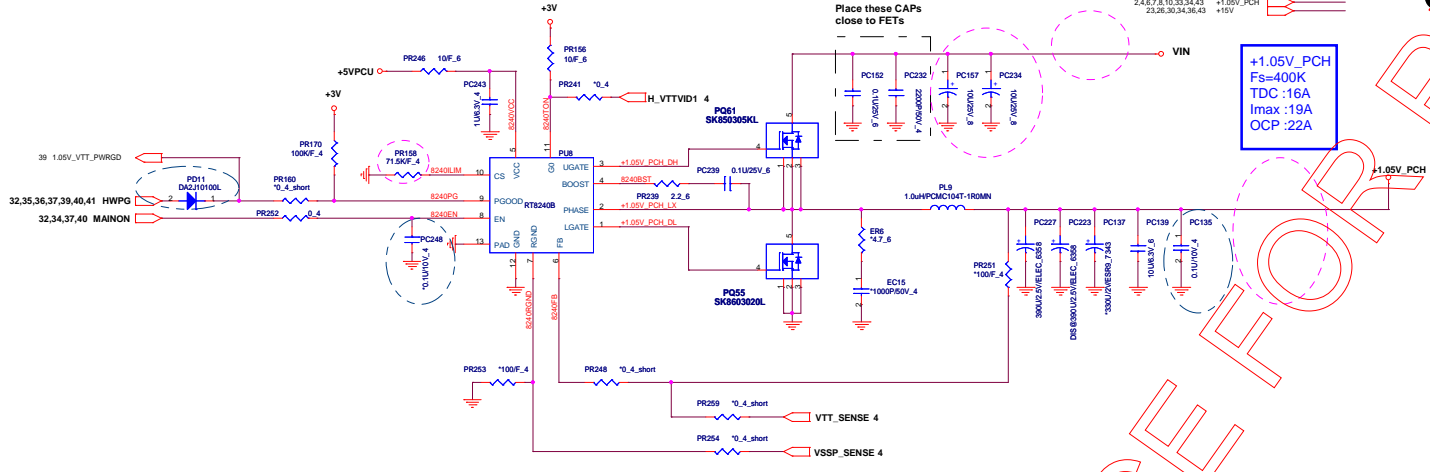
Place these CAPs
close to FETS



PROJECT : L2.2A
Quanta Computer Inc.
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DDR3/0.75V (TPSS1216)
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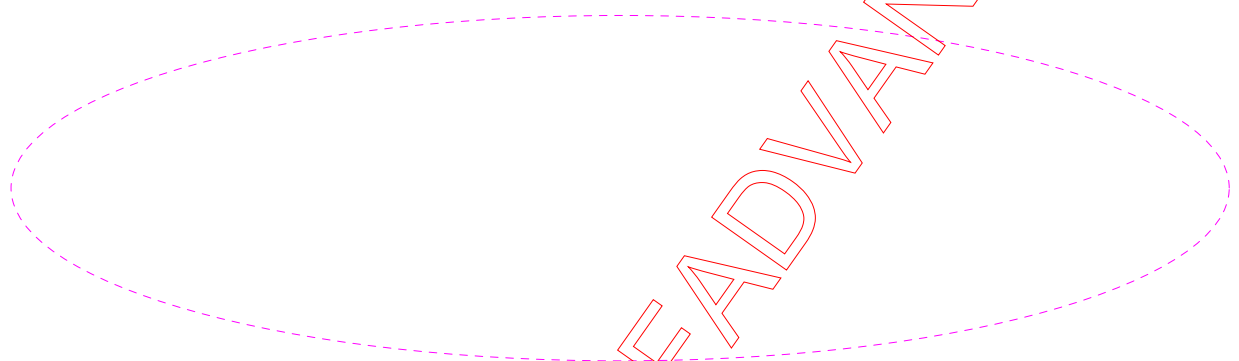
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+1.05V_PCH
 Fs=400K
 TDC :16A
 I_{max} :19A
 OCP :22A

Place these CAPs
 close to FETs

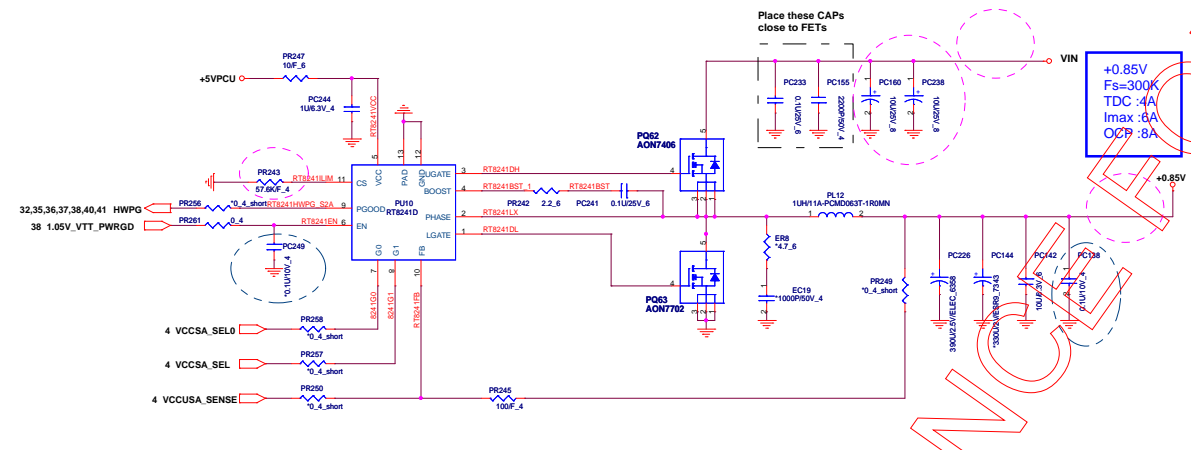


PROJECT : L2.2A
Quanta Computer Inc.

Rev	Document Number	Rev
1	+1.05V_PCH	1

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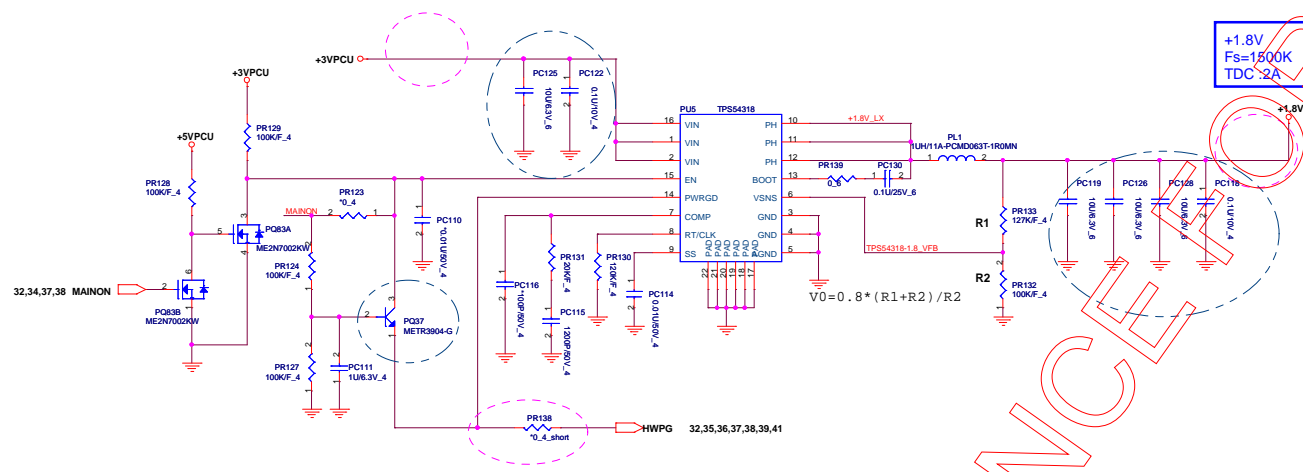


G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9v

PROJECT : L2.2A
Quanta Computer Inc.
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VCCSA (RT8241A)
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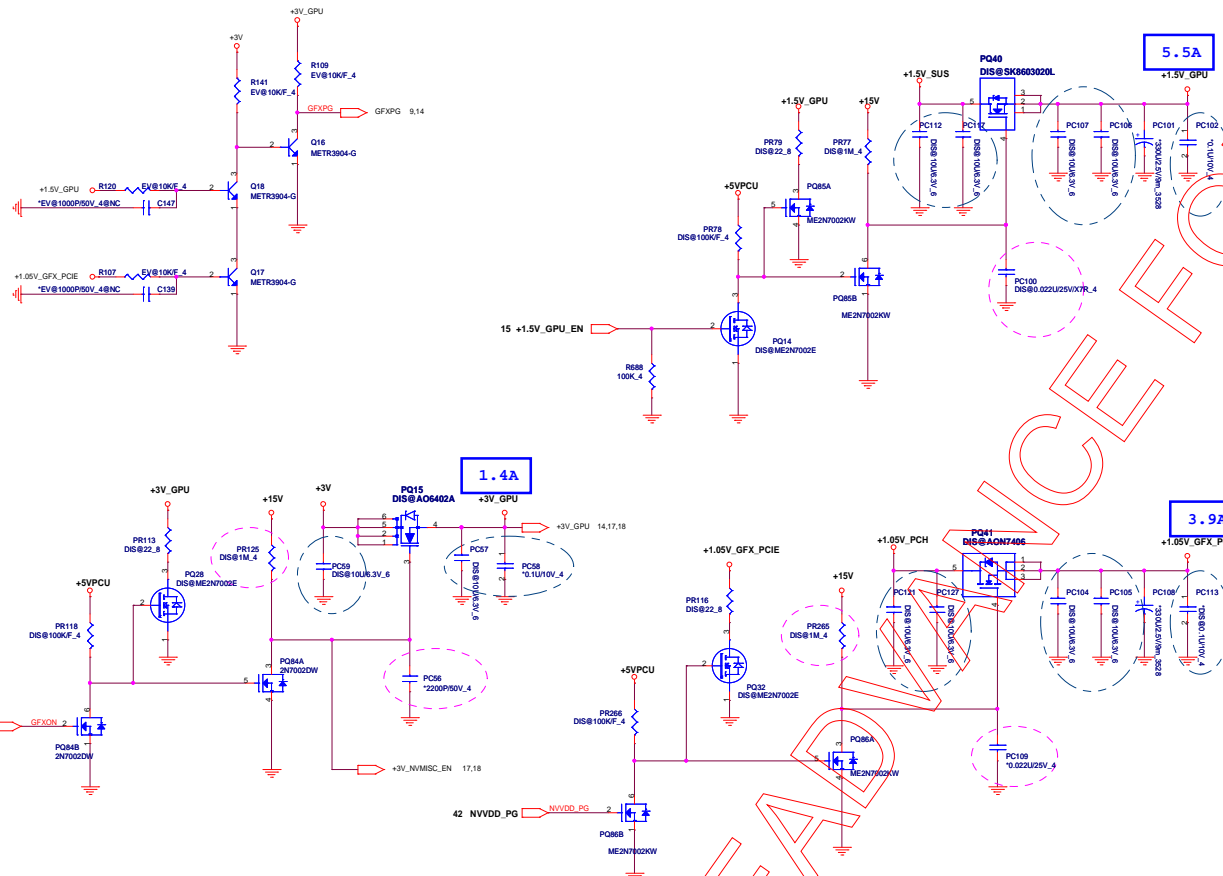
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PROJECT : LZ2A		
Quanta Computer Inc.		
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	1.8V (TPS54318)	
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6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42 14,17,18 +3V_GPU
 10,34,35,36,37,38,39,40,41,42 +3V_GPU
 14,15,18,20,33 +3V_PCU
 22,25,30,34,36 +5V
 2,4,10,12,13,33,34,37 +1.5V_SUS
 14,15,16,33 +1.05V_GFX_PCIE
 2,4,6,7,8,10,33,34,38 +1.05V_PCH



1.4A

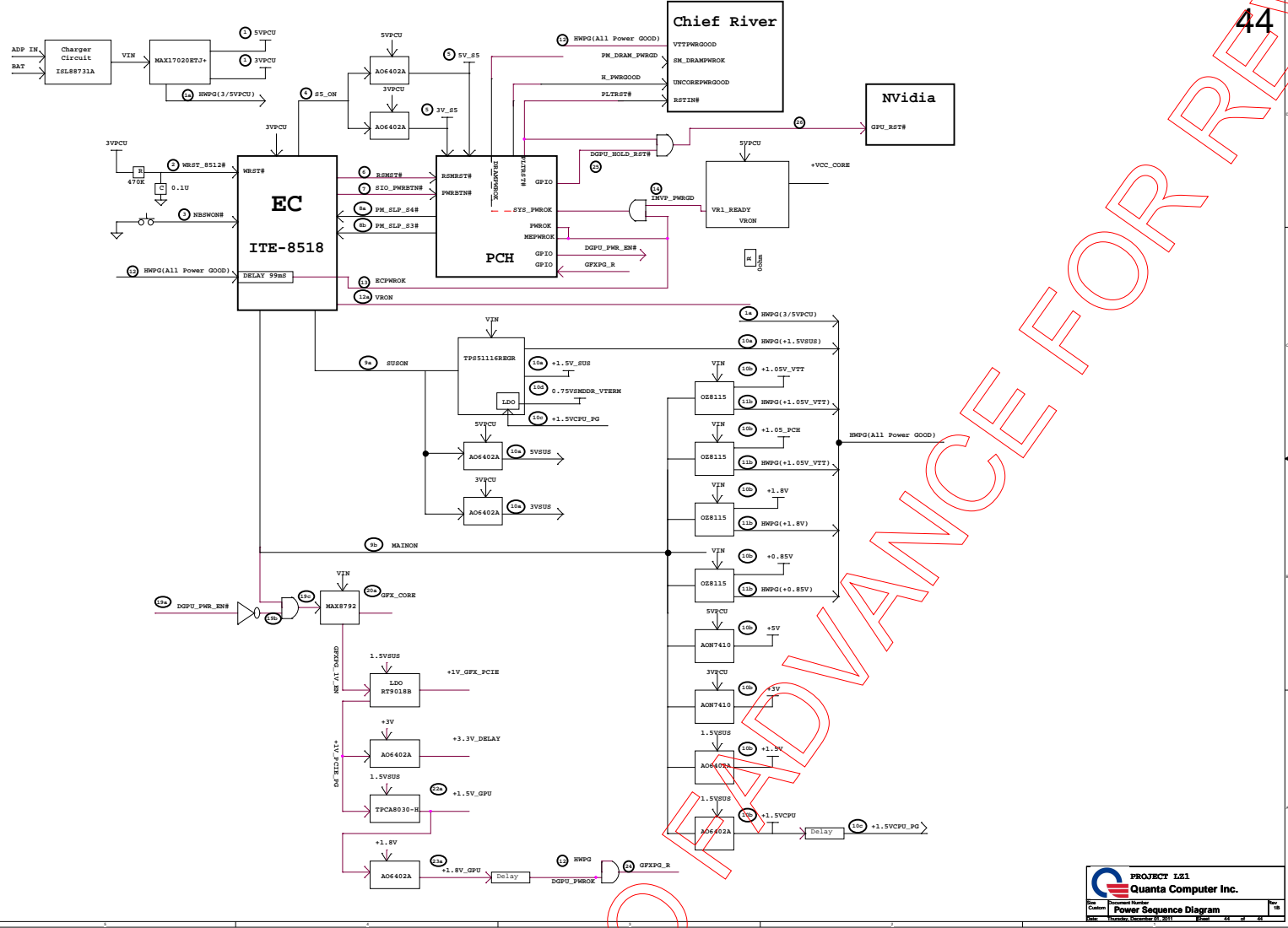
3.9A

PROJECT : L2.2A
Quanta Computer Inc.

Rev	Document Number	Rev
GPU		

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PROJECT L&1
Quanta Computer Inc.
 Power Sequence Diagram
 Date: 10/15/2011

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