

Compal Confidential

ZIWB2/ZIWB3/ZIWE1 DIS M/B Schematics Document

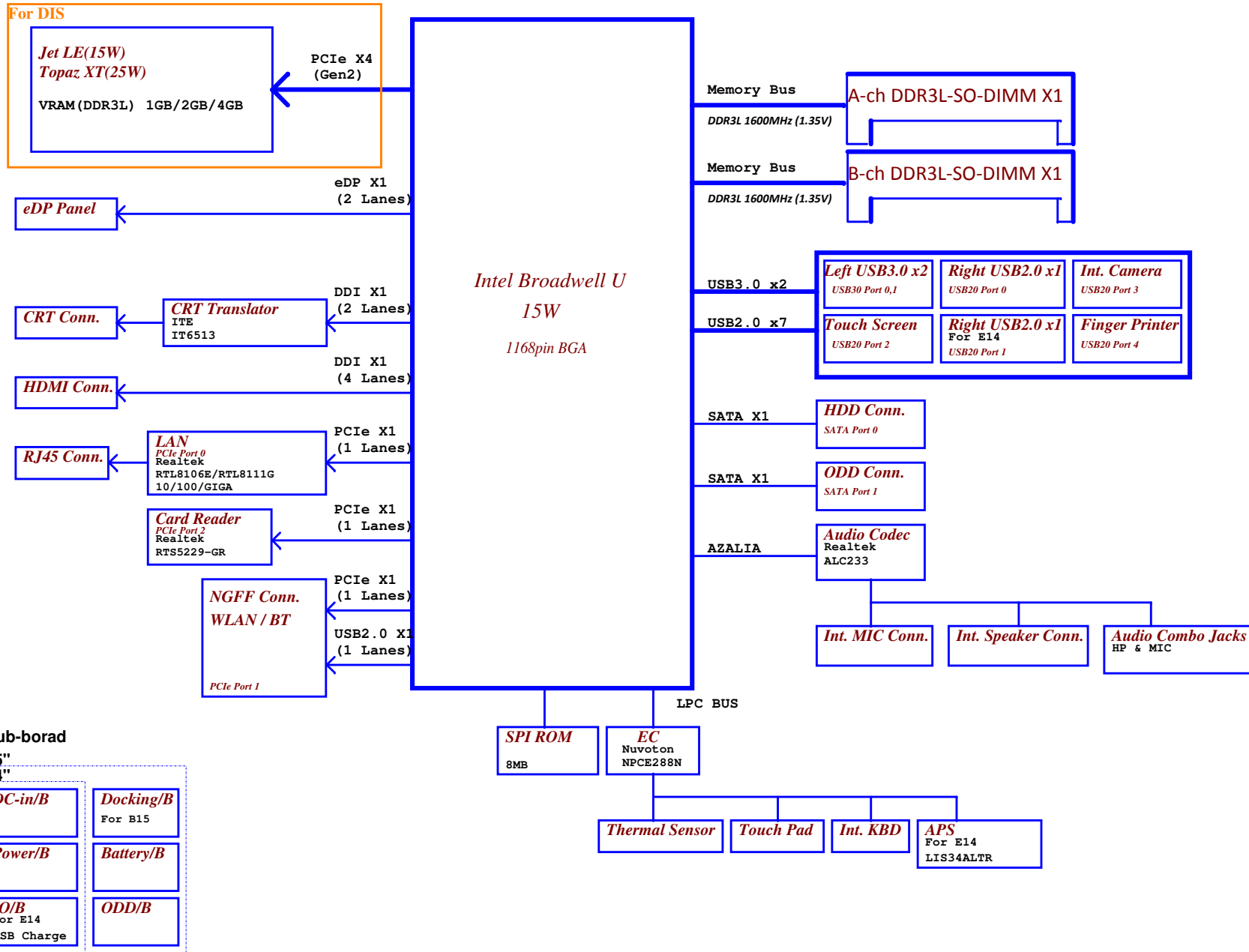
Intel Boardwell U Processor with DDR3L

2014-02-10

LA-B092P

REV : 1.0

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				Date: Tuesday, February 18, 2014	Sheet 1 of 53	



Voltage Rails

State	power plane			
	+B	+5VALW	+1.5V	+3VALW
				+5VS +3VS +1.5VS +V1_05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

USB Port Table

	USB 2.0 Port	3 External USB Port
EHCI1	UHCI0	0 USB Port (Left Side)USB3.0
		1 USB Port (Left Side)USB3.0
	UHCI1	2 Touch Screen
		3 Camera
		4
UHCI2	5	
	6	
	7	
EHCI2	UHCI4	8
		9 USB Port (Right Side USB-BD)
	UHCI5	10 Mini Card(WLAN)
		11 Card Reader
		12
	UHCI6	13

BOM Structure Table

Item	BOM Structure
ZIWB2 (14")	B14@
ZIWB3 (15")	B15@
ZIWE1 (14")	E14@
CPU_SA00006SM20	i5_4200U@
CPU_SA00007AM00	QFSY@
CPU_SA00006SU30	i3_4100U@
CPU_SA000072Q10	i3_4005U@
CPU_SA00006SX20	i3_4010U@
LAN 10/100 Transformer	100@
LAN GIGA Transformer	GIGA@
LAN Switch mode	SWITCH@
LAN RTL8106E-CG	8106ELDO@
LAN RTL8111GS-CG	8111GLDO@
LAN RTL8106EUS-CG	8106ESW@
LAN RTL8111GUS-CG	8111GSW@
Audio_233	233@
Audio_233VB	233VB@
For B15	Docking@
For B14, E14	NoDocking@
For Deep Sleep	DS3@
For No Deep Sleep	NoDS3@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@
For Intel ZERO ODD	ZODD@
For No Intel ZERO ODD	NoZODD@
For Green CLK	GCLK@
For No Green CLK	NoGCLK@
For No Green CLK	NoGCLKDIS@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
GPU support Single Rank	SR@
GPU support Dual Rank	DR@
GPU Jet LE	JET@
GPU Topaz XT	TOPAZ@
For DIS	PX@
For UMA	UMA@
Camera	COMS@
APS (G-sensor)	GS@
Touch Screen	TS@
HDMI	HDMI@
USB 2.0	USB2@
USB 3.0	USB3@
Full HD Panel (2 Lane)	FHD@
ENE EC 9012	9012@
HDMI Royalty	45@
Connector	ME@
VRAM indentify	X76@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
DA600140000	PCB_14_DIS@
DA600141000	PCB_14_UMA@
DA600140100	PCB_15_DIS@
DA600141100	PCB_15_UMA@

Only in DIS Schematic

Only in DIS Schematic

No USE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
DDR_JDIMM2	1010 010x A4h

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	0100 0001 41h

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	+3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	+3VGS	X	X	X	X	+3VS	+3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	+3VS	+3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	+3VGS	X	+3VS	X	X	+3VS	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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Date:	Wednesday, February 18, 2014	Sheet	3	of	53	

5

4

3

2

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B

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A

A

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				C	1.0
				Date: Tuesday, February 18, 2014	Sheet 4 of 53

5

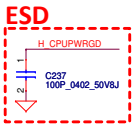
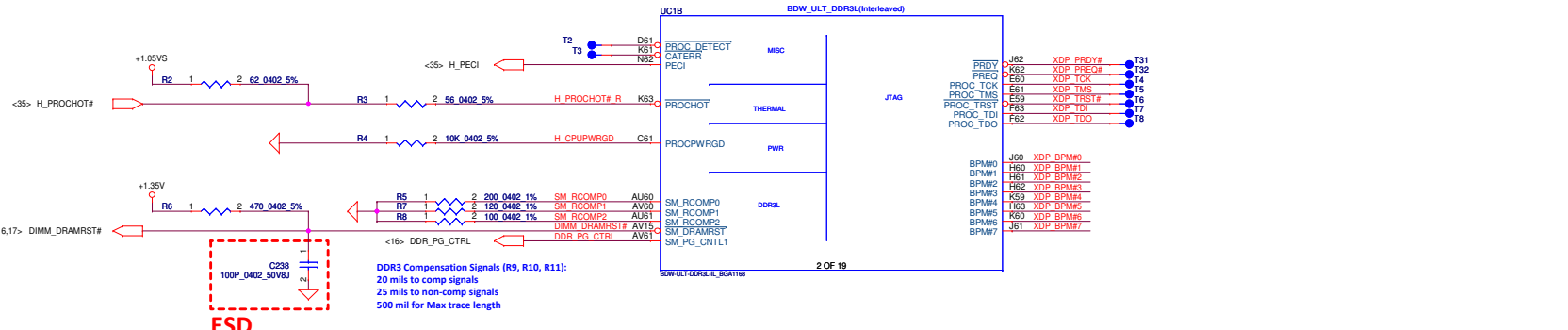
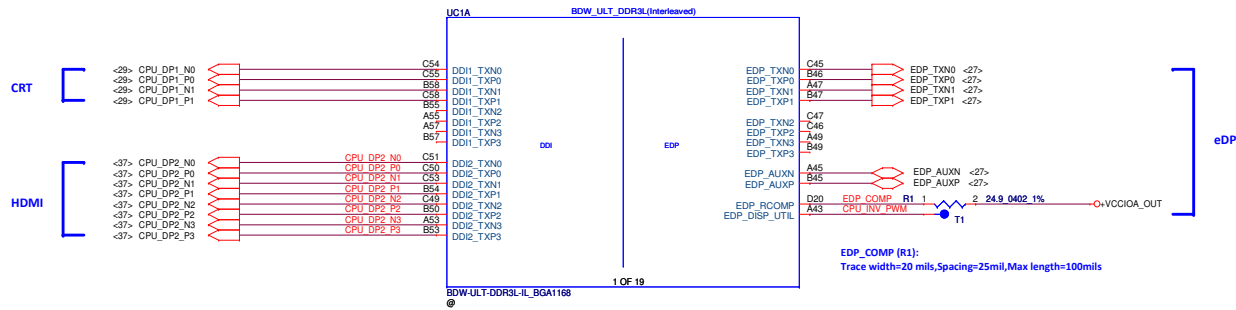
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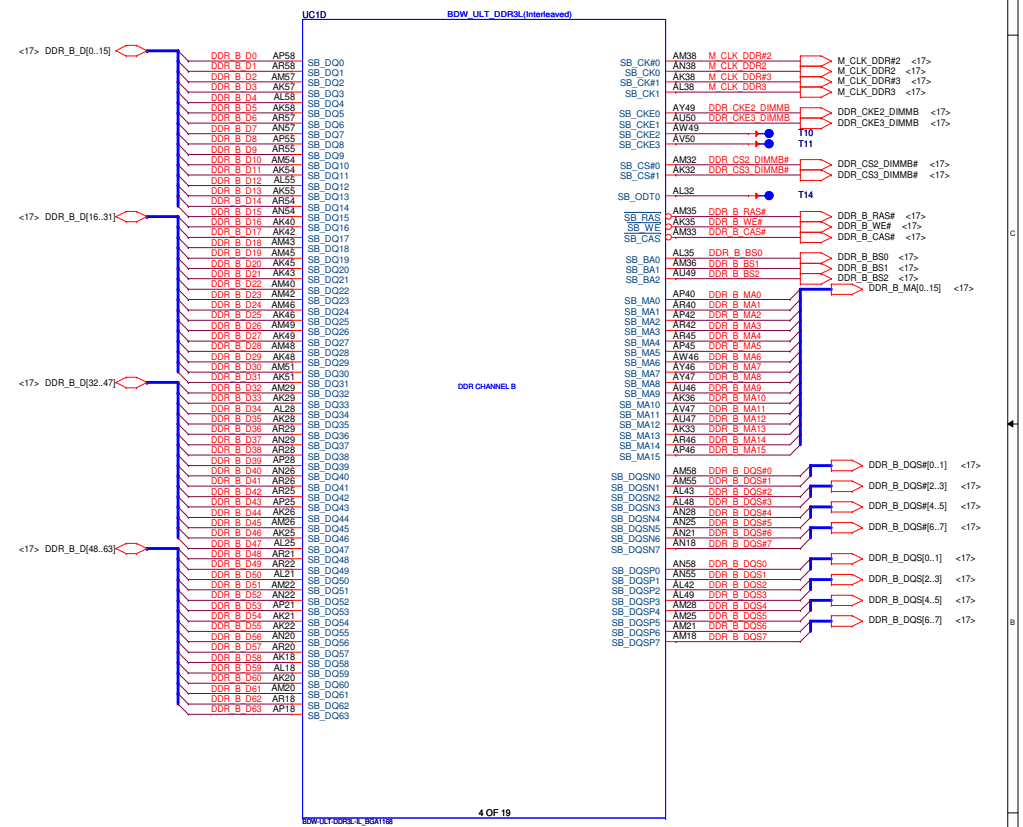
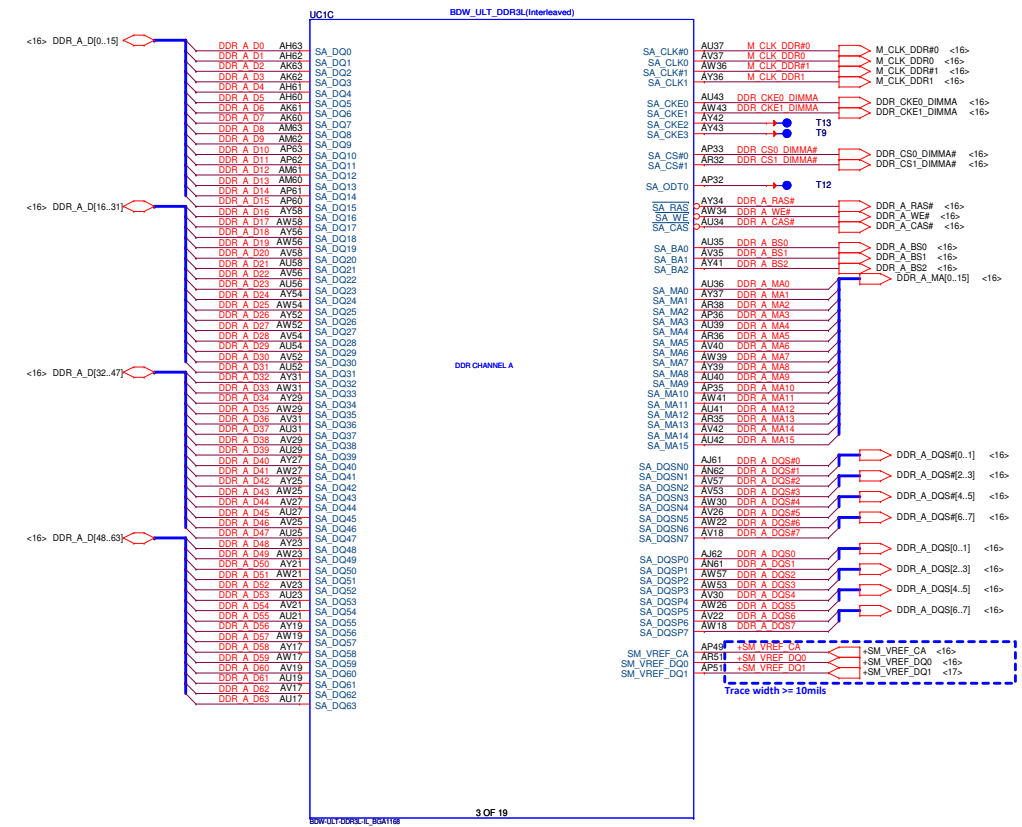
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DAZ14J00101
PCB 14I LA-B091P REV0 M/B DIS 3
PCB_B14_DIS@
- DAZ
DAZ14L00101
PCB 14K LA-B091P REV0 M/B DIS 6
PCB_B15_DIS@
- DAZ
DAZ14N00101
PCB 14K LA-B091P REV0 M/B DIS 6
PCB_E14_DIS@
- DAZ
DAZ14J00201
PCB 14I LA-B092P REV0 M/B UMA 3
PCB_B14_UMA@
- DAZ
DAZ14L00201
PCB 14K LA-B092P REV0 M/B UMA 6
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DAZ14N00201
PCB 14K LA-B092P REV0 M/B UMA 6
PCB_E14_UMA@



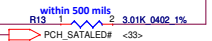
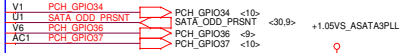
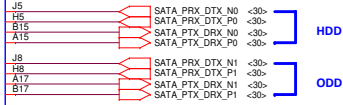
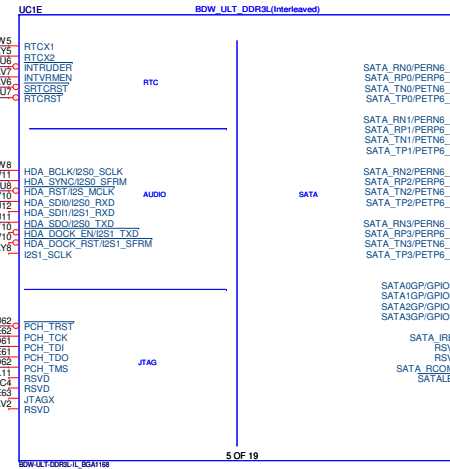
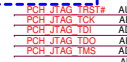
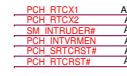
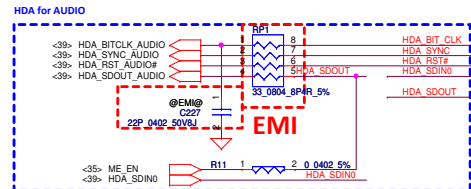
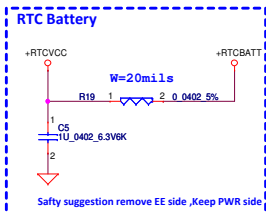
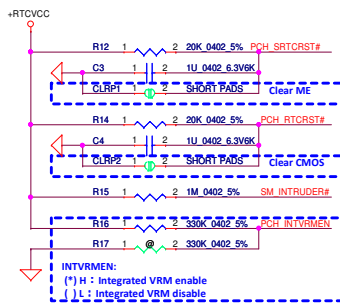
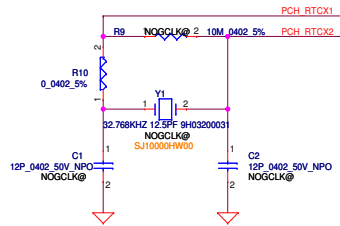
- UC1
SA00007G030
Intel 2957U 1.4G 2M D0 2u:BGA CPU
2957U@
- UC1
SA00007G230
S IC CL8064701569500 QFAN D0 1.7G BGA
3558U@
- UC1
SA00006SLA0
S IC CL8064701477202 QEVD C0 1.8G BGA
I7_4500U@
- UC1
SA00006SMC0
S IC CL8064701477702 SR170 C0 1.6G C38I
I5_4500U@
- UC1
SA00007AM00
S IC CL8064701614813 QFSY C0 1.6G BGA
QFSY@
- UC1
SA00006SL30
S IC CL8064701476302 SR16P C0 1.8G C38I
I3_4100U@
- UC1
SA00007C350
S IC CL8064701478404 QEAR D0 1.7G C38
I3_4005U@
- UC1
SA00006SX80
S IC CL8064701478202 SR16Q C0 1.7G C38I
I3_4010U@

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Date:	Tuesday, February 18, 2014	Sheet	5	of 53

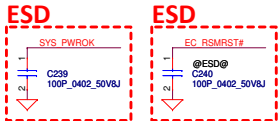
Interleaved Memory



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				LA-B092P
				Rev 1.0
				Date: Tuesday, February 18, 2014
				Sheet 6 of 53



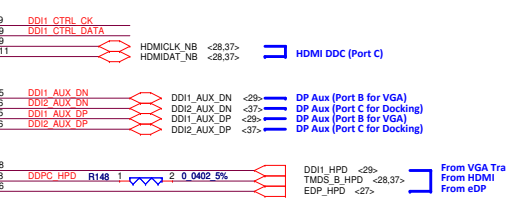
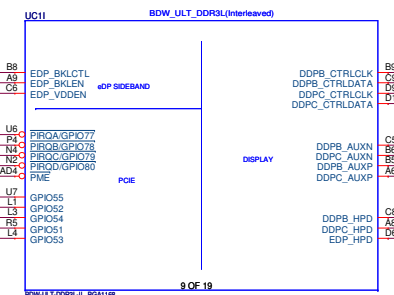
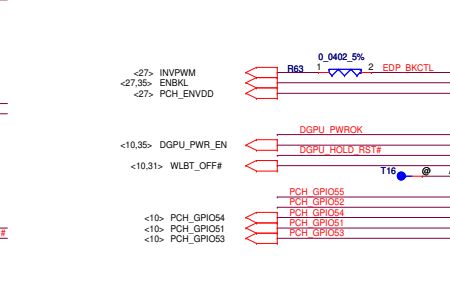
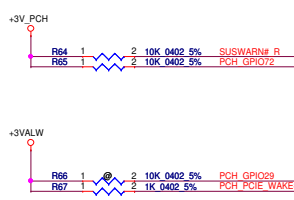
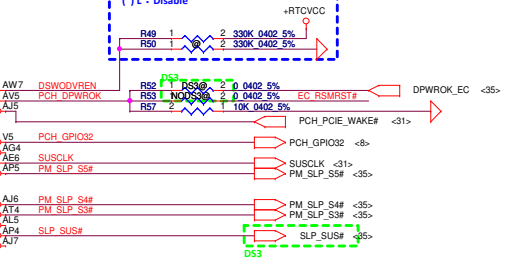
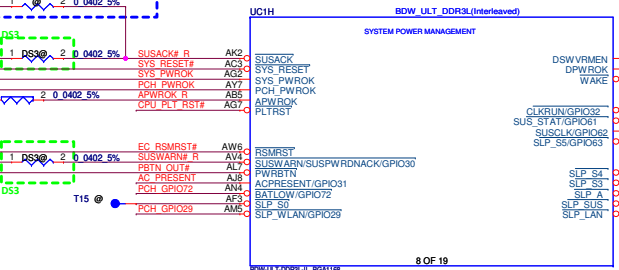
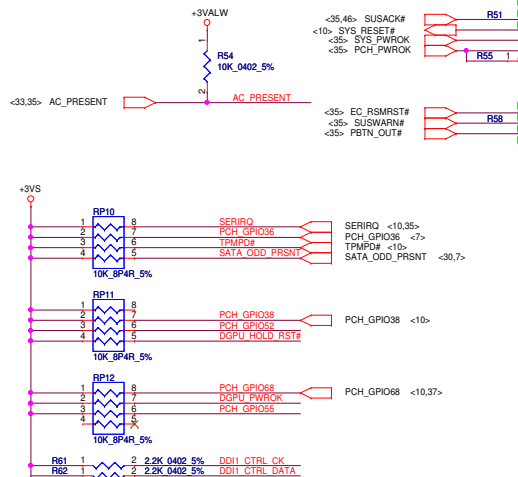
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Rev	1.0			

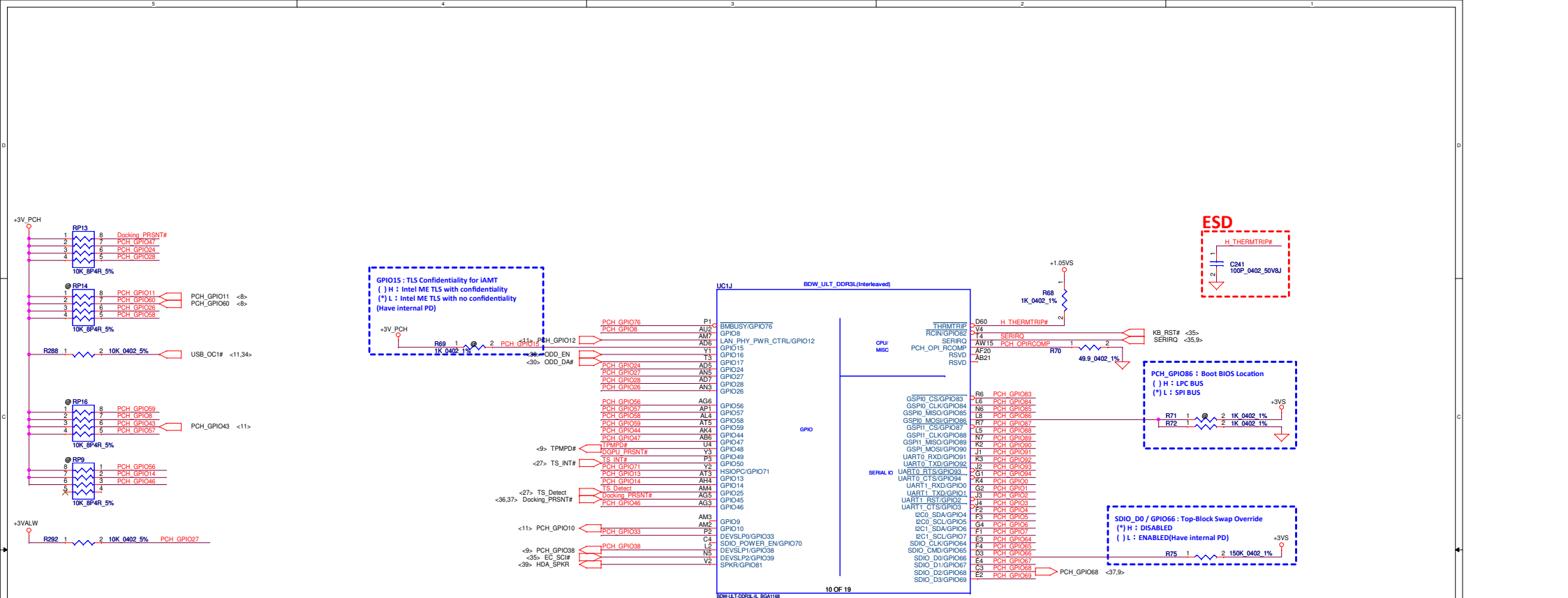


Function	(X)DS3 (X)SBA	(O)DS3 (X)SBA	(X)DS3 (O)SBA
R51	X	O	X
R55	O	O	X
R56	X	X	O
R58	X	O	X
R52	X	O	X
R53	O	X	O

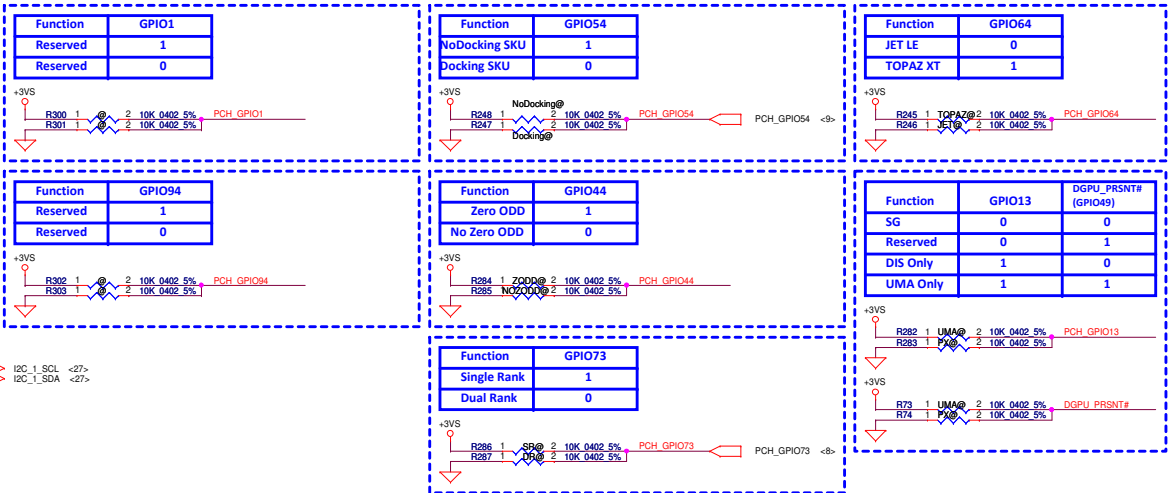
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit
CAN be NC, if not support Deep Sx
SUSWARN# R 1 R48 1 0 0.0402 5%

DSWDDVREN - On Die DSW VR Enable
(*): H : Enable(DEFAULT)
(): L : Disable
R49 1 2 330K 0.402 5%
R50 1 2 330K 0.402 5%





BIOS Strap Pin

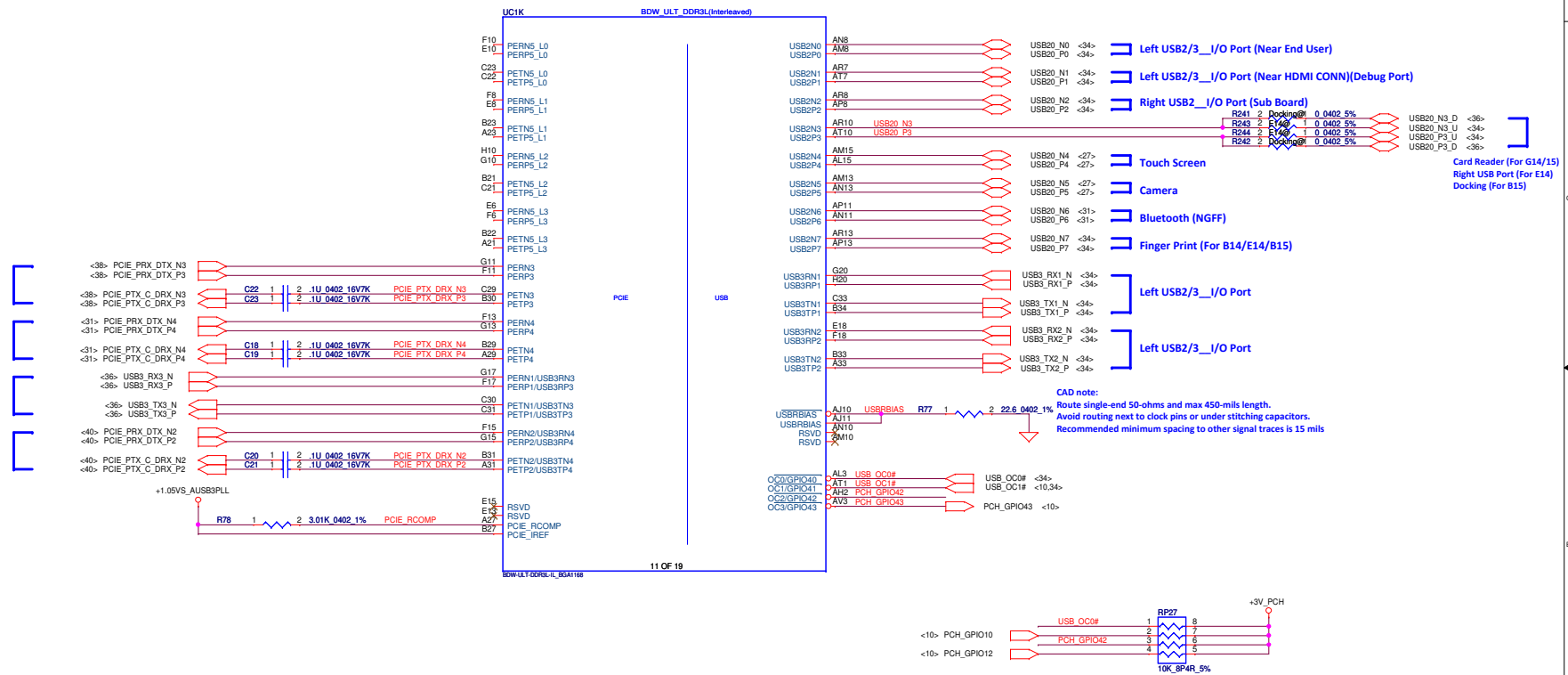


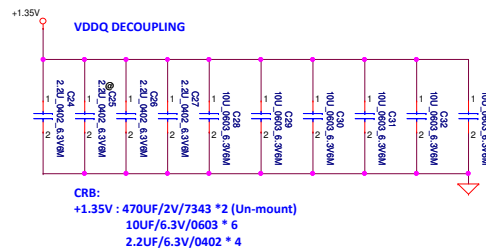
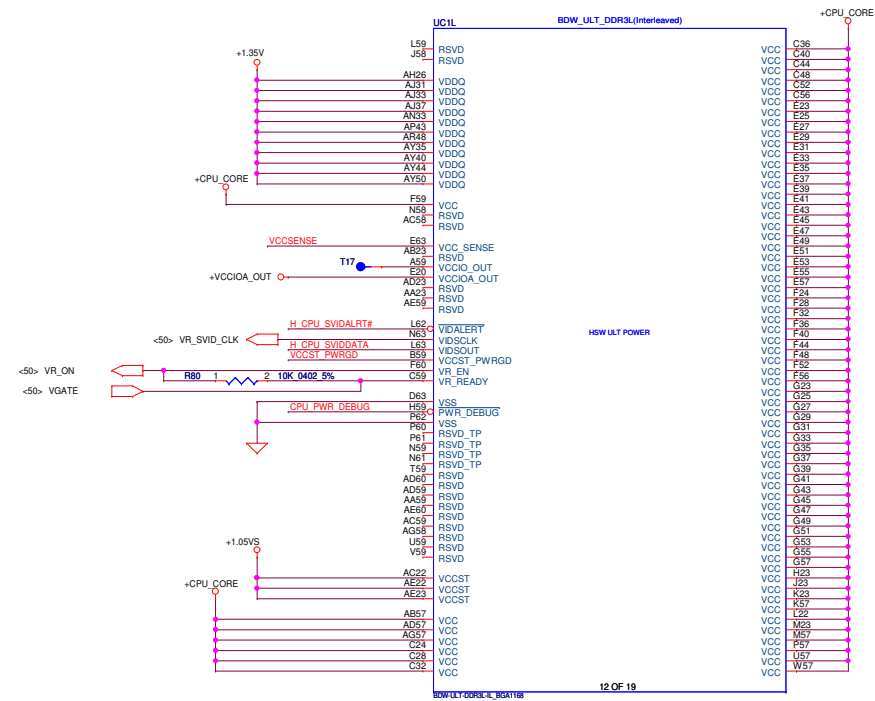
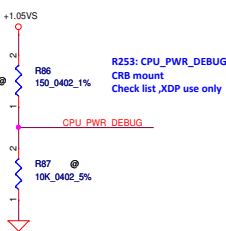
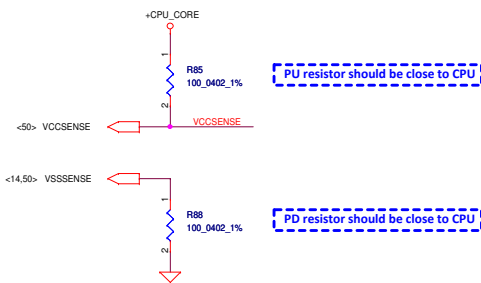
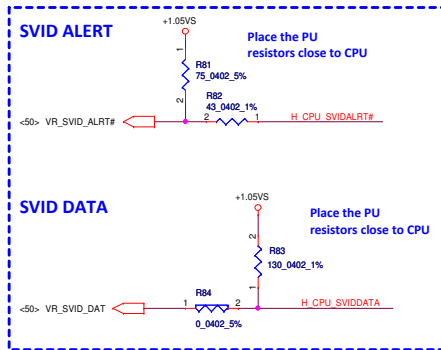
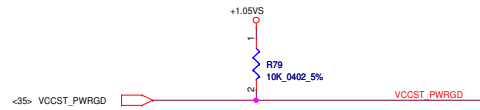
LAN

WLAN

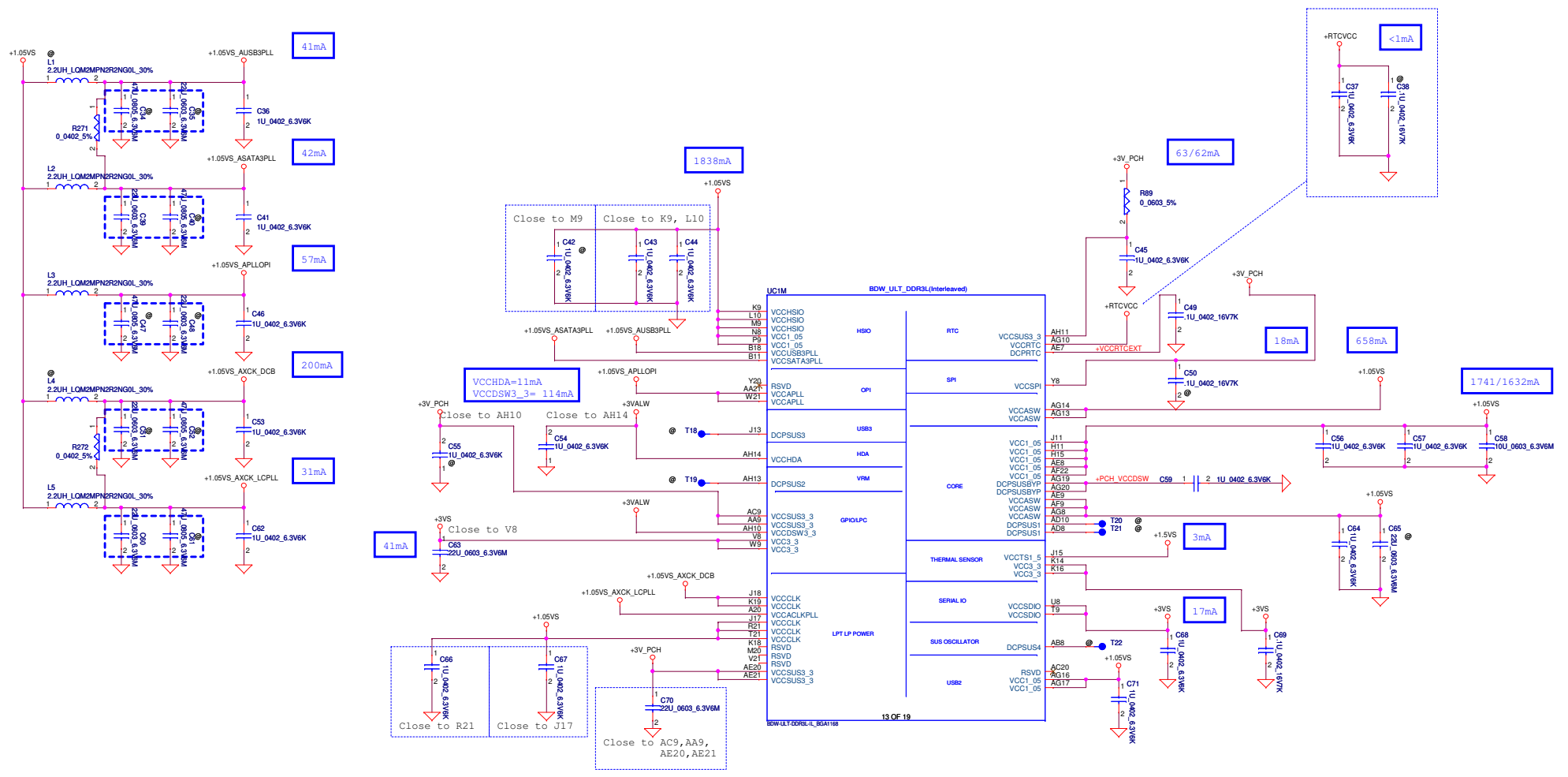
USB2/3 Docking
(For B15)

Card Reader
(For B14/E14/B15)

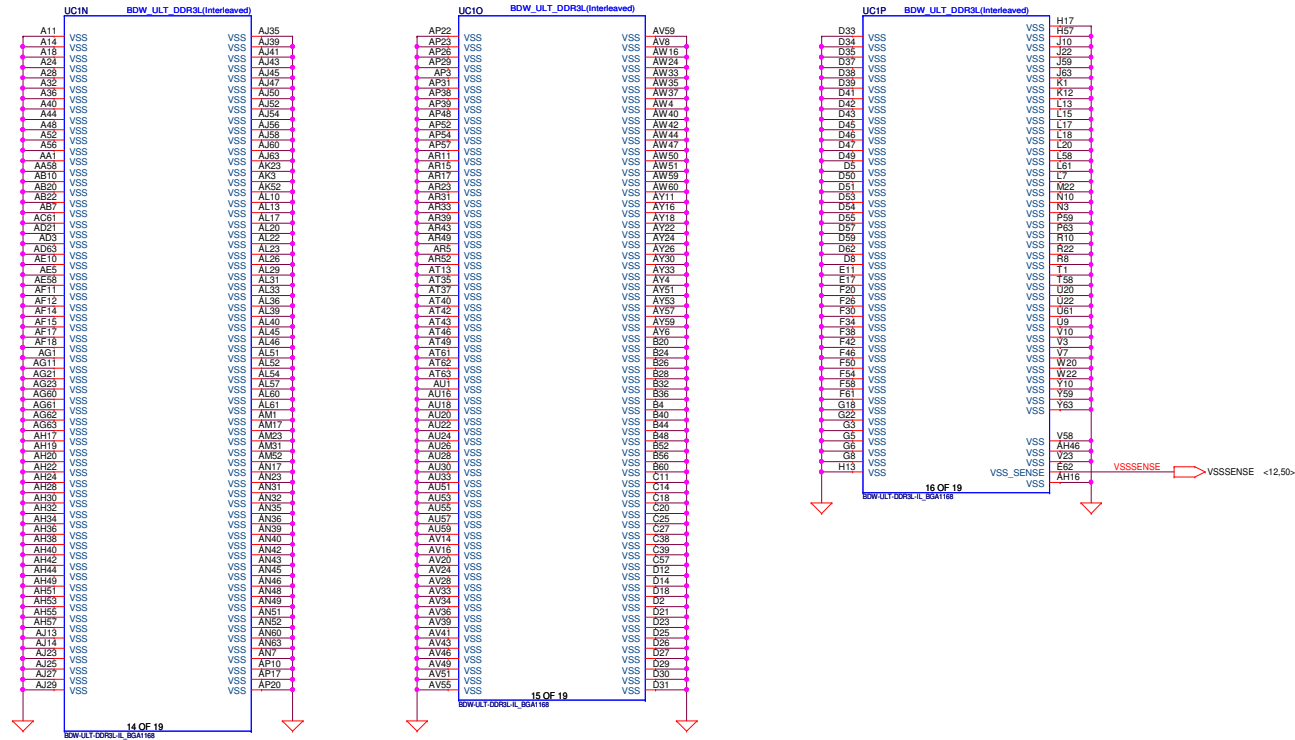


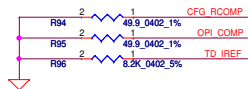
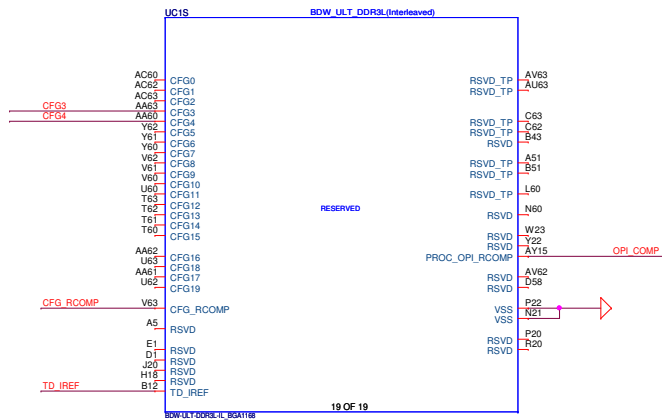
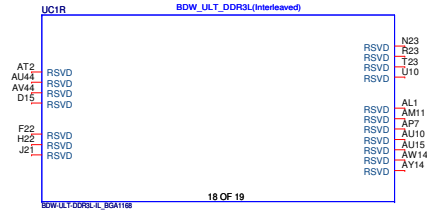
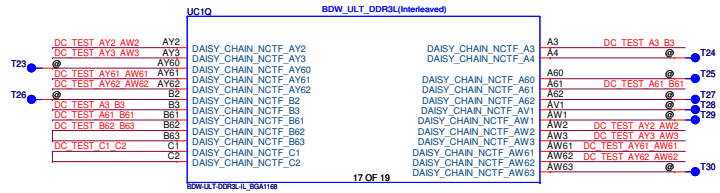


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Size	Document Number	Rev	
C	LA-B092P	1.0	
Date:	Tuesday, February 18, 2014	Sheet	12 of 53

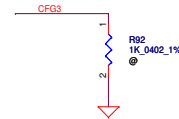


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Size	Document Number	Rev		
C	LA-B092P	1.0		
Date:	Tuesday, February 18, 2014	Sheet	13	of 53

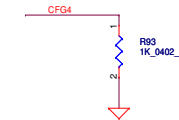




CFG Straps for Processor

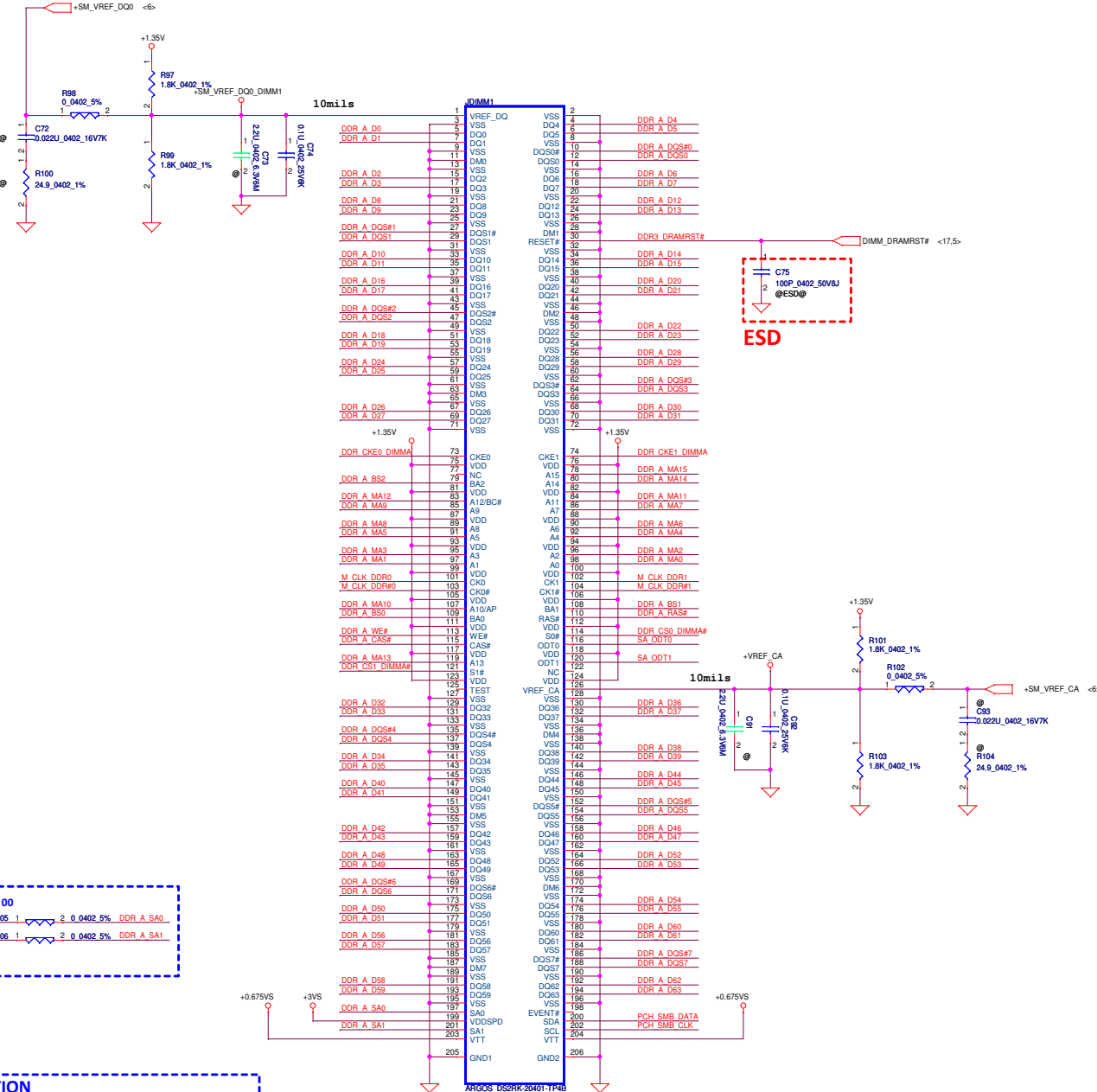
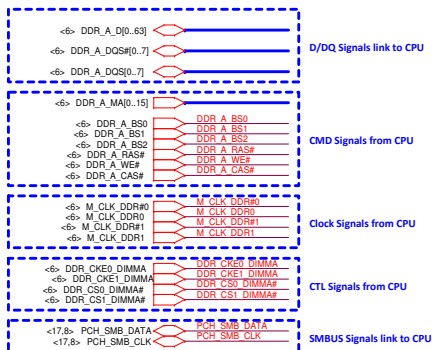


Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

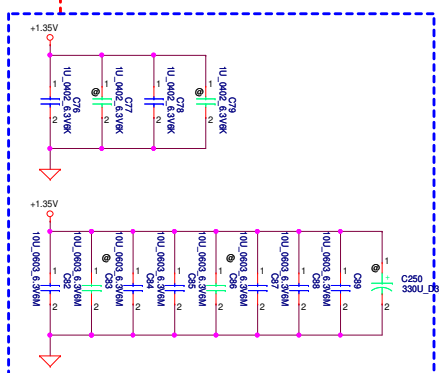


Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

DIMM1 Reverse Type Near CPU

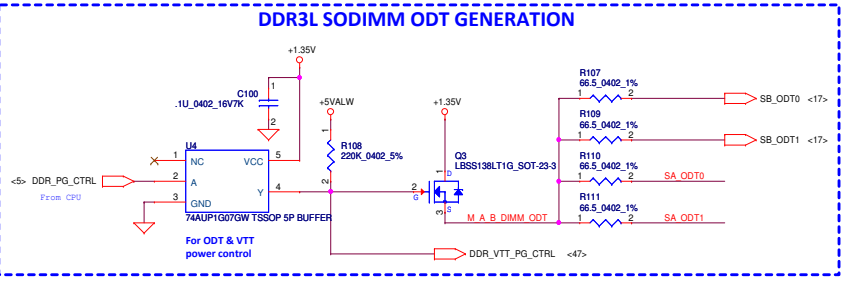
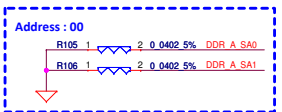
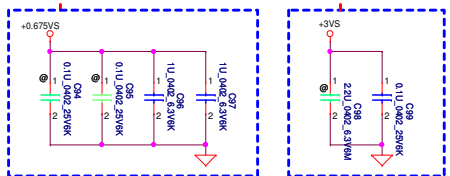


Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204

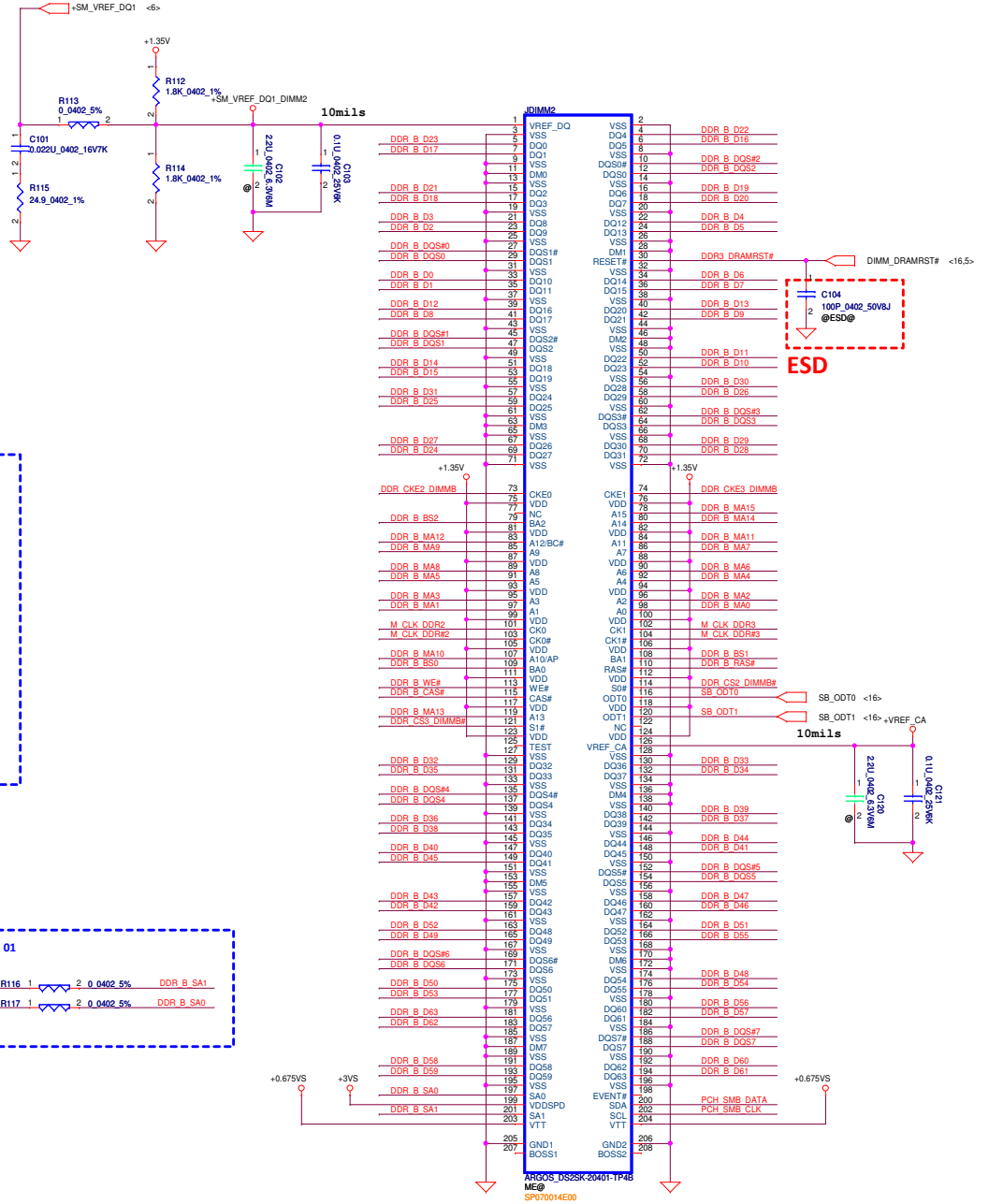
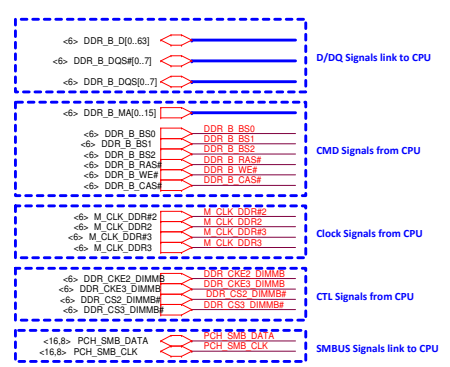
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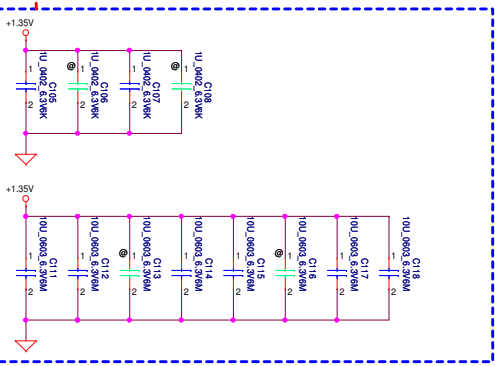
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Title				DDR3L DIMMA	
Size C				Document Number LA-B092P	
Date: Tuesday, February 18, 2014				Sheet 16 of 53	

Interleaved Memory

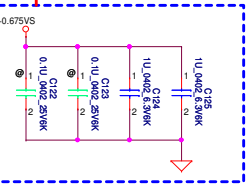
DIMM2 Standard Type Near User



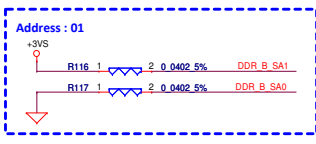
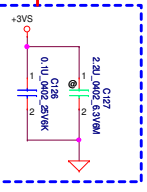
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Layout Note:
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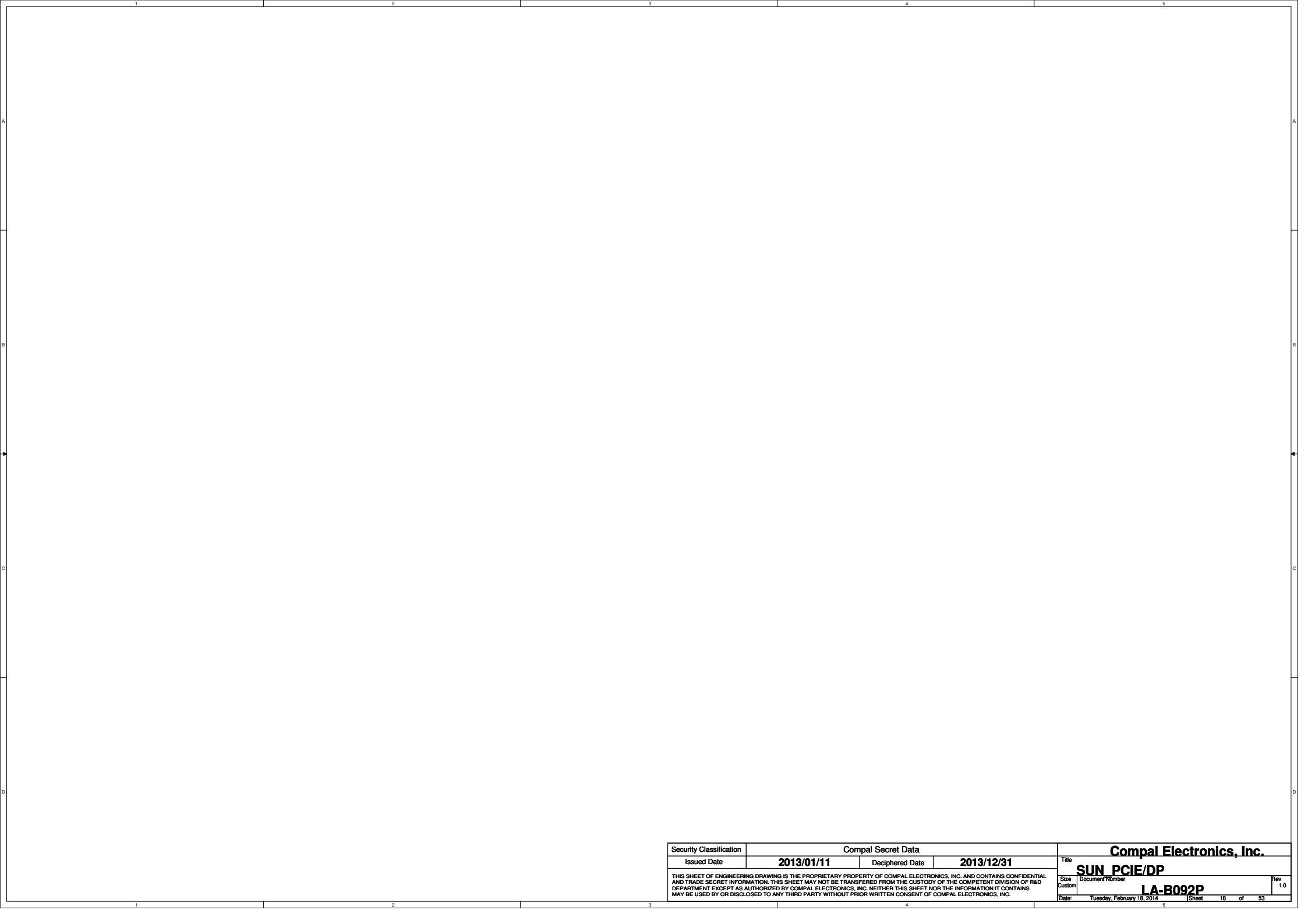


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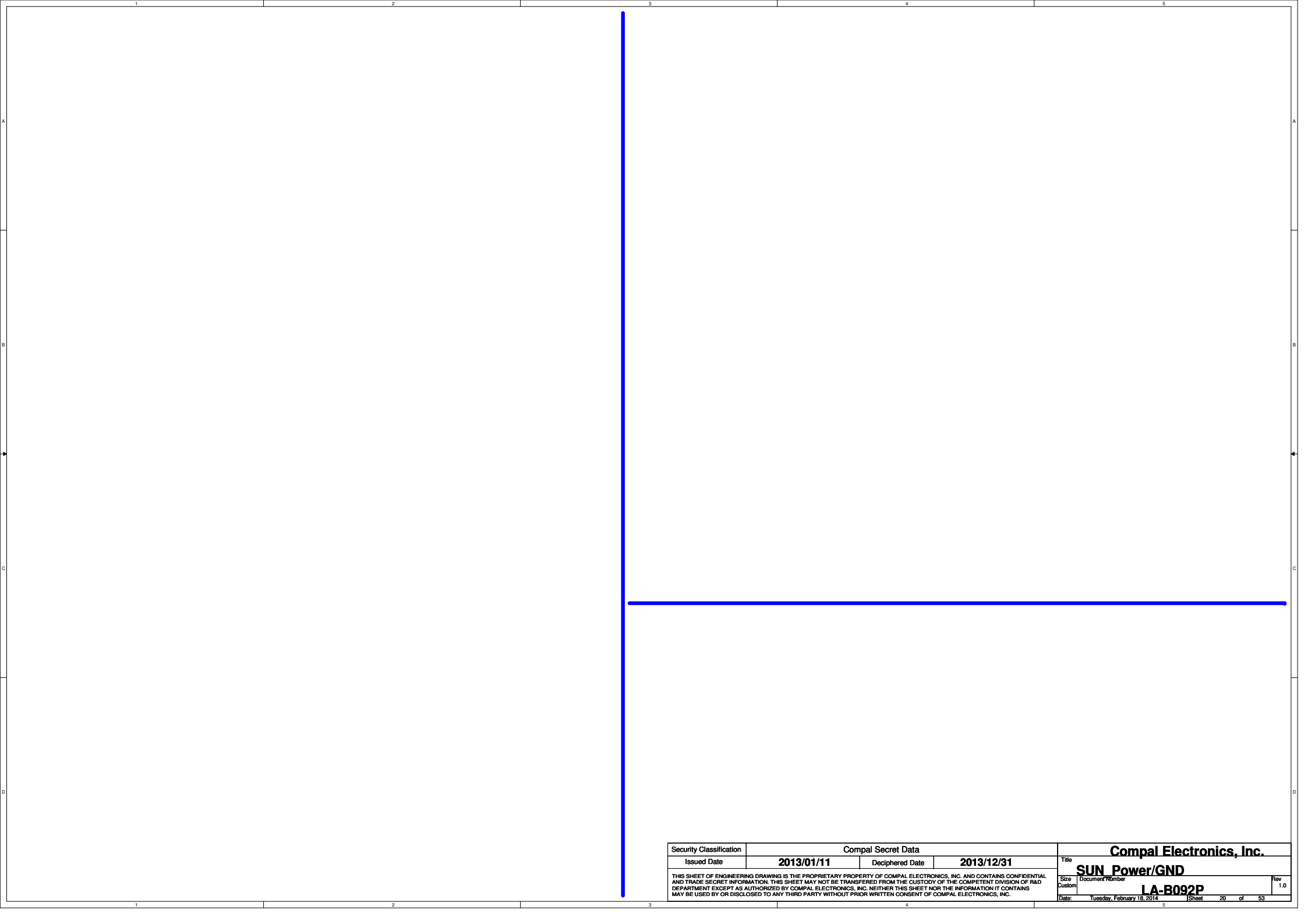
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Date:	Tuesday, February 18, 2014	Sheet	17	of 53

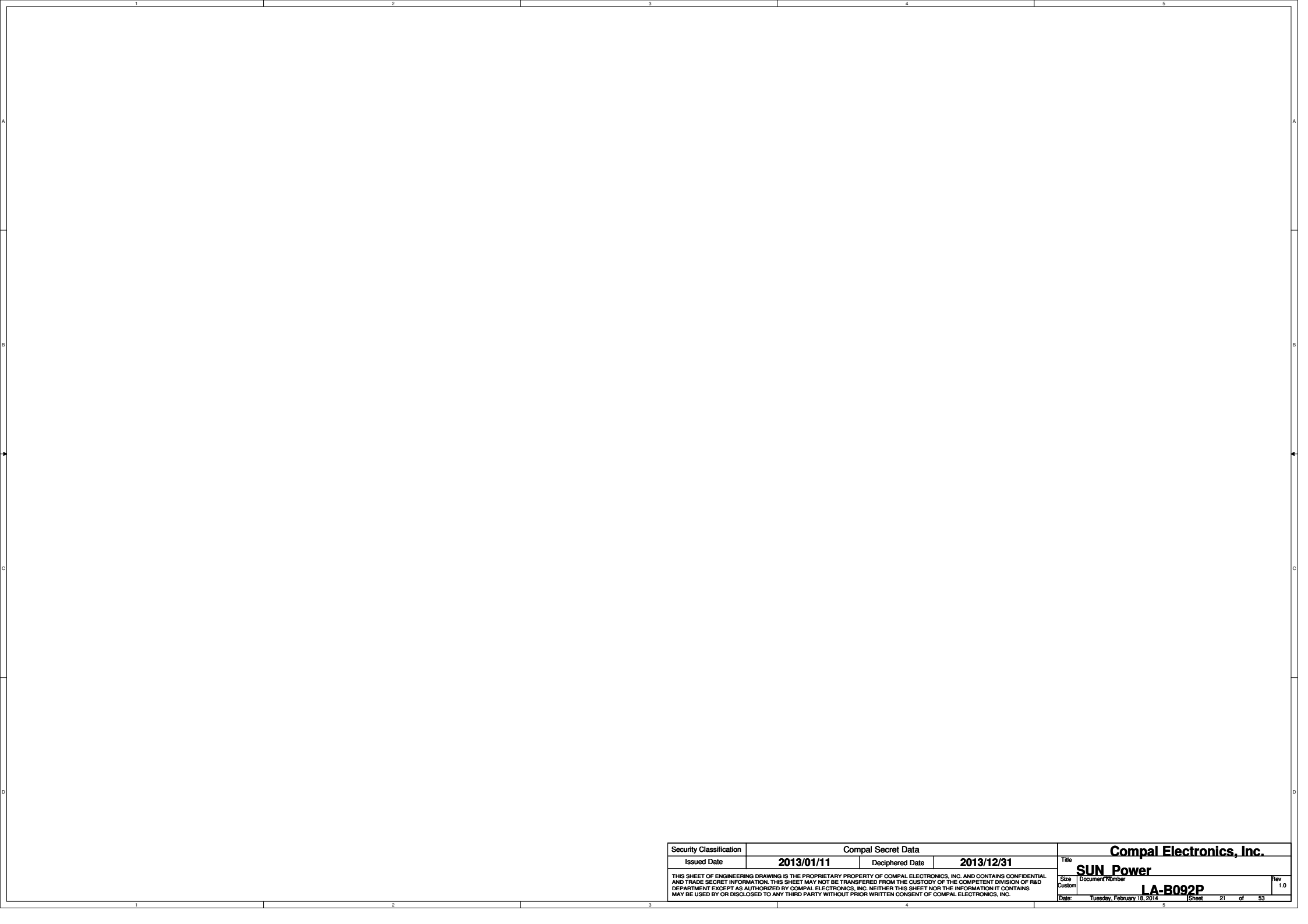


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				Date	Rev
				Tuesday, February 18, 2014	1.0
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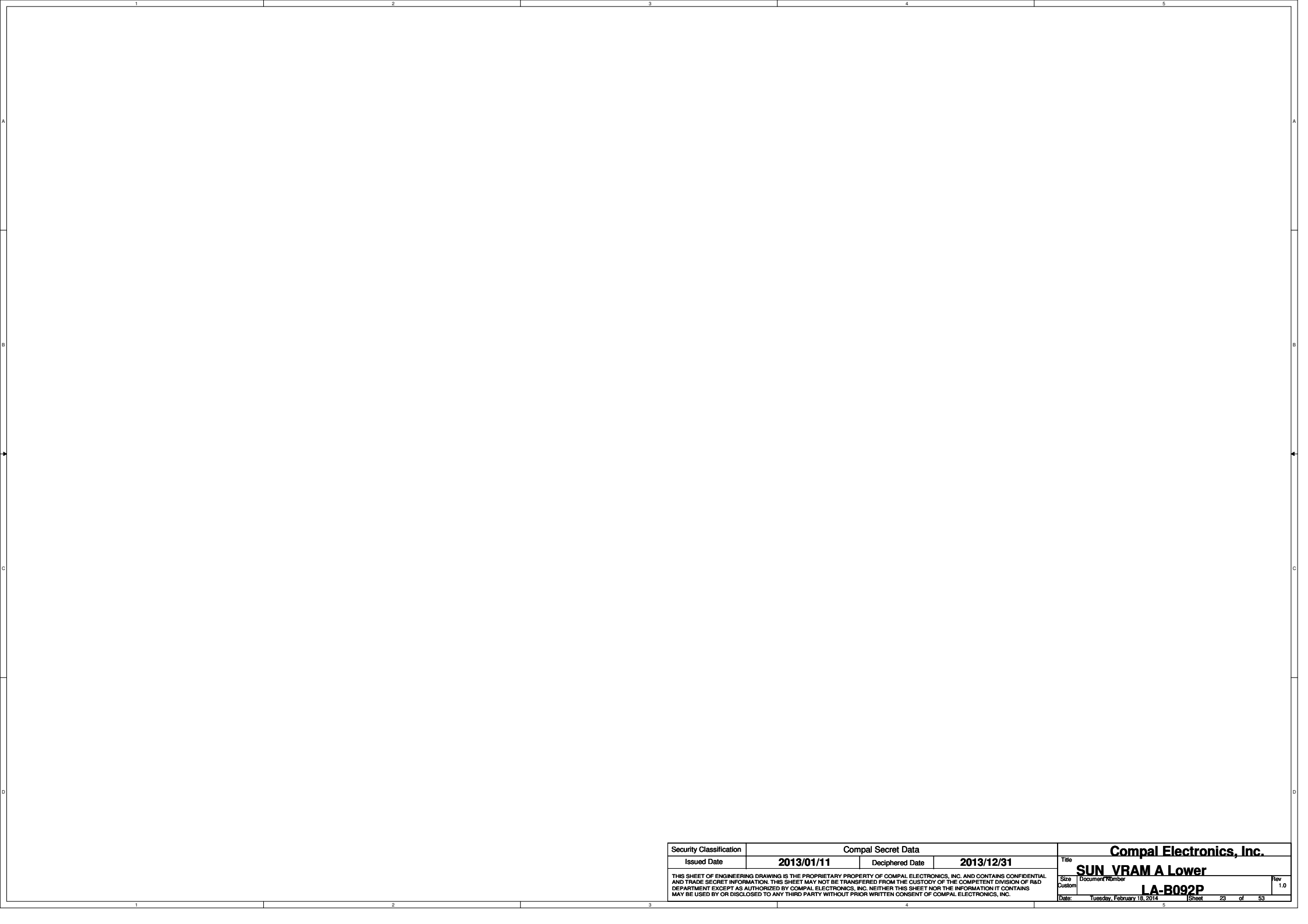


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				Date:	Tuesday, February 18, 2014	Sheet	20 of 53

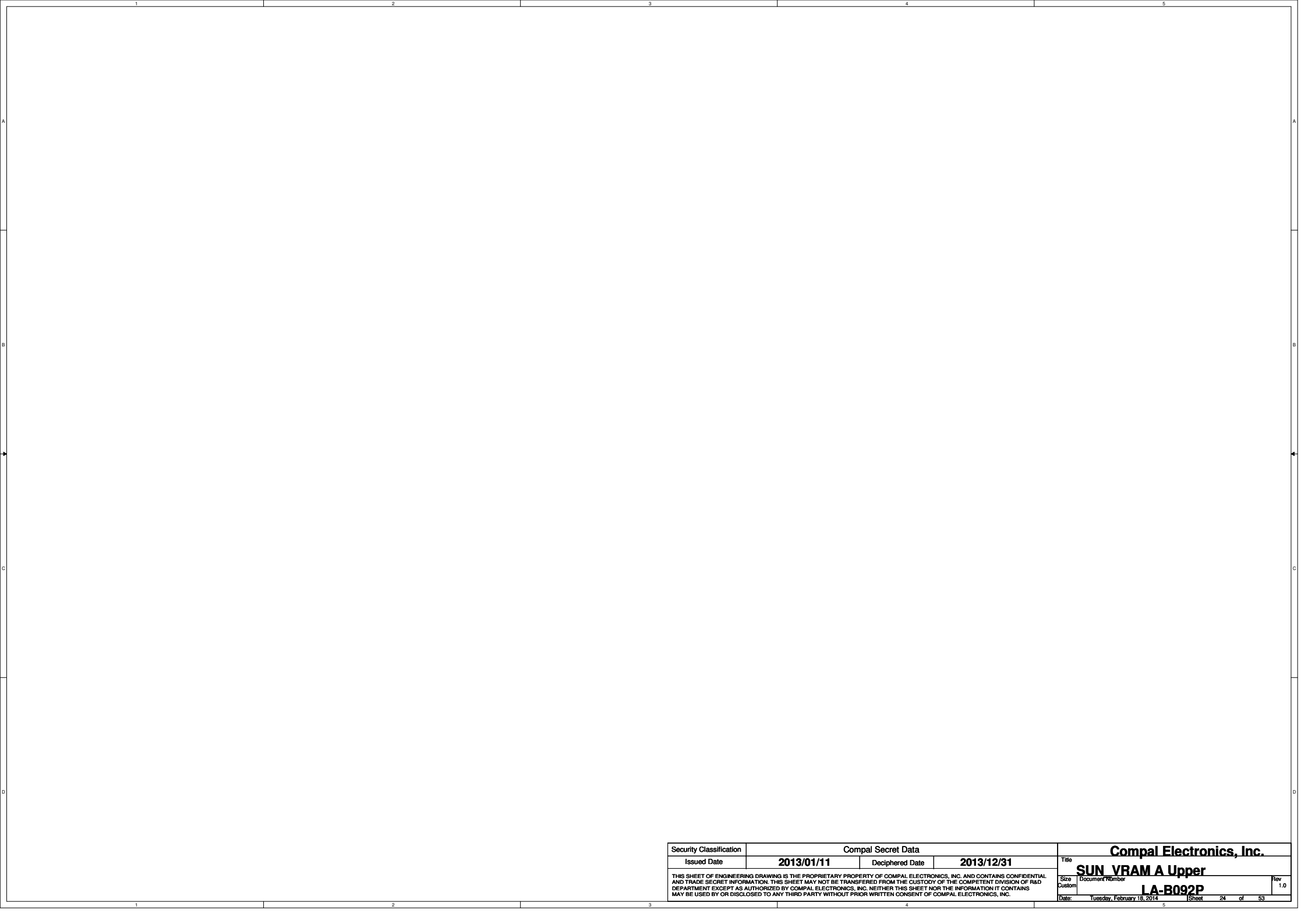


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Date: Tuesday, February 18, 2014				Sheet	21 of 53

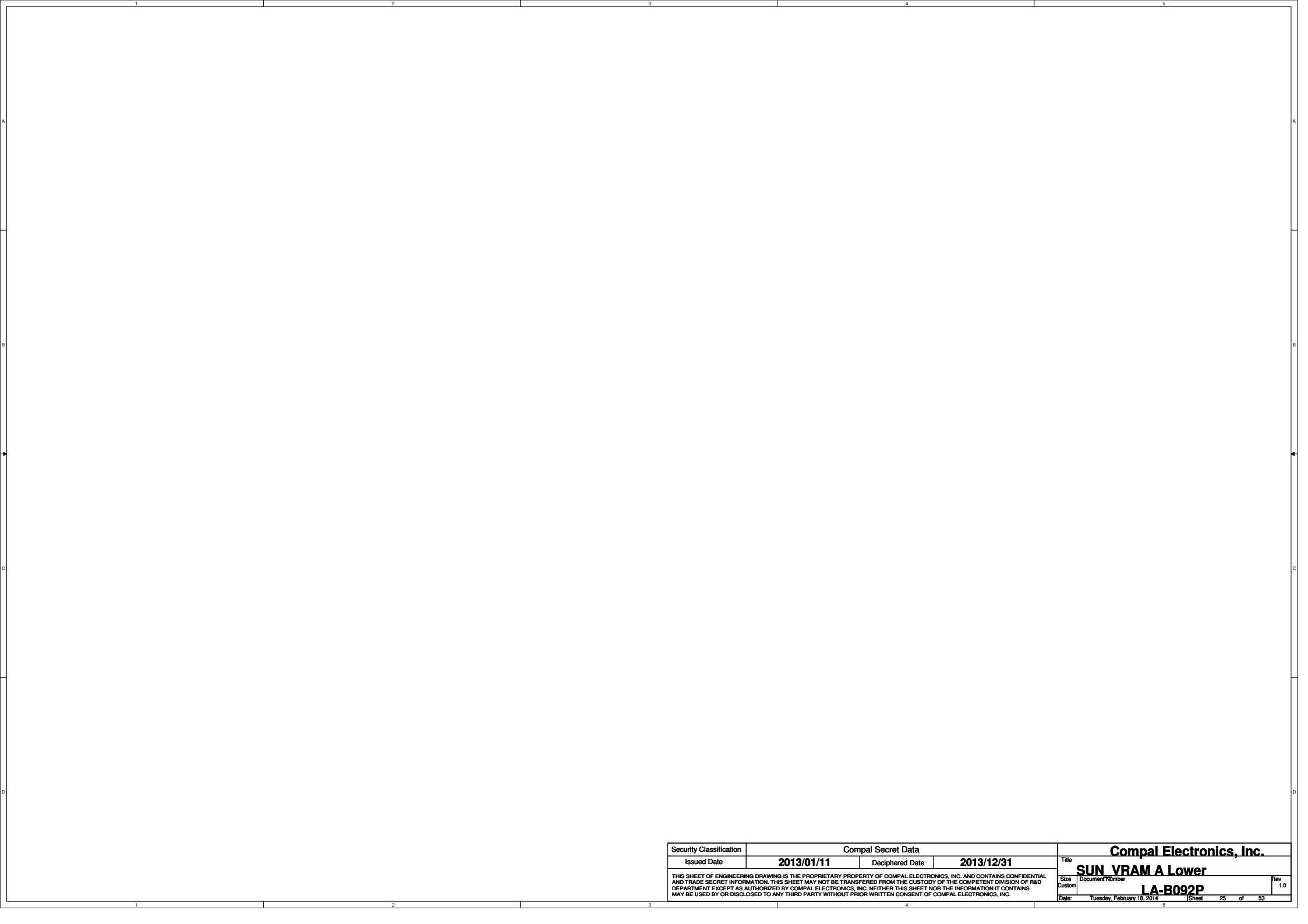
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				Date:	Tuesday, February 18, 2014
				Sheet	22 of 53



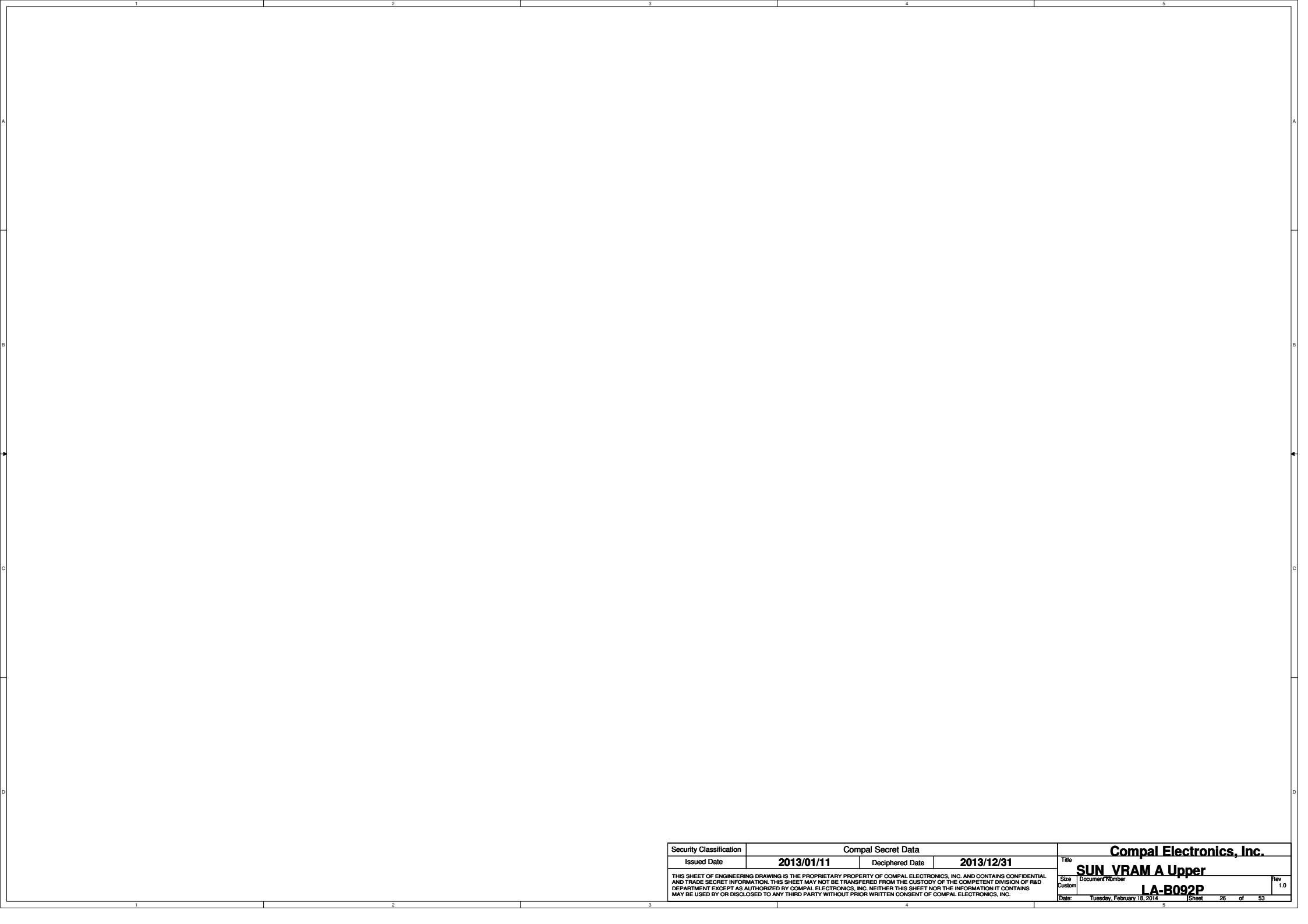
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Date: Tuesday, February 18, 2014				Sheet	23 of 53



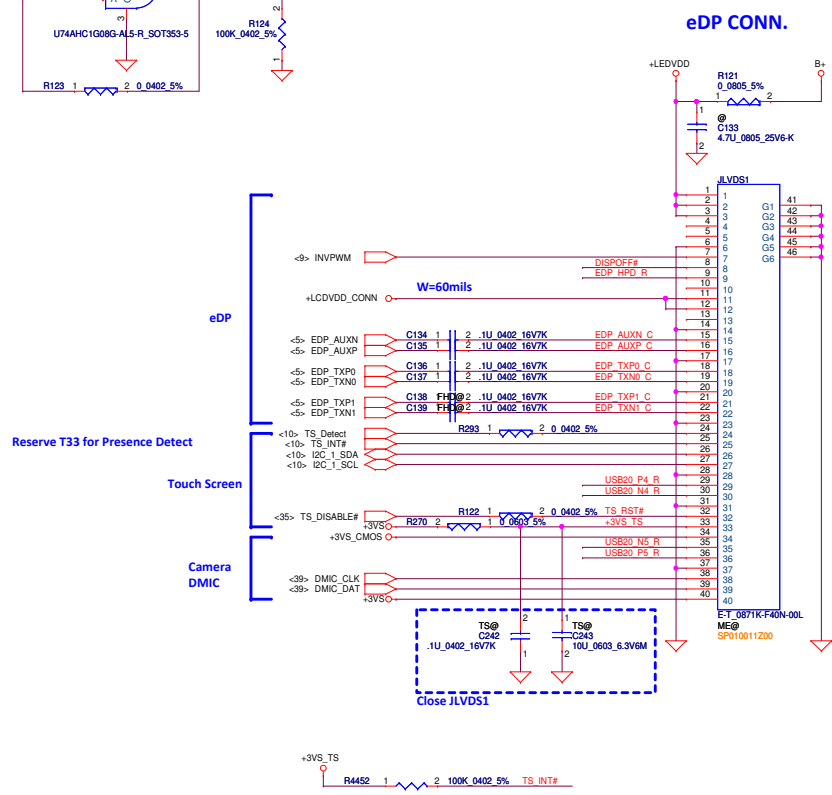
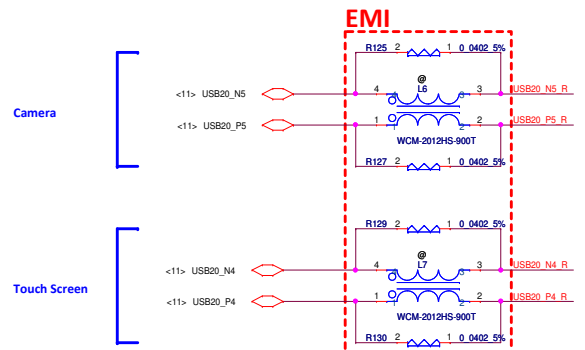
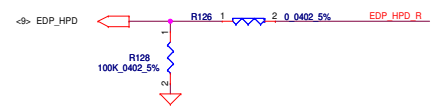
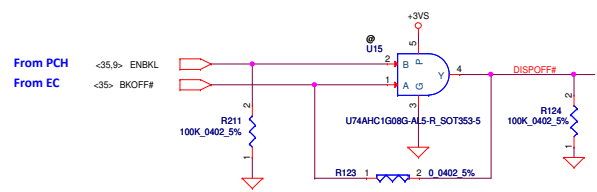
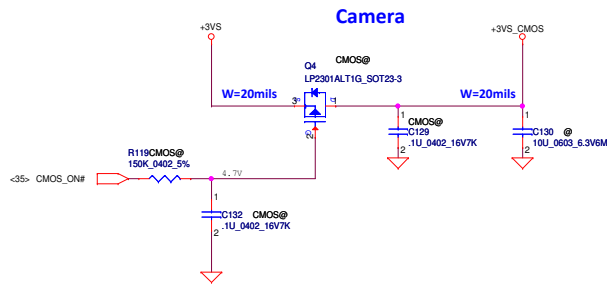
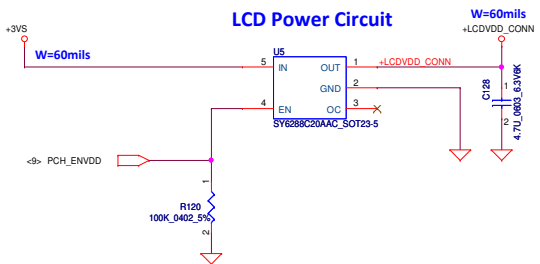
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Date: Tuesday, February 18, 2014				Rev	1.0
Sheet 24 of 53					



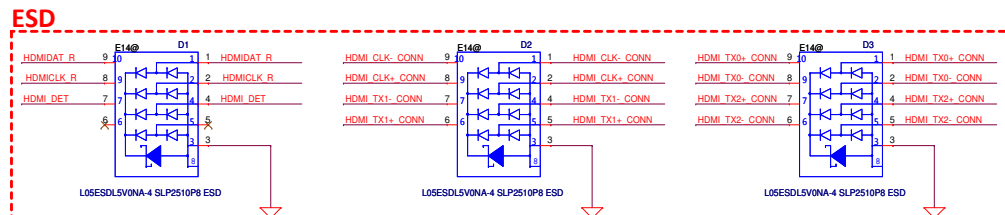
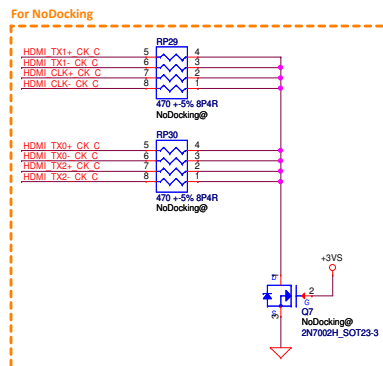
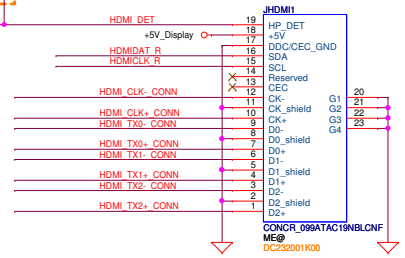
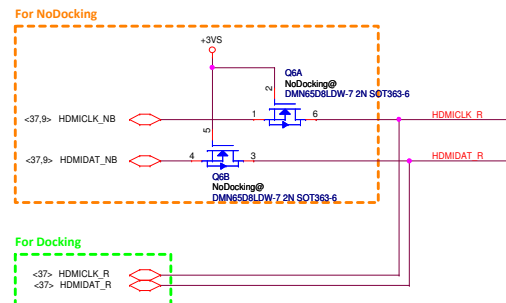
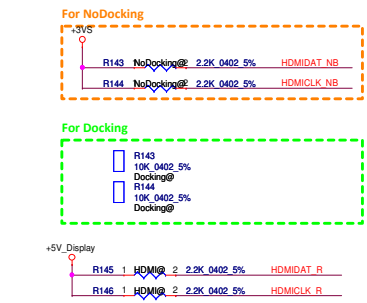
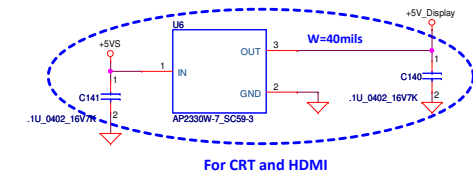
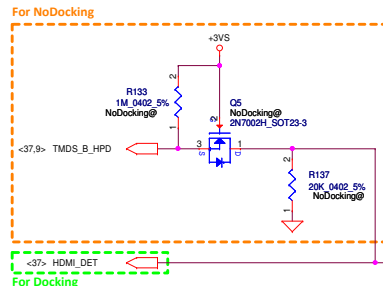
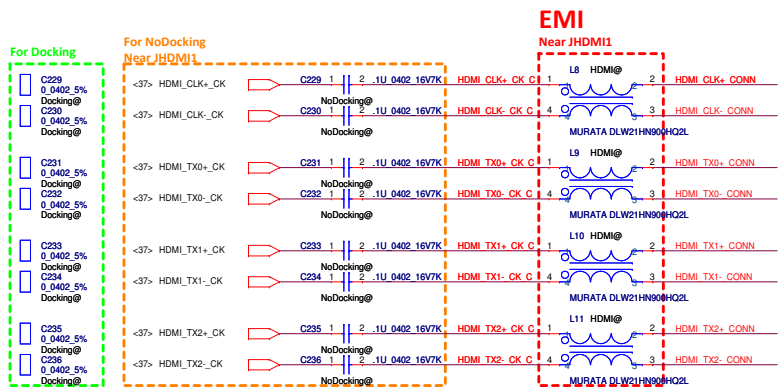
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				Date:	Tuesday, February 18, 2014
				Sheet	25 of 53



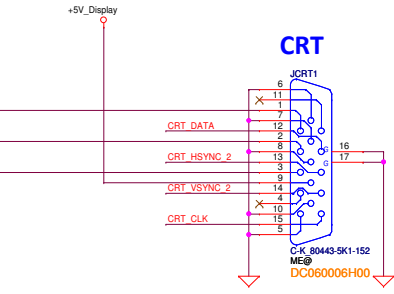
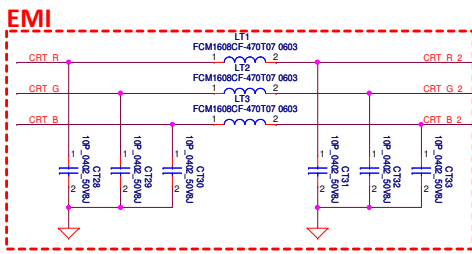
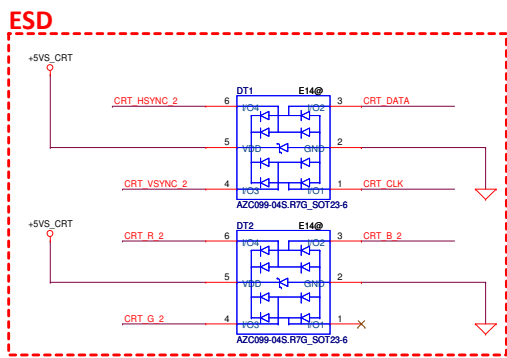
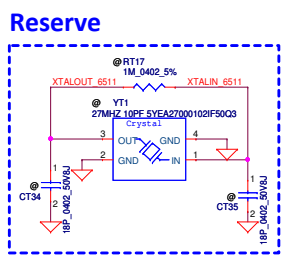
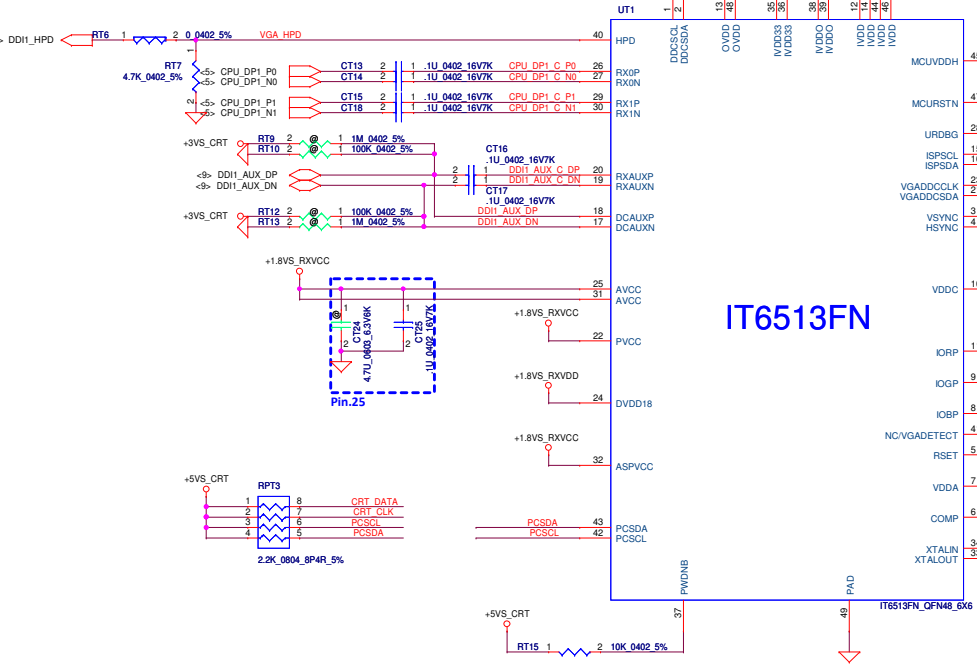
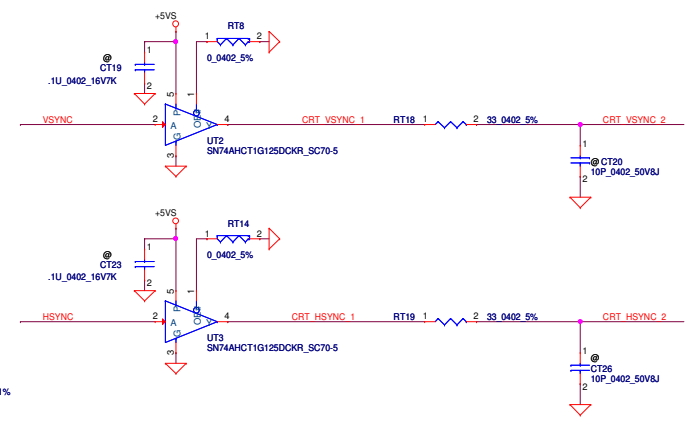
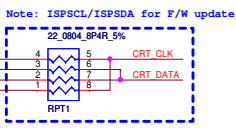
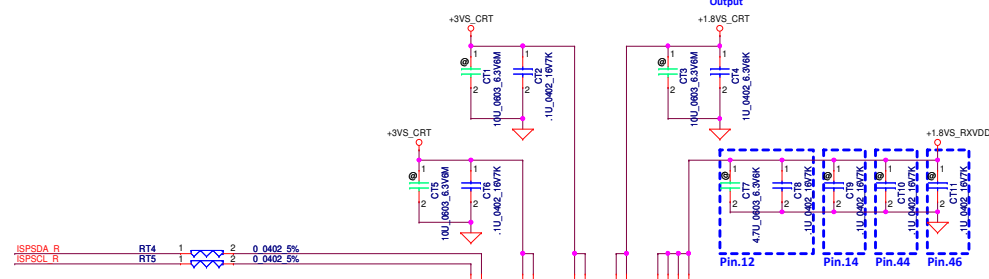
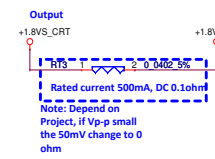
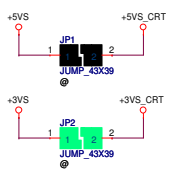
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Date: Tuesday, February 18, 2014				Sheet	26 of 53



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Date: Tuesday, February 18, 2014				Sheet 27 of 53

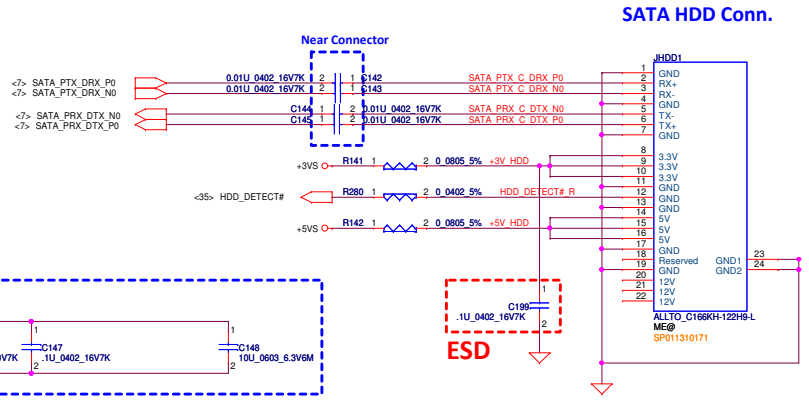


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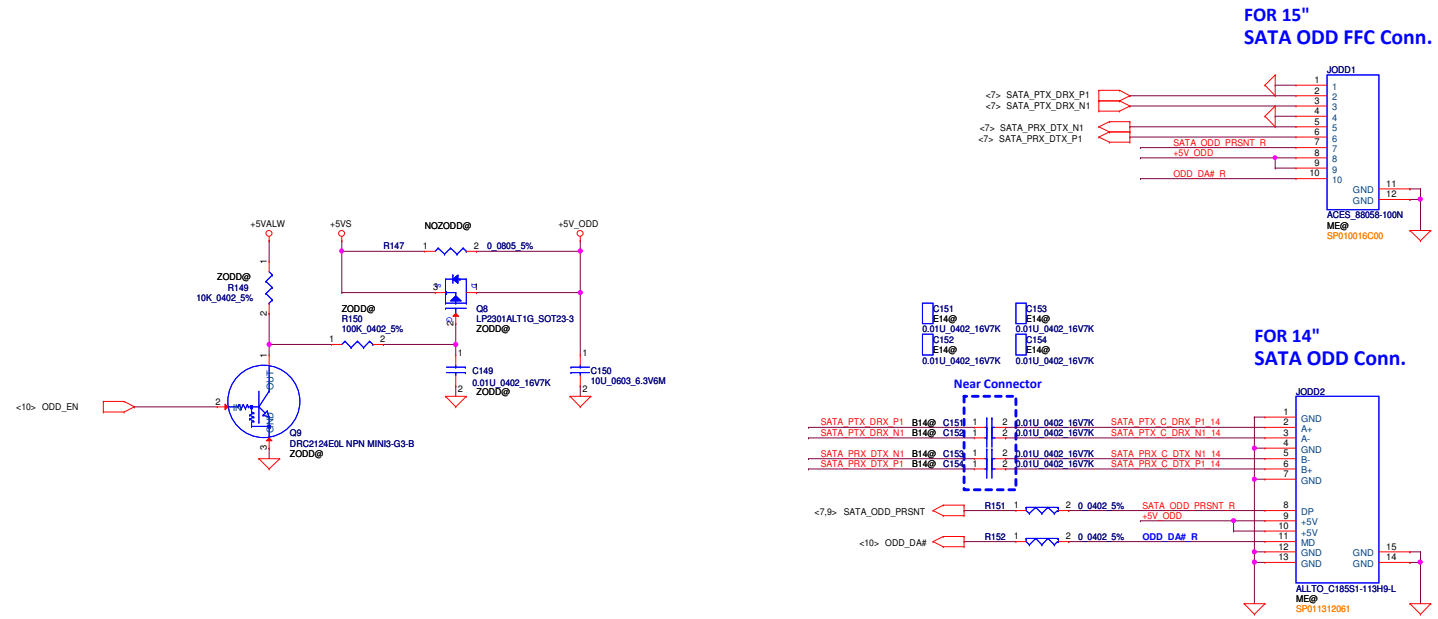


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Date:	Tuesday, February 18, 2014	Sheet	29	of 53

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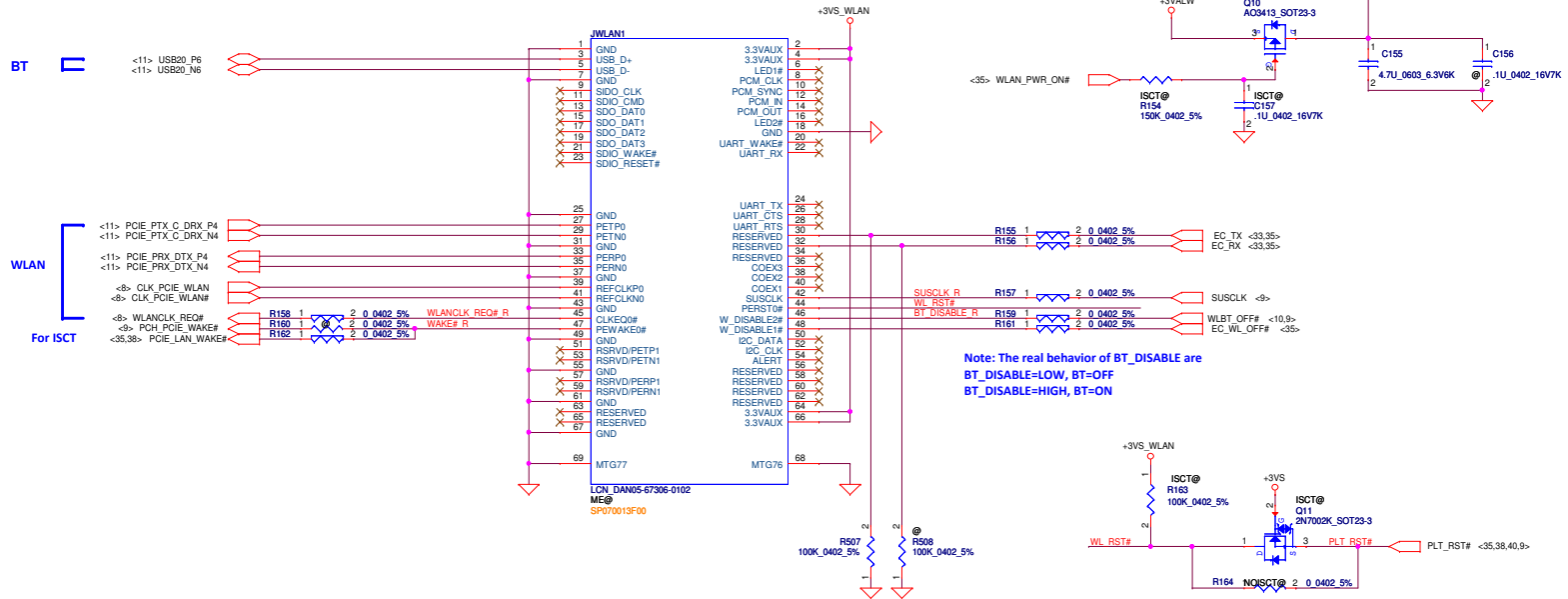


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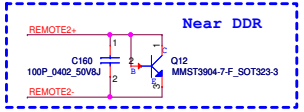
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Support ISCT(Intel Smart Connect Technology)

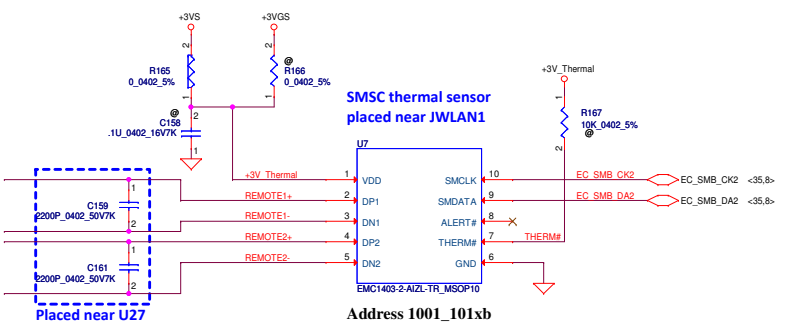


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Size	Document Number	LA-B092P		Rev	1.0
Date:	Tuesday, February 18, 2014	Sheet	31	of	53

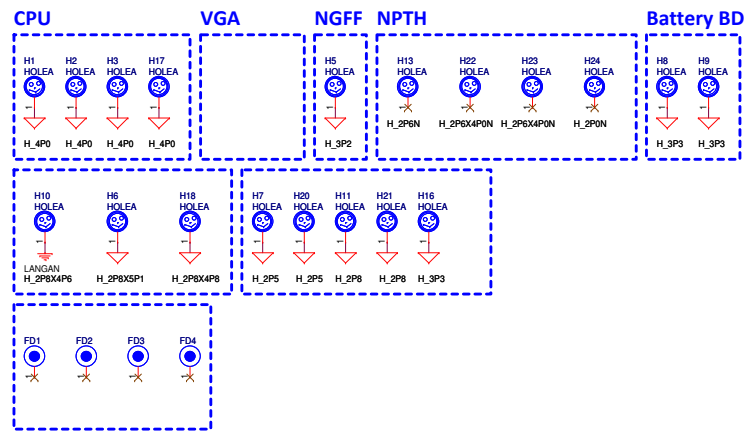
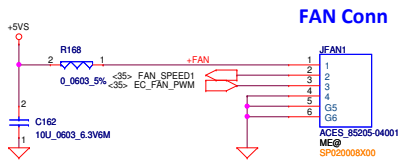
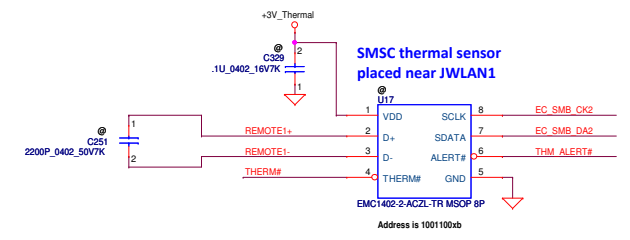
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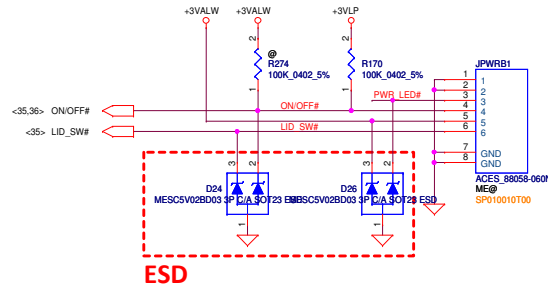
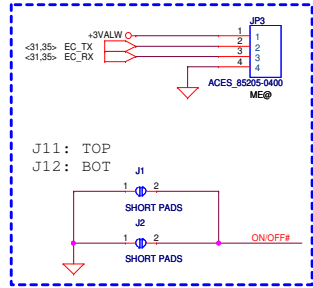
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2 Channel



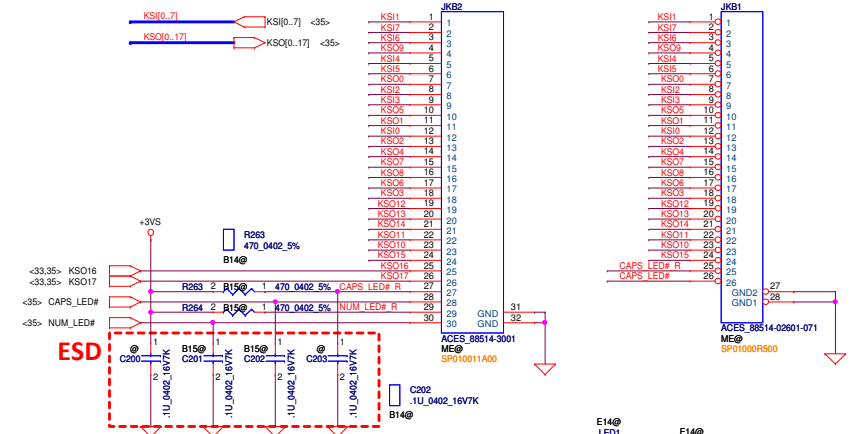
For Debug



ESD

KB For B15

KB For B14/E14



ESD

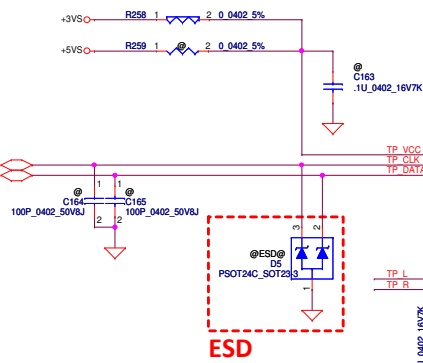
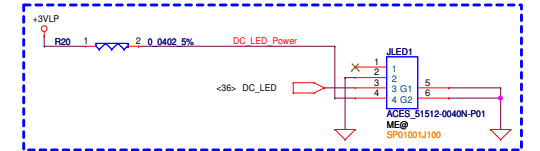
Power (Green) (E14)

Battery (Amber) (B14/B15/E14)

Battery (Green) (B14/B15/E14)

HDD (Green) (B14/B15/E14)

DC-In LED (Green) For B14 / E14



For B15/E14

RP33 0_0804_8P4R_5% E14@

RP34 0_0804_8P4R_5% E14@

For B14

RP35 0_0804_8P4R_5% B14@

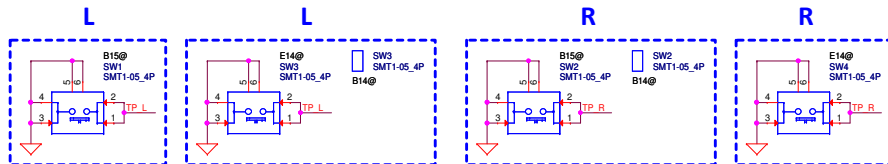
RP36 0_0804_8P4R_5% B14@

For B15/E14 TP module(100*50)

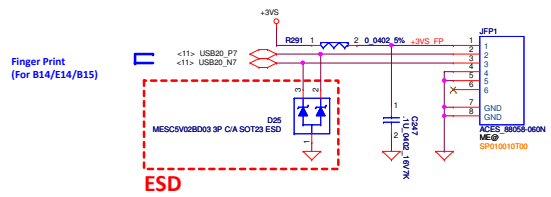
1	1	VCC	1	VCC
2	2	CLK	2	CLK
3	3	DAT	3	DAT
4	4	GND	4	L
5	5	L	5	R
6	6	R	6	GND

For B14 TP module(84*42)

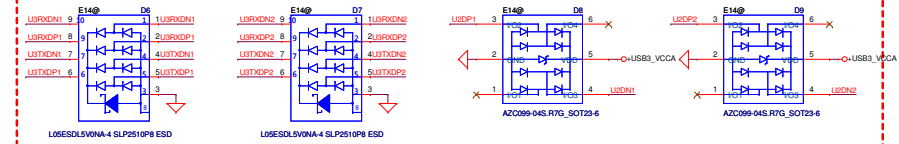
6	1	VCC	1	VCC
5	2	CLK	2	CLK
4	3	DAT	3	DAT
3	4	GND	4	L
2	5	L	5	R
1	6	R	6	GND



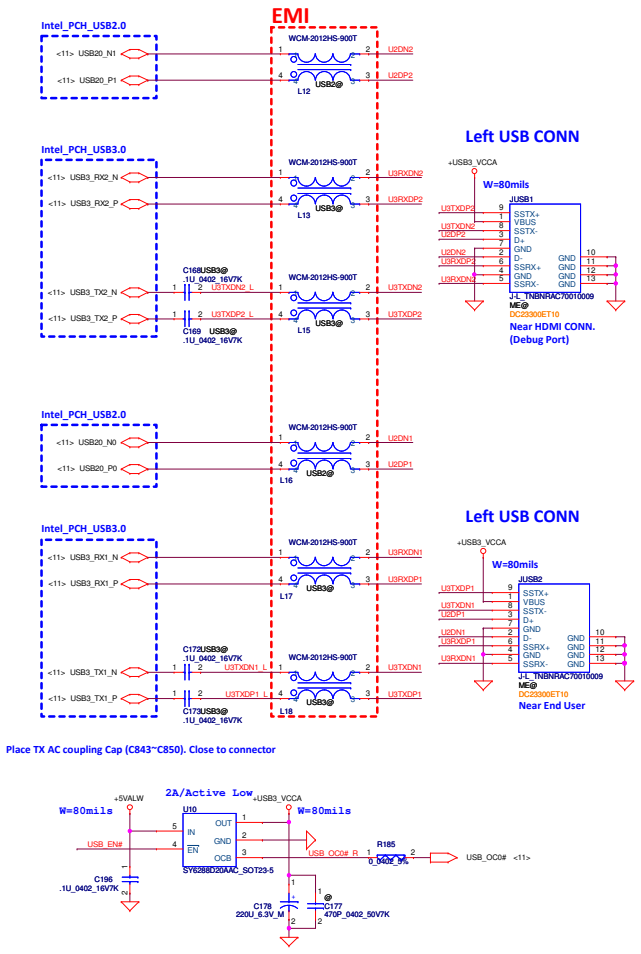
Finger Print



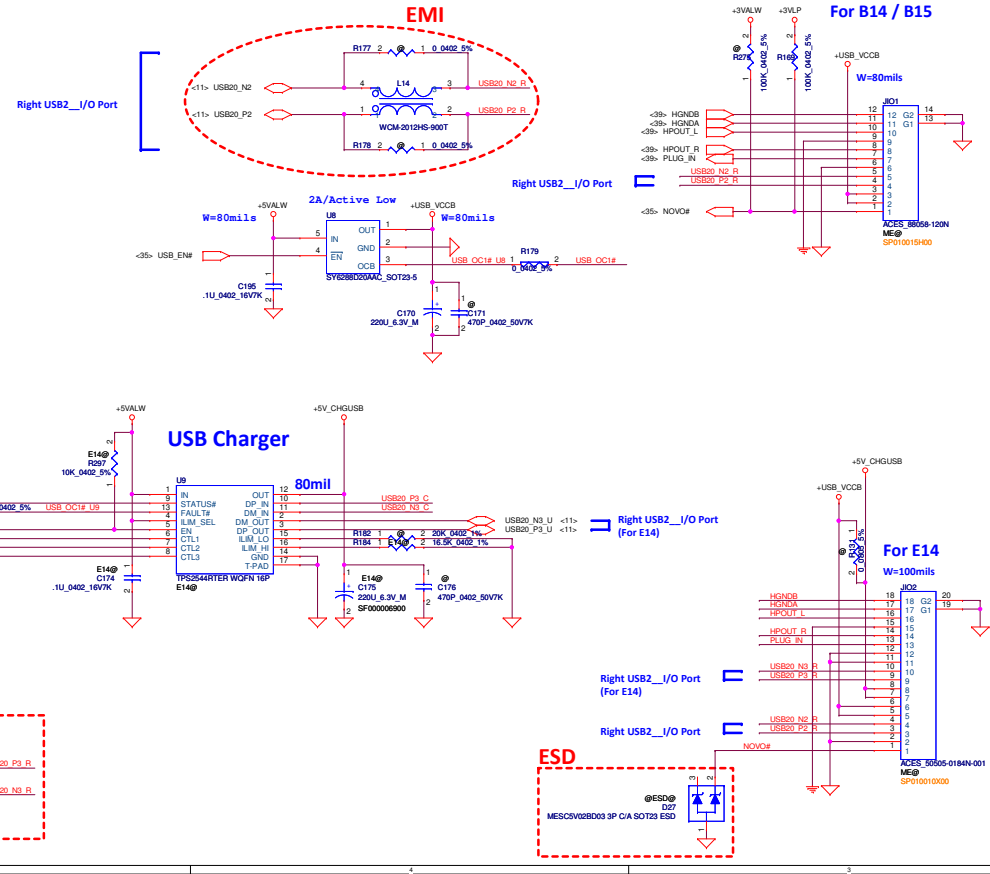
ESD



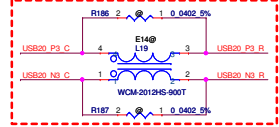
USB3.0_Port



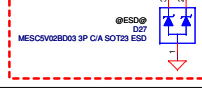
USB2.0_Port



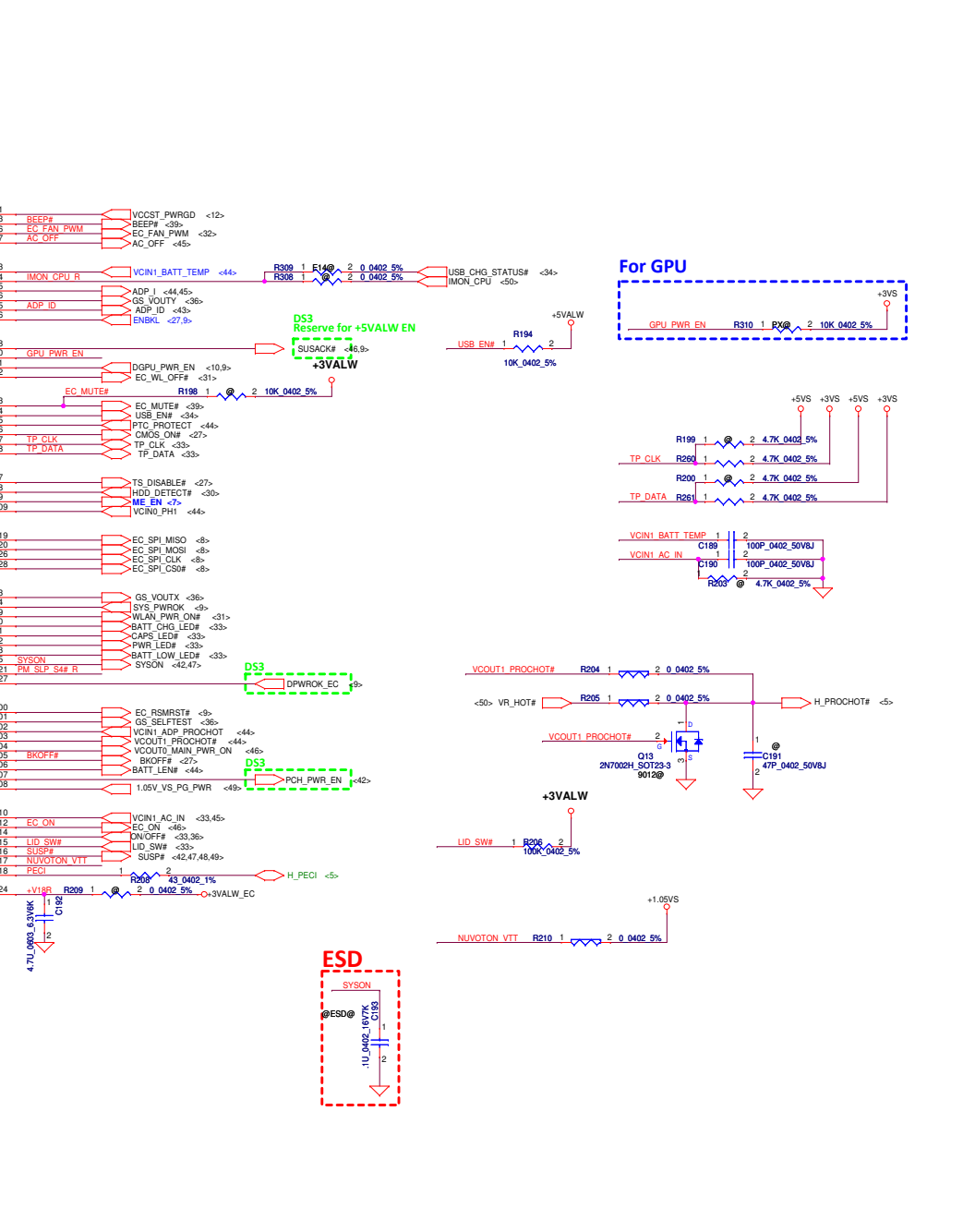
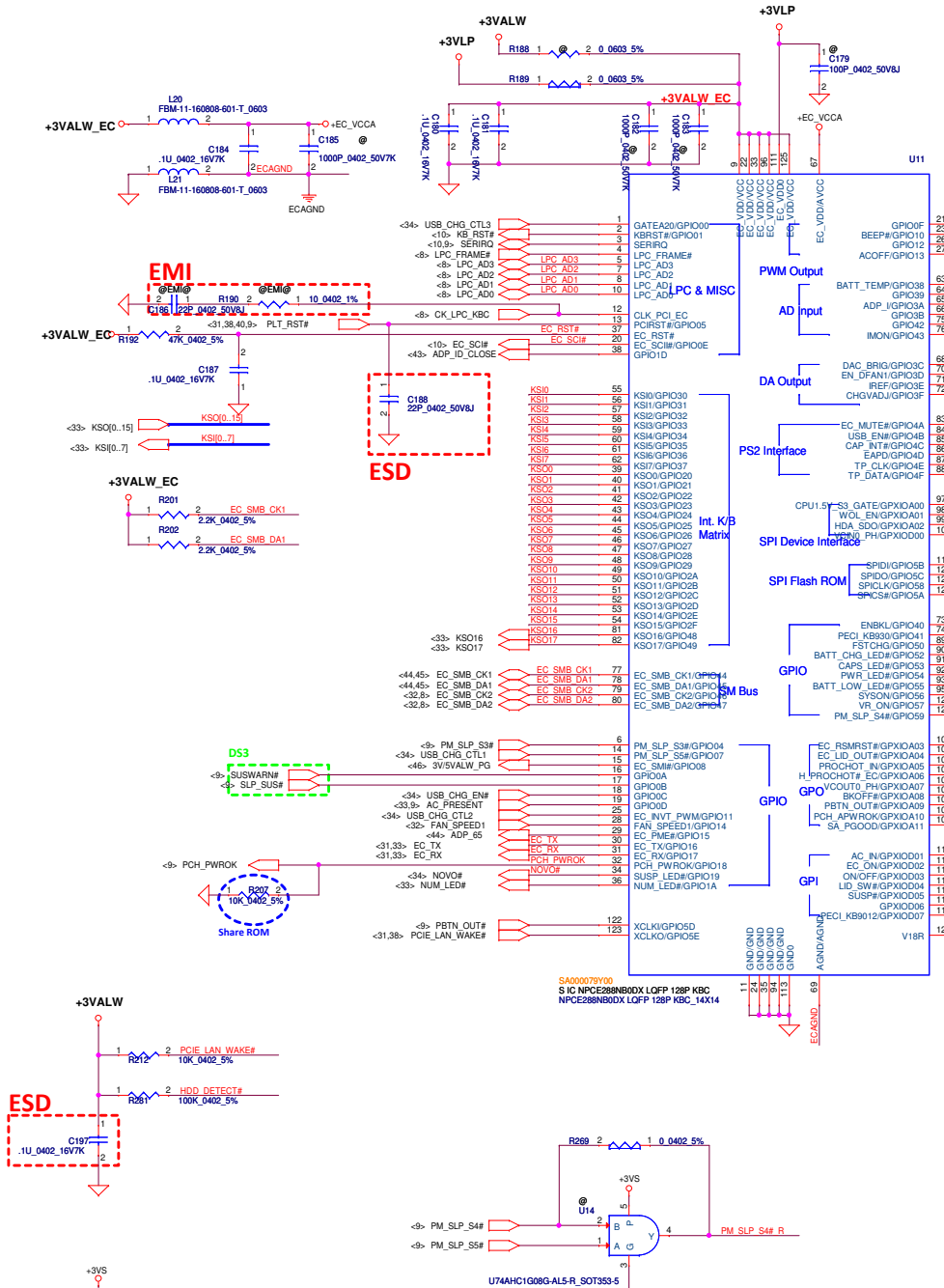
EMI



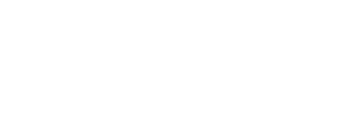
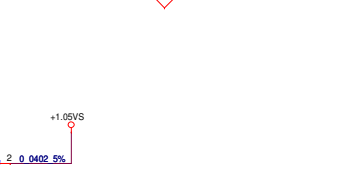
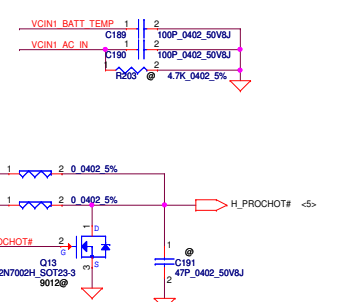
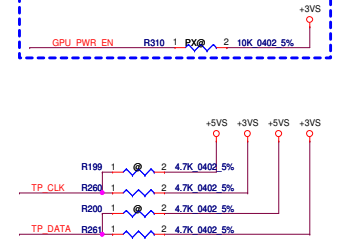
ESD



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Date	Tuesday, February 18, 2014	Sheet	34	of 83



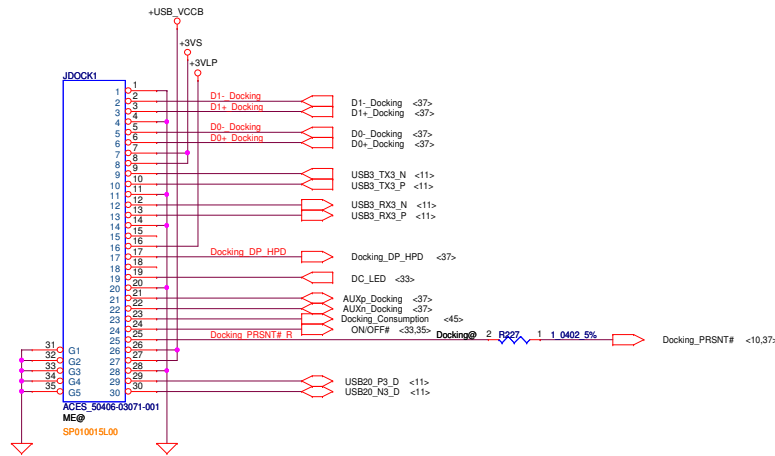
For GPU



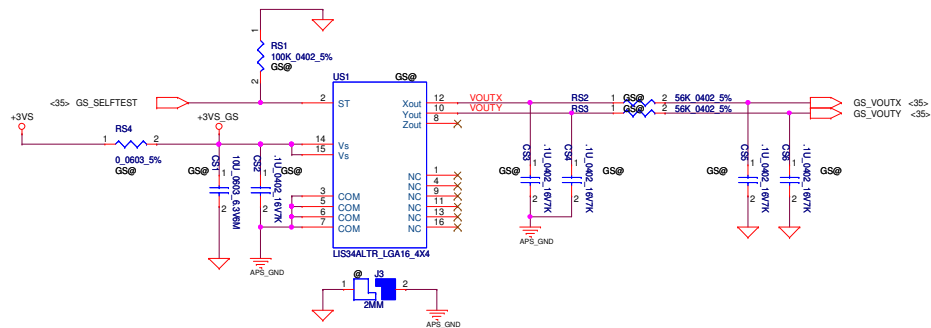
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S IC NPCE288NB0DX LOFP 128P KBC
NPCE288NB0DX LOFP 128P KBC_14X14

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Size	C	Document Number	LA-B092P		Rev
Date:	Tuesday, February 18, 2014	ISheet	35	of	53

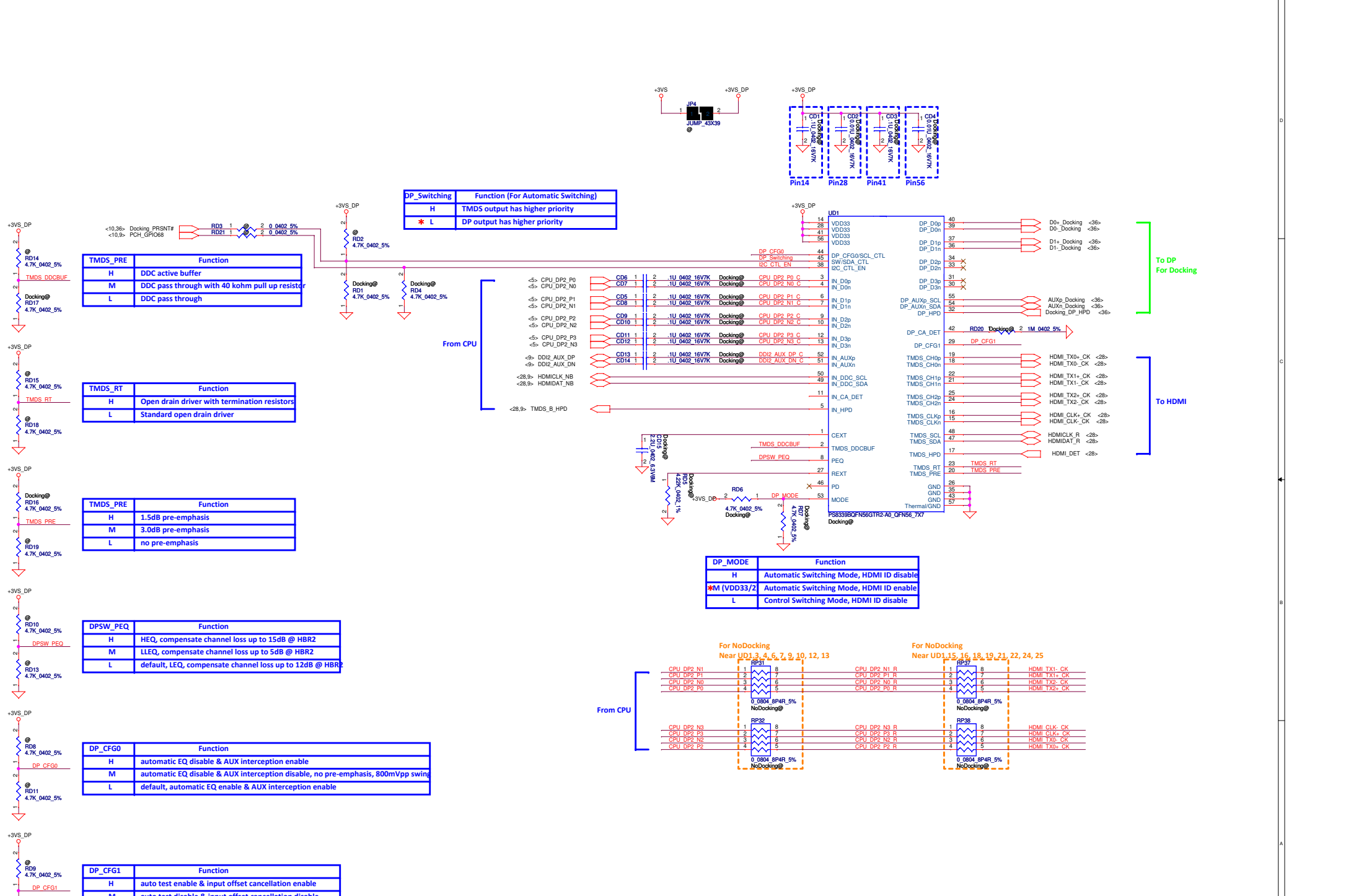
To Docking BD

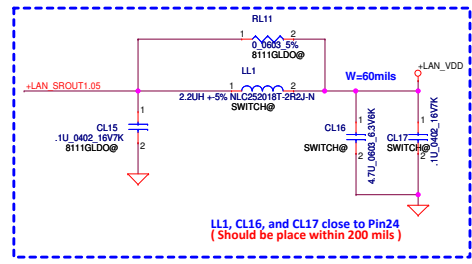
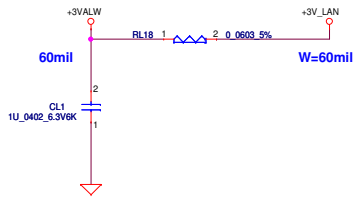


APS (G-Sensor)



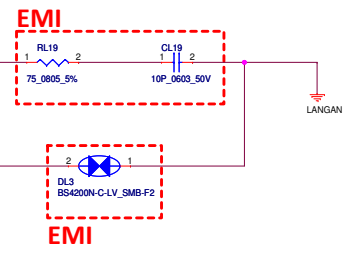
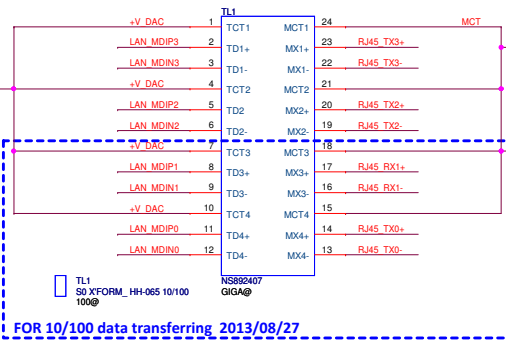
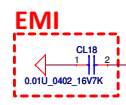
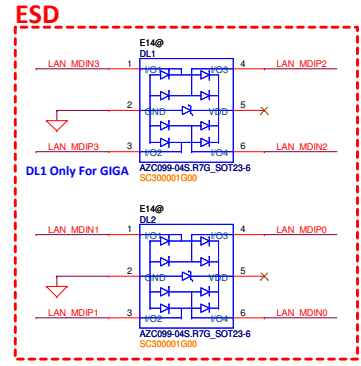
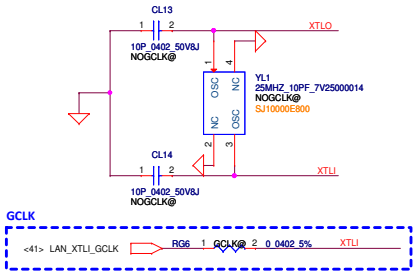
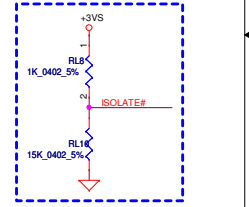
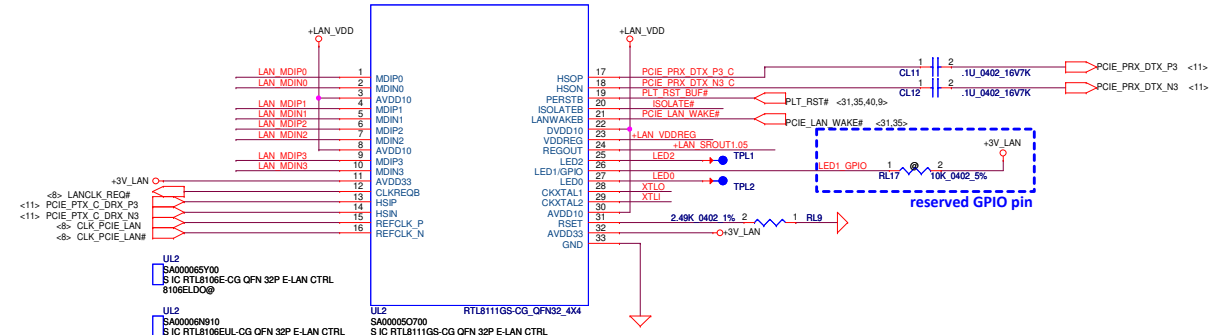
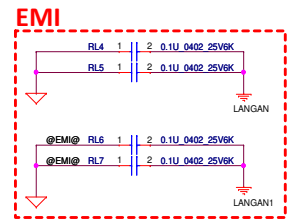
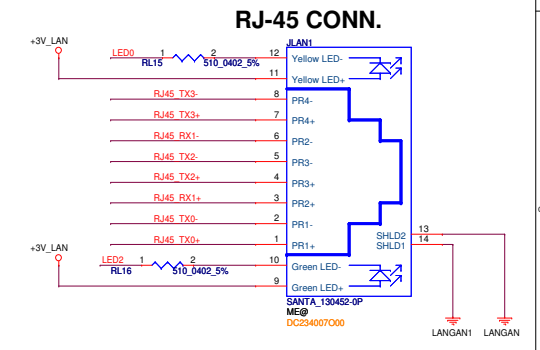
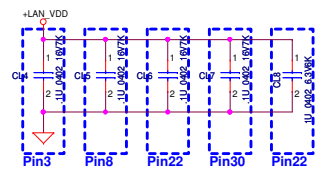
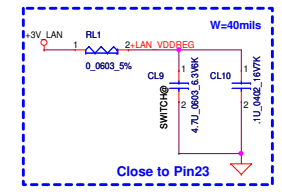
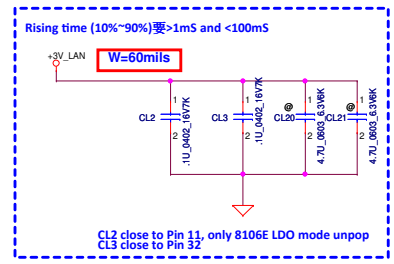
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title Docking
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				Document Number LA-B092P
				Rev 1.0
				Date: Tuesday, February 18, 2014 Sheet 36 of 53

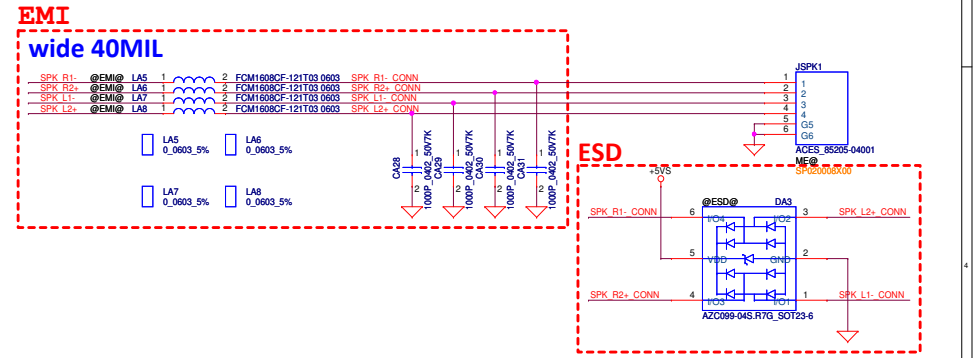
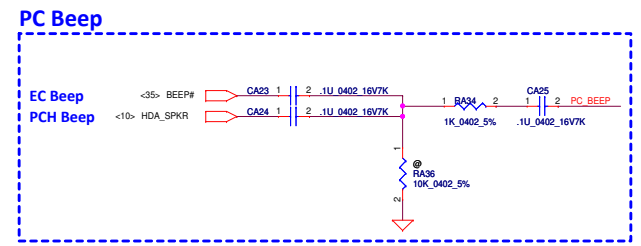
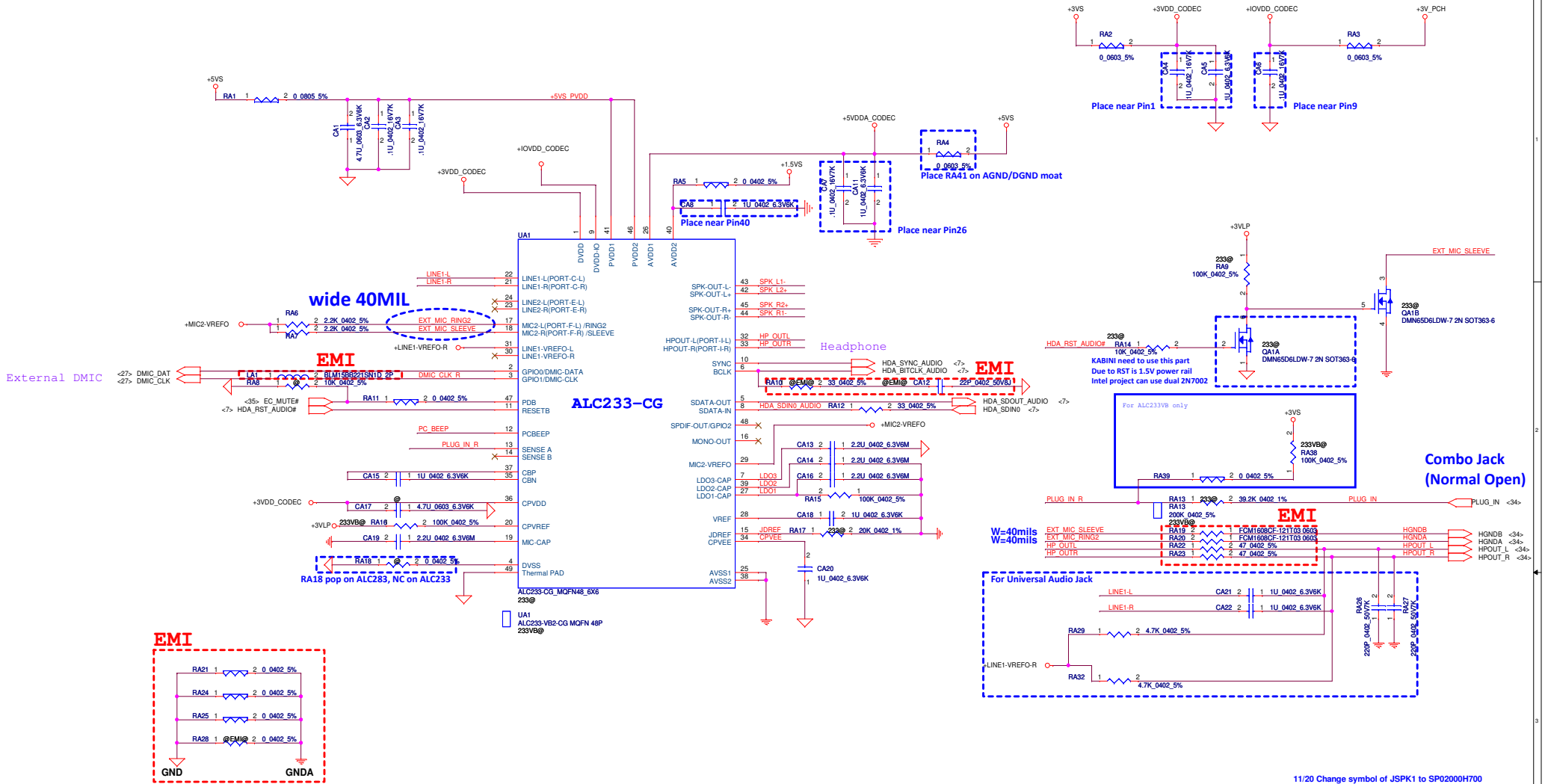




	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005Y700	RTL8111G	LDO	X	X	X	O
RTL8111G	External	X	X	X	X	O
SA000065Y00	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X
RTL8106E	LDO	X	X	X	X	X

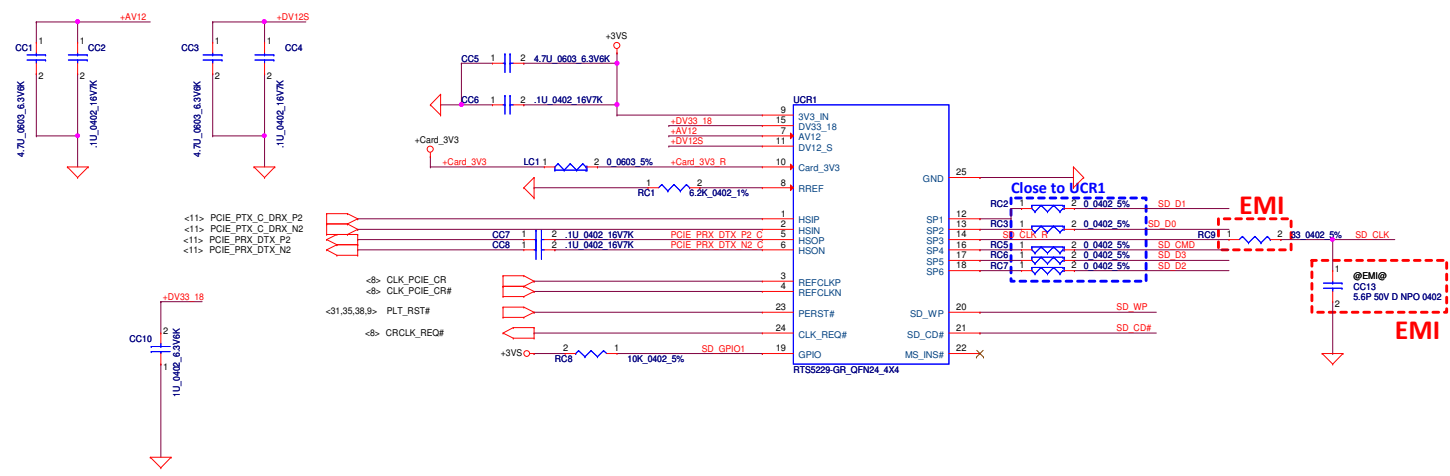
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.





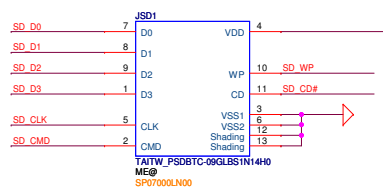
11/20 Change symbol of JSPK1 to SP2000H700

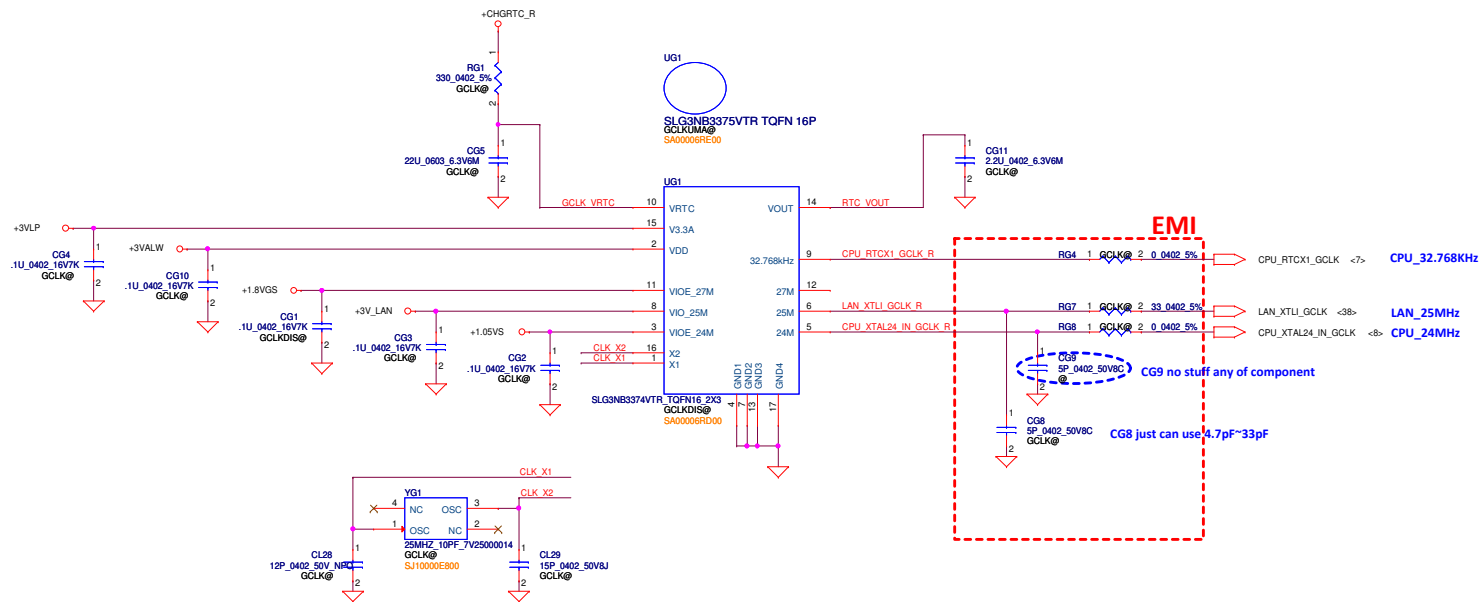
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title
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Size	LA-B092P	Document Number	LA-B092P	Rev
Date	Wednesday, February 18, 2014	Sheet	39 of 53	1.0



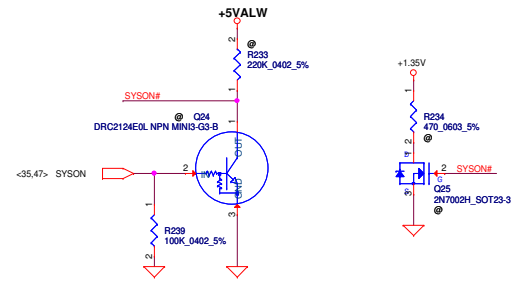
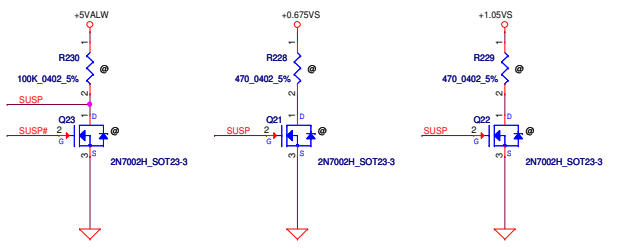
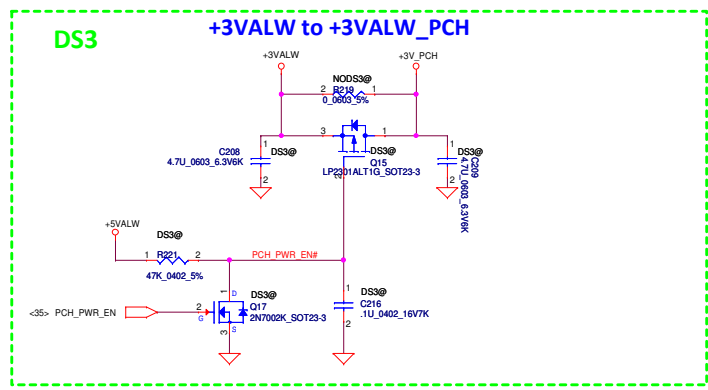
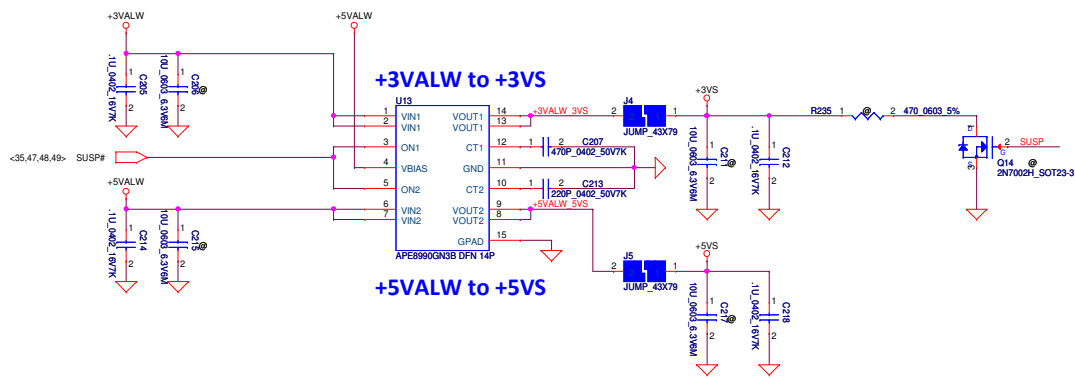
- <11> PCIE_PTX_C_DRX_P2
- <11> PCIE_PTX_C_DRX_N2
- <11> PCIE_PRX_DTX_P2
- <11> PCIE_PRX_DTX_N2

- <8> CLK_PCIE_CR
- <8> CLK_PCIE_CR#
- <31,35,38,9> PLT_RST#
- <8> CRCLK_REQ#

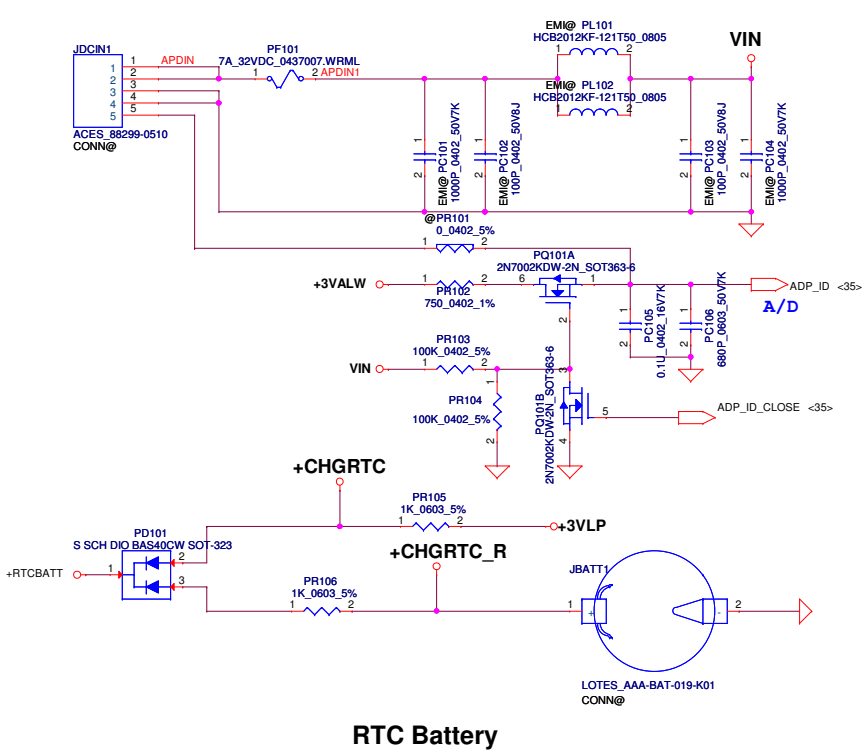




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				GCLK
				Size
				LA-B092P
				Date
				Tuesday, February 18, 2014
				Sheet
				41 of 53
				Rev
				1.0



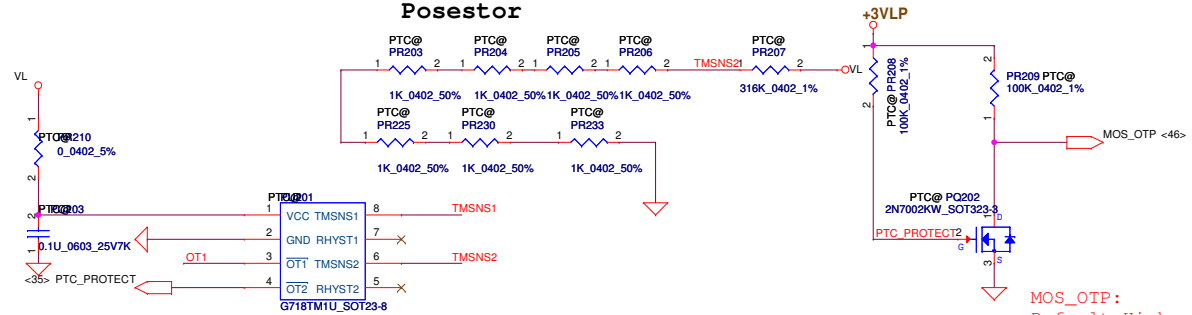
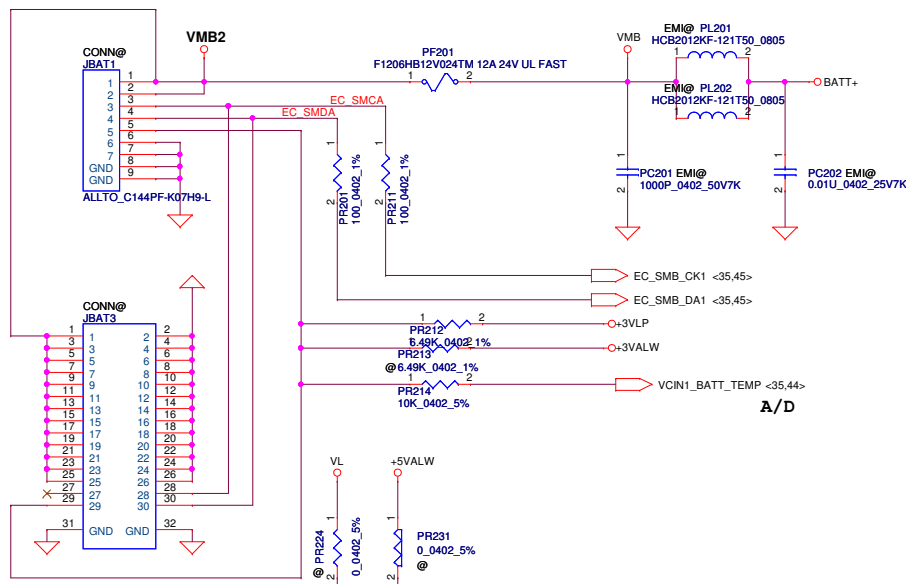
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title
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Size	C	Document Number	LA-B092P	Rev
Date:	Tuesday, February 18, 2014	Sheet	42 of 53	1.0



ADP_ID	AC Adapter	90W	65W
R(K ohm)	open	10	
ADP_ID(V)	3.3	1.65	
Detection voltage	>2.64	1.32~1.98	

RTC Battery

Security Classification	Compal Secret Data			Compal Electronics, Inc. PWR DCIN / RTC Battery		
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				Date: Tuesday, February 18, 2014	Sheet 43 of 53	

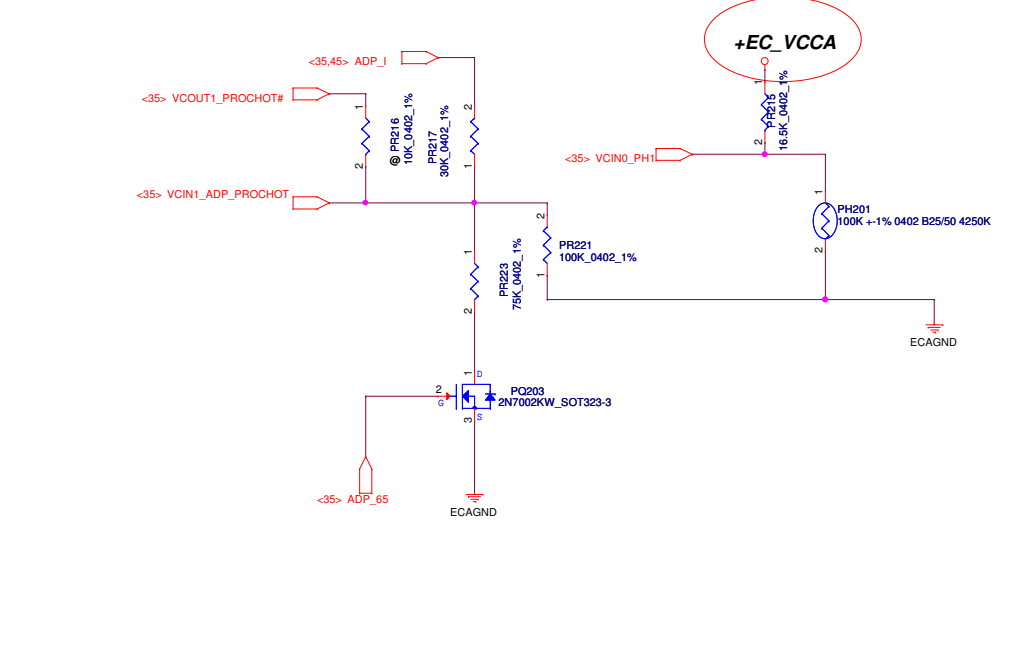
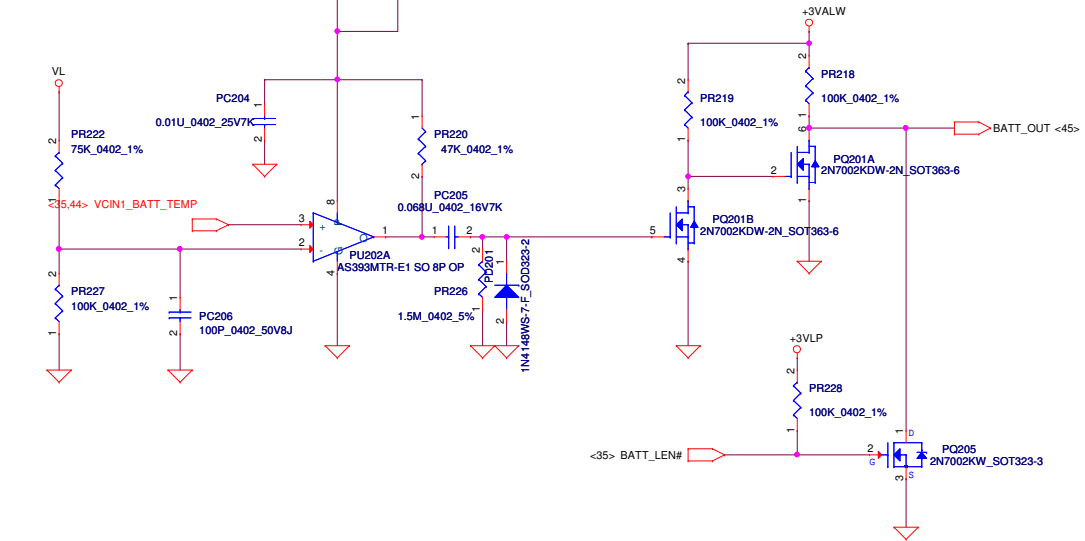


PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

20120314
 Change to +EC_VCCA from +3VLP

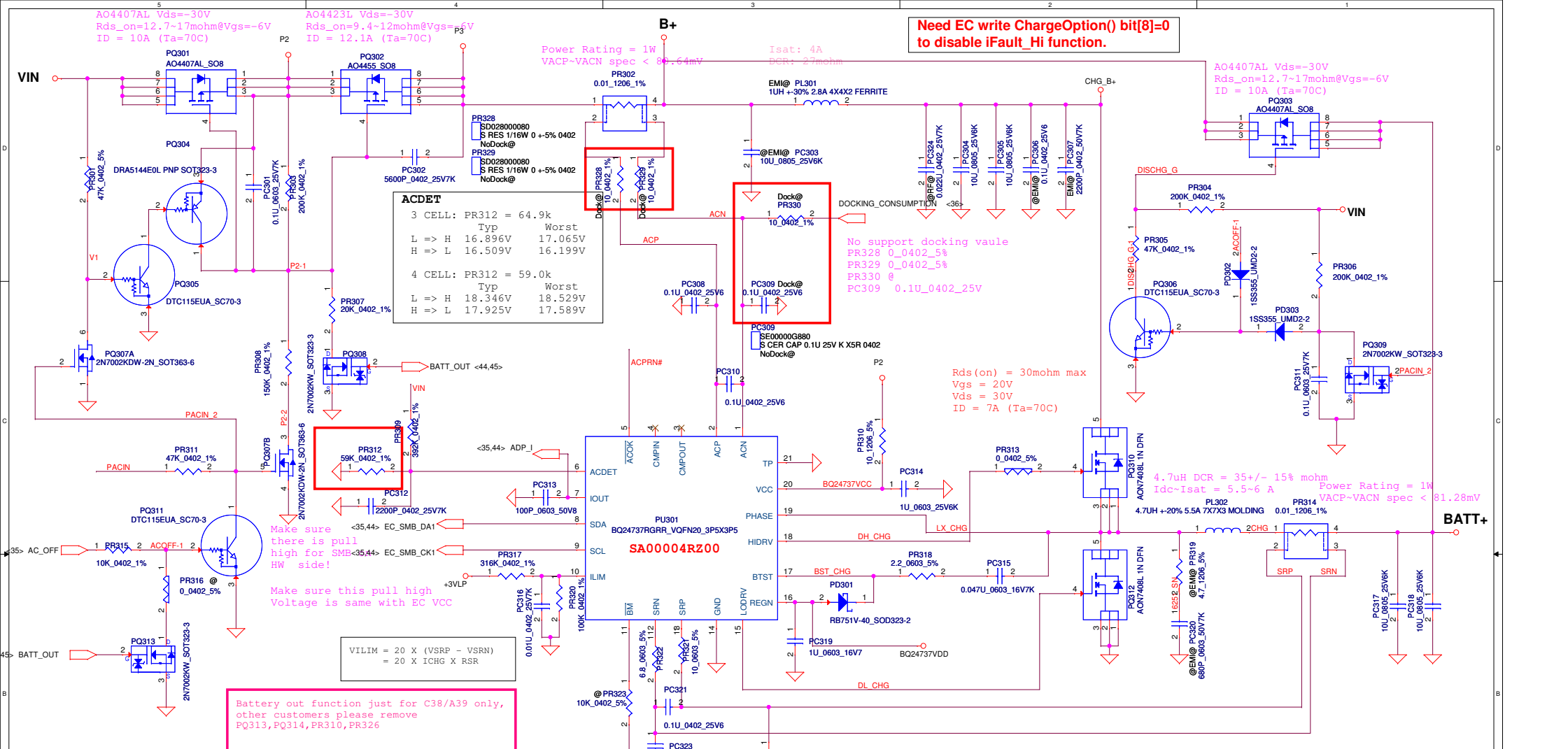
MOS_OTP:
 Default:High
 Active :Low

PTC_PROTECT:
 Default:Low
 Active :High



135W: 150W(Turbo_V=1.2) active 135W(Turbo_V=1.072) recovery
90W : 100W(Turbo_V=1.2) active 90W(Turbo_V=0.903) recovery
65W : 70W(Turbo_V=1.2) active 65W(Turbo_V=0.918) recovery
45W : 65W(Turbo_V=1.2) active 45W(Turbo_V=0.829) recovery

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				Document Number	Rev
				BE BDW	1.0
				Date: Tuesday, February 18, 2014	Sheet 44 of 53



****Design Notes****
 Maximum Charging current 2.0A
 Battery discharge power 55W.
 #Register Setting
 1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
 2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
 3. 0X12 bit[12:11] set 00 (default 11) to set BAT
 Depletion Comparator Threshold
 Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell)
 4. Disable turbo when AC only
 #Circuit Design
 1. Make sure there is pull high for SMB on HW side
 2. Use 10X10 choke and 3X3 H/L side MOSFET
 Charge current 2.0A
 Power loss : 1.82W
 Power density : 0.81 (15X15)
 3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)
 4. For hybrid design, need double check PQ301,PQ302,PQ303,PQ309 component rating
 #Protect function
 1. AC0VP : ACDET voltage > 3.15V
 2. Charger timeout : No communication within 175s(default)
 3. ACOC : 3.33 X Input current DAC setting(default)
 4. CHGOCP : 3/4.5/6A based on current setting
 5. BATOVP : 104%
 6. BATLOWV : 2.5V
 7. TSHUT : 155C
 8. IFAULT HI : 750mV (default)
 9. IFAULT LOW : 135mV (default)

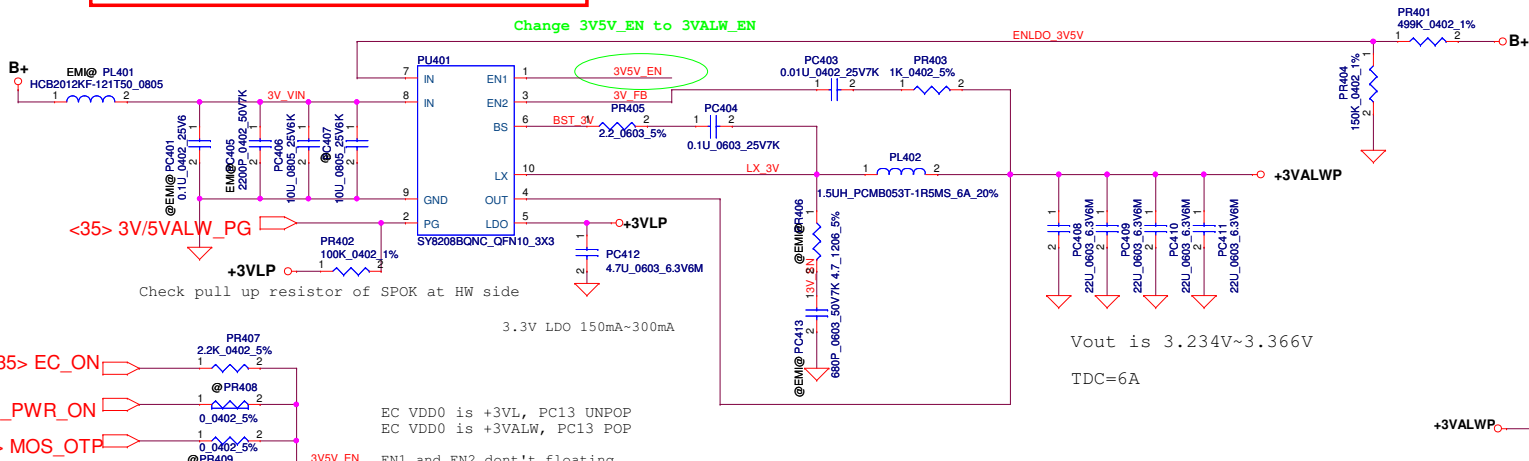
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Charger BQ24737	
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				BE_BDW	
				Date:	Tuesday, February 18, 2014
				Sheet	45 of 53

Module model information
SY8208E_V2.mdd

EN1 and EN2 don't floating

Change 3V5V_EN to 3VALW_EN

ENLDO_3V5V



<35> 3V/5VALW_PG

Check pull up resistor of SPOK at HW side

3.3V LDO 150mA~300mA

Vout is 3.234V~3.366V

TDC=6A

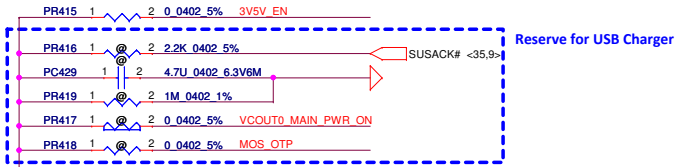
<35> EC_ON

<35> VCOUT0_MAIN_PWR_ON

<44> MOS_OTP

EC VDD0 is +3VL, PC13 UNPOP
EC VDD0 is +3VALW, PC13 POP

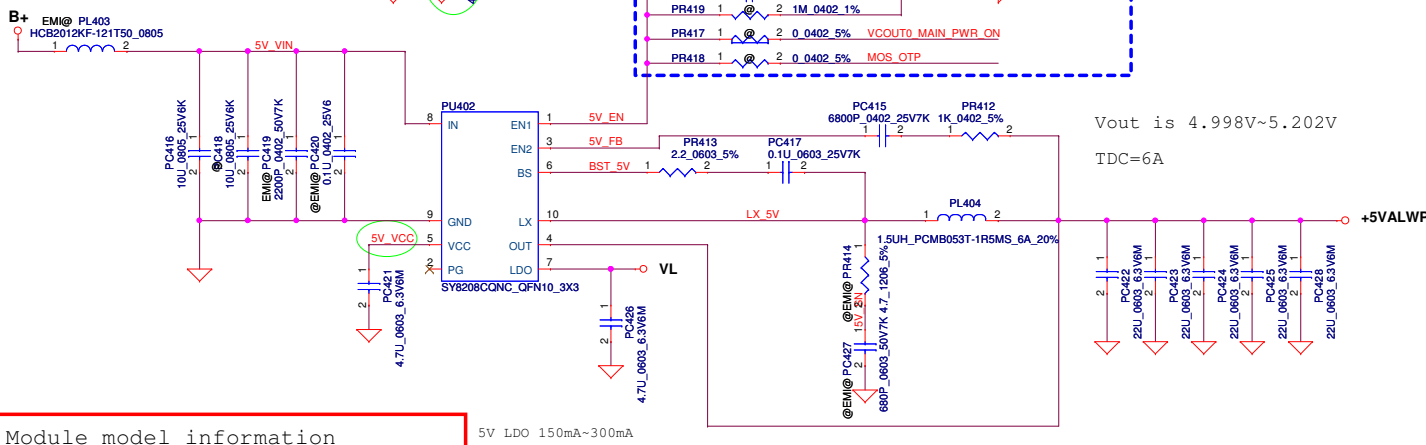
EN1 and EN2 don't floating



Reserve for USB Charger

Vout is 4.998V~5.202V

TDC=6A



5V LDO 150mA~300mA



Module model information
SY8208C_V2.mdd

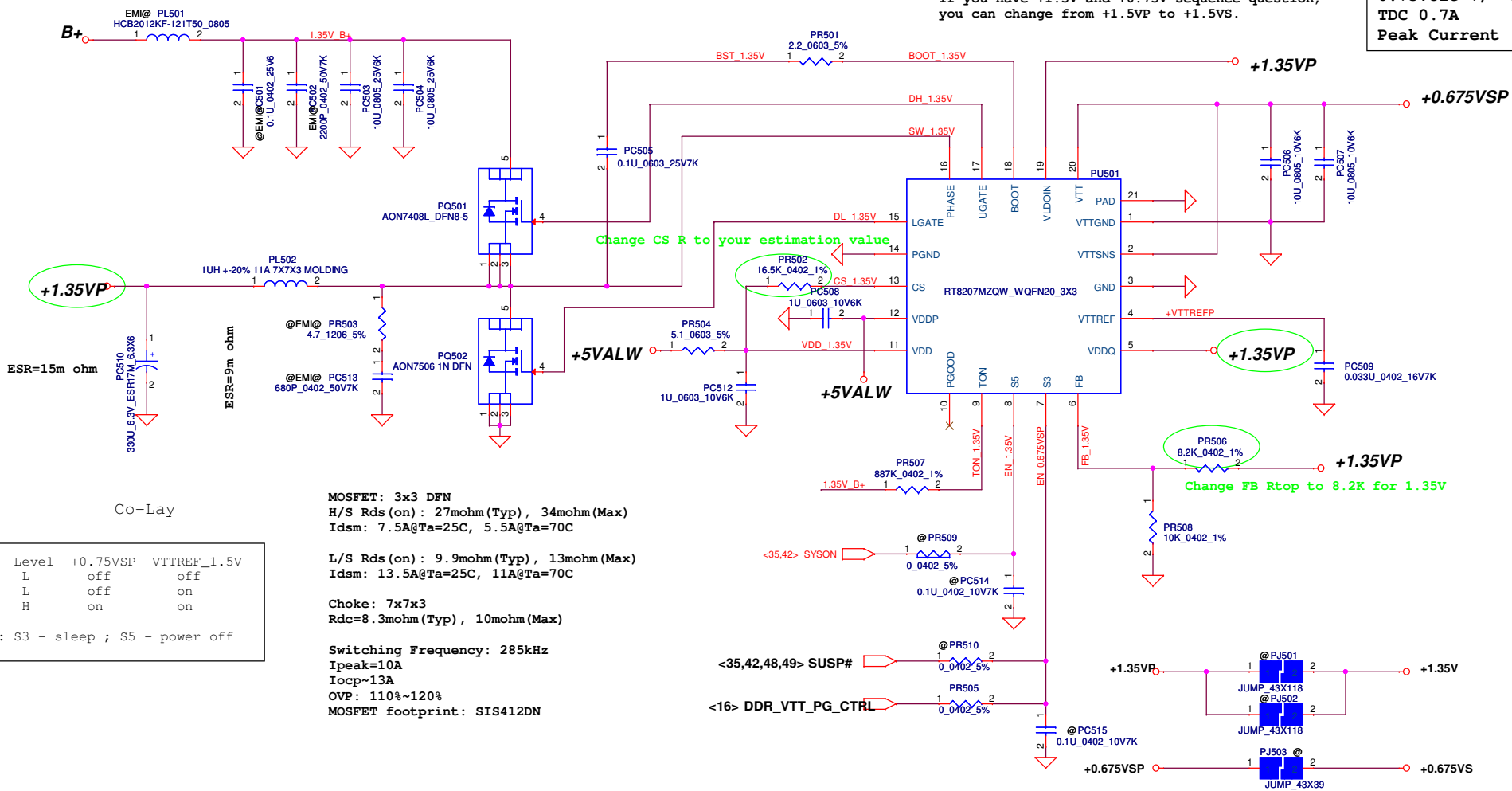
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				BE BDW
				Rev 1.0
				Date: Tuesday, February 18, 2014 Sheet 46 of 53

Module model information

RT8207M_v1.mdd For Single layer
RT8207M_v2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Co-Lay

Mode	Level	+0.75VSP	VITREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds (on) : 27mohm (Typ) , 34mohm (Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on) : 9.9mohm (Typ) , 13mohm (Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

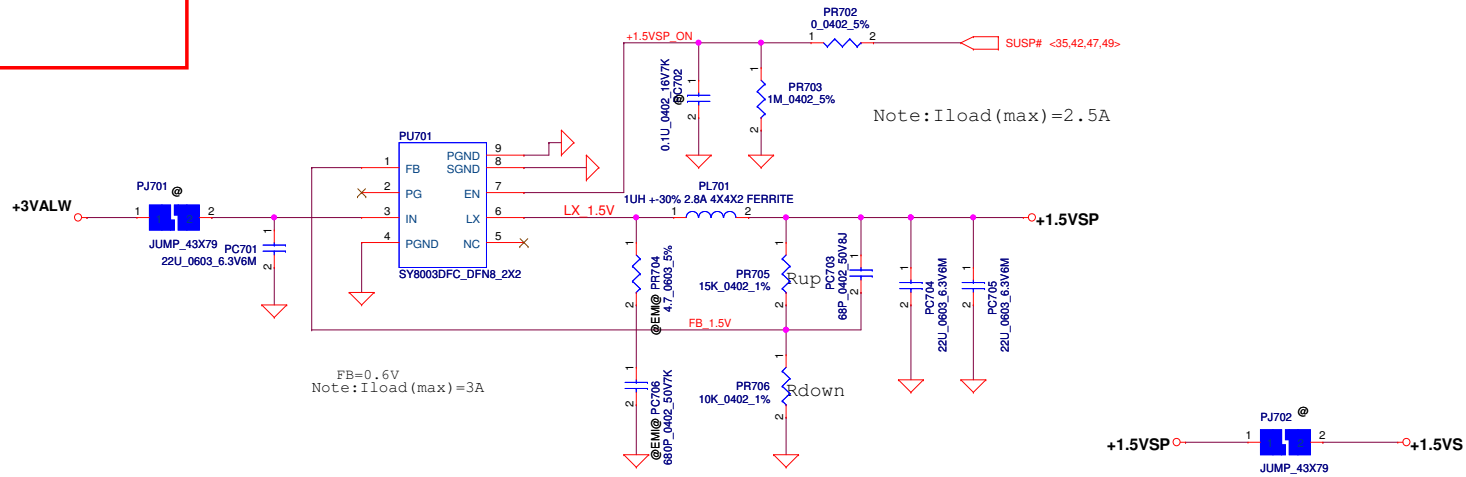
Choke: 7x7x3
Rdc=8.3mohm (Typ) , 10mohm (Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

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Size	Document Number			Rev	1.0
Custom	BE BDW				
Date:	Tuesday, February 18, 2014	Sheet	47	of	53

Module model information

SY8003_V1.mdd



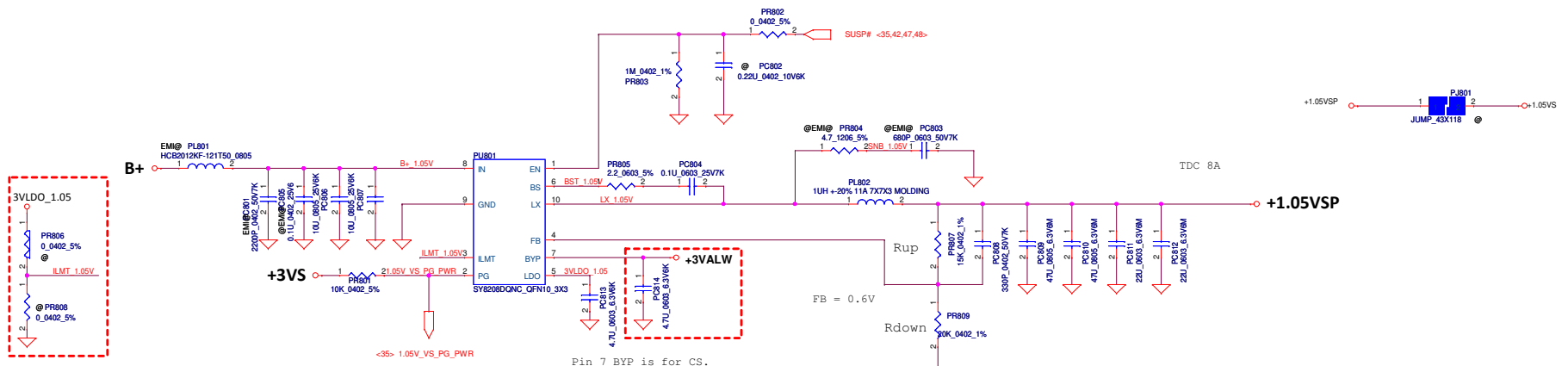
Note:
When design $V_{in}=5V$, please stuff snubber
to prevent V_{in} damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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				Size	Document Number	Rev
				Custom	BE_BDW	1.0
Date: Tuesday, February 18, 2014				Sheet	48	of 53

Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

$V_{FB} = 0.6V$
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$
 $V_{out} = 1.05V$

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Rev	1.0			

Module model information:
ISL95813 (for 15W & 28W CPU)

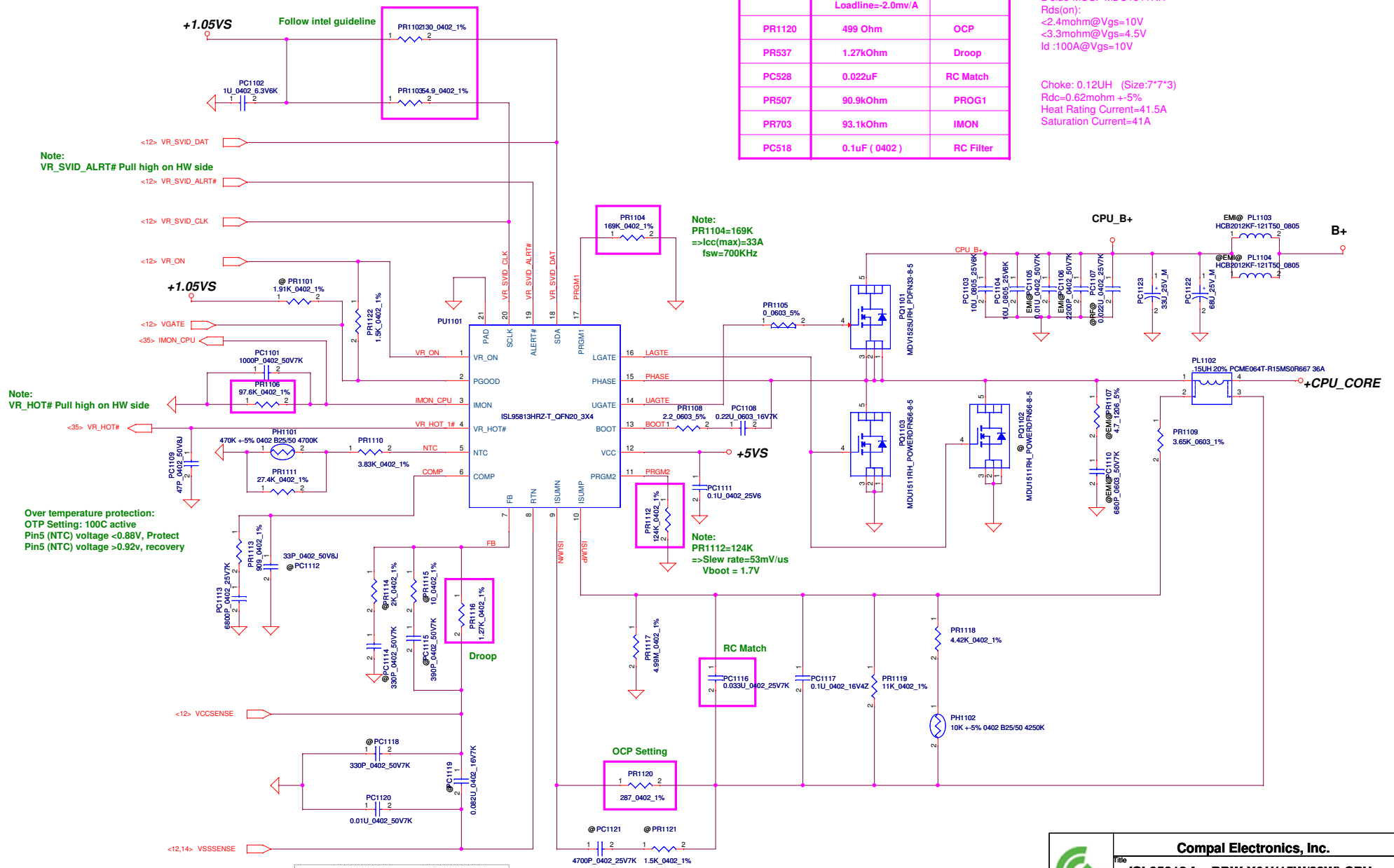
Base on BDW_PDDG Rev_0_73

Location	15W	Note
	TDC	
	MAX 32A	
	OCF 39A	
	Loadline=-2.0mv/A	
PR1120	499 Ohm	OCF
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12uH (Size:7*7*3)
Fdc=0.62mohm +5%
Heat Rating Current=41.5A
Saturation Current=41A



Note:
VR_SVID_ALRT# Pull high on HW side

Note:
VR_HOT# Pull high on HW side

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

Note:
PR1104=169K
=>Icc(max)=33A
fsw=700KHz

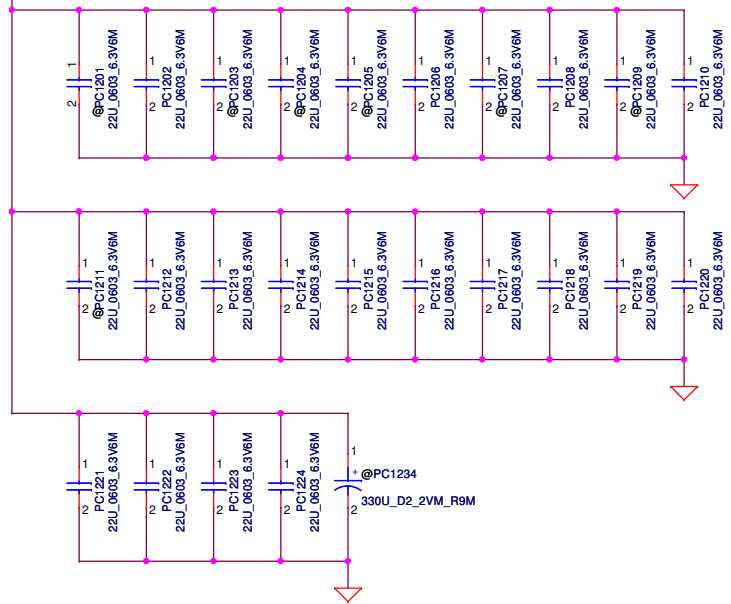
Note:
PR1112=124K
=>Slew rate=53mV/us
Vboot = 1.7V

Local sense put on HW site

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	File	ISL95813 for BDW-Y&U(15W/28W) CPU	
Size	Document Number	BE BDW	Rev 1.0
Date:	Tuesday, February 18, 2014	Sheet 50 of 53	

+CPU_CORE

24 X 22u/0603



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Size	Custom	Document Number	BE BDW		Rev 1.0
Date:	Tuesday, February 18, 2014		Sheet	51	of 53

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Size	Custom	Document Number	BE BDW	Rev	1.0
Date:	Tuesday, February 18, 2014	Sheet	52	of	53

ZIWB2/ZIWB3/ZIWE1 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	
1	P. 36	Modify DP_SEL schematic	Because the first design is wrong.	EVT TO DVT
2	P. 34	Delete D28	It already reserve in sub BD	
3	P. 36	Modify HPD schematic	Because the first design is wrong.	
4	P. 36	Modify DP AUX schematic	Cap already reserve in sub BD	
5	P. 20	Reserve +1.05VS to +0.95VGS	AMD' s suggestion	
6	P. 33	Add D26 for ESD		
7	P. 42	Add RV198, RV199	AMD' s suggestion	DVT TO PVT
1	P. 35	change U11.111 power rail to +3VLP	It only use +3VLP	
2	P. 33	un-pop R294, pop R295.	B series' s LED need to follow E series	
3	P. 10	Add R247, R248	For BIOS Stap Pin	
4	P. 37	Change DP Switch IC solution	For HDMI audio issue	
5	P. 35	Add C197 for ESD		
6	P. 33	Add C198 for ESD		
7	P. 30	Add C199 for ESD		
1	P. 33	Reserve R298, R299 for DC-in LED control	To avoid LED shimmer	PVT TO PRE-MP
2	P. 38	Change DL1 and DL2 footprint for ESD		

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				LA-B092P	1.0
Date: Tuesday, February 18, 2014				Sheet	53 of 53

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