

# Compal Confidential

## DAT20 Schematics Document

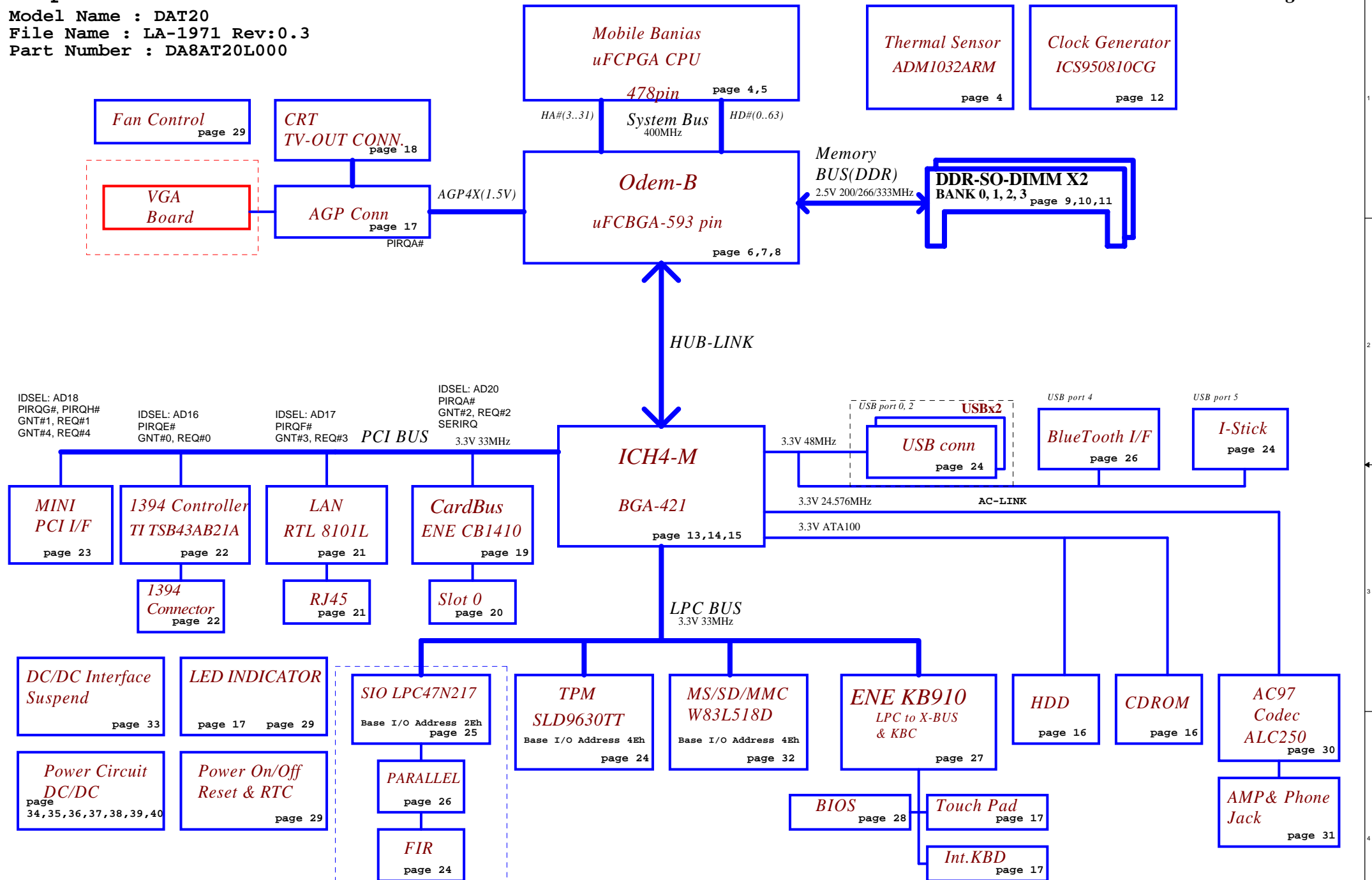
### Banias uFCPGA Package with 855PM(Odem) + ICH4-M

2003-09-25

REV: 0.3

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Title	Block Diagram	
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## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for MCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18,AD22	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000Xb		

## EC SM Bus2 address

## ICH4-M SM Bus address

Device	Address
Clock Generator (ICS950810CG)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 001Xb

## Board ID Table for AD channel

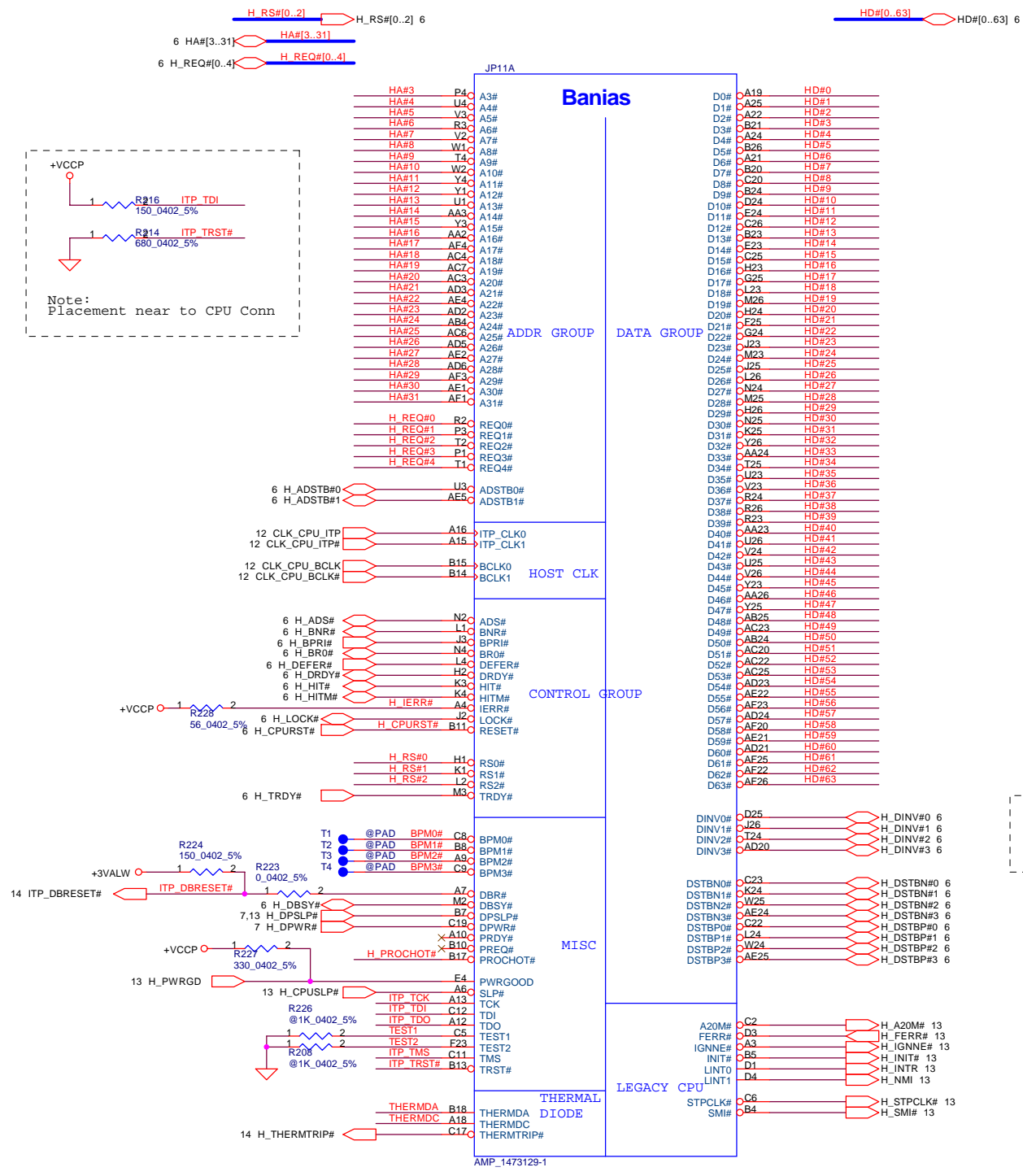
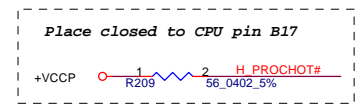
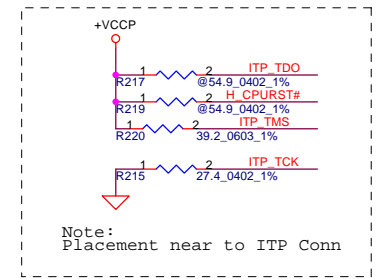
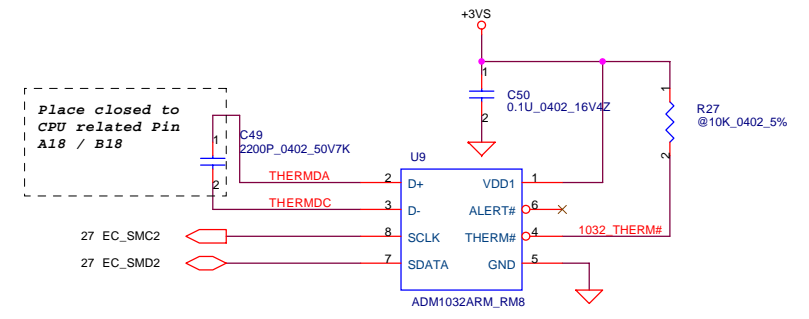
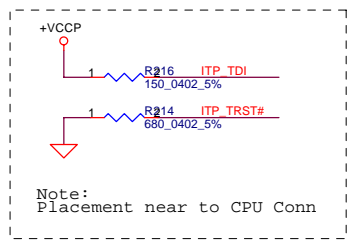
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

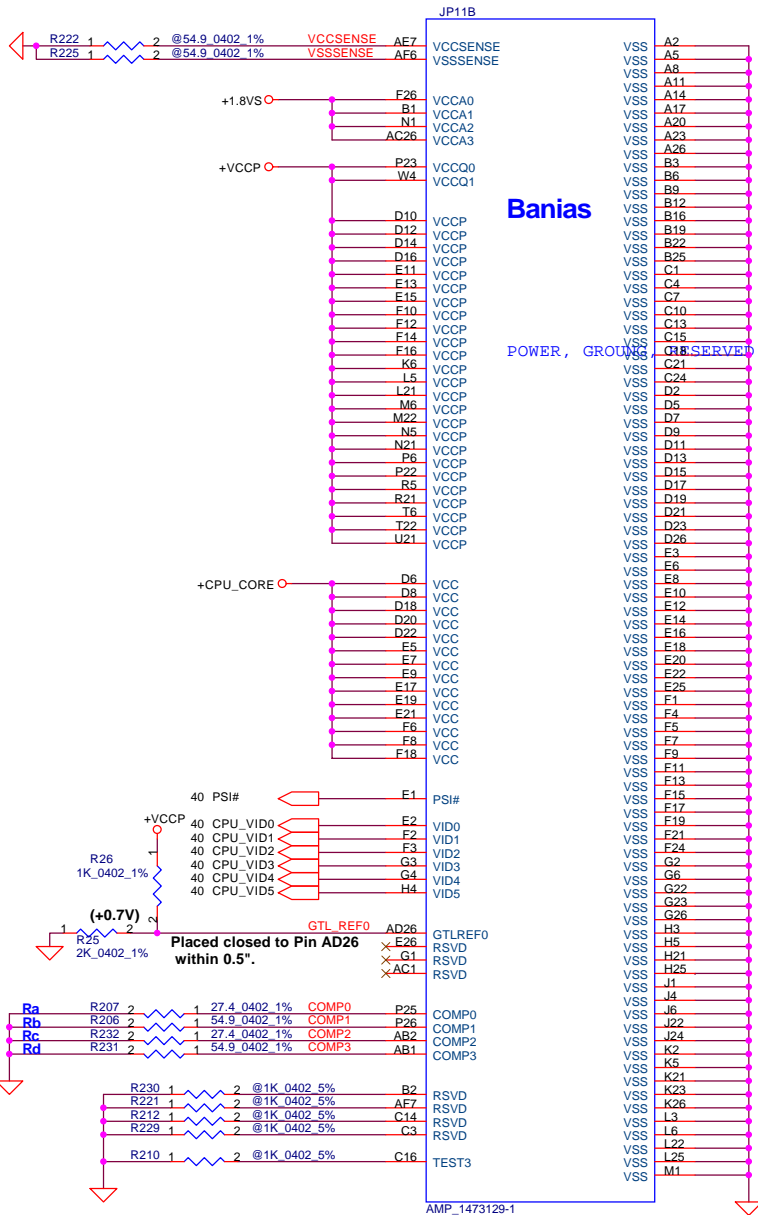
Board ID	PCB Revision
0	0.1
* 1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

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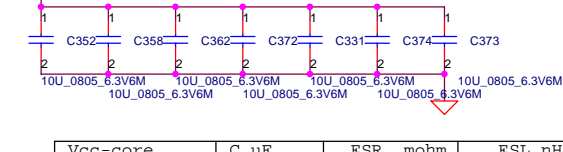
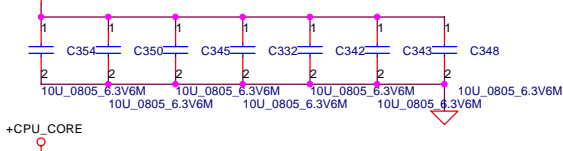
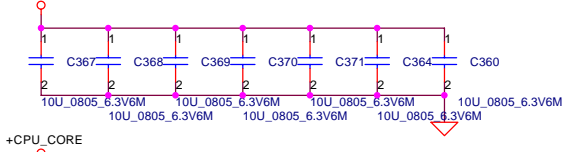
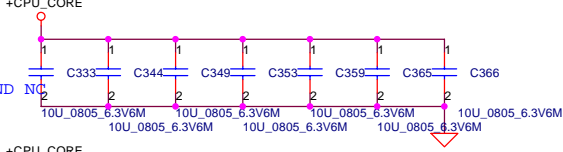
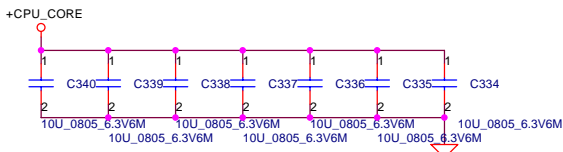
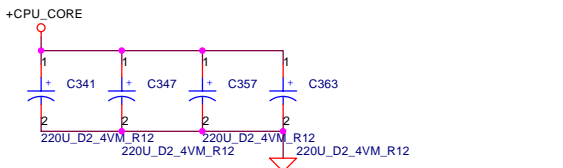




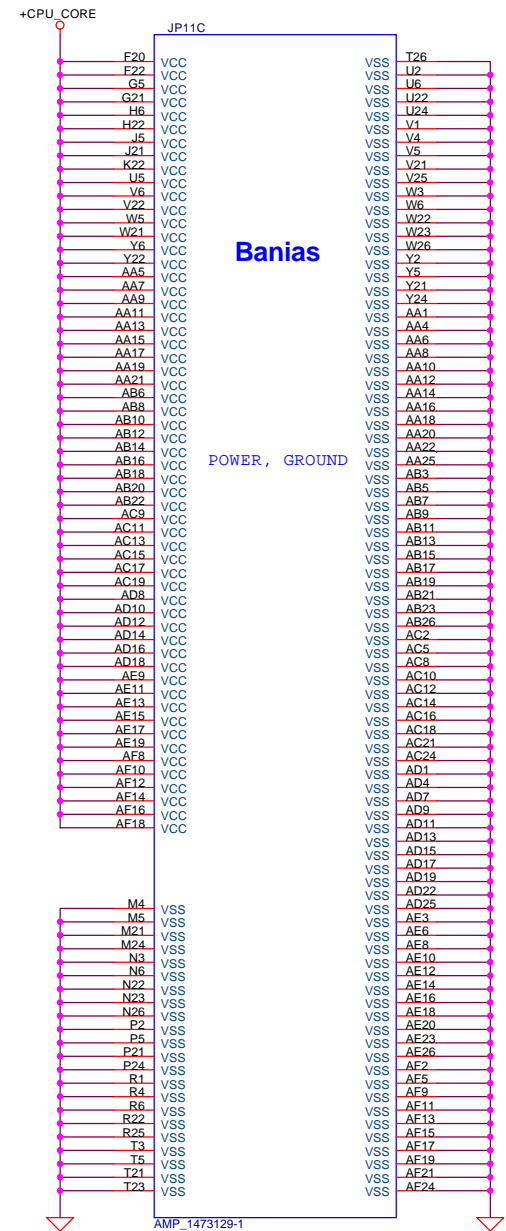
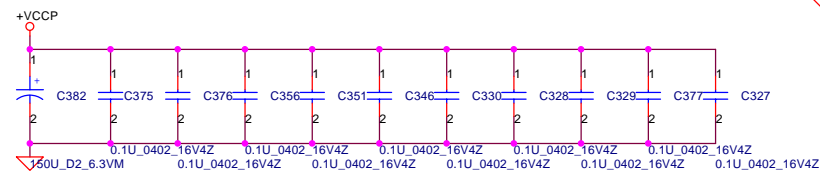
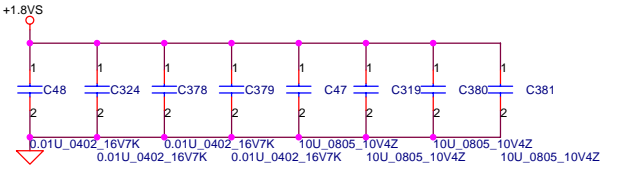
Ra, Rb, Rc, Rd placed close to related pin within 0.5".  
 COMP0/1/2/3 Trace should 25mil away from any other toggling signal.

Banias

POWER, GROUND OBSERVED SIGNALS AND NC



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



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POWER, GROUND



DDR\_SMA[0..12] ↔ DDR\_SMA[0..12] 9  
 9 DDR\_SDQ[0..63] ↔ DDR\_SDQ[0..63]  
 9 DDR\_SDQS[0..8] ↔ DDR\_SDQS[0..8]  
 9 DDR\_CB[0..7] ↔ DDR\_CB[0..7]

U8C

Odem

MEMORY

DDR SMA0 E12 SMA0  
 DDR SMA1 E17 SMA1  
 DDR SMA2 E16 SMA2  
 DDR SMA3 G17 SMA3  
 DDR SMA4 G18 SMA4  
 DDR SMA5 E18 SMA5  
 DDR SMA6 F19 SMA6  
 DDR SMA7 G20 SMA7  
 DDR SMA8 G19 SMA8  
 DDR SMA9 F21 SMA9  
 DDR SMA10 E13 SMA10  
 DDR SMA11 E20 SMA11  
 DDR SMA12 G21 SMA12  
 ×G22 RSV22

DDR SDQS0 F26 SDQS0  
 DDR SDQS1 C26 SDQS1  
 DDR SDQS2 C23 SDQS2  
 DDR SDQS3 B19 SDQS3  
 DDR SDQS4 D12 SDQS4  
 DDR SDQS5 C18 SDQS5  
 DDR SDQS6 C5 SDQS6  
 DDR SDQS7 E3 SDQS7  
 DDR SDQS8 E15 SDQS8

9 DDR\_SWE# ↔ G11 SWE#  
 9 DDR\_SRAS# ↔ F11 SRAS#  
 9 DDR\_SCAS# ↔ G8 SCAS#

9 DDR\_CLK0 ↔ J25 SCK0  
 9 DDR\_CLK0# ↔ K23 SCK#0  
 9 DDR\_CLK1 ↔ G5 SCK1  
 9 DDR\_CLK1# ↔ F5 SCK#1  
 9 DDR\_CLK2 ↔ G24 SCK2  
 9 DDR\_CLK2# ↔ E24 SCK#2  
 10 DDR\_CLK3 ↔ G25 SCK3  
 10 DDR\_CLK3# ↔ J24 SCK#3  
 10 DDR\_CLK4 ↔ G6 SCK4  
 10 DDR\_CLK4# ↔ G7 SCK#4  
 10 DDR\_CLK5 ↔ K23 SCK5  
 10 DDR\_CLK5# ↔ J23 SCK#5

9,10 DDR\_CKE0 ↔ G23 SCKE0  
 9,10 DDR\_CKE1 ↔ E22 SCKE1  
 10 DDR\_CKE2 ↔ H23 SCKE2  
 10 DDR\_CKE3 ↔ F23 SCKE3

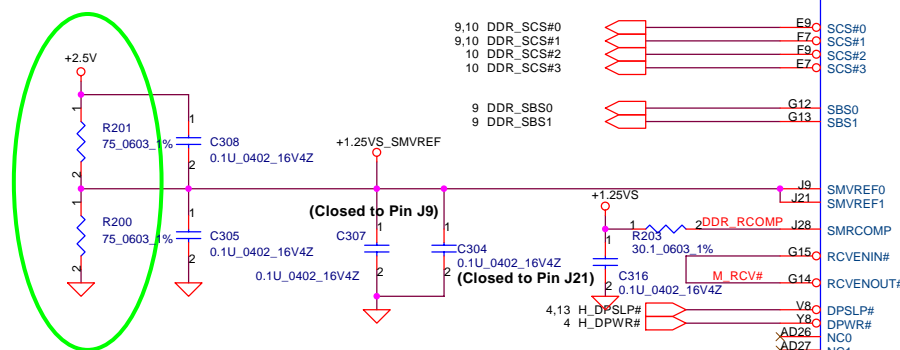
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 9,10 DDR\_SCS#1 ↔ F7 SCS#1  
 10 DDR\_SCS#2 ↔ F9 SCS#2  
 10 DDR\_SCS#3 ↔ E7 SCS#3

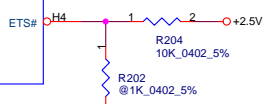
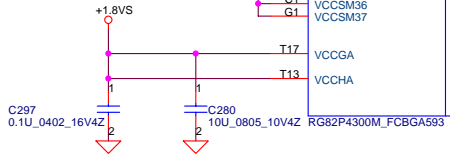
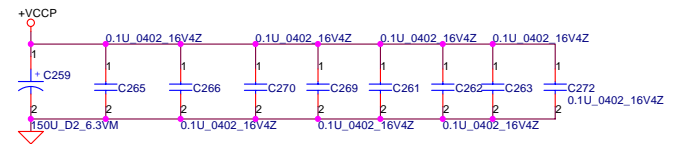
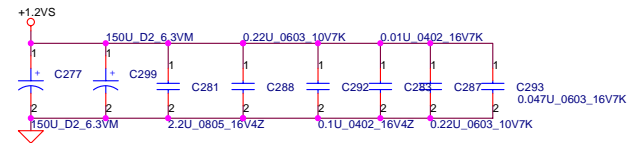
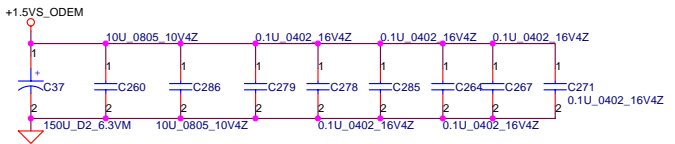
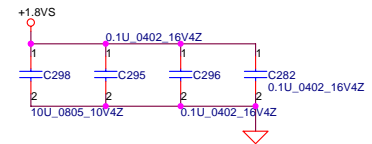
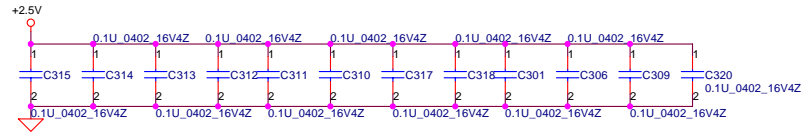
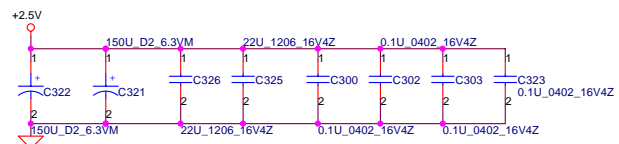
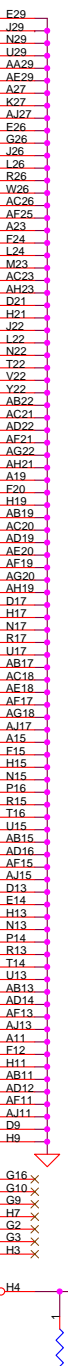
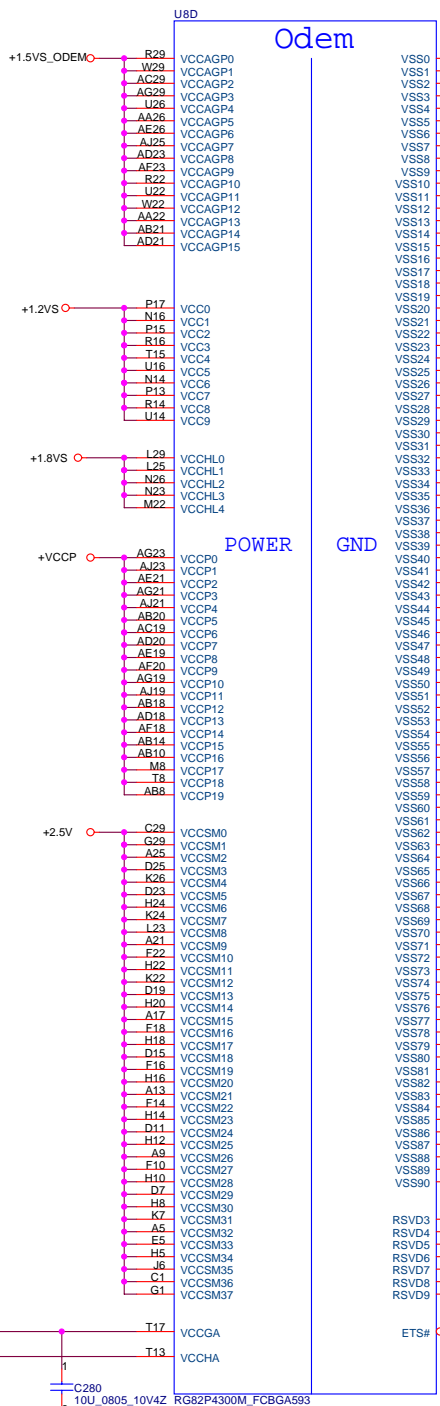
9 DDR\_SBS0 ↔ G12 SBS0  
 9 DDR\_SBS1 ↔ G13 SBS1

SDQ0 G28 DDR\_SDO0  
 SDQ1 E27 DDR\_SDO1  
 SDQ2 C28 DDR\_SDO2  
 SDQ3 E28 DDR\_SDO3  
 SDQ4 H25 DDR\_SDO4  
 SDQ5 G27 DDR\_SDO5  
 SDQ6 F25 DDR\_SDO6  
 SDQ7 B28 DDR\_SDO7  
 SDQ8 E27 DDR\_SDO8  
 SDQ9 C27 DDR\_SDO9  
 SDQ10 B25 DDR\_SDO10  
 SDQ11 C25 DDR\_SDO11  
 SDQ12 B27 DDR\_SDO12  
 SDQ13 D26 DDR\_SDO13  
 SDQ14 E25 DDR\_SDO14  
 SDQ15 D24 DDR\_SDO15  
 SDQ16 E23 DDR\_SDO16  
 SDQ17 C22 DDR\_SDO17  
 SDQ18 E21 DDR\_SDO18  
 SDQ19 C24 DDR\_SDO19  
 SDQ20 B23 DDR\_SDO20  
 SDQ21 D22 DDR\_SDO21  
 SDQ22 B21 DDR\_SDO22  
 SDQ23 C21 DDR\_SDO23  
 SDQ24 D20 DDR\_SDO24  
 SDQ25 C19 DDR\_SDO25  
 SDQ26 D18 DDR\_SDO26  
 SDQ27 C20 DDR\_SDO27  
 SDQ28 E19 DDR\_SDO28  
 SDQ29 C18 DDR\_SDO29  
 SDQ30 E17 DDR\_SDO30  
 SDQ31 E13 DDR\_SDO31  
 SDQ32 C14 DDR\_SDO32  
 SDQ33 B11 DDR\_SDO33  
 SDQ34 C10 DDR\_SDO34  
 SDQ35 B13 DDR\_SDO35  
 SDQ36 C13 DDR\_SDO36  
 SDQ37 C11 DDR\_SDO37  
 SDQ38 D10 DDR\_SDO38  
 SDQ39 E10 DDR\_SDO39  
 SDQ40 C9 DDR\_SDO40  
 SDQ41 D8 DDR\_SDO41  
 SDQ42 E8 DDR\_SDO42  
 SDQ43 E11 DDR\_SDO43  
 SDQ44 B9 DDR\_SDO44  
 SDQ45 B7 DDR\_SDO45  
 SDQ46 C7 DDR\_SDO46  
 SDQ47 C6 DDR\_SDO47  
 SDQ48 D6 DDR\_SDO48  
 SDQ49 D4 DDR\_SDO49  
 SDQ50 B3 DDR\_SDO50  
 SDQ51 E6 DDR\_SDO51  
 SDQ52 B5 DDR\_SDO52  
 SDQ53 C4 DDR\_SDO53  
 SDQ54 E4 DDR\_SDO54  
 SDQ55 C3 DDR\_SDO55  
 SDQ56 D3 DDR\_SDO56  
 SDQ57 F3 DDR\_SDO57  
 SDQ58 F9 DDR\_SDO58  
 SDQ59 B2 DDR\_SDO59  
 SDQ60 C2 DDR\_SDO60  
 SDQ61 E2 DDR\_SDO61  
 SDQ62 G4 DDR\_SDO62  
 SDQ63 C16 DDR\_CB0  
 SDQ64 D16 DDR\_CB1  
 SDQ65 B15 DDR\_CB2  
 SDQ66 C14 DDR\_CB3  
 SDQ67 B17 DDR\_CB4  
 SDQ68 C17 DDR\_CB5  
 SDQ69 C15 DDR\_CB6  
 SDQ70 D14 DDR\_CB7  
 SDQ71

RSTIN# J27 ↔ PCIRST# 13,19,20,21,23,24,25  
 RSV1# H27  
 TESTIN# H26 MCH\_TEST#1  
 R205 @4.7K\_0402\_5% +1.5VS

RG82P4300M\_FCBGA593



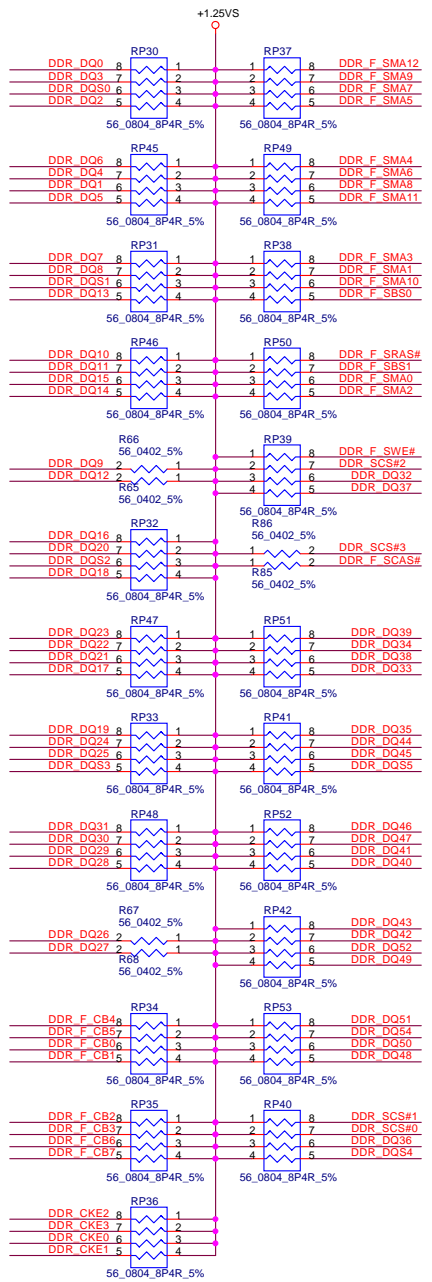


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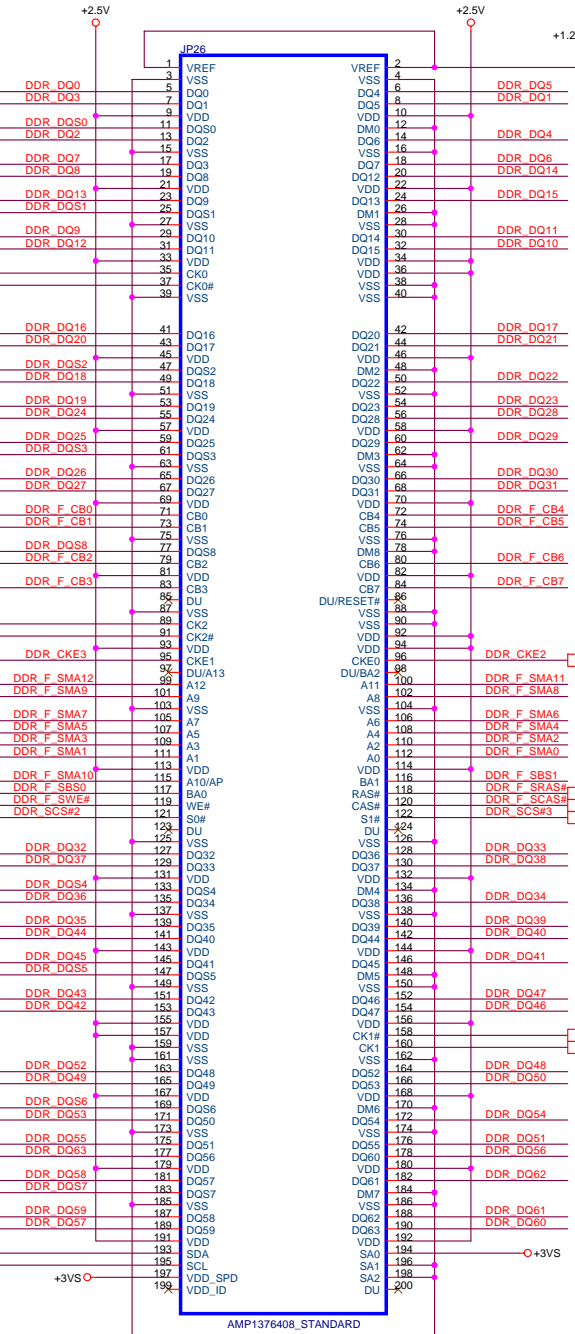
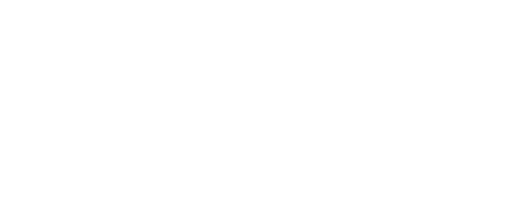
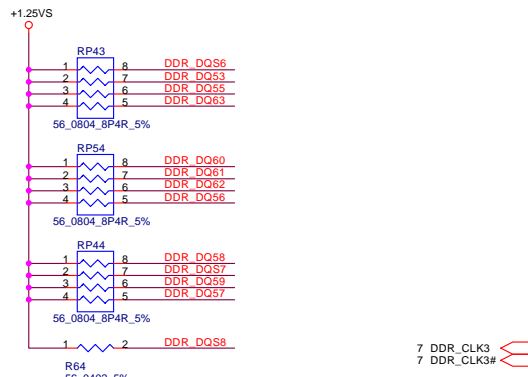
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- DDR F SB50 → DDR\_F\_SB50 9
- DDR F SB51 → DDR\_F\_SB51 9
- DDR SCS#0 → DDR\_SCS#0 7,9
- DDR SCS#1 → DDR\_SCS#1 7,9
- DDR\_CKE0 → DDR\_CKE0 7,9
- DDR\_CKE1 → DDR\_CKE1 7,9



- DDR F SMA[0..12] → DDR\_F\_SMA[0..12] 9
- DDR\_DQ[0..63] → DDR\_DQ[0..63] 9
- DDR\_DQS[0..8] → DDR\_DQS[0..8] 9
- DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

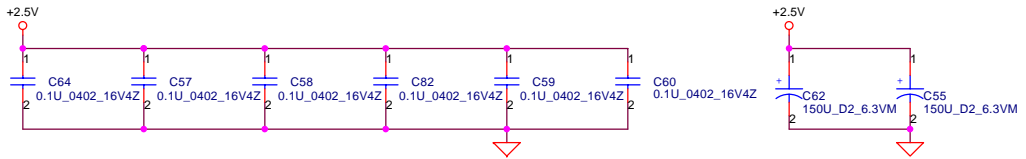
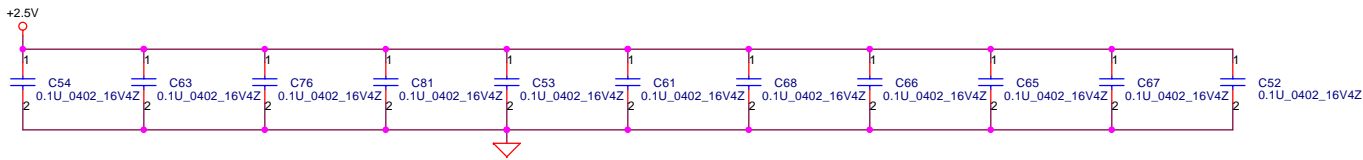
- DDR\_CKE4 → DDR\_CKE4 7
- DDR\_CKE5 → DDR\_CKE5 7
- DDR\_CKE6 → DDR\_CKE6 7
- DDR\_CKE7 → DDR\_CKE7 7
- DDR\_CKE8 → DDR\_CKE8 7
- DDR\_CKE9 → DDR\_CKE9 7
- DDR\_CKE10 → DDR\_CKE10 7
- DDR\_CKE11 → DDR\_CKE11 7
- DDR\_CKE12 → DDR\_CKE12 7
- DDR\_CKE13 → DDR\_CKE13 7
- DDR\_CKE14 → DDR\_CKE14 7
- DDR\_CKE15 → DDR\_CKE15 7
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- DDR\_CKE95 → DDR\_CKE95 7
- DDR\_CKE96 → DDR\_CKE96 7
- DDR\_CKE97 → DDR\_CKE97 7
- DDR\_CKE98 → DDR\_CKE98 7
- DDR\_CKE99 → DDR\_CKE99 7
- DDR\_CKE100 → DDR\_CKE100 7

**DIMM1**

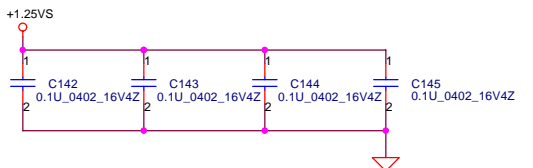
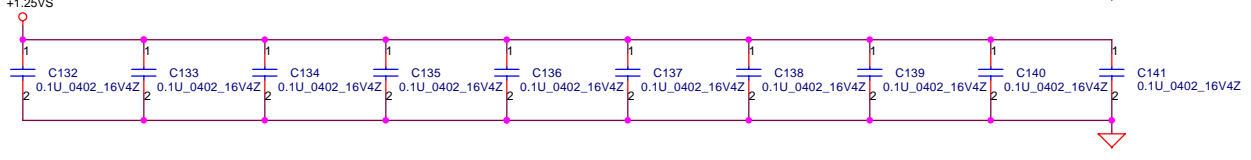
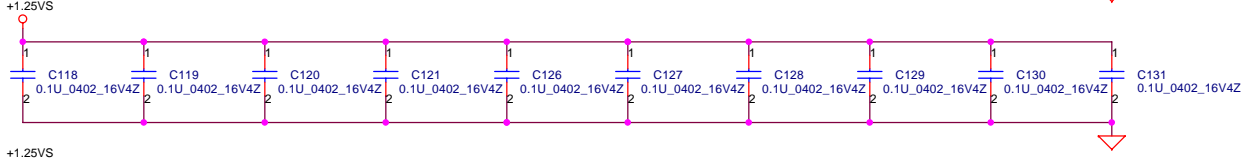
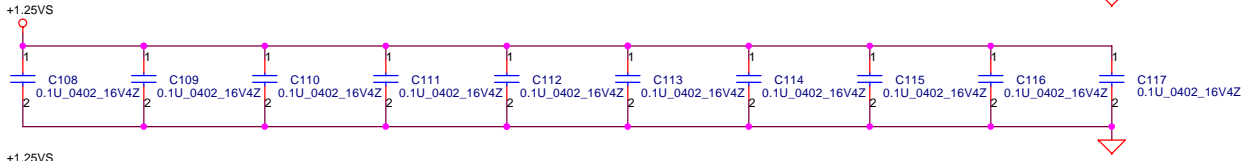
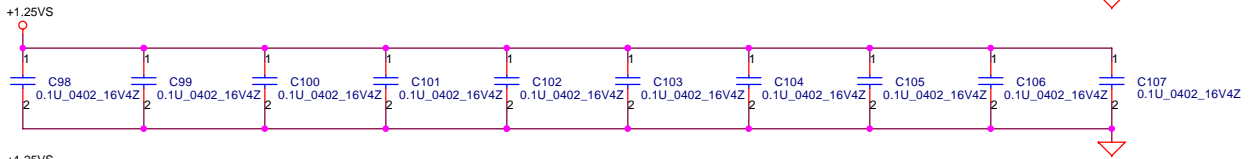
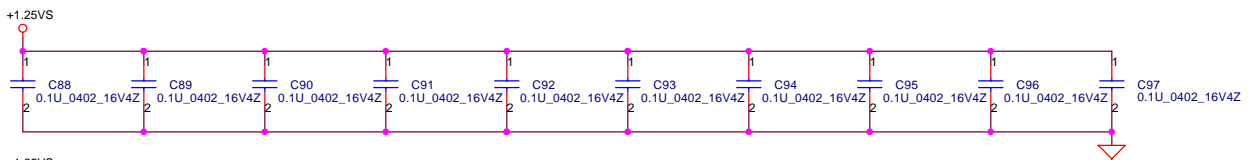
<b>Compal Electronics, Inc.</b>			
<b>DDR-SODIMM SLOT1</b>			
Title			
Size	Document Number	Rev	
Custom	<b>DAT20 LA-1971</b>	0.3	
Date:	Friday, September 26, 2003	Sheet	10 of 42

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**Layout note :**  
Distribute as close as possible to DDR-SODIMM.



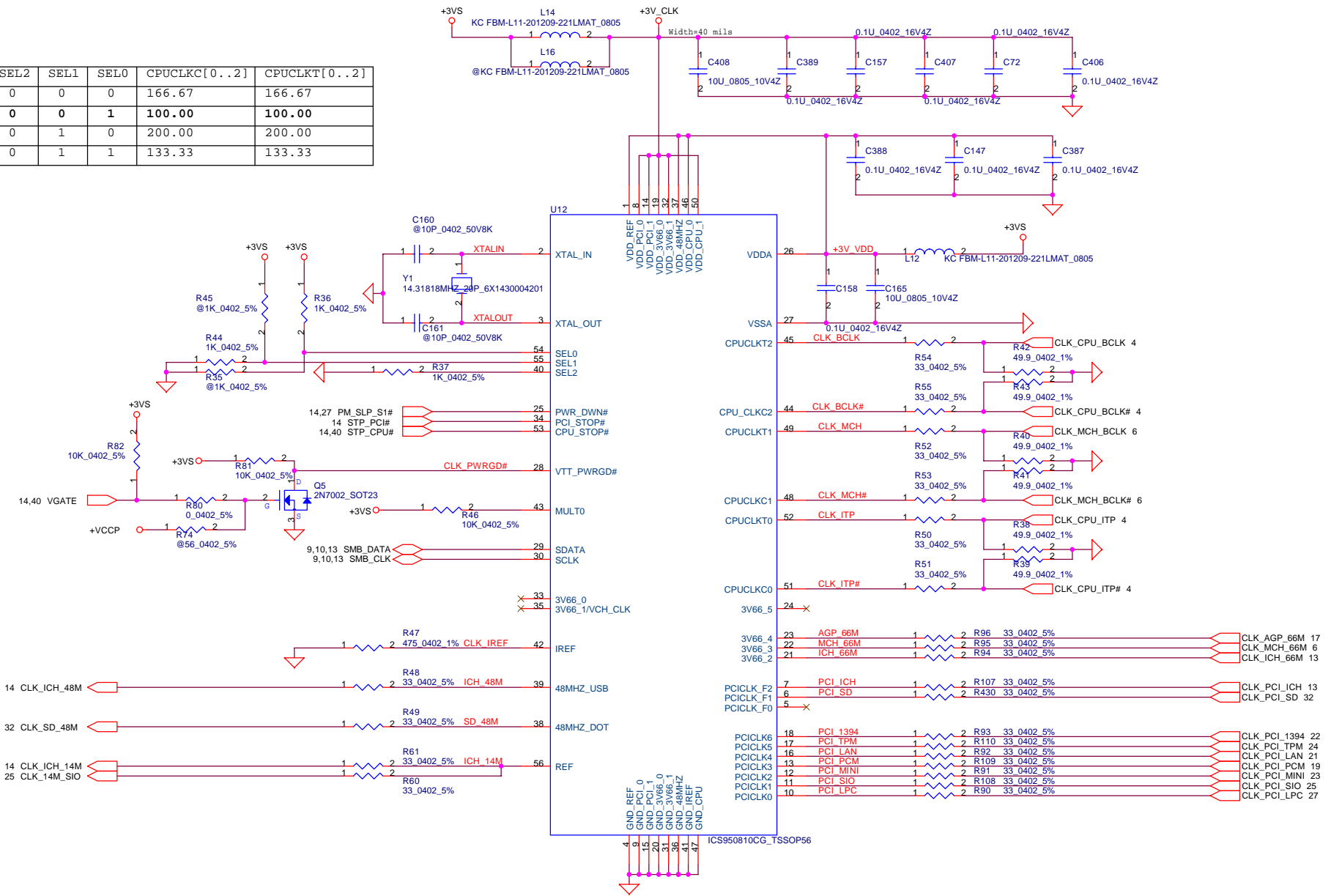
**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25V

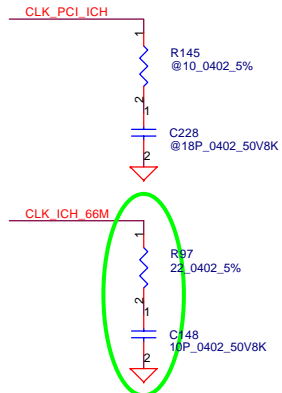


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<b>Compal Electronics, Inc.</b>			
<b>DDR SODIMM Decoupling</b>			
Title	Document Number		
Size	Custom	<b>DAT20 LA-1971</b>	Rev 0.3
Date:	Friday, September 26, 2003	Sheet 11 of 42	

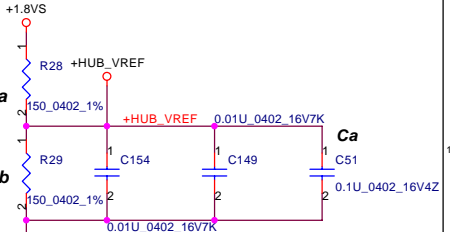
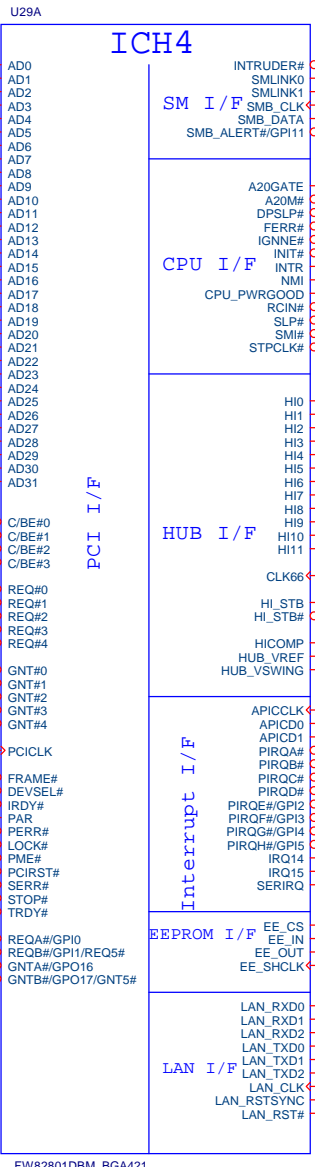
SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



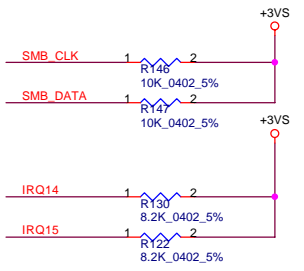


19,21,22,23 PCI\_AD[0..31] PCI\_AD[0..31]

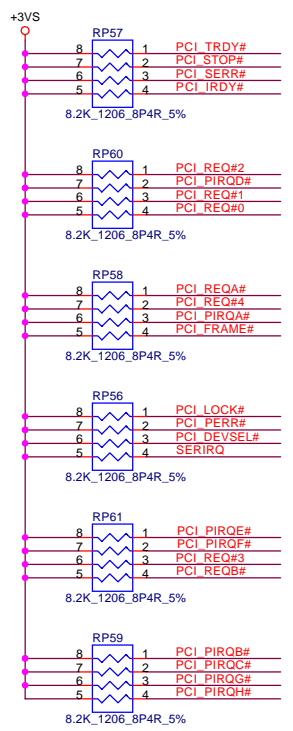
PCI AD0	H5	AD0
PCI AD1	J3	AD1
PCI AD2	H3	AD2
PCI AD3	K1	AD3
PCI AD4	G5	AD4
PCI AD5	J4	AD5
PCI AD6	H4	AD6
PCI AD7	J5	AD7
PCI AD8	K2	AD8
PCI AD9	G2	AD9
PCI AD10	L1	AD10
PCI AD11	G4	AD11
PCI AD12	L2	AD12
PCI AD13	H2	AD13
PCI AD14	L3	AD14
PCI AD15	F5	AD15
PCI AD16	F4	AD16
PCI AD17	N1	AD17
PCI AD18	E5	AD18
PCI AD19	N2	AD19
PCI AD20	E3	AD20
PCI AD21	N3	AD21
PCI AD22	E4	AD22
PCI AD23	M5	AD23
PCI AD24	E2	AD24
PCI AD25	P1	AD25
PCI AD26	E1	AD26
PCI AD27	P2	AD27
PCI AD28	D3	AD28
PCI AD29	R1	AD29
PCI AD30	D2	AD30
PCI AD31	P4	AD31



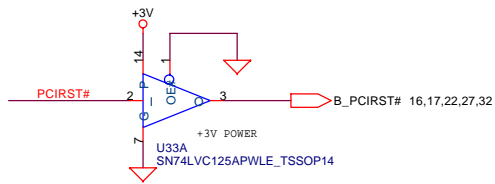
Note: Ra, Rb, Ca placement center of MCH and ICH4M



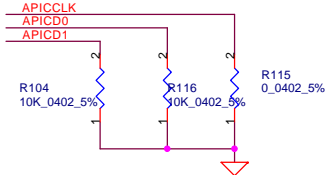
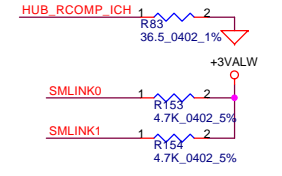
PCI Pullups



19,21,22,23	PCI_C/BE#0	PCI_C/BE#0	J2	C/BE#0
19,21,22,23	PCI_C/BE#1	PCI_C/BE#1	K4	C/BE#1
19,21,22,23	PCI_C/BE#2	PCI_C/BE#2	M4	C/BE#2
19,21,22,23	PCI_C/BE#3	PCI_C/BE#3	N4	C/BE#3
22	PCI_REQ#0	PCI_REQ#0	B1	REQ#0
23	PCI_REQ#1	PCI_REQ#1	A2	REQ#1
19	PCI_REQ#2	PCI_REQ#2	B3	REQ#2
21	PCI_REQ#3	PCI_REQ#3	C7	REQ#3
23	PCI_REQ#4	PCI_REQ#4	B6	REQ#4
22	PCI_GNT#0	PCI_GNT#0	C1	GNT#0
23	PCI_GNT#1	PCI_GNT#1	E6	GNT#1
19	PCI_GNT#2	PCI_GNT#2	A7	GNT#2
21	PCI_GNT#3	PCI_GNT#3	B7	GNT#3
23	PCI_GNT#4	PCI_GNT#4	D6	GNT#4
12	CLK_PCI_ICH	CLK_PCI_ICH	P5	PCICLK
19,21,22,23	PCI_FRAME#	PCI_FRAME#	F1	FRAME#
19,21,22,23	PCI_DEVSEL#	PCI_DEVSEL#	M3	DEVSEL#
19,21,22,23	PCI_IRDY#	PCI_IRDY#	L5	IRDY#
19,21,22,23	PCI_PAR	PCI_PERR#	G1	PAR
19,21,22,23	PCI_PERR#	PCI_LOCK#	M2	PERR#
19,21,22,23	PCI_LOCK#	PCI_RST#	U5	LOCK#
7,19,20,21,23,24,25	PCIRST#	PCIRST#	U5	PCIRST#
19,21,22,23	PCI_SERR#	PCI_SERR#	K5	SERR#
19,21,22,23	PCI_STOP#	PCI_STOP#	F3	STOP#
19,21,22,23	PCI_TRDY#	PCI_TRDY#	F2	TRDY#
16	SIDERST#	PCI_REQA#	B5	REQA#/GPIO
		PCI_REQB#	A6	REQB#/GPIO11/REQ#5
		SIDERST#	E8	GNTA#/GPO16
			C5	GNTB#/GPO17/GNT#5



Place closed to Pin AA21



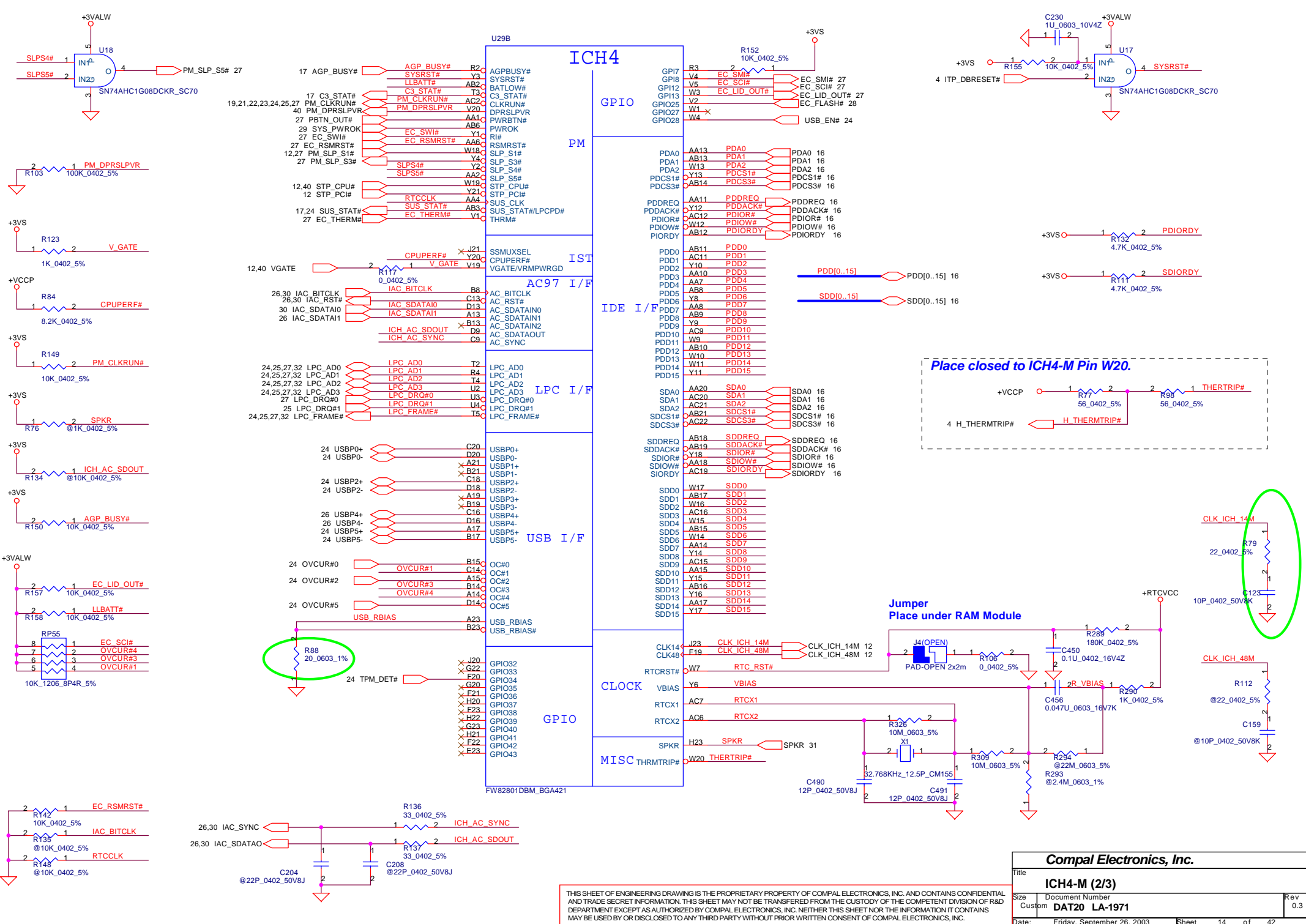
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**Compal Electronics, Inc.**

Title: **ICH4-M (1/3)**

Size: Custom    Document Number: **DAT20 LA-1971**    Rev: 0.3

Date: Friday, September 26, 2003    Sheet: 13 of 42



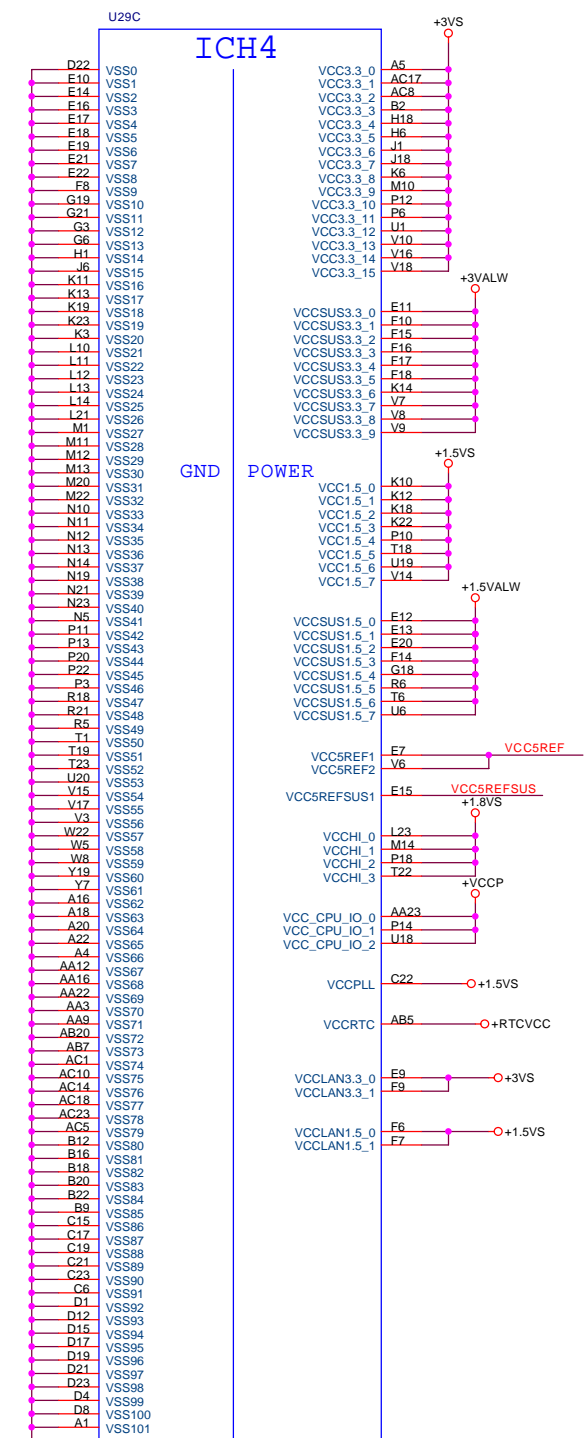
Place closed to ICH4-M Pin W20.

+VCCP --- R77 --- THERTRIP# --- R98 --- H\_THERTRIP# --- H\_THERTRIP#

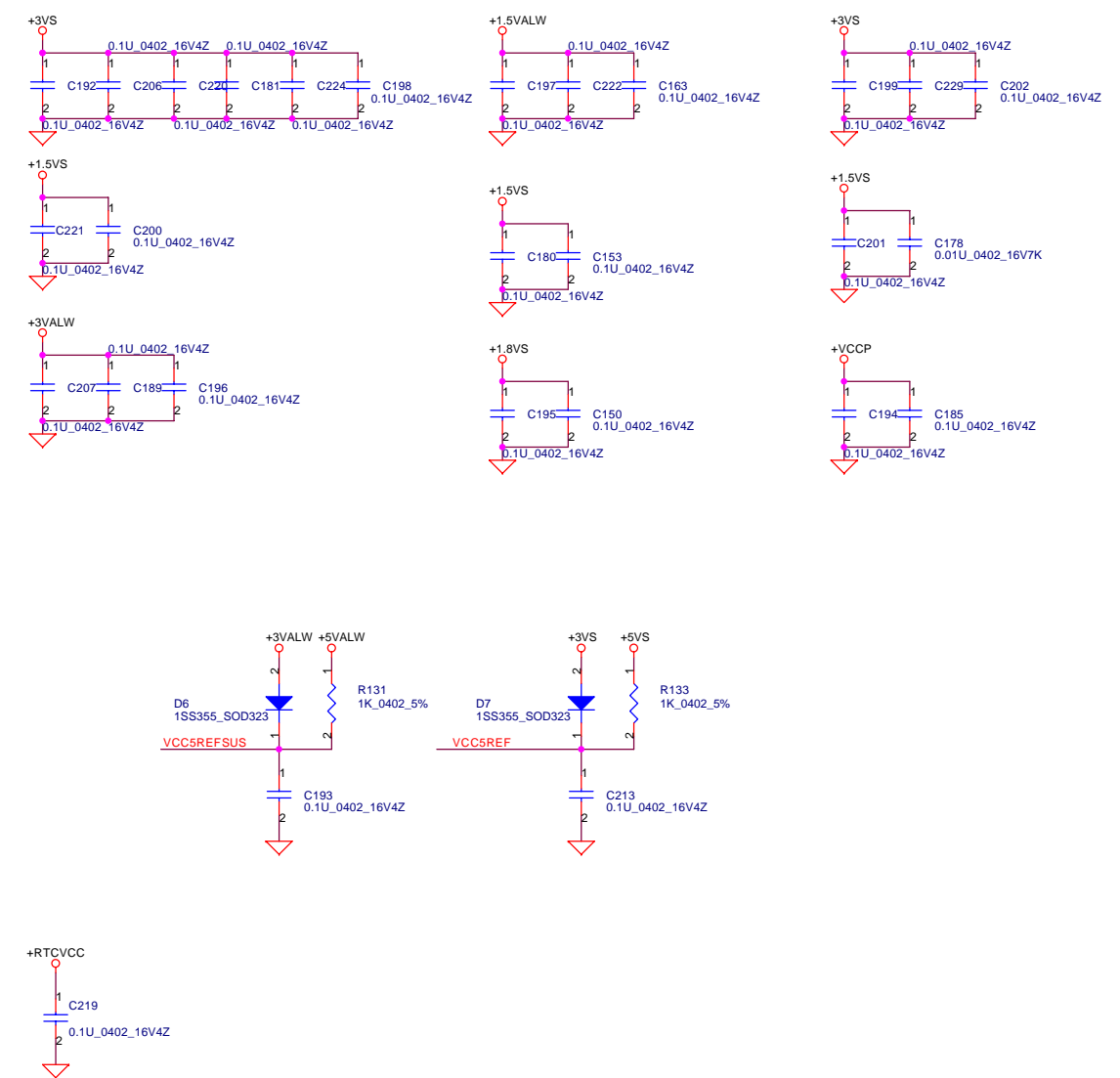
Jumper Place under RAM Module

<b>Compal Electronics, Inc.</b>		
Title: <b>ICH4-M (2/3)</b>		
Size: Custom	Document Number: <b>DAT20 LA-1971</b>	Rev: 0.3
Date: Friday, September 26, 2003	Sheet: 14 of 42	

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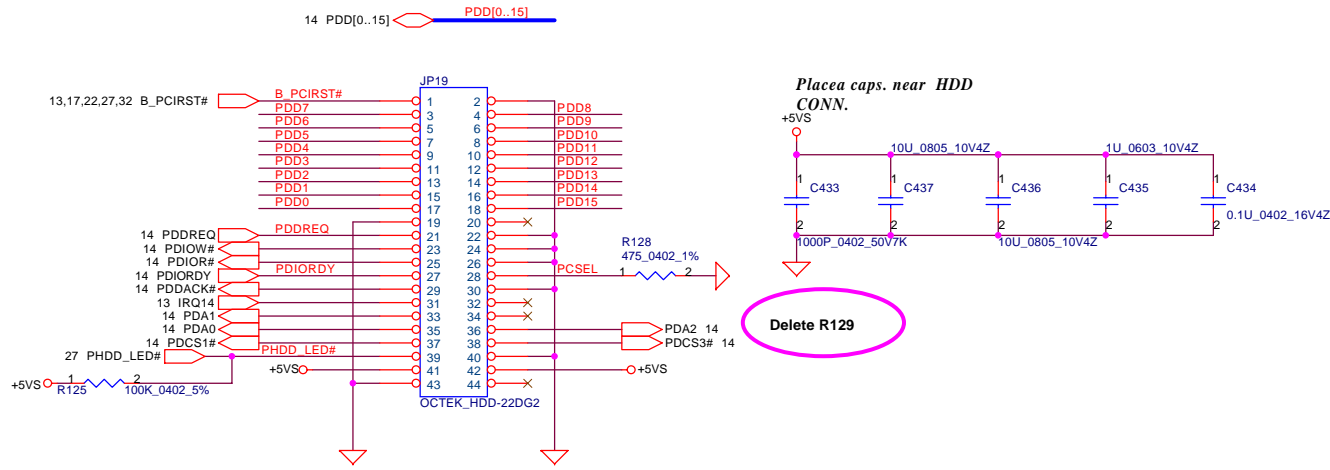
FW82801DBM\_BGA421



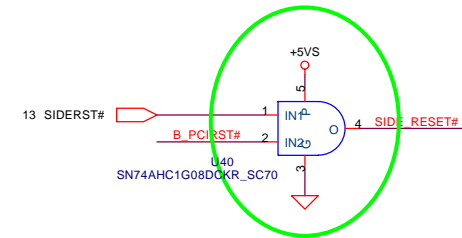
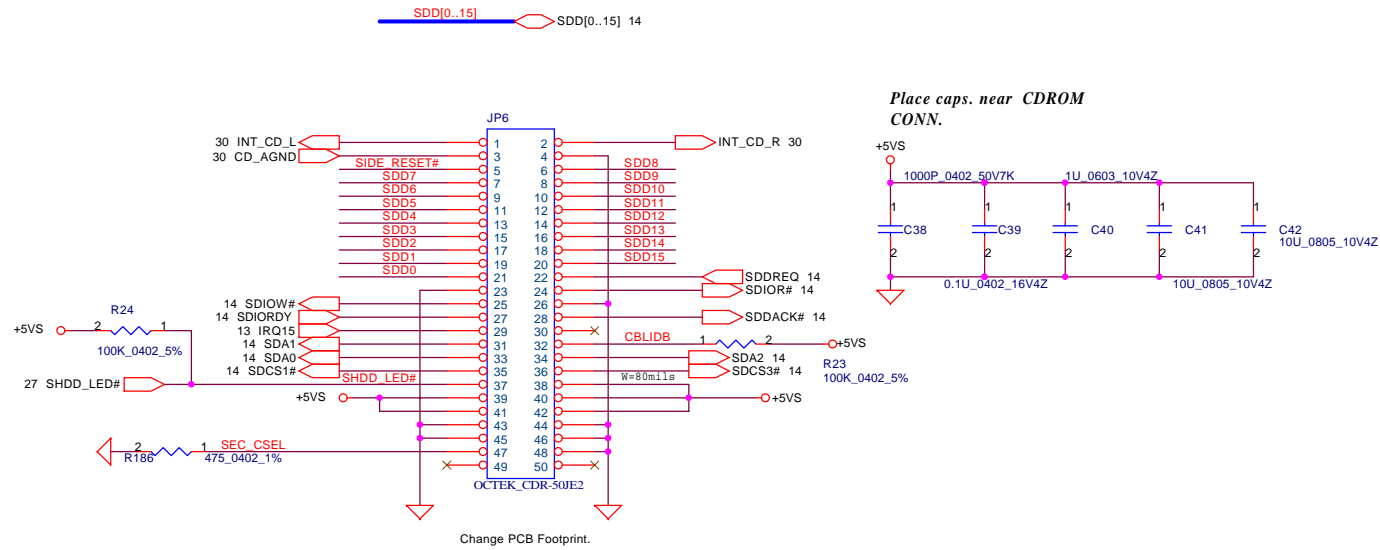
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<b>Compal Electronics, Inc.</b>		
Title		
<b>ICH4-M (3/3)</b>		
Size	Document Number	Rev
Custom	<b>DAT20 LA-1971</b>	0.3
Date:	Friday, September 26, 2003	Sheet 15 of 42

**HDD Connector**



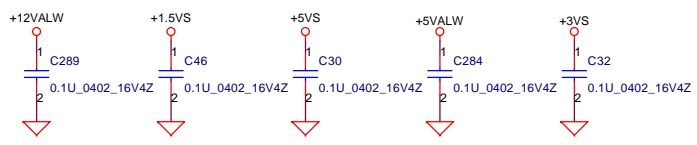
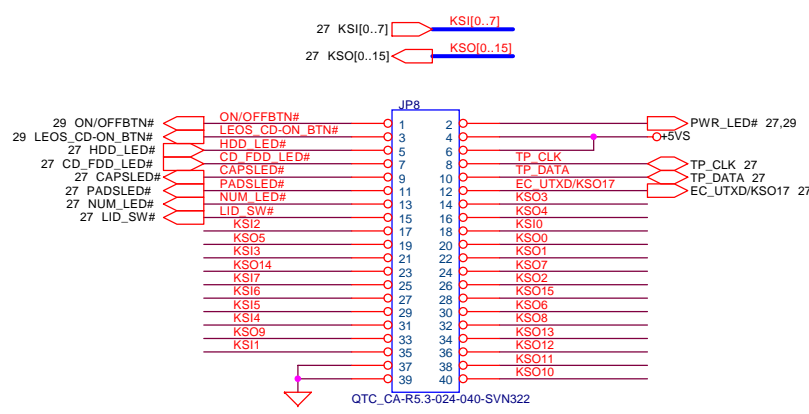
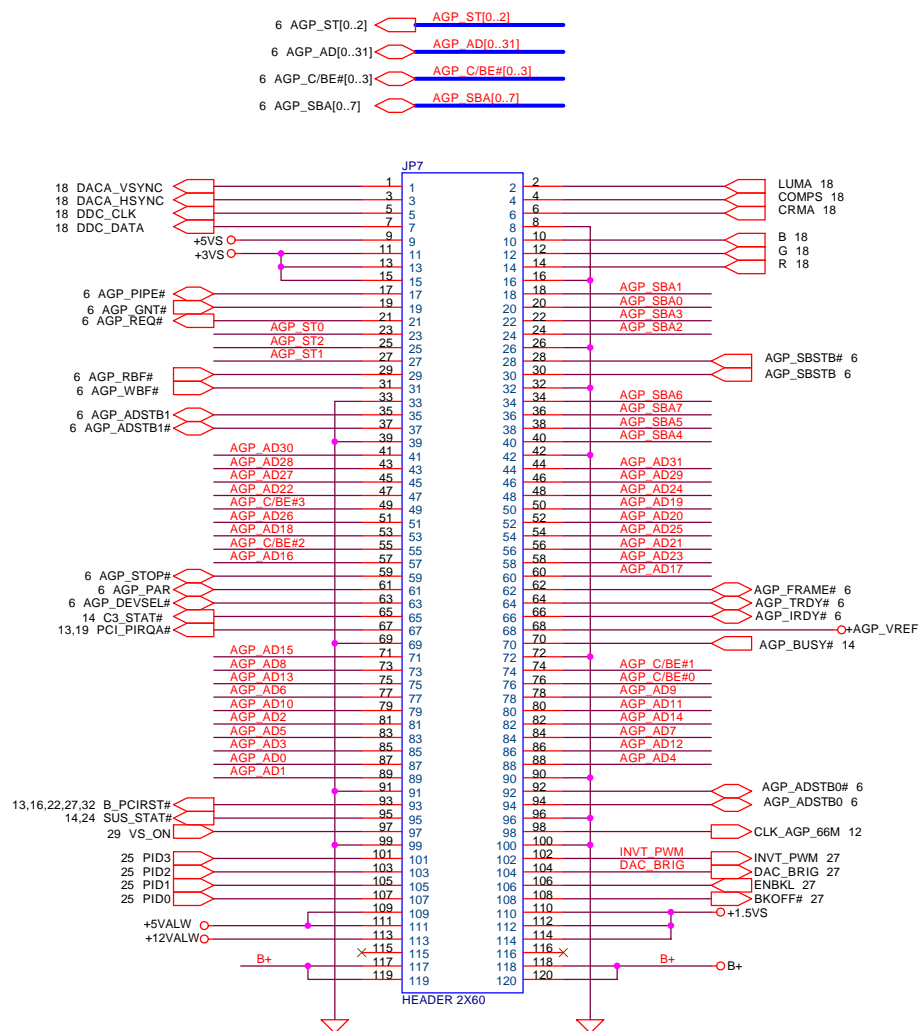
**CD-ROM Connector**



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<b>Compal Electronics, Inc.</b>		
Title	<b>IDE/CD-ROM Module</b>	
Size	Document Number	Rev
Custom	<b>DAT20 LA-1971</b>	0.3
Date:	Friday, September 26, 2003	Sheet 16 of 42

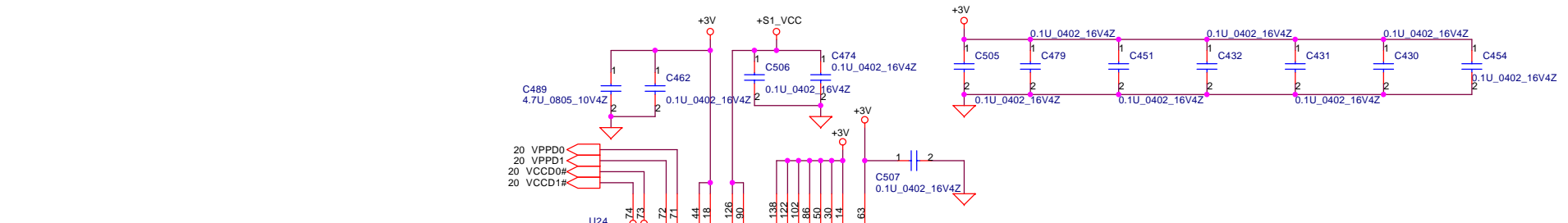




<b>Compal Electronics, Inc.</b>		
Title <b>AGP Connector</b>		
Size	Document Number	Rev
Custom	<b>DAT20 LA-1971</b>	0.3
Date:	Friday, September 26, 2003	Sheet 17 of 42

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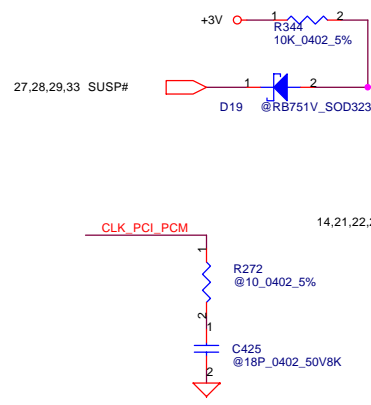
13,21,22,23 PCI\_AD[0..31] PCI\_AD[0..31]

PCI_AD31	3	AD31	CAD31/D10	144	S1_D10
PCI_AD30	4	AD30	CAD30/D9	142	S1_D9
PCI_AD29	5	AD29	CAD29/D1	141	S1_D1
PCI_AD28	7	AD28	CAD28/D8	140	S1_D8
PCI_AD27	8	AD27	CAD27/D0	139	S1_D0
PCI_AD26	9	AD26	CAD26/A0	129	S1_A0
PCI_AD25	10	AD25	CAD25/A1	128	S1_A1
PCI_AD24	11	AD24	CAD24/A2	127	S1_A2
PCI_AD23	15	AD24	CAD24/A2	124	S1_A3
PCI_AD22	16	AD23	CAD23/A3	121	S1_A4
PCI_AD21	17	AD22	CAD22/A4	120	S1_A5
PCI_AD20	19	AD20	CAD20/A6	118	S1_A6
PCI_AD19	23	AD19	CAD19/A25	116	S1_A25
PCI_AD18	24	AD18	CAD18/A7	115	S1_A7
PCI_AD17	25	AD17	CAD17/A24	113	S1_A24
PCI_AD16	26	AD17	CAD17/A24	98	S1_A17
PCI_AD15	38	AD16	CAD16/A17	96	S1_IOWR#
PCI_AD14	39	AD15	CAD15/IOWR#	97	S1_A9
PCI_AD13	40	AD14	CAD14/A9	93	S1_IORD#
PCI_AD12	41	AD12	CAD12/A11	92	S1_A11
PCI_AD11	43	AD11	CAD11/OE#	91	S1_OE#
PCI_AD10	45	AD10	CAD10/CE2#	89	S1_CE2#
PCI_AD9	46	AD9	CAD9/A10	87	S1_D15
PCI_AD8	47	AD8	CAD8/D15	85	S1_D7
PCI_AD7	49	AD7	CAD7/D7	82	S1_D13
PCI_AD6	51	AD6	CAD6/D13	83	S1_D6
PCI_AD5	52	AD5	CAD5/D6	80	S1_D12
PCI_AD4	53	AD4	CAD4/D12	81	S1_D5
PCI_AD3	54	AD3	CAD3/D5	77	S1_D11
PCI_AD2	55	AD2	CAD2/D11	79	S1_D4
PCI_AD1	56	AD1	CAD1/D4	76	S1_D3
PCI_AD0	57	AD0	CAD0/D3		

PQFP 144  
22.2 X 22.2 X 1.60

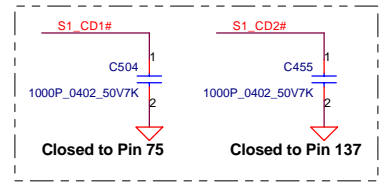
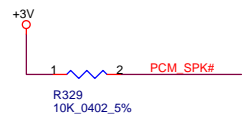
S1\_A[0..25] S1\_A[0..25] 20  
S1\_D[0..15] S1\_D[0..15] 20

IDSEL:PCI\_AD20



13,21,22,23 PCI_C/BE#3	12	C/BE3#
13,21,22,23 PCI_C/BE#2	27	C/BE2#
13,21,22,23 PCI_C/BE#1	37	C/BE1#
13,21,22,23 PCI_C/BE#0	48	C/BE0#
7,13,20,21,23,24,25 PCIRST#	20	RST#
13,21,22,23 PCI_FRAME#	28	FRAME#
13,21,22,23 PCI_IRDY#	29	IRDY#
13,21,22,23 PCI_TRDY#	31	TRDY#
13,21,22,23 PCI_DEVSEL#	32	DEVSEL#
13,21,22,23 PCI_STOP#	33	STOP#
13,21,22,23 PCI_PERR#	34	PERR#
13,21,22,23 PCI_SERR#	35	SERR#
13,21,22,23 PCI_PAR#	36	PAR#
13 PCI_REQ#2	1	REQ#
13 PCI_GNT#2	2	GNT#
12 CLK_PCI_PCM	21	CLK
21,22,23,27 PCM_PME#	59	RI_OUT#/PME#
21,22,23,27 PCM_ID	70	SUSPEND#
13,17 PCI_PIRQA#	60	IDSEL
13,24,25,27,32 SERIRQ	61	MFUNC0
	62	MFUNC1
	64	MFUNC2
	65	MFUNC3
	67	MFUNC4
	68	MFUNC5
	69	MFUNC6
14,21,22,23,24,25,27 PM_CLKRUN#	66	CBLOCK#/A19
20,24 CBRST#	66	CINT#/READY

CC/BE3#/REG#	125	S1_REG#	S1_REG# 20
CC/BE2#/A12	112	S1_A12	
CC/BE1#/A8	99	S1_A8	
CC/BE0#/CE1#	88	S1_CE1#	S1_CE1# 20
CRST#/RESET	119	S1_RST	S1_RST 20
CFRAME#/A23	111	S1_A23	
IRDY#/A15	110	S1_A15	
CTRDY#/A22	109	S1_A22	
CDEVSEL#/A21	107	S1_A21	
CSTOP#/A20	105	S1_A20	
CPERR#/A14	104	S1_A14	
CSERR#/WAIT#	133	S1_WAIT#	S1_WAIT# 20
CPAR#/A13	101	S1_A13	
CPAR#/A13	101	S1_INPACK#	S1_INPACK# 20
CREQ#/INPACK#	106	S1_WE#	S1_WE# 20
CGNT#/WE#	108	A16_CLK	S1_A16
CCLK#/A16	108	A16_CLK	
CSTSCHG/BVD1	135	S1_BVD1	S1_BVD1 20
CCLKRUN#/WP	136	S1_WP	S1_WP 20
CBLOCK#/A19	103	S1_A19	
CINT#/READY	132	S1_RDY#	S1_RDY# 20
SPKOUT	62	PCM_SPK#	PCM_SPK# 31
CAUDIO/BVD2	134	S1_BVD2	S1_BVD2 20
CCD2#/CD2#	137	S1_CD2#	S1_CD2# 20
CCD1#/CD1#	125	S1_CD1#	S1_CD1# 20
CVS2/VS2#	117	S1_VS2	S1_VS2 20
CVS1/VS1#	131	S1_VS1	S1_VS1 20



**Compal Electronics, Inc.**

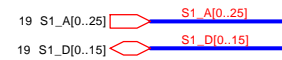
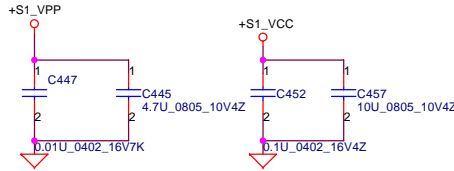
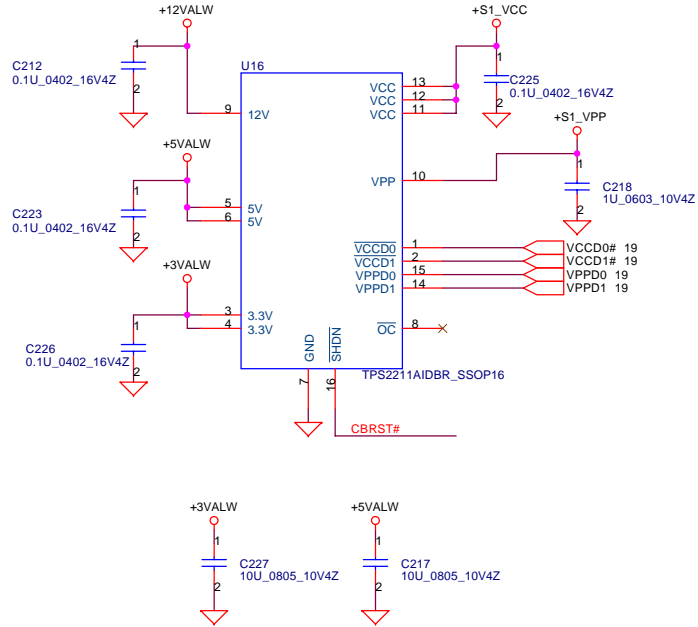
Title: **PCMCIA controller ENE CB1410**

Size: Custom Document Number: **DAT20 LA-1971** Rev: 0.3

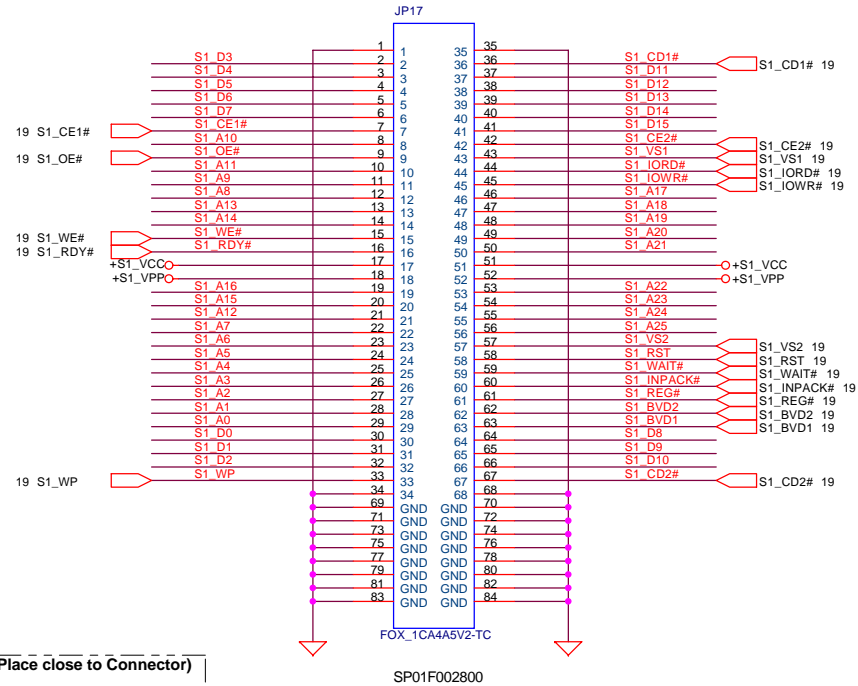
Date: Friday, September 26, 2003 Sheet: 19 of 42

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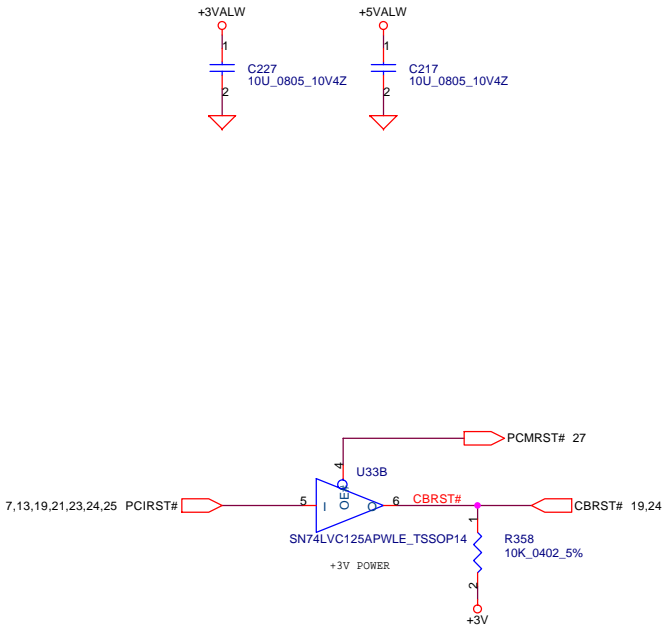
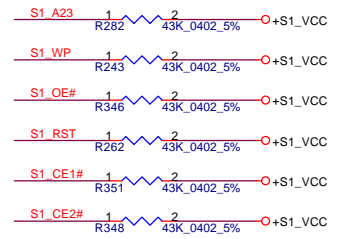
**PCMCIA Power Controller**

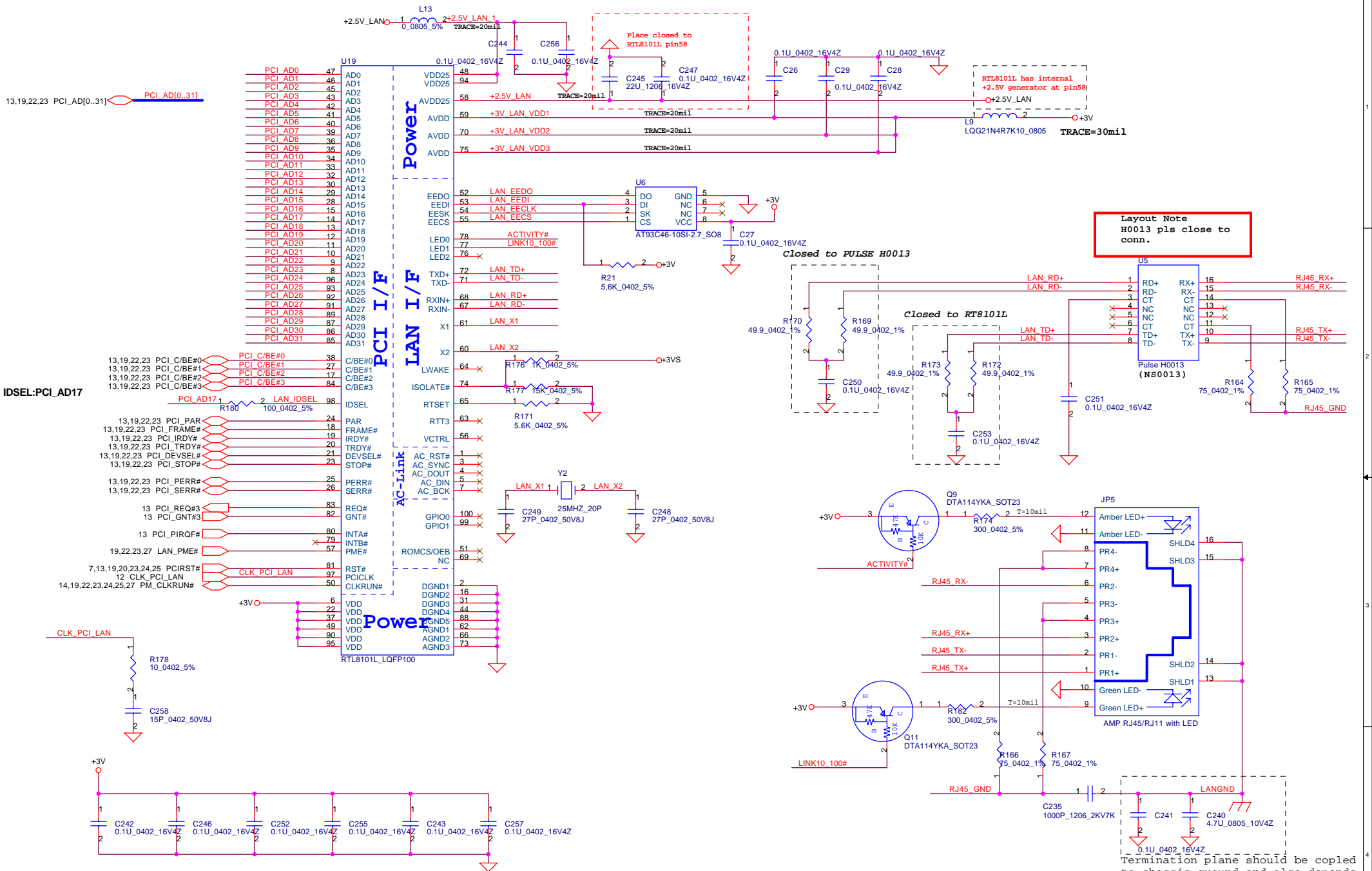


**CardBus Socket**



**For CB1410 Rev.B0 (Place close to Connector)**





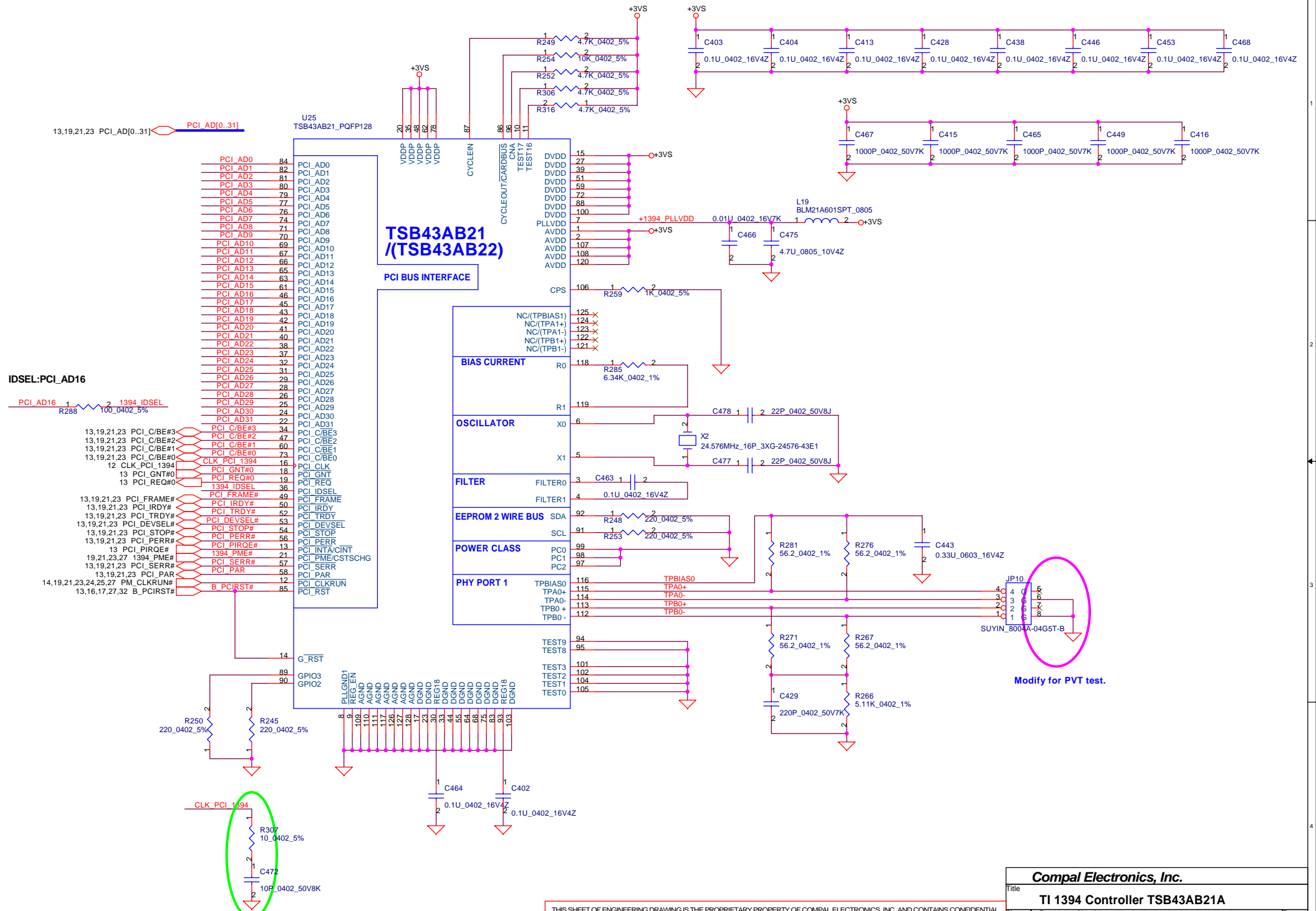
13,19,22,23 PCI\_AD[0..31] PCI\_AD[0..31]

IDSEL:PCI\_AD17

CLK\_PCI\_LAN

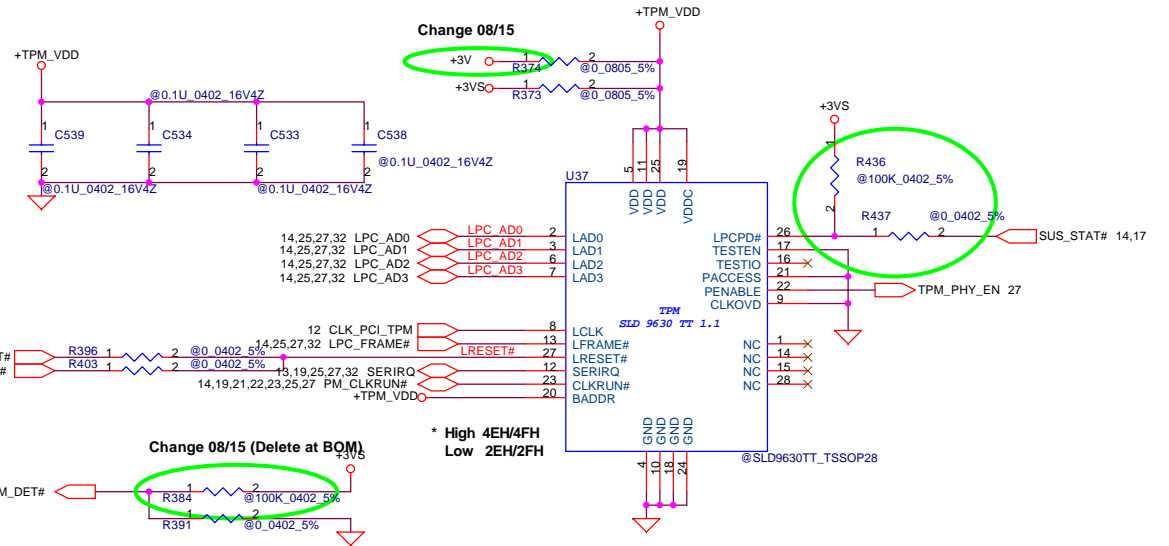
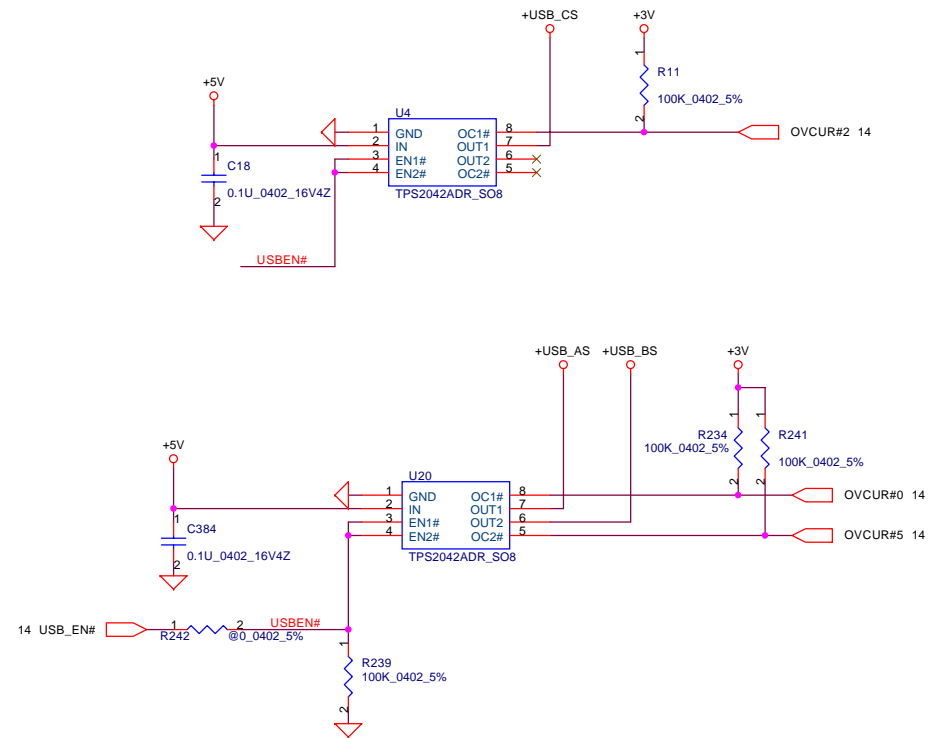
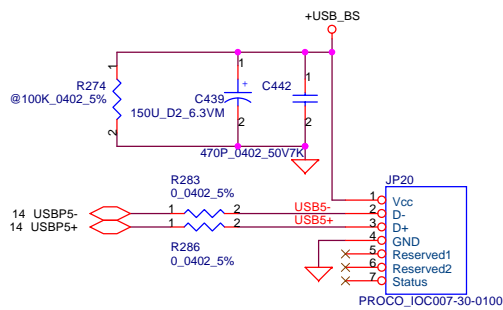
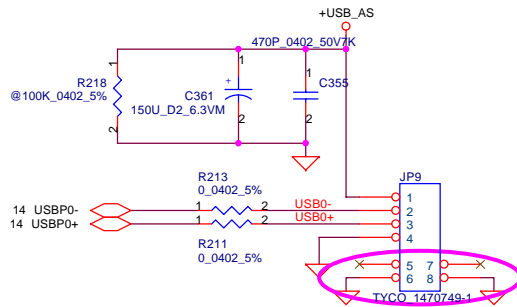
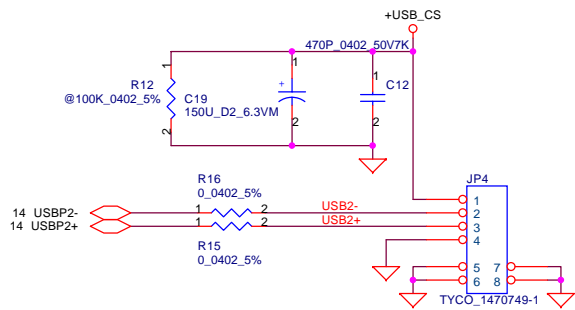
Compal Electronics, Inc.		
Title	LAN REALTEK RTL8101L	
Size	Document Number	Rev
Custom	DAT20 LA-1971	0.3
Date:	Friday, September 26, 2003	Sheet 21 of 42

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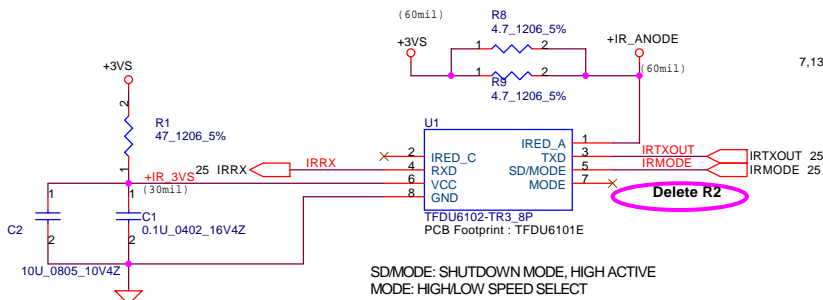


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### FIR Module



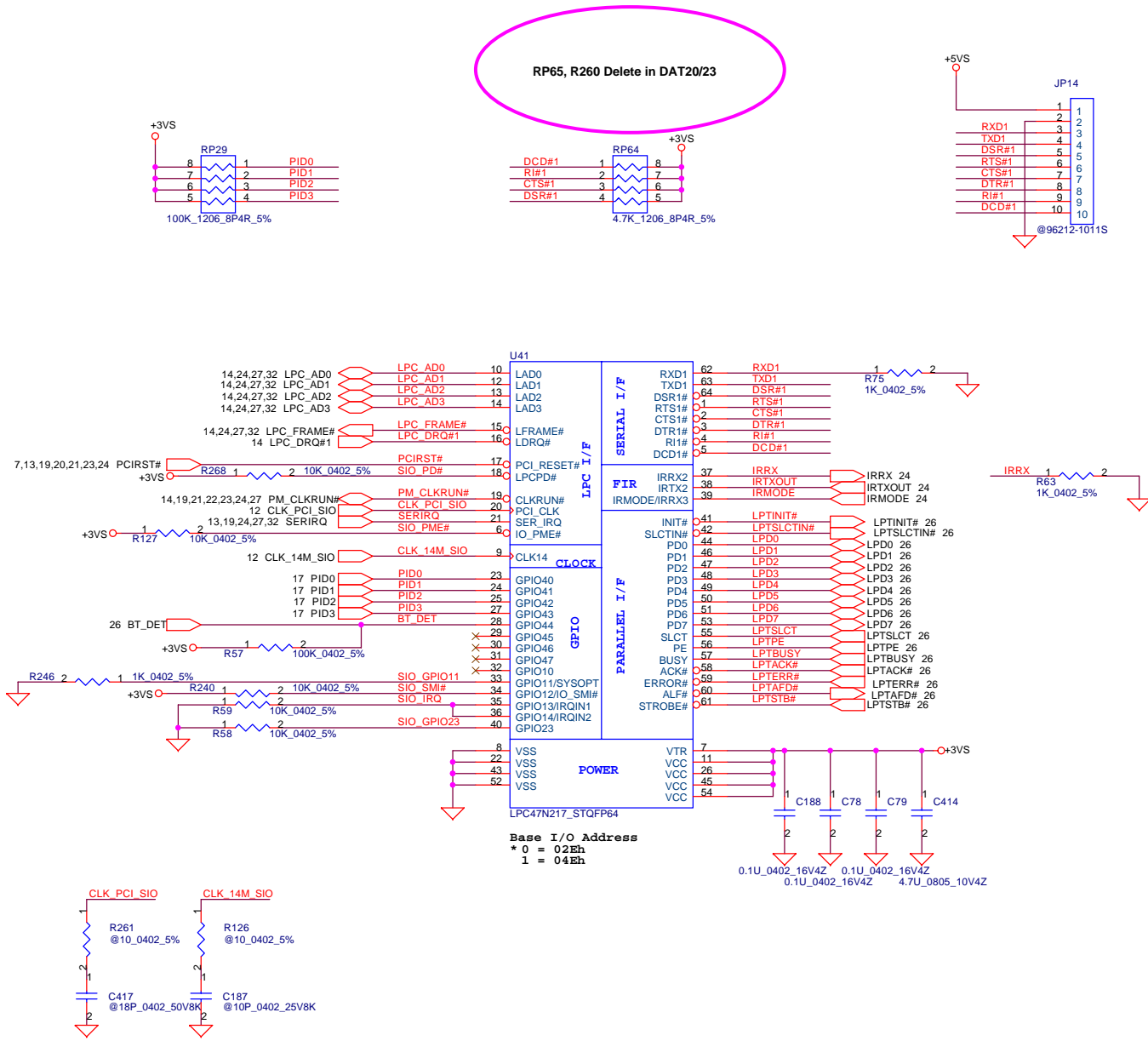
<b>Compal Electronics, Inc.</b>		
<b>USB / FIR / TPM</b>		
Size	Document Number	Rev
Custom	<b>DAT20 LA-1971</b>	0.3
Date:	Friday, September 26, 2003	Sheet 24 of 42

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# SUPER I/O SMC LPC47N217

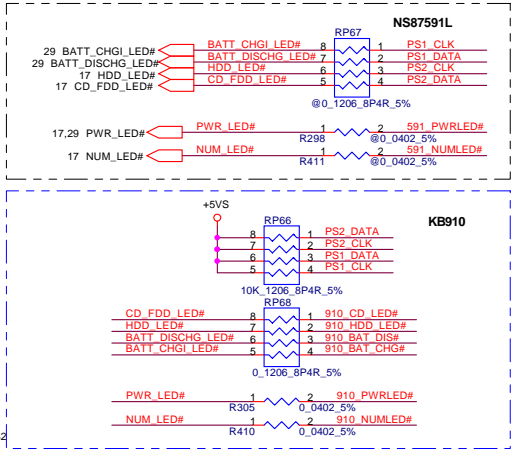
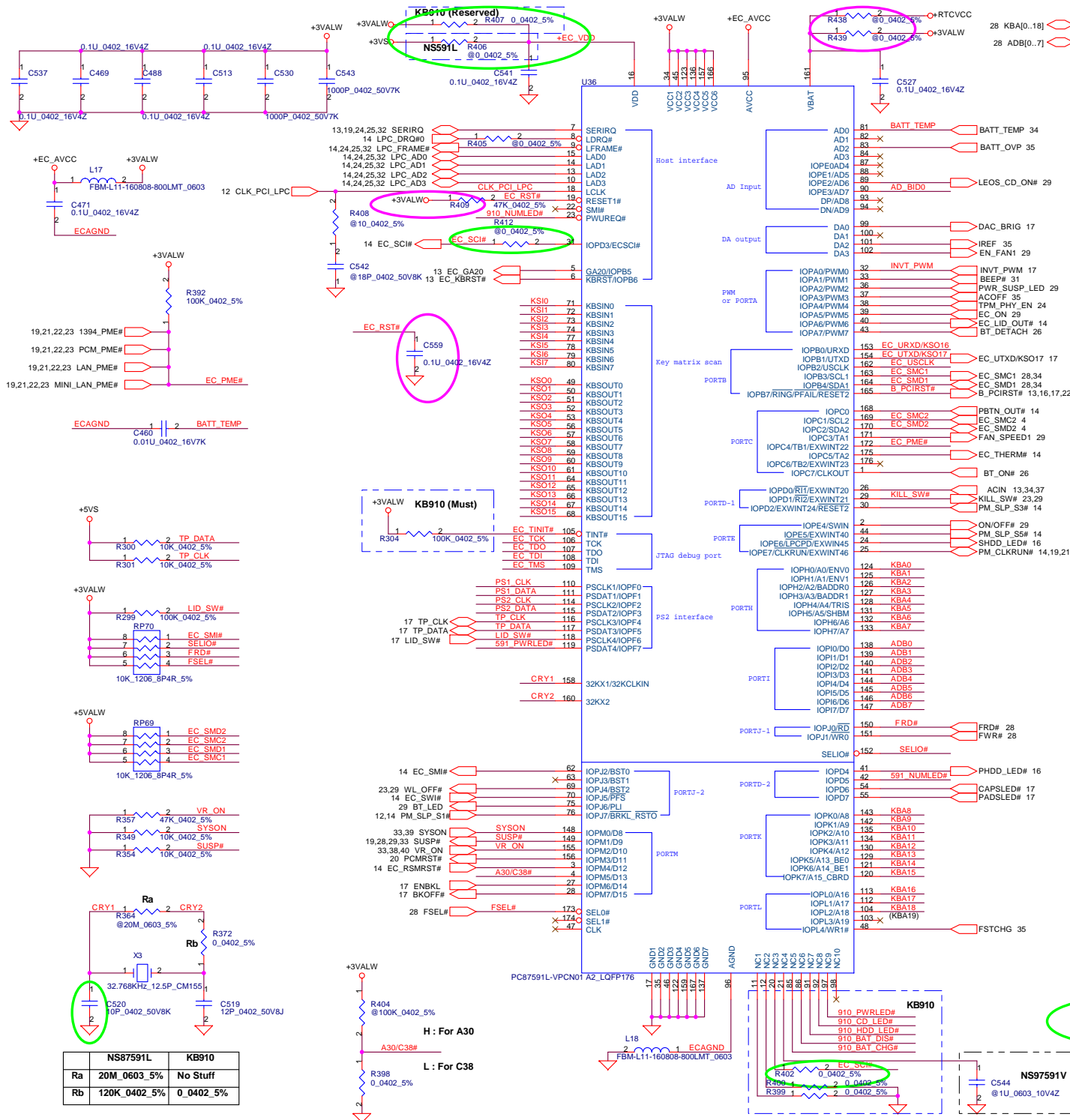
RP65, R260 Delete in DAT20/23



<b>Compal Electronics, Inc.</b>		
Title <b>SUPER I/O LPC47N217</b>		
Size Custom	Document Number <b>DAT20 LA-1971</b>	Rev 0.3
Date: Friday, September 26, 2003	Sheet 25	of 42

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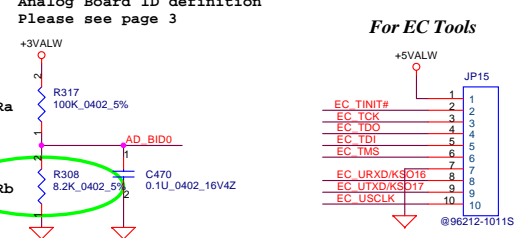
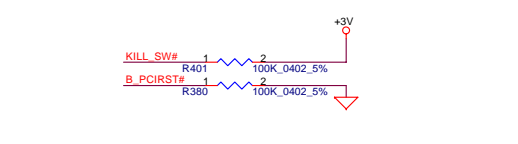
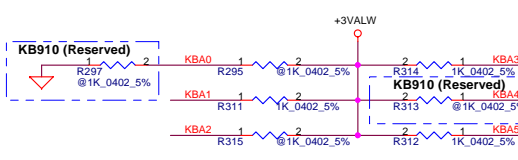




I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
Reserved			

ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0
OB	0	0
DEV	1	0
PROG	1	0

SBHM(KBA5)=1: Enable shared memory with host BIOS  
 TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

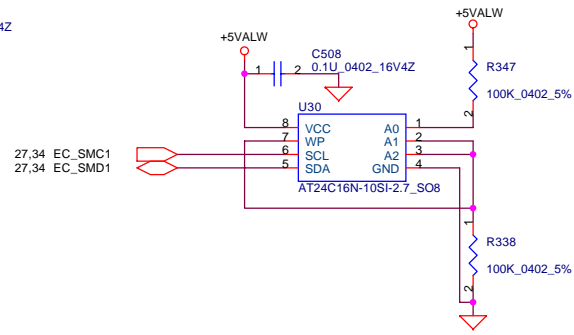
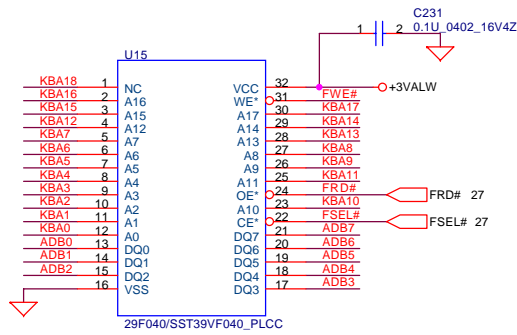
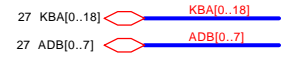
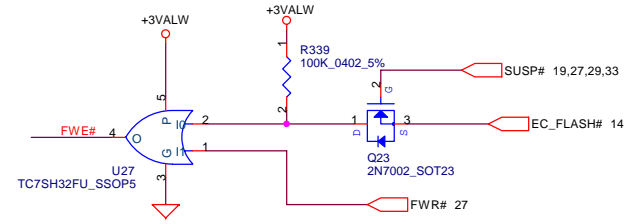
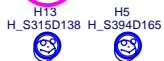
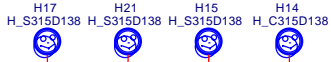
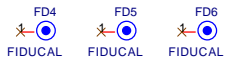
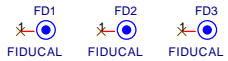
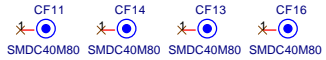
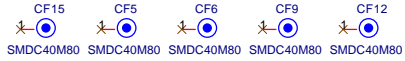
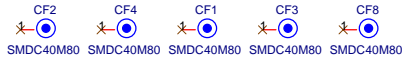


	NS87591L	KB910
Ra	20M_0603_5%	No Stuff
Rb	120K_0402_5%	0_0402_5%

Analog Board ID definition  
 Please see page 3

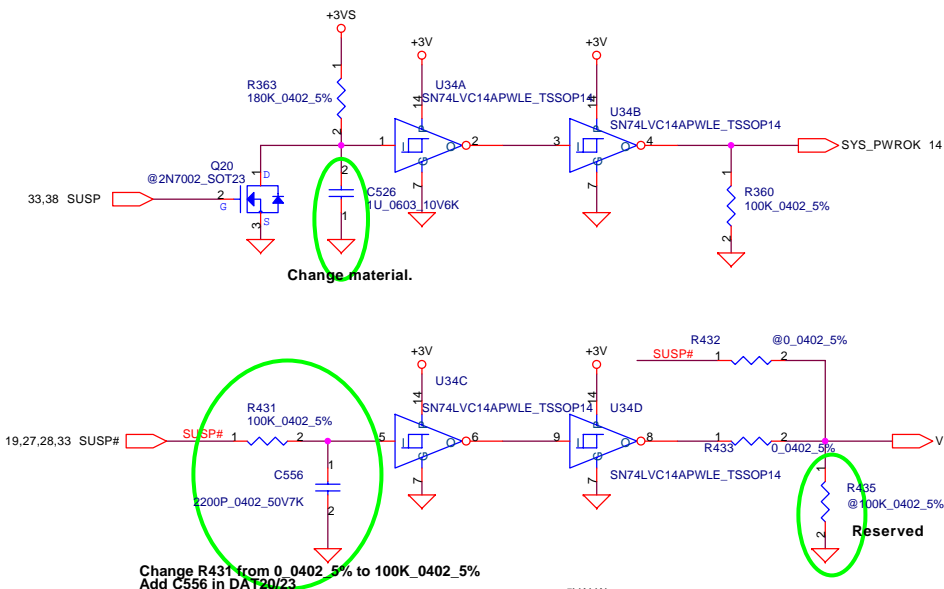
For EC Tools

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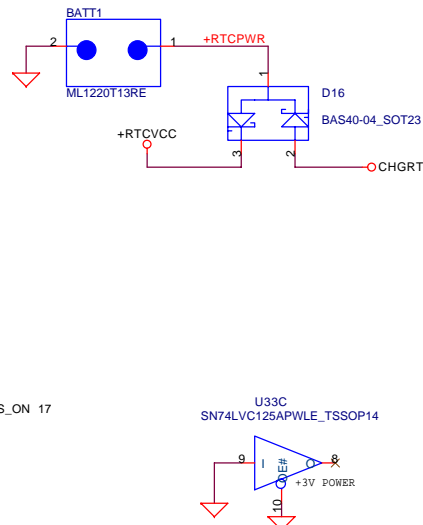


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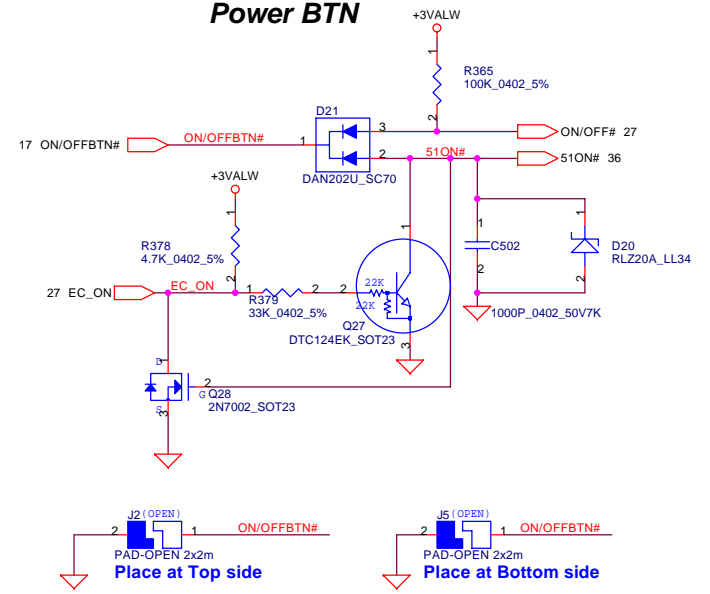
### Power ON Circuit



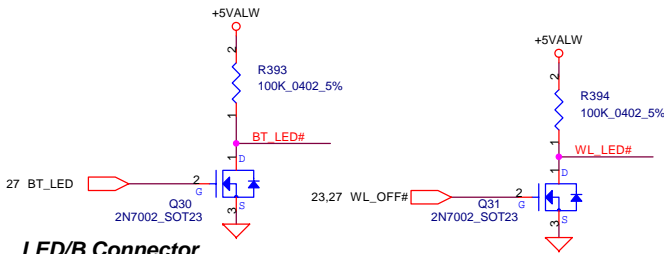
### RTC Battery



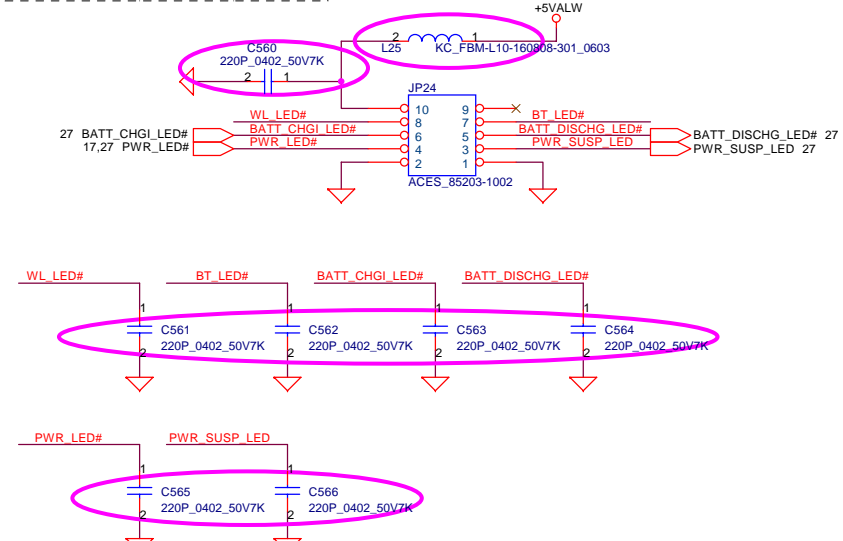
### Power BTN



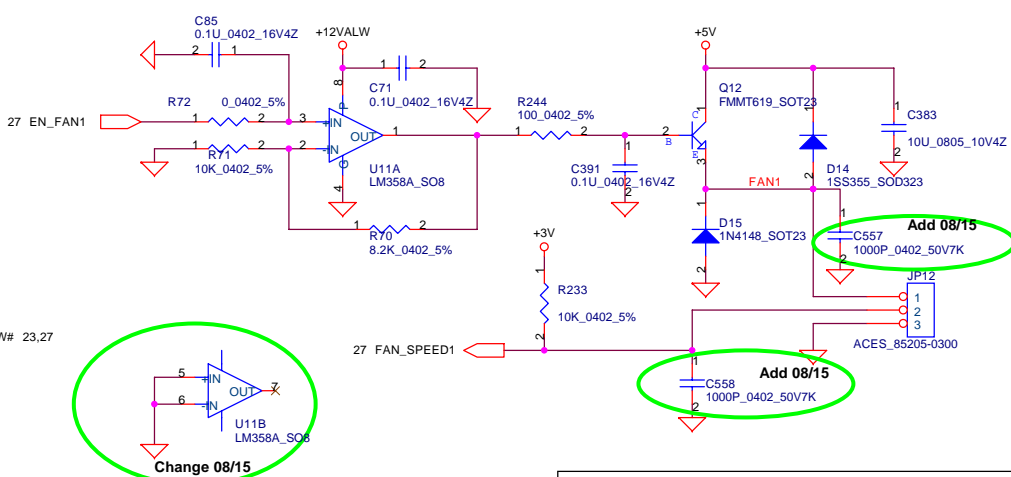
LED INDICATOR	C38	30
PWR	Blue	Green
PWR_SUSP	AMB	AMB
BATT_CHGI	Blue	Green
BATT_DISCHG	AMB	AMB
WL_LED	Blue	Green
BT_LED	AMB	AMB
SD_LED	None	Green



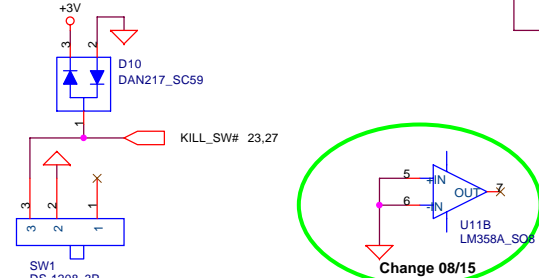
### LED/B Connector



### Fan Control circuit



### KILL\_Switch



**Compal Electronics, Inc.**

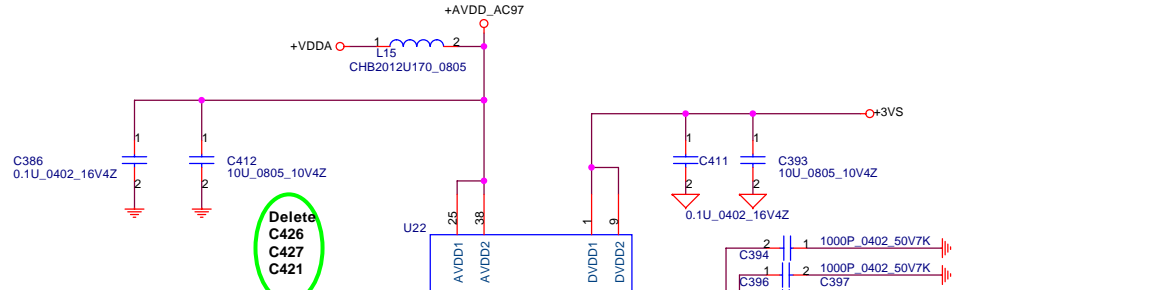
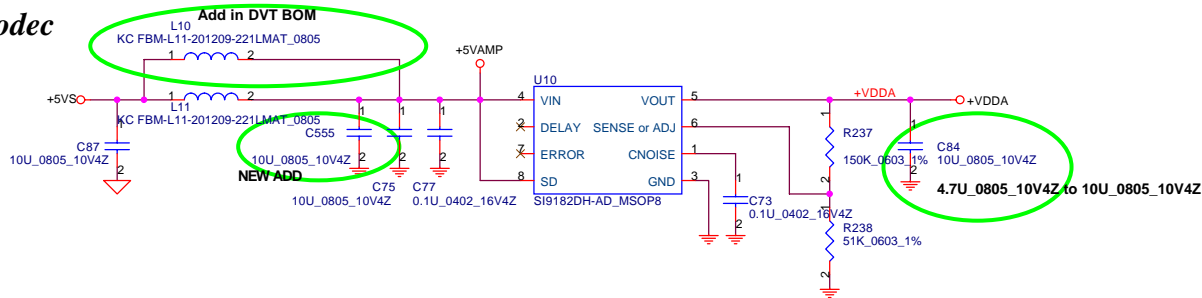
Title: **Power OK/Reset/RTC battery**

Size: Custom    Document Number: **DAT20 LA-1971**    Rev: 0.3

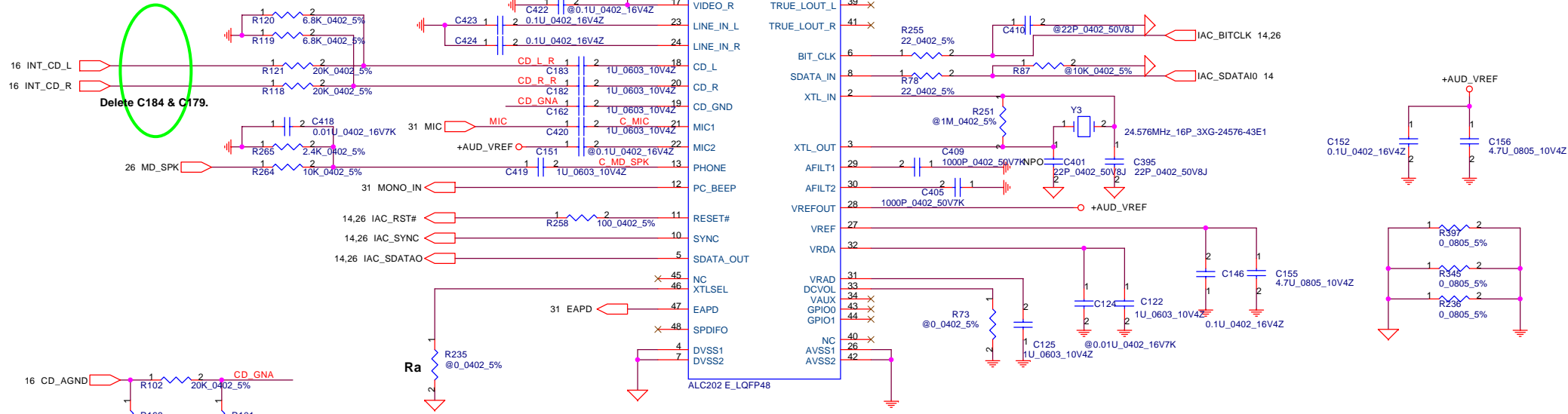
Date: Friday, September 26, 2003    Sheet: 29 of 42

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# AC97 Codec



Reserved for ALC250 disable HW EQ when Headphone plug. **NEW ADD** R434 0.0402\_5% HP SENSE

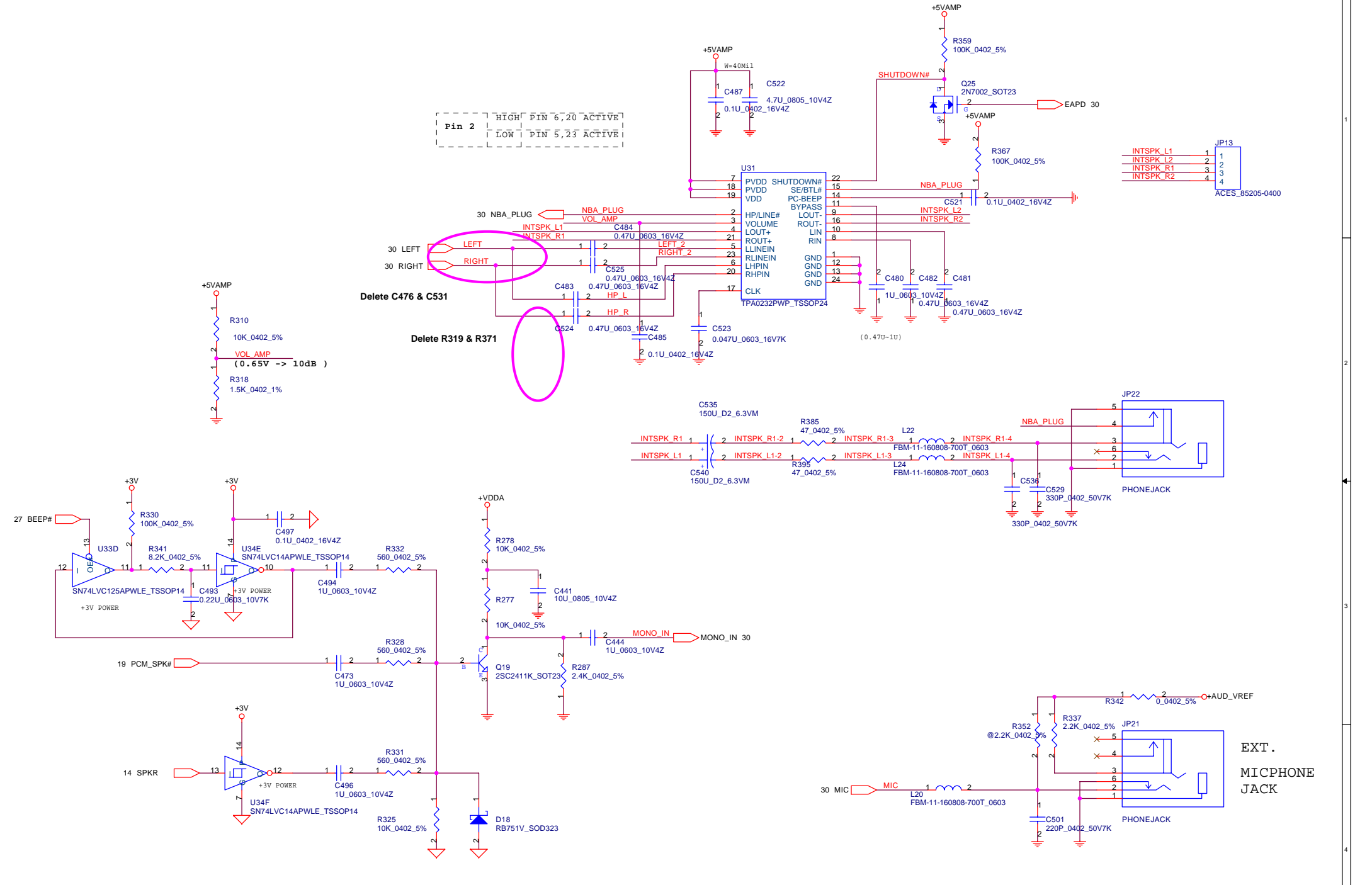


Ra	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

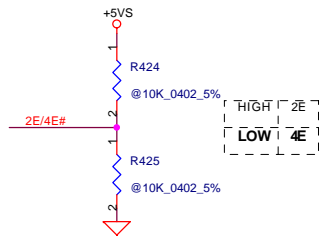
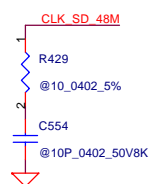
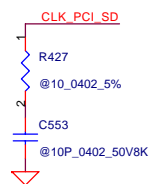
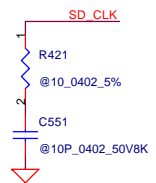
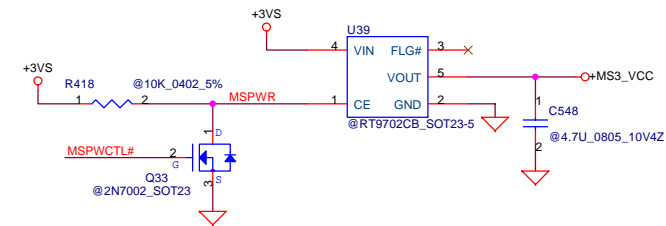
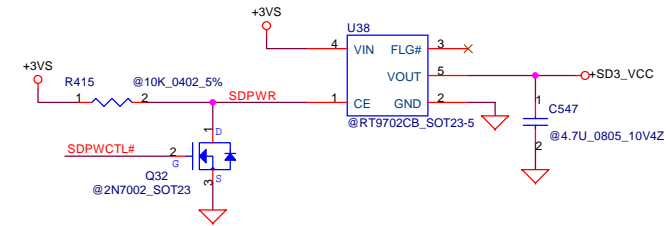
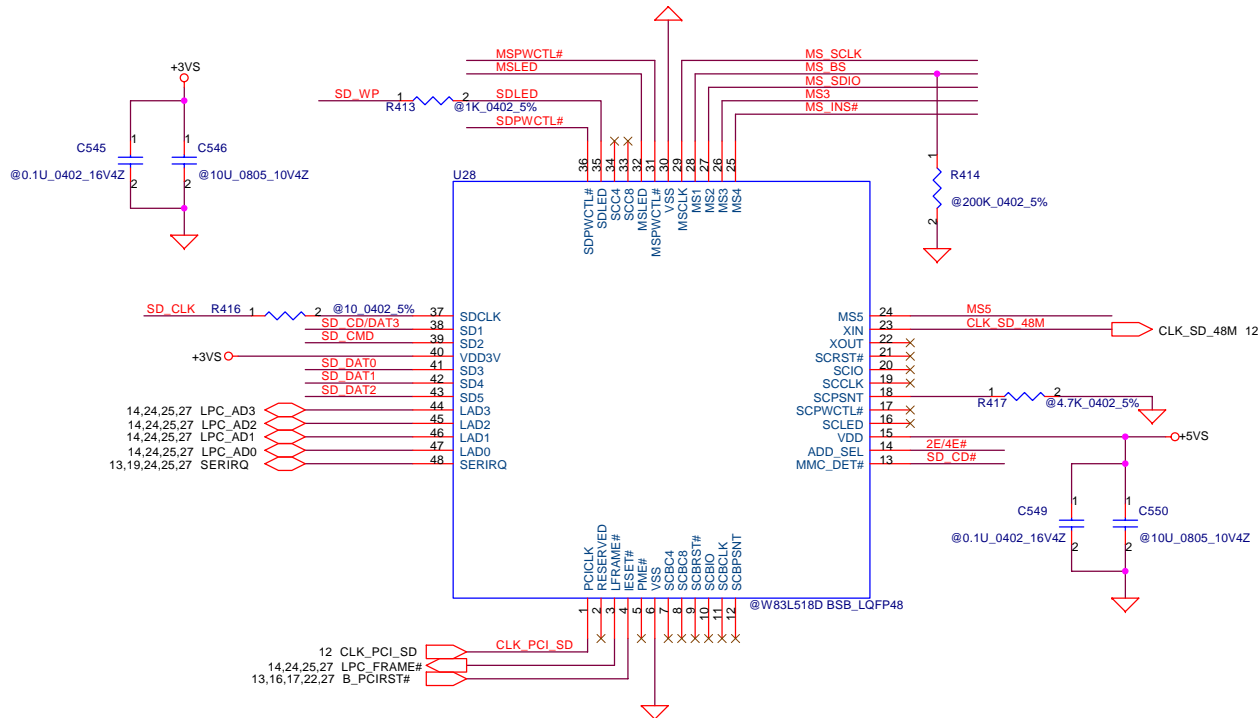
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<b>Compal Electronics, Inc.</b>		
Title <b>AC97 Codec Realtek ALC202</b>		
Size Custom	Document Number <b>DAT20 LA-1971</b>	Rev 0.3
Date: Friday, September 26, 2003	Sheet 30	of 42

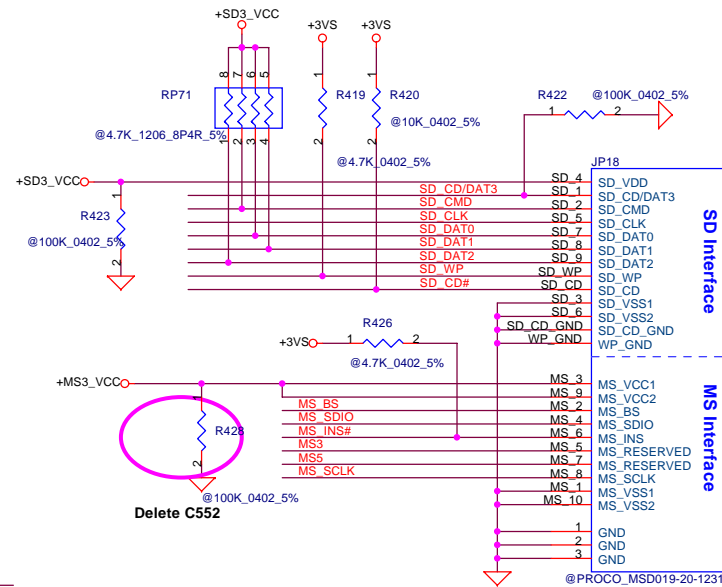
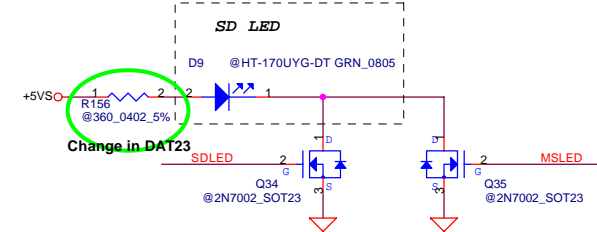
Pin 2 HIGH PIN 6, 20 ACTIVE  
LOW PIN 5, 23 ACTIVE



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Frequency depend on data access.



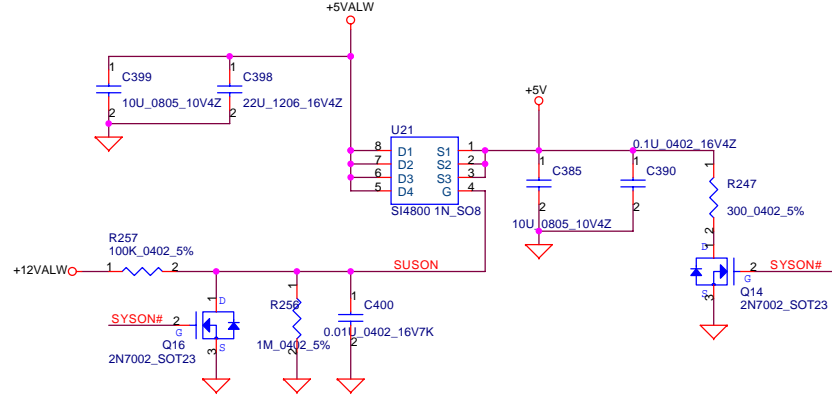
Compal Electronics, Inc.

Title			MS/SD/MMC Winbond W83L518D
Size	Document Number	Rev	0.3
Custom	DAT20 LA-1971		
Date:	Friday, September 26, 2003	Sheet	32 of 42

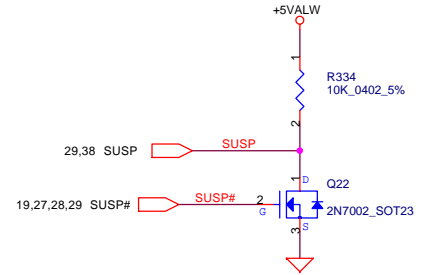
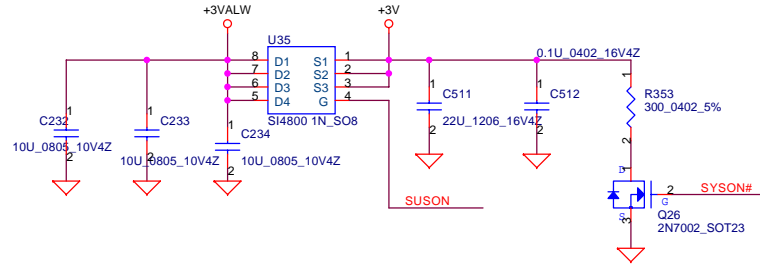
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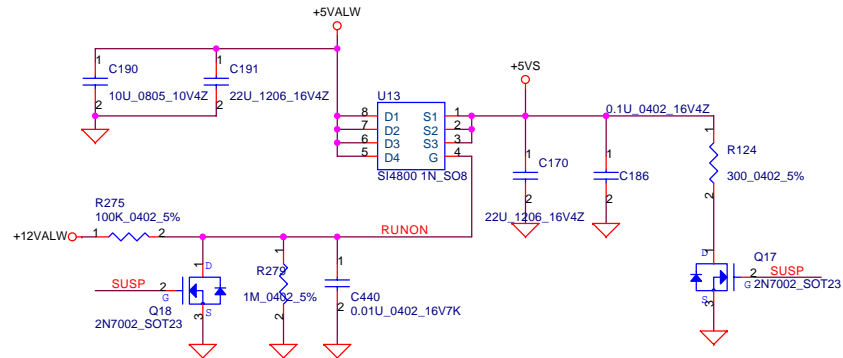
**+5VALW to +5V Transfer**



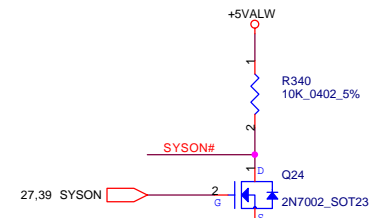
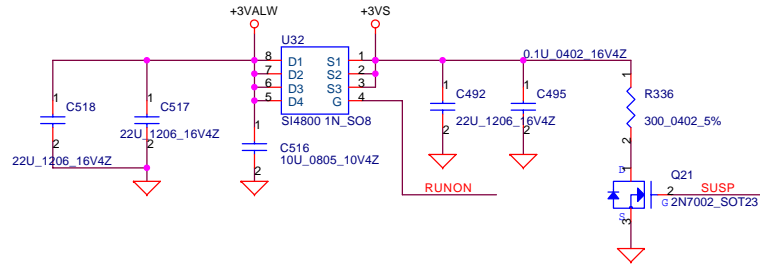
**+3VALW to +3V Transfer**



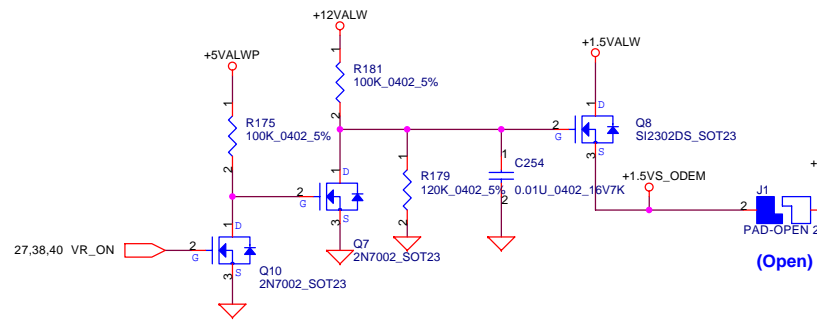
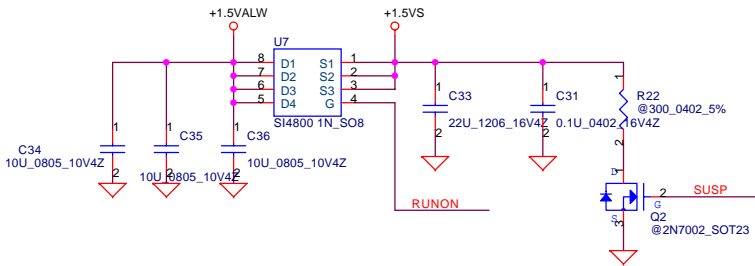
**+5VALW to +5VS Transfer**



**+3VALW to +3VS Transfer**



**+1.5VALW to +1.5VS Transfer**

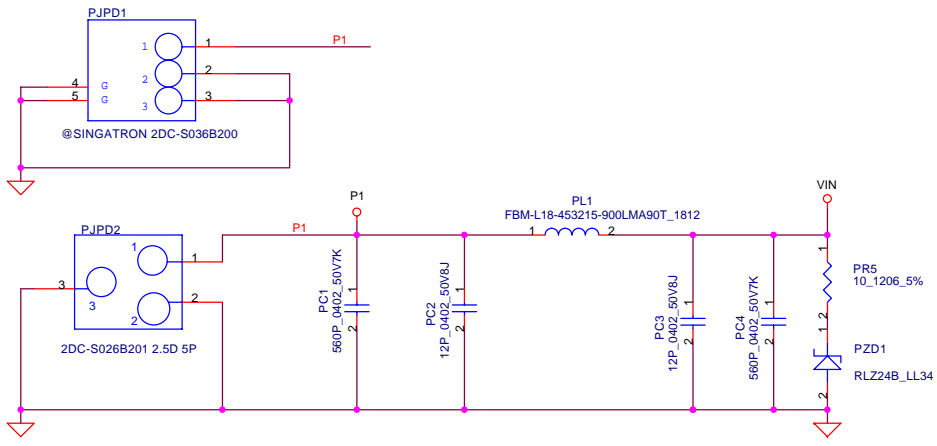


(Open)

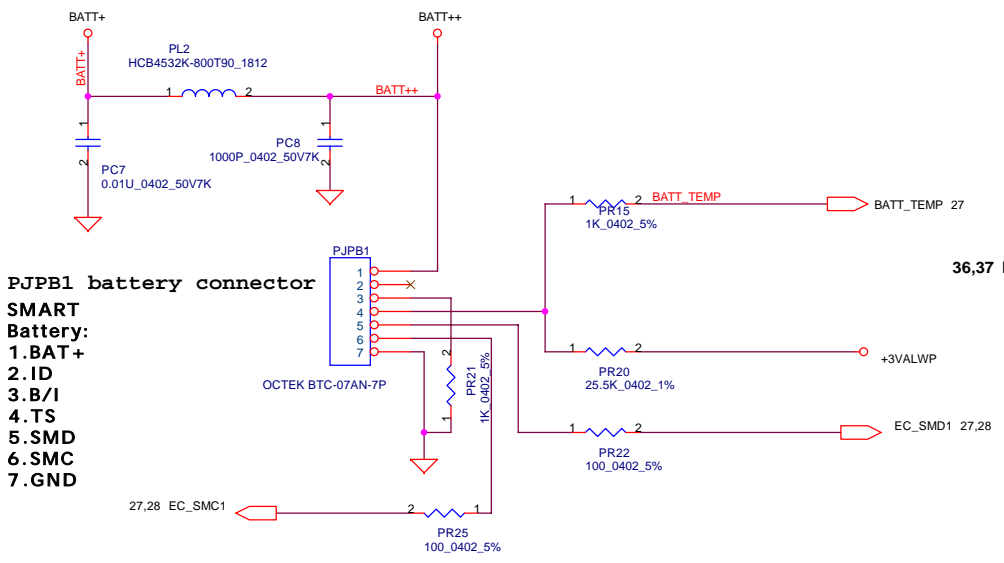
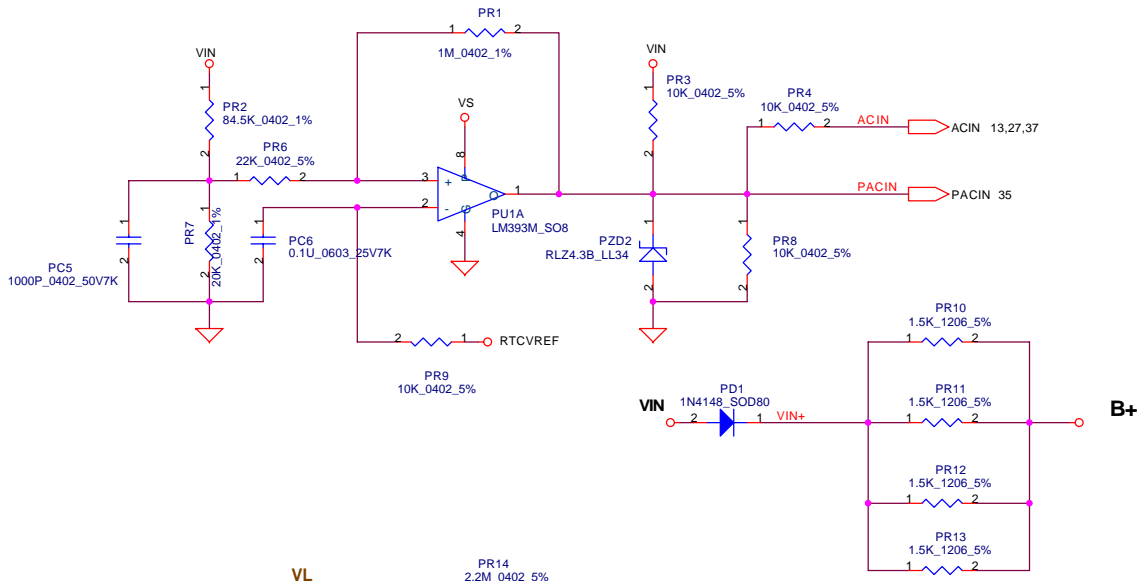
**Compal Electronics, Inc.**

Title		
DC/DC Circuit Interface		
Size	Document Number	Rev
Custom	DAT20 LA-1971	0.3
Date:	Friday, September 26, 2003	Sheet 33 of 42

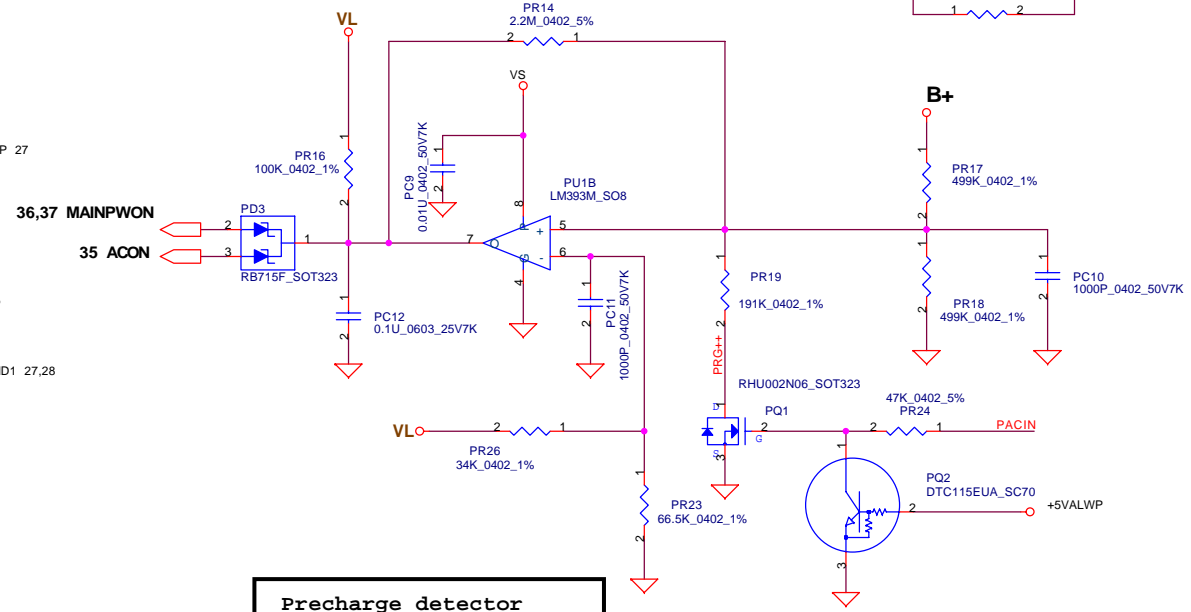
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**Vin Detector  
17.90V/17.24V**



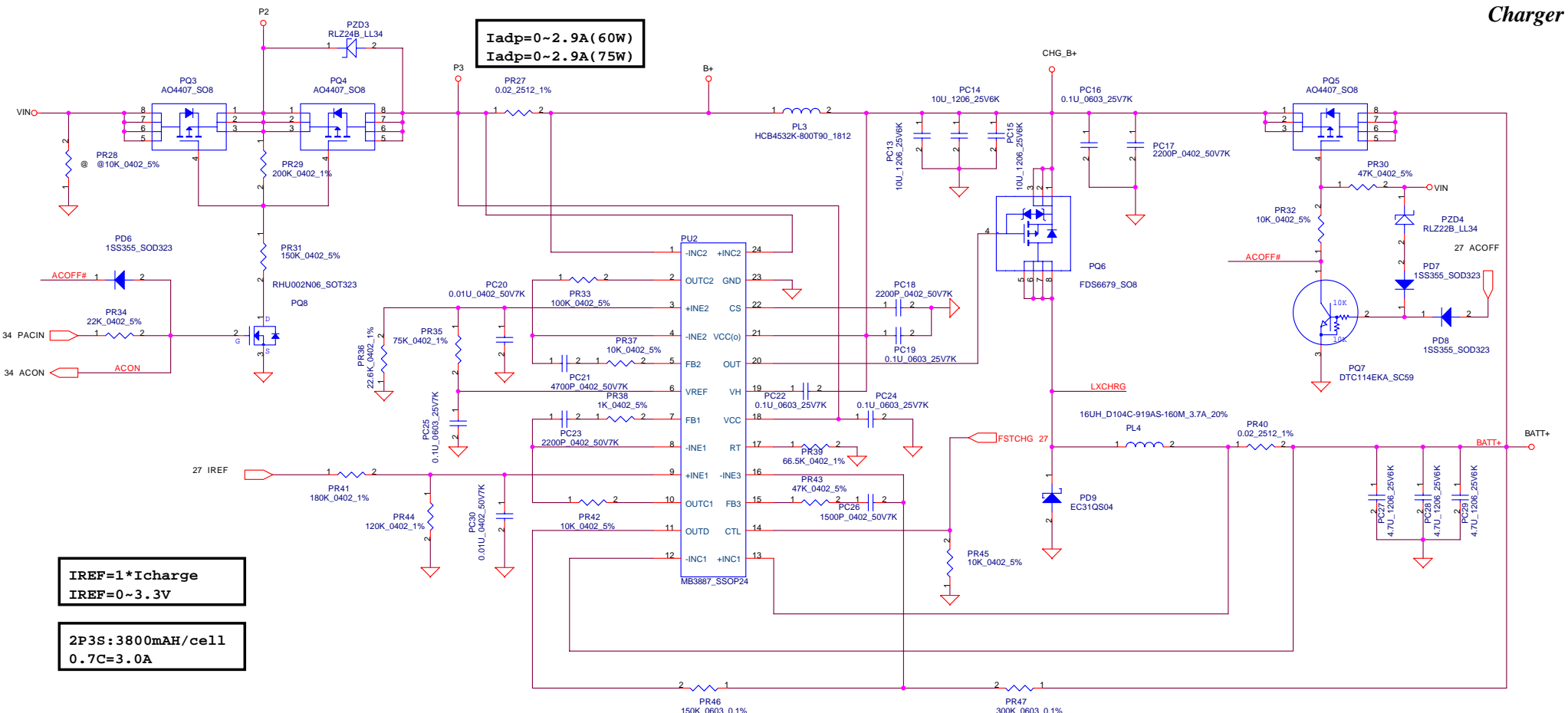
**Precharge detector  
15.97V/14.84V For ADAPTOR**



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<b>Compal Electronics, Inc.</b>		
<b>DCIN &amp; DETECTOR &amp; Precharge</b>		
Size	Document Number	Rev
Custom	<b>DAT20 LA-1971</b>	0.3
Date:	Friday, September 26, 2003	Sheet 34 of 42

**I<sub>adp</sub>=0~2.9A (60W)**  
**I<sub>adp</sub>=0~2.9A (75W)**

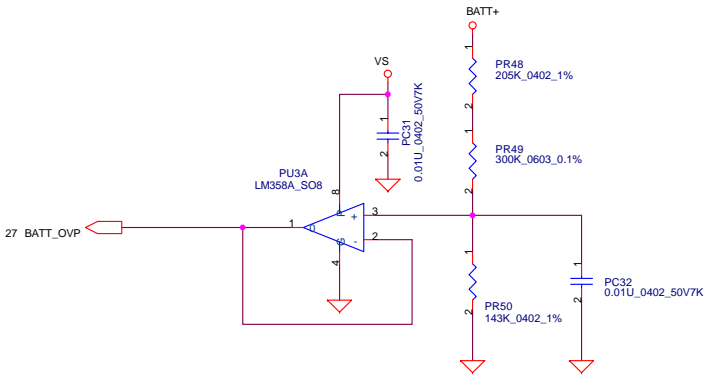


**IREF=1\*I<sub>charge</sub>**  
**IREF=0~3.3V**

**2P3S:3800mAh/cell**  
**0.7C=3.0A**

**OVP voltage :**  
**LI-3S :12.9V---BATT-OVP=2.84V**  
**BATT-OVP=0.2206\*BATT+**

**Charge voltage**  
**3S CC-CV MODE : 12.6V**

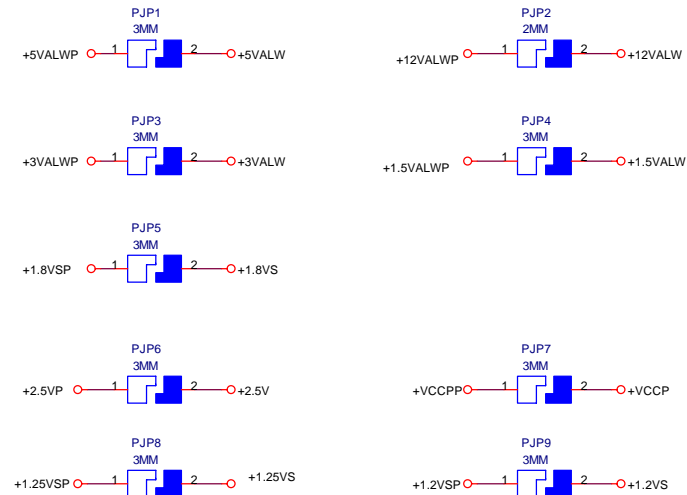
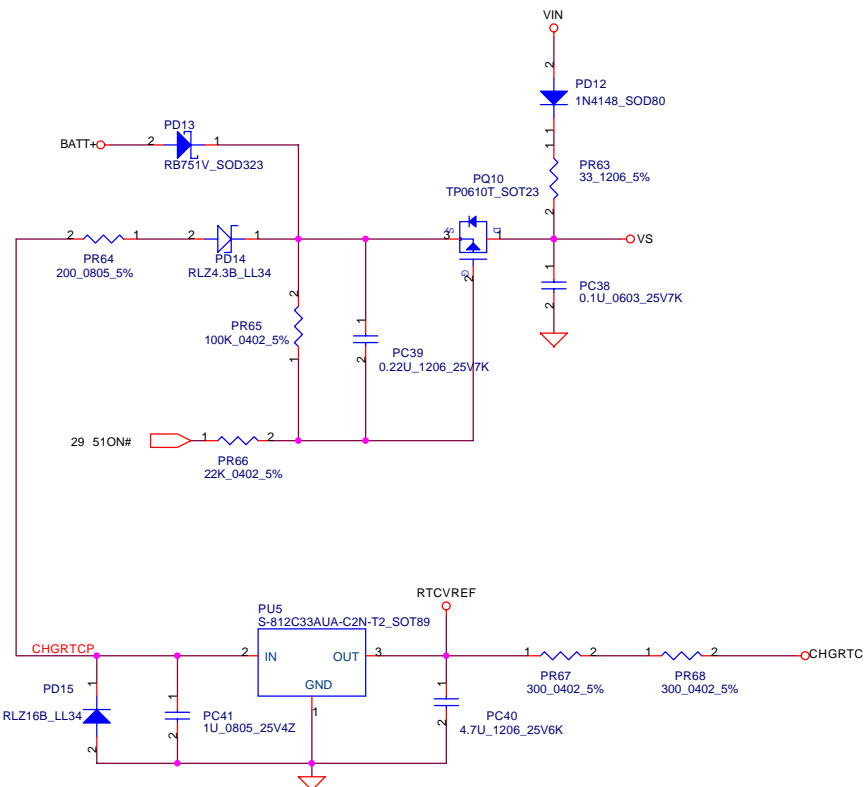
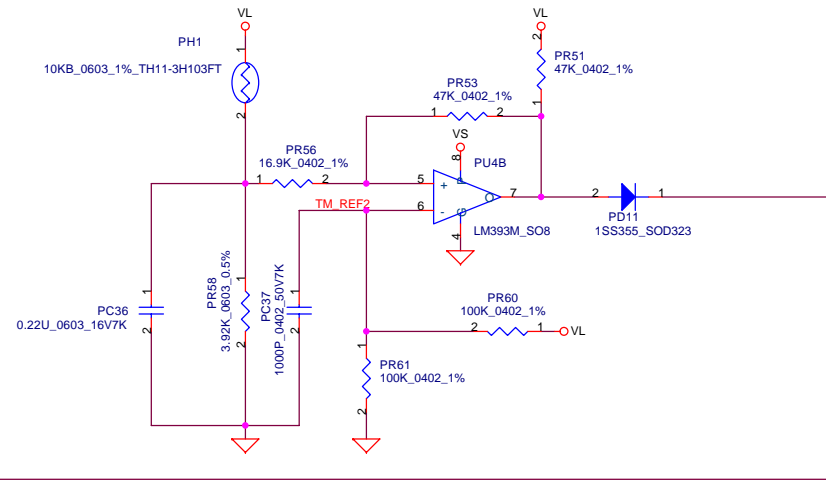
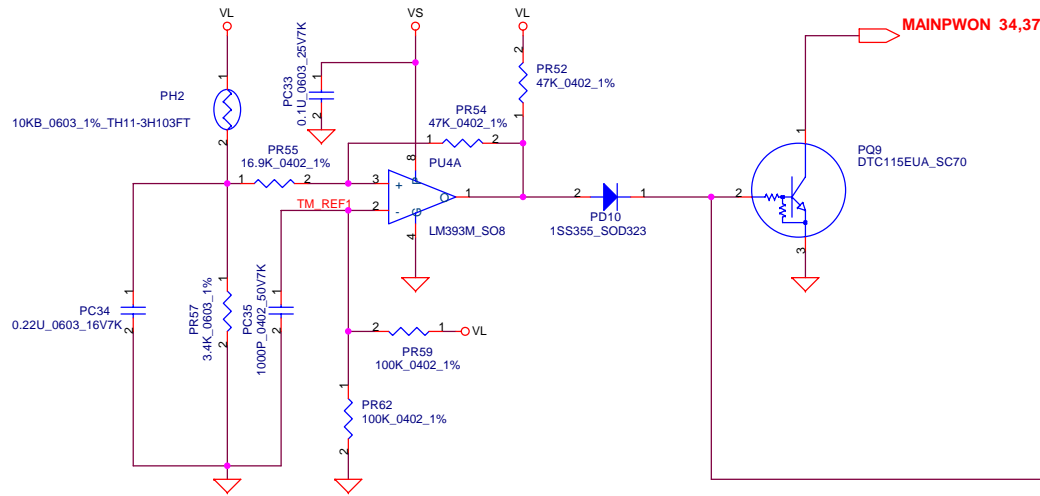


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Compal Electronics, Inc.		
Title	Charger	
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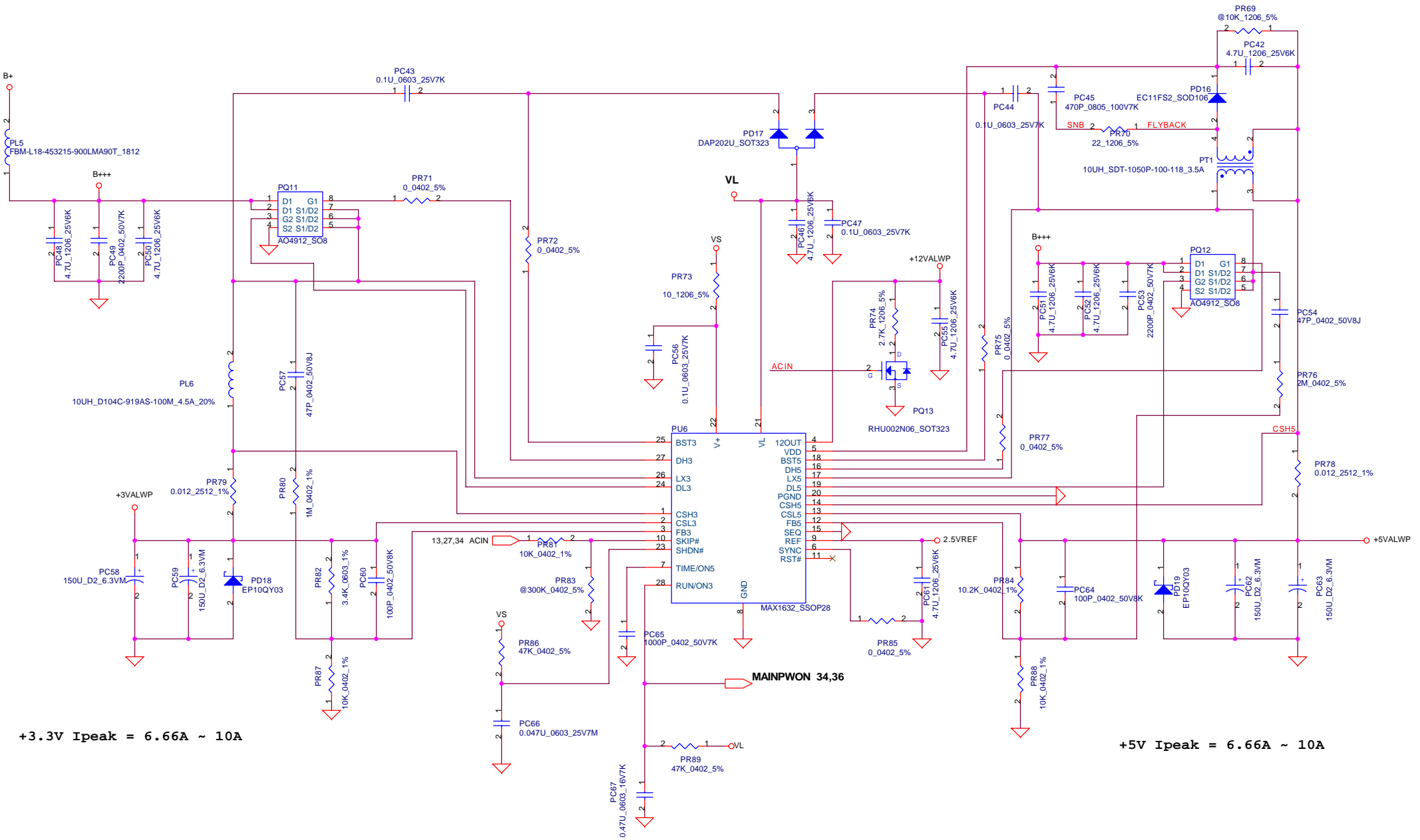
**PH1 under CPU botten side :**  
 CPU thermal protection at 85 degree C  
 Recovery at 44(45) degree C

**PH2 near main Battery CONN :**  
 BAT. thermal protection at 78 degree C  
 Recovery at 39(40) degree C



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<b>RTC Battery &amp; OTP</b>		
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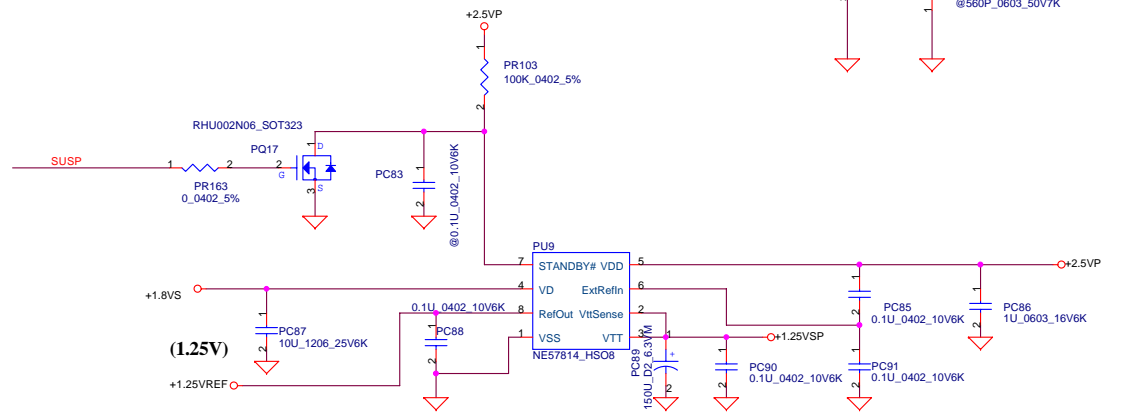
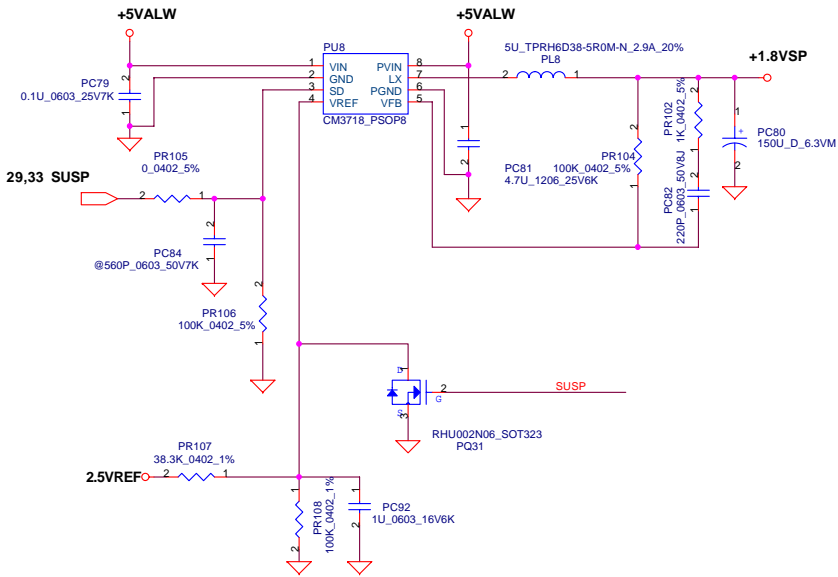
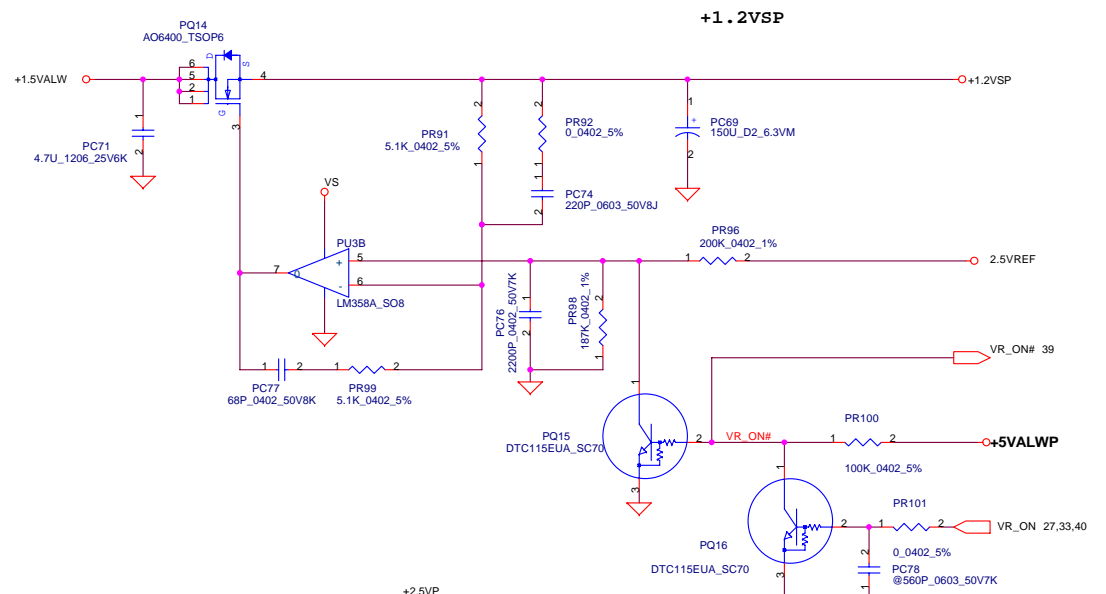
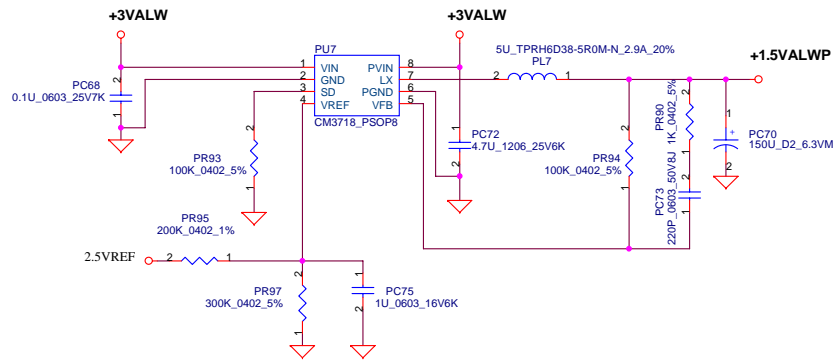


**+3.3V Ipeak = 6.66A ~ 10A**

**+5V Ipeak = 6.66A ~ 10A**

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<b>Compal Electronics, Inc.</b>			
Title: <b>+5VALWP / +3VALWP / +12VALWP</b>			
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<b>Compal Electronics, Inc.</b>			
<b>+1.8VSP &amp; +1.25VSP &amp; 1.5VALWP &amp; +1.2VSP</b>			
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# DAT20 PIR LIST

## HW PIR LIST

### EVT -> DVT

[Page 7 & 9] Change Material R33, R34, R200, R201 (75\_0603\_1%)

[Page 14] Change Material R38 (20\_0603\_1%)

[Page 16] Change Material U40

[Page 24] Modify R374 connected from +3VALW to +3V & delete R384 (Remove TPM detect function)

[Page 25] Delete RP65 & R260 which reserved for LPC47N227

[Page 26] Change SLCTIN# connection.

[Page 27] Change R308 from 0\_0402\_5% to 8.2K\_0402\_5% for DVT test AD\_BID0

[Page 29] Change material for C526 from 1U\_0603\_10V4Z to 1U\_0603\_10V6K

Add C556 2200P\_0402\_50V7K

Add C557, C558 1000P\_0402\_50V7K

[Page 30] Add L10

Change C84 from 4.7U\_0805\_10V4Z to 10U\_0805\_10V4Z

Add C555 10U\_0805\_10V4Z

Delete C184, C179 1U\_0603\_10V4Z

[Page 32] R156 from 390\_0402\_5% to 360\_0402\_5%

[Page 27] R409 from 10K\_0402\_5% to 47K\_0402\_5% & add C559 0.1U\_0402\_16V4Z

### DVT -> PVT

[Page 12] Delete C70, C80, C166, C167, C168

[Page 24] Delete R2 (Reserved for FIR)

[Page 31] Delete C476, C531, R319, R371 AudioHigh pass filter.

**Compal Electronics, Inc.**

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DAT20 PIR LIST		
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	M/B cannot power on.	RC delay time is not enough of Max1632 on3 pin.	0.2	34	1.Change PC67 from 0.047U_0805_10V6K to 0.47U_16V K X7R 0603.	0.2	DVT
2	Layout symbol error.	Layout symbol error.	0.2	37	1.Change PR26 PCB footprint from R_0603 to R_0402.	0.2	DVT
3	Layout symbol error.	Layout symbol error.	0.2	40	1.Change PD22 from EP10QY03 to EP31QS04.	0.2	DVT
4	System cannot re-start and Windows fail when into C4.	The CPU cannot into skip mode,happen the OVP when C4.	0.2	40	Swap the PR154 and PR155.	0.2	DVT
5	Rating not enough.	Rating not enough.	0.2	34	1.Change PC66 from 0.047U_00603_16V7K to 0.047U_00603_25V7M.	0.2	DVT
6.	Rating is not enough.	Surge power rating concerned.	0.2	39	1.Change PR109 from 10_0603 to 10_1206.	0.2	DVT
7.	Change size.	Change size.	0.2		1.Change PR149,PR44,PR48,PR82,PR36,PR107,PR39,PR121, PR140,PR145 and PR146 from 0603 to 0402.	0.2	DVT
8.	Change size.	Change size.	0.2		1.Change PC114,PC131,PC49,PC21,PC53,PC128,PC126,PC124,PC31, PC7 and PC9 from 0603 to 0402.	0.2	DVT
9.	Change size.	Change size.	0.2		1.Change PC56,PC24,0C38,PC100,PC16 and PC19 from 0805 to 0603.	0.2	DVT
10.	Choke rating is not enough.	Charge current power rating concerned.	0.2	35	1.Change PL4 from 22UH to 16UH.	0.2	DVT
11.	Application of CM3718 has overshoot issue during system on.	Charge control signal SHDN# to reference.	0.2	38	1.Add PQ31.	0.2	DVT
12.	EMI issue of charger.	EMI issue of charger.	0.3	35	1.Change PQ6 from AO4407 to FDS6679. Add the PR164 on GATE pin of PQ6.	0.3	PVT
13.	EMI issue of CPU_CORE.	EMI issue of CPU_CORE.	0.3	40	1.Change PQ21 and PQ25 from IRF7821 to IRF7811A. Add the 2200P on PC134 and PC135.	0.3	PVT
14.							

<b>Compal Electronics, Inc.</b>		
Title <b>PWR-PIR</b>		
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