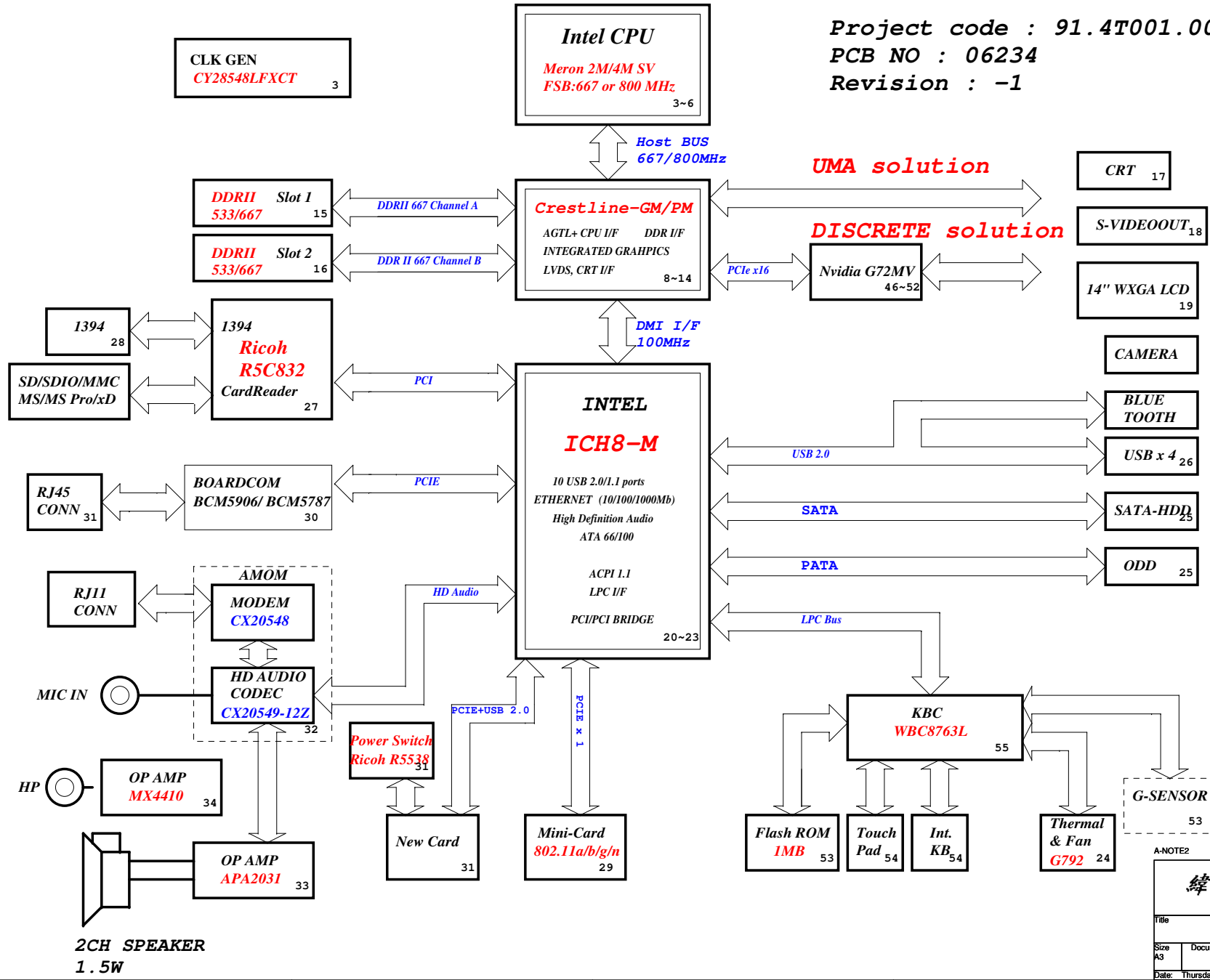


Anote2.0 Block Diagram

Project code : 91.4T001.001
 PCB NO : 06234
 Revision : -1



SYSTEM DC/DC TPS51120 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3D3V_S5
SYSTEM DC/DC ISL6268CAZ 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
SYSTEM DC/DC TPS51116 40	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 0D9V_S0
CHARGER ISL6255	
INPUTS	OUTPUTS
DCBATOUT	BT+ 20V 3.0A 5V 100mA
CPU DC/DC ISL6262ACRZ 36, 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
PCB LAYER	
L1: Signal 1	
L2: VCC	
L3: Signal 2	
L4: Signal 3	
L5: GND	
L6: Signal 4	

2CH SPEAKER
 1.5W

A-NOTE2

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Title: **Block Diagram**

Size A3 Document Number: **Anote2.0 INTEL** Rev: **-1**

Date: Thursday, March 22, 2007 Sheet 1 of 56

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Config Registers: offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC (Config Registers: Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC (Config Registers: Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN. NOTE: This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCLI_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCLI_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCLI_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05, VccCLI_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL. Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR (Device28: Function0: Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. (Offset: 3410h: bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up. If sampled low, the Flash Descriptor Security will be overridden. If high, the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

ICH_RSVD#p3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (default)
1	1	Set PCIe port config bit1

PCI_GNT#3	low = A16 swap override enable	high = default
0	1	SPT
1	0	PCT
1	1	LPC (Default)

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC (Default)

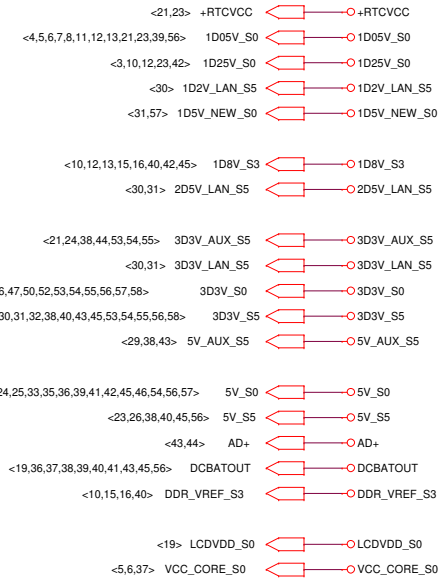
SM_INTVRMEN	High=Enable	Low=Disable
LAN100_SLP	High=Enable	Low=Disable

No Reboot Strap	LOW = Defaule	High=No Reboot
SPKR	LOW = Defaule	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal ★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode (lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIe	Only PCIe or SDVO is operation ★	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13 LH(0)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HL(11)	Normal Operation	

A-NOTE2

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Title Table of Content	
Size A3	Document Number Anote2.0 INTEL
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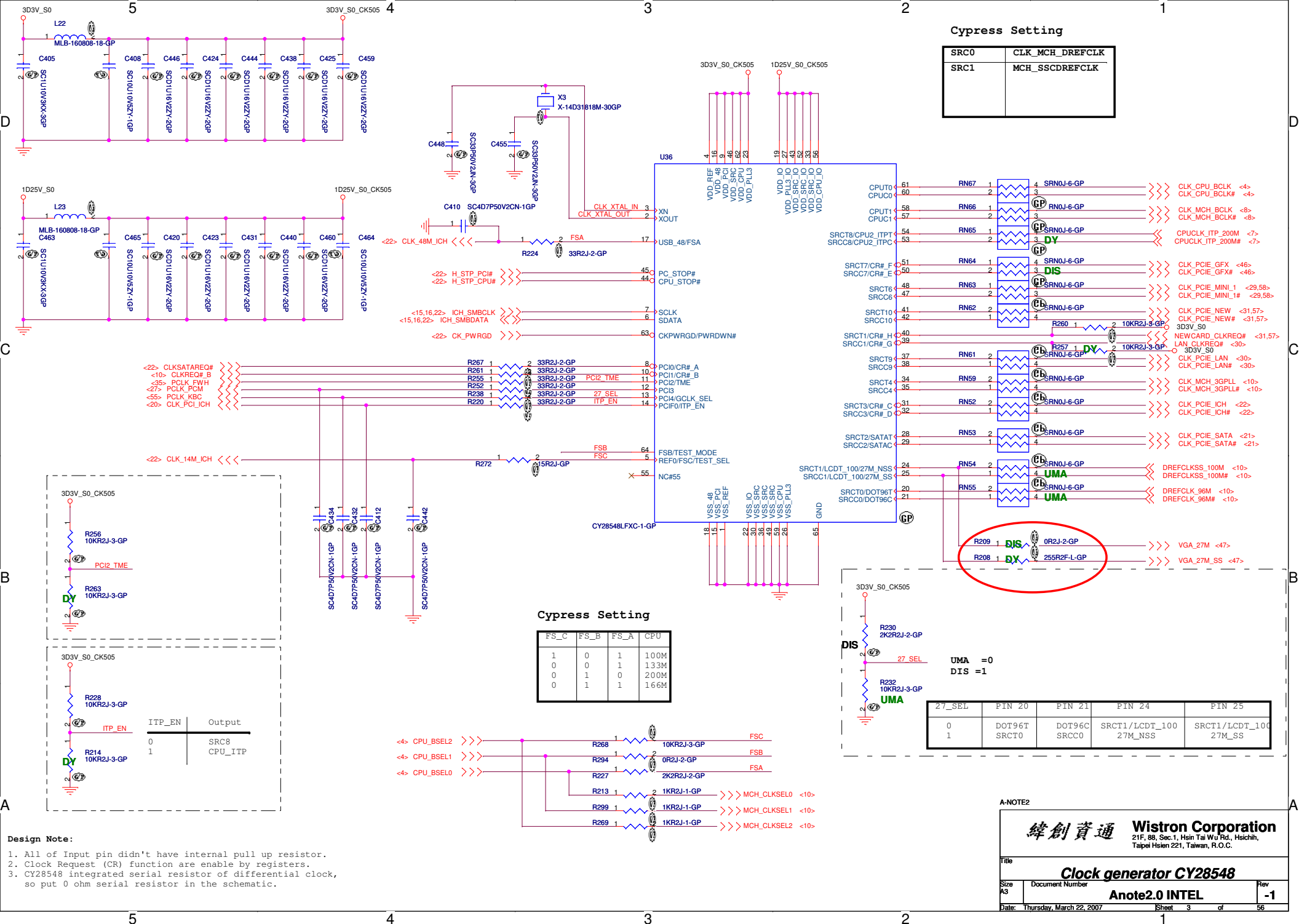
A

B

C

D

E



Cypress Setting

SRC0	CLK_MCH_DREFCLK
SRC1	MCH_SSCDREFCLK

Cypress Setting

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T SRCT0	DOT96C SRCC0	SRCT1/LCDT_100 27M_NSS	SRCT1/LCDT_100 27M_SS
1				

A-NOTE2

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Clock generator CY28548

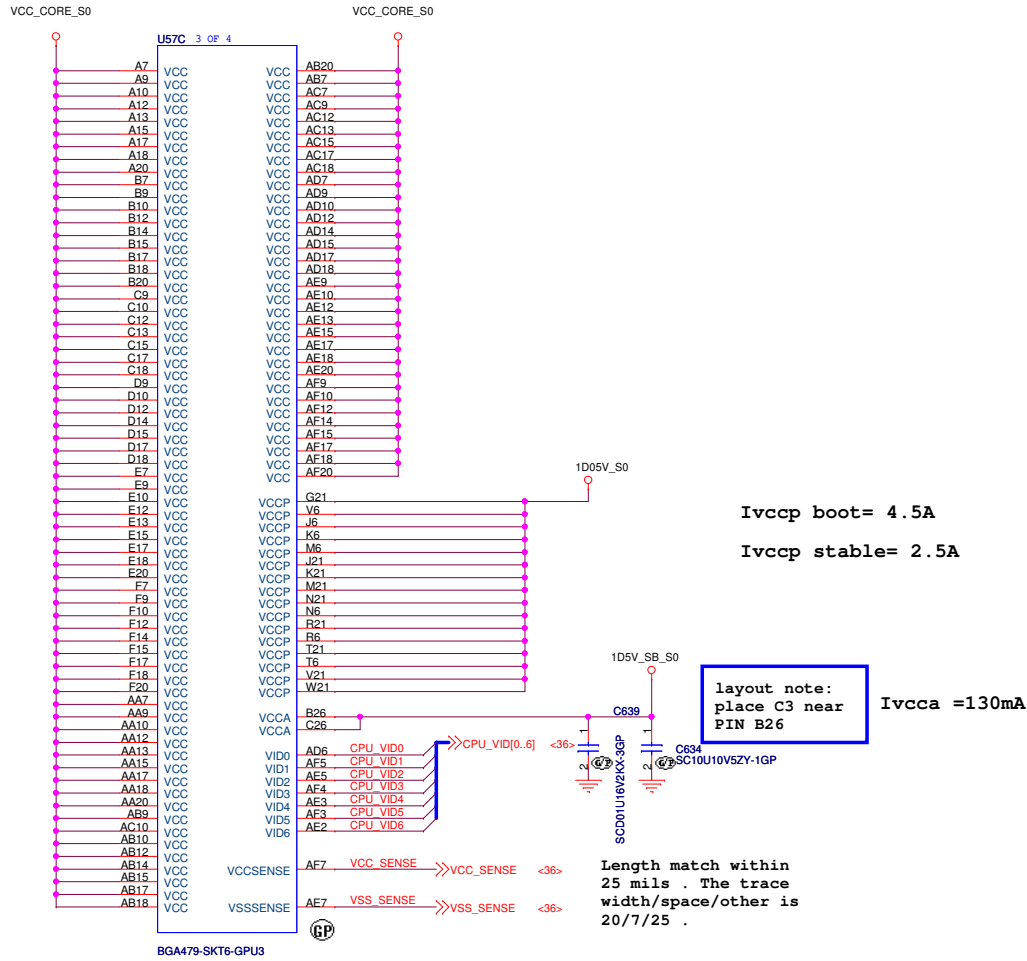
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Size A3 Document Number _____ Rev -1

Date: Thursday, March 22, 2007 Sheet 3 of 56

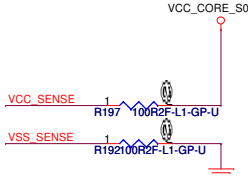
Design Note:

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.



layout note:
place C3 near
PIN B26

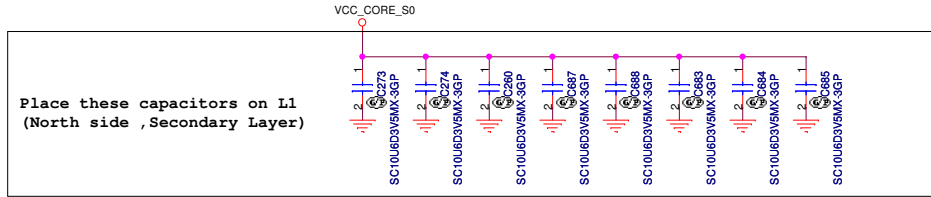
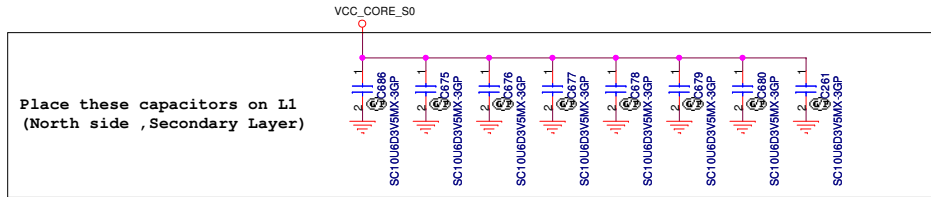
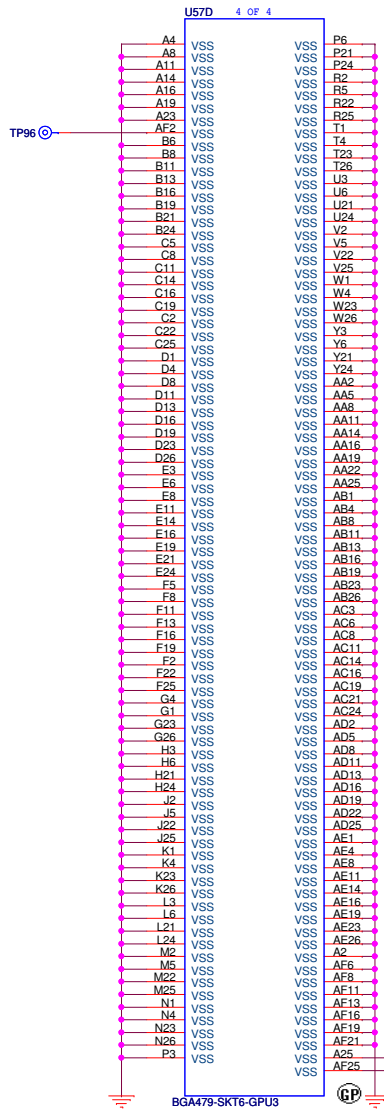
Length match within
25 mils . The trace
width/space/other is
20/7/25 .



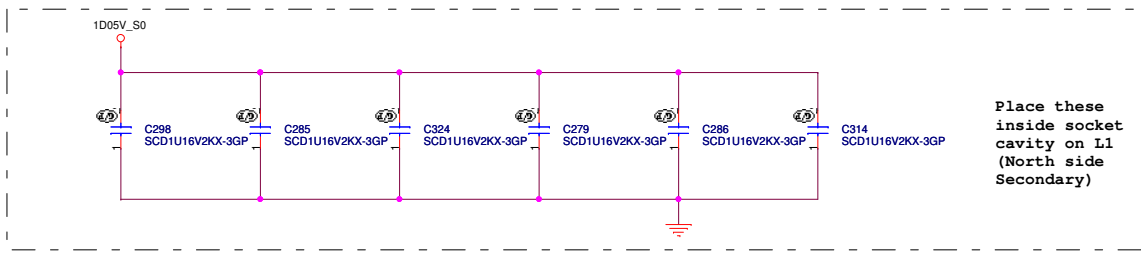
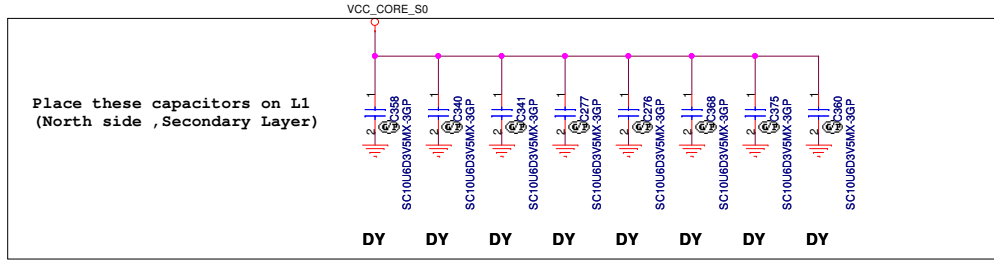
Close to CPU pin
within 500mils

A-NOTE2

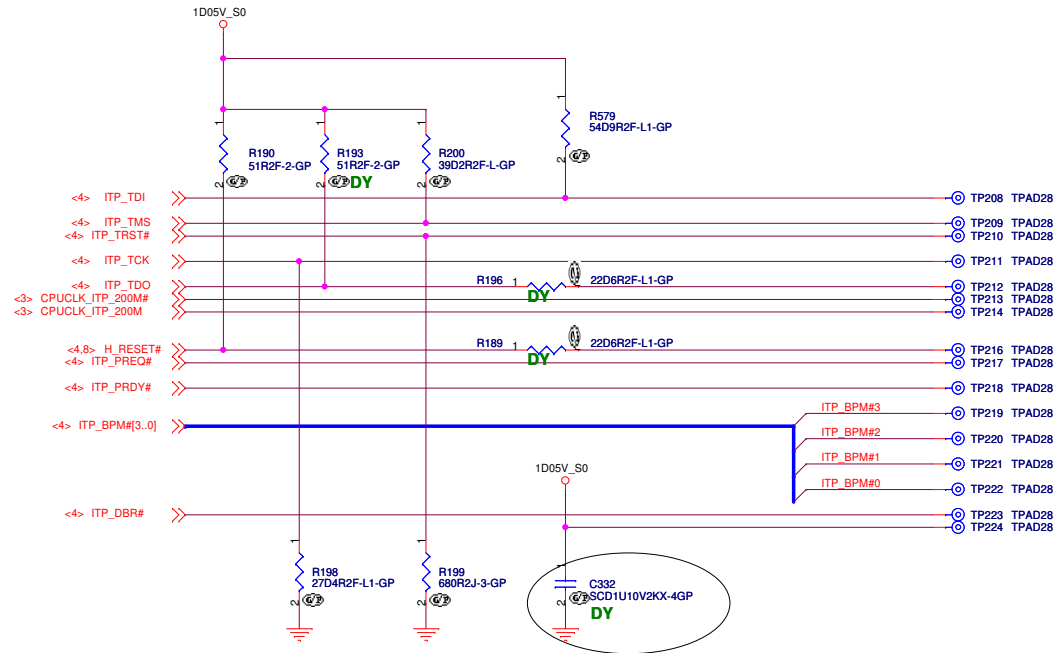
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Title			
Meron(2/3)-AGTL+/PWR			
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Mid Freqeuncd Decoupling



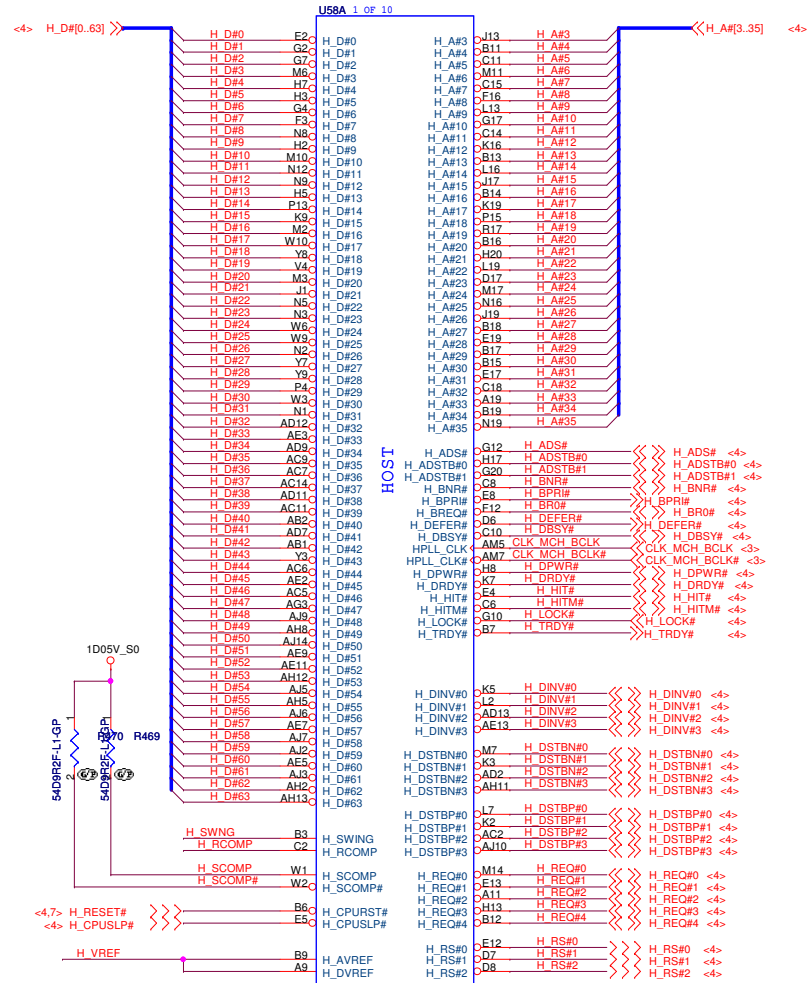
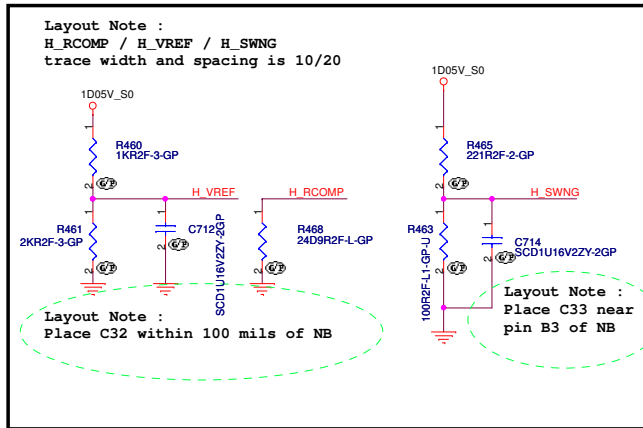
ITP Connector



A-NOTE2

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Meron(3/3)-GND&Bypass	
Size A3	Document Number Anote2.0 INTEL
Date: Thursday, March 22, 2007	Rev -1

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



<< >> DDR_A_D[0..63] <15>
 << >> DDR_A_BS[0..2] <15>
 << >> DDR_A_DM[0..7] <15>
 << >> DDR_A_DQS[0..7] <15>
 << >> DDR_A_DQS#[0..7] <15>
 << >> DDR_A_MA[0..14] <15>

<< >> DDR_B_D[0..63] <16>
 << >> DDR_B_BS[0..2] <16>
 << >> DDR_B_DM[0..7] <16>
 << >> DDR_B_DQS[0..7] <16>
 << >> DDR_B_DQS#[0..7] <16>
 << >> DDR_B_MA[0..14] <16>

US80 4 OF 10

DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS# >>> DDR_A_CAS# <15>
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1
DDR A D8	BB45	SA_DQ8	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ11	SA_DM5	EG38	DDR A DM5
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D20	BE44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D21	BH45	SA_DQ21	SA_DQS6	B22	DDR A DQS6
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D23	BF40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0
DDR A D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR A DQS#1
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2
DDR A D26	AT39	SA_DQ26	SA_DQS#3	BA37	DDR A DQS#3
DDR A D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR A DQS#4
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D36	AU15	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D43	EG10	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D44	AY9	SA_DQ44	SA_MA12	BJ16	DDR A MA12
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ29	DDR A MA13
DDR A D46	BD7	SA_DQ46	SA_MA14		
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS# >>> DDR_A_RAS# <15>
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA RCVEN# TP36
DDR A D50	AT5	SA_DQ50	SA_WE#	BA19	DDR A WE# >>> DDR_A_WE# <15>
DDR A D51	AT7	SA_DQ51			
DDR A D52	AY6	SA_DQ52			
DDR A D53	BE7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR8	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AN8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AN9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

CRESTLINE-GP-U

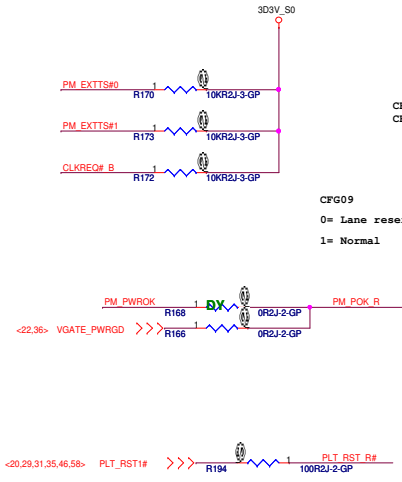
US8E 5 OF 10

DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS# >>> DDR_B_CAS# <16>
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	BB50	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BF50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AU50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BJ41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BF2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BQ25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BF25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BQ28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BK5	SB_DQ42	SB_MA10	BG17	DDR B MA10
DDR B D43	BL5	SB_DQ43	SB_MA11	BA39	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BE37	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BF4	SB_DQ48	SB_RAS#	AV16	DDR B RAS# >>> DDR_B_RAS# <16>
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB RCVEN# TP46
DDR B D50	BG1	SB_DQ50	SB_WE#	BC17	DDR B WE# >>> DDR_B_WE# <16>
DDR B D51	BC2	SB_DQ51			
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AG1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

CRESTLINE-GP-U

A-NOTE2

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.		
Title		
CRESTLINE(2/7)-DDR2 A/B CH		
Size	Document Number	Rev
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CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

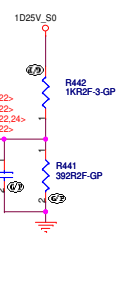
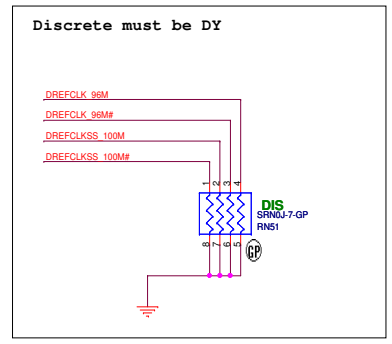
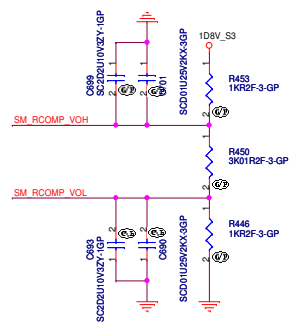
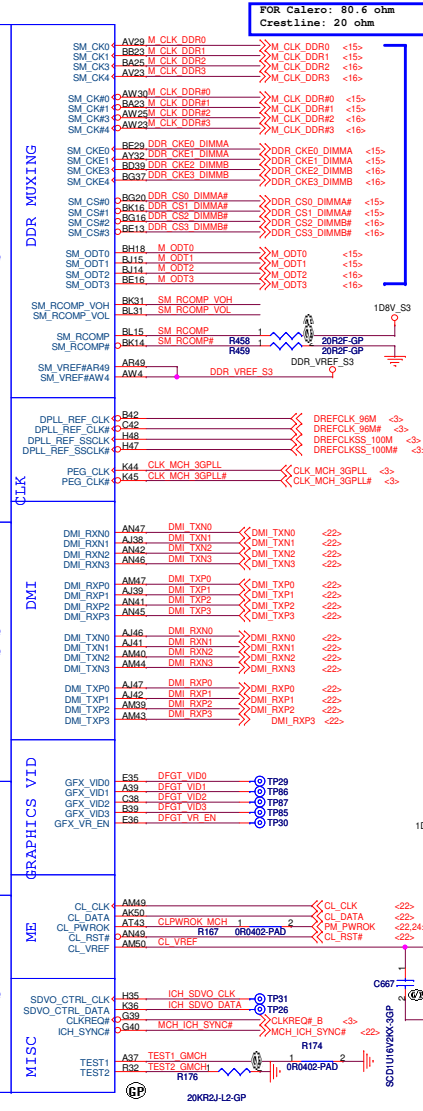
From Astro demo schematic

R188 20R2J-2-GP
DY

CFG09
0= Lane reserved
1= Normal

U68B 2 of 10

X P36	RSVDHP36	SM_CK0	AV29 M_CLK_DDR0	>>>	CLK_DDR0	<-15>
X P47	RSVDHP37	SM_CK1	B823 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X P48	RSVDHP38	SM_CK2	B424 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X N45	RSVDHP35	SM_CK3	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R12	RSVDHP35	SM_CK4	AW30 M_CLK_DDR0	>>>	CLK_DDR0	<-15>
X R13	RSVDHP36	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R14	RSVDHP37	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R15	RSVDHP38	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R16	RSVDHP39	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R17	RSVDHP40	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R18	RSVDHP41	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R19	RSVDHP42	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R20	RSVDHP43	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R21	RSVDHP44	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R22	RSVDHP45	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R23	RSVDHP46	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R24	RSVDHP47	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R25	RSVDHP48	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R26	RSVDHP49	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R27	RSVDHP50	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R28	RSVDHP51	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R29	RSVDHP52	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R30	RSVDHP53	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R31	RSVDHP54	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R32	RSVDHP55	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R33	RSVDHP56	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R34	RSVDHP57	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R35	RSVDHP58	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R36	RSVDHP59	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R37	RSVDHP60	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R38	RSVDHP61	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R39	RSVDHP62	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R40	RSVDHP63	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R41	RSVDHP64	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R42	RSVDHP65	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R43	RSVDHP66	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R44	RSVDHP67	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R45	RSVDHP68	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R46	RSVDHP69	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R47	RSVDHP70	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R48	RSVDHP71	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R49	RSVDHP72	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R50	RSVDHP73	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R51	RSVDHP74	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R52	RSVDHP75	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R53	RSVDHP76	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R54	RSVDHP77	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R55	RSVDHP78	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R56	RSVDHP79	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R57	RSVDHP80	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R58	RSVDHP81	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R59	RSVDHP82	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R60	RSVDHP83	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R61	RSVDHP84	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R62	RSVDHP85	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R63	RSVDHP86	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R64	RSVDHP87	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R65	RSVDHP88	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R66	RSVDHP89	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R67	RSVDHP90	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R68	RSVDHP91	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R69	RSVDHP92	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R70	RSVDHP93	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R71	RSVDHP94	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R72	RSVDHP95	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R73	RSVDHP96	SM_CK0	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R74	RSVDHP97	SM_CK1	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>
X R75	RSVDHP98	SM_CK2	AW23 M_CLK_DDR3	>>>	CLK_DDR3	<-16>
X R76	RSVDHP99	SM_CK3	B423 M_CLK_DDR1	>>>	CLK_DDR1	<-15>
X R77	RSVDHP100	SM_CK4	AW20 M_CLK_DDR2	>>>	CLK_DDR2	<-16>



Strap Pin Table

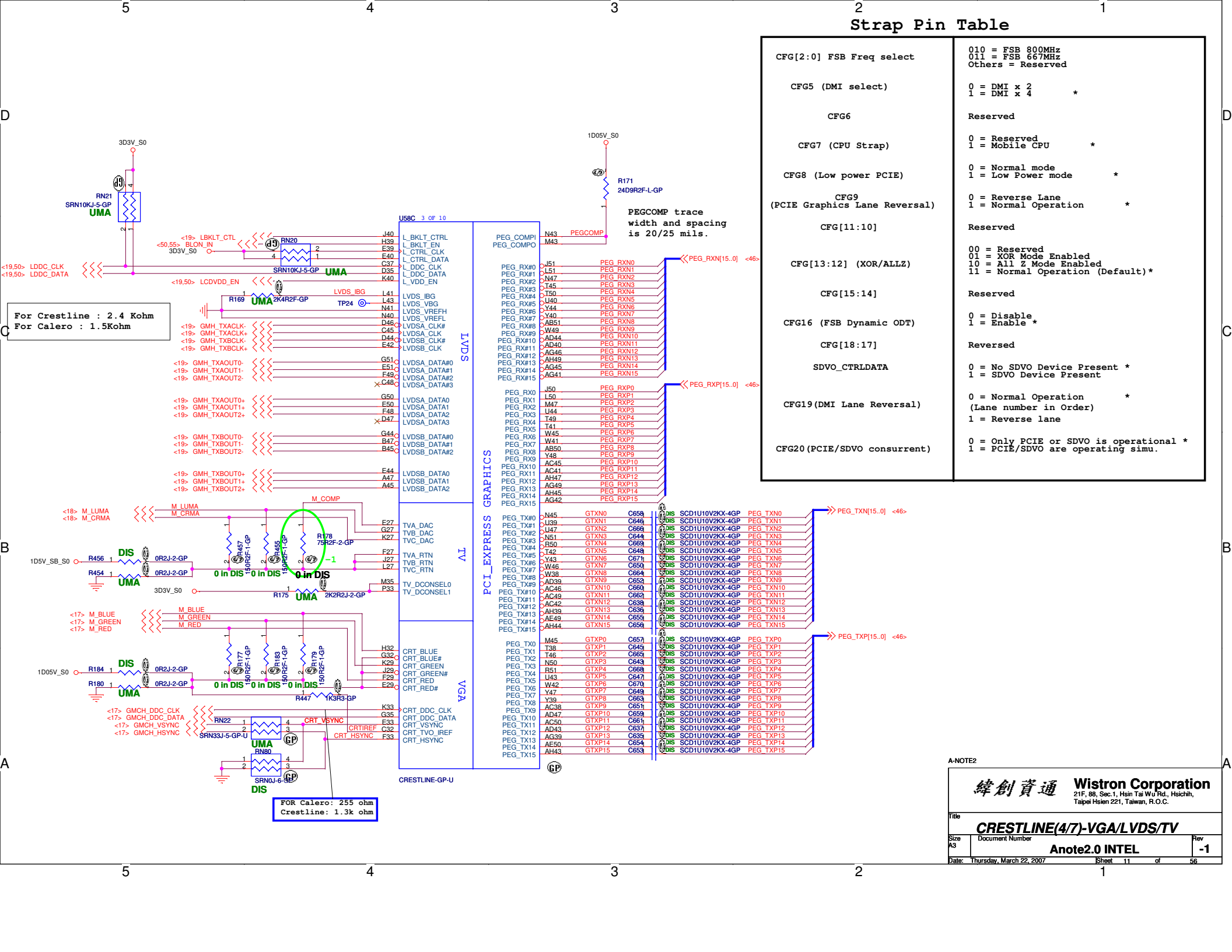
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

D

C

B

A



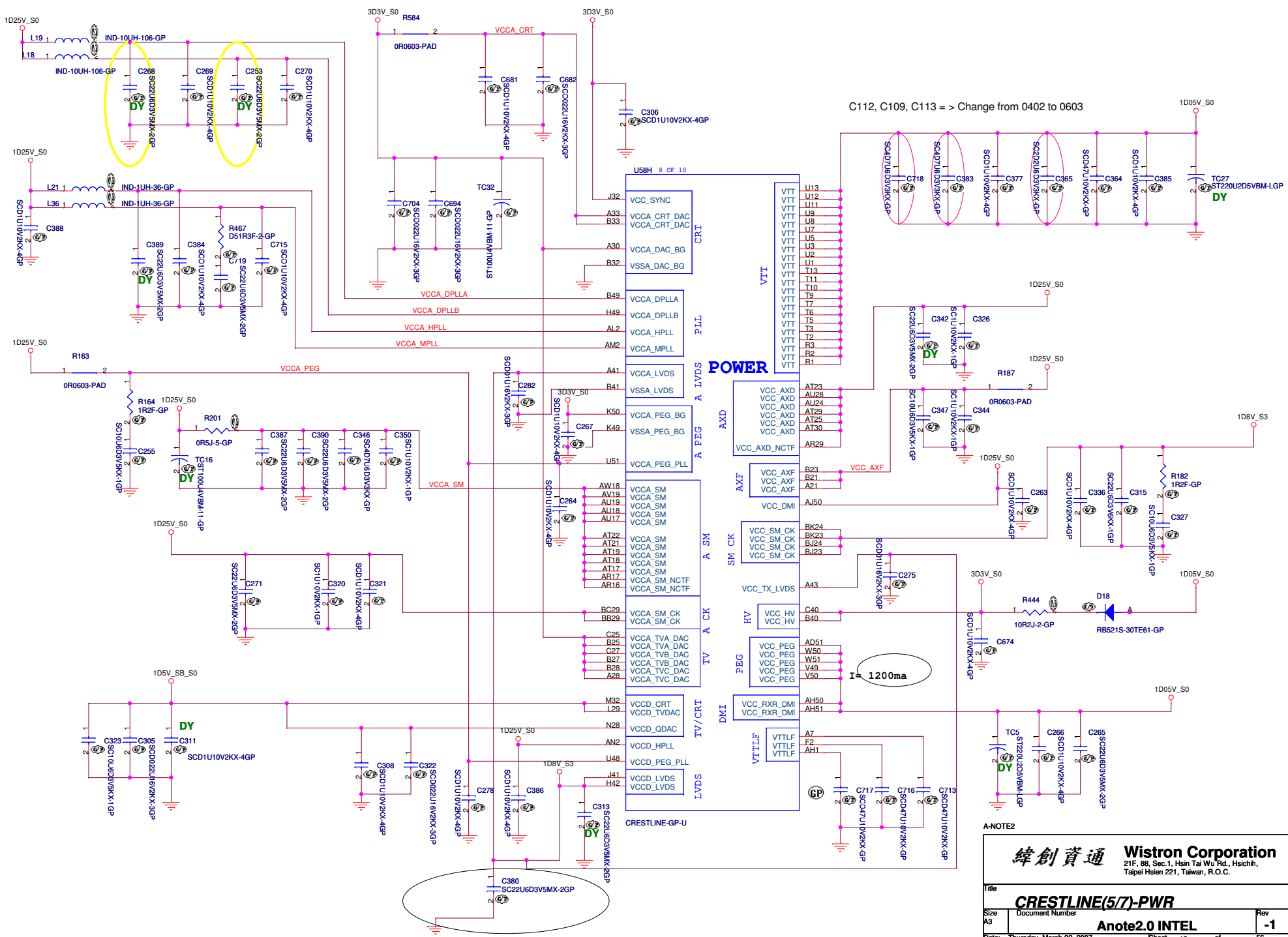
For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

FOR Calero: 255 ohm
Crestline: 1.3k ohm

PEGCOMP trace width and spacing is 20/25 mils.

A-NOTE2

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
Title	
CRESTLINE(4/7)-VGA/LVDS/TV	
Size	Rev
A3	-1
Date:	Sheet
Thursday, March 22, 2007	11 of 56



C112, C109, C113 => Change from 0402 to 0603

POWER

I = 1200ma

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

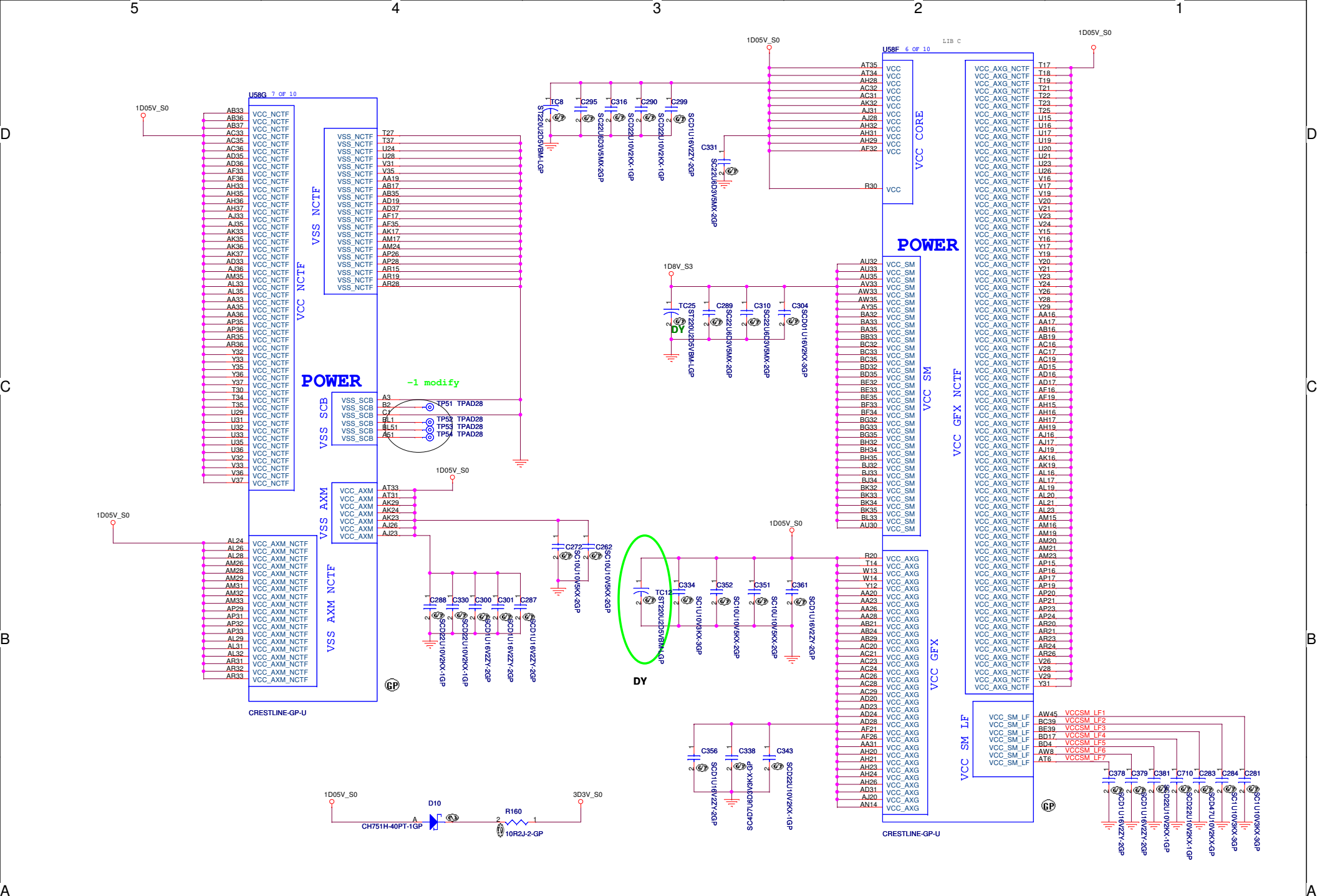
Title: **CRESTLINE(5/7)-PWR**

Size A3 Document Number

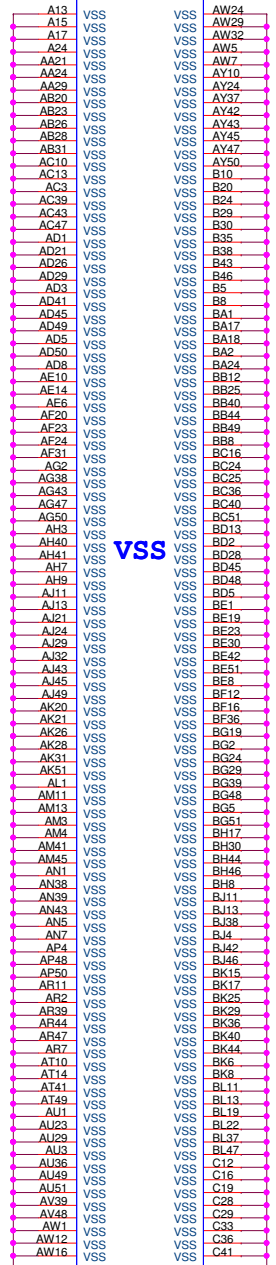
Date: Thursday, March 22, 2007 Sheet 12 of 56

Rev -1

A-NOTE2

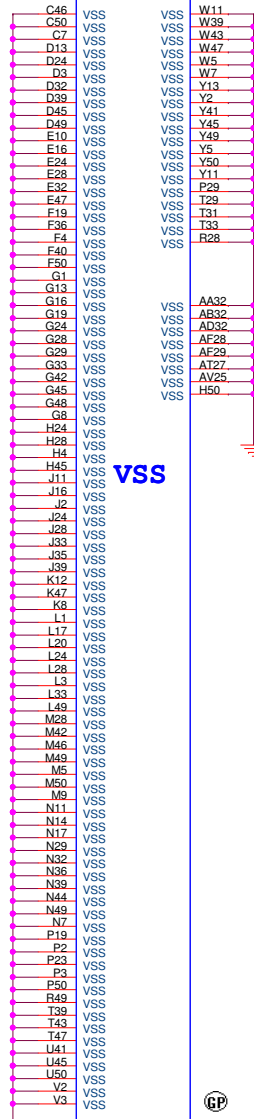


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CRESTLINE-GP-U

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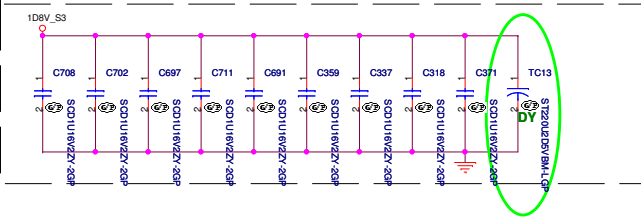
CRESTLINE-GP-U

A-NOTE2

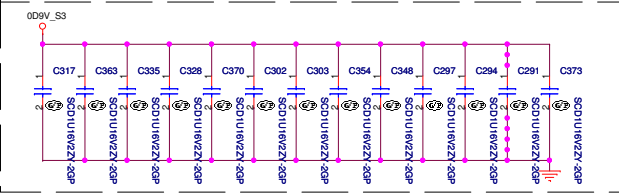
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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
CRESTLINE(7/7)-PWR/GND			
Title			
Size	Document Number	Sheet	Rev
A3		14	-1
Date: Thursday, March 22, 2007			

<-> DDR_A_DQS[0..7] <<>>
 <-> DDR_A_DQ[0..63] <<>>
 <-> DDR_A_DM[0..7] <<>>
 <-> DDR_A_DQS[0..7] <<>>
 <-> DDR_A_MA[0..14] <<>>
 <-> DDR_A_BS[0..2] <<>>

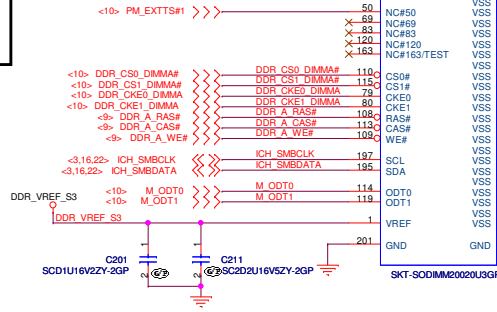
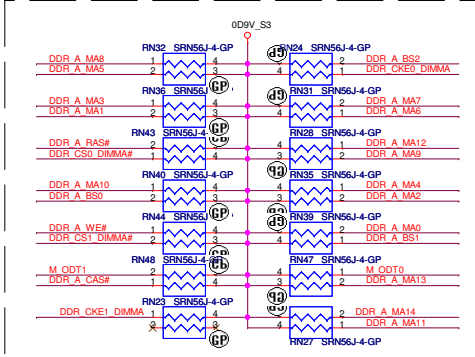
Layout Note:
Place near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"



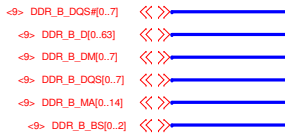
CN21		MH1		MH2		MH2	
DDR A MA0	102	A0		DDR A DQ0	13	DDR A DQ0	
DDR A MA1	101	A1		DDR A DQ1	31	DDR A DQ1	
DDR A MA2	100	A2		DDR A DQ2	51	DDR A DQ2	
DDR A MA3	99	A3		DDR A DQ3	70	DDR A DQ3	
DDR A MA4	98	A4		DDR A DQ4	131	DDR A DQ4	
DDR A MA5	97	A5		DDR A DQ5	148	DDR A DQ5	
DDR A MA6	94	A6		DDR A DQ6	169	DDR A DQ6	
DDR A MA7	92	A7		DDR A DQ7	188	DDR A DQ7	
DDR A MA8	91	A8		DDR A DQS0	11	DDR A DQS0	
DDR A MA9	91	A9		DDR A DQS1	29	DDR A DQS1	
DDR A MA10	105	A10/AP		DDR A DQS2	49	DDR A DQS2	
DDR A MA11	90	A11		DDR A DQS3	68	DDR A DQS3	
DDR A MA12	89	A12		DDR A DQS4	129	DDR A DQS4	
DDR A MA13	116	A13		DDR A DQS5	146	DDR A DQS5	
DDR A MA14	86	A14		DDR A DQS6	167	DDR A DQS6	
DDR A BS2	85	A15		DDR A DQS7	186	DDR A DQS7	
DDR A BS0	107	BA0		DDR A DM0	10	DDR A DM0	
DDR A BS1	106	BA1		DDR A DM1	26	DDR A DM1	
DDR A D0	5	D00		DDR A DM2	62	DDR A DM2	
DDR A D1	7	D01		DDR A DM3	67	DDR A DM3	
DDR A D2	17	D02		DDR A DM4	130	DDR A DM4	
DDR A D3	19	D03		DDR A DM5	147	DDR A DM5	
DDR A D4	14	D04		DDR A DM6	170	DDR A DM6	
DDR A D5	6	D05		DDR A DM7	185	DDR A DM7	
DDR A D6	14	D06		M CLK DDR0	30	M CLK DDR0 <10>	
DDR A D7	16	D07		M CLK DDR#0	32	M CLK DDR#0 <10>	
DDR A D8	23	D08		M CLK DDR1	154	M CLK DDR1 <10>	
DDR A D9	23	D09		M CLK DDR#1	166	M CLK DDR#1 <10>	
DDR A D10	25	D010		SA0	198	SA0	
DDR A D11	37	D011		SA1	200	SA1	
DDR A D12	22	D012		VDD_SPD	199		
DDR A D13	20	D013		VDD	81		
DDR A D14	36	D014		VDD	82		
DDR A D15	38	D015		VDD	87		
DDR A D16	43	D016		VDD	88		
DDR A D17	45	D017		VDD	89		
DDR A D18	55	D018		VDD	95		
DDR A D19	57	D019		VDD	96		
DDR A D20	44	D020		VDD	98		
DDR A D21	46	D021		VDD	104		
DDR A D22	58	D022		VDD	104		
DDR A D23	58	D023		VDD	111		
DDR A D24	61	D024		VDD	112		
DDR A D25	63	D025		VDD	117		
DDR A D26	73	D026		VDD	118		
DDR A D27	75	D027		VSS	2		
DDR A D28	62	D028		VSS	3		
DDR A D29	64	D029		VSS	8		
DDR A D30	74	D030		VSS	8		
DDR A D31	76	D031		VSS	9		
DDR A D32	123	D032		VSS	12		
DDR A D33	125	D033		VSS	12		
DDR A D34	135	D034		VSS	15		
DDR A D35	137	D035		VSS	18		
DDR A D36	134	D036		VSS	21		
DDR A D37	126	D037		VSS	24		
DDR A D38	134	D038		VSS	27		
DDR A D39	136	D039		VSS	33		
DDR A D40	141	D040		VSS	34		
DDR A D41	143	D041		VSS	39		
DDR A D42	151	D042		VSS	40		
DDR A D43	153	D043		VSS	41		
DDR A D44	140	D044		VSS	42		
DDR A D45	142	D045		VSS	47		
DDR A D46	152	D046		VSS	48		
DDR A D47	157	D047		VSS	53		
DDR A D48	154	D048		VSS	54		
DDR A D49	159	D049		VSS	59		
DDR A D50	173	D050		VSS	60		
DDR A D51	175	D051		VSS	65		
DDR A D52	158	D052		VSS	66		
DDR A D53	160	D053		VSS	71		
DDR A D54	174	D054		VSS	72		
DDR A D55	176	D055		VSS	77		
DDR A D56	179	D056		VSS	78		
DDR A D57	181	D057		VSS	121		
DDR A D58	189	D058		VSS	122		
DDR A D59	191	D059		VSS	127		
DDR A D60	190	D060		VSS	128		
DDR A D61	182	D061		VSS	132		
DDR A D62	192	D062		VSS	133		
DDR A D63	194	D063		VSS	138		
PM_EXTTS#1	50	NC#50		VSS	139		
DDR_CS0_DIMMA#	110	NC#69		VSS	144		
DDR_CS1_DIMMA#	115	NC#83		VSS	145		
DDR_CKE0_DIMMA	79	NC#120		VSS	149		
DDR_CKE1_DIMMA	80	NC#163/TEST		VSS	150		
DDR_CKE2_DIMMA	80	CS0#		VSS	155		
DDR_A_RAS#	108	CS1#		VSS	161		
DDR_A_CAS#	113	CKE0		VSS	162		
DDR_A_WE#	109	CKE1		VSS	168		
ICH_SMBCLK	197	RAS#		VSS	171		
ICH_SMBDATA	195	CAS#		VSS	172		
M_ODT0	114	WE#		VSS	177		
M_ODT1	119	SCL		VSS	178		
VREF	1	SDA		VSS	183		
ODT0	4	ODT0		VSS	187		
ODT1	1	ODT1		VSS	190		
VREF	1	VREF		VSS	193		
GND	201	GND		VSS	196		
SKT_SODIMM2002U3GP				VSS	202		

High 5.2mm

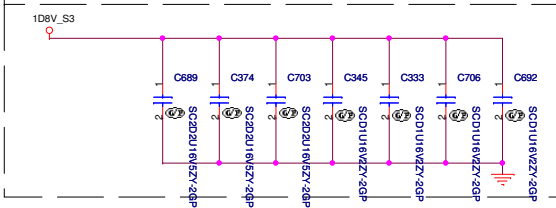
A-NOTE2

緯創資通 Wistron Corporation
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

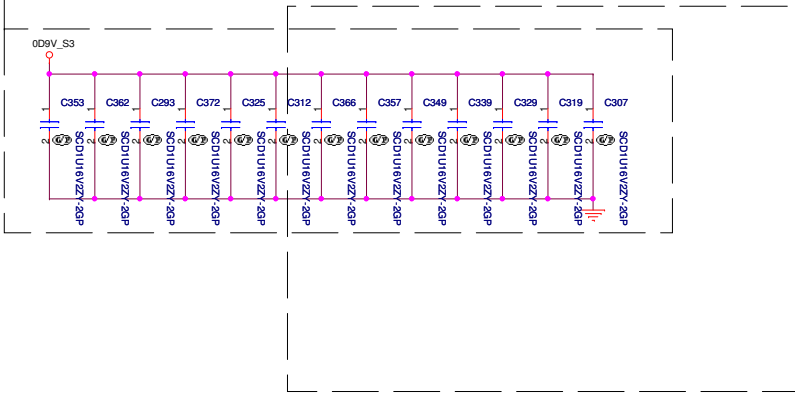
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Size	Document Number	Rev
Customer	Anote2.0 INTEL	-1
Date:	Thursday, March 22, 2007	Sheet 15 of 56



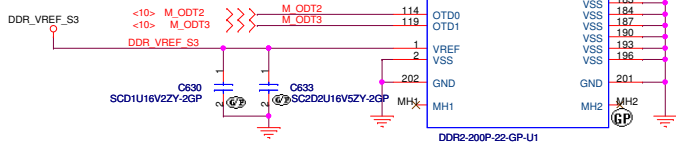
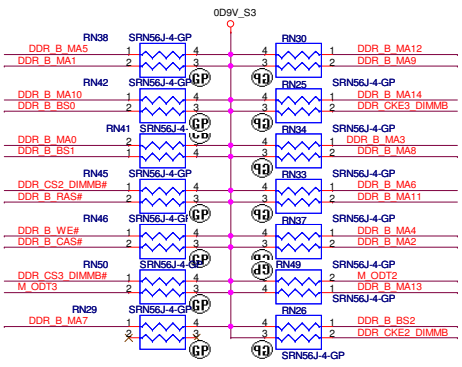
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

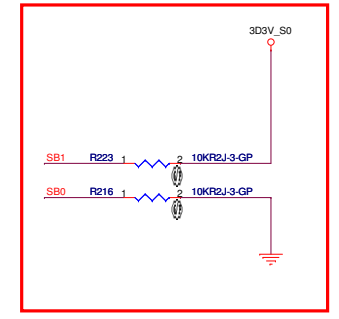
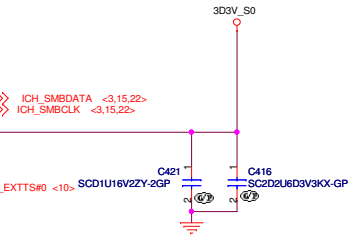


Layout Note:
Place these resistors closely DM2, all trace length Max=1.5"



DDR B MA0	102	DO0
DDR B MA1	101	DO1
DDR B MA2	100	DO2
DDR B MA3	99	DO3
DDR B MA4	98	DO4
DDR B MA5	97	DO5
DDR B MA6	94	DO6
DDR B MA7	92	DO7
DDR B MA8	93	DO8
DDR B MA9	91	DO9
DDR B MA10	105	DO10
DDR B MA11	90	DO11
DDR B MA12	116	DO12
DDR B MA13	112	DO13
DDR B MA14	86	DO14
DDR B BS2	85	DO15
DDR B BS0	107	DO16
DDR B BS1	106	DO17
DDR B D0	5	DO18
DDR B D1	7	DO19
DDR B D2	17	DO20
DDR B D3	14	DO21
DDR B D4	19	DO22
DDR B D5	4	DO23
DDR B D6	6	DO24
DDR B D7	23	DO25
DDR B D8	14	DO26
DDR B D9	25	DO27
DDR B D10	37	DO28
DDR B D11	37	DO29
DDR B D12	20	DO30
DDR B D13	22	DO31
DDR B D14	38	DO32
DDR B D15	38	DO33
DDR B D16	45	DO34
DDR B D17	45	DO35
DDR B D18	55	DO36
DDR B D19	57	DO37
DDR B D20	44	DO38
DDR B D21	46	DO39
DDR B D22	56	DO40
DDR B D23	58	DO41
DDR B D24	61	DO42
DDR B D25	63	DO43
DDR B D26	73	DO44
DDR B D27	75	DO45
DDR B D28	75	DO46
DDR B D29	64	DO47
DDR B D30	64	DO48
DDR B D31	74	DO49
DDR B D32	123	DO50
DDR B D33	125	DO51
DDR B D34	185	DO52
DDR B D35	137	DO53
DDR B D36	124	DO54
DDR B D37	126	DO55
DDR B D38	134	DO56
DDR B D39	136	DO57
DDR B D40	141	DO58
DDR B D41	142	DO59
DDR B D42	151	DO60
DDR B D43	153	DO61
DDR B D44	140	DO62
DDR B D45	142	DO63
DDR B D46	152	DO64
DDR B D47	154	DO65
DDR B D48	157	DO66
DDR B D49	159	DO67
DDR B D50	173	DO68
DDR B D51	175	DO69
DDR B D52	176	DO70
DDR B D53	160	DO71
DDR B D54	174	DO72
DDR B D55	174	DO73
DDR B D56	179	DO74
DDR B D57	181	DO75
DDR B D58	189	DO76
DDR B D59	191	DO77
DDR B D60	180	DO78
DDR B D61	182	DO79
DDR B D62	192	DO80
DDR B D63	194	DO81
DDR B DQS#0	114	DO82
DDR B DQS#1	29	DO83
DDR B DQS#2	49	DO84
DDR B DQS#3	58	DO85
DDR B DQS#4	153	DO86
DDR B DQS#5	146	DO87
DDR B DQS#6	167	DO88
DDR B DQS#7	186	DO89
DDR B DQS#0	13	DO90
DDR B DQS#1	31	DO91
DDR B DQS#2	70	DO92
DDR B DQS#3	70	DO93
DDR B DQS#4	148	DO94
DDR B DQS#5	131	DO95
DDR B DQS#6	169	DO96
DDR B DQS#7	188	DO97
M_ODT2	114	DO98
M_ODT3	119	DO99
VREF	1	DO100
VSS	2	DO101
GND	202	DO102
MH1	1	DO103
MH2	1	DO104
MH2	1	DO105

CN20	A0	RAS#	108	DDR B RAS#	<<>>	DDR_B_RAS#	<->
	A1	WE#	101	DDR B WE#	<<>>	DDR_B_WE#	<->
	A2	CAS#	111	DDR B CAS#	<<>>	DDR_B_CAS#	<->
	A3	CS0#	110	DDR CS2 DIMMB#	<<>>	DDR_CS2_DIMMB#	<-10>
	A4	CS1#	115	DDR CS3 DIMMB#	<<>>	DDR_CS3_DIMMB#	<-10>
	A5	CKE0	79	DDR CKE2 DIMMB	<<>>	DDR_CKE2_DIMMB	<-10>
	A6	CKE1	80	DDR CKE3 DIMMB	<<>>	DDR_CKE3_DIMMB	<-10>
	A7	CK0	30	M_CLK_DDR2	<<>>	M_CLK_DDR2	<-10>
	A8	CK0#	32	M_CLK_DDR#2	<<>>	M_CLK_DDR#2	<-10>
	A9	CK1	164	M_CLK_DDR3	<<>>	M_CLK_DDR3	<-10>
	A10/AP	CK1#	166	M_CLK_DDR#3	<<>>	M_CLK_DDR#3	<-10>
	A11	DM0	10	DDR B DM0	<<>>		
	A12	DM1	26	DDR B DM1	<<>>		
	A13	DM2	52	DDR B DM2	<<>>		
	A14	DM3	67	DDR B DM3	<<>>		
	A15	DM4	130	DDR B DM4	<<>>		
	A16/BA2	DM5	147	DDR B DM5	<<>>		
	BA0	DM6	170	DDR B DM6	<<>>		
	BA1	DM7	185	DDR B DM7	<<>>		
	DO0	SDA	195	ICH_SMBDATA	<<>>	ICH_SMBDATA	<-3.15,2.2>
	DO1	SCL	197	ICH_SMBCLK	<<>>	ICH_SMBCLK	<-3.15,2.2>
	DO2	VDDSPD	199				
	DO3	SA0	198	SB0			
	DO4	SA1	200	SB1			
	DO5	NC#50	50	PM_EXTT#0	<<>>	PM_EXTT#0	<-10>
	DO6	NC#69	69				
	DO7	NC#83	83				
	DO8	NC#120	120				
	DO9	NC#129	129				
	DO10	NC#163/TEST	163				
	DO11	VDD	81				
	DO12	VDD	82				
	DO13	VDD	87				
	DO14	VDD	88				
	DO15	VDD	95				
	DO16	VDD	96				
	DO17	VDD	103				
	DO18	VDD	104				
	DO19	VDD	111				
	DO20	VDD	112				
	DO21	VDD	117				
	DO22	VDD	118				
	DO23	VSS	3				
	DO24	VSS	8				
	DO25	VSS	12				
	DO26	VSS	15				
	DO27	VSS	18				
	DO28	VSS	21				
	DO29	VSS	24				
	DO30	VSS	27				
	DO31	VSS	33				
	DO32	VSS	34				
	DO33	VSS	39				
	DO34	VSS	40				
	DO35	VSS	41				
	DO36	VSS	42				
	DO37	VSS	47				
	DO38	VSS	48				
	DO39	VSS	53				
	DO40	VSS	54				
	DO41	VSS	59				
	DO42	VSS	60				
	DO43	VSS	65				
	DO44	VSS	66				
	DO45	VSS	71				
	DO46	VSS	72				
	DO47	VSS	77				
	DO48	VSS	78				
	DO49	VSS	121				
	DO50	VSS	122				
	DO51	VSS	127				
	DO52	VSS	128				
	DO53	VSS	132				
	DO54	VSS	133				
	DO55	VSS	138				
	DO56	VSS	139				
	DO57	VSS	144				
	DO58	VSS	145				
	DO59	VSS	149				
	DO60	VSS	150				
	DO61	VSS	155				
	DO62	VSS	156				
	DO63	VSS	161				
	DO64	VSS	162				
	DO65	VSS	165				
	DO66	VSS	168				
	DO67	VSS	171				
	DO68	VSS	172				
	DO69	VSS	177				
	DO70	VSS	178				
	DO71	VSS	183				
	DO72	VSS	184				
	DO73	VSS	187				
	DO74	VSS	190				
	DO75	VSS	193				
	DO76	VSS	196				
	DO77	GND	201				
	DO78	GND	201				



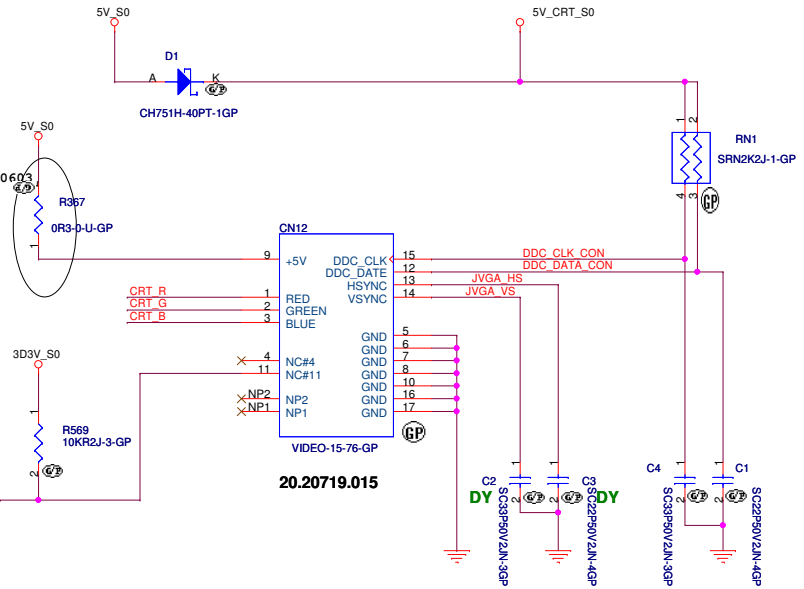
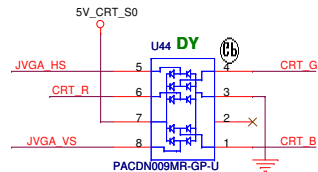
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tsu Wu Rd., Hsinchu, Taipei District 221, Taiwan, R.O.C.

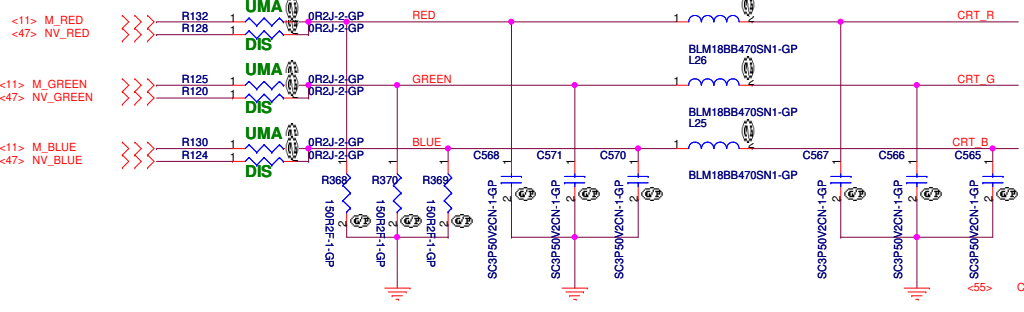
Title		DDRII-SODIMM SLOT2	
Size	Document Number	Rev	
Custom		Anote2.0 INTEL	
Date	Thursday, March 22, 2007	Sheet	16 of 56

62.10017.A61
High 9.2mm
2nd source: 62.10017.A61

CRT I/F & CONNECTOR

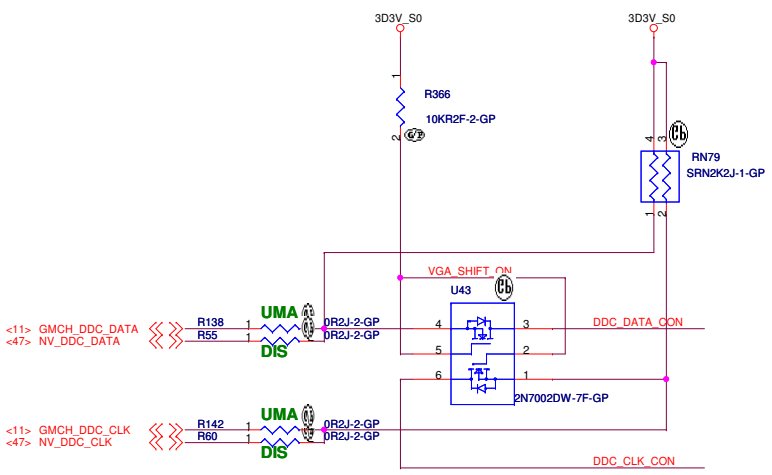
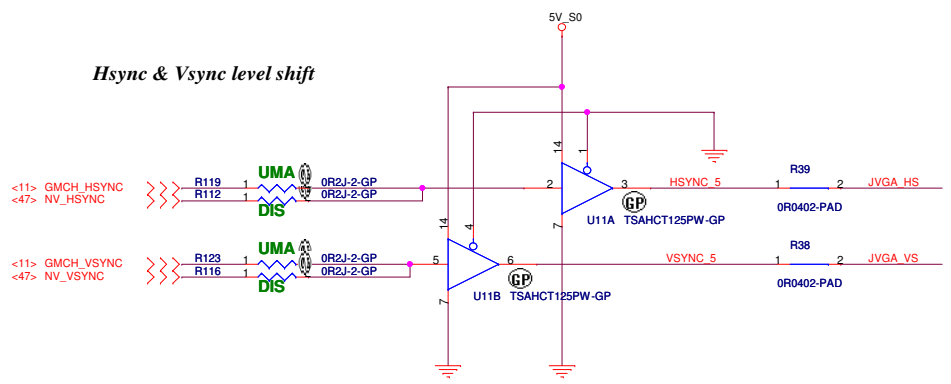


Layout Note:
Place these resistors close to the CRT-out connector



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

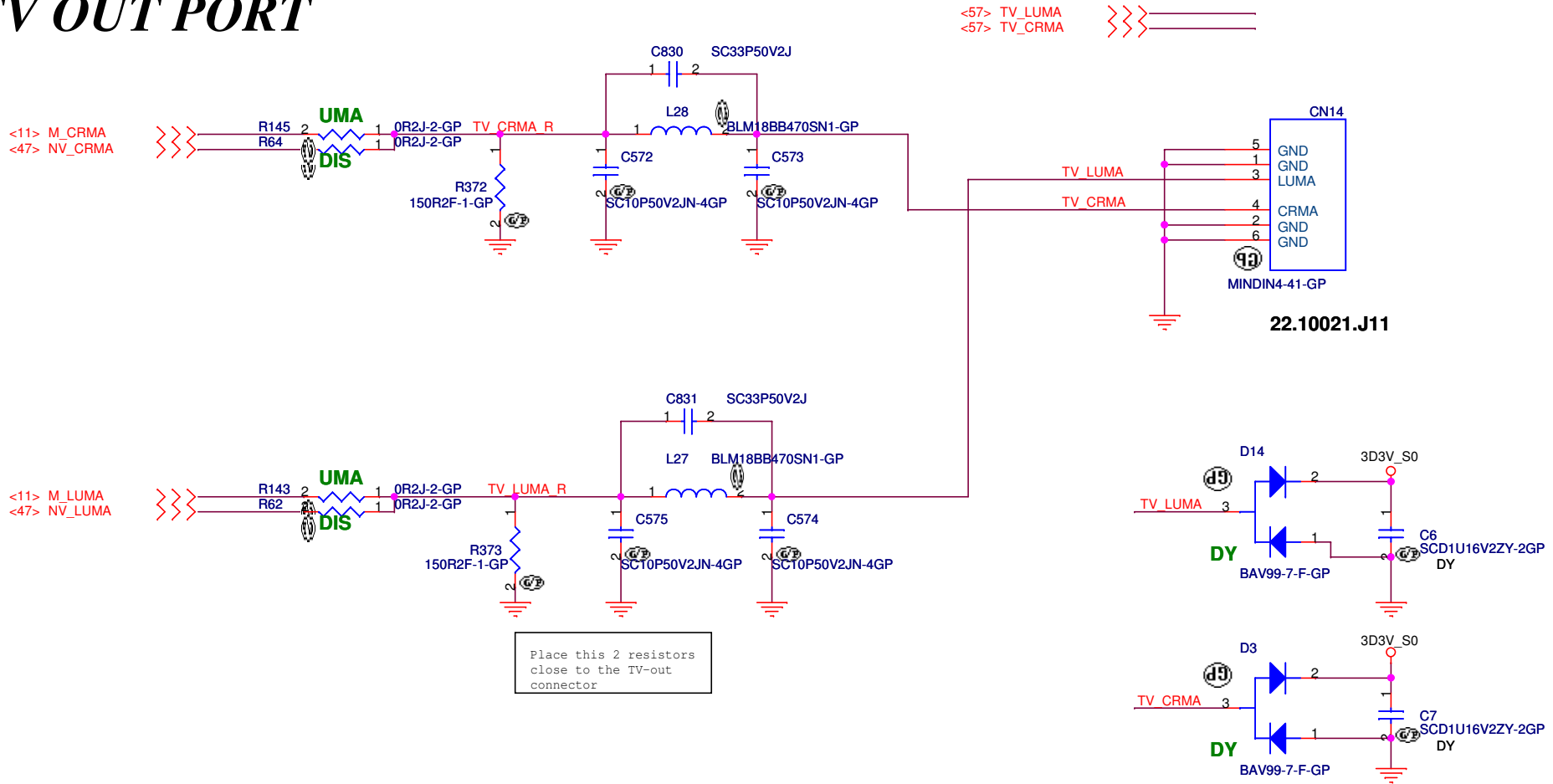
Hsync & Vsync level shift



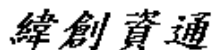
A-NOTE2

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CRT Connector	
Size A3	Document Number
Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Sheet 17 of 56

TV OUT PORT

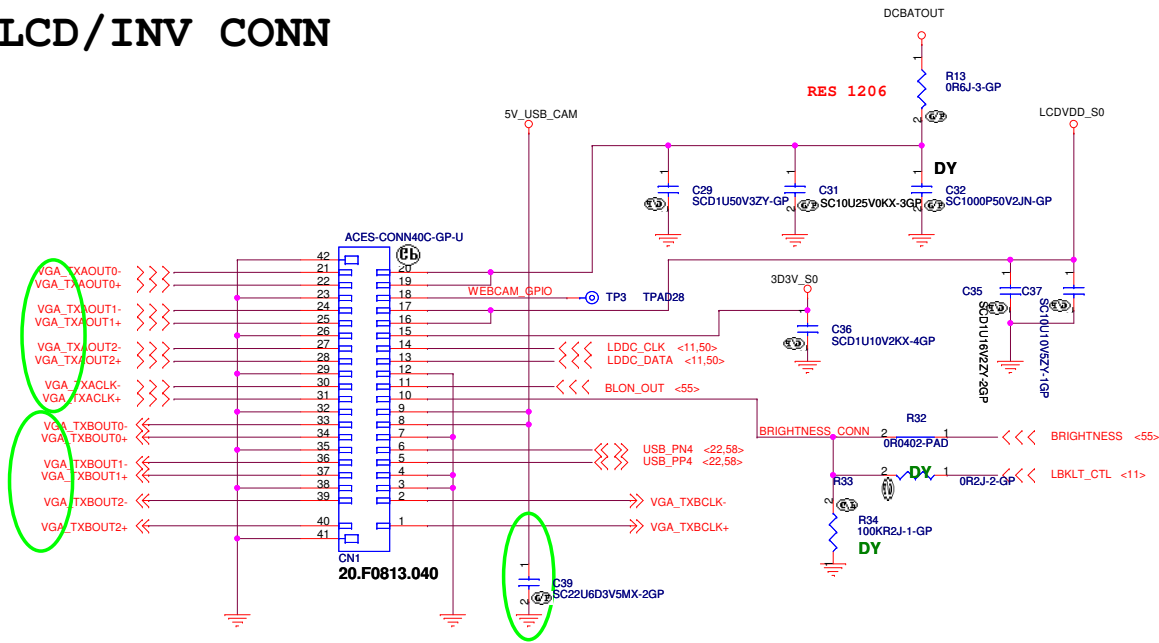


A-NOTE2

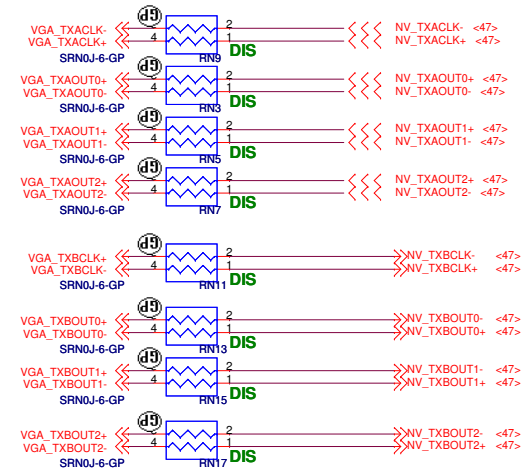
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TV Connector	
Size A4	Document Number Anote2.0 INTEL
Date: Thursday, March 22, 2007	Rev -1

LED / INVERTER INTERFACE

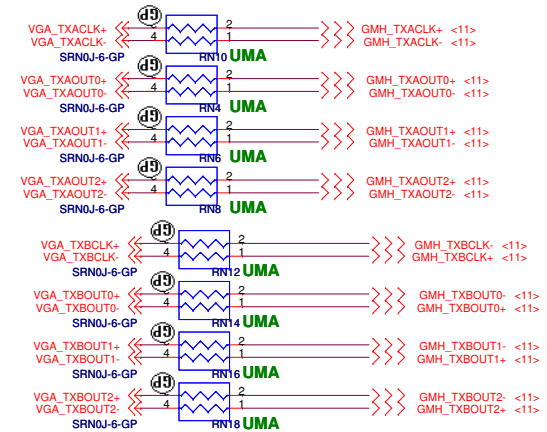
LCD/INV CONN



ATI LVDS INTERFACE



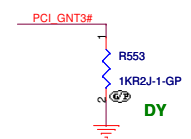
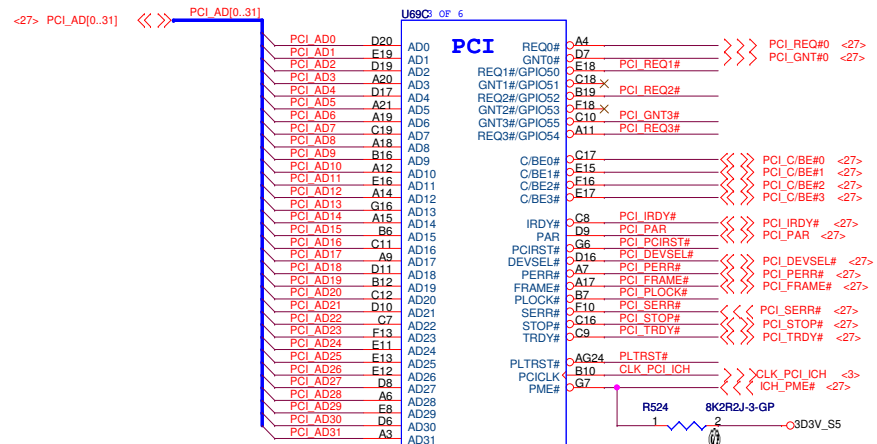
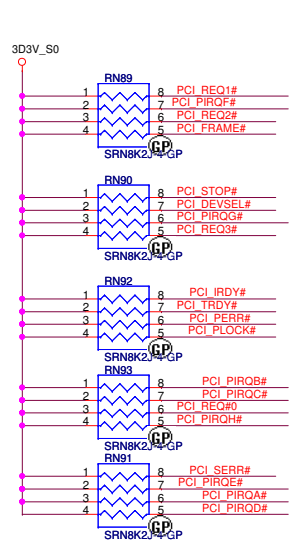
UMA LVDS INTERFACE



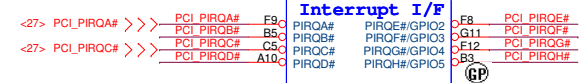
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

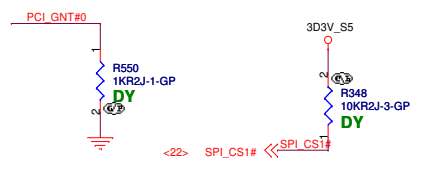
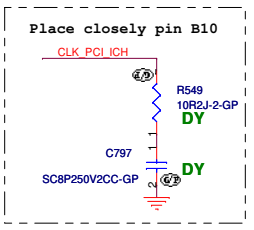
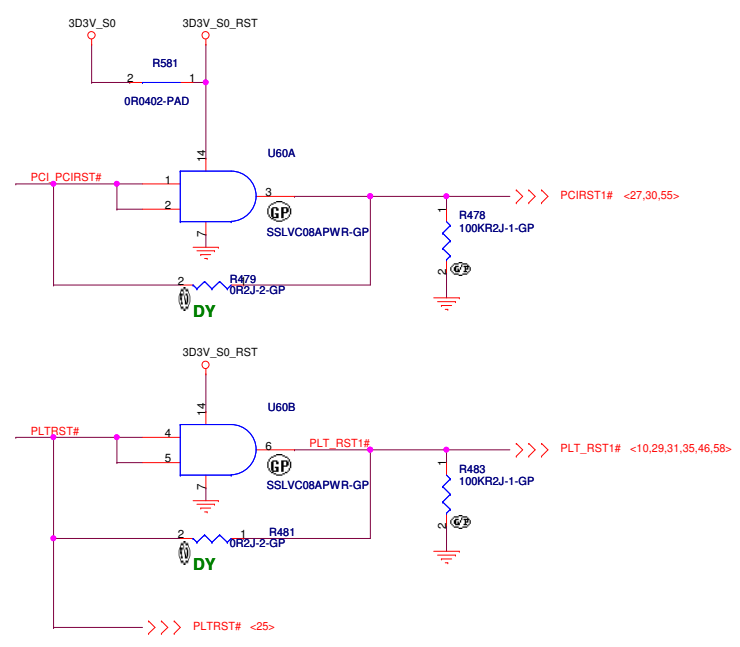
Title LCD/Inverter Connector			Rev -1
Size A3	Document Number Anote2.0 INTEL		
Date: Thursday, March 22, 2007	Sheet	19	of 56



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



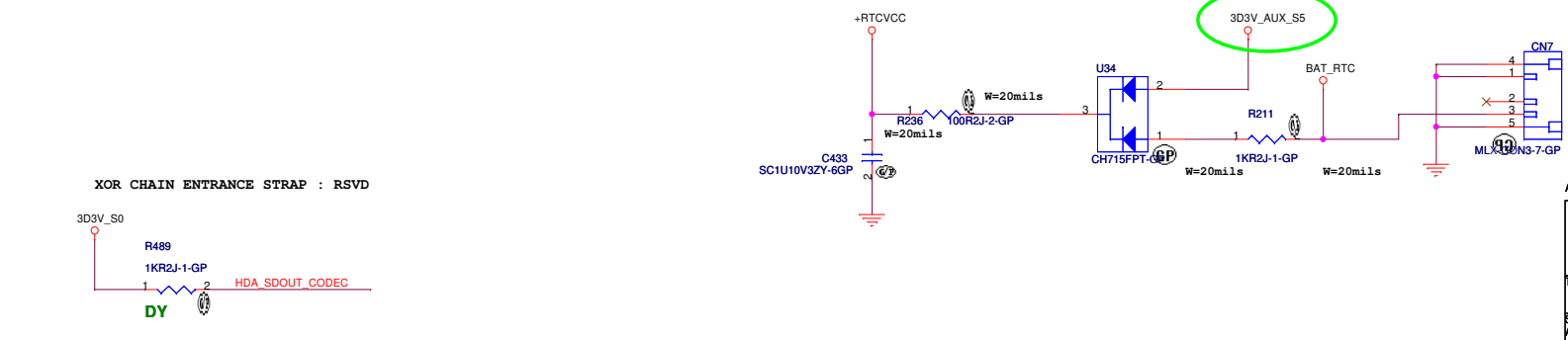
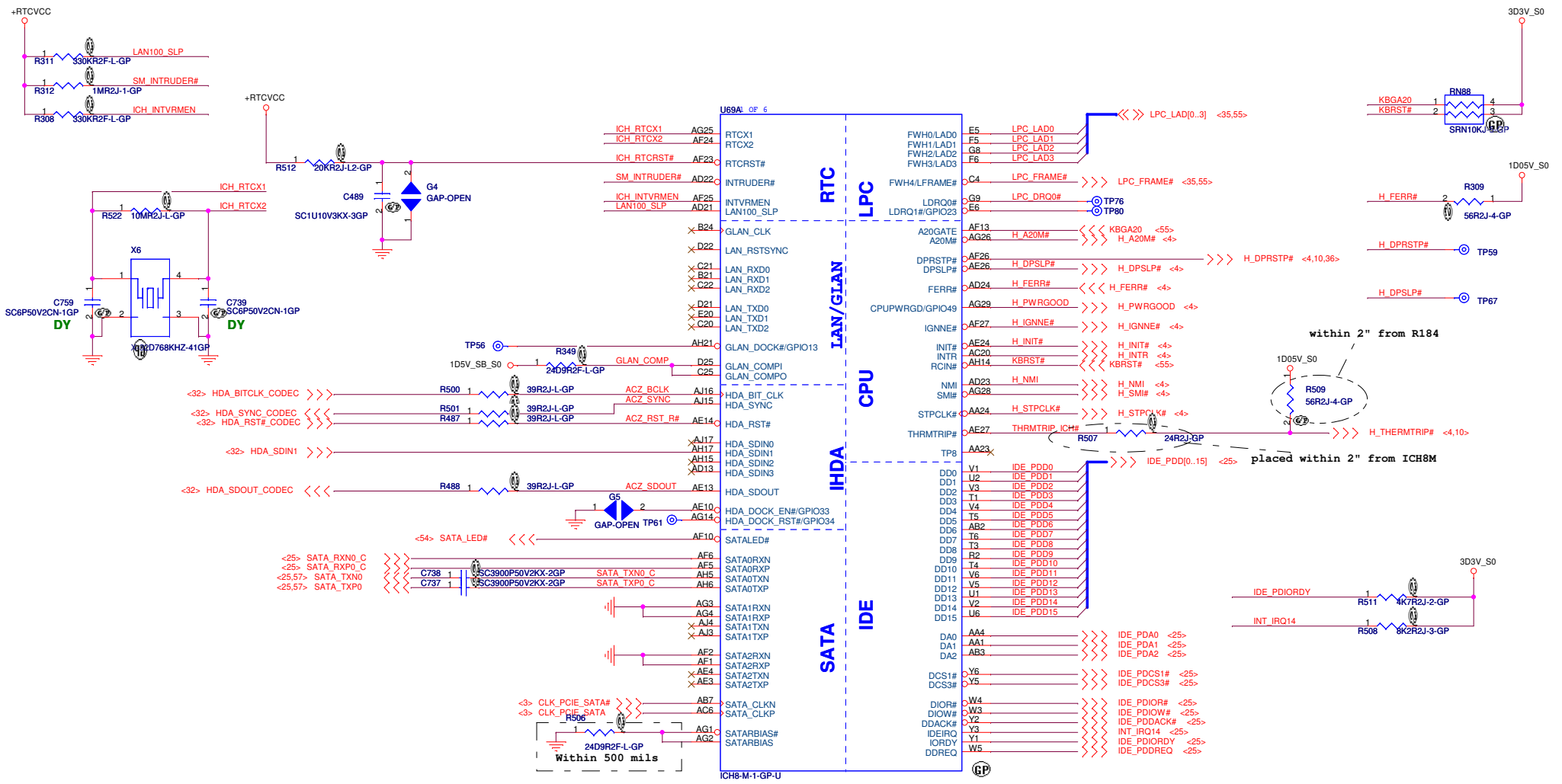
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8(1/4)-PCI/INT**

Size A3 | Document Number: **Anote2.0 INTEL** | Rev: **-1**

Date: Thursday, March 22, 2007 | Sheet 20 of 56



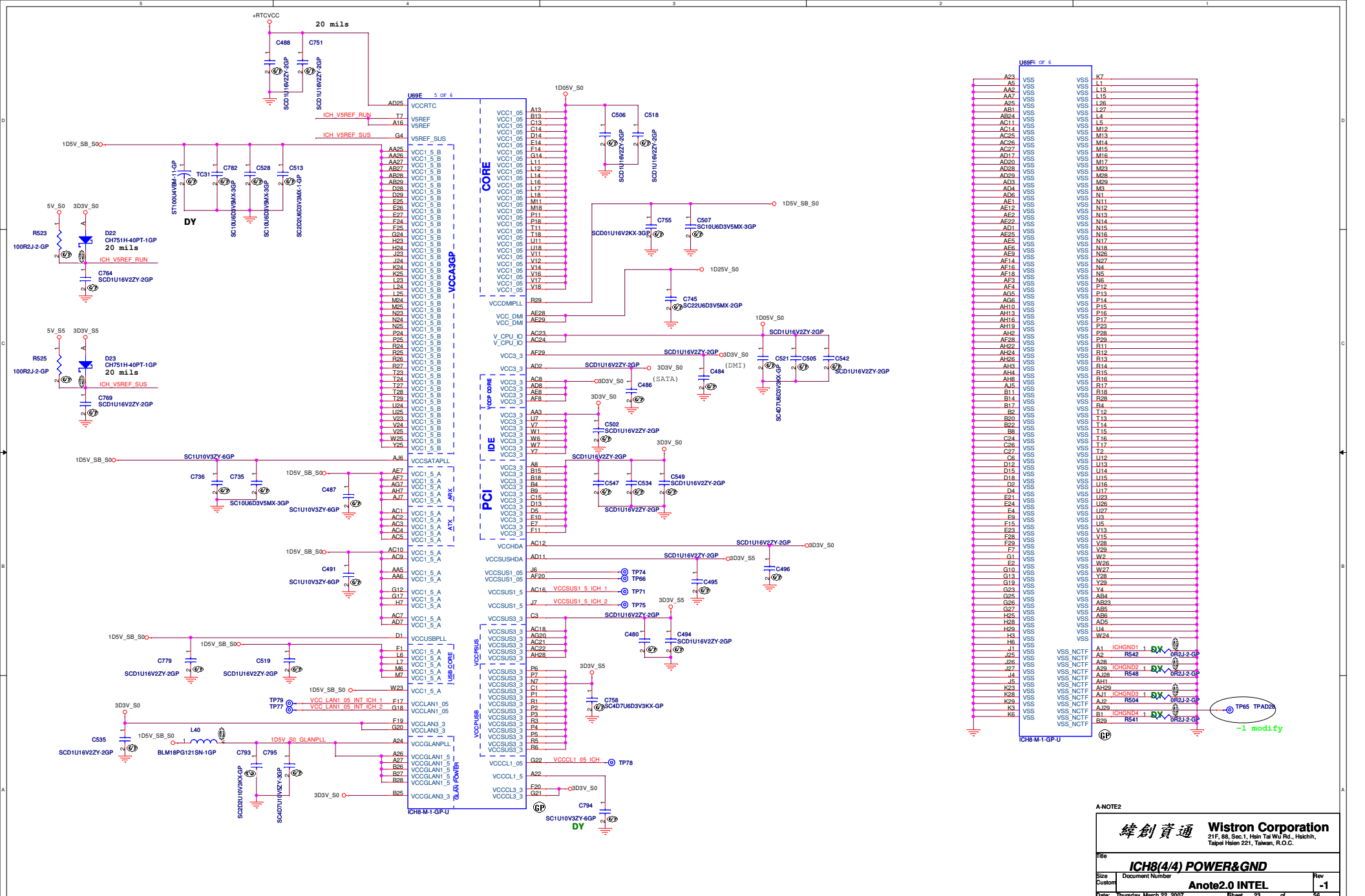
A-NOTE2

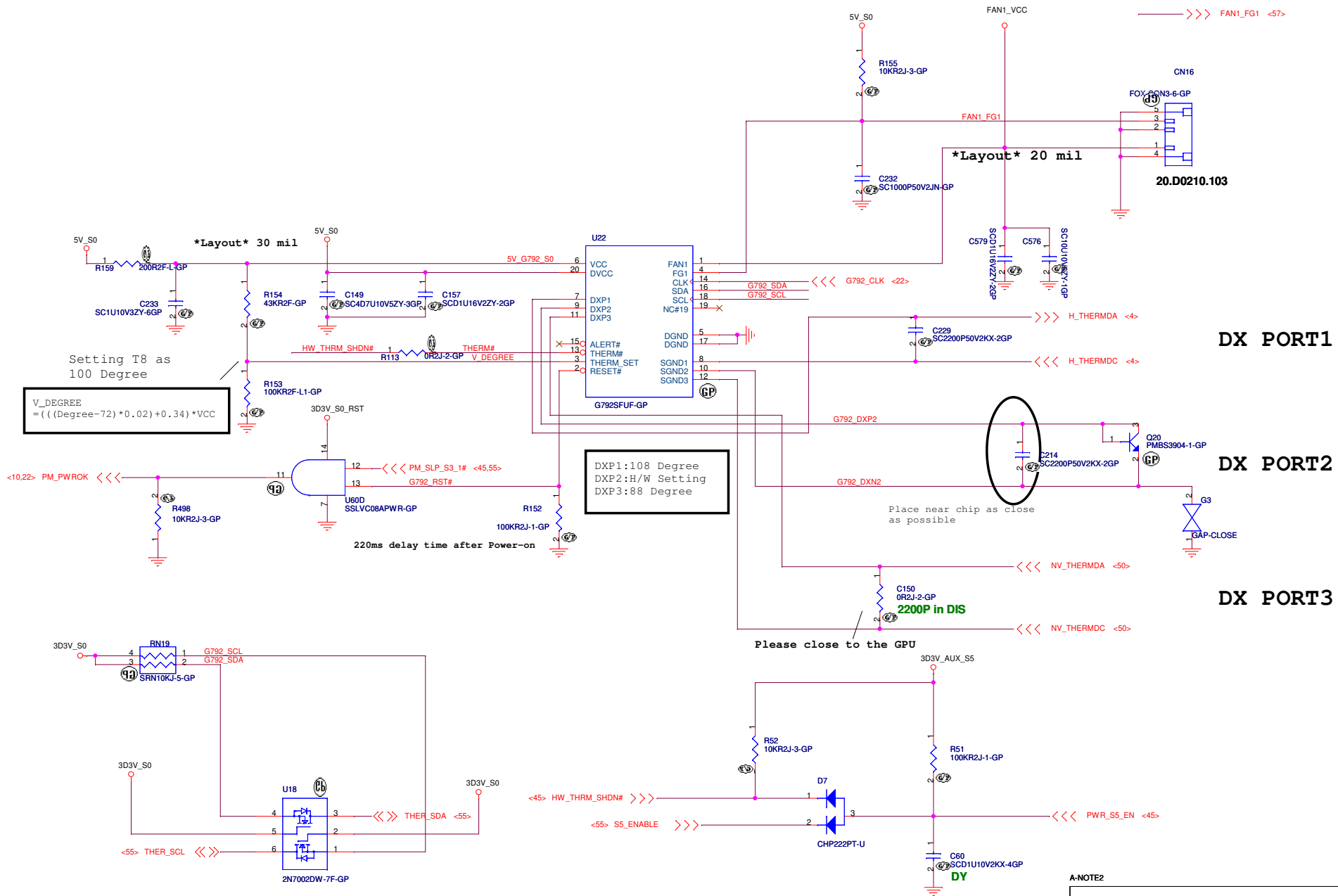
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8(2/4) LAN,HD,IDE,LPC**

Size A3 Document Number **Anote2.0 INTEL** Rev -1

Date: Thursday, March 22, 2007 Sheet 21 of 56





Setting T8 as 100 Degree

$$V_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

DX PORT1

DX PORT2

DX PORT3

Please close to the GPU

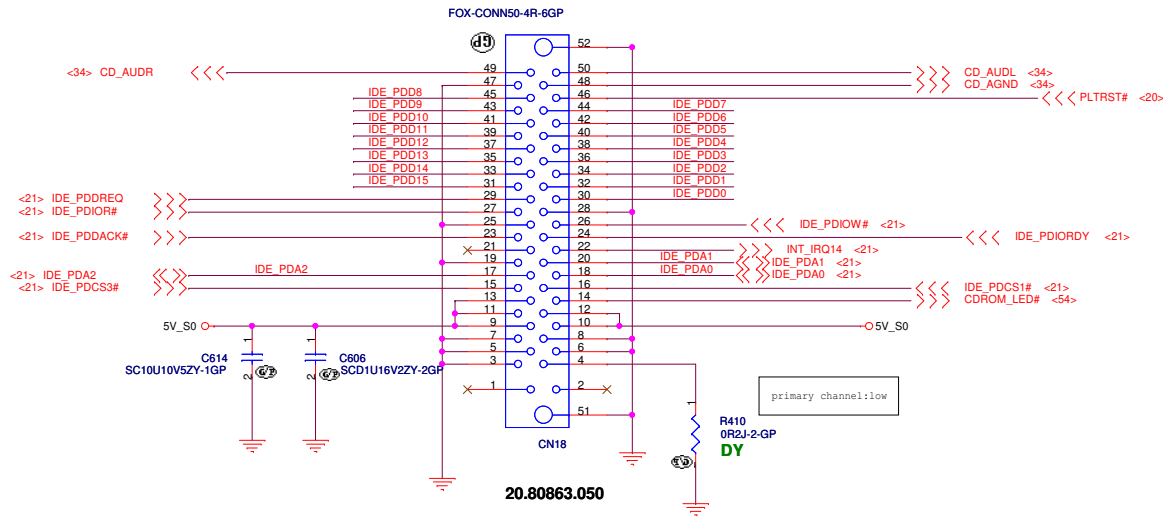
A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Thermal/Fan Controller G792	
Title	Rev
Size	Document Number
Custom	Anote2.0 INTEL
Date: Thursday, March 22, 2007	Sheet 24 of 56

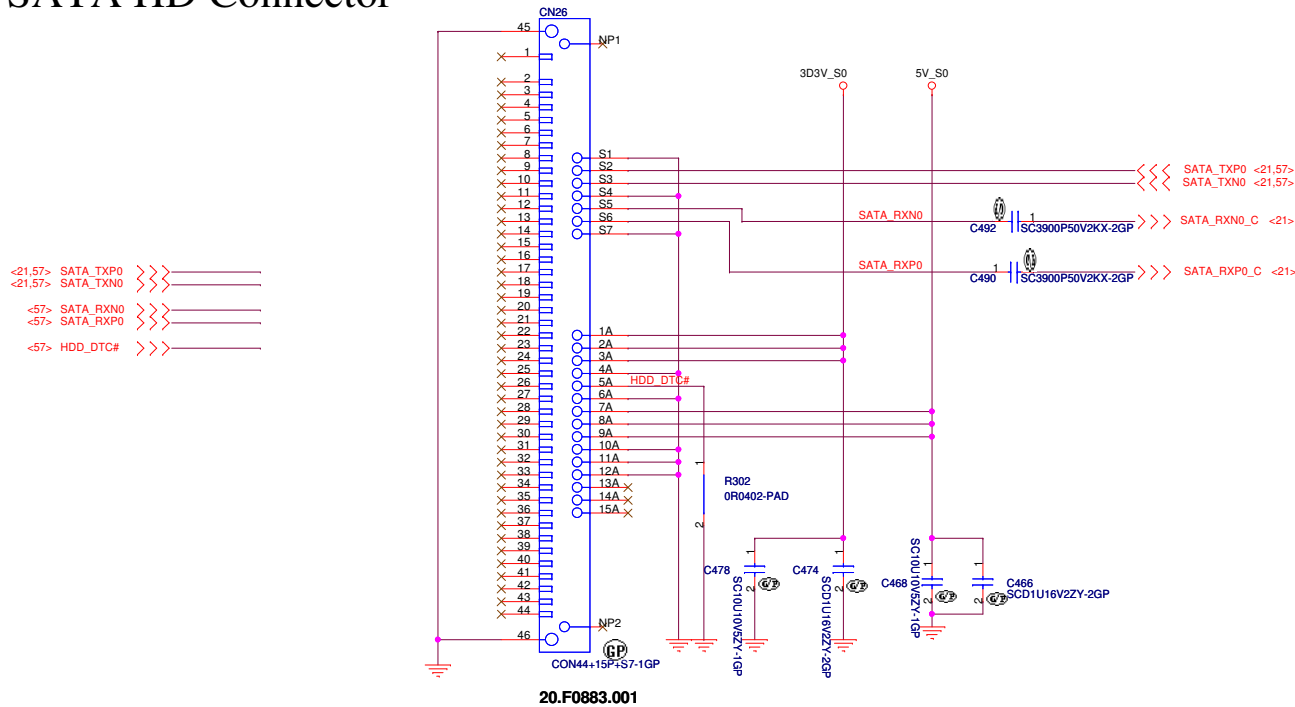
CD-ROM CONNECTOR

Lab1 20.80346.050

Lab2 20.80863.050



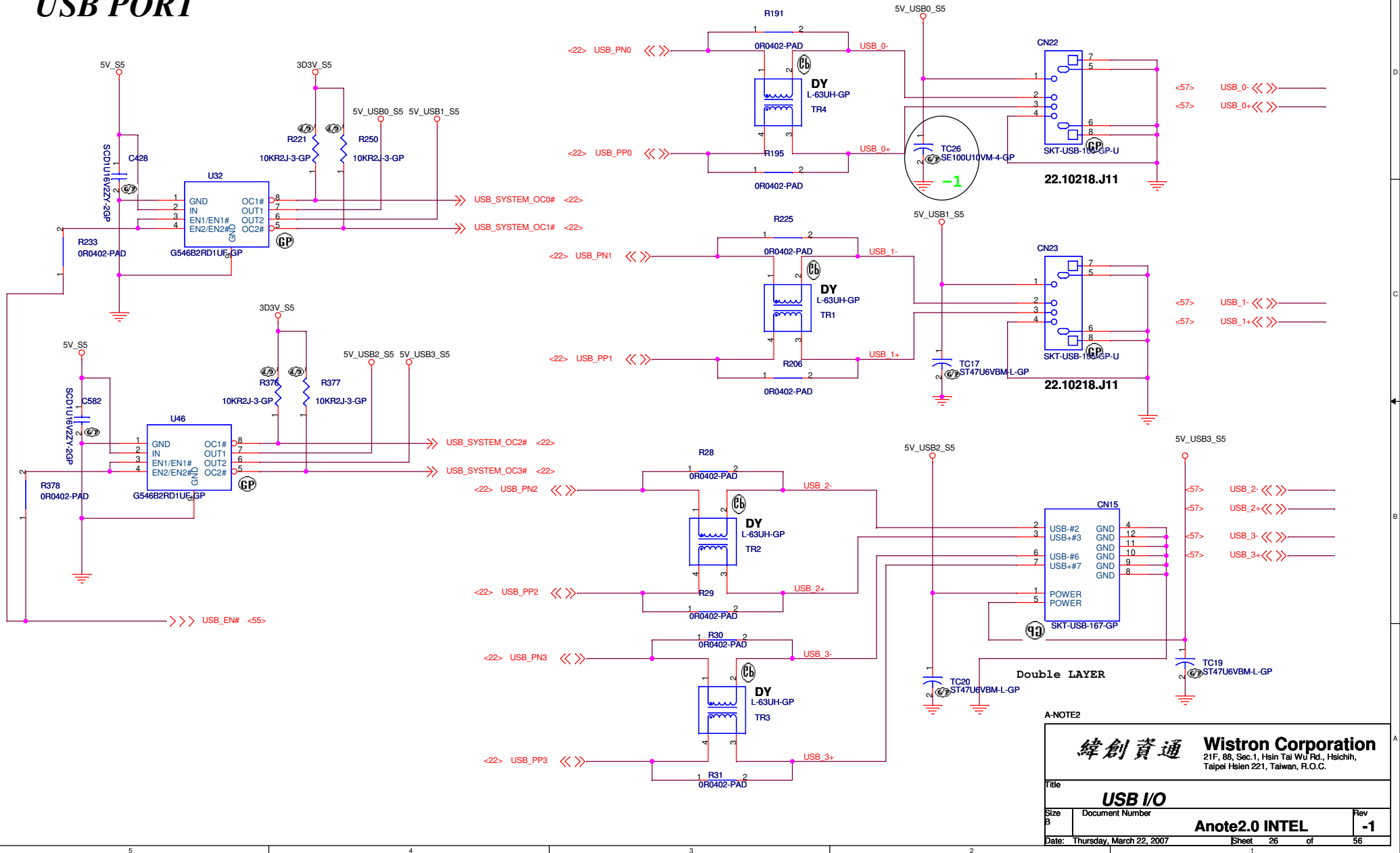
SATA HD Connector



A-NOTE2

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
Title			
HD/CDROM/USB			
Size	Document Number	Rev	
A3		Anote2.0 INTEL	
Date: Thursday, March 22, 2007		Sheet	56

USB PORT

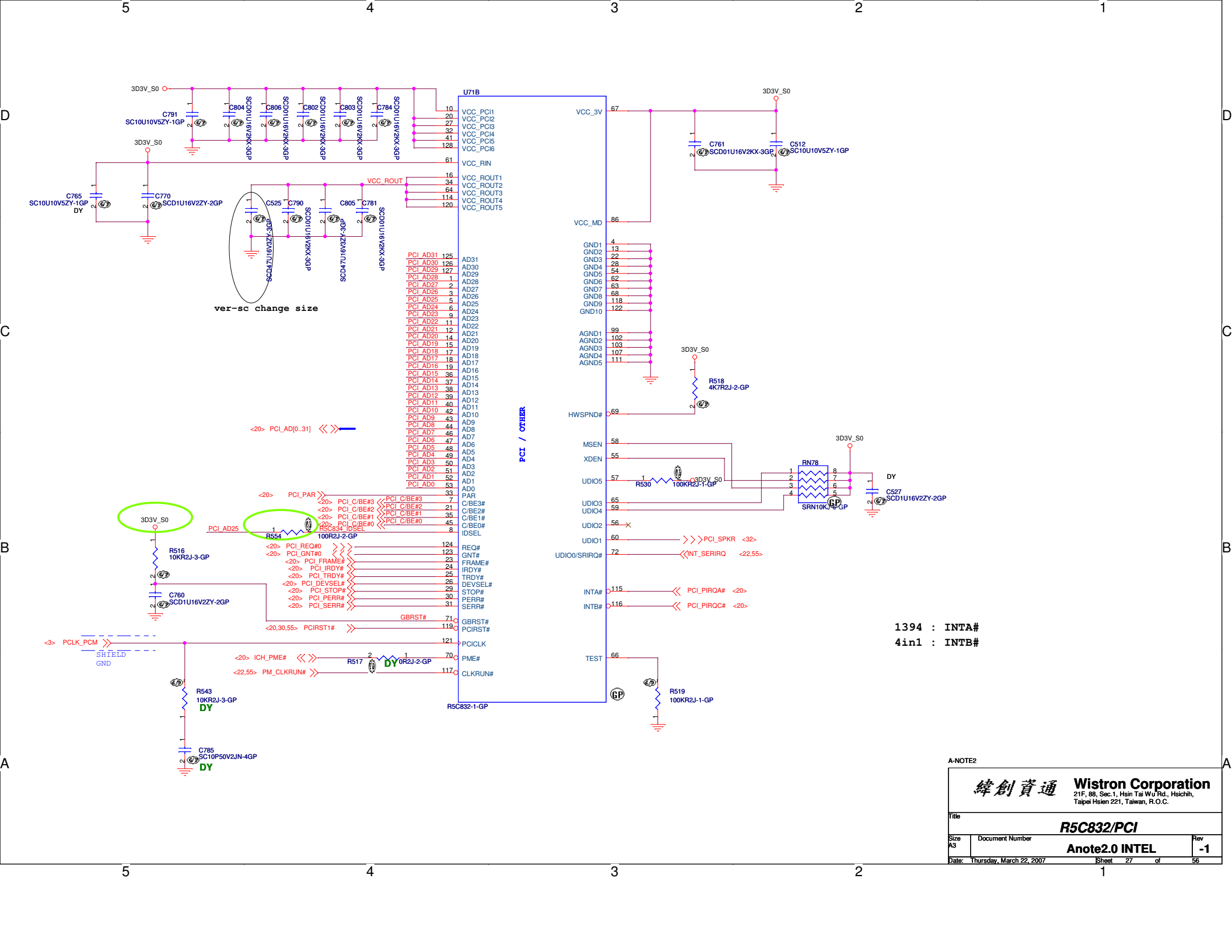


A-NOTE2

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB I/O**

Size: B	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet: 26	of: 56



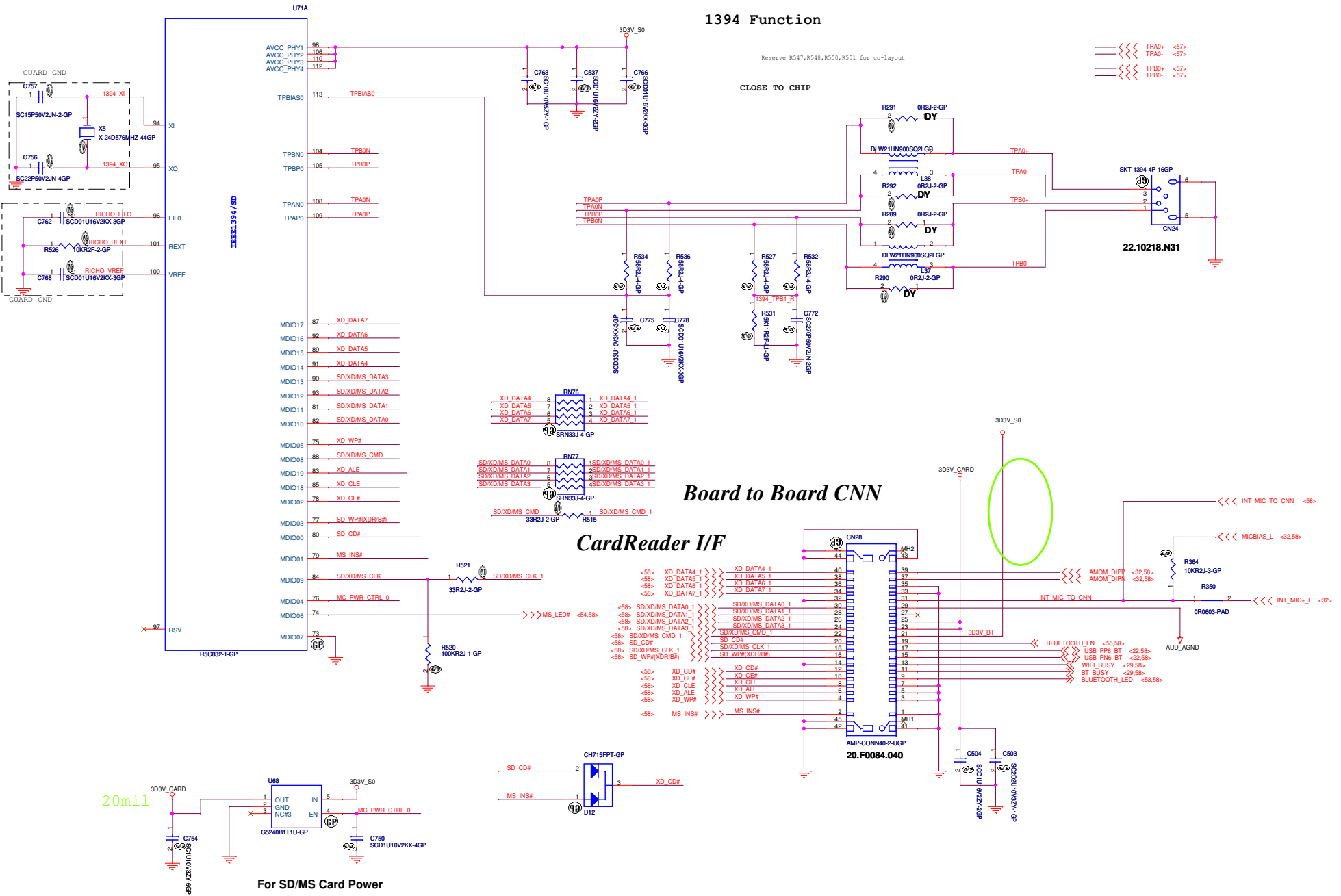
ver-sc change size

PCI / OTHER

1394 : INTA#
4in1 : INTB#

A-NOTE2

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
Title R5C832/PCI	
Size A3	Document Number Anote2.0 INTEL
Date: Thursday, March 22, 2007	Sheet 27 of 56
Rev -1	



1394 Function

Reserve R547, R548, R550, R551 for co-layout

CLOSE TO CHIP

TPA0+ <-57>
TPA0- <-57>
TPB0+ <-57>
TPB0- <-57>

Board to Board CNN

CardReader I/F

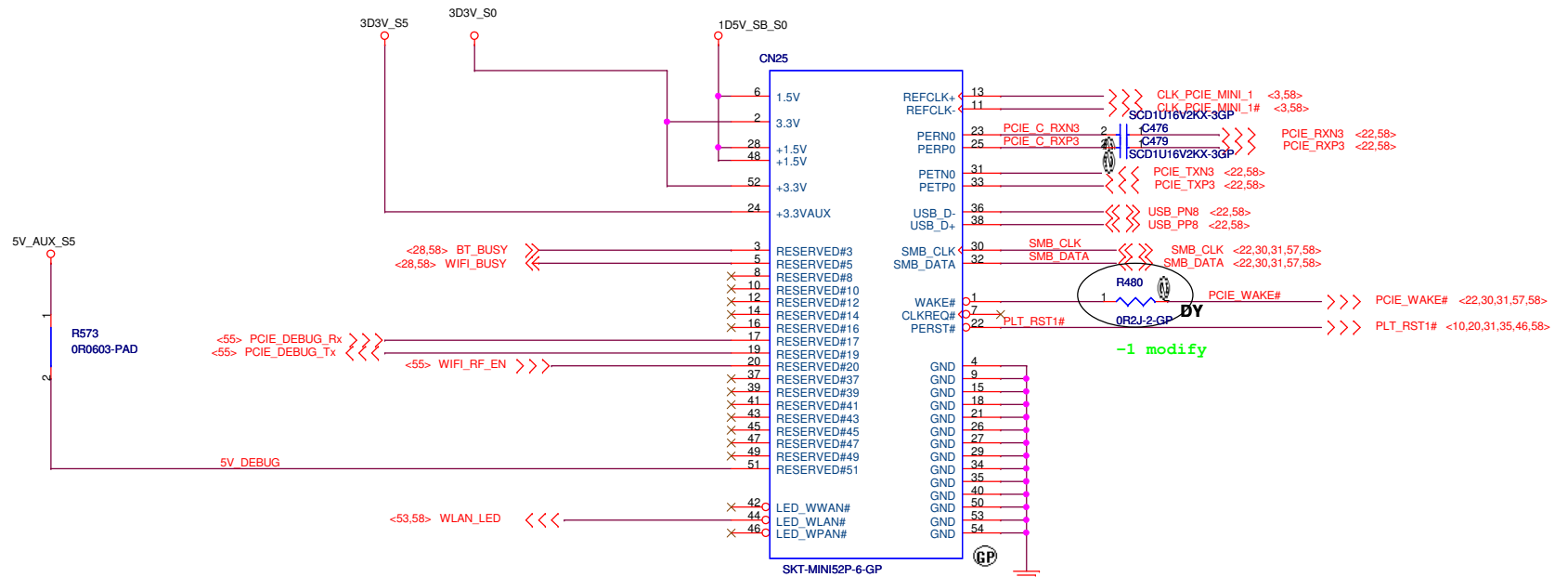
20mil

For SD/MS Card Power

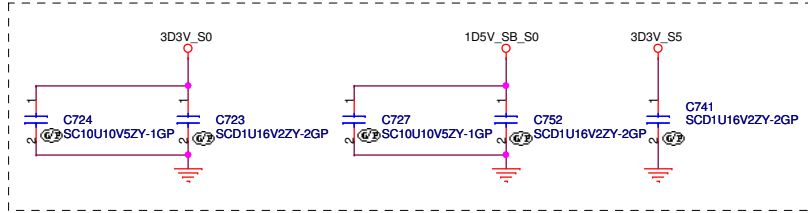
Mini PCI-E Connector

Port-1

Only port-1 support USB



62.10043.261 Note: 9/5 ME update



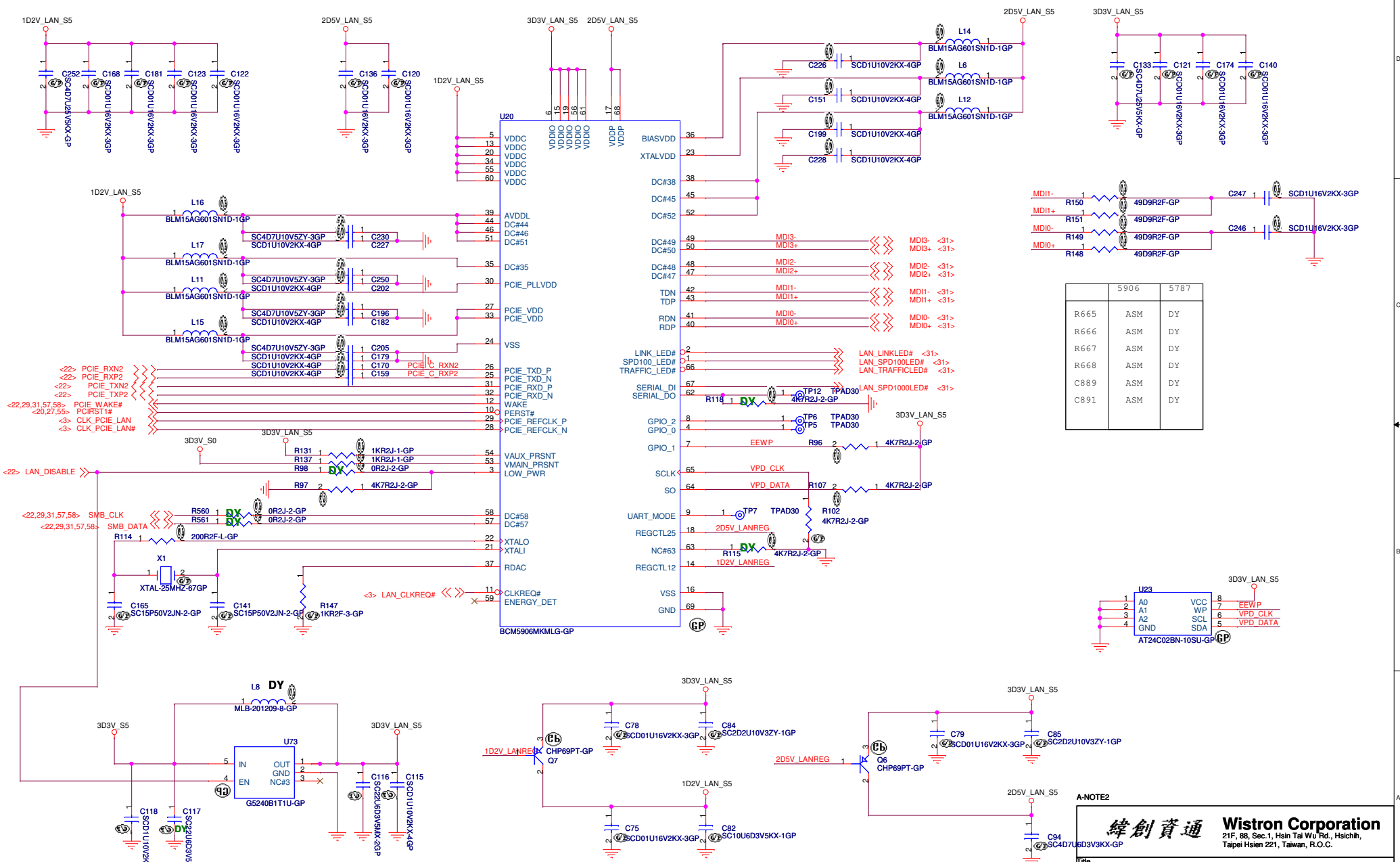
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

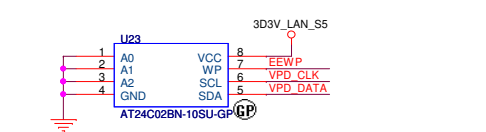
Title: **MINI CARD CONN.**

Size B Document Number **Anote2.0 INTEL** Rev **-1**

Date: Thursday, March 22, 2007 Sheet 29 of 56



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY



A-NOTE2

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

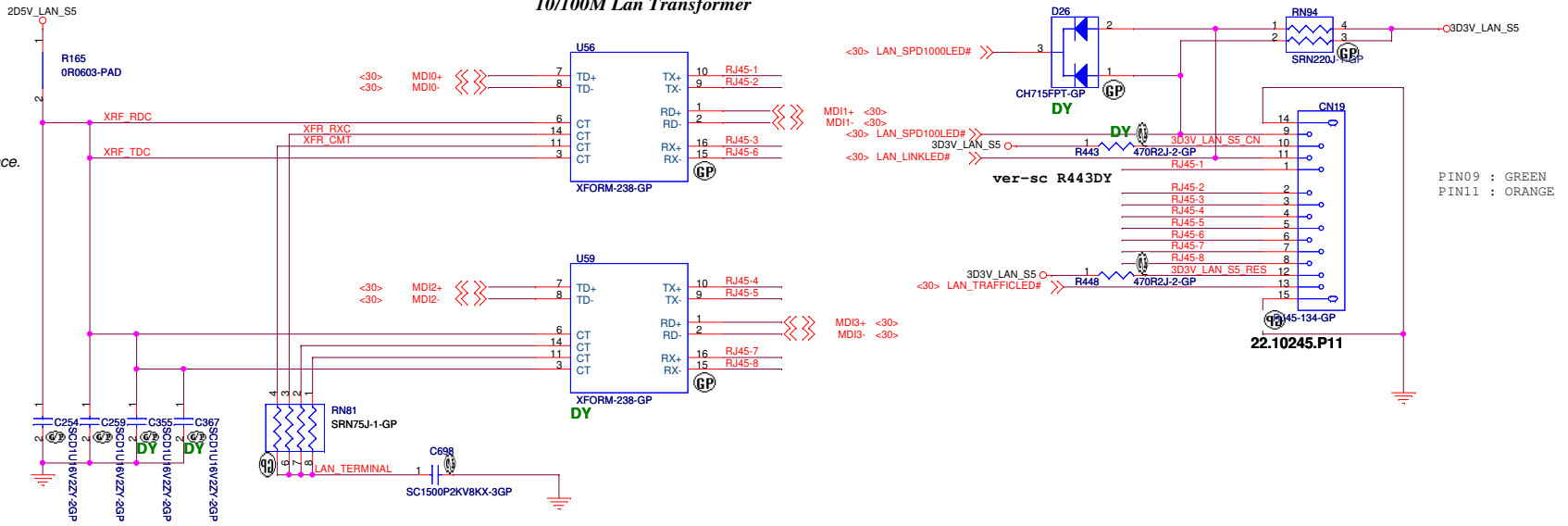
Title: **LAN BCM5906M**

Size A3	Document Number	Rev -1
---------	-----------------	--------

Date: Thursday, March 22, 2007 Sheet 30 of 56

10/100M Lan Transformer

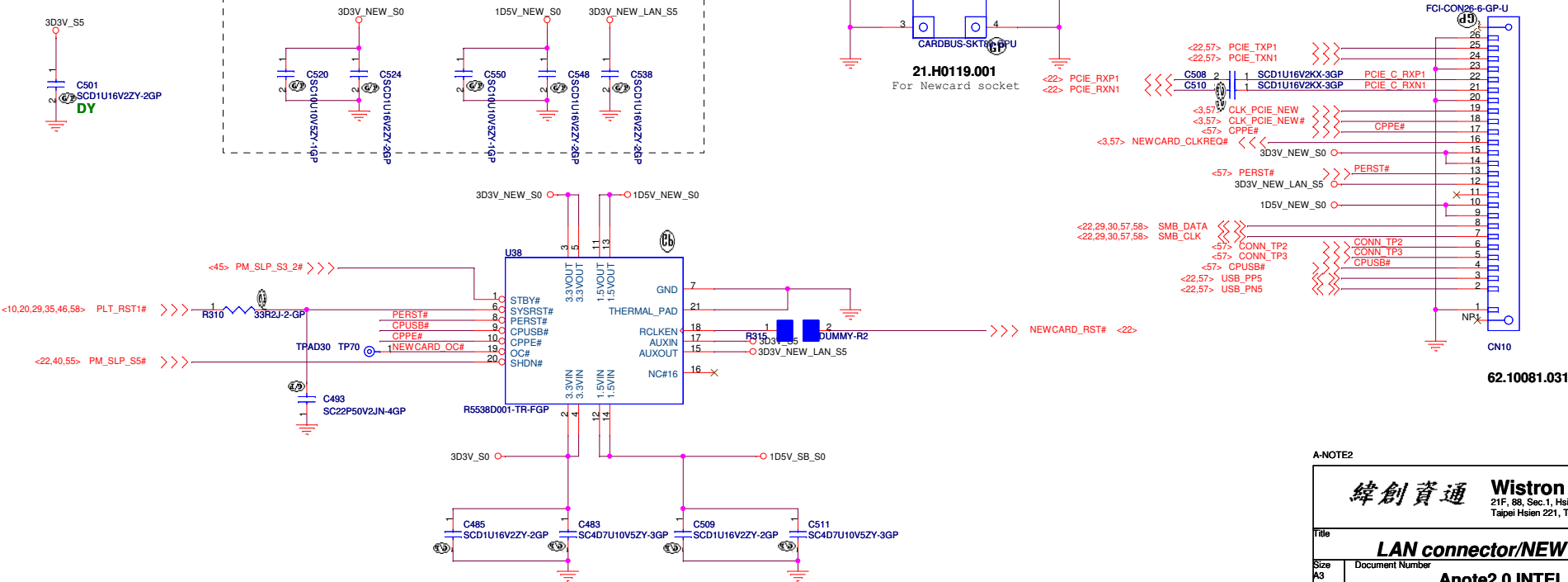
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



NEWCARD Connector

Place them Near to Chip

Place them Near to Connector

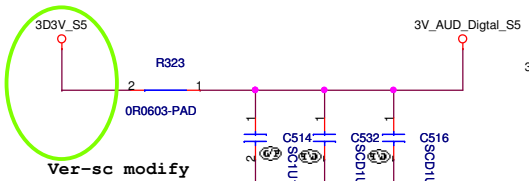


A-NOTE2

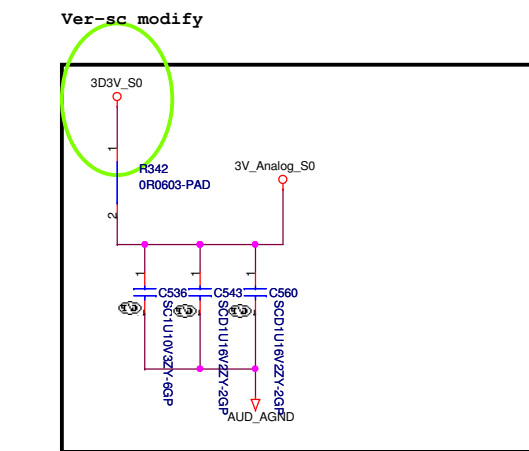
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File	LAN connector/NEW CARD/SIM		
Size	Document Number	Anote2.0 INTEL	Rev -1
Date	Thursday, March 22, 2007	Sheet 31	of 56

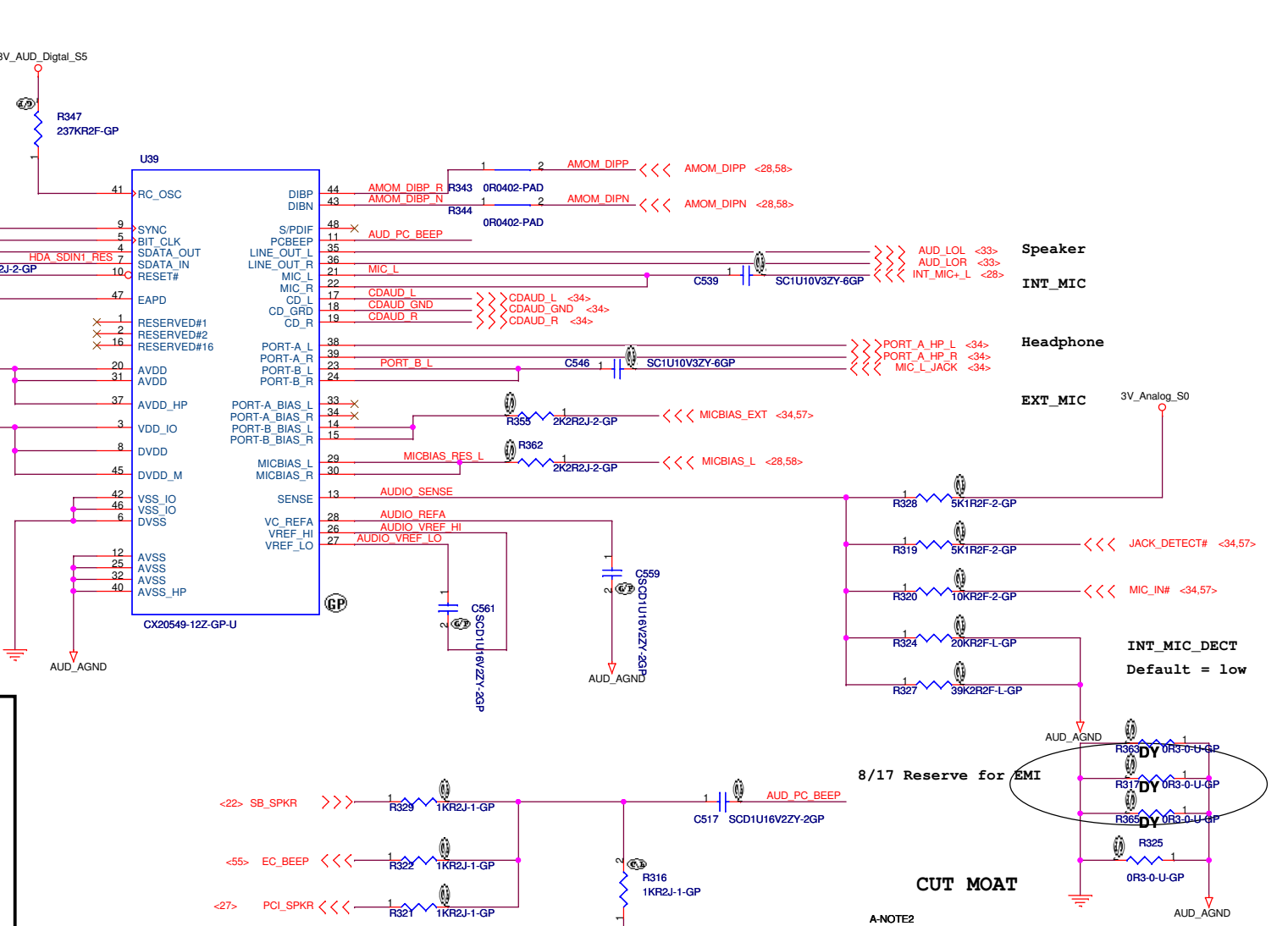
CLOSE TO TRANSFORMER



Ver-sc modify



Ver-sc modify



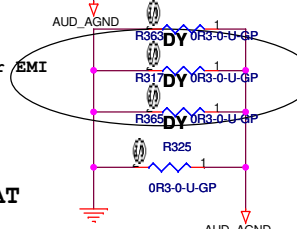
Speaker
INT_MIC

Headphone
EXT_MIC

3V_Analog_S0

JACK_DETECT#
MIC_IN#

INT_MIC_DECT
Default = low

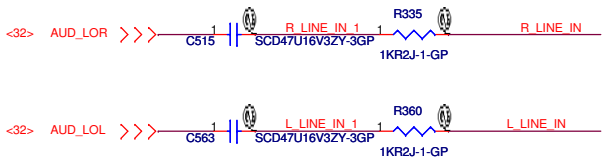
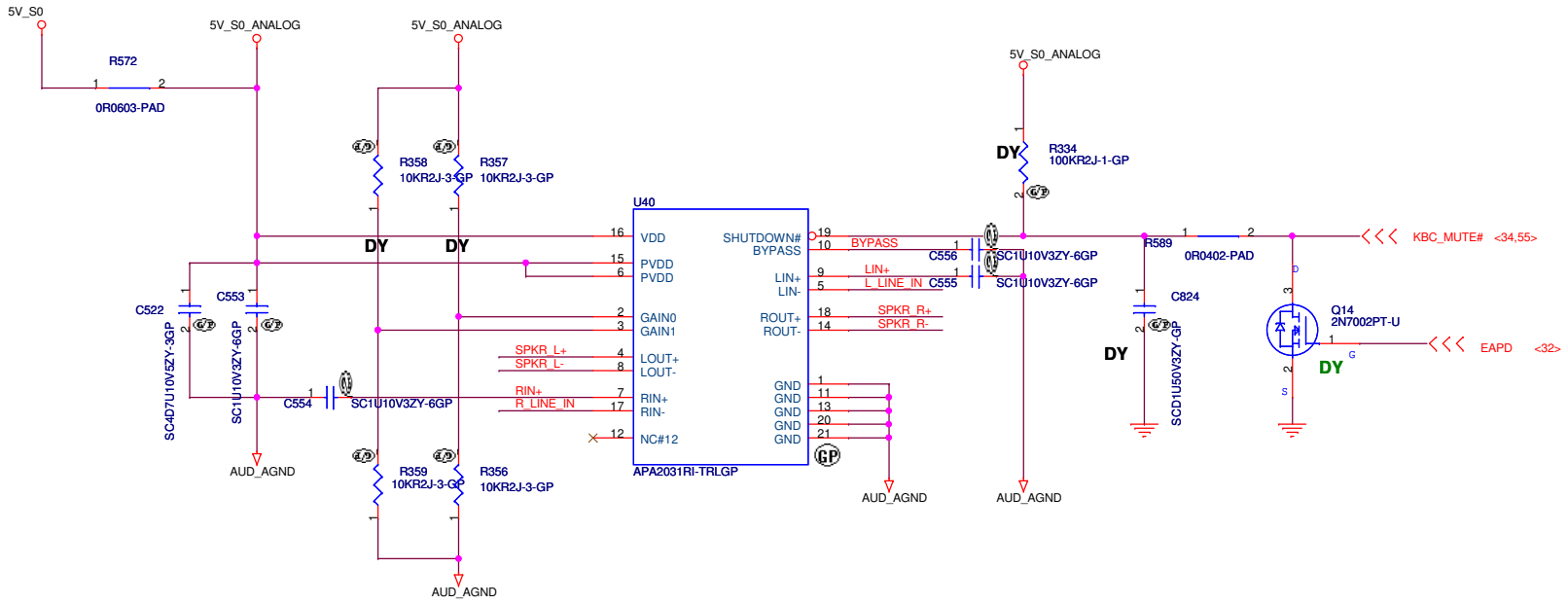


8/17 Reserve for EMI

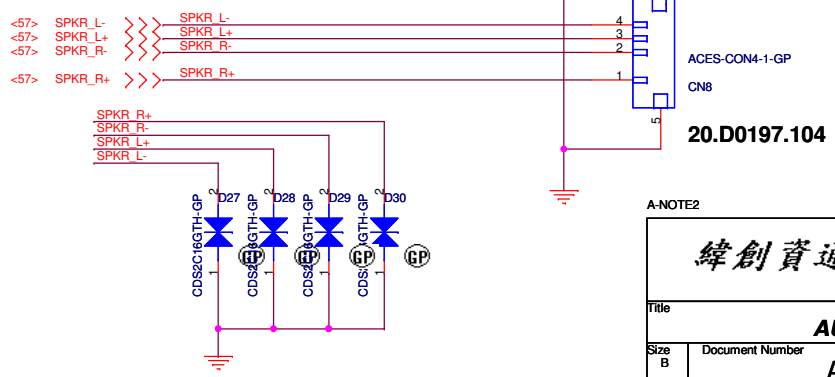
CUT MOAT

A-NOTE2

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
AUDIO CODEC CX20549-12Z			
Title		Rev	
Size B		Document Number	
Date: Thursday, March 22, 2007		Sheet 32 of 56	
-1		Anote2.0 INTEL	

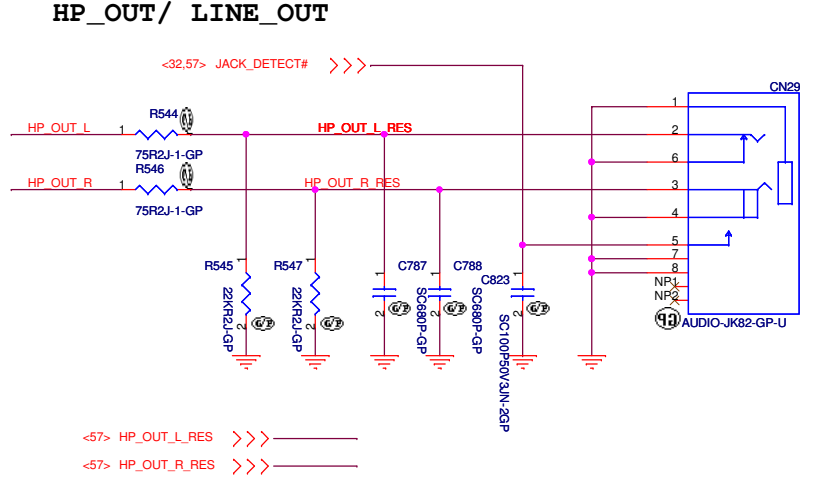
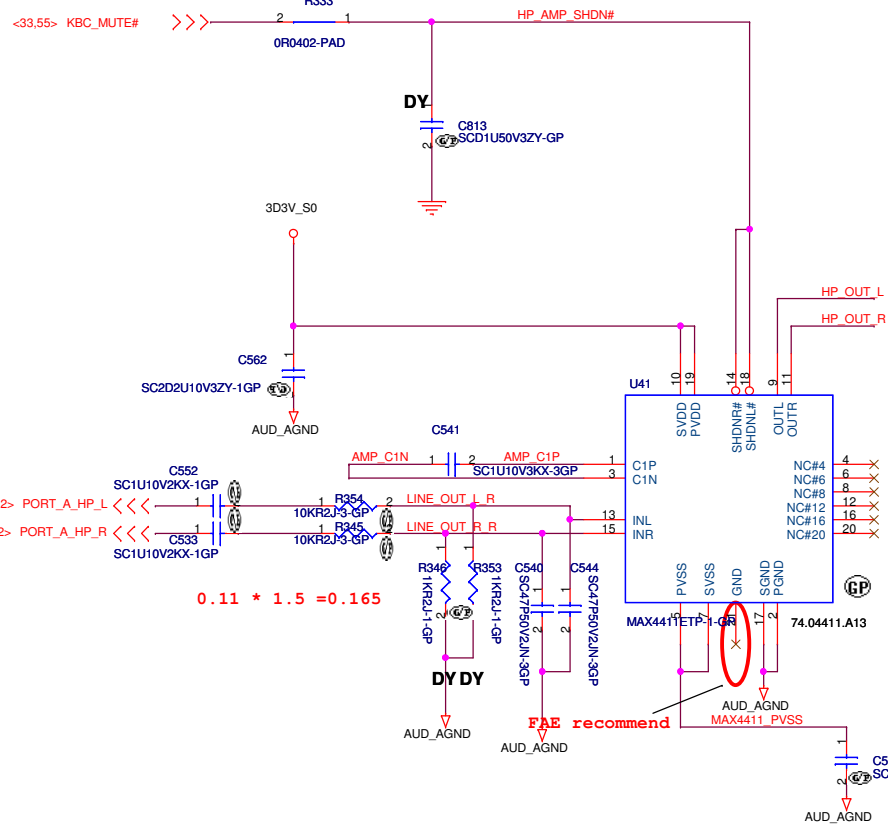
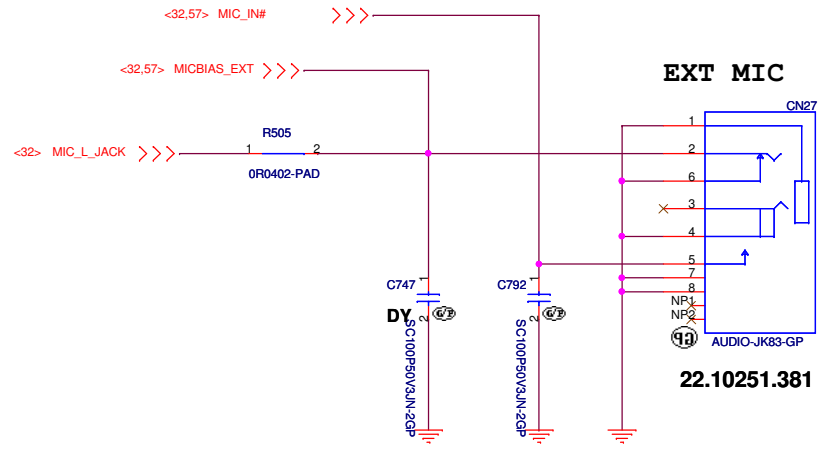
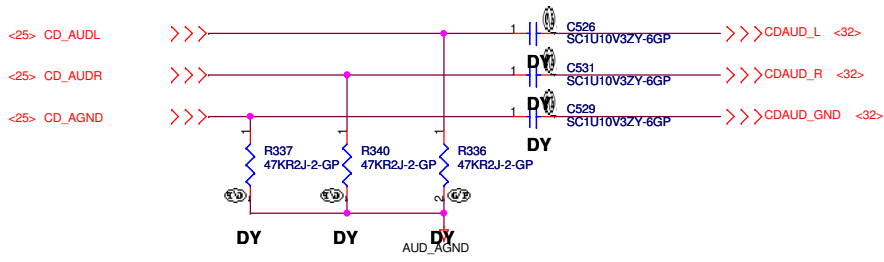


Speaker



A-NOTE2

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO AMP/SPEAKER	
Anote2.0 INTEL	
Title Size B	Document Number Date: Thursday, March 22, 2007
Rev -1	
Sheet 33 of 56	

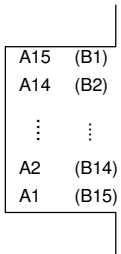


$0.11 * 1.5 = 0.165$

A-NOTE2

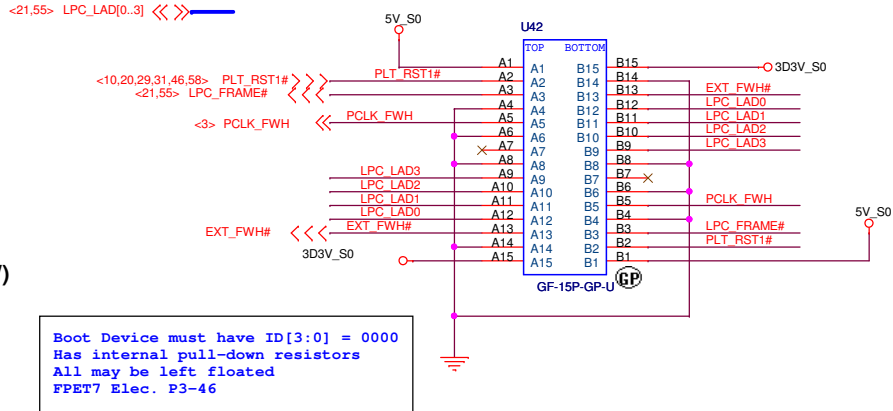
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO HP_JK/ MIC_JK	
Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Sheet 34 of 56

TOP VIEW

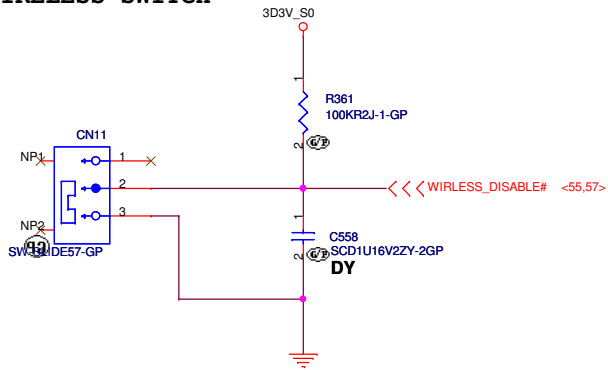


(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

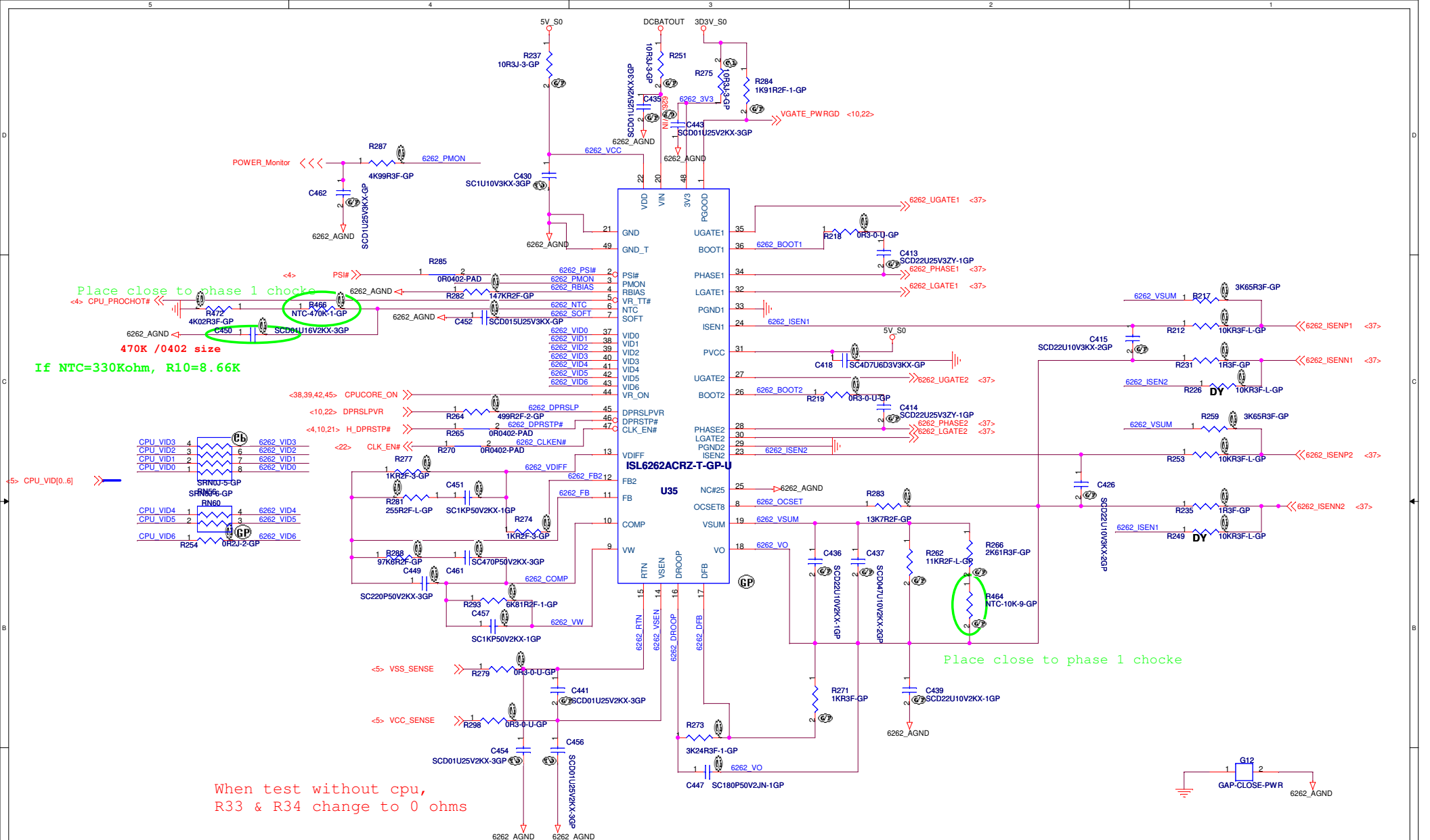


WIRELESS SWITCH



A-NOTE2

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title FWH and Debug			
Size B	Document Number	Anote2.0 INTEL	Rev -1
Date: Thursday, March 22, 2007		Sheet 35 of 56	



Place close to phase 1 choke
 CPU_PROCHOT# <<< R472 4K02R3F-GP
 R466 NTC-470K-1-GP
 C450 SCD01U16V2KX-3GP
 470K /0402 size
 If NTC=330Kohm, R10=8.66K

Place close to phase 1 choke

When test without cpu,
 R33 & R34 change to 0 ohms

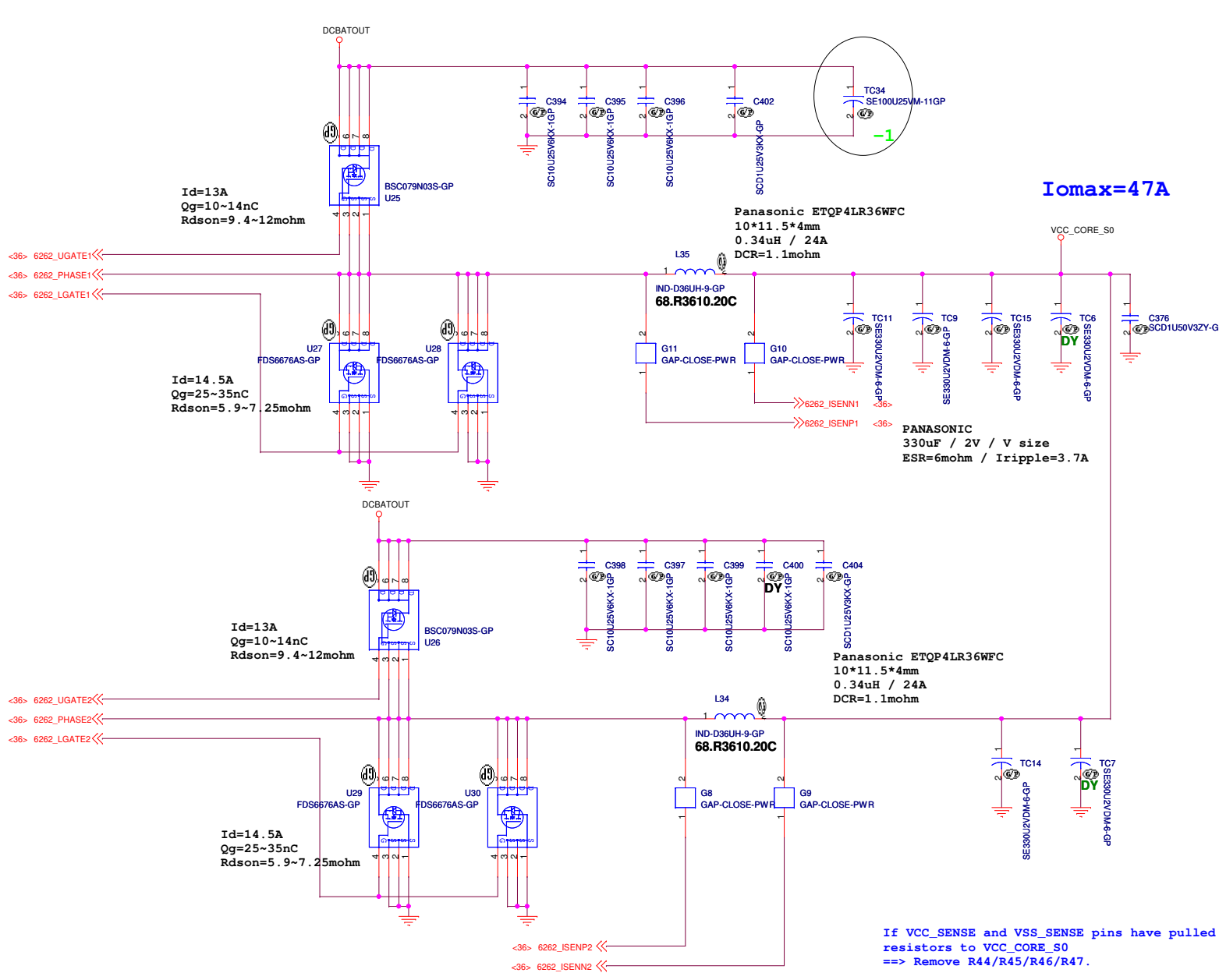
A-NOTE2

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **VCC CORE-1**

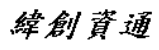
Size A3 Document Number **Anote2.0 INTEL** Rev -1

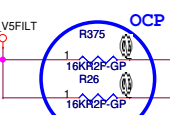
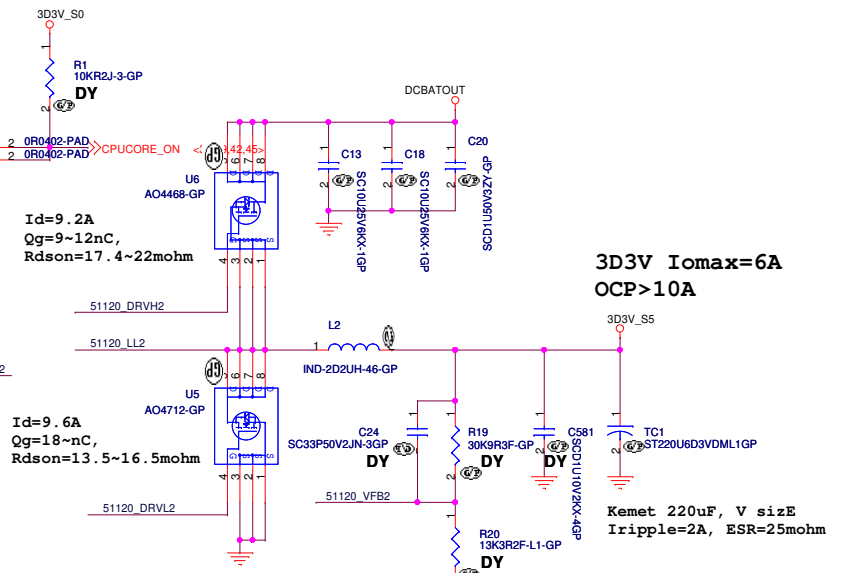
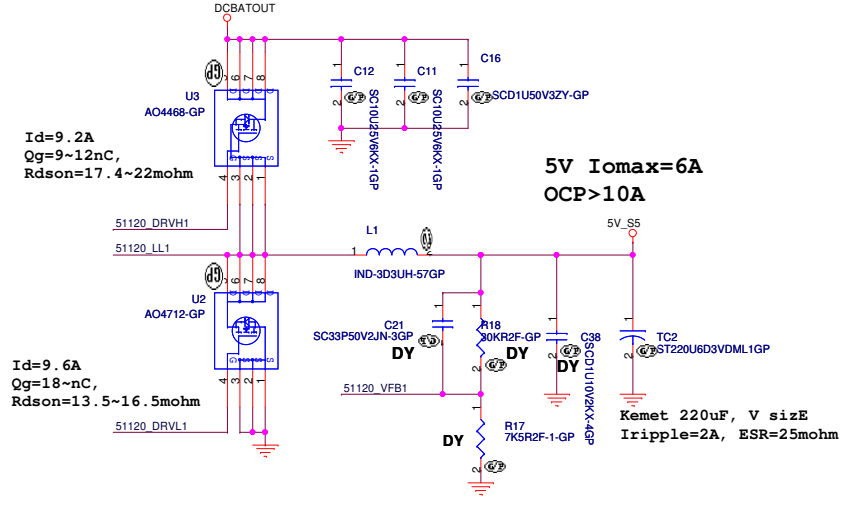
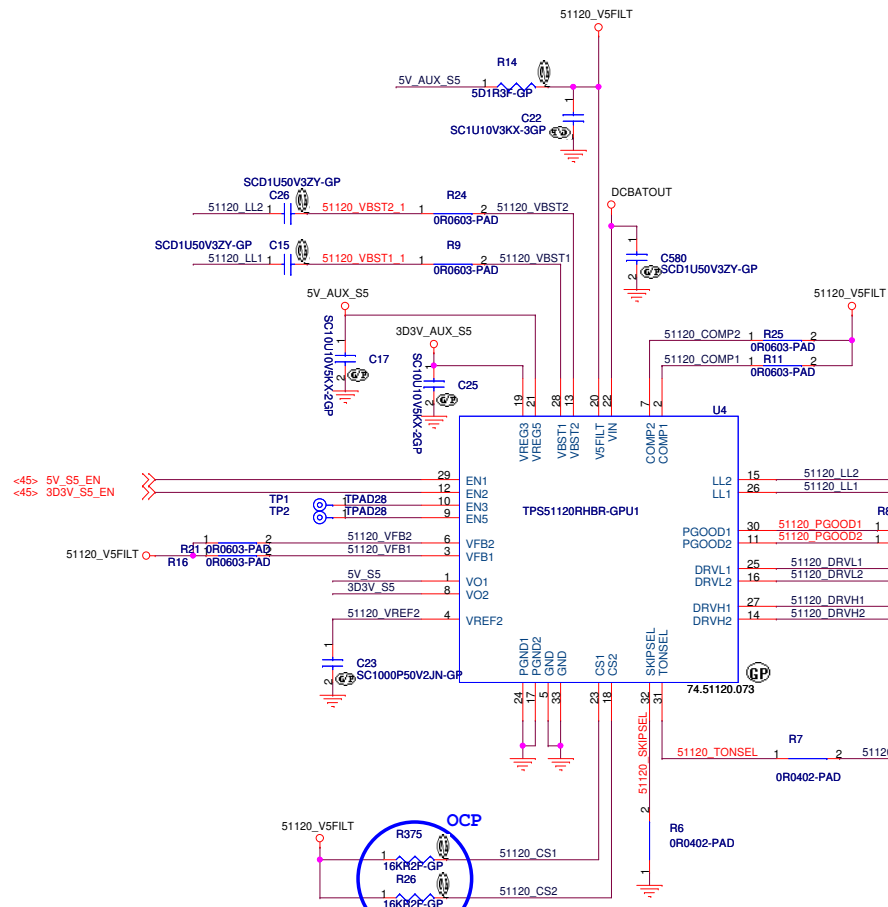
Date: Thursday, March 22, 2007 Sheet 36 of 56



Iomax=47A

A-NOTE2

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
VCC CORE 2	
Size A3	Document Number
Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Rev -1



$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

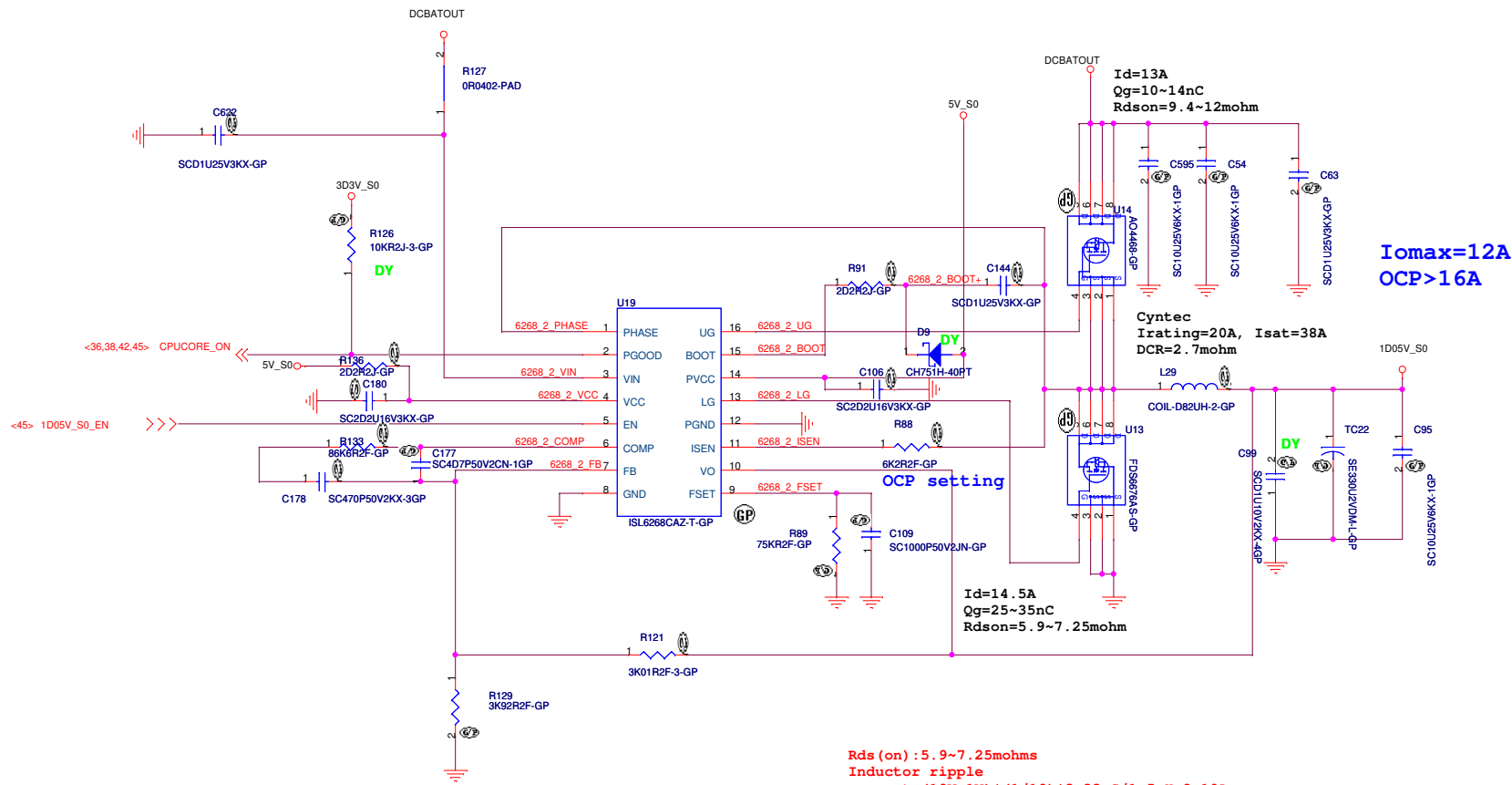
A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120 5V / 3.3V**

Size A3 | Document Number | Rev -1

Date: Thursday, March 22, 2007 | Sheet 38 of 56

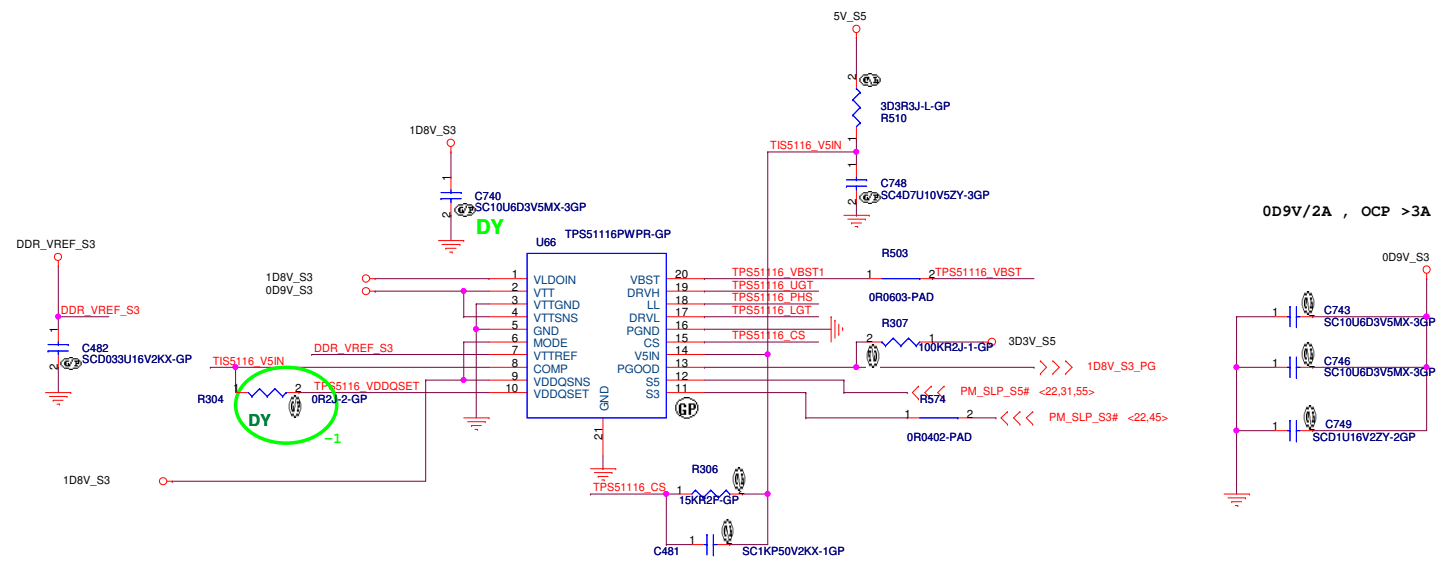


Rds (on) : 5.9~7.25mohms
Inductor ripple
current: $(19V-1V) * (1/19) * 3.33\mu s / 1.5\mu H = 2.10A$
If OCP=16A
Risen = $[16A + (2.1/2)] * (7.5m\Omega * 1.3) / 26\mu A = 6.18K$

A-NOTE2

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 1D05V_S0 ISL6268	
Size A3	Document Number Anote2.0 INTEL
Date: Thursday, March 22, 2007	Rev -1

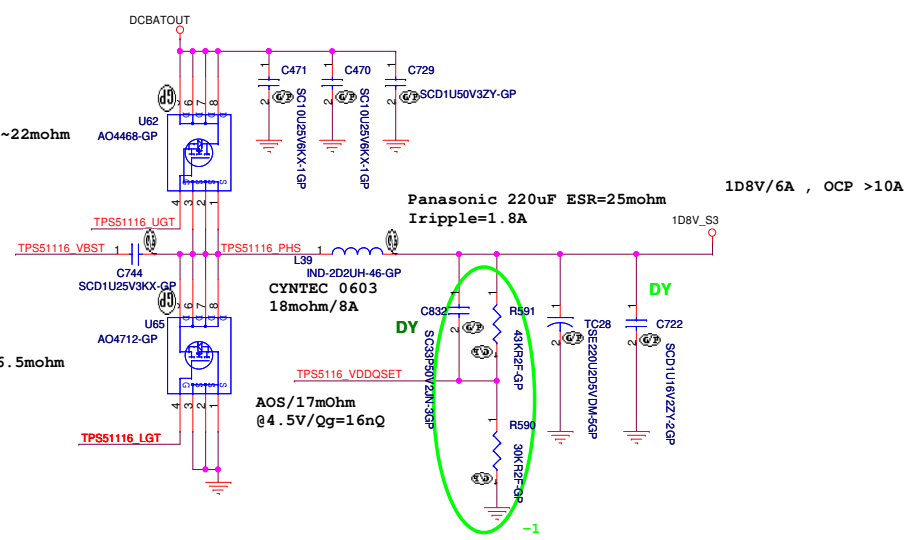
TI TPS51116 for 1D8V and 0D9V



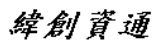
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

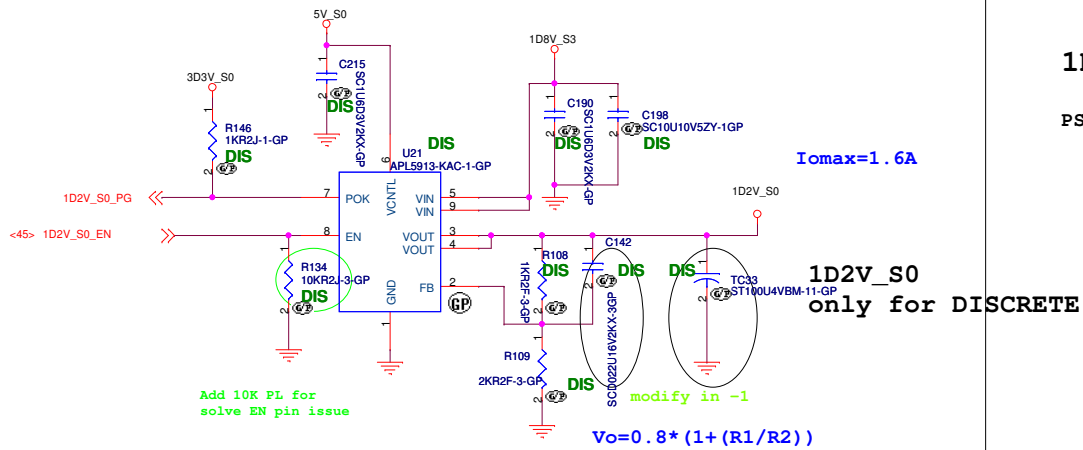
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm



A-NOTE2

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TPS51116 1D8V/0D9V	
Size A3	Document Number
Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Sheet 40 of 56

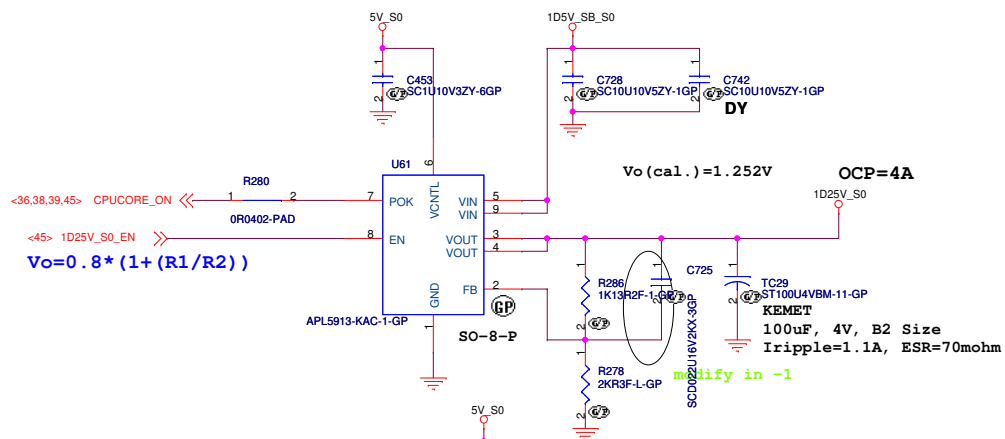
VGA 1.2V Power



1D5V_NB

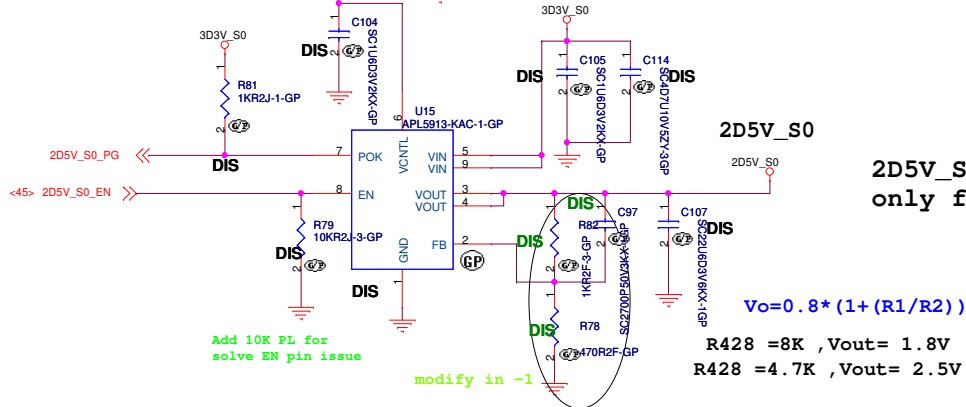
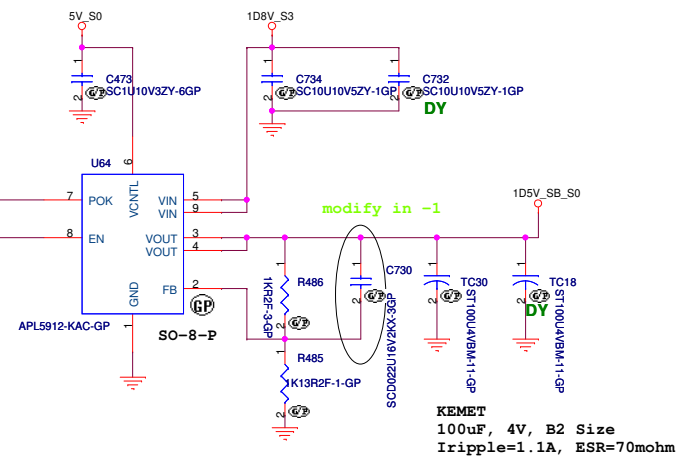
PS: SB del

1D25V_S0 Iomax=2.0A



1D5V_SB

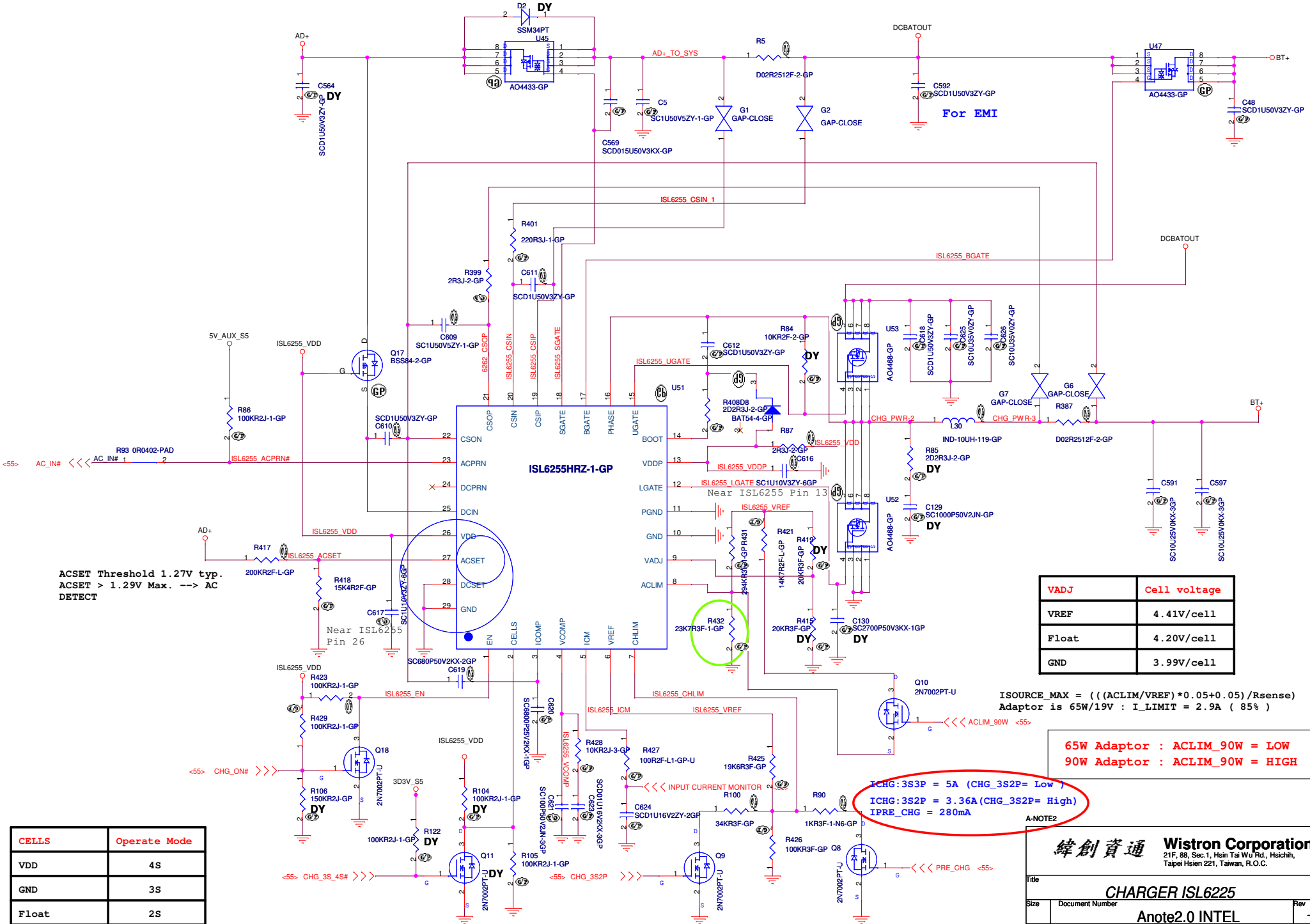
<36,38,39,45> CPUCORE_ON
<45> 1D5V_SB_S0_EN
 $Vo = 0.8 * (1 + (R1/R2))$



2D5V_S0 only for DISCRETE

A-NOTE2

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title 1D2V_VGA/2D5V/1D25V/1D5V LDO			
Size	Document Number	Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Sheet 42	of	56



ACSET Threshold 1.27V typ.
 ACSET > 1.29V Max. ---> AC
 DETECT

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = ((ACLIM/VREF)*0.05+0.05)/Rsense
 Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

65W Adaptor : ACLIM_90W = LOW
 90W Adaptor : ACLIM_90W = HIGH

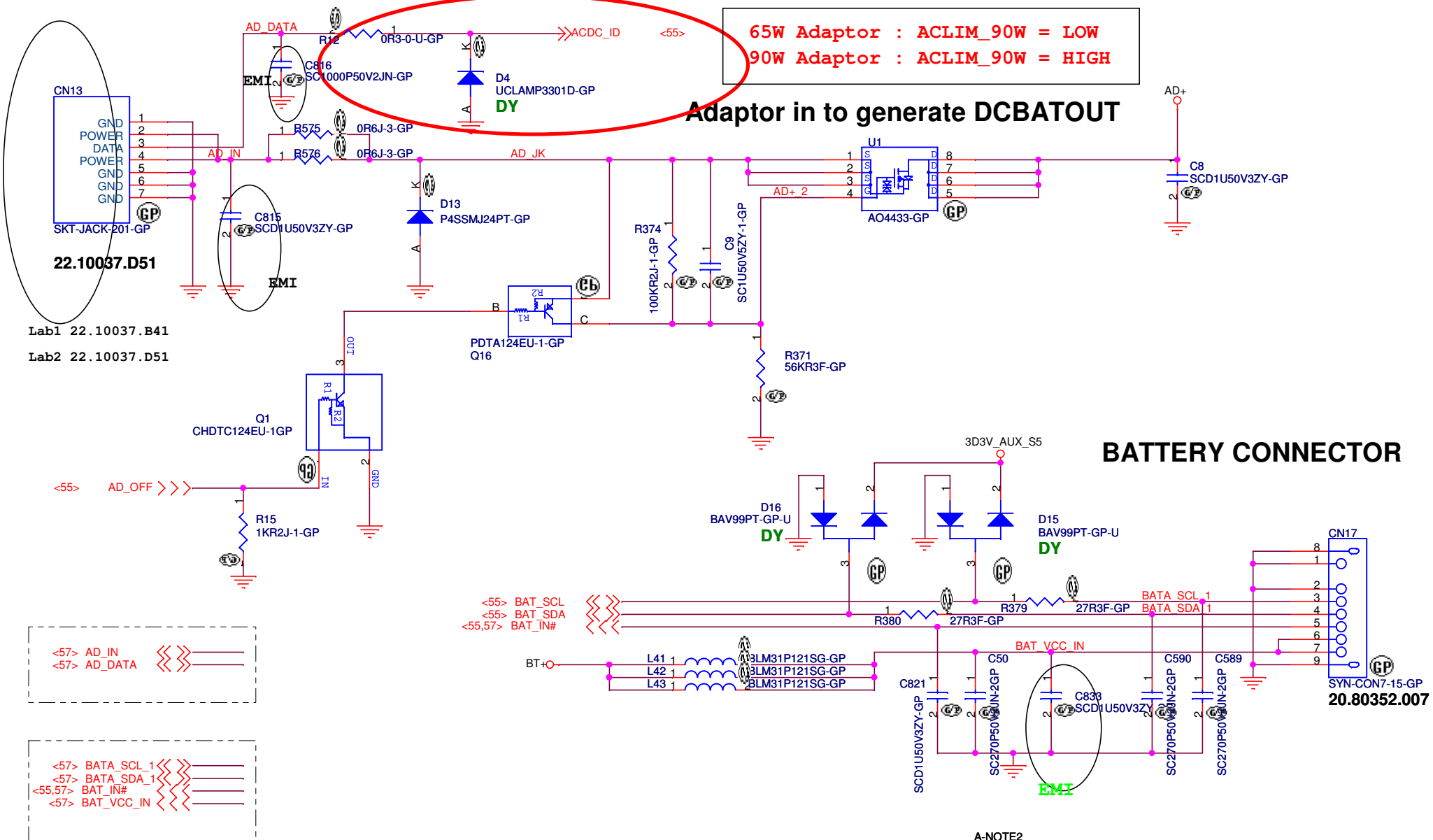
ICHG:3S3P = 5A (CHG_3S2P= Low)
 ICHG:3S2P = 3.36A (CHG_3S2P= High)
 IPRE_CHG = 280mA

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
 Taipei Hsein 221, Taiwan, R.O.C.

File: CHARGER ISL6225
 Size: Document Number
 Date: Thursday, March 22, 2007 Sheet 43 of 56

A-NOTE2
 Anote2.0 INTEL -1



65W Adaptor : ACLIM_90W = LOW
 90W Adaptor : ACLIM_90W = HIGH

Adaptor in to generate DCBATOUT

BATTERY CONNECTOR

22.10037.D51

Lab1 22.10037.B41

Lab2 22.10037.D51

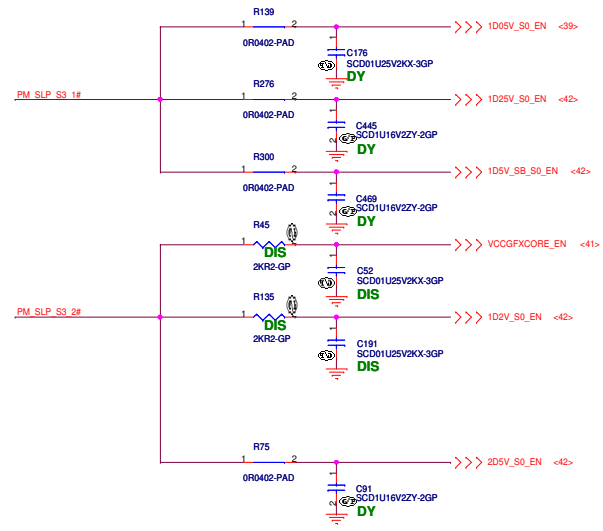
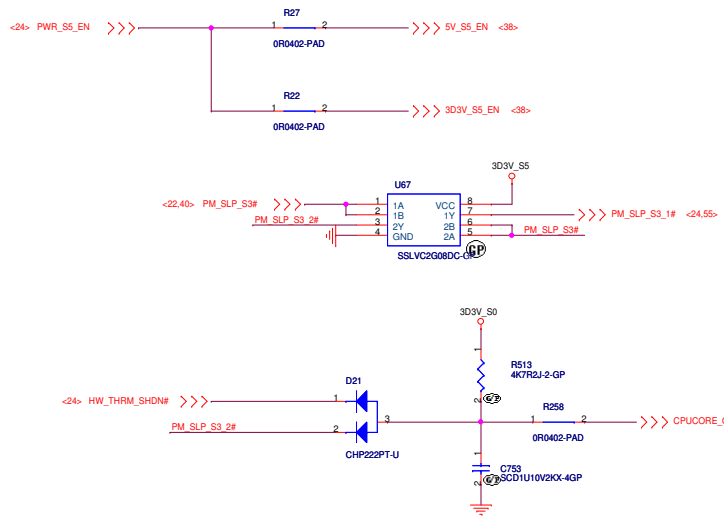
20.80352.007

<57> AD_IN
 <57> AD_DATA

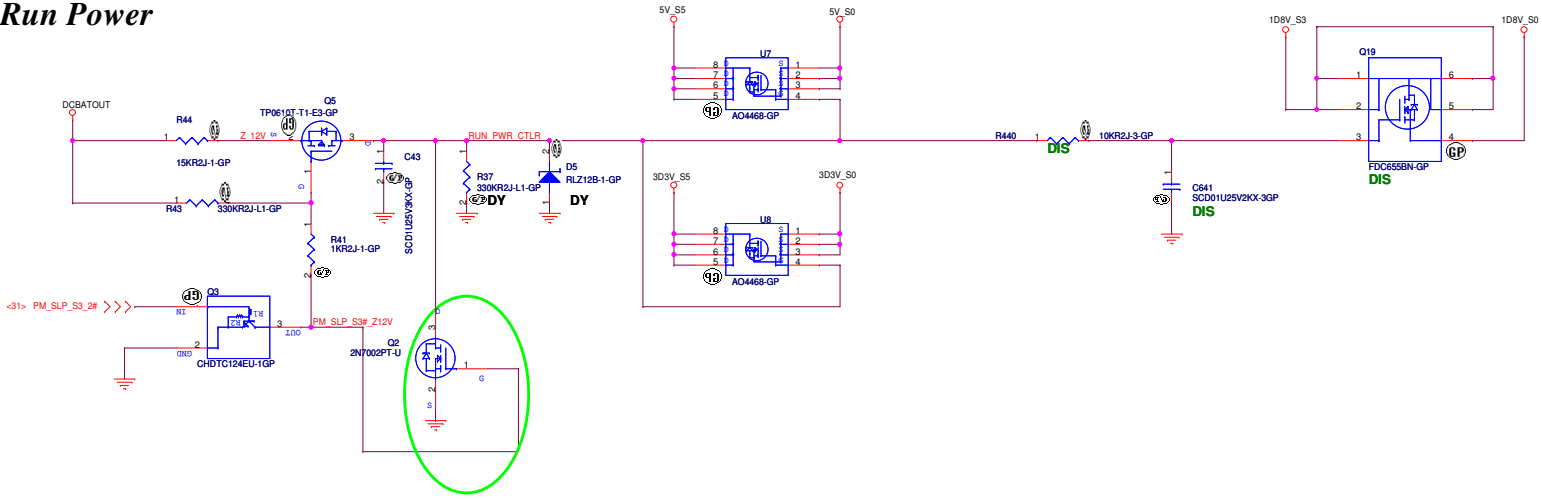
<57> BATA_SCL_1
 <57> BATA_SDA_1
 <55,57> BAT_IN#
 <57> BAT_VCC_IN

A-NOTE2

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AD/BATT CONN	
Size	Document Number
Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Rev -1



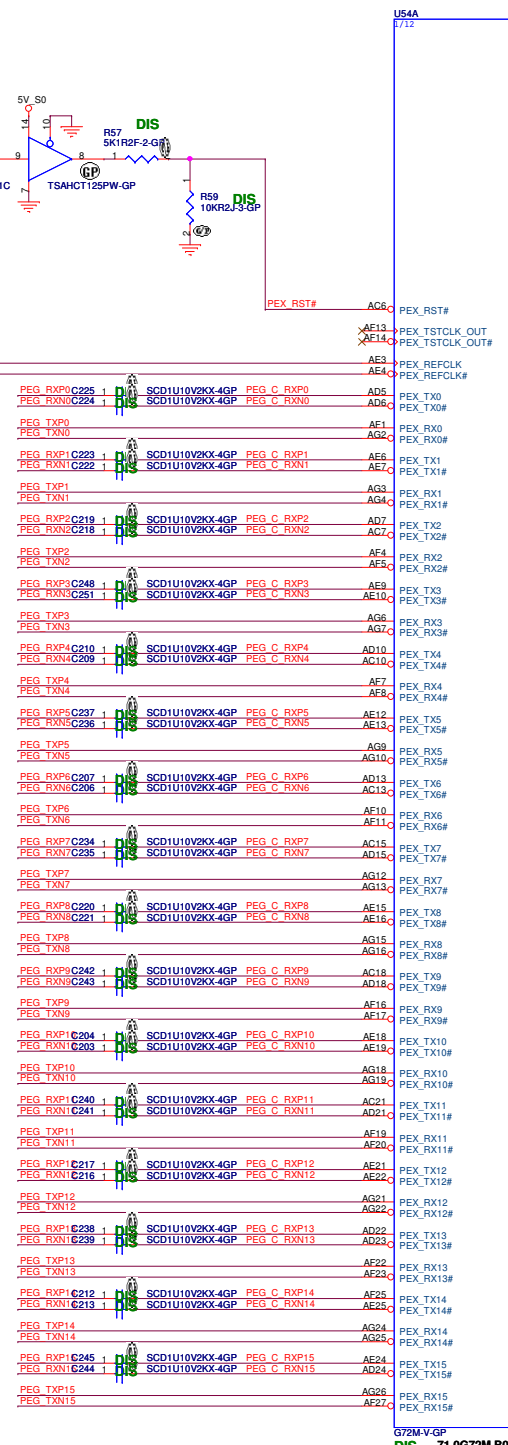
Run Power



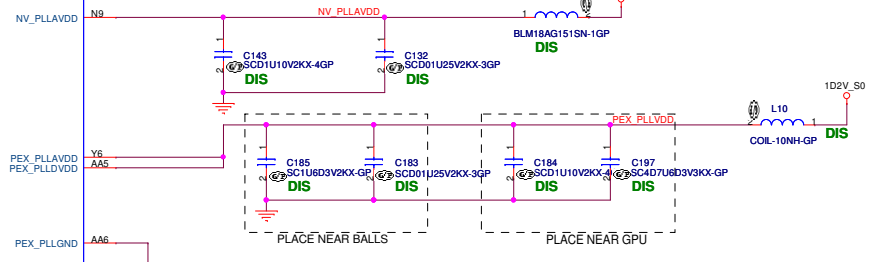
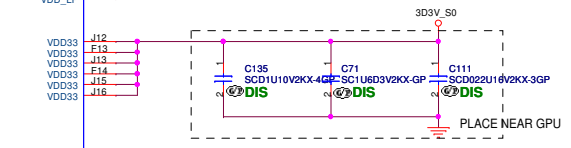
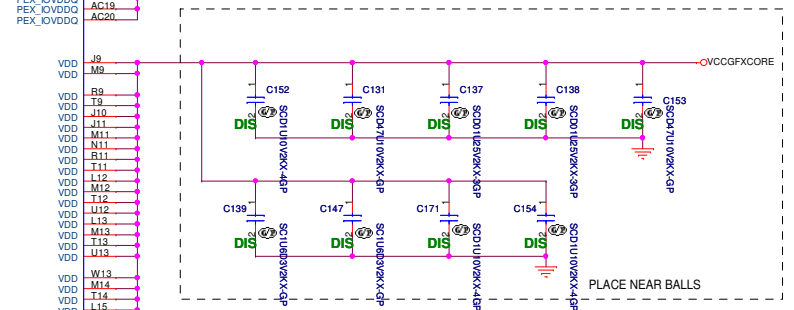
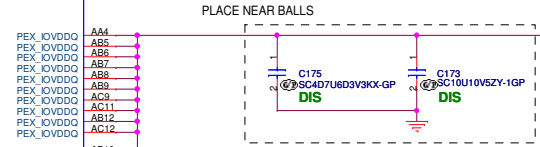
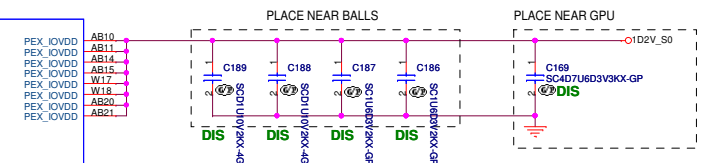
<10,20,29,31,35,58> PLT_RST#

<3> CLK_POE_GFX
<3> CLK_POE_GFX#

<11> PEG_TXN[15..0]
<11> PEG_TXP[15..0]
<11> PEG_RXN[15..0]
<11> PEG_RXP[15..0]



G72M-V-GP
DIS 71.0G72M.B0U



NC#D12
NC#E12
NC#F12
NC#C13

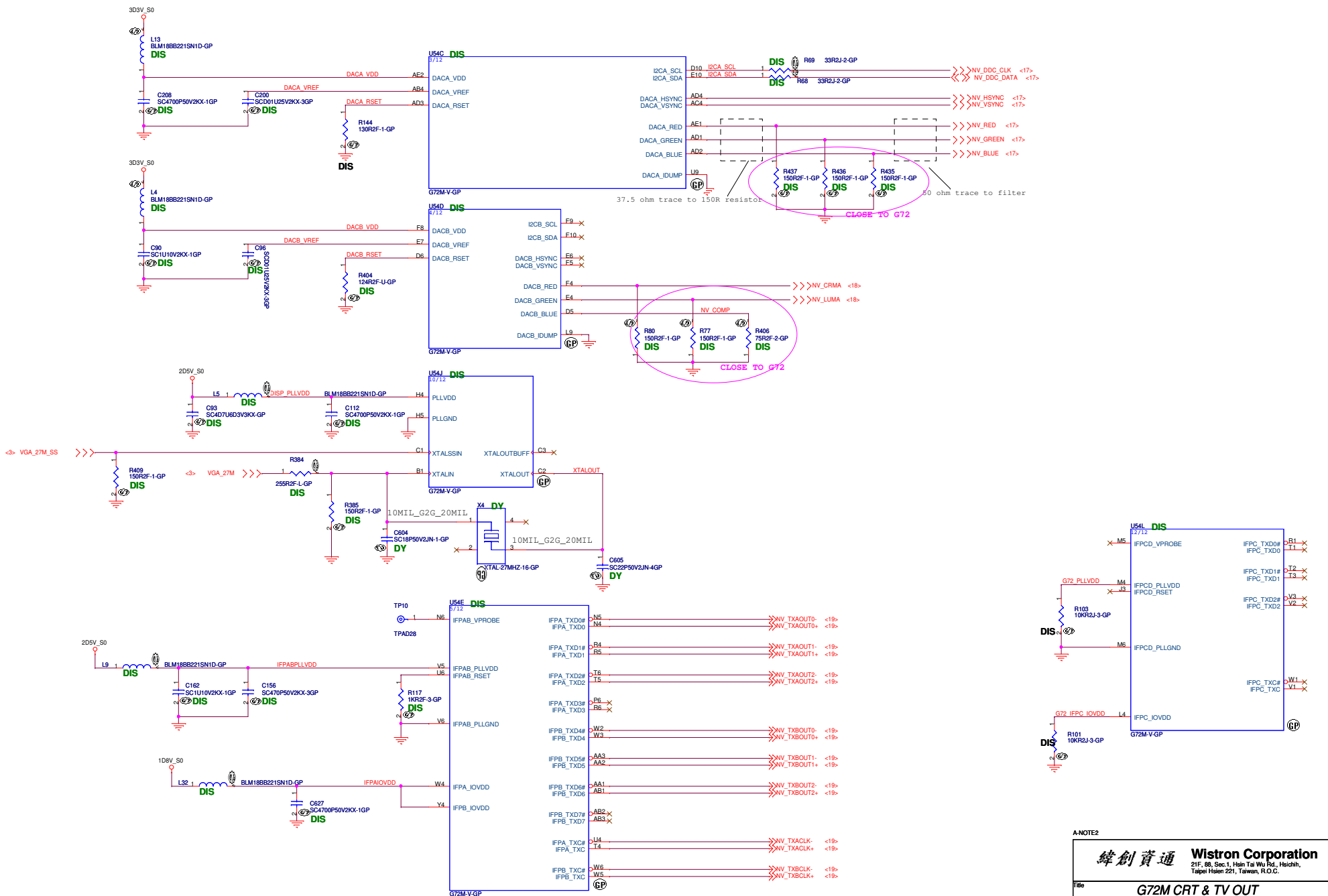
A-NOTE2

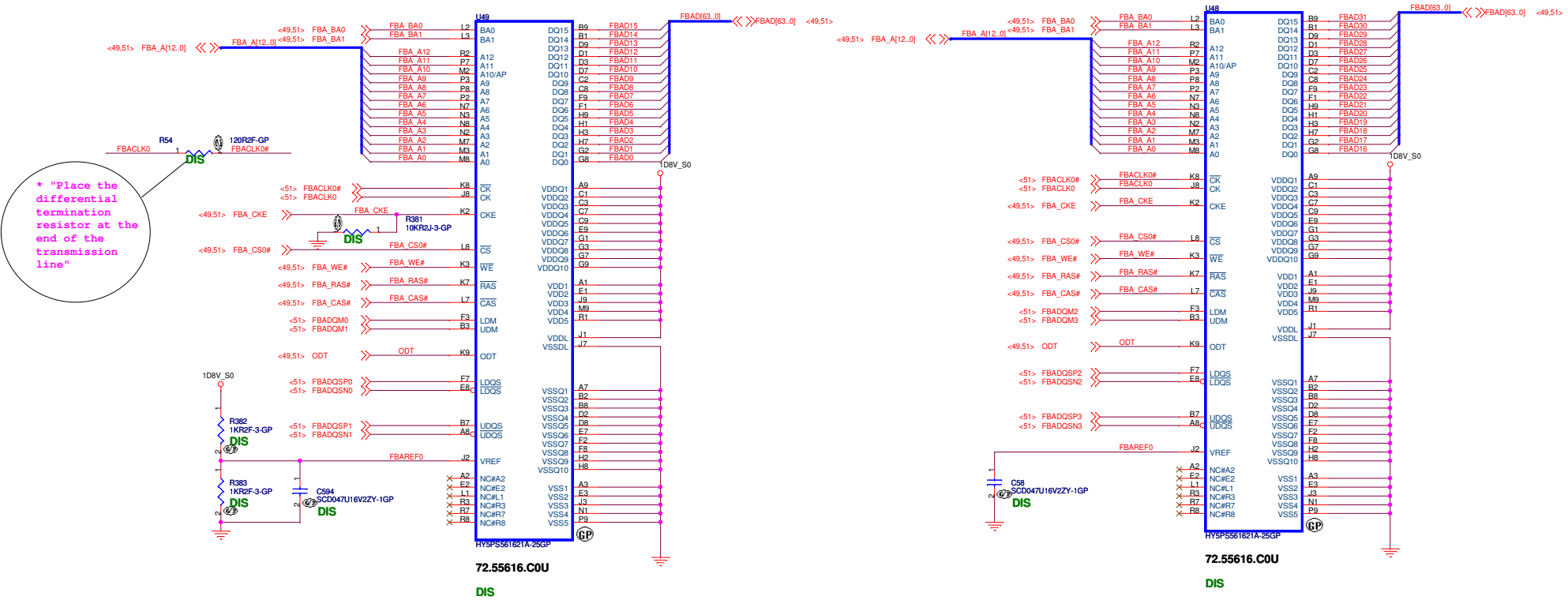
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G72M PCIE**

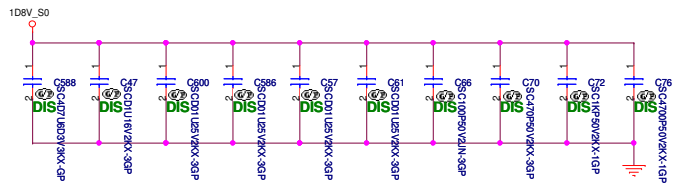
Size: Document Number: **Anote2.0 INTEL** Rev: **-1**

Date: Thursday, March 22, 2007 Sheet: 46 of 56

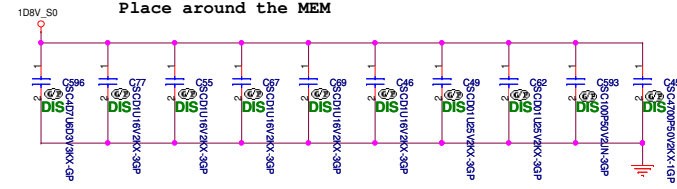




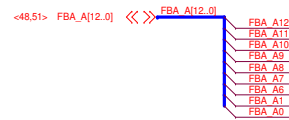
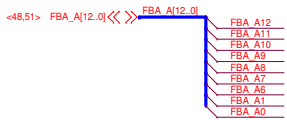
Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM

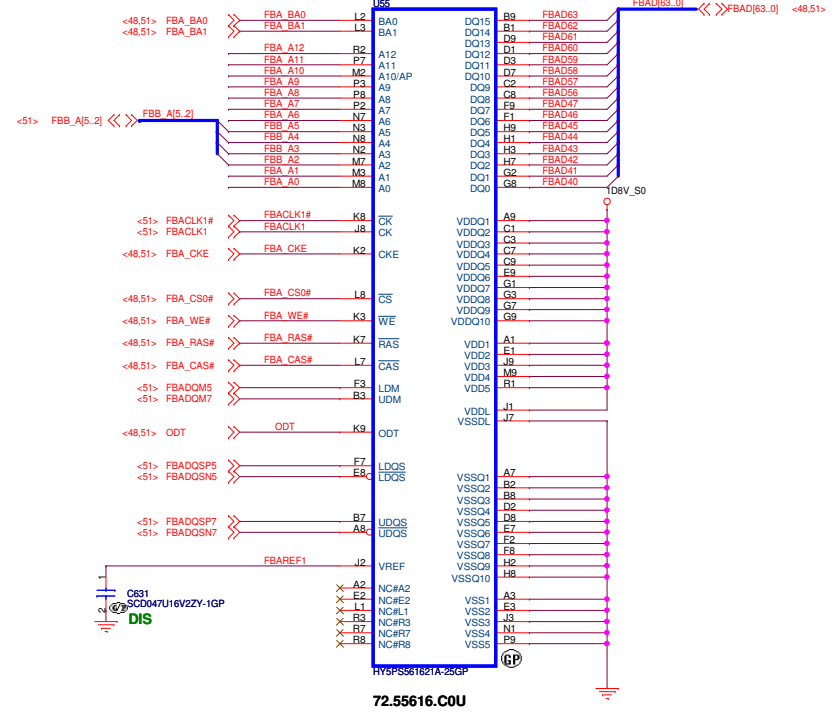
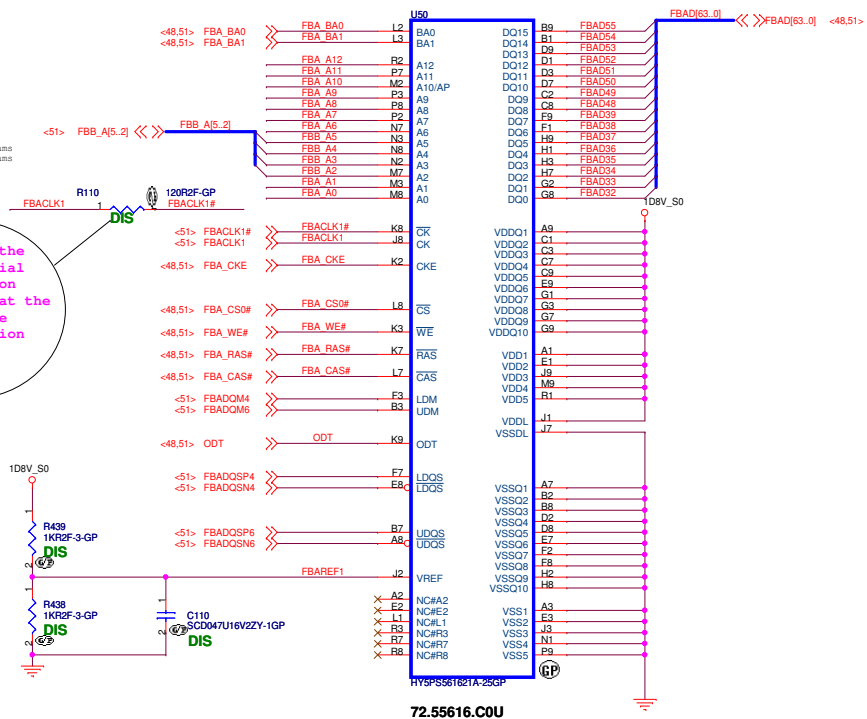


72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)

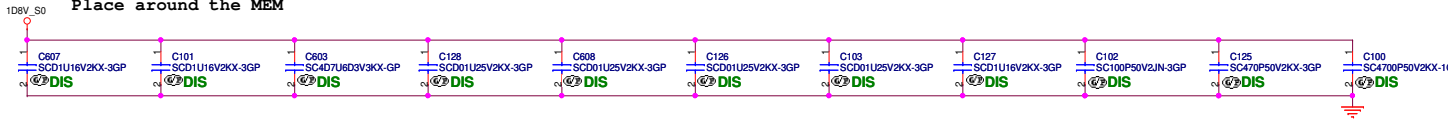


for G73M use 120 ohms
for G73M use 480 ohms

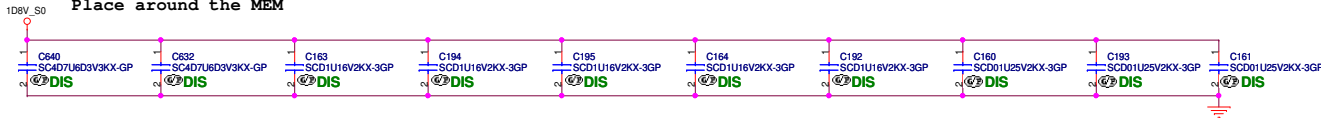
* "Place the differential termination resistor at the end of the transmission line"



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



A-NOTE2

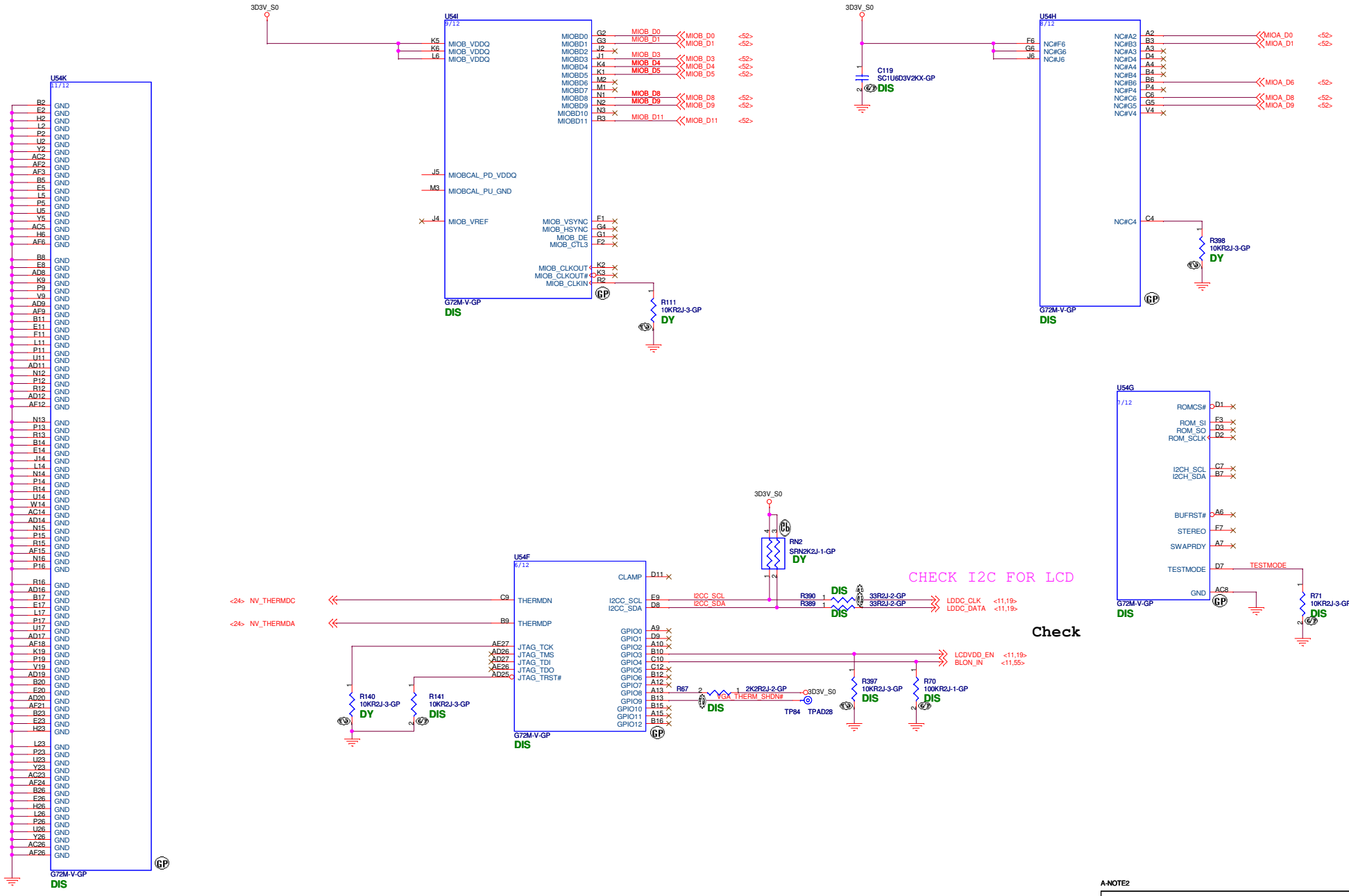
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: G72M VRAM (1ST 2/2)

Size: Document Number

Anote2.0 INTEL

Date: Thursday, March 22, 2007 Sheet 49 of 56



A-NOTE2

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **G72M ROM & Spread Spectrum**

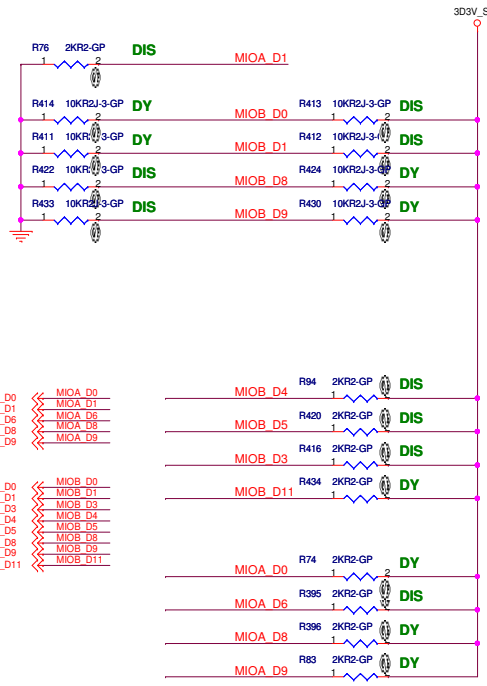
Size: Document Number Rev: -1

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STRAPS, Mechanical Parts

Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0



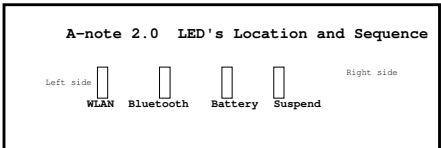
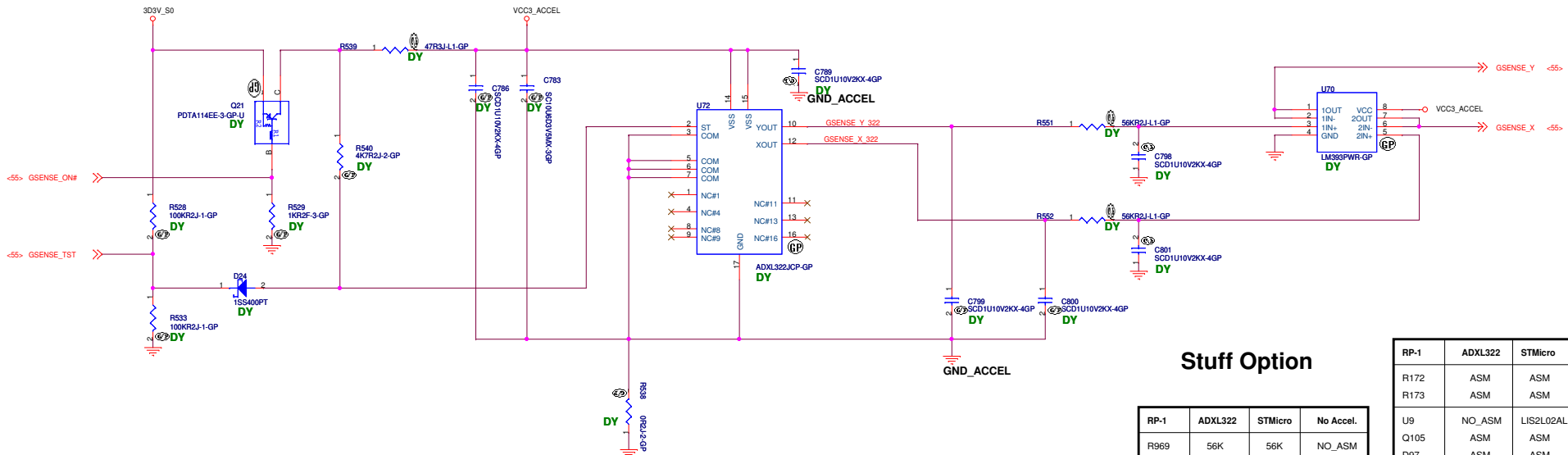
- <-50> MIOA_D0 << MIOA_D0
- <-50> MIOA_D1 << MIOA_D1
- <-50> MIOA_D6 << MIOA_D6
- <-50> MIOA_D8 << MIOA_D8
- <-50> MIOA_D9 << MIOA_D9
- <-50> MIOB_D0 << MIOB_D0
- <-50> MIOB_D1 << MIOB_D1
- <-50> MIOB_D3 << MIOB_D3
- <-50> MIOB_D4 << MIOB_D4
- <-50> MIOB_D5 << MIOB_D5
- <-50> MIOB_D8 << MIOB_D8
- <-50> MIOB_D9 << MIOB_D9
- <-50> MIOB_D11 << MIOB_D11

Bit Signal	Values
MIOA_D1: SUB_VENDOR	0 NO BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

RAM_CFG[9.8.1.0]	Config	FB Bus Width	Definitions
RAM_CFG[3..0]			
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

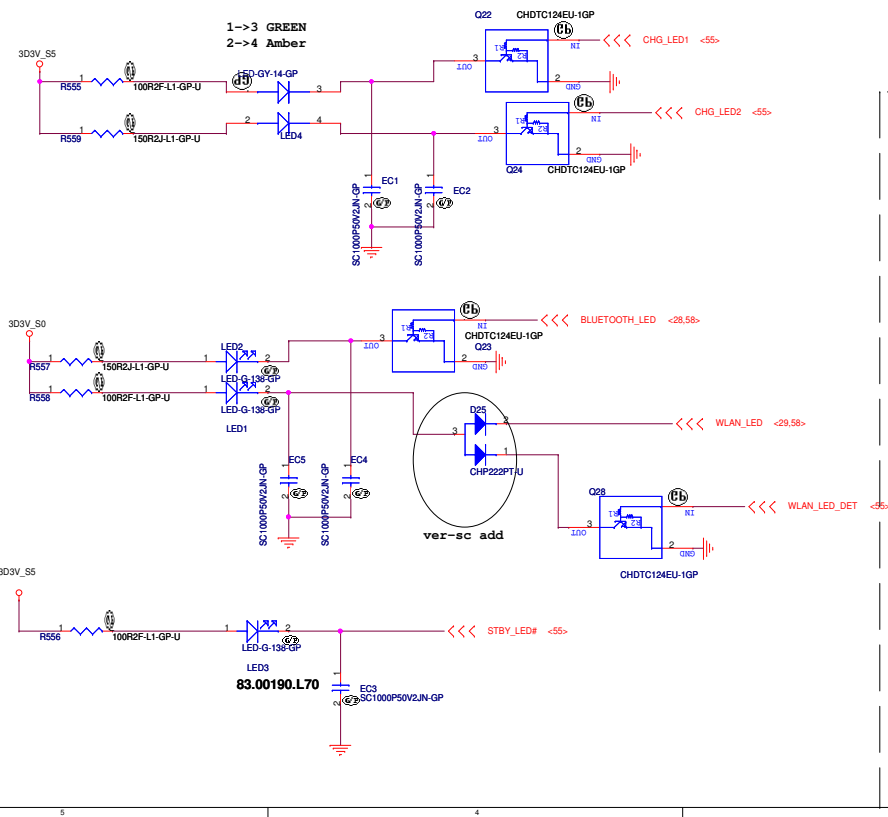
MIOB_D4: PCI_DEVID_0	
MIOB_D5: PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3: PCI_DEVID_2	
MIOB_D11: PCI_DEVID_3	0111 G72MV G72MZ=6, G73=8
MIOA_D0: PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT



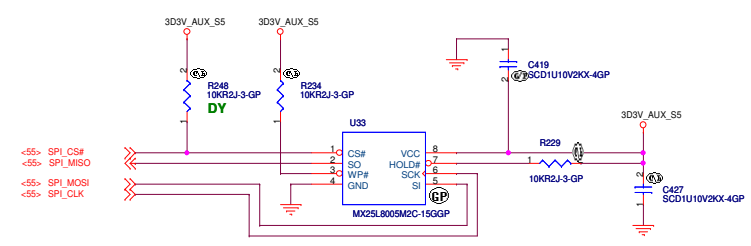
Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM



SPI ROM for System & KBC



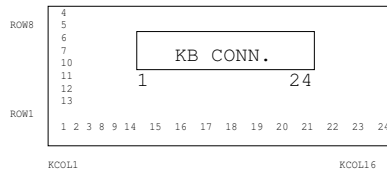
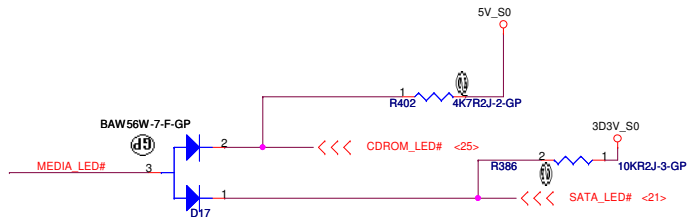
1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01

A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hein Tai Wu Rd., Hsichü,
Taipei Hsien 221, Taiwan, R.O.C.

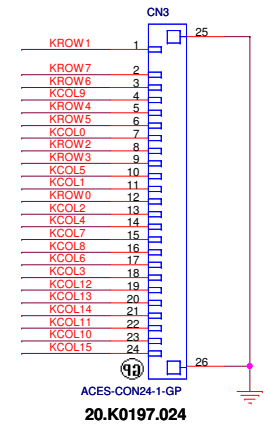
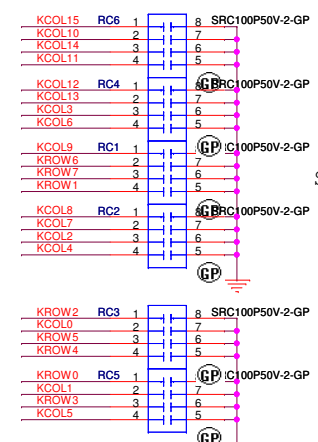
G-sensor / SPI / LEDs

File: _____
Size: _____ Document Number: _____ Rev: **-1**
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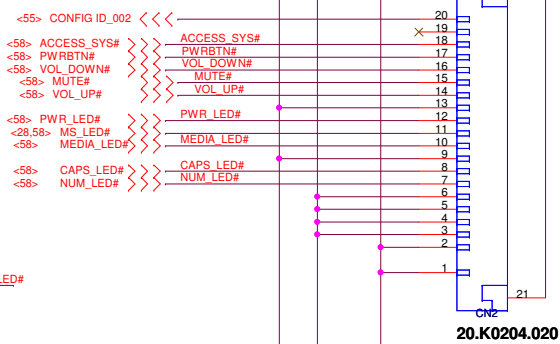
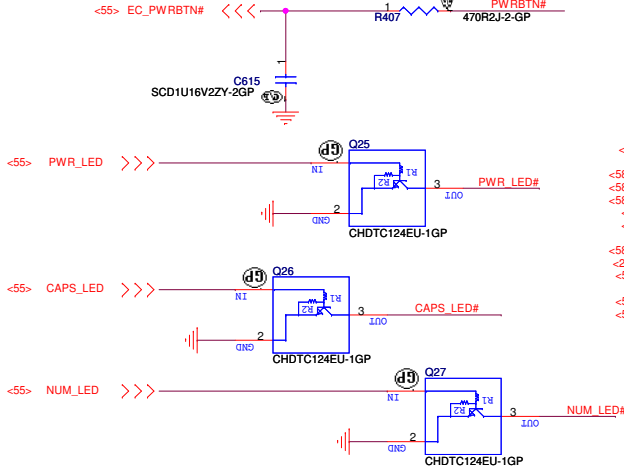


Internal Keyboard Connector

<55,57> KROW[0..7] <<<
<55,57> KCOL[0..15] <<<

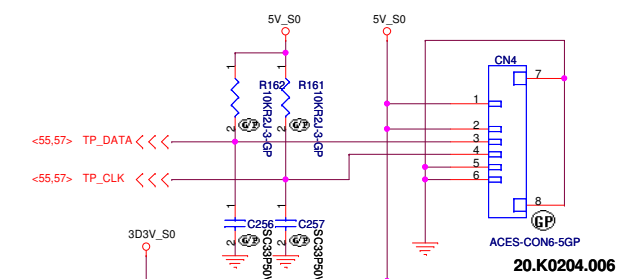


Lanuch Board CNN

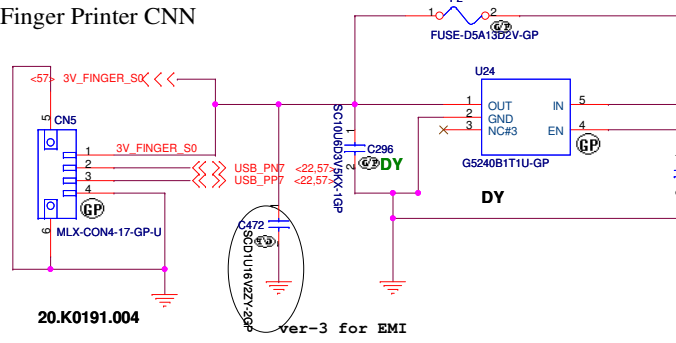
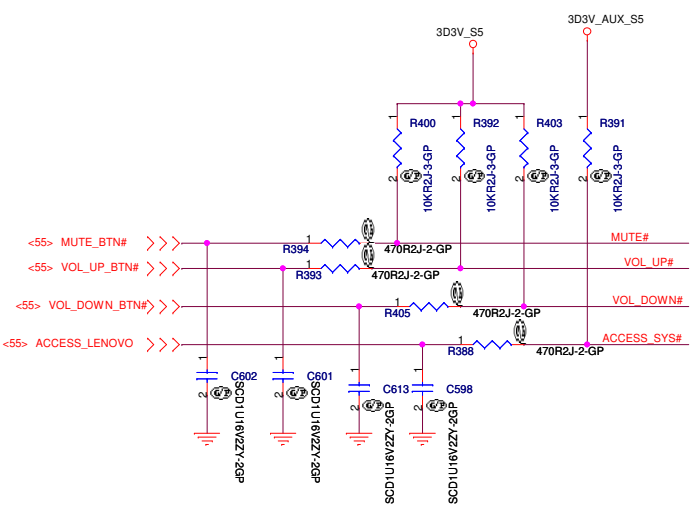


LAB2 20.K0204.020

TouchPad Connector

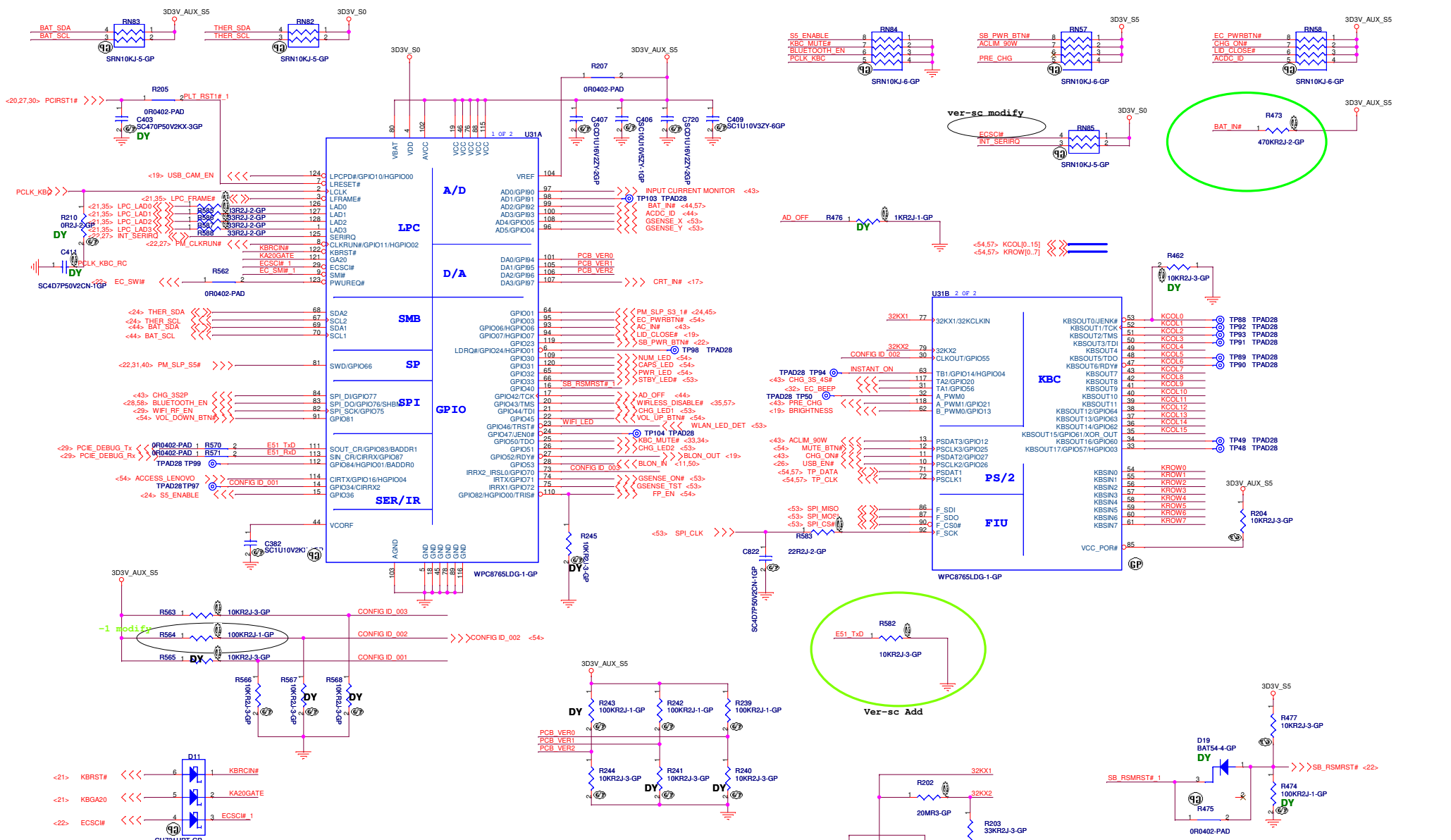


Finger Printer CNN



A-NOTE2

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Keyboard /Touch Pad	
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CONFIG_ID	PIN	0	1
001	GPIO34	A-Note2	F-Note2
002	GPIO55	China	WW
003	GPIO70	AMD	Intel

PID_LAB1 = 000b ; Lab1
 PID_LAB2 = 001b ; Lab2
 PID_ENG = 010b ; ENG
 PID_PD = 011b ; PD

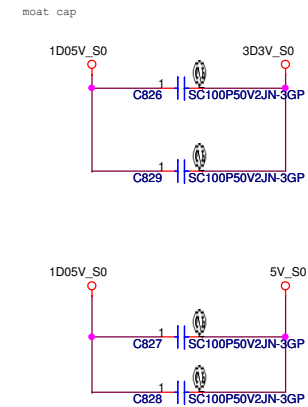
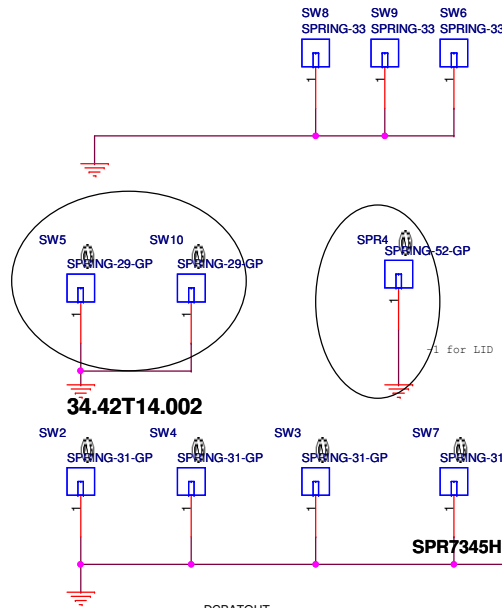
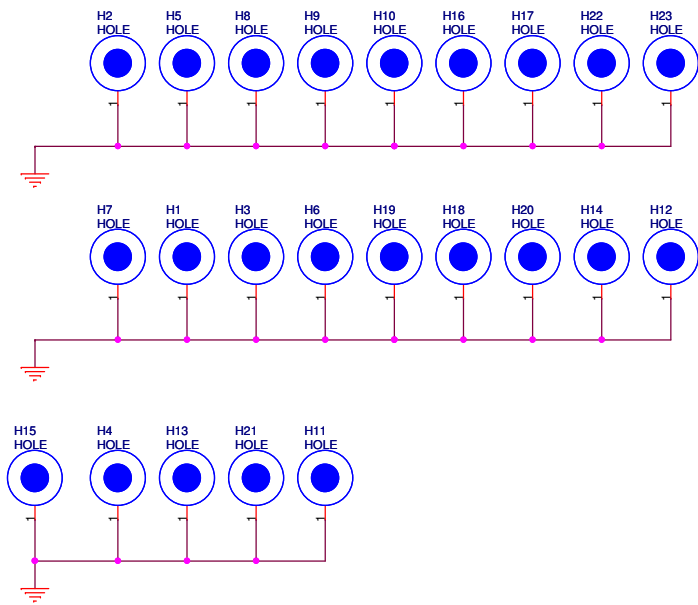
A-NOTE2

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC WPC8765L**

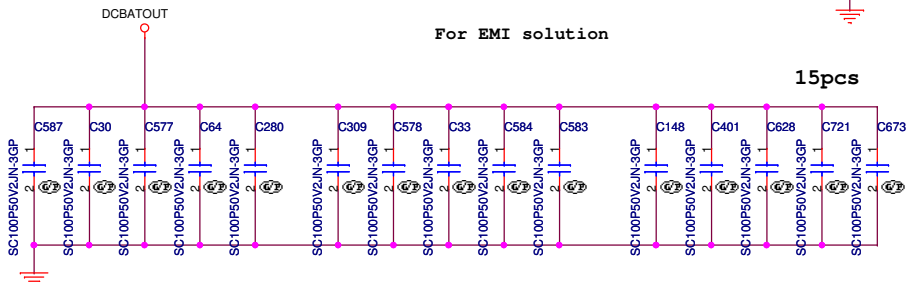
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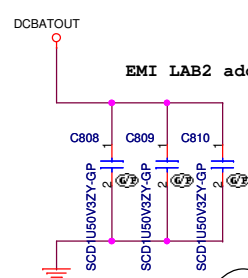


For EMI solution

15pcs

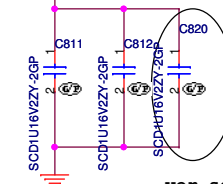


EMI LAB2 add

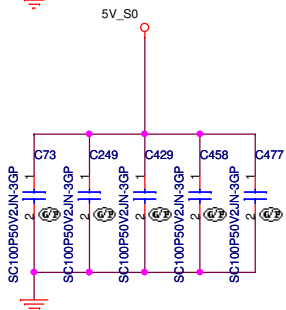


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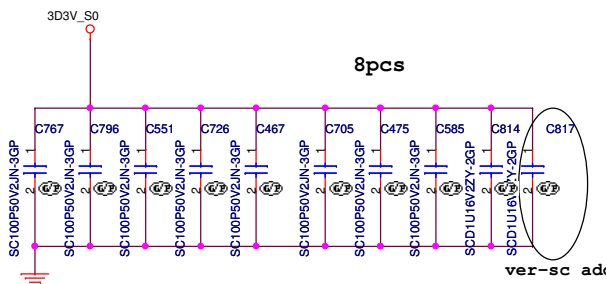
5V_S5



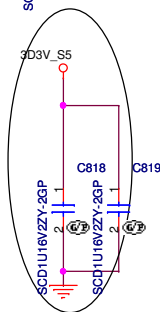
5pcs



8pcs



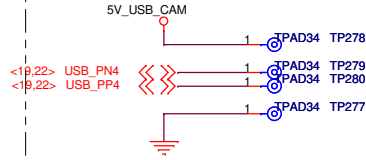
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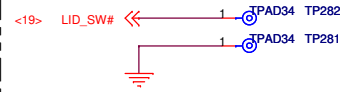
A-NOTE2

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Title		HOLE/ SPRING	
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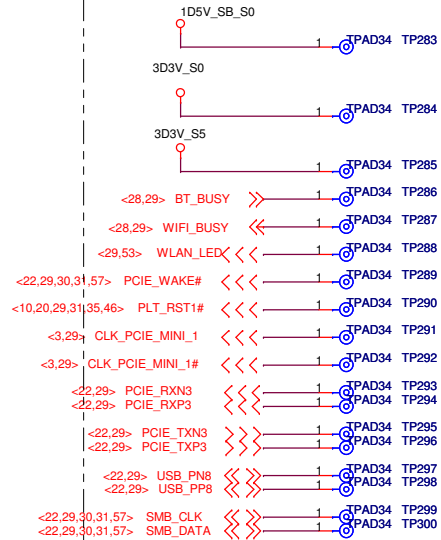
Near LCD CNN--CAM



Near SW1



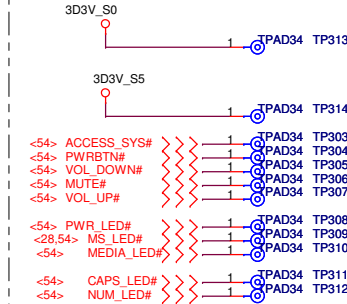
Near CN25--Mini -PCIE



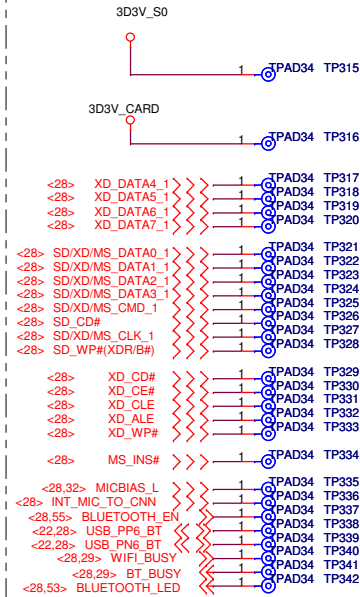
Modem



Launch-BD



Daughter-BD



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TEST_PAD		
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