

Compal Confidential

NAWA2 Schematics Document

AMD Tigris: Caspian Processor with RS880M/SB710/Park-S3 & M93-S3

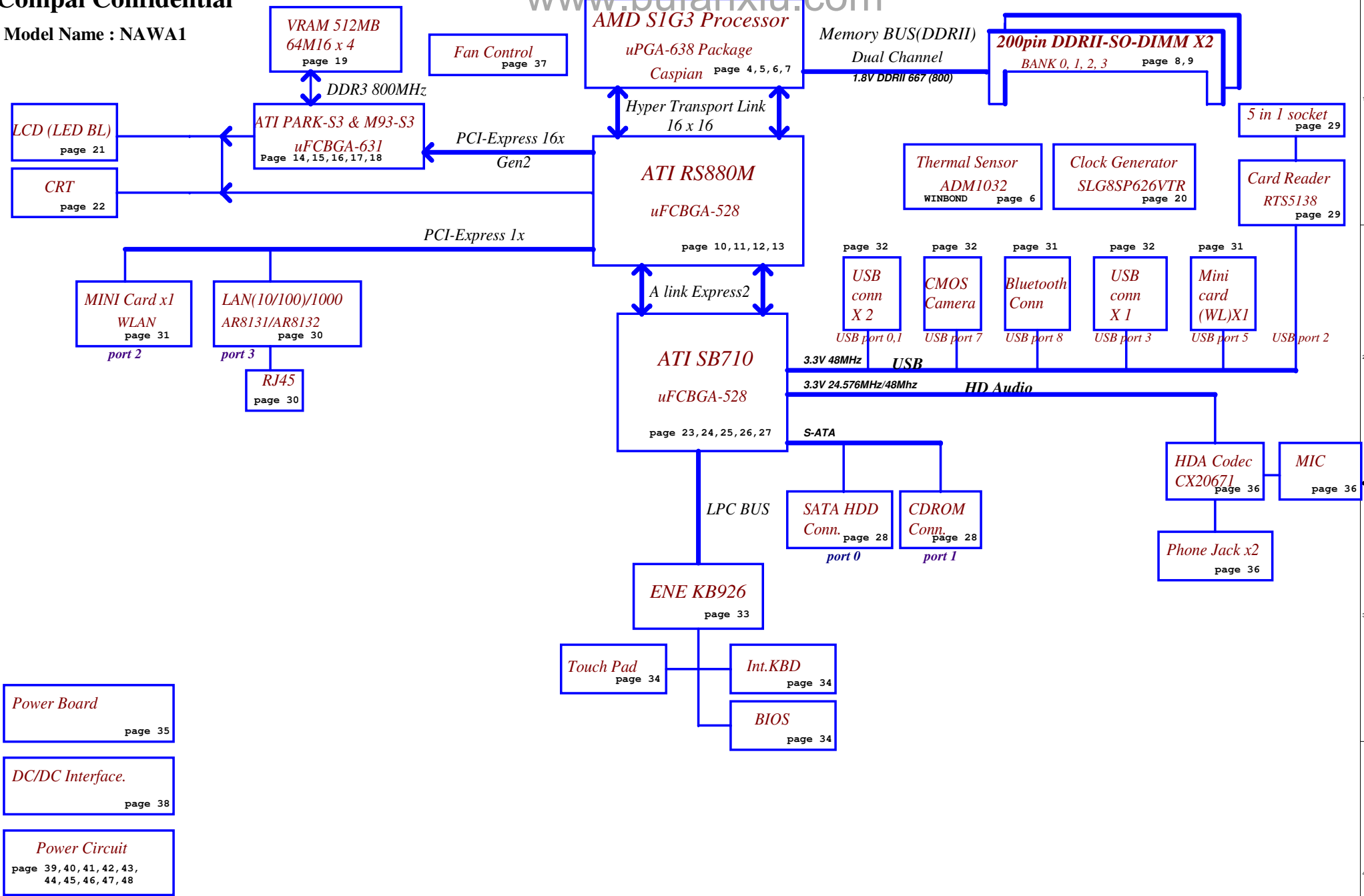
2009-11-26

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Model Name : NAWA1

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				Rev	1.0

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BTO Option Table

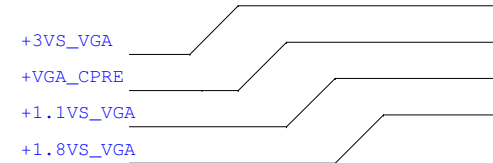
BTO Item	BOM Structure
Discrete	VGA@
PARK	PARK@
M93	M93@
HDT debug	HDT@
UMA	UMA@
Wireless LAN	WLAN@
Blue Tooth	BT@
Camera	CMOS@
New Card	New Card@
VRAM	X76@
UNPON	@

SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	CLock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF

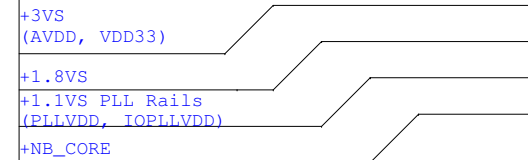
NAWA1_UMA : UMA@/WLAN@/BT@/CMOS@/NEW_CARD@

NAWA1_DIS : VGA@/M93@/WLAN@/BT@/NEW_CARD@/CMOS@/X76@

PARK-S3 power on sequence



RS880M power on sequence



External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

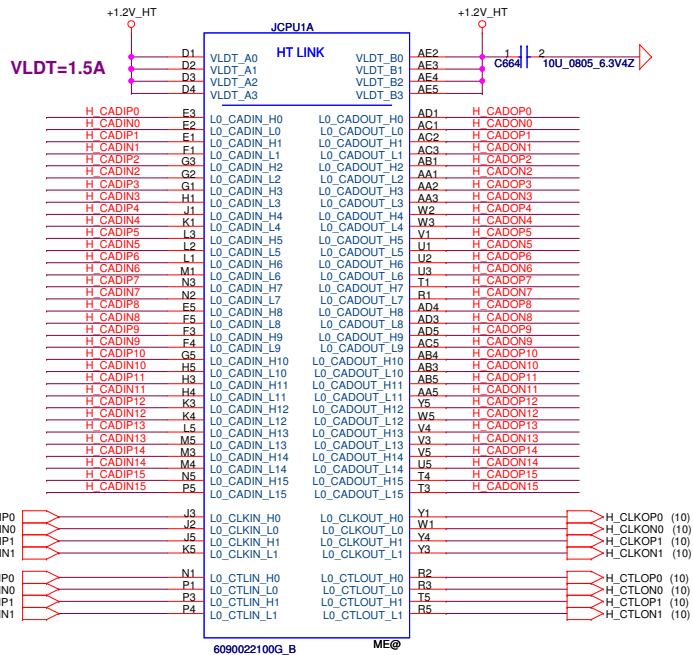
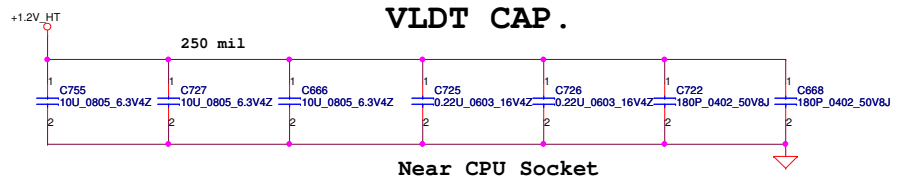
EC SM Bus2 address

SB710 SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP26)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

SB710 SM Bus 1 address

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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR WITHIN 1.2 INCH

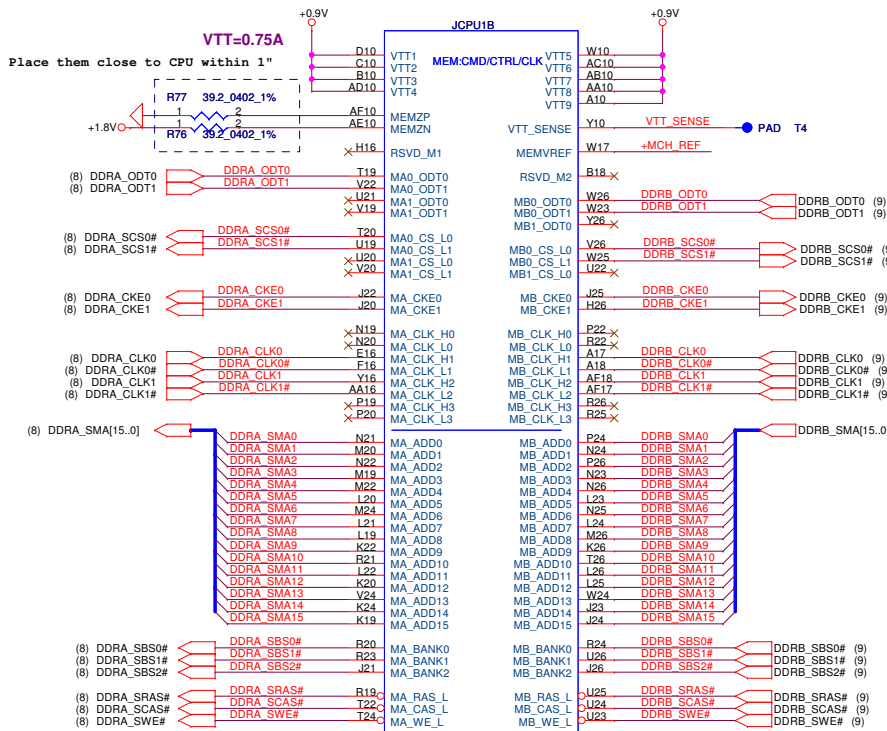
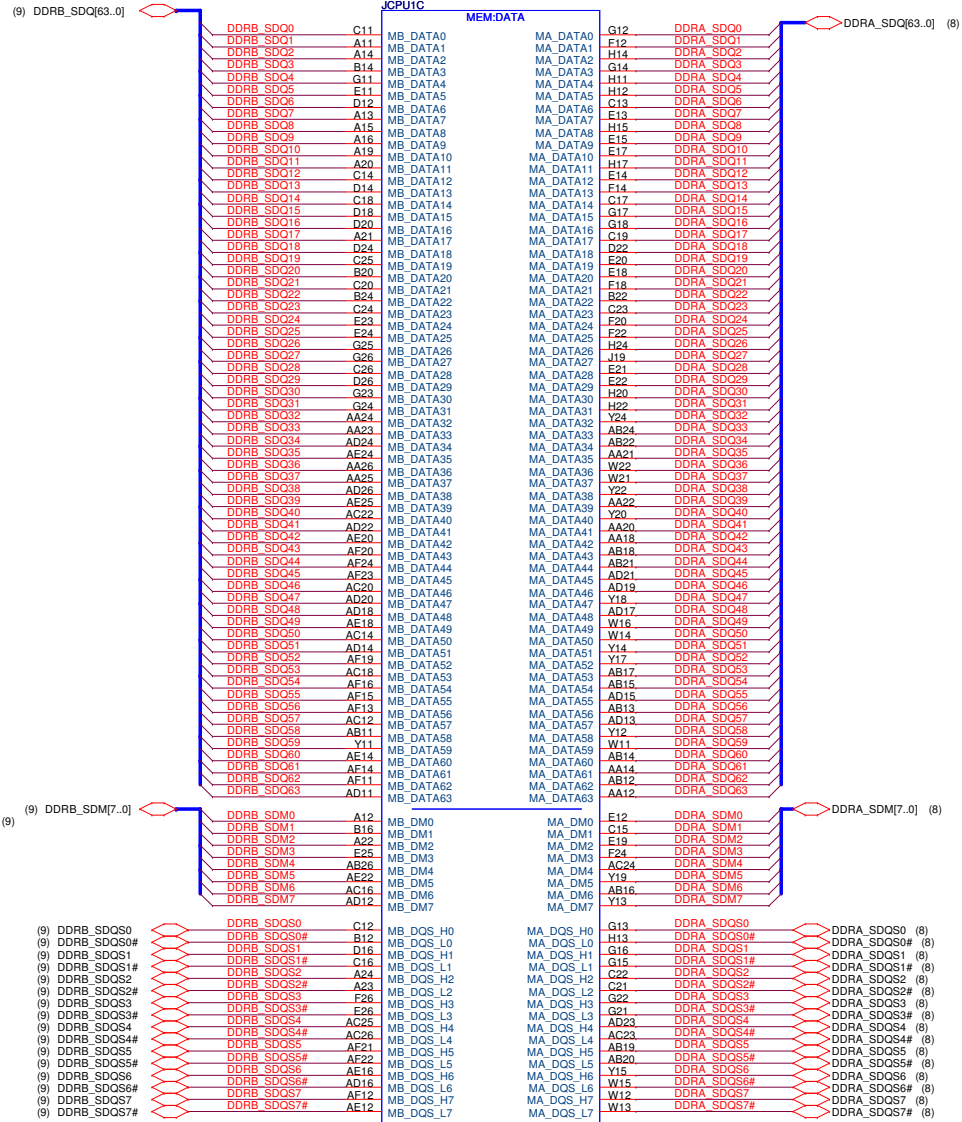
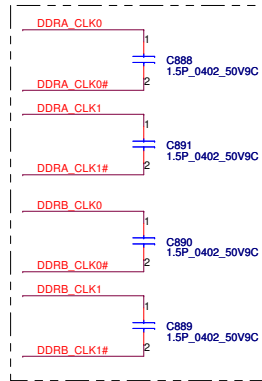
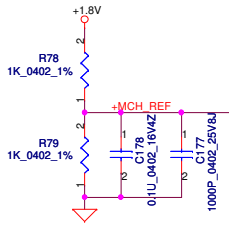
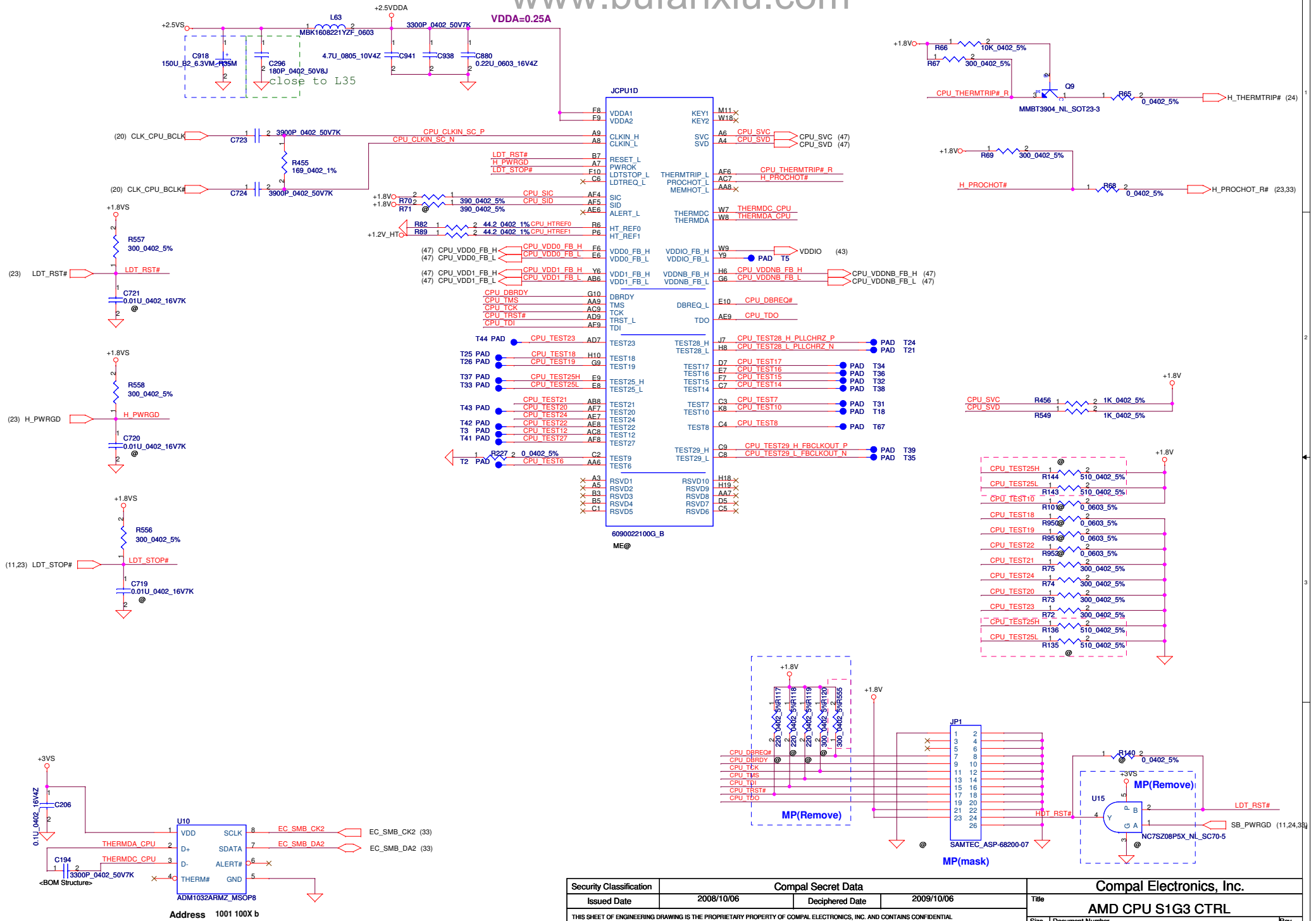


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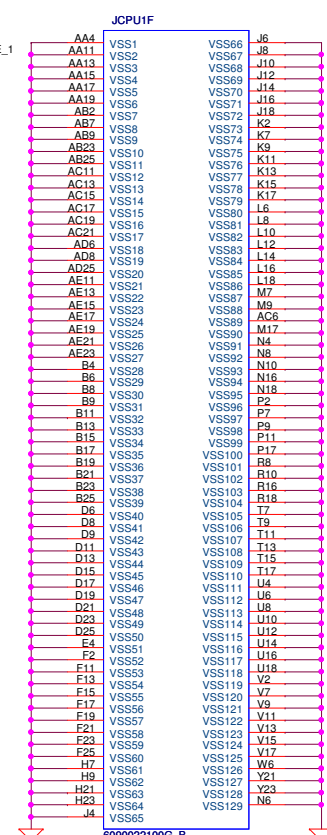
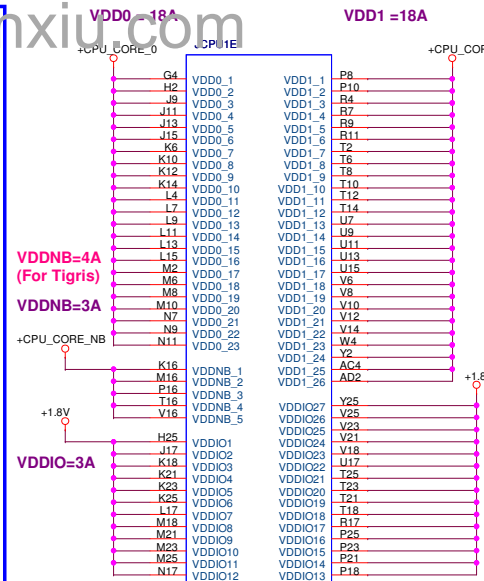
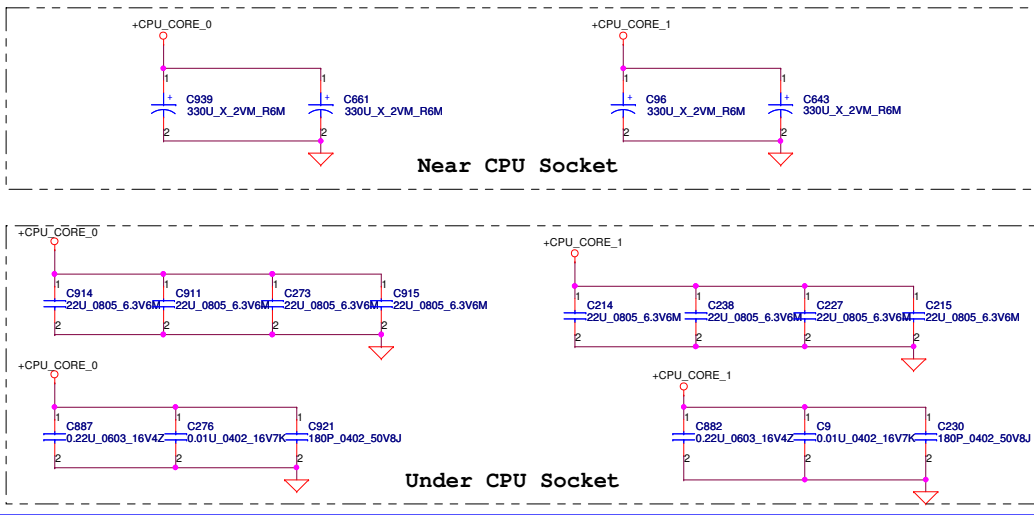


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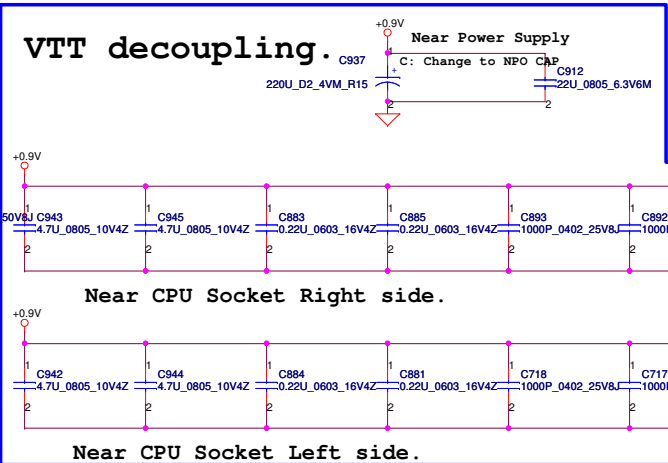
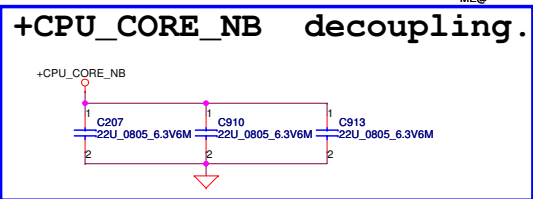
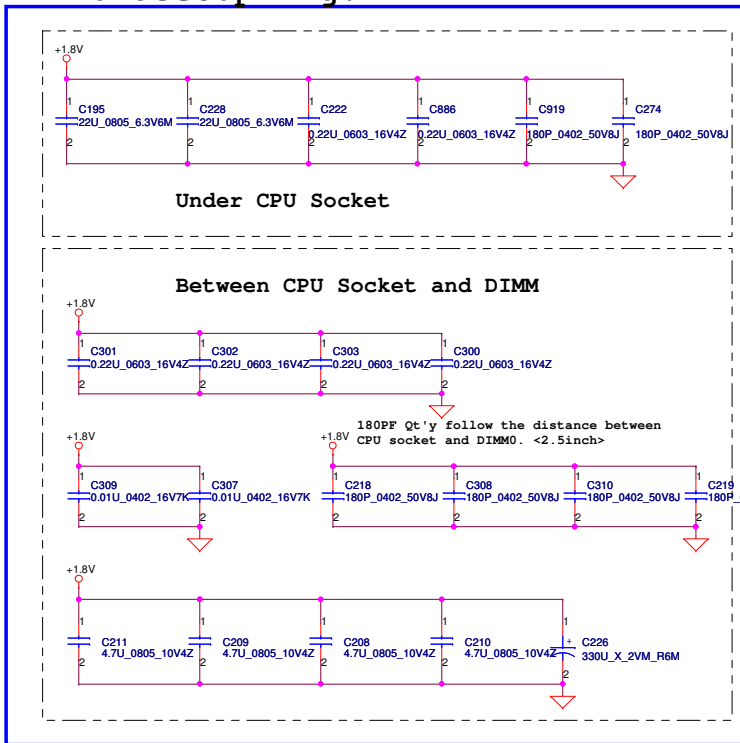
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AMD CPU S1G3 CTRL		
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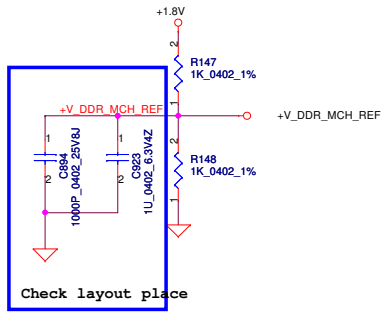
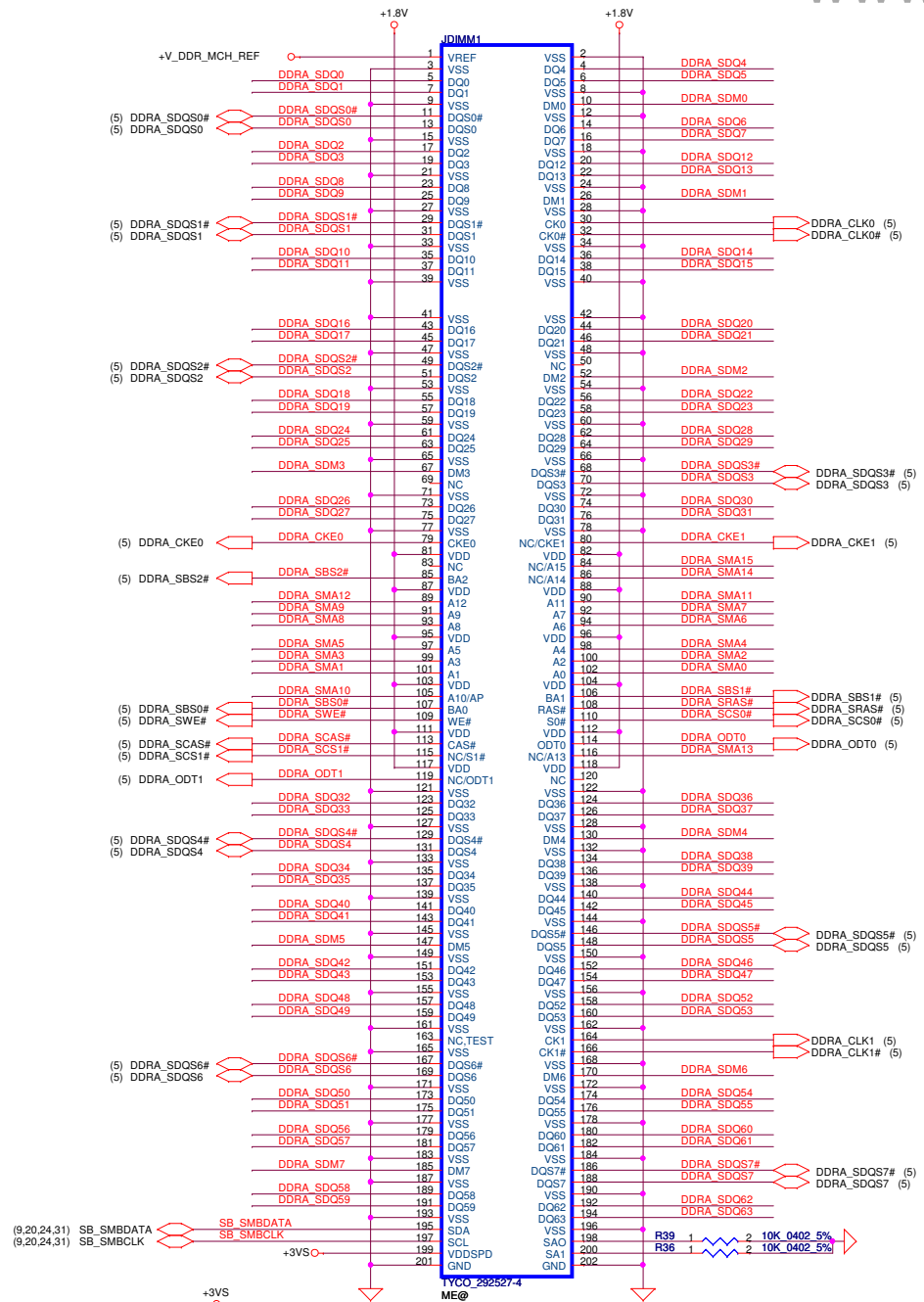
VDD (+CPU_CORE) decoupling.



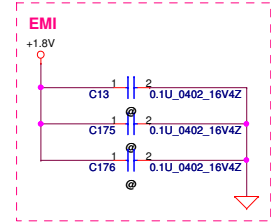
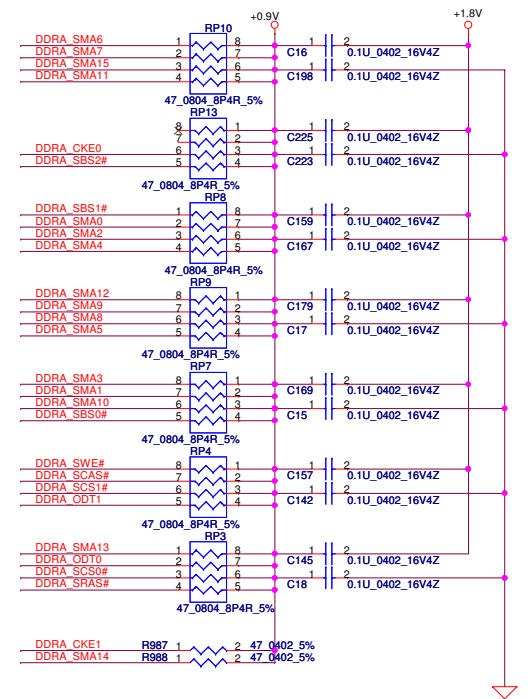
VDDIO decoupling.



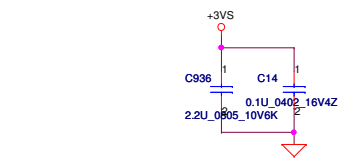
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Check layout place



DIMM1 REV H:5.2mm (BOT)



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(14) PCIE GTX_C_MRX_P[0..15]
(14) PCIE GTX_C_MRX_N[0..15]

PCIE_MTX_C_GRX_P[0..15]
PCIE_MTX_C_GRX_N[0..15]
(14)

Table listing PCIE GTX_C_MRX connections (D4-D15) to various GFX components (GFX_RX0P to GFX_RX15N).

PART 2 OF 6
PCIE I/F GFX

Main table listing PCIE_MTX_C_GRX connections (A5-A15) to various VGA components (VGA@0.1U_0402_10V7K).

Table listing PCIE GTX_C_IRX connections (P1-P4, N1-N4) to various GPP components (GPP_RX0P to GPP_RX5N).

PCIE I/F GPP

Table listing PCIE ITX connections (PRX P1-P4, N1-N4) to various WLAN and LAN components.

Table listing SB connections (RX0P to RX3N) to various SB components (SB_TX0P to SB_TX3N).

PCIE I/F SB

Table listing SB connections (TX0P to TX3N) to various SB components (SB_TX0P to SB_TX3N).

RS880M_FCBGA528
PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

Table for RS780M Display Port Support (muxed on GFX) showing DP0 and DP1 connections to AUX1 and HPD1.

New Card (4) H_CADOP[0..15]
(4) H_CADON[0..15]

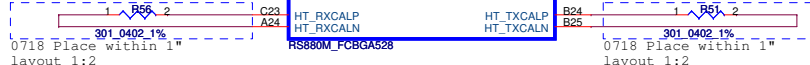
Table listing H_CADOP and H_CADON connections (Y25-Y28, AC24-AC25) to various HT_RXCAD components.

PART 1 OF 6
HYPER TRANSPORT CPU I/F

Table listing H_CADIP connections (D24-D27, K21-K22, G21-G22, H21-H22, J21-J22, L21-L22, M21-M22, N21-N22, P21-P22, Q21-Q22, R21-R22, S21-S22, T21-T22, U21-U22, V21-V22, W21-W22, X21-X22, Y21-Y22, Z21-Z22) to various HT_TXCAD components.

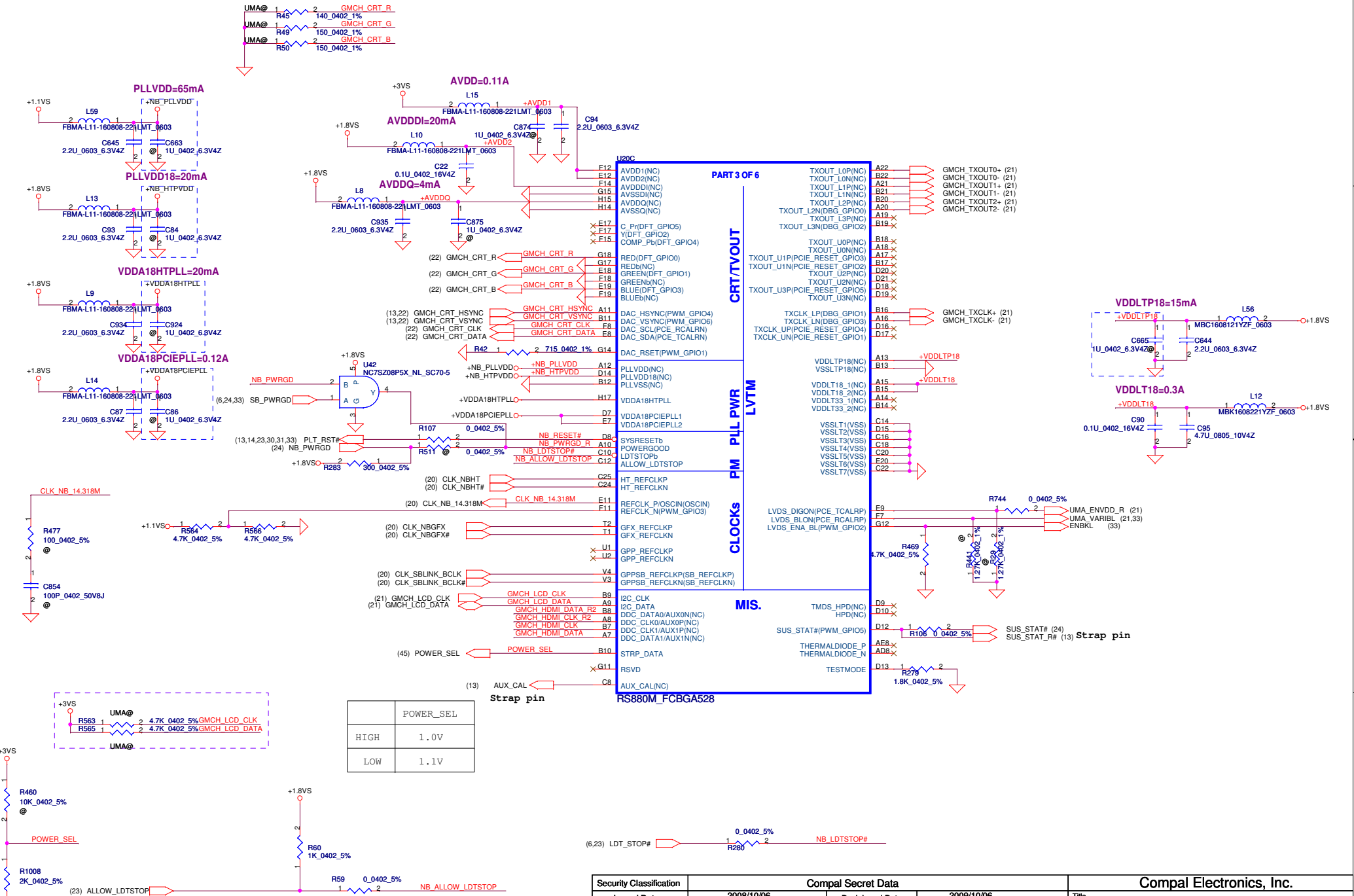
Table listing H_CLKOP and H_CTLOP connections (T22-T23, M22-M23, R21-R20) to various HT_RXCLKOP and HT_RXCTLOP components.

Table listing H_CLKIP and H_CTLIP connections (H24-H25, L21-L20, M24-M25, P19-P18, R18-R17) to various HT_TXCLKIP and HT_TXCTLIP components.



SA00002DR30 S IC 216-0674026 A13 RS780M FCBGA 0FA
SA000032T10 S IC 216-0752001 A11 RS880M FCBGA528 0FA

For RS780M A13
 RED: Connected to GND through two separate 140ohm 1% resistor

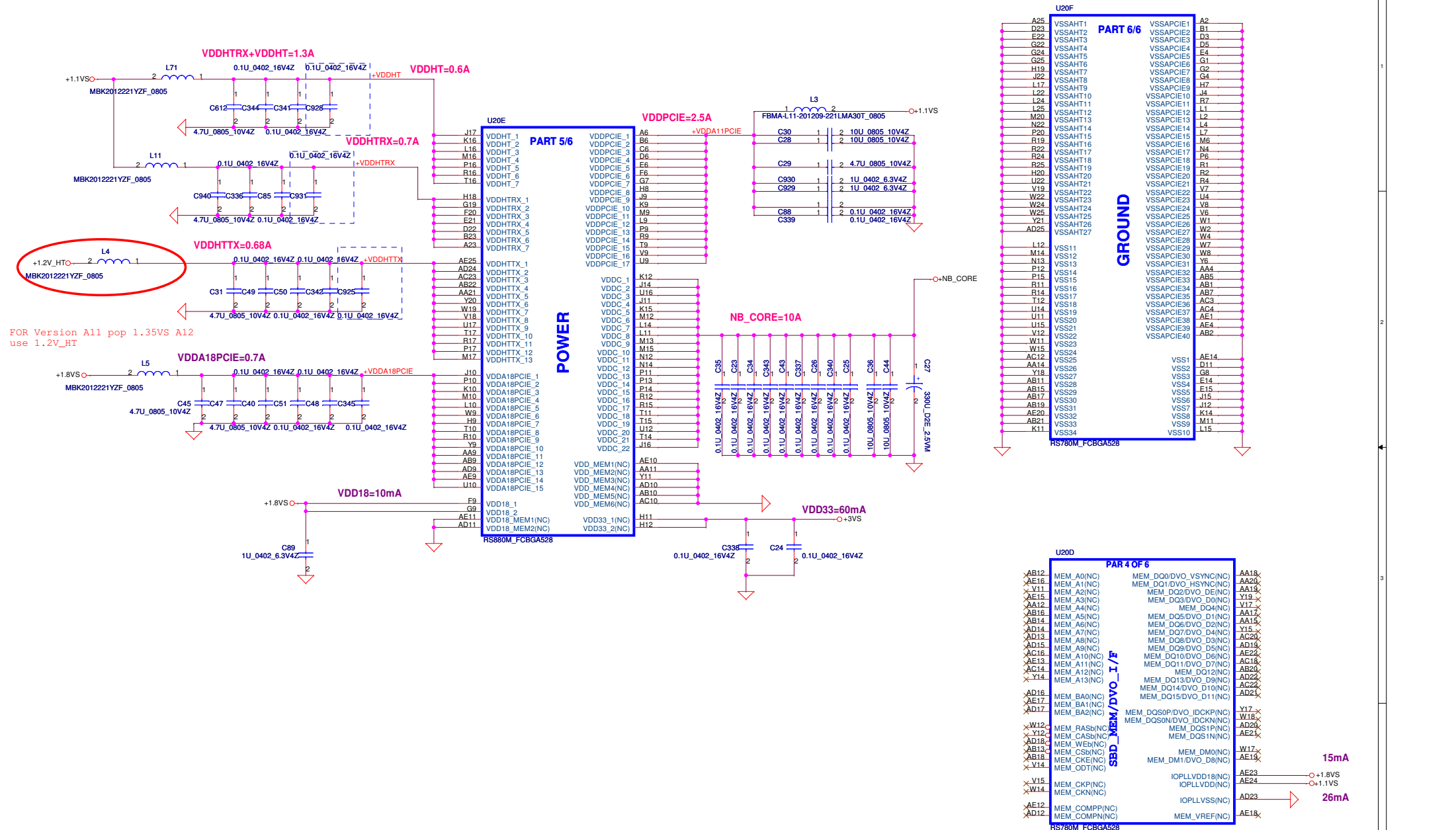


	POWER_SEL
HIGH	1.0V
LOW	1.1V

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RS880 VEDIO/CLK GEN		
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FOR Version A11 pop 1.35VS A12 use 1.2V_HT

15mA
26mA

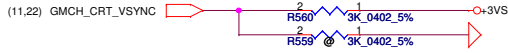
+1.8VS=W/S=20/10mil For Memory PLL power
+1.1VS=W/S=20/10mil For Memory PLL power

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RS800 PWR/GND

LA-5972P



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

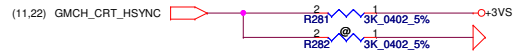
Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS880M)
 0 : Enable (RS880M)



DFT_GPIO1:LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

RS780 use HSYNC to enable SIDE PORT

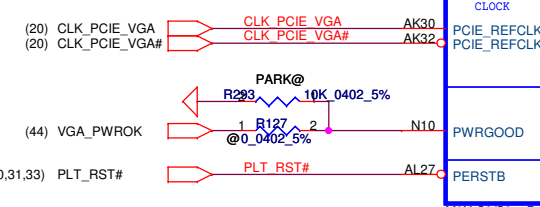
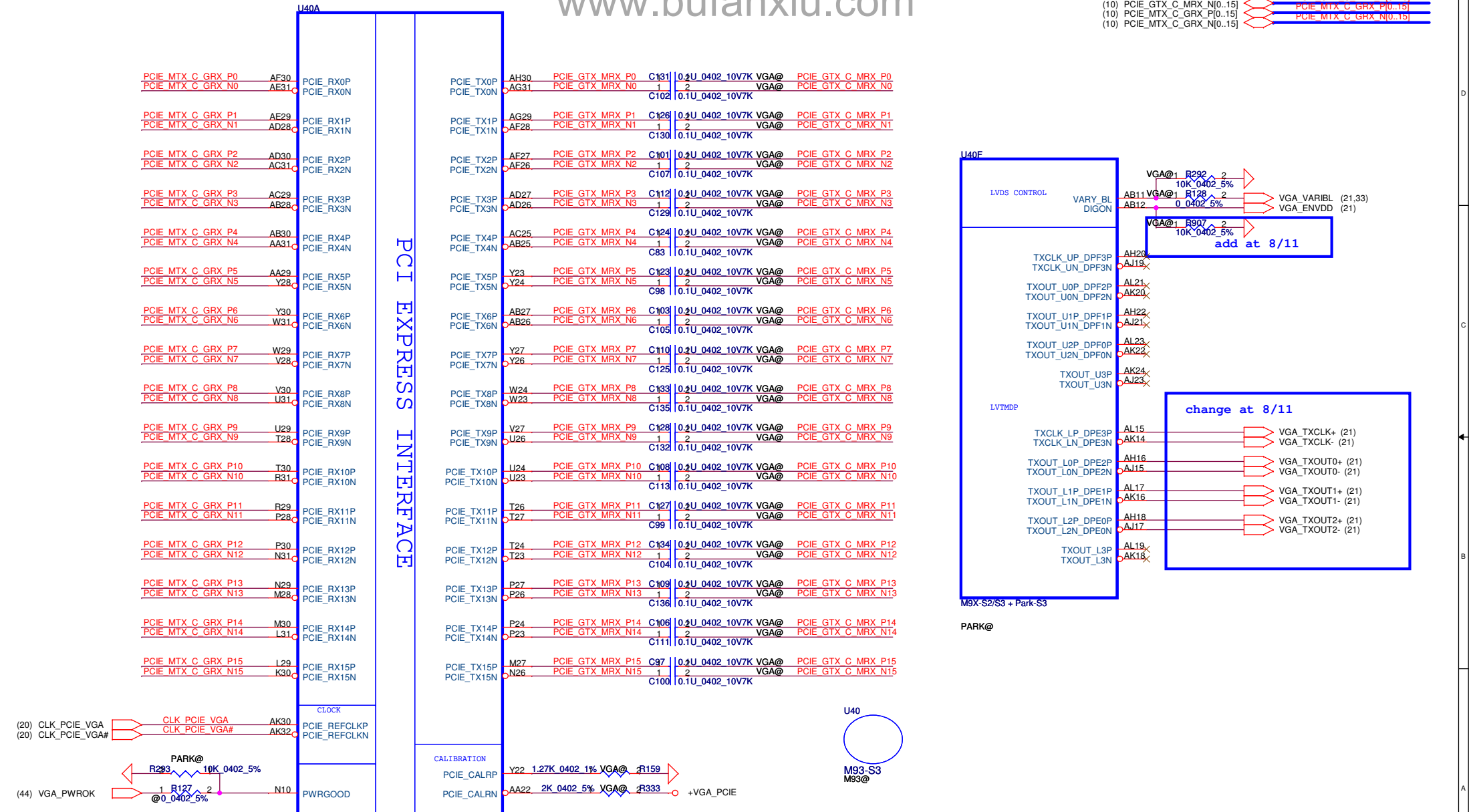


RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0 : Enable (RS880M)
 1 : Disable(RS880M)

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(10) PCIE GTX_C_MRX_P[0..15] → PCIE GTX_C_MRX_P[0..15]
 (10) PCIE GTX_C_MRX_N[0..15] → PCIE GTX_C_MRX_N[0..15]
 (10) PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]
 (10) PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]



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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X= DESIGN DEPENDANT
 NA= NOT APPLICABLE

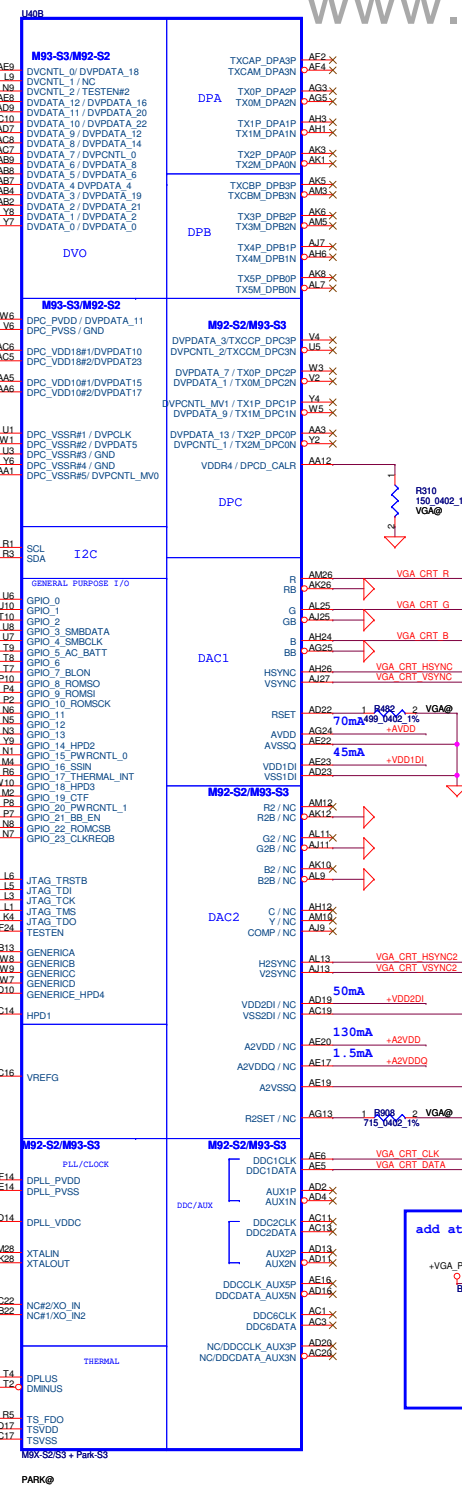
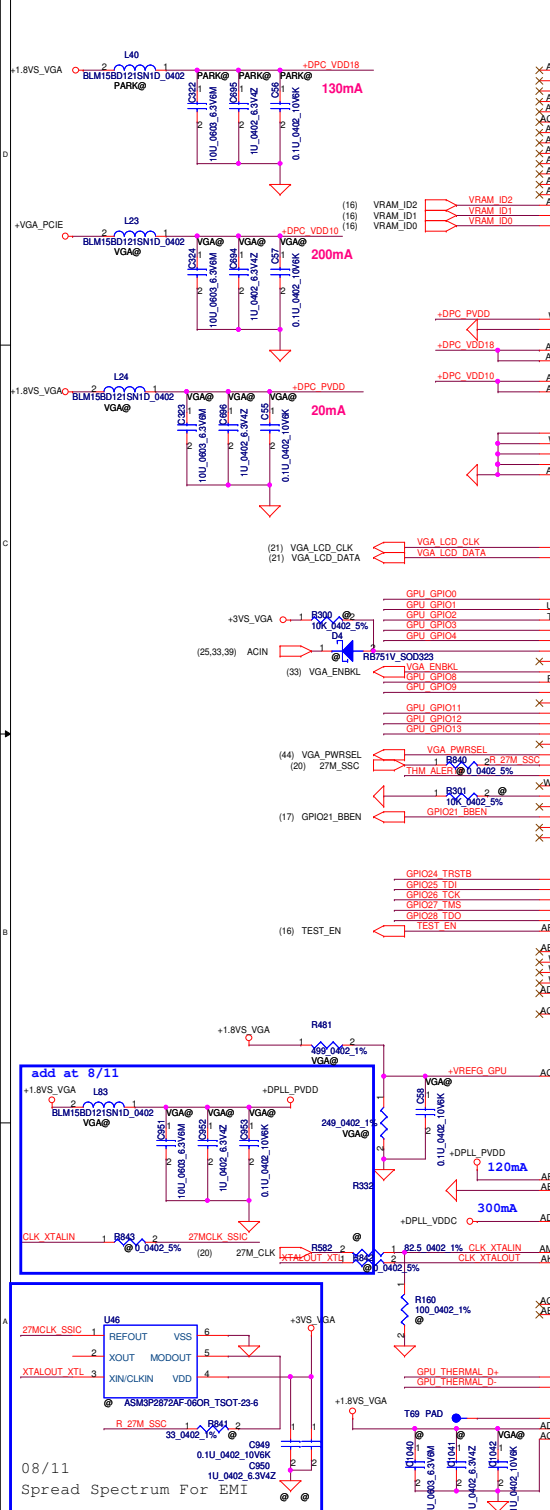
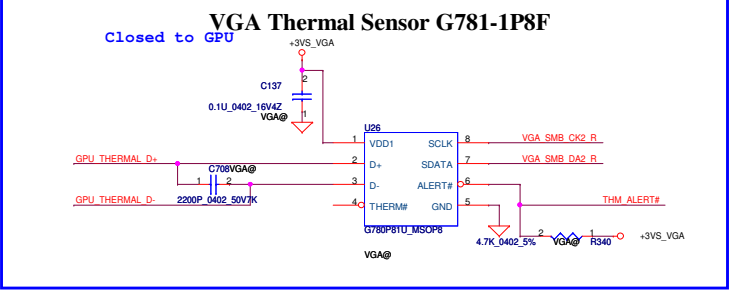
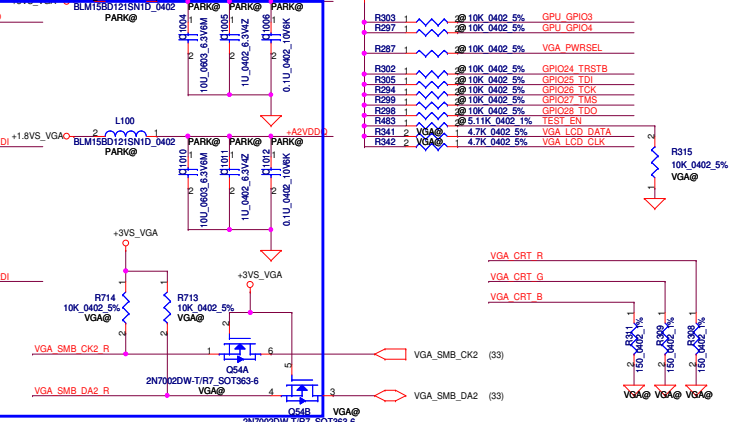
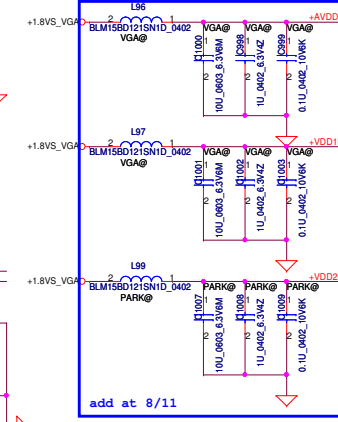
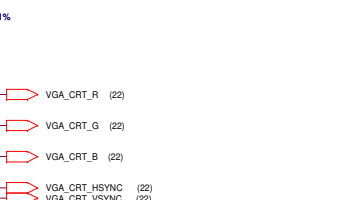
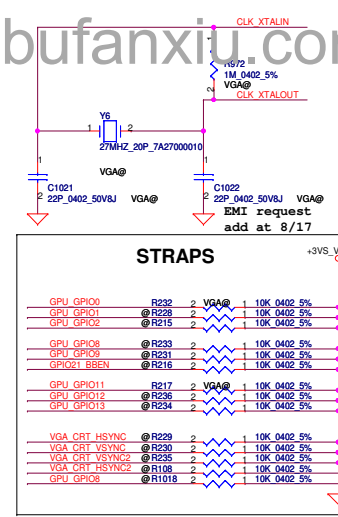
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_VGA_DIS	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_VGA_DIS	GPIO21	VGA ENABLED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VSYNC		

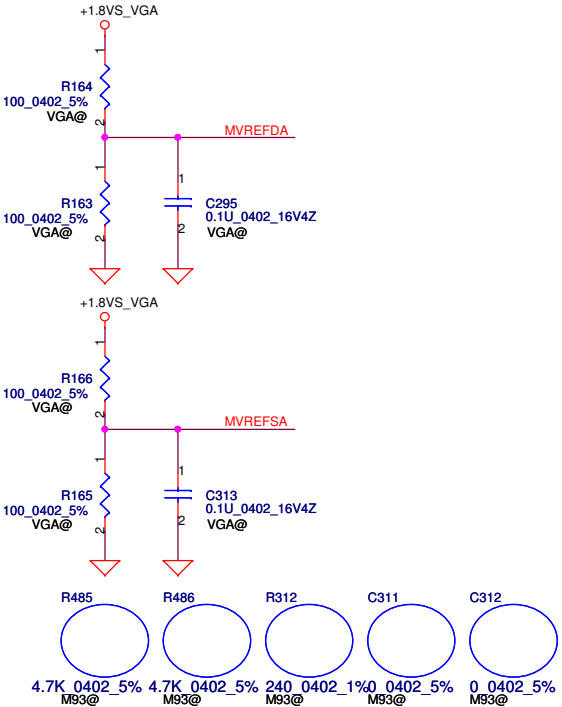
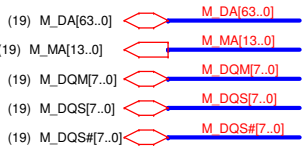
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

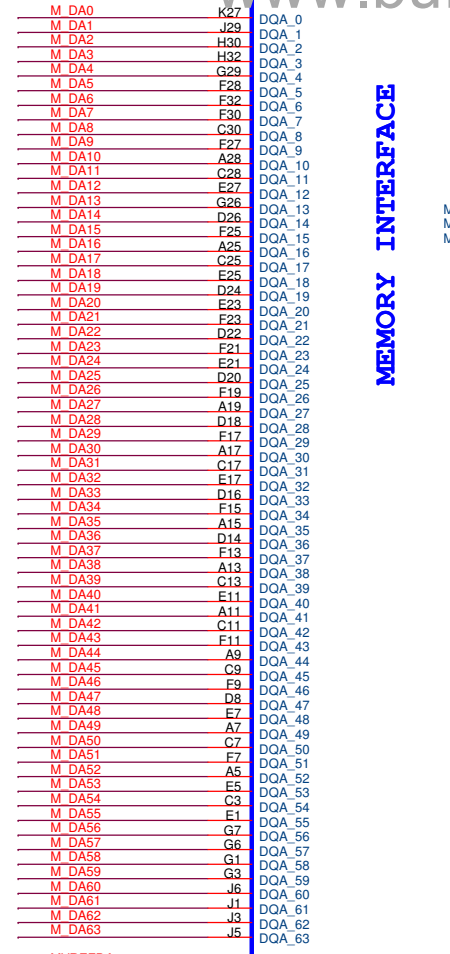
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
H2SYNC	GENERICC		
	GENERICC		
	GPIO21_BB_EN		

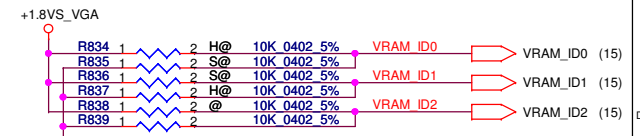
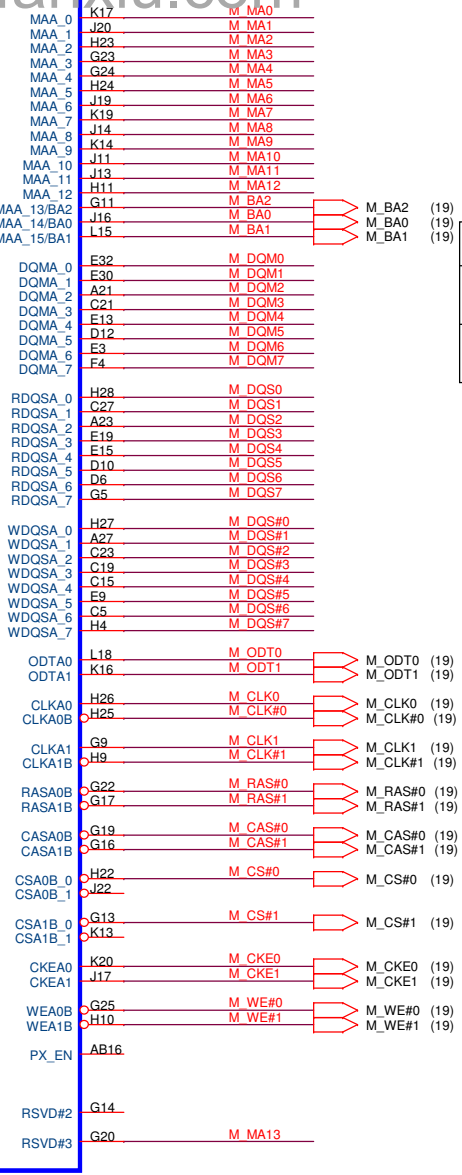




	M93-S3	PARK-S3
R330	NC	240
R130	NC	0/short
R312	240	150
R331	NC	240
	M93-S3	PARK-S3
R485	4.7K	51.1
R486	4.7K	51.1
C311	0/short	0.1uF
C312	0/short	0.1uF

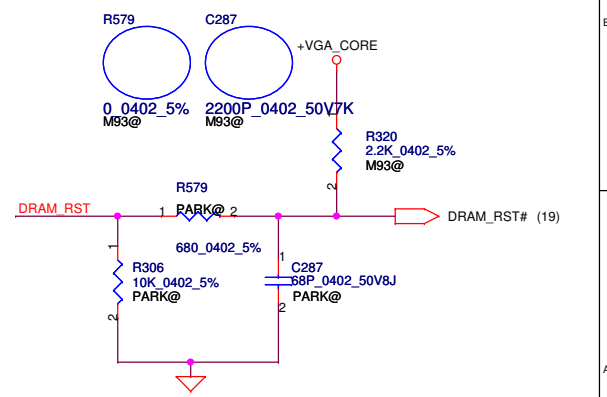


MEMORY INTERFACE



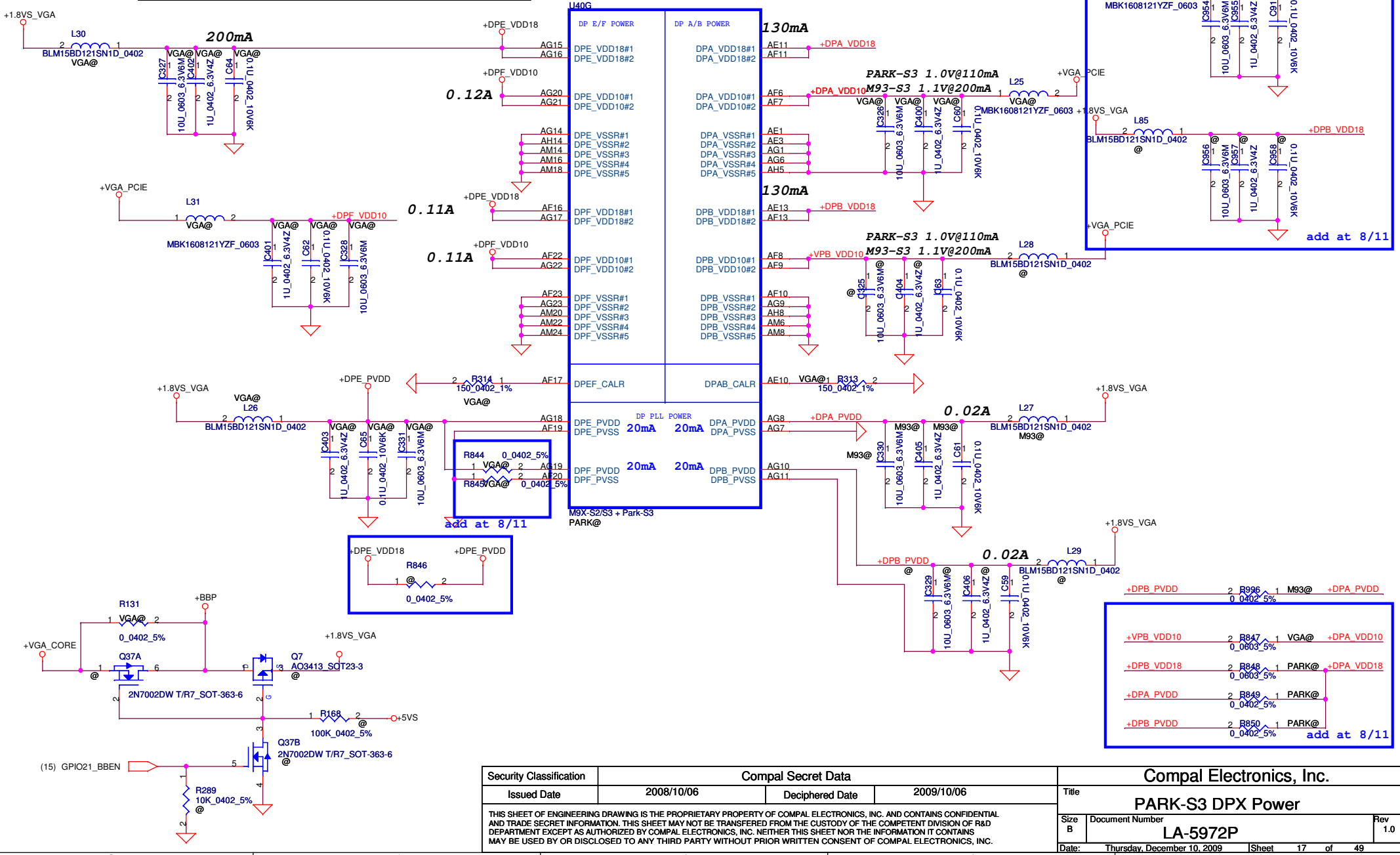
Vendor		VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix	H5TQ1G63BFR-12C	1	0	0
Samsung	K4W1G1646E-HC12	0	1	0

	M93-S3	PARK-S3
R306	NA	10K
R579	0/short	680
R320	2.2K	NA
C287	2.2nF	68pF



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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title PARK-S3 MEM Interface	
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				Date	Thursday, December 10, 2009
				Sheet	16 of 49
				Rev	1.0

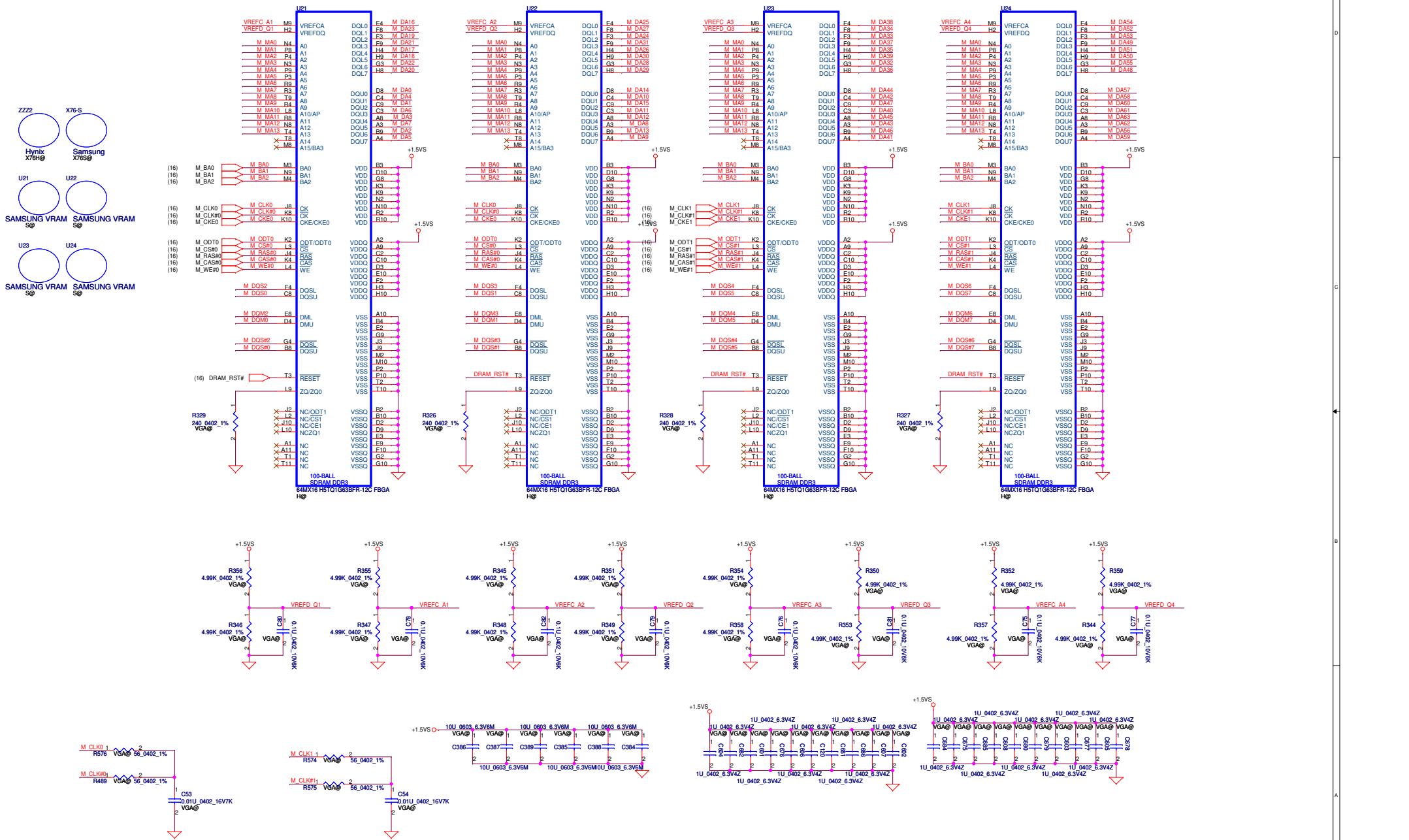
DPE_VDD10	Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V
DPF_VDD10	M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V

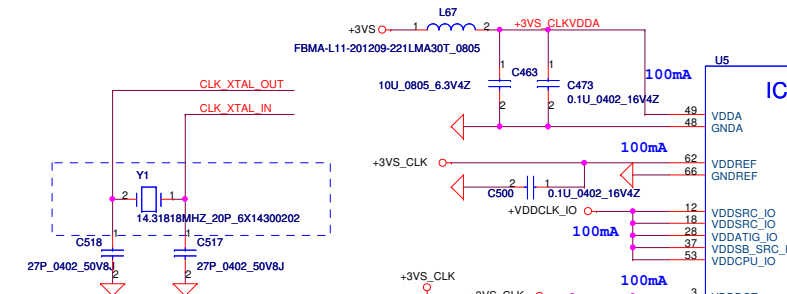
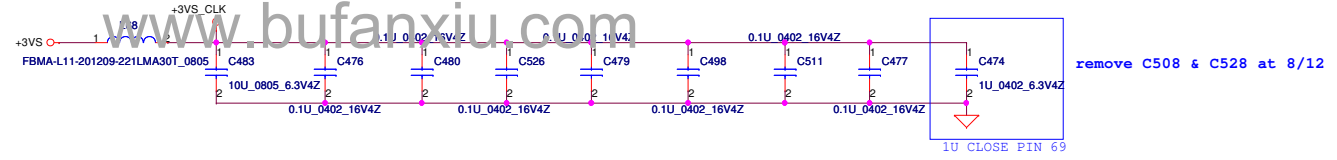
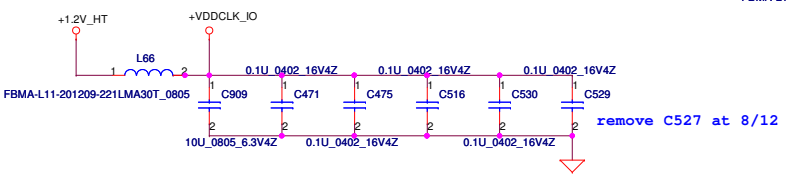


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Compal Electronics, Inc.		
Title		
PARK-S3 DPX Power		
Size	Document Number	Rev
B	LA-5972P	1.0
Date:	Thursday, December 10, 2009	Sheet 17 of 49

- (16) M_DA[63..0] M_DA[0..63]
- (16) M_MA[13..0] M_MA[13..0]
- (16) M_DQM[7..0] M_DQM[7..0]
- (16) M_DQS[7..0] M_DQS[7..0]
- (16) M_DQS# [7..0] M_DQS# [7..0]

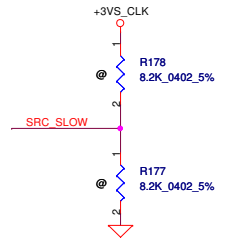
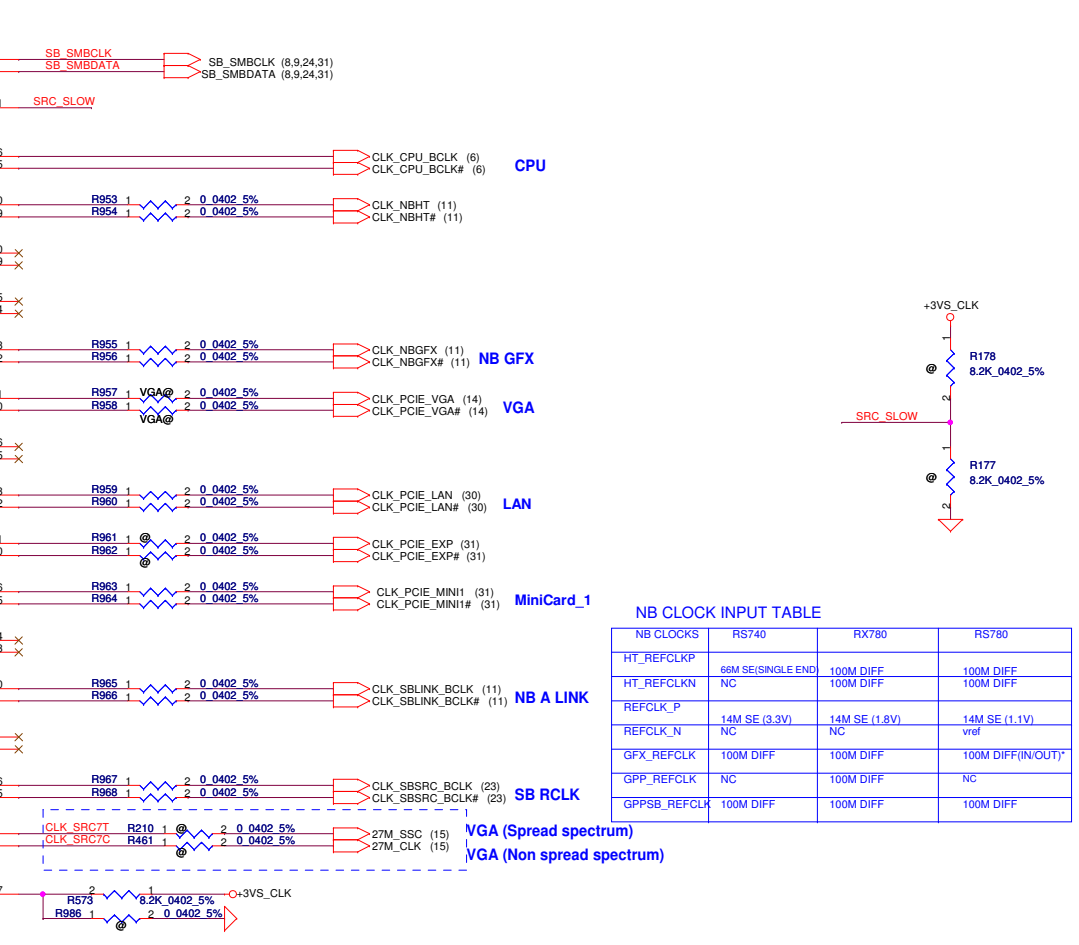
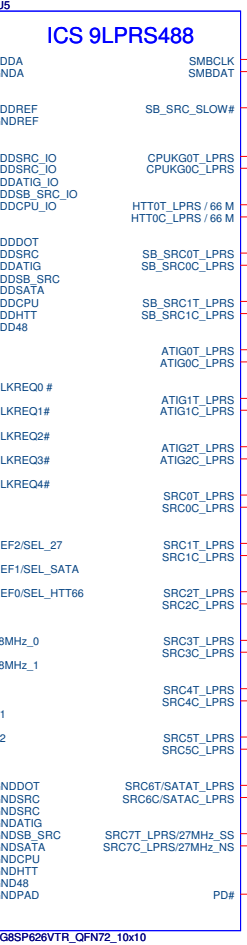
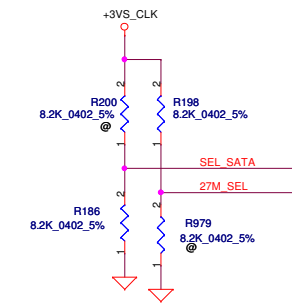
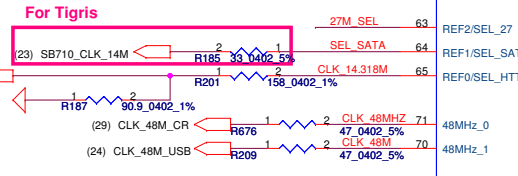




Routing the trace at least 10mil

NEW CARD
Mini Card1

CLK_NB_14.318M	RS780
1.1V 158R/90.0R	



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF('N/OUT')
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CLKLT MLF 72P CLK GEN

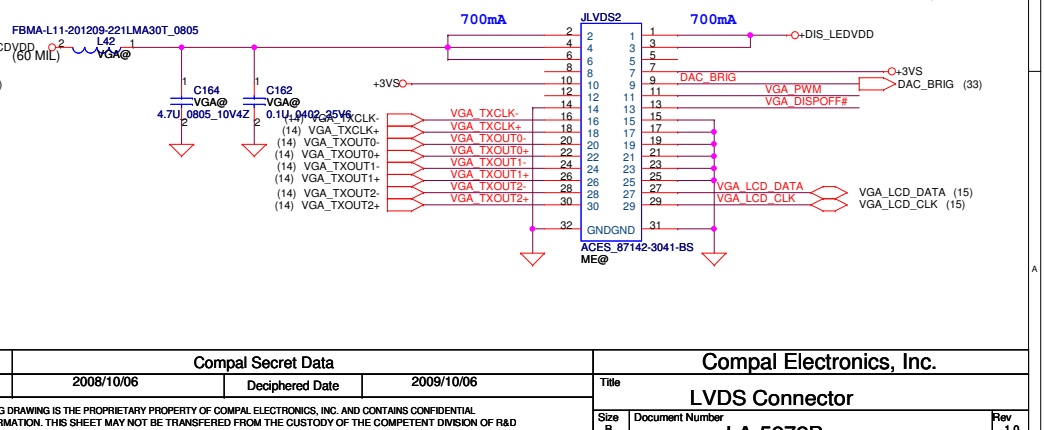
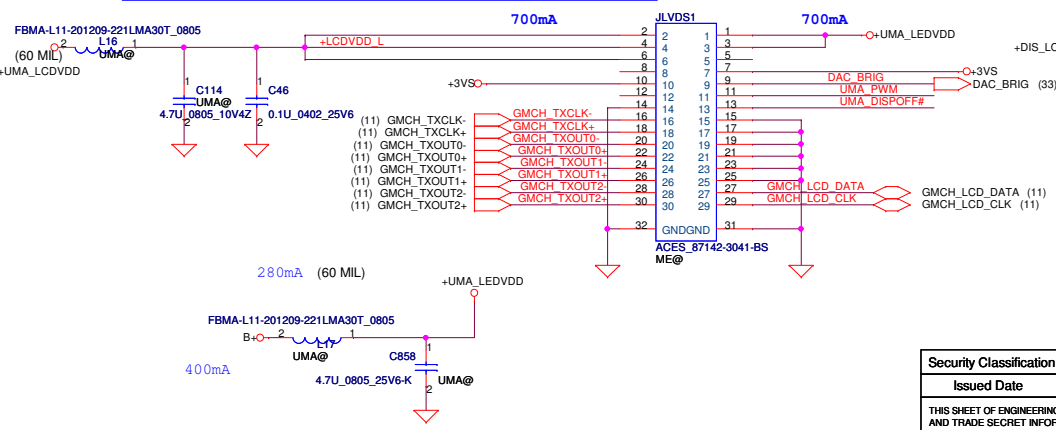
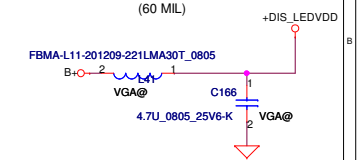
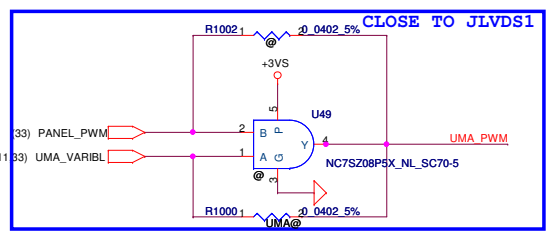
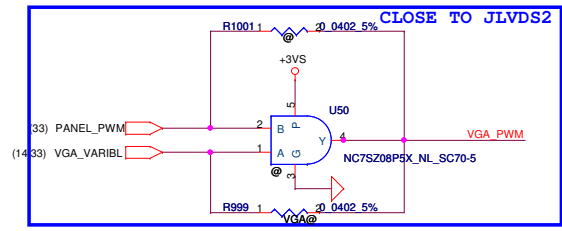
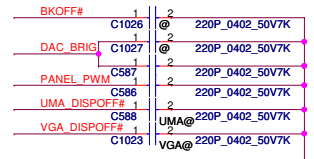
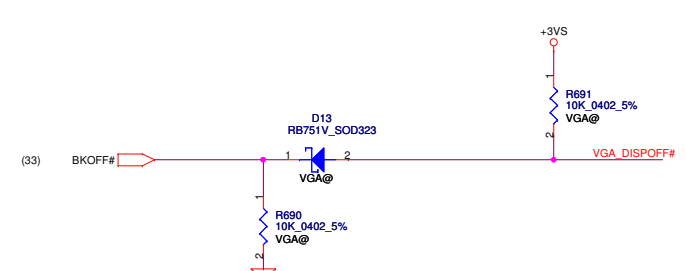
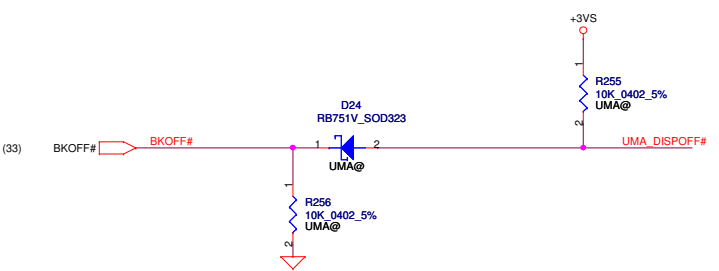
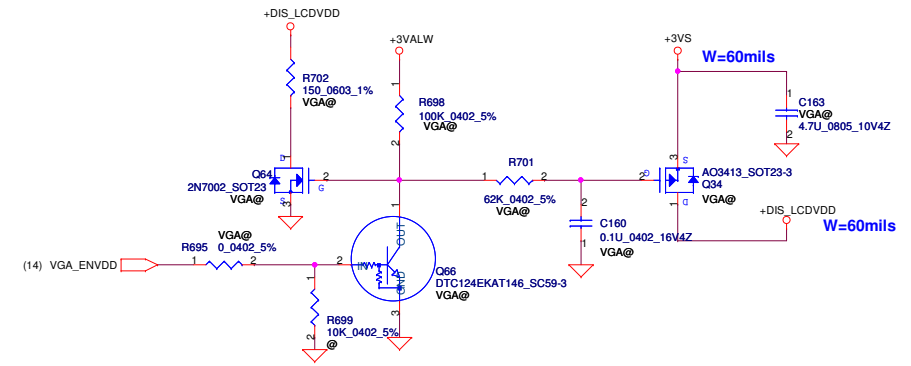
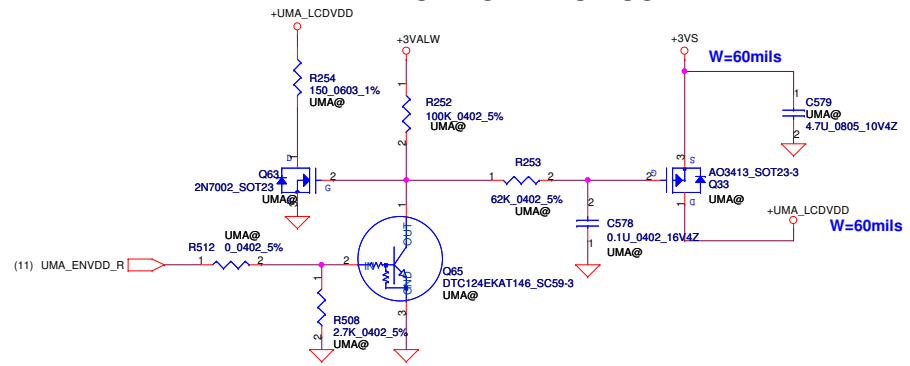
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1	NON SPREAD 100M SATA SRC6 output
	0*	SPREAD 100M SATA SRC6 output

27M_SEL	1*	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

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Compal Electronics, Inc.			
Clock generator			
Title	Size	Document Number	Rev
	Custom	LA-5972P	1.0
Date:	Thursday, December 10, 2009	Sheet	20 of 49

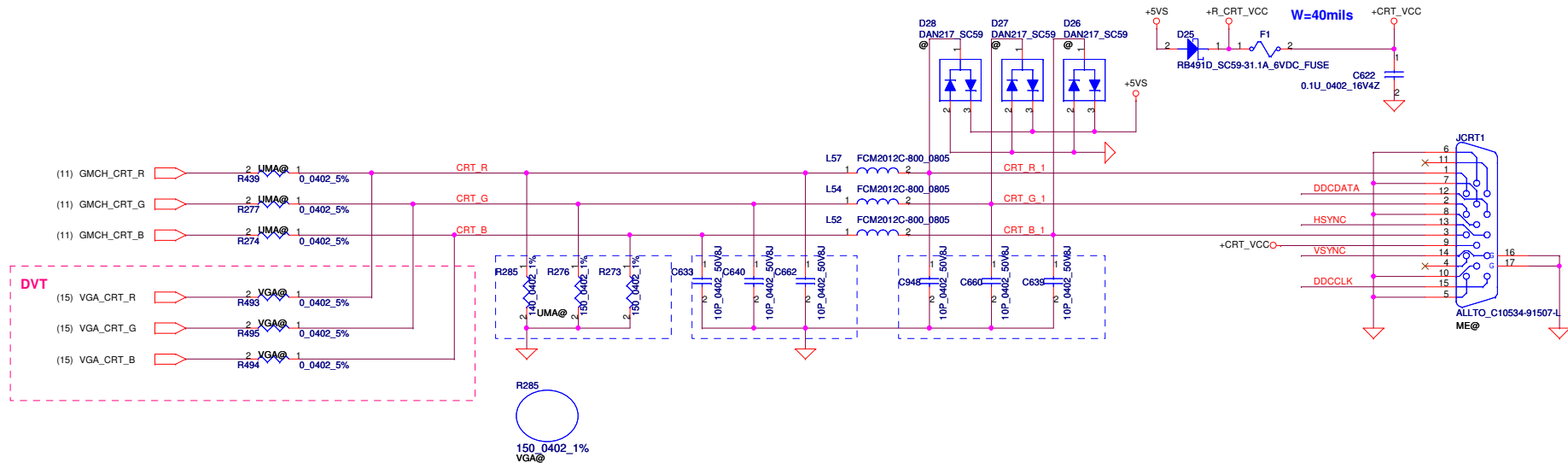
LCD POWER CIRCUIT



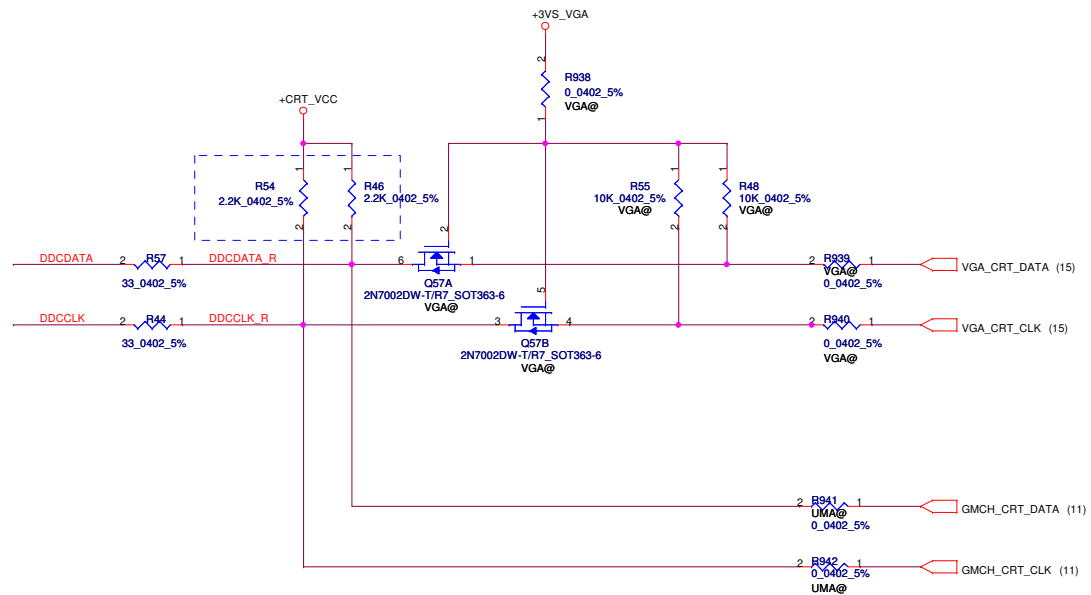
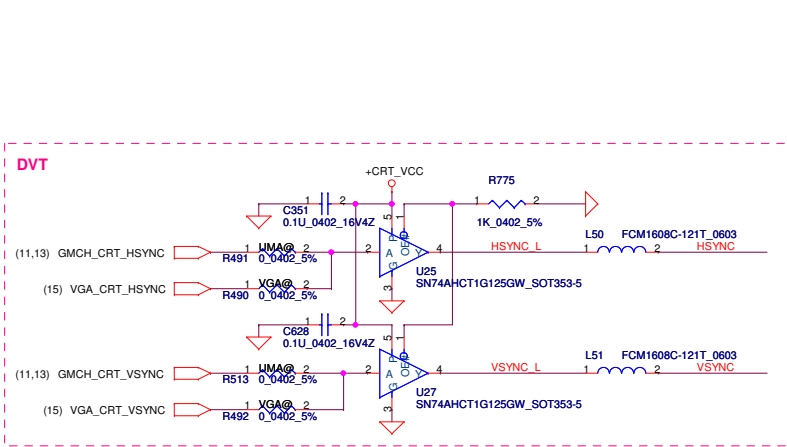
Security Classification	Compal Secret Data	
Issued Date	2008/10/06	Deciphered Date
		2009/10/06

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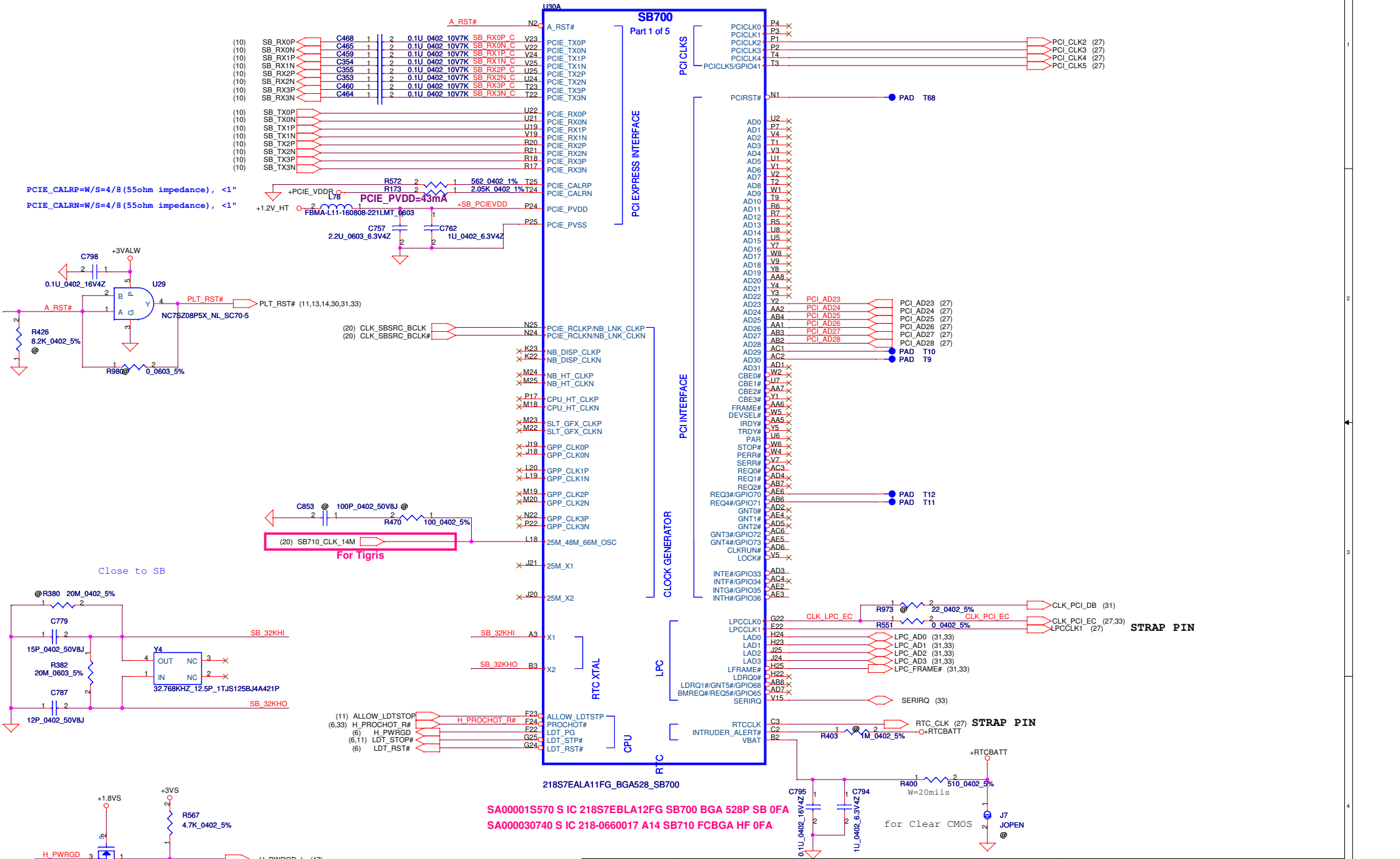
Compal Electronics, Inc.		
Title		
LVDS Connector		
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Place closed to chipset



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Size B	Document Number	LA-5972P		Rev	1.0
Date:	Thursday, December 10, 2009	Sheet	22	of	49

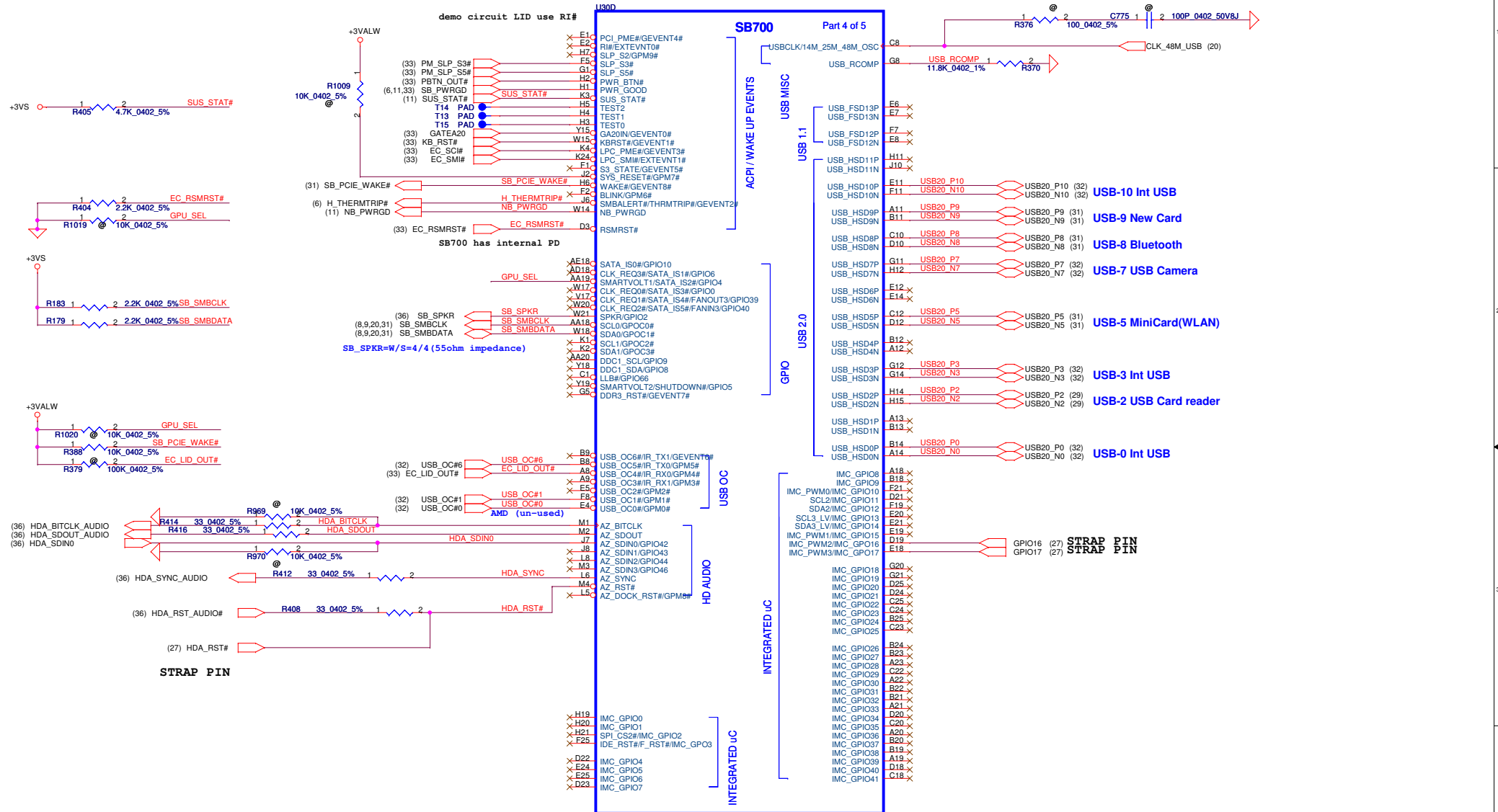


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Compal Electronics, Inc.		
Title		
SB710-PCIE/PCI/ACPI/LPC/RTC		
Size	Document Number	Rev
Custom	LA-5972P	1.0
Date:	Thursday, December 10, 2009	Sheet 23 of 49

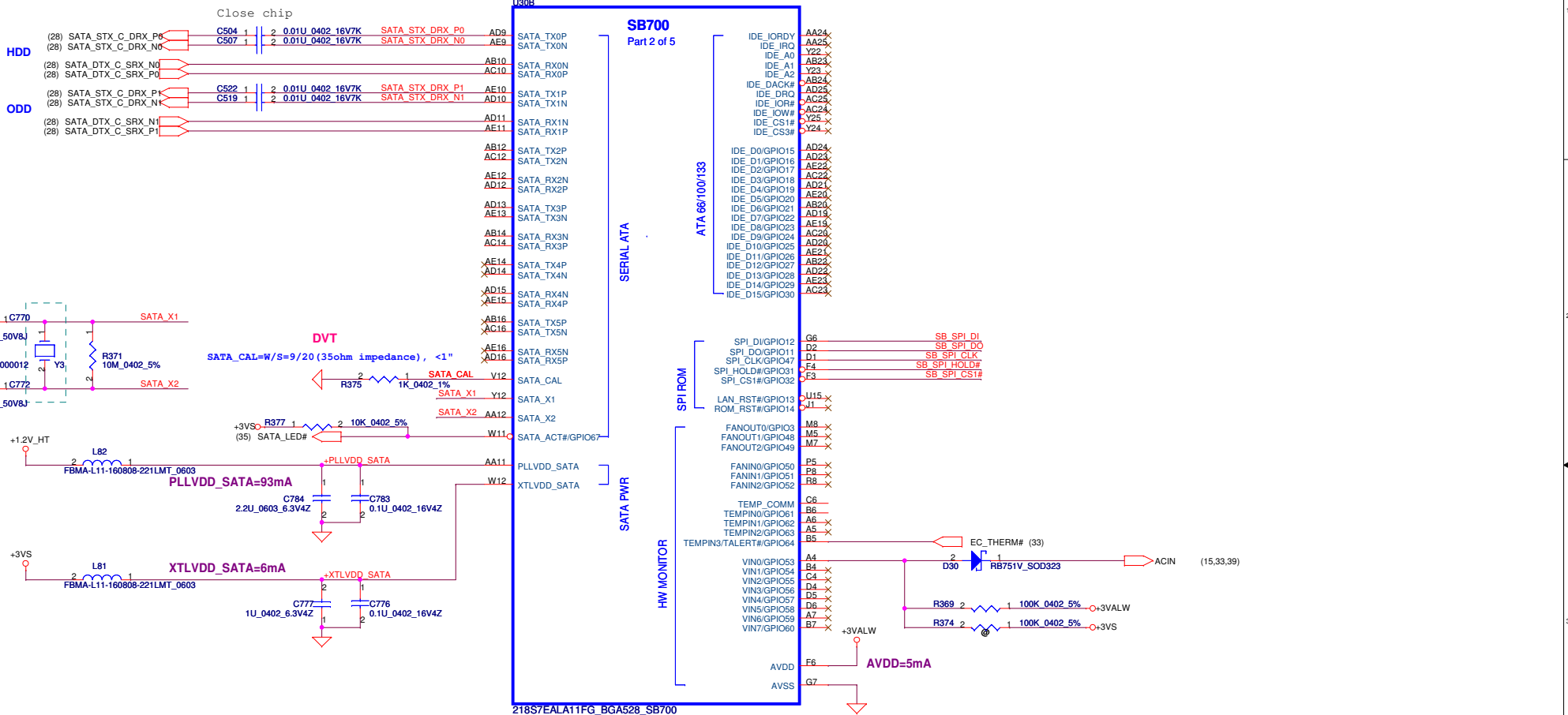
level shift to ISL6265



21857/EAL11FG_BGA528_SB700

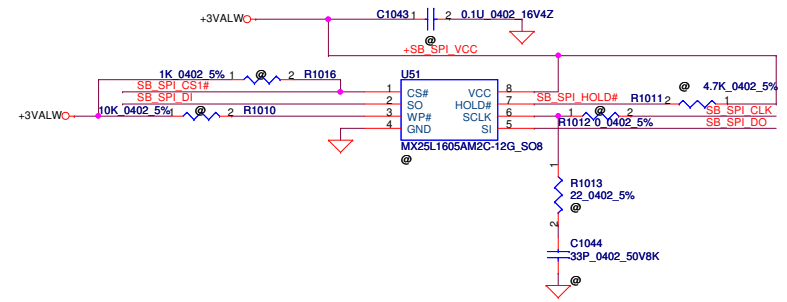
Security Classification	Compal Secret Data		Title	
	Issued Date	Deciphered Date	SB710 USB/HD audio	
	2008/10/06	2009/10/06	Size	Rev
			Custom	1.0
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>			Date: Thursday, December 10, 2009 Sheet 24 of 49	

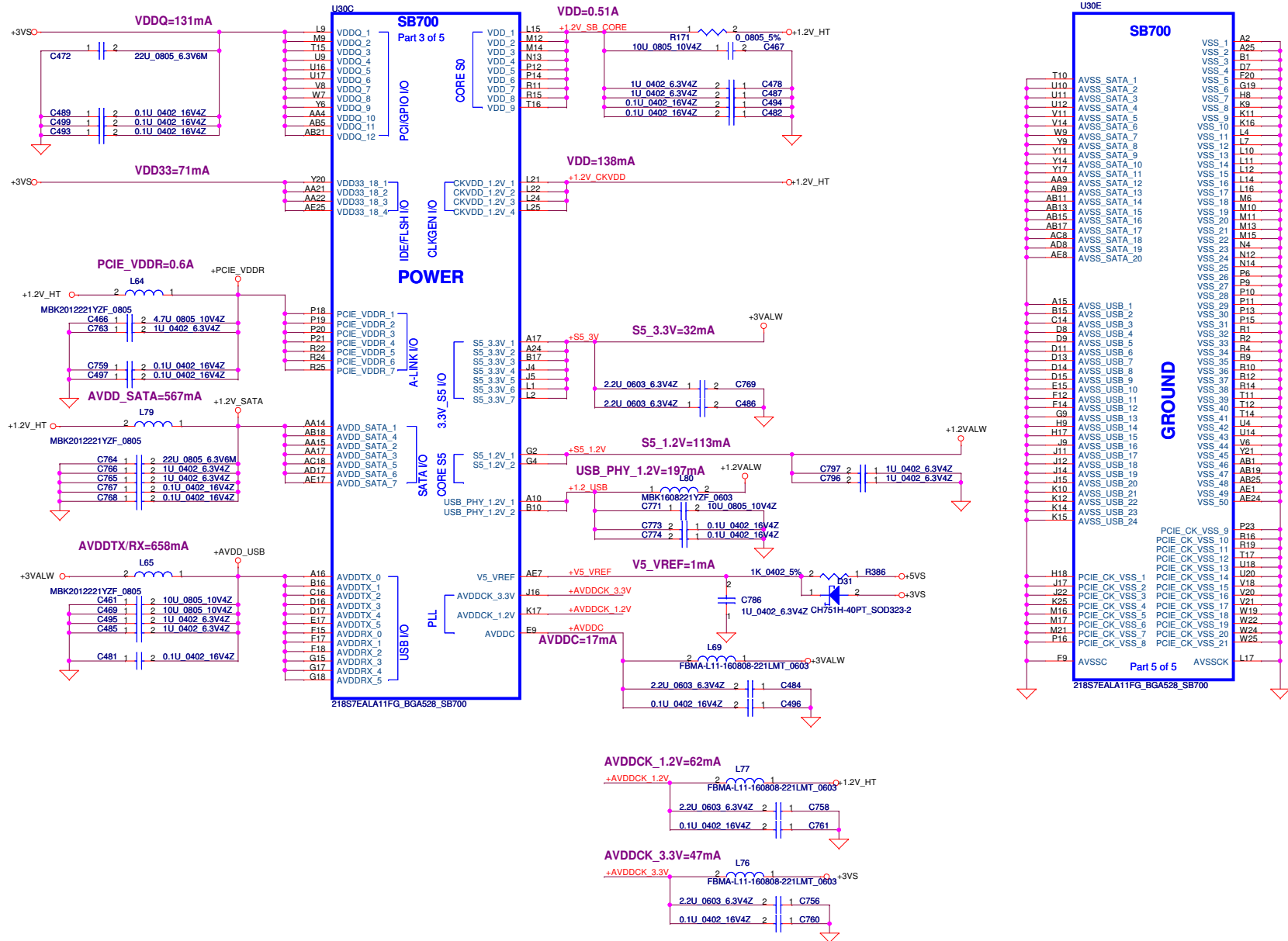
Compal Electronics, Inc.
 SB710 USB/HD audio
 LA-5972P
 Thursday, December 10, 2009 | Sheet 24 of 49



21857/EAL111FG_BGA528_SB700

Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller





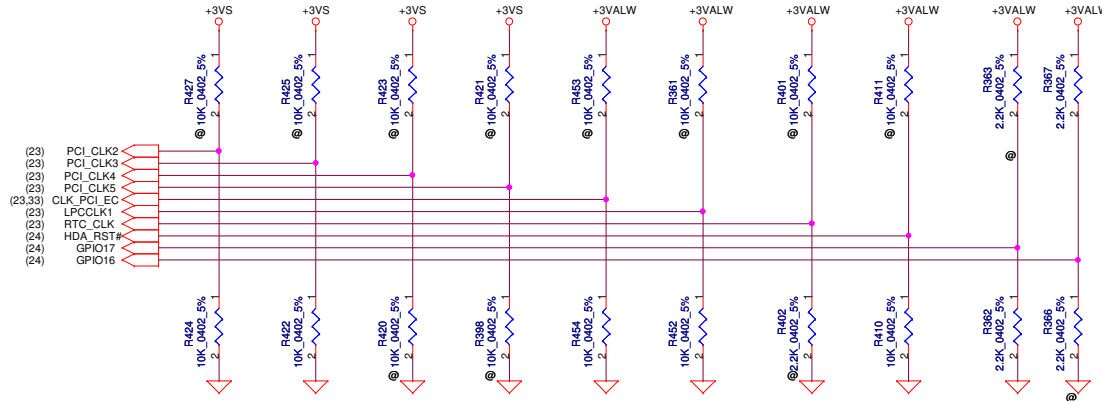
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Compal Electronics, Inc.		
Title SB710 power/GND		
Size Custom	Document Number LA-5972P	Rev 1.0
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

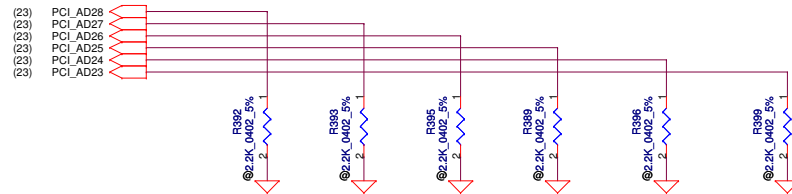
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	



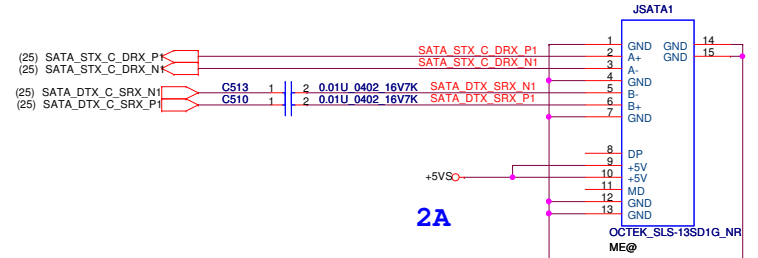
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

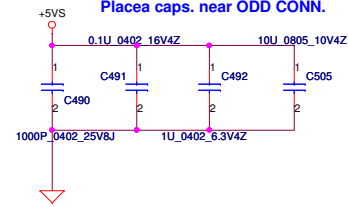


SATA ODD Conn.

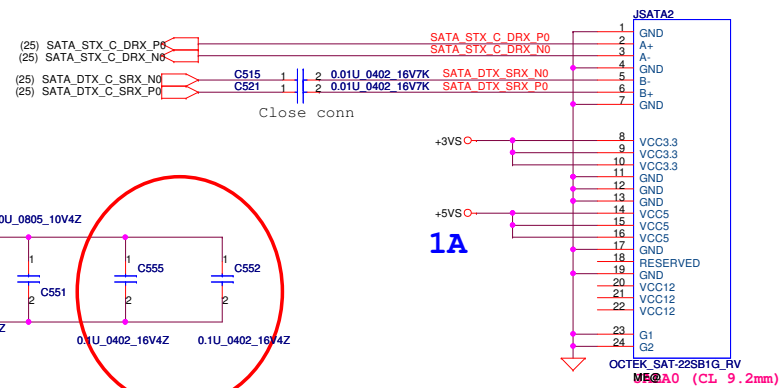


2A

Place caps. near ODD CONN.

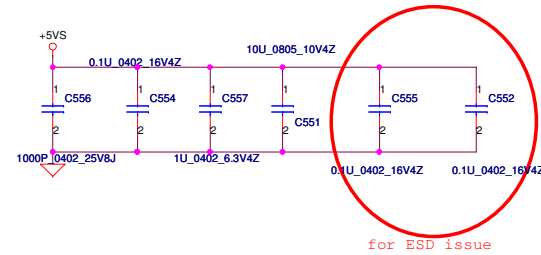
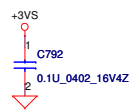


SATA HDD Conn.



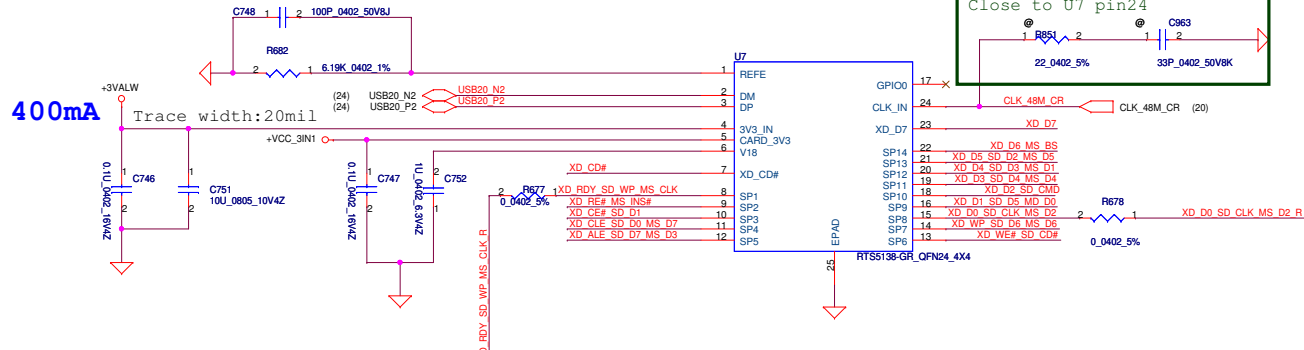
1A

Close conn

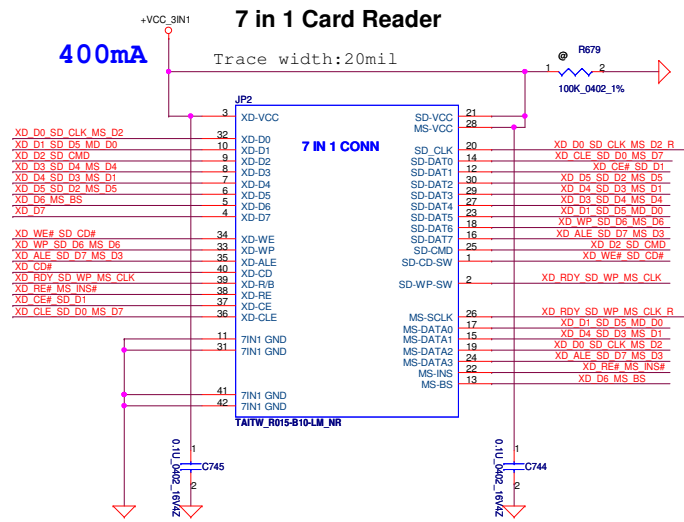
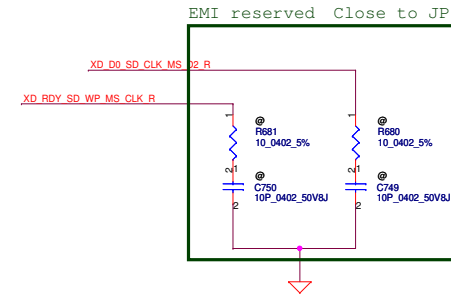


for ESD issue

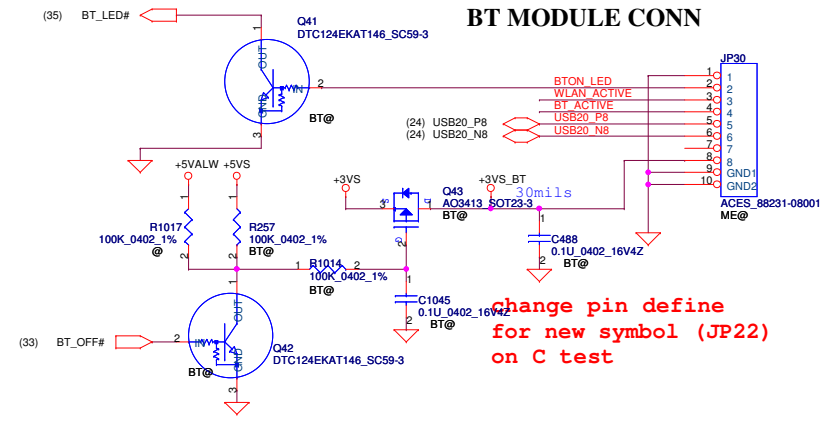
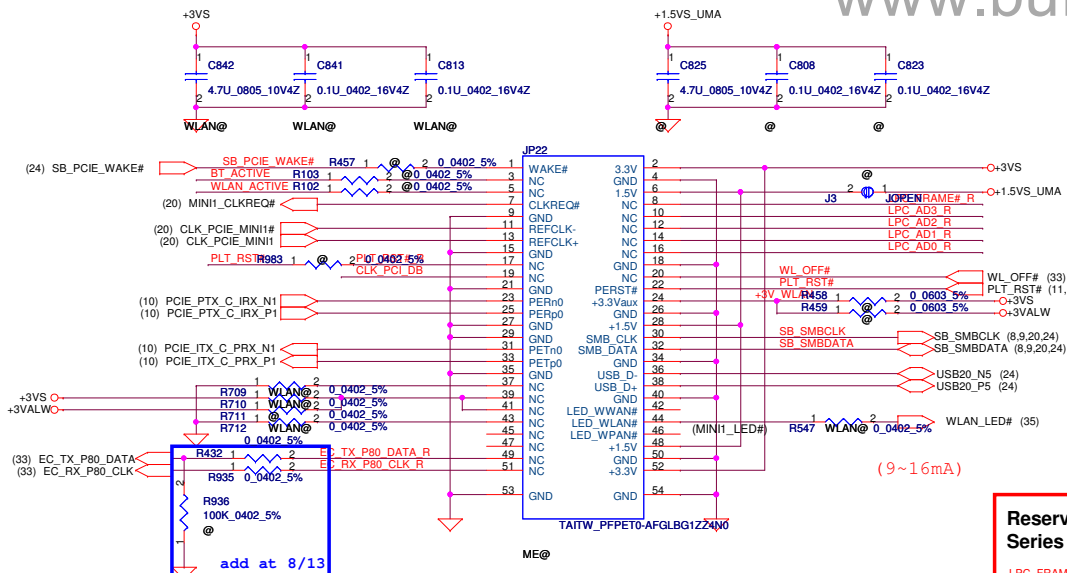
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title		
				HDD & ODD Connector		
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Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



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Size	Document Number	Rev		
Custom	LA-5972P	1.0		
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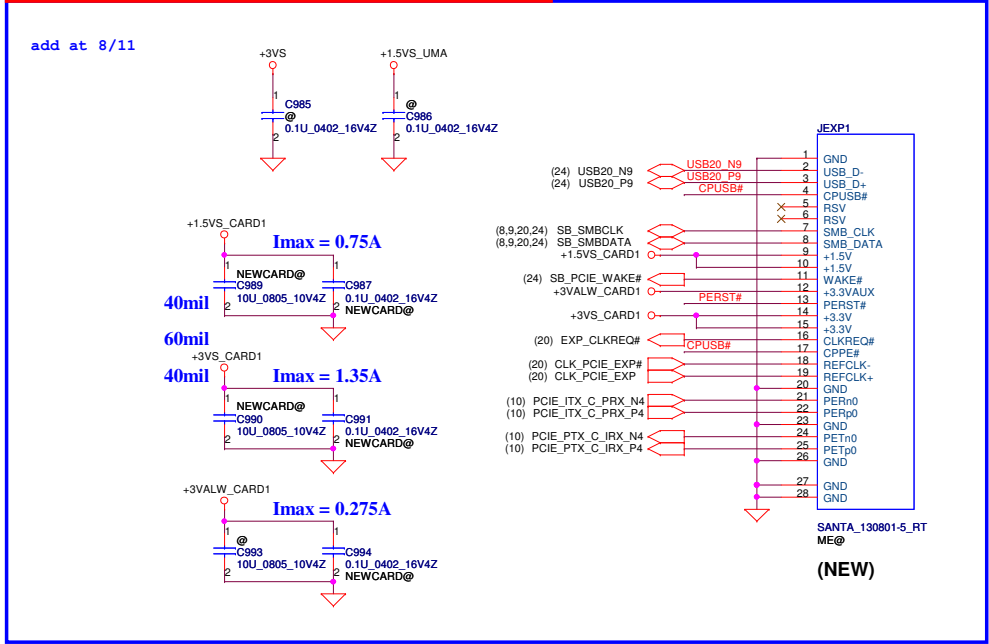
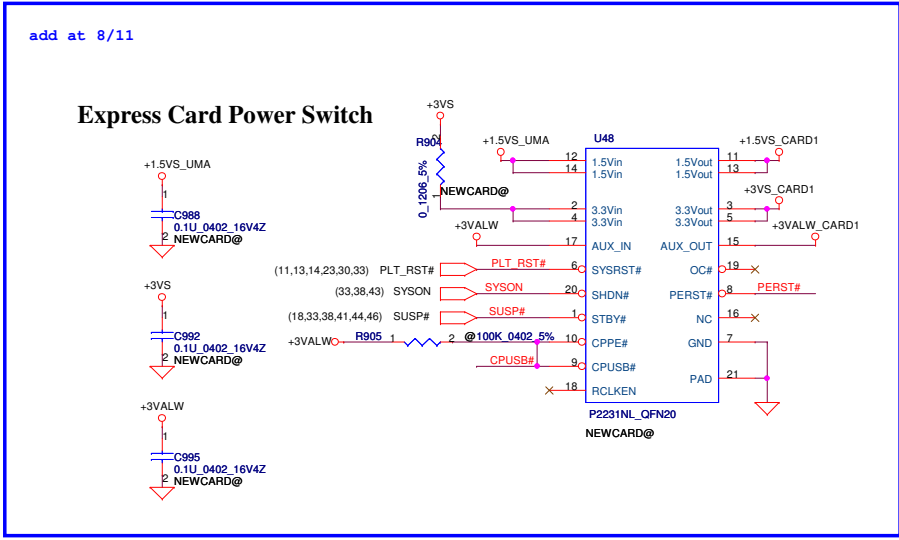


change pin define for new symbol (JP22) on C test

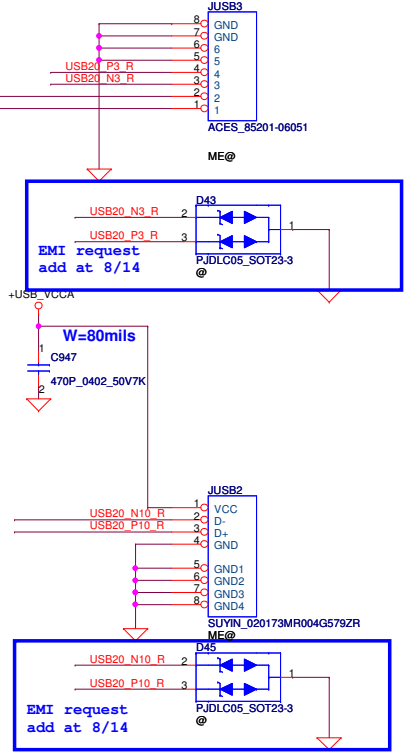
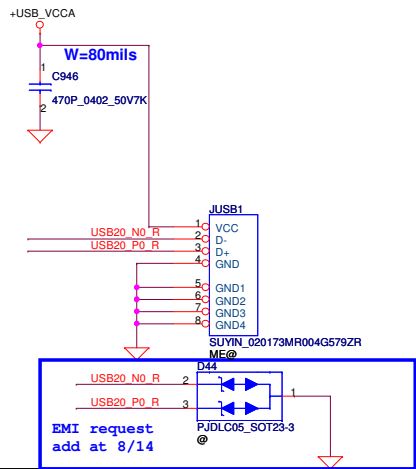
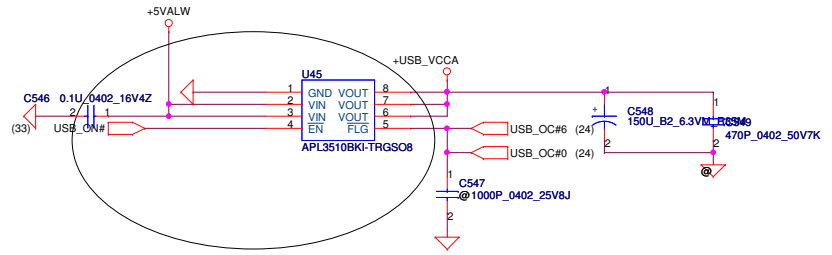
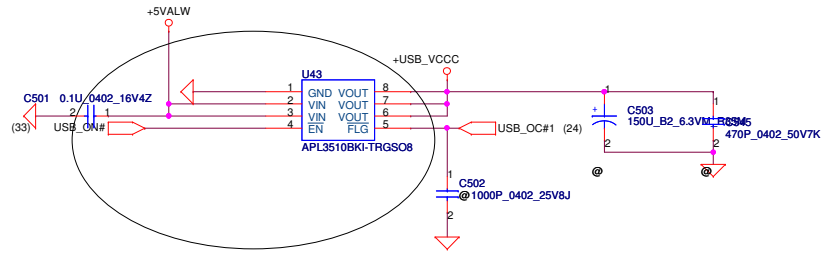
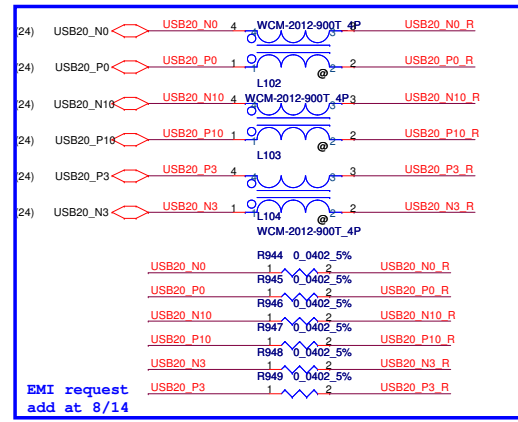
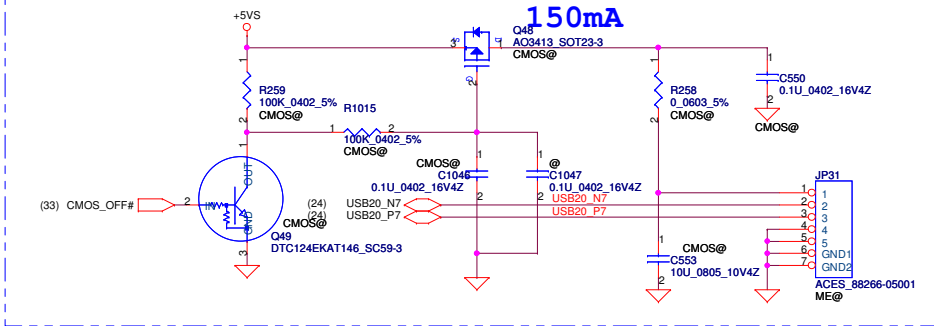
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Reserve for SW mini-pcie debug card. Series resistors closed to KBC side.

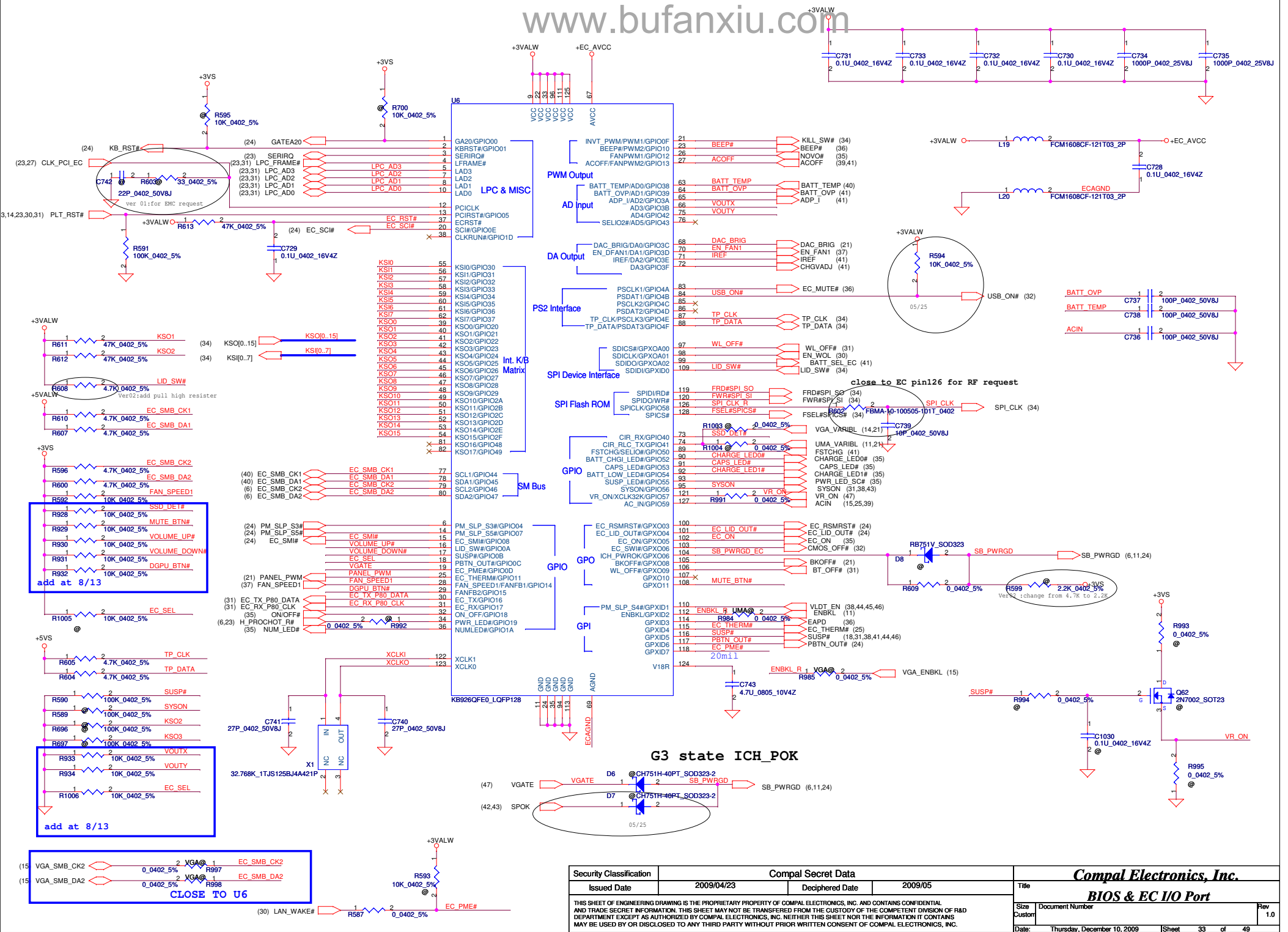
LPC_FRAME#_R	R974	1	2	0.0402_5%	LPC_FRAME#	(23,33)
LPC_AD3_R	R975	1	2	0.0402_5%	LPC_AD3	(23,33)
LPC_AD2_R	R976	1	2	0.0402_5%	LPC_AD2	(23,33)
LPC_AD1_R	R977	1	2	0.0402_5%	LPC_AD1	(23,33)
LPC_ADD0_R	R978	1	2	0.0402_5%	LPC_ADD0	(23,33)
CLK_PCI_DB					CLK_PCI_DB	(23)



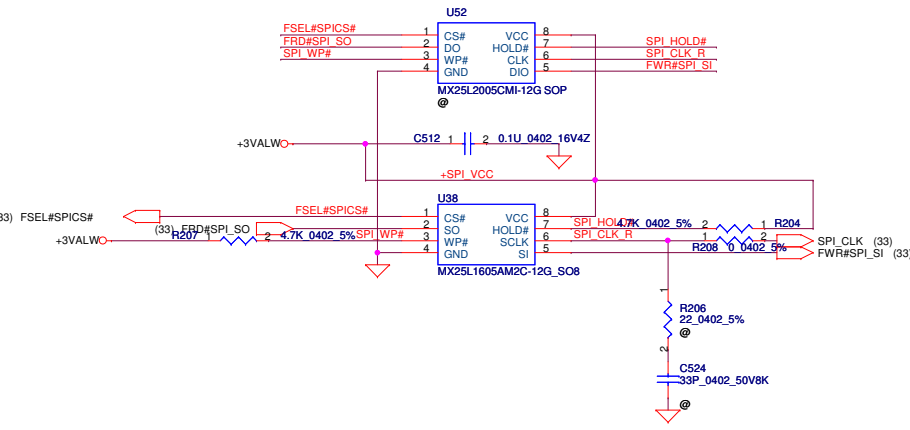
CMOS Camera Conn



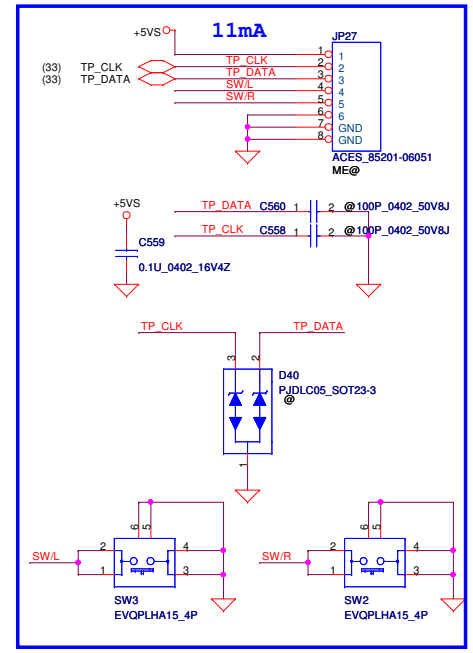
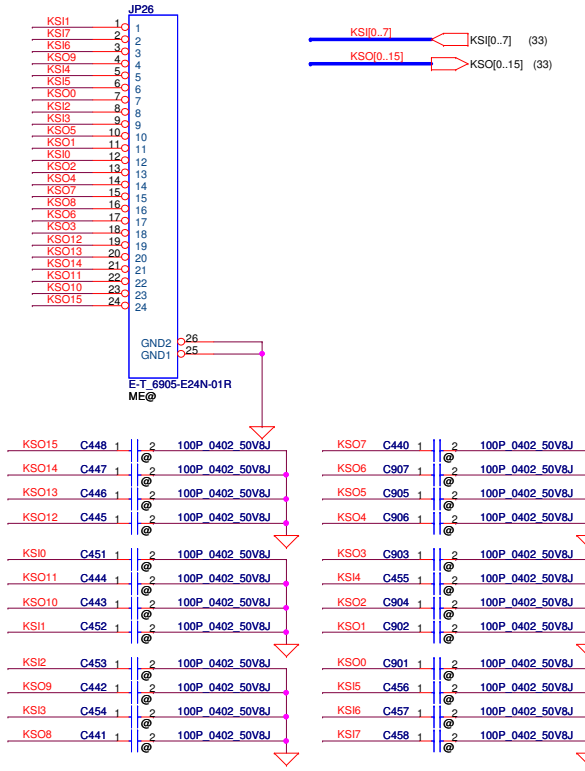
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				Date: Thursday, December 10, 2009	Sheet 32 of 49



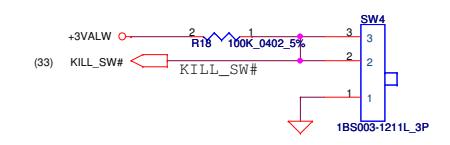
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Issued Date	2009/04/23	Deciphered Date	2009/05	Title	
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Size	Document Number	Rev		1.0	
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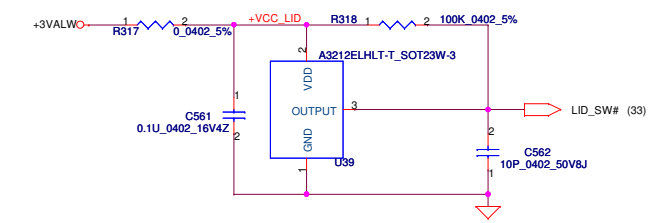
INT_KBD Conn.



Kill Switch



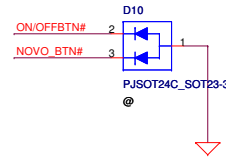
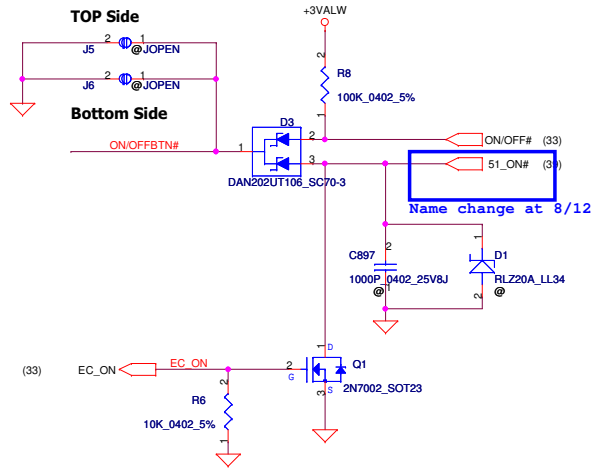
Lid Switch



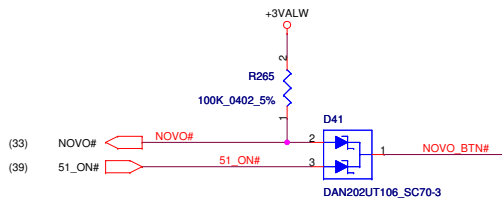
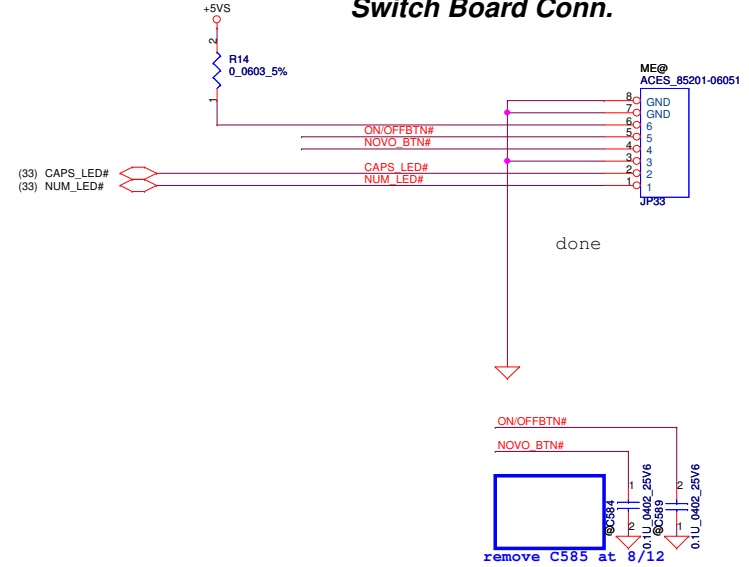
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title
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Size B	Document Number	LA-5972P	Rev	1.0
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Power Button

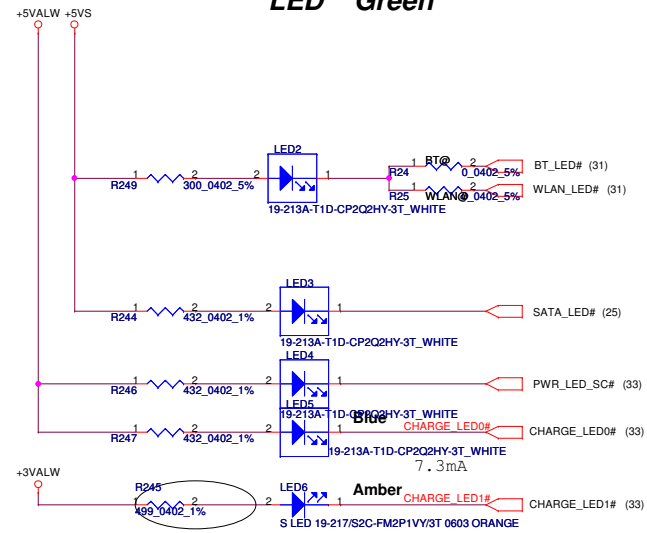
ON/OFF switch



Switch Board Conn.

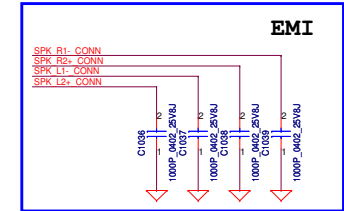
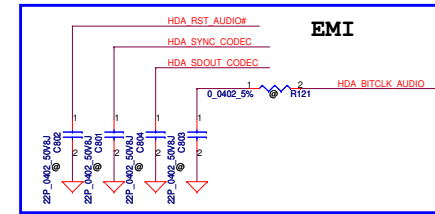


LED Green



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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



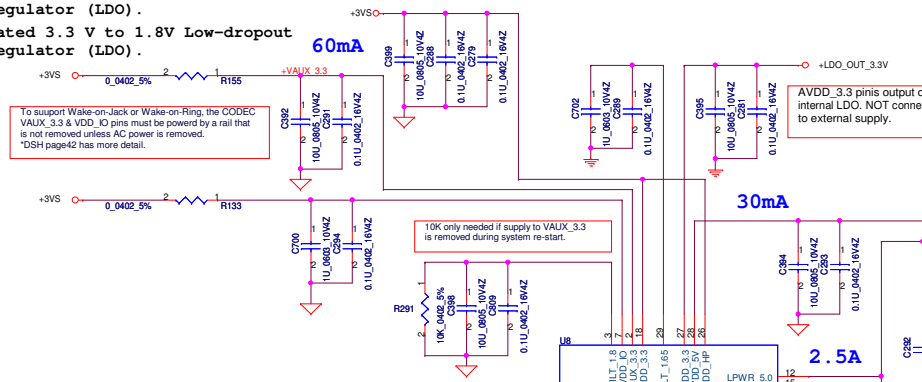
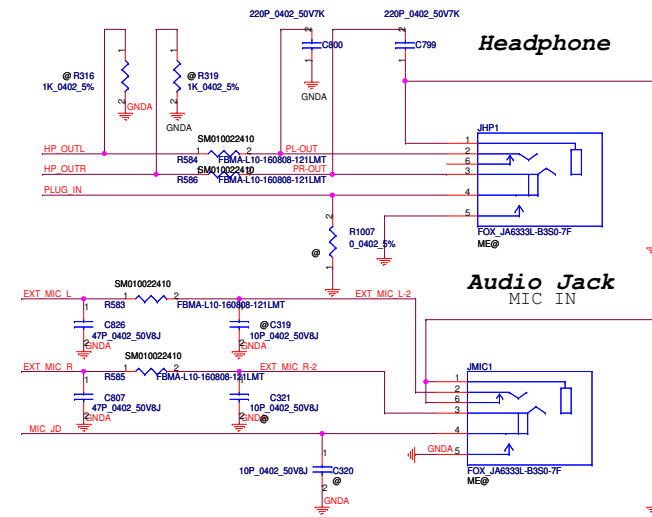
Port C
Port A

Sense resistors must be connected same power that is used for VAUX_3.3

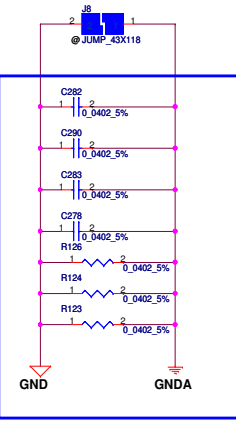
External MIC

wide 20MIL

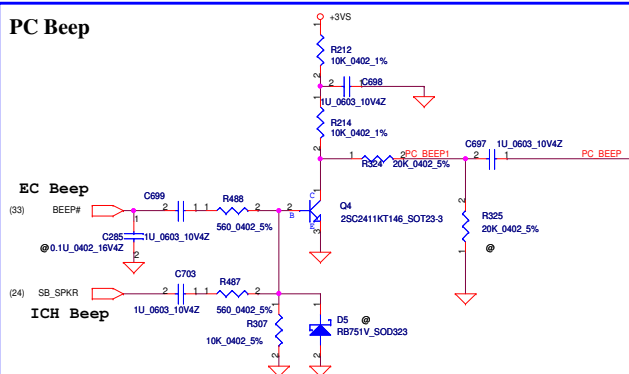
SPK R1-	L37	1	FBMA-L11-160808-121LMA30T	SPK R1- CONN	4
SPK R2-	L36	1	FBMA-L11-160808-121LMA30T	SPK R2- CONN	3
SPK L1-	L36	1	FBMA-L11-160808-121LMA30T	SPK L1- CONN	2
SPK L2-	L34	1	FBMA-L11-160808-121LMA30T	SPK L2- CONN	1



EAPD active low
0=power down ex AMP
1=power up ex AMP

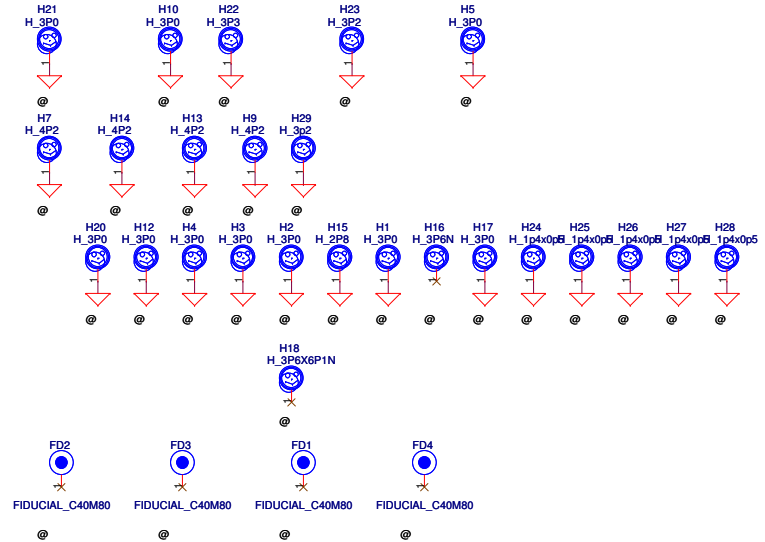
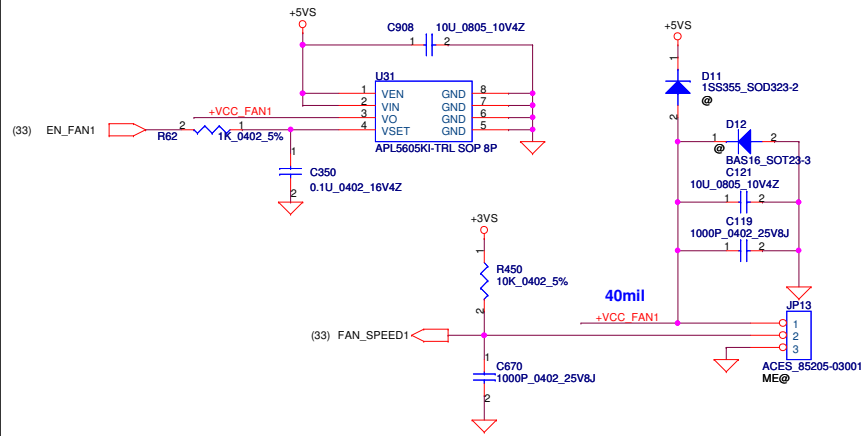


Audio Jack



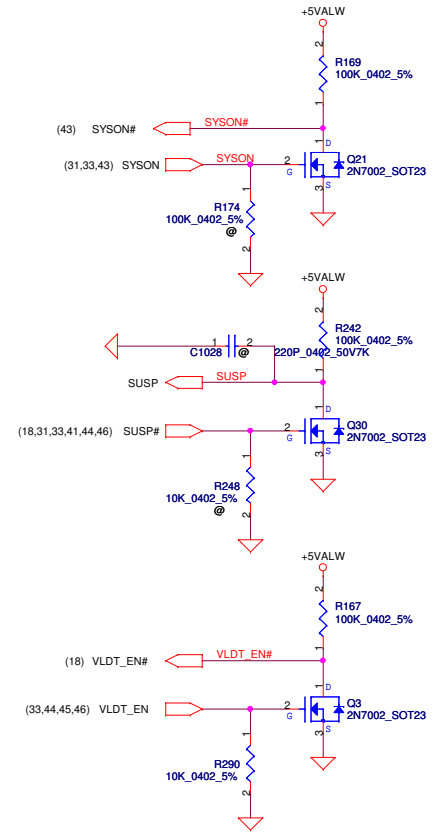
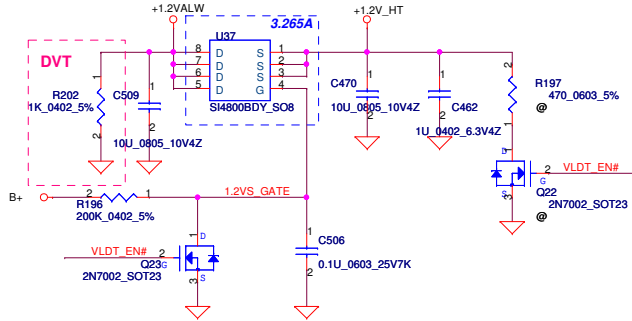
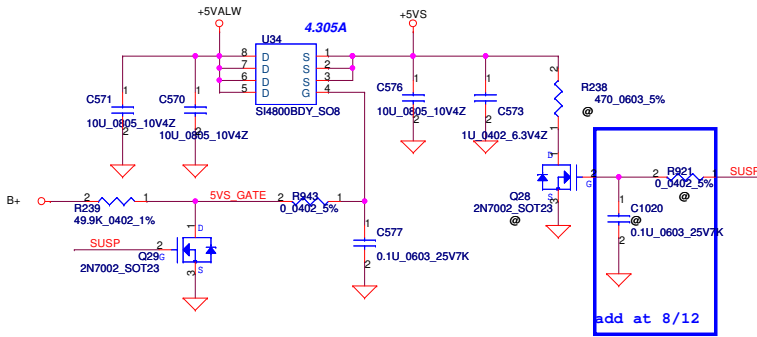
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Size	C	Document Number	LA-5972P	Rev
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FAN1 Conn

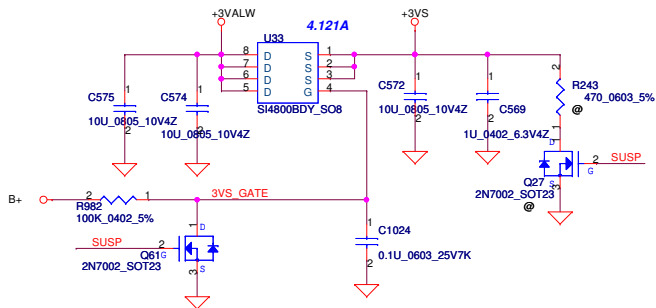


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				Document Number LA-5972P
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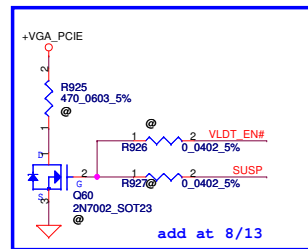
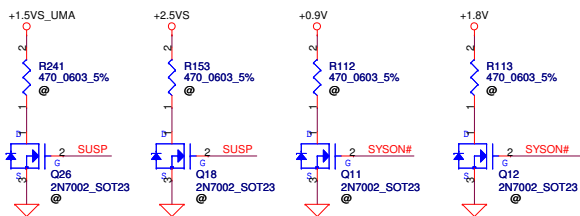
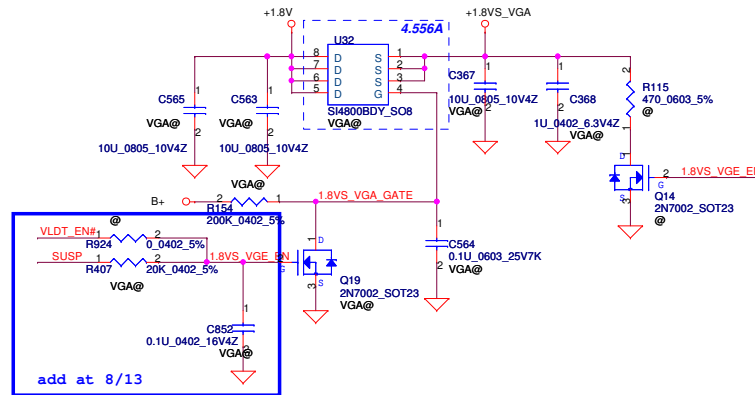
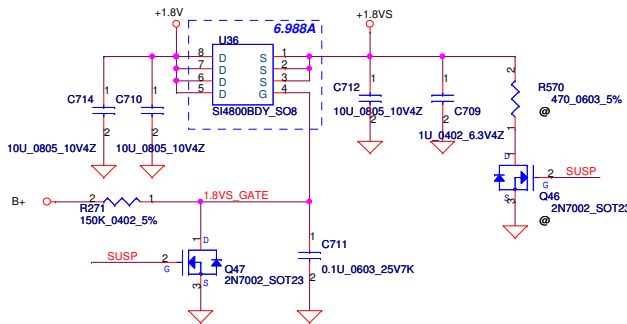
+5VALW TO +5VS



+3VALW TO +3VS



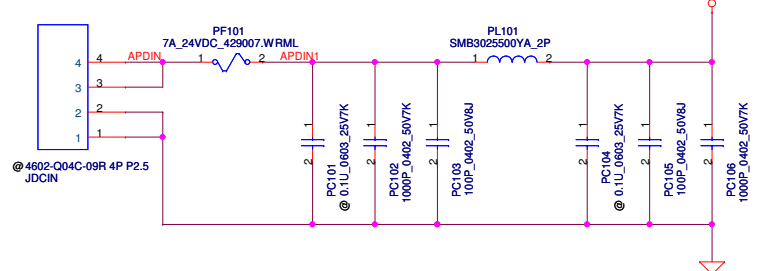
+1.8V to +1.8VS



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				DC Interface		
				Size B	Document Number	Rev 1.0
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				Date:	Thursday, December 10, 2009	Sheet 38 of 49

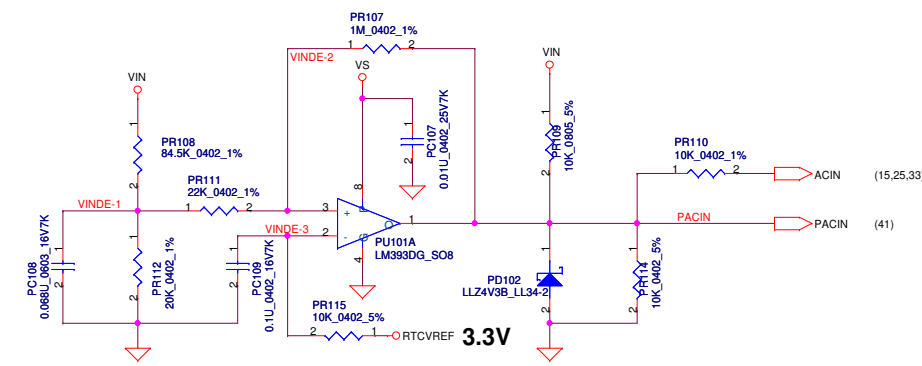
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DC030006J00



Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

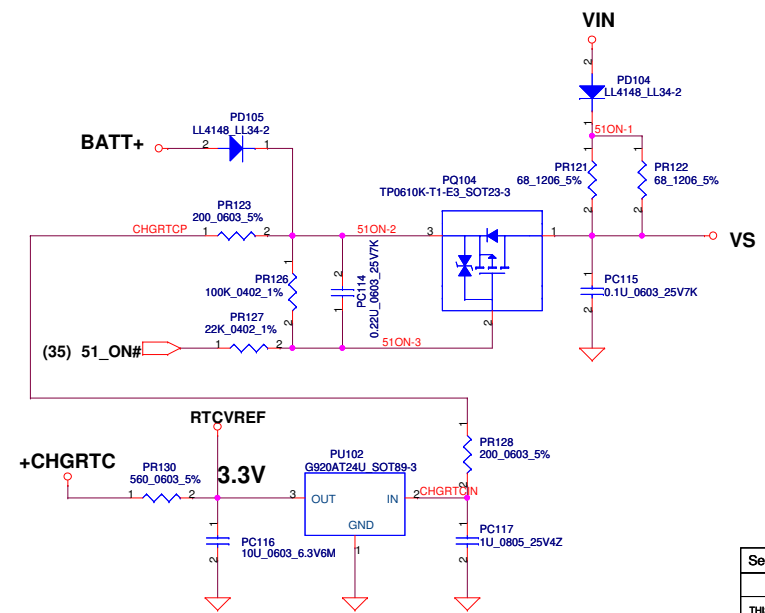
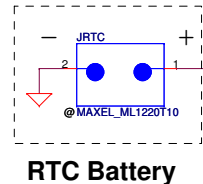
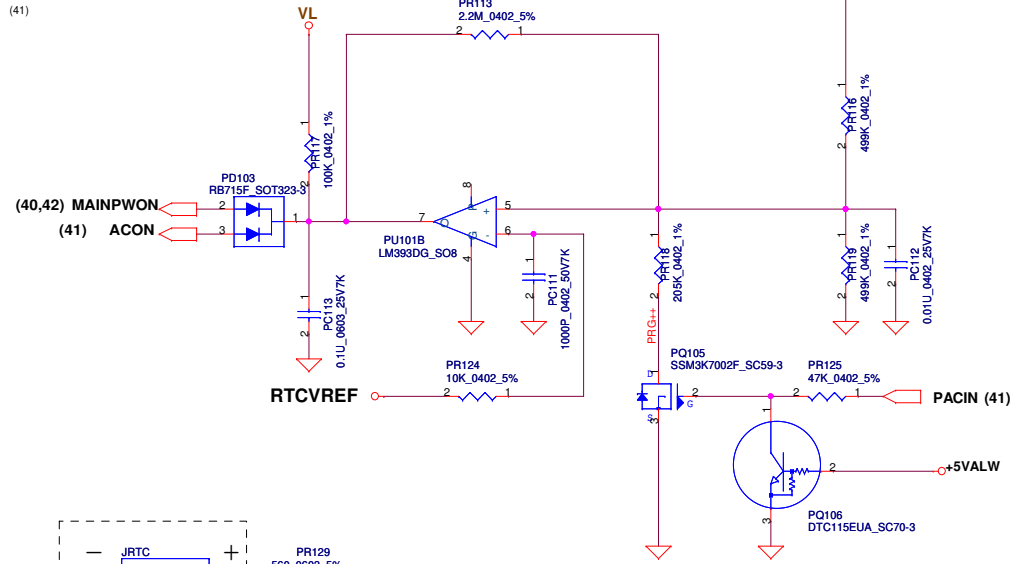
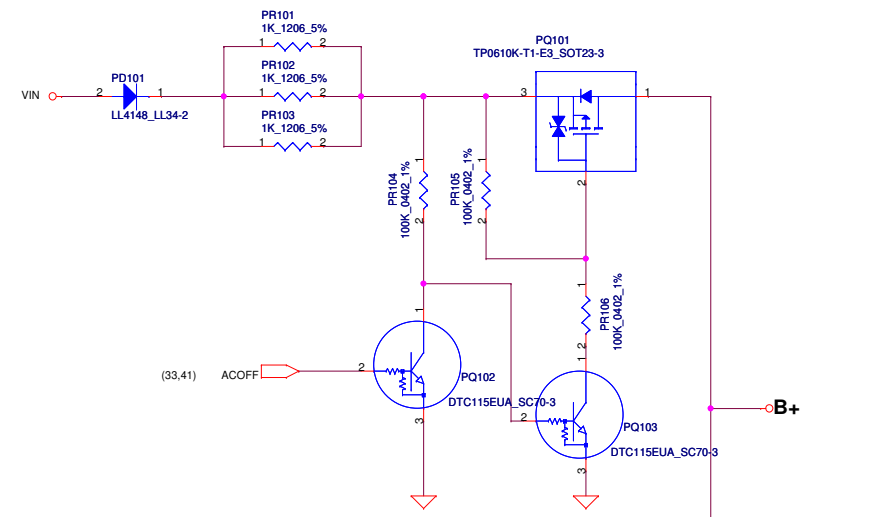


Precharge detector

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

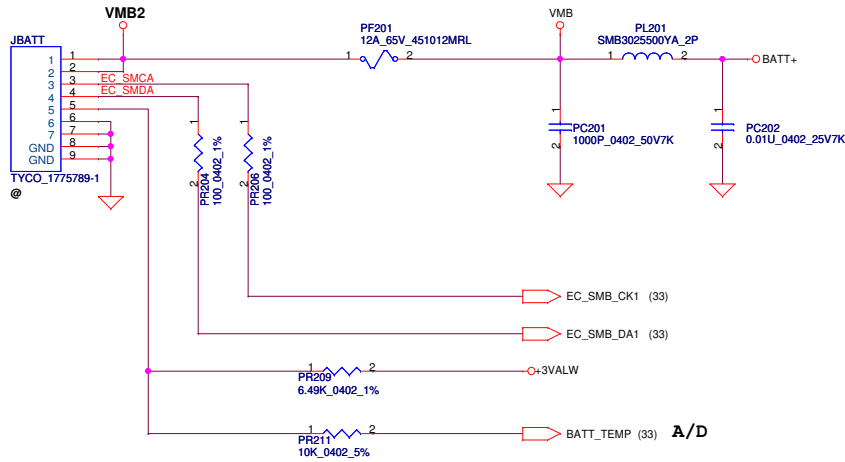
BATT ONLY

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



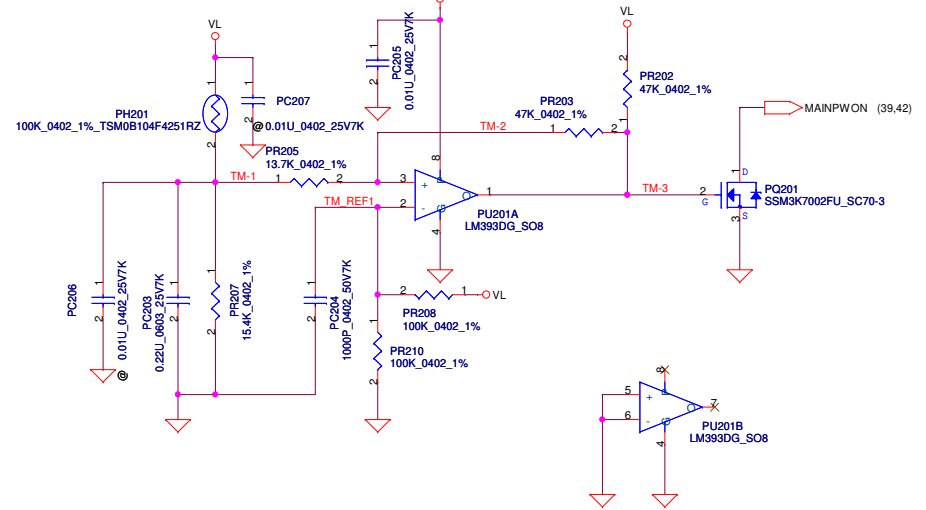
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Compal Electronics, Inc.			
Title: DCIN & DETECTOR			
Size: Custom	Document Number:	Rev: 1.0	
Date: Thursday, December 10, 2009	Sheet: 39	of 49	

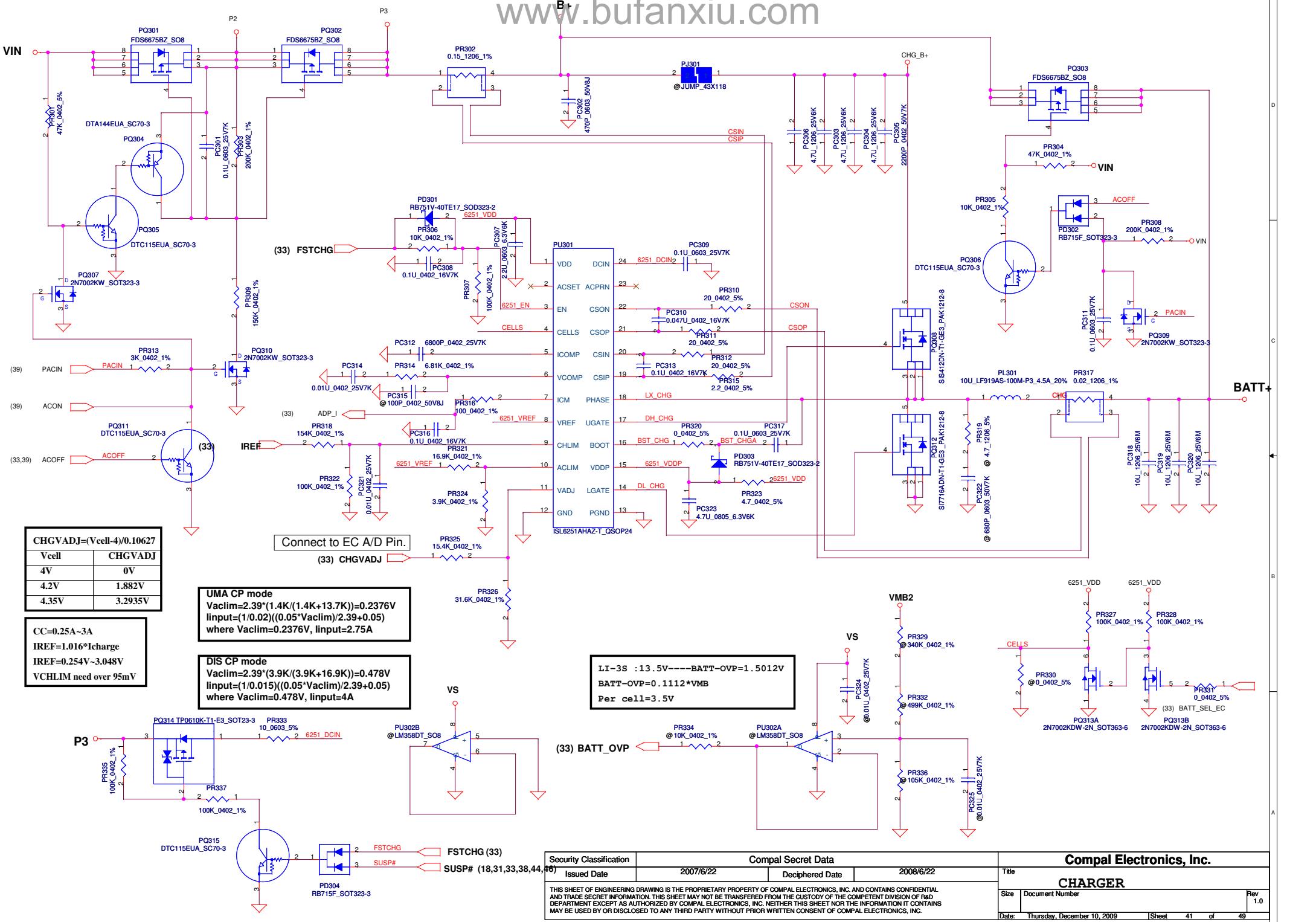


PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

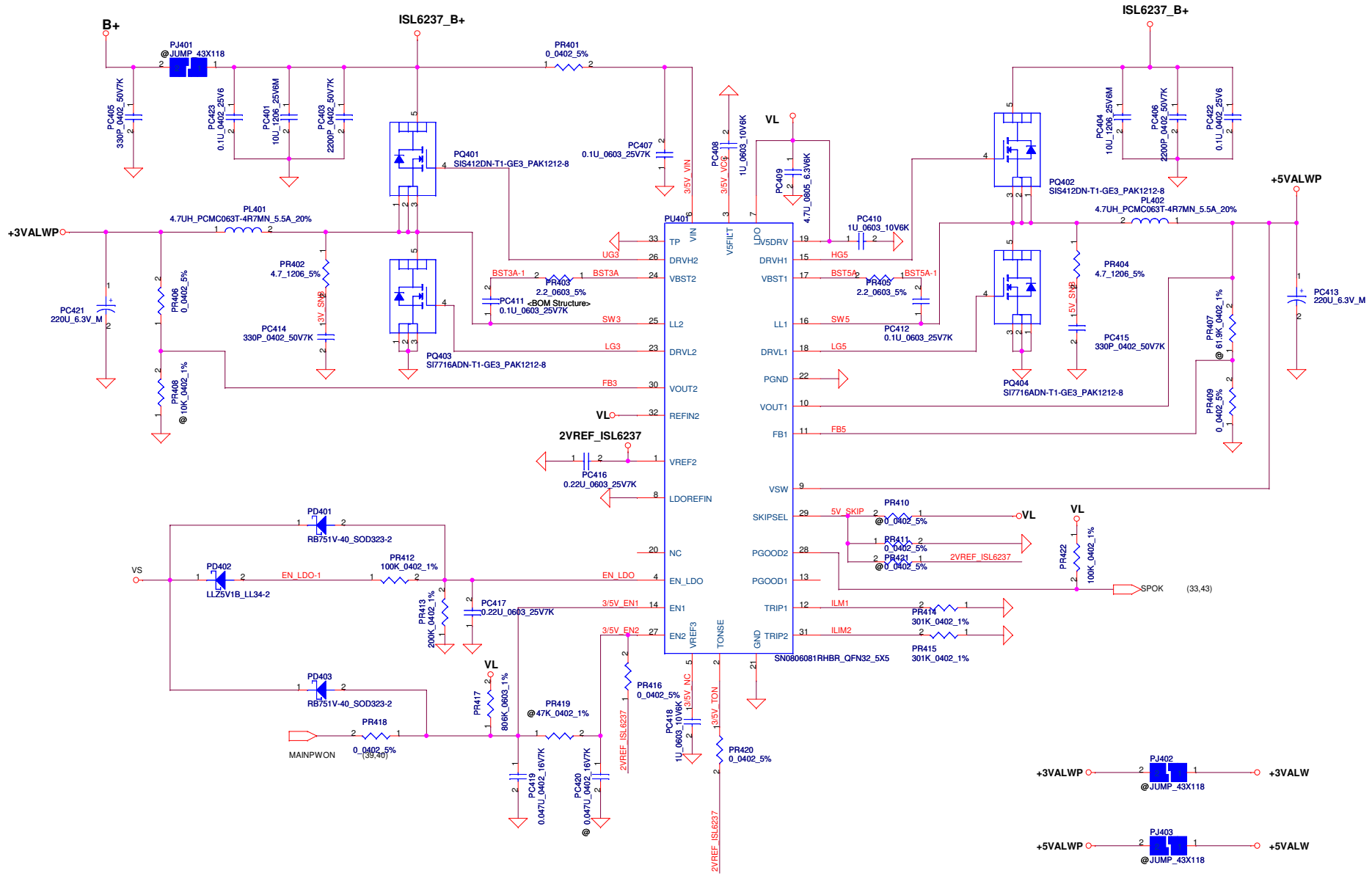
UMA CP mode
 $V_{acli} = 2.39 * (1.4K / (1.4K + 13.7K)) = 0.2376V$
 $I_{in} = (1 / 0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 0.2376V$, $I_{in} = 2.75A$

DIS CP mode
 $V_{acli} = 2.39 * (3.9K / (3.9K + 16.9K)) = 0.478V$
 $I_{in} = (1 / 0.015) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 0.478V$, $I_{in} = 4A$

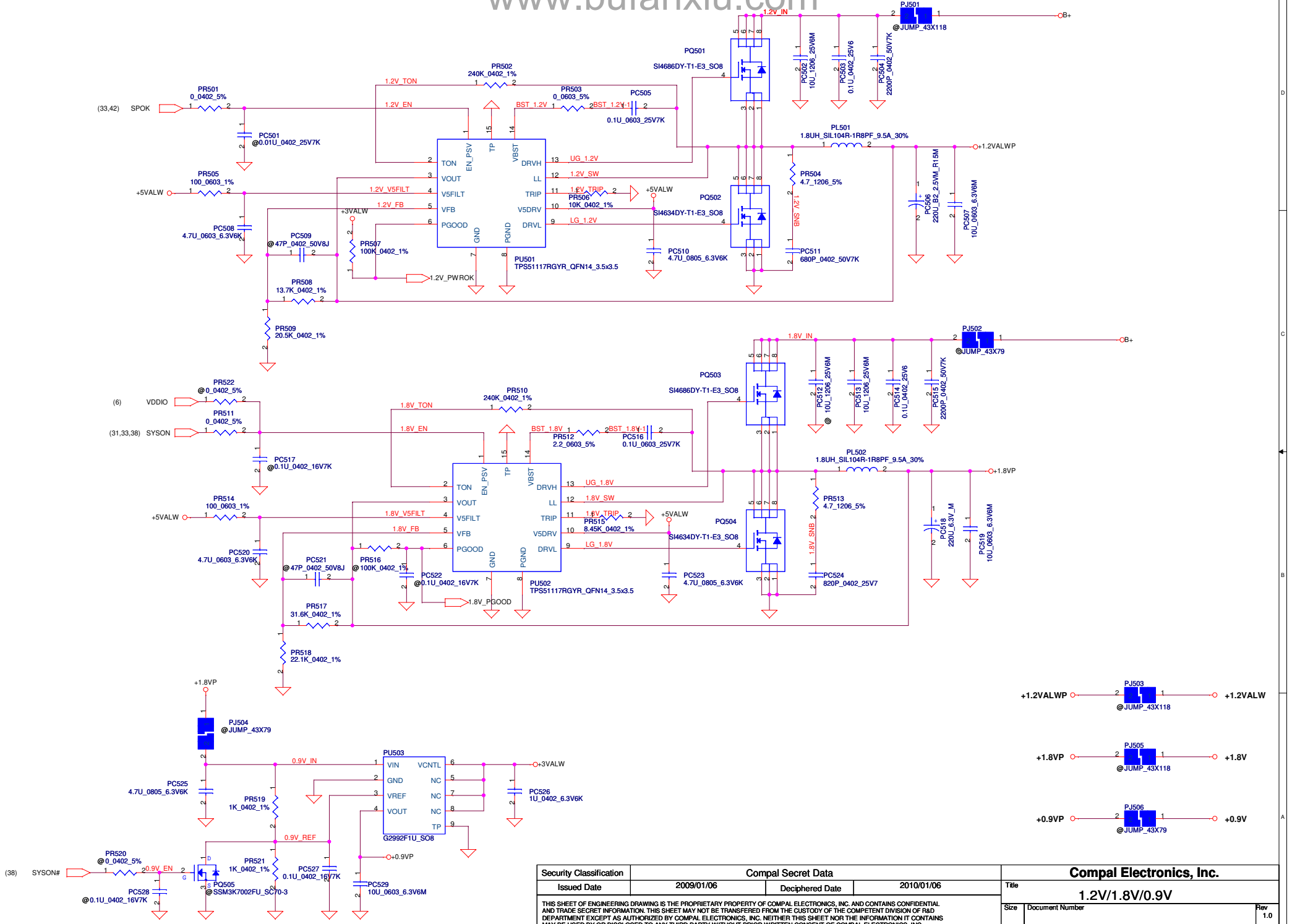
LI-3S : 13.5V --- BATT-OVP = 1.5012V
 $BATT-OVP = 0.1112 * VMB$
 Per cell = 3.5V

Connect to EC A/D Pin.
 (33) CHGVADJ

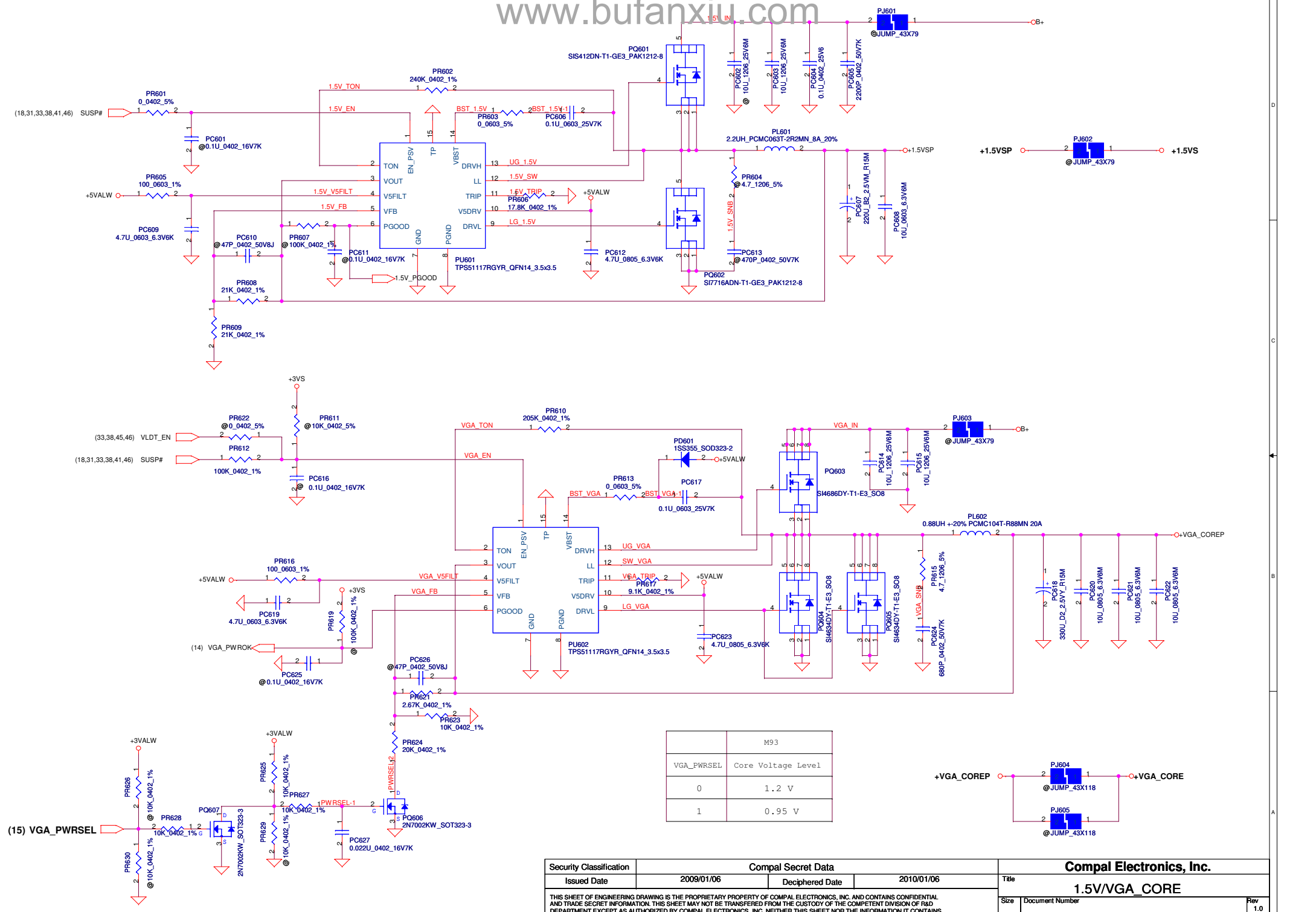
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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Compal Electronics, Inc.
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				Document Number
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				1.0
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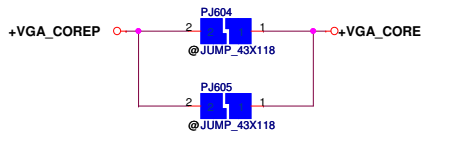
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Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title
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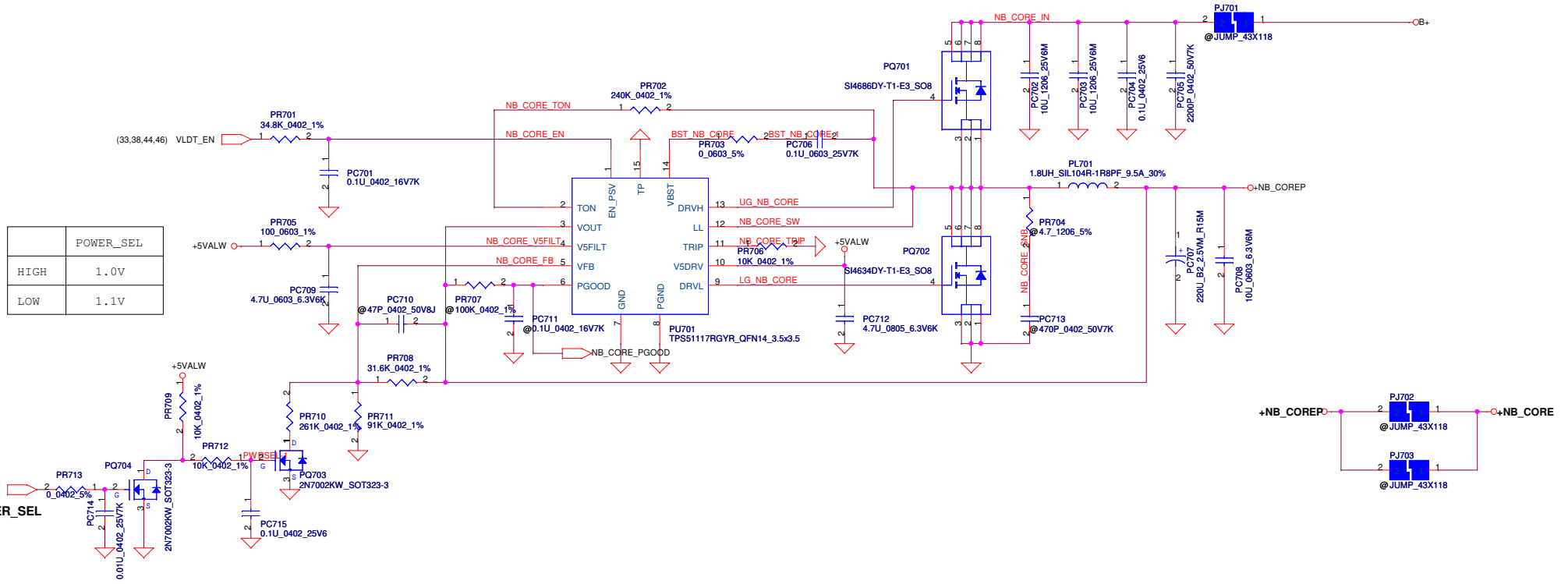
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title
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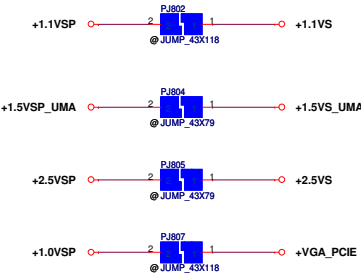
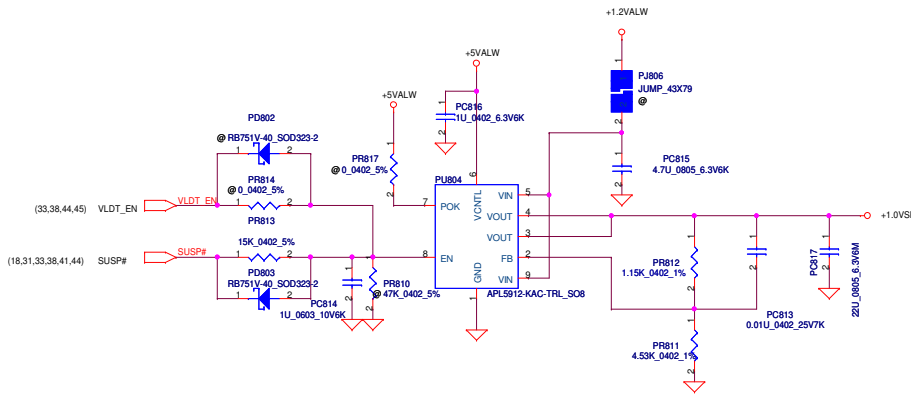
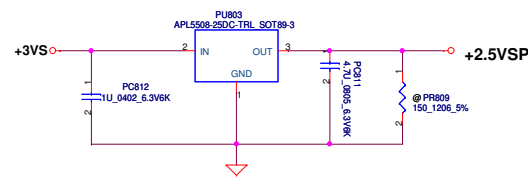
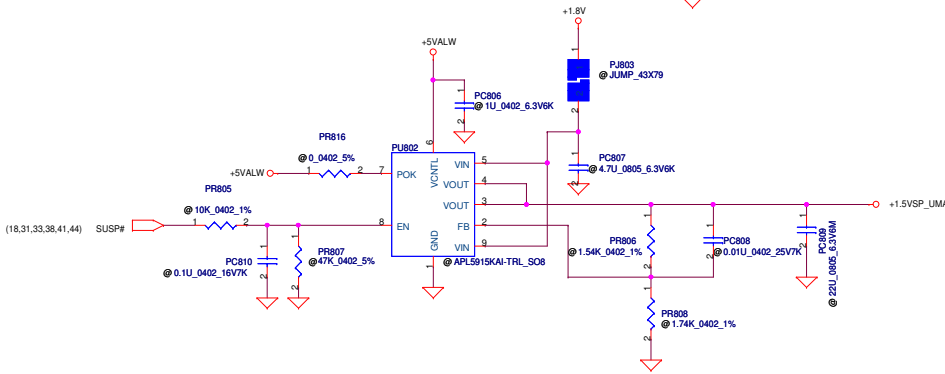
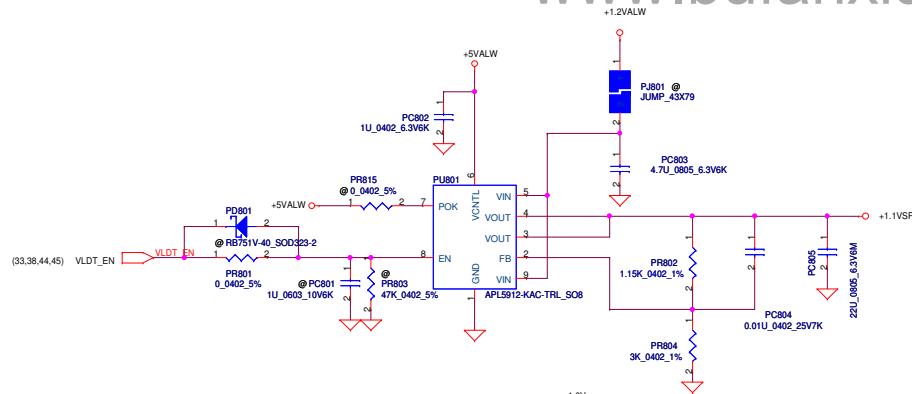
	M93
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V



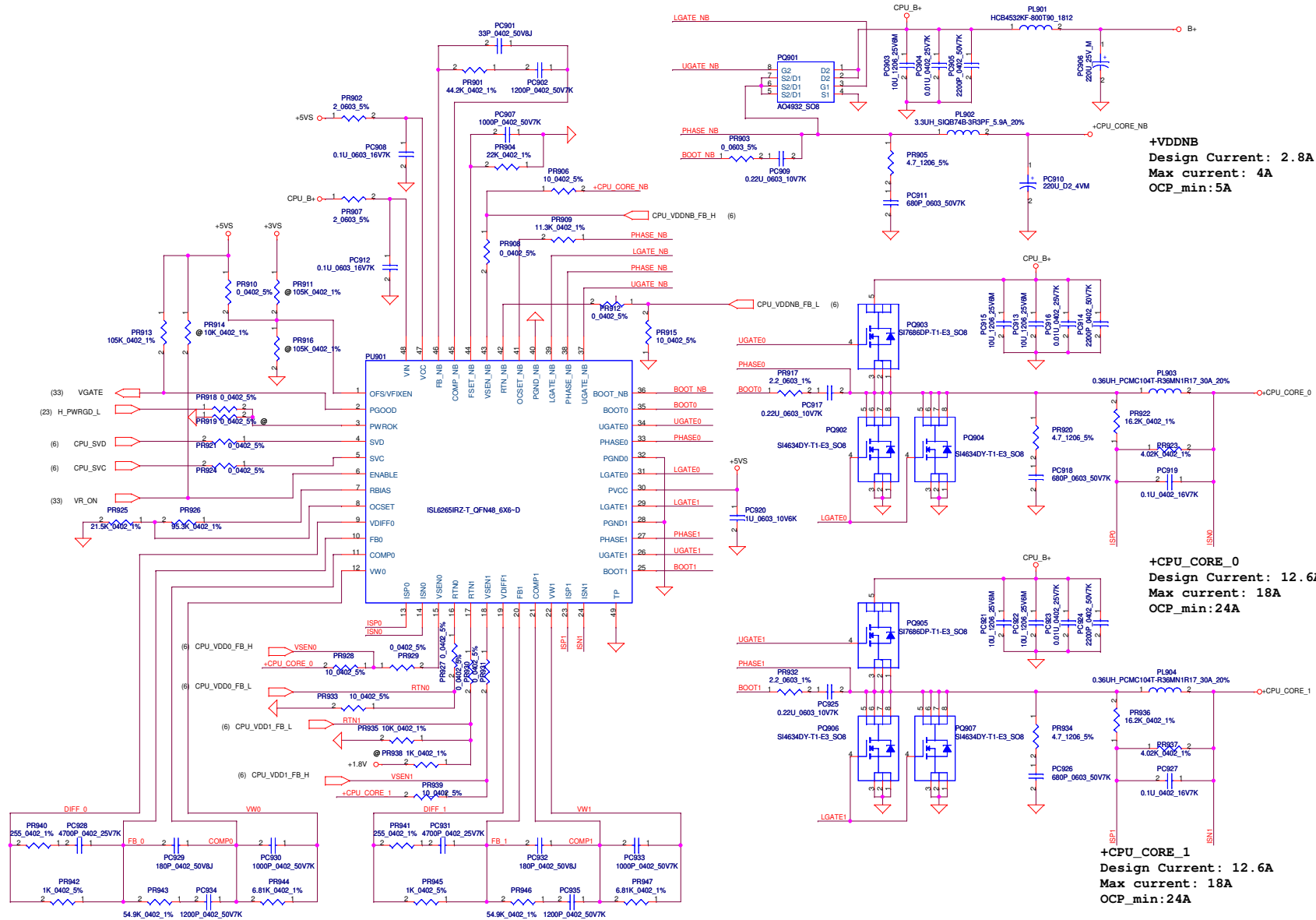
POWER_SEL	
HIGH	1.0V
LOW	1.1V



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	Part	M93
VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Adjust power sequence for VGA_PCIE by HW request	P46	PR831=15K	2009.10.27	EVT
2	Change PC108 from 1000pF to 0.068uF for issue solution	P39	PC108=0.068uF	2009.11.17	PVT
3	Add snubber R & C and modify boost resistor for 1.8VP	P43	PR512=2.2 ohm;PR513=4.7 ohm;PC524=820pF	2009.11.17	PVT
4	Adjust power sequence	P45	PR701=34.8K,PC701=0.1uF Un-pop PR520,PQ505	2009.12.03	PVT
5					
6					
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8					
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17					

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1. change component AP2301GN to AO3413
2. remove R521, R517, R520 and R518, and reserve U49 , U50, R999, R1000, R1001 and R1002 for experiment Vari-bright function.
3. U6.18 add a pull up resistor R1005 and pull down resistor R1006 for check ENE KB926 version.
4. reserve R1003 and R1004 for Vari-bright test.
5. add J8, C1034, C1035, C1036, C1037, C1038 and C1039 for EMI request.
6. Change R583, R584, R585 and R586 Bead from SM010018110 to SM010022410.
7. reserve R1007 for EMI request.
8. Change C633, C640, C662, C948, C660 and C639 to 10pF for EMI rquest.

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				Size	Document Number	Rev
				B	LA-5972P	1.0
				Date:	Thursday, December 10, 2009	Sheet 49 of 49