

ZZZ1



FCB

SE000008600

# Compal Confidential

## Everest Schematics Document

### Intel Merom Processor with Crestline + DDRII + ICH8M

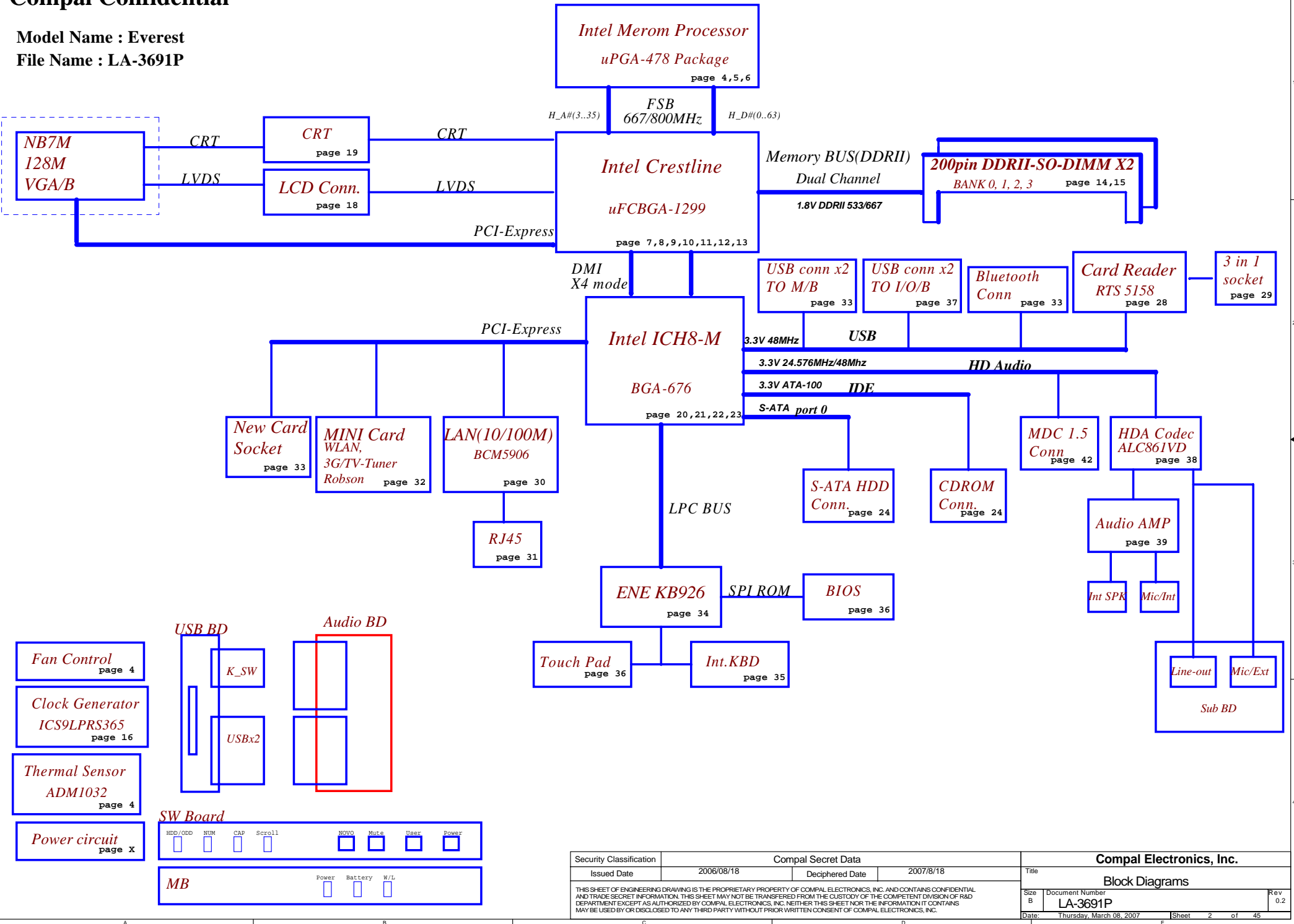
2007-03-05

REV: 0.2

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				B	LA-3691P
Date:				Thursday, March 08, 2007	Sheet 1 of 45

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Model Name : Everest  
File Name : LA-3691P



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Title Block Diagrams			
Size B	Document Number LA-3691P	Rev 0.2	
Date:	Thursday, March 08, 2007	Sheet	2 of 45

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

STATE	SIGNAL								
		SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	GMT-781	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

## ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

## BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

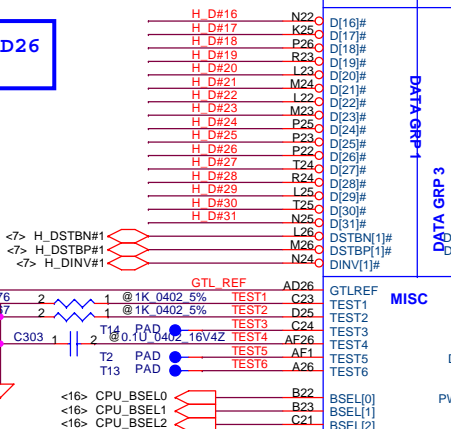
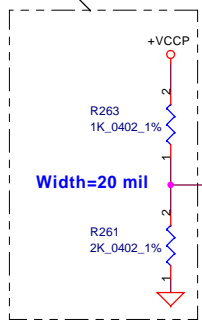
## PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

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Close to CPU pin AD26 within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

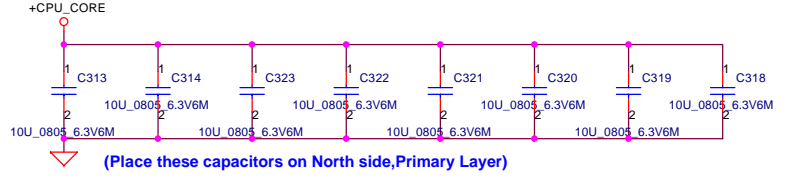
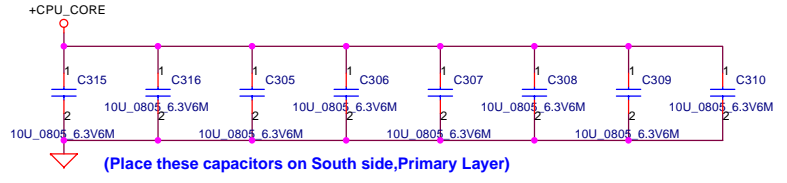
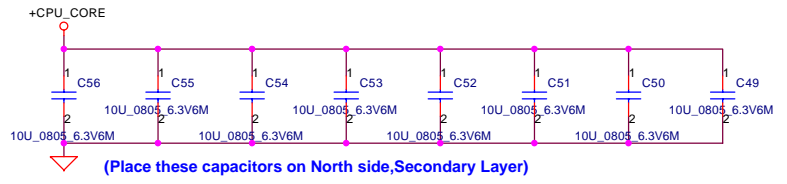
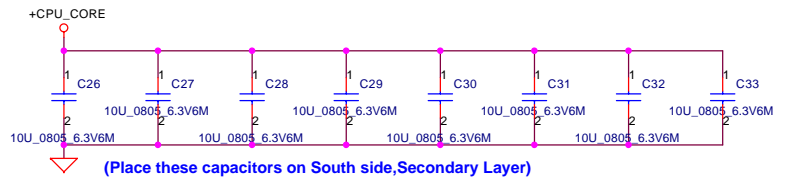
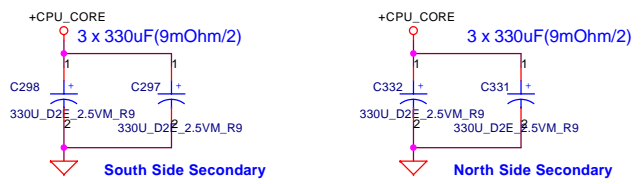
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

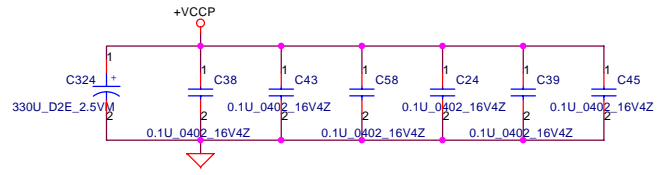
Close to CPU pin within 500mils.

JP15D		
A4	VSS[001]	D6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	A2
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N23	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
		AF25

FOX\_PZ4782A-274M-41\_Merom  
ME@



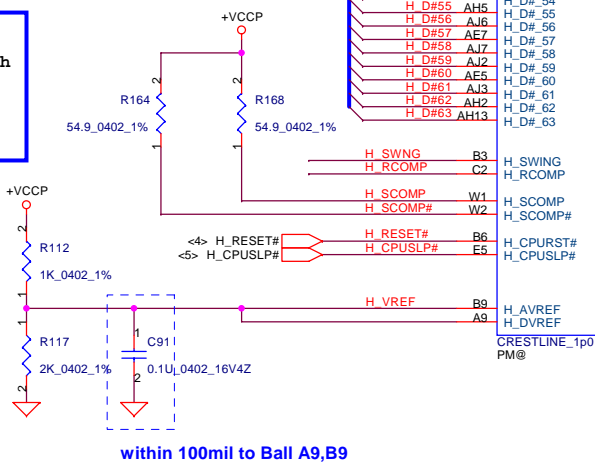
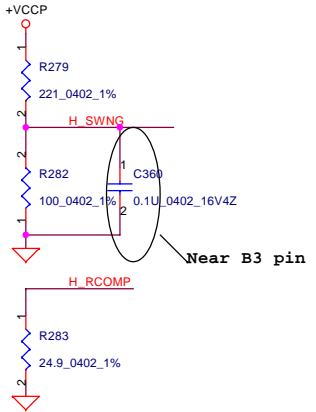
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



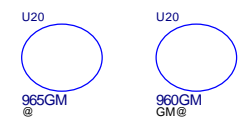
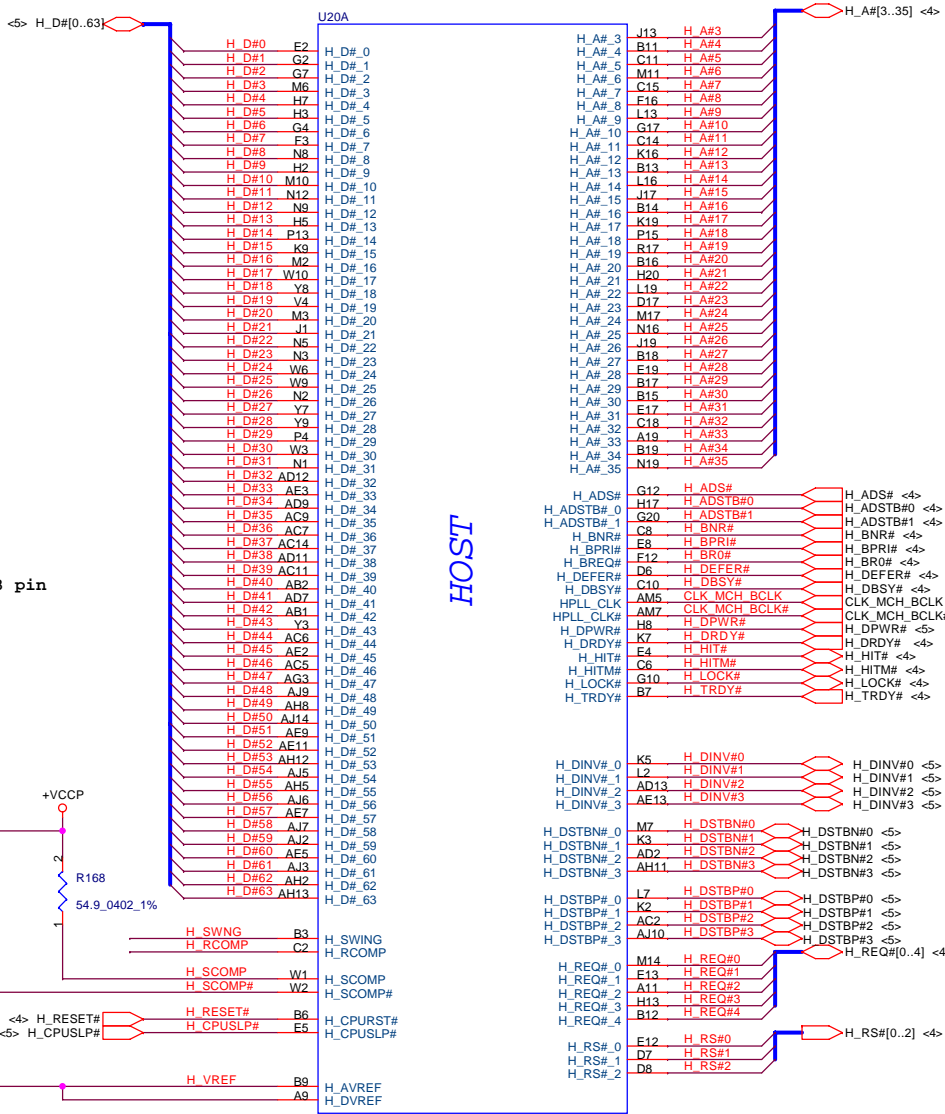
9/25 10U checked. OK for use!

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Size B	Document Number			Date:	Rev
	LA-3691P			Thursday, March 08, 2007	0.2
				Sheet	6 of 45

**layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

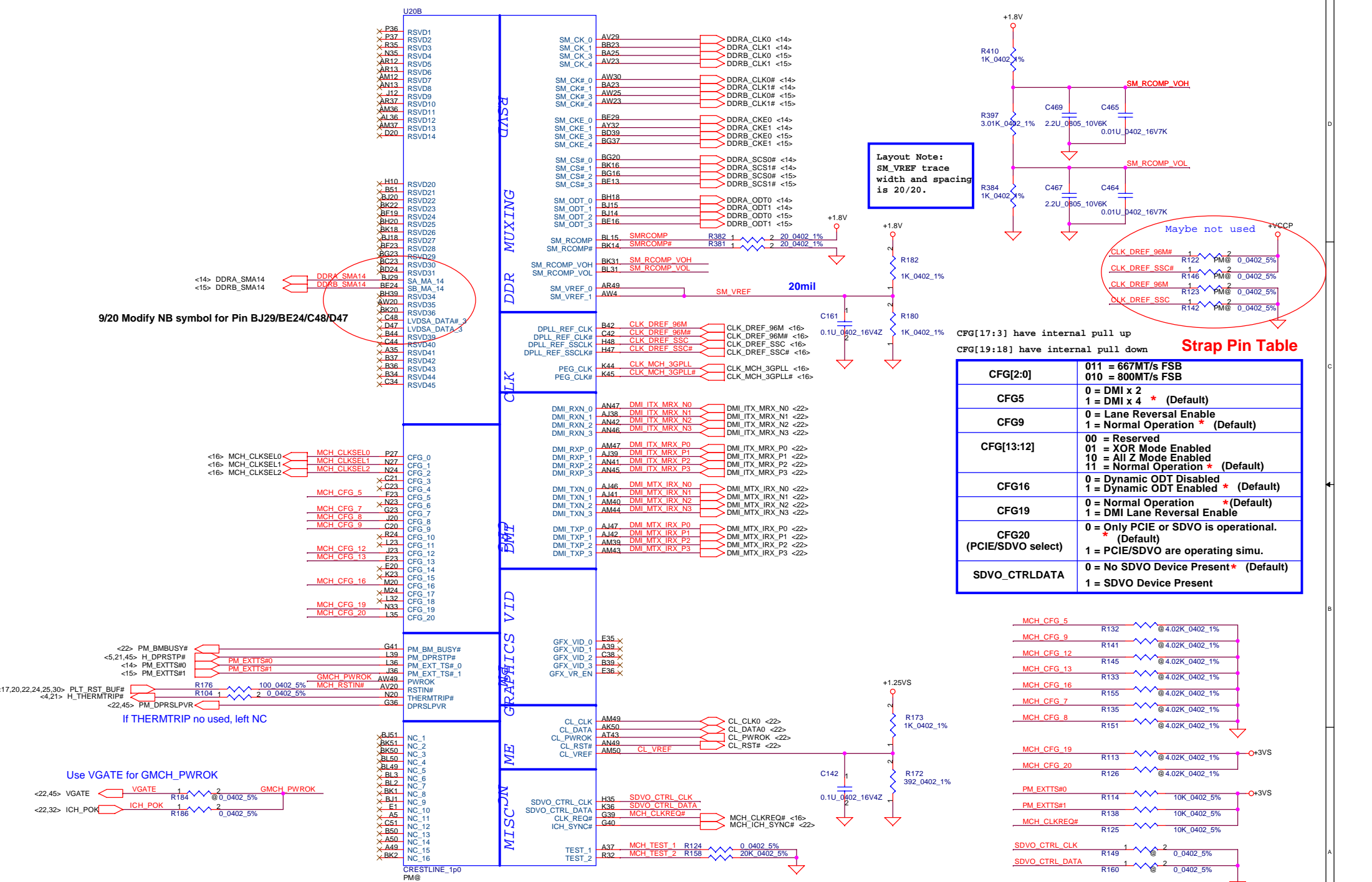


**Layout Note:**  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

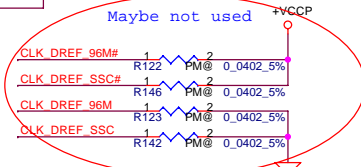


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Title Crestline (1/7)-GTL		
Size B	Document Number LA-3691P	Rev 0.2
Date:	Thursday, March 08, 2007	Sheet 7 of 45



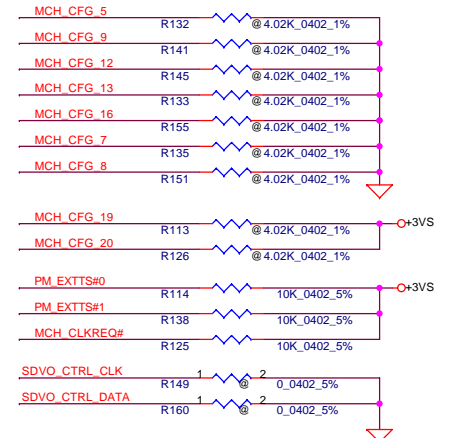
**Layout Note:**  
SM\_VREF trace width and spacing is 20/20.



**Strap Pin Table**

CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down

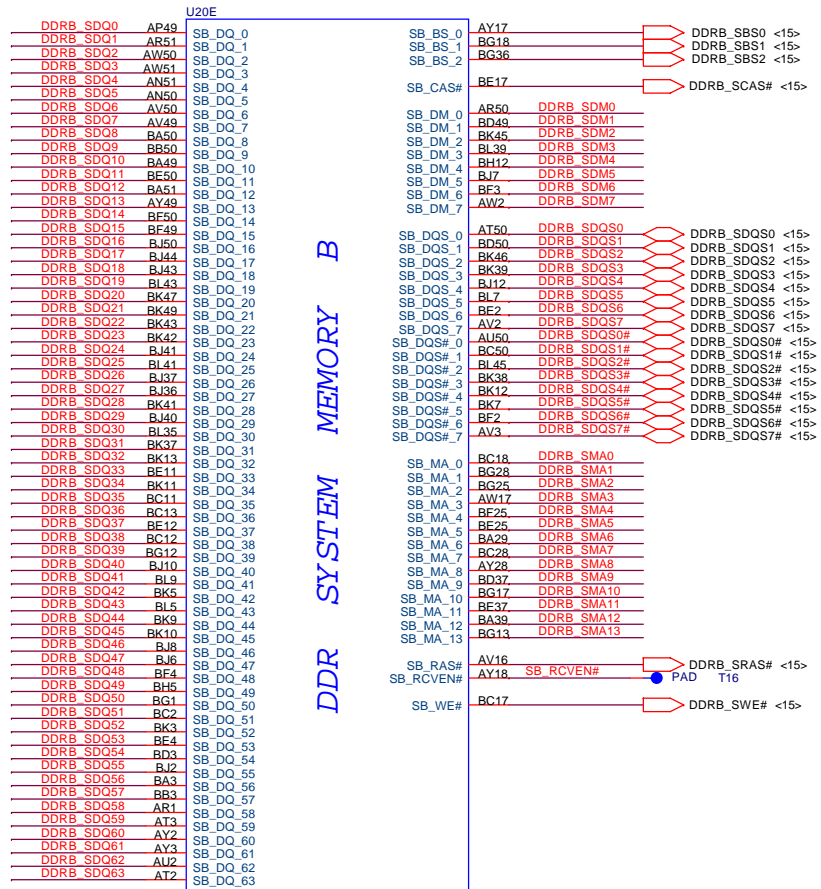
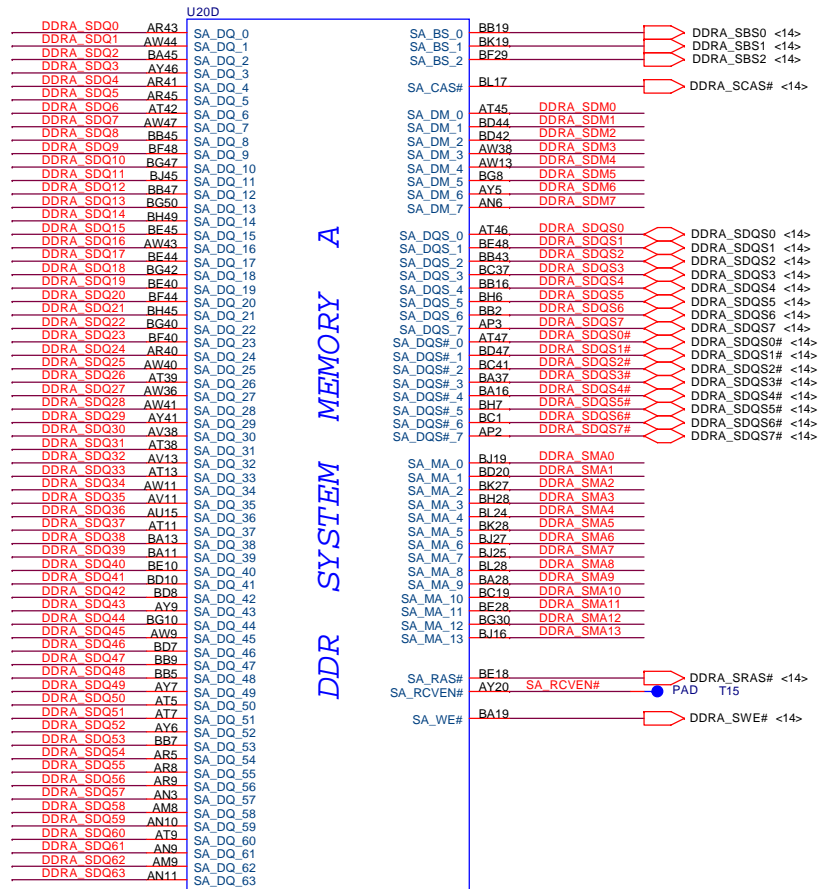
CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled * (Default) 1 = Dynamic ODT Enabled *
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simul.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present





<14> DDRA\_SDQ[0..63] ↔ DDRA\_SDQ[0..63]  
 <14> DDRA\_SDM[0..7] ↔ DDRA\_SDM[0..7]  
 <14> DDRA\_SMA[0..13] ↔ DDRA\_SMA[0..13]

<15> DDRB\_SDQ[0..63] ↔ DDRB\_SDQ[0..63]  
 <15> DDRB\_SDM[0..7] ↔ DDRB\_SDM[0..7]  
 <15> DDRB\_SMA[0..13] ↔ DDRB\_SMA[0..13]

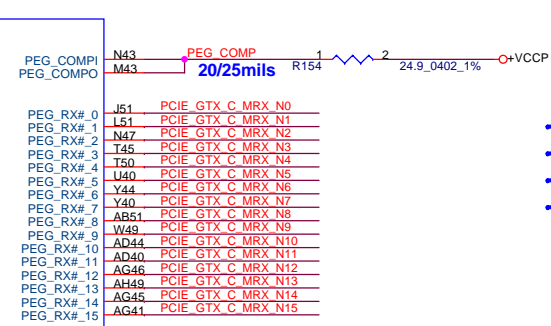
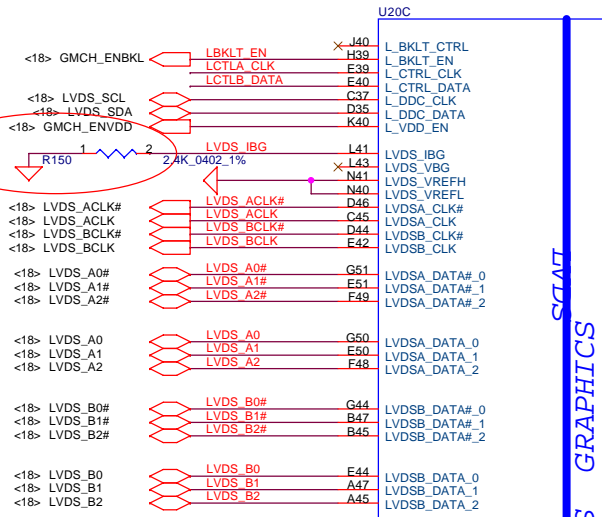


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

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Size	Document Number	Date:		Rev	
B	LA-3691P	Thursday, March 08, 2007		9	of 45
				Sheet	9 of 45

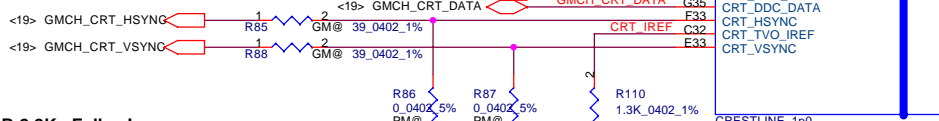
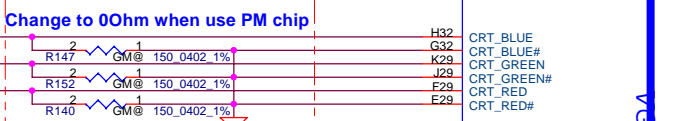
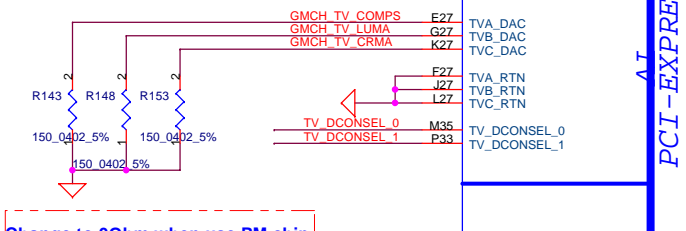
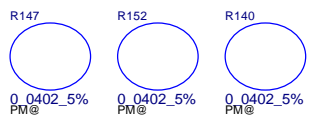
CRB 2.37K\_1% to GND



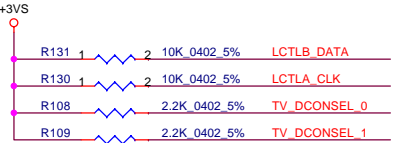
- PCIE\_MTX\_C\_GRX\_N0[0..15] <17>
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- PCIE\_GTX\_C\_MRX\_N0[0..15] <17>
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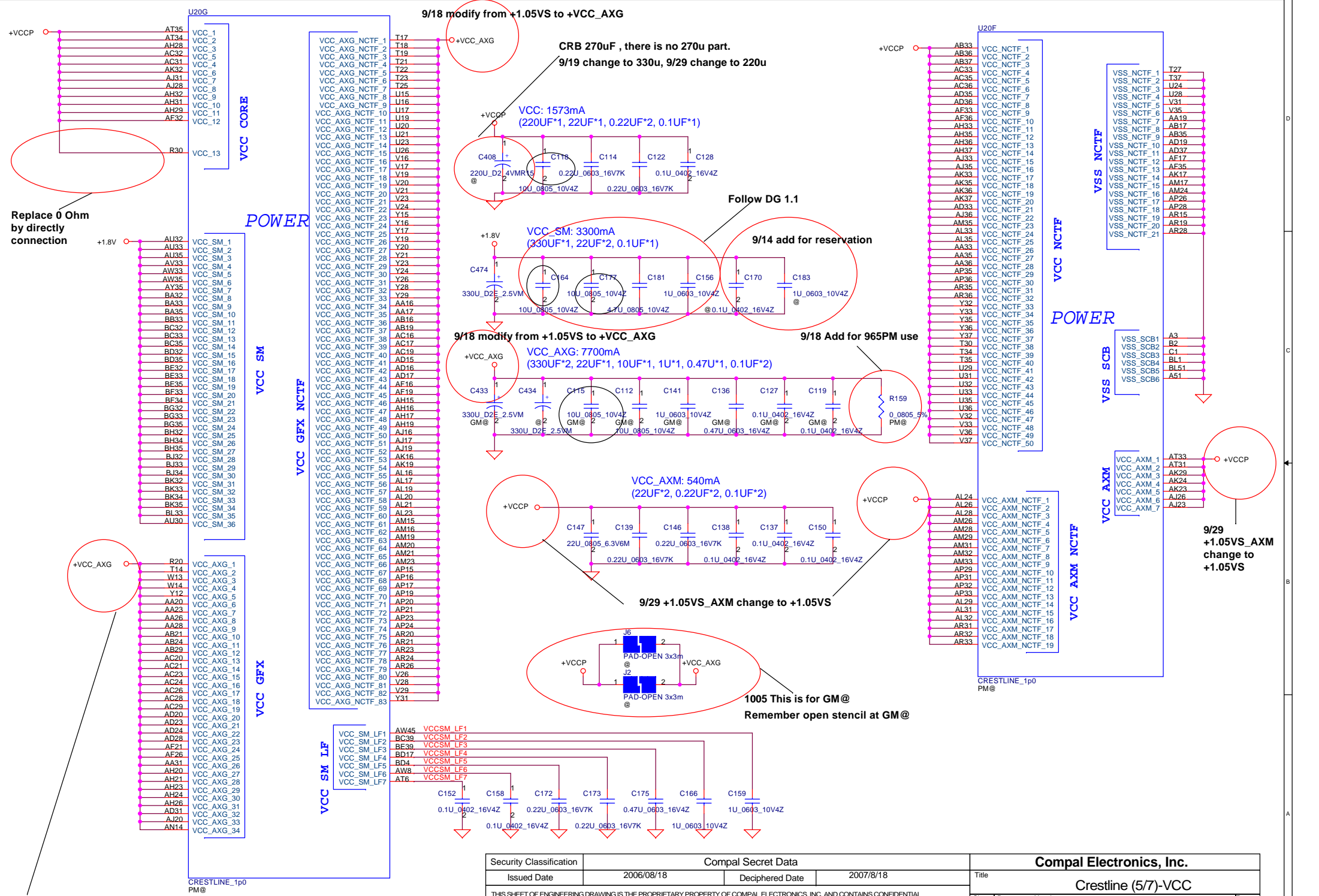
Signal	Pin	Value	Notes
N45	PCIE_MTX_GRX_N0	C124 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N0
U39	PCIE_MTX_GRX_N1	C396 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N1
U47	PCIE_MTX_GRX_N2	C130 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N2
N51	PCIE_MTX_GRX_N3	C400 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N3
R50	PCIE_MTX_GRX_N4	C140 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N4
T42	PCIE_MTX_GRX_N5	C410 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N5
W48	PCIE_MTX_GRX_N6	C145 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N6
W48	PCIE_MTX_GRX_N7	C422 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N7
W38	PCIE_MTX_GRX_N8	C153 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N8
AD39	PCIE_MTX_GRX_N9	C425 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N9
AC46	PCIE_MTX_GRX_N10	C157 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N10
AC49	PCIE_MTX_GRX_N11	C430 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N11
AC42	PCIE_MTX_GRX_N12	C165 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N12
AC41	PCIE_MTX_GRX_N13	C432 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N13
AE49	PCIE_MTX_GRX_N14	C171 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N14
AH44	PCIE_MTX_GRX_N15	C442 1	2 PM@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_N15



CRB 2.2K , Follow!

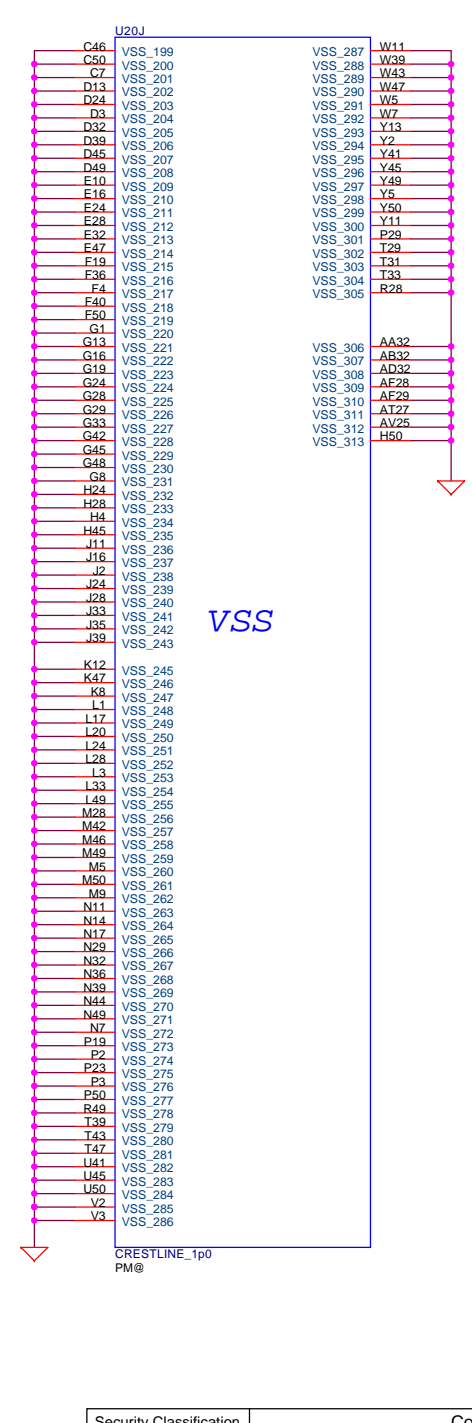
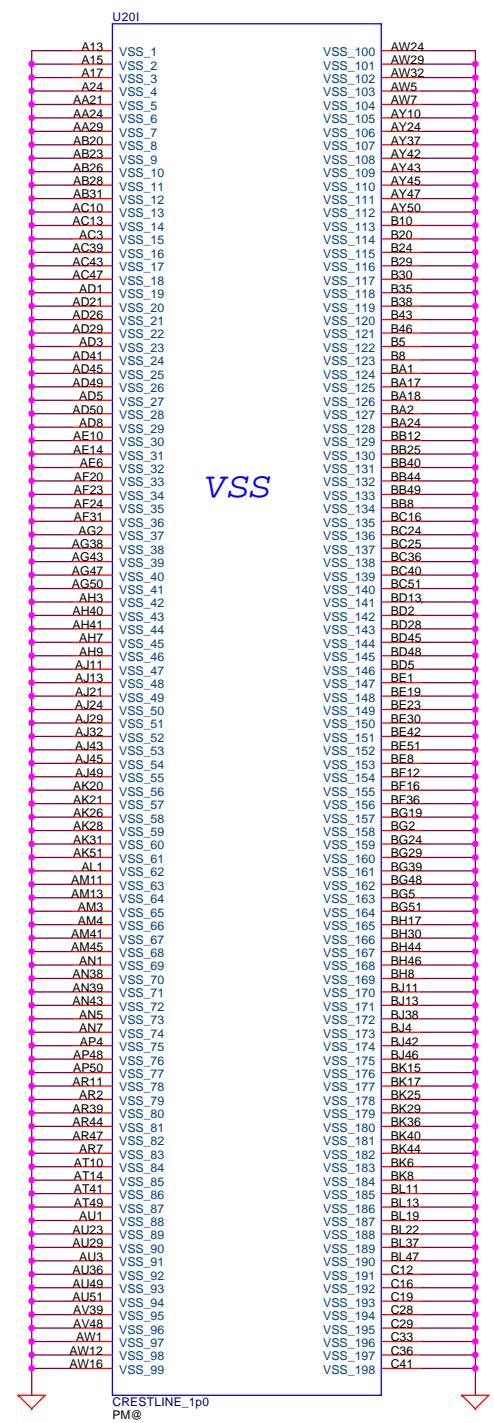


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Size B	Document Number	Rev		0.2	
	LA-3691P				
Date:	Thursday, March 08, 2007	Sheet	10	of	45



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Size	Document Number	Rev		
B	LA-3691P	0.2		
Date:	Thursday, March 08, 2007	Sheet	11	of 45

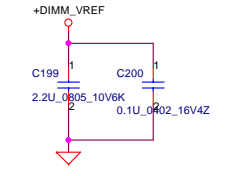
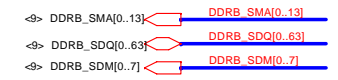
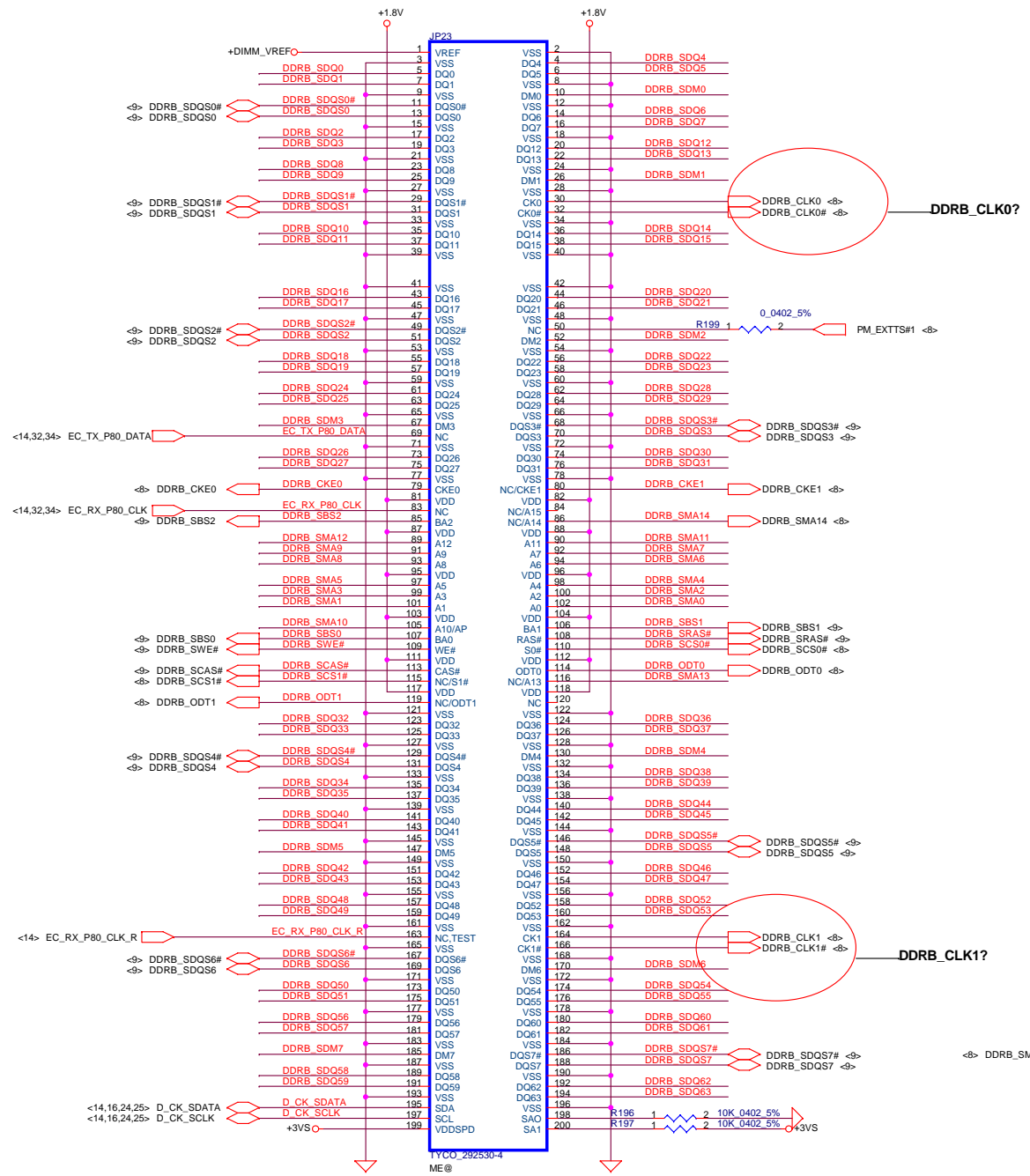




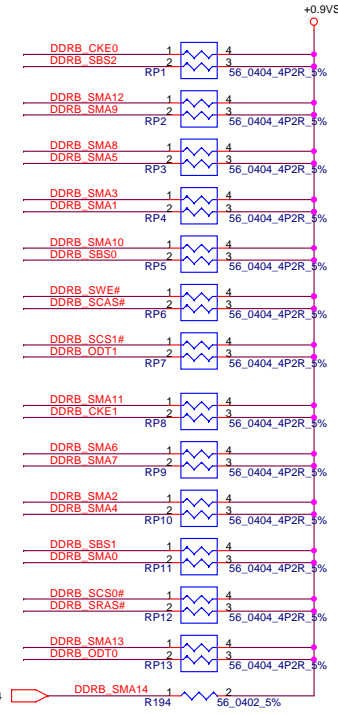
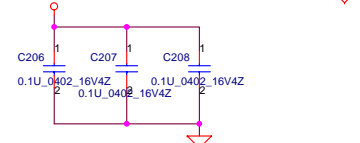
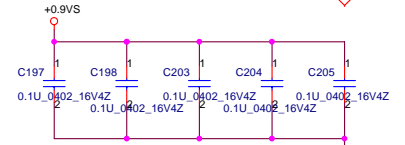
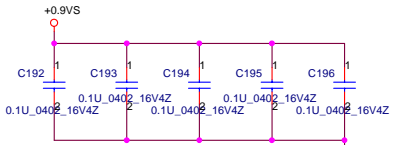
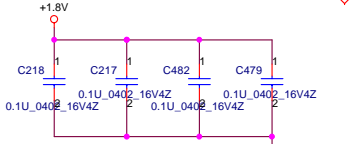
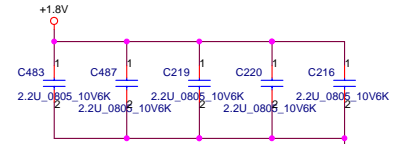
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title Crestline (7/7)-GND	
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				Date:	Thursday, March 08, 2007
				Sheet	13 of 45



# 9/25 Change DIMM1 to SP070006F00



**Layout Note:**  
Place near JP34



**Layout Note:**  
Place these resistor closely JP35, all trace length Max=1.5"

**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

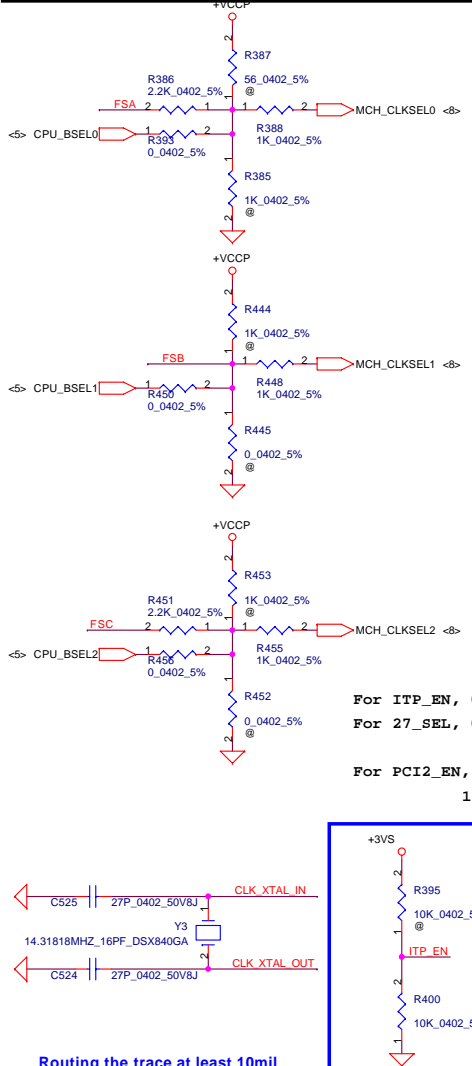
**DIMM1 STD H:9.2mm (BOT)**

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	DDR11-SODIMM1
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Size	Document Number	Rev	Date	
B	LA-3691P	0.2	Thursday, March 06, 2007	
Sheet		15 of 45		

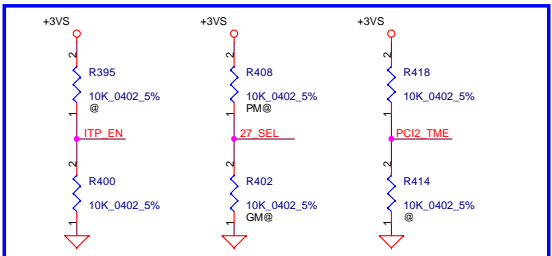
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

**FSB Frequency Selet:**

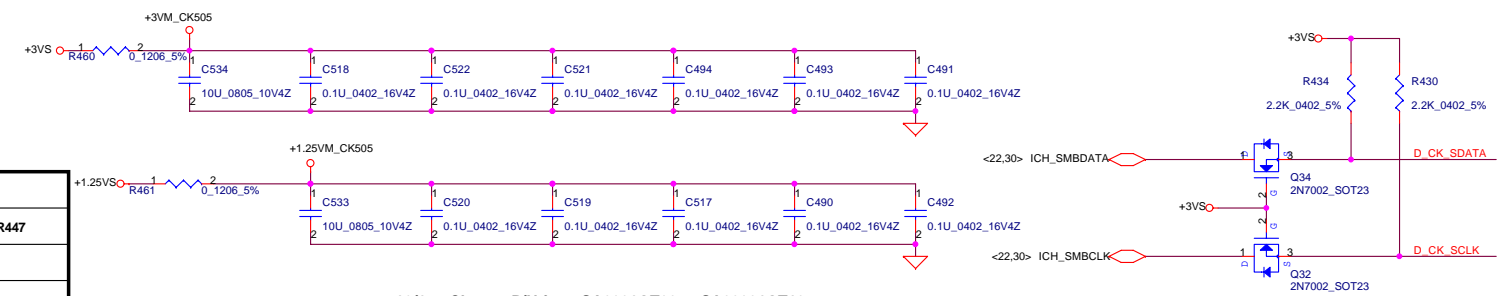
CPU Driven	Stuff	R401	R408	R417	R430	R438	R447
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447
	Stuff	R401	R417	R447			
667MHz	No Stuff	R408	R430	R438			
	Stuff	R408	R417	R447			
800MHz	No Stuff	R401	R430	R438			
	Stuff	R401	R430	R438			



For ITP\_EN, 0 = SRC8/SRC8#, 1 = ITP/ITP#  
 For 27\_SEL, 0 = Enable DOT96 & SRC1, 1 = Enable SRC0 & 27MHz  
 For PCI2\_EN, 0 = Overclocking of CPU and SRC Allowed, 1 = Overclocking of CPU and SRC NOT allowed

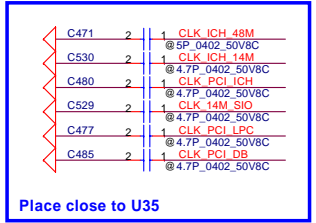
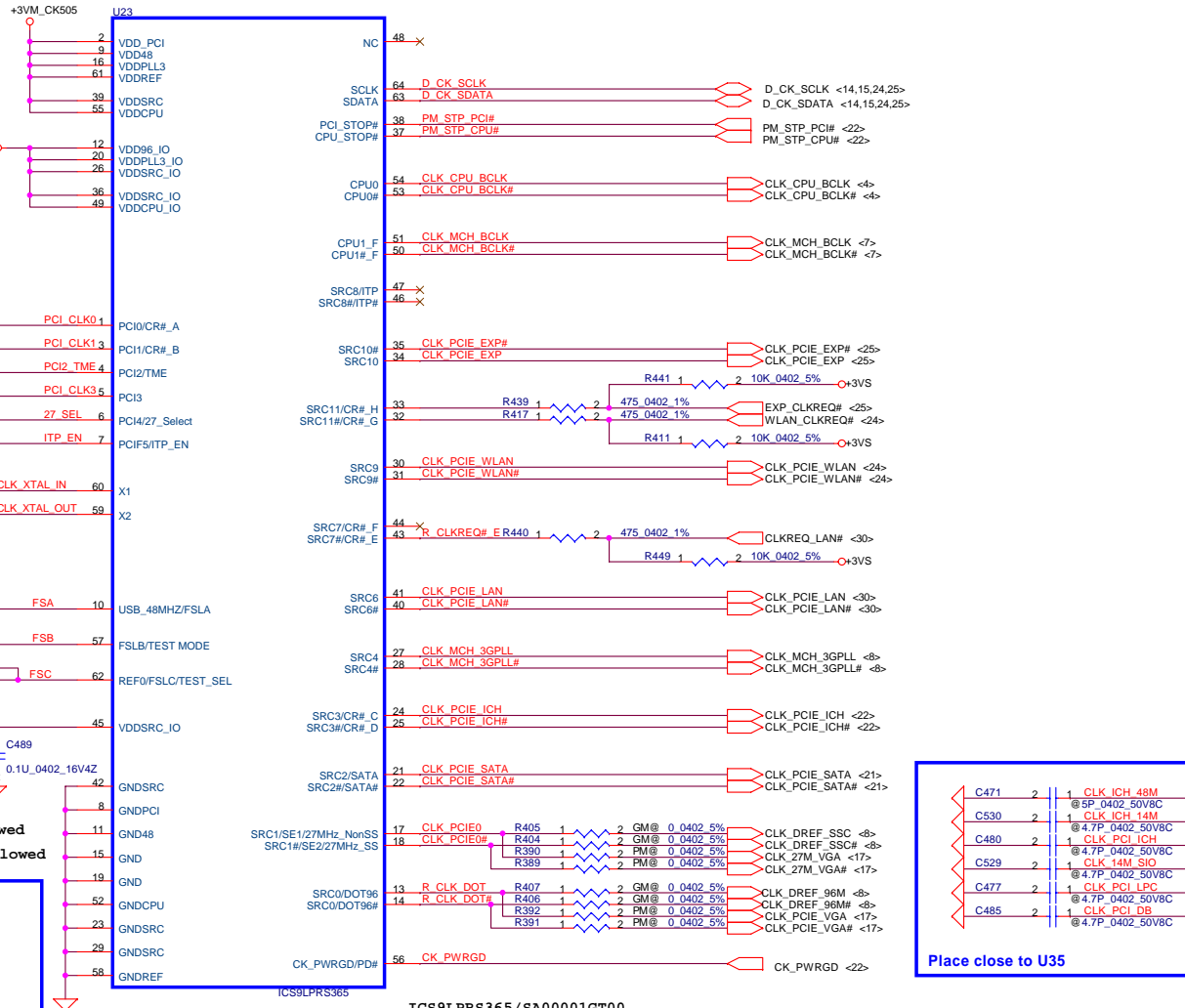


Routing the trace at least 10mil



10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol



Place close to U35

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Issued Date	2006/08/04	Deciphered Date	2006/10/06	<b>Compal Electronics, Inc.</b>
				<b>Clock generator</b>
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				LA-3691P
				Rev
				0.2
				Date
				Thursday, March 08, 2007
				Sheet
				16
				of
				45

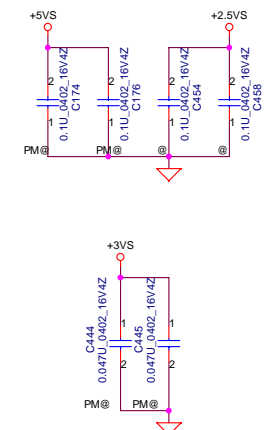
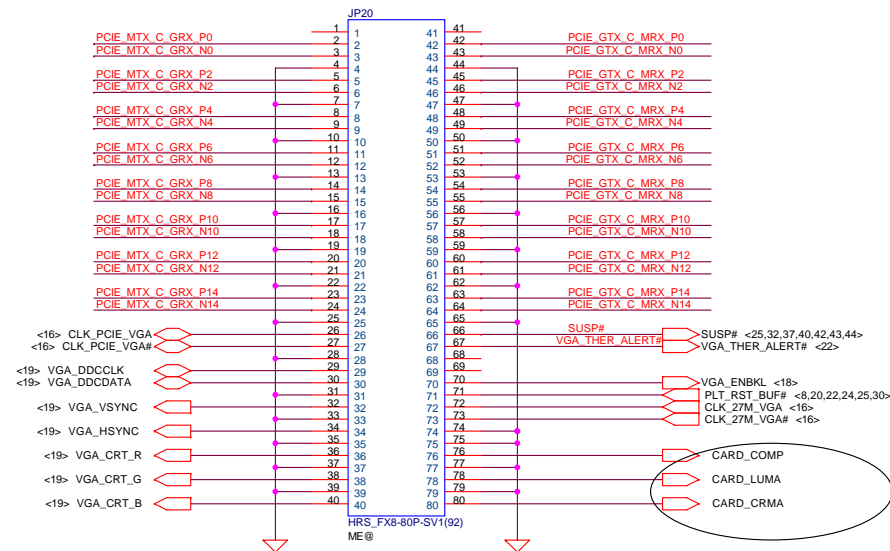
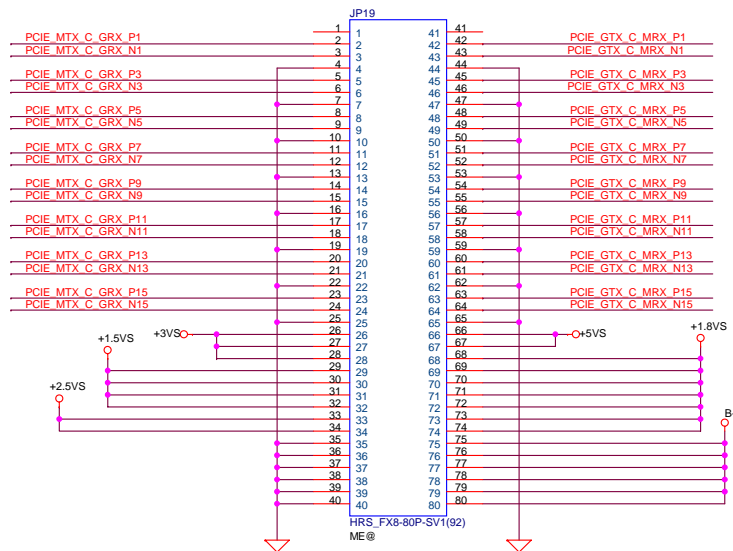


MAX. 4.06A @ 1.8V

MAX. 130mA @ 2.5V

MAX. 655mA @ 3.3V

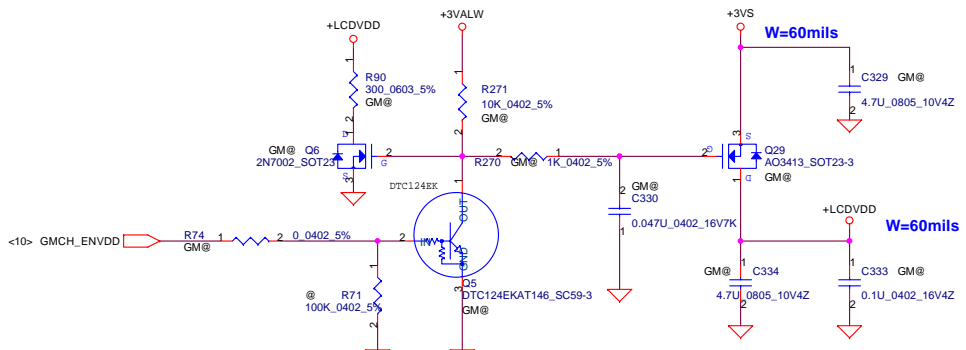
- <10> PCIE\_MTX\_C\_GRX\_N[0..15] PCIE\_MTX\_C\_GRX\_N[0..15]
- <10> PCIE\_MTX\_C\_GRX\_P[0..15] PCIE\_MTX\_C\_GRX\_P[0..15]
- <10> PCIE\_GTX\_C\_MRX\_N[0..15] PCIE\_GTX\_C\_MRX\_N[0..15]
- <10> PCIE\_GTX\_C\_MRX\_P[0..15] PCIE\_GTX\_C\_MRX\_P[0..15]



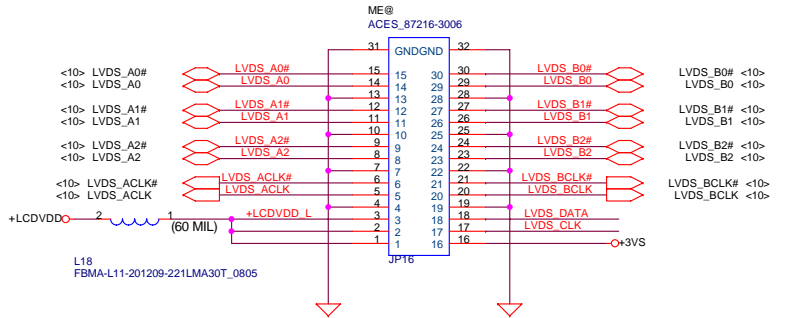
<b>Compal Electronics, Inc.</b>		
<b>VGA/B connector</b>		
Title	Document Number	Rev
	IEL10 LA-3451P	0.2
Date:	Thursday, March 08, 2007	Sheet 17 of 45

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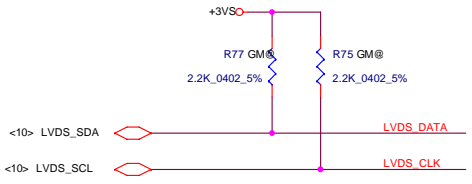
# LCD POWER CIRCUIT



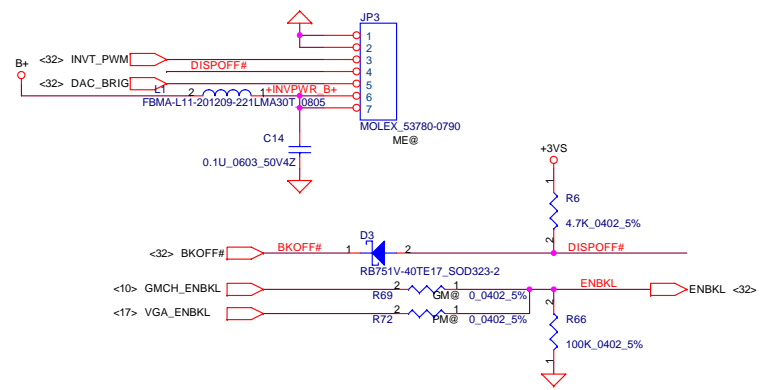
# LCD/PANEL BD. Conn.



Follow HEL80's pin definition  
Except pin 29



# INVERTER Conn.

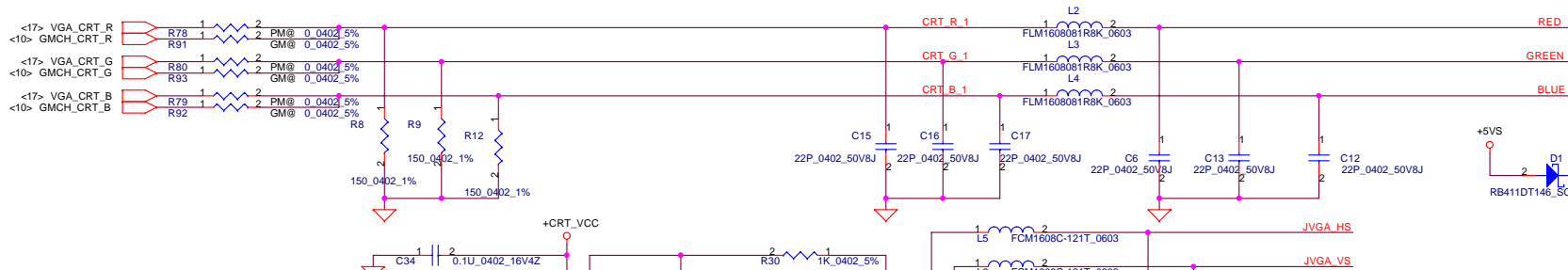


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
				LVDS & DVI Connector		
				Size B	Document Number	Rev
				LA-3691P		0.2
				Date:	Thursday, March 06, 2007	Sheet 18 of 45

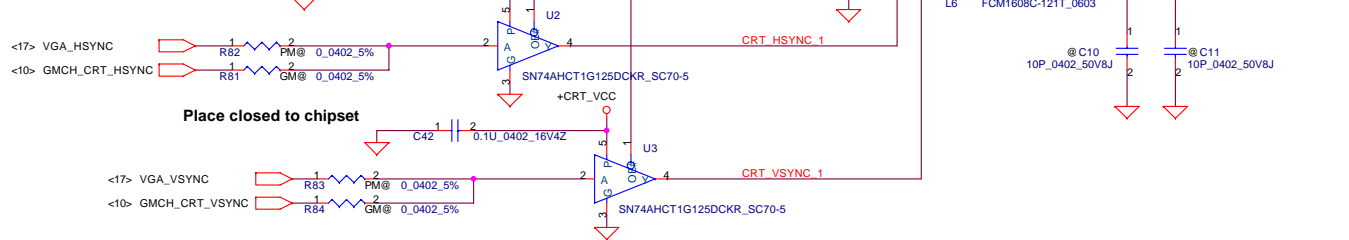
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# CRT Connector

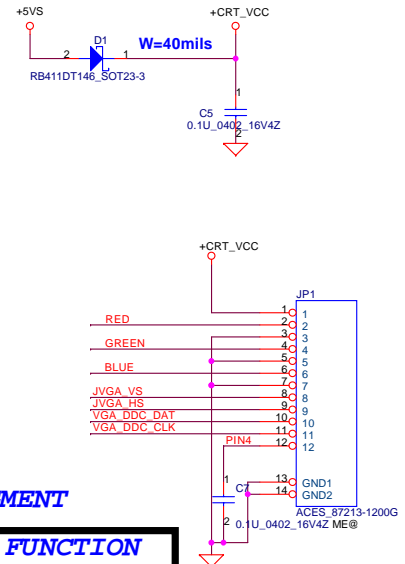
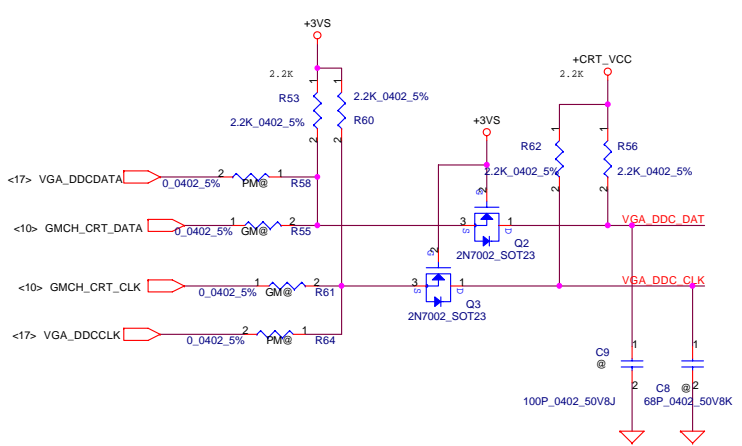
Place closed to chipset



Place closed to chipset



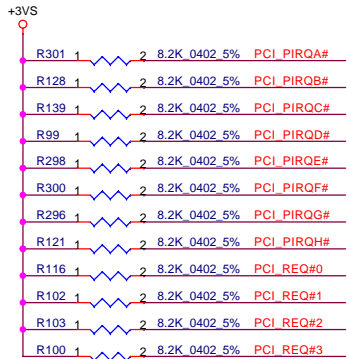
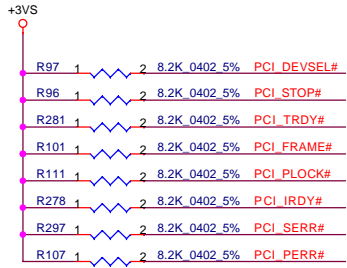
Update Footprint



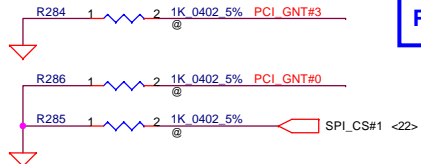
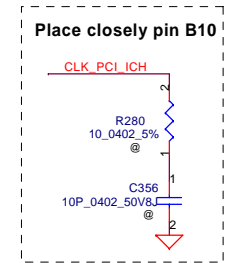
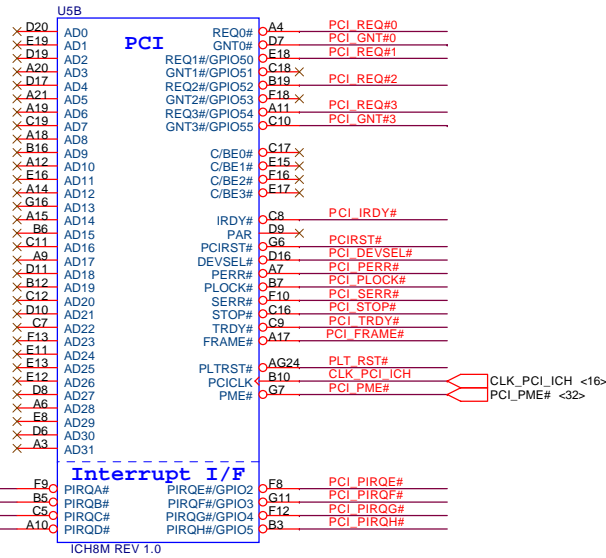
## PIN ASSIGNMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
9	10	GND
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
12	4	PIN4

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				LA-3691P
Date:	Thursday, March 06, 2007	Sheet	19 of 45	Rev
				0.2

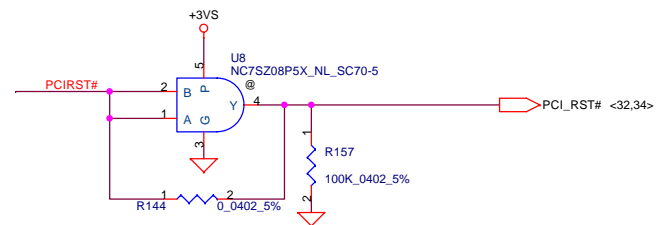
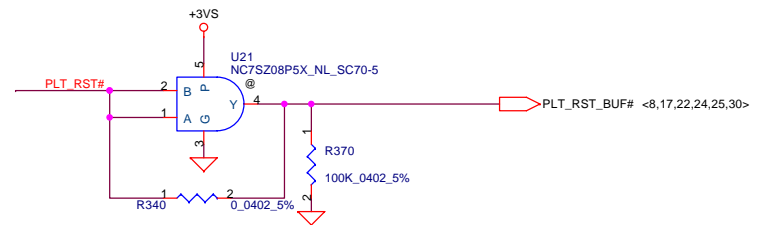


10/17 : Change P/N from SA000010G00 to SA00001JU10  
 10/17 : FootPrint : SA000010G00  
 BOM : SA00001JU10

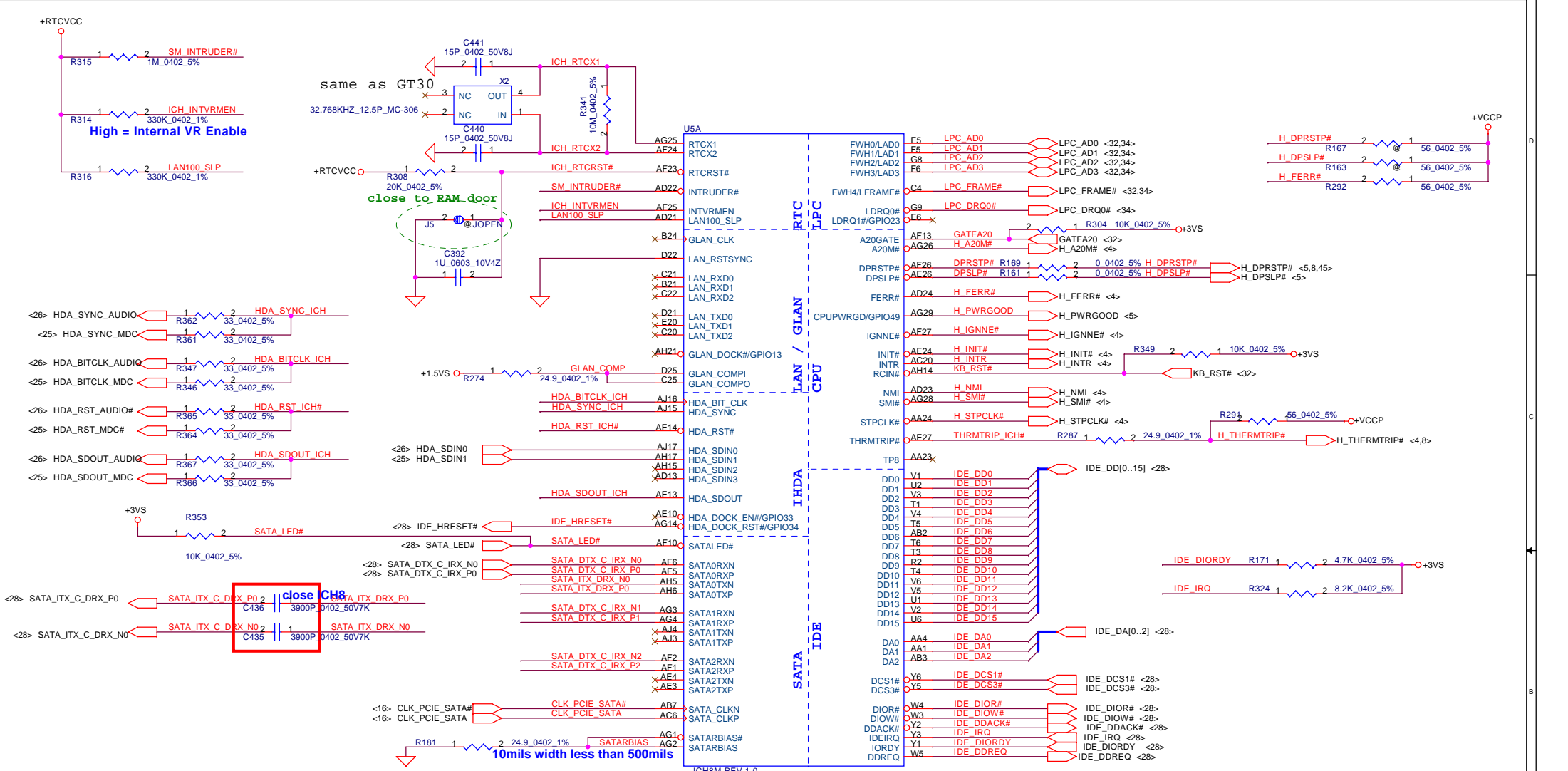


**A16 Swap Override Strap**  
 PCI\_GNT#3 Low= A16 swap override Enable  
 High= Default\*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

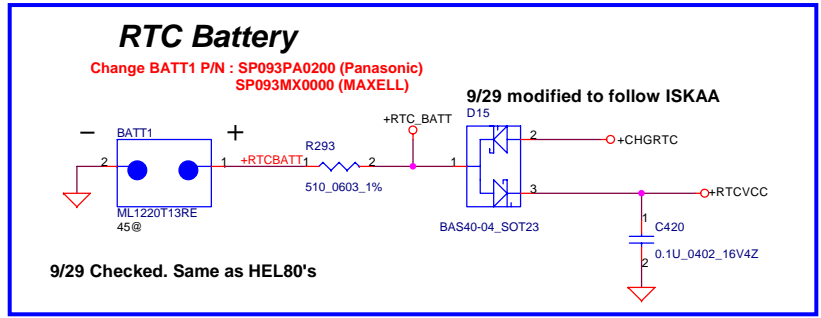


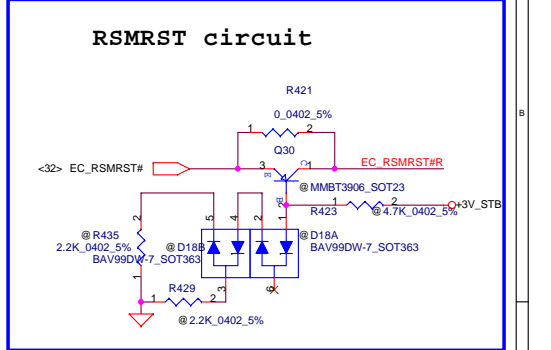
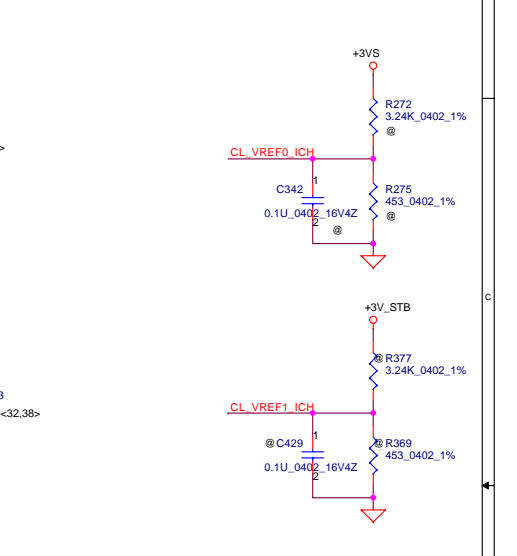
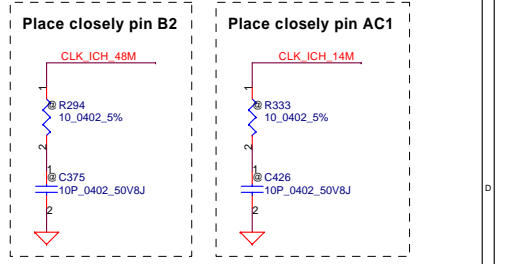
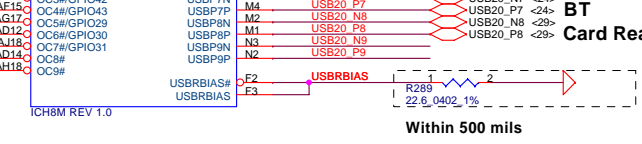
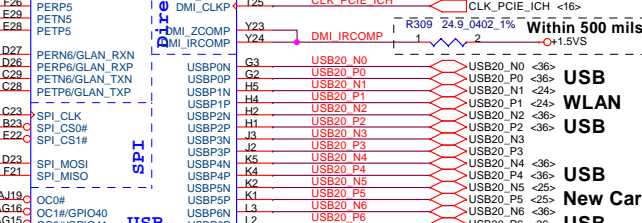
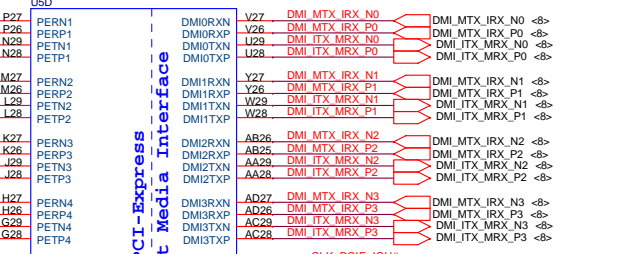
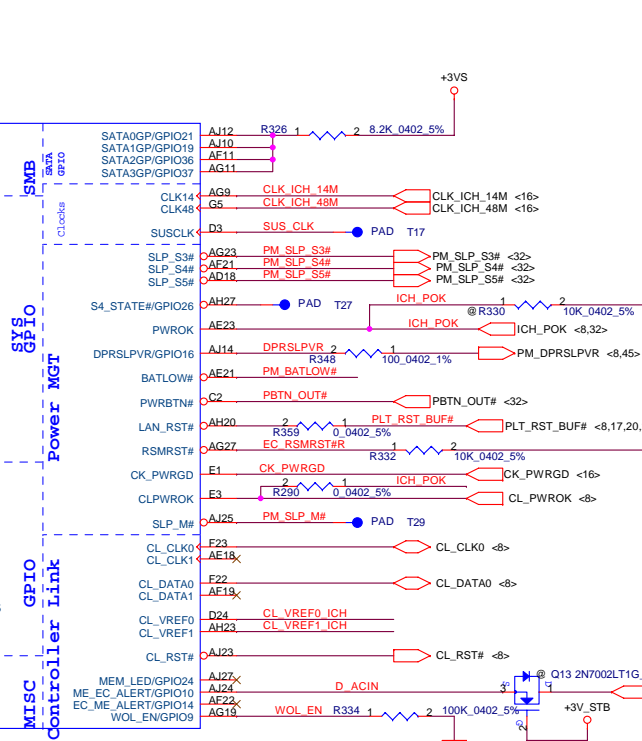
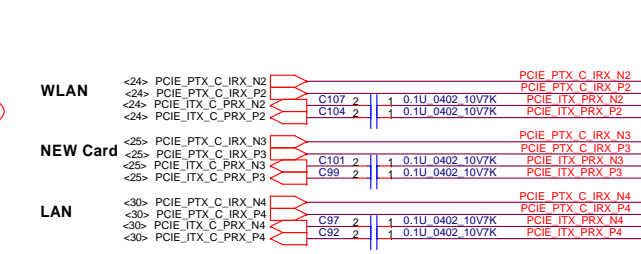
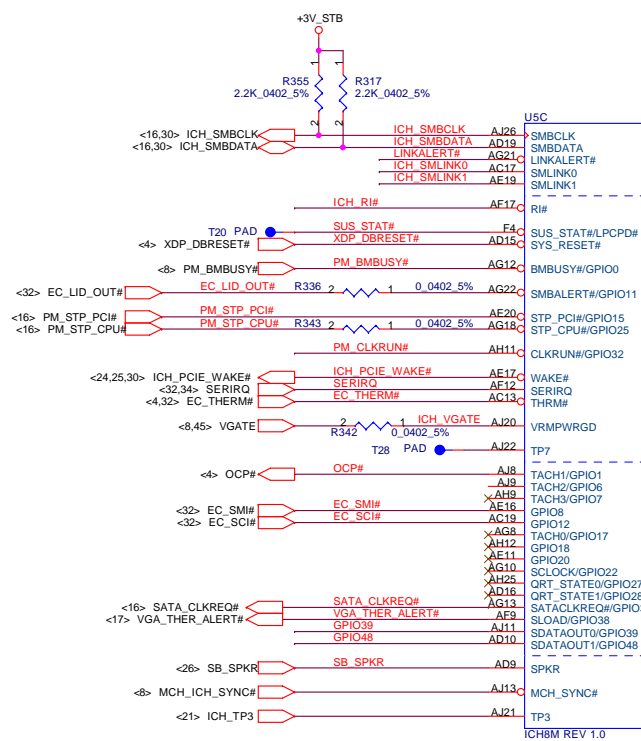
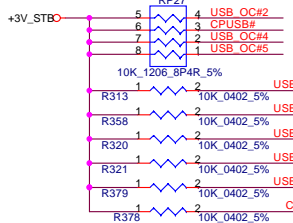
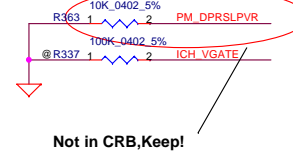
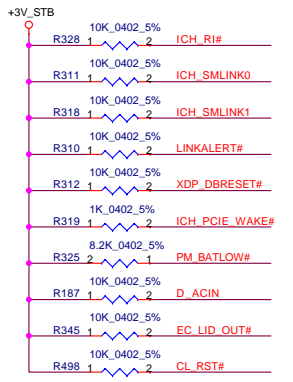
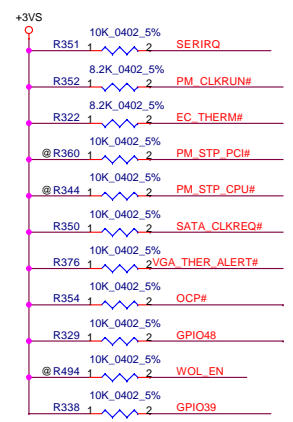
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number			Rev	0.2
LA-3691P		Date: Thursday, March 08, 2007		Sheet	20 of 45



**XOR Chain Entrance Strap**

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

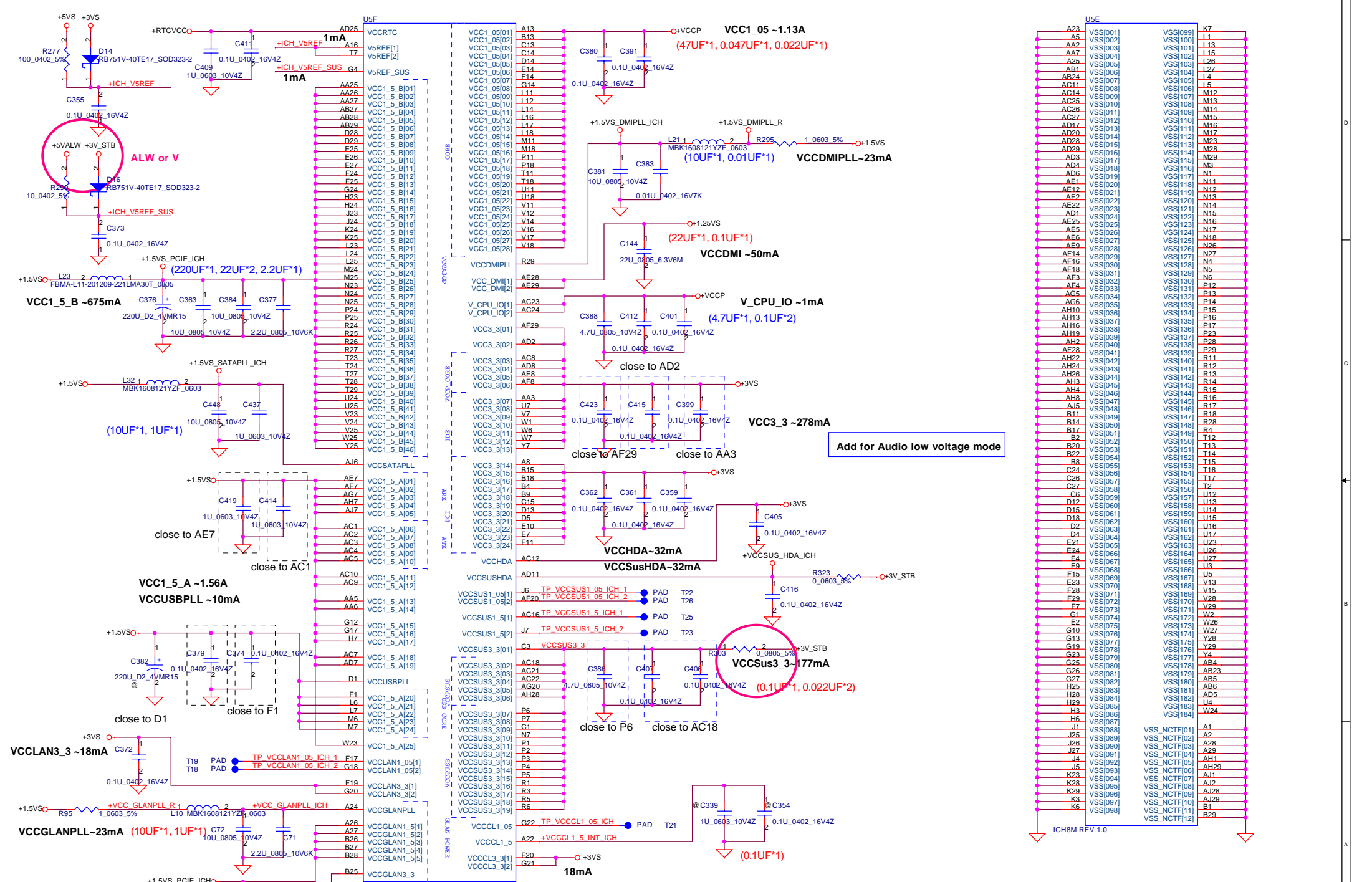




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Issued Date	2006/08/18	Deciphered Date
		2007/8/18

Compal Electronics, Inc.		
Title	ICH8M(3/4)-USB,GPIO,PCIE	
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Customer	LA-3691P	0.2
Date	Thursday, March 08, 2007	Sheet 22 of 45

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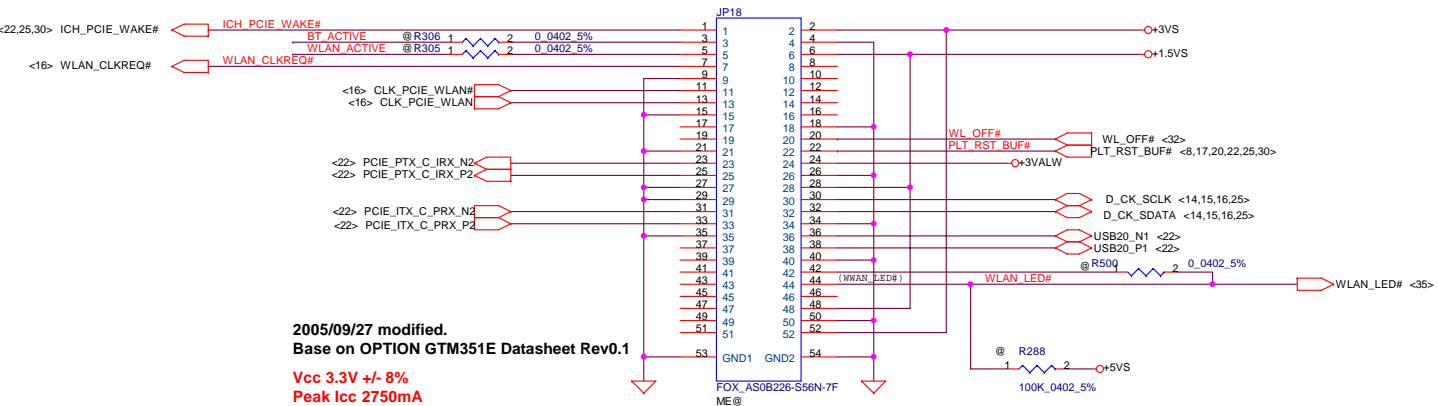
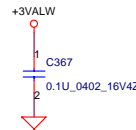
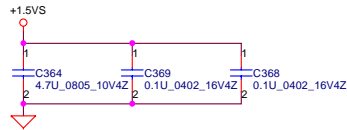
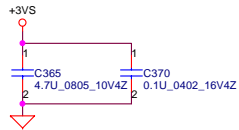


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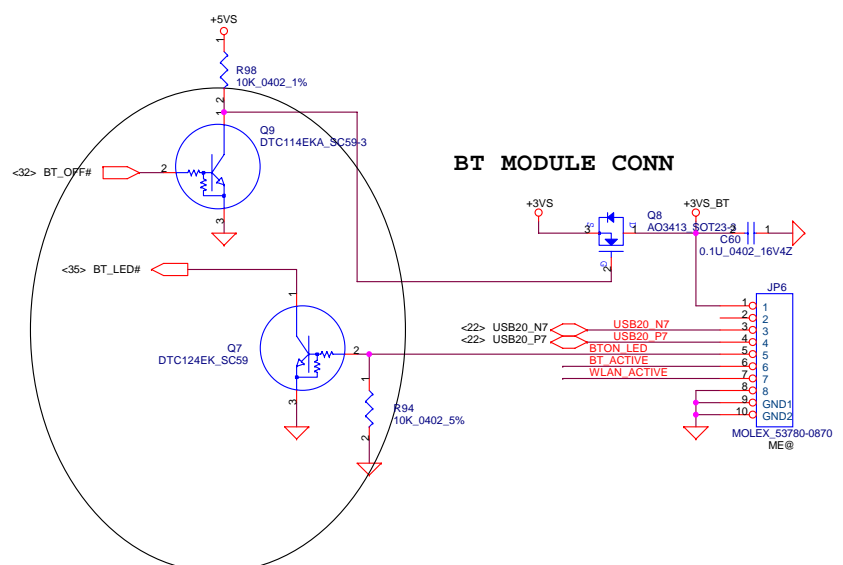
Compal Electronics, Inc.			
Title	IFTXX MB LA-3541P Schematic		
Size	Document Number	Rev	0.2
Customer	LA-3691P		
Date:	Thursday, March 08, 2007	Sheet	23 of 45

# Mini-Express Card for 3G Or TV Tuner

## Mini-Express Card for WLAN



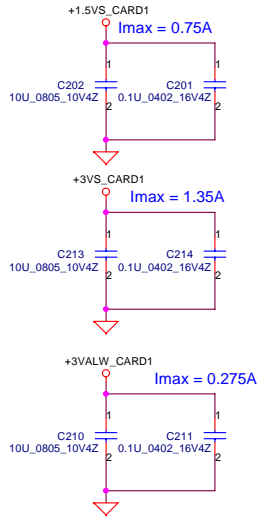
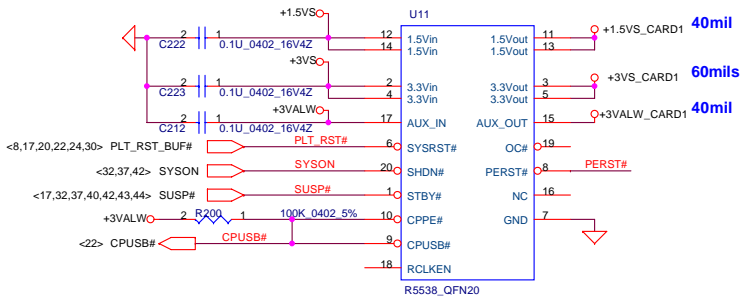
2005/09/27 modified.  
 Base on OPTION GTM351E Datasheet Rev0.1  
**Vcc 3.3V +/- 8%**  
**Peak Icc 2750mA**  
**with max supply droop 50mA**  
**Average Icc 1000mA**



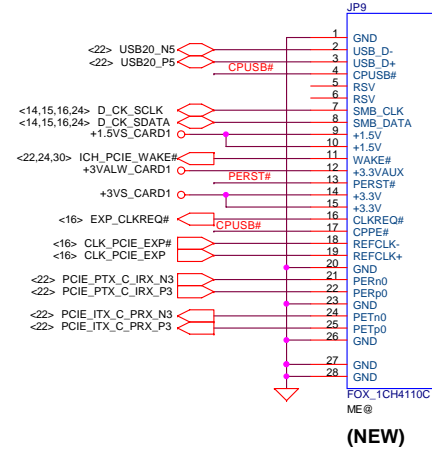
Security Classification	Compal Secret Data			Title		
Issued Date	2006/08/05	Deciphered Date	2007/08/05	<b>Compal Electronics, Inc.</b> <b>Mini-Card/3G/FeliCa/FP</b>		
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					LA-3691P	0.2
				Date:	Thursday, March 08, 2007	Sheet 24 of 45



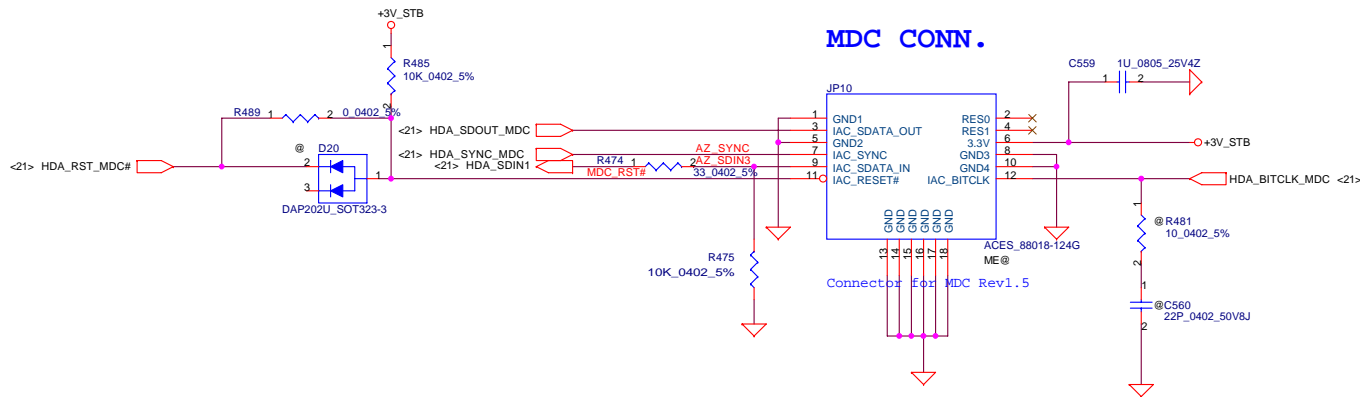
### Express Card Power Switch



### New Card Socket (Left/TOP)



### MDC CONN.



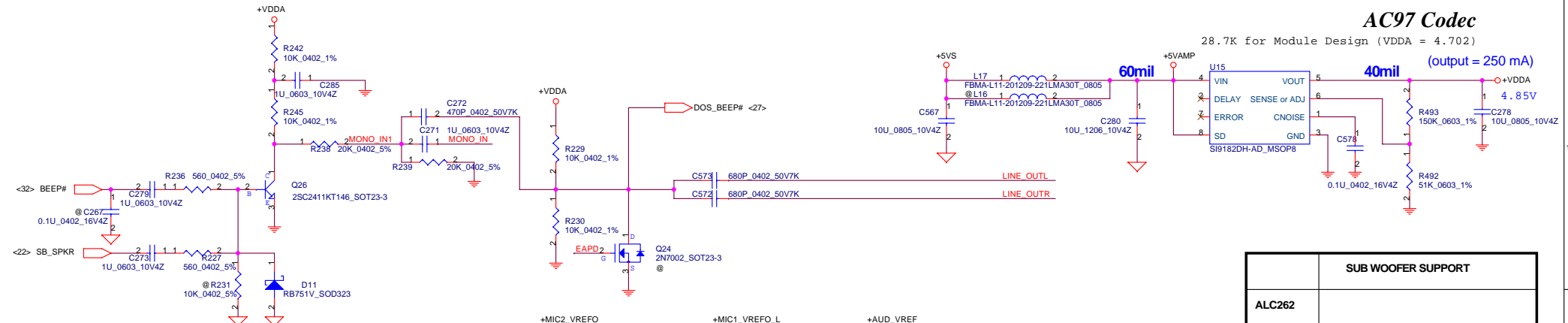
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
				NEW CARD & USB Connector		
Size	Document Number	Rev				
B	LA-3691P	0.2				
Date:	Thursday, March 06, 2007	Sheet	25 of 45			

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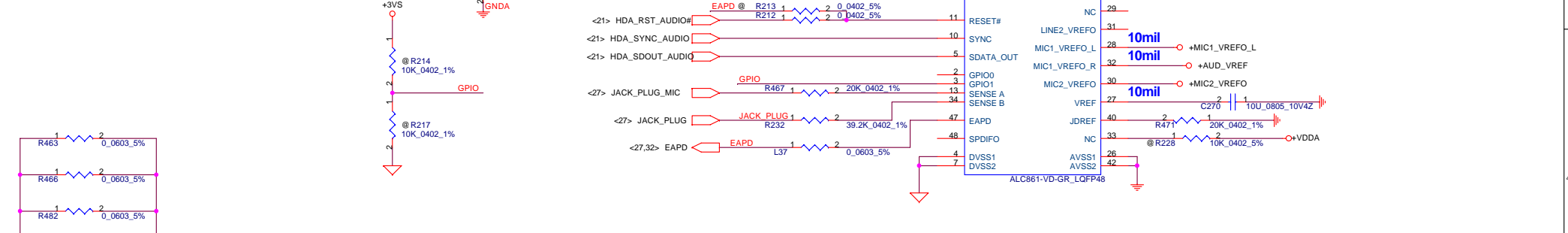
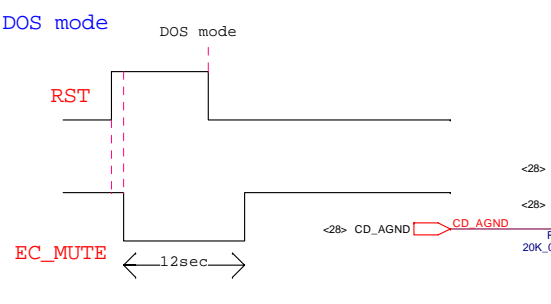
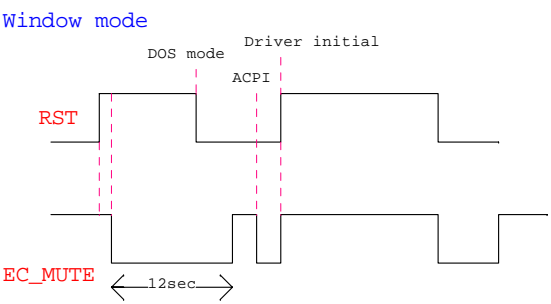
# AC97 Codec

28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)



SUB WOOFER SUPPORT	
ALC262	
ALC861D	

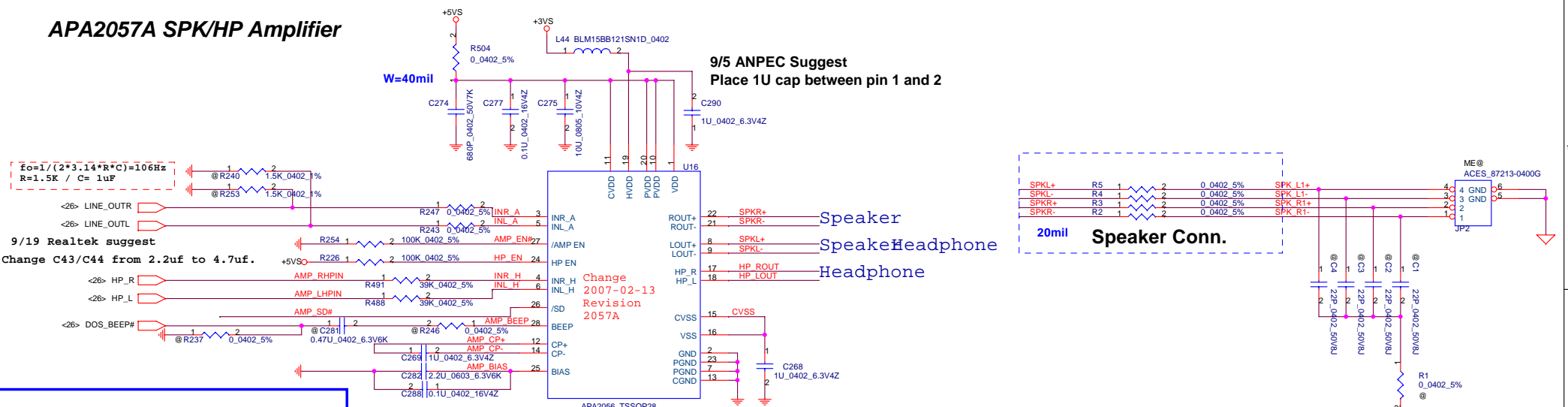


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Issued Date	2006/08/04	Deciphered Date
		2006/10/06

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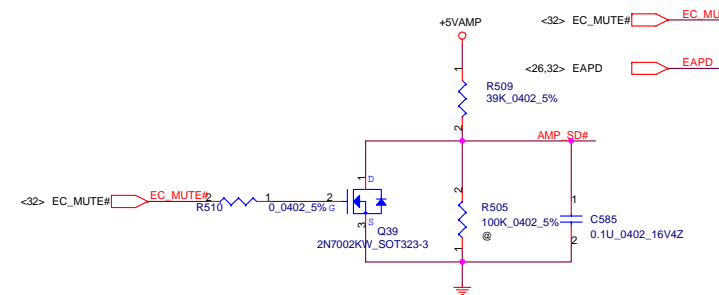
Compal Electronics, Inc.		
Title <b>ALC861D VD Codec</b>		
Size	Document Number	Rev
Custom	<b>IEL10 LA-3451P</b>	0.2
Date:	Thursday, March 08, 2007	Sheet 26 of 45

# APA2057A SPK/HP Amplifier

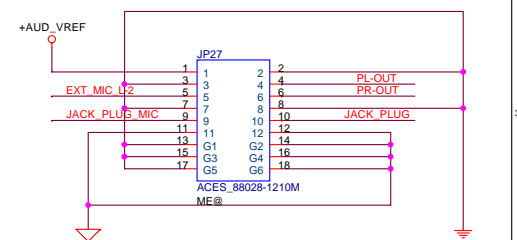
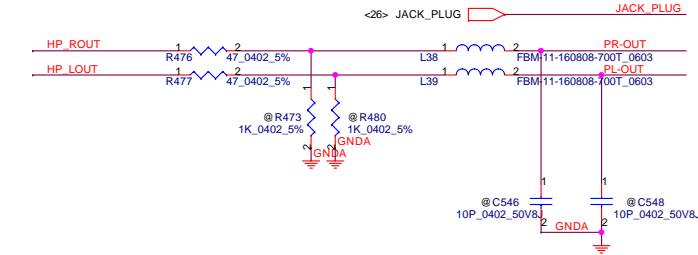
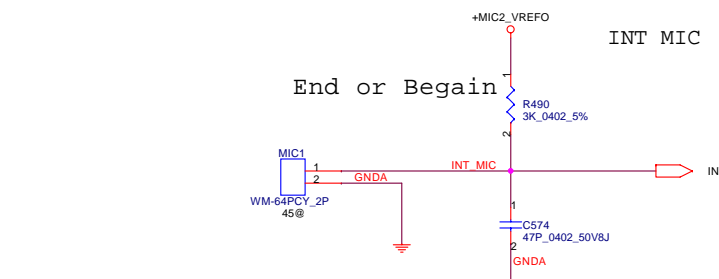
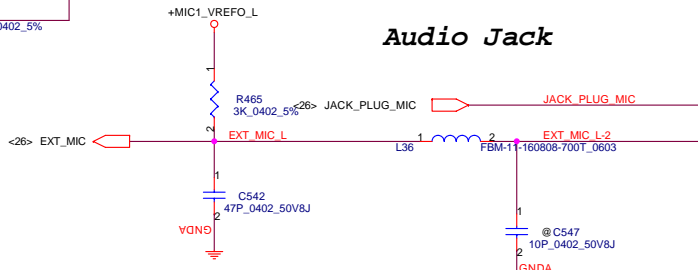


**9/5 If implement AMP BEEP, Swap C155 and R79. R79 change from 0 Ohm to 47K**

**IN\_A Gain = 10dB (Internal Speaker)  
IN\_H Gain = 0dB (Headphone)**



## EXT MIC Audio Jack

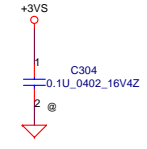
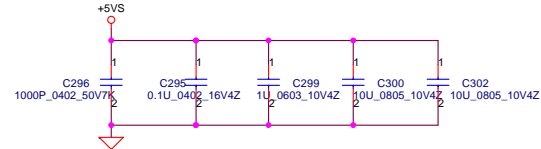
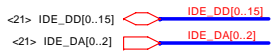
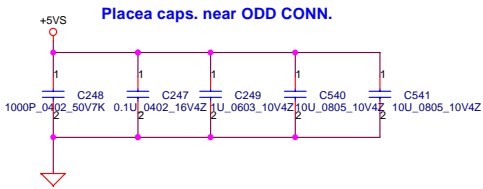


Security Classification	Compal Secret Data	
Issued Date	2006/08/05	Deciphered Date
		2007/08/05

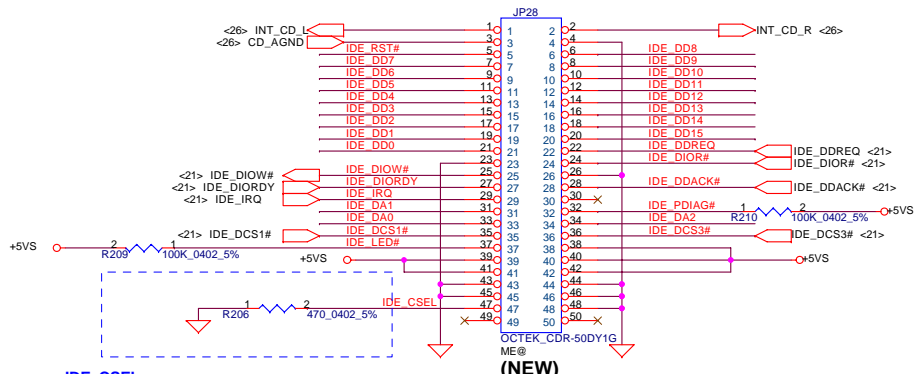
Title		Compal Electronics, Inc.	
		AMP/V/R/Audio Jack/MIC	

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Size	Document Number	Rev
Custom	LA-3691P	0.2
Date:	Thursday, March 08, 2007	Sheet 27 of 45

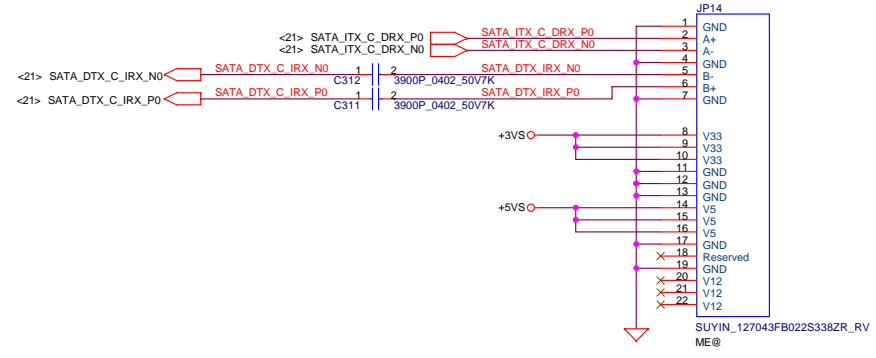


**SATA HDD Conn.**

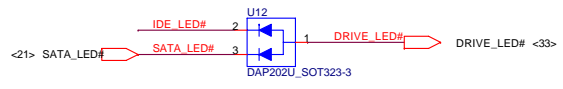
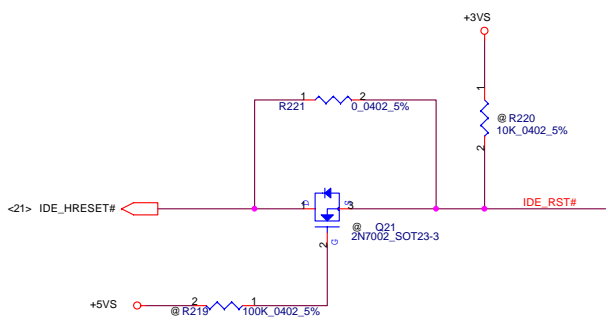


**IDE\_CSEL**  
 Grounding for Master (When use SATA HDD)  
 Open or High for Slaver (Normal)

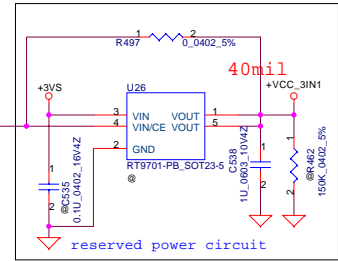
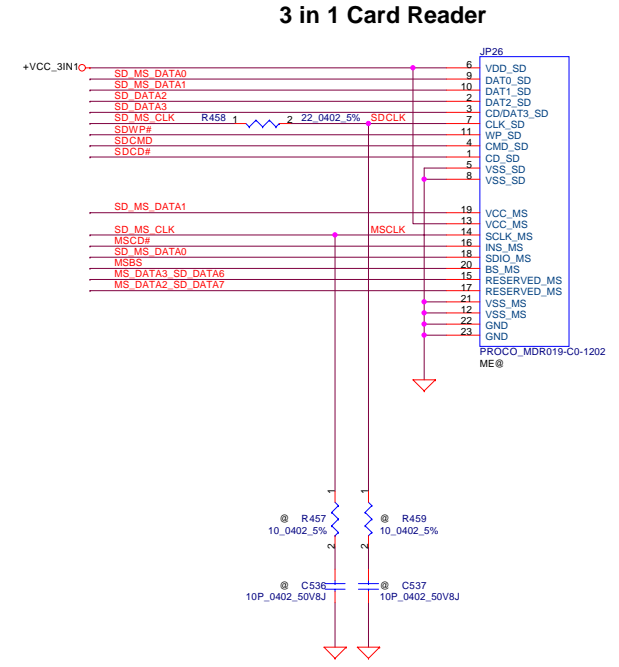
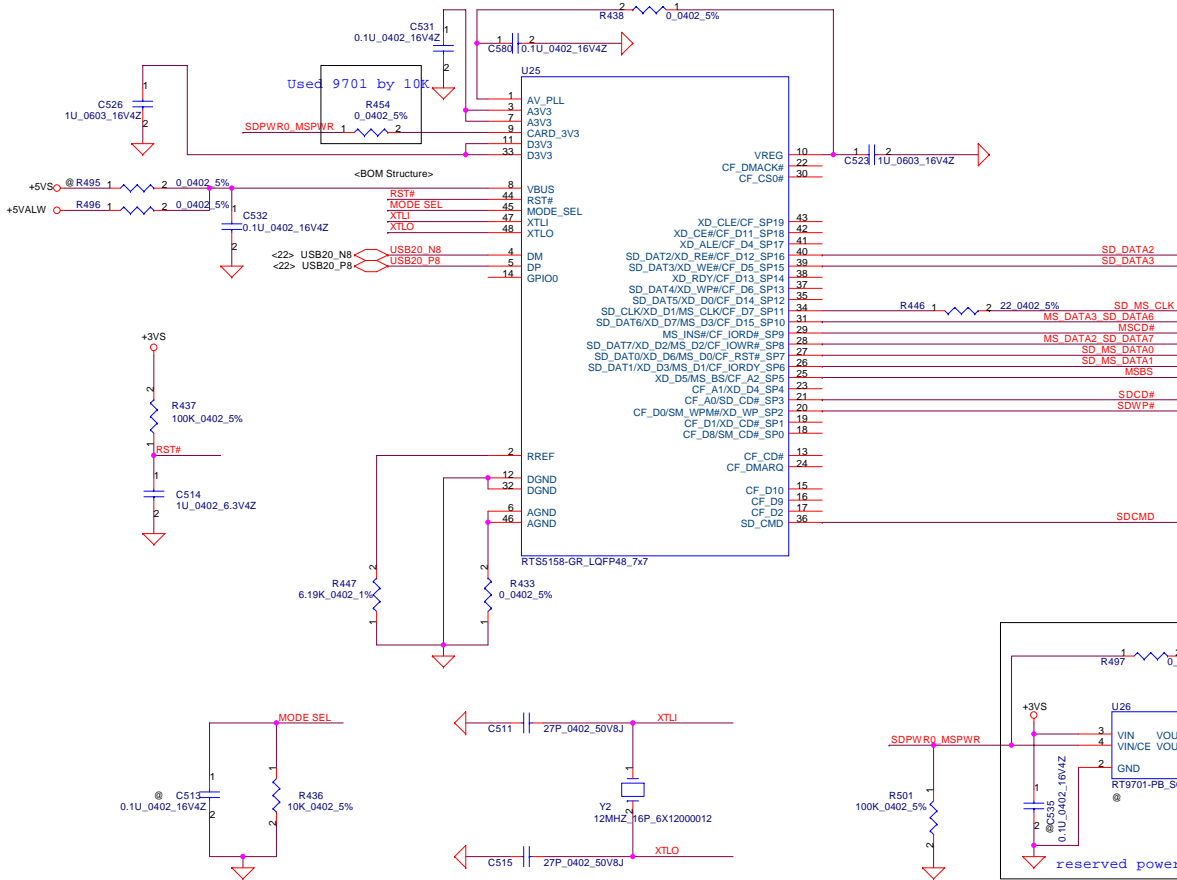
**(NEW)**



**(NEW)**  
 Change Library

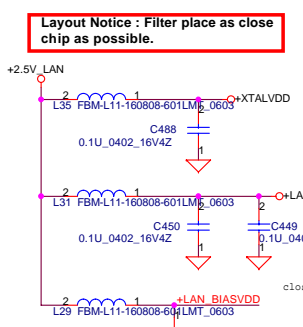


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	HDD & ODD Connector	
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Date:	Thursday, March 06, 2007	Sheet	28	of	45

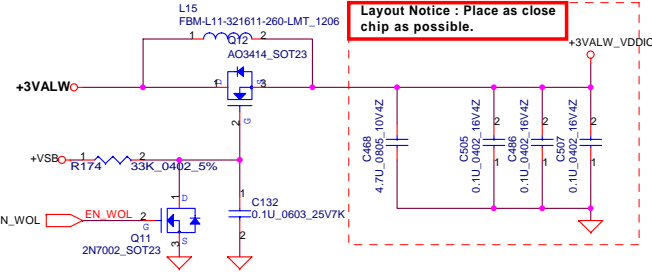


Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	<b>1394+3 in 1 Card</b>
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Date: Thursday, March 08, 2007				Sheet 29 of 45

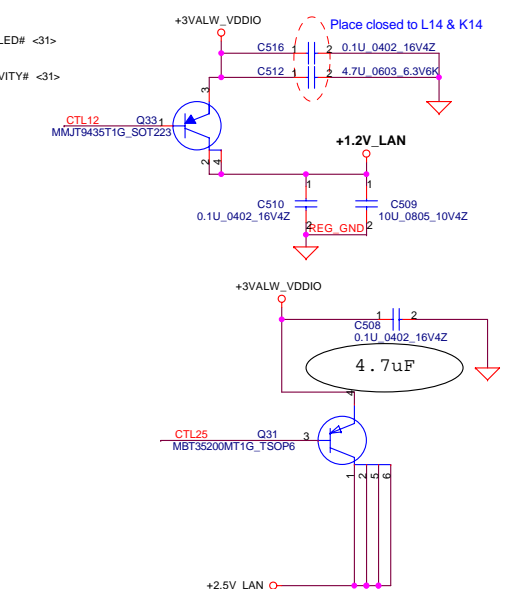
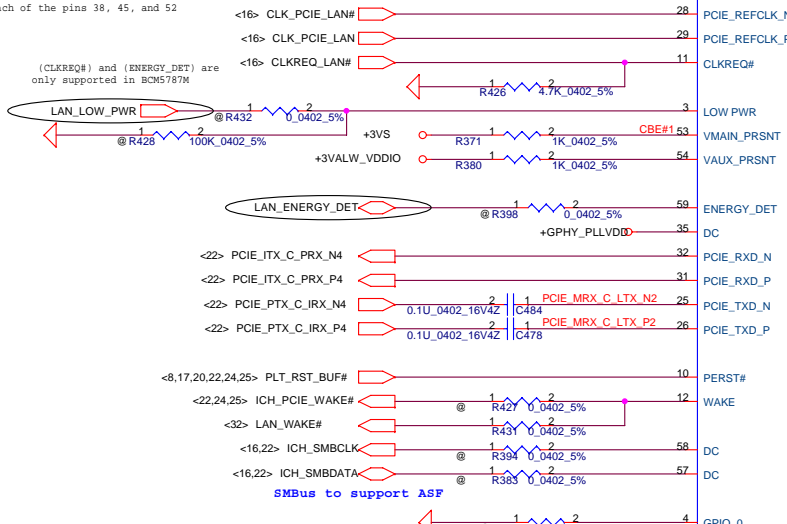
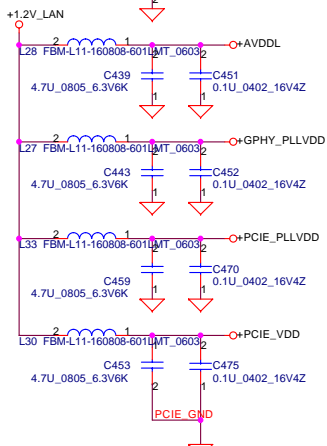
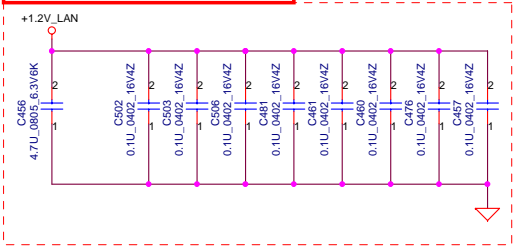
**Layout Notice : Filter place as close chip as possible.**



**Layout Notice : Place as close chip as possible.**



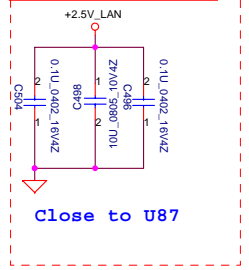
**Layout Notice : 1.2V filter. Place as close chip as possible.**



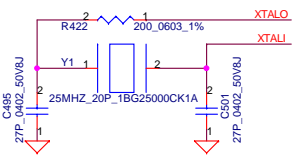
**Notice : 4.7u 6.3V capacitor Thickness 1.25mm**

**Layout Notice : Filter place as close chip as possible.**

**Layout Notice : Place as close chip as possible.**

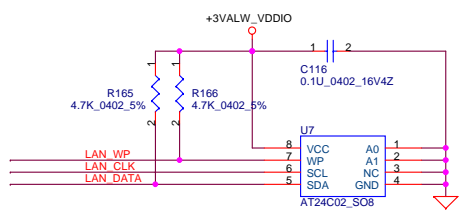


**Close to U87**



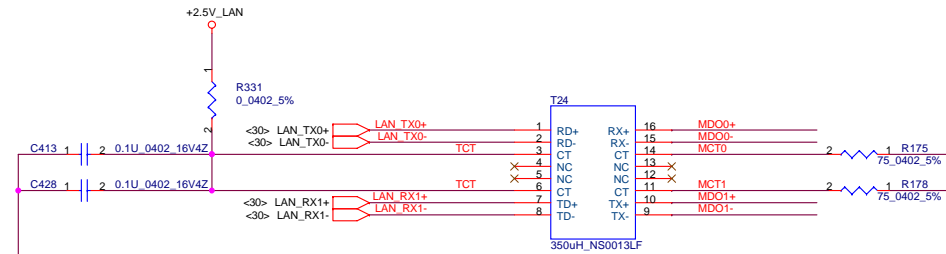
Pin16 connect to C1206 Pin1

Pin 24 connect to C1339 Pin1

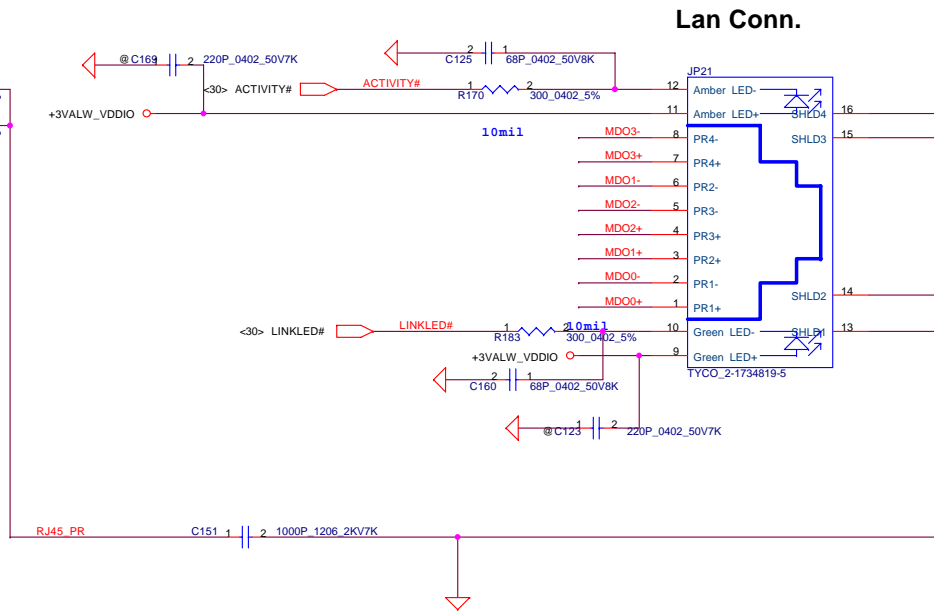
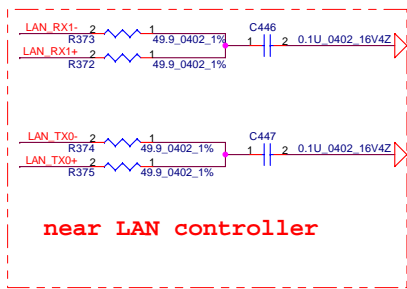


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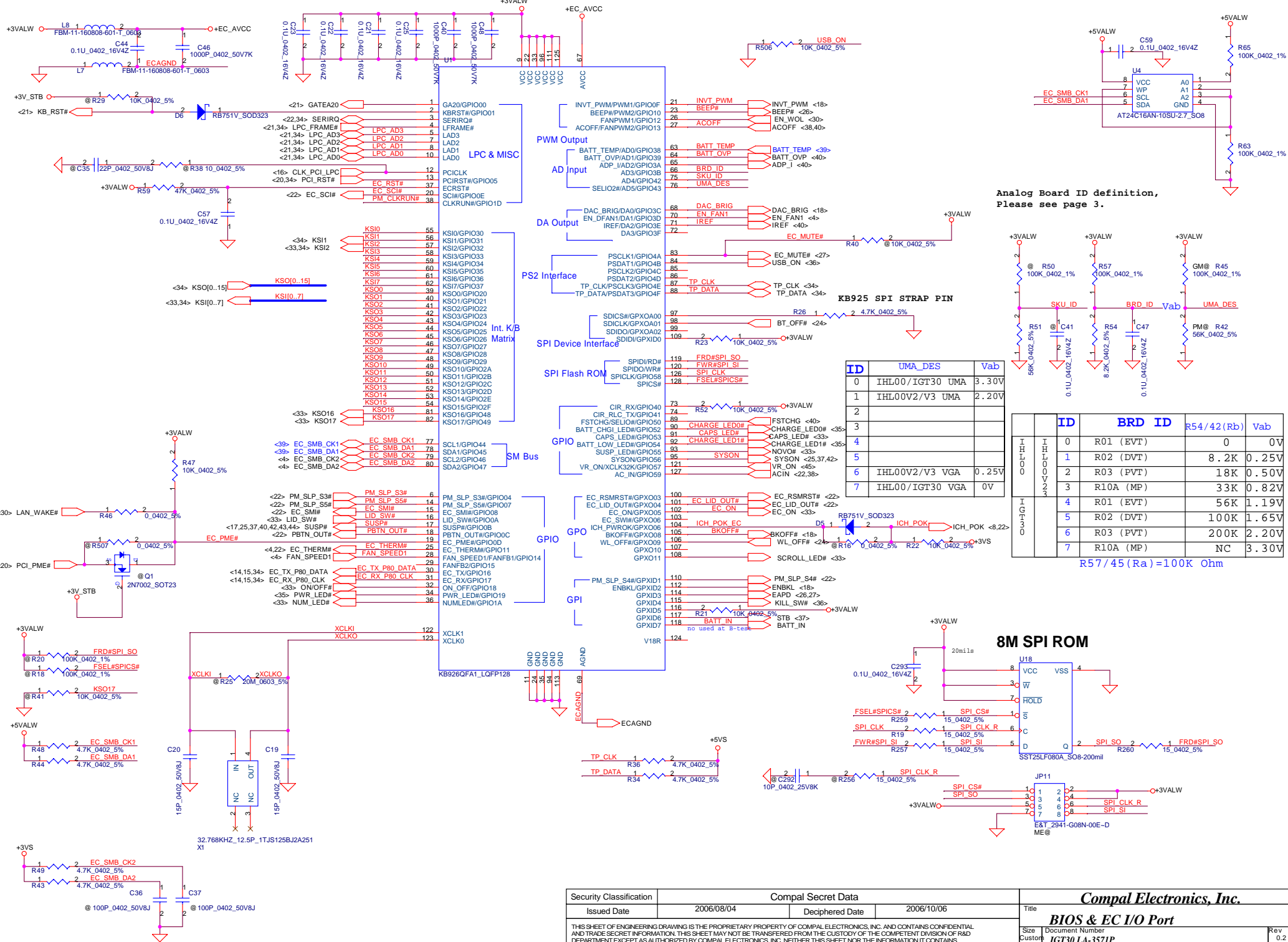
Compal Electronics, Inc.		
Title		
BCM5787M-GLAN		
Size	Document Number	Rev
	IEL20 LA-3471P	0.2
Date:	Thursday, March 08, 2007	Sheet 30 of 45



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



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Date:	Thursday, March 08, 2007	Sheet	31	of	45	



Analog Board ID definition, Please see page 3.

ID	UMA_DES	Vab
0	IHL00/IGT30 UMA	3.30V
1	IHL00V2/V3 UMA	2.20V
2		
3		
4		
5		
6	IHL00V2/V3 VGA	0.25V
7	IHL00/IGT30 VGA	0V

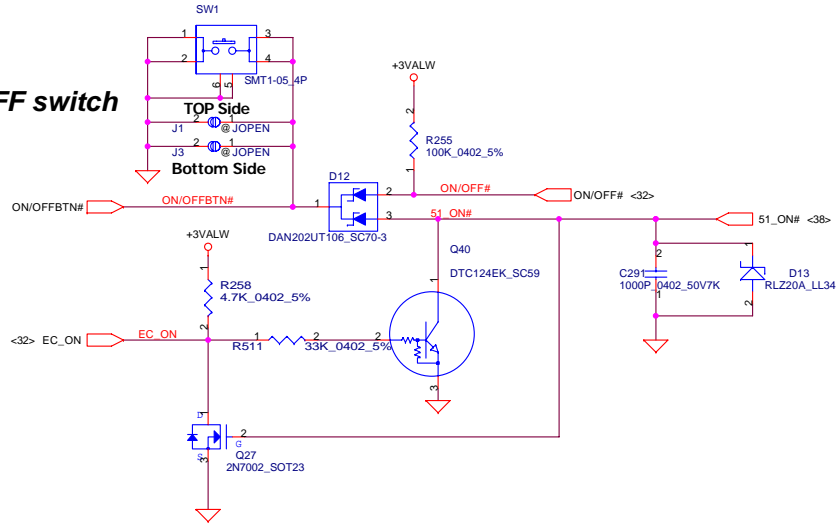
ID	BRD ID	R54/42(Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03 (PVT)	18K	0.50V
3	R10A (MP)	33K	0.82V
4	R01 (EVT)	56K	1.19V
5	R02 (DVT)	100K	1.65V
6	R03 (PVT)	200K	2.20V
7	R10A (MP)	NC	3.30V

R57/45 (Ra) = 100K Ohm

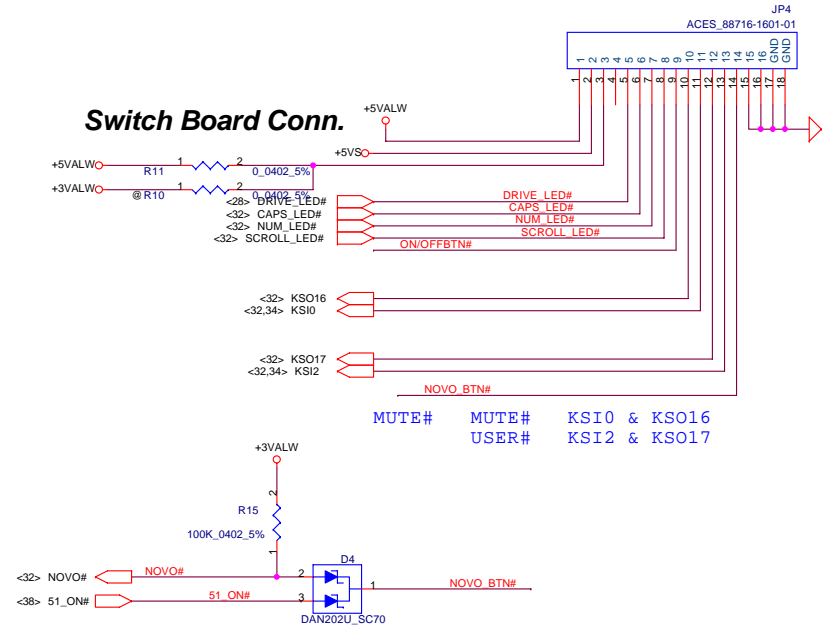


### Power Button

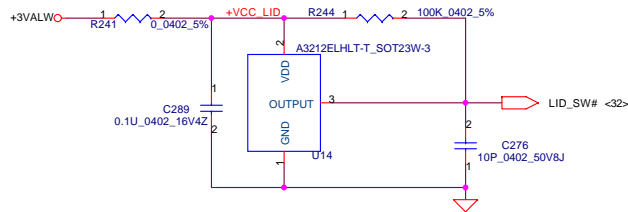
#### ON/OFF switch



#### Switch Board Conn.

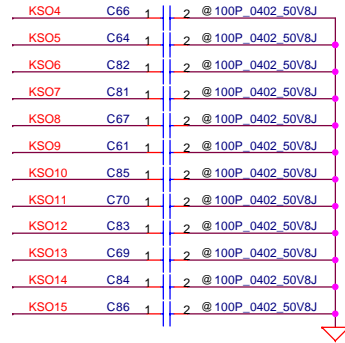
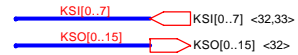


### Lid Switch

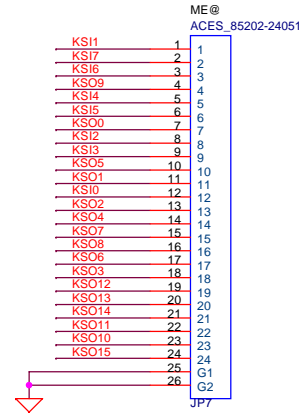


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Size	Document Number	Rev		
B	LA-3691P	0.2		
Date:	Thursday, March 08, 2007	Sheet	33	of 45

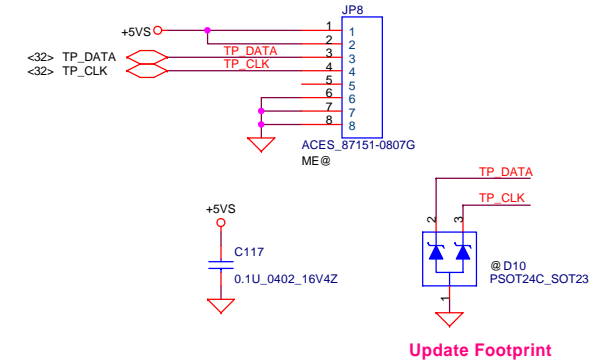
# INT\_KBD Conn.



## For IHL00

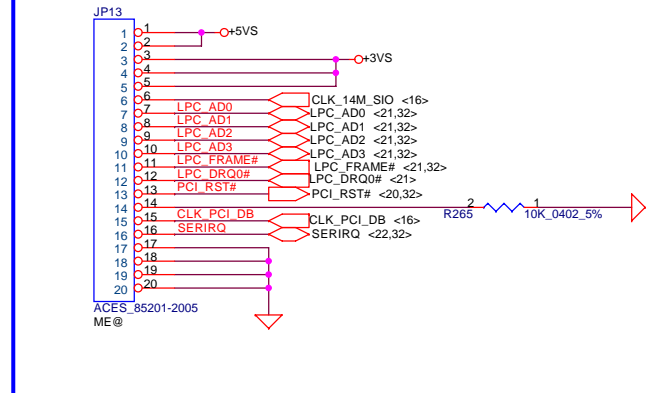


## To TP/B Conn.

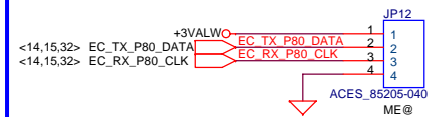


Update Footprint

## FOR LPC SIO DEBUG PORT

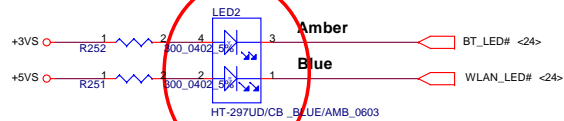
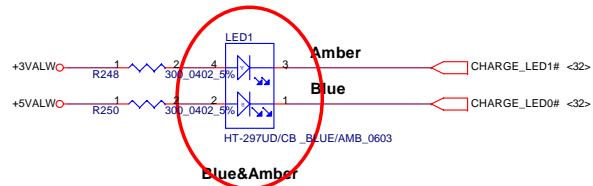
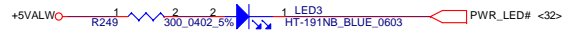


## EC DEBUG PORT



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Size	Document Number			Rev	
B	LA-3691P			0.2	
Date:	Thursday, March 08, 2007			Sheet	34 of 45

# LED

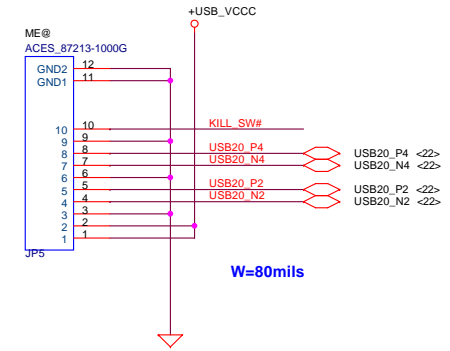
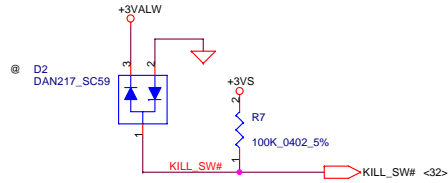


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
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				Size	Document Number	Rev
				B	LA-3691P	0.2
				Date:	Thursday, March 08, 2007	Sheet 35 of 45

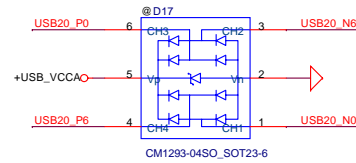
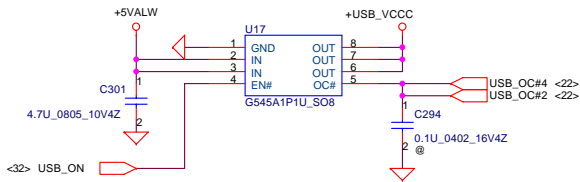
# USB Conn.

W=80mils

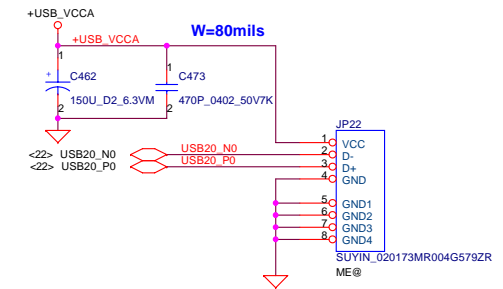
## Kill SWITCH



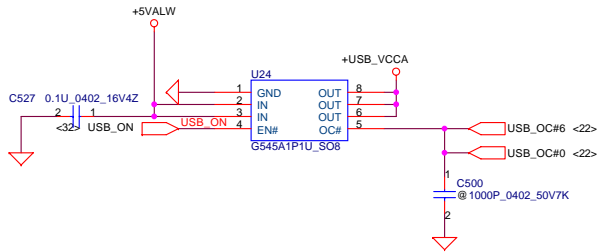
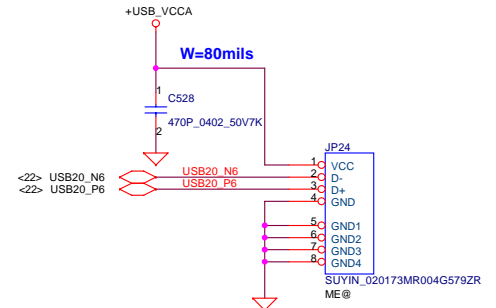
W=80mils



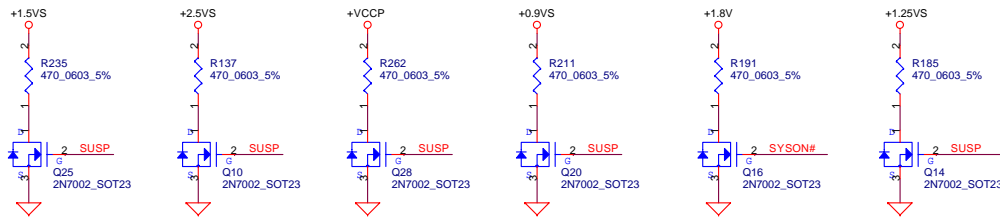
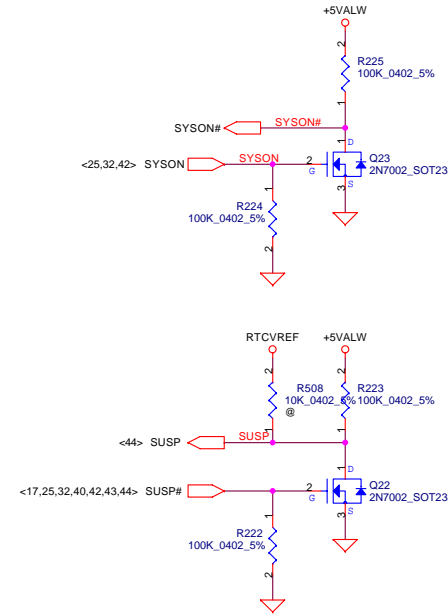
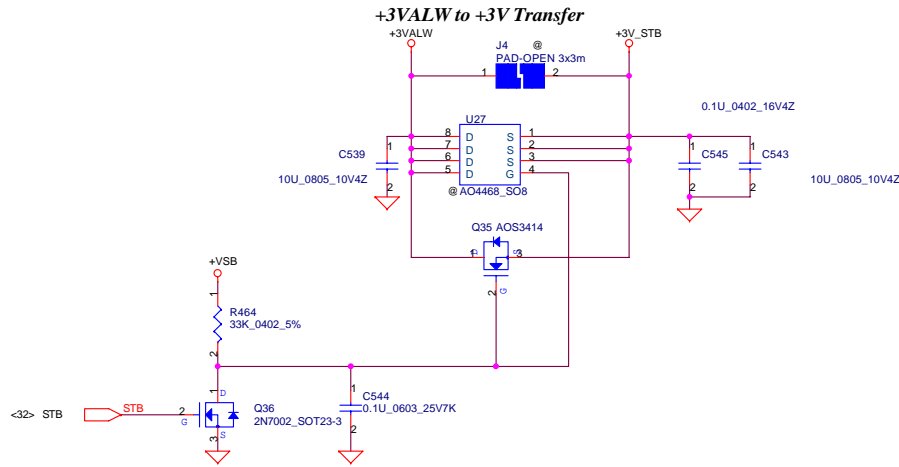
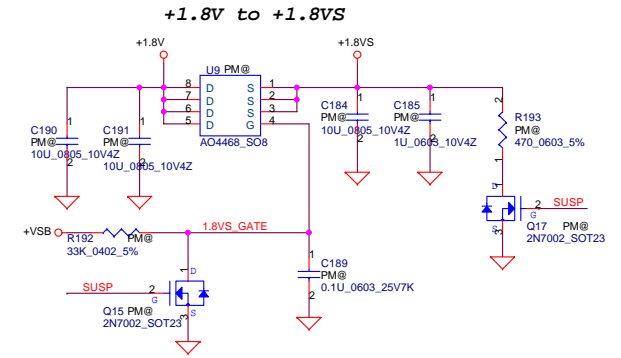
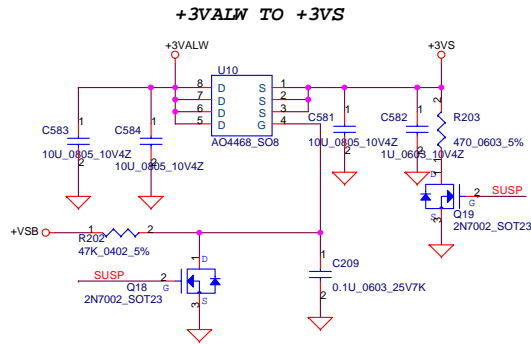
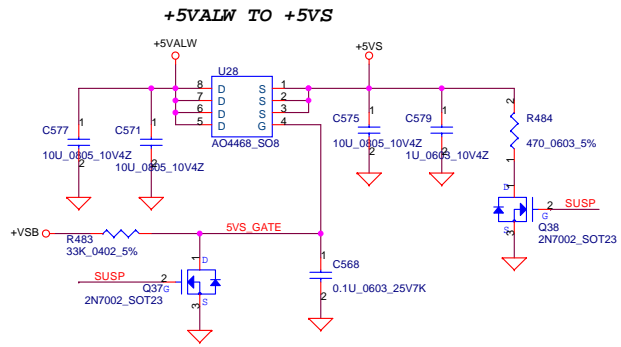
## USB CONN. 1



## USB CONN. 2

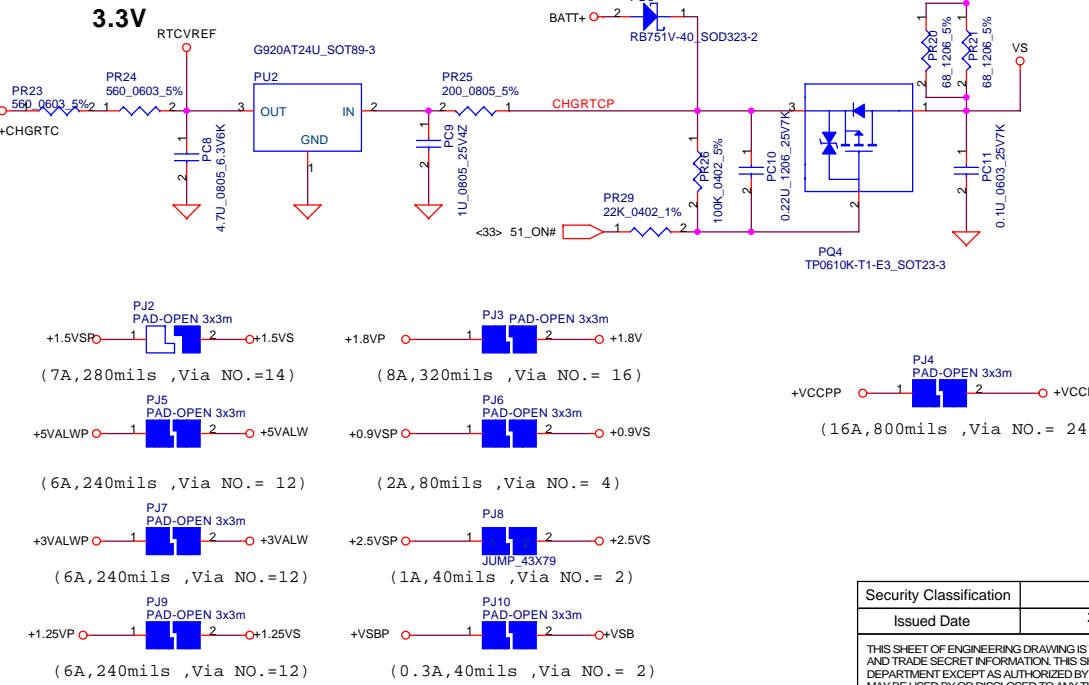
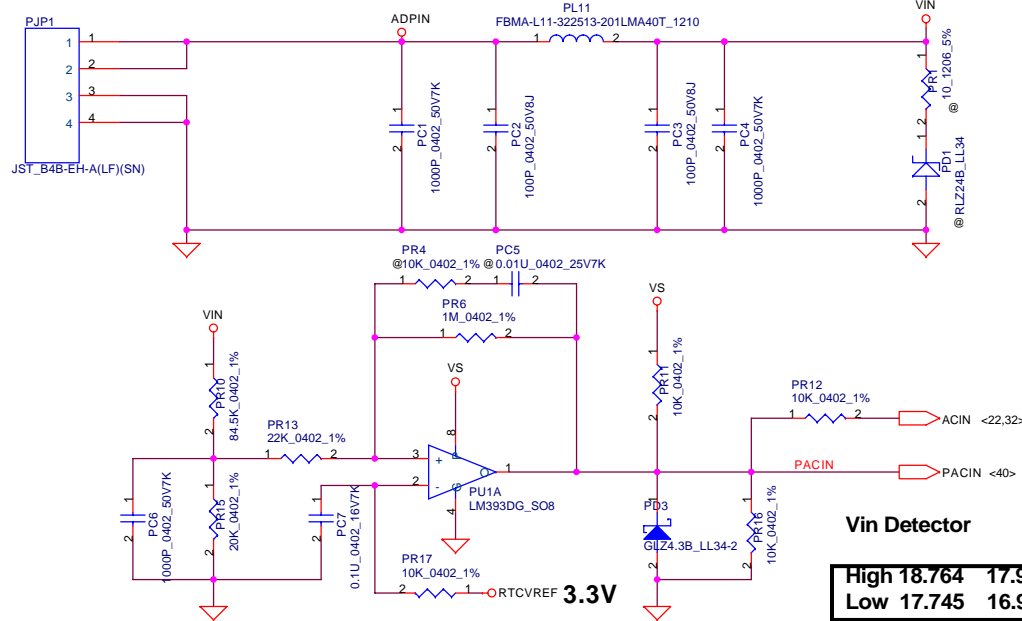


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title Power OK, Reset and RTC Circuit, TP		
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				Date:	Thursday, March 06, 2007	Sheet 36 of 45



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC Interface		
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				Date:	Thursday, March 06, 2007	Sheet 37 of 45

DC030005Q00

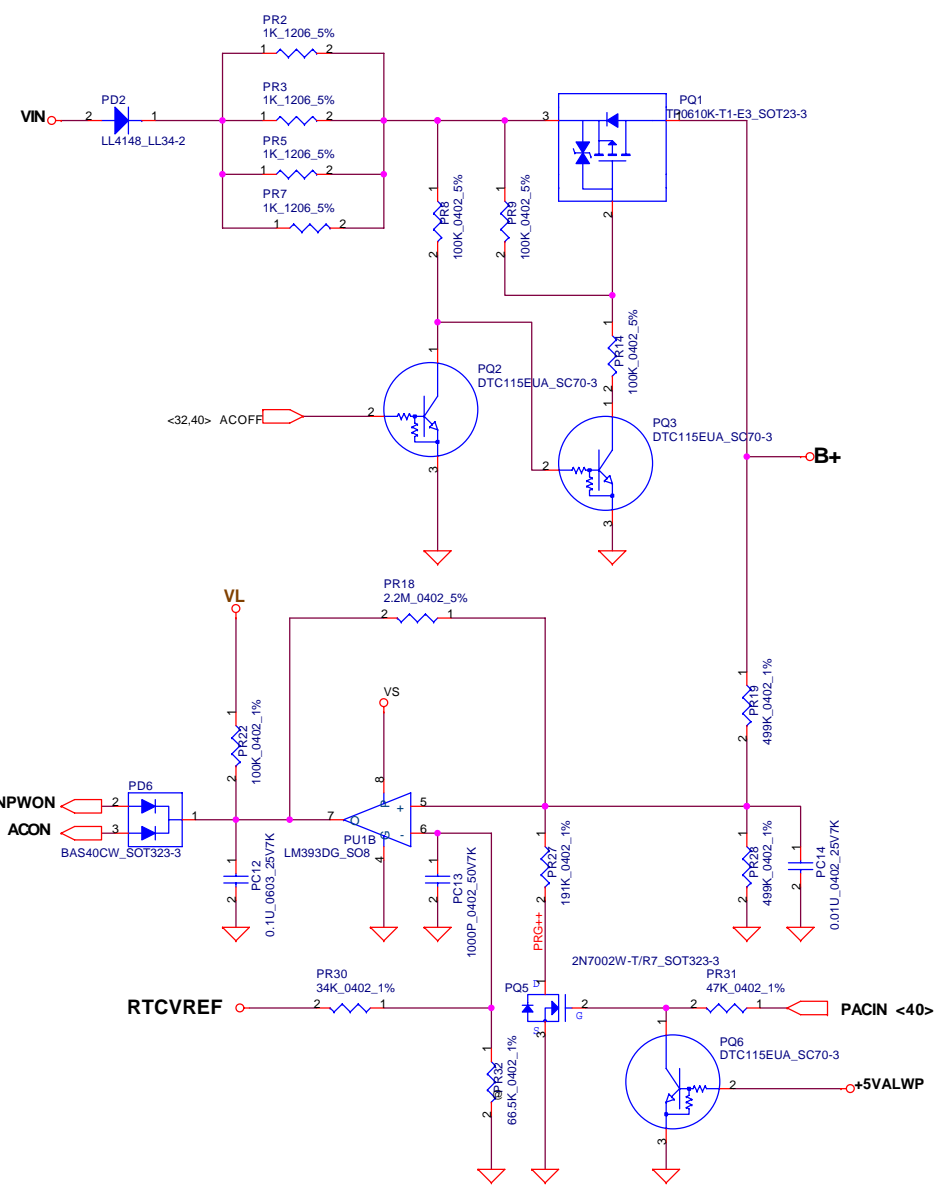


**ACIN**

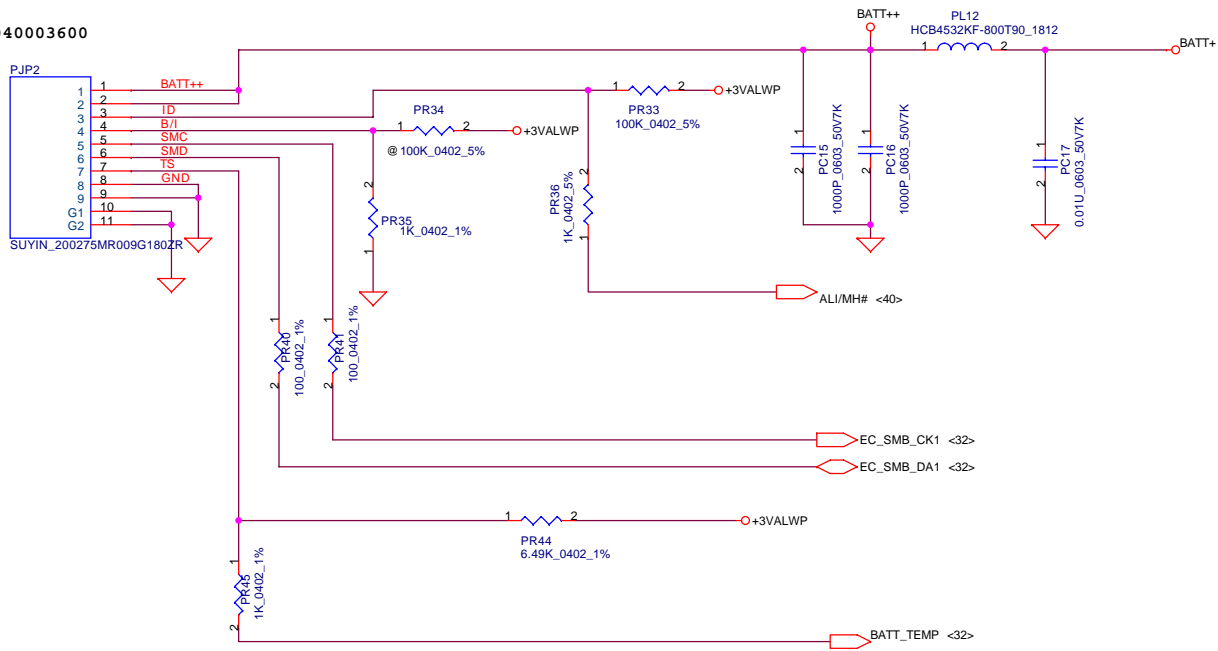
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

**BATT ONLY**

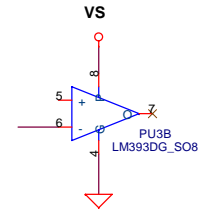
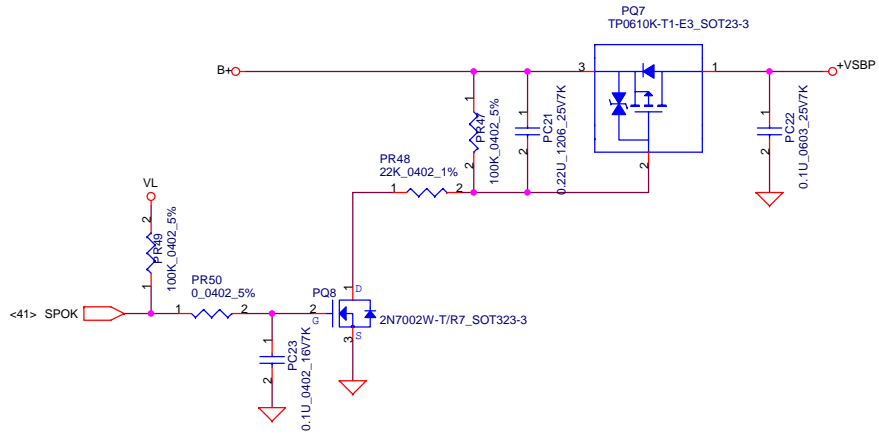
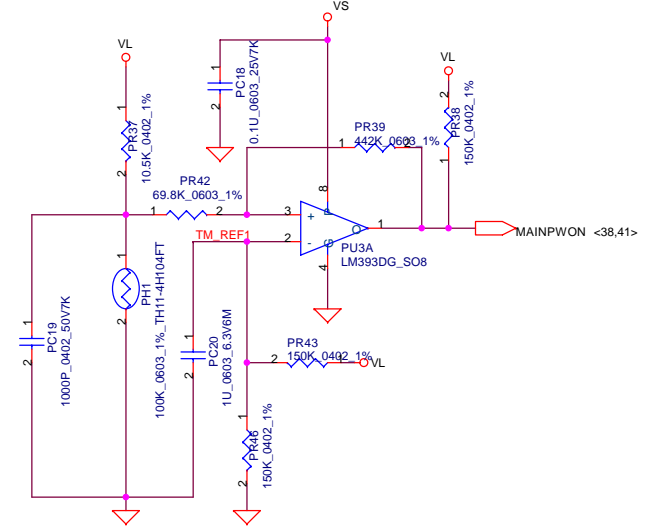
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



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Size	B	Document Number	IHL00 LA-3691P		Rev
Date:		Thursday, March 08, 2007	Sheet	38	of 45



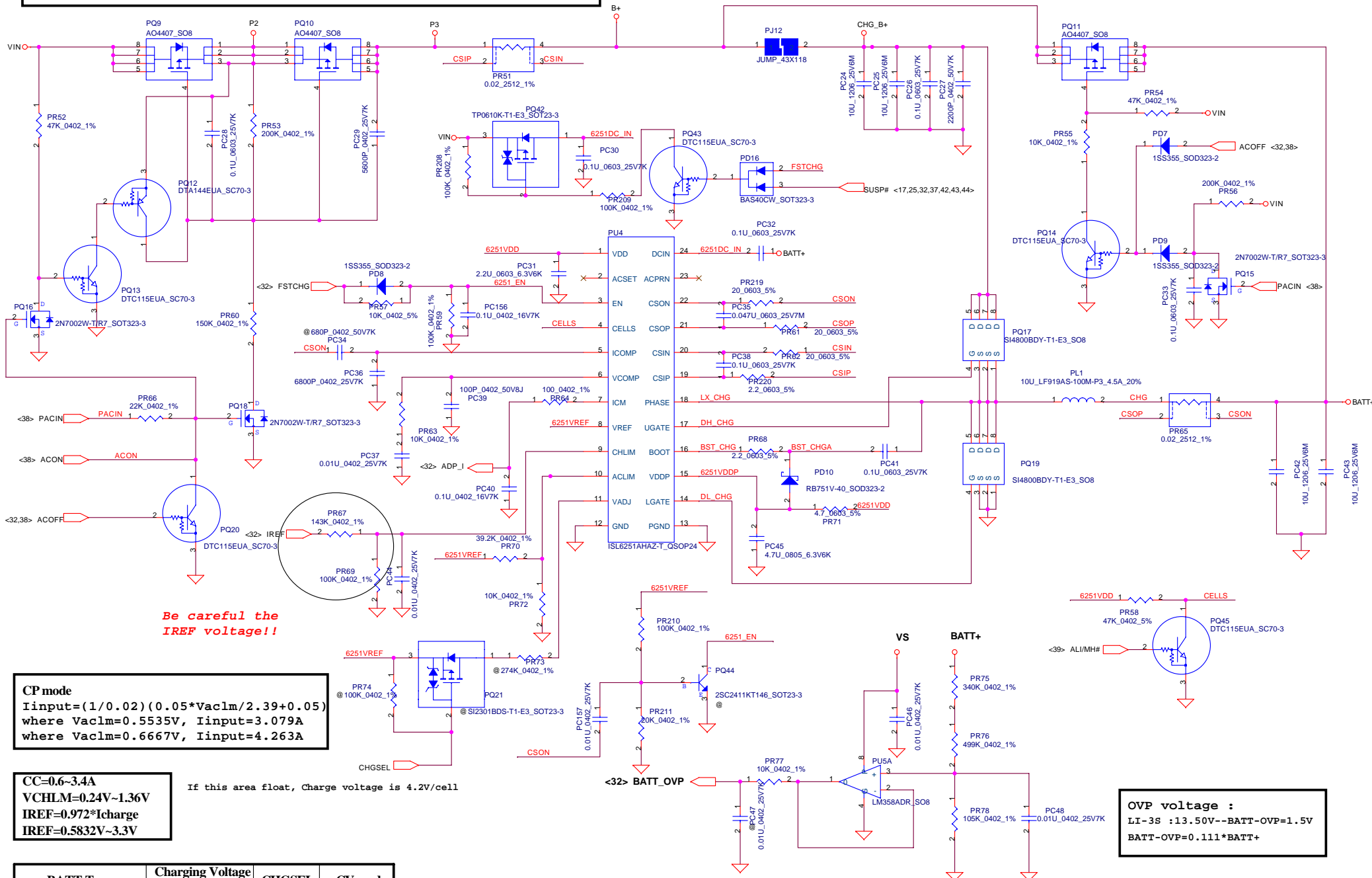
PH1 under CPU bottom side :  
 CPU thermal protection at 87 degree C  
 Recovery at 70 degree C



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Size B	Document Number			Rev	
	IHL00 LA-3691P			0.2	
Date:	Thursday, March 08, 2007	Sheet	39	of	45

65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR70=39.2K, CP=3.079A  
 90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR70=28.7K, CP=4.263A

$$ADP\_I = 19.9 * I_{adapter} * R_{sense}$$



**Be careful the IREF voltage!!**

**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$   
 where  $V_{aclm} = 0.5535V$ ,  $I_{input} = 3.079A$   
 where  $V_{aclm} = 0.6667V$ ,  $I_{input} = 4.263A$

**CC=0.6~3.4A**  
 $V_{CHLM} = 0.24V \sim 1.36V$   
 $I_{REF} = 0.972 * I_{charge}$   
 $I_{REF} = 0.5832V \sim 3.3V$   
 If this area float, Charge voltage is 4.2V/cell

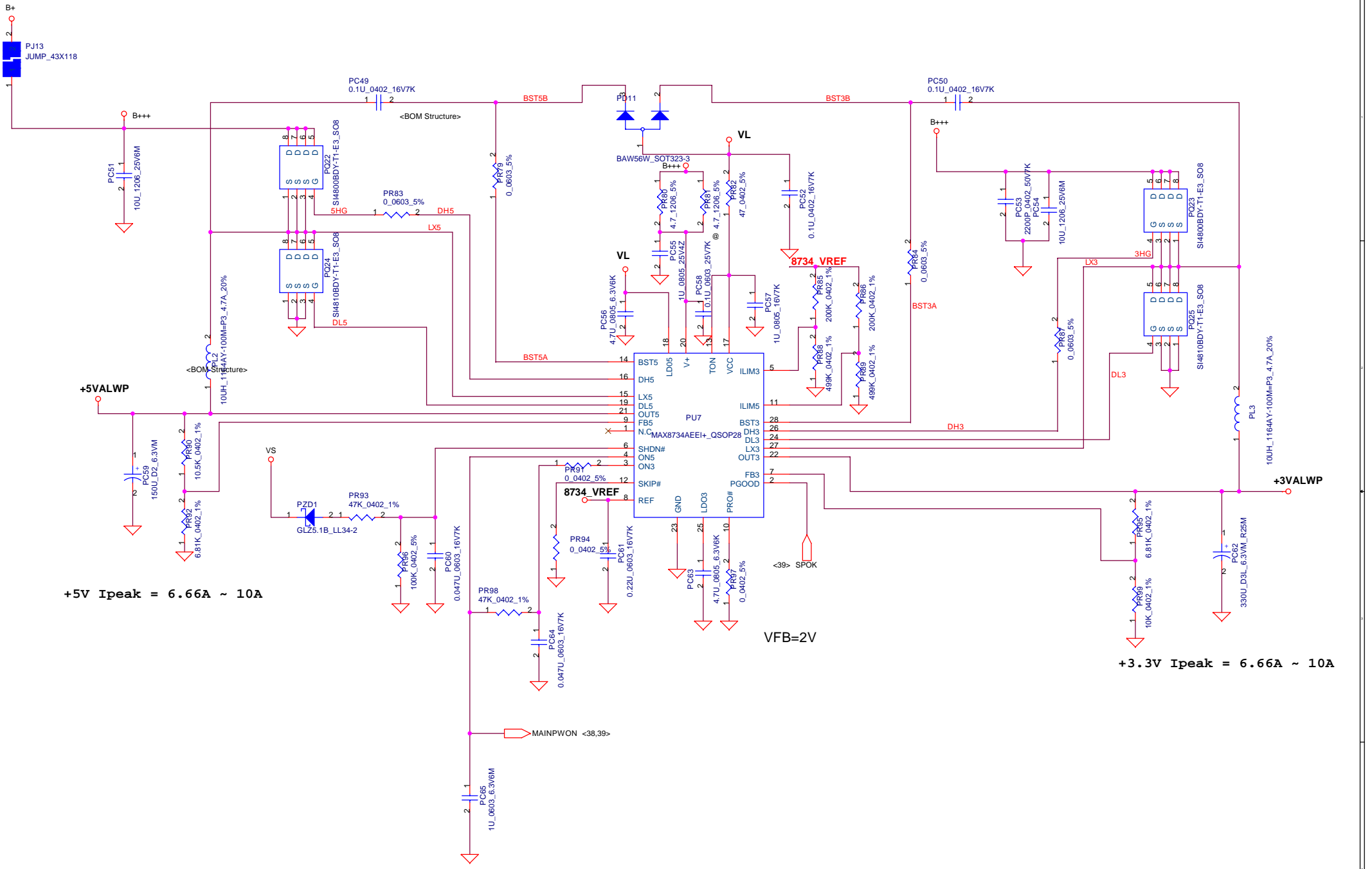
**OVP voltage :**  
 $LI-3S : 1.3.50V \sim BATT-OVP = 1.5V$   
 $BATT-OVP = 0.111 * BATT+$

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

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Title <b>CHARGER</b>			
Size	Document Number	Rev	
	<b>IHL00 LA-3691P</b>	0.2	
Date:	Thursday, March 08, 2007	Sheet	40 of 45



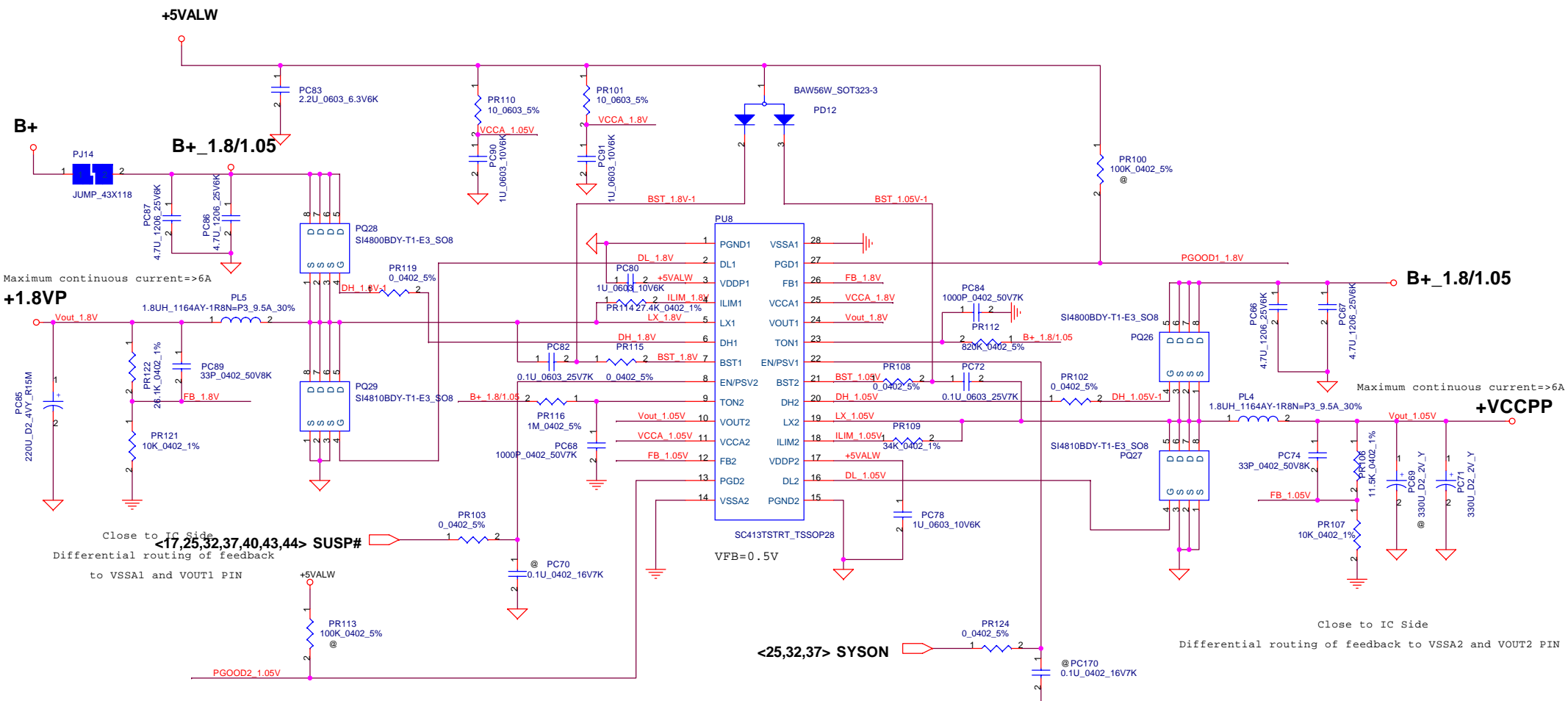


**+5V Ipeak = 6.66A ~ 10A**

**+3.3V Ipeak = 6.66A ~ 10A**

VFB=2V

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				<b>+5VALWP/+3VALWP</b>		
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				Custom	IHL00 LA-3691P	0.2
				Date:	Thursday, March 08, 2007	Sheet 41 of 45



Maximum continuous current=>6A

Maximum continuous current=>6A

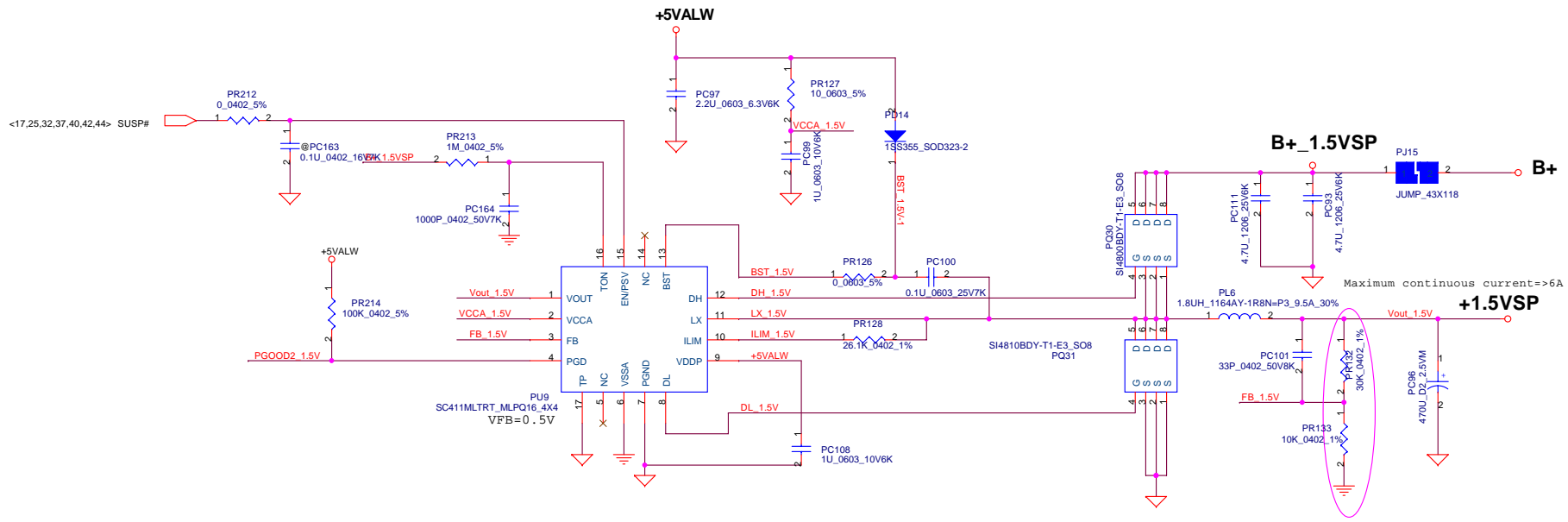
VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
**Ipeak=12.17A, Imax=8.519A**  
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$   
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$   
 FDS6670AS:Rds(on)=>Typ:9 mOhm  
 Max:11.5 mOhm  
 $Iocp = Ivalley + Iripple / 2$   
 $Iripple = (vin - vout) * (Ton / L) = 5.467A, 1/2 Iripple = 2.734A$   
 $Ivalleymin = 10E-6 * (PR120 / Rds(ON)max * 1.5)$   
 $= 9 * 10e-6 * (27.4K / 0.0115 * 1.5) = 14.295A > 11.73 * 1.2 = 14.076A$   
 $Ivalleymax = 10E-6 * (PR120 / Rds(ON)typ * 1.2)$   
 $= 11 * 10e-6 * (27.4K / 0.009 * 1.2) = 27.907A$   
 OCP=>17.029A~30.641A

VFB=0.5V  
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$   
**Ipeak=5.16A, Imax=3.612A**  
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$   
 $= 0.3201us$   
 AO4916 Rds(on)=>Typ:21 mOhm  
 Max:27 mOhm  
 $Ivalleymin = 9 * 10u * (29.4K / 0.027 * 1.4) = 7A$   
 $Ivalleymax = 11 * E-6 * (29.4K / 0.021 * 1.1) = 12.833A$   
 $Iripple = (vin - vout) * (Ton / L) = 2.546A, 1/2 Iripple = 1.273A$   
 $Iocp = Ivalley + Iripple / 2$   
 OCP=>8.273A~14.106A



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Date:	Thursday, March 08, 2007	Sheet	42	of	45

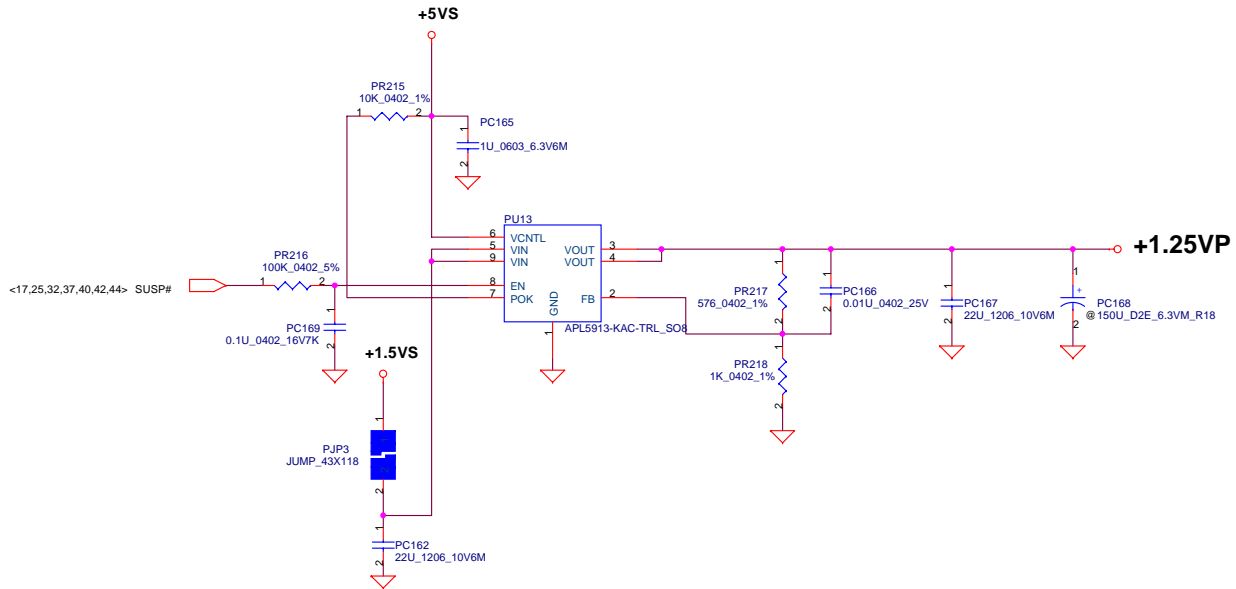
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**B+ 1.5VSP**  
 Maximum continuous current=>6A

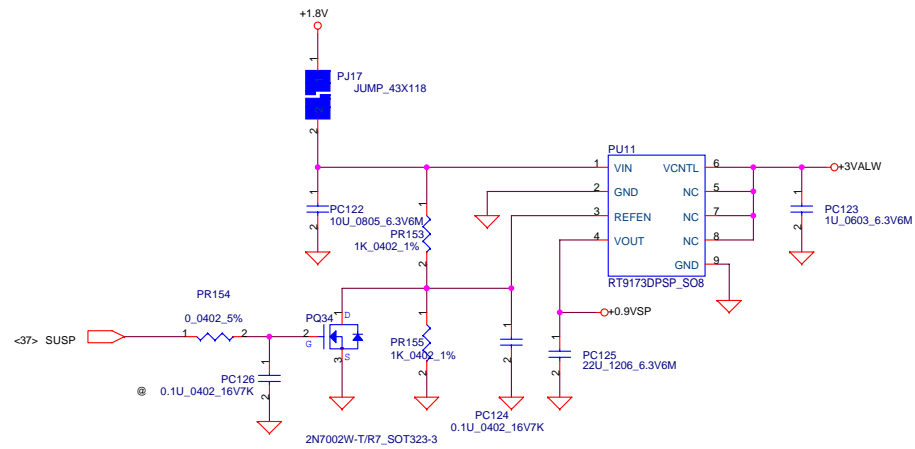
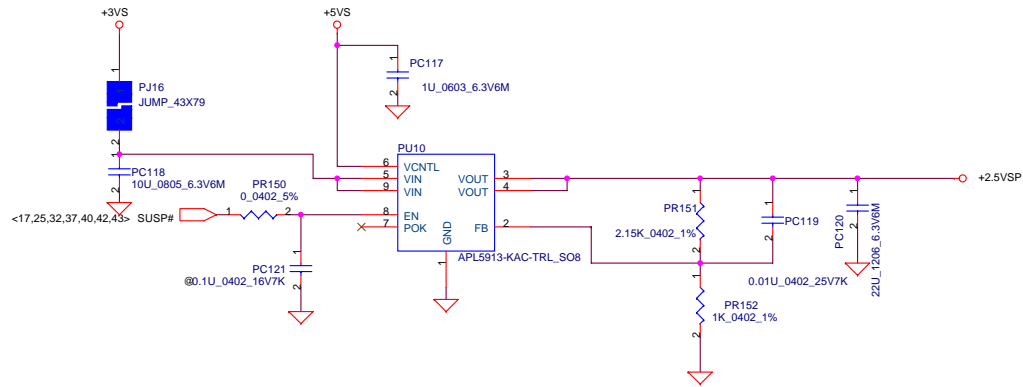
Close to IC Side  
 Differential routing of feedback to VSSA2 and VOUT2 PIN

**Ipeak=2.91A, Imax=2A.**  
**Vo=0.8\*(1+PR190/PR191)=1.2608V**



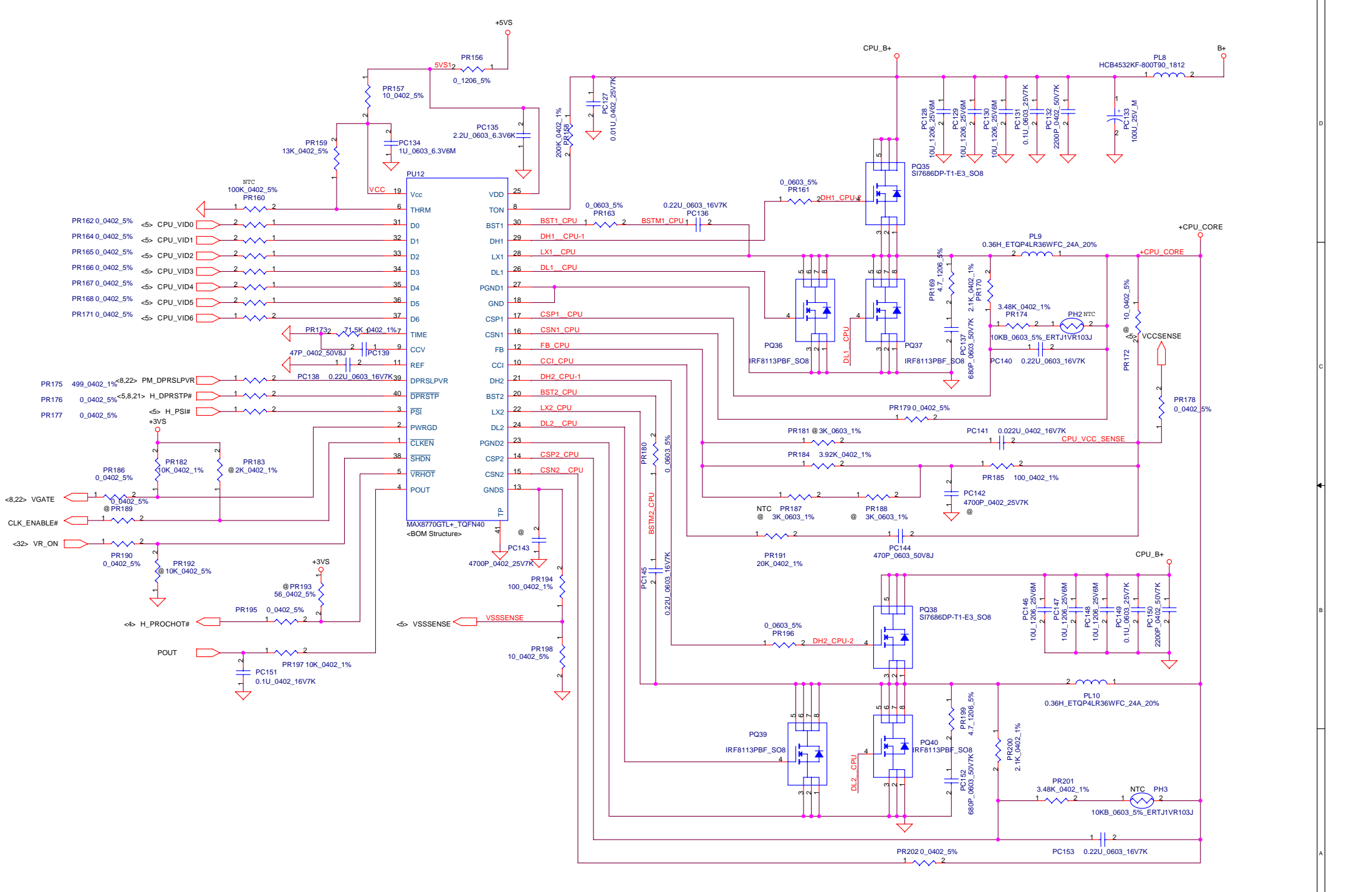
**VFB=0.5V, Ipeak=14.02A, Imax=9.814A**  
 The current rating of +1.05VSP include +VCC\_GFX current.  
 $V_o = V_{FB} * (1 + PR146 / PR147) = 1.05V$   
 $Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.2391us$   
 $SI4810BDY:Rds(on) => Typ: 9mOhm$   
 Max: 11.5 mOhm  
 $Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON))max * 1.5$   
 **$= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A$**   
 $Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON))min * 1.2$   
 $= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$   
 $Iripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Iripple = 2.146A$   
 $Iocp = Ivalley + Iripple / 2$   
**OCP => 15.763A ~ 22.222A**

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Date: Thursday, March 08, 2007				Rev 0.2



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<b>+2.5VSP/0.9VSP</b>		
Size	Document Number	Rev
Custom	IHL00 LA-3691P	0.2
Date:	Thursday, March 08, 2007	Sheet 44 of 45



Security Classification	Compal Secret Data		Title	
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Date:	Thursday, March 08, 2007	Sheet	45	of 45

*Version change list (P.I.R. List)*

Item	Fixed Issue	Rev.	PG#	Modify List	B. Ver#	Phase
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						

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Title	<b>POWER PIR</b>	
Size	Document Number	Rev
Date:	Thursday, March 08, 2007	Sheet 48 of 48

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B. Ver#	Phase
1	XDP_BPM#0~4 test point short as EMI request	B	4	Modify Layout		
2	ADD J6 for +VCC_AXG UMA VGA power shape	B	11	Modify Layout		
3	Fixed Speaker no function	A2	37	Change Q91 form SI2301BDS to MMBT3906, Del R895		
4	Fixed SWDJ function can't work	A2	36	Add R904		
5	Fixed Audio Codec can't work	A2	29	Add R905,Q96		
6	Fixed USB Port4 can't work	A2	27	Swap USB_N4 & USB_P4		
7	Fixed EMI issue	A2	32 37	Add R908,C878,C879		
8	Fixed SWDJ mode EC_MUTE# ISSUE	B	30	Add D39,Q99,R914		
9	Fixed CMOS noise	B	36	Add R912,C880		
10	Fixed EMI	B	25	Add C881,C882		
11	Add chipset id	B	33	Add R915,R916		
12	Fix SWDJ Subwoofer issue	B	31	Add R917		
13	Fix DFX issue	C	22,33	Change Y3,X1,Y2 footprint		
14	FOR E-STAR V4 wake on lan	C	22,33	Add R918,R919		
15	For ESD issue	C	36	Add C883~C887 D40,D41		
16	For AUDIO team design	C	30	Add R920 R921		
17	Change LAN led function	C	25	Swap JP73 PIN12 & PIN14		

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Title		POWER PIR	
Size	Document Number	Rev	
Date:	Thursday, March 08, 2007	Sheet	48 of 48

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