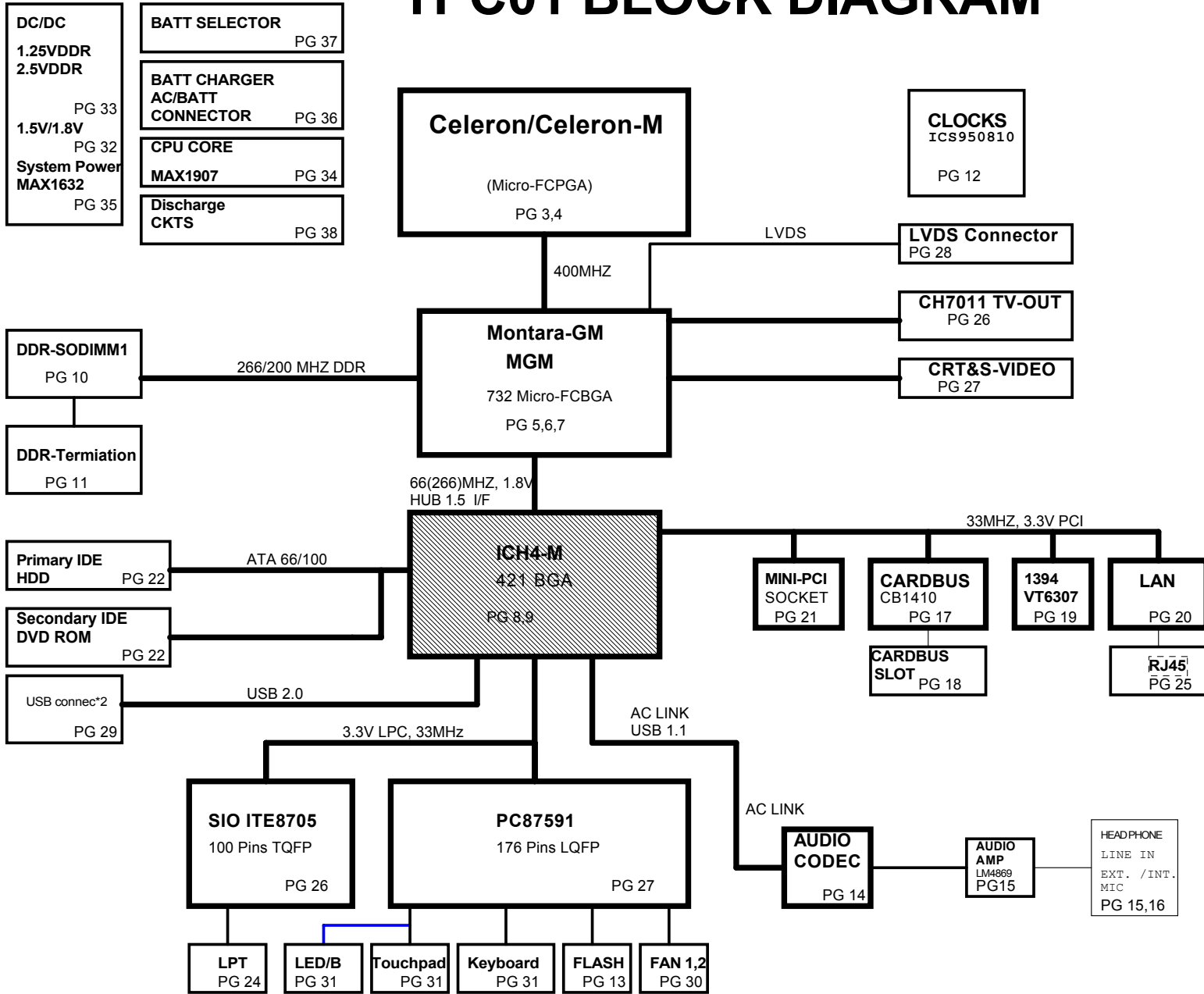


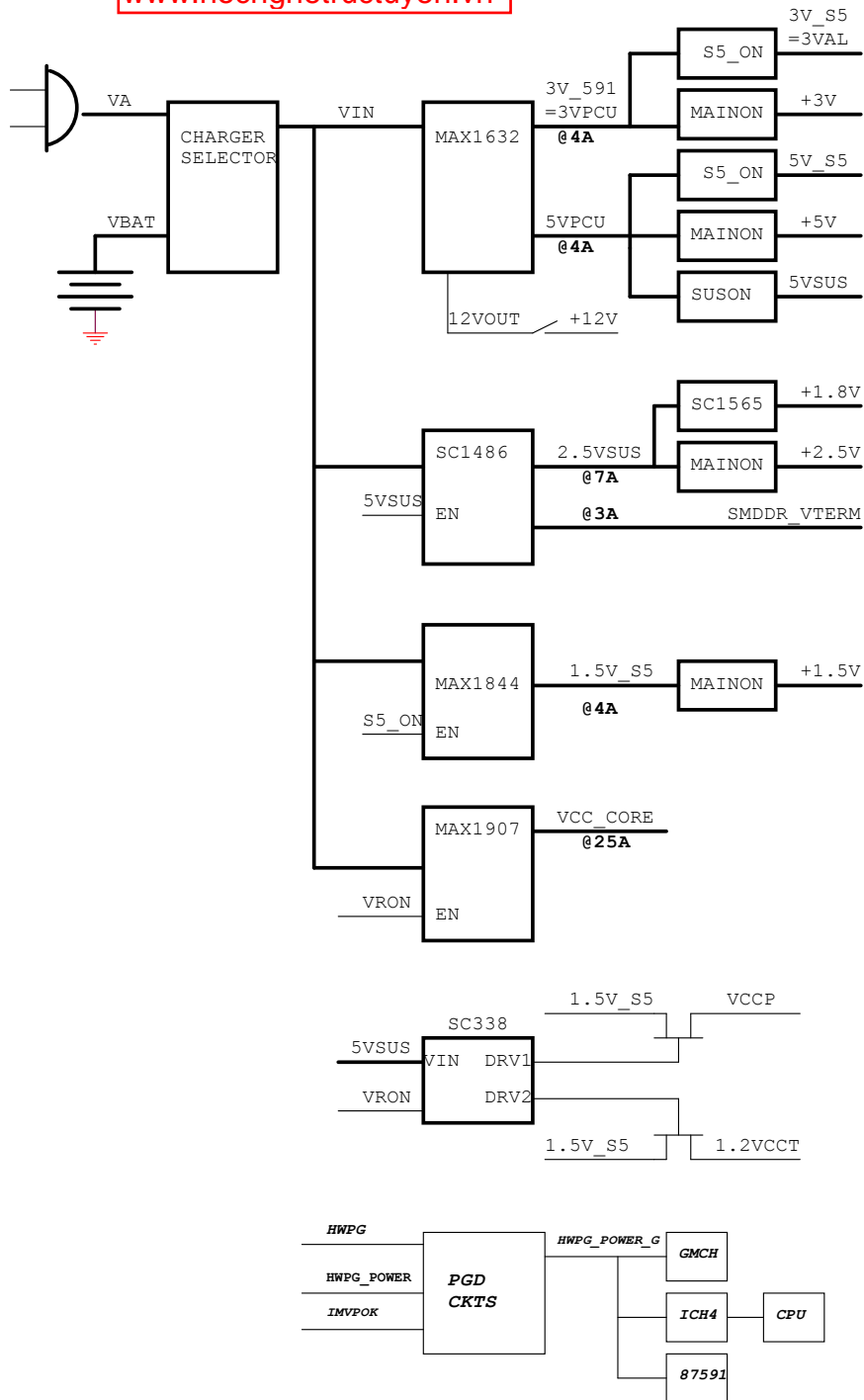
TPC01 BLOCK DIAGRAM

	PIRQ#	REQ#/GNT#	IDSEL
VGA	X	X	X
CARDBUS	C, (B)	3	22
IEEE 1394	B	2	23
MINI-PCI	E, F	1	20
LAN	D	0	18
USB 2.0	X	X	X



**I/O BOARD
50 Pins**
*LINEOUT
MIC JACK
USB 2.0 X2
RJ11*

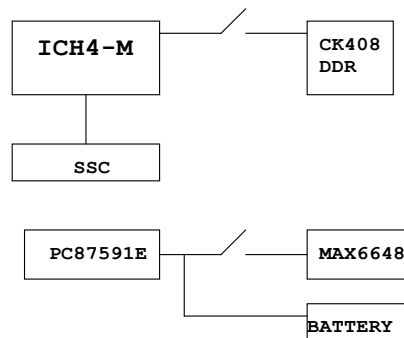
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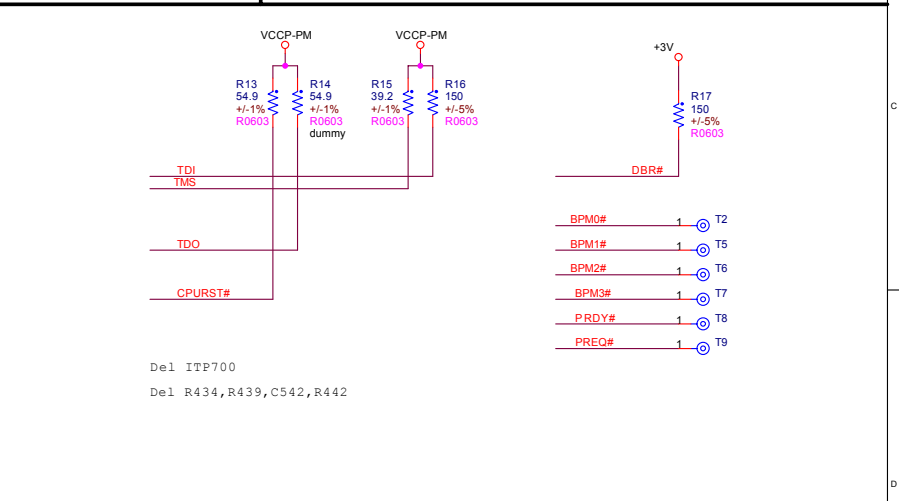
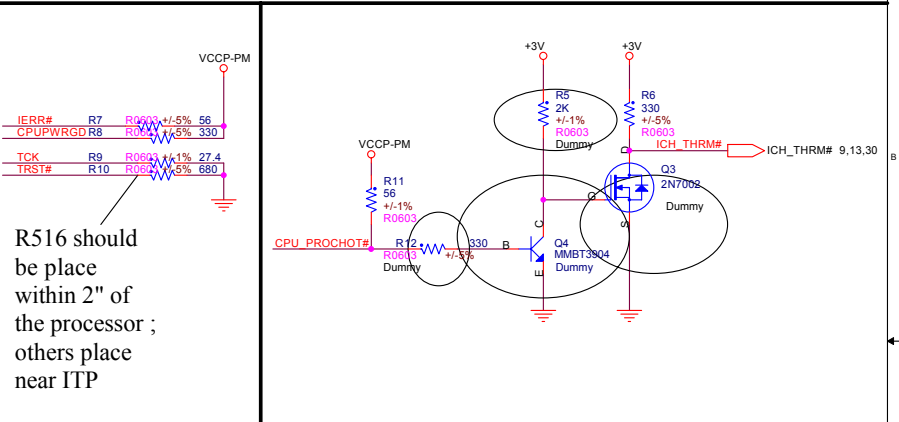
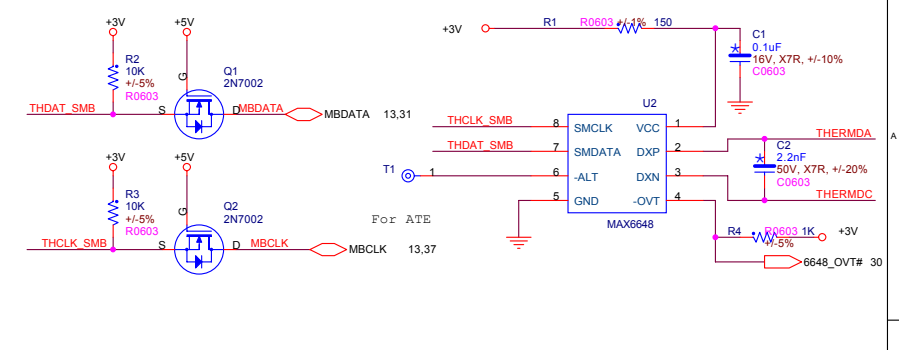
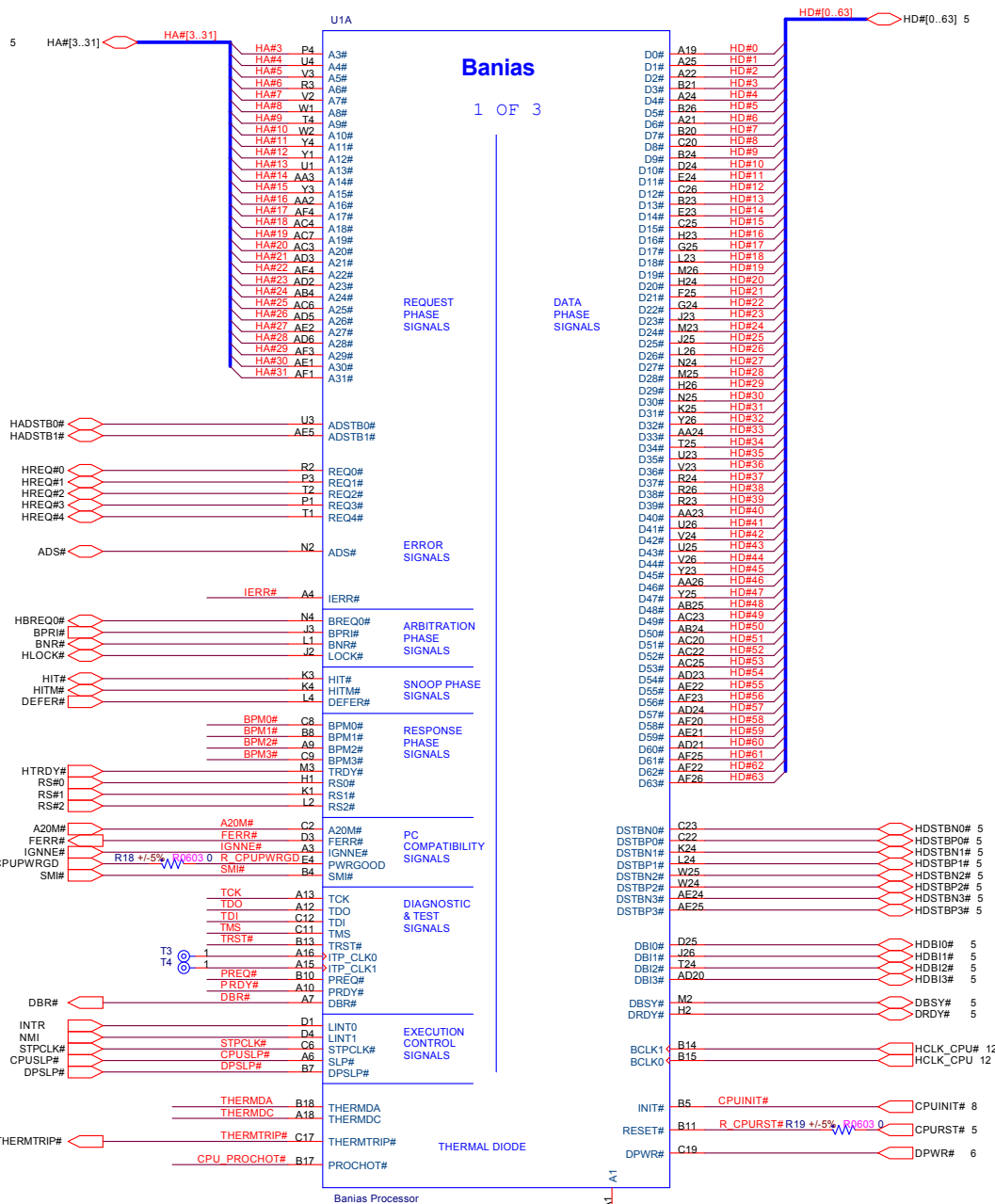


Device	CPU	GMCH	ICH4-M	PC87591	DDR	AUDIO	HDD	LCD	INV	USB2.0	LAN
5VPCU											
3V_591				●							
3V_S5			●								
5V_S5			●								
1.5V_S5			●								
5VSUS											
2.5VSUS		●			●						
SMDDR_VTERM		●			●						
+5V						●			●	●	
+3V			●			●	●	●			
+2.5V		●									
+1.5V		●	●								
1.2VCCT		●									
+1.8V	●										
VCC_CORE	●										
VCCP	●		●								
+12V											

S0 POWER => ICH4 3.3*165 +67.5*1.5
=> ICH4 LAN LOGIC =3.3*9.2+1.5*15.5 700MW

SMB DIAGRAM





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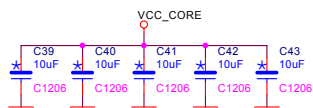
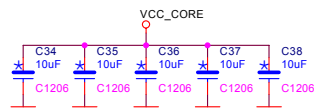
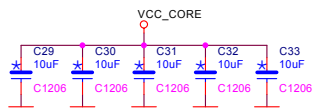
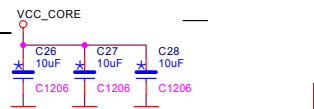
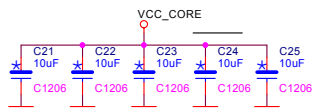
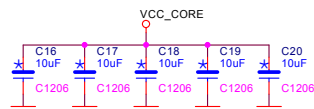
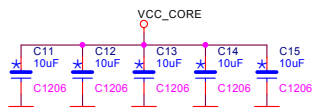
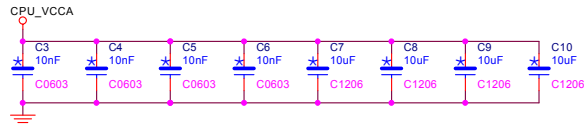
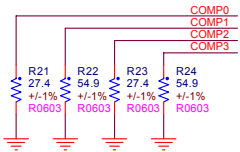
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Title: **Banias Host**

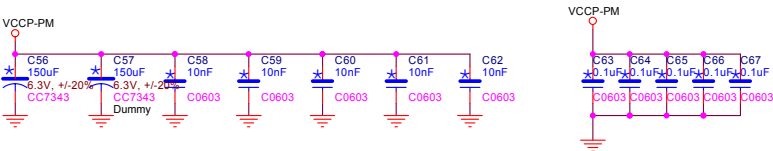
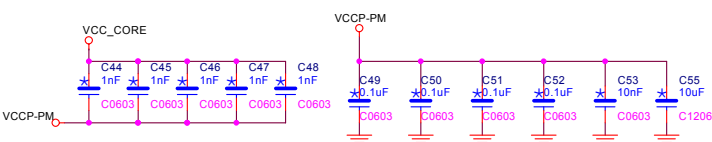
Document Number: **TPC01**

Date: Thursday, February 12, 2004 Sheet 3 of 39

These 4 Resistors need to place with 0.5" of CPU.
 Comp0,2 trace need to be $z_0=27.4\ \Omega$,
 comp1,3 traces need to be $z_0=55\ \Omega$.



-10U/6.3V Total
 caps (X5R)
 33PCS=330U



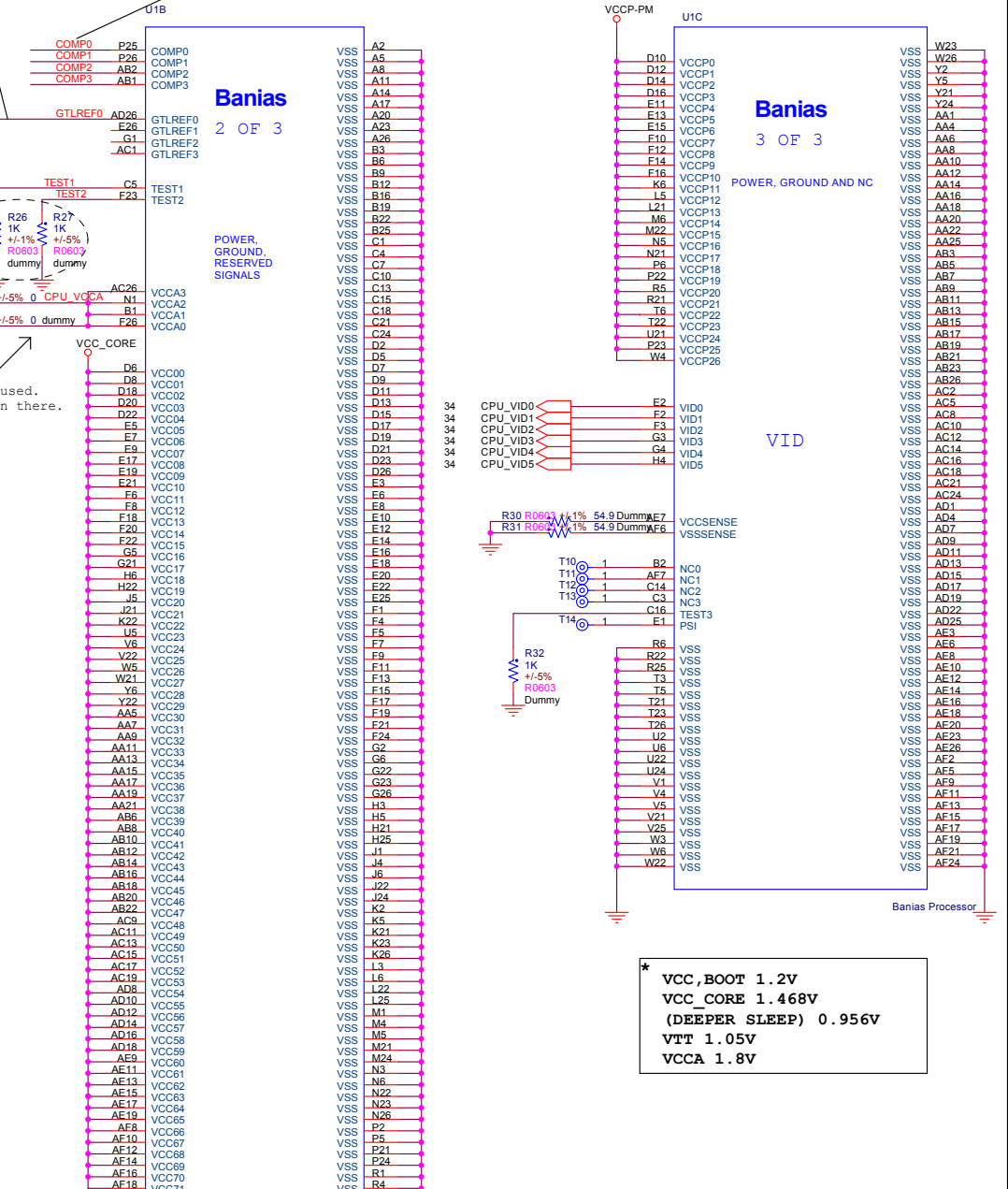
GTLREF: 2/3 VCCP+-2% 25 MILS (>50 MILS PREFERRED) SPACE
 T<0.5" 25 mils space T < 0.5"

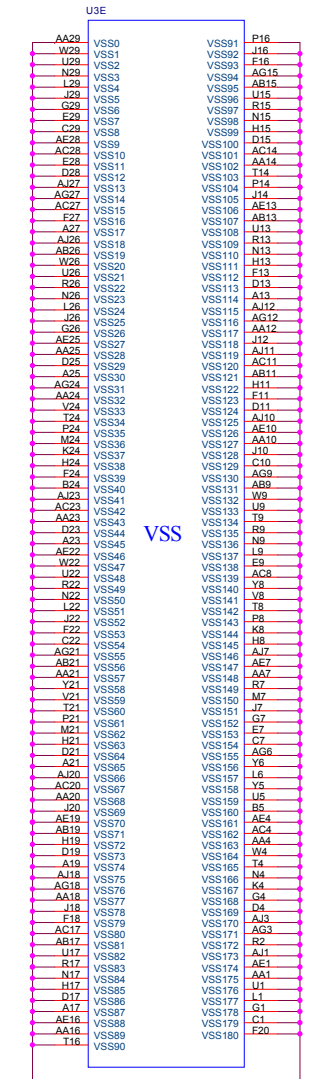
A0 CPU install R514 R502

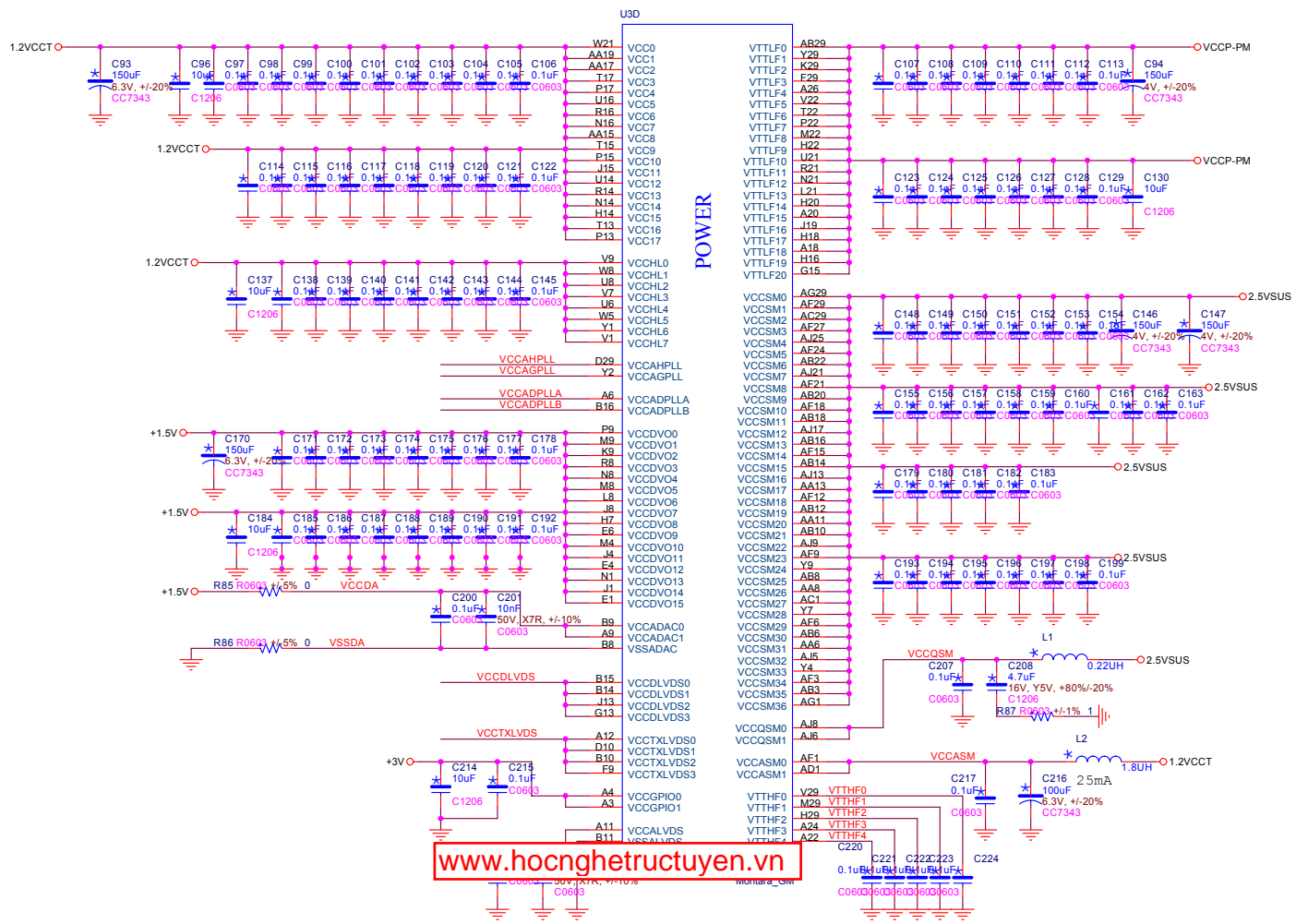
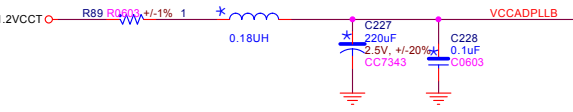
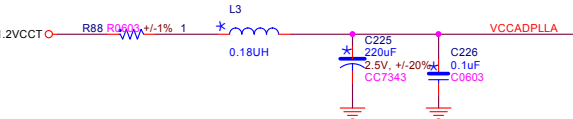
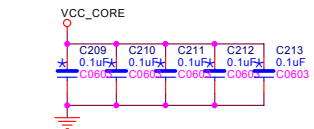
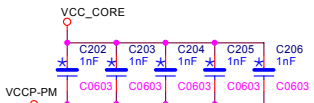
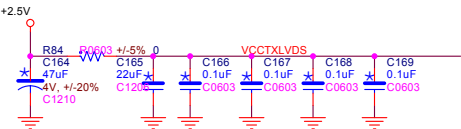
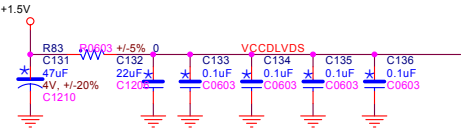
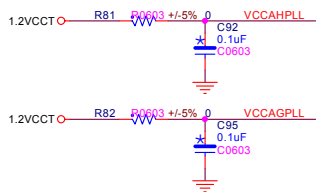
A1 CPU not install R514 R502

1.5V option is not used.
 It is ok to leave in there.

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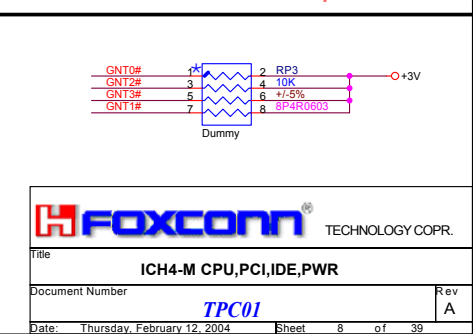
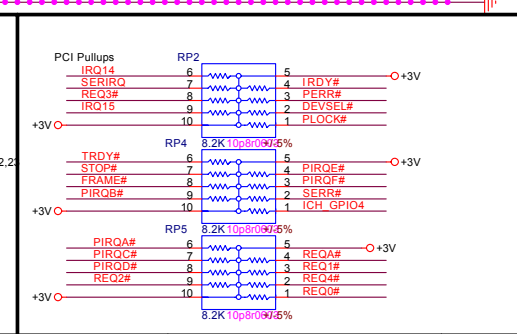
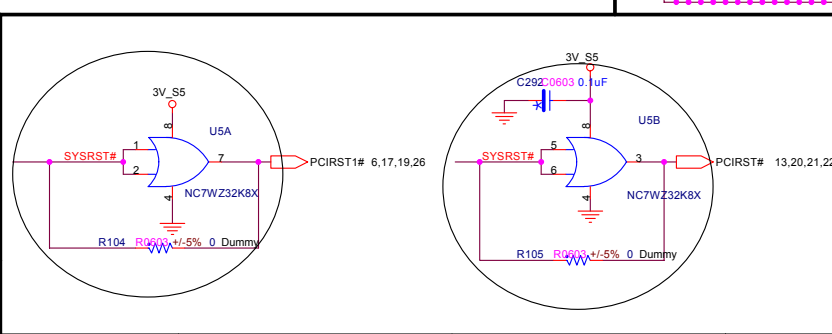
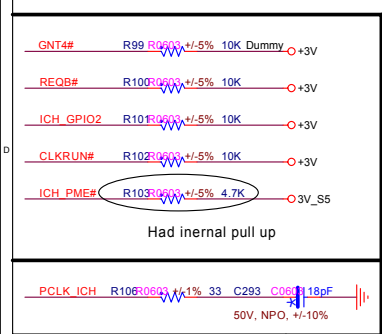
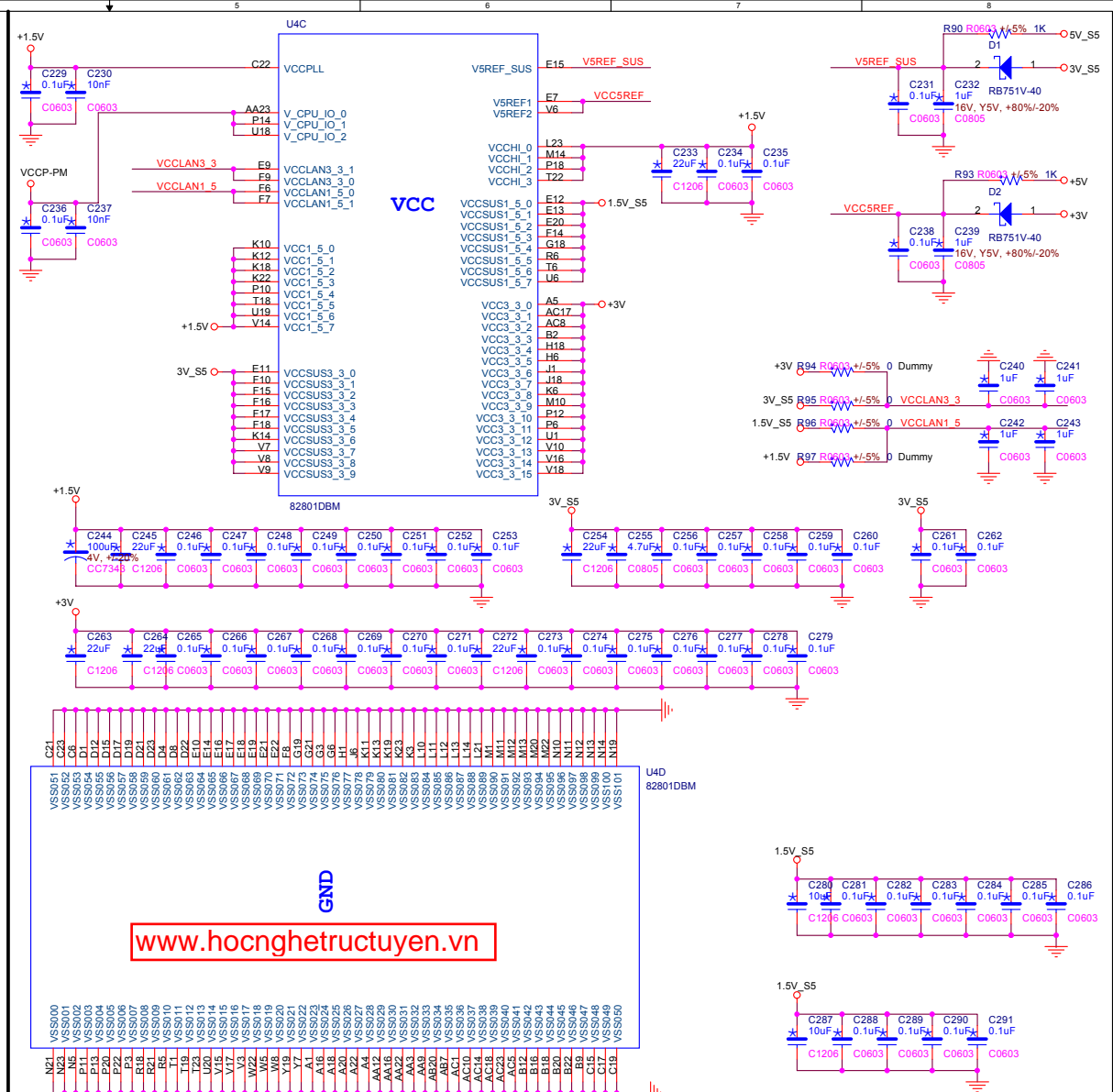
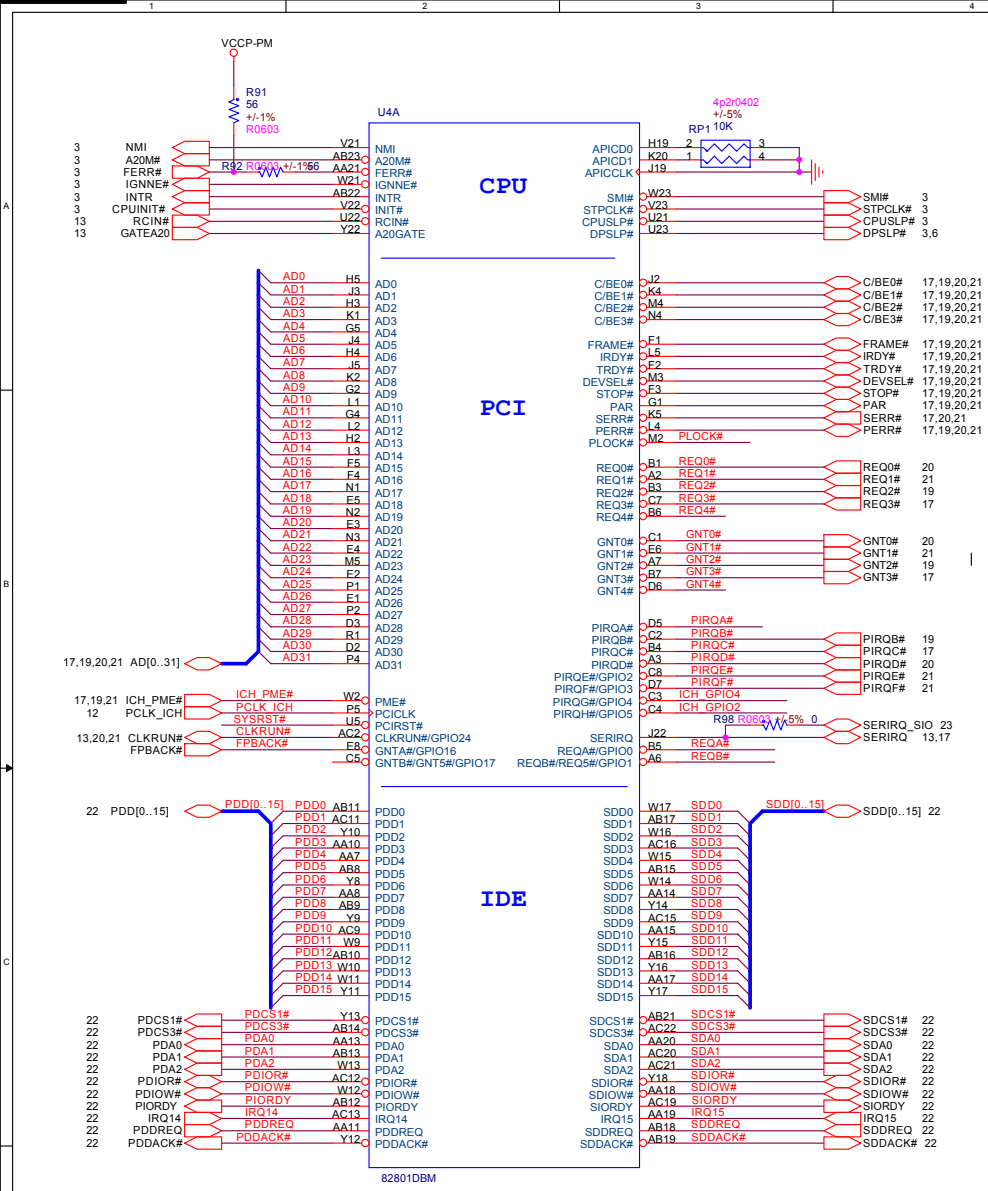






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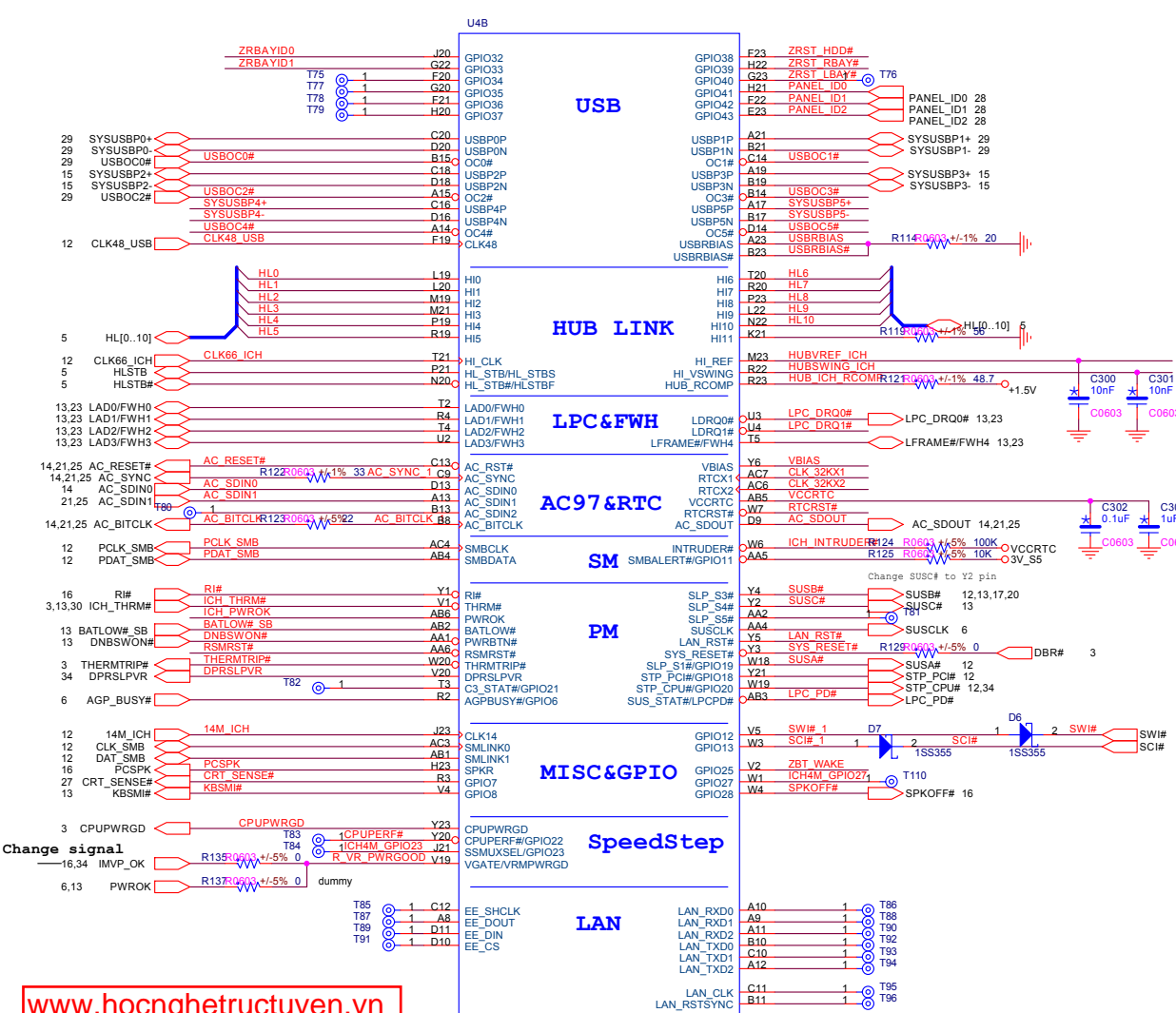


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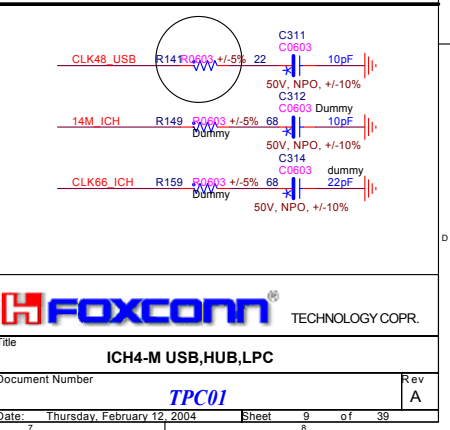
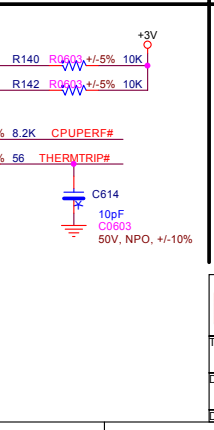
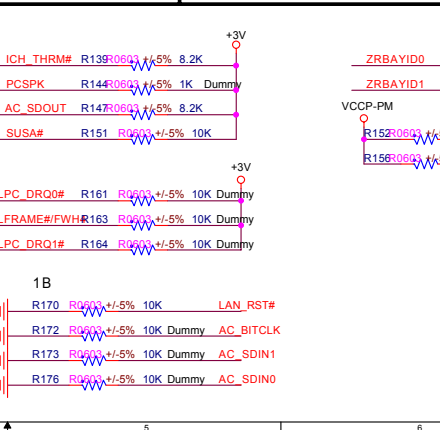
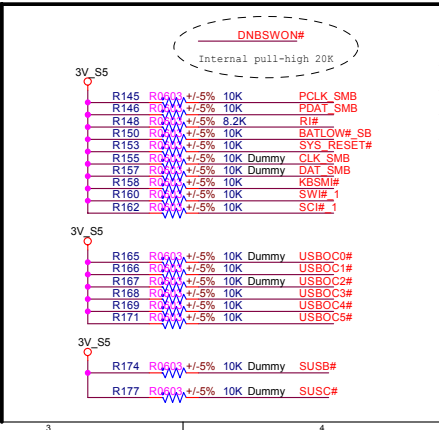
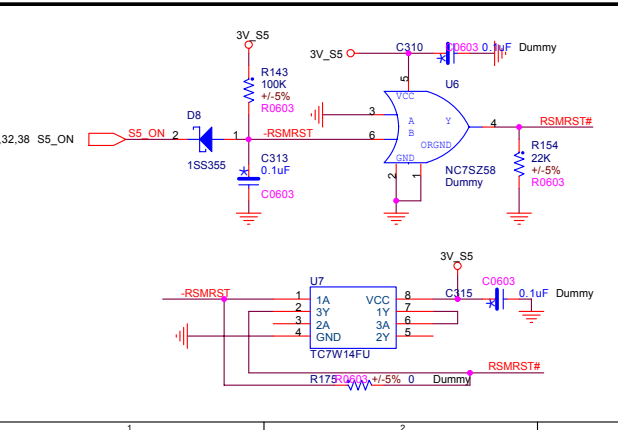
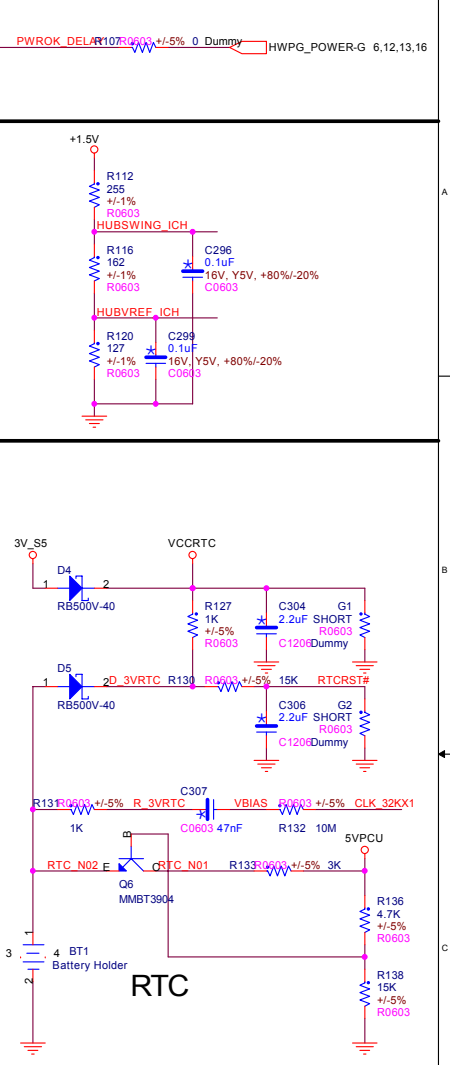
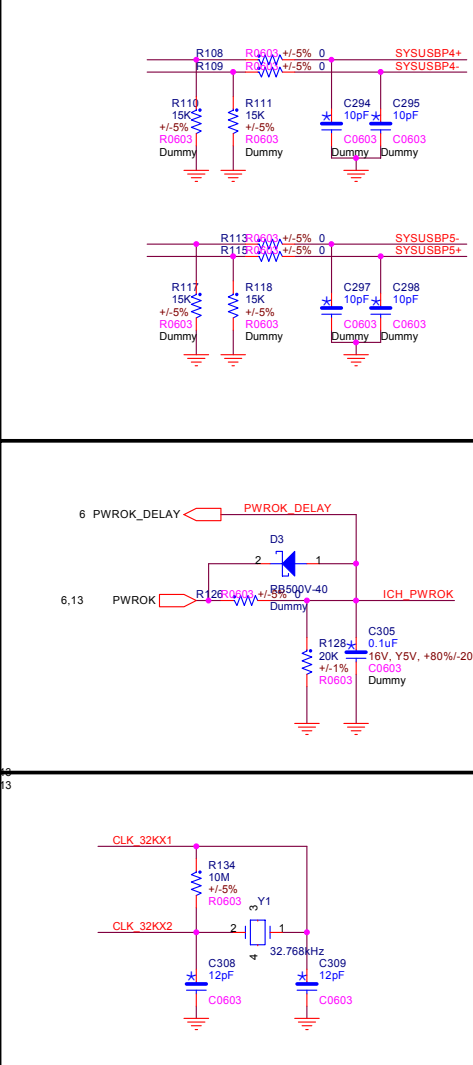
Title: **ICH4-M CPU,PCI,IDE,PWR**

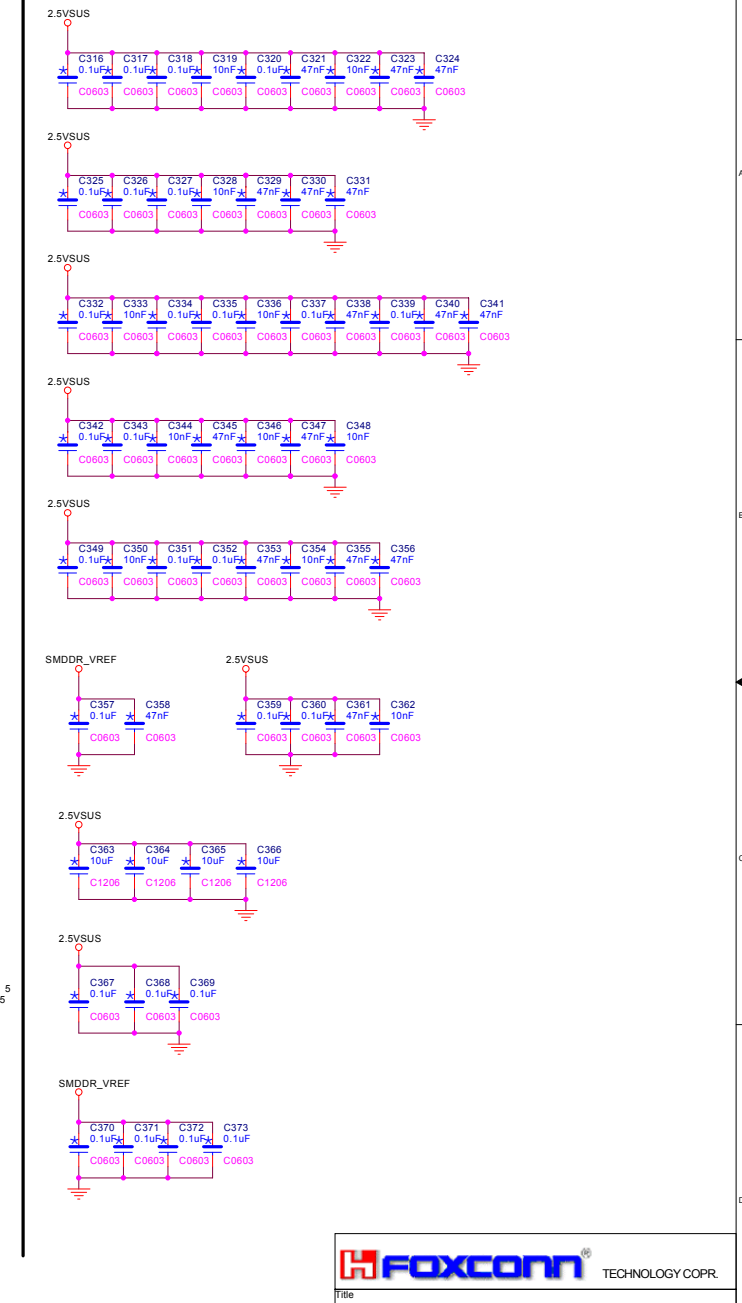
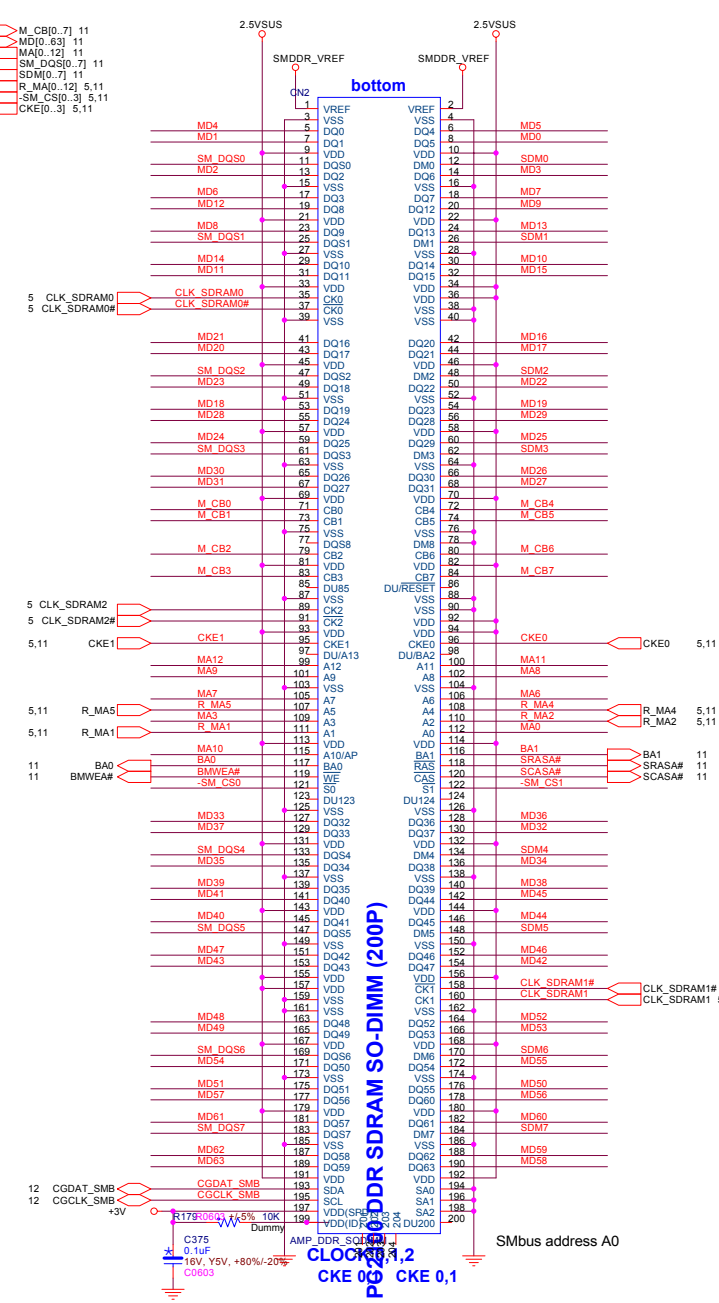
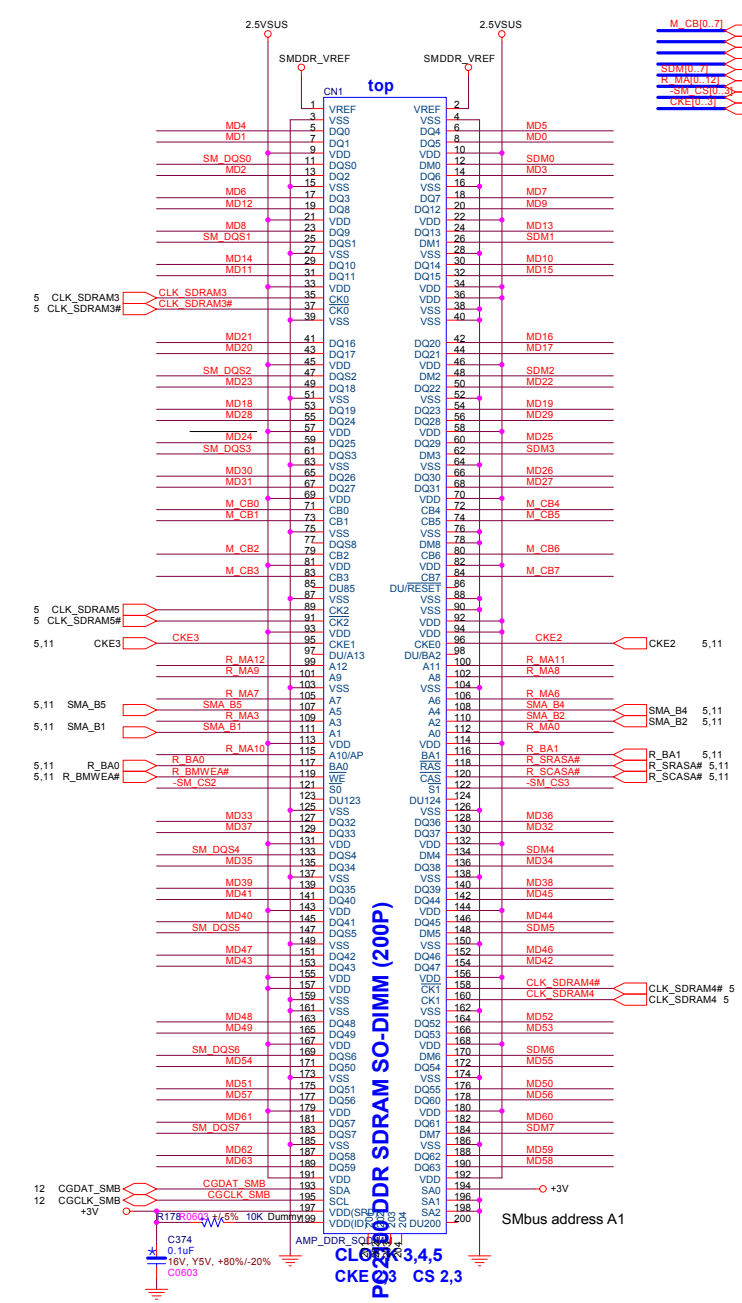
Document Number: **TPC01**

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DDR SDRAM SO-DIMM (200P)
CLK 2, 3, 4, 5
CS 2, 3

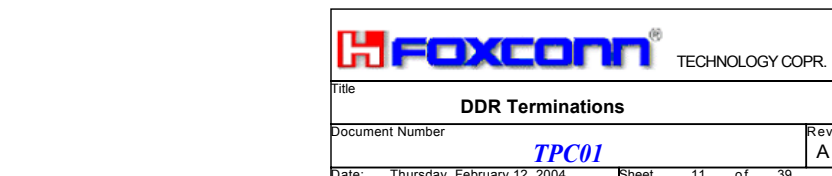
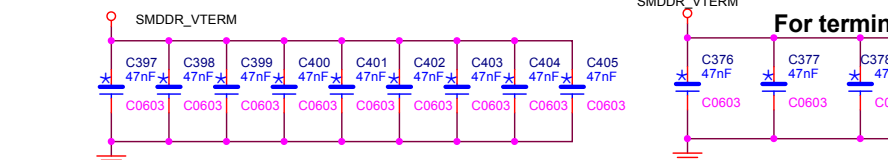
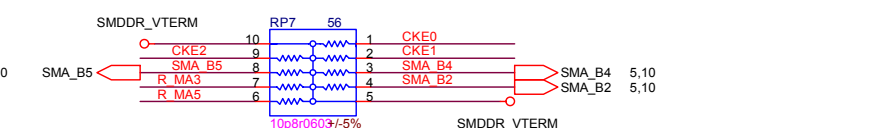
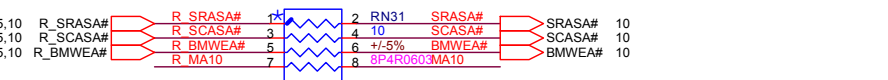
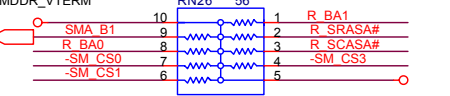
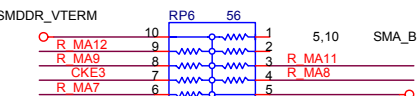
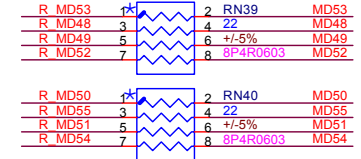
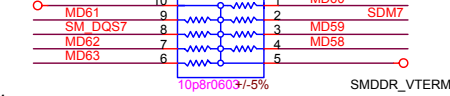
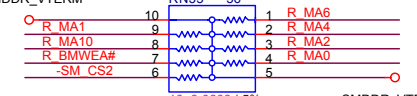
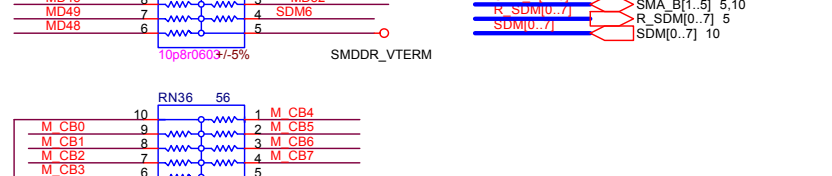
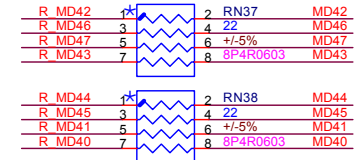
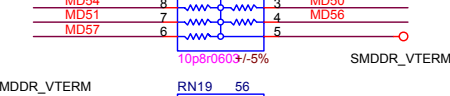
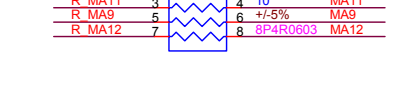
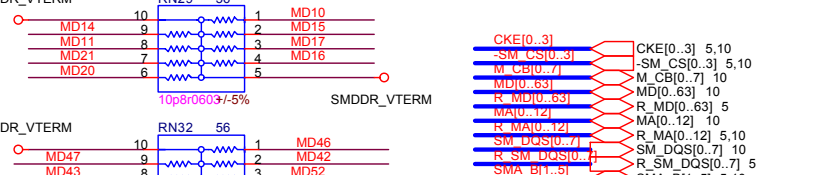
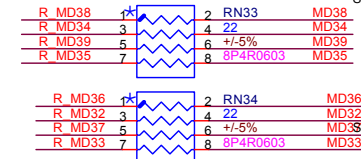
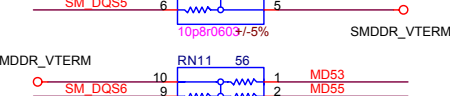
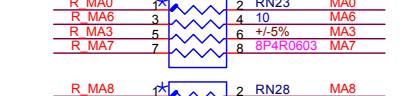
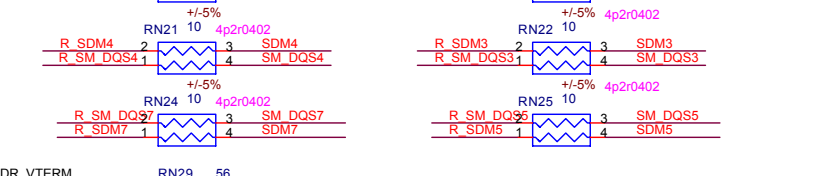
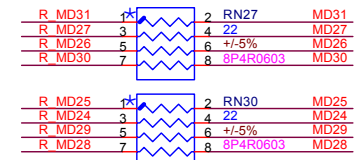
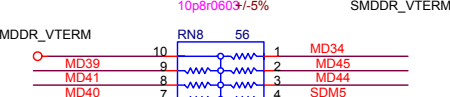
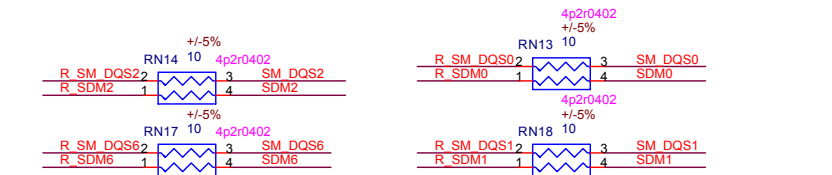
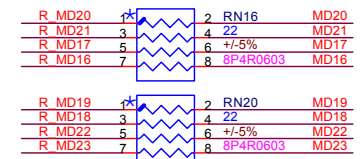
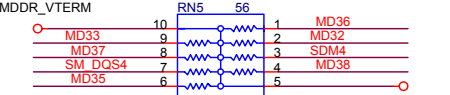
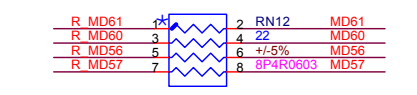
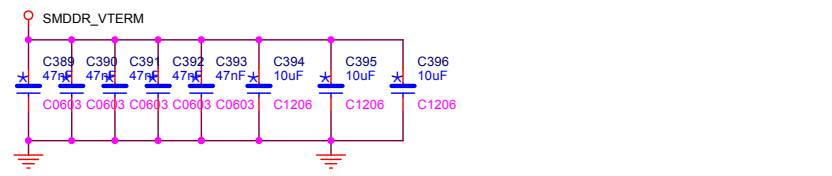
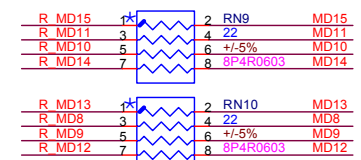
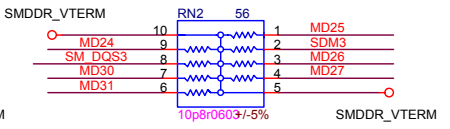
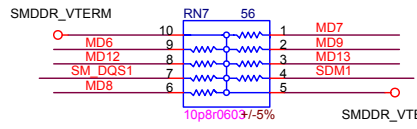
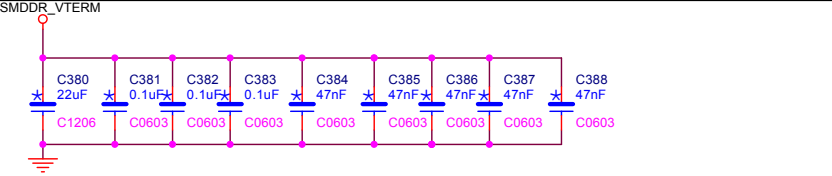
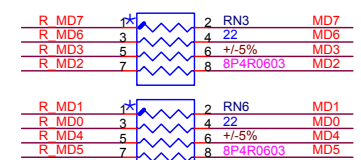
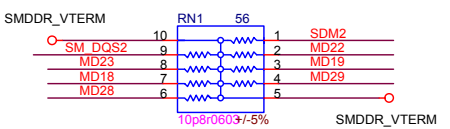
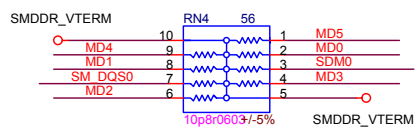
DDR SDRAM SO-DIMM (200P)
CLK 0, 1, 2
CKE 0, 1

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Title: **DDR SO-DIMM(200P)**

Document Number: **TPC01**

Date: Thursday, February 12, 2004 Sheet 10 of 39



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Title: **DDR Terminations**

Document Number: **TPC01**

Date: Thursday, February 12, 2004

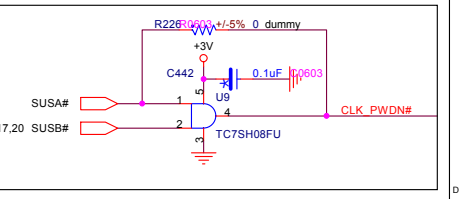
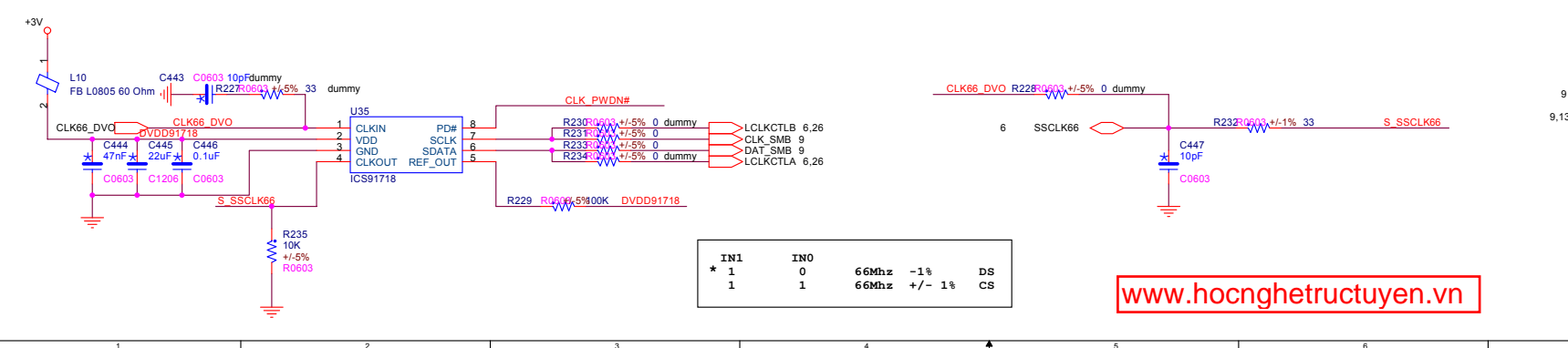
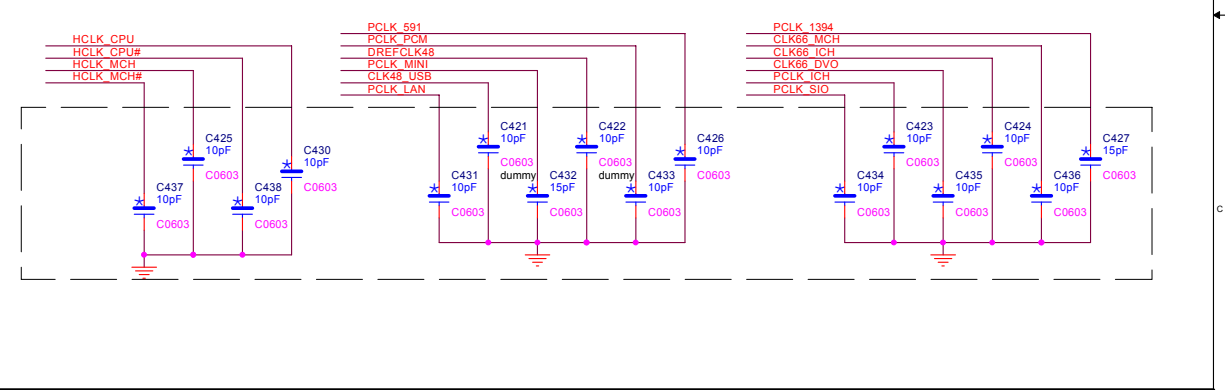
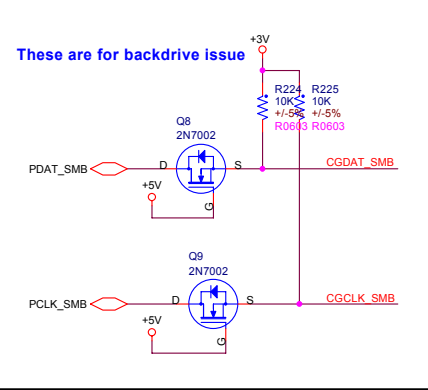
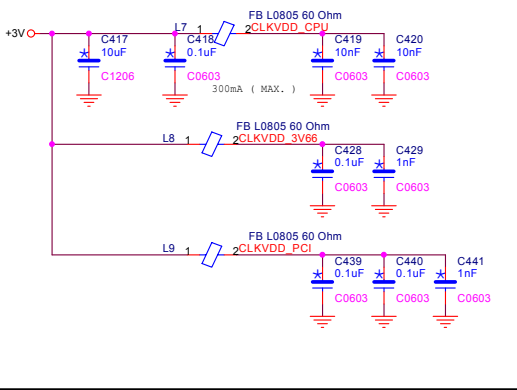
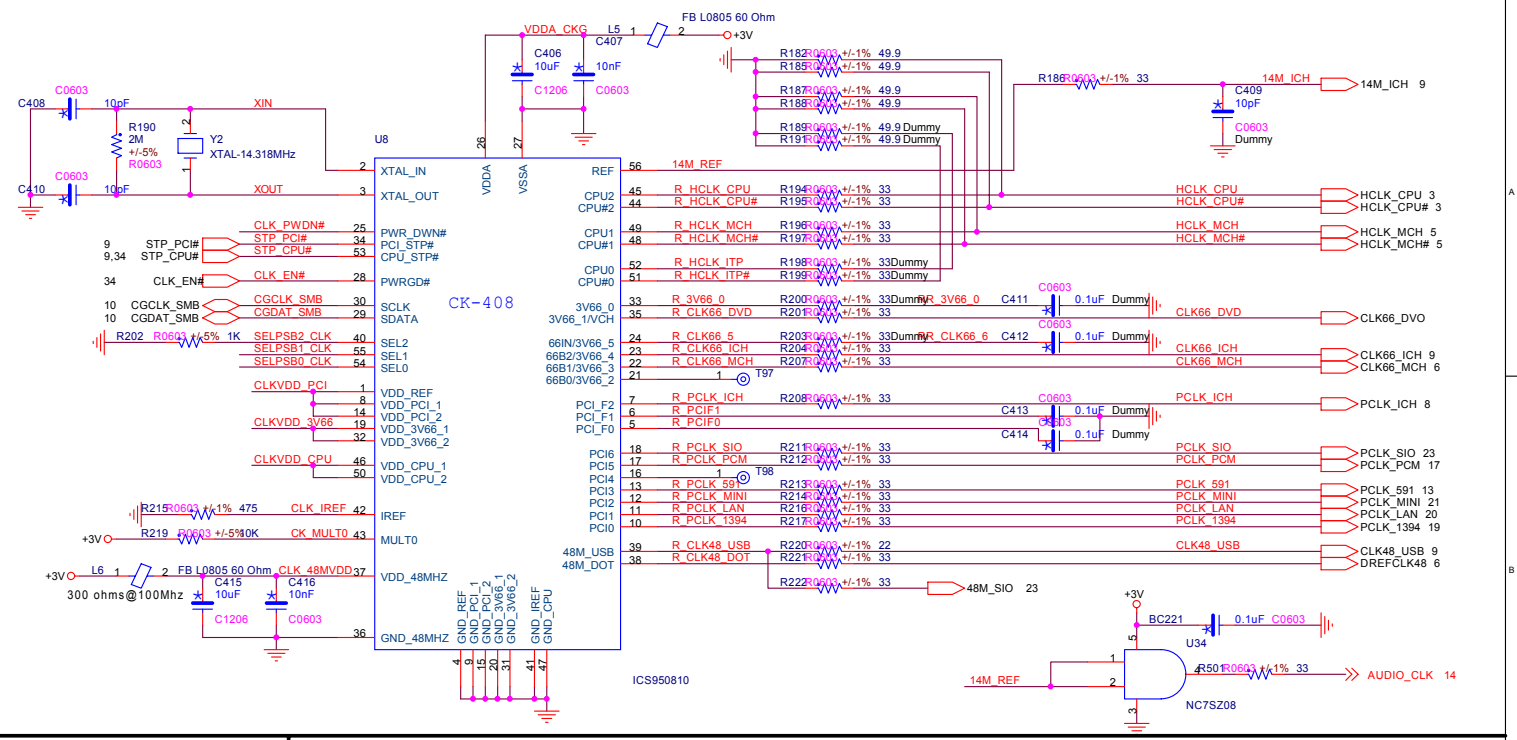
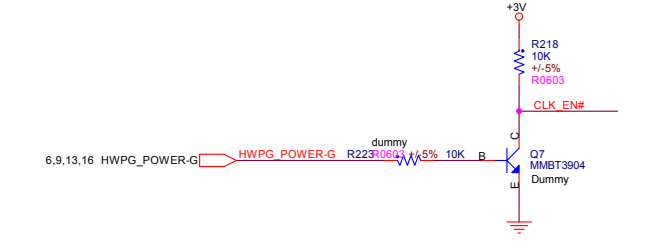
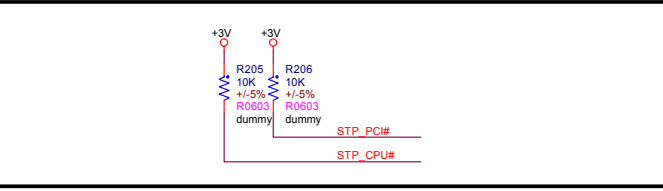
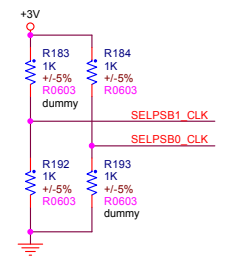
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Rev A

For terminal R-pack.

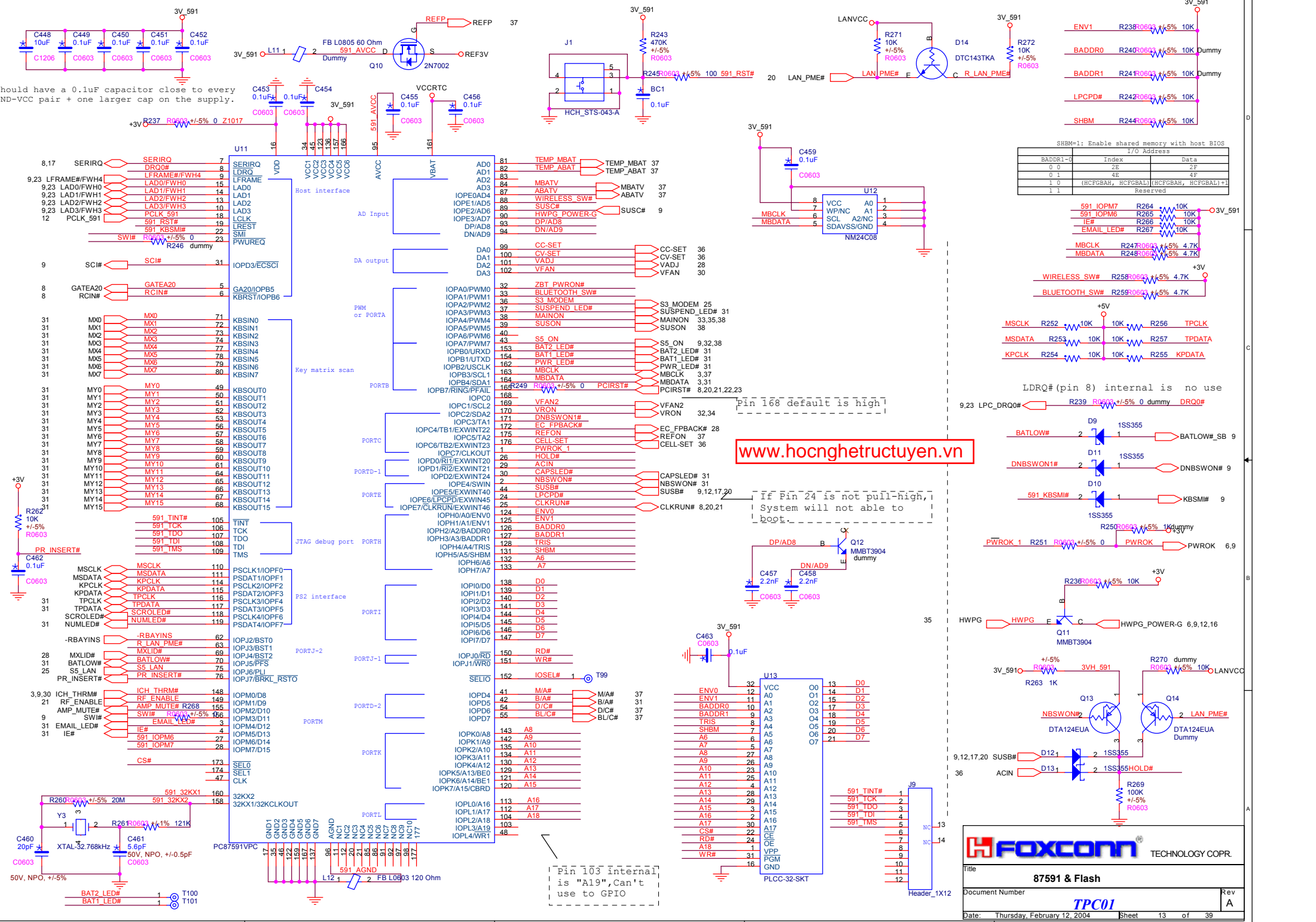
ECC

S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input



IN1	INO	Frequency	Tolerance	Mode
* 1	0	66Mhz	-1%	DS
1	1	66Mhz	+/- 1%	CS

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Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

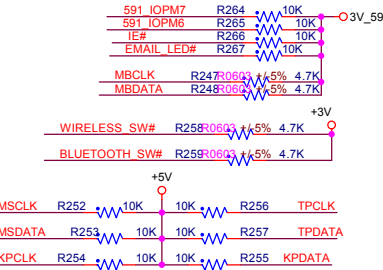
Pin 103 internal is "A19", can't use to GPIO

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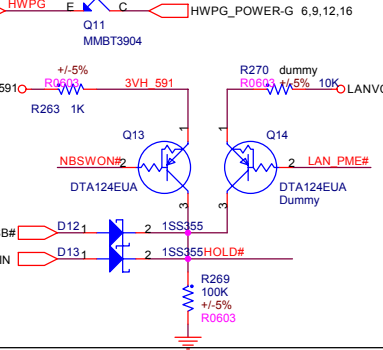
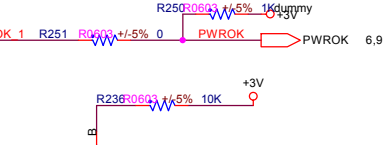
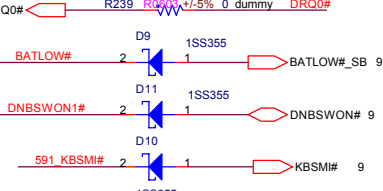
If Pin 24 is not pull-high, System will not able to boot

SHM=1: Enable shared memory with host BIOS

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAR, HCFGBAL)	(BCFGBAR, HCFGBAL)+1
1 1		Reserved



LDRQ# (pin 8) internal is no use



FOXCONN TECHNOLOGY CORP.

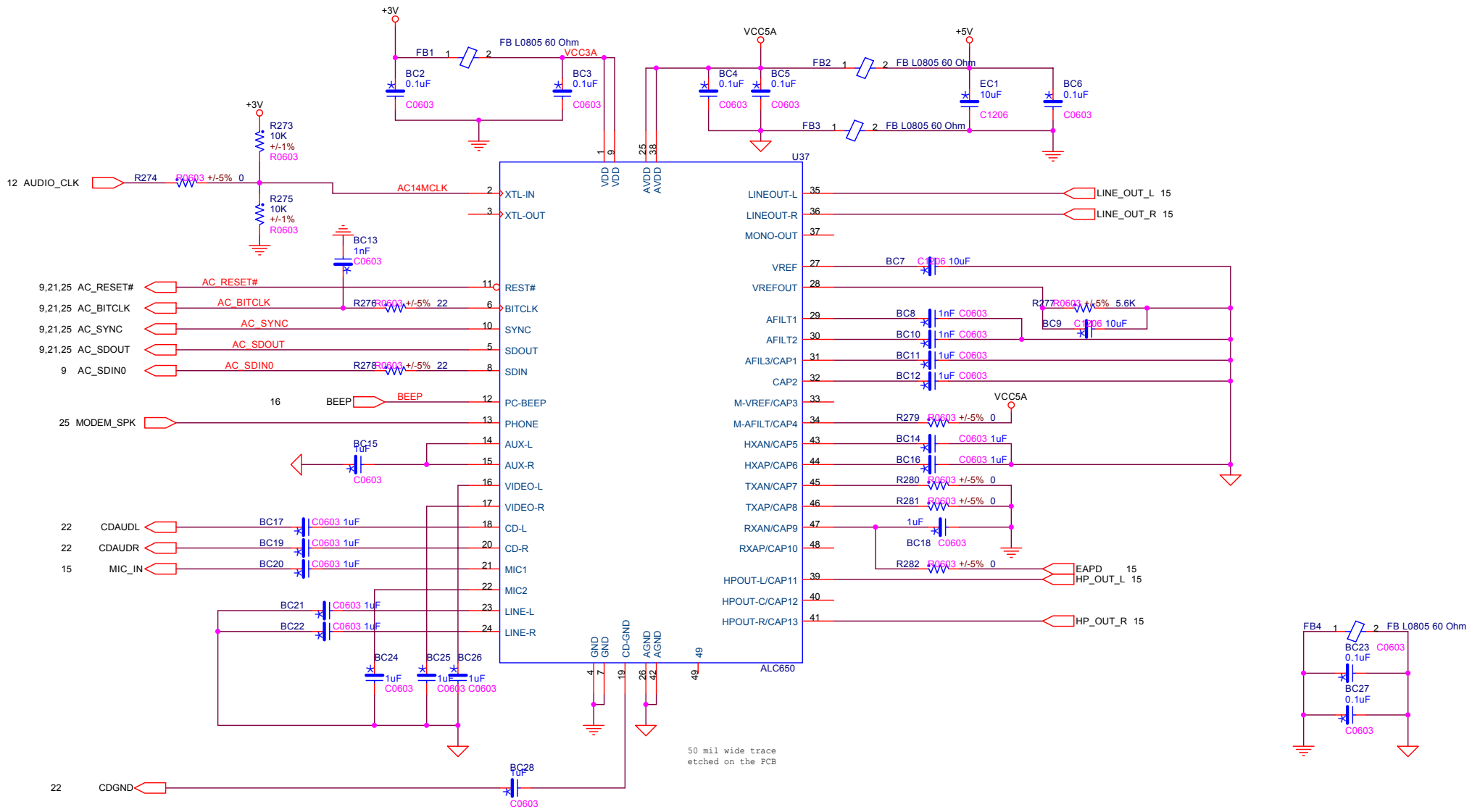
Title: **87591 & Flash**

Document Number: **TPC01**

Date: Thursday, February 12, 2004

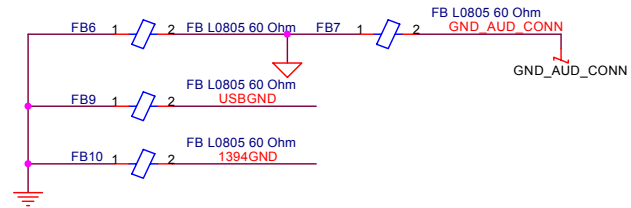
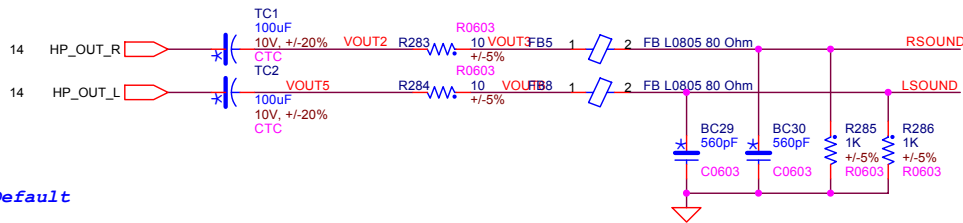
Sheet 13 of 39

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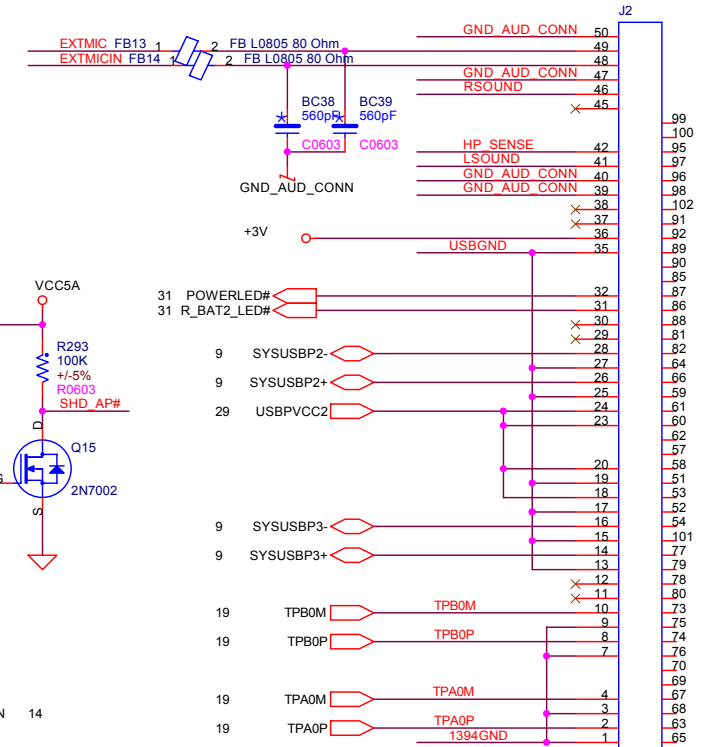
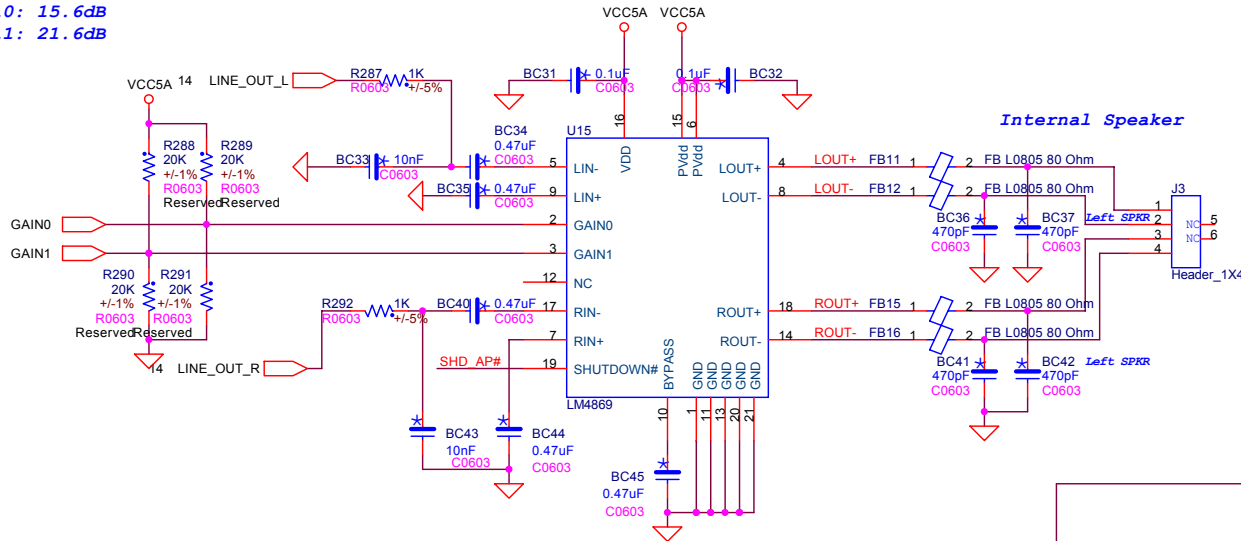


50 mil wide trace etched on the PCB

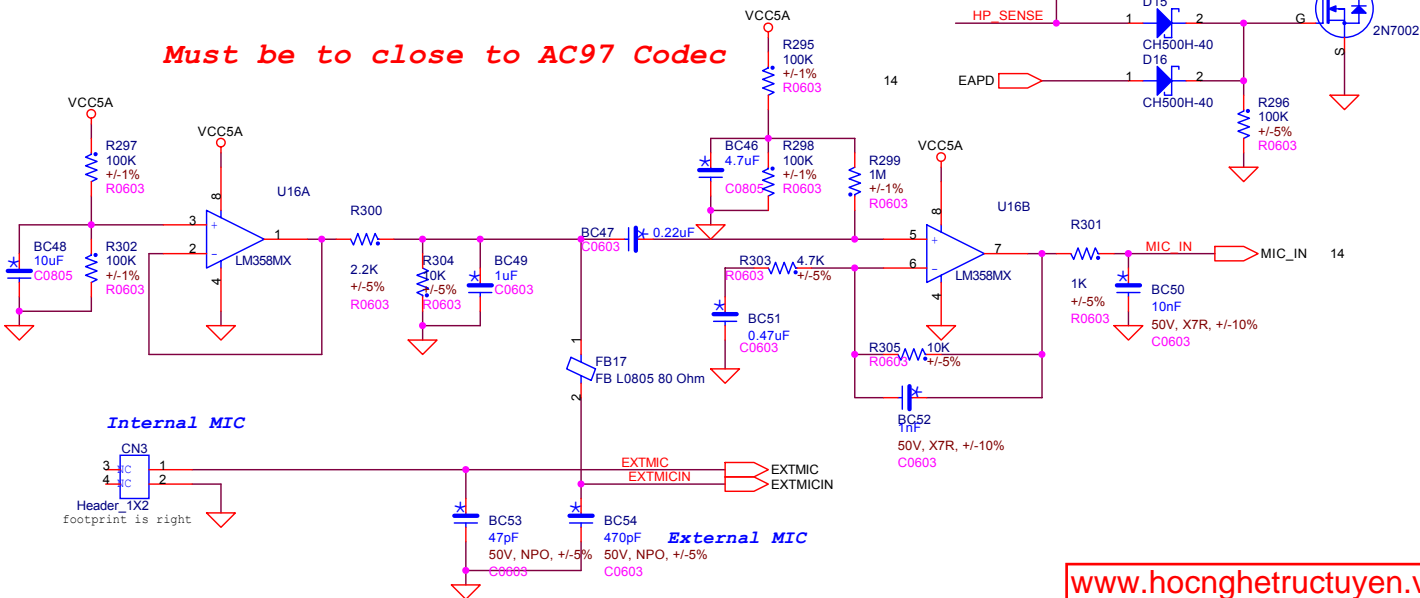
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Gain0, Gain1:
 00: 6dB (Av=2) <= Default
 01: 10dB
 10: 15.6dB
 11: 21.6dB



Must be to close to AC97 Codec



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FOXCONN TECHNOLOGY COPR.

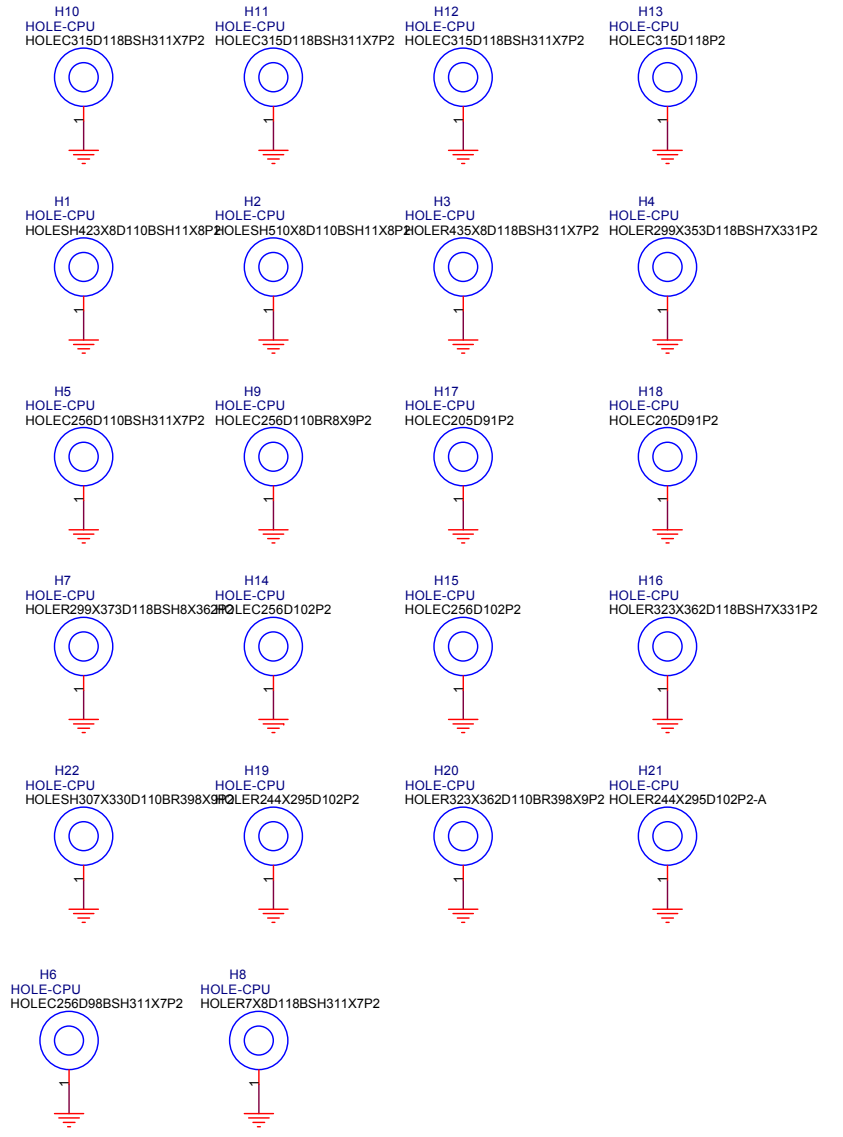
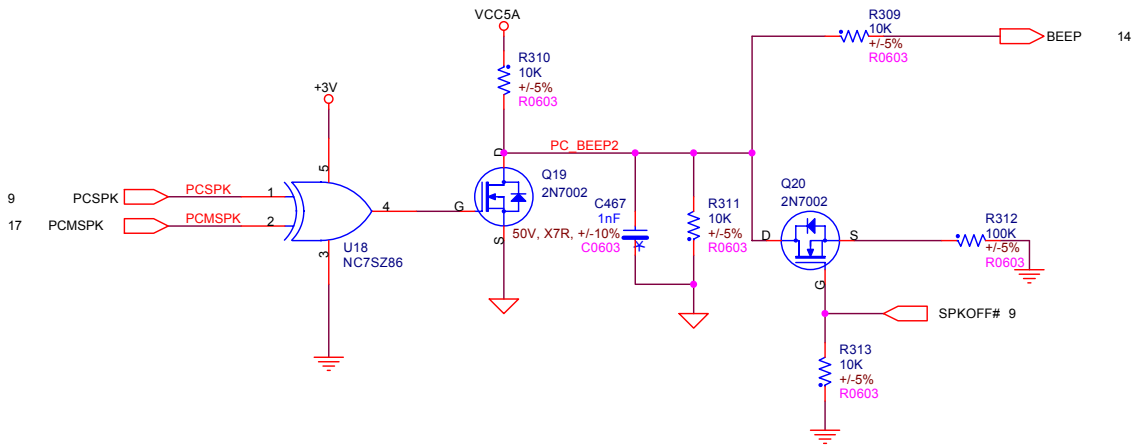
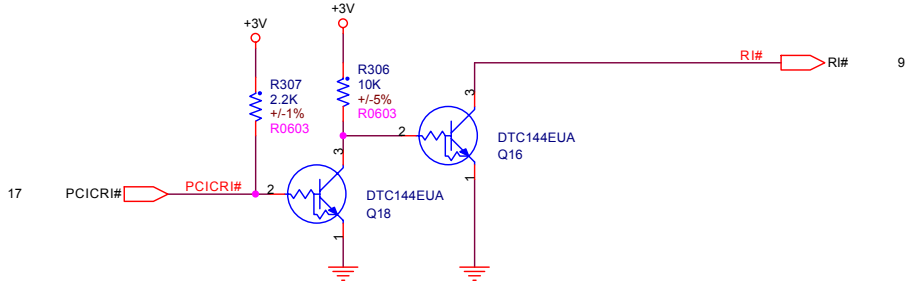
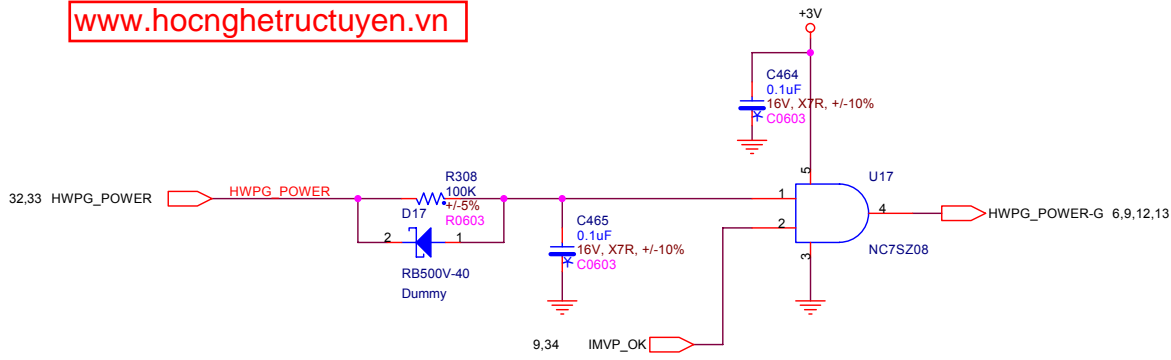
Title: **Audio MDC**

Document Number: **TPC01**

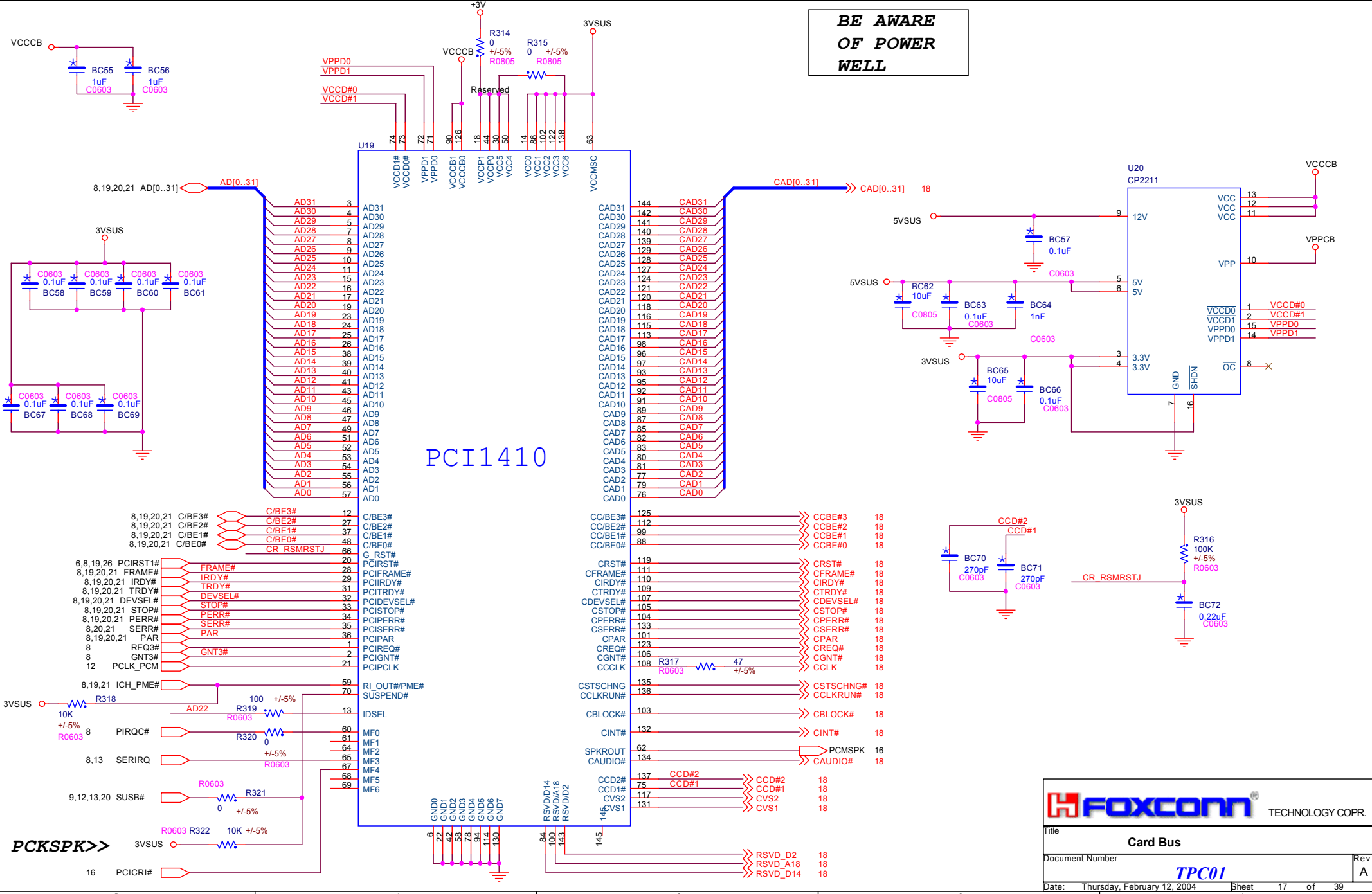
Date: Thursday, February 12, 2004

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**BE AWARE
OF POWER
WELL**



FOXCONN TECHNOLOGY CORP.

Title: **Card Bus**

Document Number: **TPC01**

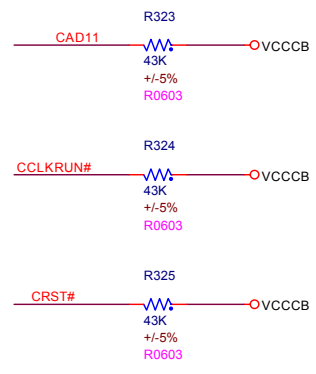
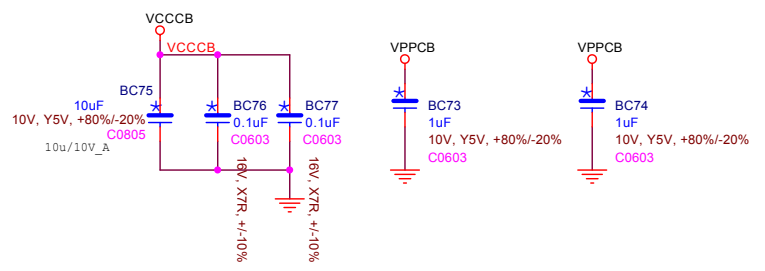
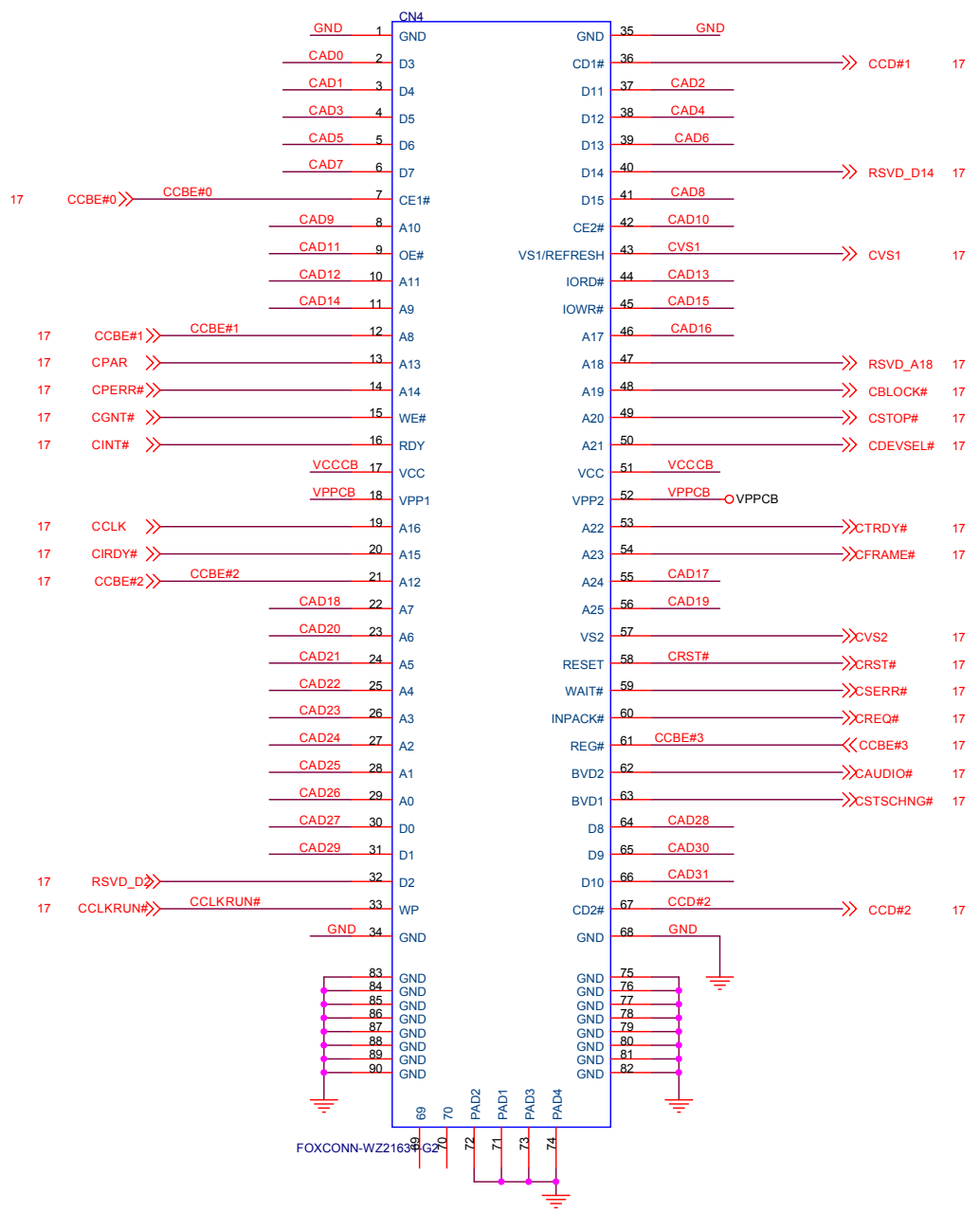
Date: Thursday, February 12, 2004

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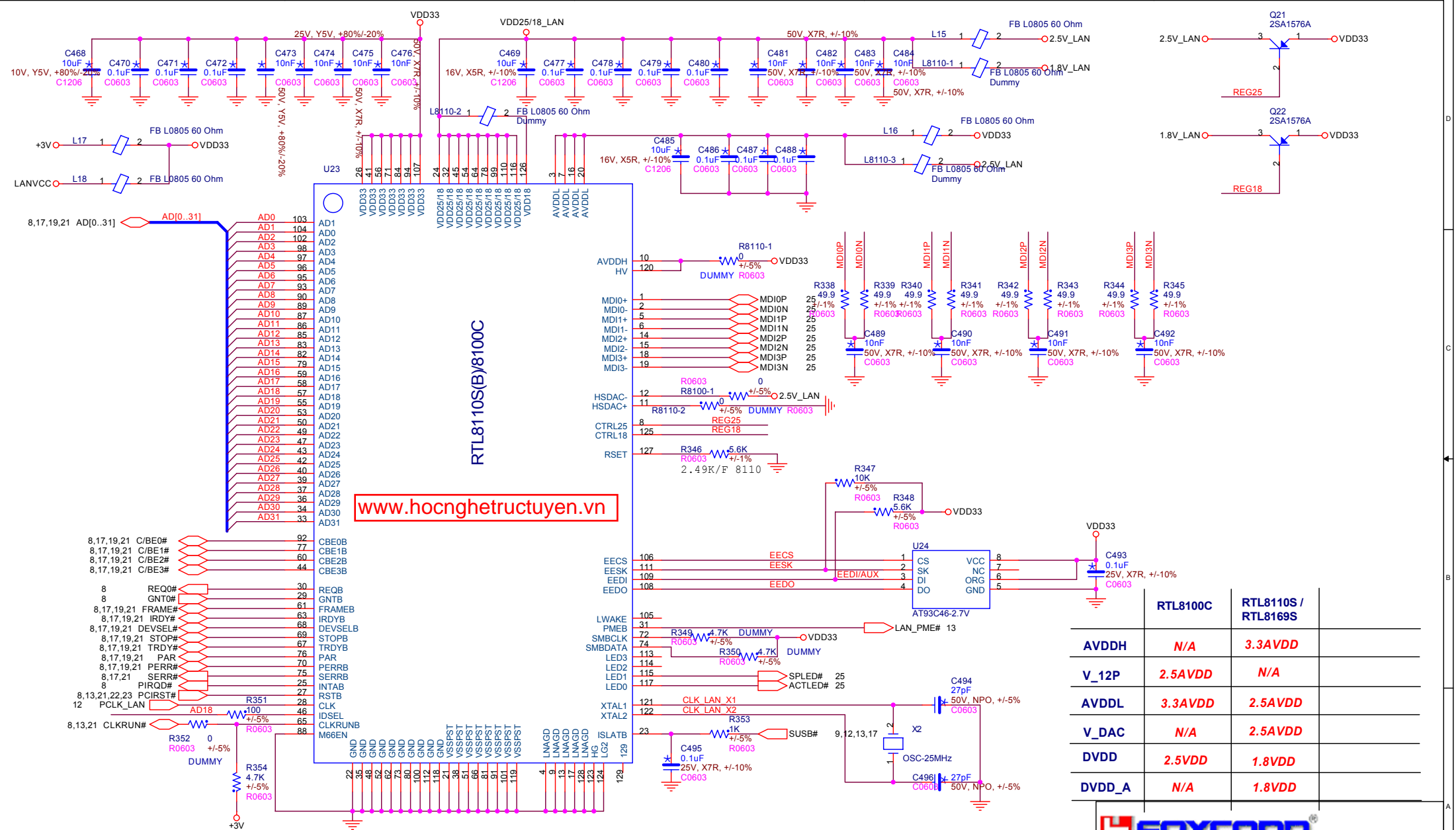
Rev: **A**

PCMCIA SLOT

CAD[0..31] << CAD[0..31] 17



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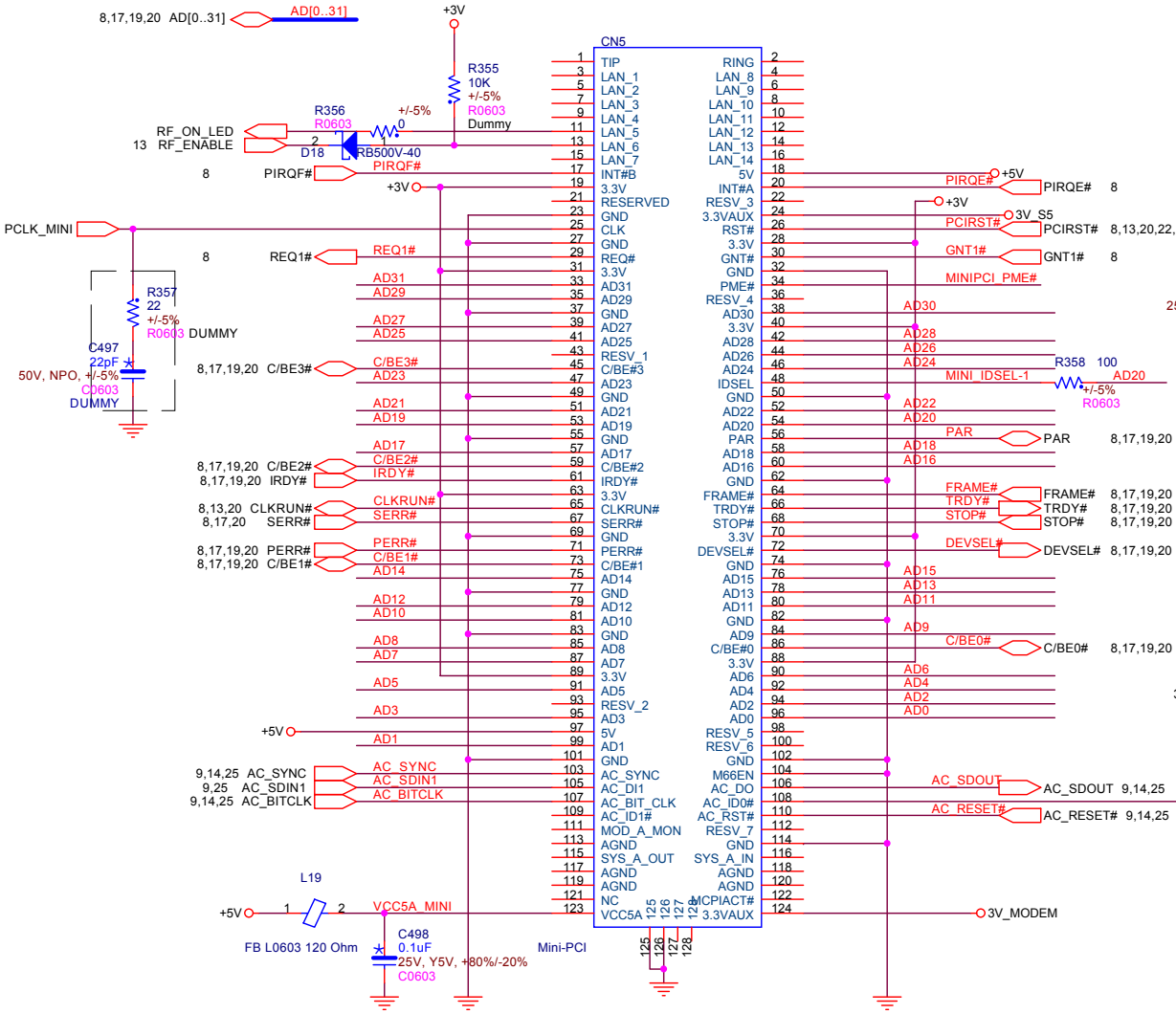


	RTL8100C	RTL8110S / RTL8169S
AVDDH	N/A	3.3AVDD
V_12P	2.5AVDD	N/A
AVDDL	3.3AVDD	2.5AVDD
V_DAC	N/A	2.5AVDD
DVDD	2.5VDD	1.8VDD
DVDD_A	N/A	1.8VDD

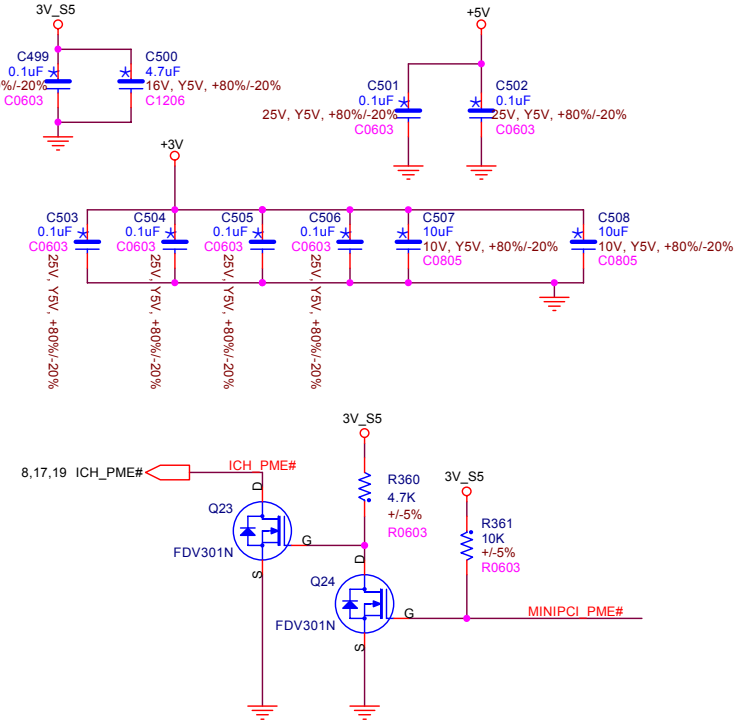


Title		RTL8100
Document Number		TPC01
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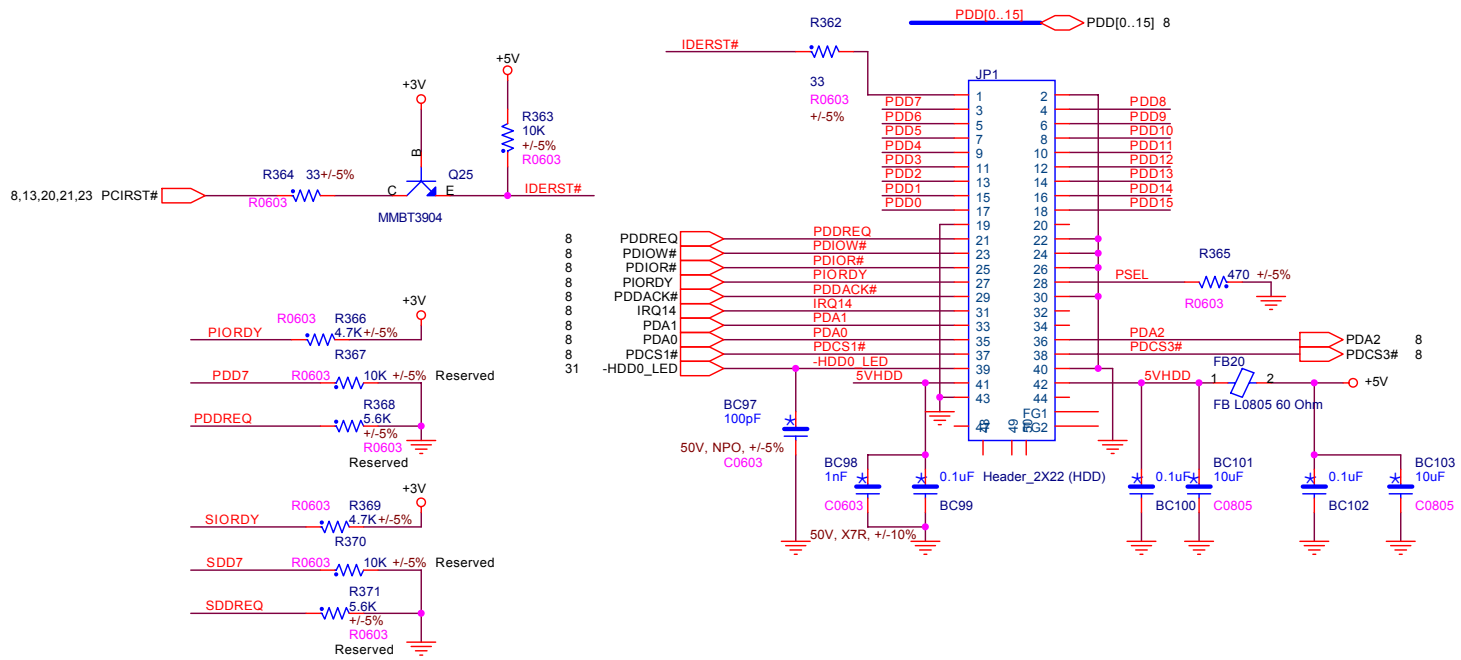
ID Select : AD20
Interrupt Pin : PIRQE# , PIRQF#
Request indicates : REQ1#
Grant indicates : GNT1#



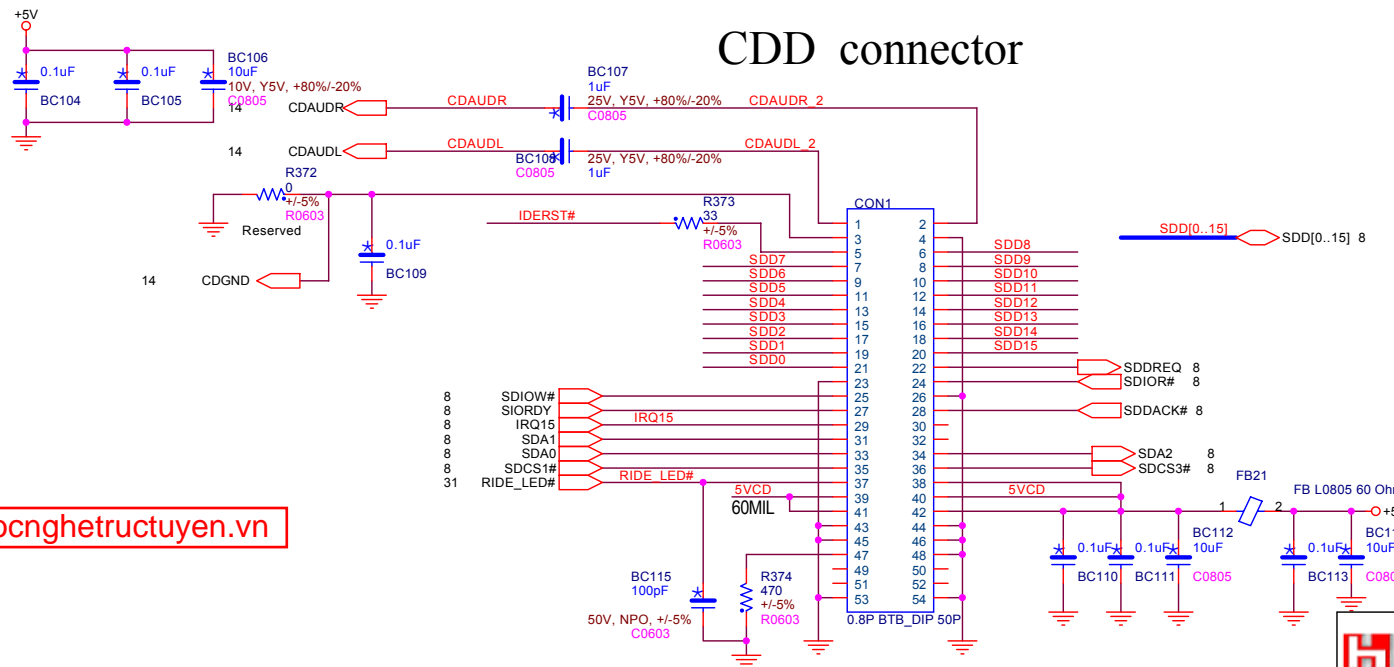
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Title MINI PCI	
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HDD connector

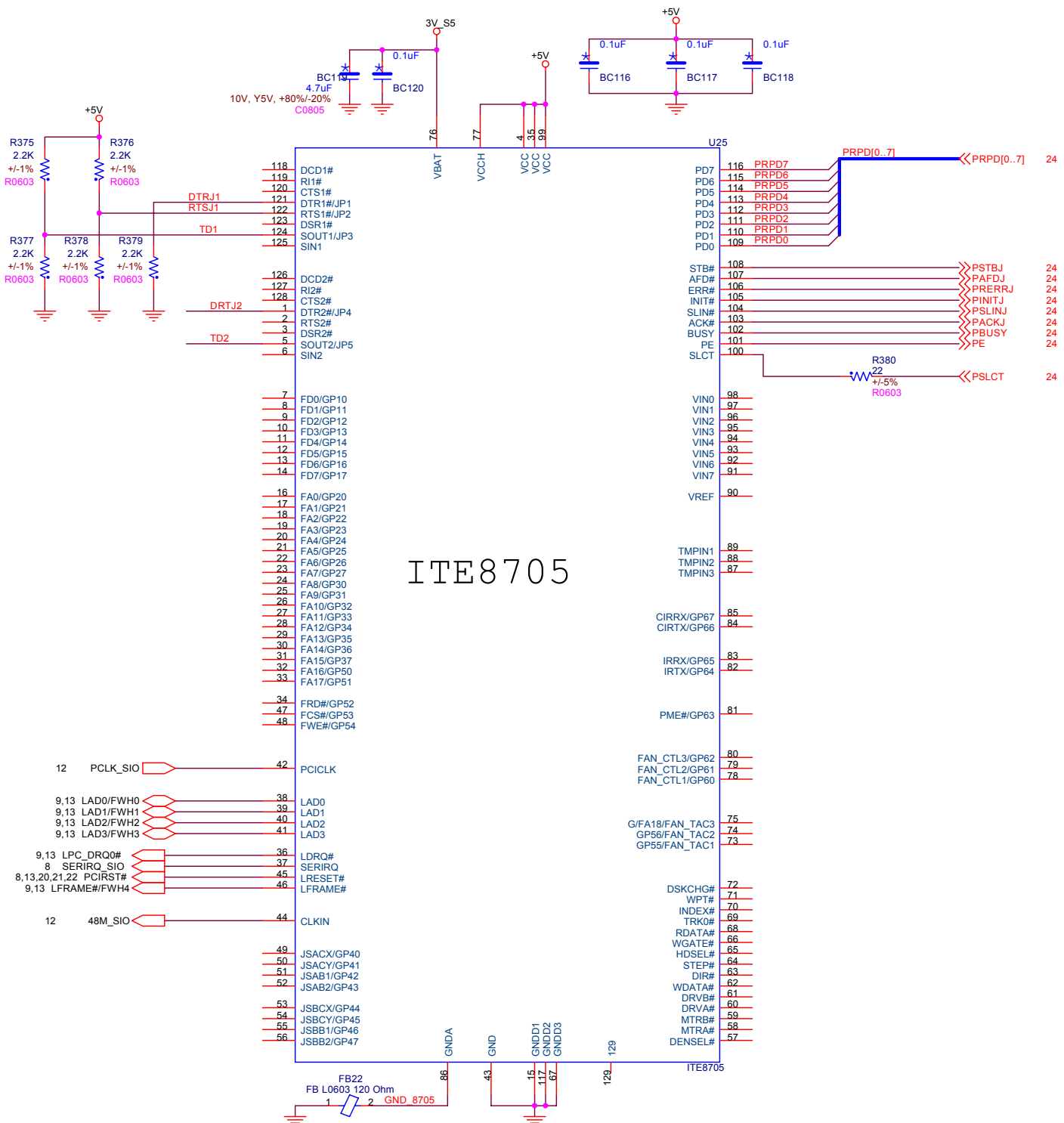


CDD connector



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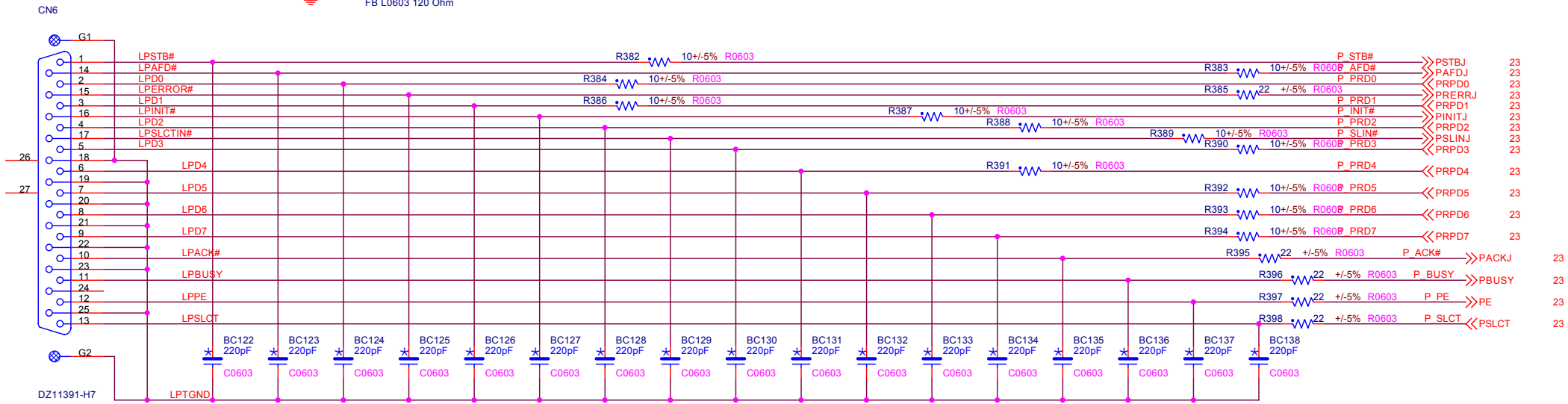
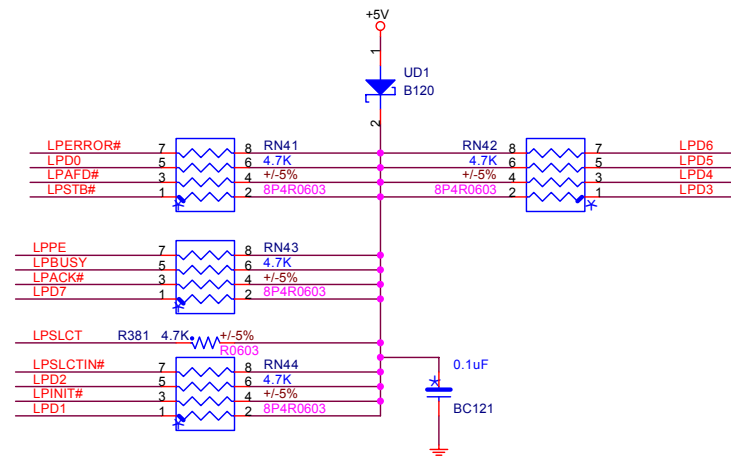
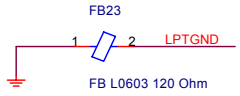




ITE8705

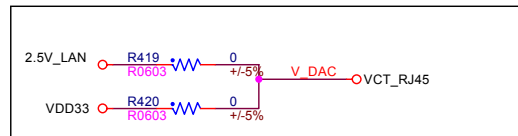
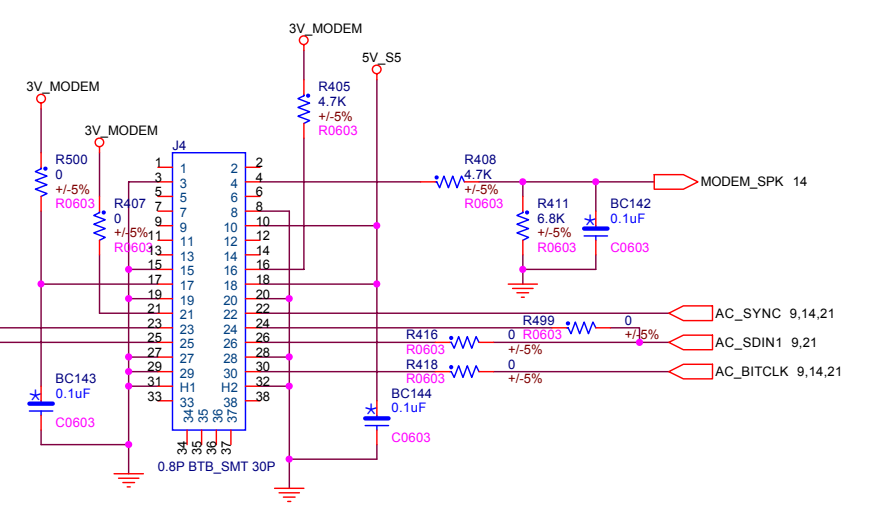
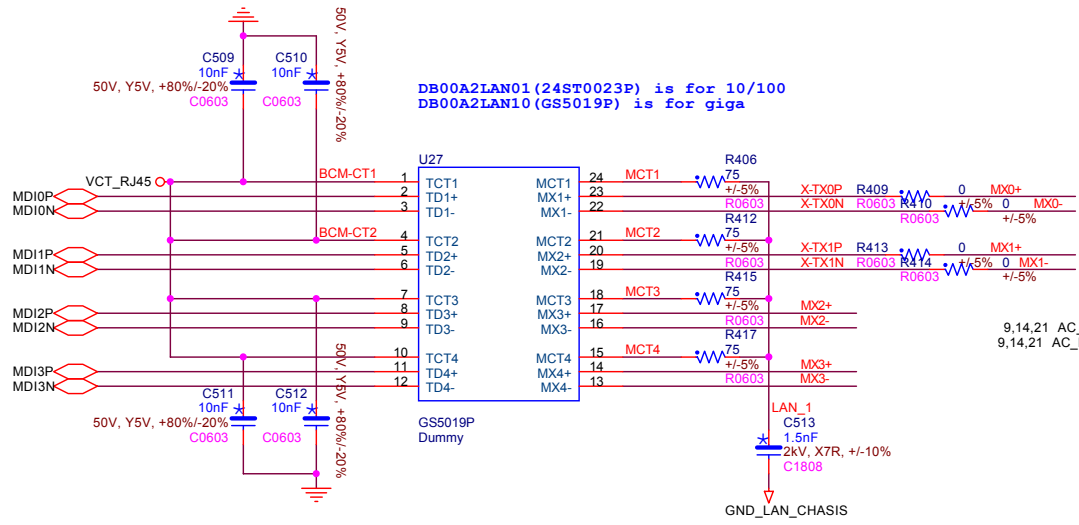
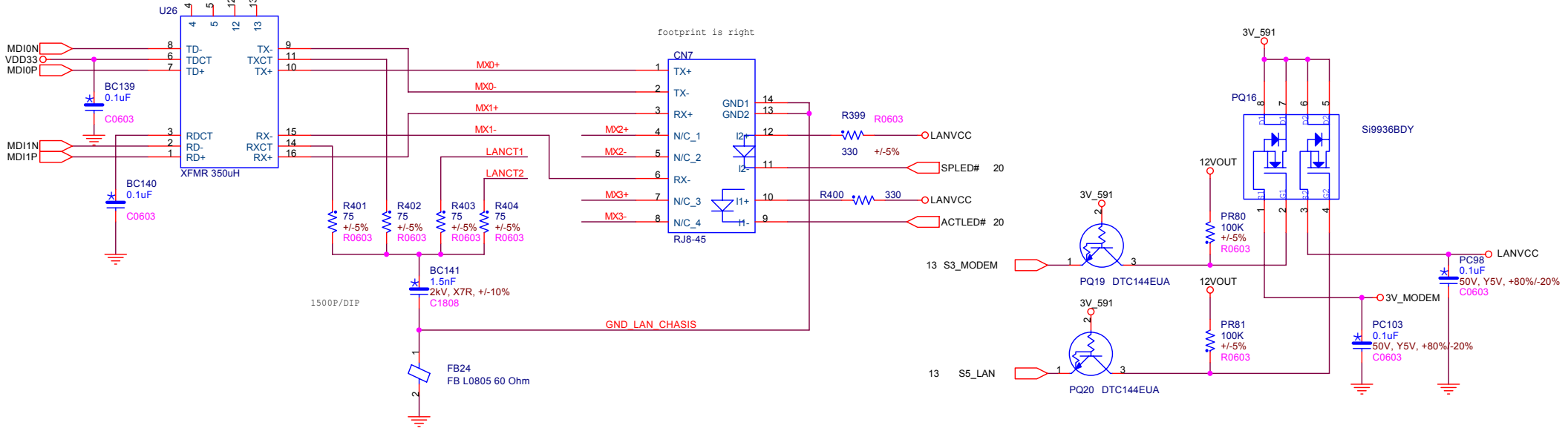
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CIS NEED UPDATE

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Title PRT	
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FOXCONN TECHNOLOGY CORP.

Title: LAN PHY.RJ45 & MDC

Document Number: TPC01

Date: Thursday, February 12, 2004

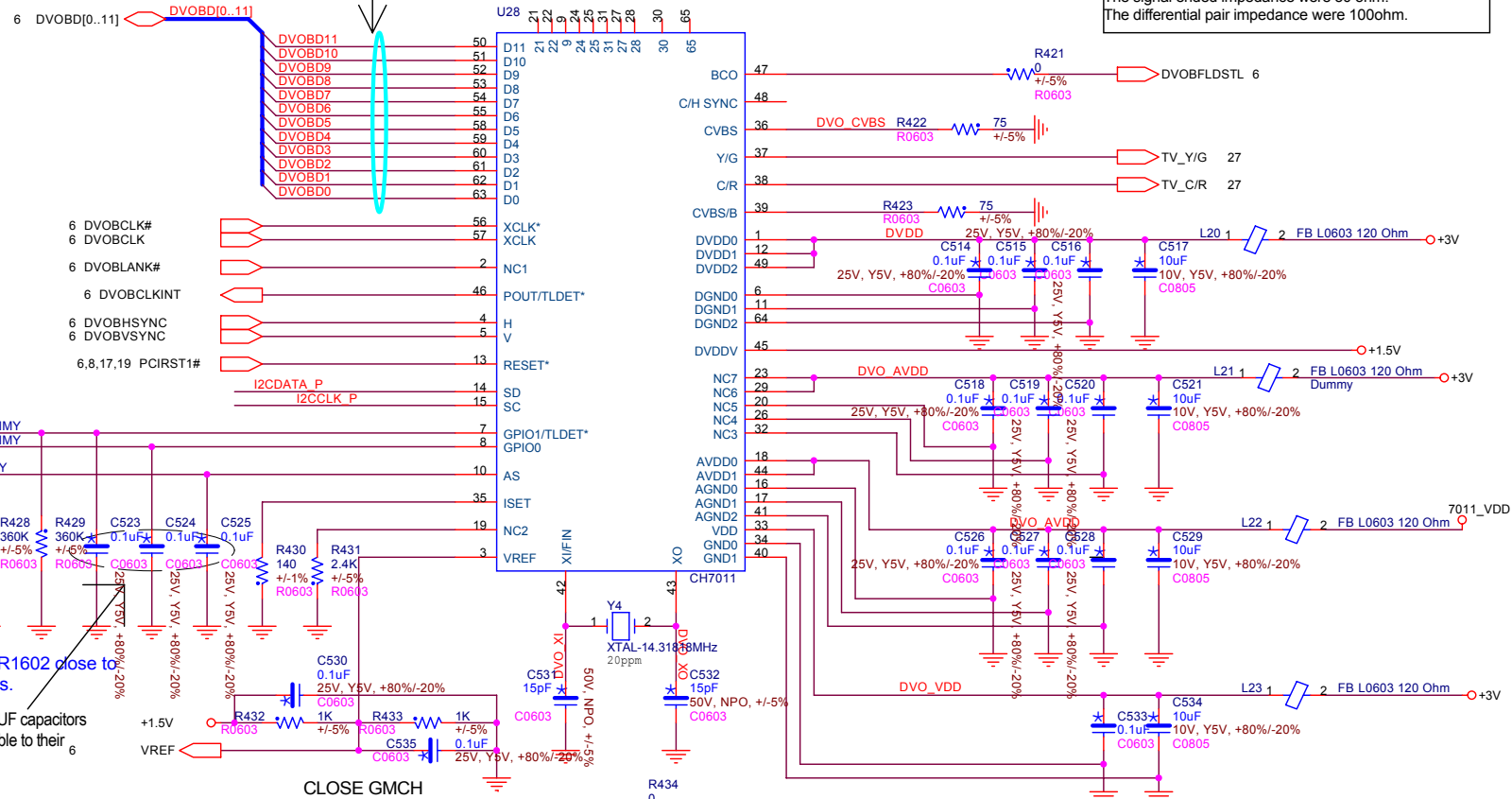
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Please use 8 mil traces to route those signal.

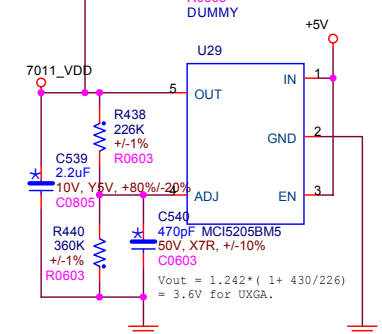
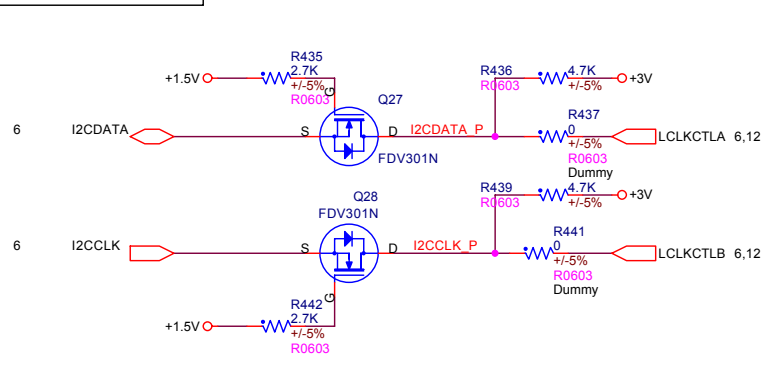
CH7009 =TV+DVI
CH7011 =TV

These trace used 12 mil wide & 12 mil spacing.
Please kept as closed to the same as possible.
The maximum length difference must not exceed 100 mil.
The corner angle kept from 4 to 45 degree.
The signal ended impedance were 50 ohm.
The differential pair impedance were 100ohm.



Place R1601,R1602 close to respective pins.
Placed all of 0.1uF capacitors as close as possible to their respective pins

CLOSE GMCH



DVOBCLK#	66MHz
DVOBCLK	66MHz
DVOBLANK#	56KHz
DVOBCLKINT	66MHz
DVOBHSYNC	56KHz
DVOBVSYSNC	60Hz

FOXCONN TECHNOLOGY COPR.

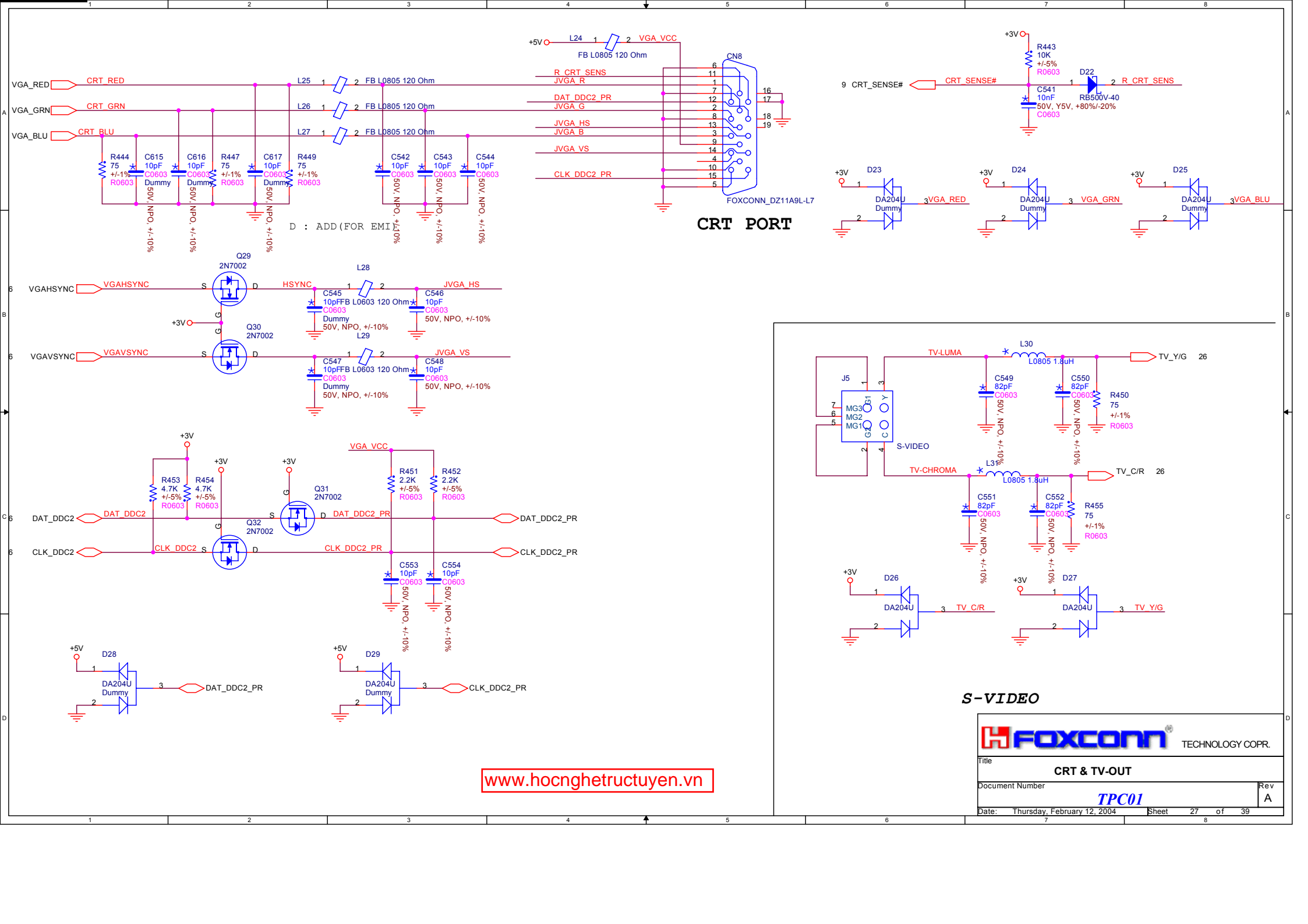
Title: **TV Encoder**

Document Number: **TPC01**

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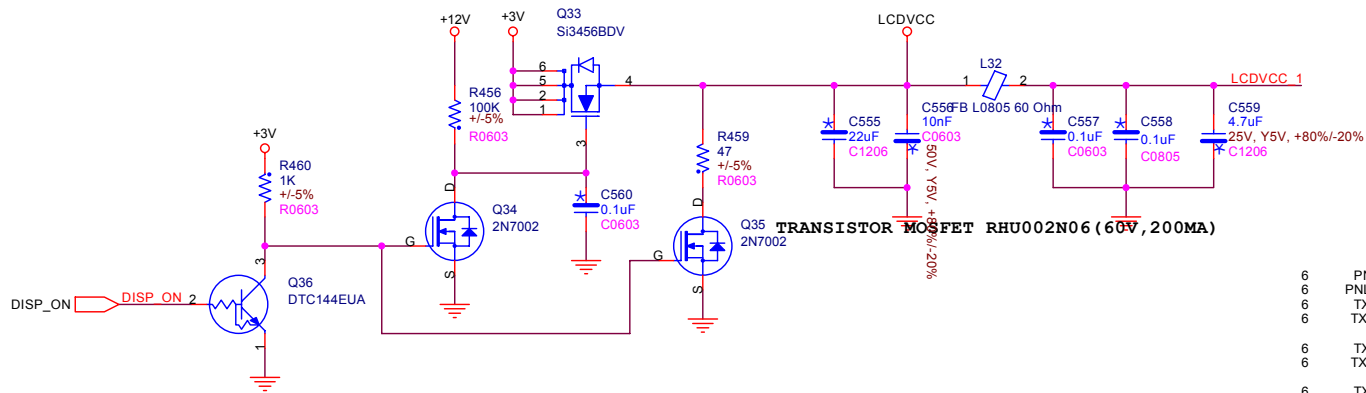
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S-VIDEO

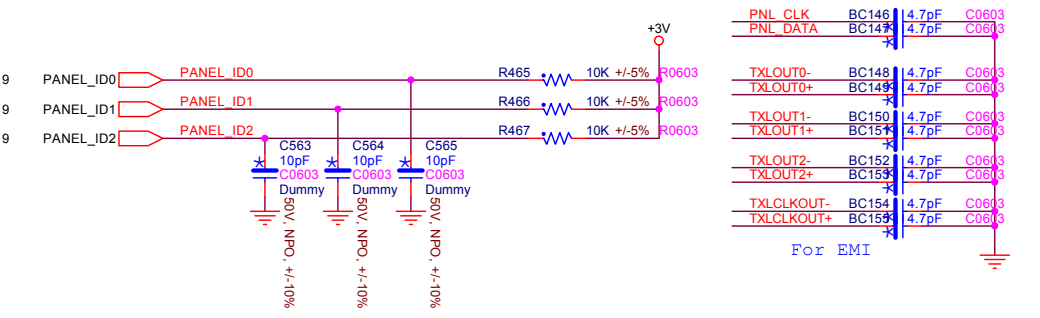
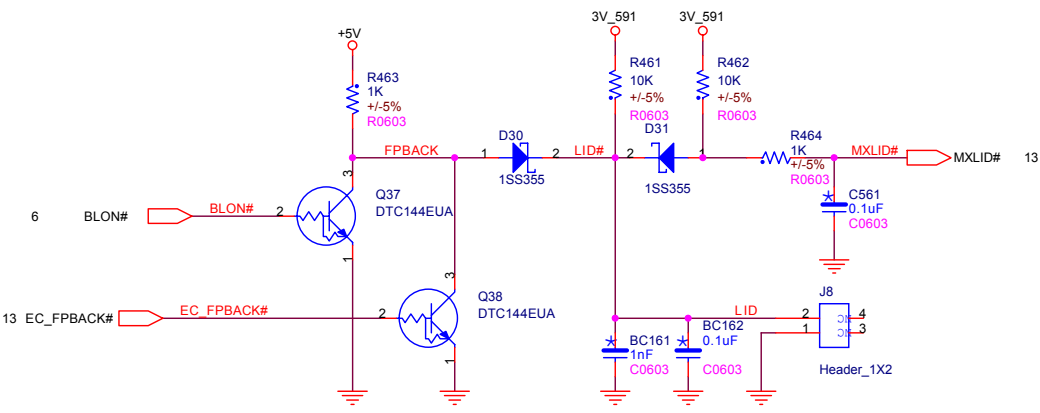
FOXCONN TECHNOLOGY CORP.

Title		CRT & TV-OUT	
Document Number		TPC01	
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FILTER FBM2125 HM330-T (4A, 0.015)

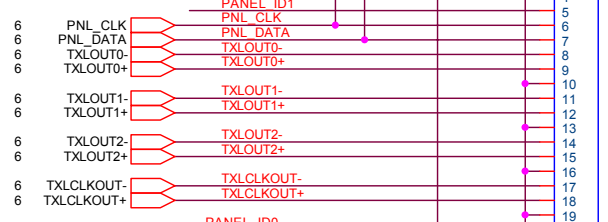
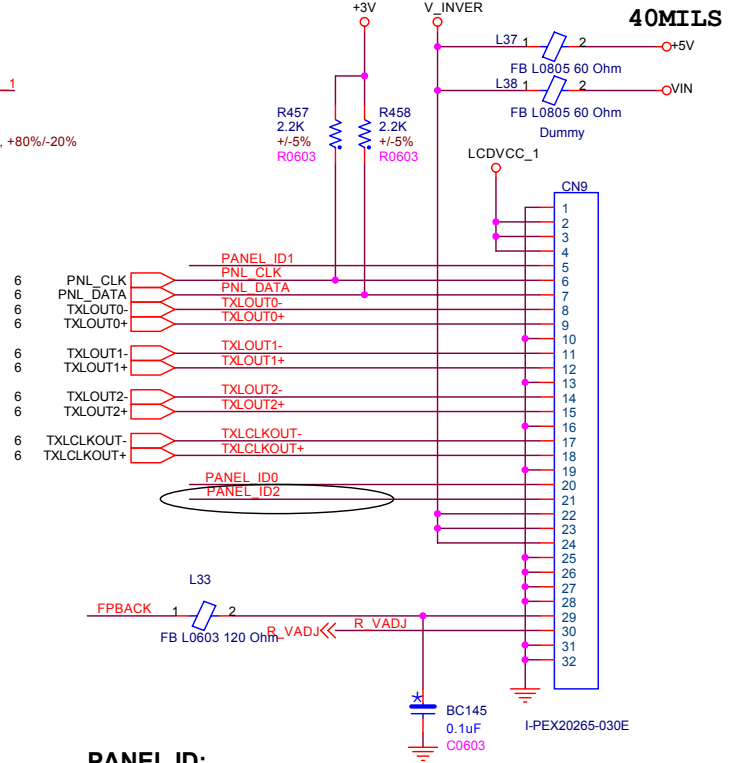


TRANSISTOR MOSFET RHM002N06 (60V, 200MA)



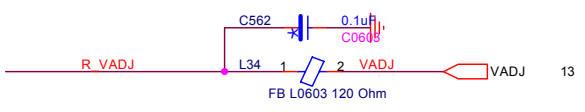
PANEL_CLK	BC146	4.7pF	C0603
PANEL_DATA	BC147	4.7pF	C0603
TXLOUT0-	BC148	4.7pF	C0603
TXLOUT0+	BC149	4.7pF	C0603
TXLOUT1-	BC150	4.7pF	C0603
TXLOUT1+	BC151	4.7pF	C0603
TXLOUT2-	BC152	4.7pF	C0603
TXLOUT2+	BC153	4.7pF	C0603
TXLCLKOUT-	BC154	4.7pF	C0603
TXLCLKOUT+	BC155	4.7pF	C0603

For EMI



PANEL ID:

	PANEL_ID2	PANEL_ID1	PANEL_ID0
D3	0	1	1
D4	1	0	0
D5	1	0	1
D6	1	1	0
D7	1	1	1



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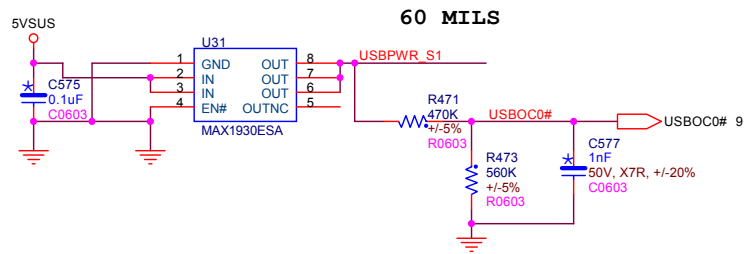
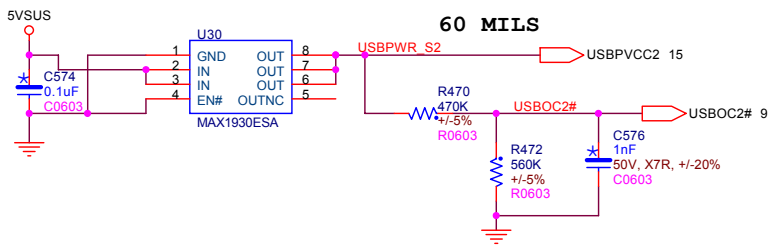
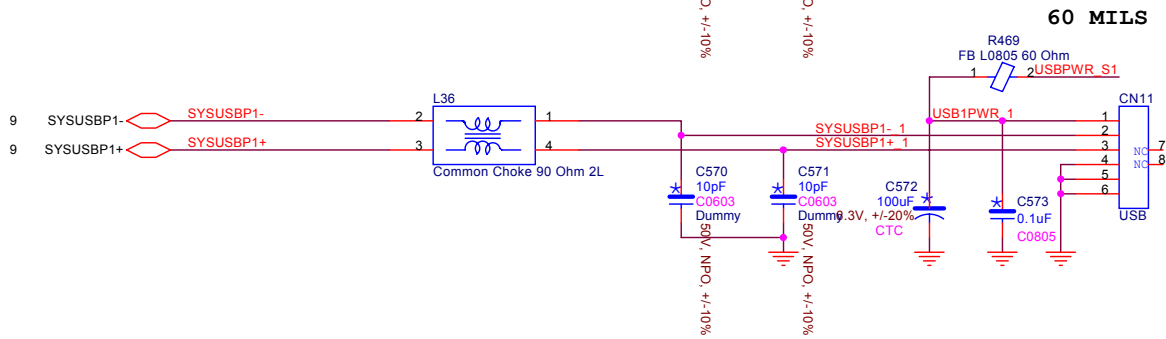
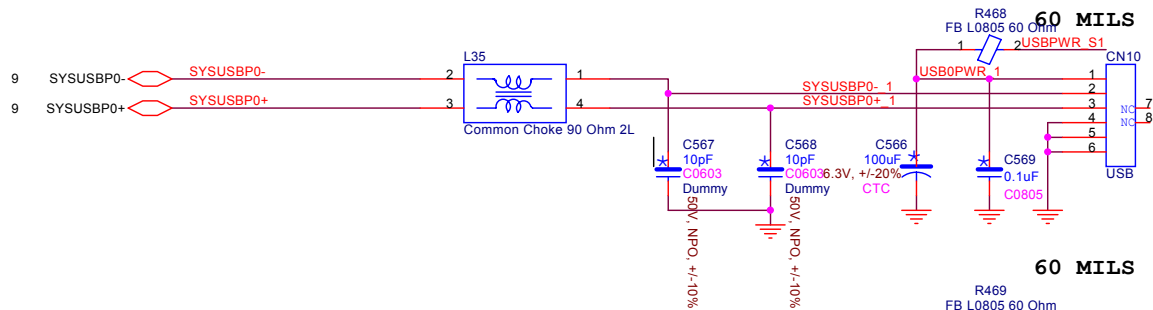
FOXCONN TECHNOLOGY CORP.

Title: **LCD CKTS & CONN.**

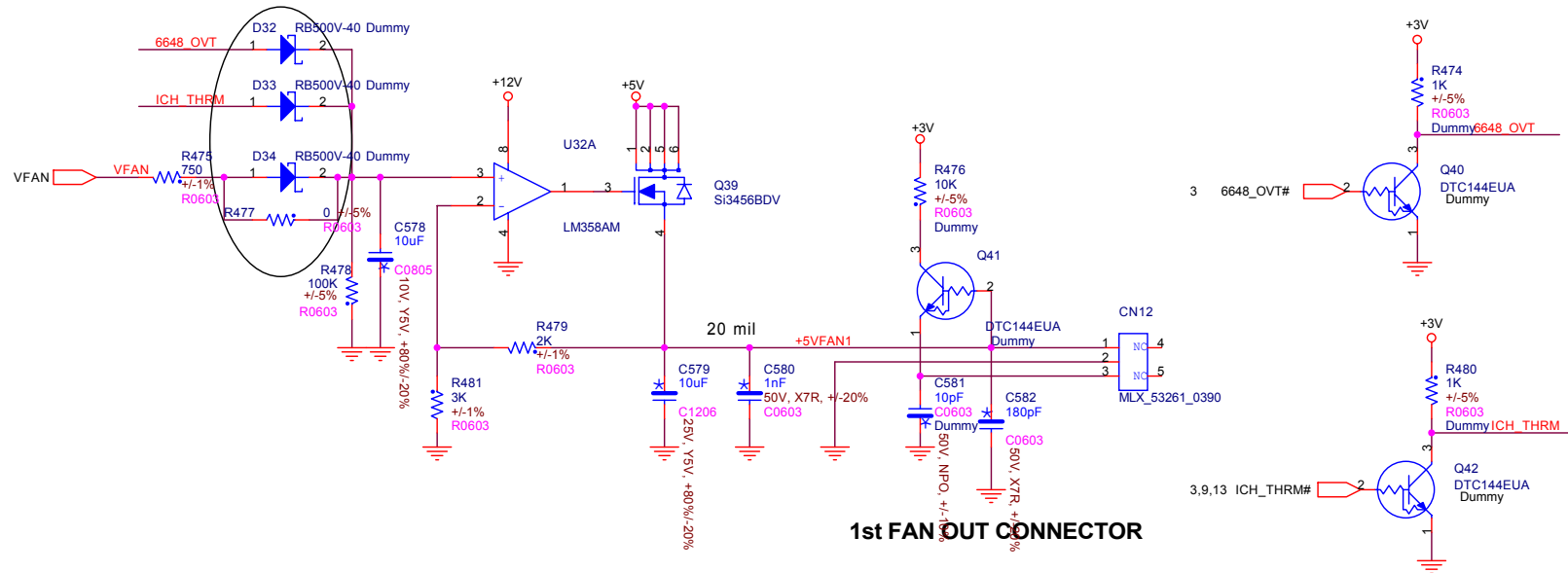
Document Number: **TPC01**

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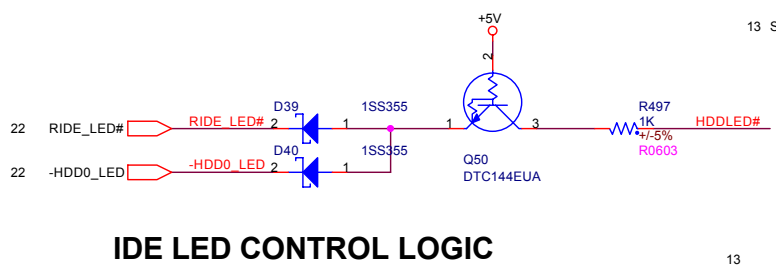
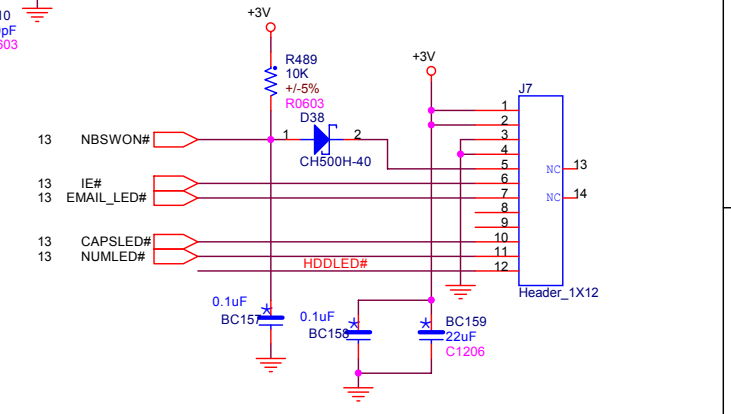
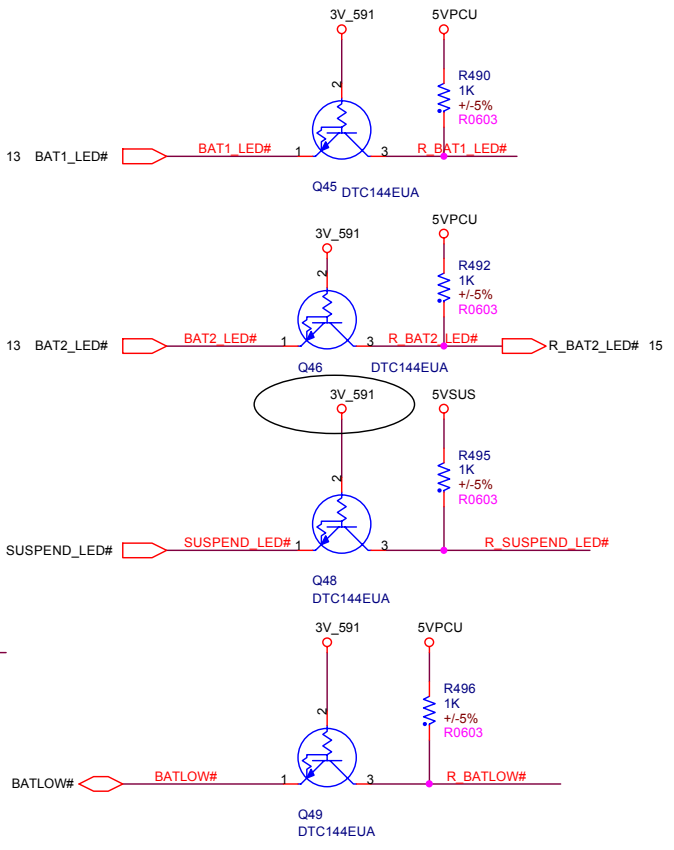
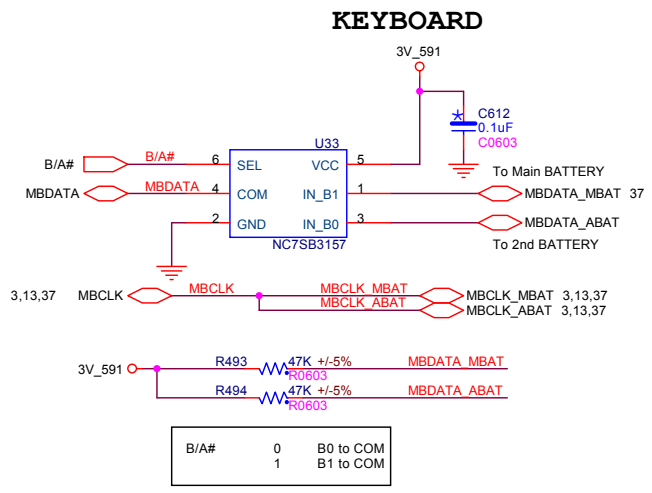
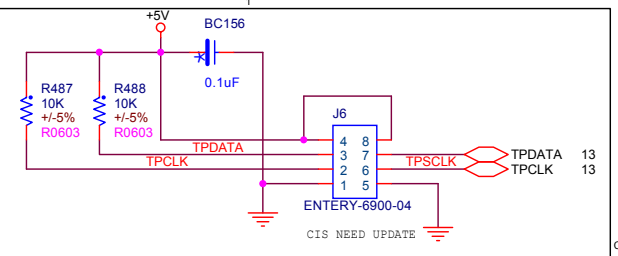
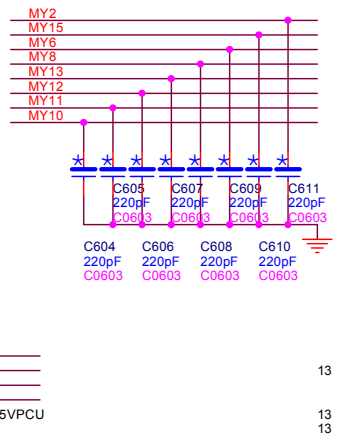
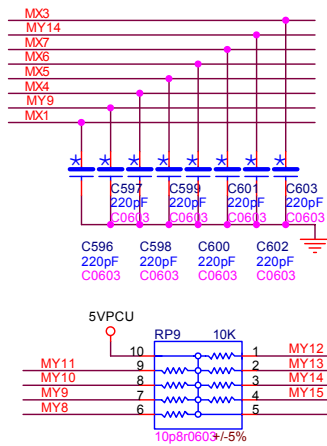
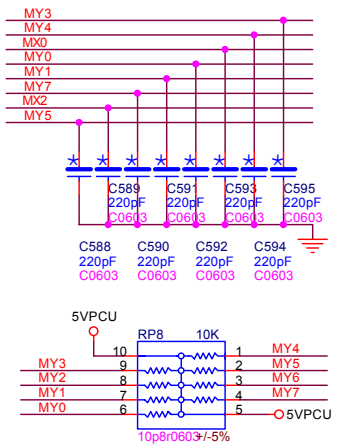
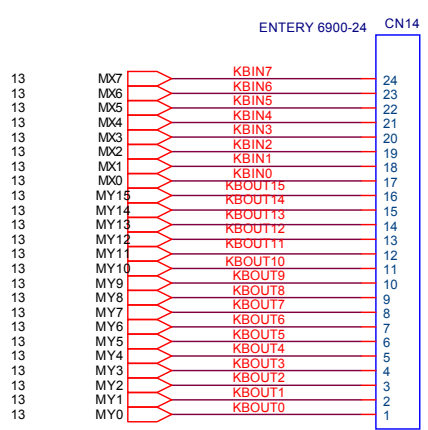


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1st FAN OUT CONNECTOR

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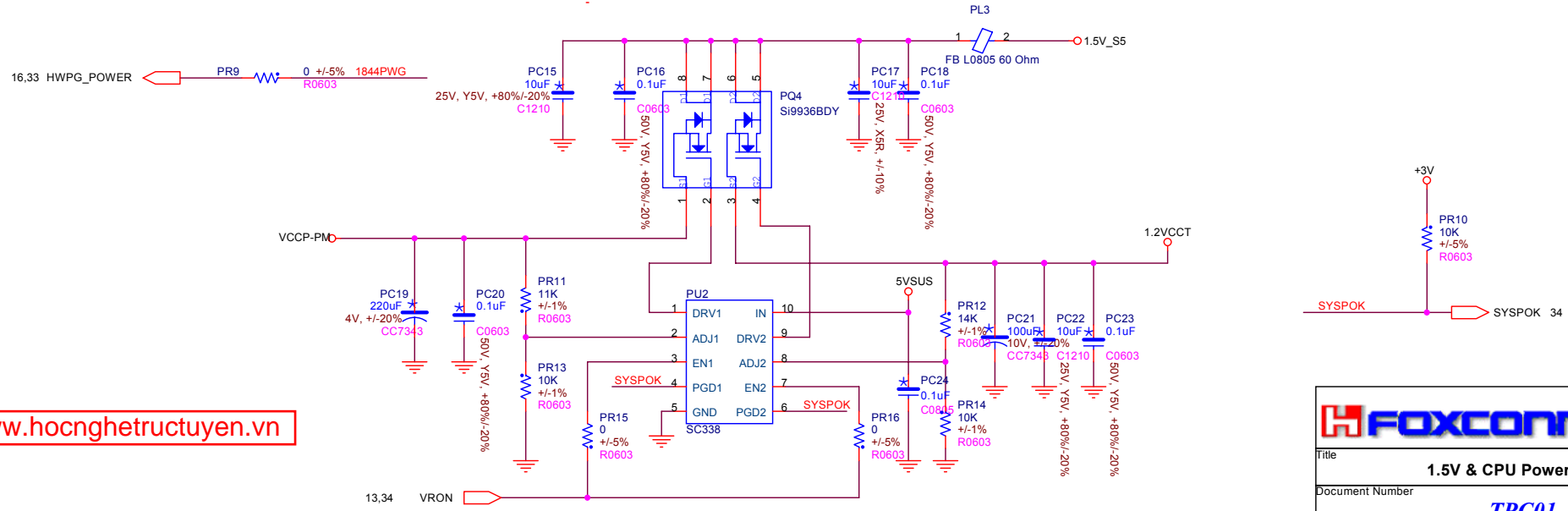
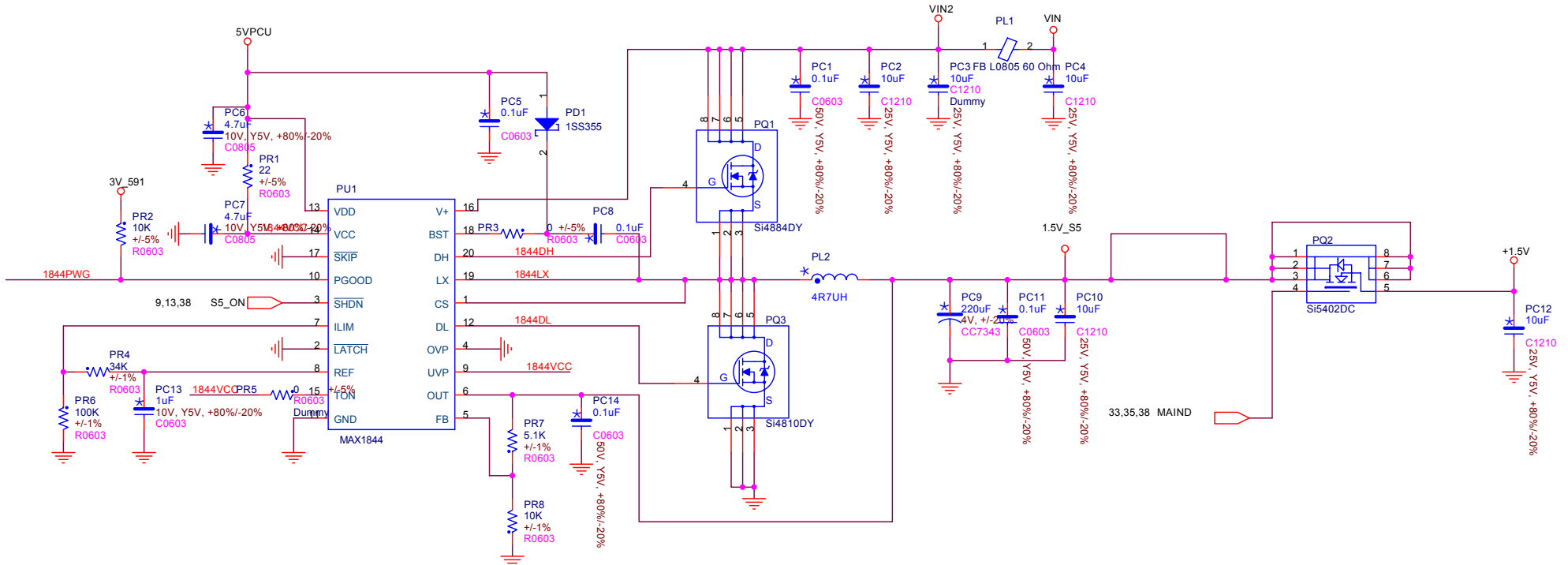
FOXCONN TECHNOLOGY CORP.

Title: **KB TP LED**

Document Number: **TPC01**

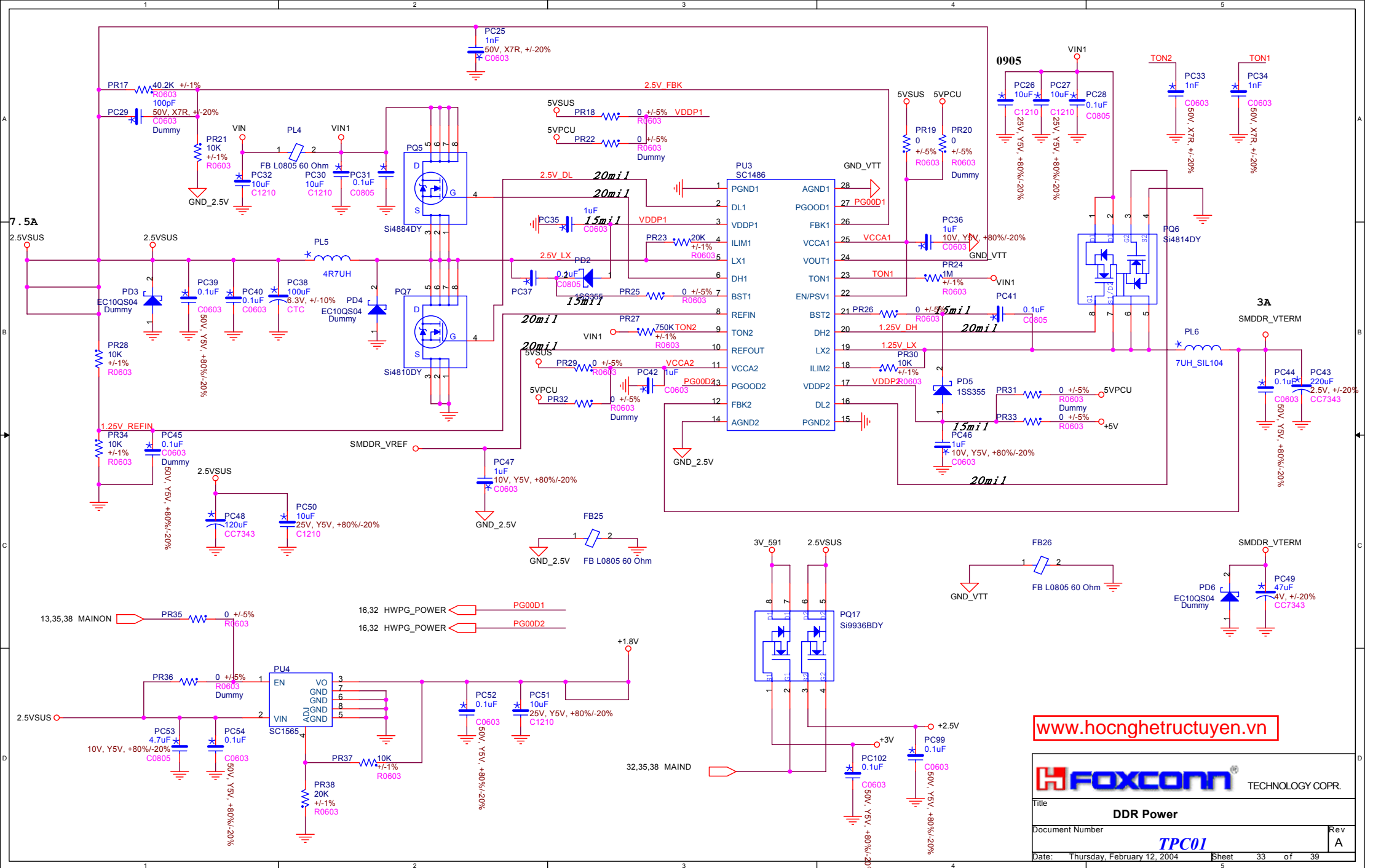
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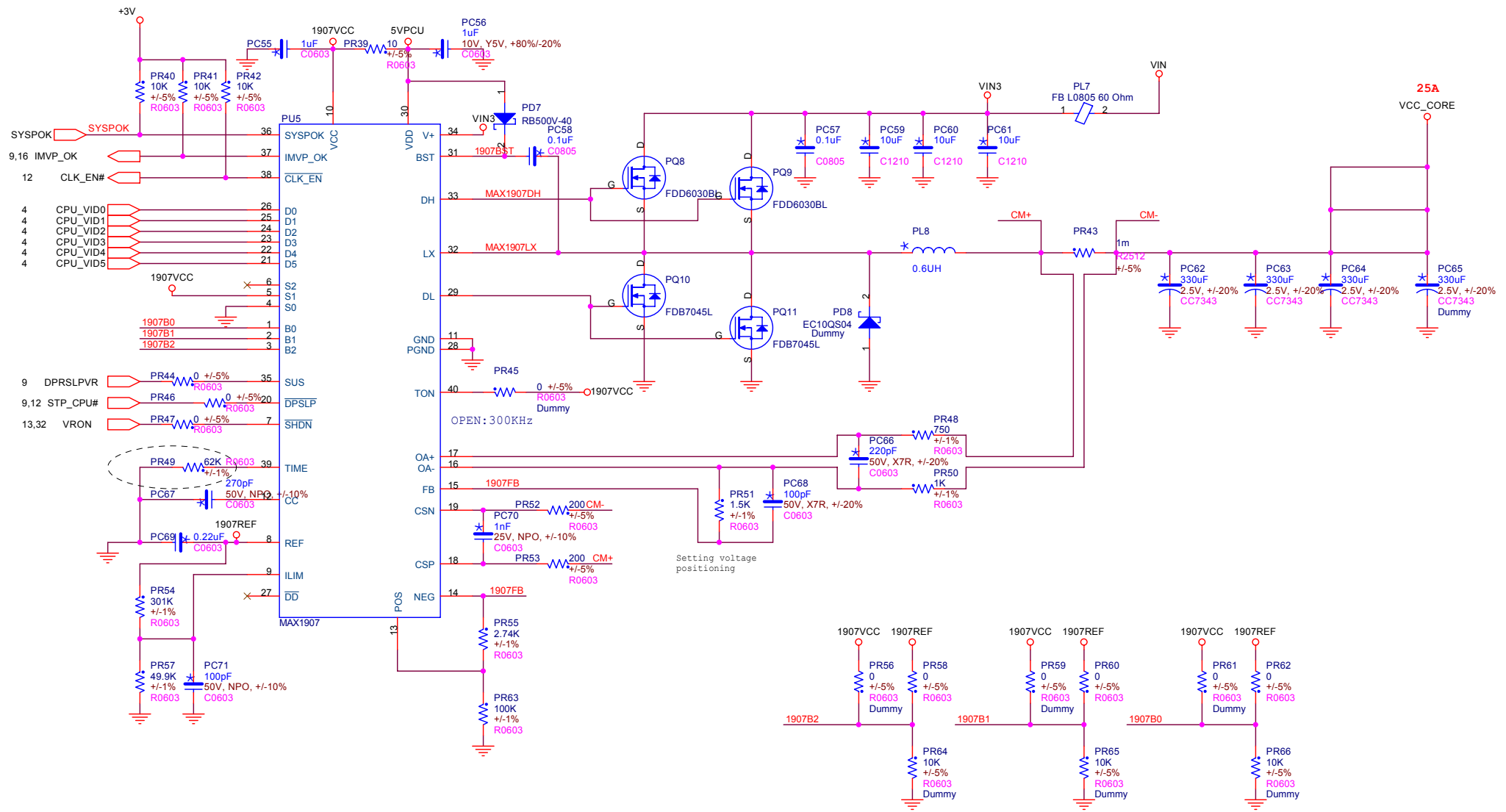
FOXCONN TECHNOLOGY CORP.	
Title 1.5V & CPU Power	
Document Number TPC01	
Date: Thursday, February 12, 2004	
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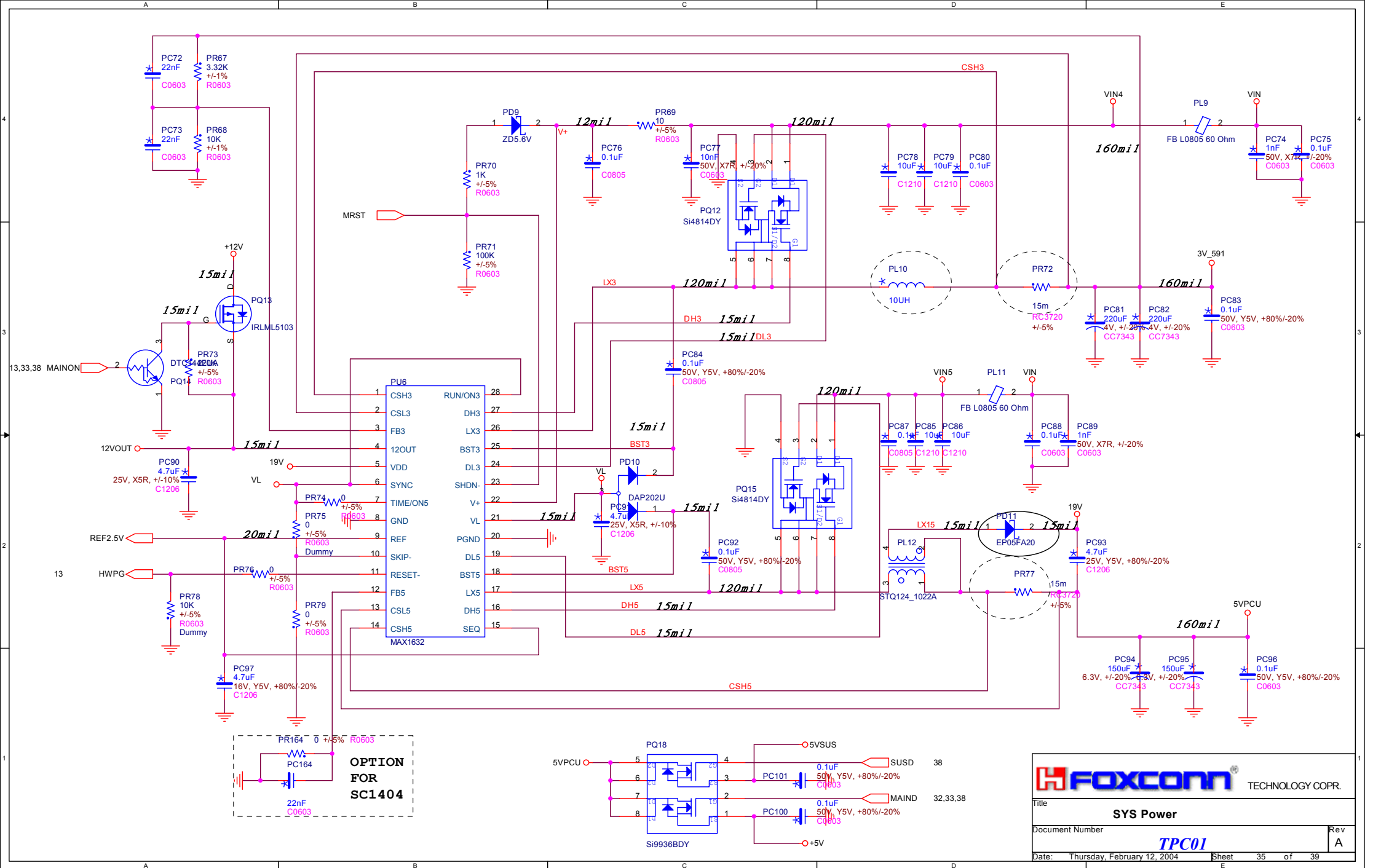


Title		DDR Power
Document Number		TPC01
Date:	Thursday, February 12, 2004	Sheet 33 of 39
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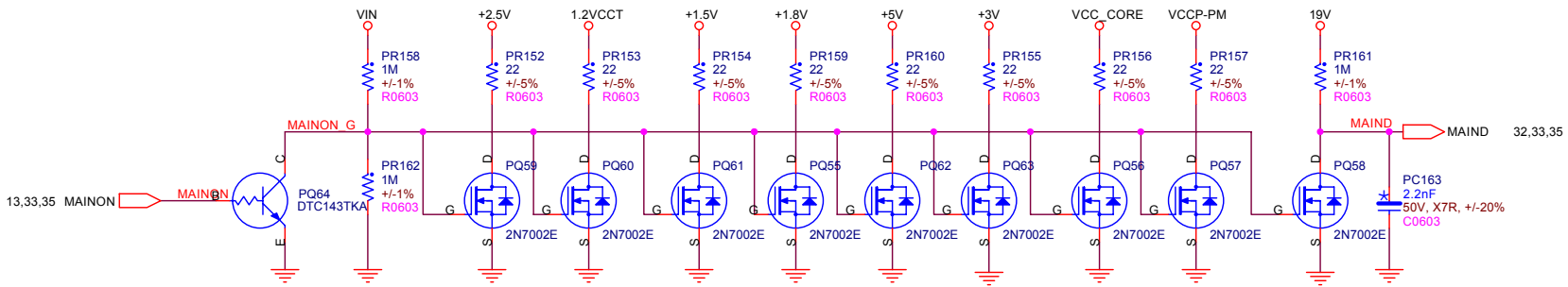
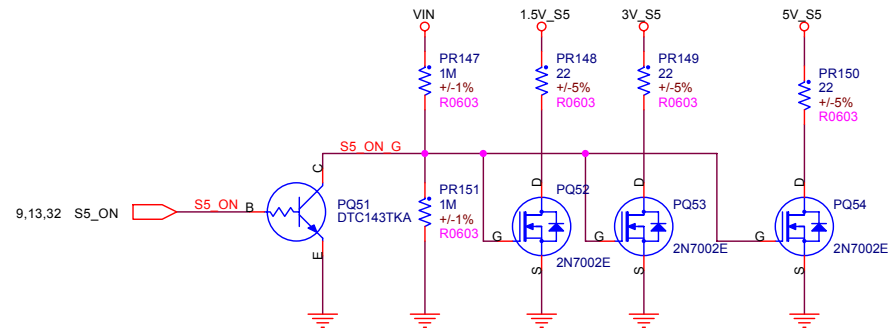
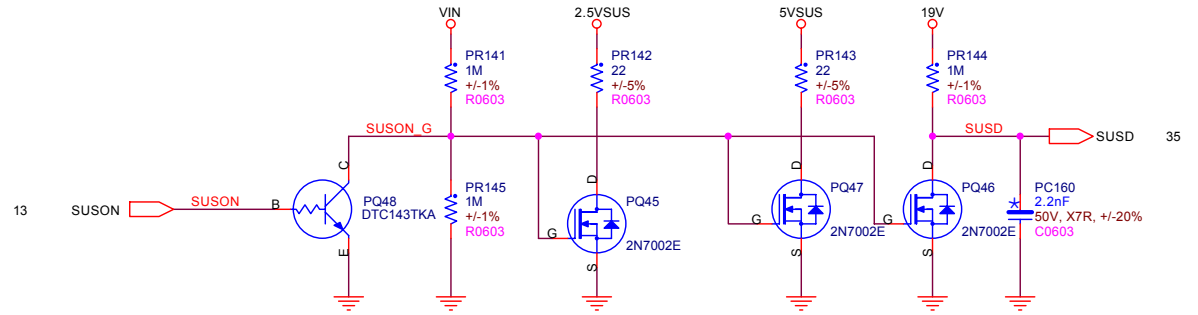
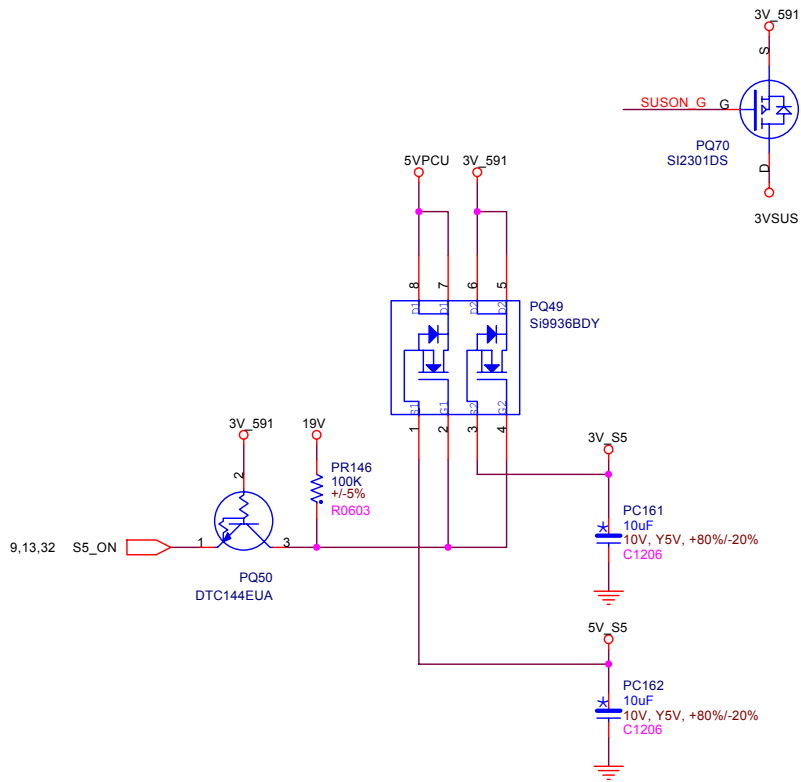


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FOXCONN TECHNOLOGY CORP.	
Title MAX1907 CPU Power	
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Title SYS Power	
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FOXCONN TECHNOLOGY CORP.	
Title Discharge Circuit	
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<i>Date</i>	<i>Page</i>	<i>Modification</i>
01/14	26	Swop Q28 D S pins'connection.
01/14	27	Rename R445,R446 and R448 to C615,C616,C617.
01/15	38	Connect PR158 pin2 with net MAINON_G.
01/15	15	Change J2 35,27,25,19,17,15,13 pins'GND net to USBGND.
01/16	09	Modify the nets:
		Name Original change
	13	IE# J7.6 U4B.J21 J7.6 U11.4 EMAIL_LED# J7.7 U4B.W1 J7.7 U11.3

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