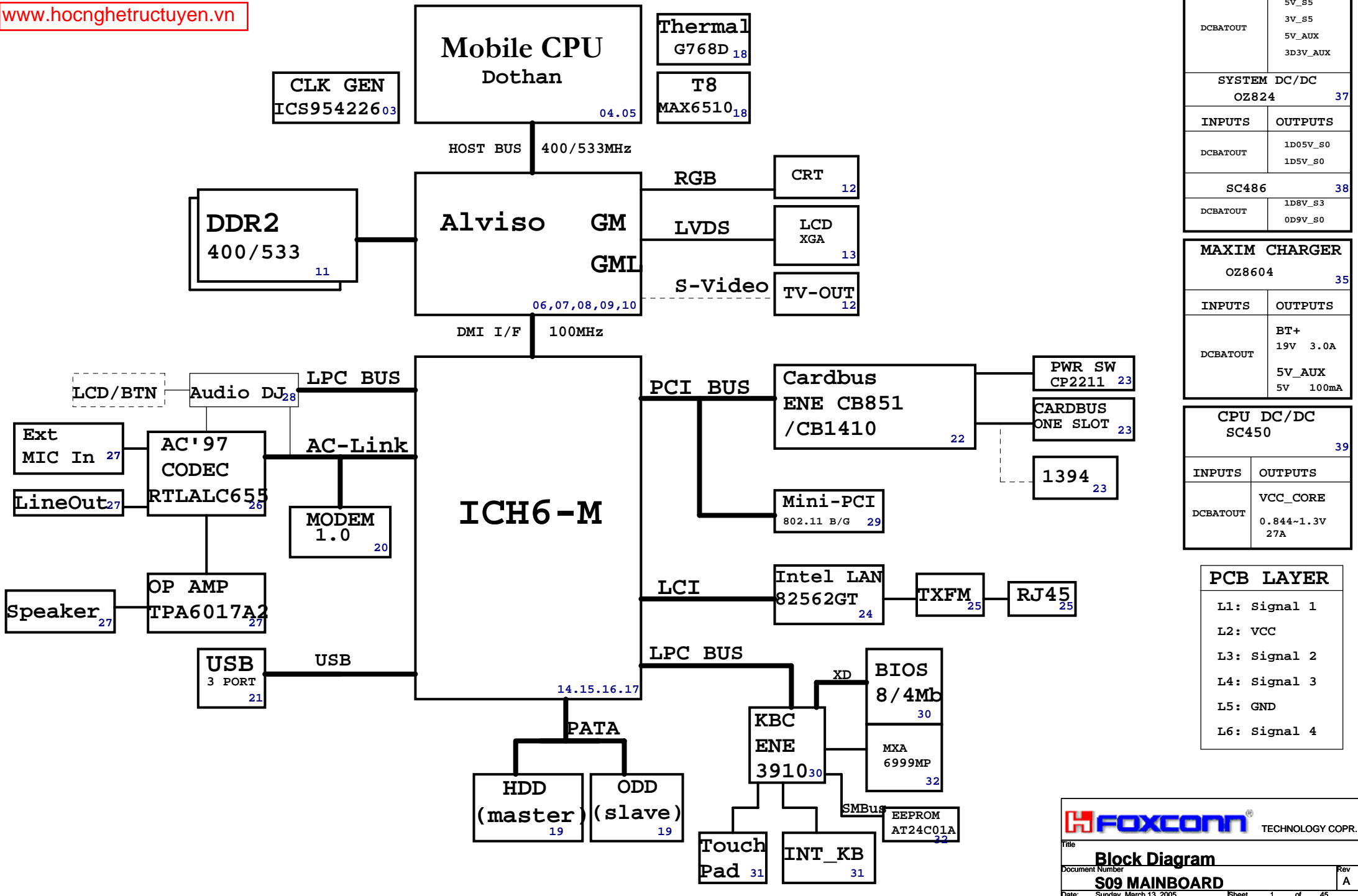


S09 Block Diagram

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| SYSTEM DC/DC MAX1999 36 | |
|-------------------------|--------------------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_S5 3V_S5 5V_AUX 3D3V_AUX |

| SYSTEM DC/DC OZ824 37 | |
|-----------------------|---------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_S0 1D5V_S0 |

| SC486 38 | |
|----------|--------------------|
| DCBATOUT | OUTPUTS |
| | 1D8V_S3 0D9V_S0 |

| MAXIM CHARGER OZ8604 35 | |
|-------------------------|---------------------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | BT+ 19V 3.0A 5V_AUX 5V 100mA |

| CPU DC/DC SC450 39 | |
|--------------------|-------------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE 0.844-1.3V 27A |

| PCB LAYER |
|--------------|
| L1: Signal 1 |
| L2: VCC |
| L3: Signal 2 |
| L4: Signal 3 |
| L5: GND |
| L6: Signal 4 |

Alviso Strapping Signals and Configuration

| Pin Name | Strap Description | Configuration |
|----------------|---|---|
| CFG[2:0] | FSB Frequency Select | 000 = Reserved 001 = FSB533 101 = FSB400 011-111 = Reversed |
| CFG[3:4] | Reversed | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | DDR I / DDR II | 0 = DDR II (Default) 1 = DDR I |
| CFG7 | CPU Strap | 0 = Reserved 1 = Dothan (Default) |
| CFG8 | Reversed | |
| CFG9 | PCI Express Graphics Lane reverse option for layout convenience | 0 = Reverse Lanes 1 = Normal Operation (Default) |
| CFG10 | Reversed | |
| CFG11 | Reversed | |
| CFG[13:12] | XOR/ALL Z test straps | 00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default) |
| CFG[14:15] | Reversed | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG17 | Reversed | |
| CFG18 | GMCH core VCC Select | 0 = 1.05V (For GML) 1 = 1.5V (For GM) |
| CFG19 | CPU VTT Select | 0 = 1.05V (Default) 1 = 1.2V |
| CFG20 | Reversed | |
| SDVO CRTL_DATA | SDVO Present | 0 = No SDVO device present (Default) 1 = SDVO device present |

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.

KBC Hardware Strap

| PinNumber | PinName | Function |
|-----------|---------|--|
| 125 | A1 | High:Enable the internal pull-up resistors on XIOCS [F:0] pins Low:Disable the internal pull-up resistors on XIOCS [F:0] |
| 128 | A4 | High: Diasble DMPP(Recommended) Low : Enable DMPP |
| 131 | A5 | High:Enable EMWB(Recommended for application using shared BIOS) Low:Disable EMWB |
| 11 | GPIO05 | High:Test Mode Low:32KHz clock in normal running(Recommend) |
| 12 | GPIO06 | High:Test Mode(KSOUT0~15 become DPLL internal data outputs, KS016 becomes internal power-on reset output Low:Normal operation(Recommended) |
| 105 | GPIO20 | High:Normal operation(Recommended) Low:Enable ISP mode during which the RD#,WR#,MEMSEL#,A[20:0] andD[7:0]will be controlled by ISP Contriller |

ICS954226 Spread Spectrum Select

| Byte 6b7 | Byte 6b6 | byte 6b5 | Byte 6b4 | Spread Mode | Spread Amount% | Pin17/18 Mhz |
|----------|----------|----------|----------|-------------|----------------|--------------|
| 1 | 0 | 0 | 0 | Down | 0.8 | 100 |
| 1 | 0 | 0 | 1 | Down | 1.25 | 100 |
| 1 | 0 | 1 | 0 | Down | 1.75 | 100 |
| 1 | 0 | 1 | 1 | Down | 2.5 | 100 |
| 1 | 1 | 0 | 0 | Center | +/-0.3 | 100 |
| 1 | 1 | 0 | 1 | Center | +/-0.5 | 100 |
| 1 | 1 | 1 | 0 | Center | +/-0.8 | 100 |
| 1 | 1 | 1 | 1 | Center | +/-1.25 | 100 |

PCI Routing

| | IDSEL | IRQ | REQ/GNT |
|---------|-------|-----|---------|
| CB851 | 25 | E | 0 |
| MiniPCI | 21 | C | 1 |
| 1394 | 19 | E | 3 |

ICH6-M IDE Integrated Series Termination Resistors

| | |
|--|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ, | approximately 33 ohm |
| DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ | |

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ICH6-M Integrated Pull-up and Pull-down Resistors

| | |
|--|--------------------------------|
| EE_DIN, EE_DOUT, GNT[3:0] GNT[4]#/GPO[48], GNT[5]#/GPO[17], GNT[6]#/GPO[16], GPIO[25] LAD[3:0]#/FB[3:0]#, LAN_RXD[2:0], LDRQ[0], LDRQ[1]/GPI[41],PME#, PWRBTN#, TP[3] | ICH6 internal 20K pull-ups |
| ACZ_BITCLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSTP# DPRSLPVR, EE_CS, SPKR, | ICH6 internal 20K pull-downs |
| USB[7:0][P,N] SATALED# | ICH6 internal 15K pull-downs |
| DD[7], DDREQ | ICH6 internal 11.5K pull-downs |
| LAN_CLK | ICH6 internal 100K pull-downs |

ICH6-M Strapping Options

| REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE |
|------|-------------------|---------|-------------------|
| R275 | No Reboot | Dummy | Reserved |
| R279 | A16 Swap Override | Dummy | Reserved |
| R282 | Boot BIOS | Dummy | Reserved |

I2C/SMB Addresses

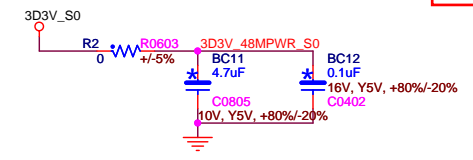
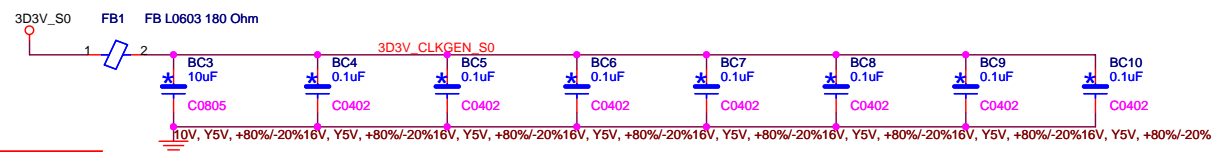
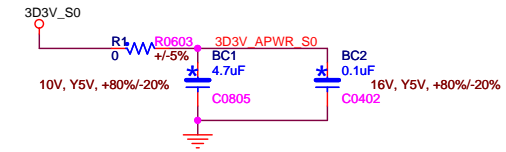
| Device | Address | Bus |
|-----------------|-----------|------------|
| Clock Generator | 1101 001x | SMB_ICH_S0 |
| SO-DIMMO | 1010 000x | SMB_ICH_S0 |
| SO-DIMM1 | 1010 010x | SMB_ICH_S0 |
| Thermal Sensor | 0111 101x | SMB_KBC_S0 |
| Battery | 0001 000x | SMB_KBC_S5 |
| Antitheft | 1010 000x | SMB_KBC_S5 |
| Light Sensor | 0111 001x | SMB_KBC_S0 |
| | | |
| | | |
| | | |

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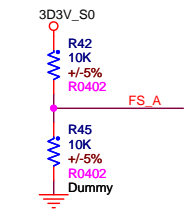
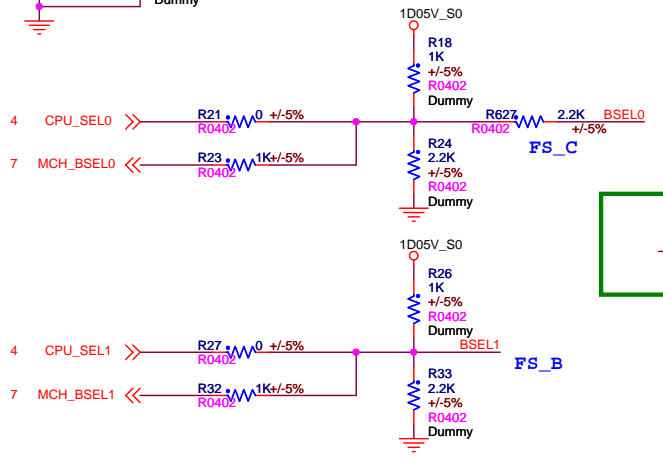
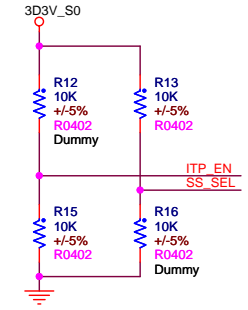


| | | |
|-----------------|-------------------------|---------------|
| Title | Table of content | |
| Document Number | S09 MAINBOARD | Rev A |
| Date: | Tuesday, March 15, 2005 | Sheet 2 of 45 |

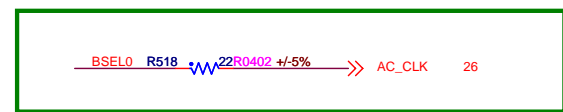
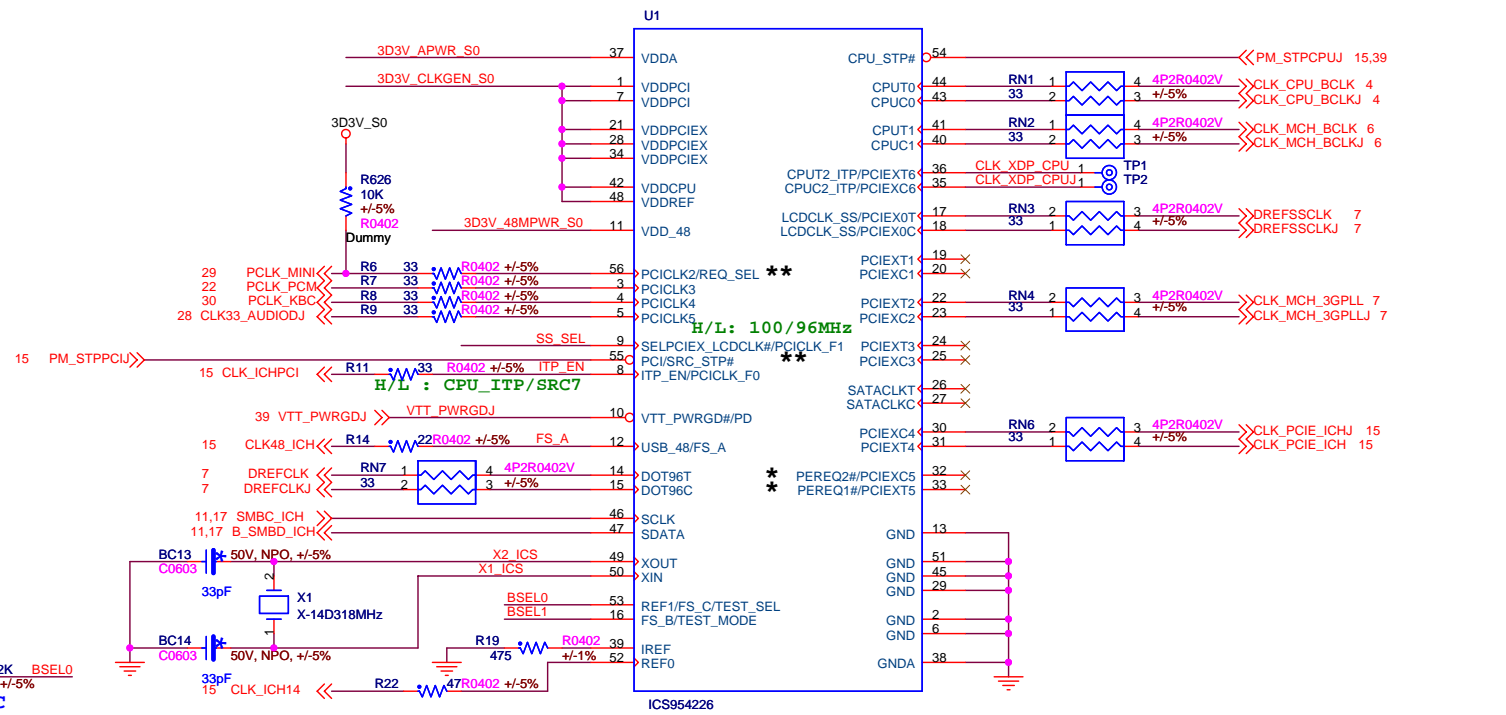
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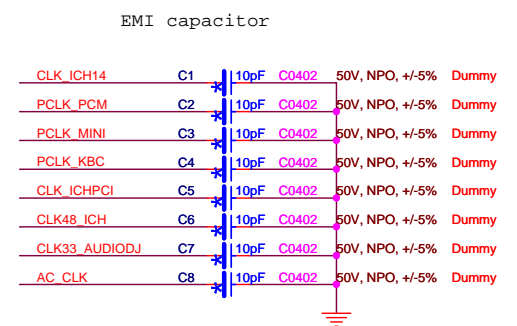
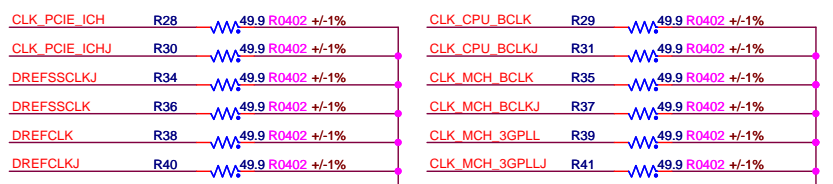
ITP_EN 0=PCIEX_6 1=CPU_2_ITP
 SS_SEL 0=LCDCLK 1=PCIEX/free running
 3.3V PCI clock output



| FS_C | FS_B | FS_A | CPU |
|------|------|------|------|
| 0 | 0 | 0 | 266M |
| 0 | 0 | 1 | 133M |
| 0 | 1 | 0 | 200M |
| 0 | 1 | 1 | 165M |
| 1 | 0 | 0 | 333M |
| 1 | 0 | 1 | 100M |
| 1 | 1 | 0 | 400M |



*internal Pull-Up resistors
 **internal Pull-Down resistor
 To external AC'97 CLK



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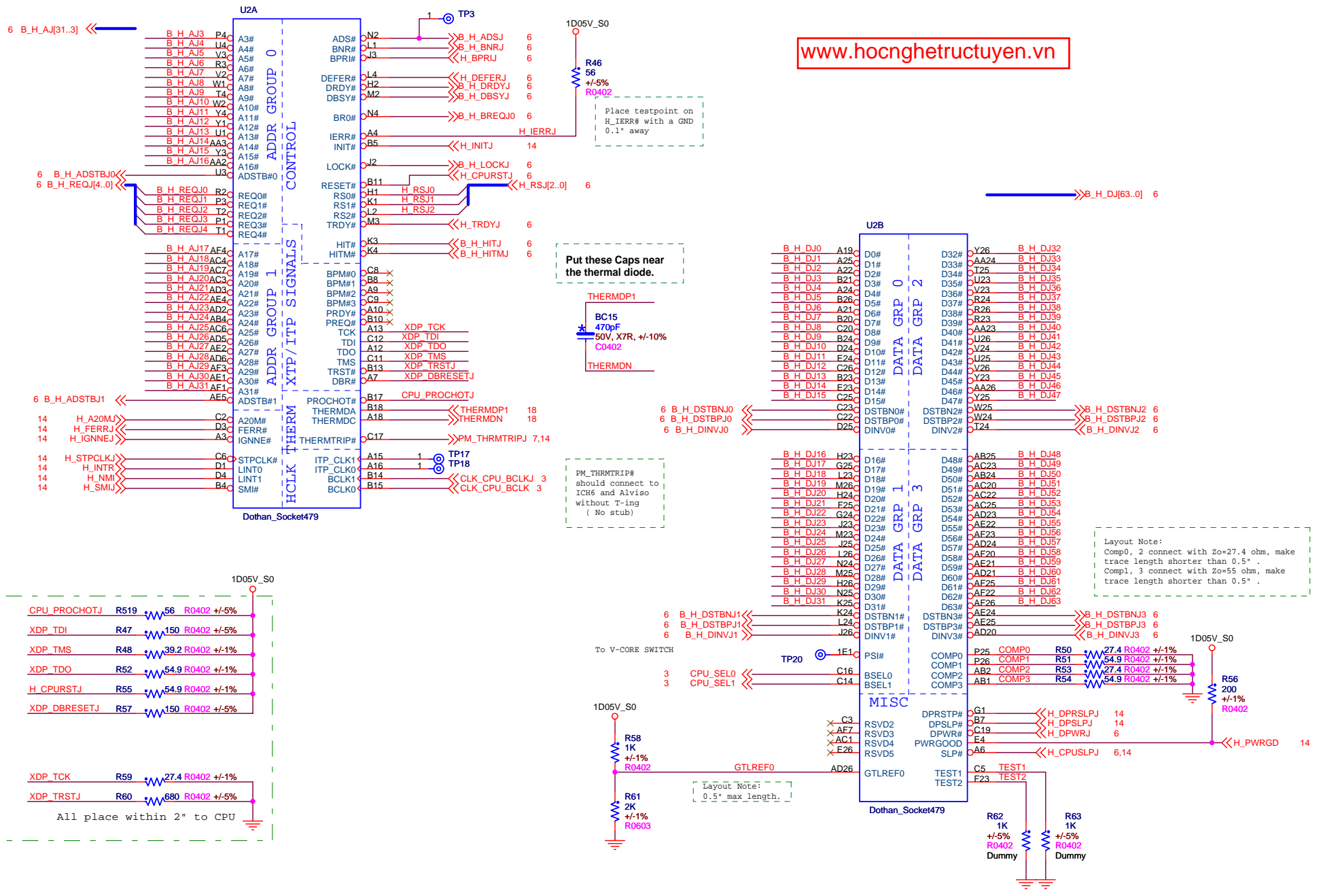
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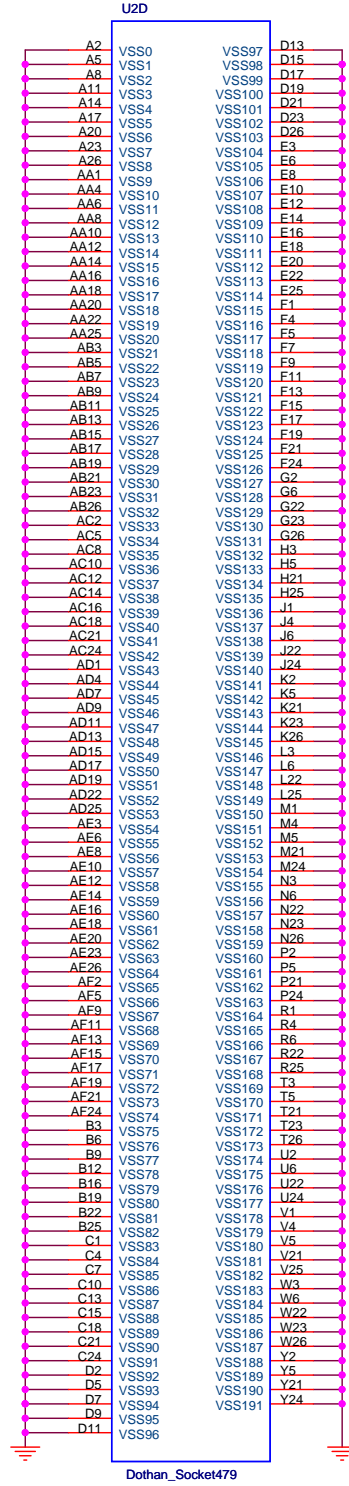
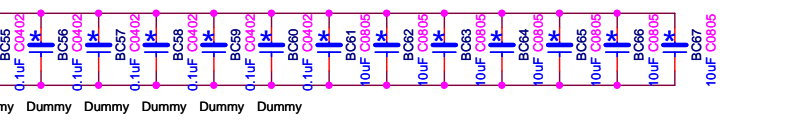
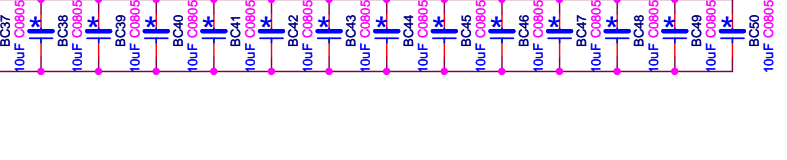
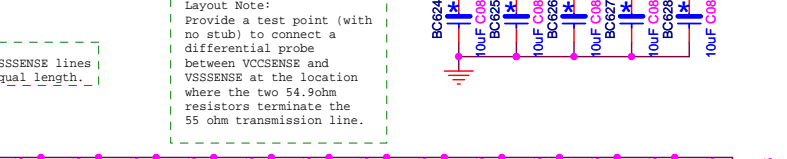
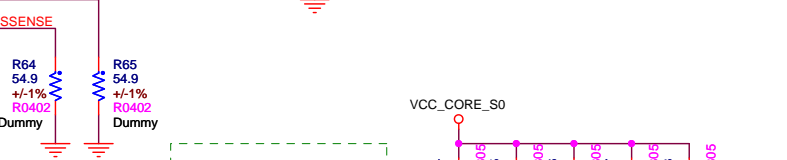
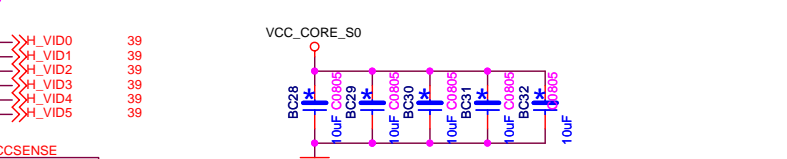
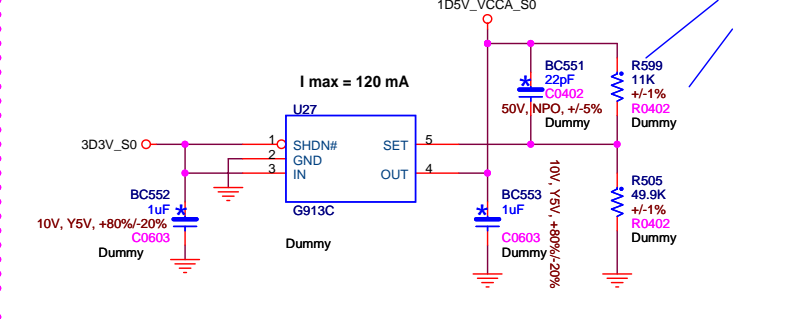
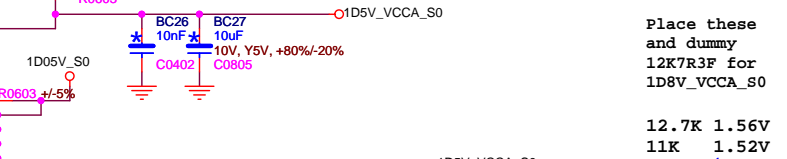
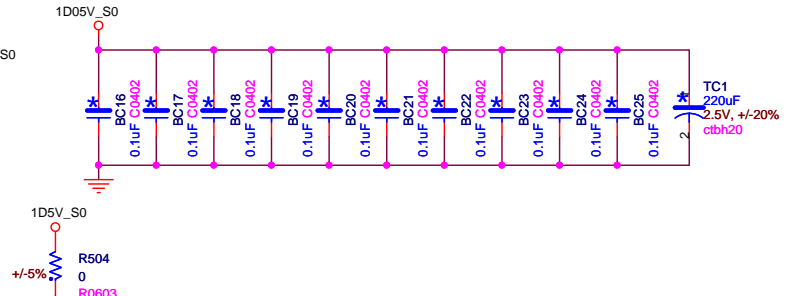
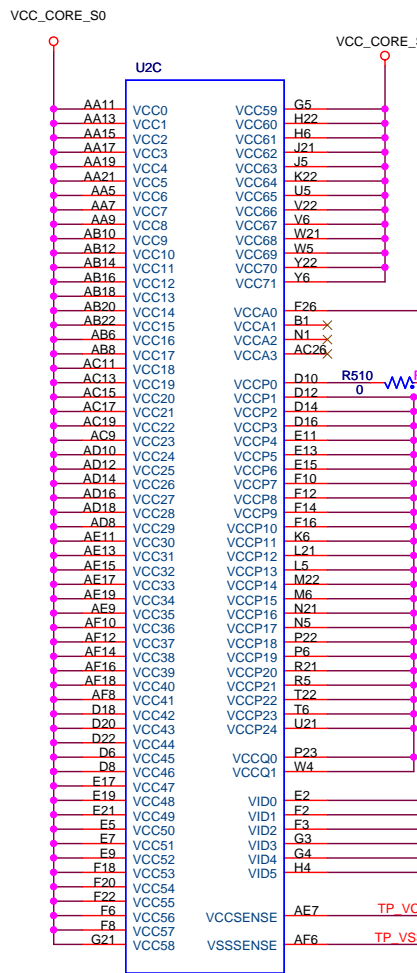
Document Number: **S09 MAINBOARD**

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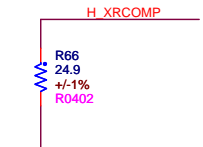
Place these and dummy 12K7R3F for 1D8V_VCCA_S0

12.7K 1.56V
11K 1.52V

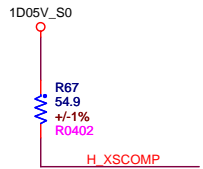
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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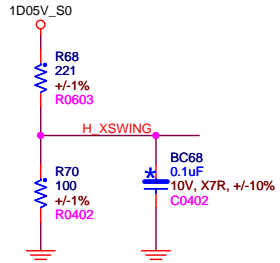
Document Number: **CPU(2 of 2)**
S09 MAINBOARD
 Date: Thursday, March 17, 2005 Sheet 5 of 45



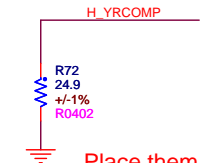
Place them near to the chip



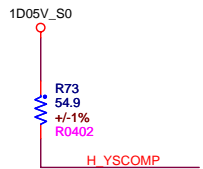
Place them near to the chip



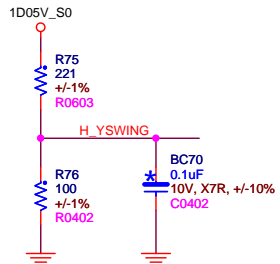
Place them near to the chip



Place them near to the chip



Place them near to the chip



Place them near to the chip

4 B_H_DJ[63..0]

U3A

| | |
|----------|----|
| B_H_DJ0 | E4 |
| B_H_DJ1 | E1 |
| B_H_DJ2 | F4 |
| B_H_DJ3 | H7 |
| B_H_DJ4 | E2 |
| B_H_DJ5 | F1 |
| B_H_DJ6 | E3 |
| B_H_DJ7 | D3 |
| B_H_DJ8 | K7 |
| B_H_DJ9 | F2 |
| B_H_DJ10 | J7 |
| B_H_DJ11 | J8 |
| B_H_DJ12 | H6 |
| B_H_DJ13 | F3 |
| B_H_DJ14 | K8 |
| B_H_DJ15 | H5 |
| B_H_DJ16 | H1 |
| B_H_DJ17 | H2 |
| B_H_DJ18 | K6 |
| B_H_DJ19 | K5 |
| B_H_DJ20 | J4 |
| B_H_DJ21 | G3 |
| B_H_DJ22 | H3 |
| B_H_DJ23 | J1 |
| B_H_DJ24 | L5 |
| B_H_DJ25 | K4 |
| B_H_DJ26 | J5 |
| B_H_DJ27 | P7 |
| B_H_DJ28 | L7 |
| B_H_DJ29 | J3 |
| B_H_DJ30 | P5 |
| B_H_DJ31 | L3 |
| B_H_DJ32 | U7 |
| B_H_DJ33 | V6 |
| B_H_DJ34 | R6 |
| B_H_DJ35 | R5 |
| B_H_DJ36 | P3 |
| B_H_DJ37 | T8 |
| B_H_DJ38 | R7 |
| B_H_DJ39 | R8 |
| B_H_DJ40 | U8 |
| B_H_DJ41 | R4 |
| B_H_DJ42 | T4 |
| B_H_DJ43 | T5 |
| B_H_DJ44 | R1 |
| B_H_DJ45 | T3 |
| B_H_DJ46 | V8 |
| B_H_DJ47 | U6 |
| B_H_DJ48 | W6 |
| B_H_DJ49 | U3 |
| B_H_DJ50 | V5 |
| B_H_DJ51 | W8 |
| B_H_DJ52 | W7 |
| B_H_DJ53 | U2 |
| B_H_DJ54 | U1 |
| B_H_DJ55 | Y5 |
| B_H_DJ56 | Y2 |
| B_H_DJ57 | V4 |
| B_H_DJ58 | Y7 |
| B_H_DJ59 | W1 |
| B_H_DJ60 | W3 |
| B_H_DJ61 | Y3 |
| B_H_DJ62 | Y6 |
| B_H_DJ63 | W2 |
| H_XRCOMP | C1 |
| H_XSCOMP | C2 |
| H_XSWING | D1 |
| H_YRCOMP | T1 |
| H_YSCOMP | L1 |
| H_YSWING | P1 |

H02

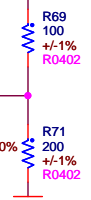
ALVISO-GM
71.0GMCH.08U

| | | |
|----------|-----|-----------------|
| HA3# | G9 | B_H_AJ3 |
| HA4# | C9 | B_H_AJ4 |
| HA5# | E9 | B_H_AJ5 |
| HA6# | B7 | B_H_AJ6 |
| HA7# | A10 | B_H_AJ7 |
| HA8# | F9 | B_H_AJ8 |
| HA9# | D8 | B_H_AJ9 |
| HA10# | E10 | B_H_AJ10 |
| HA11# | G10 | B_H_AJ11 |
| HA12# | D9 | B_H_AJ12 |
| HA13# | E11 | B_H_AJ13 |
| HA14# | F10 | B_H_AJ14 |
| HA15# | G11 | B_H_AJ15 |
| HA16# | G13 | B_H_AJ16 |
| HA17# | C10 | B_H_AJ17 |
| HA18# | C11 | B_H_AJ18 |
| HA19# | C12 | B_H_AJ19 |
| HA20# | C13 | B_H_AJ20 |
| HA21# | B13 | B_H_AJ21 |
| HA22# | A12 | B_H_AJ22 |
| HA23# | E12 | B_H_AJ23 |
| HA24# | G12 | B_H_AJ24 |
| HA25# | E12 | B_H_AJ25 |
| HA26# | E12 | B_H_AJ26 |
| HA27# | C13 | B_H_AJ27 |
| HA28# | B11 | B_H_AJ28 |
| HA29# | D13 | B_H_AJ29 |
| HA30# | A13 | B_H_AJ30 |
| HA31# | E13 | B_H_AJ31 |
| HADS# | E8 | B_H_ADSJ 4 |
| HADSTB#0 | B9 | B_H_ADSTBJ0 4 |
| HADSTB#1 | E13 | B_H_ADSTBJ1 4 |
| HVREF | J11 | H_VREF |
| HBNR# | A5 | B_H_BNRJ 4 |
| HBPRJ# | D5 | H_BPRJ 4 |
| HBREQ0# | E7 | B_H_BREQJ0 4 |
| HCPURST# | H10 | H_CPURSTJ 4 |
| HCLKINN | AB1 | CLK_MCH_BCLKJ 3 |
| HCLKINP | AB2 | CLK_MCH_BCLK 3 |
| HDBSY# | C6 | B_H_DBSYJ 4 |
| HDEFER# | E6 | H_DEFERJ 4 |
| HDINV#0 | H8 | B_H_DINVJ0 4 |
| HDINV#1 | K3 | B_H_DINVJ1 4 |
| HDINV#2 | T7 | B_H_DINVJ2 4 |
| HDINV#3 | U5 | B_H_DINVJ3 4 |
| HDPWR# | C7 | H_DPWRJ 4 |
| HDRDY# | C7 | B_H_DRDYJ 4 |
| HDSTBN#0 | G4 | B_H_DSTBNJ0 4 |
| HDSTBN#1 | K1 | B_H_DSTBNJ1 4 |
| HDSTBN#2 | R3 | B_H_DSTBNJ2 4 |
| HDSTBN#3 | V3 | B_H_DSTBNJ3 4 |
| HDSTBP#0 | G5 | B_H_DSTBPJ0 4 |
| HDSTBP#1 | K2 | B_H_DSTBPJ1 4 |
| HDSTBP#2 | R2 | B_H_DSTBPJ2 4 |
| HDSTBP#3 | W4 | B_H_DSTBPJ3 4 |
| HEDRDY# | E6 | TP_H_EDRDYJ 1 |
| HHIT# | D4 | B_H_HITJ 4 |
| HHITM# | D6 | B_H_HITMJ 4 |
| HLOCK# | B3 | B_H_LOCKJ 4 |
| HPCREQ# | A11 | TP_H_PCREQJ 1 |
| HREQ#0 | A7 | B_H_REQJ0 4 |
| HREQ#1 | D7 | B_H_REQJ1 4 |
| HREQ#2 | B8 | B_H_REQJ2 4 |
| HREQ#3 | C7 | B_H_REQJ3 4 |
| HREQ#4 | A8 | B_H_REQJ4 4 |
| HRS#0 | A4 | H_RSJ0 4 |
| HRS#1 | C5 | H_RSJ1 4 |
| HRS#2 | B4 | H_RSJ2 4 |
| HCPUSLP# | G8 | H_CPUSLPJ 0 |
| HTRDY# | B5 | H_TRDYJ 4 |

>>>B_H_AJ[31..3] 4

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1D05V_S0



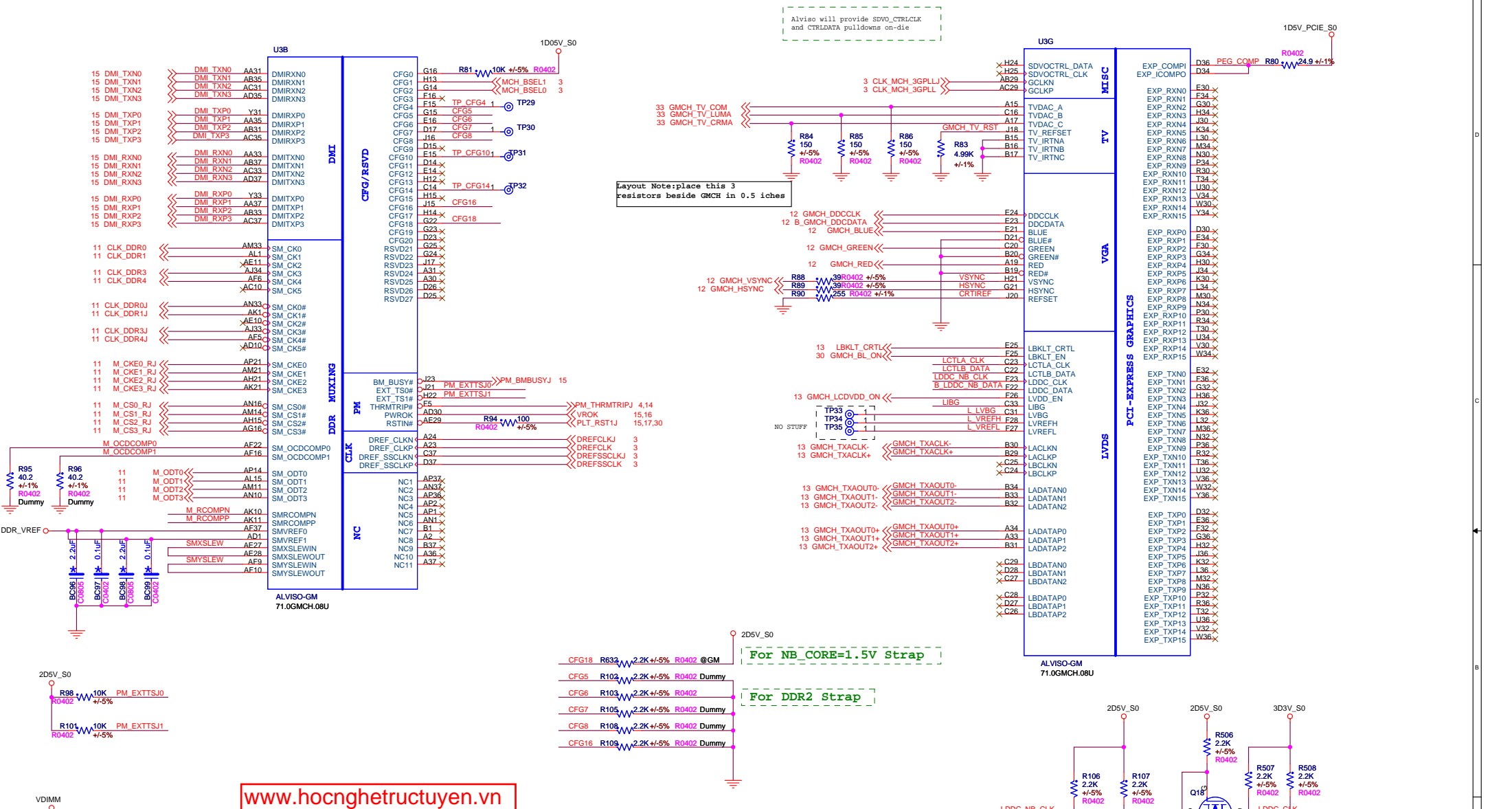
Place them near to the chip

TP25

TP26

DUMMY FOR DOTAN A STEPPING





Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die

Layout Note: place this 3 resistors beside GMCH in 0.5 inches

For NB CORE=1.5V Strap

For DDR2 Strap

Layout Note: place this 3 resistors beside GMCH in 0.5 inches

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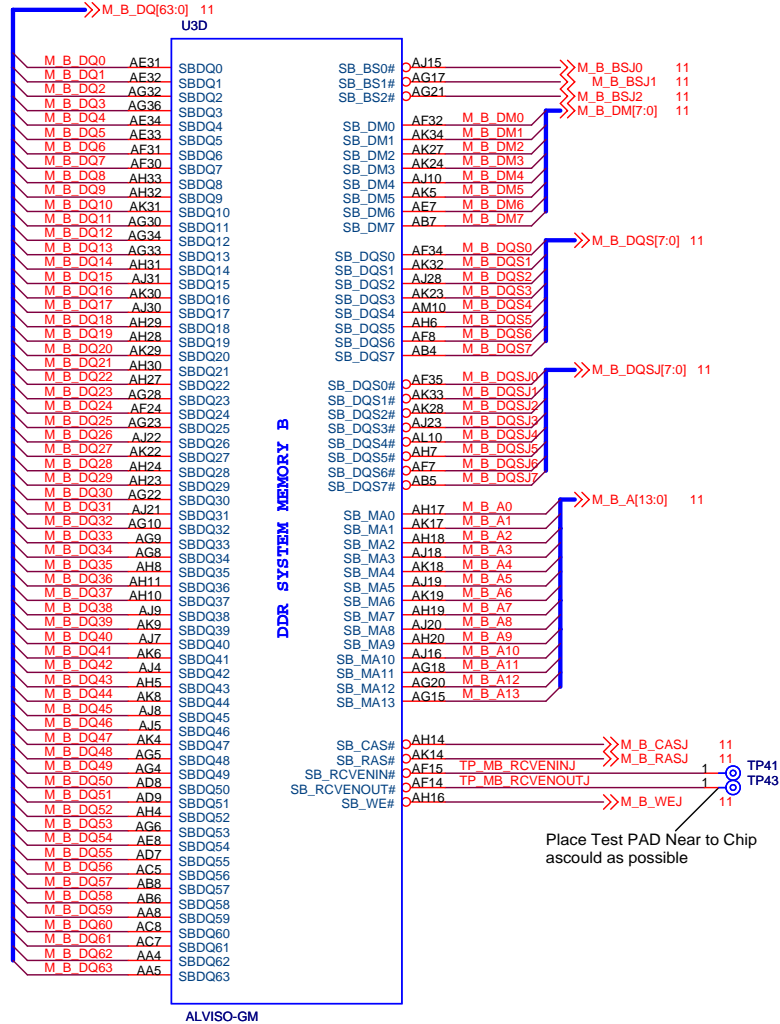
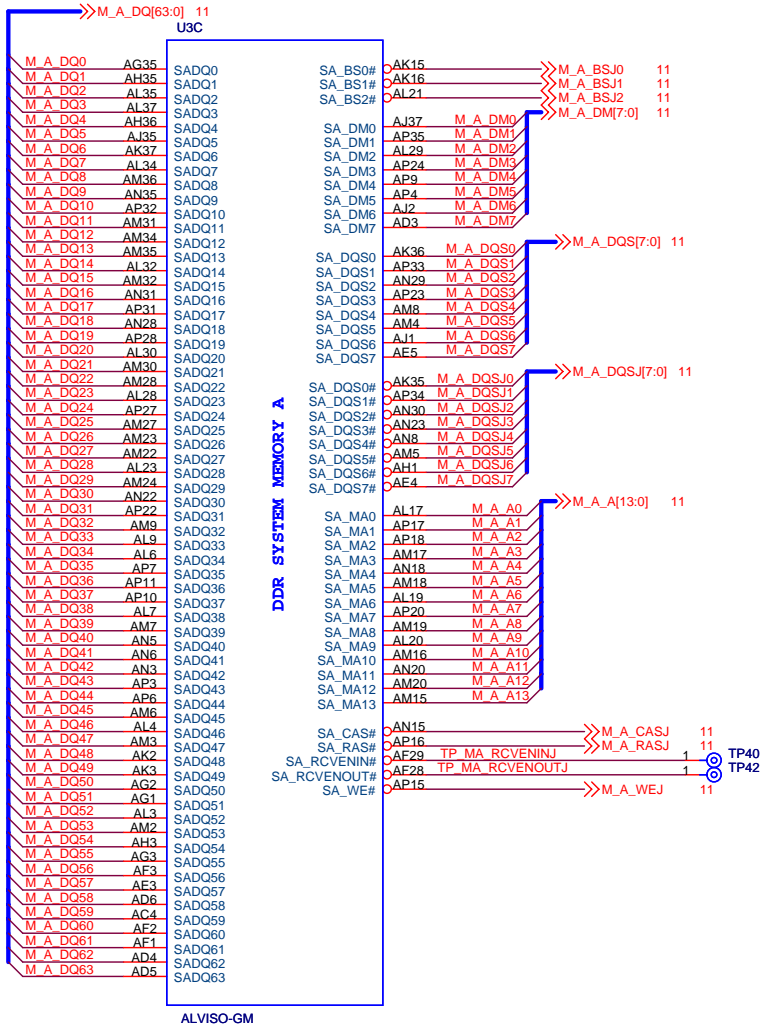
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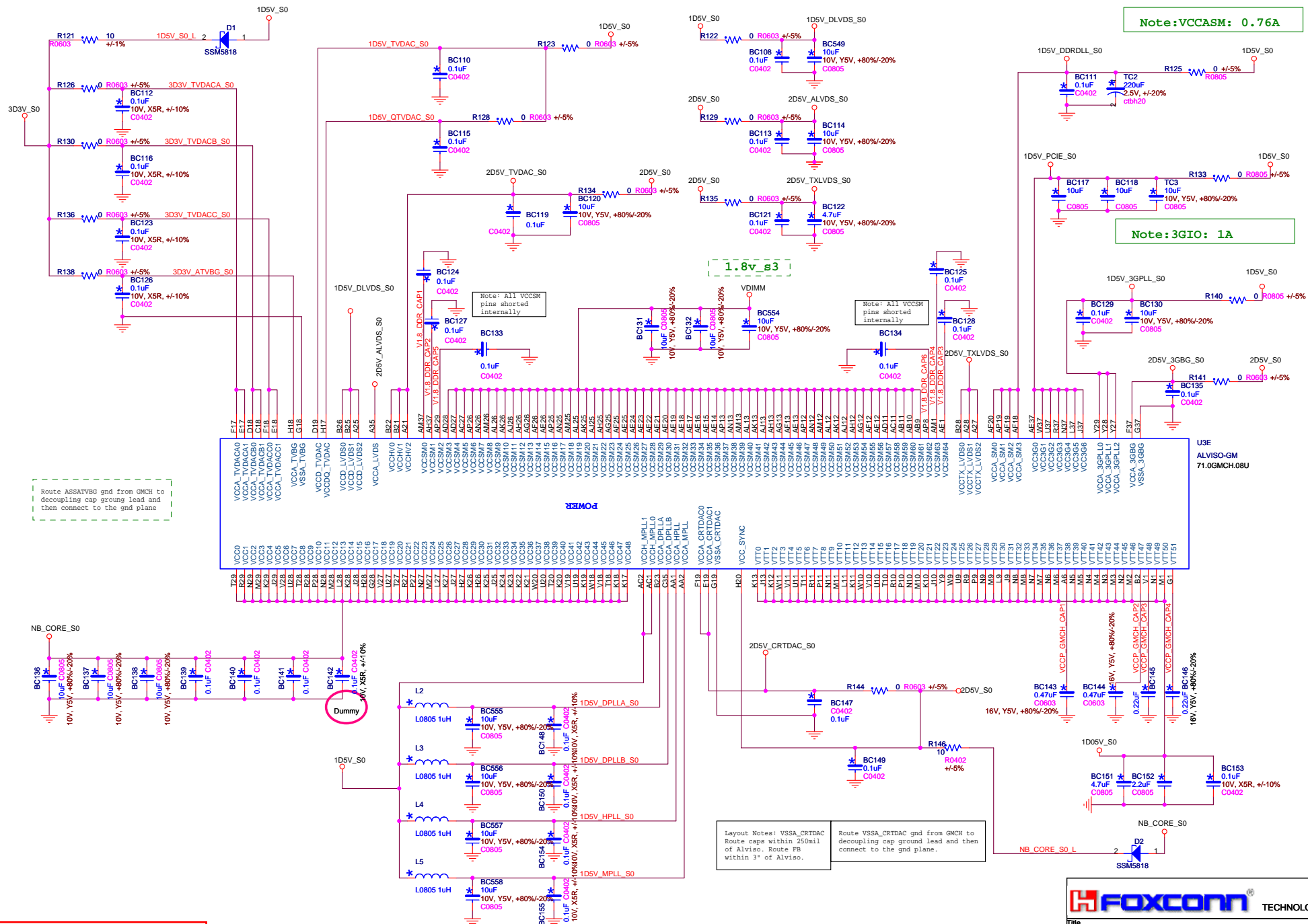
Document Number **S09 MAINBOARD**

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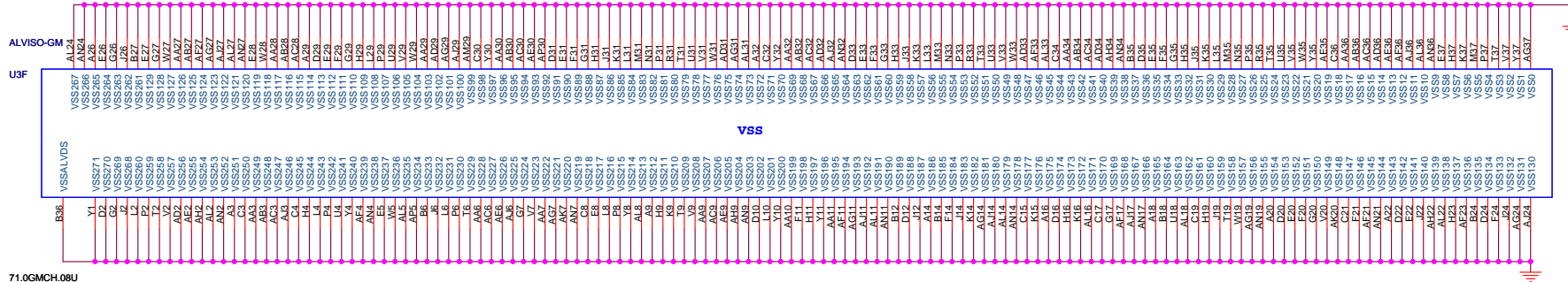
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Document Number: **S09 MAINBOARD**

Date: Monday, March 14, 2005

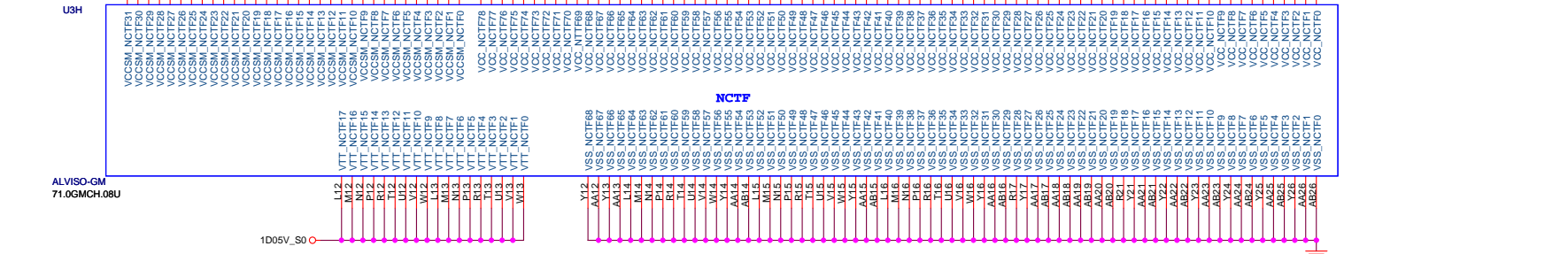
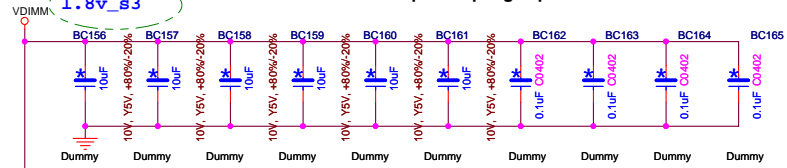
Sheet 9 of 45

Rev: **A**

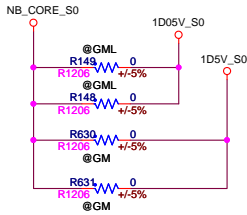


71.0GMCH.08U

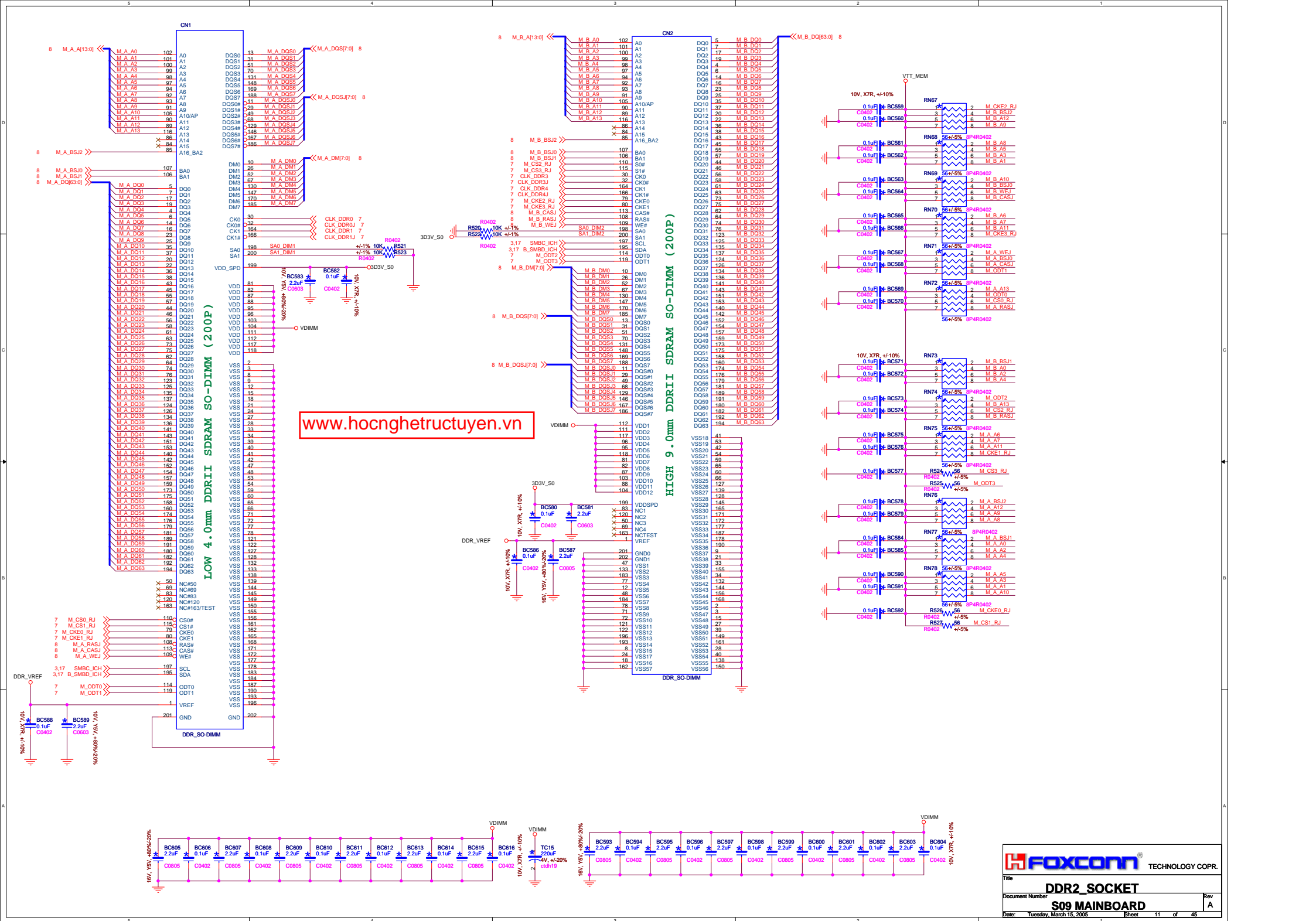
Place these HI-Freq decoupling caps near GMCH



ALVISO-GM 71.0GMCH.08U



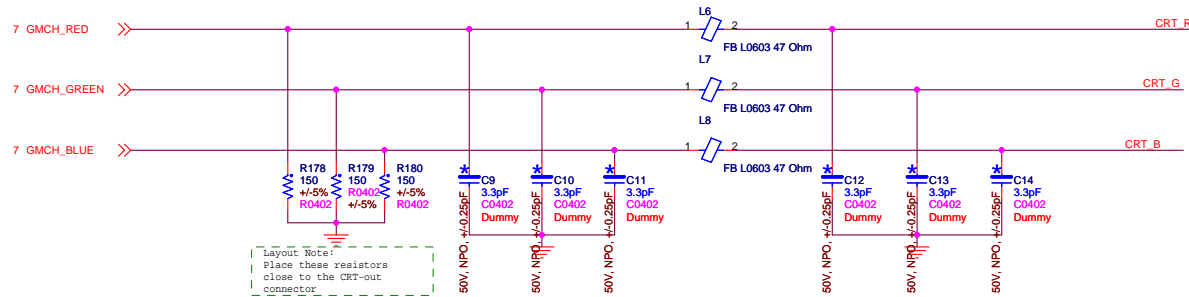
GML: NB_CORE=1.05V
 GM: NB_CORE=1.5V



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CRT I/F & CONNECTOR

Ferrite bead impedance: 47ohm@100MHz

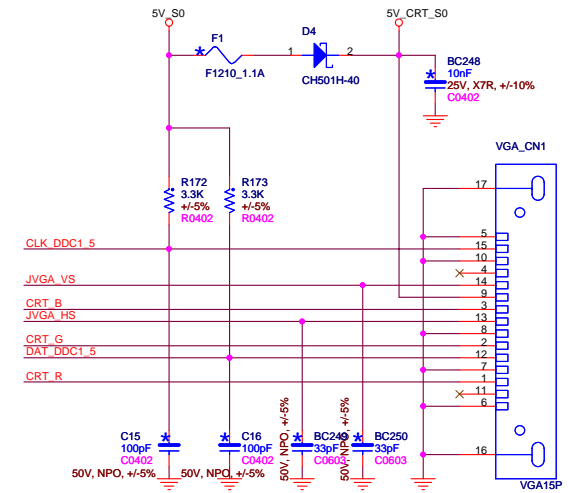
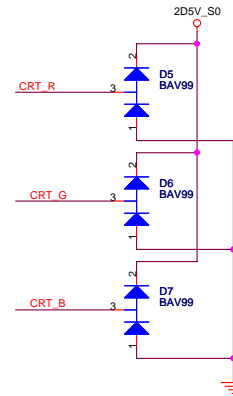
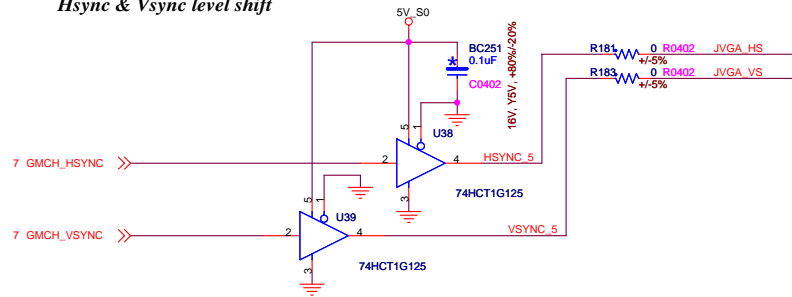


Layout Note:
Place these resistors
close to the CRT-out
connector

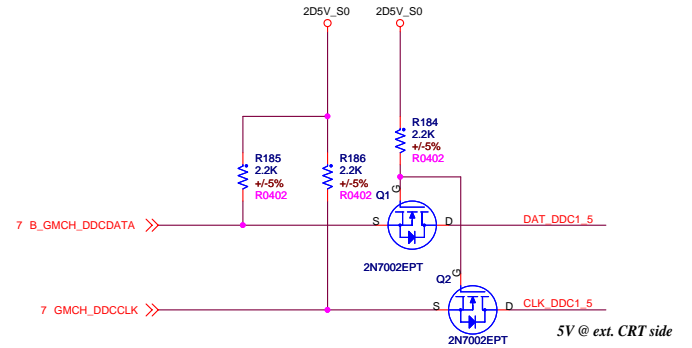
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

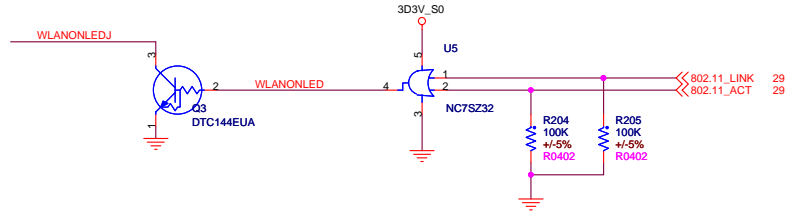


DDC_CLK & DATA level shift

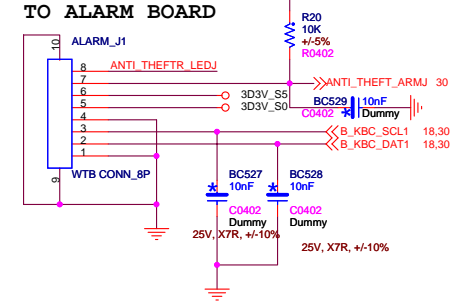
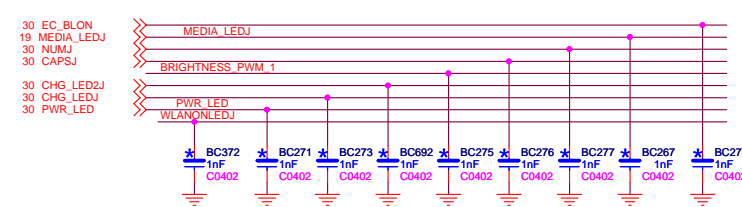
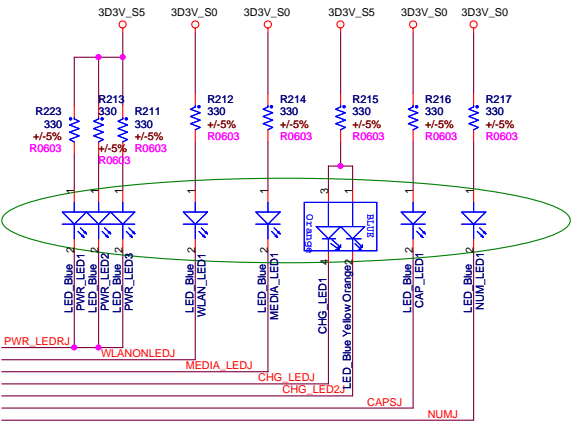
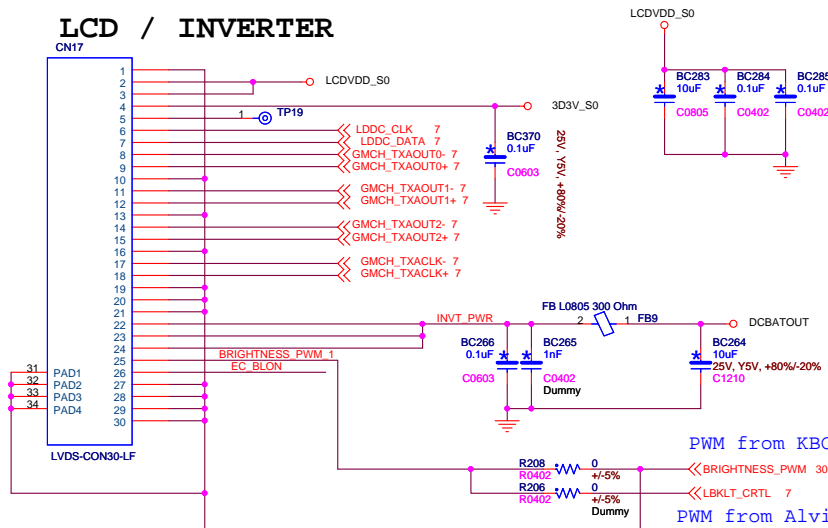


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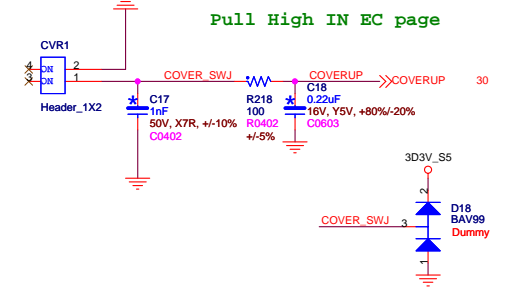
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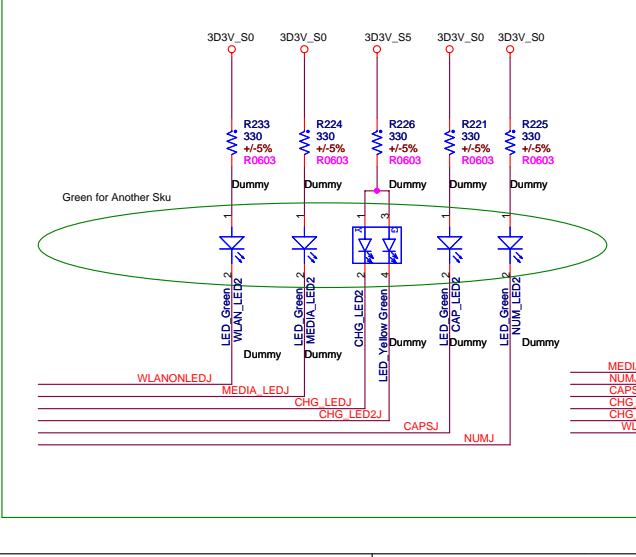
LCD / INVERTER



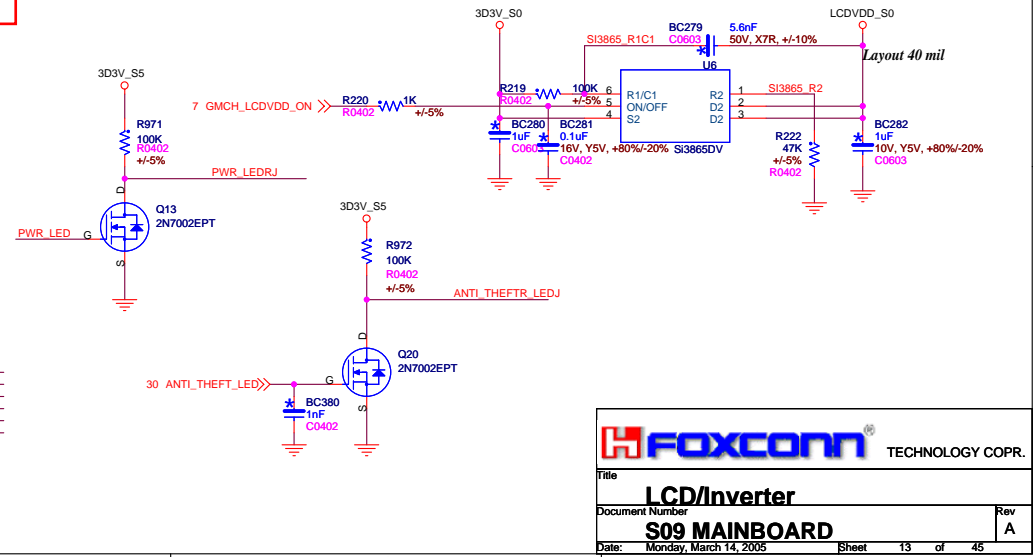
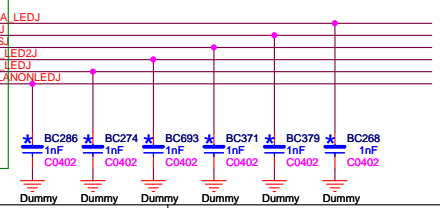
PWM from KBC
PWM from Alviso

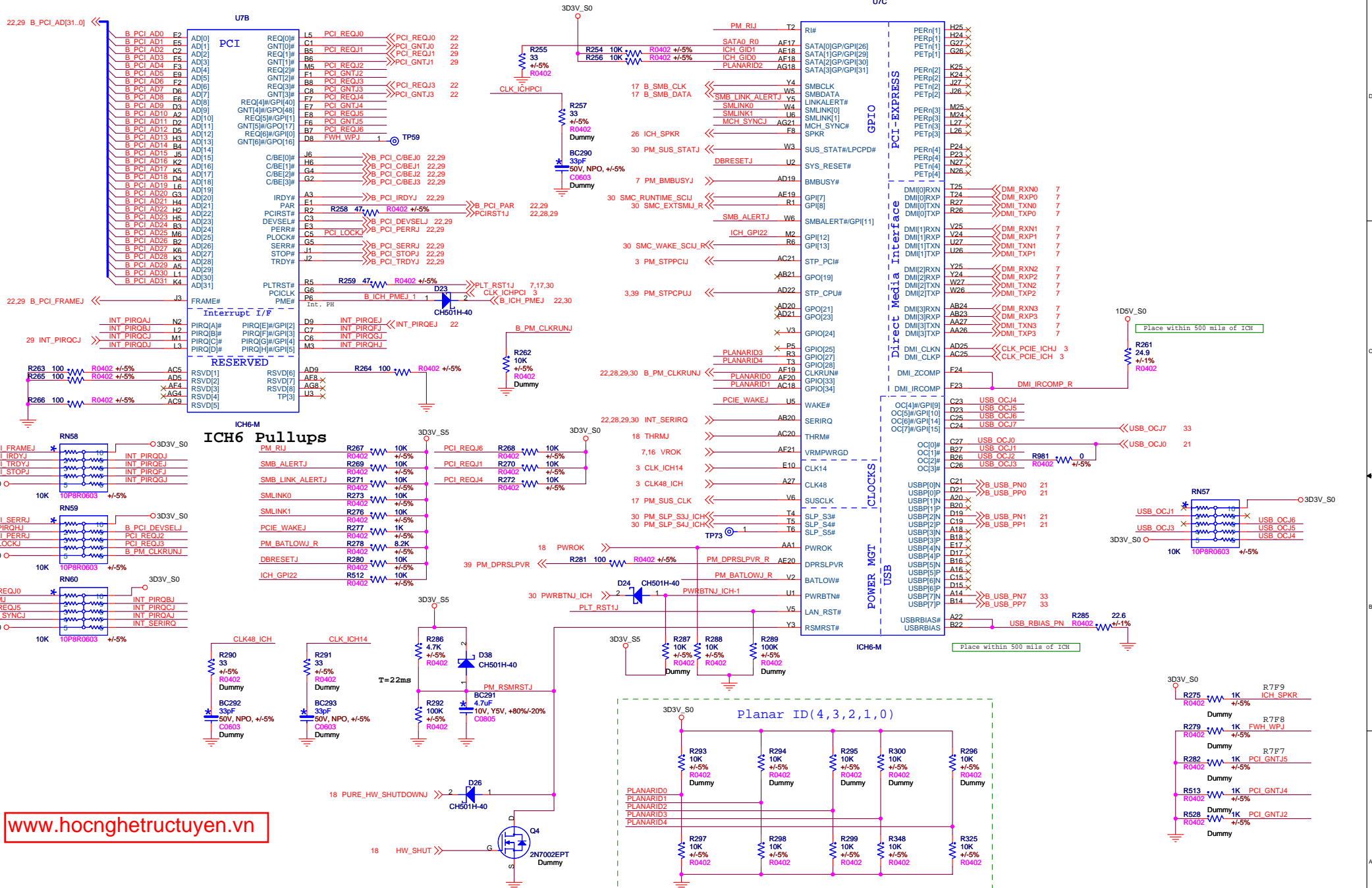


For Another SKU



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Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail

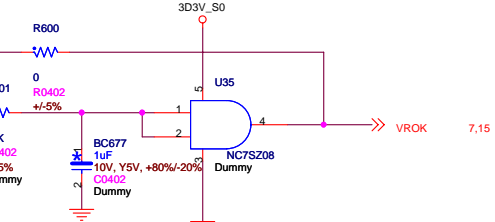
ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6

Place within 100
mils of ICH pin
AG13, AG16

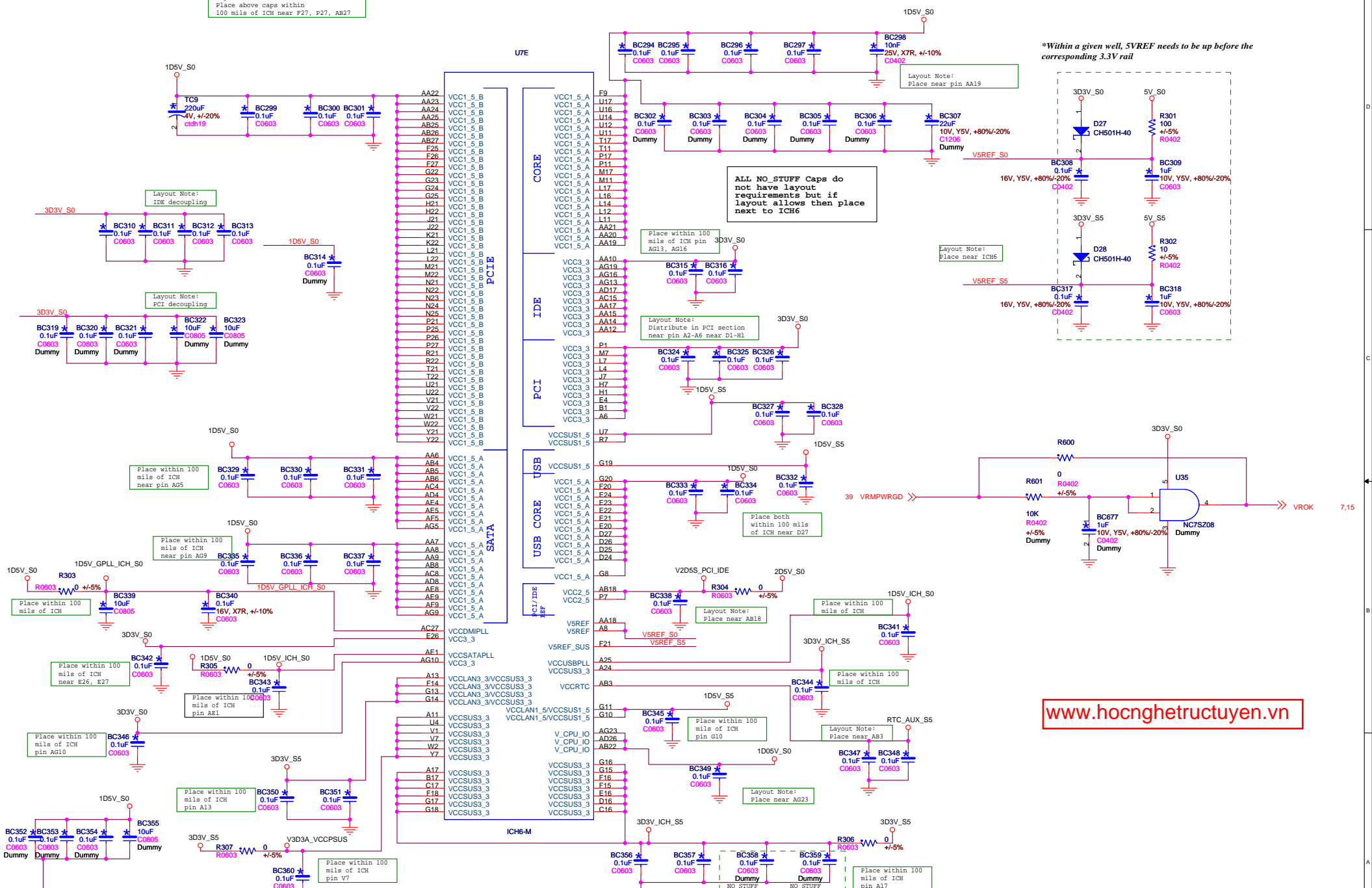
Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1

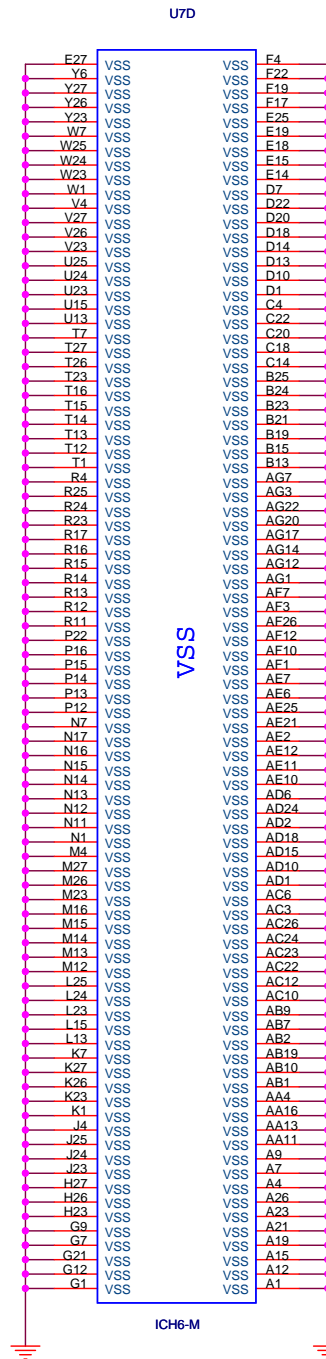
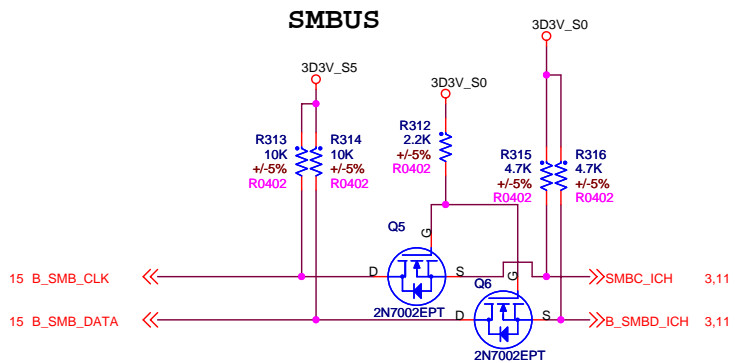
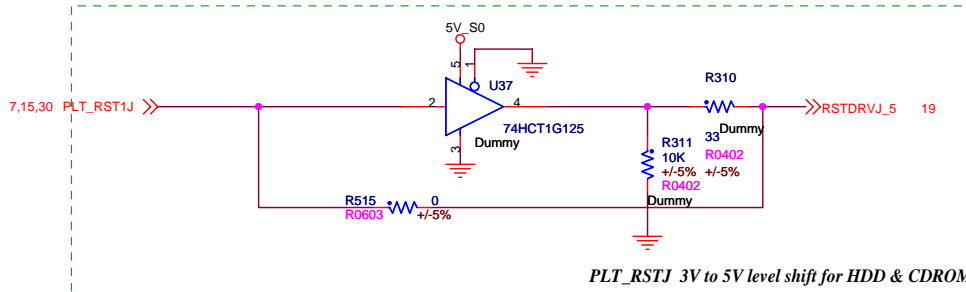
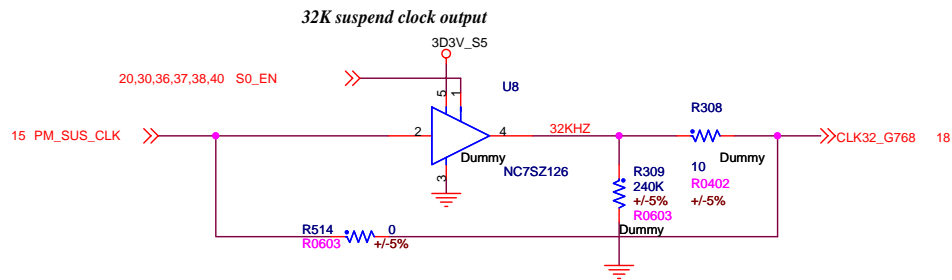
Layout Note:
Place near
pin AA19

Layout Note:
Place near
ICH6



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Title: **ICH6(4 of 4)**

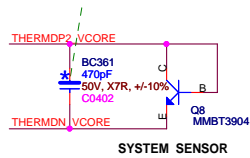
Document Number: **S09 MAINBOARD**

Date: Monday, March 14, 2005

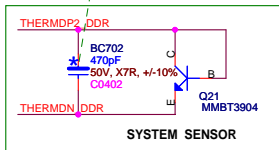
Sheet 17 of 45

Rev A

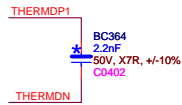
Put thisCap near the thermal diode.



Put thisCap near the thermal diode.



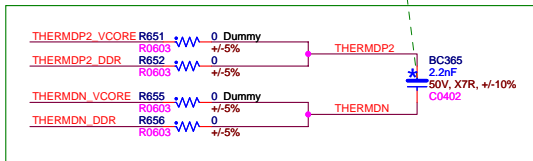
Another Thermal Group



THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

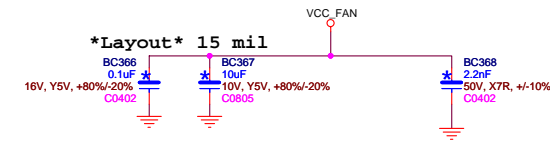
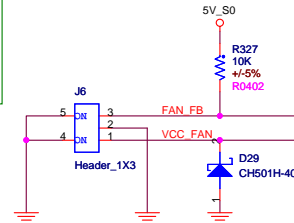
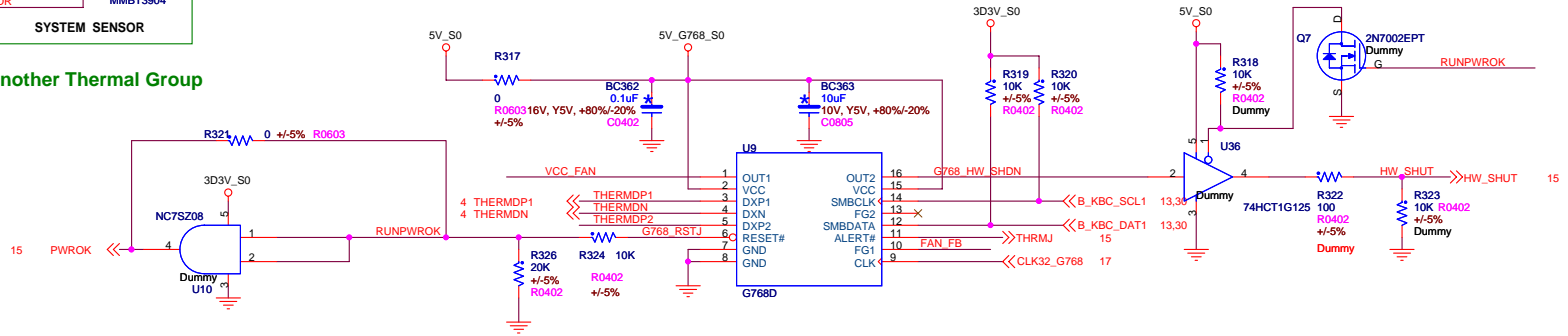
HW thermal shut down tempature
setting 95 degree . Put Near CPU .

Put these two Caps near U9

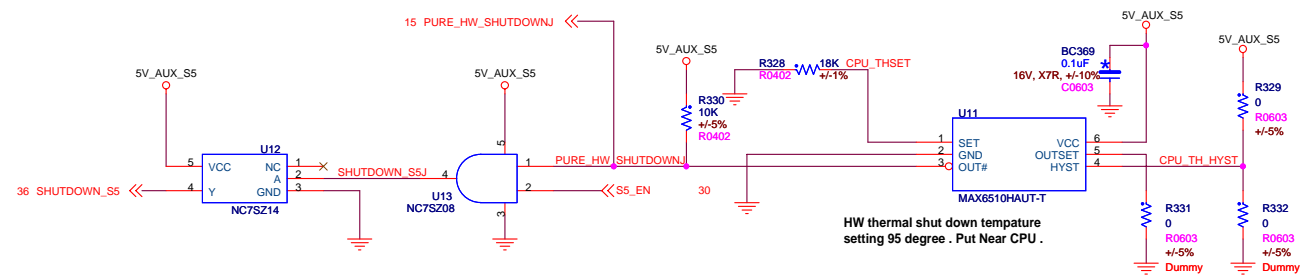


Thermal Group Option

Reserve for G768B
works at High
Speed

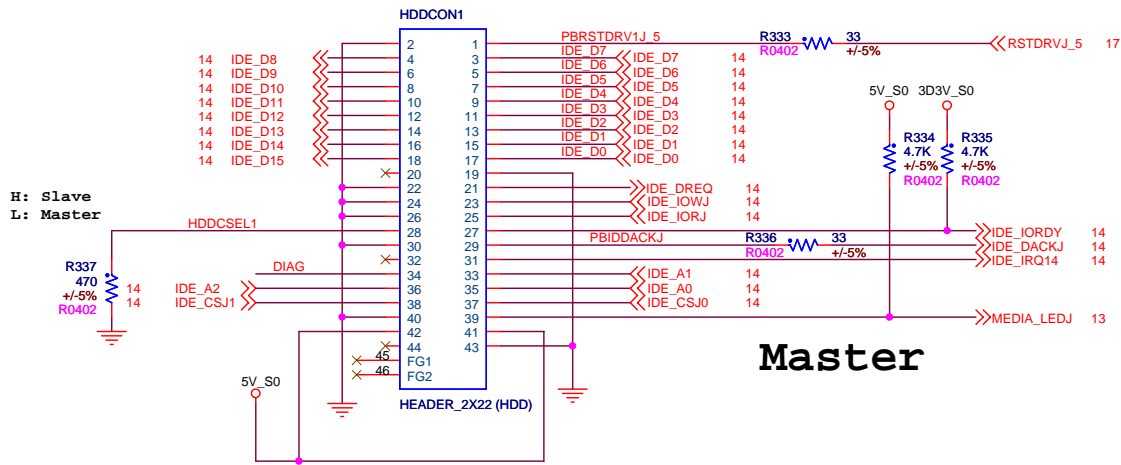


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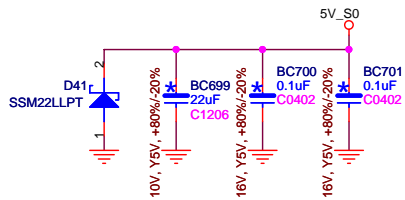


HW thermal shut down tempature
setting 95 degree . Put Near CPU .

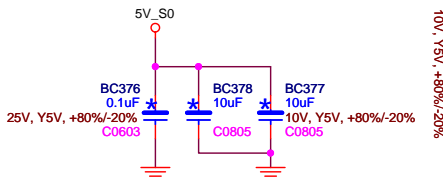
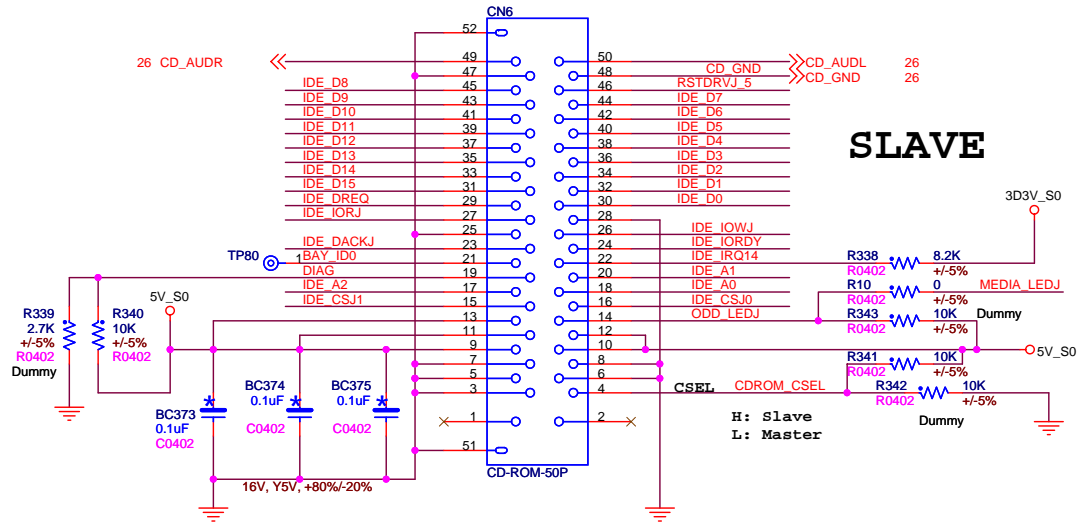
HDD Connector

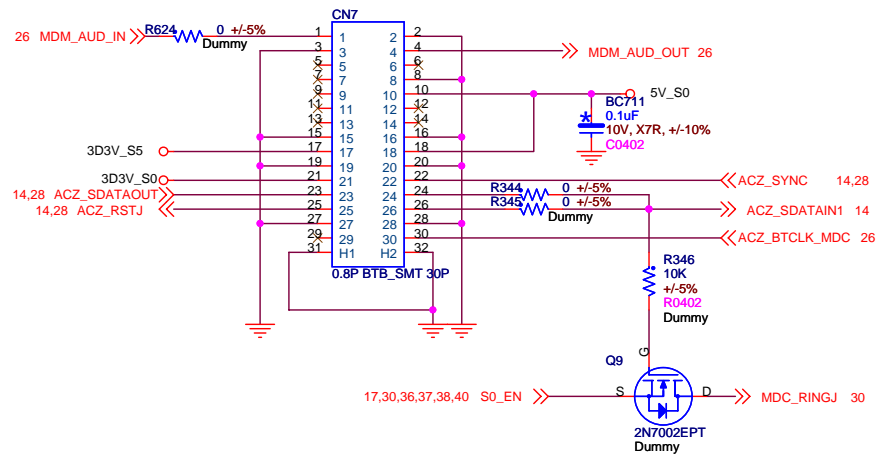


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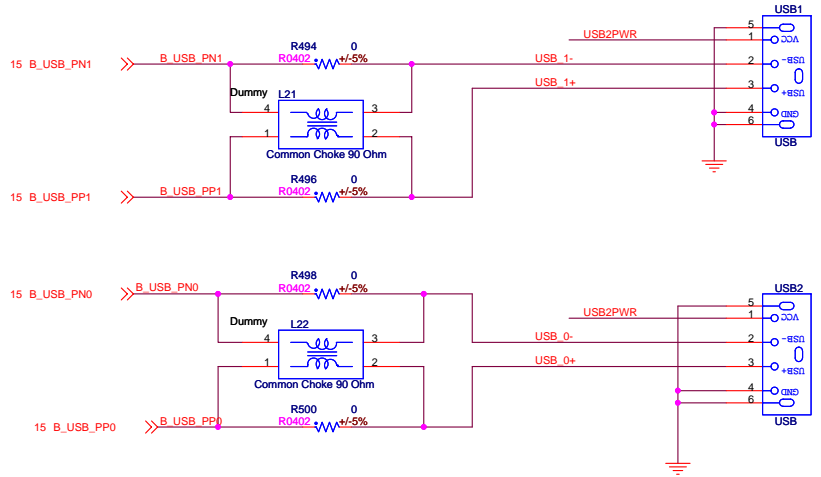
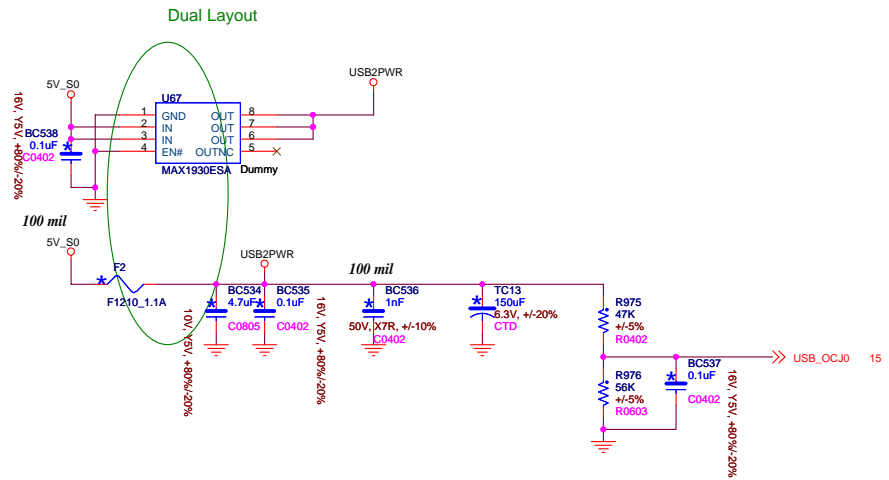
CDROM

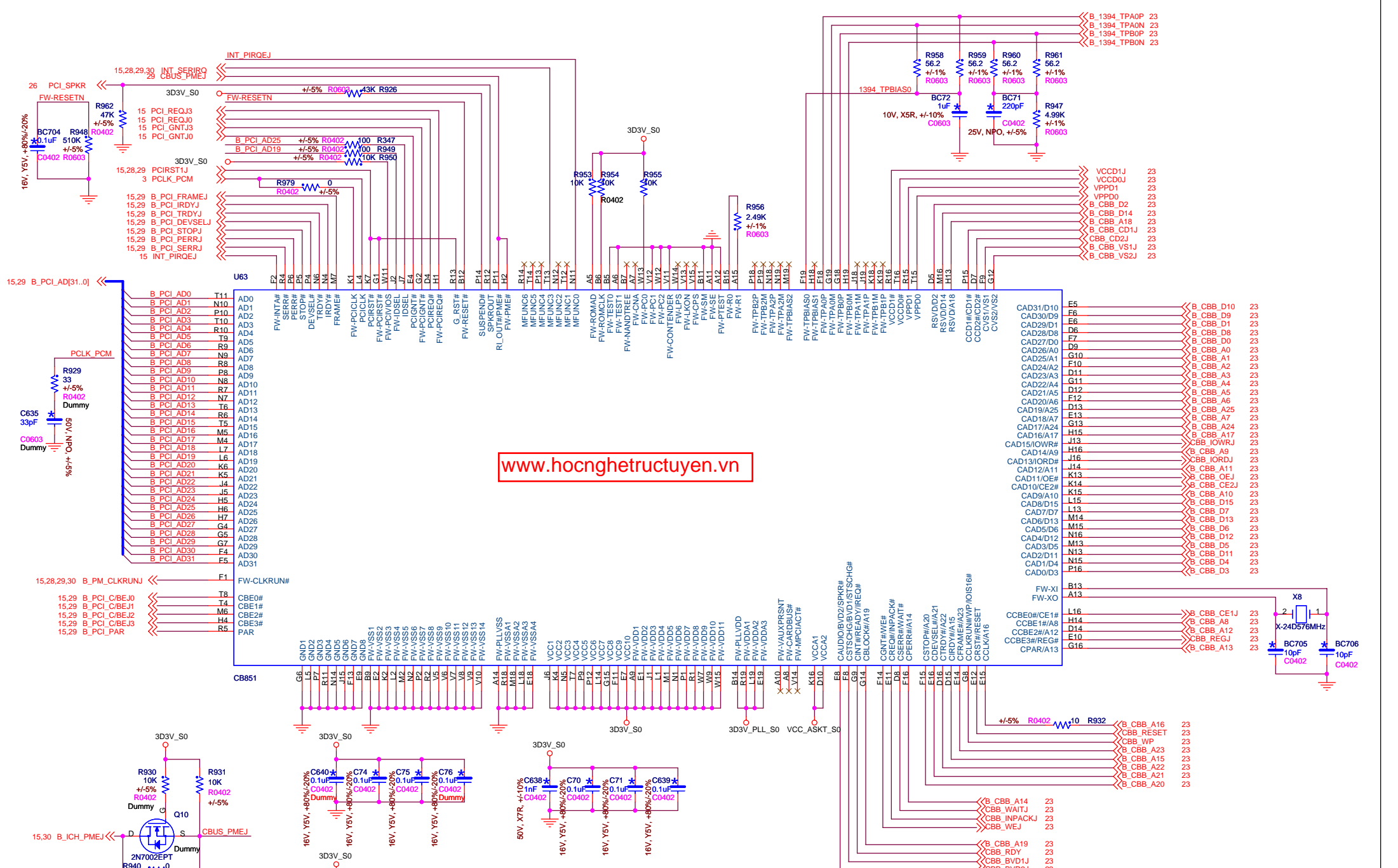




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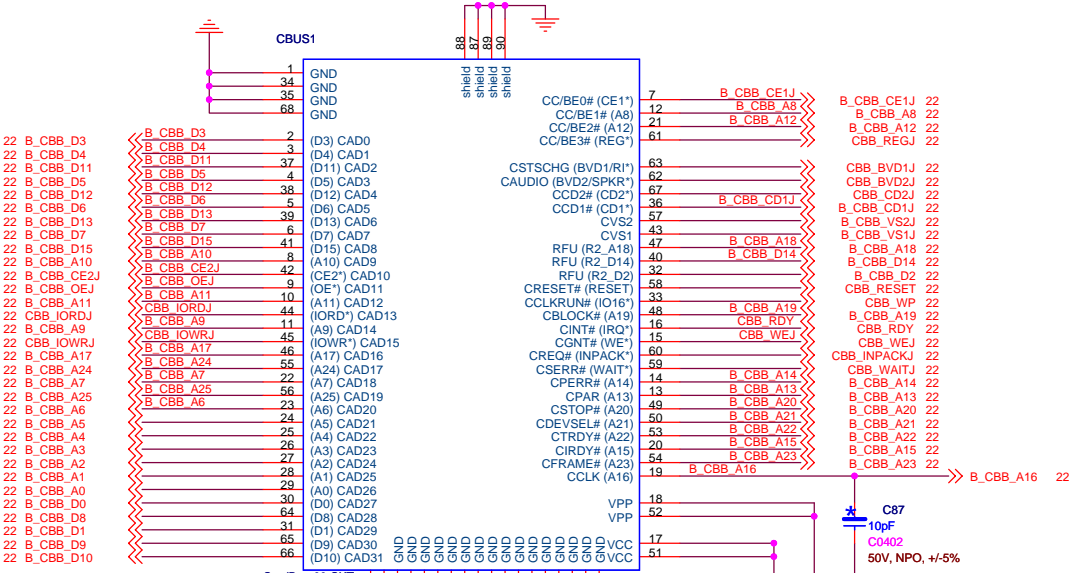
www.hocnghetructuyen.vn



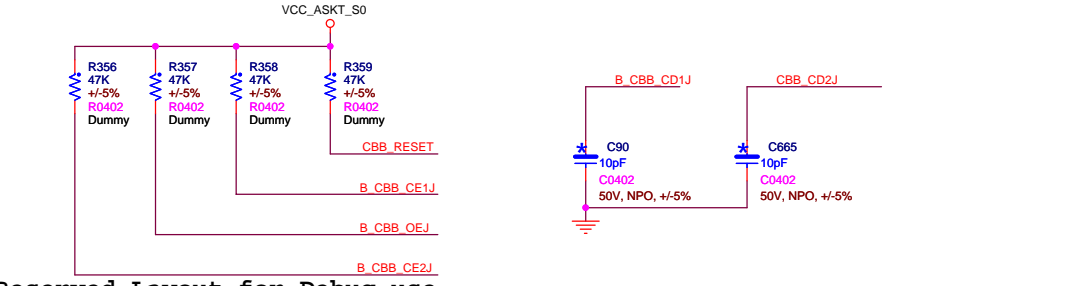
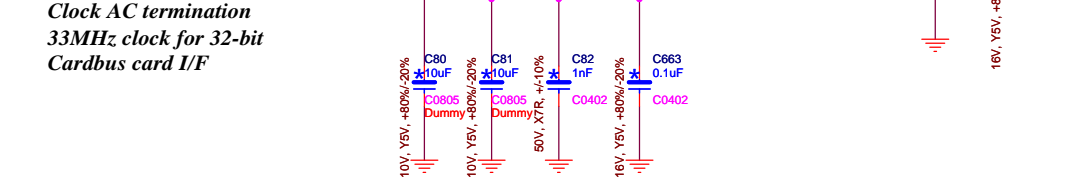
ENE CB851
 Document Number: S09
S09 MAINBOARD
 Date: Monday, March 14, 2005 Sheet 22 of 45
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PCMCIA Socket

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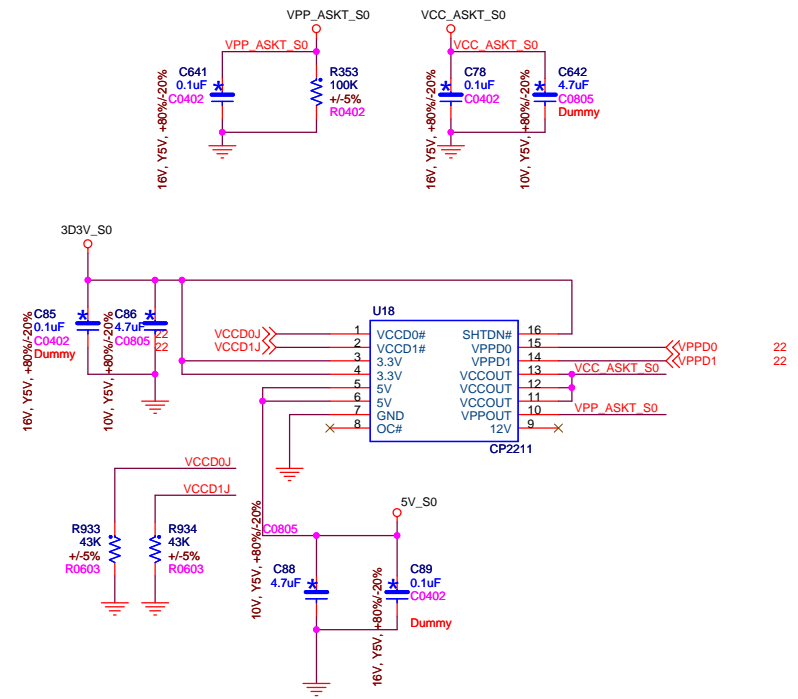


Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

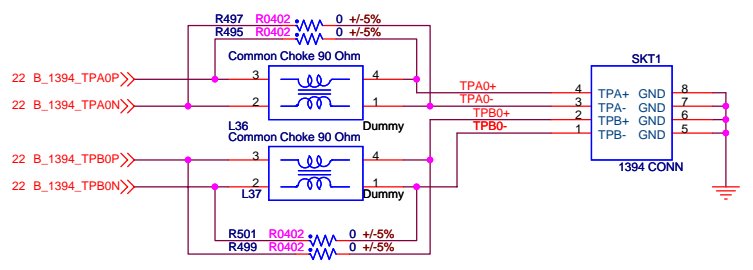


Reserved Layout for Debug use

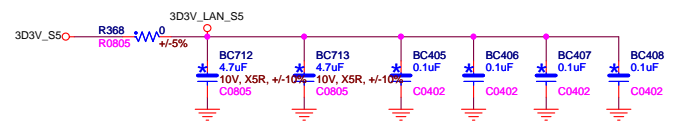
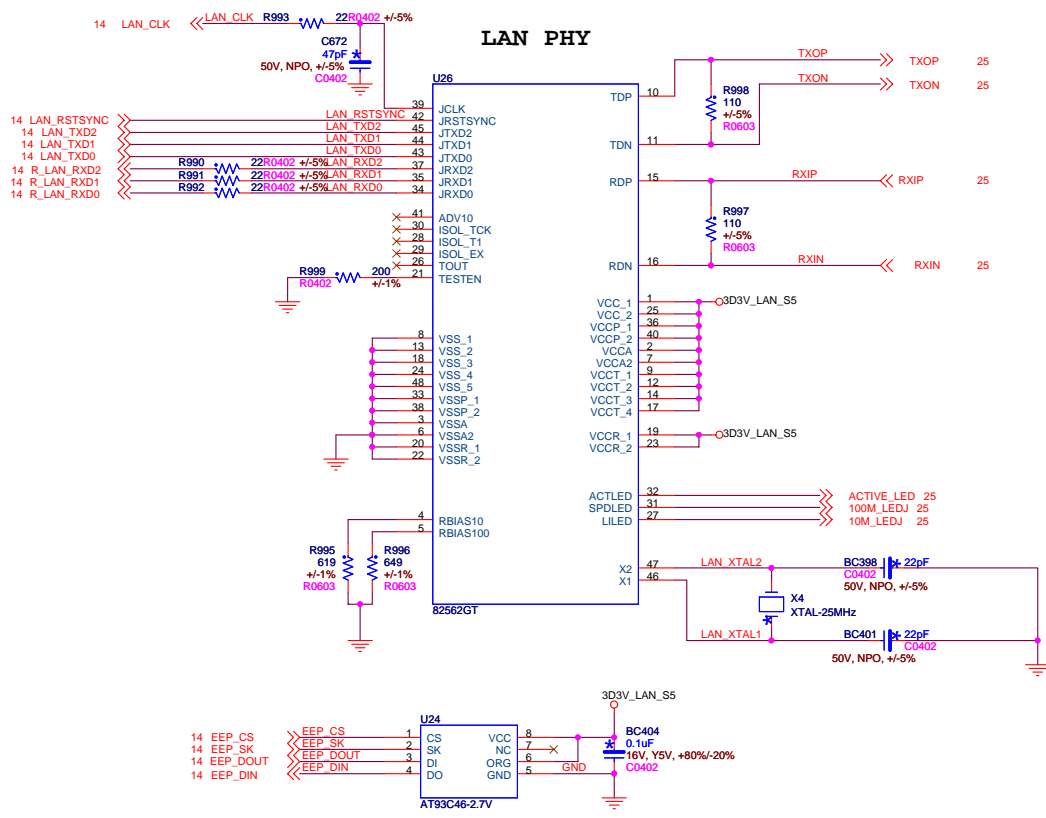
Power switch

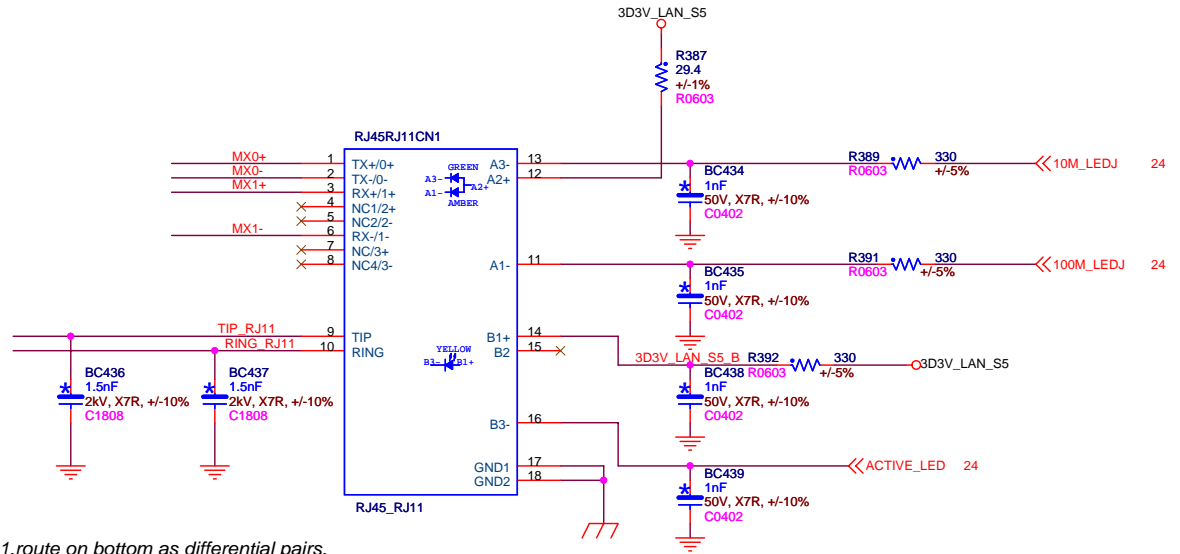
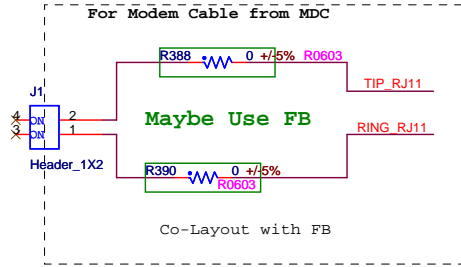


1394

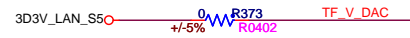
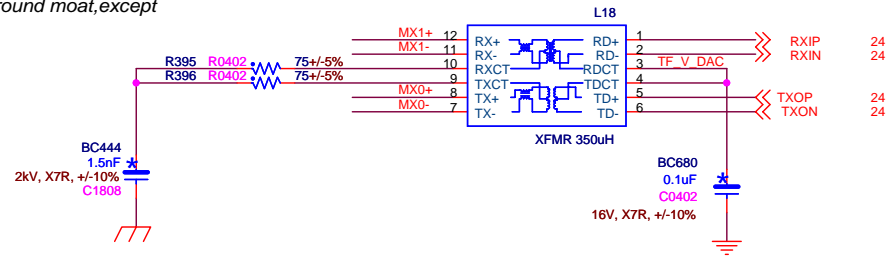
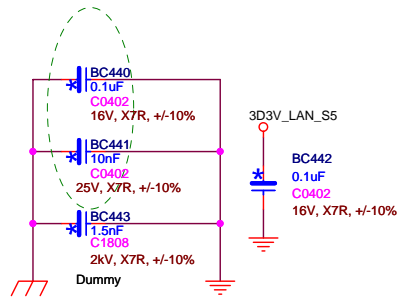


| | |
|---------------------------------------|----------------|
| FOXCONN TECHNOLOGY COPR. | |
| Title: PCMCIA/1394 | |
| Document Number: S09 MAINBOARD | |
| Date: Thursday, March 17, 2005 | Sheet 23 of 45 |
| Rev A | |





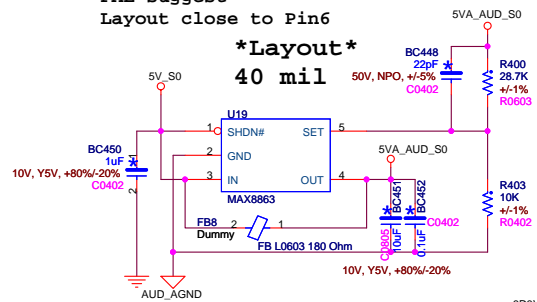
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



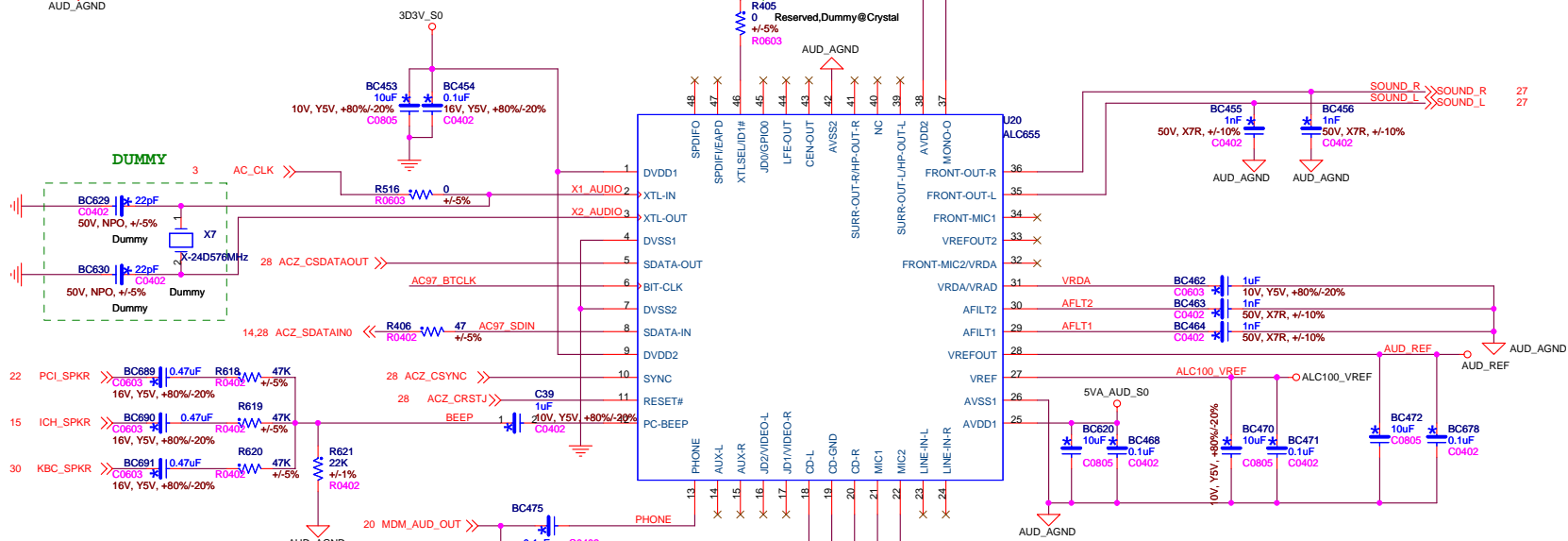
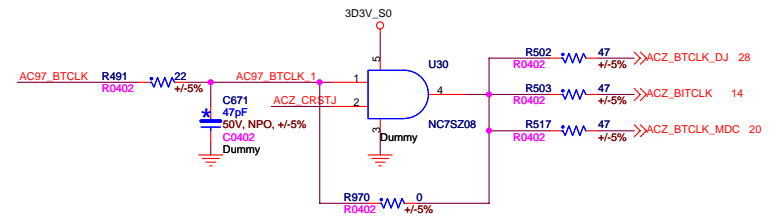
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FAE suggest
Layout close to Pin6

Layout
40 mil

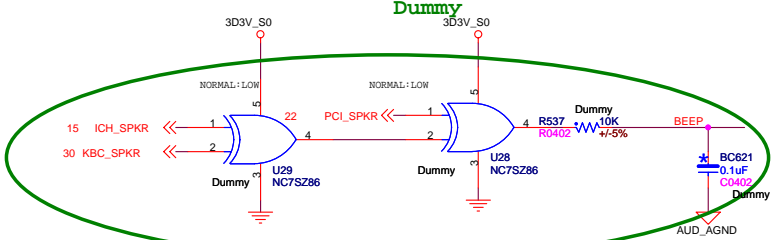


Low for external CLK
NC for Crystal



Layout
20 mil

If use this circuit, R621 change to 1K



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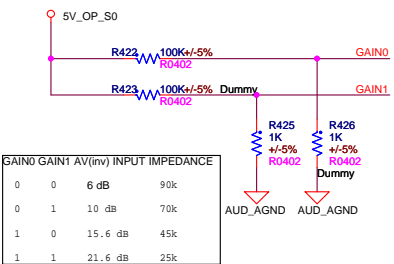
FOXCONN TECHNOLOGY COPR.

File
AUDIO_AC97_ALU655-U

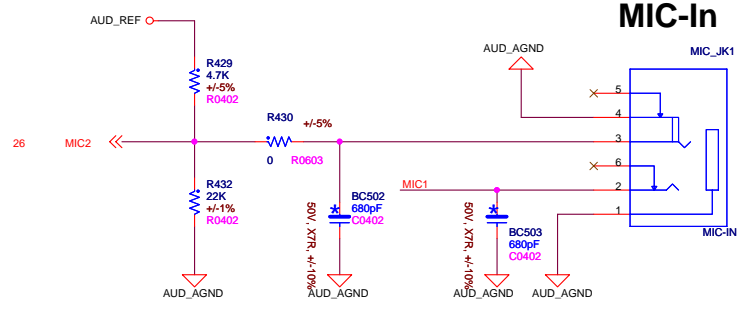
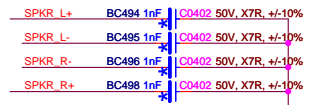
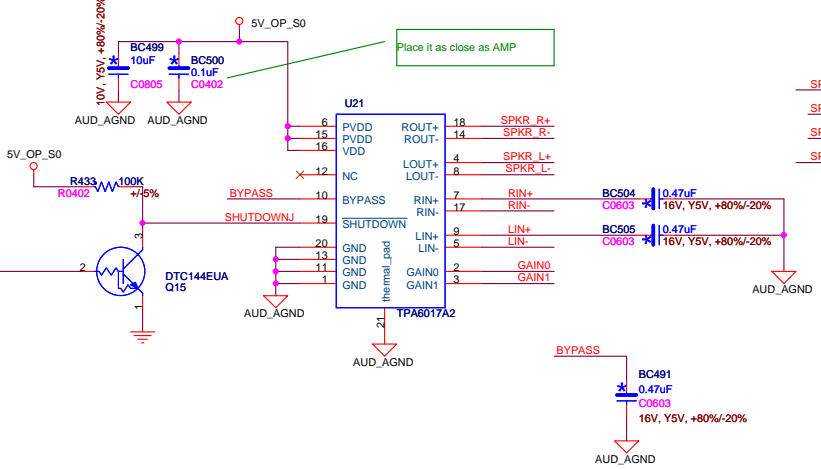
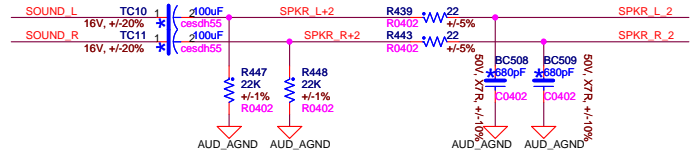
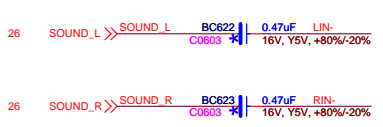
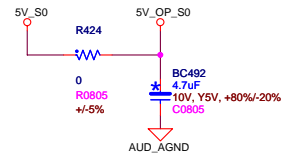
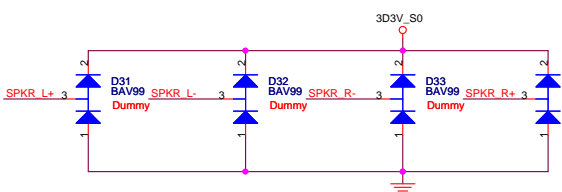
Document Number
S09 MAINBOARD

Date: Monday, March 14, 2005

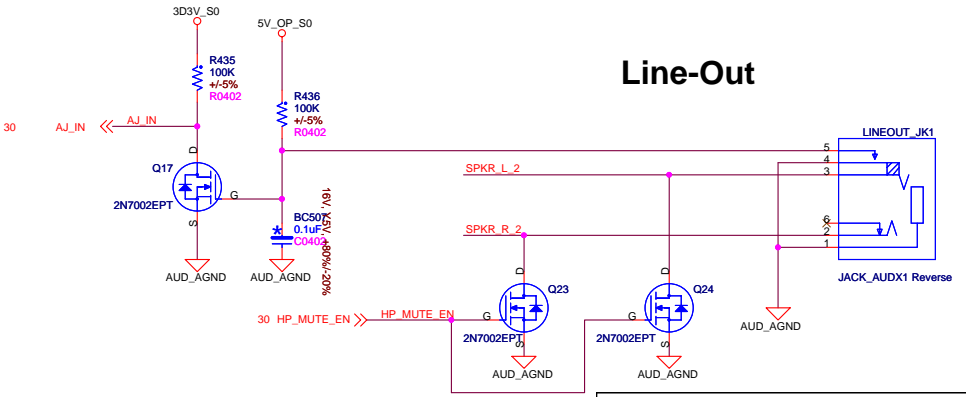
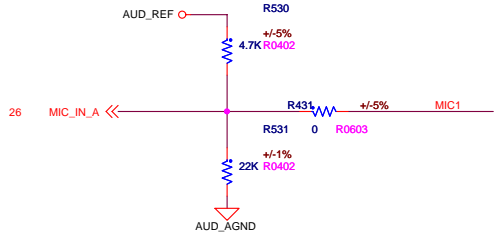
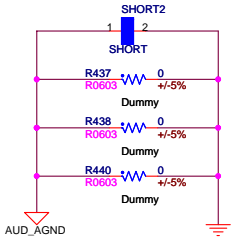
Sheet 26 of 45

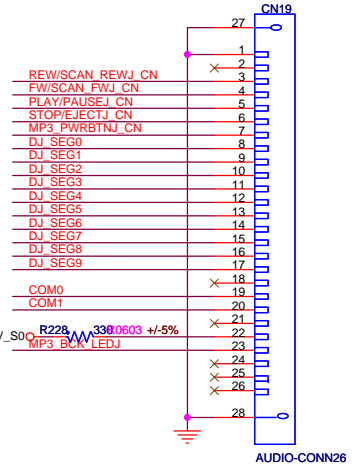
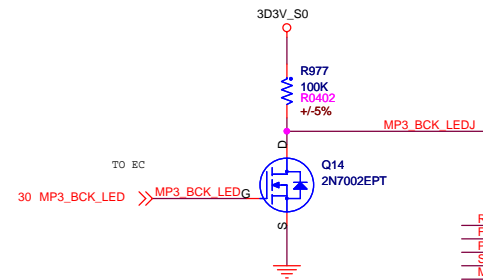
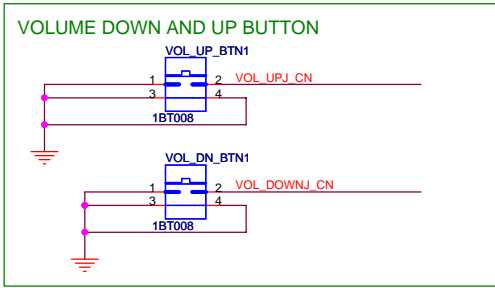


| GAIN0 | GAIN1 | AV(inv) | INPUT IMPEDANCE |
|-------|-------|---------|-----------------|
| 0 | 0 | 6 dB | 90k |
| 0 | 1 | 10 dB | 70k |
| 1 | 0 | 15.6 dB | 45k |
| 1 | 1 | 21.6 dB | 25k |

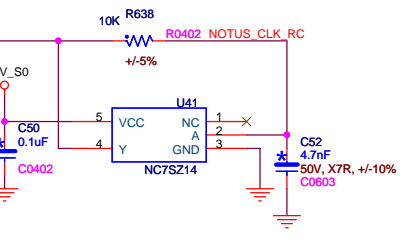
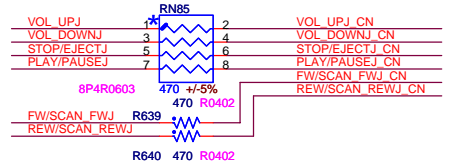
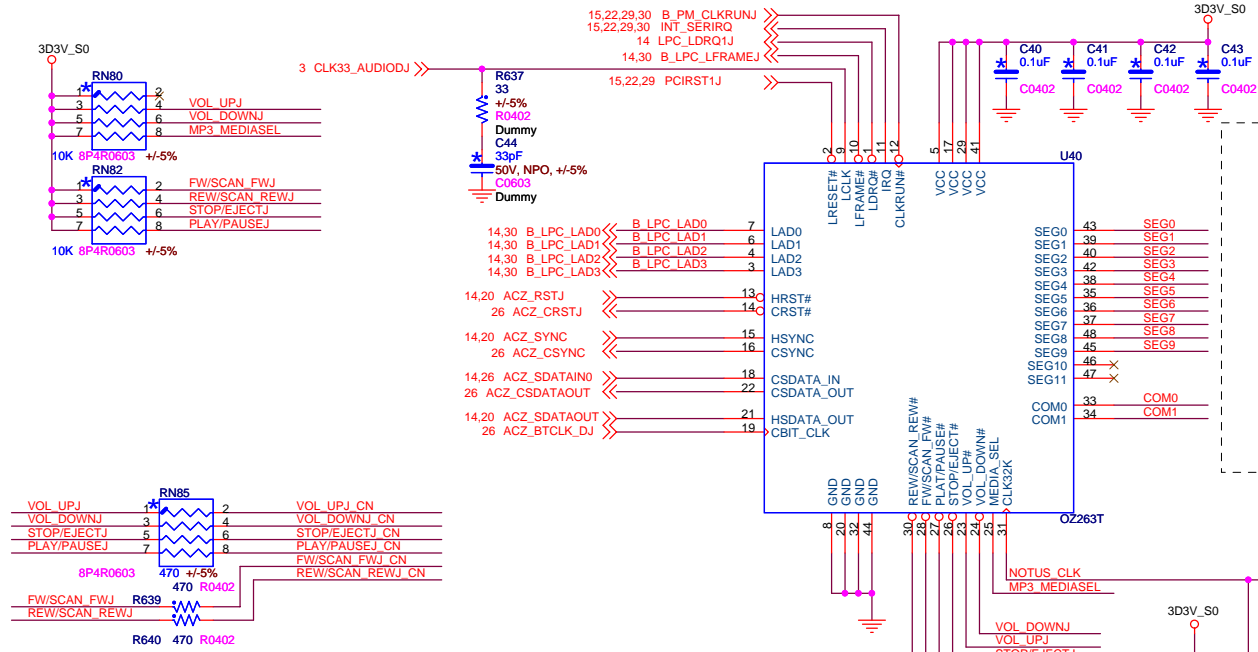
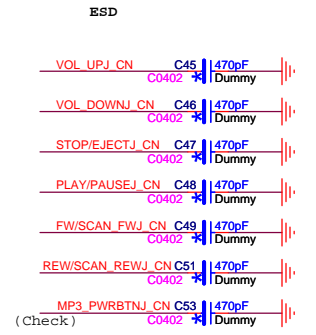


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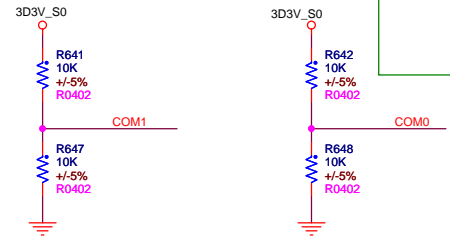
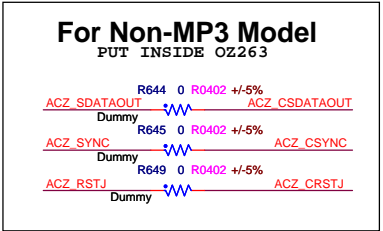
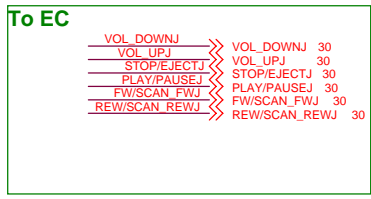




AudioDJ Connector



MP3 POWER BUTTON



15,22 B_PCI_AD[31..0]

30 RF_KILLJ



13 802.11_ACT

3D3V_S0

TP83

3 PCLK_MINI



BC482

33pF

50V, NPO, +/-5%

C0603

Dummy

15 PCI_REQJ1

15,22 B_PCI_C/BEJ3

15,22 B_PCI_C/BEJ2

15,22 B_PCI_IRDYJ

15,22,28,30 B_PM_CLKRUNJ

15,22 B_PCI_SERRJ

15,22 B_PCI_PERRJ

15,22 B_PCI_C/BEJ1

15,22 B_PCI_C/BEJ0

5V_S0

3D3V_S0

BC483

0.1uF

C0402

Dummy

BC484

0.1uF

C0402

Dummy

BC485

0.1uF

C0402

Dummy

BC486

0.1uF

C0402

Dummy

BC487

0.1uF

C0402

Dummy

BC488

0.1uF

C0402

Dummy

BC489

4.7uF

10V, Y5V, +80%/-20%

C0805

Dummy

5V_S0

BC490

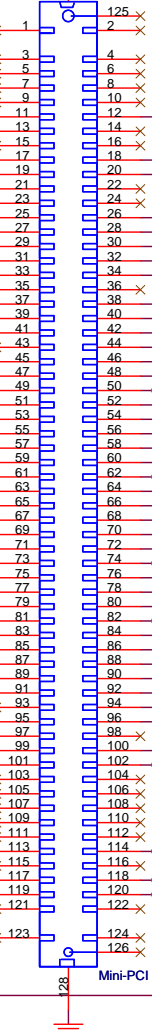
4.7uF

10V, Y5V, +80%/-20%

C0805

Dummy

MINI1



PIN 3-16 : LAN RESERVE

802.11_LINK 13

5V_S0

INT_PIRQJ

PCI_RST1J

3D3V_S0

PCI_GNTJ1

CBUS_PMEJ

B_PCI_AD30

B_PCI_AD28

B_PCI_AD26

B_PCI_AD24

MOD_IDSEL

B_PCI_AD22

B_PCI_AD20

B_PCI_PAR

B_PCI_AD18

B_PCI_AD16

B_PCI_FRAMEJ

B_PCI_TRDYJ

B_PCI_STOPJ

B_PCI_DEVSELJ

B_PCI_AD15

B_PCI_AD13

B_PCI_AD11

B_PCI_AD9

B_PCI_C/BEJ0

B_PCI_AD6

B_PCI_AD4

B_PCI_AD2

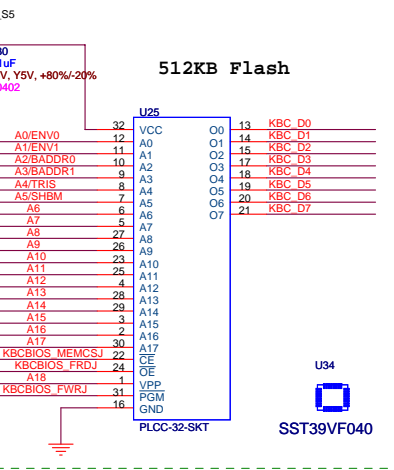
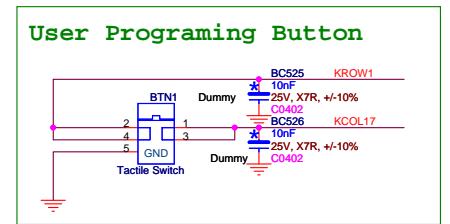
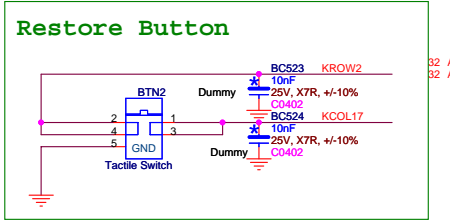
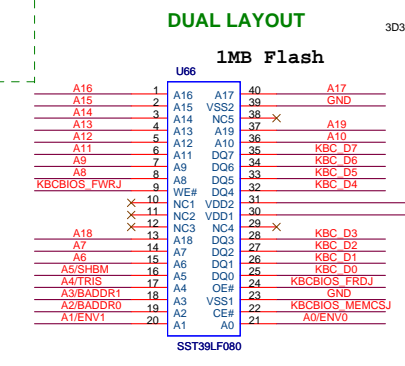
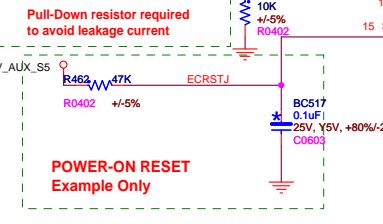
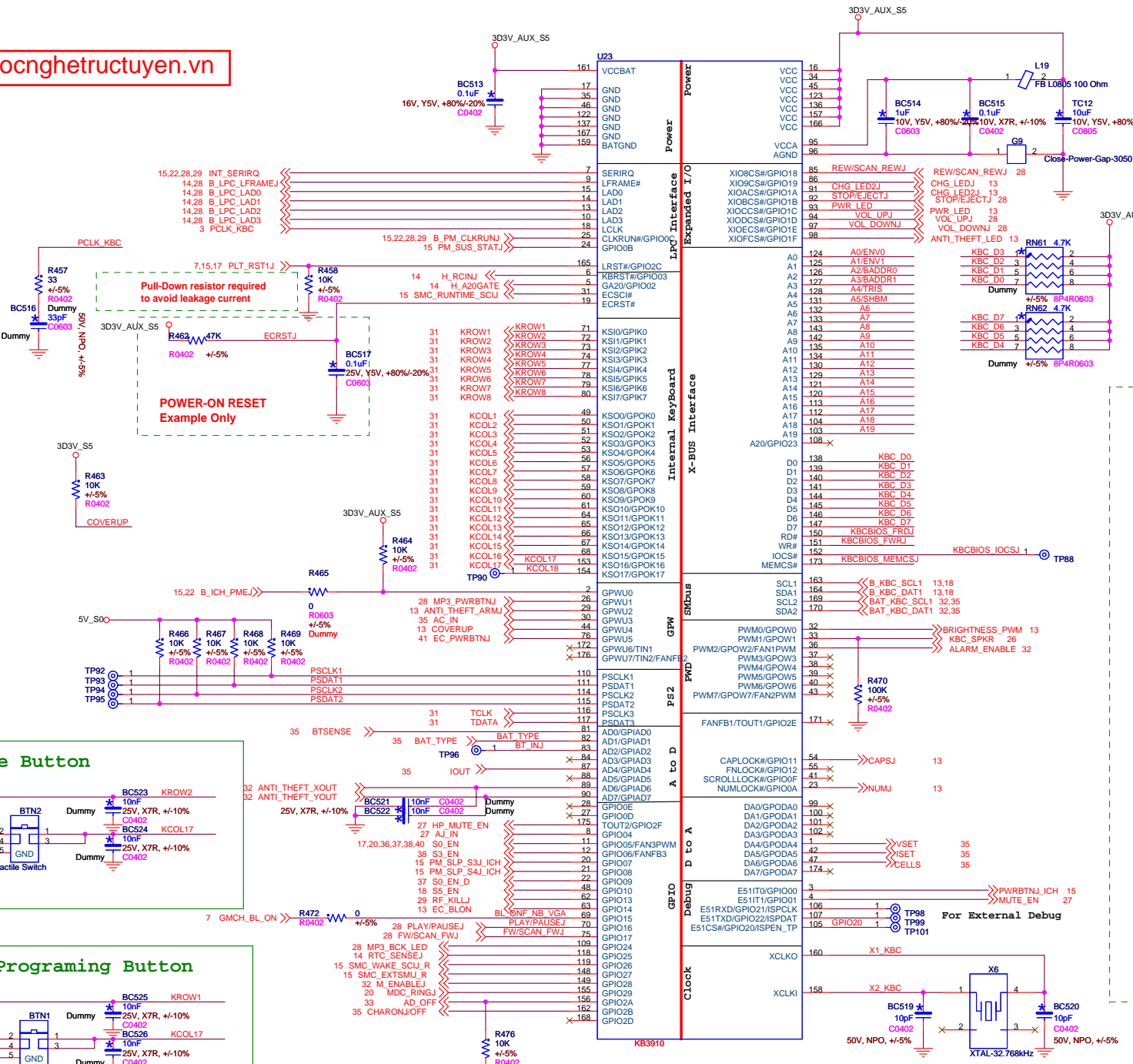
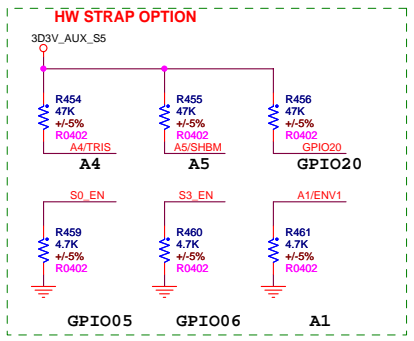
B_PCI_AD0

INT_SERIRQ

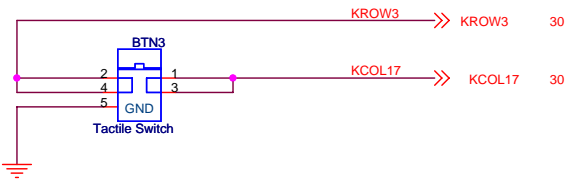
Mini-PCI

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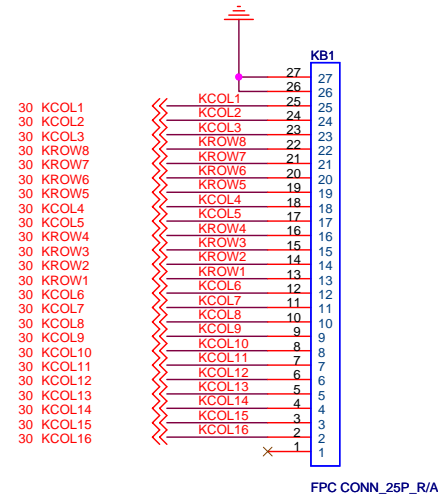




ENABLE/DISABLE TOUCH PAD BUTTON

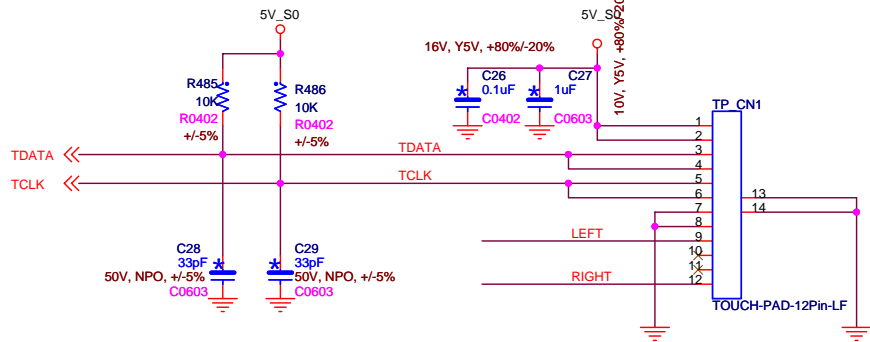


Internal KeyBoard Connector



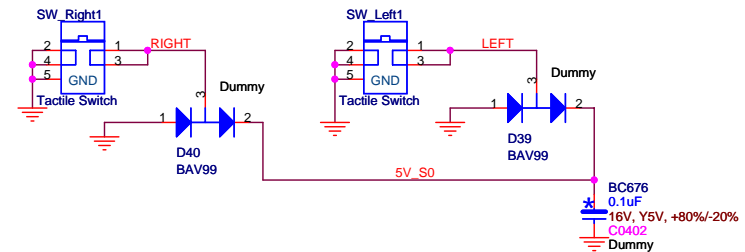
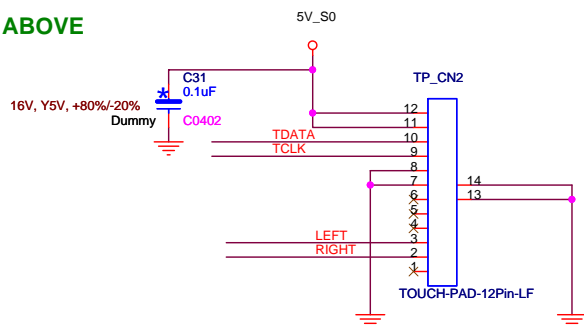
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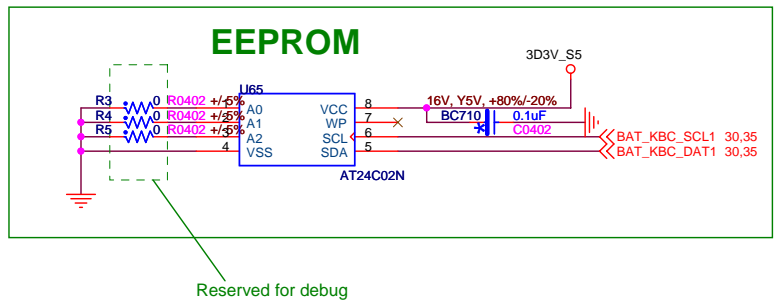
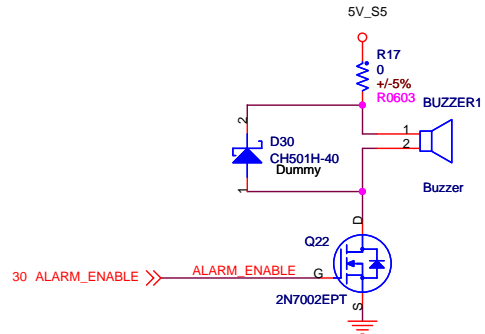
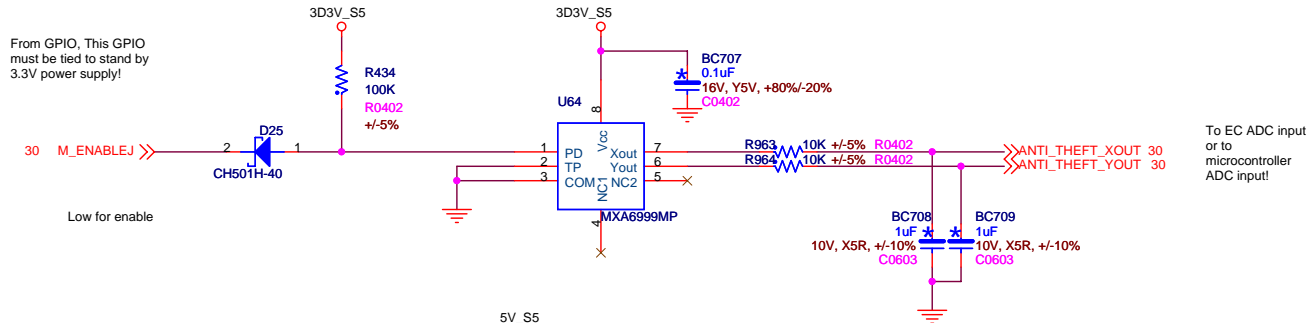
TouchPad Connector For Module TM42PU-351 (UP Orientation)



TouchPad Connector For Module TM51-389(Up Orientation)

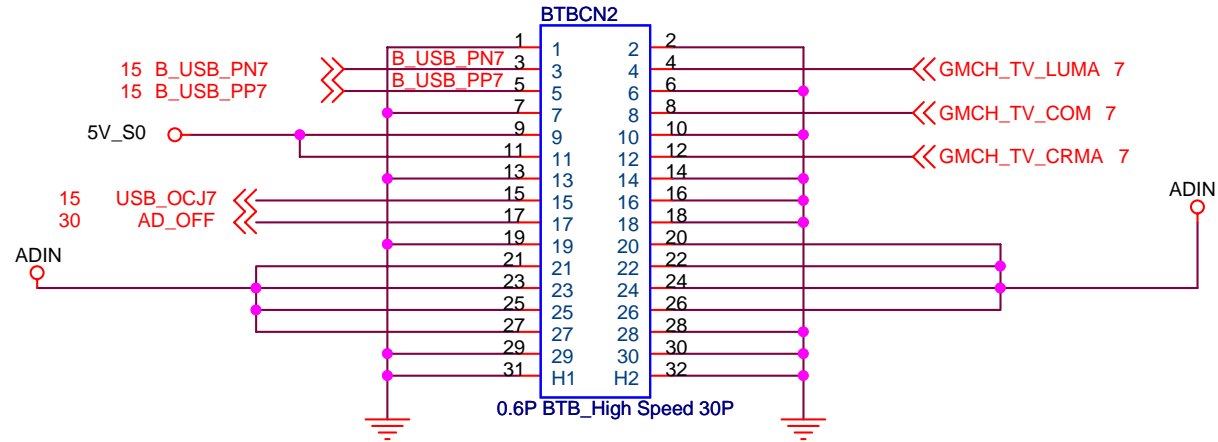
DUAL LAYOUT WITH ABOVE





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Board To Board CONN

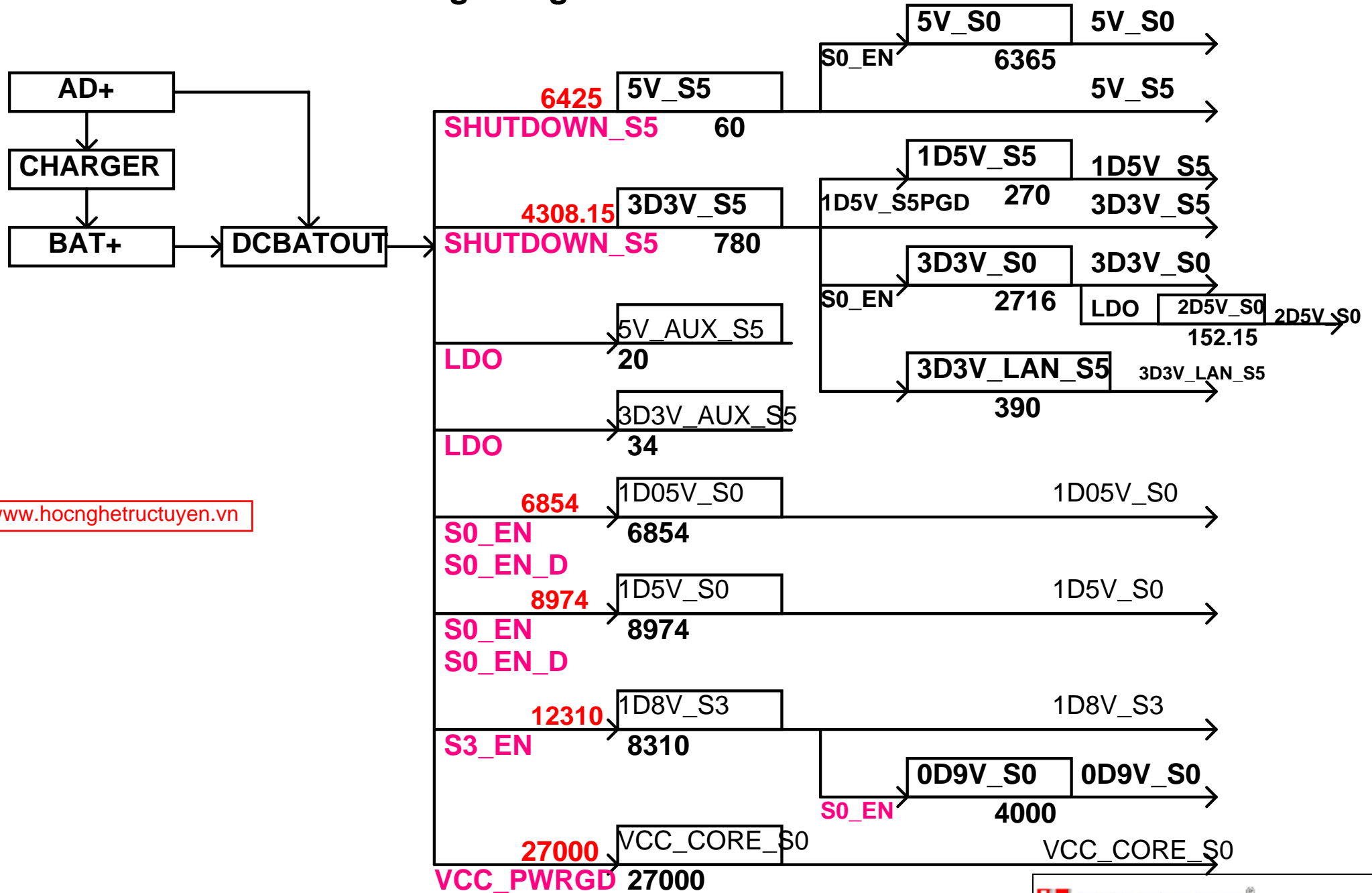


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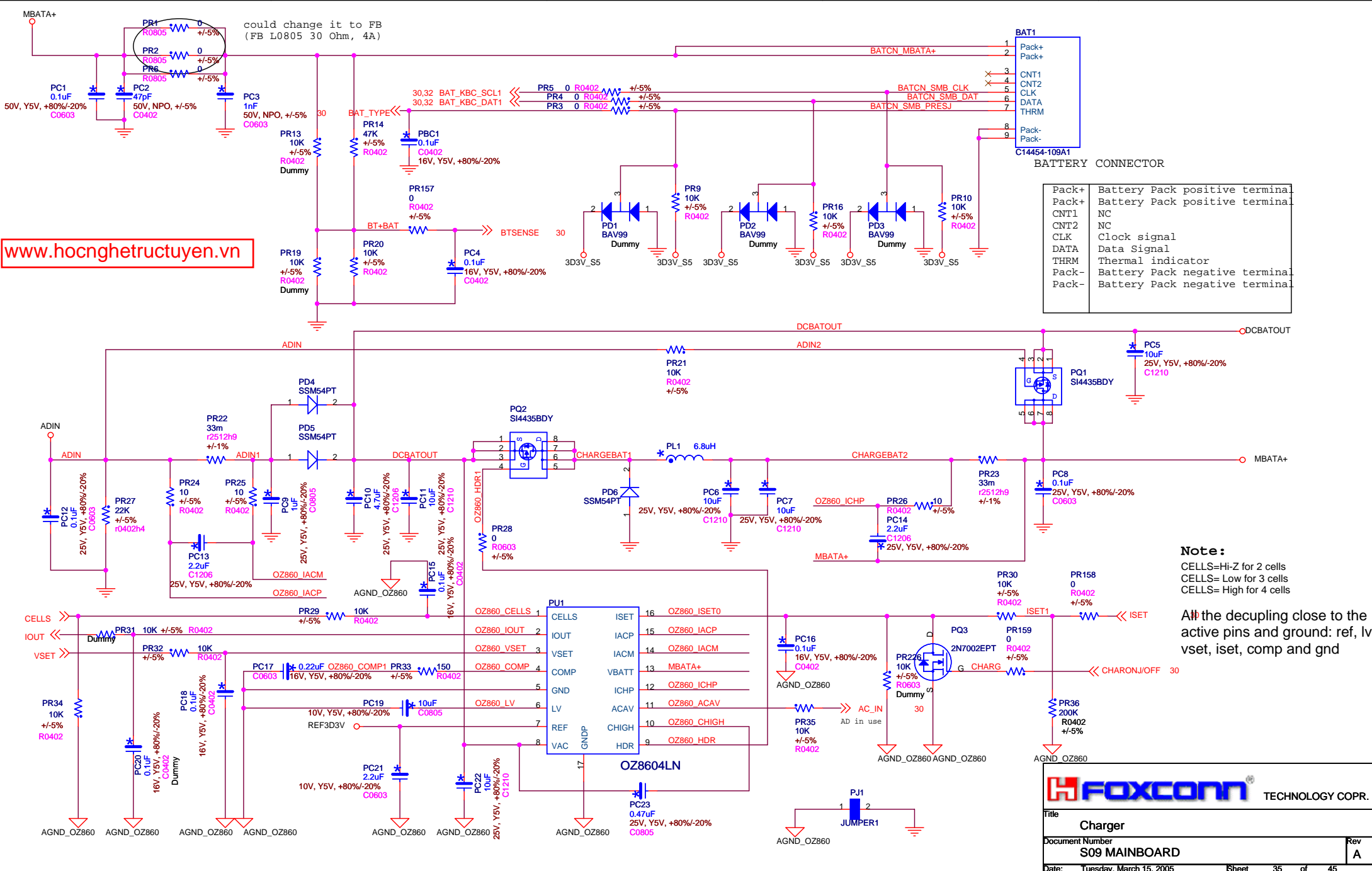
| | | | |
|-----------------|---------------------------|----------------------------|----------|
| Title | | Board To Board CONN | |
| Document Number | | S09 MAINBOARD | |
| Date: | Wednesday, March 16, 2005 | Sheet | 33 of 45 |
| | | Rev | A |

Power design diagram

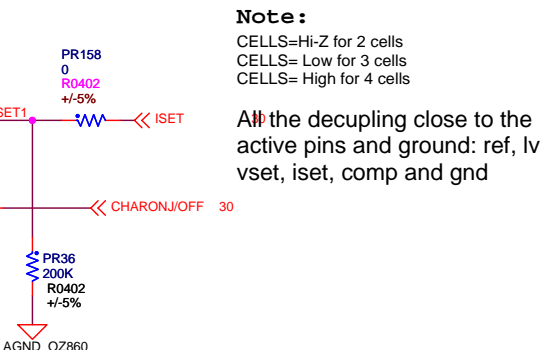
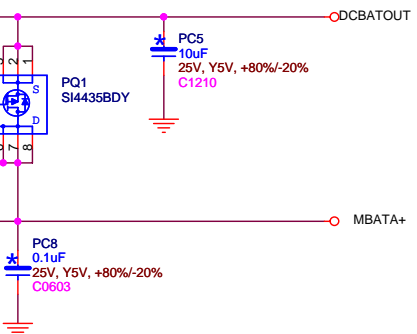


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| | |
|-------|--------------------------------|
| Pack+ | Battery Pack positive terminal |
| Pack- | Battery Pack positive terminal |
| CNT1 | NC |
| CNT2 | NC |
| CLK | Clock signal |
| DATA | Data Signal |
| THRM | Thermal indicator |
| Pack- | Battery Pack negative terminal |
| Pack- | Battery Pack negative terminal |



FOXCONN TECHNOLOGY COPR.

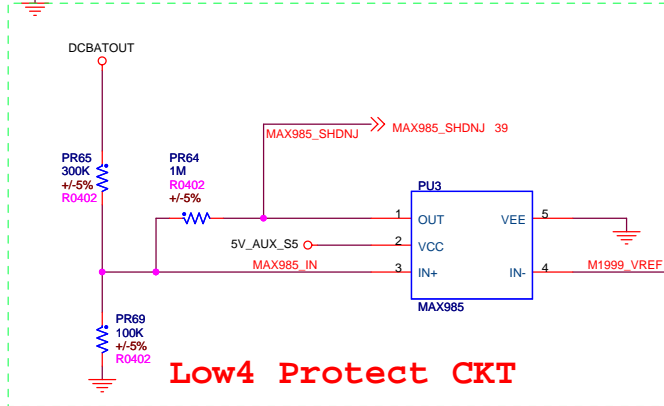
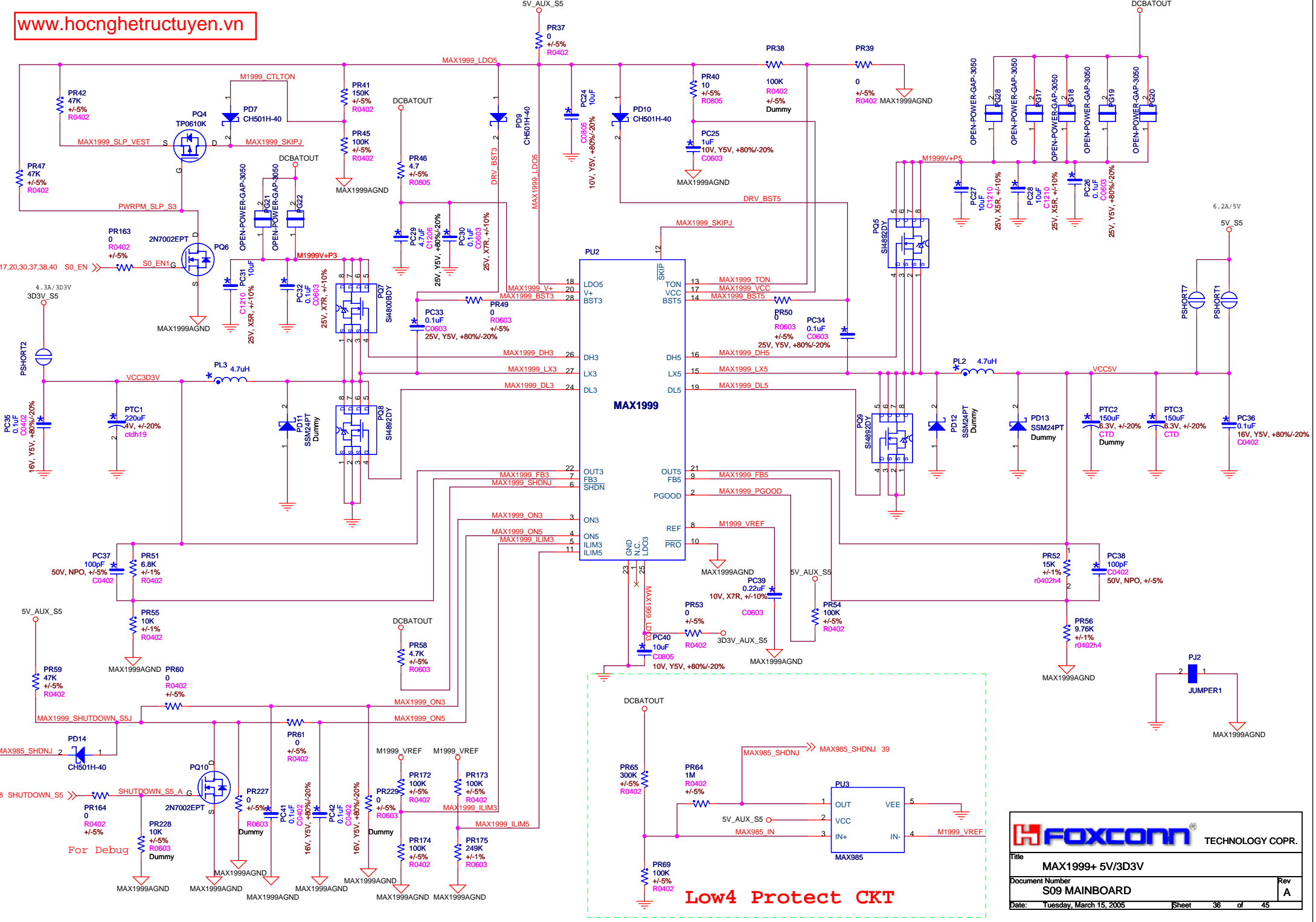
Title: **Charger**

Document Number: **S09 MAINBOARD**

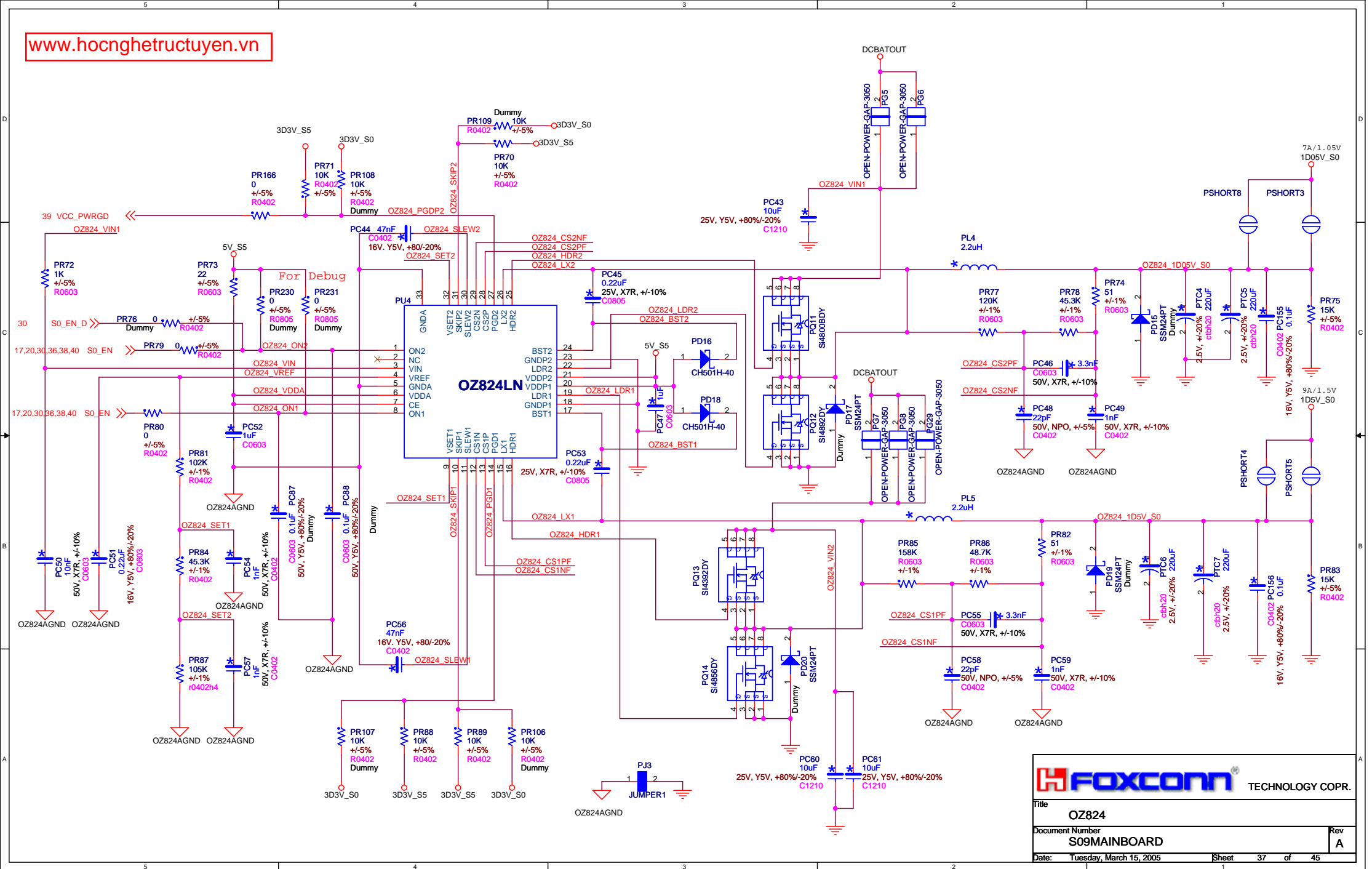
Date: Tuesday, March 15, 2005

Sheet: 35 of 45

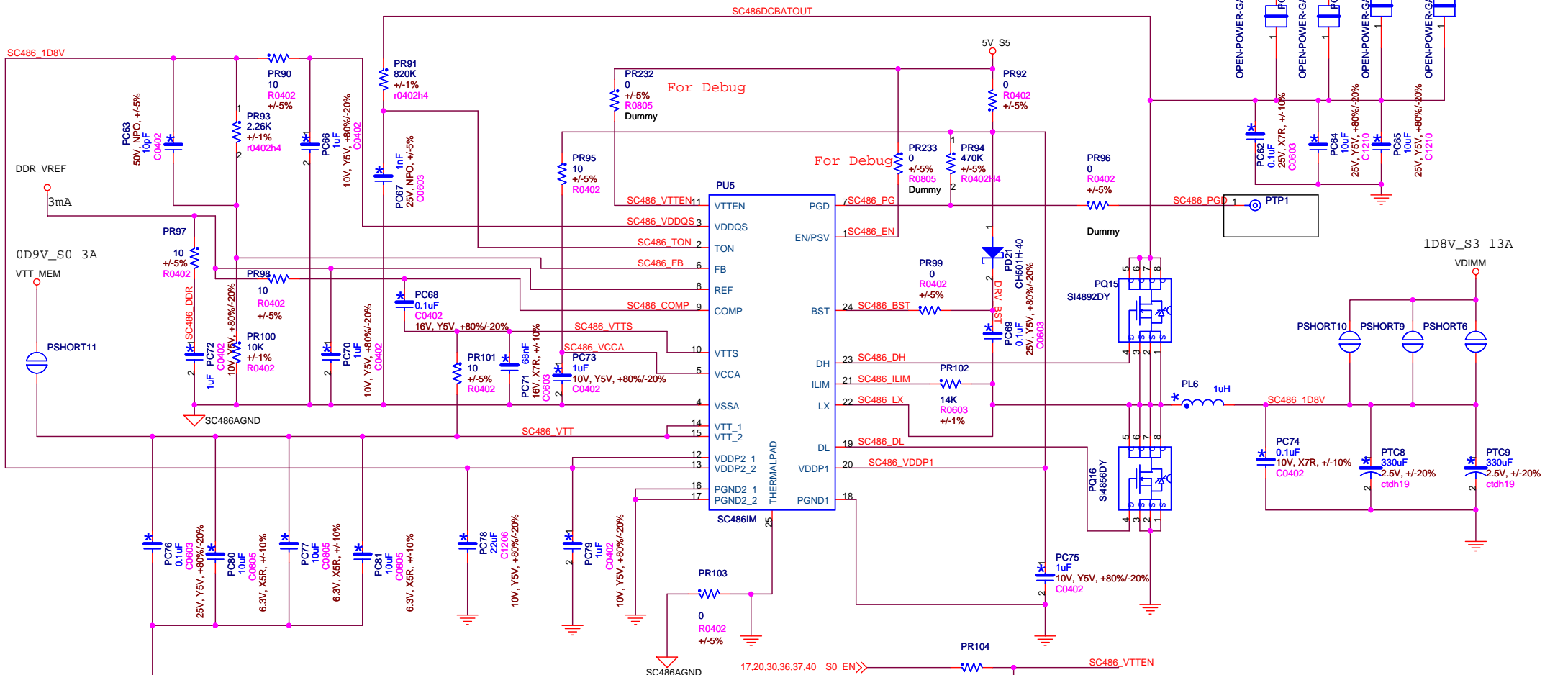
Rev: **A**



| | |
|--------------------------------|-----------------|
| | |
| Title: MAX1999+ 5V/3D3V | |
| Document Number: S09 MAINBOARD | Rev: A |
| Date: Tuesday, March 15, 2005 | Sheet: 36 of 45 |



| | |
|--|-------------------|
| Title OZ824 | |
| Document Number S09MAINBOARD | |
| Date: Tuesday, March 15, 2005 | Sheet 37 of 45 |
| Rev A | |



| VDIMM/EN | VTT_MEM/EN | VDIMM | VTT_MEM | VREF |
|----------|------------|-------|---------|------|
| 0 | 0 | X | X | X |
| 0 | 1 | X | X | X |
| 1 | 0 | 1.8 | X | 0.9 |
| 1 | 1 | 1.8 | 0.9 | 0.9 |

FOXCONN TECHNOLOGY COPR.

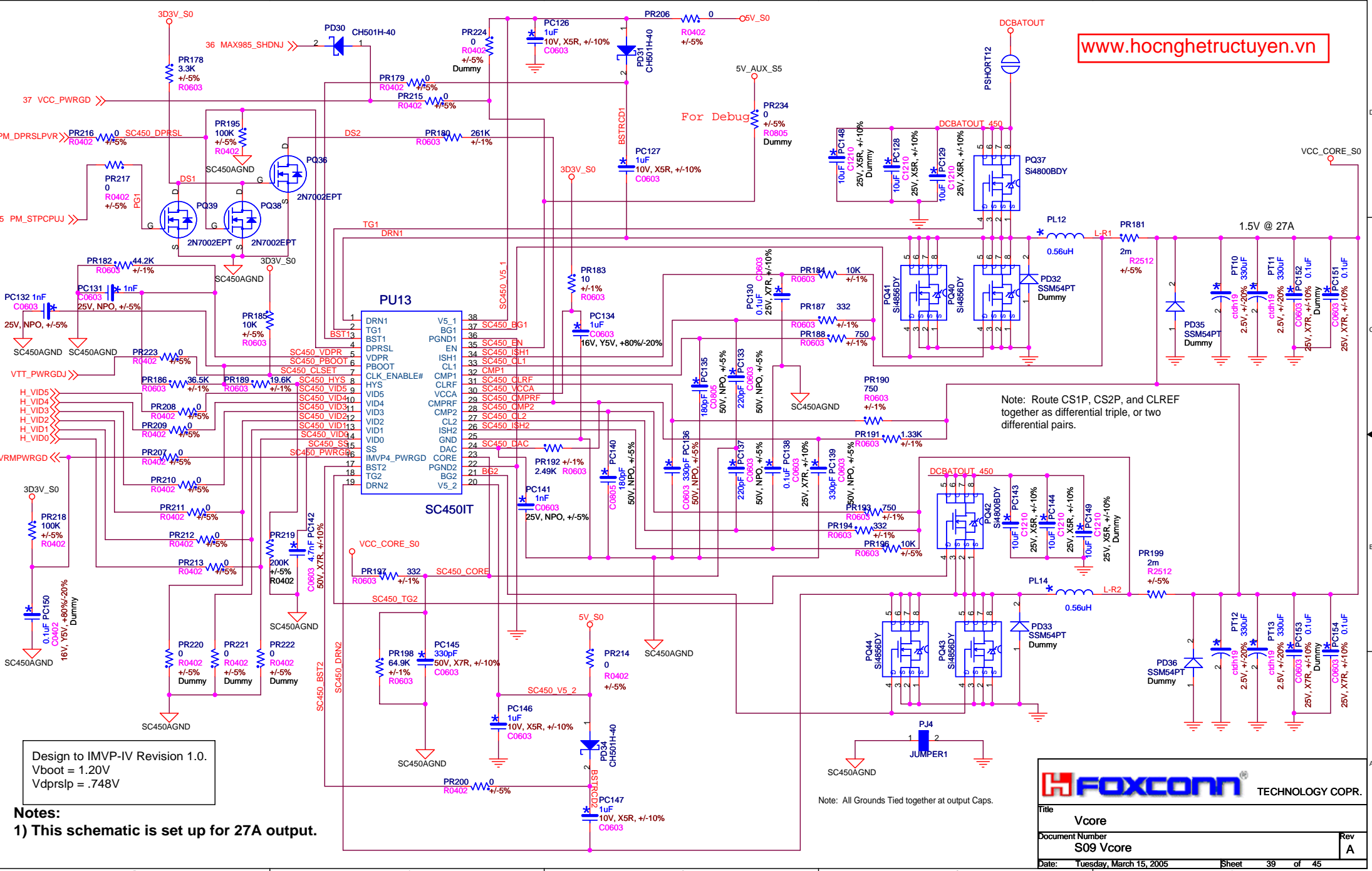
Title: SC486(1D8V-S3&0D9V-S0)

Document Number: S09 MAINBOARD

Date: Tuesday, March 15, 2005

Sheet 38 of 45

Rev A



Design to IMVP-IV Revision 1.0.
 Vboot = 1.20V
 Vdprslp = .748V

Notes:
 1) This schematic is set up for 27A output.

Note: Route CS1P, CS2P, and CLREF together as differential triple, or two differential pairs.

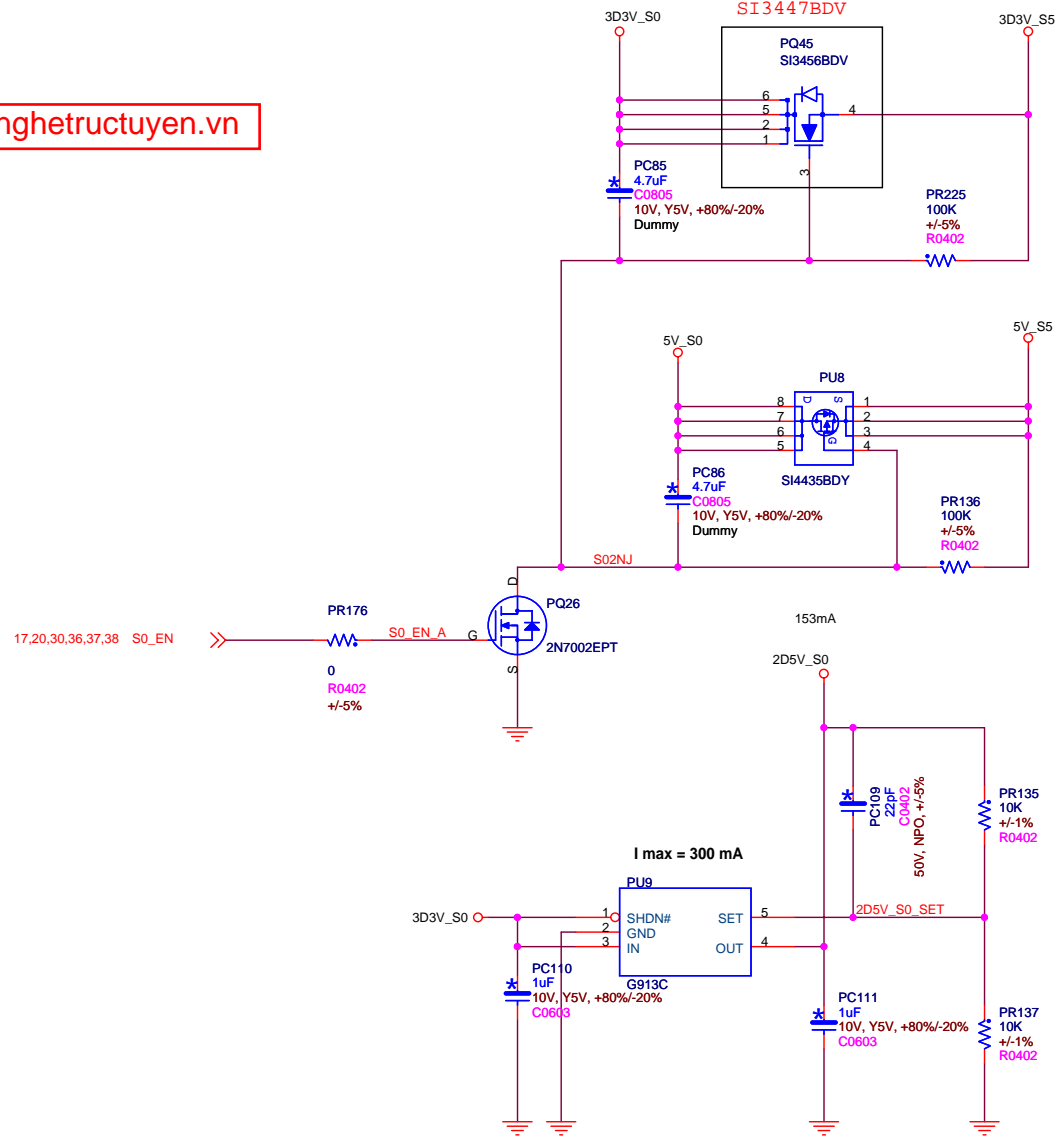
Note: All Grounds Tied together at output Caps.

FOXCONN TECHNOLOGY COPR.

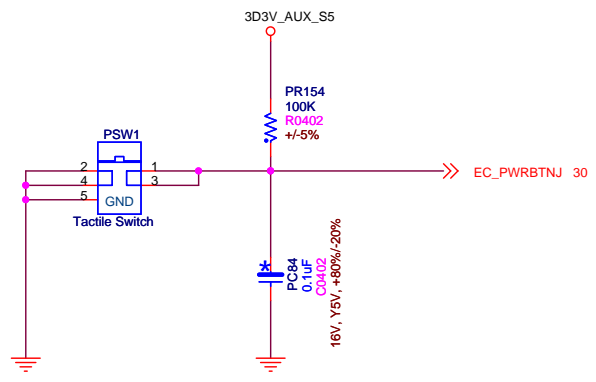
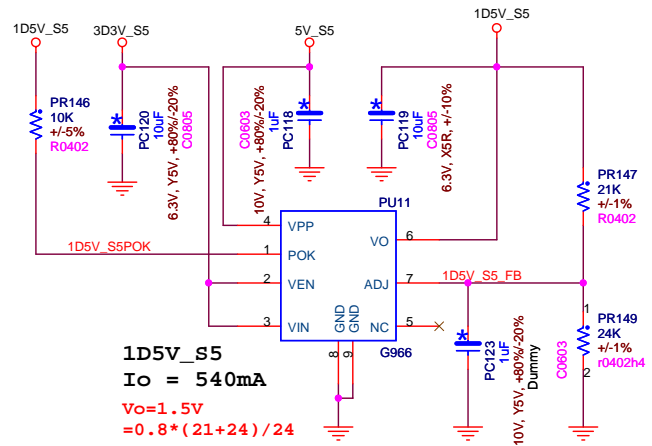
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|-----------------|-------------------------|-------|----------|
| Title | Vcore | Rev | A |
| Document Number | S09 Vcore | | |
| Date: | Tuesday, March 15, 2005 | Sheet | 39 of 45 |

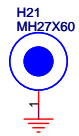
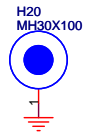
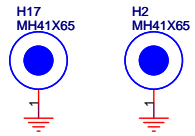
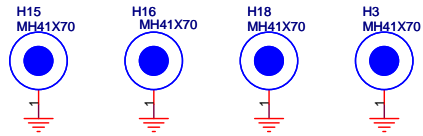
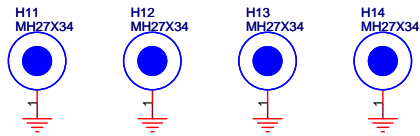
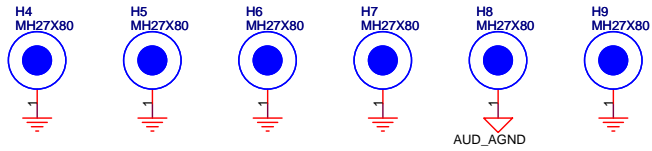
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暂时使用此零件
待申请完后再用
SI3447BDV



| | |
|---------------------------------|--------|
| FOXCONN TECHNOLOGY CORP. | |
| Title: Other power | |
| Document Number: S09 MAINBOARD | |
| Date: Tuesday, March 15, 2005 | Rev: A |
| Sheet: 40 | of 45 |

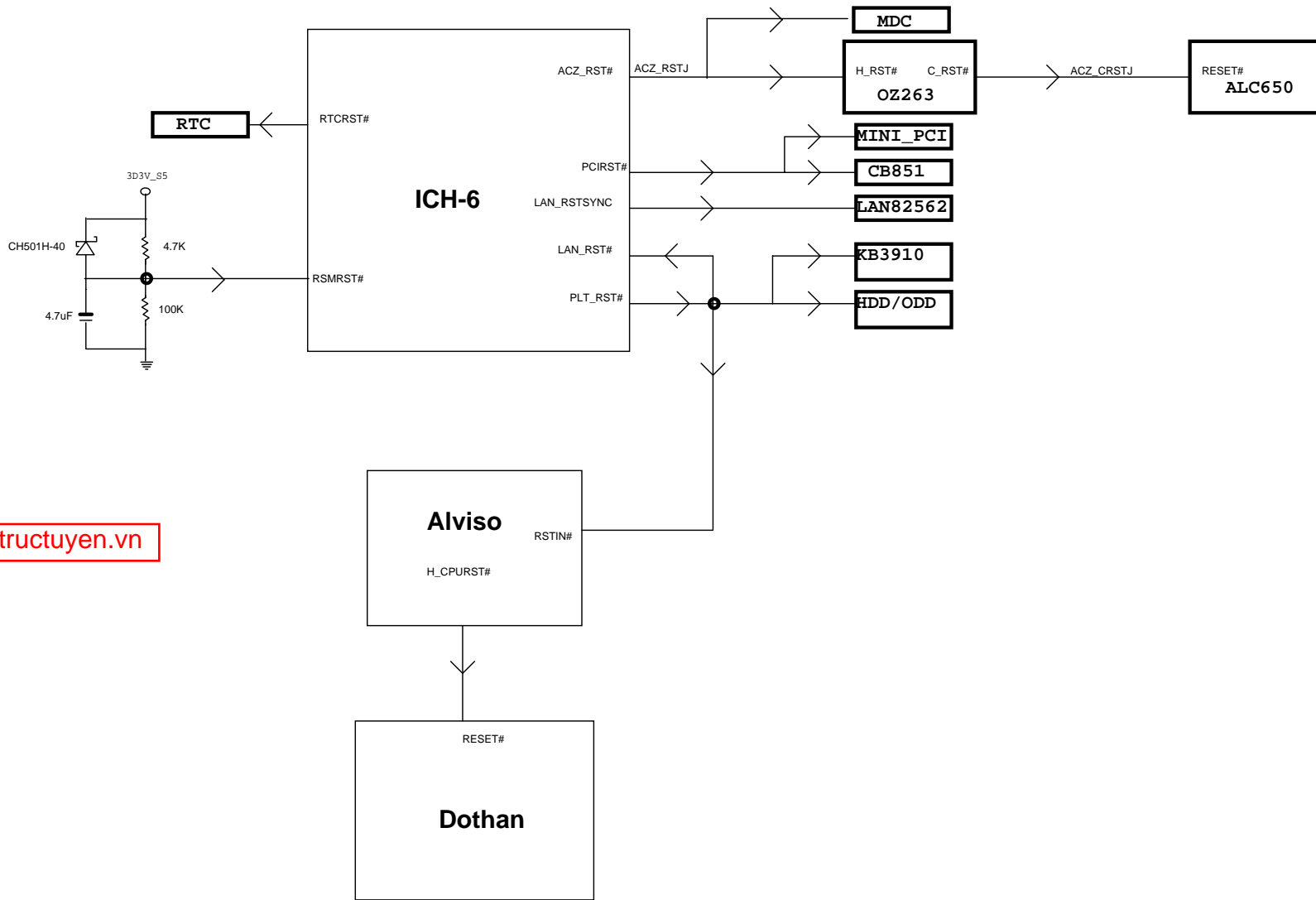




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| | |
|----------------------------------|---------------|
| Title HOLE/UNUSED PARTS | |
| Document Number S09 MAINBOARD | Rev A |
| Date: Thursday, March 17, 2005 | Sheet 1 of 45 |



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| Device Rails | CPU | GMCH | ICH6-MENE3910 | DDRII | Audio | HDD | ODD | LCD | INV | USB2.0 | LAN | CB851 | Oz263 | CLK GEN | ANTITHEFT |
|----------------------|-----|------|---------------|-------|-------|-----|-----|-----|-----|--------|-----|-------|-------|------------|-----------|
| 3D3V_AUX_S5 | | | ● | | | | | | | | | | | | |
| 5V_AUX_S5 | | | | | | | | | | | | | | | |
| 3D3V_S5 | | | ● | | | | | | | | ● | | | | ● |
| 5V_S5 | | | | | | | | | | | | | | | ● |
| 1D5V_S5 | | | ● | | | | | | | | ● | | | | |
| VDIMM (1D8V_S3) | | ● | | ● | | | | | | | | | | | |
| VTT_MEM (0D9V_S0) | | | | ● | | | | | | | | | | | |
| 3D3V_S0 | | ● | ● | ● | ● | | | ● | ● | | | ● | ● | ● | |
| 5V_S0 | | | | | ● | ● | ● | | | ● | | ● | | | |
| 2D5V_S0 | | ● | ● | | | | | | | | | | | | |
| 1D5V_S0 | ● | ● | ● | | | | | | | | | | | | |
| 1D05V_S0 | ● | ● | ● | | | | | | | | | | | | |
| VCC_CORE_S0 | ● | | | | | | | | | | | | | | |
| 1D8V_S0 | | | | | | | | | | | | | | | |
| DCBATOUT | | | | | | | | | ● | | | | | | |

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0218. P39, change Vcore to two phase
0222. P14,add SATA diable circuit when use PATA
0224. P24,change Lan to 82625GT
0225. P14,P19,Del SATA
0303. ADD RESET MAP
0312. del AUD_AGND_S

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| | |
|---|---------------|
|  | |
| Title | |
| HISTORY | |
| Document Number | Rev |
| S09 MAINBOARD | A |
| Date: Saturday, March 12, 2005 | Sheet 1 of 45 |