

Device Rails	CPU	M661FX	963L	PC87591	DDR	M10	302LV	LCD	MiniPCI	LAN	AUDIO	HDD	MDC	Buffer	CLK GEN.	cardbus
+1.5VSUS																
+3VALW				●												
+3v		●	●	●		●		●	●	●		●	●		●	●
+1.8V	●	●	●													
3VAUX		●	●							●			●			●
+1.8VAUX			●													
5VAUX																
VDDQ		●					●									
VDIMM		●			●											
DDR_VTT					●											
+1.2V						●										
+1.5V	●															
+5VALW																
+12V																
VCORE_CPU	●															
VCCP	●	●	●													
+5V				●												
3VSUS									●							
VCORE_VGA						●										

[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

**FOXCONN** TECHNOLOGY COPR.

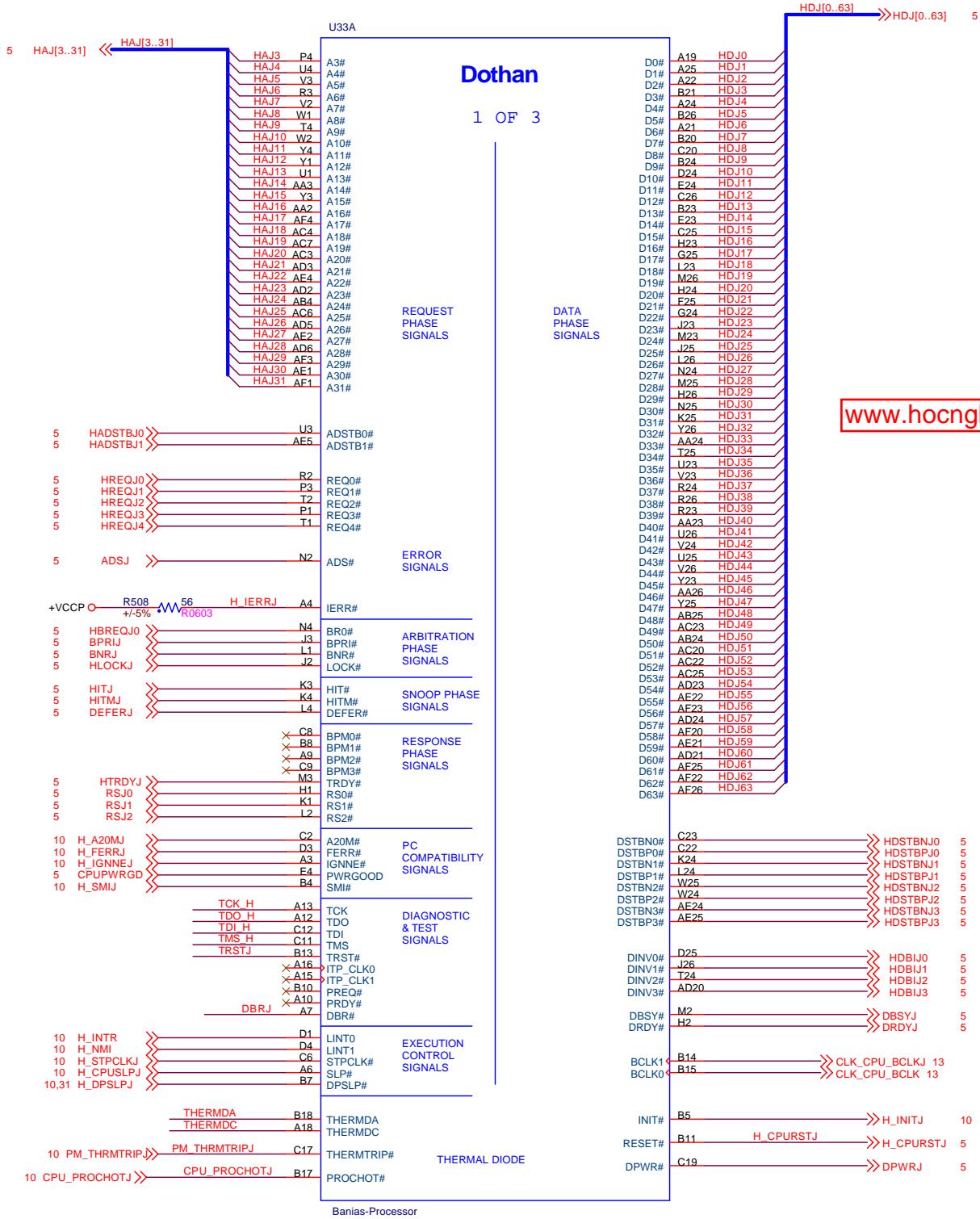
Title: **Power Diagram**

Document Number: **661S03**

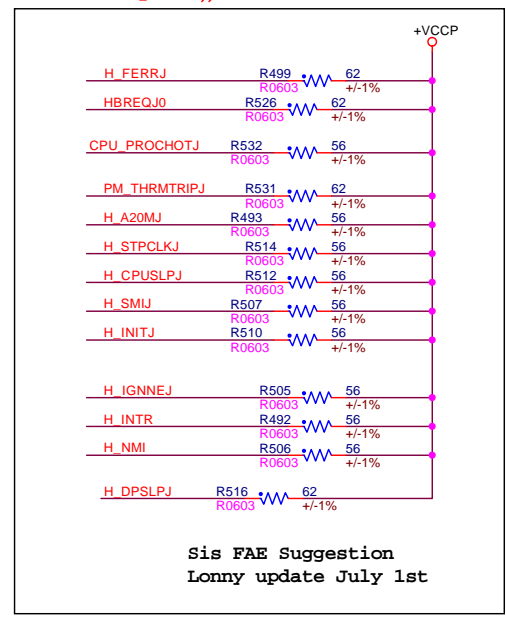
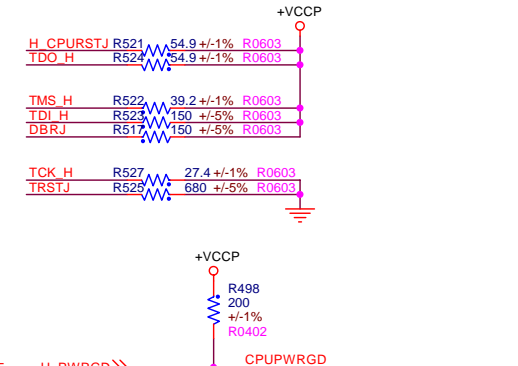
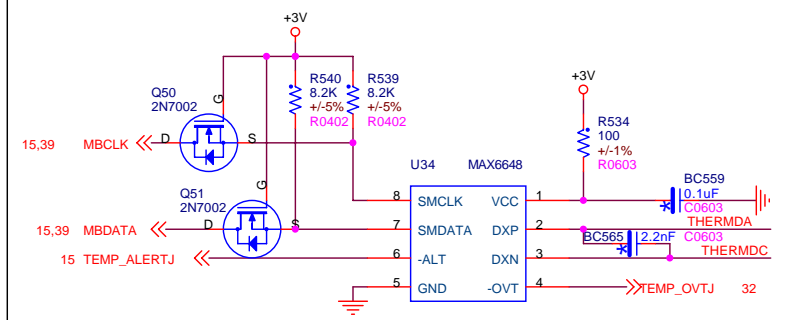
Date: Friday, August 13, 2004

Sheet: 2 of 50

Rev: **A**



www.hocnghetructuyen.vn



Sis FAE Suggestion  
Lonny update July 1st

**FOXCONN** TECHNOLOGY COPR.

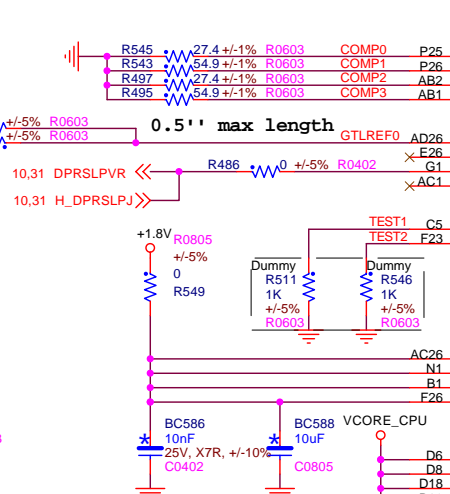
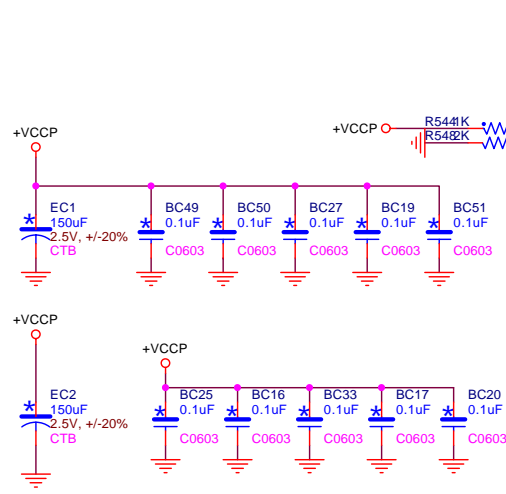
Title: Dothan CPU-1

Document Number: 661S03

Date: Friday, August 13, 2004

Sheet 3 of 50

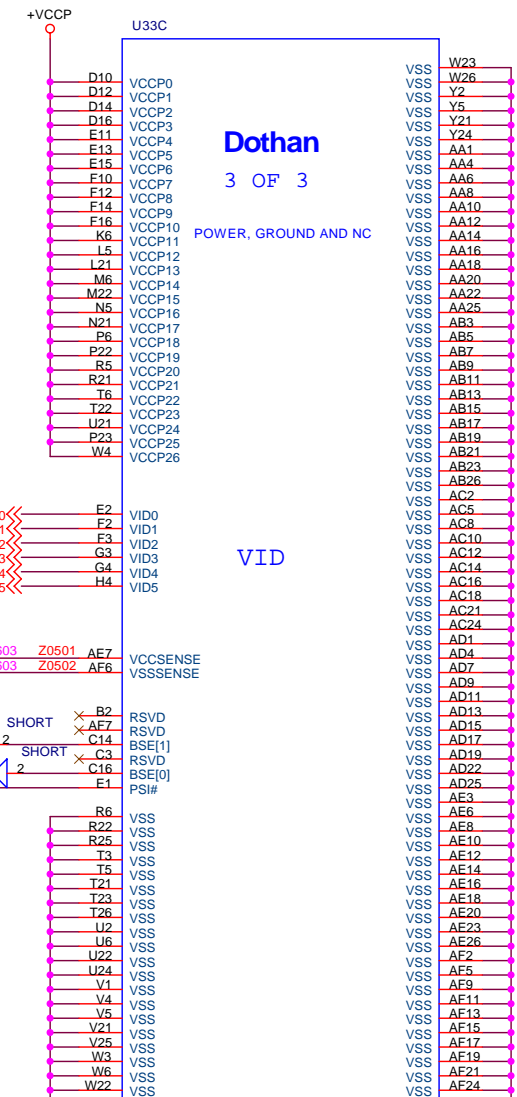
Rev A



U33B

COMP0	A2	VSS	A26	TEST1	C5
COMP1	A5	VSS	A27	TEST2	F23
COMP2	A8	VSS	A28		
COMP3	A11	VSS	A29		
	A14	VSS	A30		
	A17	VSS	A31		
	A20	VSS	A32		
	A23	VSS	A33		
	A26	VSS	A34		
	A3	VSS	A35		
	A6	VSS	A36		
	A9	VSS	A37		
	B12	VSS	A38		
	B15	VSS	A39		
	B19	VSS	A40		
	B22	VSS	A41		
	B25	VSS	A42		
	C1	VSS	A43		
	C4	VSS	A44		
	C7	VSS	A45		
	C10	VSS	A46		
	C13	VSS	A47		
	C15	VSS	A48		
	C18	VSS	A49		
	C21	VSS	A50		
	C24	VSS	A51		
	D2	VSS	A52		
	D5	VSS	A53		
	D7	VSS	A54		
	D9	VSS	A55		
	D11	VSS	A56		
	D13	VSS	A57		
	D15	VSS	A58		
	D17	VSS	A59		
	D19	VSS	A60		
	D21	VSS	A61		
	D23	VSS	A62		
	D26	VSS	A63		
	E3	VSS	A64		
	E6	VSS	A65		
	E8	VSS	A66		
	E10	VSS	A67		
	E12	VSS	A68		
	E14	VSS	A69		
	E16	VSS	A70		
	E18	VSS	A71		
	E20	VSS	A72		
	E22	VSS	A73		
	E25	VSS	A74		
	F1	VSS	A75		
	F4	VSS	A76		
	F5	VSS	A77		
	F7	VSS	A78		
	F9	VSS	A79		
	F11	VSS	A80		
	F13	VSS	A81		
	F15	VSS	A82		
	F17	VSS	A83		
	F19	VSS	A84		
	F21	VSS	A85		
	F24	VSS	A86		
	G2	VSS	A87		
	G6	VSS	A88		
	G22	VSS	A89		
	G23	VSS	A90		
	G26	VSS	A91		
	H3	VSS	A92		
	H5	VSS	A93		
	H21	VSS	A94		
	H25	VSS	A95		
	J1	VSS	A96		
	J4	VSS	A97		
	J25	VSS	A98		
	J6	VSS	A99		
	J22	VSS	A100		
	J24	VSS	A101		
	K2	VSS	A102		
	K5	VSS	A103		
	K21	VSS	A104		
	K23	VSS	A105		
	K26	VSS	A106		
	L3	VSS	A107		
	L6	VSS	A108		
	L22	VSS	A109		
	L25	VSS	A110		
	M1	VSS	A111		
	M4	VSS	A112		
	M5	VSS	A113		
	M21	VSS	A114		
	M24	VSS	A115		
	N3	VSS	A116		
	N6	VSS	A117		
	N22	VSS	A118		
	N23	VSS	A119		
	N26	VSS	A120		
	P2	VSS	A121		
	P5	VSS	A122		
	P21	VSS	A123		
	P24	VSS	A124		
	R1	VSS	A125		
	R4	VSS	A126		

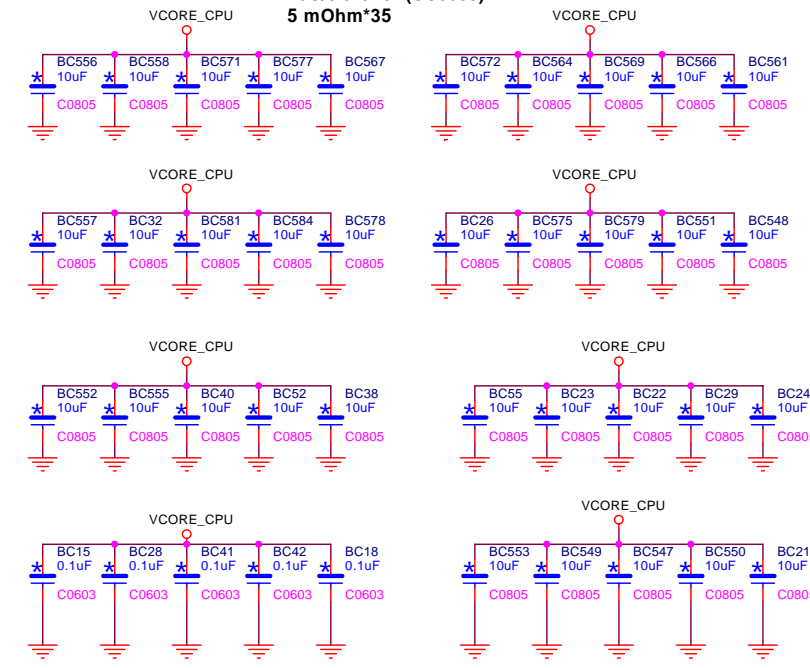
Dothan  
2 OF 3  
POWER, GROUND, RESERVED SIGNALS



Dothan  
3 OF 3  
POWER, GROUND AND NC

www.hocnghetructuyen.vn

10U/6.3V/X5R(CC0805)  
5 mOhm\*35



**FOXCONN** TECHNOLOGY COPR.

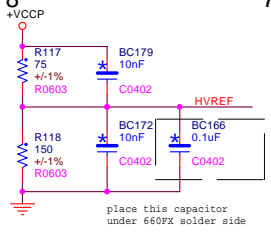
Title: Dothan CPU-2

Document Number: 661S03

Date: Friday, August 13, 2004

Sheet 4 of 50

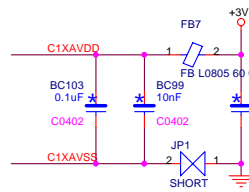
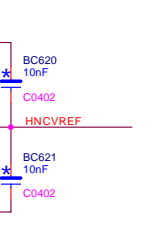
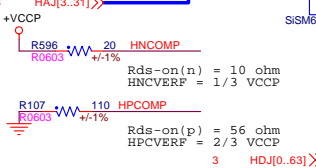
Rev A



13 CLK_MCH_BCLK	CLK_MCH_BCLK	AJ31	CPULCLK
13 CLK_MCH_BCLK	CLK_MCH_BCLK	AJ33	CPULCLK#
3 HLOCKJ	HLOCKJ	T33	HLOCK#
3 DEFERJ	DEFERJ	T35	DEFER#
3 HTRDY#	HTRDY#	Y32	HTRDY#
3 H_CPURETJ	H_CPURETJ	B23	CPURST#
3 CPUPWRGD	CPUPWRGD	F22	CPUPWRGD
3 BPRIJ	BPRIJ	R34	BPRI#
3 HBREQJ0	HBREQJ0	U31	BREQ0#
3 RSJ2	H_RSJ2	R33	RS#2
3 RSJ1	H_RSJ1	T32	RS#1
3 RSJ0	H_RSJ0	U35	RS#0
3 ADSJ	ADSJ	V35	ADS#
3 HITMJ	HITMJ	R35	HITM#
3 HITJ	HITJ	U34	HIT#
3 DRDYJ	DRDYJ	W34	DRDY#
3 DBSYJ	DBSYJ	U33	DBSY#
3 BNRJ	BNRJ	V33	BNR#
3 HREQJ4	H_REQJ4	W35	HREQ4#
3 HREQJ3	H_REQJ3	Y33	HREQ3#
3 HREQJ2	H_REQJ2	W31	HREQ2#
3 HREQJ1	H_REQJ1	W33	HREQ1#
3 HREQJ0	H_REQJ0	Y35	HREQ0#
3 HADSTBJ1	HADSTBJ1	AG31	HASTB1#
3 HADSTBJ0	HADSTBJ0	AA33	HASTB0#
3 DPWRJ	DPWRJ	R36	DPWR#

HAIJ31	AH33	HA31#
HAIJ30	AG33	HA30#
HAIJ29	AJ35	HA29#
HAIJ28	AF32	HA28#
HAIJ27	AL34	HA27#
HAIJ26	AH32	HA26#
HAIJ25	AG35	HA25#
HAIJ24	AF34	HA24#
HAIJ23	AH35	HA23#
HAIJ22	AF35	HA22#
HAIJ21	AE35	HA21#
HAIJ20	AE34	HA20#
HAIJ19	AE34	HA19#
HAIJ18	AF33	HA18#
HAIJ17	AG34	HA17#
HAIJ16	AC34	HA16#
HAIJ15	AD32	HA15#
HAIJ14	AD33	HA14#
HAIJ13	AC35	HA13#
HAIJ12	AD35	HA12#
HAIJ11	AC31	HA11#
HAIJ10	AC34	HA10#
HAIJ9	AB35	HA9#
HAIJ8	AB32	HA8#
HAIJ7	AB33	HA7#
HAIJ6	AA35	HA6#
HAIJ5	AA31	HA5#
HAIJ4	Y32	HA4#
HAIJ3	AA34	HA3#

# HOST



# LVDS / AGP

[www.hocnghetrucuyen.vn](http://www.hocnghetrucuyen.vn)

# M661FX-1

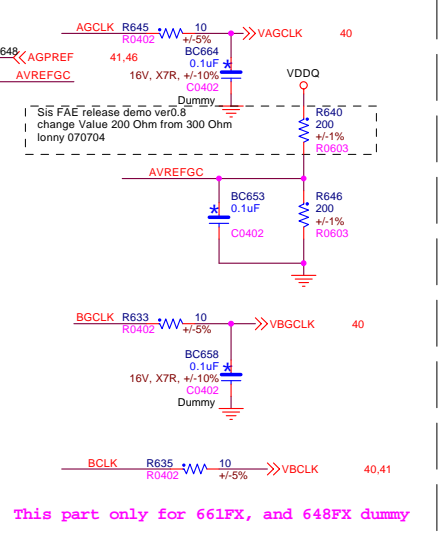
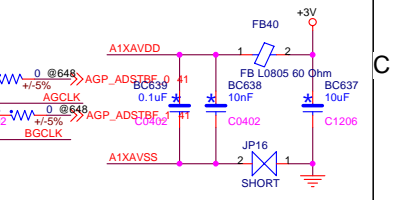
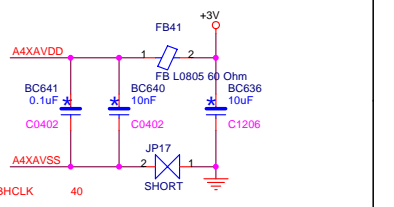
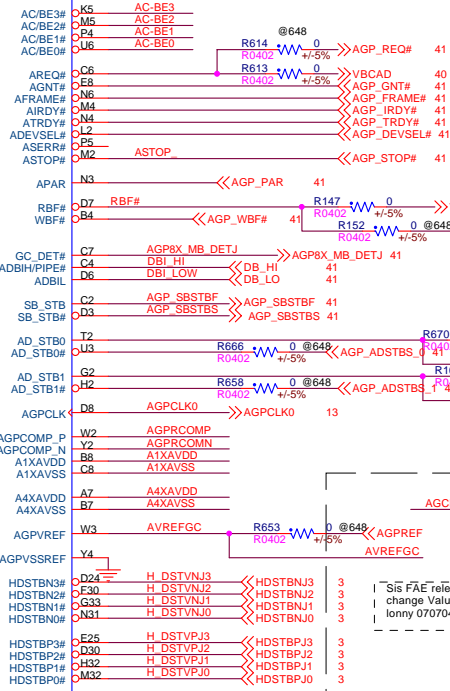
3	HDBUJ3	H_DINVJ3
3	HDBUJ2	H_DINVJ2
3	HDBUJ1	H_DINVJ1
3	HDBUJ0	H_DINVJ0

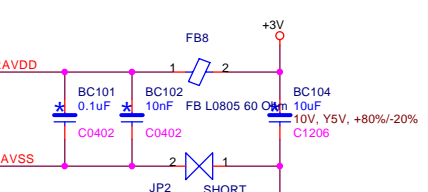
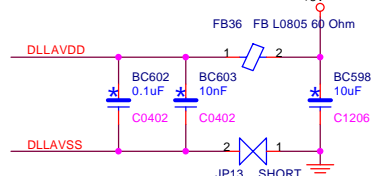
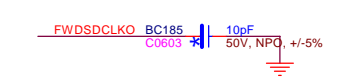
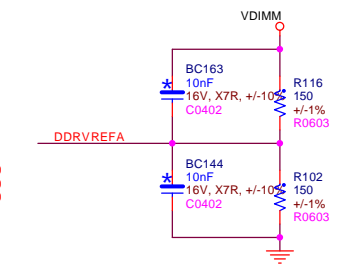
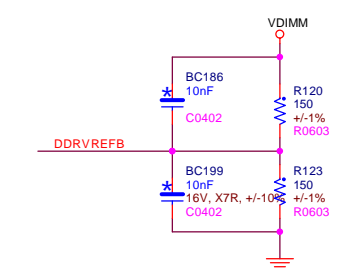
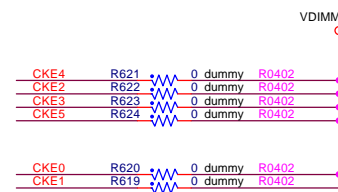
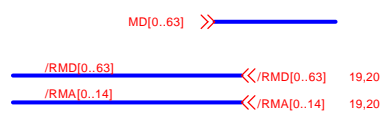
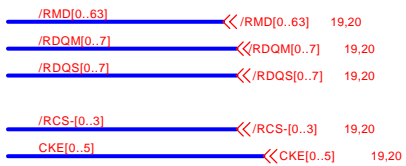
AGP 3.0 = 50 ohm  
Demo is 50 Ohm 1%  
lonny 2004-06-02

AGPRCOMP R639 43  
R0603 +/-1%

Demo is 43.75 Ohm 1%  
lonny 2004-06-02

VAD[0..11]	>>>VAD[0..11]	40,41
VBD[0..11]	>>>VBD[0..11]	40,41
VBCTL[0..11]	>>>VBCTL[0..11]	40,41
AHSYNC	>>>VAHSYNC	40,41
AVSYNC	>>>VAVSYNC	40,41
BHSYNC	>>>VBHSYNC	40,41
BVSYNC	>>>VBVSYNC	40,41
VADE	>>>VADE	40,41
VBDE	>>>VBDE	40,41
41	ST[0..2]	>>>ST[0..2]
	SBA[1..7]	<<<SBA[1..7]
	AC-BE[0..3]	<<<AC-BE[0..3]





/RMD7	RN24	1*	2	MD7
/RDQM0	10	3	4	DQM0
/RMD1	+/-5%	5	6	MD1
/RMD0	8P4R0603	7	8	MD0
/RMD6	RN23	1*	2	MD6
/RDQS0	10	3	4	DQS0
/RMD5	+/-5%	5	6	MD5
/RMD4	8P4R0603	7	8	MD4
/RDQS1	RN25	1*	2	DQS1
/RMD12	10	3	4	MD12
/RMD8	+/-5%	5	6	MD8
/RMD3	8P4R0603	7	8	MD3
/RMD21	RN28	1*	2	MD21
/RMD16	10	3	4	MD16
/RMD17	+/-5%	5	6	MD17
/RMD20	8P4R0603	7	8	MD20
/RDQM1	RN26	1*	2	DQM1
/RMD13	10	3	4	MD13
/RMD9	+/-5%	5	6	MD9
/RMD2	8P4R0603	7	8	MD2
/RMD11	RN27	1*	2	MD11
/RMD14	10	3	4	MD14
/RMD15	+/-5%	5	6	MD15
/RMD10	8P4R0603	7	8	MD10
/RMD29	RN30	1*	2	MD29
/RMD24	10	3	4	MD24
/RMD23	+/-5%	5	6	MD23
/RDQM2	8P4R0603	7	8	DQM2
/RMD19	RN31	1*	2	MD19
/RMD22	10	3	4	MD22
/RMD18	+/-5%	5	6	MD18
/RDQS2	8P4R0603	7	8	DQS2
/RMD27	RN33	1*	2	MD27
/RMD30	10	3	4	MD30
/RDQM3	+/-5%	5	6	DQM3
/RDQS3	8P4R0603	7	8	DQS3
/RMD31	RN32	1*	2	MD31
/RMD26	10	3	4	MD26
/RMD25	+/-5%	5	6	MD25
/RMD28	8P4R0603	7	8	MD28
/RMD39	RN35	1*	2	MD39
/RDQS4	10	3	4	DQS4
/RMD33	+/-5%	5	6	MD33
/RMD32	8P4R0603	7	8	MD32
/RMD53	RN39	1*	2	MD53
/RMD49	10	3	4	MD49
/RMD47	+/-5%	5	6	MD47
/RMD42	8P4R0603	7	8	MD42
/RDQM4	RN34	1*	2	DQM4
/RMD34	10	3	4	MD34
/RMD37	+/-5%	5	6	MD37
/RMD36	8P4R0603	7	8	MD36
/RDQM5	RN37	1*	2	DQM5
/RMD45	10	3	4	MD45
/RMD44	+/-5%	5	6	MD44
/RMD38	8P4R0603	7	8	MD38
/RMD52	RN38	1*	2	MD52
/RMD48	10	3	4	MD48
/RMD46	+/-5%	5	6	MD46
/RMD43	8P4R0603	7	8	MD43
/RDQS5	RN36	1*	2	DQS5
/RMD41	10	3	4	MD41
/RMD40	+/-5%	5	6	MD40
/RMD35	8P4R0603	7	8	MD35
/RDQM6	RN41	1*	2	DQM6
/RMD54	10	3	4	MD54
/RMD51	+/-5%	5	6	MD51
/RDQS6	8P4R0603	7	8	DQS6
/RMD57	RN40	1*	2	MD57
/RMD50	10	3	4	MD50
/RMD55	+/-5%	5	6	MD55
/RMD60	8P4R0603	7	8	MD60
/RMD63	RN42	1*	2	MD63
/RMD62	10	3	4	MD62
/RDQM7	+/-5%	5	6	DQM7
/RMD59	8P4R0603	7	8	MD59
/RMD58	10	3	4	MD58
/RMD59	8P4R0603	7	8	MD59
/RMD58	10	3	4	MD58
/RDQS7	10	5	6	DQS7
/RMD61	+/-5%	7	8	MD61
/RMD61	8P4R0603	7	8	MD61

MD0	AN35	MD0
MD1	AK36	MD1
MD2	AK33	MD2
MD3	AM33	MD3
MD4	AN34	MD4
MD5	AK32	MD5
MD6	AK34	MD6
MD7	AN33	MD7
MD8	AK35	MD8
DQM0	AP34	DQM0
MD8	AM32	DQS0/CSB0#
MD9	AL31	MD9
MD10	AR31	MD10
MD11	AL30	MD11
MD12	AN32	MD12
MD13	AR33	MD13
MD14	AN31	MD14
MD15	AM31	MD15
DQM1	AR32	DQM1
DQS1	AP32	DQS1/CSB1#
MD16	AP30	MD16
MD17	AL30	MD17
MD18	AR30	MD18
MD19	AM29	MD19
MD20	AL27	MD20
MD21	AN30	MD21
MD22	AN29	MD22
MD23	AL28	MD23
MD24	AN28	MD24
DQM2	AL29	DQM2
DQS2	AP28	DQS2/CSB2#
MD25	AN25	MD25
MD26	AR24	MD26
MD27	AL24	MD27
MD28	AL25	MD28
MD29	AR26	MD29
MD30	AM25	MD30
MD31	AN25	MD31
DQM3	AP24	DQM3
DQS3	AR25	DQS3/CSB3#
MD32	AN21	MD32
MD33	AP23	MD33
MD34	AN20	MD34
MD35	AL18	MD35
MD36	AM21	MD36
MD37	AR21	MD37
MD38	AL19	MD38
MD39	AM19	MD39
DQM4	AL20	DQM4
DQS4	AR20	DQS4/CSB4#
MD40	AL15	MD40
MD41	AL14	MD41
MD42	AN15	MD42
MD43	AL15	MD43
MD44	AN16	MD44
MD45	AL15	MD45
MD46	AN14	MD46
MD47	AL13	MD47
DQM5	AP16	DQM5
DQS5	AR16	DQS5/CSB5#
MD48	AM13	MD48
MD49	AL12	MD49
MD50	AL11	MD50
MD51	AR12	MD51
MD52	AP14	MD52
MD53	AR14	MD53
MD54	AN13	MD54
MD55	AP12	MD55
MD56	AM12	MD56
DQM6	AR13	DQM6
DQS6	AL10	DQS6/CSB6#
MD57	AR11	MD57
MD58	AM9	MD58
MD59	AR9	MD59
MD60	AM11	MD60
MD61	AN11	MD61
MD62	AP10	MD62
MD63	AN9	MD63
DQM7	AN10	DQM7
DQS7	AR10	DQS7/CSB7#

M661FX-2

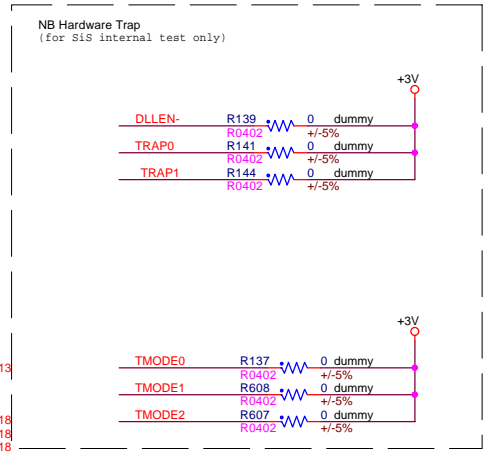
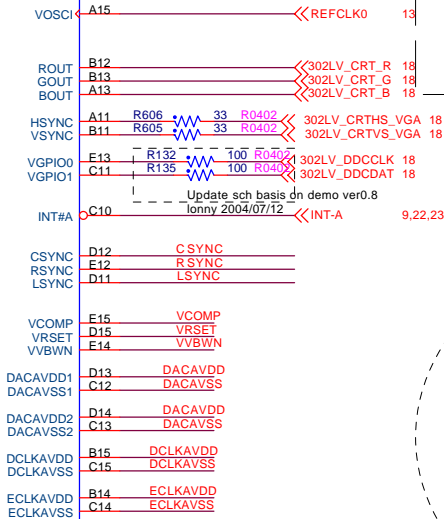
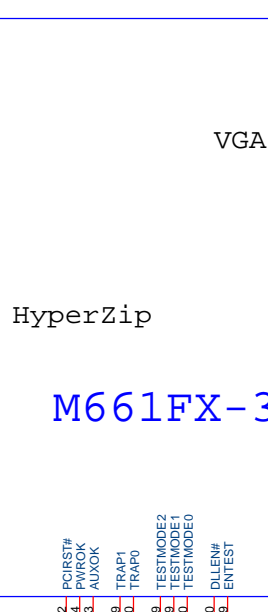
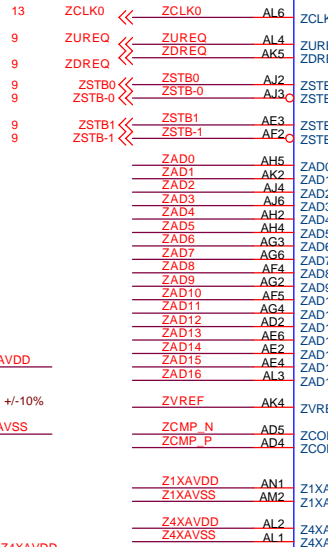
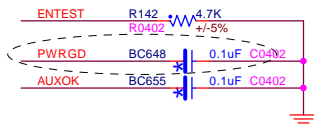
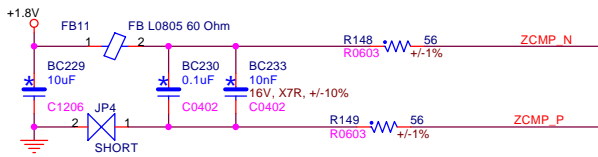
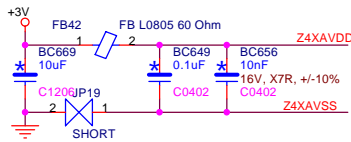
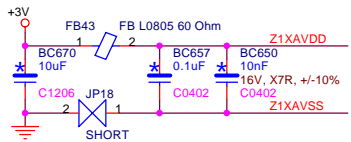
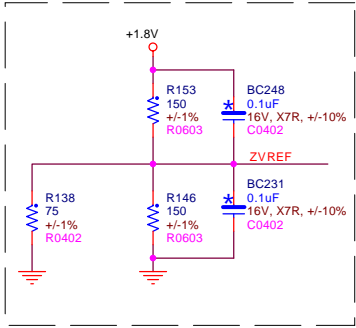
SISM661FX

www.hocnghetructuyen.vn

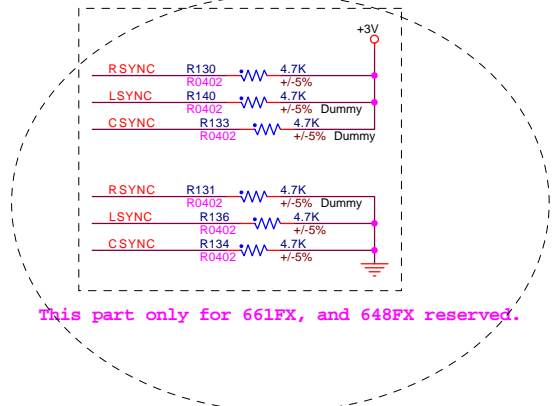
Title: \_\_\_\_\_
   
 Document Number: 661S03
   
 Date: Friday, August 13, 2004
   
 Sheet: 6 of 50
   
 Rev: A

9 ZAD[0..16] ← ZAD[0..16]

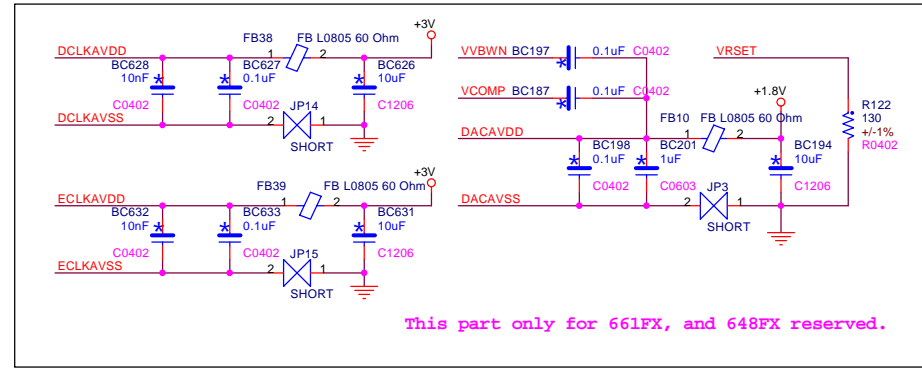
www.hocnghetructuyen.vn



		Enable	Disable
RSYNC	VGA Interrupt	1	0
LSYNC	TBD	1	0
CSYNC	TBD	1	0



This part only for 661FX, and 648FX reserved.

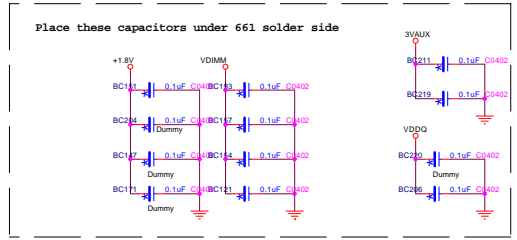
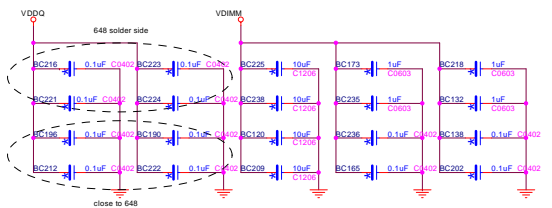
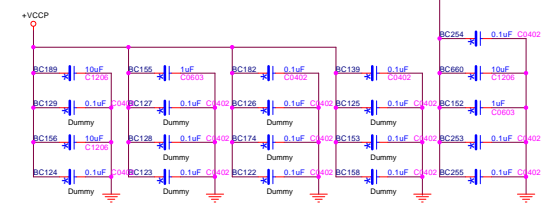
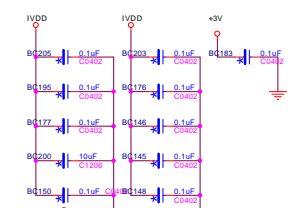
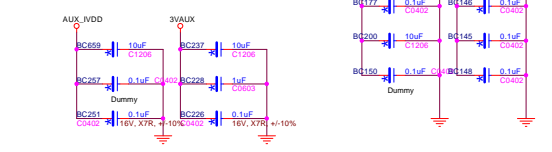
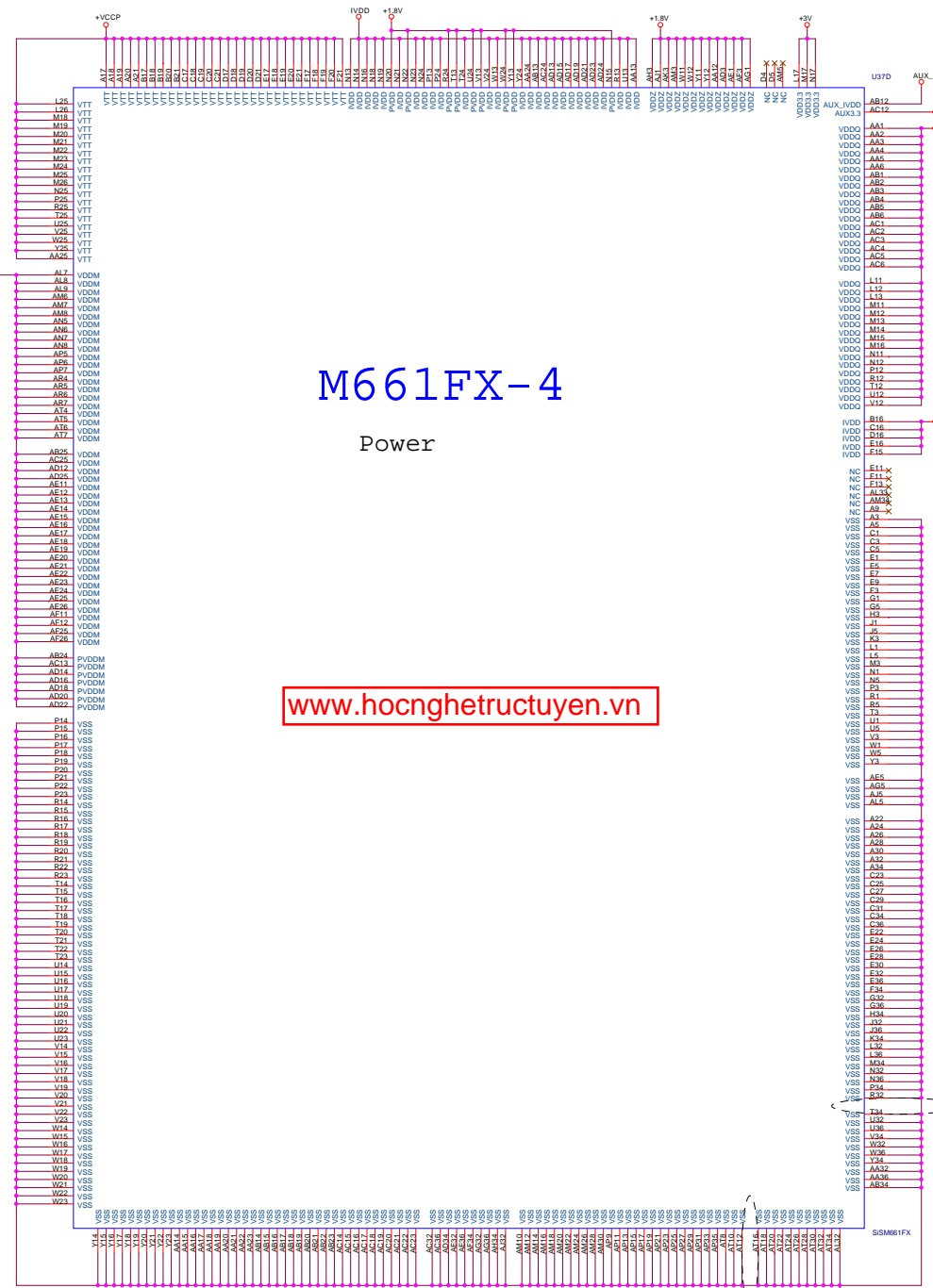


This part only for 661FX, and 648FX reserved.

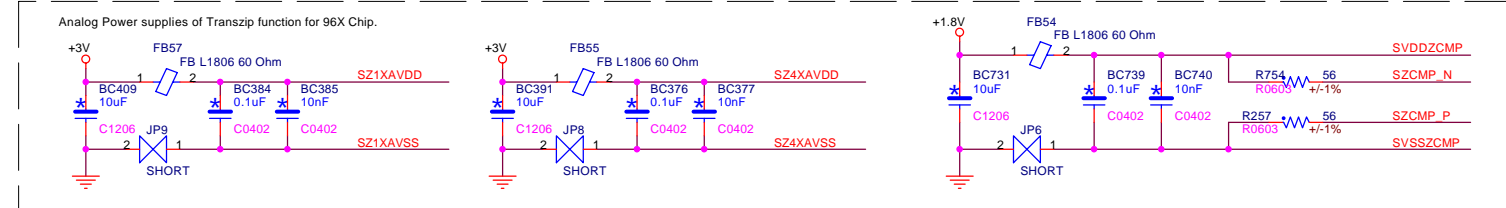
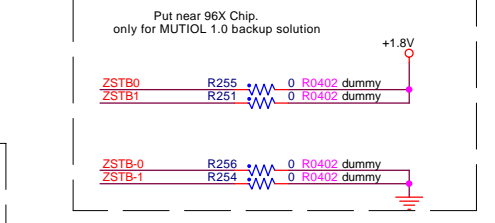
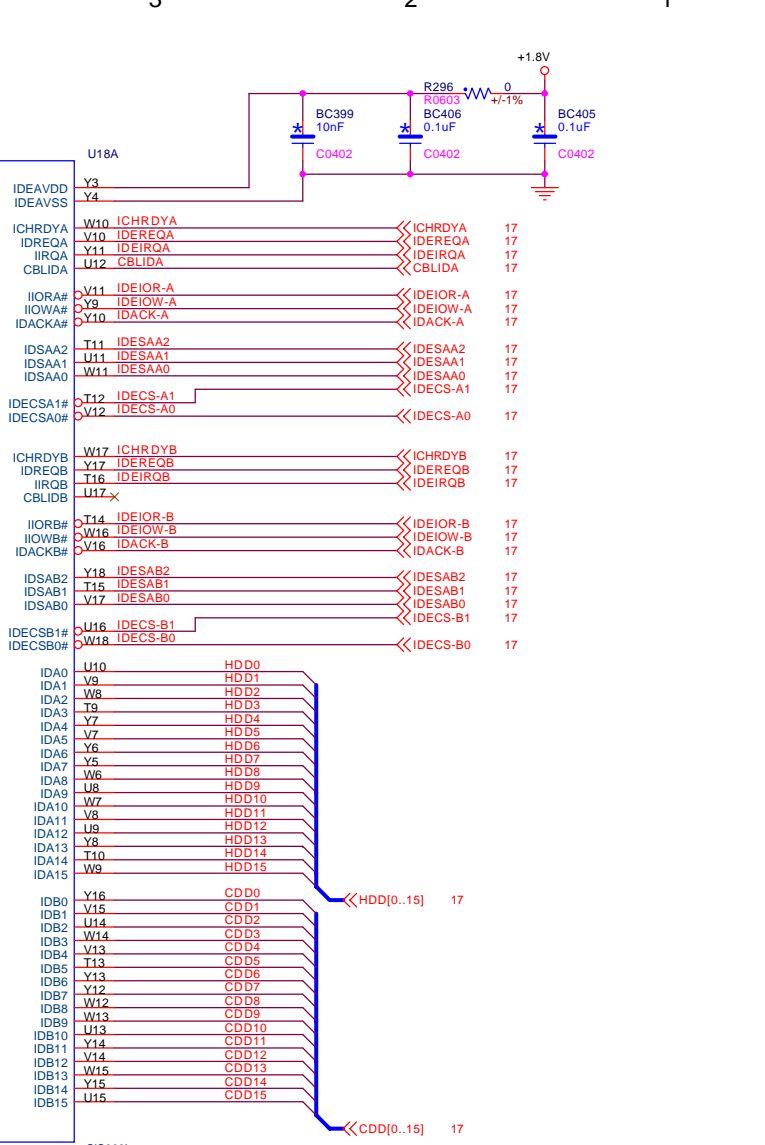
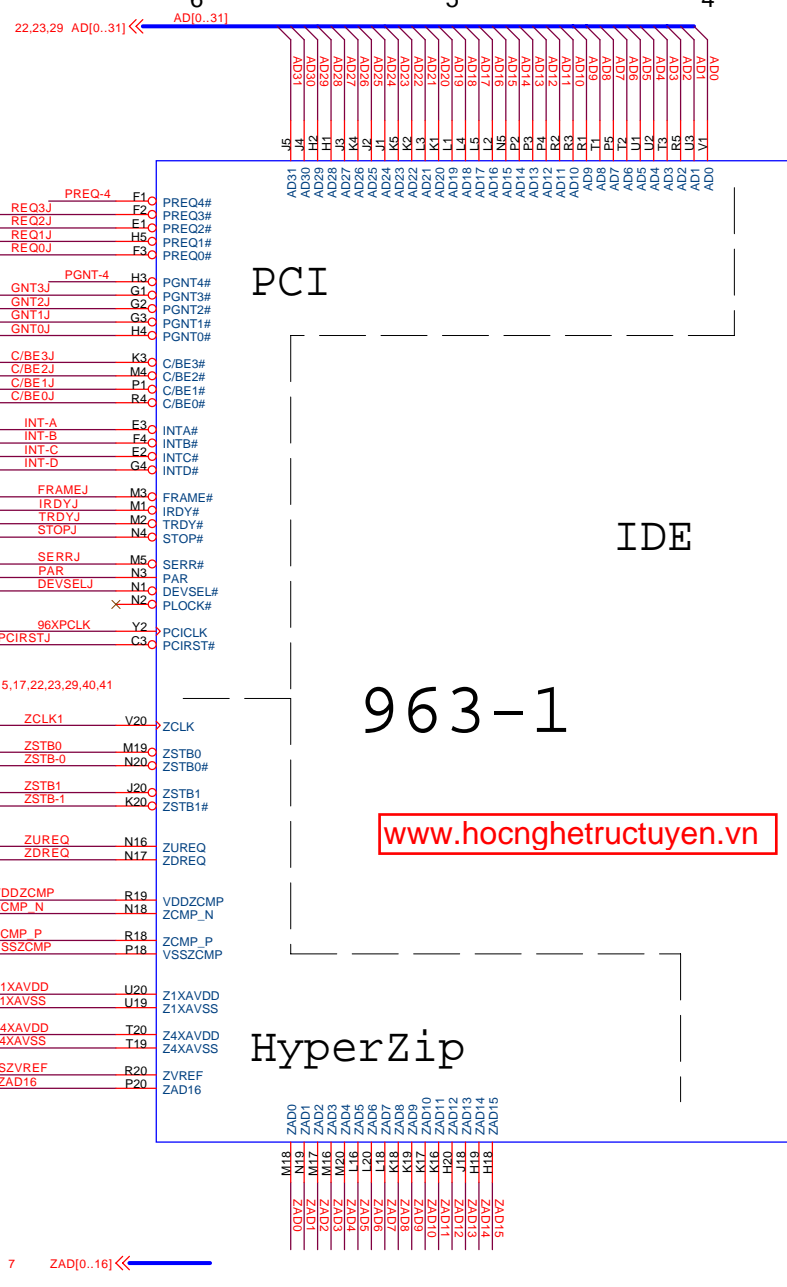
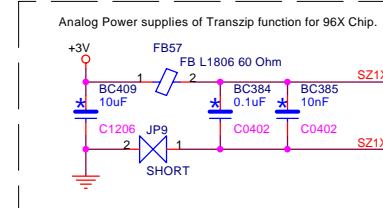
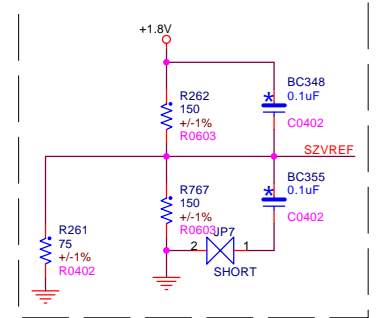
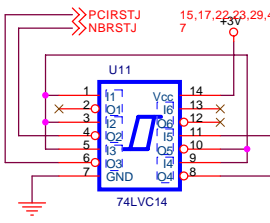
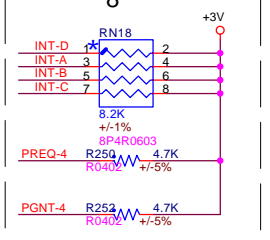
# M661FX-4

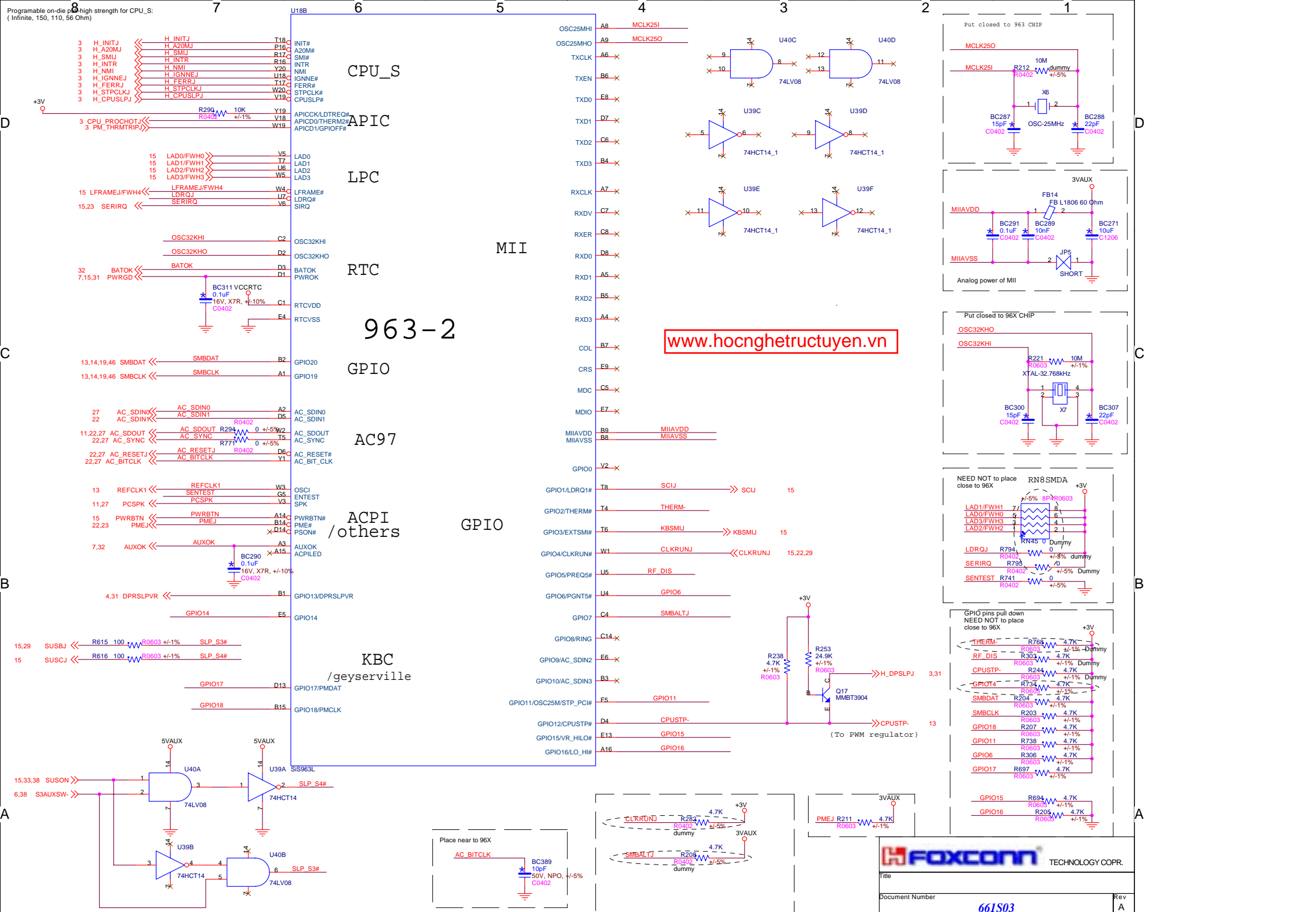
## Power

[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

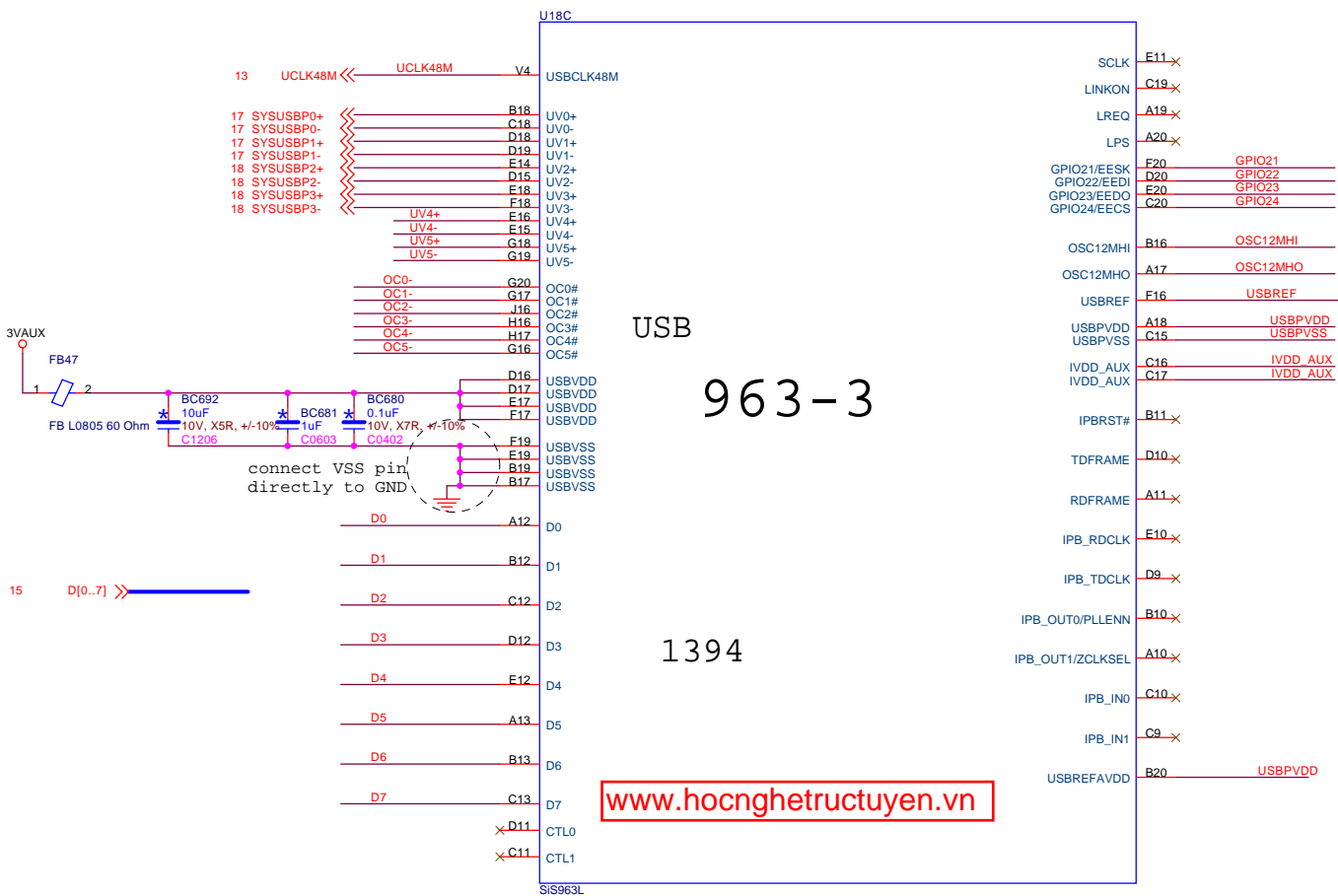








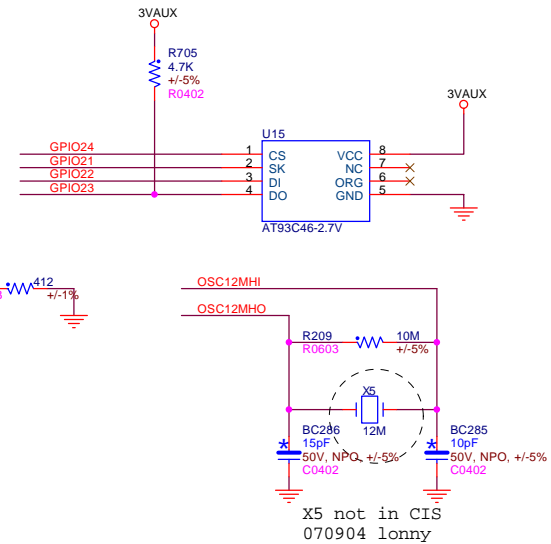
SDATO( Trap mode)



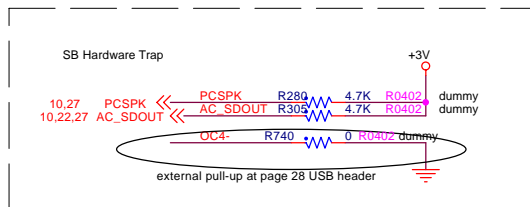
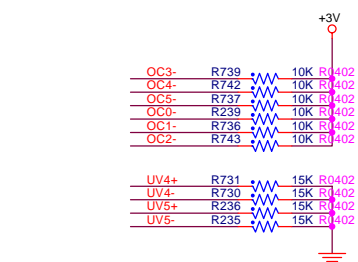
USB  
963-3

1394

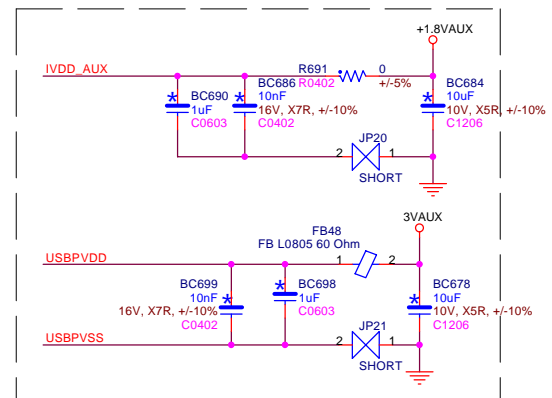
[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

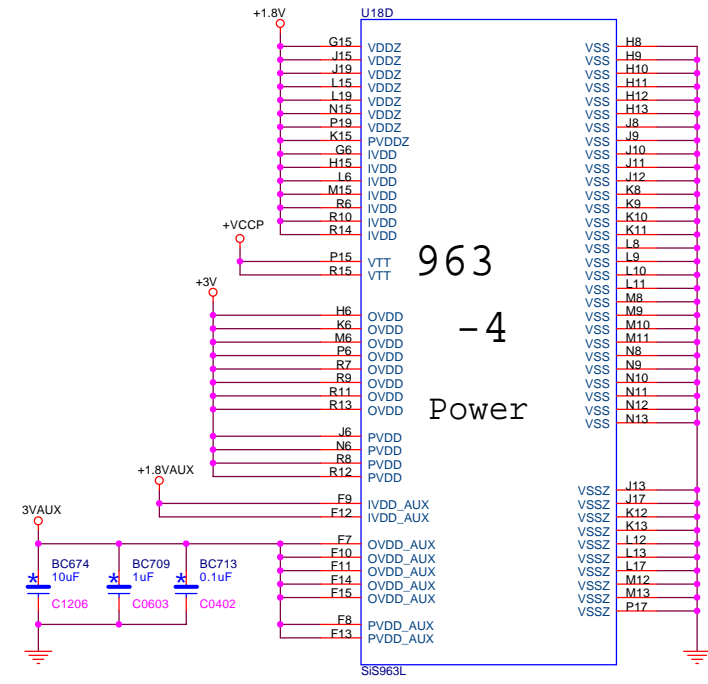
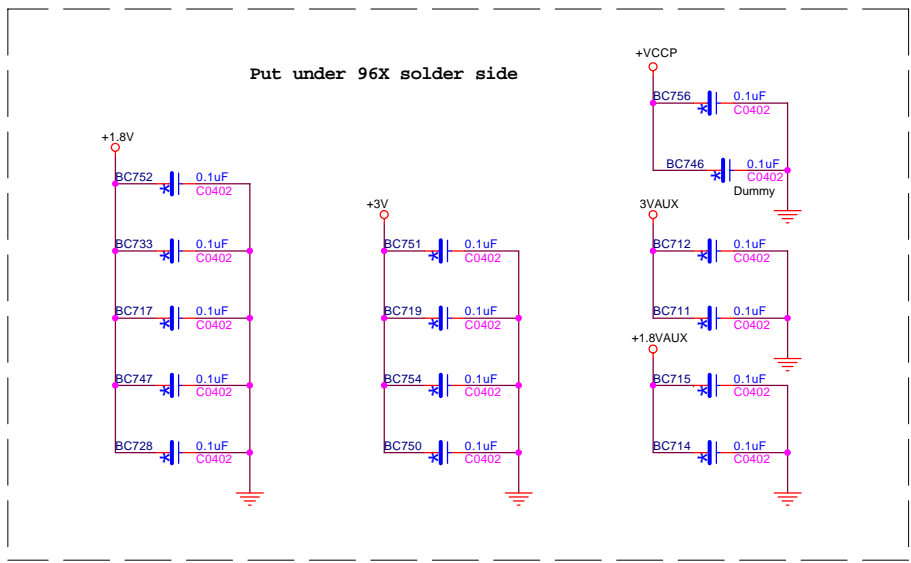
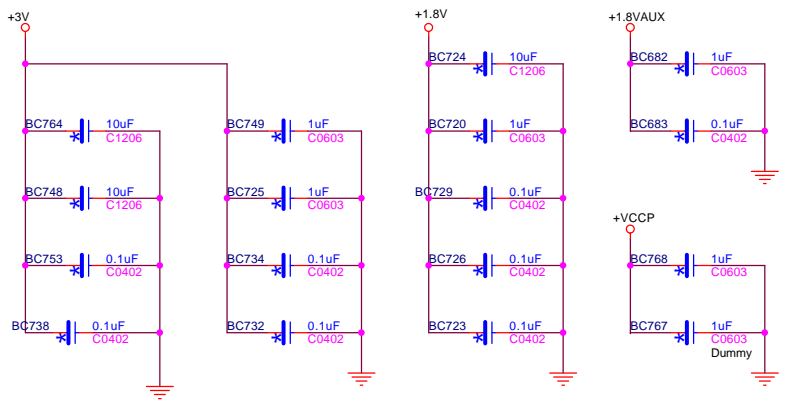


X5 not in CIS  
070904 lonny



	0	1	Default	
SPKR( LPC addr mapping)	disable	enable	R169 un-stuff	yes
SDATO( Trap from)	ROM	PCI AD	R170 un-stuff	yes
OC4-( SB debug mode)	enable	disable	R171 un-stuff	NO
SYNC( PCICLK PLL)	enable	disable	NONE	yes

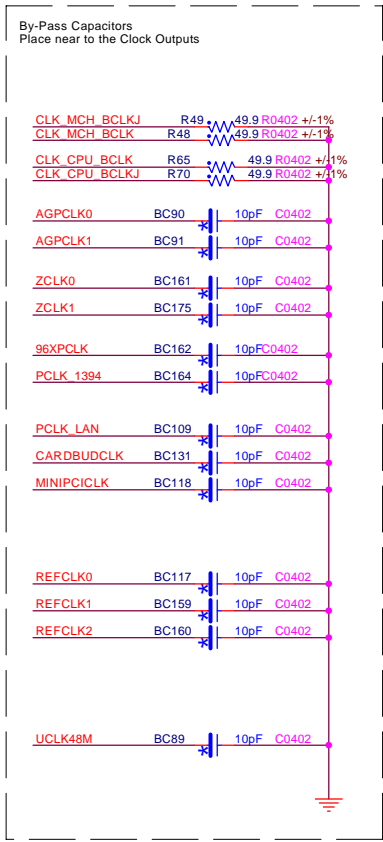
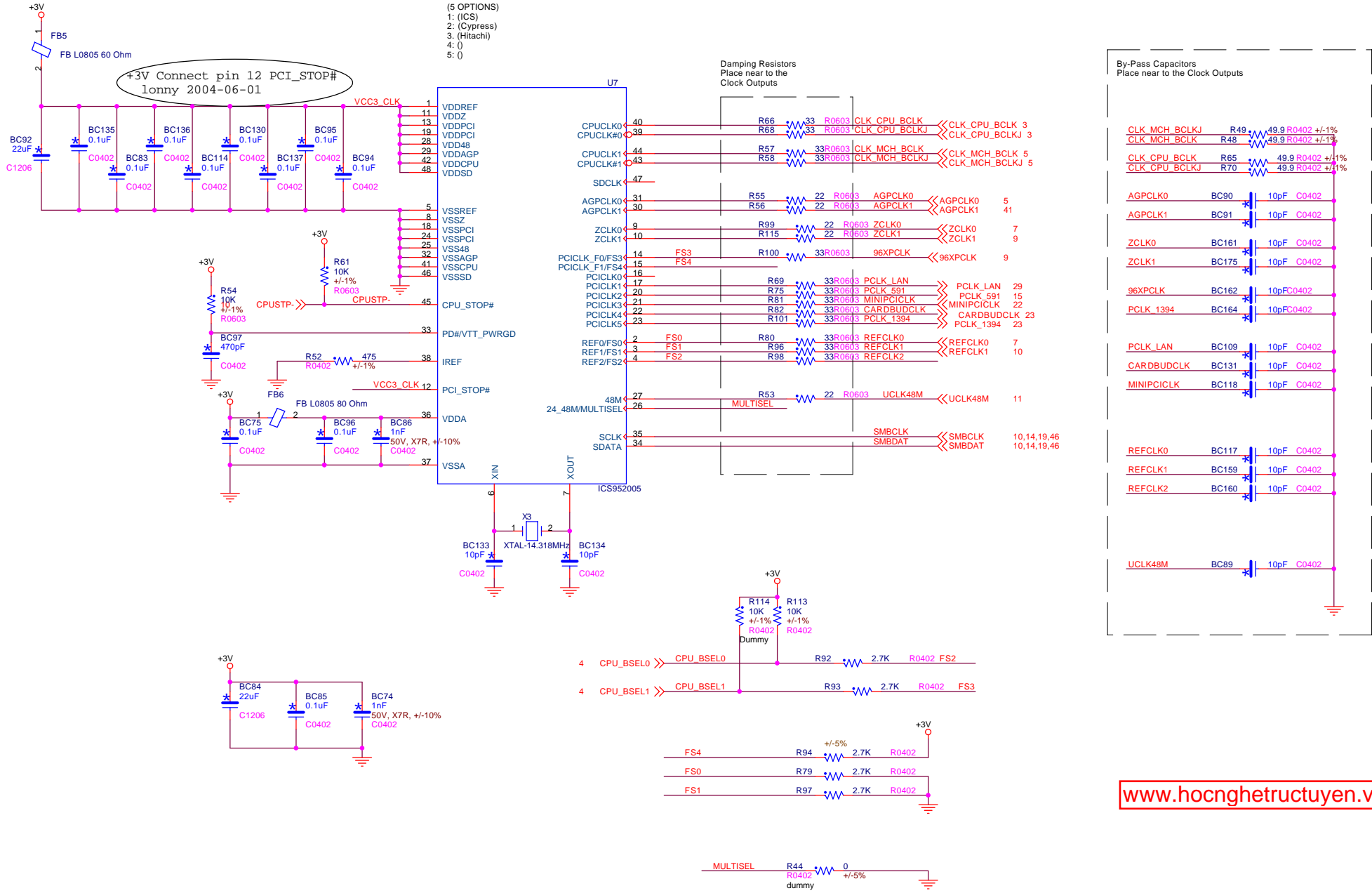




[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

# Main Clock Generator

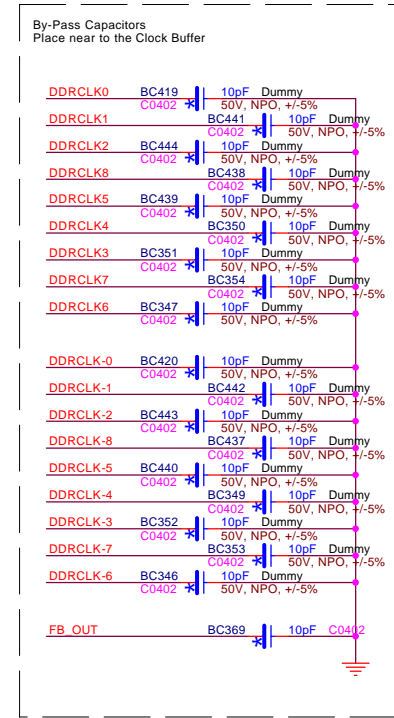
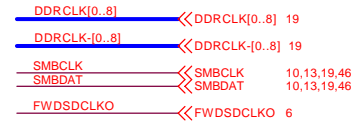
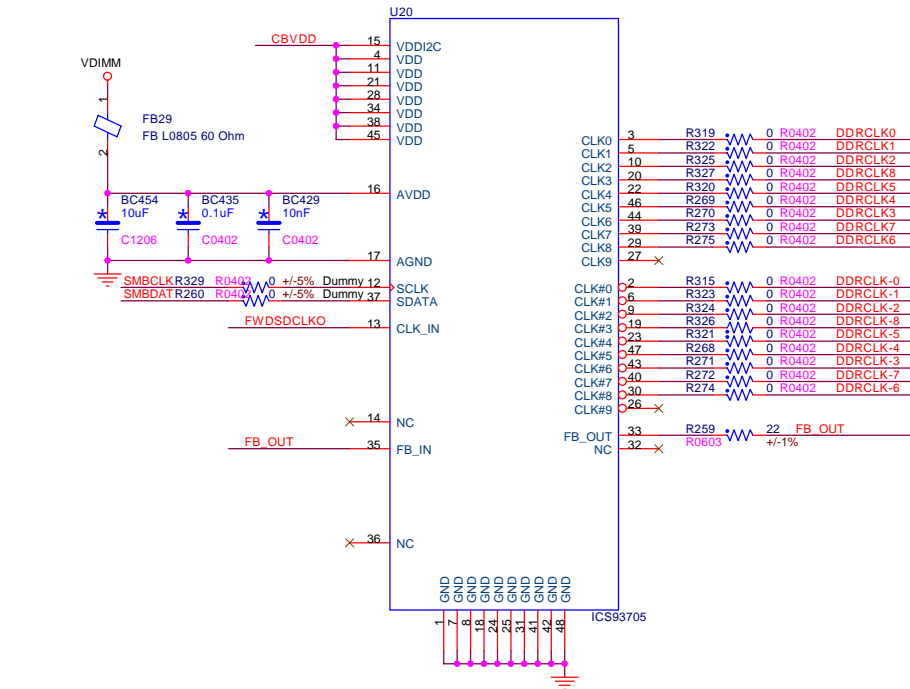
- (5 OPTIONS)  
 1: (ICS)  
 2: (Cypress)  
 3: (Hitachi)  
 4: ()  
 5: ()



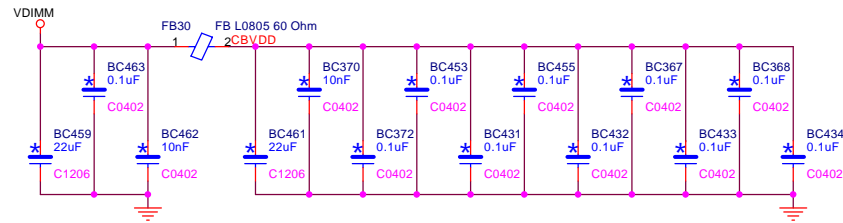
[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

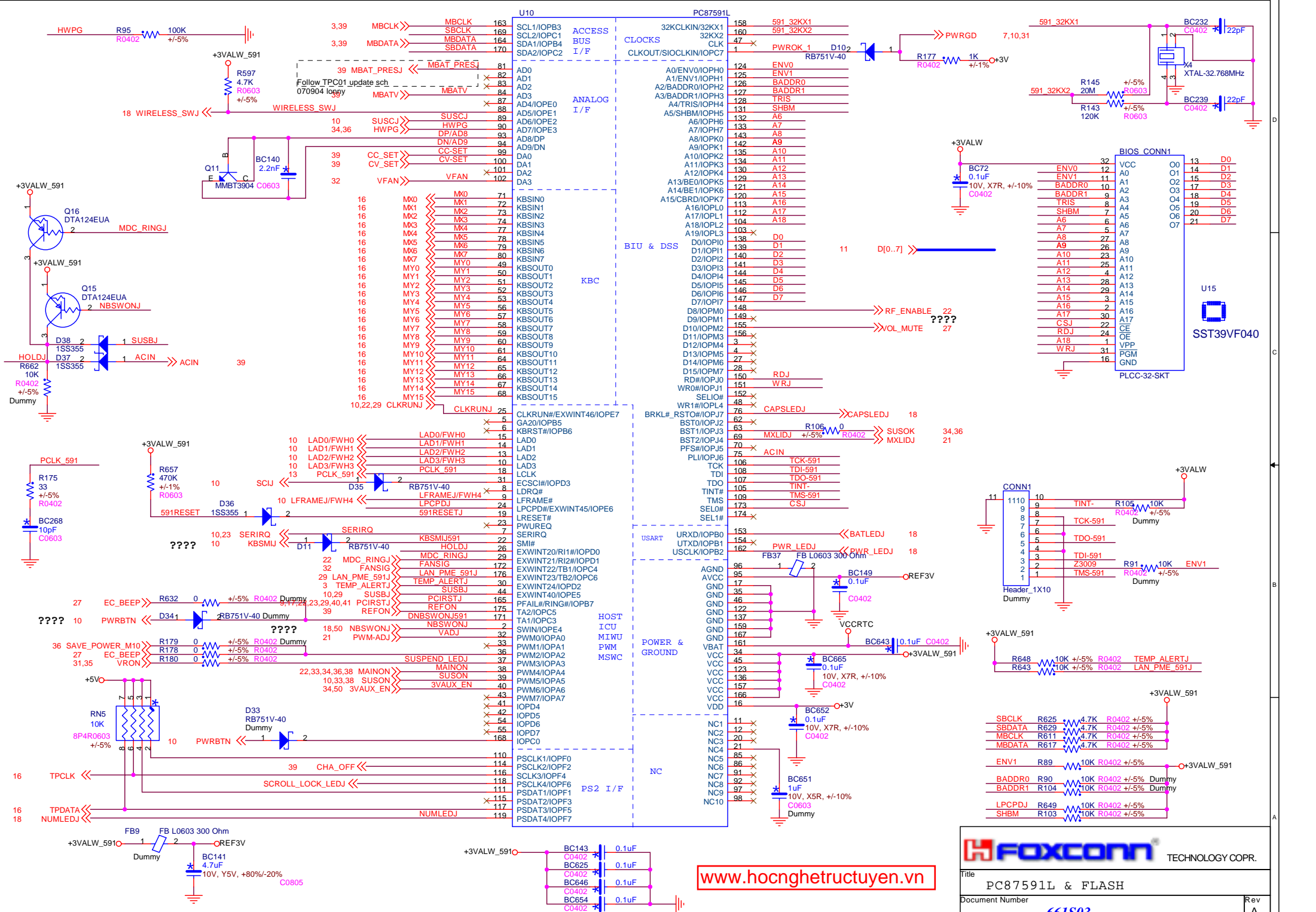
# Clock Buffer (DDR)

(OPTIONS)  
1: (ICS-93705)



www.hocnghetructuyen.vn





www.hocnghetructuyen.vn

**FOXCONN TECHNOLOGY COPR.**

Title: PC87591L & FLASH

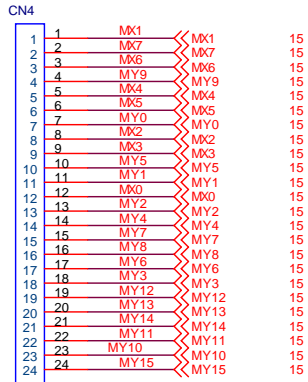
Document Number: 661S03

Date: Friday, August 13, 2004

Sheet 15 of 50

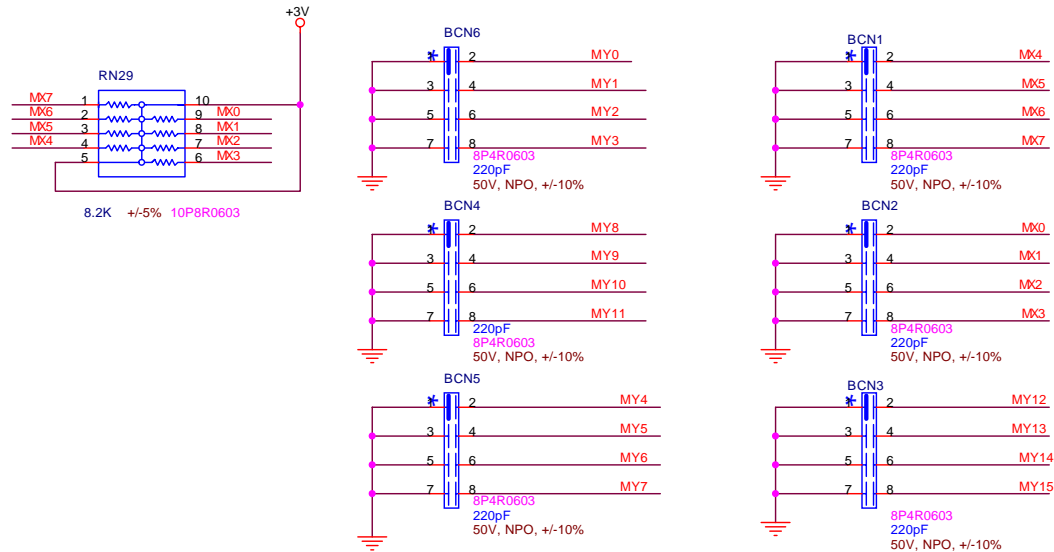
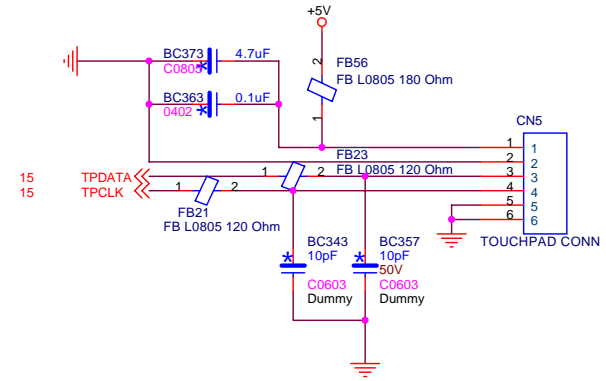
Rev A

# KEY BOARD



KB CONN

# TOUCH PAD



[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

**FOXCONN** TECHNOLOGY COPR.

Title: **KB & TOUCHPAD**

Document Number: **661S03**

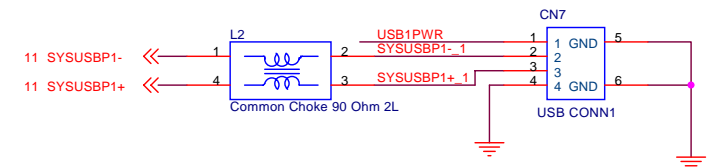
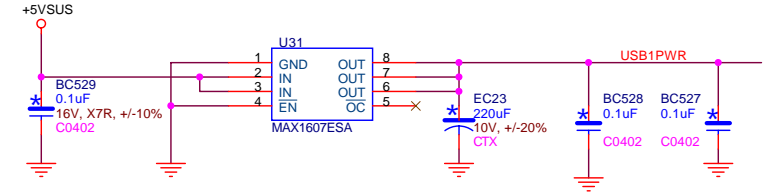
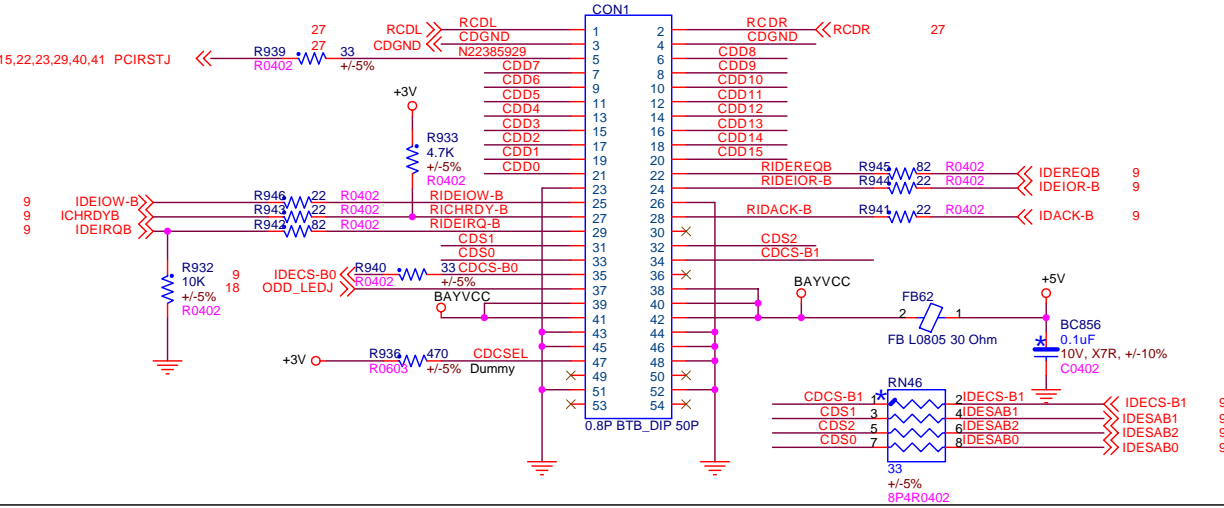
Date: Friday, August 13, 2004

Rev: **A**

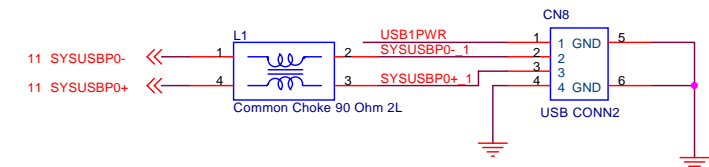
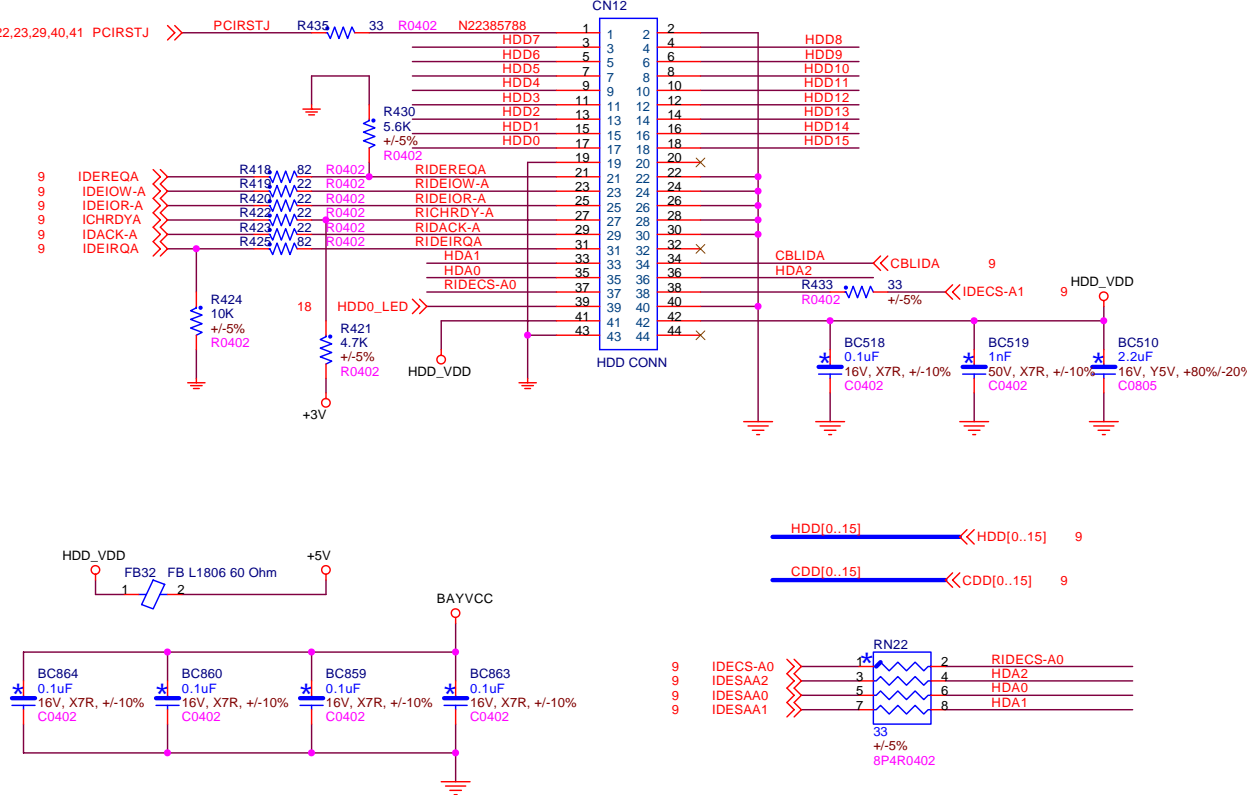
Sheet 16 of 50



### ODD CONNECTOR

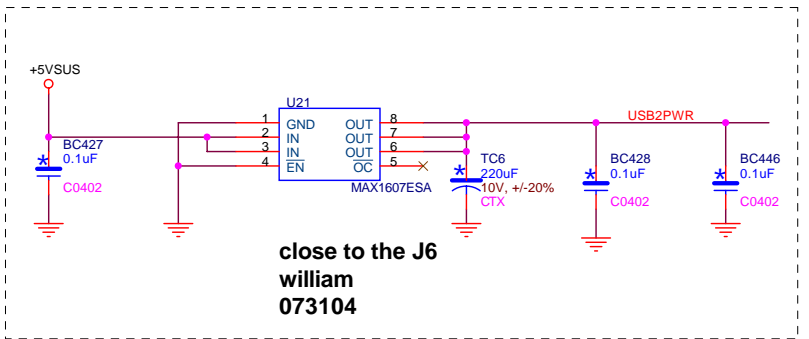
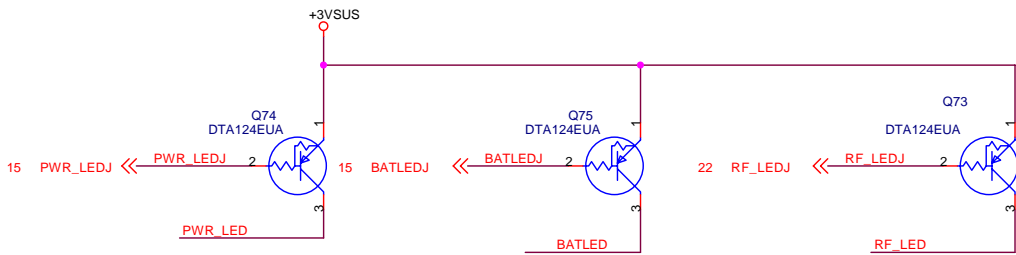
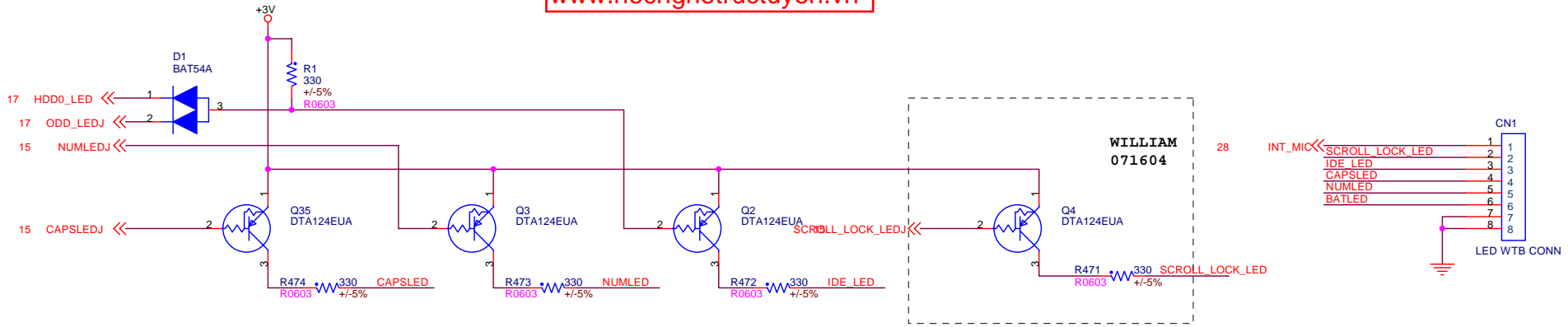


### HDD CONNECTOR

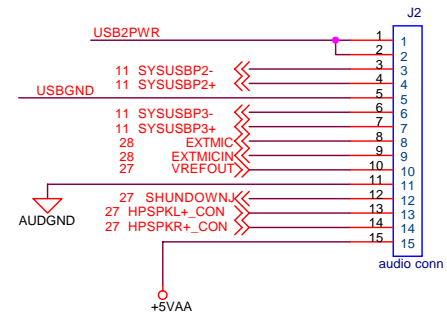
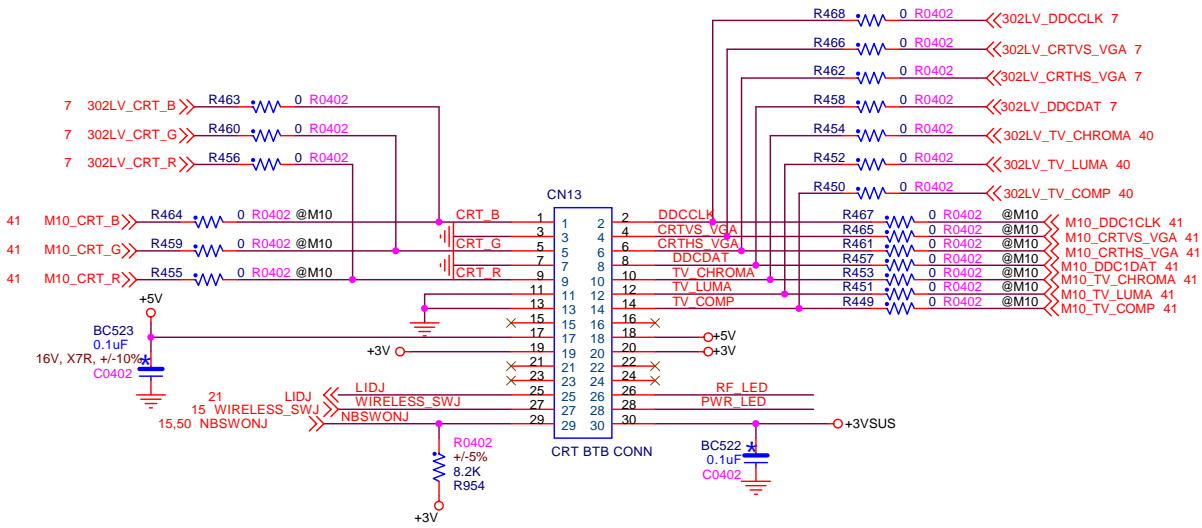


www.hocnghetructuyen.vn

**FOXCONN** TECHNOLOGY COPR.  
 Title: HDD / ODD / USB\_1  
 Document Number: 661S03  
 Date: Friday, August 13, 2004  
 Sheet: 17 of 50  
 Rev: A

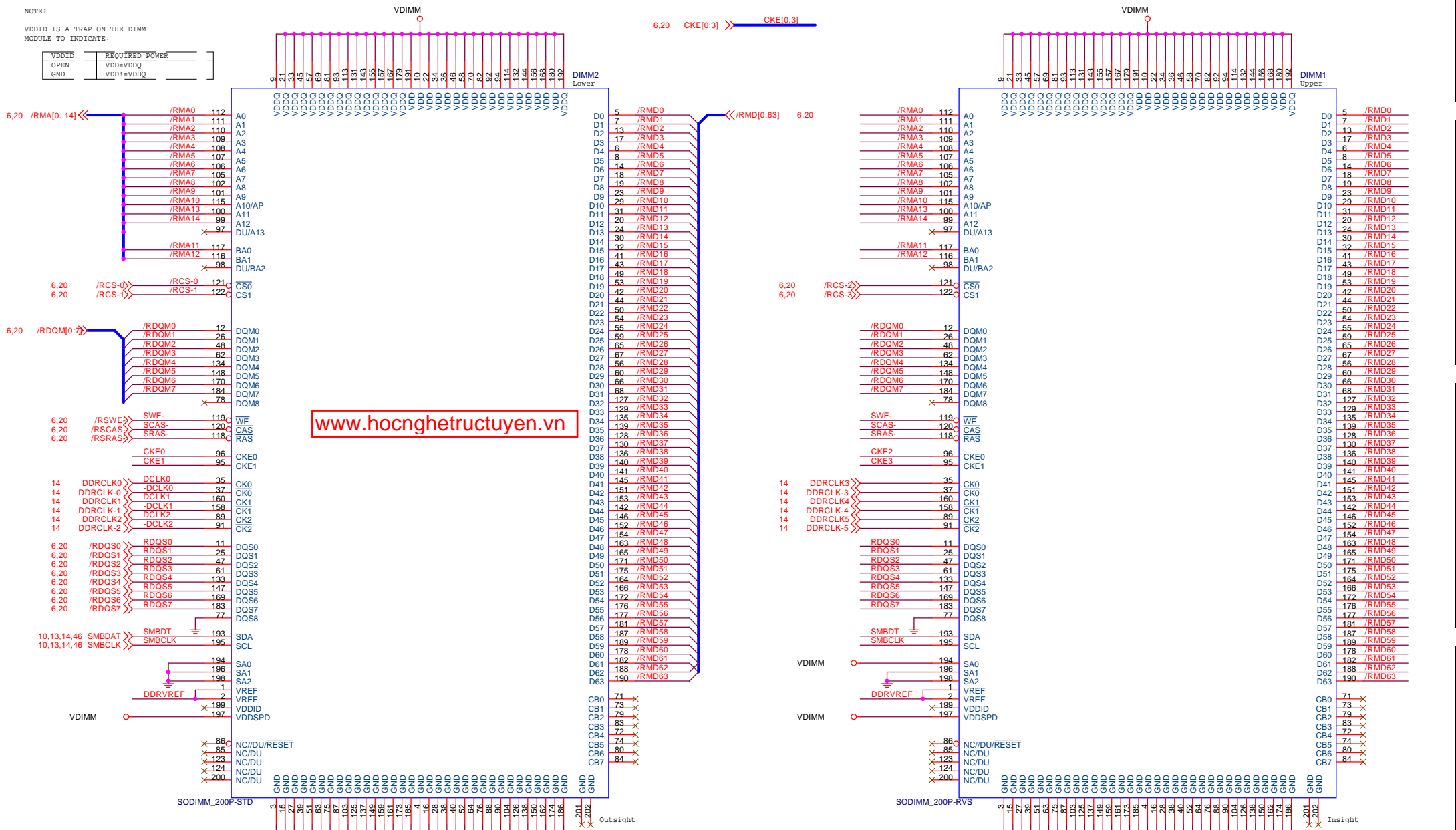


close to the J6  
william  
073104

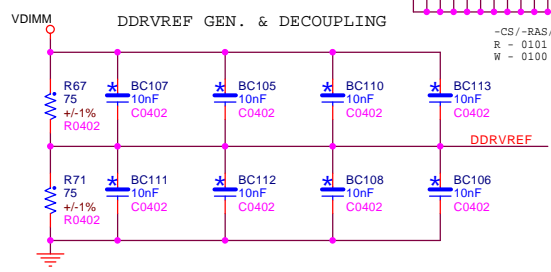


NOTE:  
VDDID IS A TRAP ON THE DIMM MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ



www.hocnghetructuyen.vn



-CS/-RAS/-CAS/-WE PC2100 - CL2 = 15 to Data 2-2-2/2.5-3-3  
R = 0101 CL2.5 = 18.75 to Data  
W = 0100 DDR266 256MB 4Bks Pmax = 8W  
Ptyp = 7W  
64MB/128MB/256MB - 500MB/s - 1.0W  
- 1000MB/s - 1.65W  
- 1500MB/s - 2.5W  
- 2000MB/s - 3.2W

**FOXCONN** TECHNOLOGY CORP.

Title

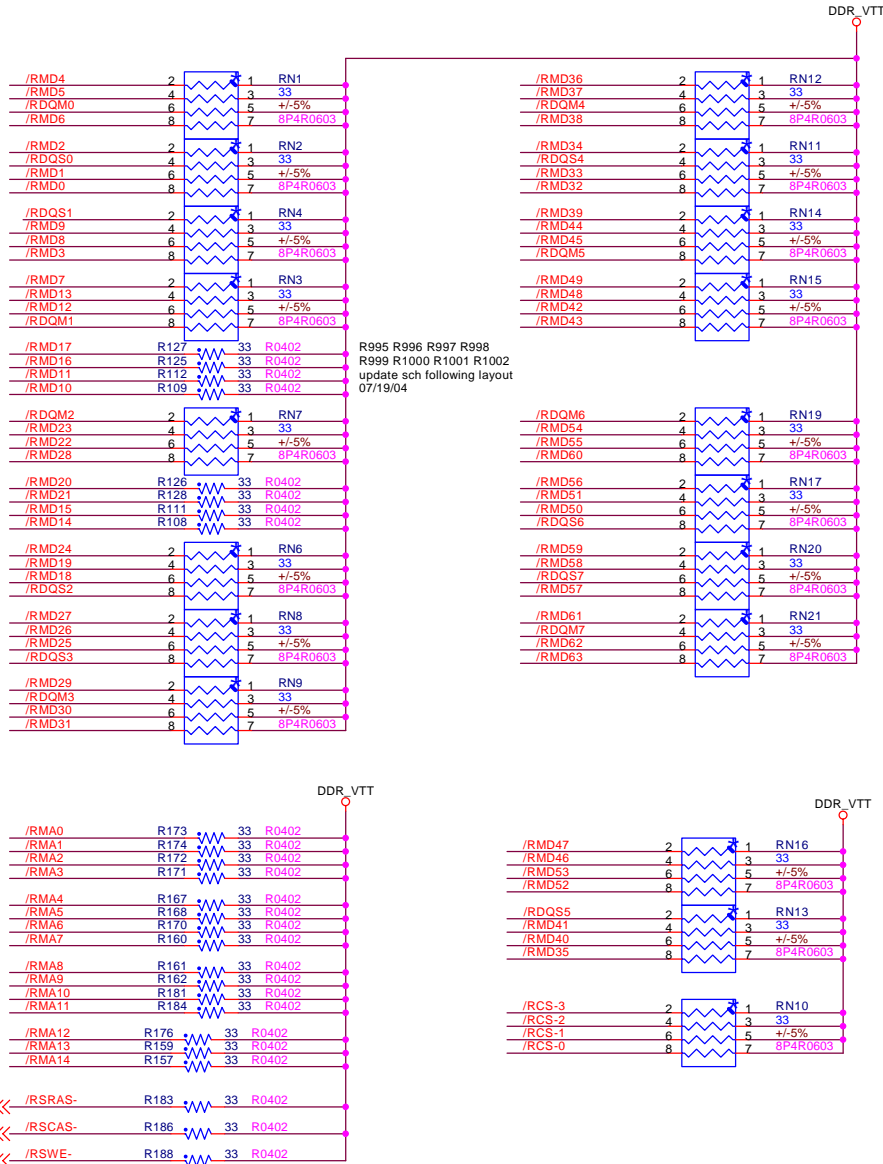
Document Number **66IS03** Rev A

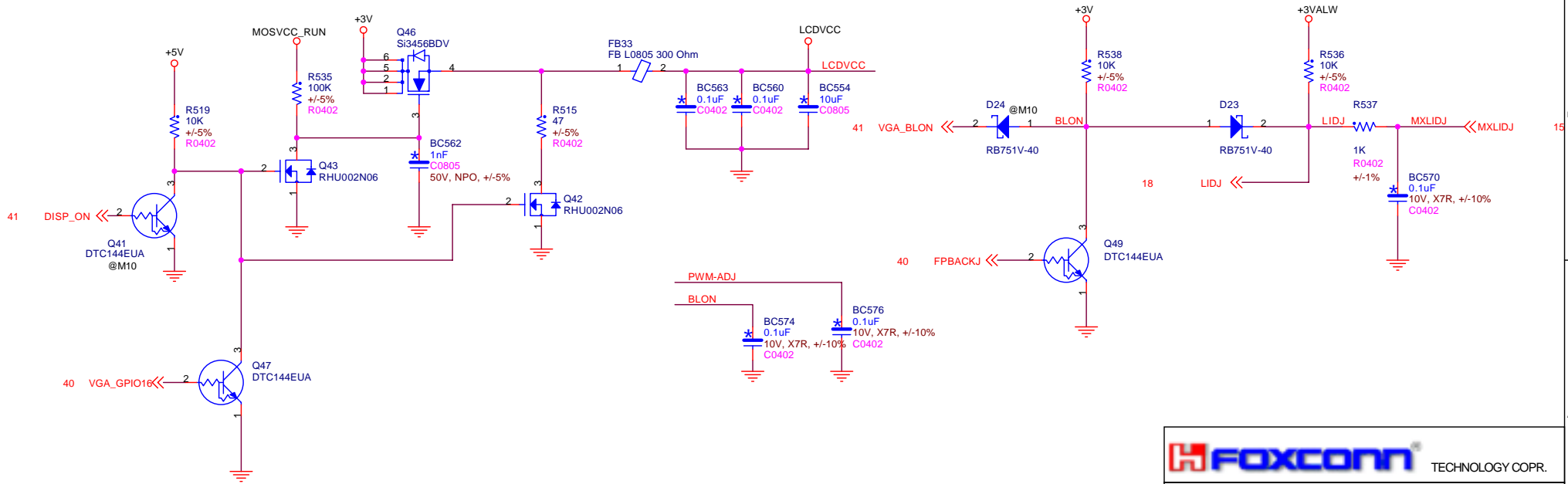
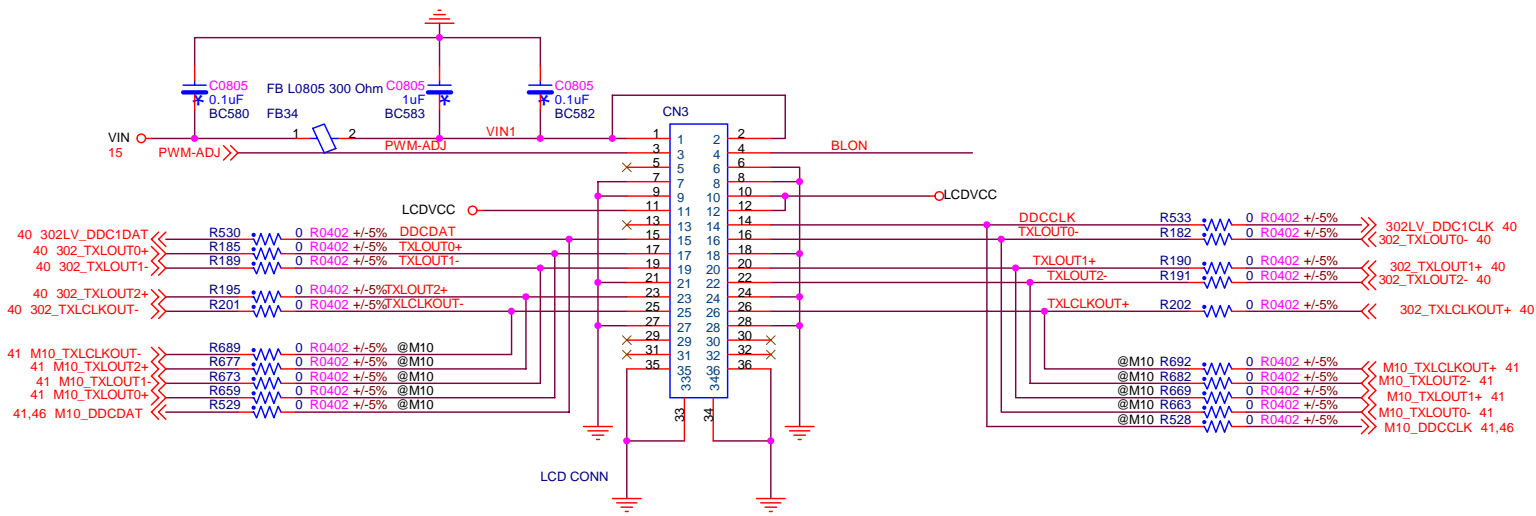
Date: Friday, August 13, 2004 Sheet 19 of 50

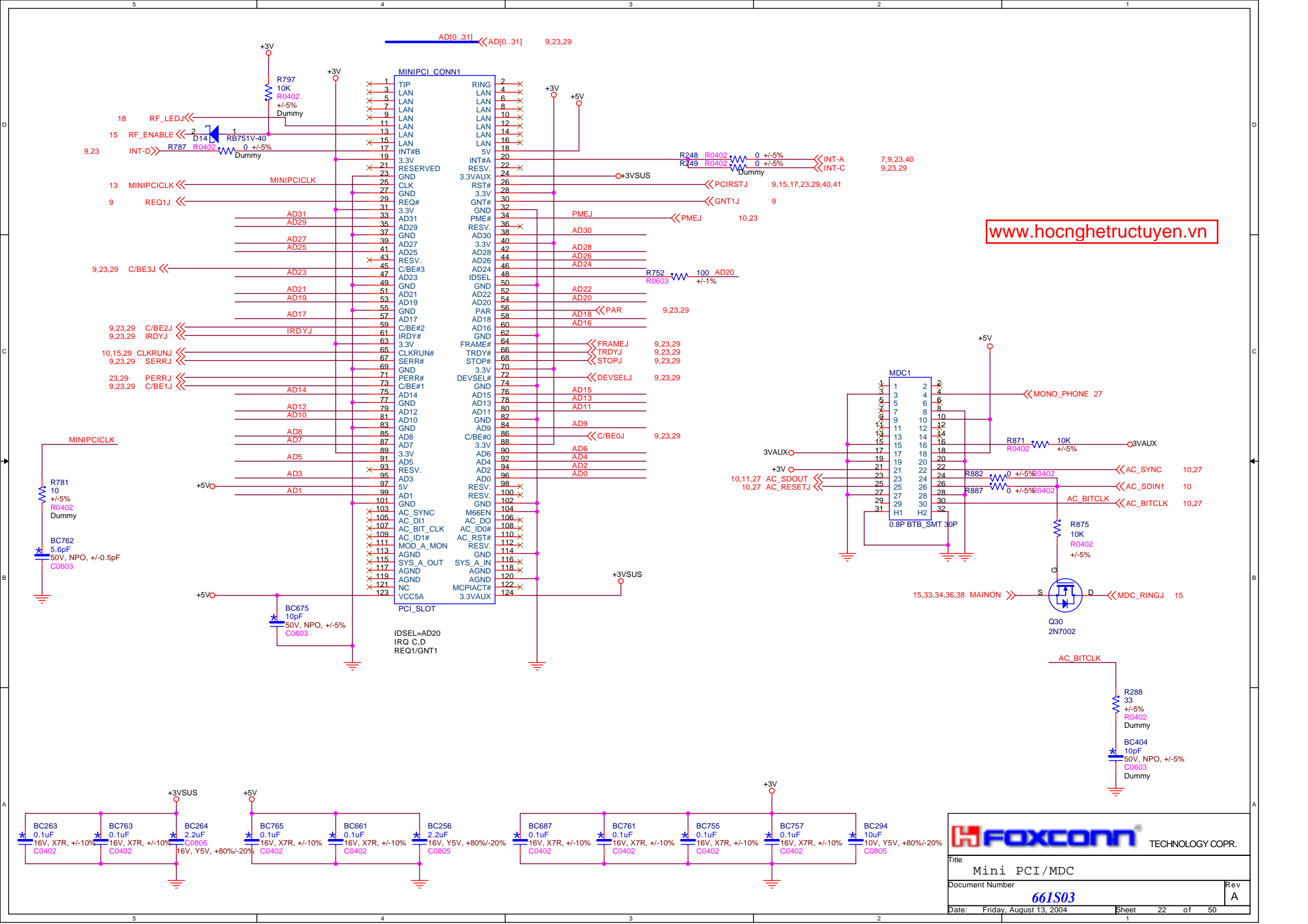
# SSTL-2 Termination Resistors



	SDR	DDR
MD/DQM/(DQS)	LV-CMOS	SSTL-2
MA/Control	LV-CMOS	SSTL-2
C/S	LV-CMOS	SSTL-2
CKE	DD 3.3V	DD 2.5V
	$R_s$ 0/10/ 10	$R_s$ 0 0
		$R_{tt}$ 33 33 47



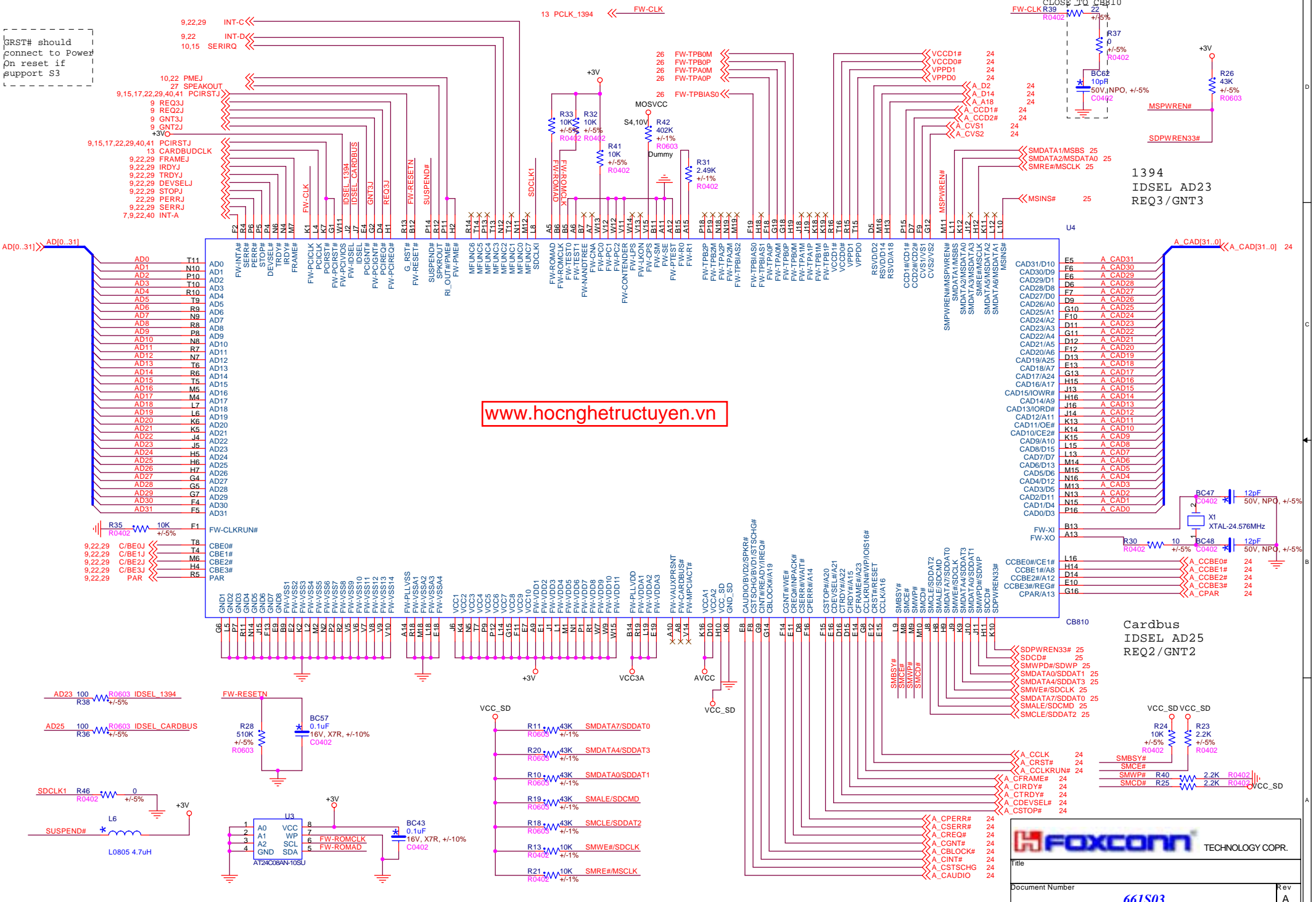




www.hocnghetructuyen.vn



SRST# should connect to Power On reset if support S3



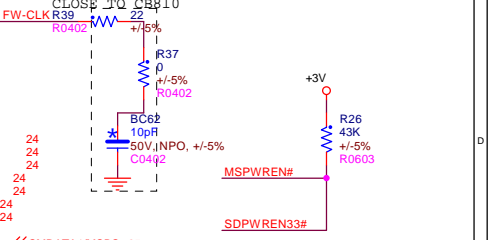
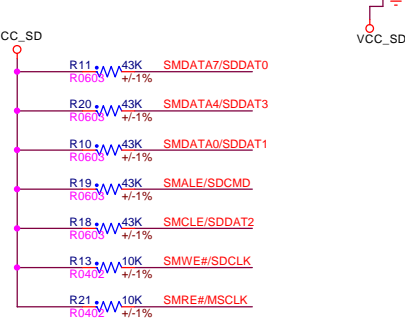
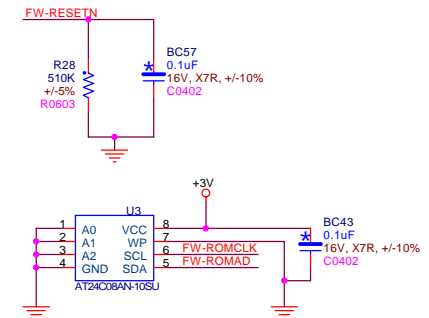
- 9,22,29 INT-C
- 9,22 INT-D
- 10,15 SERIRQ
- 10,22 PMEJ
- 27 SPEAKOUT
- 9,15,17,22,29,40,41 PCIRSTJ
- 9 REQ3J
- 9 REQ2J
- 9 GNT3J
- 9 GNT2J
- +3V
- 9,15,17,22,29,40,41 PCIRSTJ
- 13 CARDBUCLK
- 9,22,29 FRAMEJ
- 9,22,29 IRDYJ
- 9,22,29 TRDYJ
- 9,22,29 DEVSELJ
- 9,22,29 STOPJ
- 2,29 PERRJ
- 9,22,29 SERRJ
- 7,9,22,40 INT-A

- AD0
- AD1
- AD2
- AD3
- AD4
- AD5
- AD6
- AD7
- AD8
- AD9
- AD10
- AD11
- AD12
- AD13
- AD14
- AD15
- AD16
- AD17
- AD18
- AD19
- AD20
- AD21
- AD22
- AD23
- AD24
- AD25
- AD26
- AD27
- AD28
- AD29
- AD30
- AD31

- 9,22,29 C/BE0J
- 9,22,29 C/BE1J
- 9,22,29 C/BE2J
- 9,22,29 C/BE3J
- 9,22,29 PAR

- AD23 100 R0603 IDESEL 1394
- AD25 100 R0603 IDESEL CARDBUS

- SDCLK1 R46 0 R0402
- SUSPEND# L6



www.hocnghetructuyen.vn

1394  
IDSEL AD23  
REQ3/GNT3

Cardbus  
IDSEL AD25  
REQ2/GNT2

**FOXCONN** TECHNOLOGY COPR.

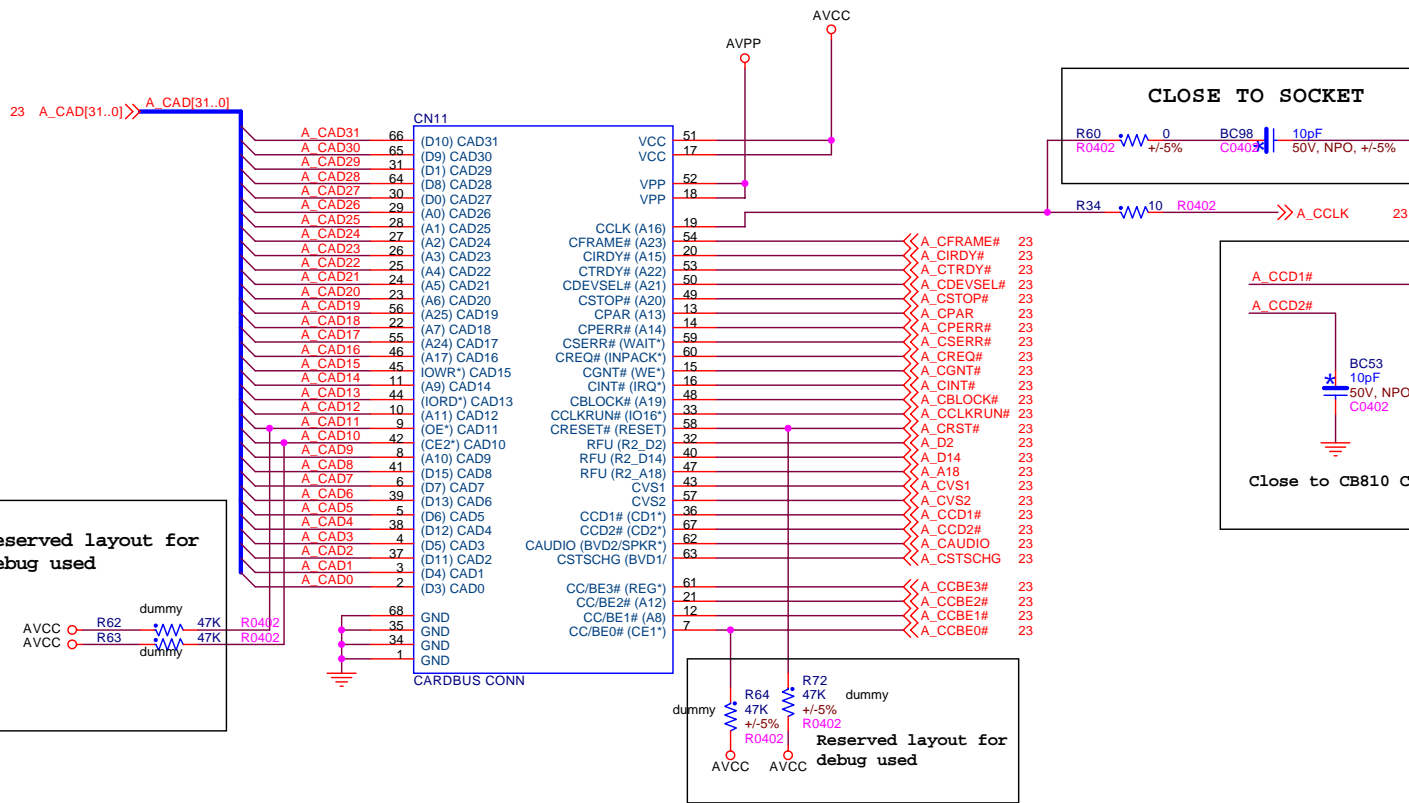
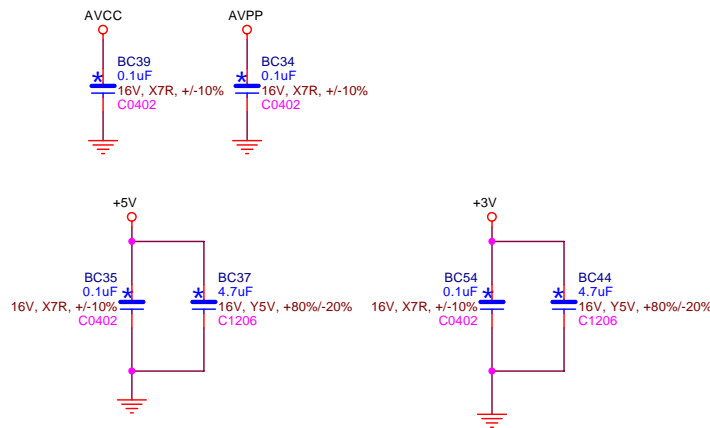
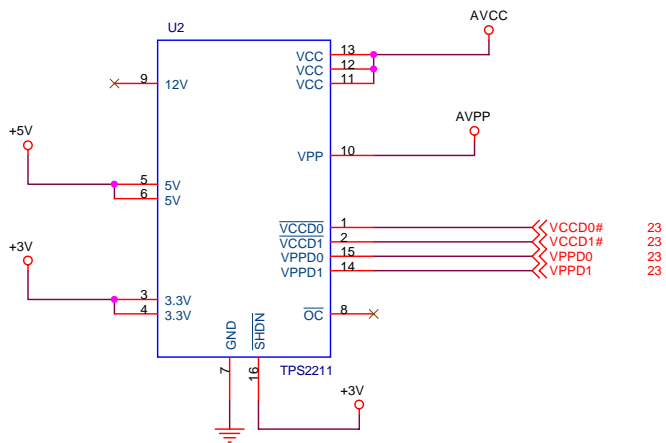
File: \_\_\_\_\_

Document Number: **661S03**

Date: Friday, August 13, 2004

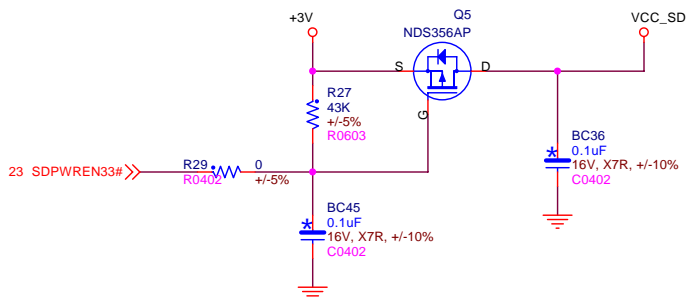
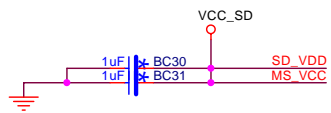
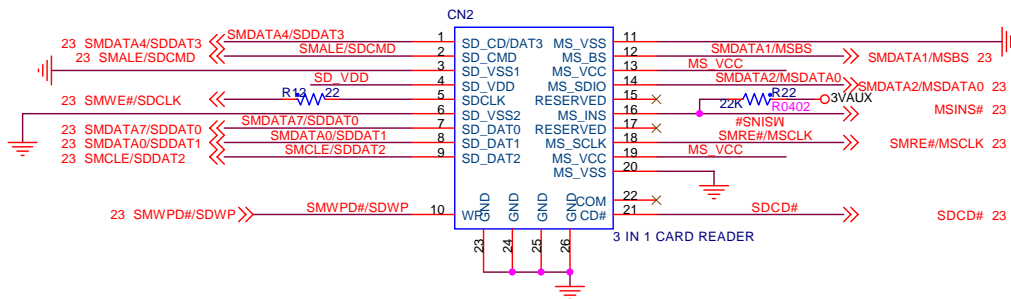
Sheet 23 of 50

Rev A

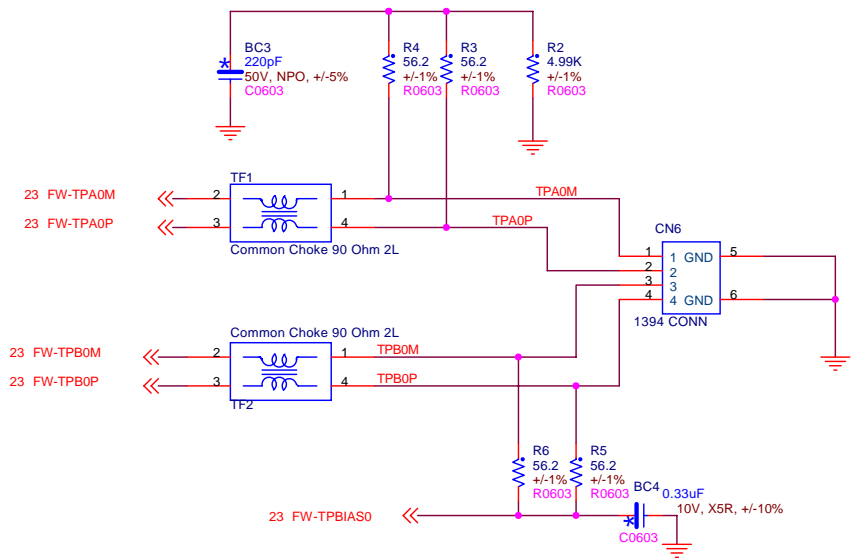


[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

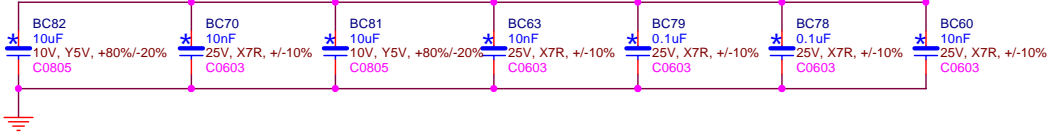
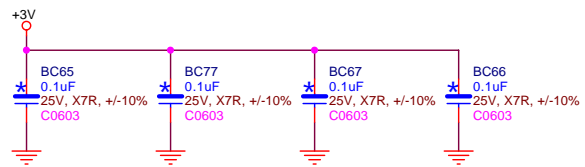
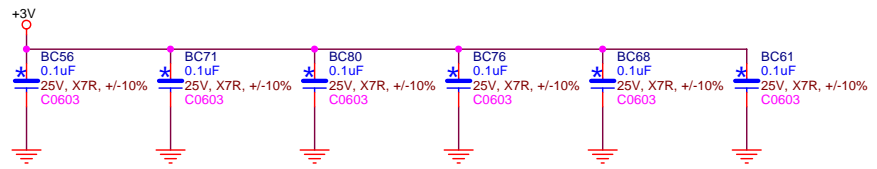
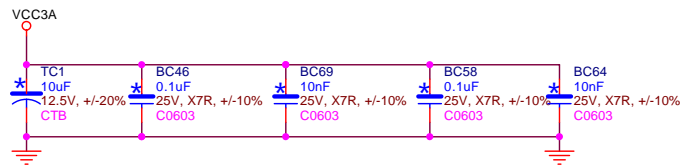




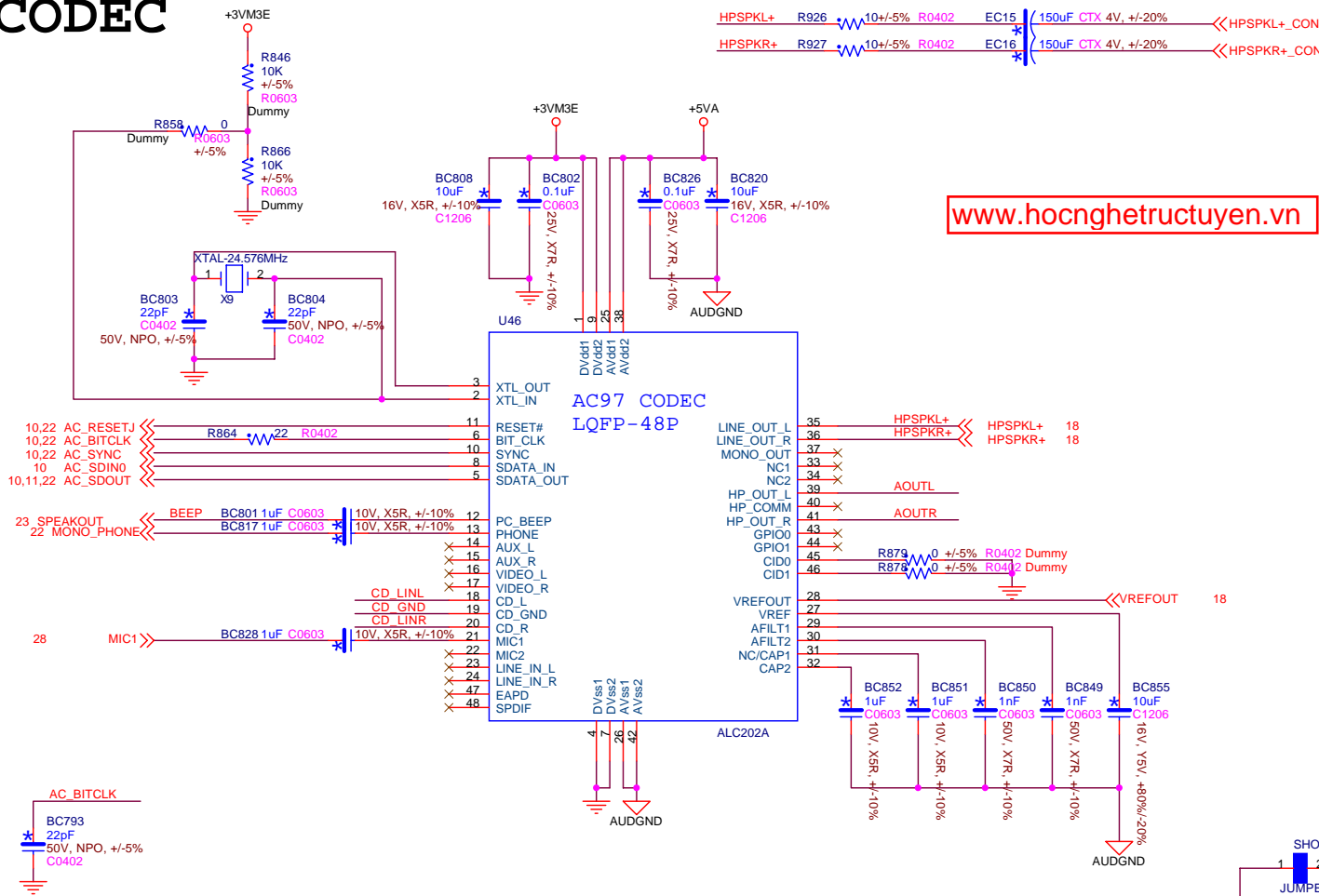
[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)



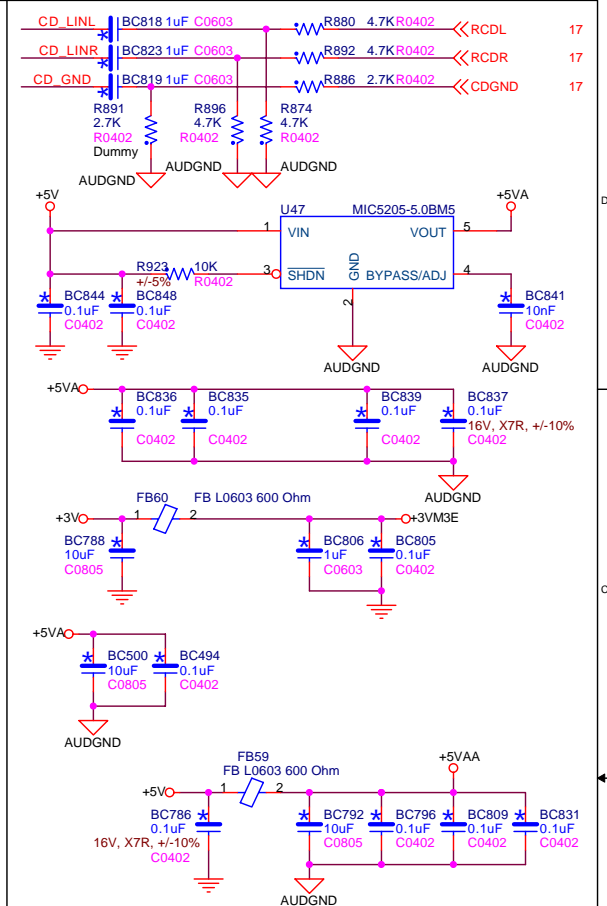
[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)



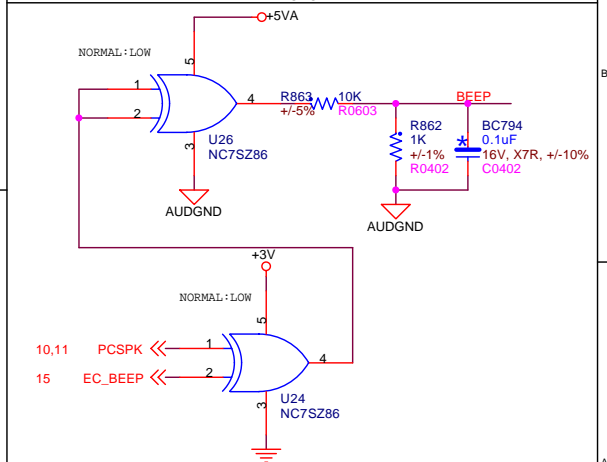
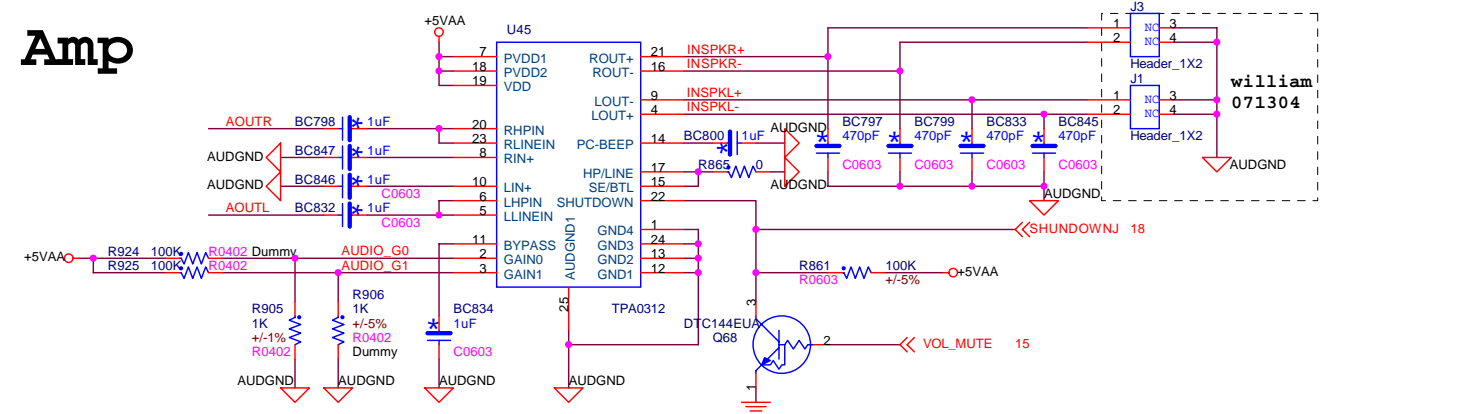
# CODEC



www.hocnghetructuyen.vn



# Amp



**FOXCONN** TECHNOLOGY COPR.

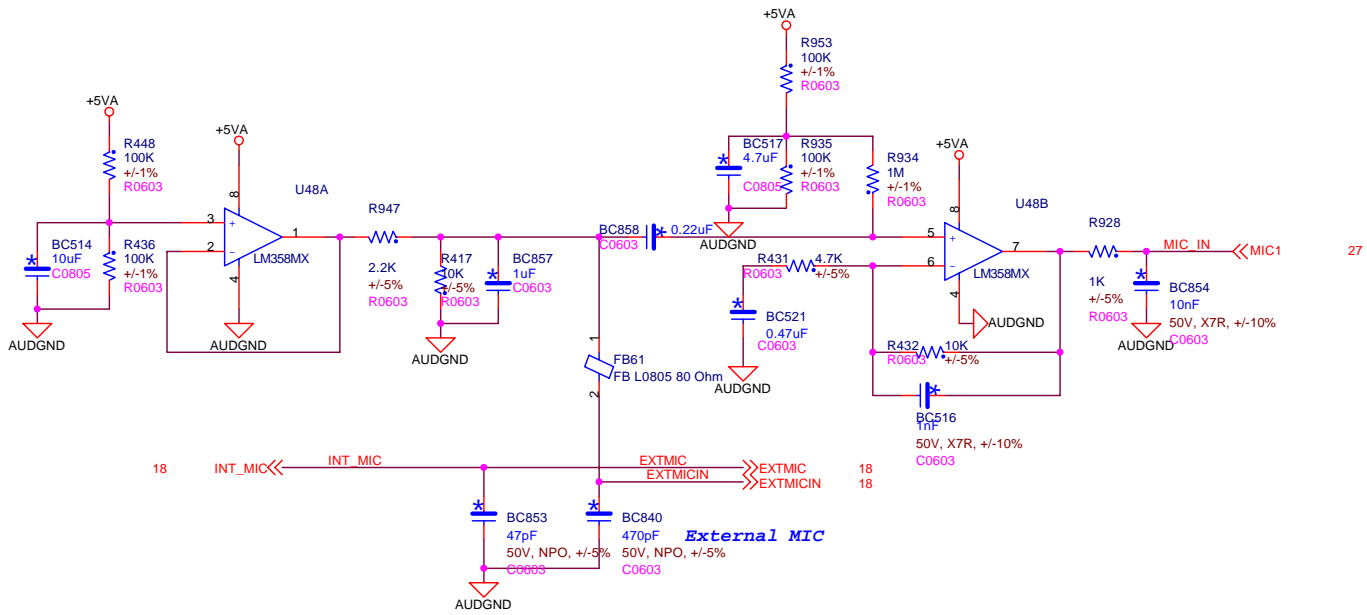
Title: **AUDIO ALC202A & AMP**

Document Number: **661S03**

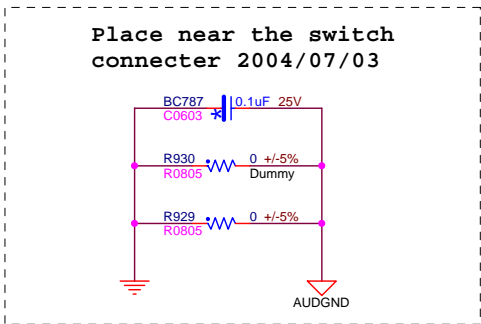
Date: Friday, August 13, 2004

Sheet 27 of 50

Rev A



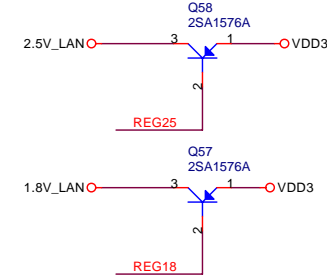
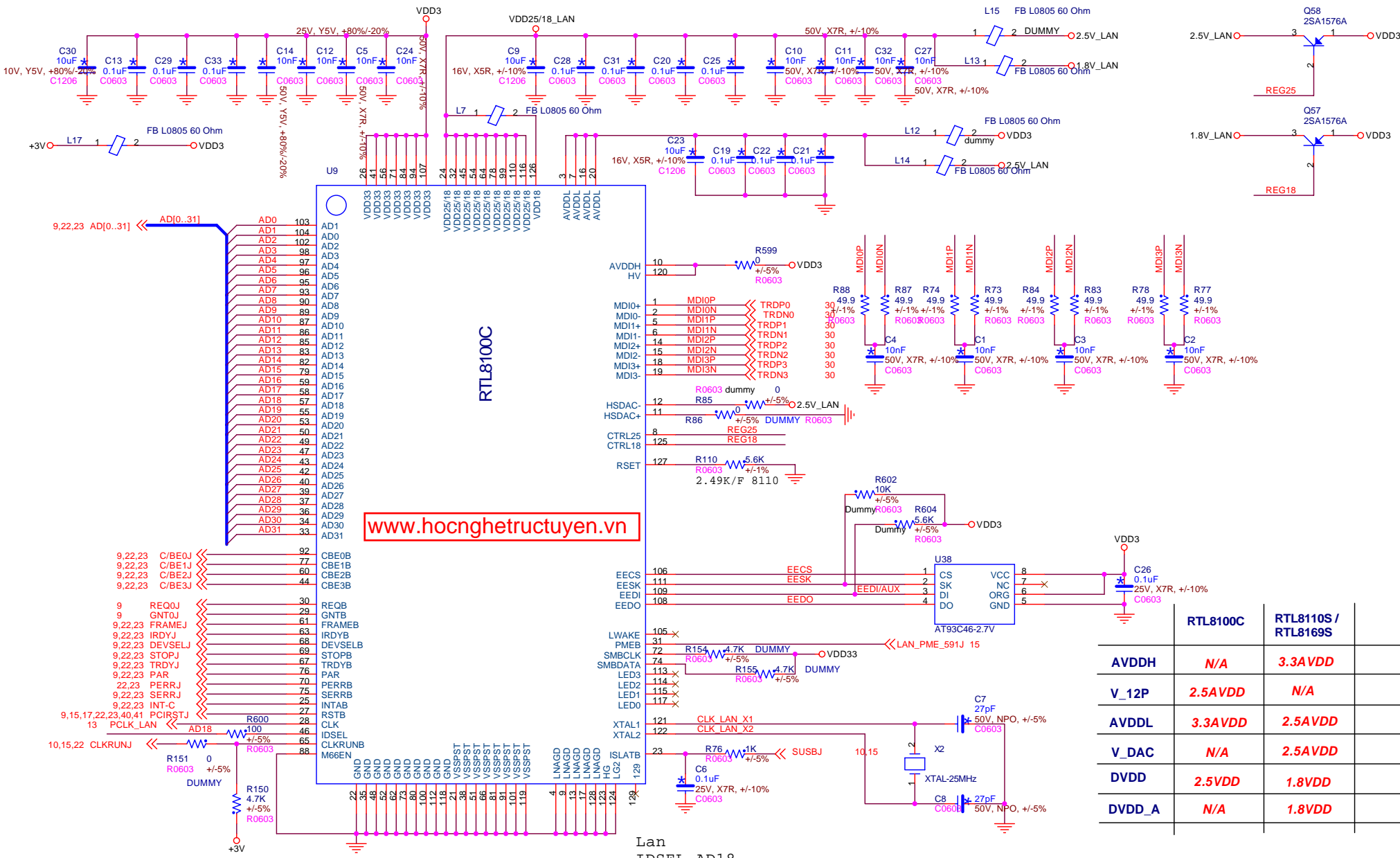
[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)



Title  
MIC Jack & AUDIO Jack

Document Number  
661S03

Rev  
A



www.hocnghetructuyen.vn

	RTL8100C	RTL8110S / RTL8169S	
AVDDH	N/A	3.3AVDD	
V_12P	2.5AVDD	N/A	
AVDDL	3.3AVDD	2.5AVDD	
V_DAC	N/A	2.5AVDD	
DVDD	2.5VDD	1.8VDD	
DVDD_A	N/A	1.8VDD	

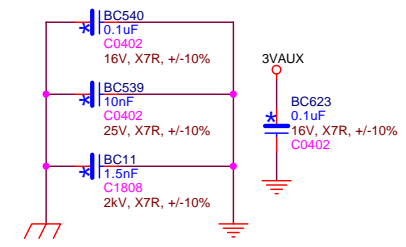
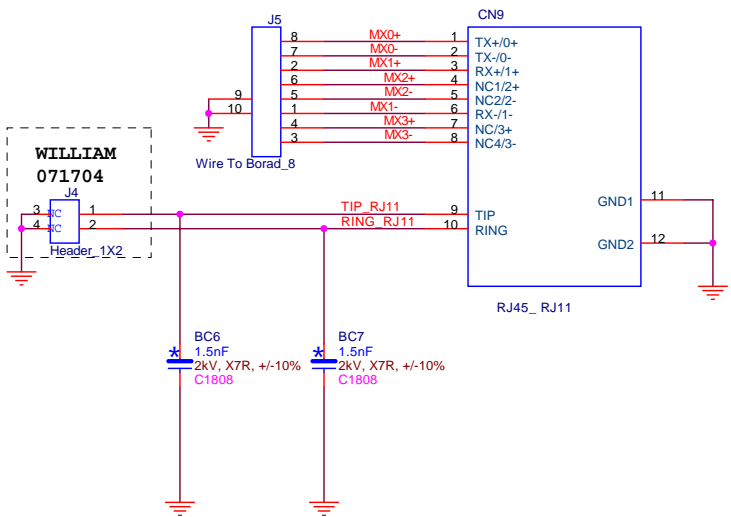
Lan  
IDSEL AD18  
REQ0/GNT0

**FOXCONN** TECHNOLOGY COPR.

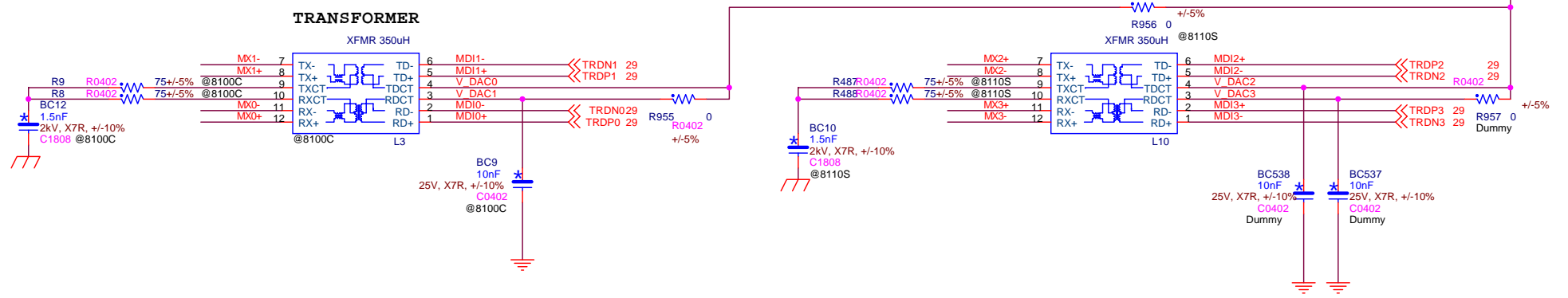
Title: **RTL8100**

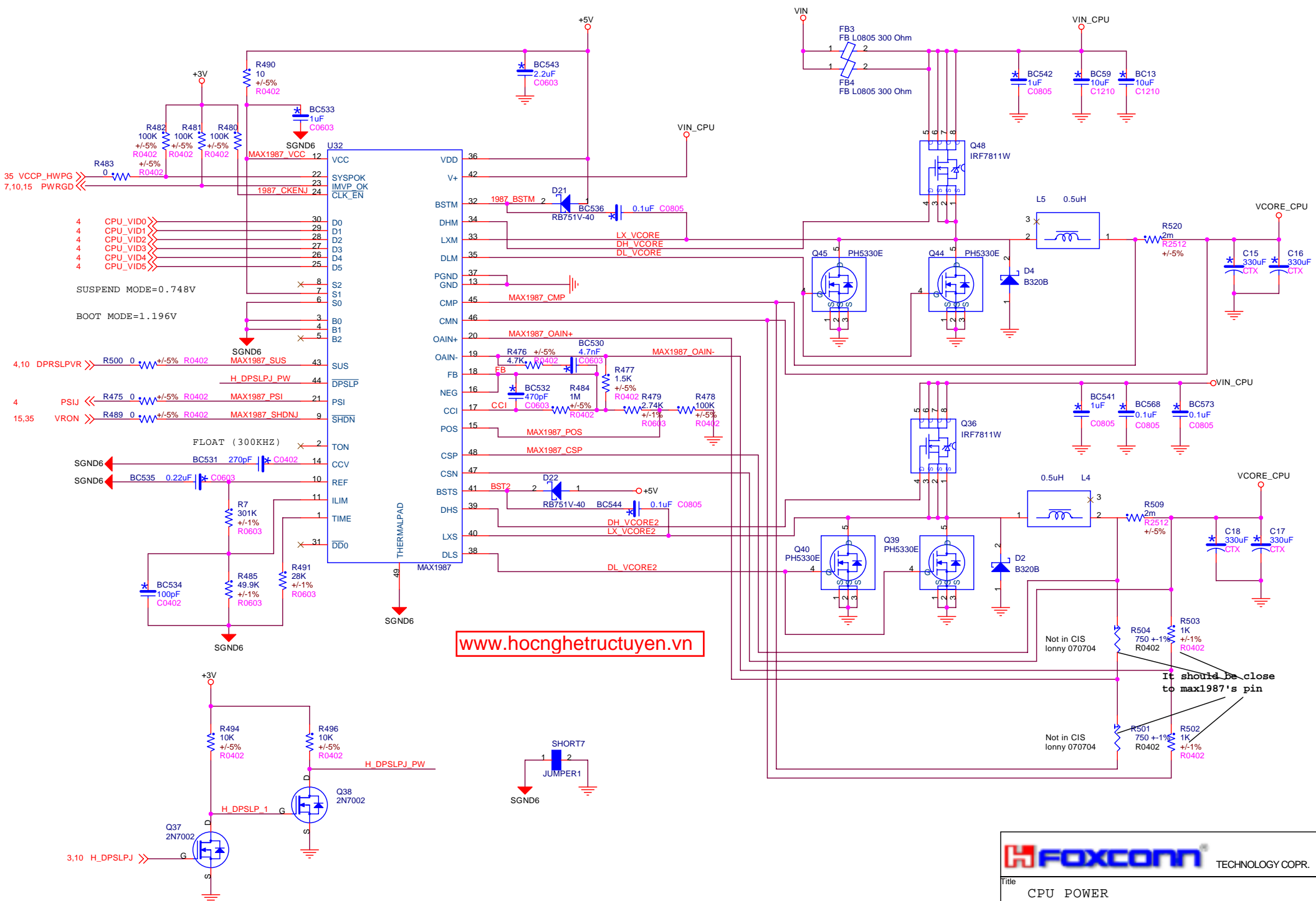
Document Number: \_\_\_\_\_ Rev: **A**

Date: Friday, August 13, 2004 Sheet: 29 of 50



www.hocnghetructuyen.vn





www.hocnghetructuyen.vn

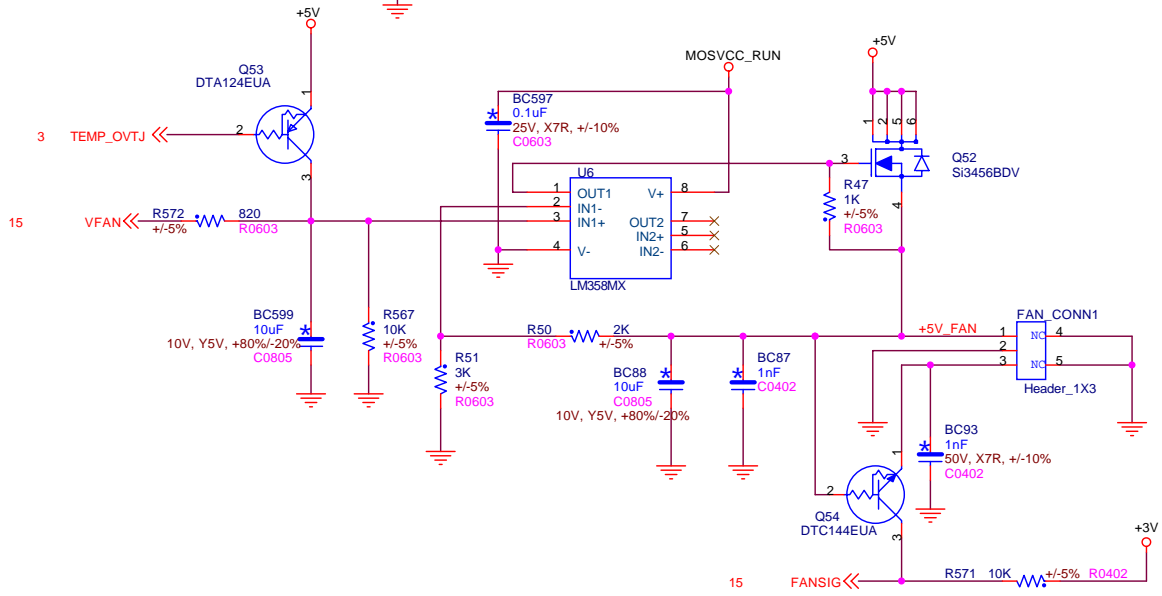
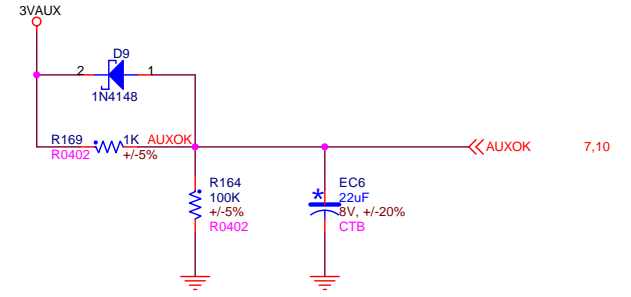
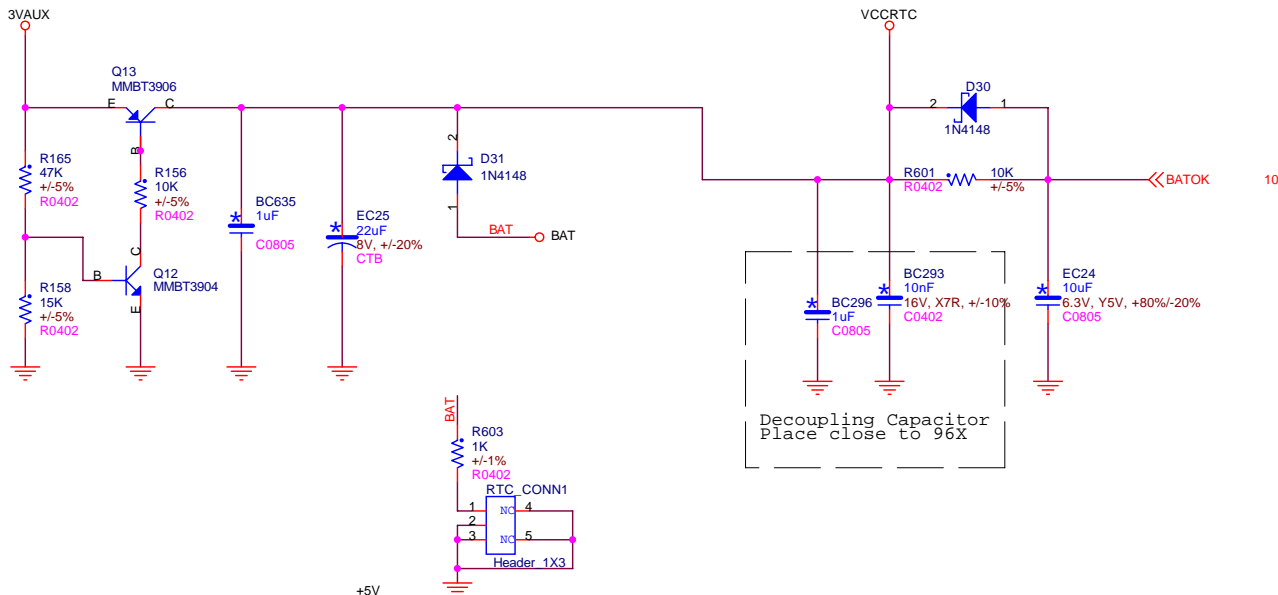
It should be close to max1987's pin



Title		CPU POWER	
Document Number		661S03	
Date:	Friday, August 13, 2004	Sheet	31 of 50
Rev	A		

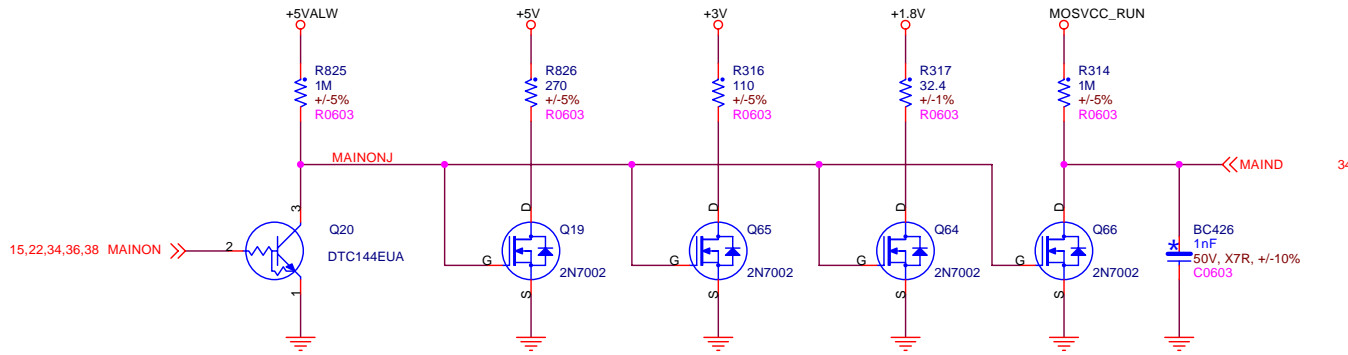
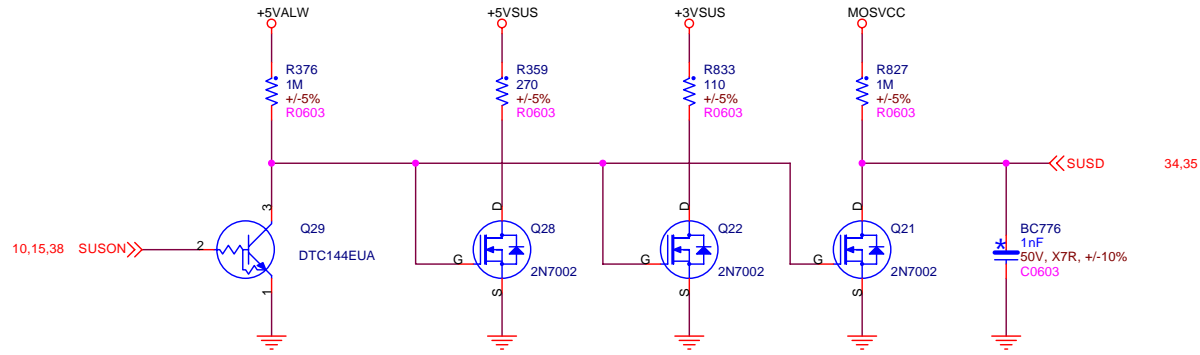
NOTE!

- 1.The VCCRTC is 3V
- 2.Decoupling capacitor must be close to 652 RTCVDD pin.
- 3.RTC circuit must strictly follow SiS's recommended design  
SiS is not responsible for RTC problems from foreign designs.

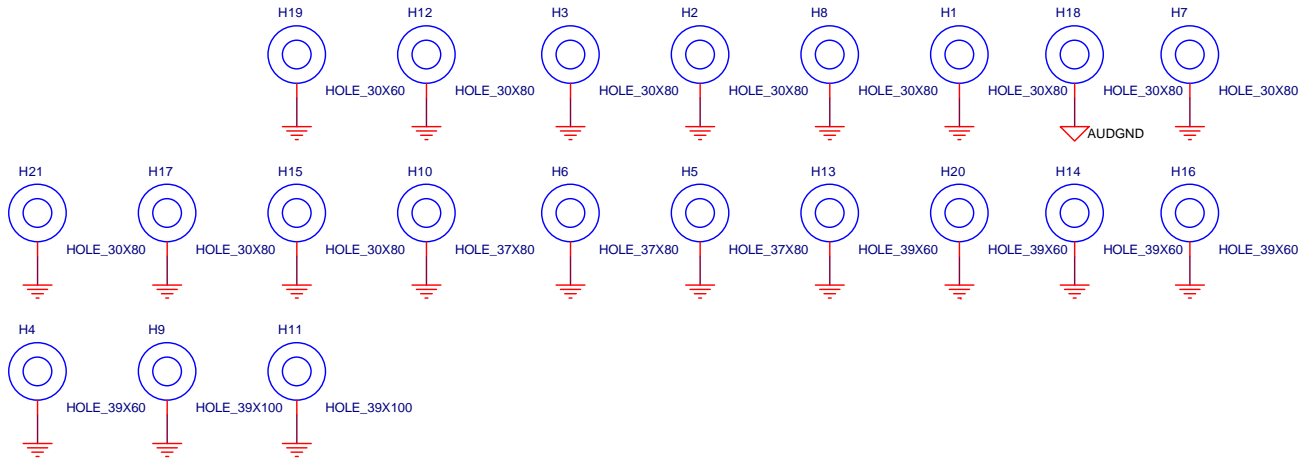


[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

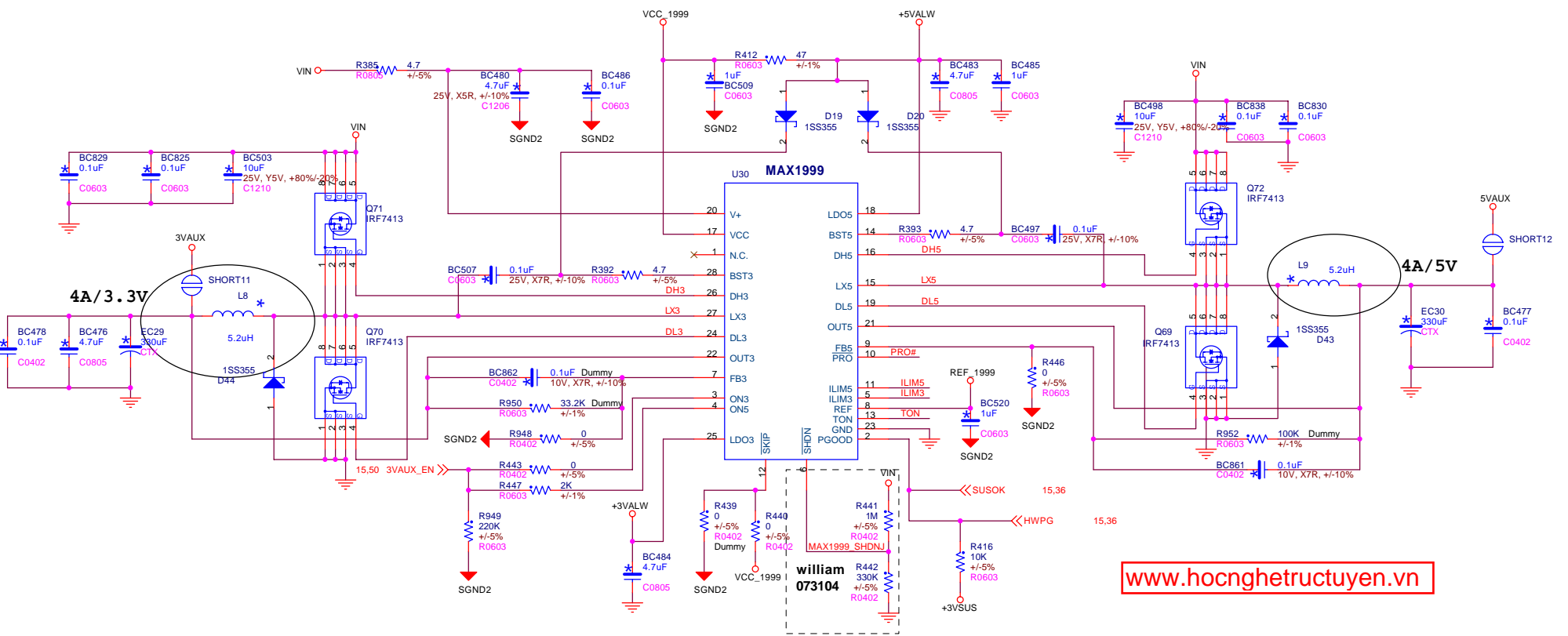




www.hocnghetructuyen.vn

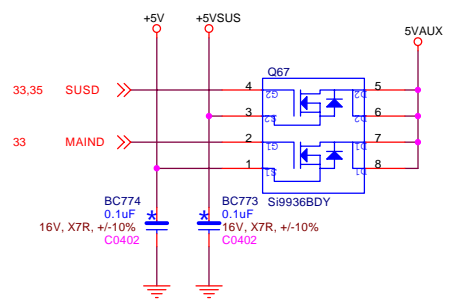
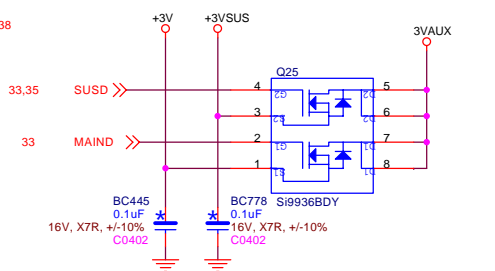
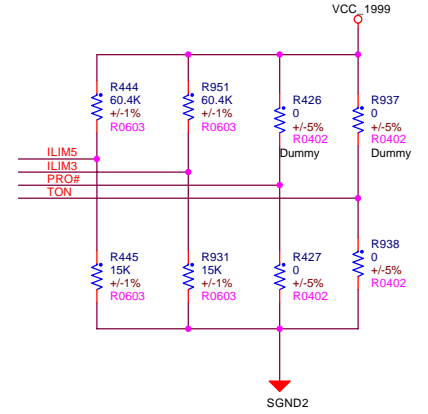
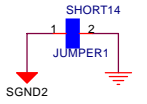
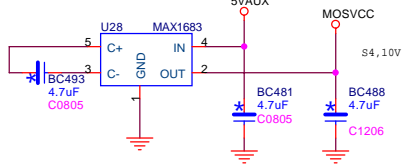
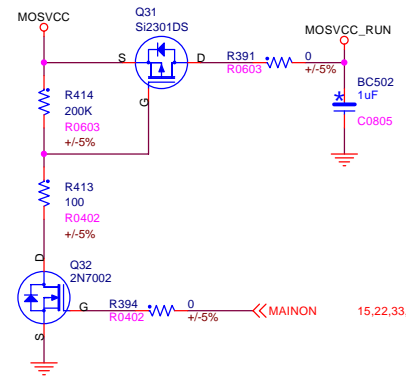


Title Discharge		Rev A
Document Number 661S03		
Date: Friday, August 13, 2004	Sheet 33	of 50



william  
073104

www.hocnghetructuyen.vn



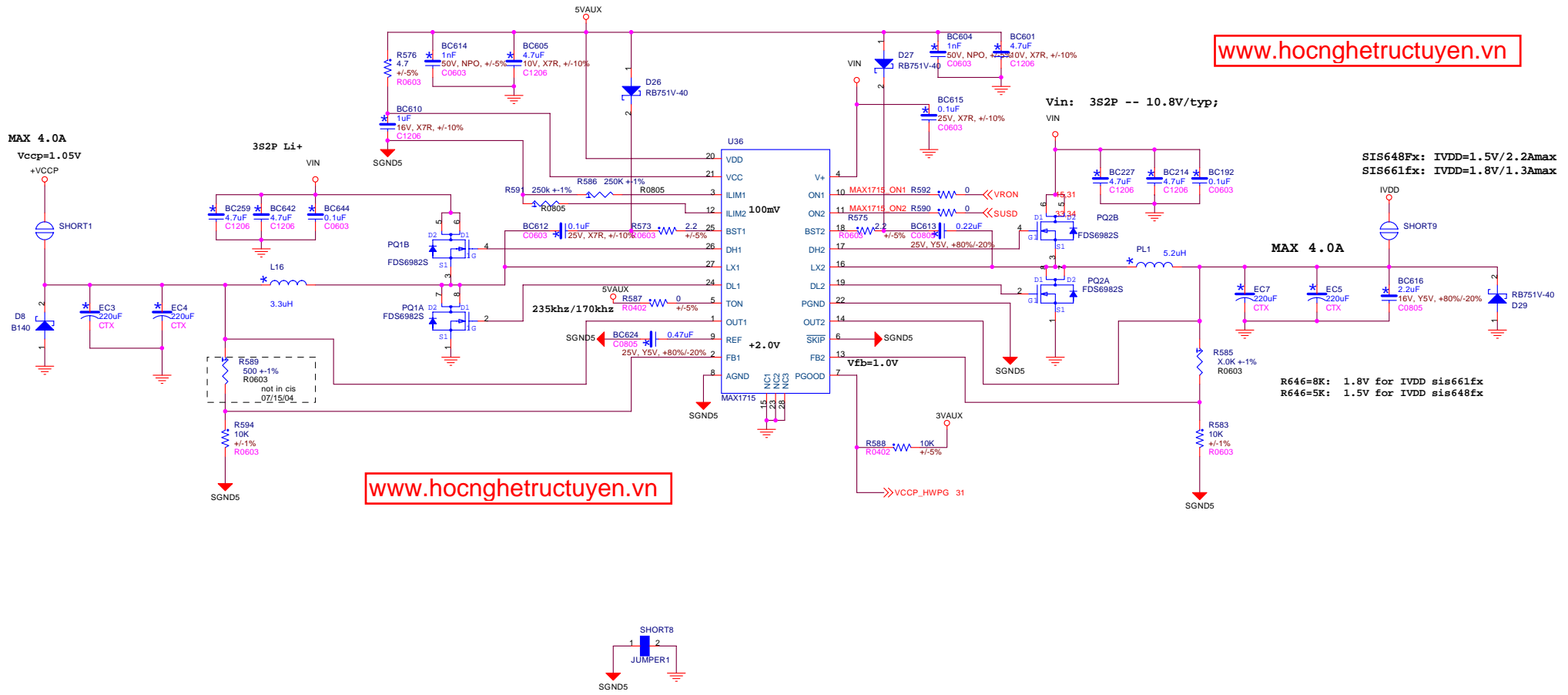
www.hocnghetructuyen.vn

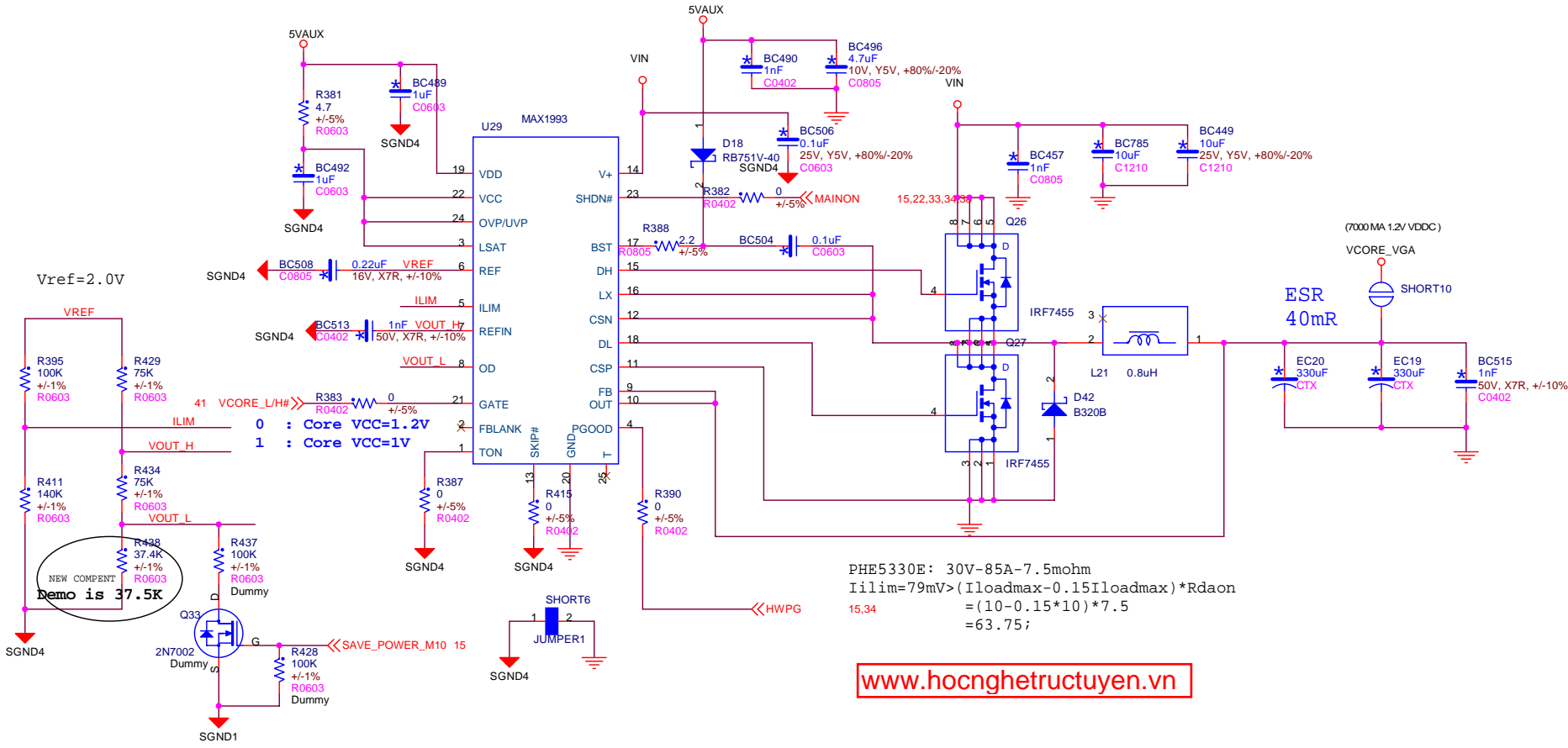
**FOXCONN** TECHNOLOGY COPR.

Title

Document Number **661S03** Rev **A**

Date: Friday, August 13, 2004 Sheet 34 of 50





Vref=2.0V

NEW COMPONENT  
Demo is 37.5K

PHE5330E: 30V-85A-7.5mohm  
 $I_{lim} = 79mV > (I_{loadmax} - 0.15 I_{loadmax}) * R_{daon}$   
 $= (10 - 0.15 * 10) * 7.5$   
 $= 63.75;$

www.hocnghetructuyen.vn

www.hocnghetructuyen.vn

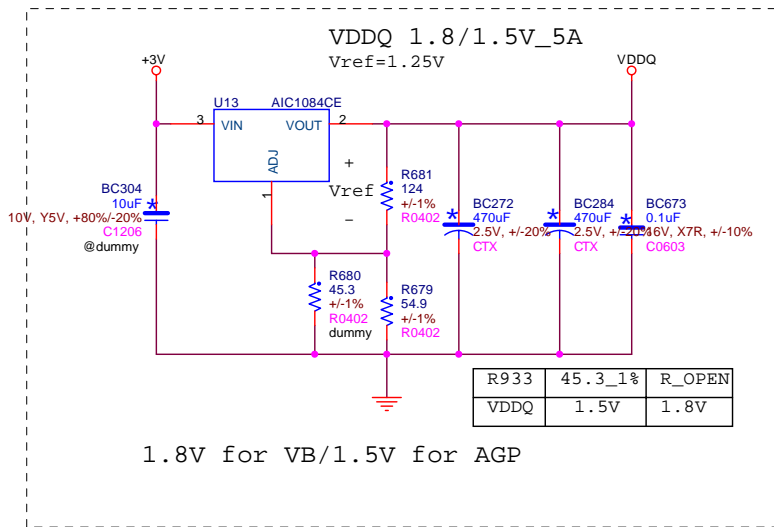


Title VCORE VGA

Document Number 661S03 Rev A

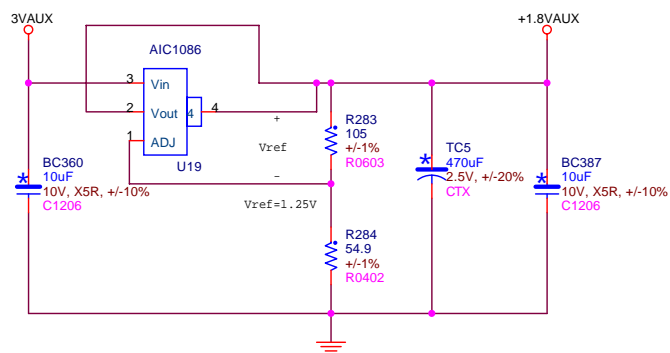
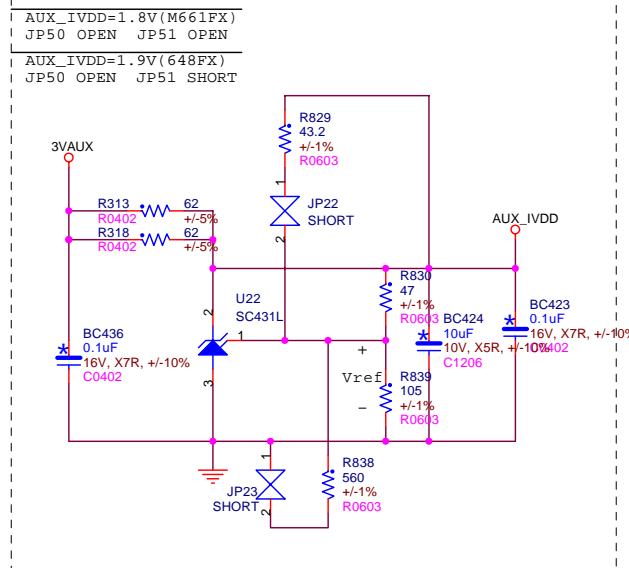
Date: Friday, August 13, 2004 Sheet 36 of 50

VDDQ  
M661FX+302LV is 1.8V ; 648FX+M10 is 1.5V  
Lonny 070804

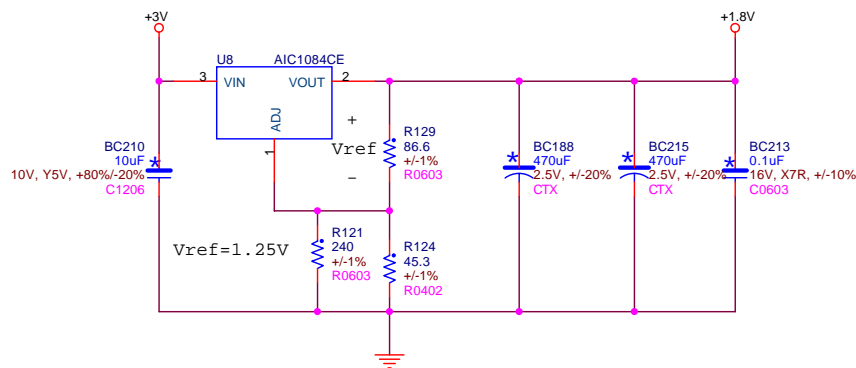


VDDQ Sis consumption Spec  
Current is 281.3mA( Only AGP8X)  
Lonny 070804

AUX\_IVDD 1.8V/1.9V  
Vref=1.24V  
for SB1.8V current 38mA (max)  
for SB1.5V current 48mA (max)



[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)



**FOXCONN** TECHNOLOGY COPR.

Title

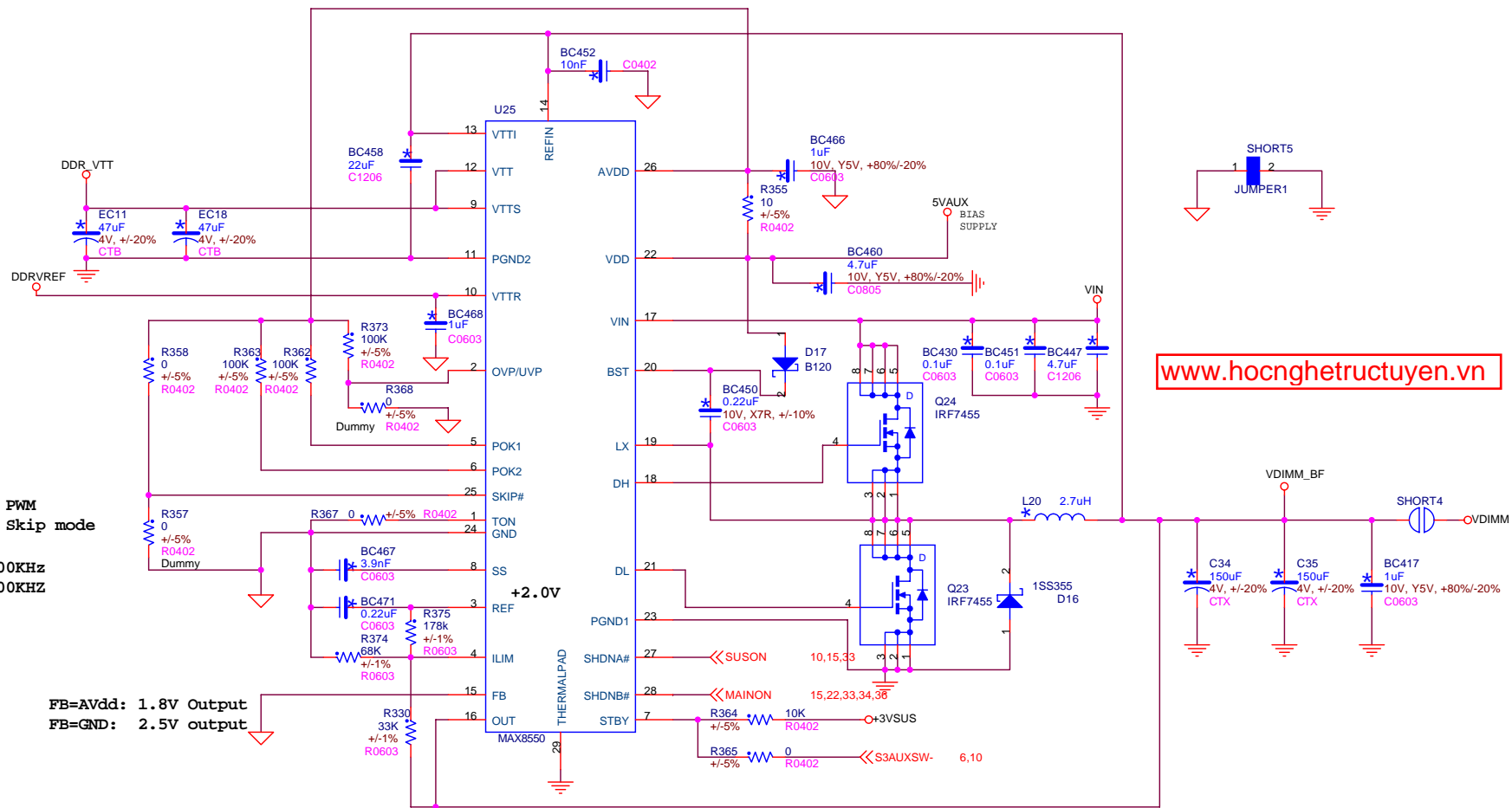
Document Number

661S03

Rev

A

Date: Friday, August 13, 2004 Sheet 37 of 50



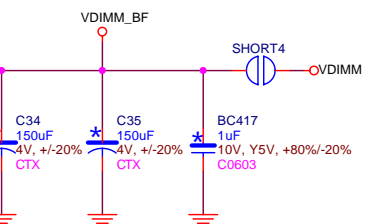
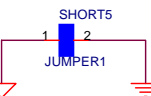
SKIP#=AVdd: PWM  
SKIP#=GND: Skip mode

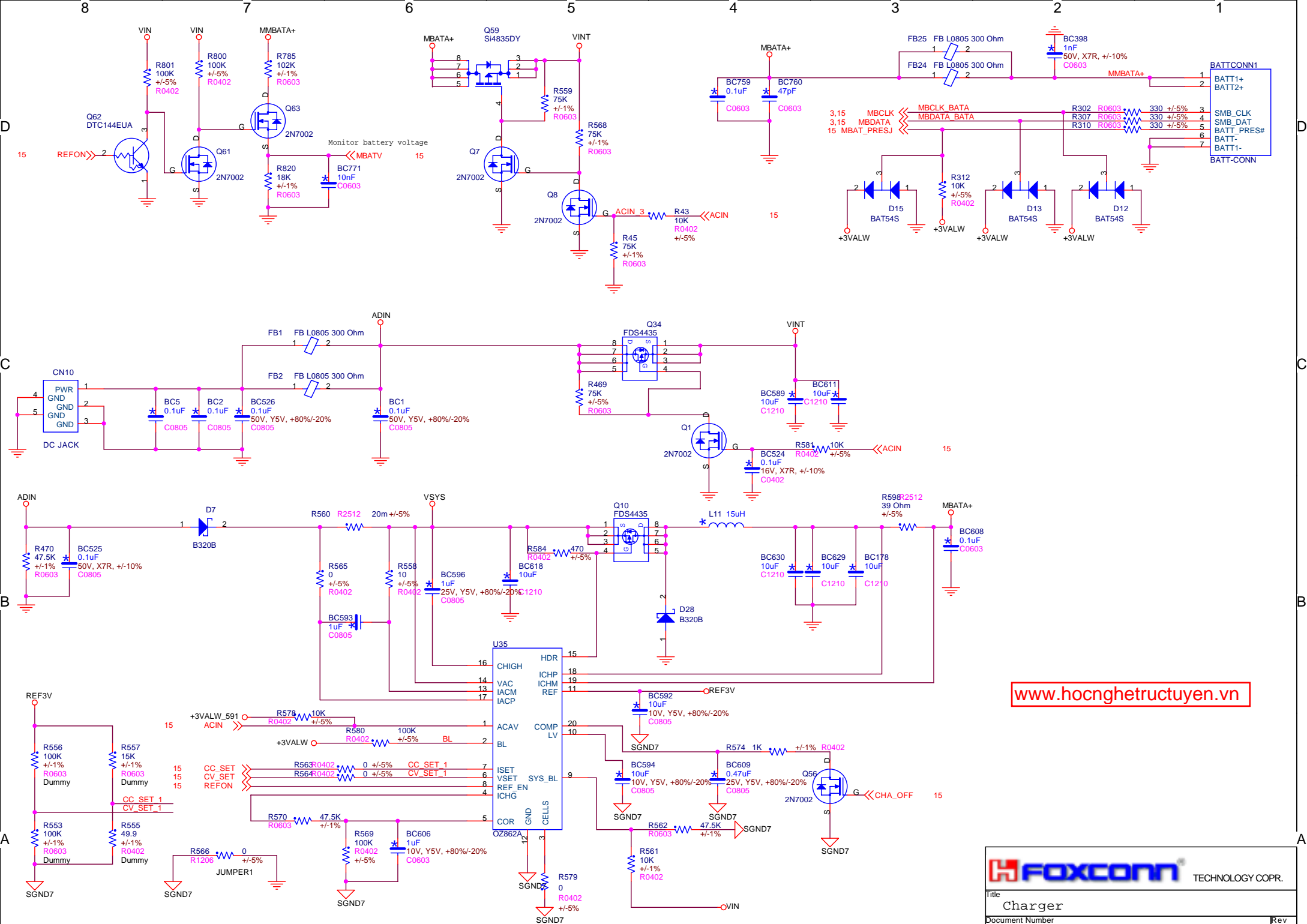
TON=open: 300KHz  
TON=GND: 600KHz

FB=AVdd: 1.8V Output  
FB=GND: 2.5V output

$$\begin{aligned} V_{ilim}(\min) &= 10 * I_{outmax} * (1 - LIR/2) * R_{dsonlow25c} * 1.25 \\ &= 10 * 12 * 0.85 * 5 * 1.25 \\ &= 637.5MV \end{aligned}$$

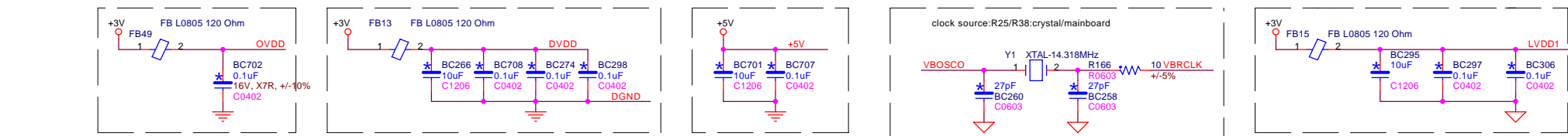
$$\begin{aligned} V_{ilim\_rating} &= 637.5 * 1.15 = 733.125MV \\ R4 &= (2V - 0.3 * V_{ilim\_rating}) / 10 = 178Kohm; \end{aligned}$$





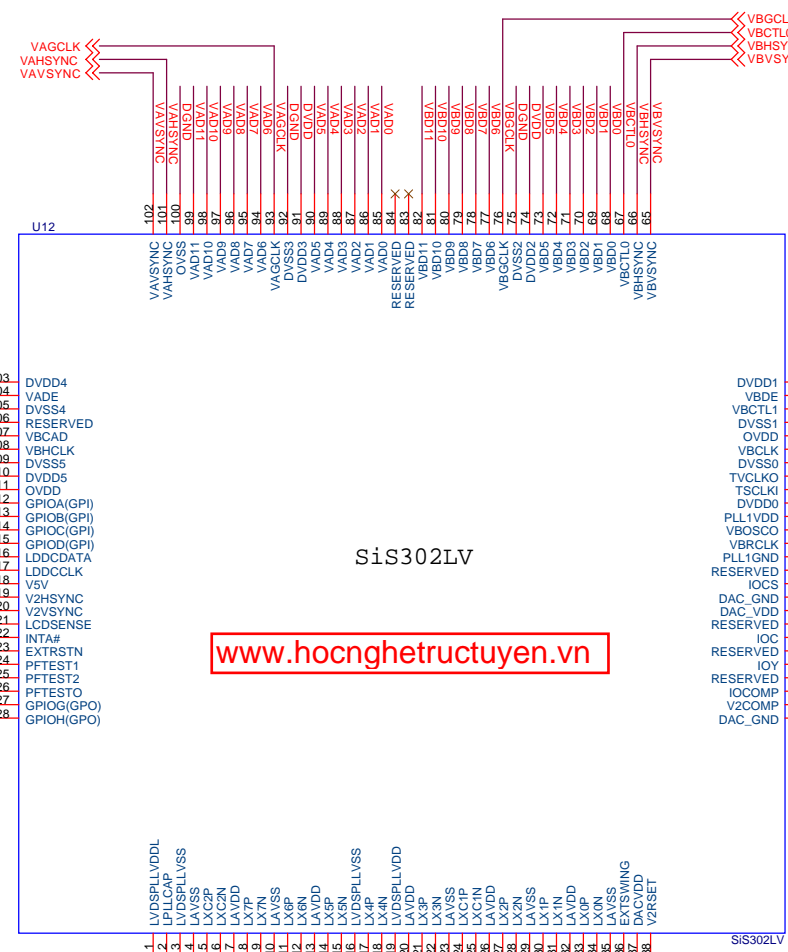
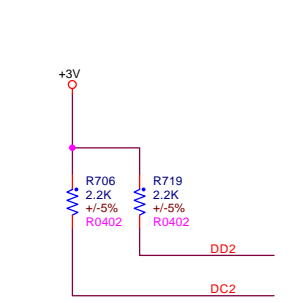
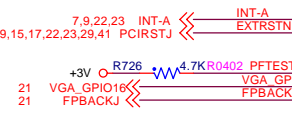
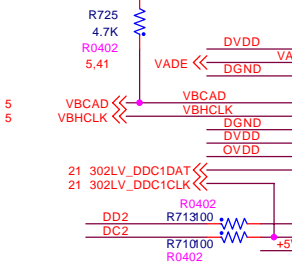
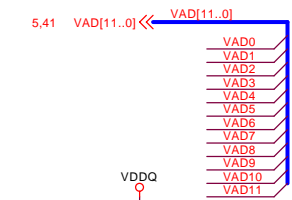
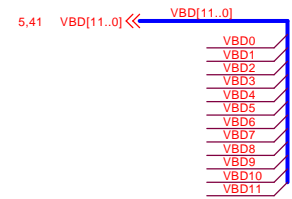
[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

<b>FOXCONN</b> TECHNOLOGY COPR.	
Title <b>Charger</b>	
Document Number <b>661S03</b>	Rev <b>A</b>
Date: Friday, August 13, 2004	Sheet 39 of 50

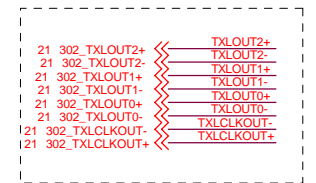
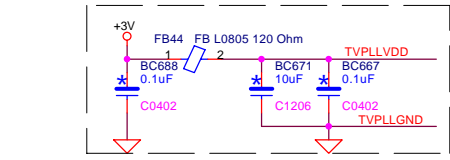
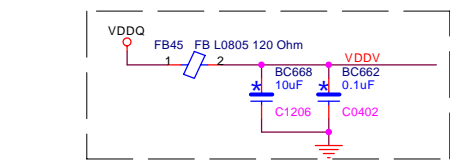
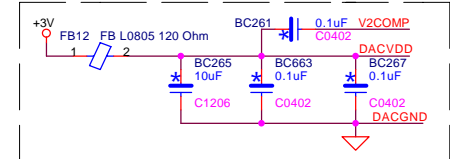
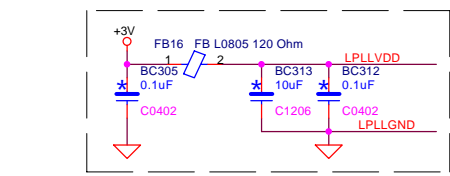


Choose clock source:

Clock Source	Main Board	Crystal
R38	10	NC
R25	NC	10



[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)



LXC2+, LXC2-, LX7+, LX7-, LX6+, LX6-, LX5+, LX5-, LX4+, LX4- are 302LV LVDS dual link signals

301lv/302lv: R63/R59

R694 Demo Valve is 6K lonny 20040601



NOTE:  
 M9CSP32/64 AND M9+CSP32/64  
 AND M10CSP32 ARE 31MM X 31MM PACKAGES  
 M10CSP64 IS 35MM X 31MM PACKAGE

www.hocnghetructuyen.vn

M9 ↔ M10  
 CONNECT DBI\_LO/DBI\_HI  
 TO AGP CONN FOR AGP3.0 ON M10  
 OR TO VDDP FOR AGP2.0 ON M10  
 OR TO VDDP FOR M9

M9 ↔ M10  
 CONNECT AGP\_DET#  
 TO VDDP FOR M9 OR  
 TO 1.5V PU OR TO AGP CONN WITH 1.5V PU FOR M10

THIS DESIGN SHOWS DAC2 CONFIGURED FOR TV OUT  
 DAC2 CAN ALSO BE CONFIGURED FOR SECONDARY CRT  
 MUX LOGIC IS REQUIRED FOR DAC2 AS BOTH TVOUT AND SECONDARY CRT

REMOVE TESTEN PULL DOWN  
 FOR OPTIONAL TEST MODE ENABLE  
 REFER TO DATA BOOK  
 FOR JTAG AND SCAN SIGNAL SOURCES

M9 ↔ M10  
 PULL-UP TEST\_YCLK/MCLK  
 TO BE COMPATIBLE WITH M9

M9 ↔ M10  
 CONNECT RSTB\_MSK TO GND OR TO AGP CONN FOR M10  
 CONNECT RSTB\_MSK TO GND FOR M9

FOR ALL GPIO AND ZV\_DATA SIGNALS  
 THAT ARE ALSO CONFIGURATION STRAPS  
 ENSURE CORRECT PULL UP/DOWN ARE MAINTAINED  
 DURING POWER ON RESET CONFIGURATION  
 SEE DATA BOOK

DVO IS CONFIGURED FOR ZVPORT (DVOMODE = GND)  
 ON THIS DESIGN  
 IT CAN ALSO BE DDR EXTERNAL TMDs (DVOMODE = 1.8V)  
 SEE DATA BOOK

UNUSED GPIO, DDC OR ZV\_LCDDATA CAN BE  
 USED FOR PANEL OR MEMORY ID  
 IF DVO IS CONFIGURED FOR 12 BIT EXT DDR TMDs  
 ANY UNUSED LCDDATA PULLUP STRAPPING  
 MUST BE TO +1.8V

M9 ↔ M10  
 CONNECT VREFG TO VDDC FOR M9  
 CONNECT VREFG TO VOLTAGE DIVIDER FOR M10

www.hocnghetructuyen.vn

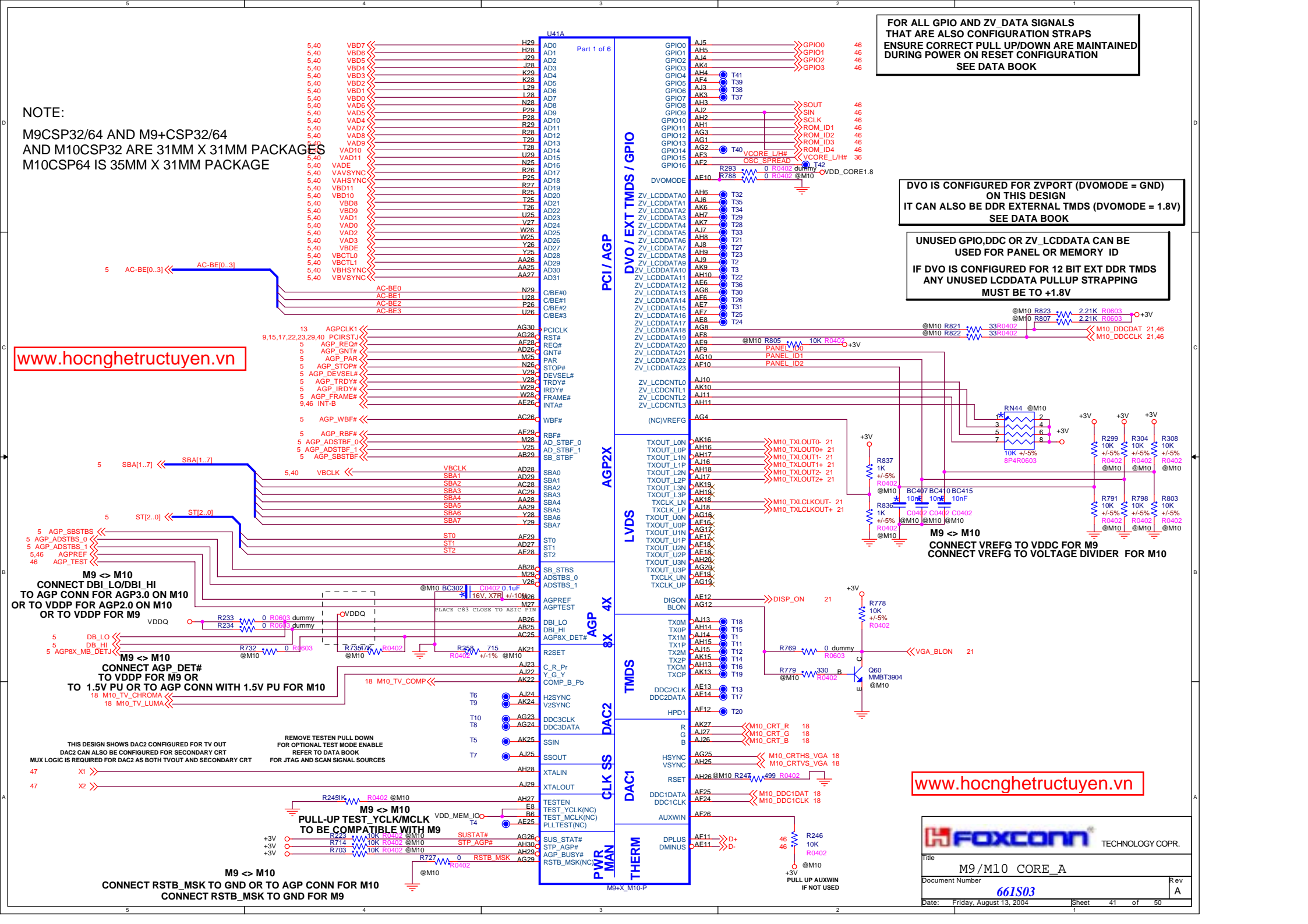
FOXCONN TECHNOLOGY COPR.

Title  
 M9/M10 CORE A

Document Number  
 661S03

Date: Friday, August 13, 2004 Sheet 41 of 50

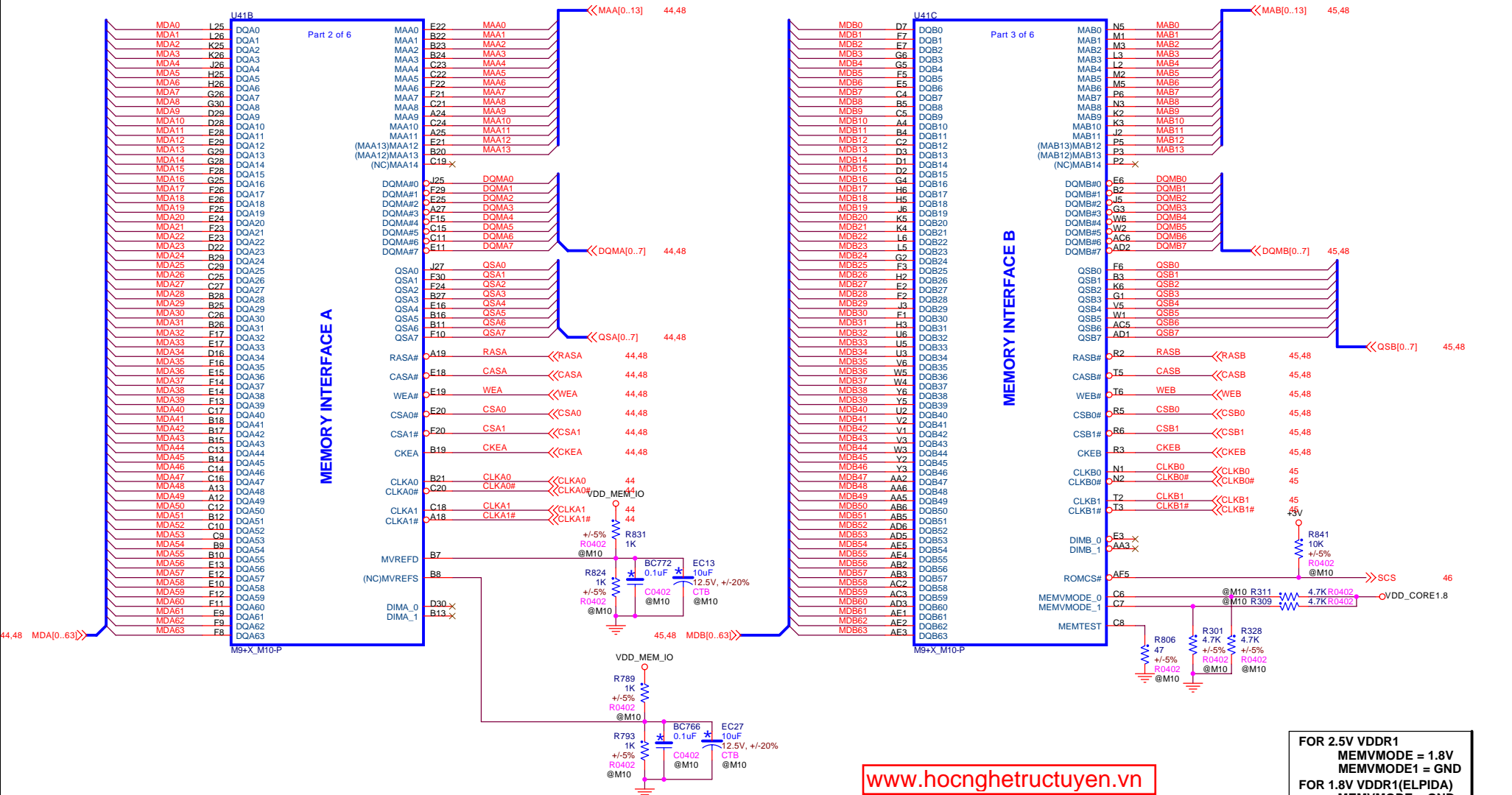
Rev  
 A



M9 <-> M10  
 EXTERNAL MEMORY CAN BE CONNECTED TO CHANNEL B ON M9CSP32 AND M9+CSP32  
 INTERNAL MEMORY IS CONNECTED TO CHANNEL A WITH SIGNALS AVAILABLE FOR TESTING ONLY ON M9CSP32 AND M9+CSP32

ALL CHANNEL A AND B MEMORY SIGNALS ARE GROUNDS ON M9CSP64, M9+CSP64 AND M10CSP64  
 SO ENSURE THEY ARE NOT CONNECTED TO GROUND ON THE BOARD IF M10CSP32 OR M9+CSP32 IS AN OPTION

NO EXTERNAL MEMORY CAN BE CONNECTED TO CHANNEL A OR B ON M10CSP32 OR M10CSP64  
 CHANNEL B MEMORY HAS BYTES 2 AND 3 SWAPPED AND SIGNALS ARE AVAILABLE FOR TESTING ONLY ON M10CSP32



MVREF DIVIDER RESISTORS AND DECOUPLING CAPS MUST BE PLACED AS CLOSE AS POSSIBLE TO THE ASIC MVREF BALLS

IT IS IMPORTANT TO HAVE NO MEMORY SIGNAL TRACE STUBS FROM THE UNUSED CHANNELS

[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

FOR 2.5V VDDR1  
 MEMVMODE = 1.8V  
 MEMVMODE1 = GND  
 FOR 1.8V VDDR1(ELPIDA)  
 MEMVMODE = GND  
 MEMVMODE1 = 1.8V  
 SEE DESIGN GUIDE

**FOXCONN** TECHNOLOGY COPR.

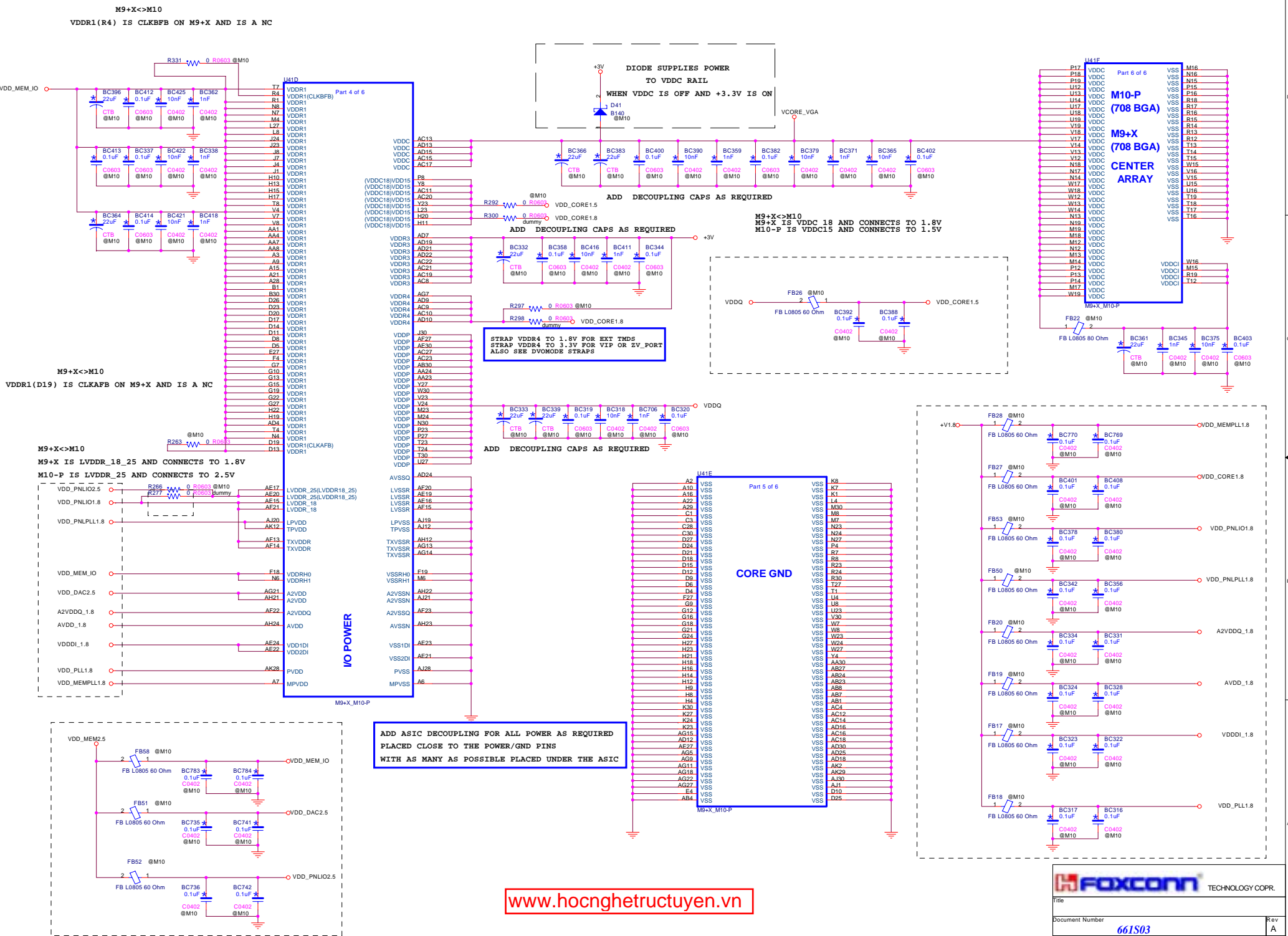
Title: M9/M10-2

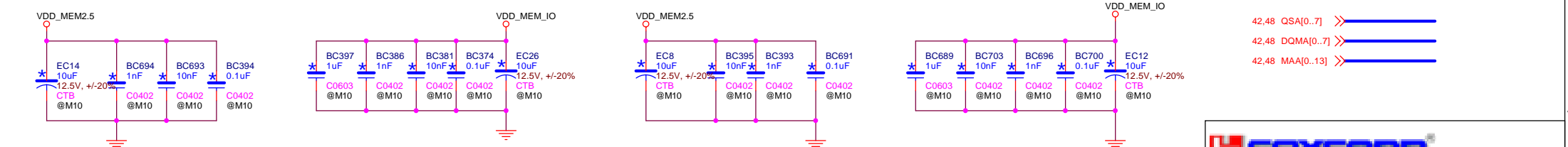
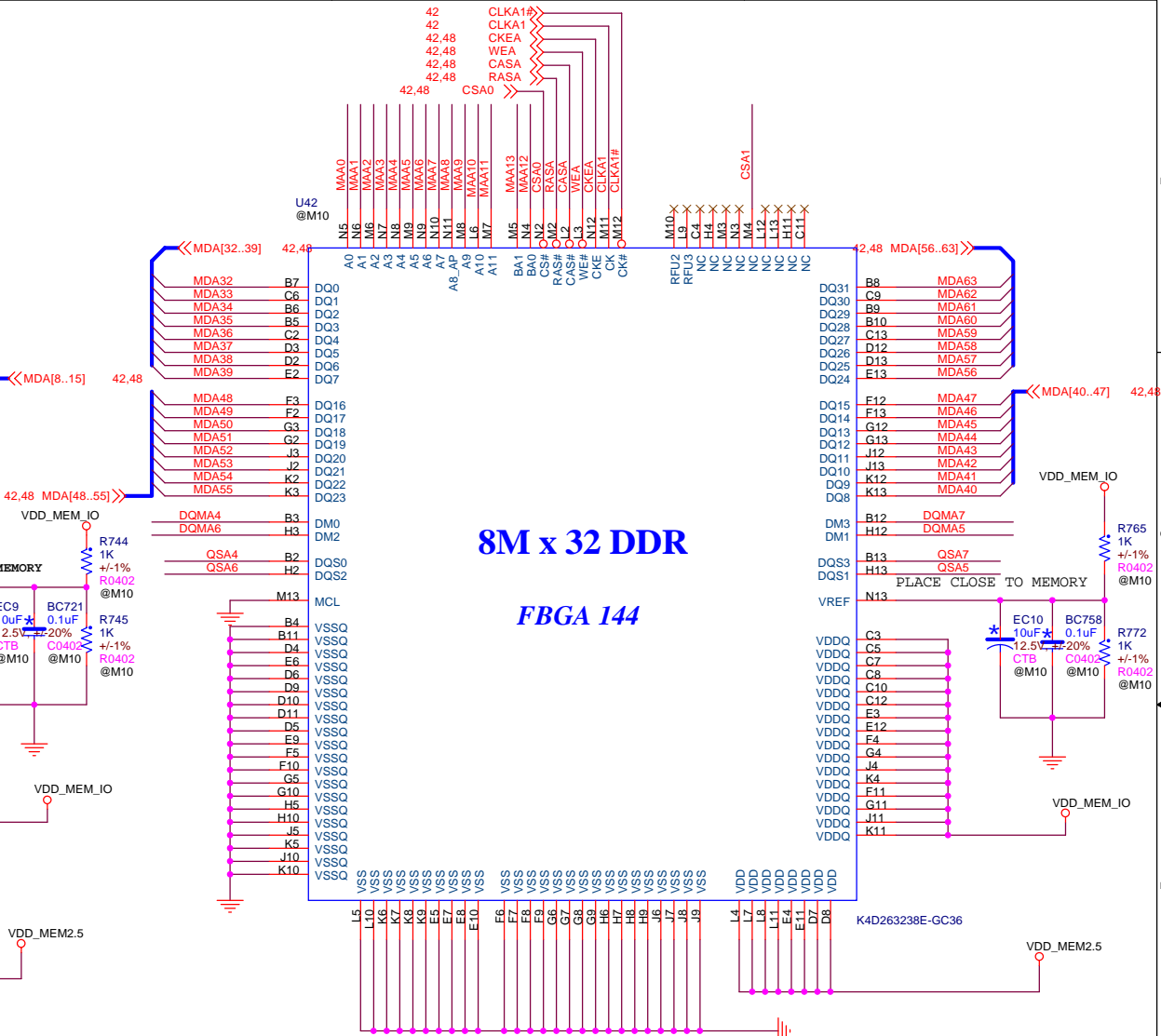
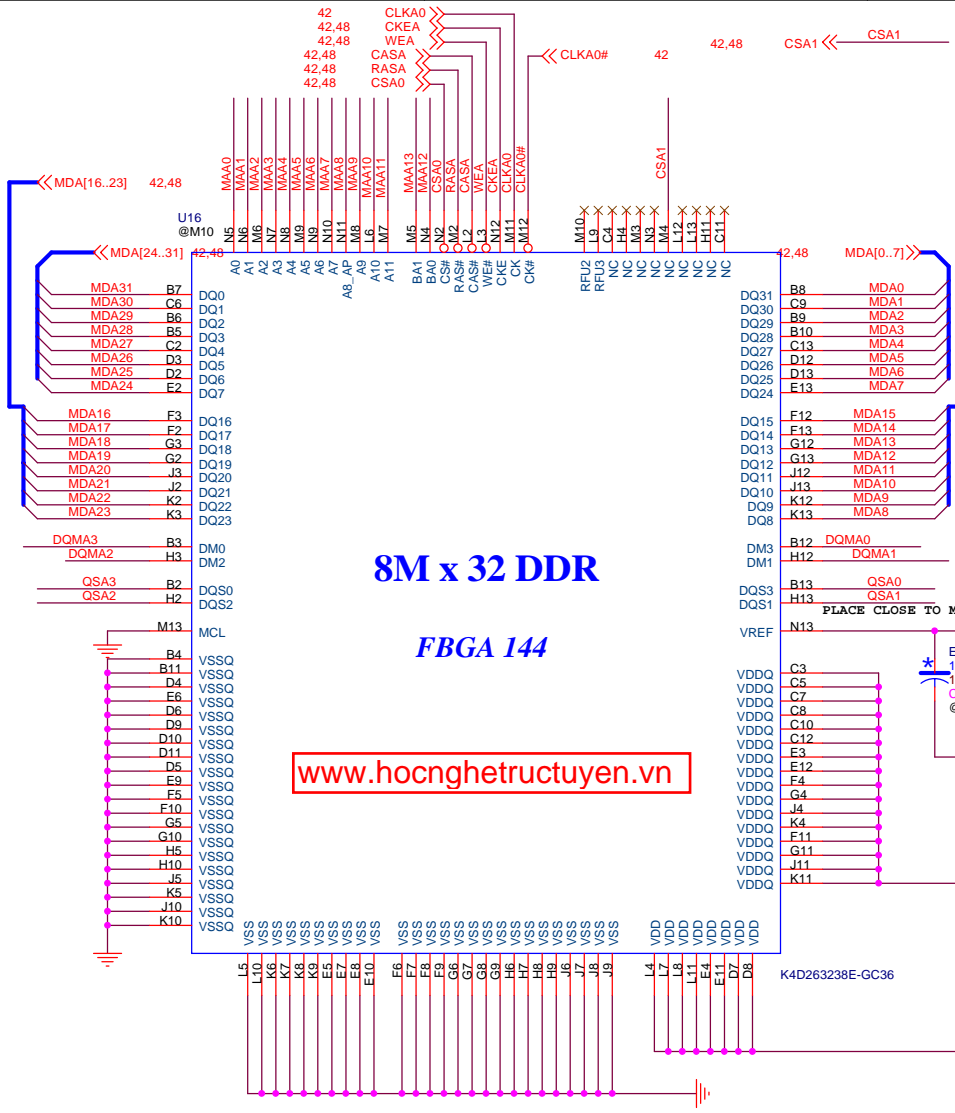
Document Number: 661S04

Date: Friday, August 13, 2004

Sheet: 42 of 50

Rev: A





**FOXCONN** TECHNOLOGY CORP.

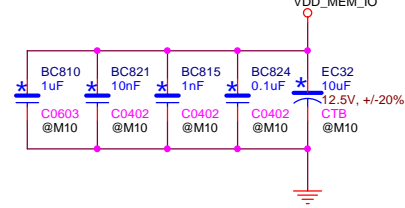
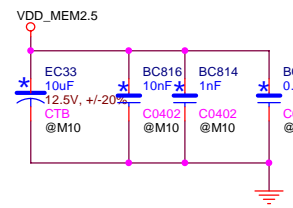
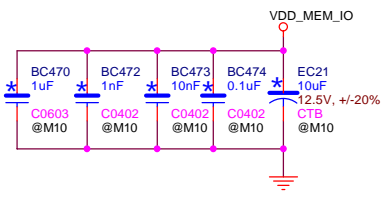
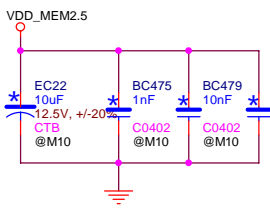
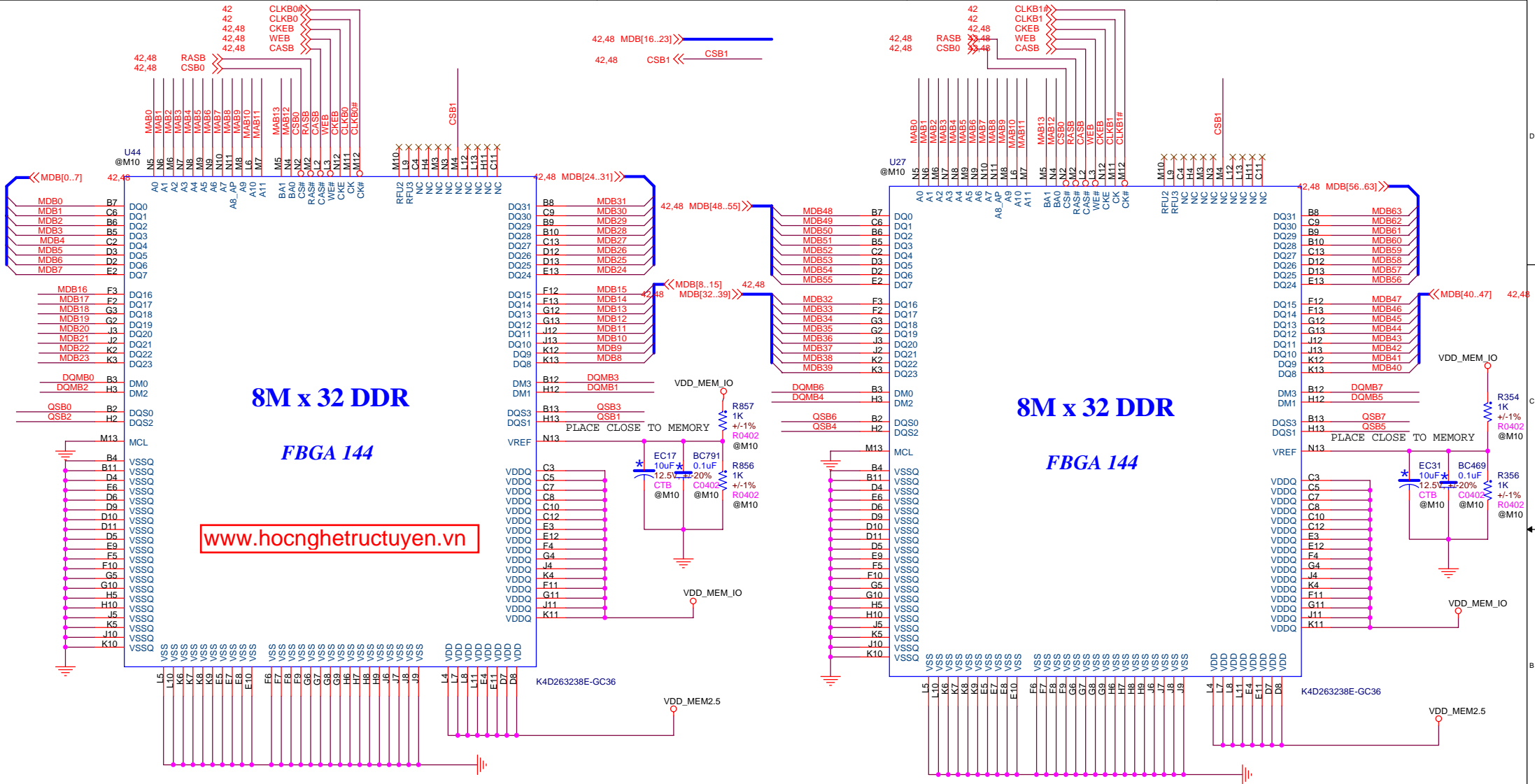
Title

Document Number **661S03**

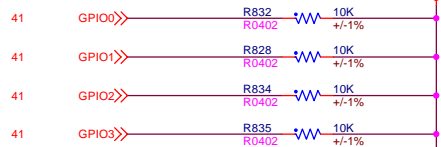
Date: Friday, August 13, 2004

Sheet 44 of 50

Rev **A**



OTHER OPTION STRAPS ARE AVAILABLE IF REQUIRED  
SEE DESIGN GUIDE

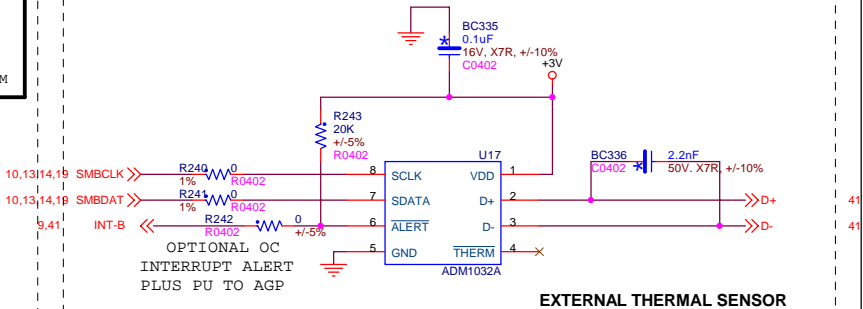
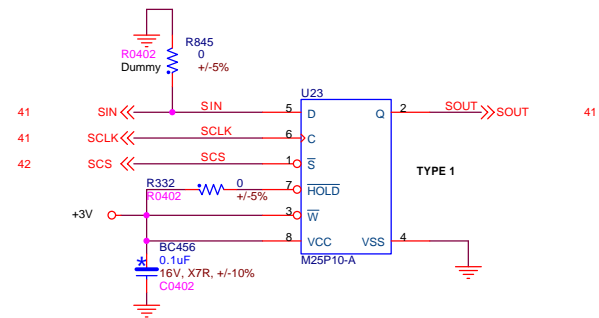


GPIO1	GPIO0	AGP 1X CLOCK FEEDBACK PHASE ADJUST WITH RESPECT TO REFCLK
DNI	DNI	REFCLK SLIGHTLY EARLIER THAN FEEDBACK (DEFAULT)
GPIO3	GPIO2	CLOCK PHASE ADJUSTMENT BETWEEN X1 AND X2 CLK
DNI	DNI	0 TAP DELAY (DEFAULT)



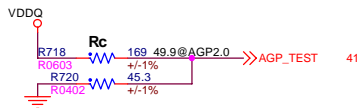
ROM_ID4	ROM_ID3	ROM_ID2	ROM_ID1	ROM ID CONFIG
DNI	DNI	DNI	DNI	NO ROM (DEFAULT)
10K	DNI	DNI	10K	SERIAL AT25F1024 (ATMEL) ROM
10K	DNI	DNI	DNI	SERIAL AT2545DB011 (ATMEL) ROM
10K	DNI	10K	10K	SERIAL M25P10 (ST) ROM
10K	10K	DNI	DNI	SERIAL M25P05 (ST) ROM
10K	DNI	DNI	10K	SERIAL SST45LF010 (SST) ROM
10K	10K	10K	DNI	SERIAL SST25VF010 (SST) ROM
10K	10K	10K	10K	SERIAL NX25F011B (NEXFLASH) ROM

OPTIONAL SERIAL FLASH EEPROM  
FOR VIDEO BIOS OUTSIDE SYSTEM BIOS



AGP\_TEST RESISTOR SELECTION

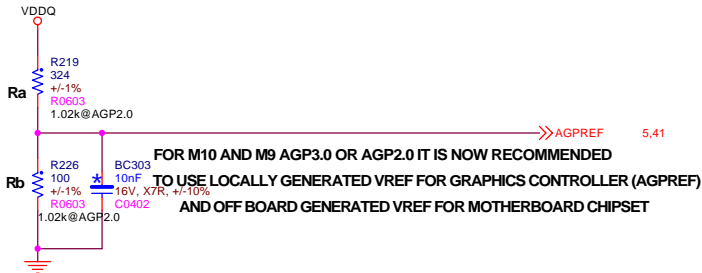
AGP MODE	Rc
AGP 2.0 (4X)	499R 1%
AGP 3.0 (8X)	166R 1%



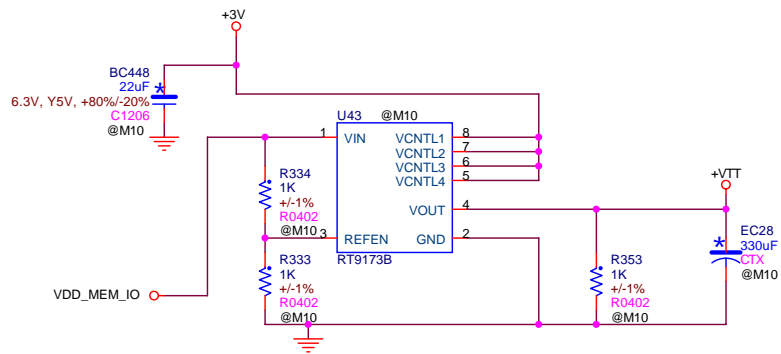
M9 <> M10  
ON M9 AGPTEST IS PULLED DOWN  
ON M9+ AND M10 AGPTEST IS PULLED UP TO VDDP

AGPREFVREFGC RESISTOR SELECTION

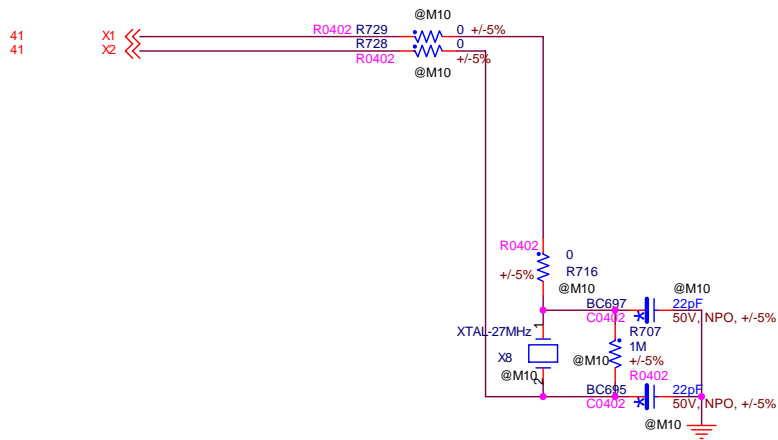
AGP MODE	Ra	Rb
AGP 2.0 (4X) .75V	1.02K 1%	1.02K 1%
AGP 3.0 (8X) .35V	324R 1%	100R 1%

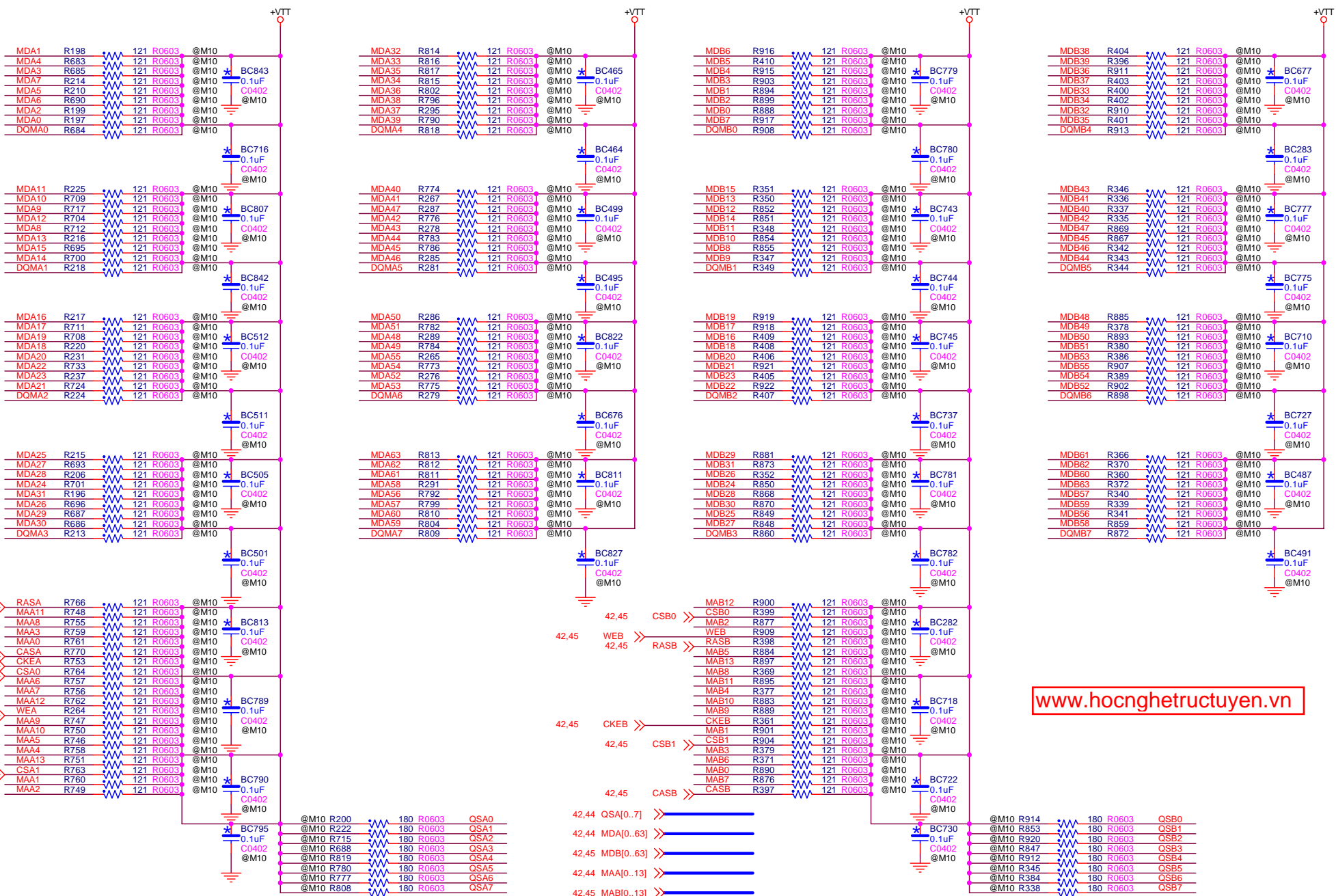


FOR M10 AND M9 AGP3.0 OR AGP2.0 IT IS NOW RECOMMENDED  
TO USE LOCALLY GENERATED VREF FOR GRAPHICS CONTROLLER (AGPREF)  
AND OFF BOARD GENERATED VREF FOR MOTHERBOARD CHIPSET



www.hocnghetructuyen.vn





[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

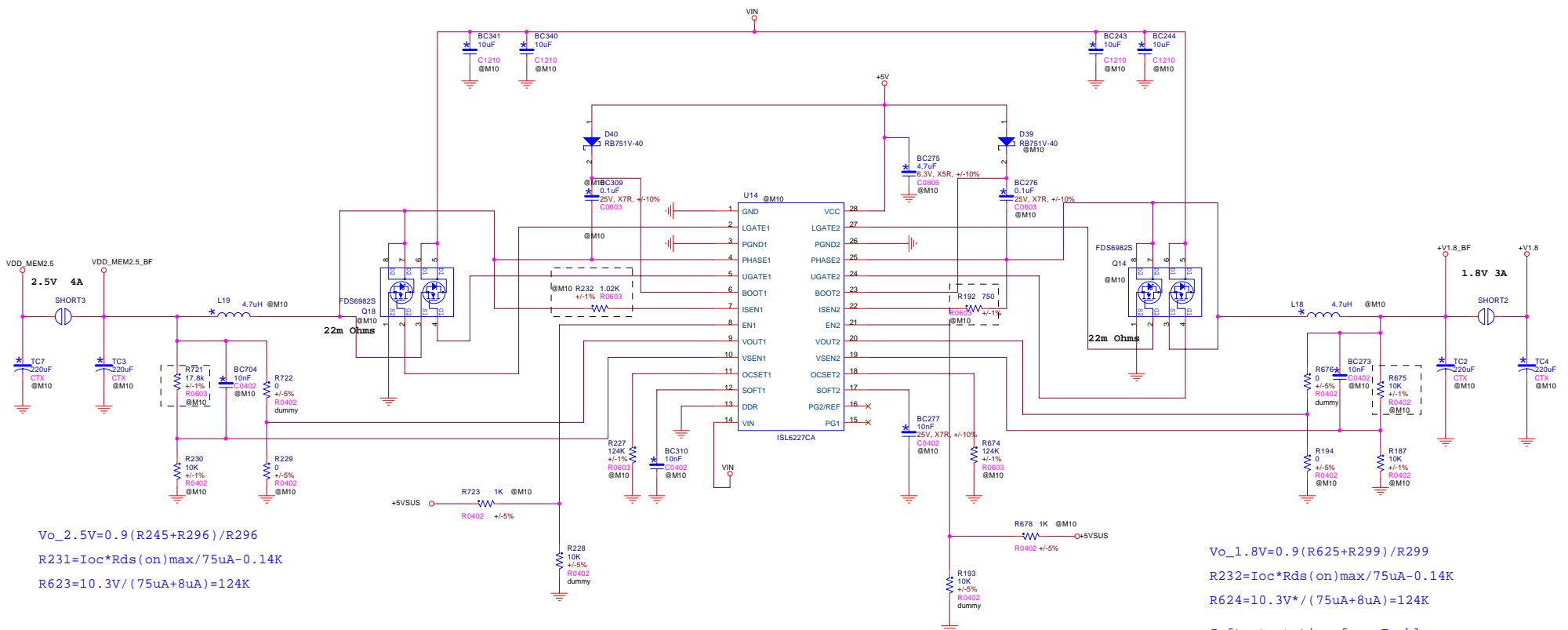
**FOXCONN** TECHNOLOGY CO., P.R.

Title

Document Number **661S03** Rev **A**

Date: Friday, August 13, 2004 Sheet 48 of 50





$$V_{o\_2.5V} = 0.9 (R_{245} + R_{296}) / R_{296}$$

$$R_{231} = I_{oc} * R_{ds(on)max} / 75\mu A - 0.14K$$

$$R_{623} = 10.3V / (75\mu A + 8\mu A) = 124K$$

$$V_{o\_1.8V} = 0.9 (R_{625} + R_{299}) / R_{299}$$

$$R_{232} = I_{oc} * R_{ds(on)max} / 75\mu A - 0.14K$$

$$R_{624} = 10.3V * (75\mu A + 8\mu A) = 124K$$

Soft start time from Enable to Power good indicate  

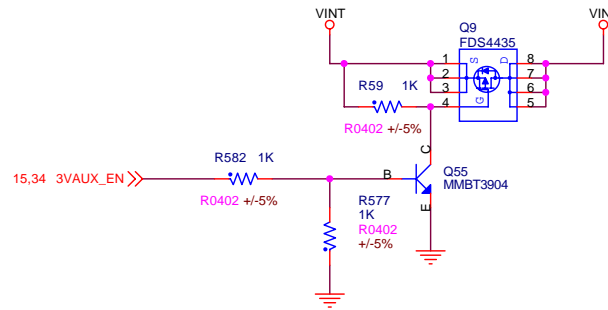
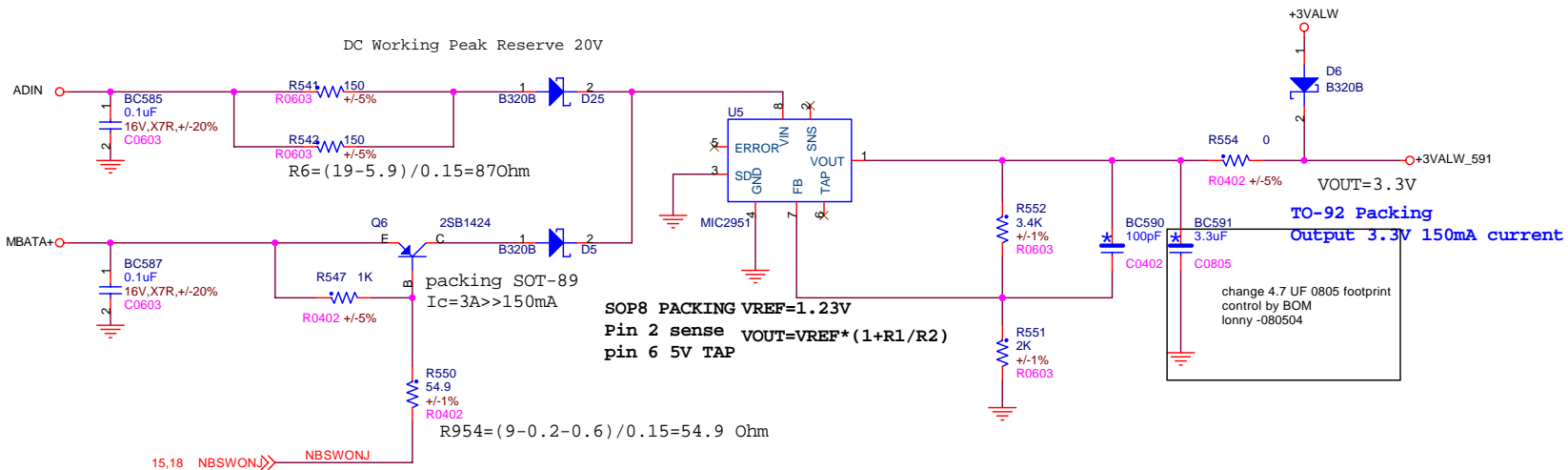
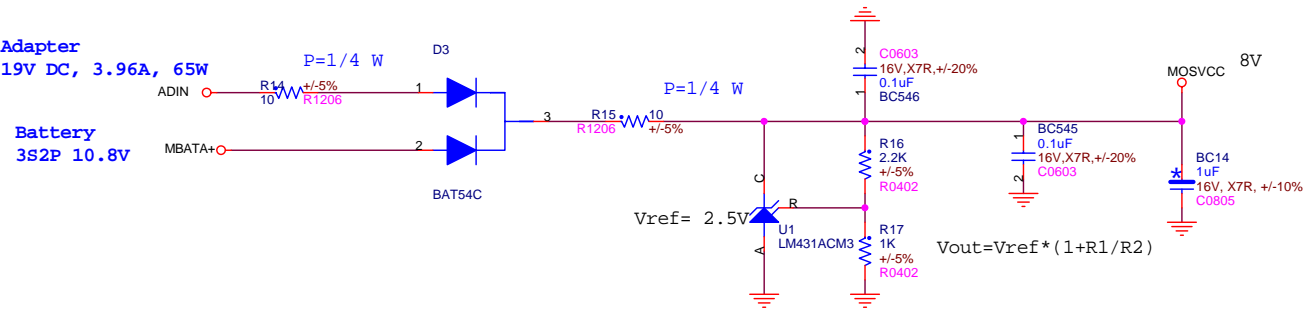
$$T_{soft} = 1.5V * C_{soft} / 5\mu A = 3ms$$

DDR	EN1	EN2	PIN14	Phase
0	1	1	4.2V < V <sub>IN</sub> < 24V	180 degree

[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

Adapter  
19V DC, 3.96A, 65W

Battery  
3S2P 10.8V



update sch VINT for save power only battery mode lonny update  
2004/07/17

[www.hocnghetructuyen.vn](http://www.hocnghetructuyen.vn)

**FOXCONN** TECHNOLOGY COPR.

Title: **SAVE POWER**

Document Number: **661S03**

Date: Friday, August 13, 2004

Sheet 50 of 50

Rev A