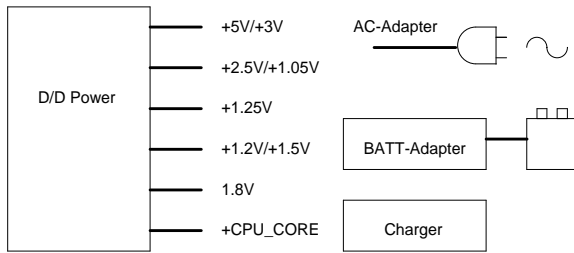
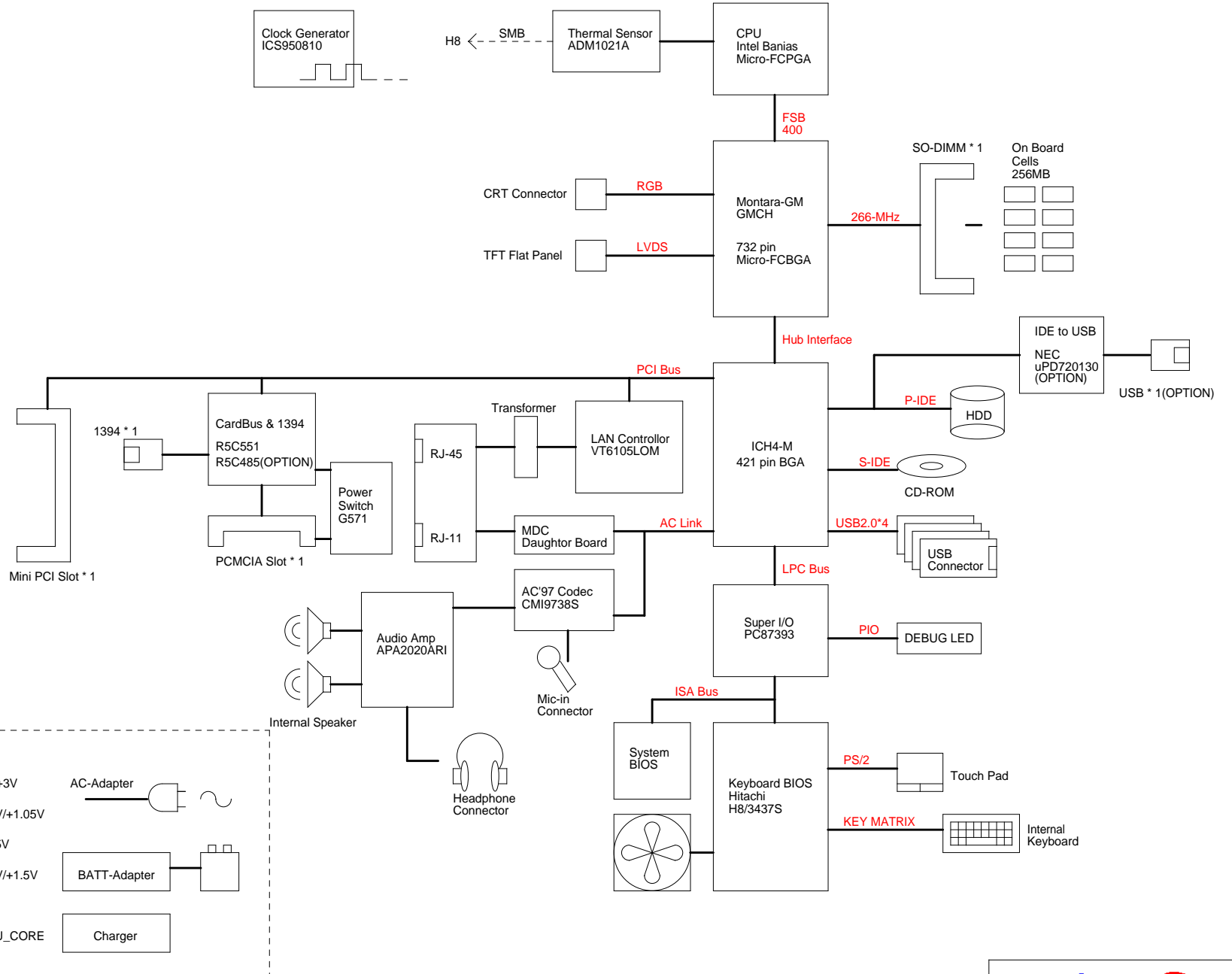


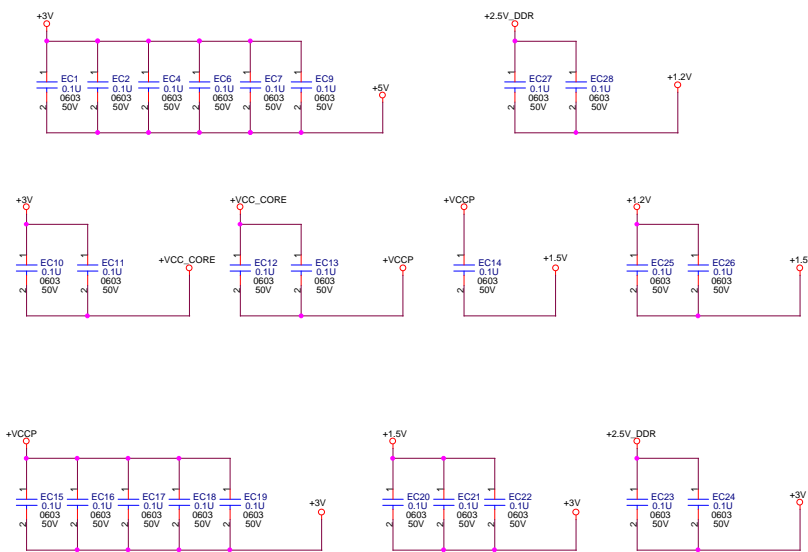
8081 MB R01

Project Code : G072
Product Code : 6785

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- PAGE02 Mounting Hole
- PAGE03 Banais
- PAGE04 Clock Generator
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- PAGE27 3V & 5V(LTC3728L)
- PAGE28 CPU_CORE(MAXIM1907)



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Block Diagram	
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Date: Wednesday, June 11, 2003	Sheet 1 of 28

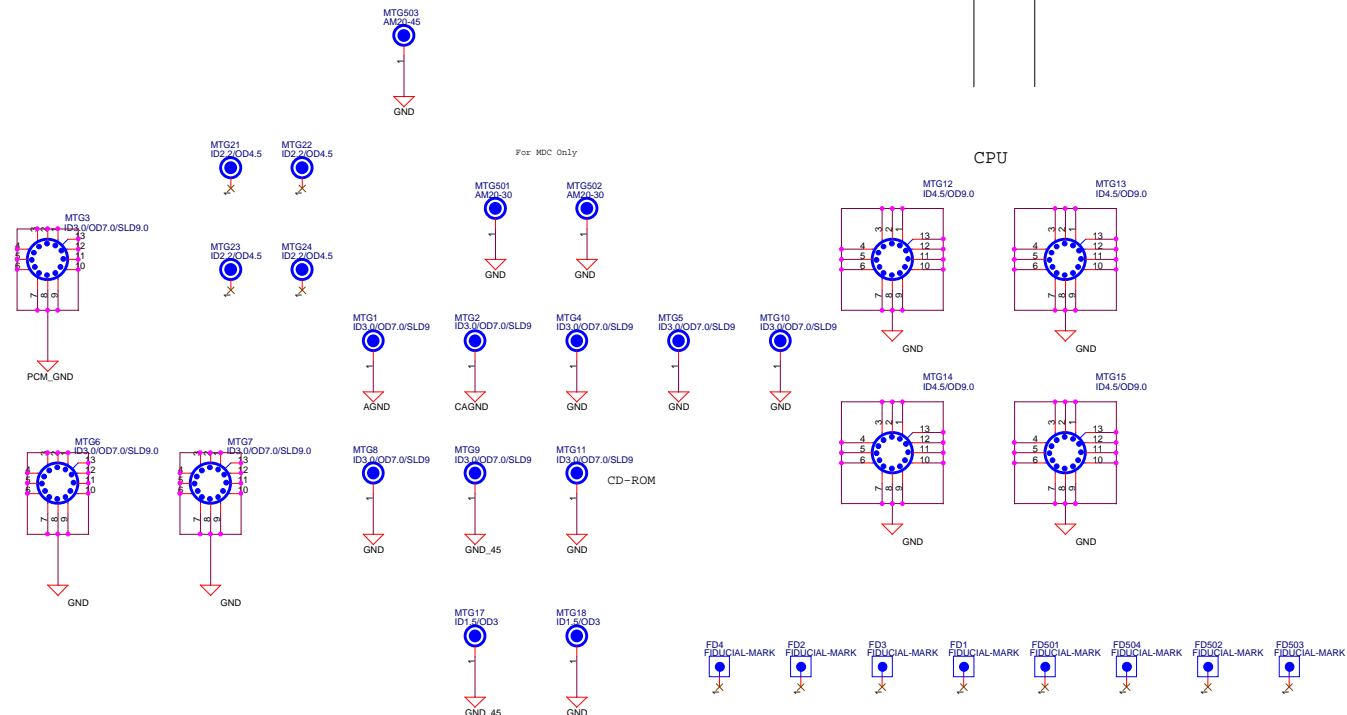


VT6105LOM(LAN)
 IDSEL: AD18
 PCI REQ1#
 PCI GNT1#
 PCI INTE#

Mini PCI
 IDSEL: AD17
 PCI REQ3#
 PCI GNT3#
 PCI INTD# INTF#

R5C551
 IDSEL: AD20
 PCI REQ2#
 PCI GNT2#
 PCI INTB# INTG#

REV	Change detail	DATE	ECR No.
R00	Initial release (base on PUMA)	2003/05/02	
R01	1.Change PR4 ,PR29 and PR45 to 470 ohm for SUSB# signal quality. 2.LAN signal add fuse to protect LAN transformer. 3.Modify U533 control signal(SUSCH# and 2 * 2N7002) for leakage current. 4.Remove R98 for leakage current and change pull high to +3V. 5.Change R202 and R217(M/B ID) pull high to +VDD3. 6.Change Q24 pin2 pull high to +EXT3V. 7.Change R777 and R778 to 6.8K for CD ROM audio noise. 8.Inverter input voltage add VMAIN option for future use. 9.Change Q517 to 2N7002 and rename Q33 for LED flash issue. 10.Change U522 power to +AVDDAD, C753 to AGND, R736 to AGND. 11.Change J10(MIC) pin6 to CAGND. 12.Reserve band pass tuning capacitor.(Page 13) 13.Add a resistor on CD LED# signal to prevent signal O.D. 14.Delete M/B to charger BD connector USB signal reserver resistors and connector original pin to GND. 15.Add a resistor(1M) and change R505 to 47K ohm and rename R507 for divided DVMAIN to tuen on LCDVCC MOS.(Reserved) 16.Reserve a regulator for audio +5V input. 17.Modify back light circuit. 18.Re-assign M/B to Charger BD pin. 19.Change R766 pull high to +VA. 20.Add R505 between CLK_DDR3/CLK_DDR3# and R686 between CLK_DDR4/CLK_DDR4#	2003/05/26	



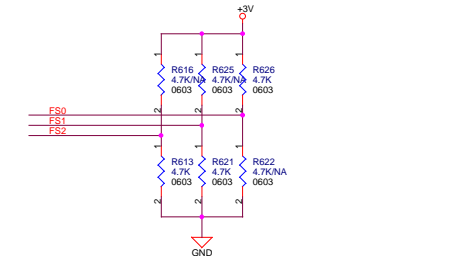
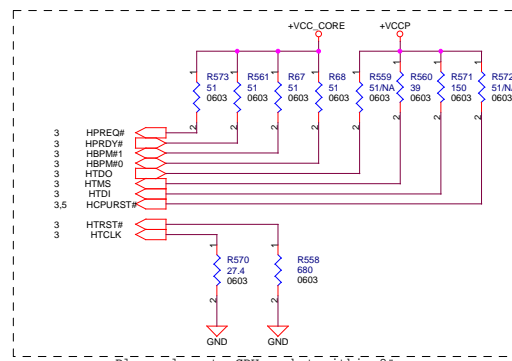
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Mounting Hole

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VID	VCC-Core
5 4 3 2 1 0	1.708
0 0 0 0 0 1	1.692
0 0 0 0 1 0	1.676
0 0 0 0 1 1	1.660
0 0 0 1 0 0	1.644
0 0 0 1 0 1	1.628
0 0 0 1 1 0	1.612
0 0 0 1 1 1	1.596
0 0 1 0 0 0	1.580
0 0 1 0 0 1	1.564
0 0 1 0 1 0	1.548
0 0 1 0 1 1	1.532
0 0 1 1 0 0	1.516
0 0 1 1 0 1	1.500
0 0 1 1 1 0	1.484
0 0 1 1 1 1	1.468
0 1 0 0 0 0	1.452
0 1 0 0 0 1	1.436
0 1 0 0 1 0	1.420
0 1 0 0 1 1	1.404
0 1 0 1 0 0	1.388
0 1 0 1 0 1	1.372
0 1 0 1 1 0	1.356
0 1 0 1 1 1	1.340
0 1 1 0 0 0	1.324
0 1 1 0 0 1	1.308
0 1 1 0 1 0	1.292
0 1 1 0 1 1	1.276
0 1 1 1 0 0	1.260
0 1 1 1 0 1	1.244
0 1 1 1 1 0	1.228
0 1 1 1 1 1	1.212

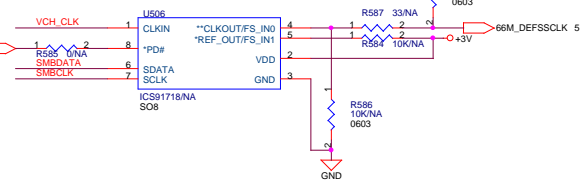
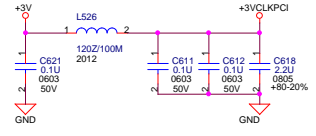
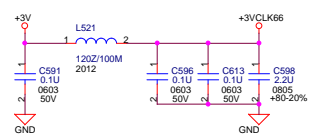
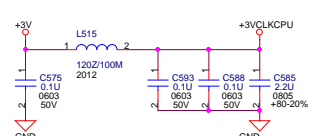
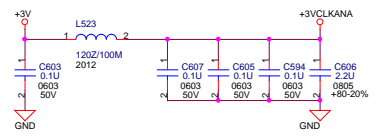
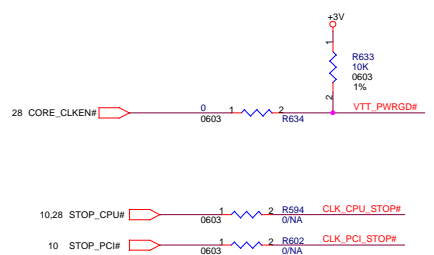
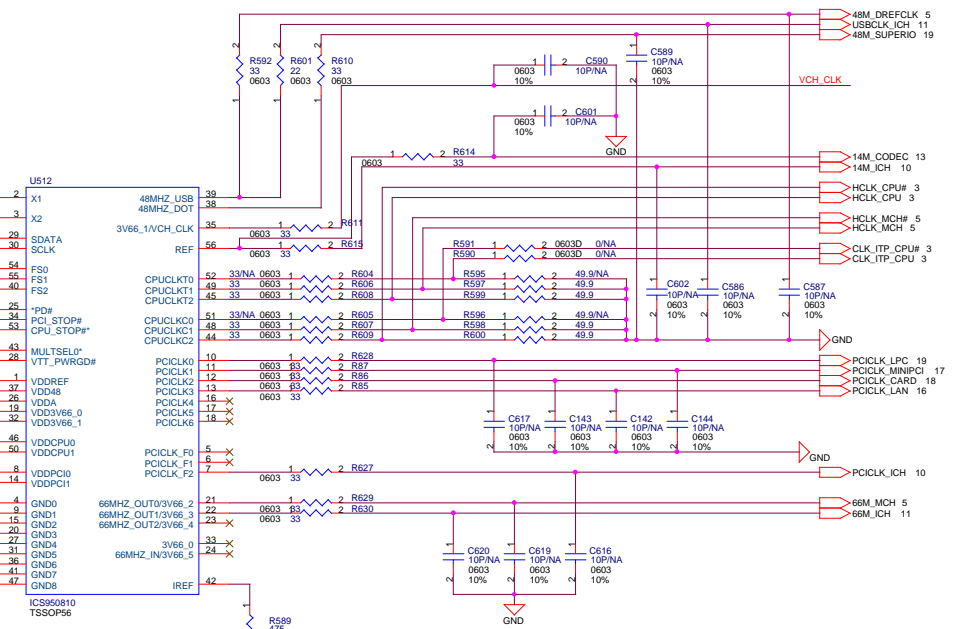
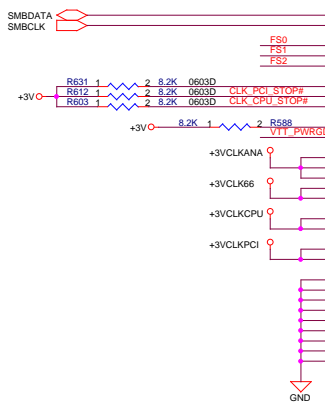
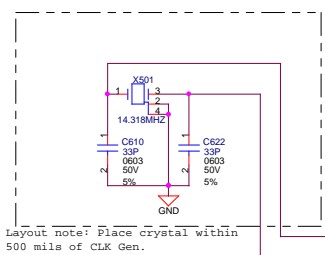
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1 0 0 0 1 0	1.164
1 0 0 0 1 1	1.148
1 0 0 1 0 0	1.132
1 0 0 1 0 1	1.116
1 0 0 1 1 0	1.100
1 0 0 1 1 1	1.084
1 0 1 0 0 0	1.068
1 0 1 0 0 1	1.052
1 0 1 0 1 0	1.036
1 0 1 0 1 1	1.020
1 0 1 1 0 0	1.004
1 0 1 1 0 1	0.988
1 0 1 1 1 0	0.972
1 0 1 1 1 1	0.956
1 1 0 0 0 0	0.940
1 1 0 0 0 1	0.924
1 1 0 0 1 0	0.908
1 1 0 0 1 1	0.892
1 1 0 1 0 0	0.876
1 1 0 1 0 1	0.860
1 1 0 1 1 0	0.844
1 1 0 1 1 1	0.828
1 1 1 0 0 0	0.812
1 1 1 0 0 1	0.796
1 1 1 0 1 0	0.780
1 1 1 0 1 1	0.764
1 1 1 1 0 0	0.748
1 1 1 1 0 1	0.732
1 1 1 1 1 0	0.716
1 1 1 1 1 1	0.700



001 →

FS2	FS1	FS0	CPU	3V66[5:0]	PCI*
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

0:10V
1:3.3V
UNIT: MHz

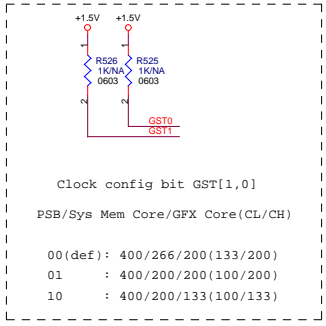
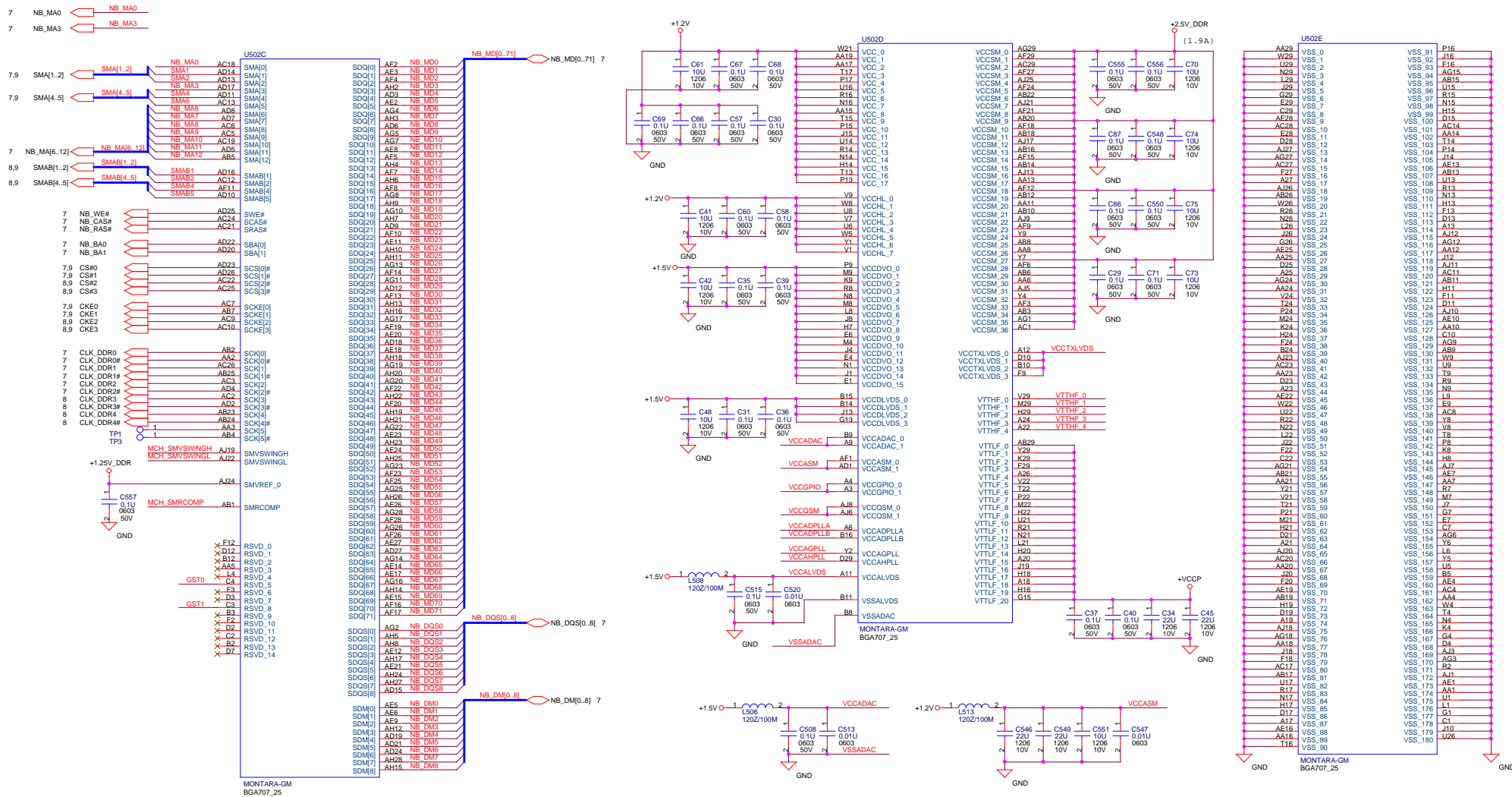


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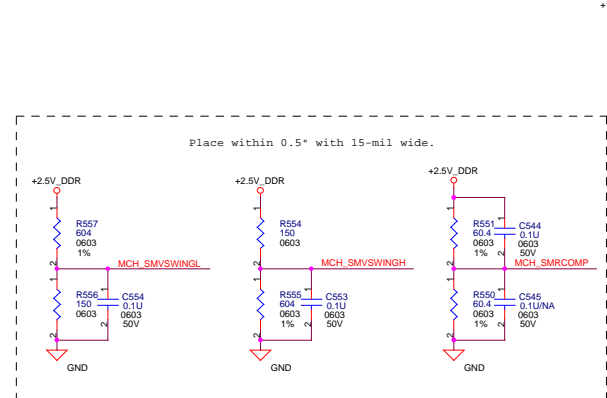
Clock Generator

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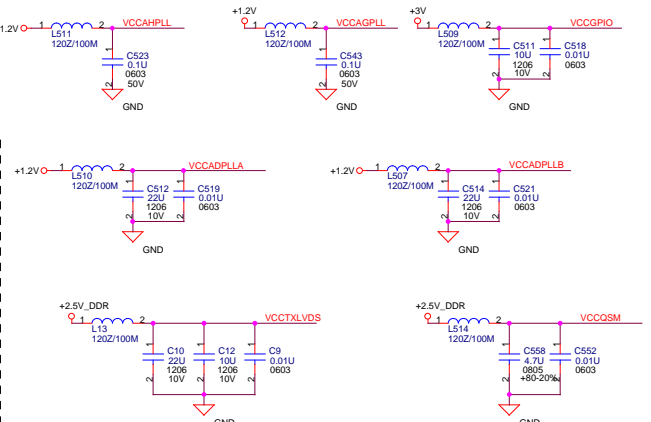
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Clock config bit GST[1,0]
 PSB/Sys Mem Core/GFX Core(CL/CH)
 00 (def) : 400/266/200(133/200)
 01 : 400/200/200(100/200)
 10 : 400/200/133(100/133)



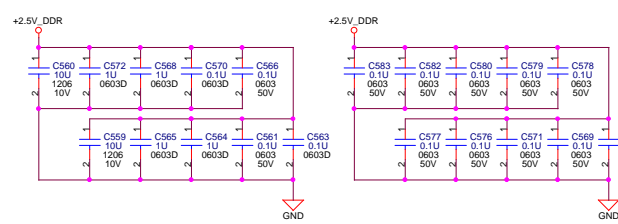
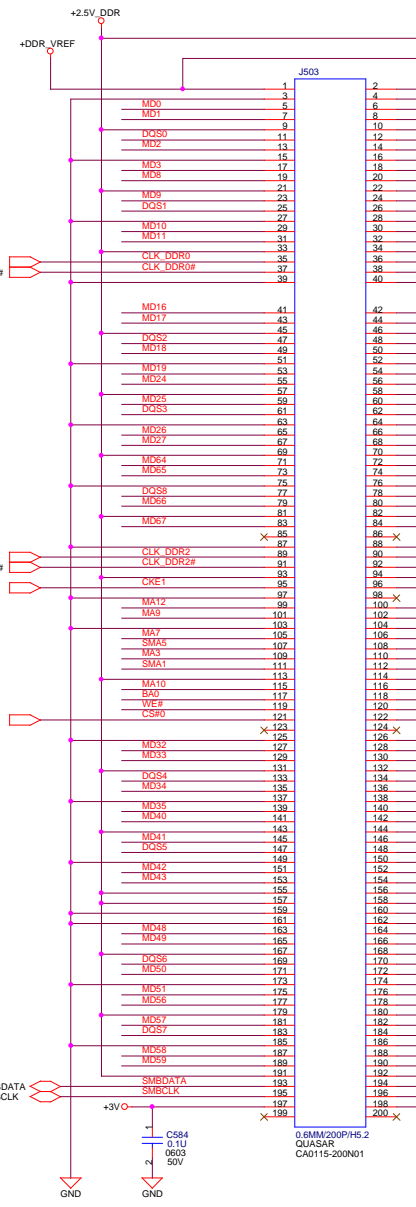
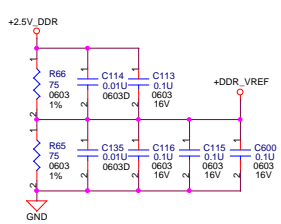
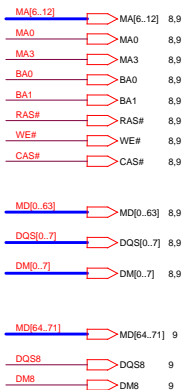
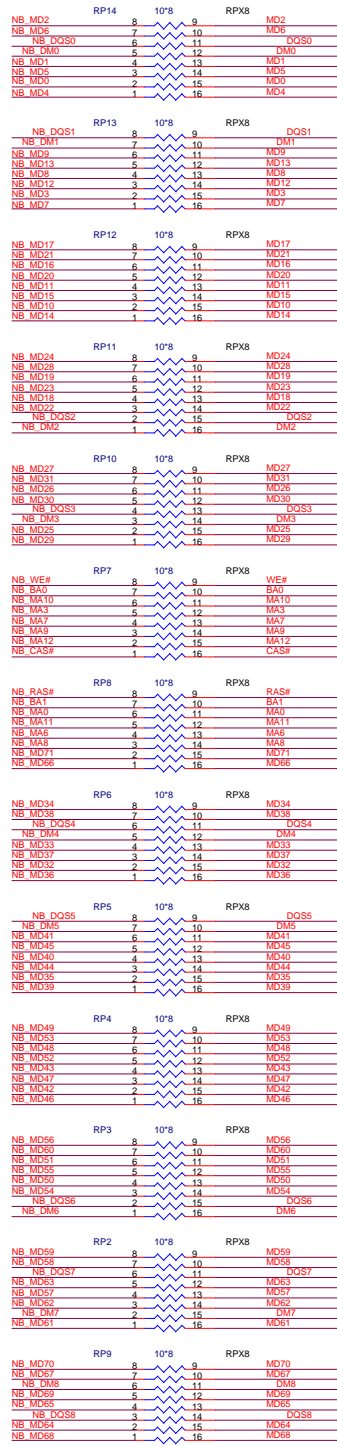
Place within 0.5" with 15-mil wide.



VTTFF_0	C536	2	0.1U
VTTFF_1	C532	2	0.1U
VTTFF_2	C530	2	0.1U
VTTFF_3	C519	2	0.1U
VTTFF_4	C518	2	0.1U

Montara_GM(2)

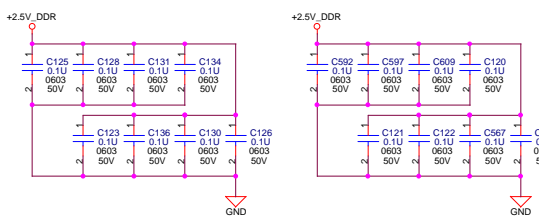
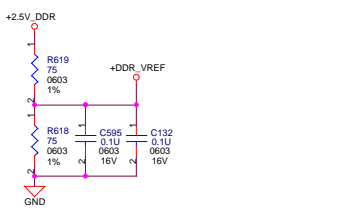
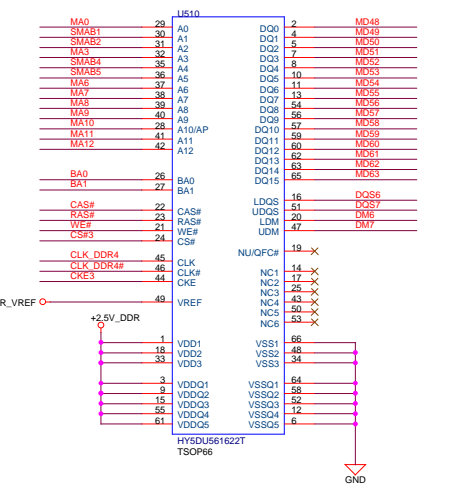
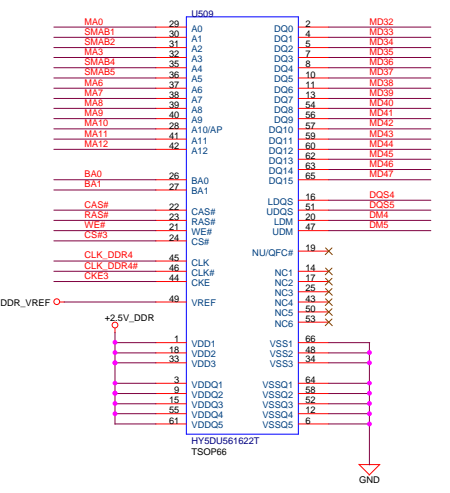
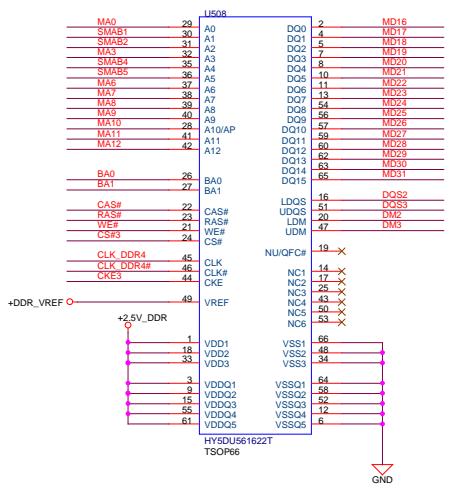
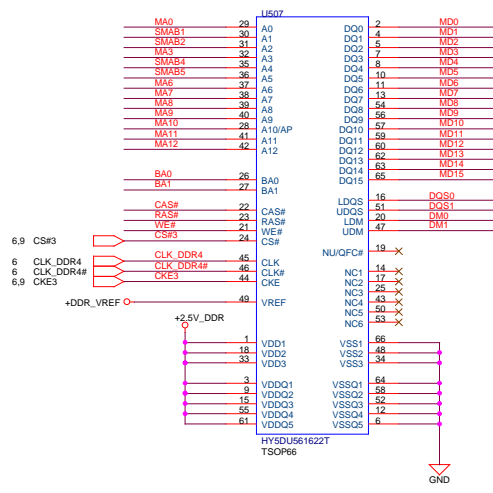
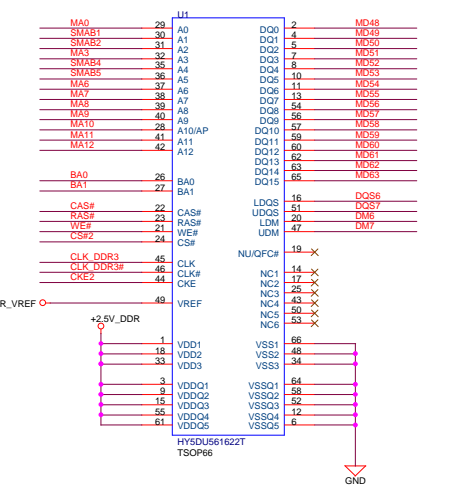
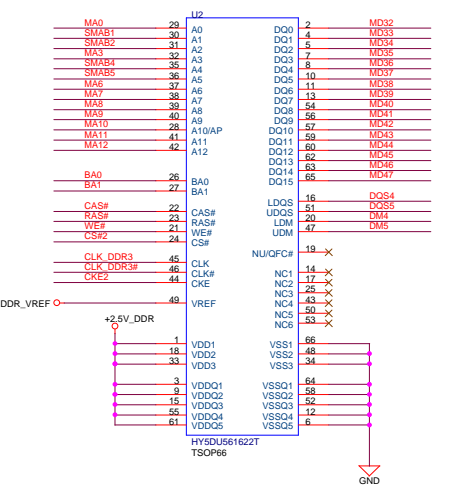
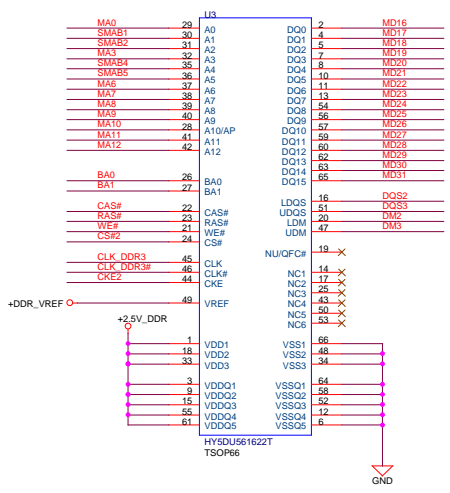
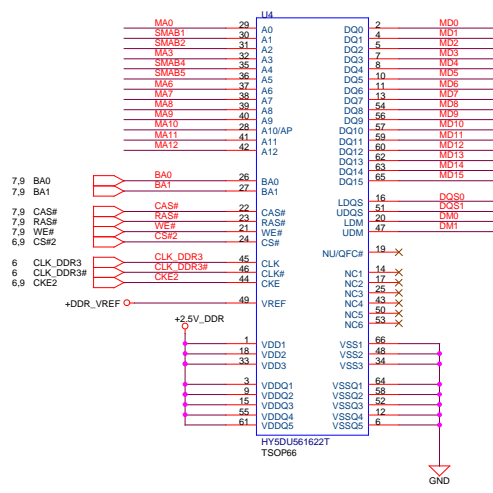
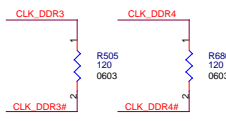
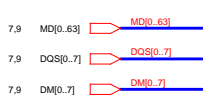
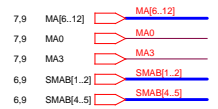
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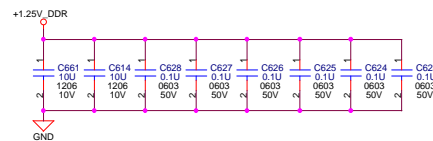
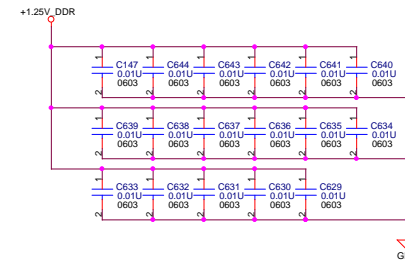
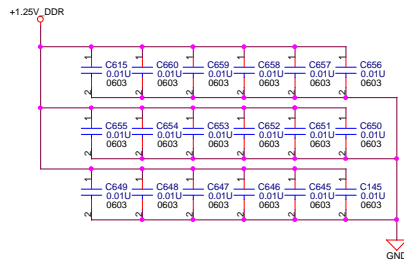
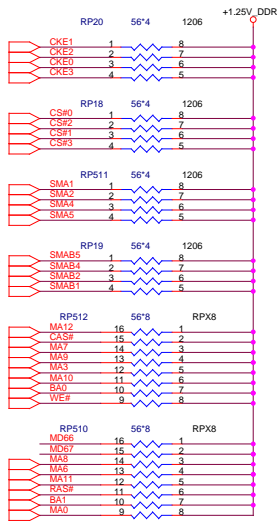
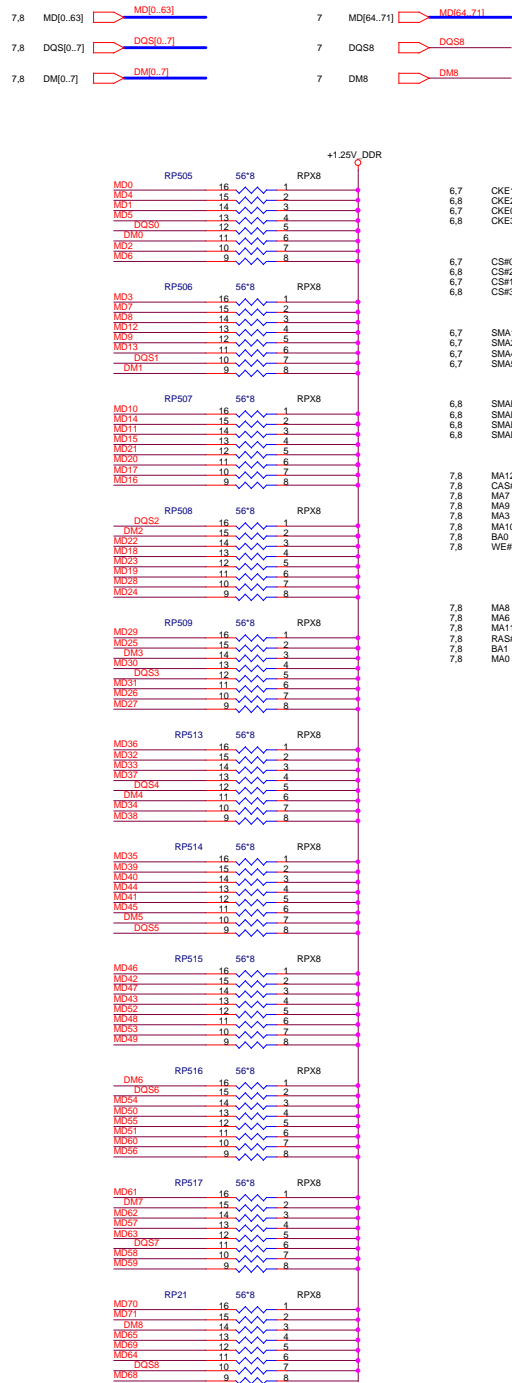


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SO-DIMM

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Data Signals - SDQ[63:0],DM[7:0],DQS[7:0]

Chip -> Rs -> So-DIMM0 -> So-DIMM1 -> Rt

Control Signals - CKE[3:0],CS#[3:0]

Chip -> So-DIMM0 -> So-DIMM1 -> Rt

Command Signals - MA[12:6,3,0],BA[1:0],RAS#,CAS#,WE#

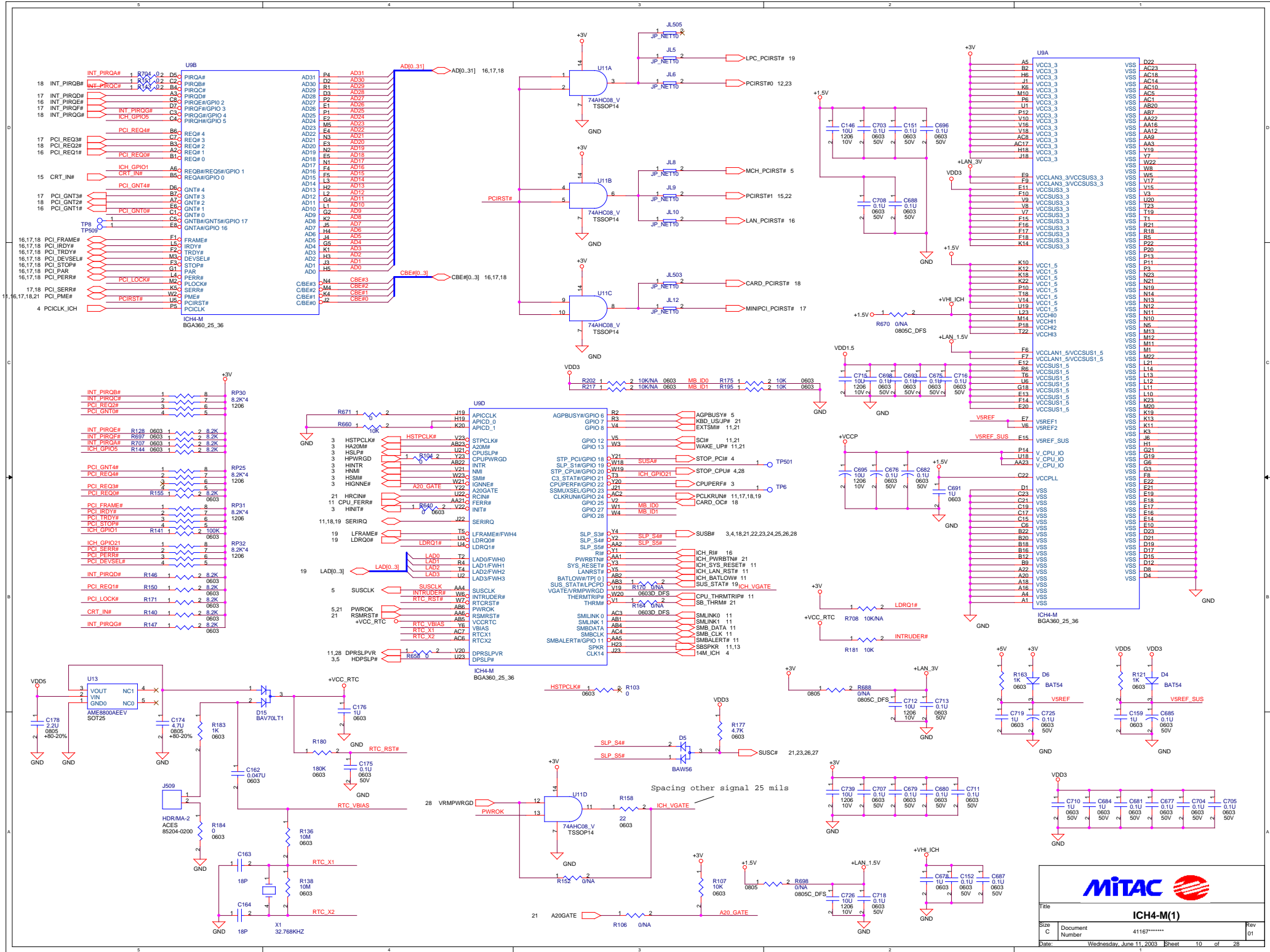
1. Chip -> So-DIMM0 -> Rs -> So-DIMM1 -> Rt

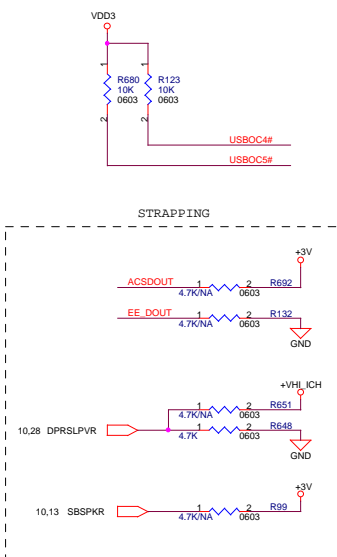
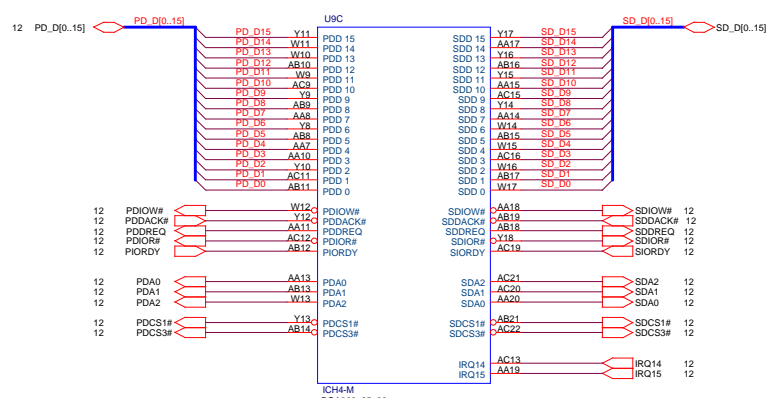
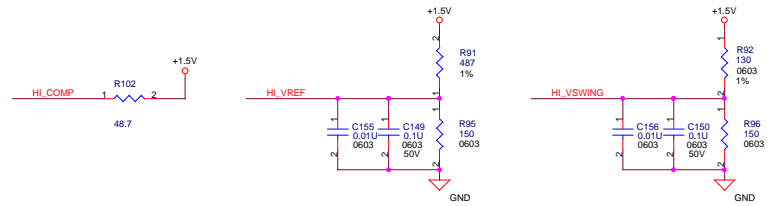
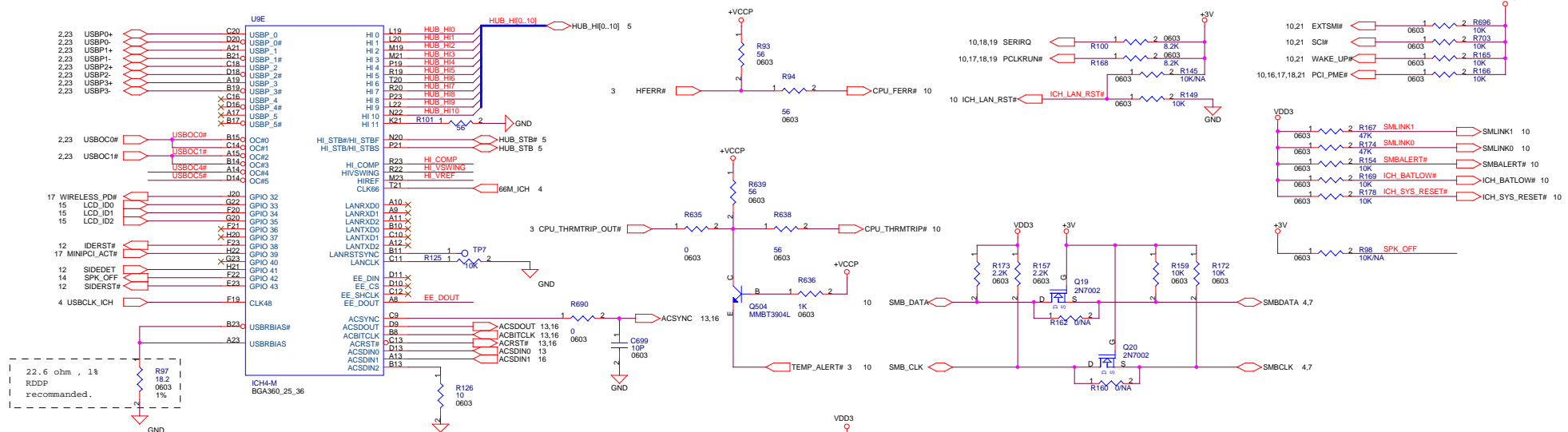
2. Chip -> Rs -> So-DIMM0 -> So-DIMM1 -> Rt Intel DEMO ckt using this topology

3. Chip -> So-DIMM0 -> Rt -> Rs -> So-DIMM1

CPC Signals - SMA[5,4,2,1],SMAB[5,4,2,1]

Chip -> So-DIMM0 -> So-DIMM1 -> Rt





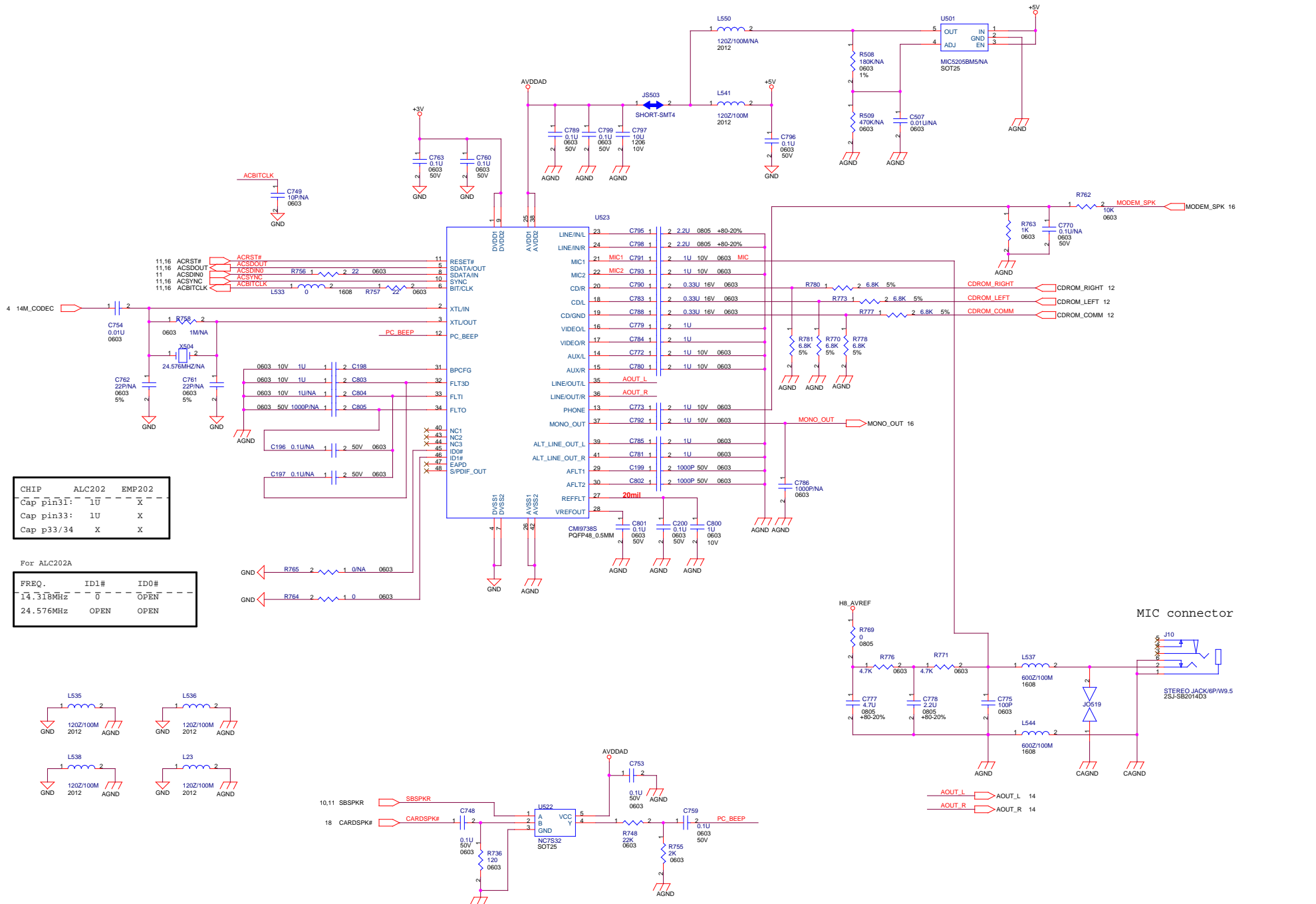
STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
GNTA#	OP-BLOCK SWAP OVERRIDE
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME
HUB_ICH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT

GPIO CHARACTERISTIC LIST

NAME	TYPE	POWER PLANE	CURRENT DEFINE
GPIO[0]	I	MAIN POWER WELL	CRT_IN#
GPIO[1]	I	MAIN POWER WELL	X
GPIO[2]	I	MAIN POWER WELL	INT_PIRQ#
GPIO[3]	I	MAIN POWER WELL	INT_PIRQ#
GPIO[4]	I	MAIN POWER WELL	INT_PIRQ#(Pull high only)
GPIO[5]	I	MAIN POWER WELL	X
GPIO[6]	I	MAIN POWER WELL	AGP_BUSY#
GPIO[7]	I	MAIN POWER WELL	KB_US/JP#
GPIO[8]	I	RESUME POWER WELL	EXTSMI#
GPIO[11]	I	RESUME POWER WELL	SMBALERT#(Pull high only)
GPIO[12]	I	RESUME POWER WELL	SCI#
GPIO[13]	I	RESUME POWER WELL	WAKE_UP#
GPIO[16]	O	MAIN POWER WELL	X
GPIO[17]	O	MAIN POWER WELL	X
GPIO[18]	O	MAIN POWER WELL	STOP_FCI#
GPIO[19]	O	MAIN POWER WELL	SUSA#
GPIO[20]	O	MAIN POWER WELL	STOP_CPU#
GPIO[21]	O	MAIN POWER WELL	X
GPIO[22]	OD	MAIN POWER WELL	CPUPERF#
GPIO[23]	O	MAIN POWER WELL	X
GPIO[24]	I/O	RESUME POWER WELL	PCLKRUN#
GPIO[25]	I/O	RESUME POWER WELL	CARD_OC#
GPIO[27]	I/O	RESUME POWER WELL	MB_ID0
GPIO[28]	I/O	RESUME POWER WELL	MB_ID1
GPIO[32]	I/O	MAIN POWER WELL	WIRELESS_PDH
GPIO[33]	I/O	MAIN POWER WELL	LCDDI0
GPIO[34]	I/O	MAIN POWER WELL	LCDDI1
GPIO[35]	I/O	MAIN POWER WELL	LCDDI2
GPIO[36]	I/O	MAIN POWER WELL	X
GPIO[37]	I/O	MAIN POWER WELL	X
GPIO[38]	I/O	MAIN POWER WELL	IDERST#
GPIO[39]	I/O	MAIN POWER WELL	MINIFCI_ACT#
GPIO[40]	I/O	MAIN POWER WELL	X
GPIO[41]	I/O	MAIN POWER WELL	SIDEDBT
GPIO[42]	I/O	MAIN POWER WELL	SPK_OFF
GPIO[43]	I/O	MAIN POWER WELL	SIDERST#

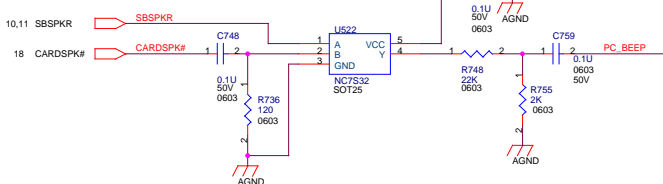
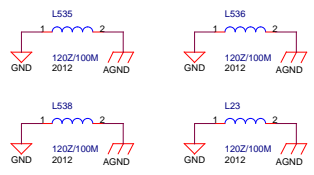


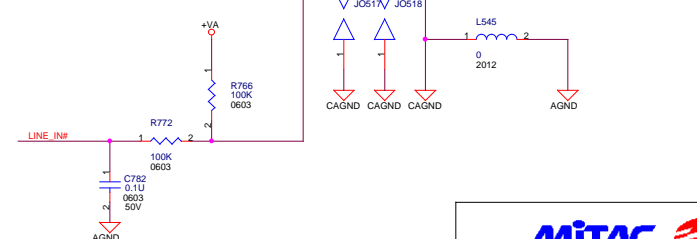
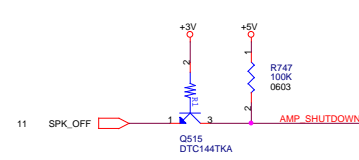
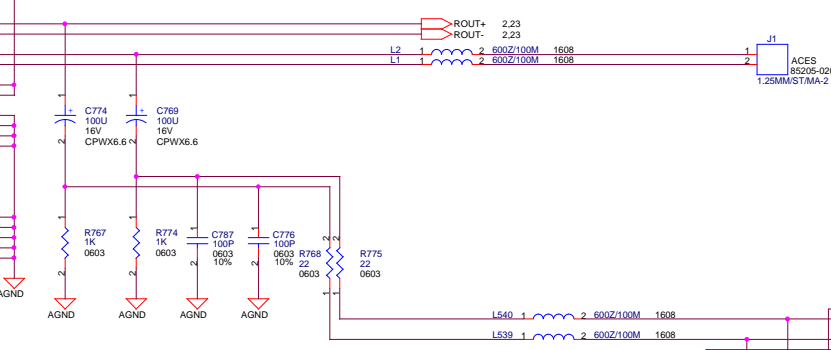
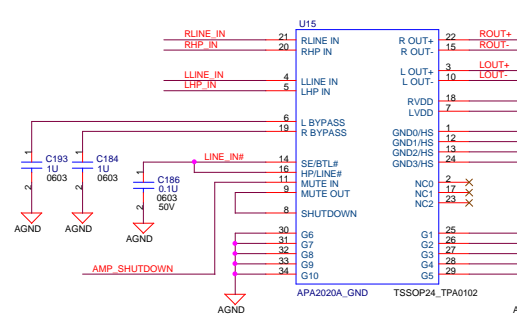
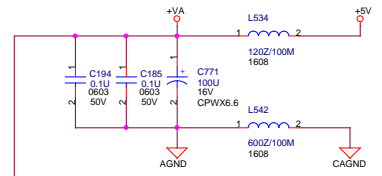
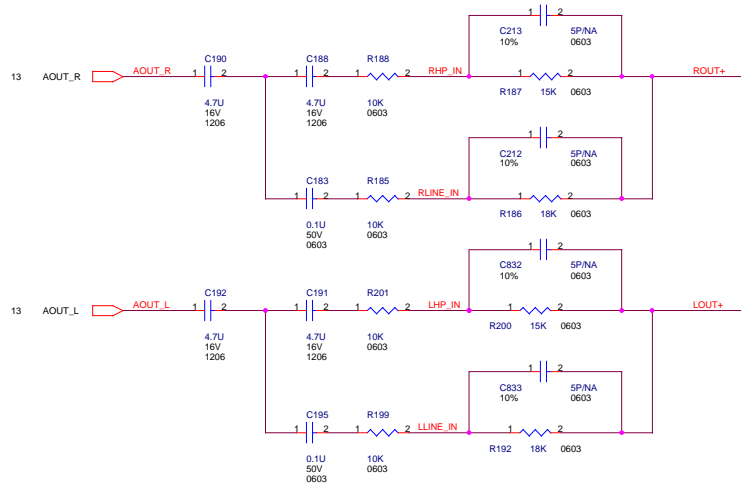


CHIP	ALC202	EMP202
Cap pin31:	1U	X
Cap pin33:	1U	X
Cap p33/34	X	X

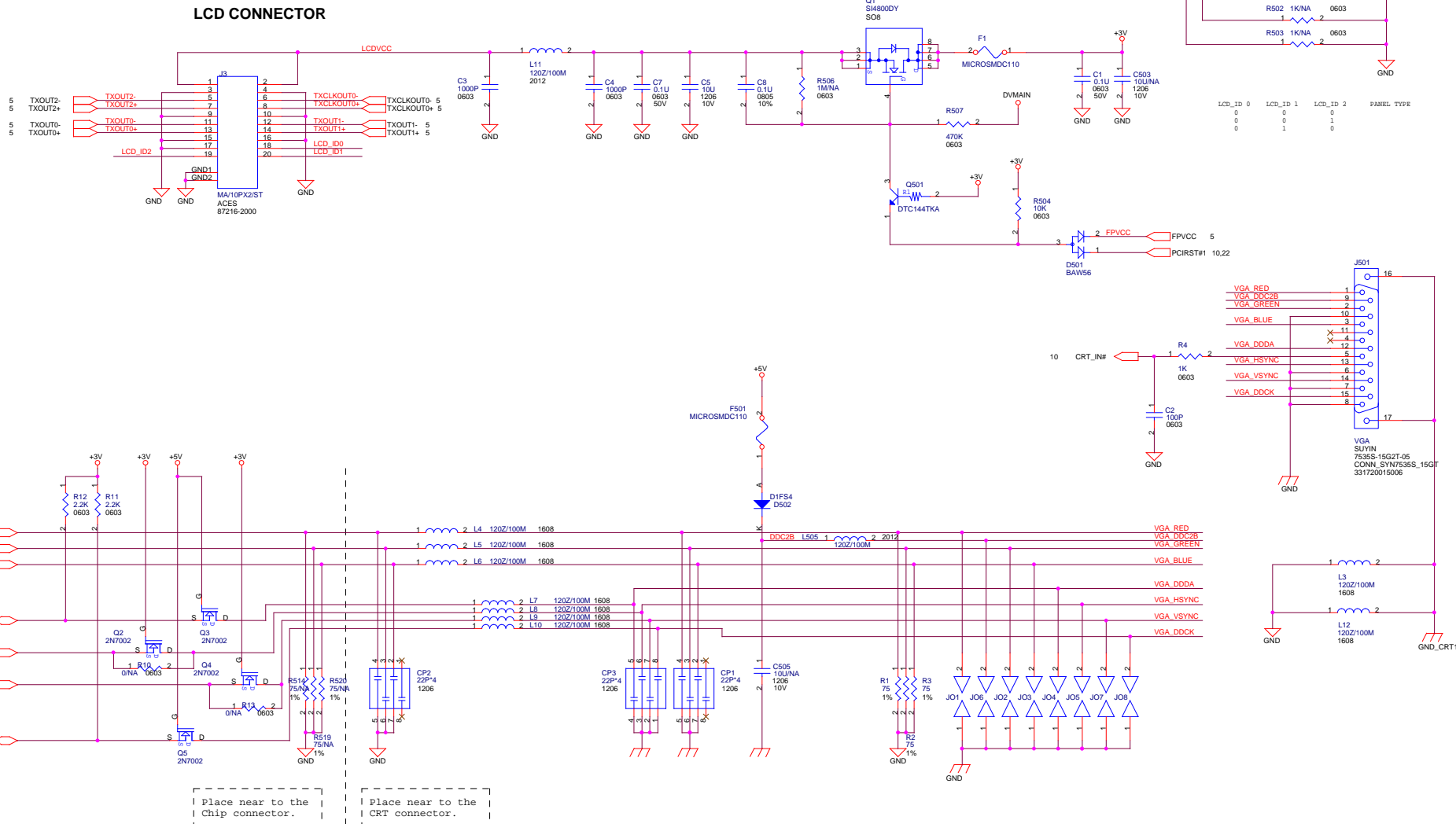
For ALC202A

FREQ.	ID1#	ID0#
14.318MHz	0	OPEN
24.576MHz	OPEN	OPEN





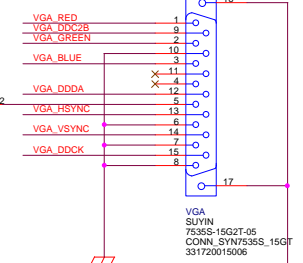
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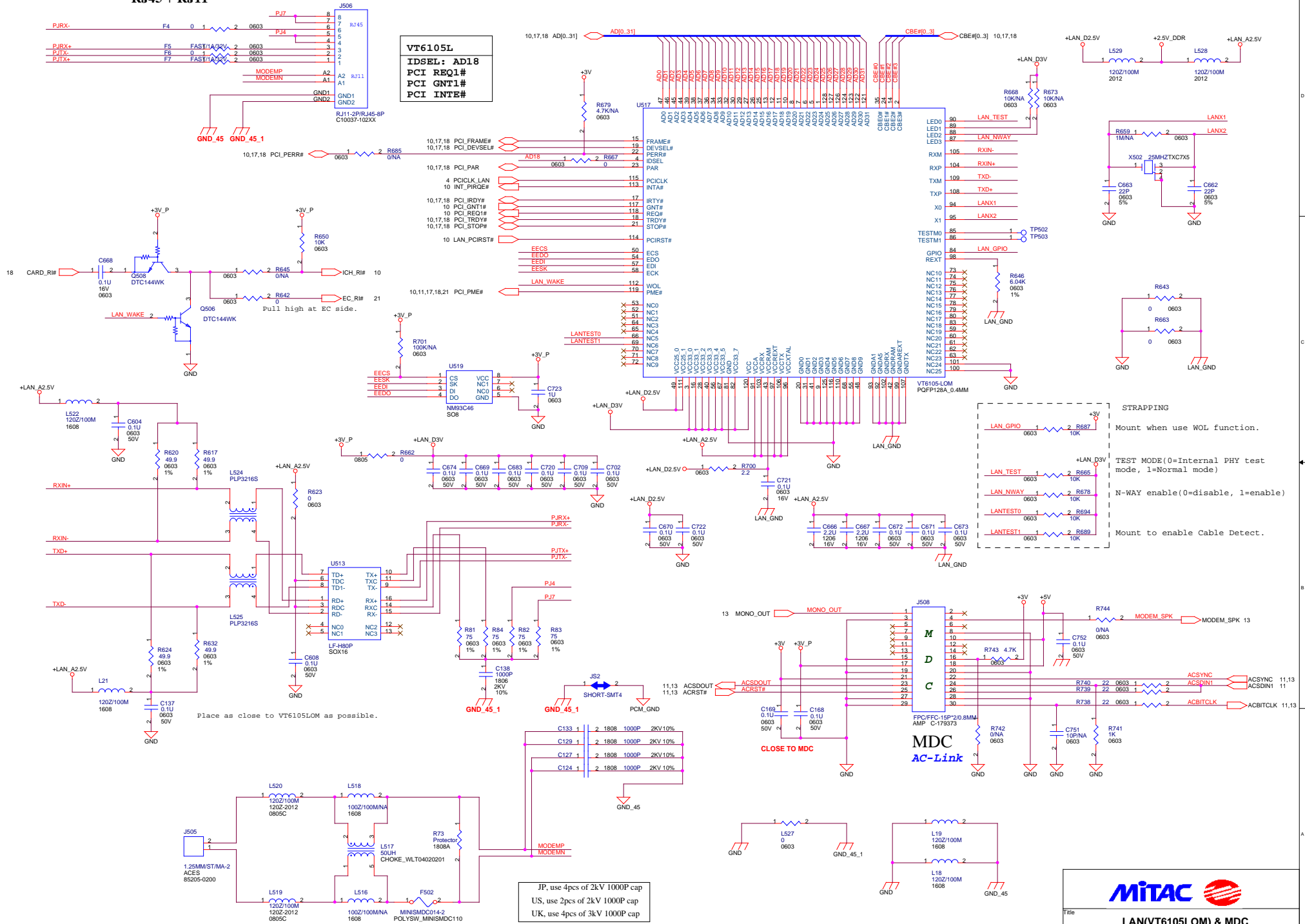
Place near to the
Chip connector.

Place near to the
CRT connector.

LCD_ID 0	LCD_ID 1	LCD_ID 2	PANEL TYPE
0	0	0	0
0	1	0	1



RJ45 + RJ11



VT6105L
IDSEL: AD18
PCI REQ1#
PCI GNT1#
PCI INTE#

STRAPPING

Mount when use WOL function.

TEST MODE(0=Internal PHY test mode, 1=Normal mode)

N-WAY enable(0=disable, 1=enable)

Mount to enable Cable Detect.

JP, use 4pcs of 2kV 1000P cap
 US, use 2pcs of 2kV 1000P cap
 UK, use 4pcs of 3kV 1000P cap

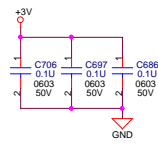
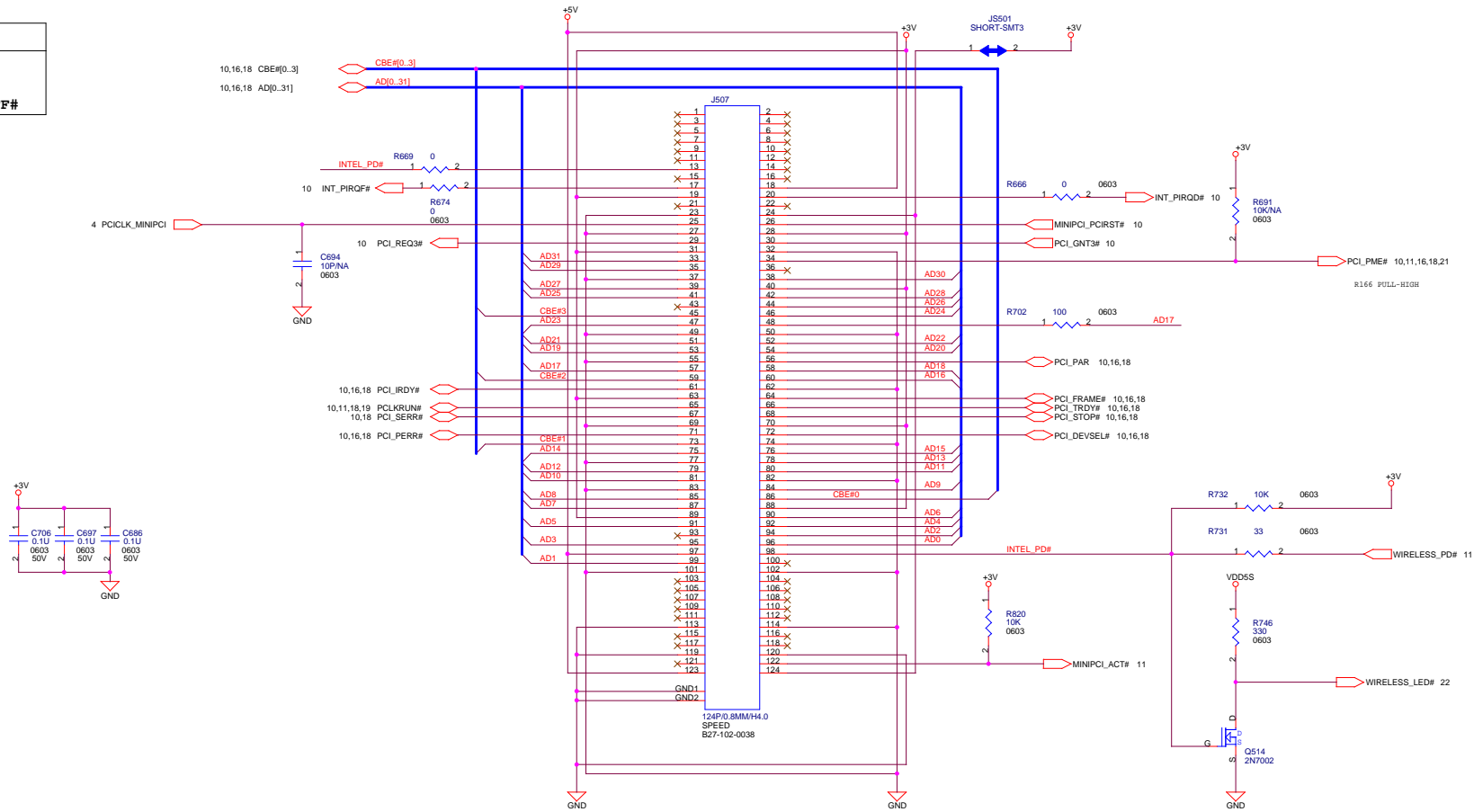
MITAC

LAN(VT6105LOM) & MDC

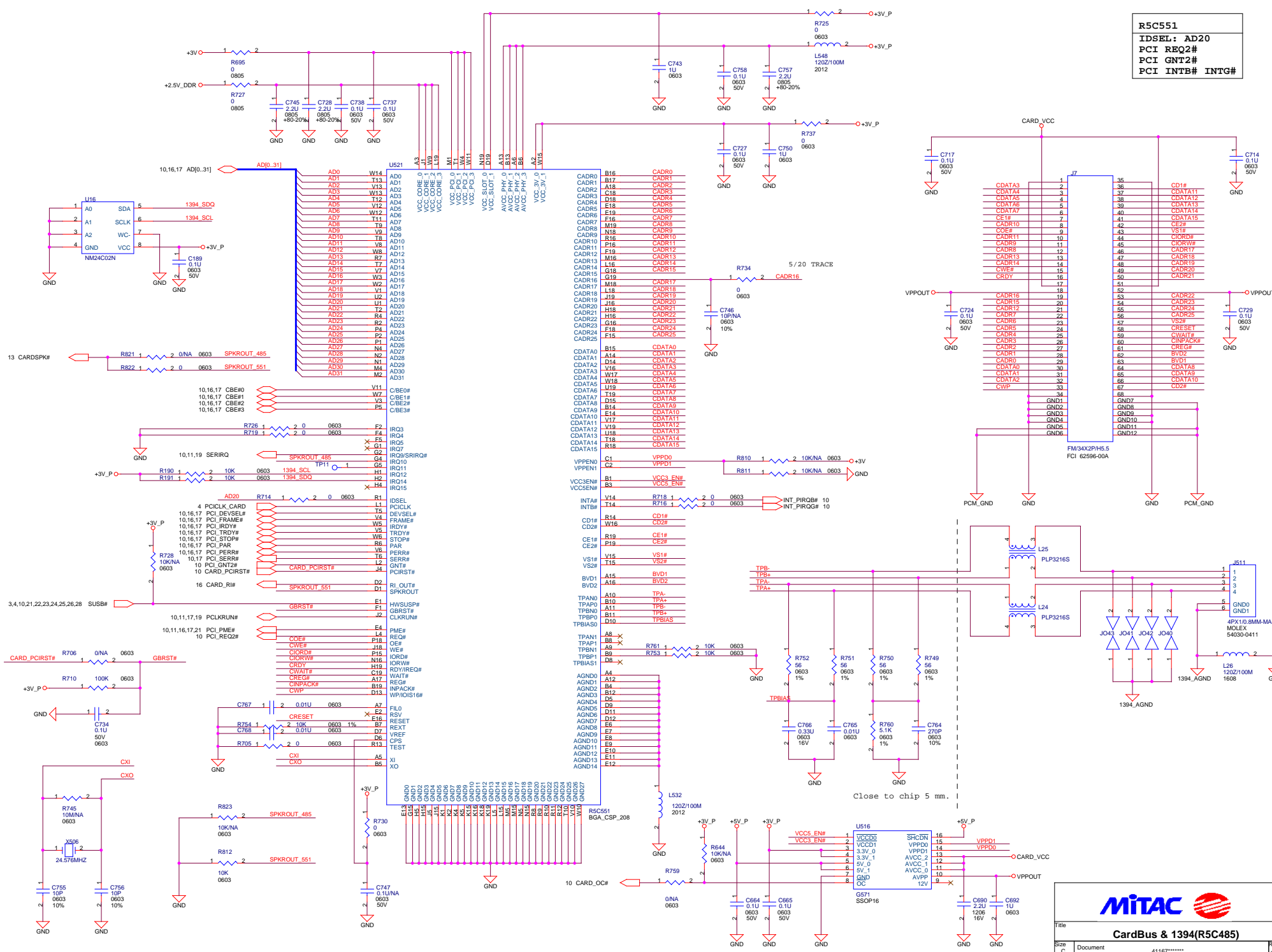
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Mini PCI
 IDSEL: AD17
 PCI REQ3#
 PCI GNT3#
 PCI INTD# INTF#



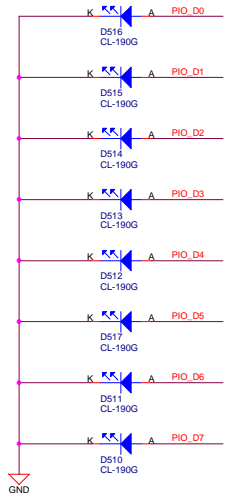
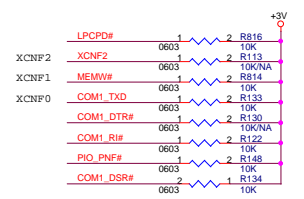
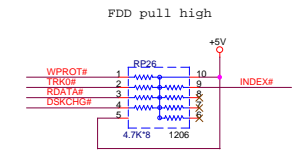
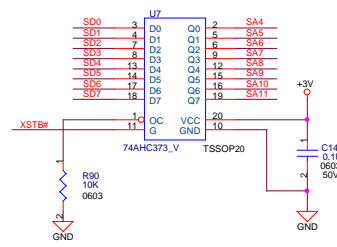
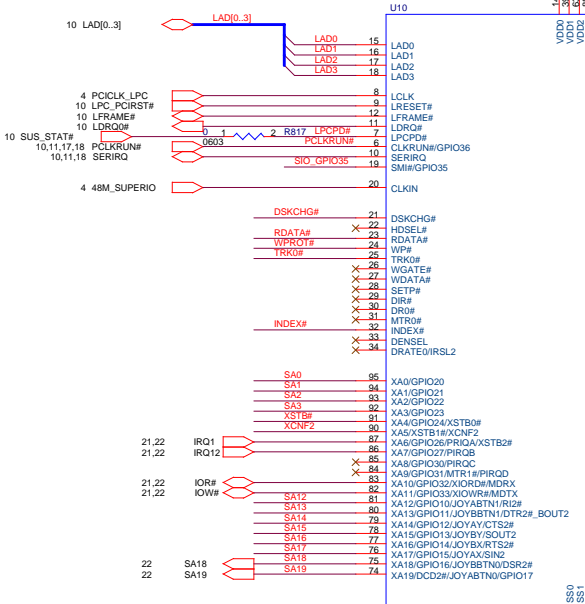
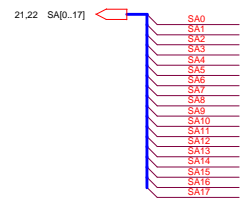
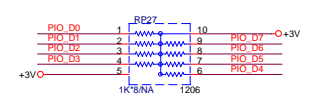
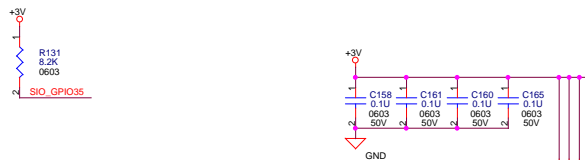
R5C551
IDSEL: AD20
PCI REQ2#
PCI GNT2#
PCI INTB# INTG#



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CardBus & 1394(R5C485)

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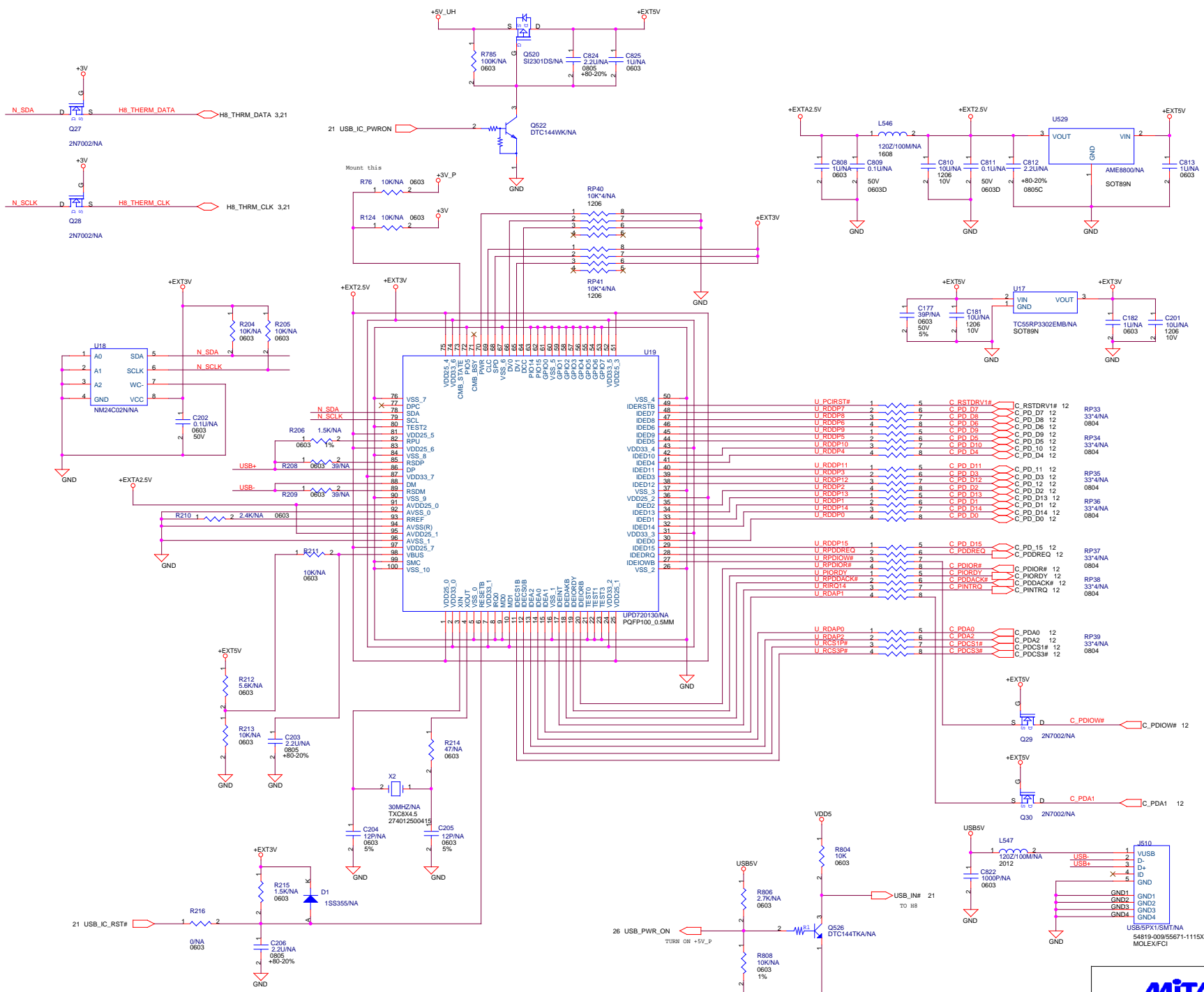
XCNF	DESCRIPTION
2 1 0	
X 0 0	NO BIOS
X 0 1	NORMAL MODE, XRDY DISABLED
0 1 0	LATCH MODE, XA12-19, XRDY ENABLED
1 1 0	LATCH MODE, GPIO10-17, XRDY ENABLED
0 1 1	LATCH MODE, XA12-19, XRDY DISABLED
1 1 1	LATCH MODE, GPIO10-17, XRDY DISABLED

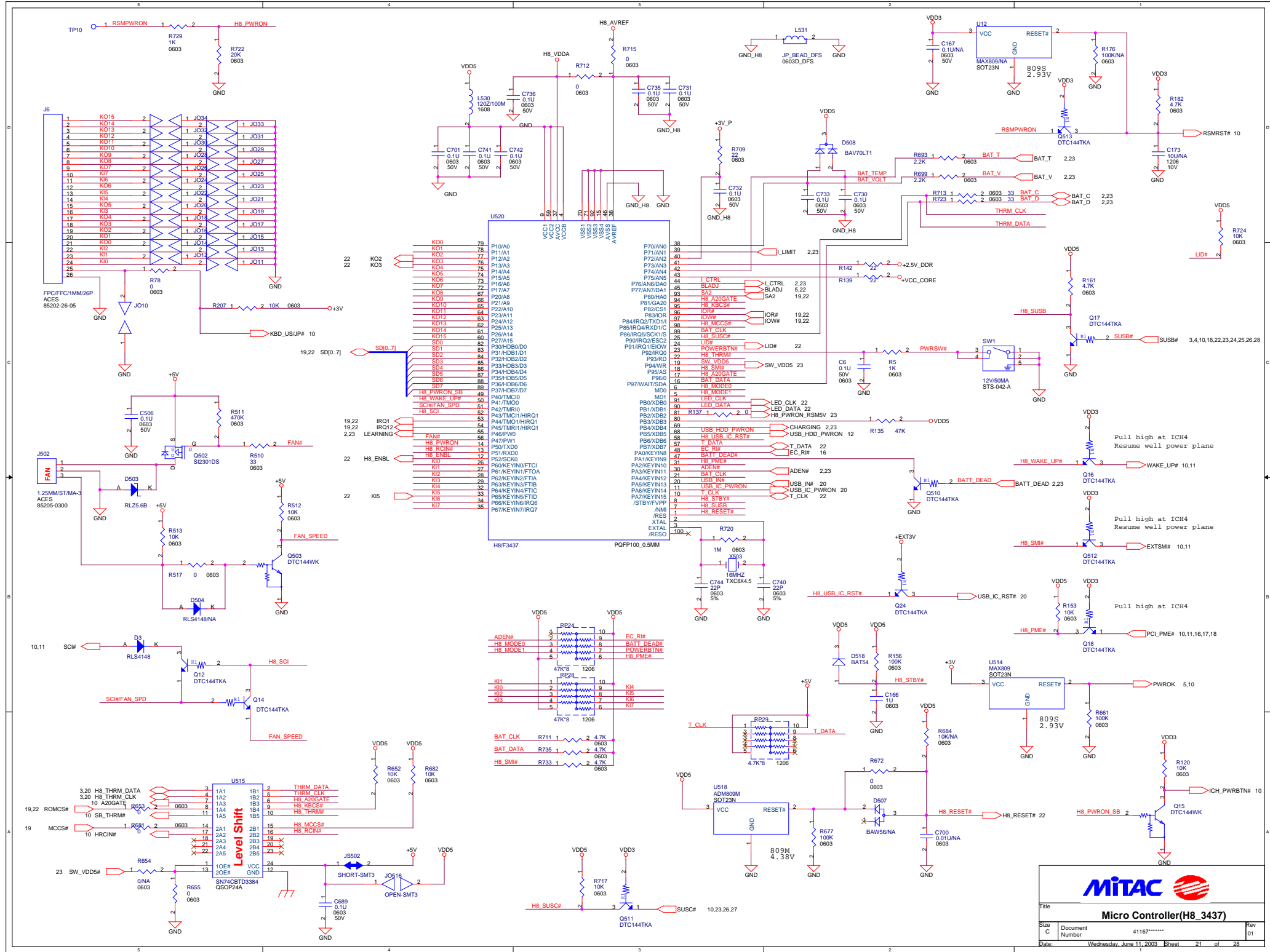
RS232/SIO

MITAC

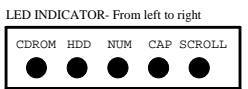
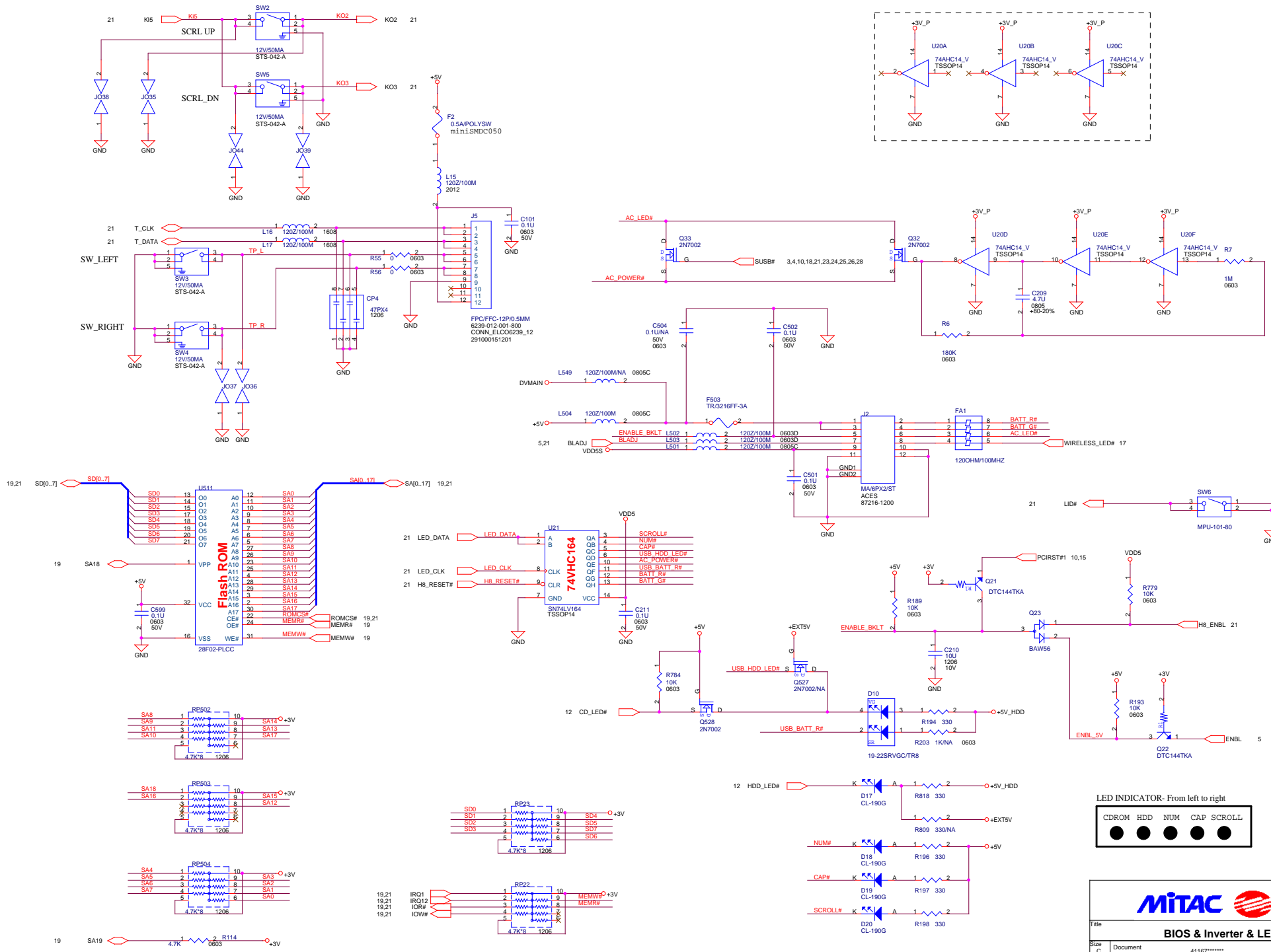
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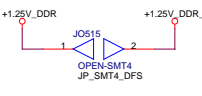
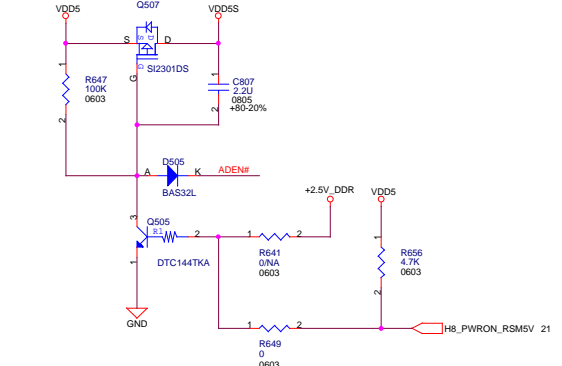
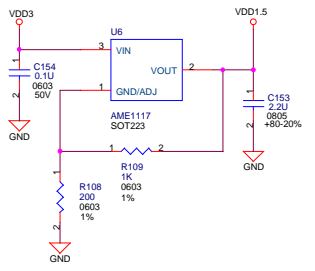
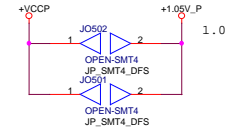
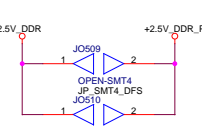
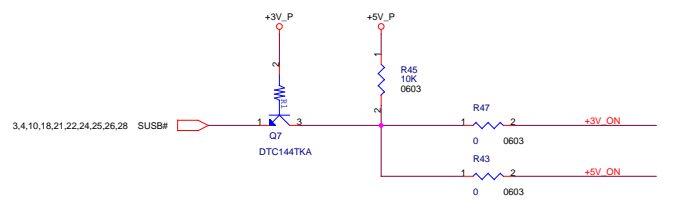
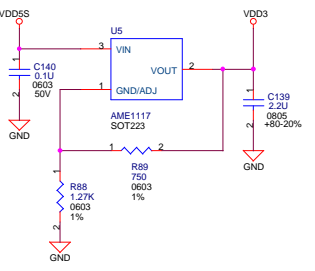
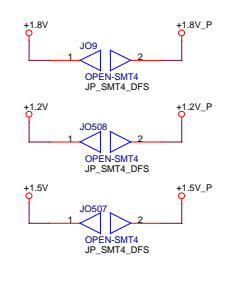
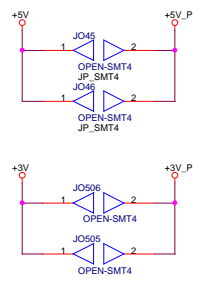
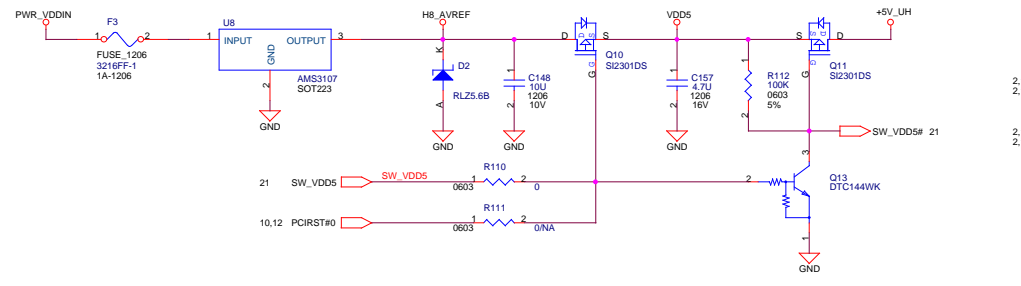
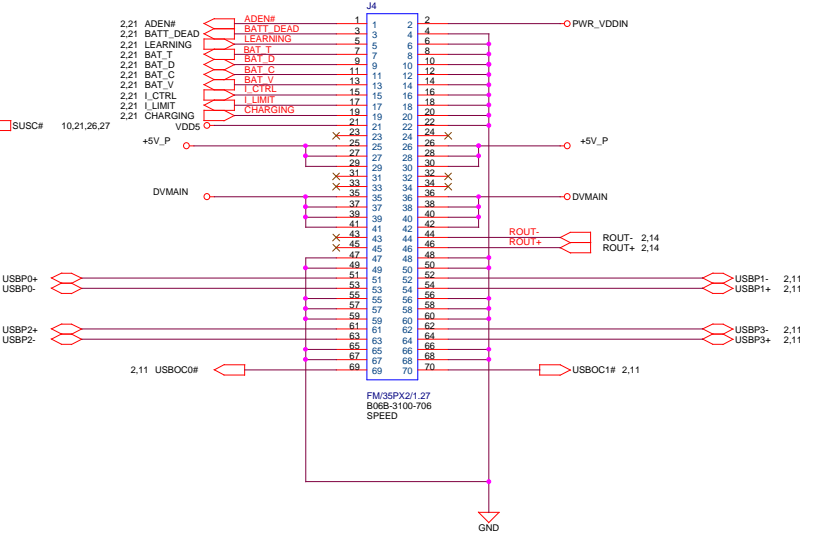
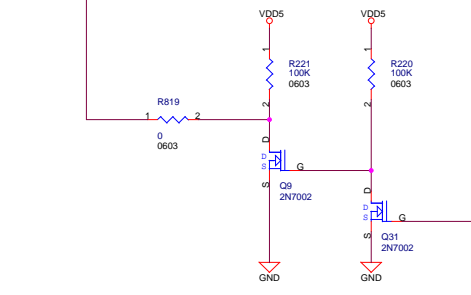
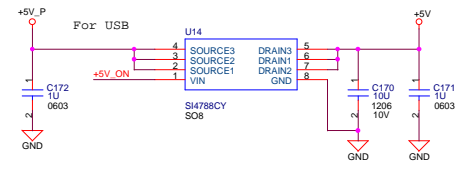
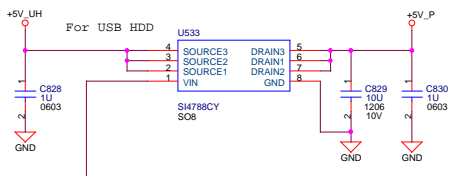
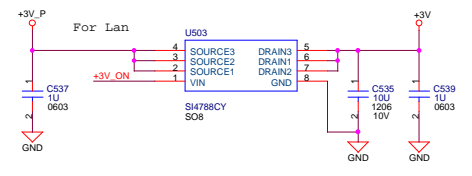
TOUCH_PAD

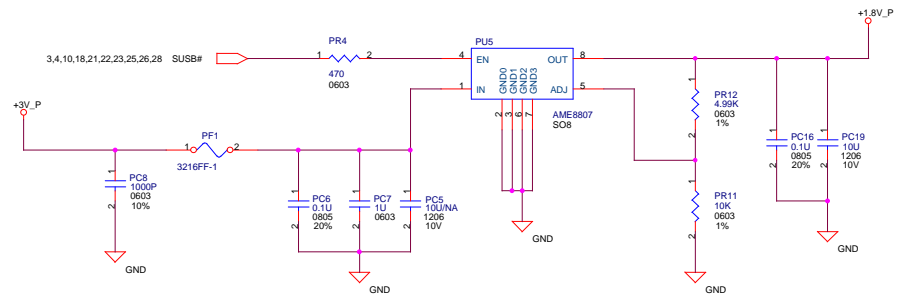
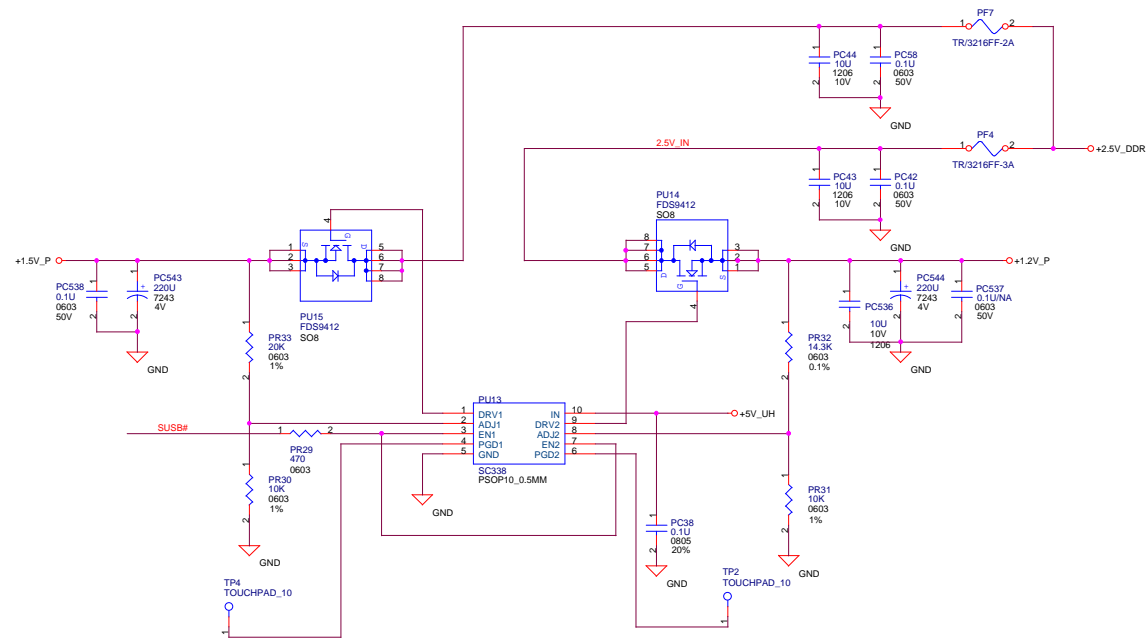


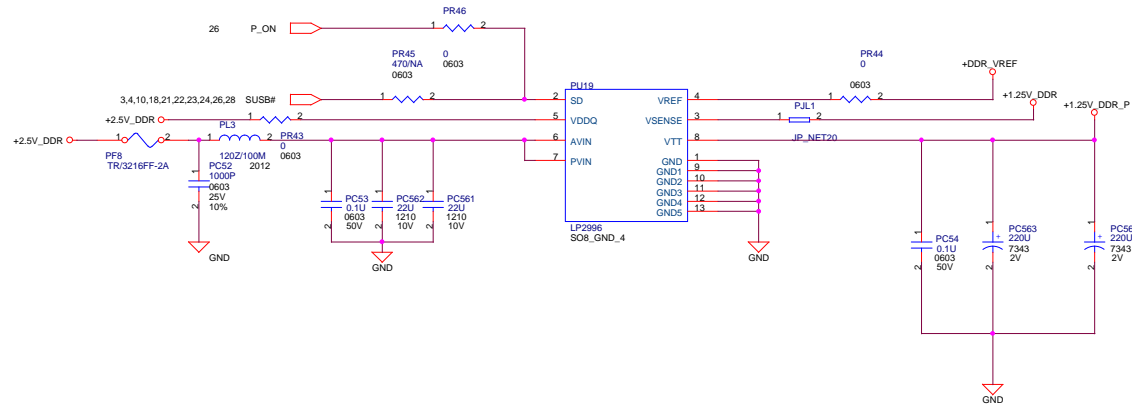
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BIOS & Inverter & LED

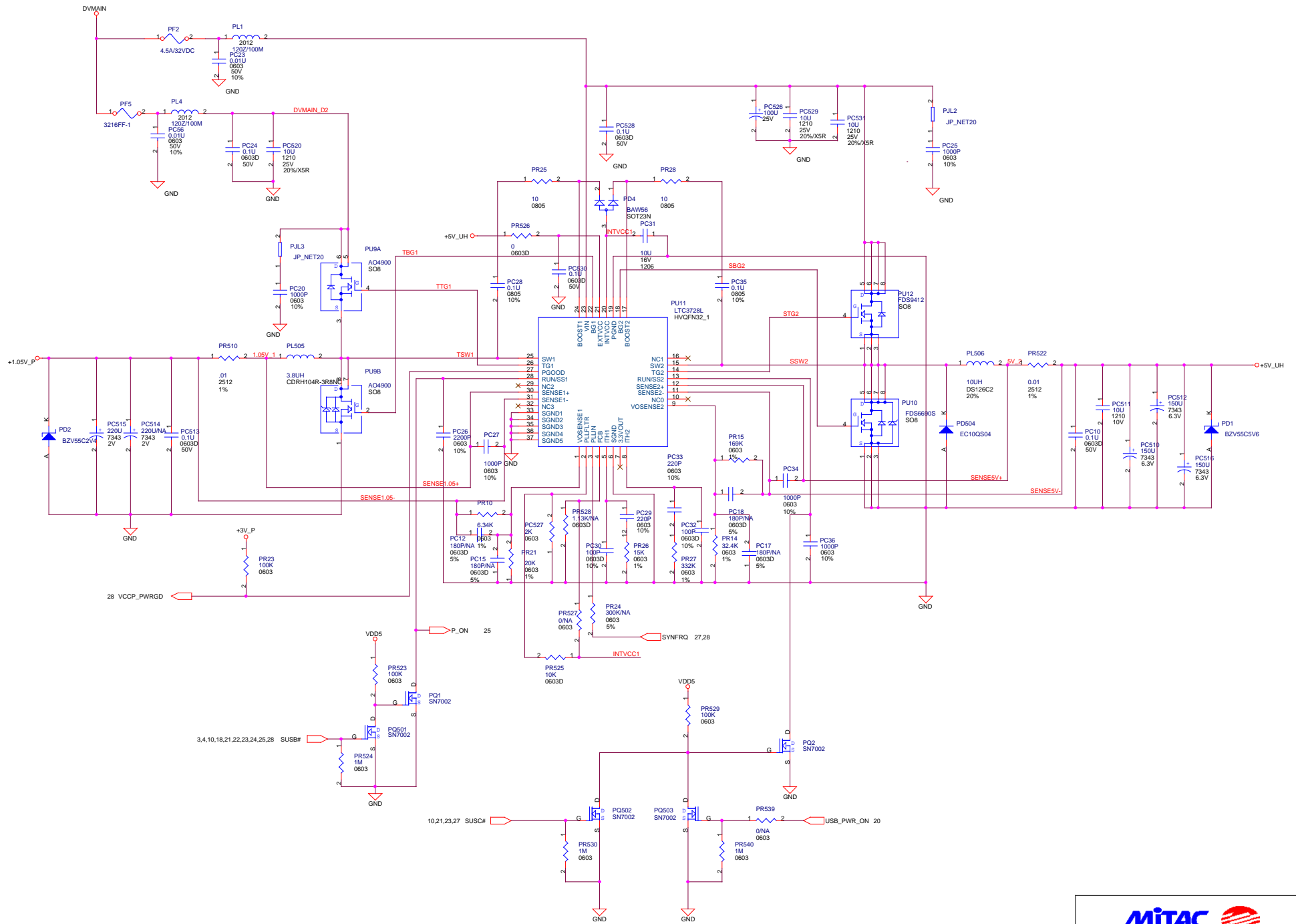
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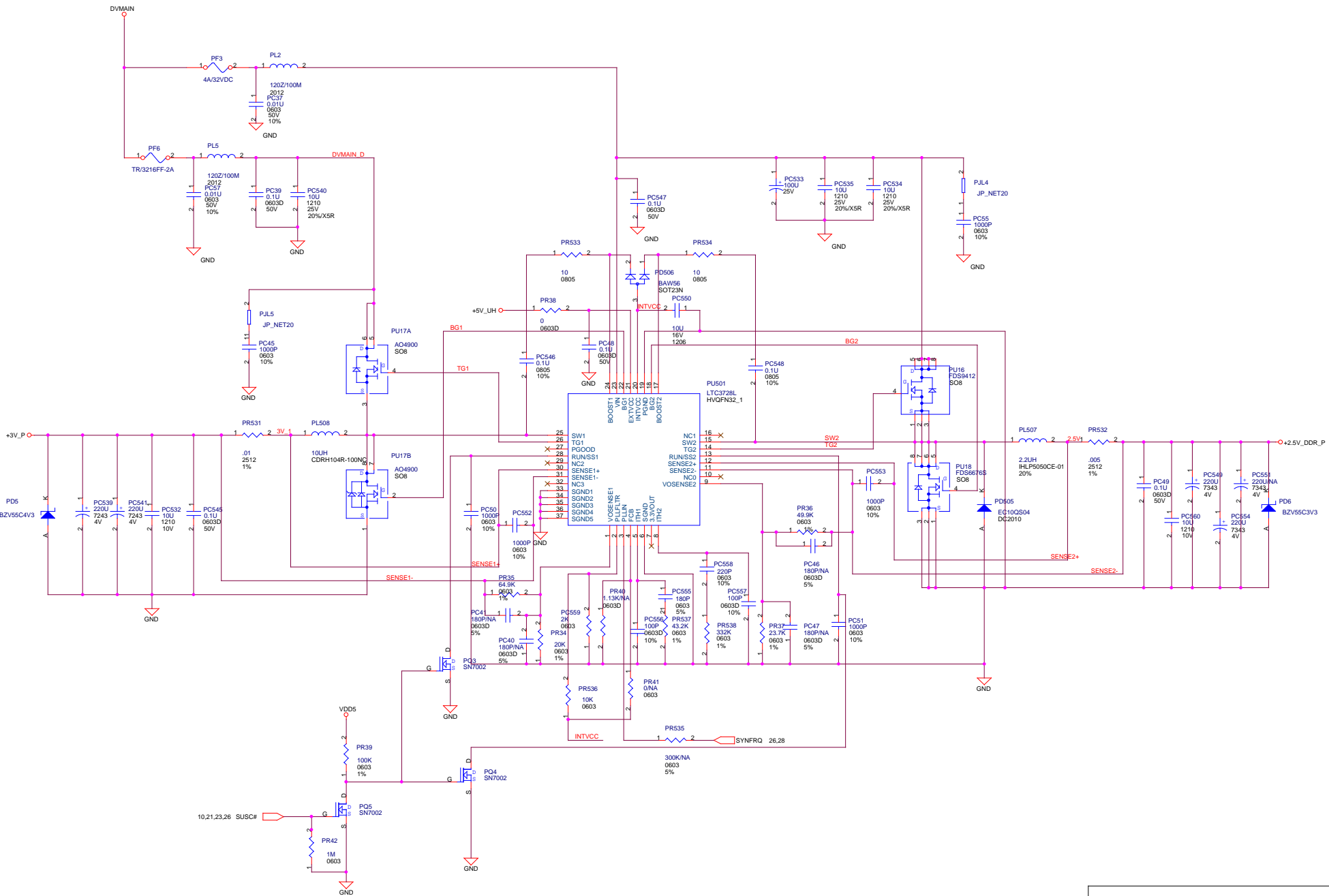




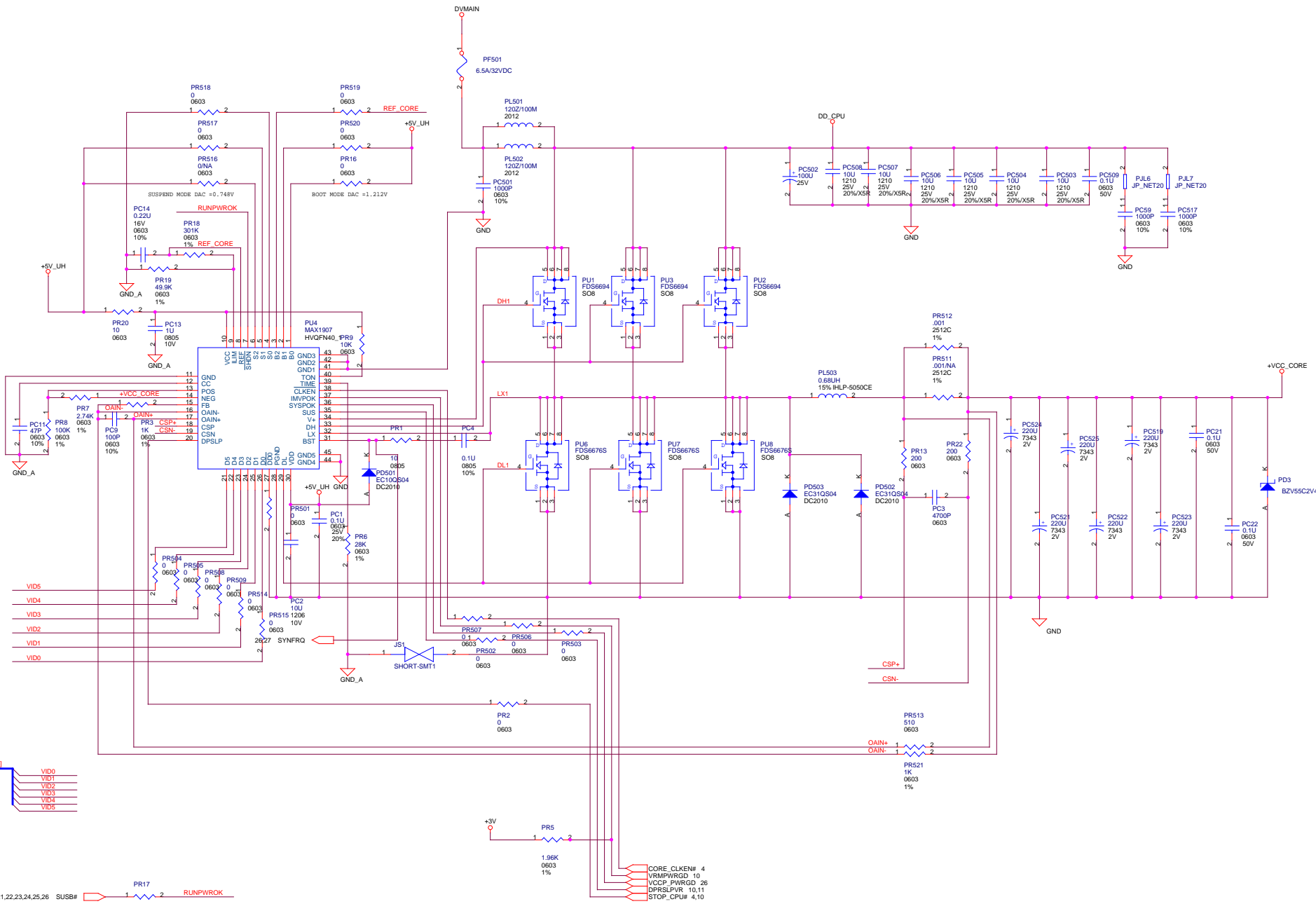


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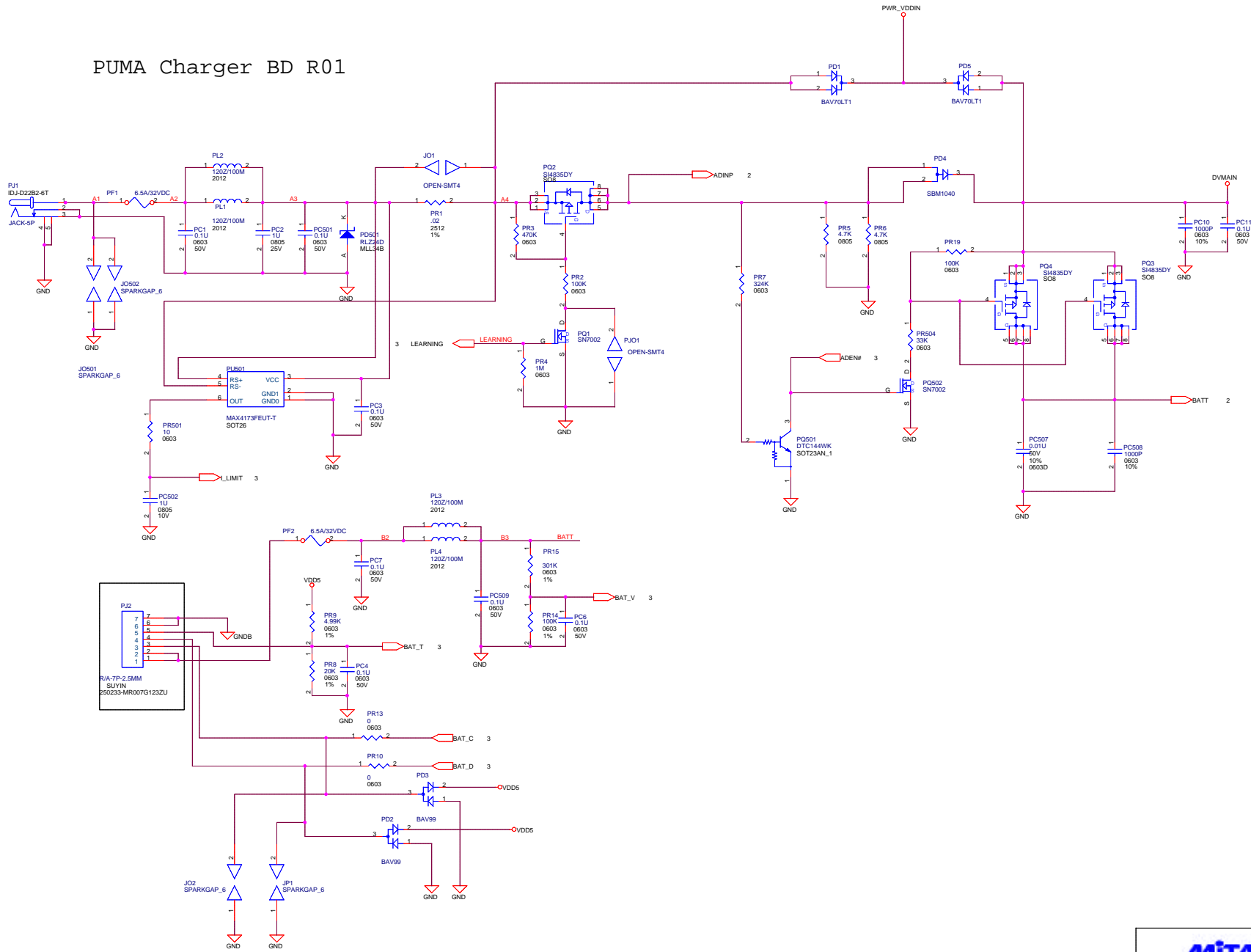


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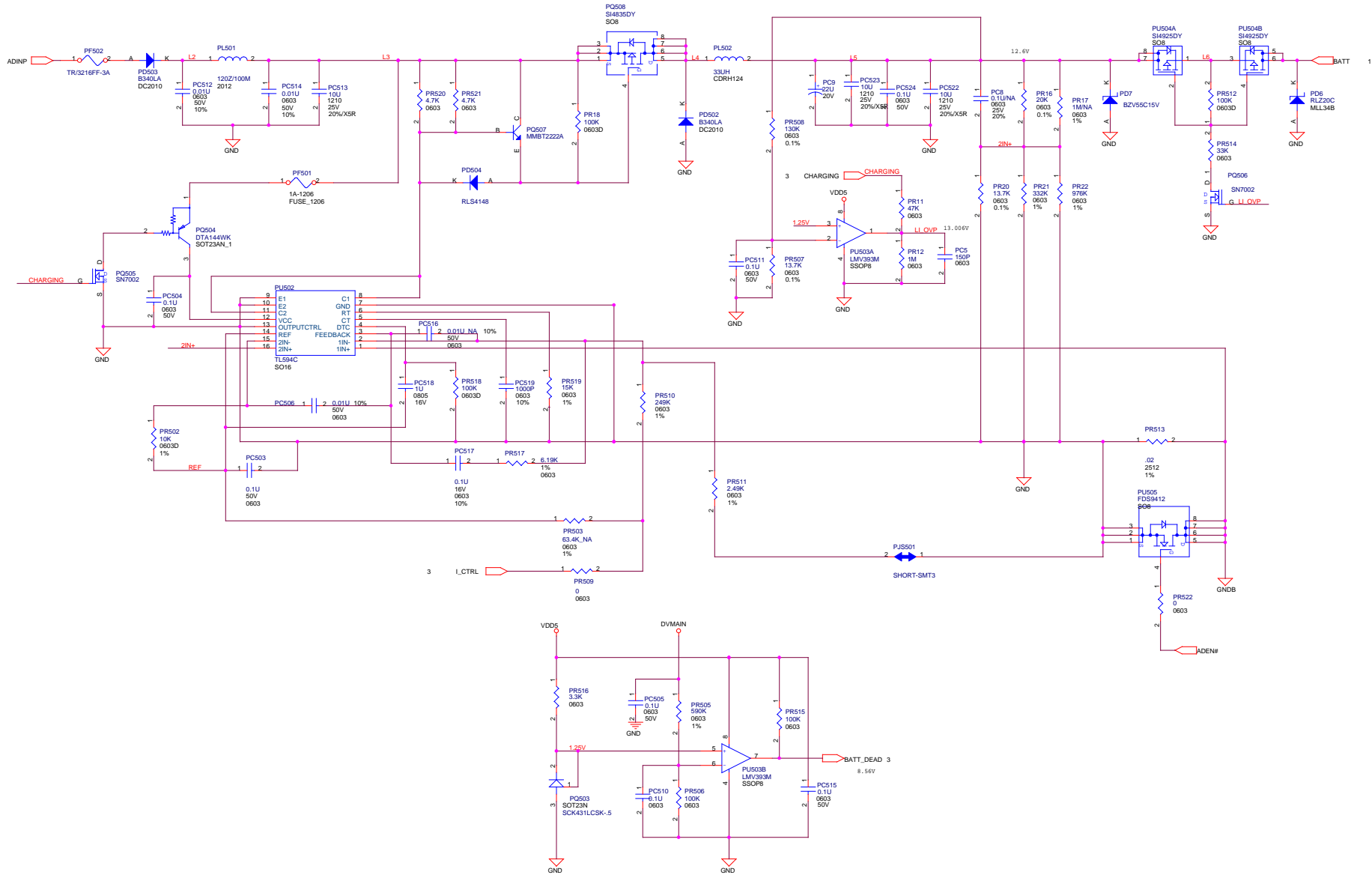
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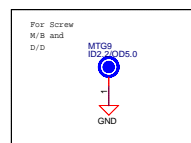
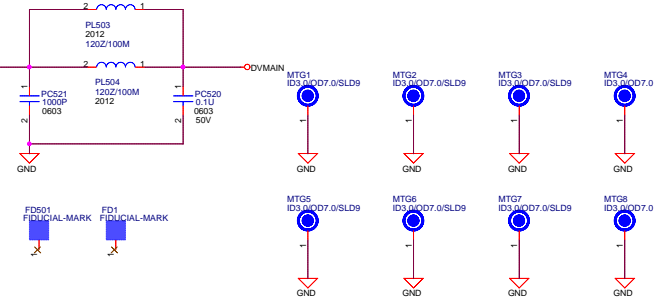
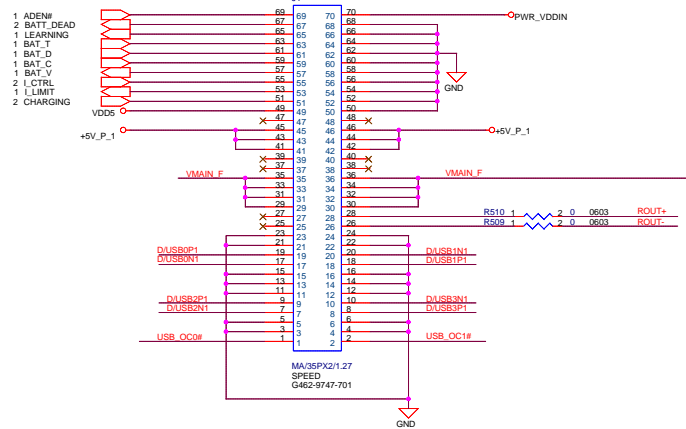
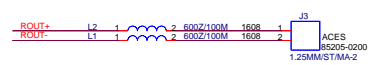
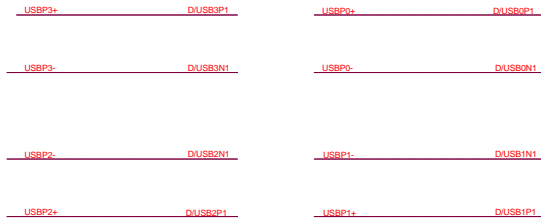
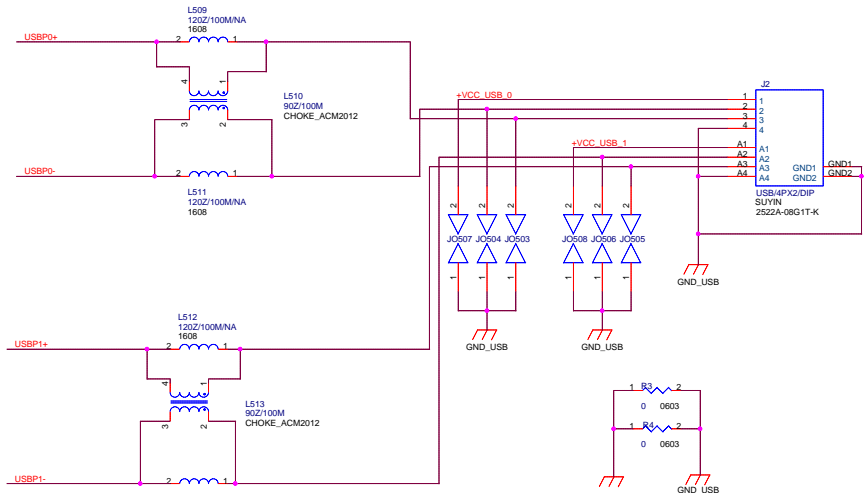
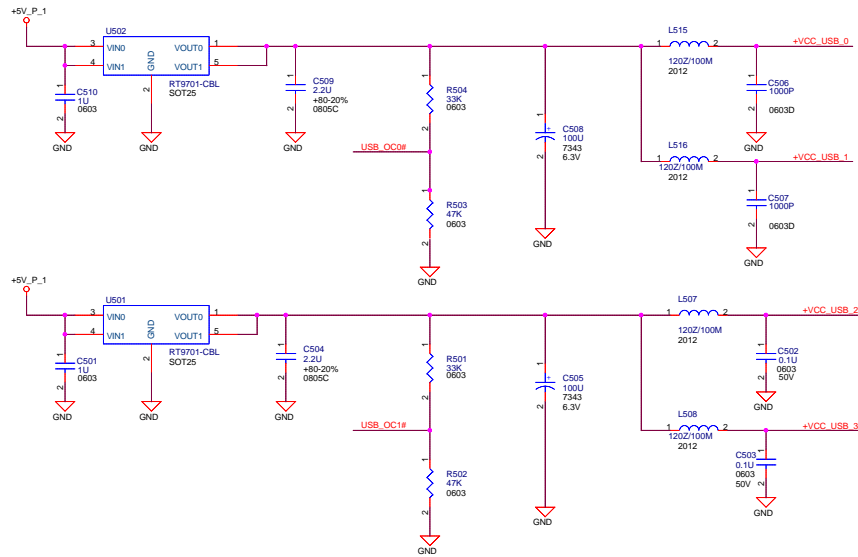
PUMA Charger BD R01



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CHARGING





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USB CONNCOTR

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Reference Material

- ❖ Intel Banias Pentium M Processor Intel, INC
- ❖ Intel 82855GM Memory Controller Hub (GMCH) Intel, INC
- ❖ Intel 82801DBM I/O Controller Hub Mobile (ICH4-M) Intel, INC
- ❖ 8081 Hardware Engineering Specification *Technology Corp./MiTAC*

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