

Compal Confidential

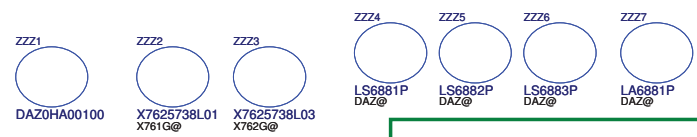
PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT

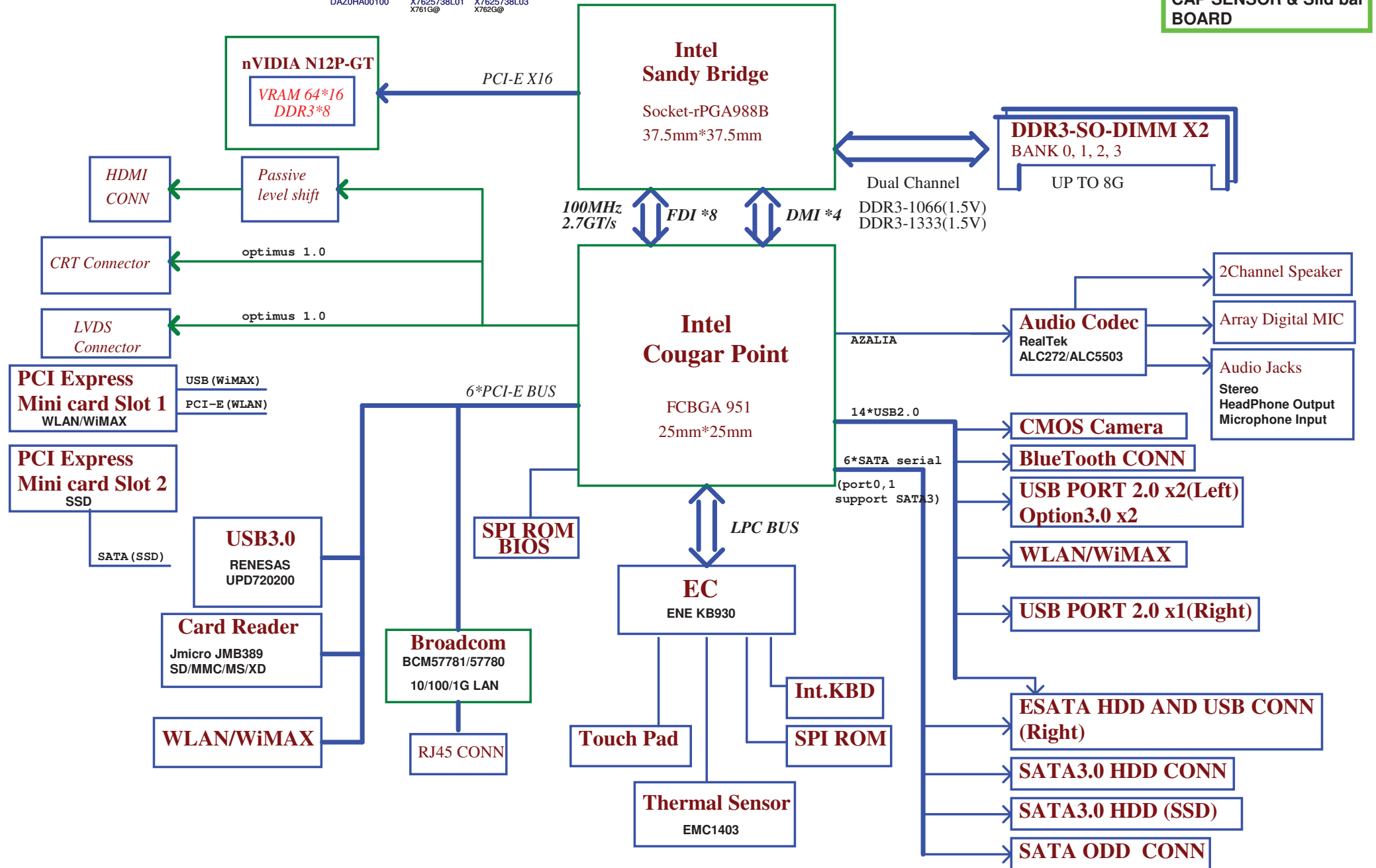
2010-12-30

REV: 1.0

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POWER & ALS BOARD
CAP SENSOR & Slid bar BOARD



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Voltage Rails

power plane	+B	+5VALW	+1.5V	+3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101Xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
		12	
UHCI6	13	Blue Tooth	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

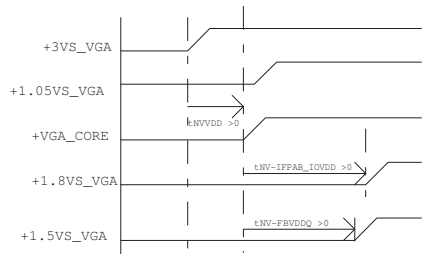
VRAM BOM Config

X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

GPU BOM Config

N12P SKU:	OPTI@
GS SKU:	GS@
GT SKU:	GT@

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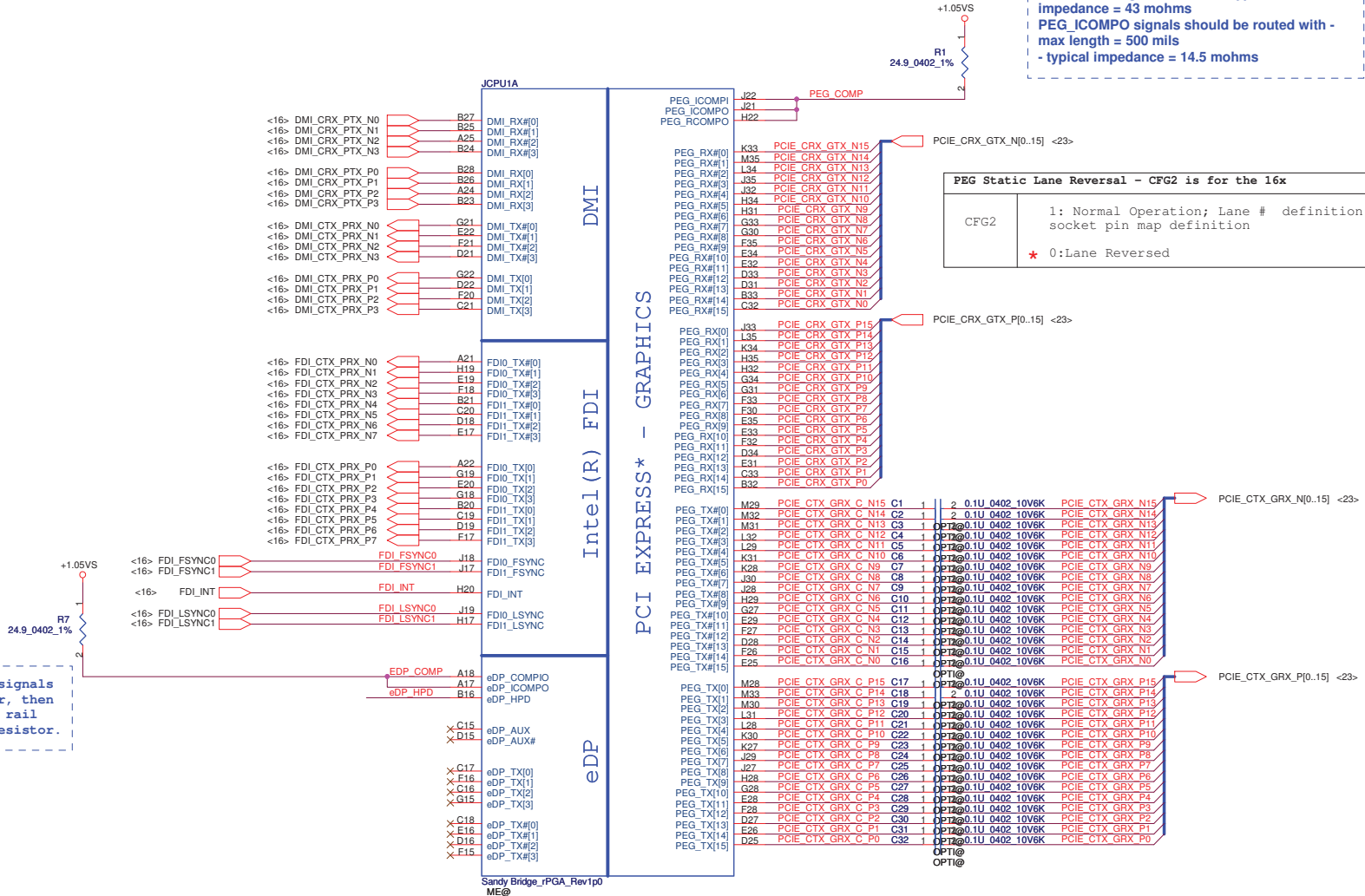


1. The ramp rate for any rail must be more than 40us.
2. +VGA_CORE <= +3VS_VGA +0.5V
3. +1.5VS_VGA <= +3VS_VGA +0.5V
4. Optimus follows power sequencing rules specified in discrete GPU design guide.

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eDP_COMPIO and ICOMPO signals should be tied together, then connected to the VCCIO rail via a single 24.9ohm resistor.

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



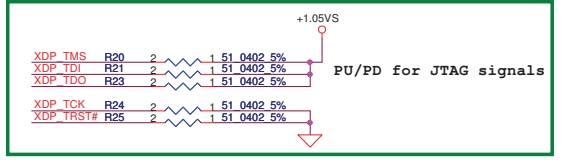
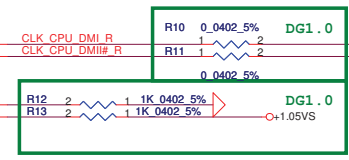
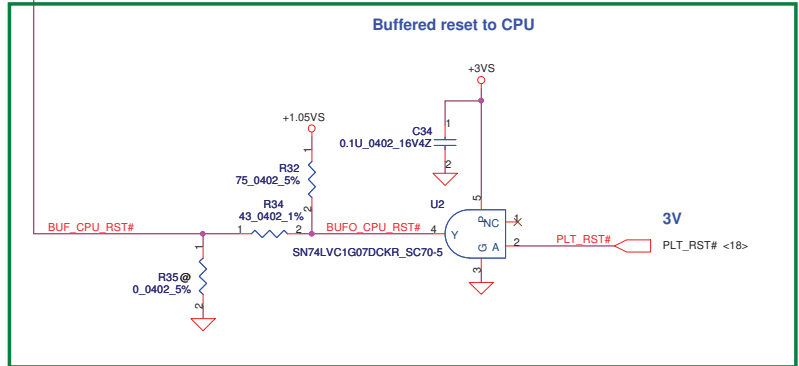
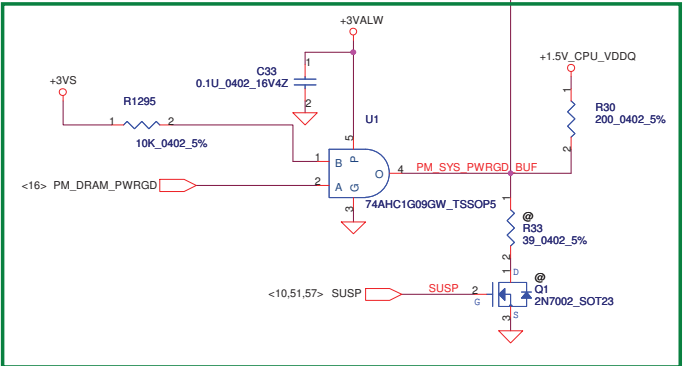
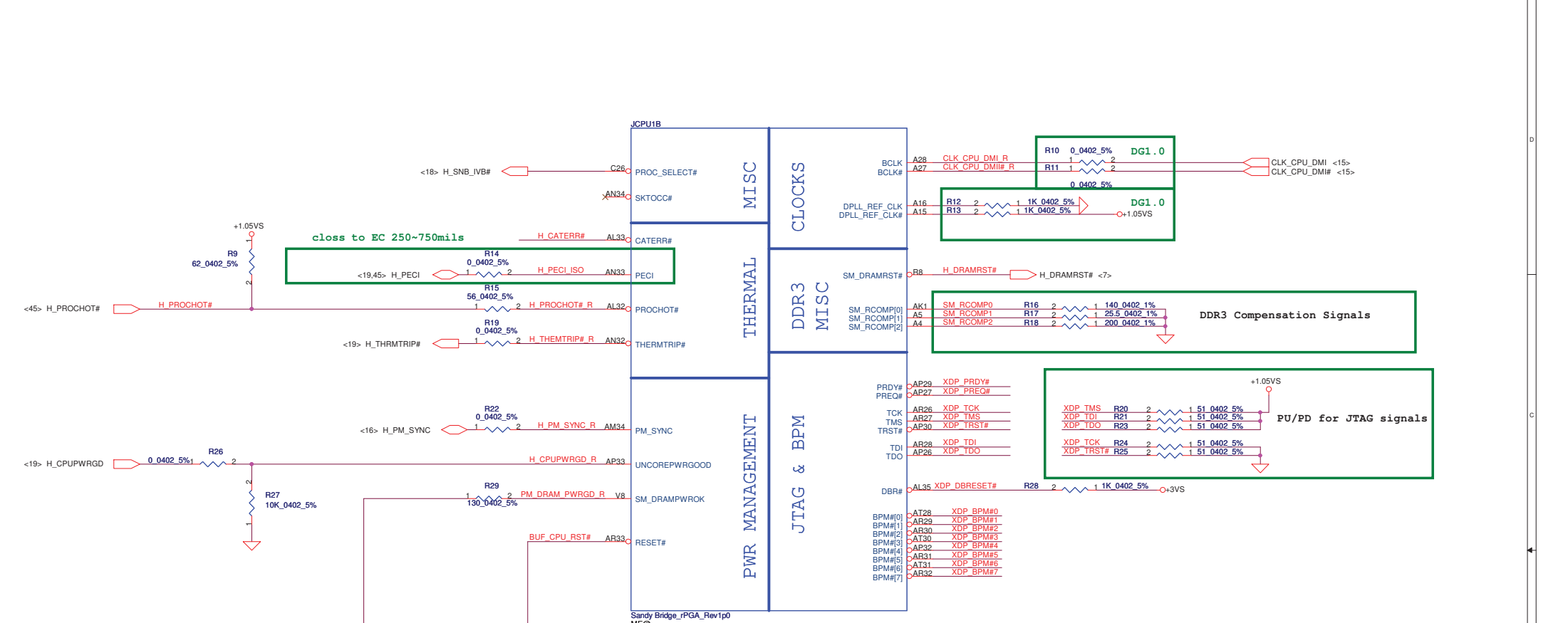
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
*	0: Lane Reversed

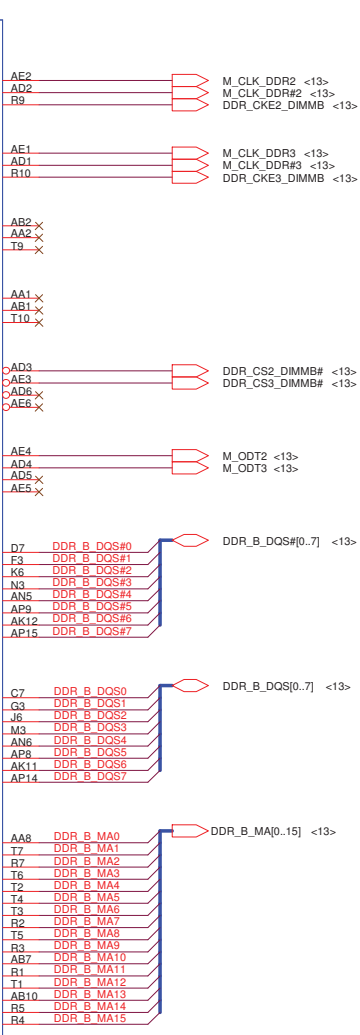
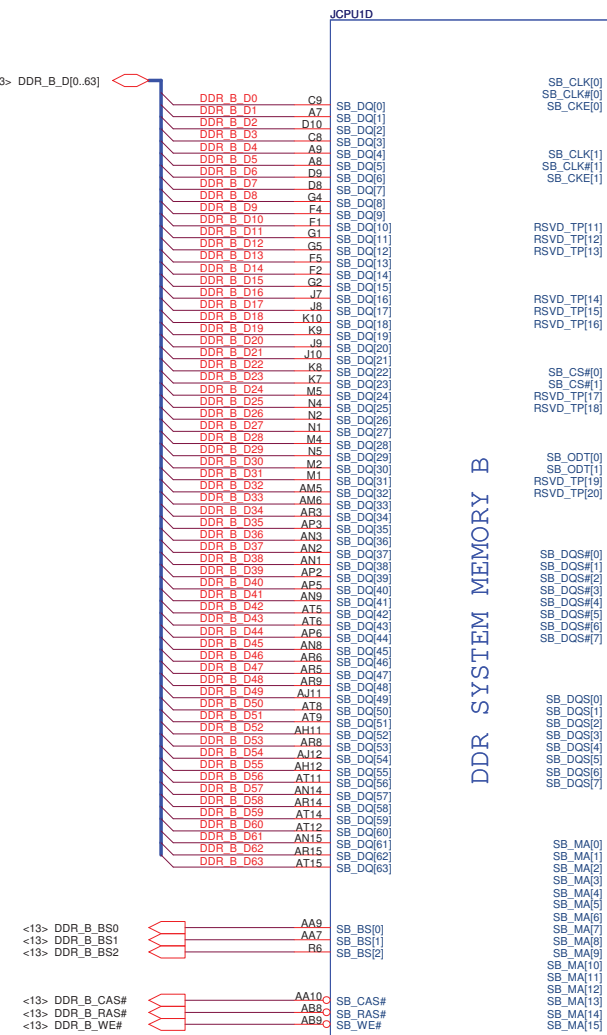
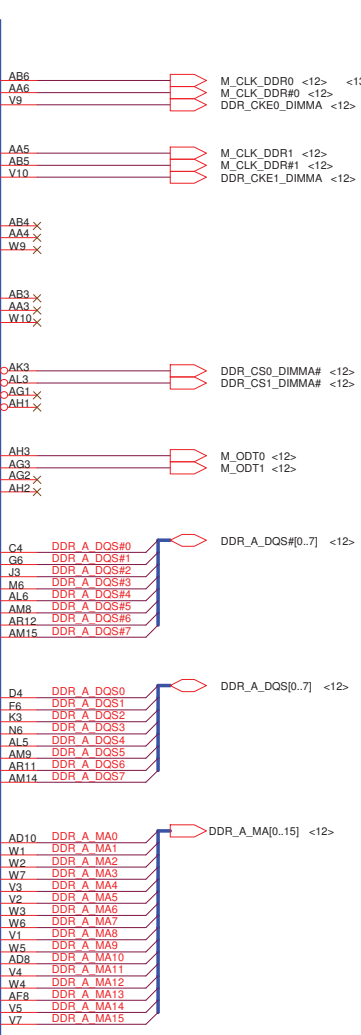
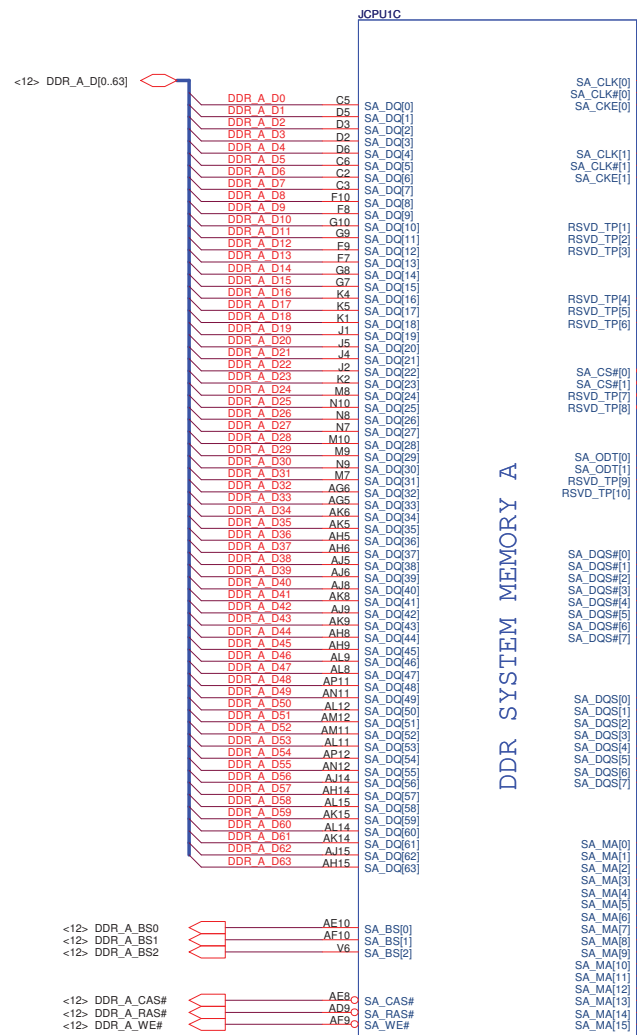
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Compal Electronics, Inc.	
PROCESSOR(I7) DMI,FDI,PEG	
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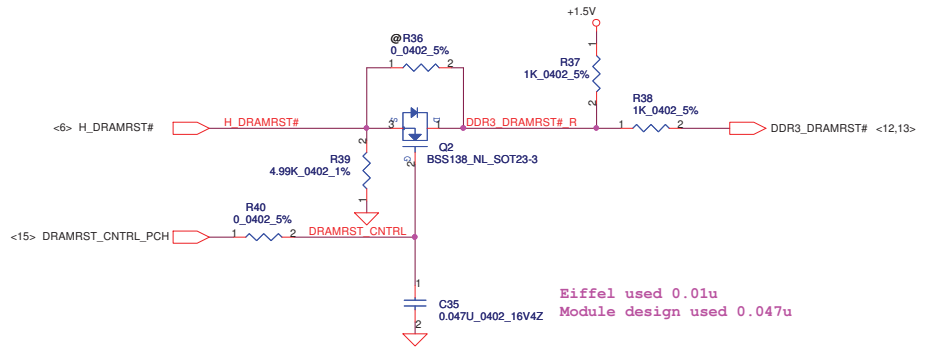


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

Sandy Bridge_rPGA_Rev1p0
ME@

Sandy Bridge_rPGA_Rev1p0
ME@

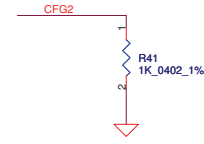
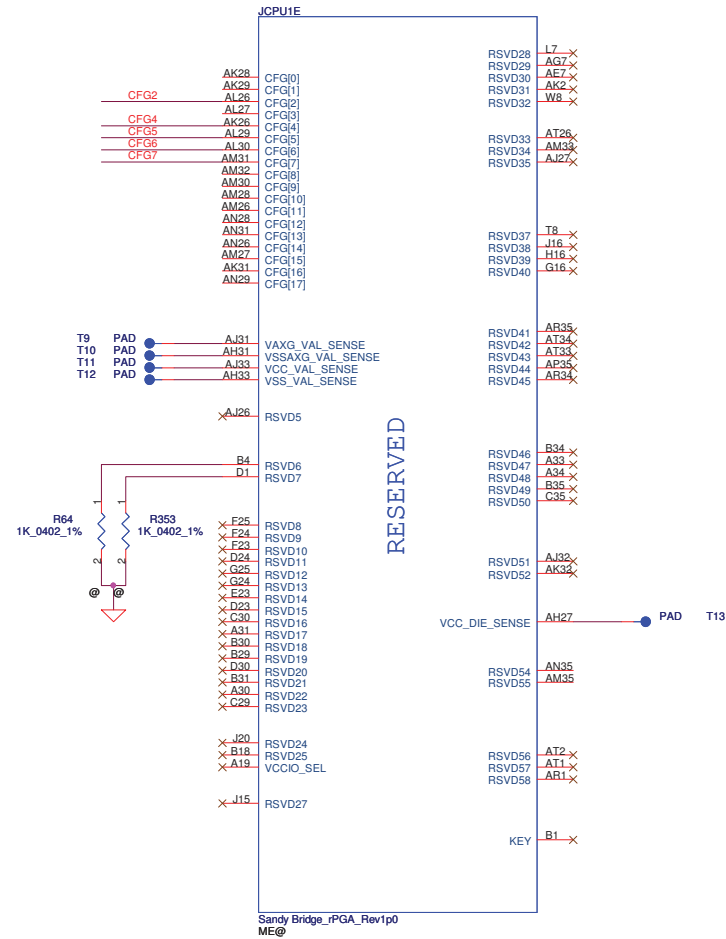


Eiffel used 0.01u
Module design used 0.047u

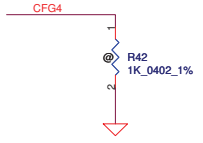
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Title PROCESSOR(3/7) DDRIII		
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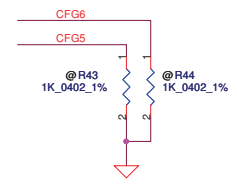
CFG Straps for Processor



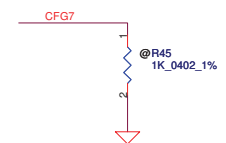
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



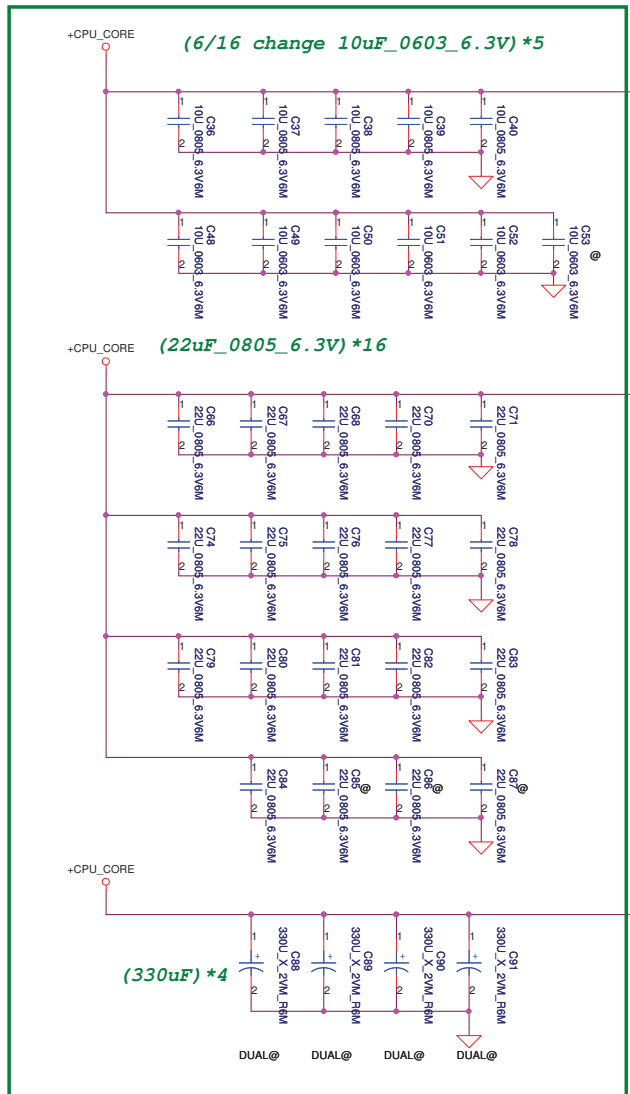
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

POWER

JCPU1F



QC=94A
DC=53A

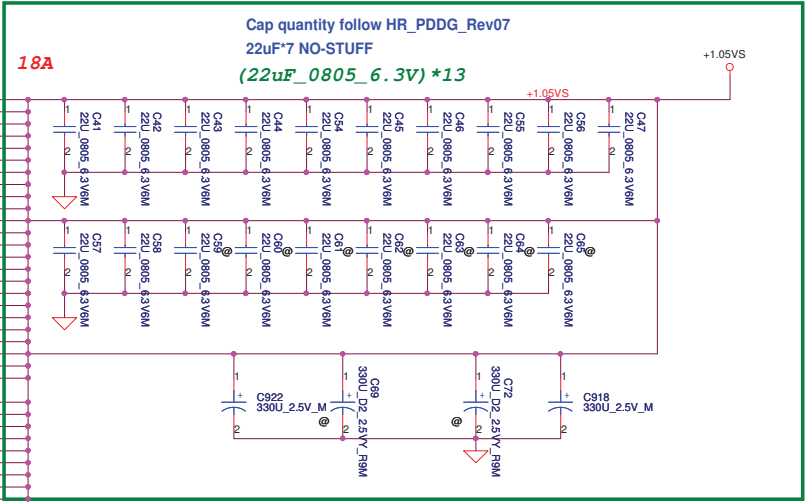
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AF35 VCC9
- AF34 VCC10
- AF33 VCC11
- AF32 VCC12
- AF31 VCC13
- AF30 VCC14
- AF29 VCC15
- AF28 VCC16
- AF27 VCC17
- AF26 VCC18
- AD35 VCC19
- AD34 VCC20
- AD33 VCC21
- AD32 VCC22
- AD31 VCC23
- AD30 VCC24
- AD29 VCC25
- AD28 VCC26
- AD27 VCC27
- AD26 VCC28
- AC35 VCC29
- AC34 VCC30
- AC33 VCC31
- AC32 VCC32
- AC31 VCC33
- AC30 VCC34
- AC29 VCC35
- AA35 VCC36
- AA34 VCC37
- AA33 VCC38
- AA32 VCC39
- AA31 VCC40
- AA30 VCC41
- AA29 VCC42
- AA28 VCC43
- AA27 VCC44
- AA26 VCC45
- Y35 VCC46
- Y34 VCC47
- Y33 VCC48
- Y32 VCC49
- Y31 VCC50
- Y30 VCC51
- Y29 VCC52
- Y28 VCC53
- Y27 VCC54
- Y26 VCC55
- Y25 VCC56
- Y24 VCC57
- Y23 VCC58
- Y22 VCC59
- Y21 VCC60
- Y20 VCC61
- Y19 VCC62
- Y18 VCC63
- Y17 VCC64
- Y16 VCC65
- Y15 VCC66
- Y14 VCC67
- Y13 VCC68
- Y12 VCC69
- Y11 VCC70
- Y10 VCC71
- Y9 VCC72
- Y8 VCC73
- Y7 VCC74
- Y6 VCC75
- Y5 VCC76
- Y4 VCC77
- Y3 VCC78
- Y2 VCC79
- Y1 VCC80
- V35 VCC81
- V34 VCC82
- V33 VCC83
- V32 VCC84
- V31 VCC85
- V30 VCC86
- V29 VCC87
- V28 VCC88
- V27 VCC89
- V26 VCC90
- V25 VCC91
- V24 VCC92
- V23 VCC93
- V22 VCC94
- V21 VCC95
- V20 VCC96
- V19 VCC97
- V18 VCC98
- V17 VCC99
- V16 VCC100

CORE SUPPLY

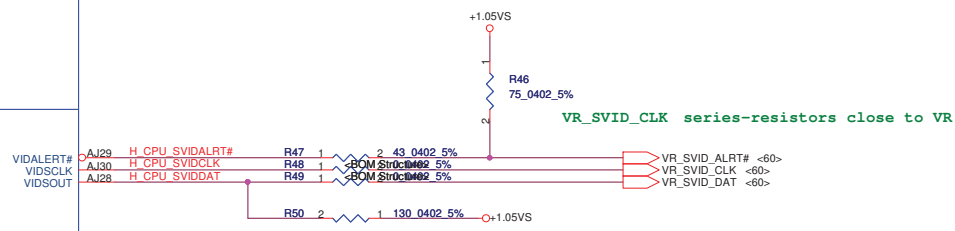
SVID

SENSE LINES

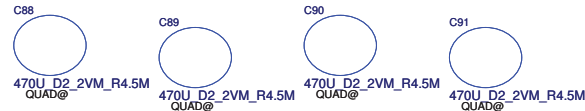
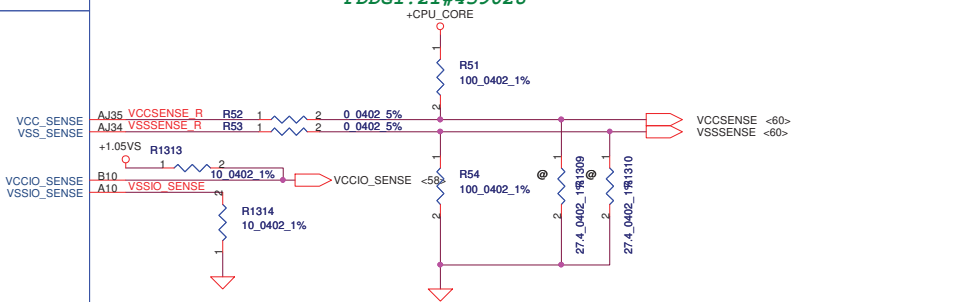
PEG AND DDR



- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AC10
- VCCIO4 Y10
- VCCIO5 Y10
- VCCIO6 U10
- VCCIO7 P10
- VCCIO8 L10
- VCCIO9 J14
- VCCIO10 J13
- VCCIO11 J12
- VCCIO12 J11
- VCCIO13 H14
- VCCIO14 H12
- VCCIO15 H11
- VCCIO16 G14
- VCCIO17 G13
- VCCIO18 G12
- VCCIO19 F14
- VCCIO20 F13
- VCCIO21 F12
- VCCIO22 F11
- VCCIO23 E14
- VCCIO24 E12
- VCCIO25 D14
- VCCIO26 D13
- VCCIO27 D12
- VCCIO28 D11
- VCCIO29 C14
- VCCIO30 C13
- VCCIO31 C12
- VCCIO32 C11
- VCCIO33 B14
- VCCIO34 B12
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- VCCIO37 A13
- VCCIO38 A12
- VCCIO39 A11
- VCCIO40 J23



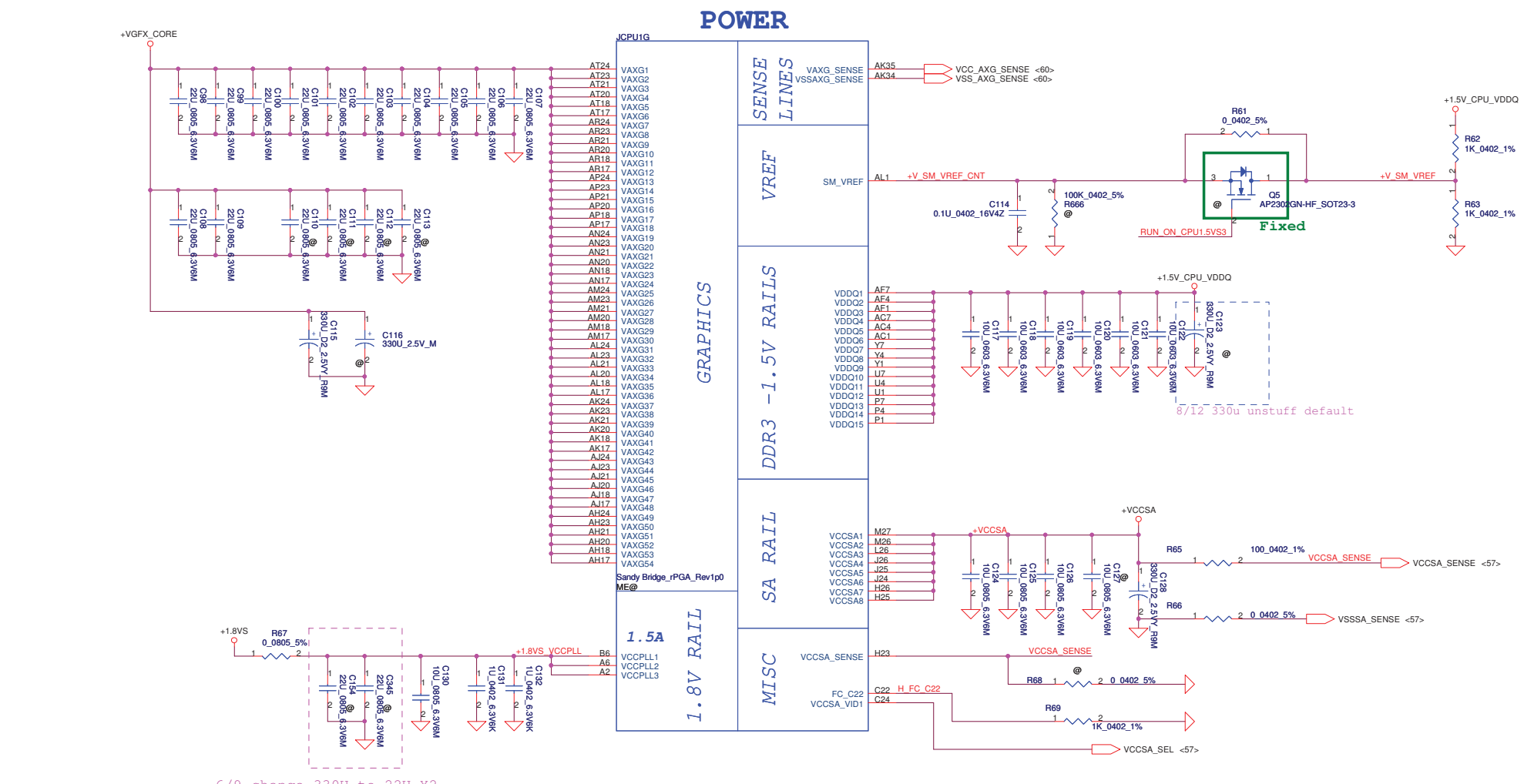
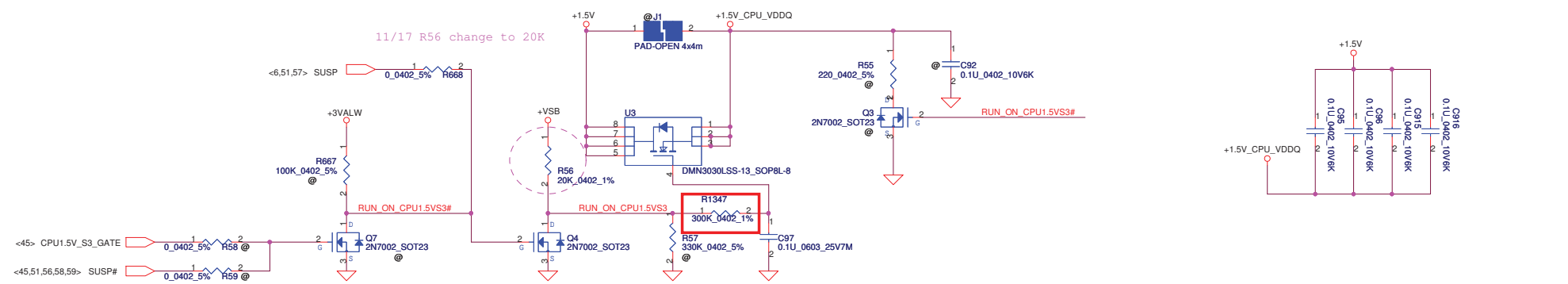
8/11 update: Add R1309, R1310.
PDDG1.21#439028



Sandy Bridge_PGA Rev.1.0
ME@

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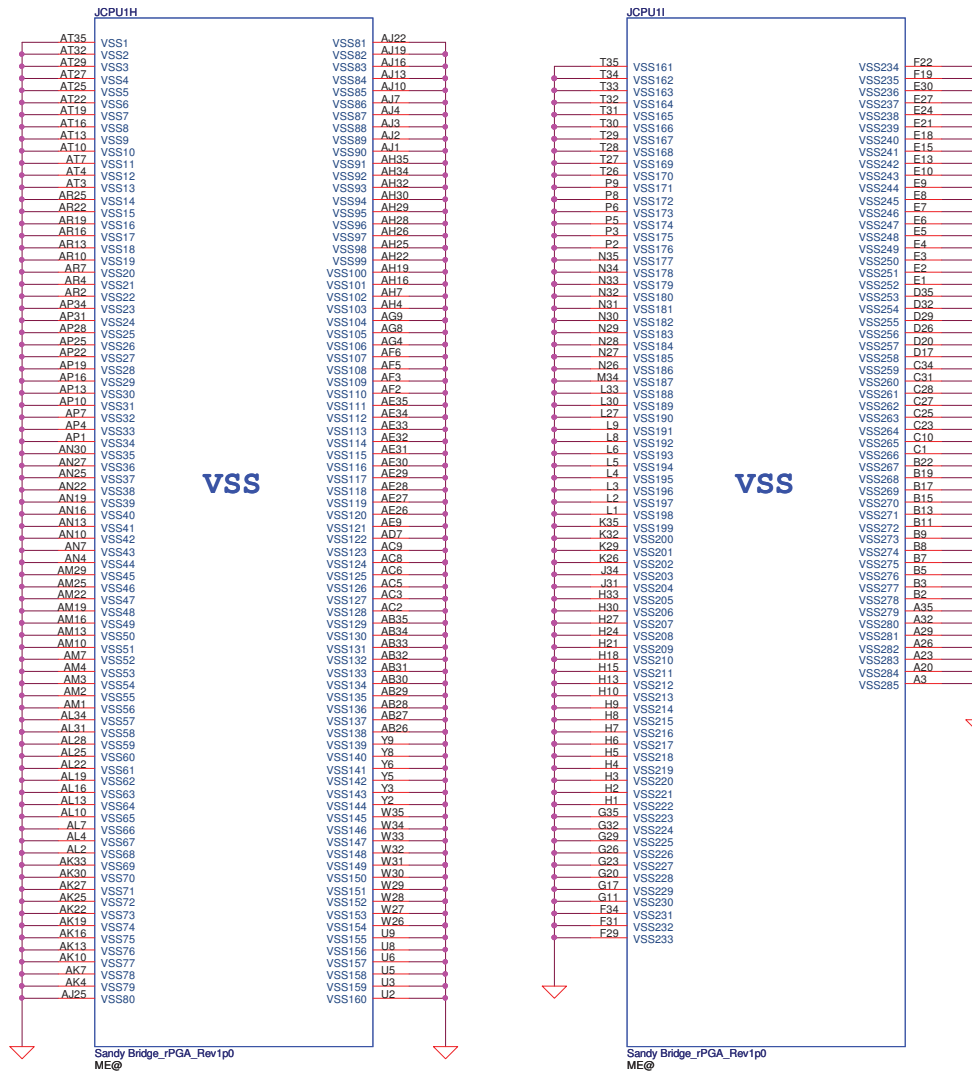
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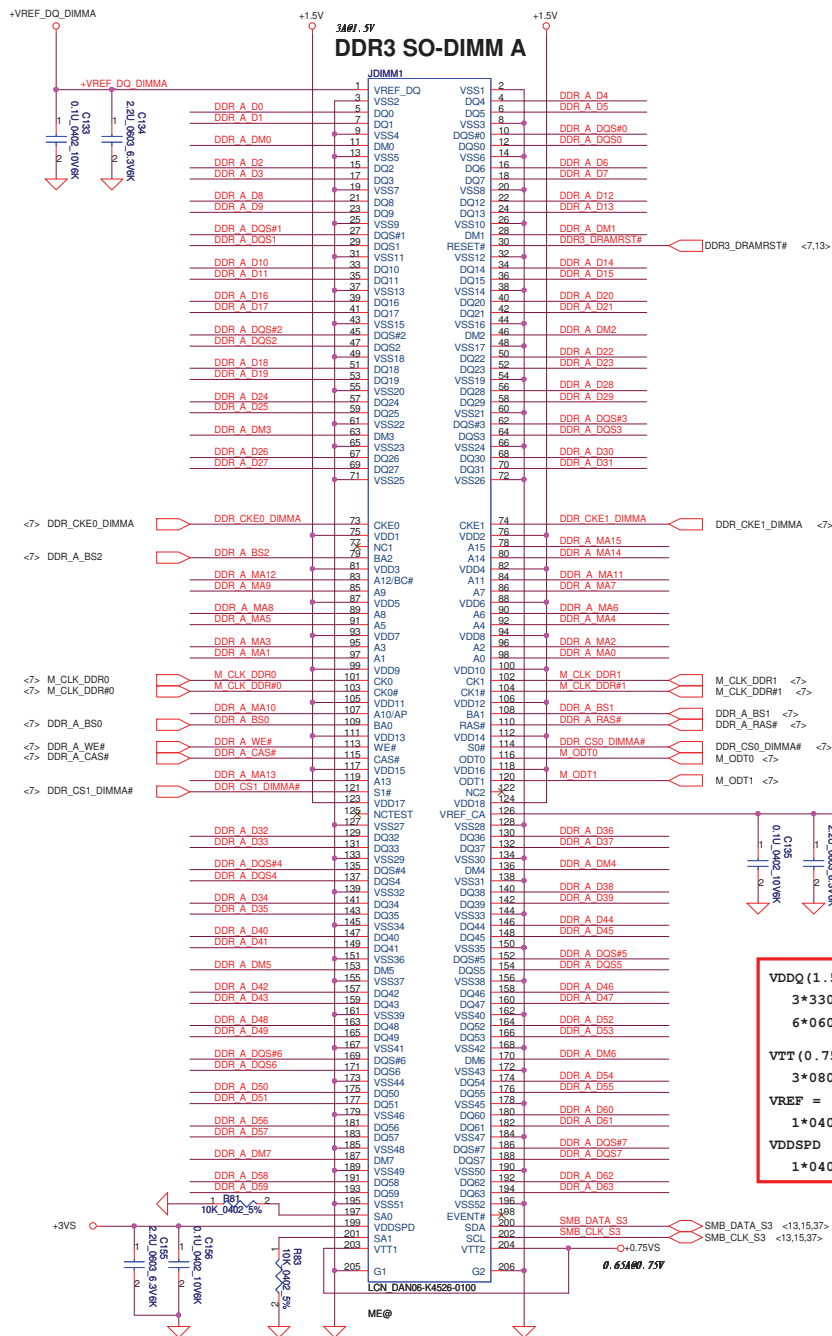
6/9 change 330U to 22U X2

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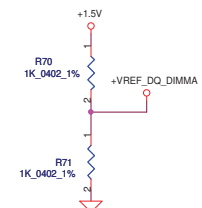
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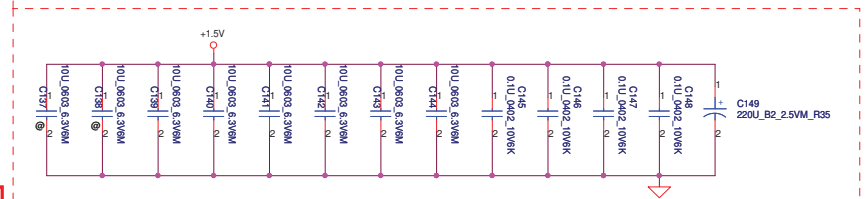


- <7> DDR_A_D[0..63]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_DQS#0..15]
- <7> DDR_A_MAI[0..15]

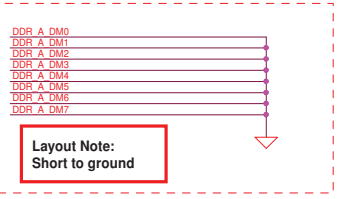
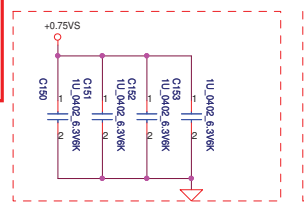


Layout Note:
Place near DIMM

$(10\mu F_{0603_6.3V}) * 8$
 $(0.1\mu F_{402_10V}) * 4$



Layout Note:
Place near DIMM



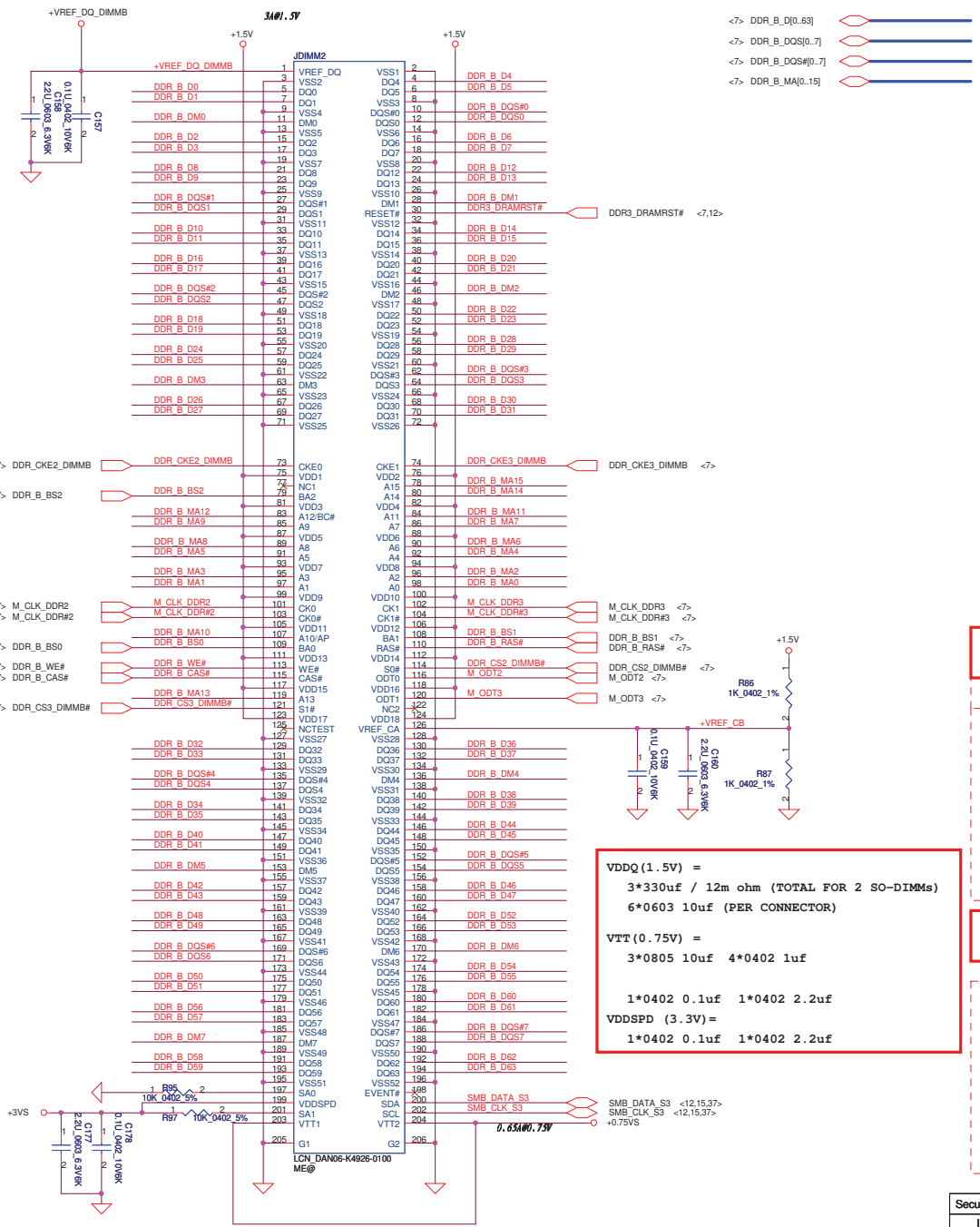
VDDQ (1.5V) =
 $3 * 330\mu f / 12m\ ohm$ (TOTAL FOR 2 SO-DIMMs)
 $6 * 0603\ 10\mu f$ (PER CONNECTOR)

VTT (0.75V) =
 $3 * 0805\ 10\mu f + 4 * 0402\ 1\mu f$

VREF =
 $1 * 0402\ 0.1\mu f + 1 * 0402\ 2.2\mu f$

VDDSPD (3.3V) =
 $1 * 0402\ 0.1\mu f + 1 * 0402\ 2.2\mu f$

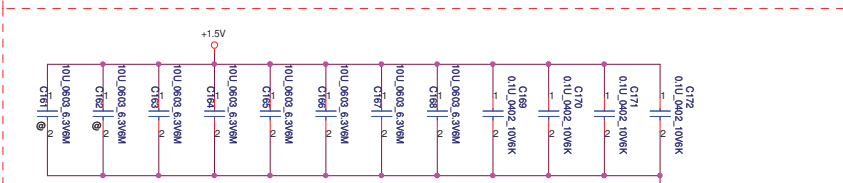
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	DDRIII-SODIMM SLOT1	
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				PIQY0 LA6881P	1.0
Date:	Wednesday, January 05, 2011	Sheet	12	of	63



For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM

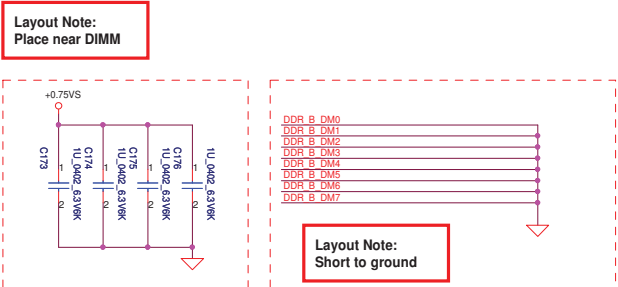
$(10\mu F_{0603_6.3V}) * 8$
 $(0.1\mu F_{402_10V}) * 4$



VDDQ (1.5V) =
 $3 * 330\mu f / 12m\ ohm\ (TOTAL\ FOR\ 2\ SO-DIMMS)$
 $6 * 0603\ 10\mu f\ (PER\ CONNECTOR)$

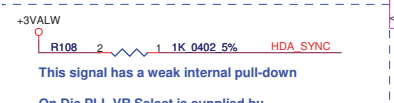
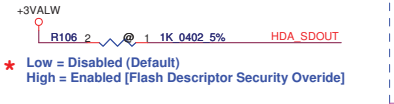
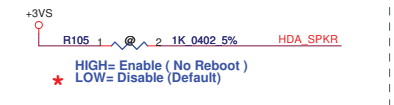
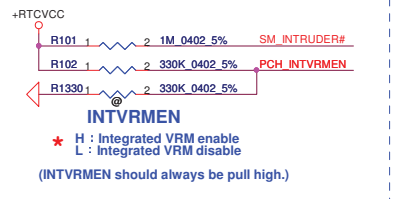
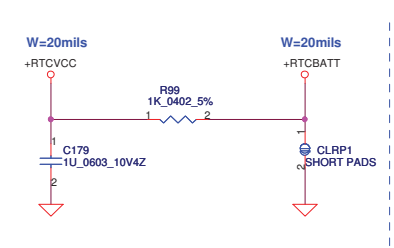
VTI (0.75V) =
 $3 * 0805\ 10\mu f\ 4 * 0402\ 1\mu f$

VDDSPD (3.3V) =
 $1 * 0402\ 0.1\mu f\ 1 * 0402\ 2.2\mu f$
 $1 * 0402\ 0.1\mu f\ 1 * 0402\ 2.2\mu f$

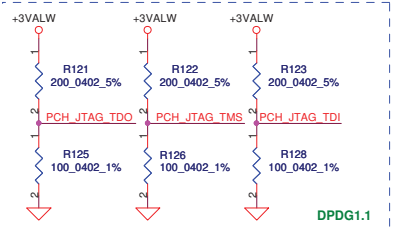
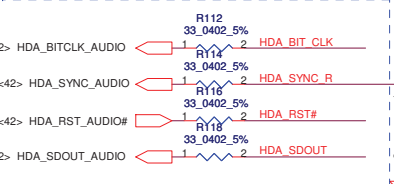


Layout Note:
Short to ground

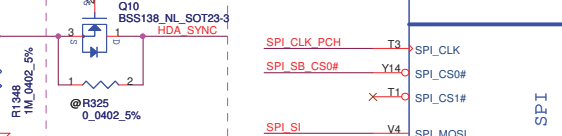
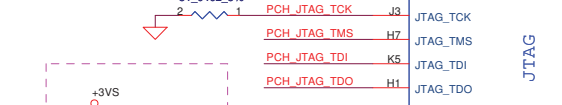
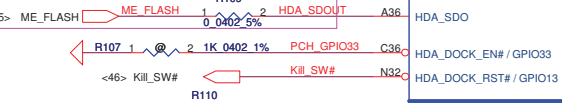
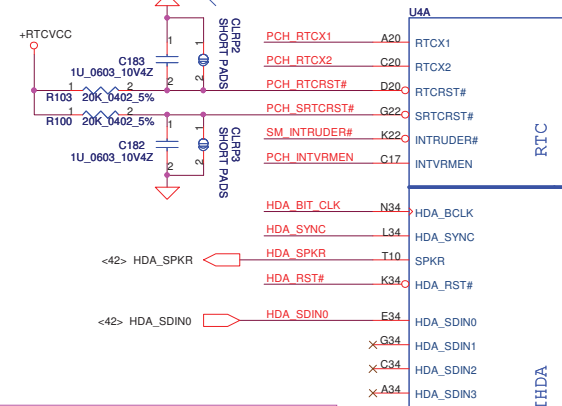
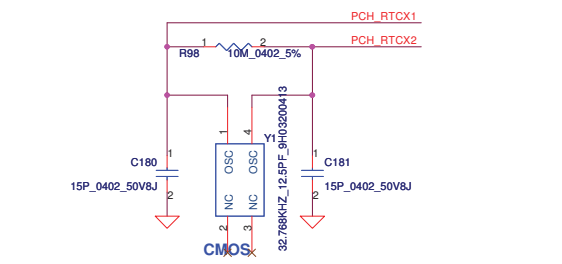
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Date:	Wednesday, January 05, 2011	Sheet	13	of 63



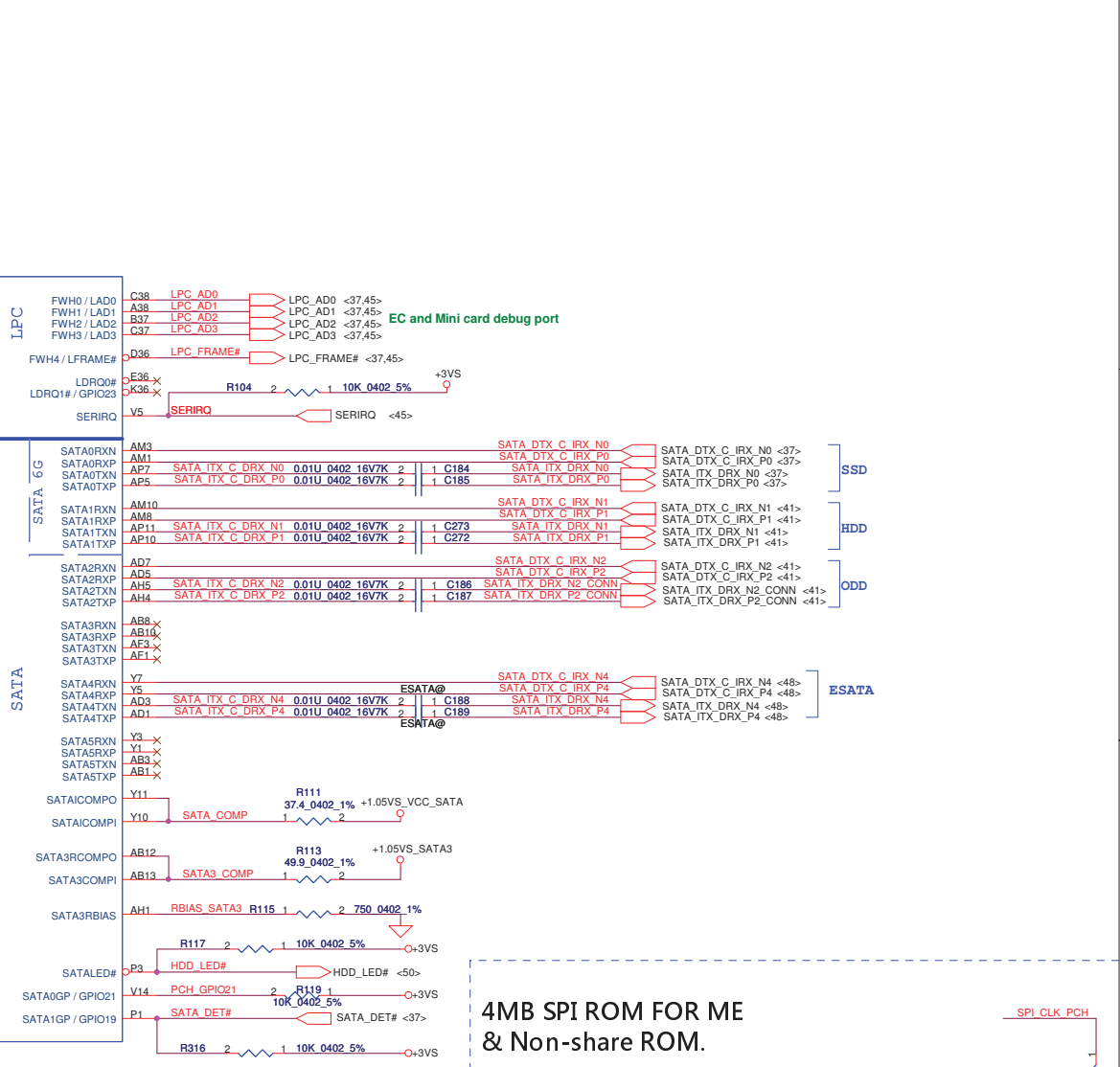
On Die PLL VR Select is supplied by 1.5V when sampled high, 1.8V when sampled low. Needs to be pulled High for Huron River platform.



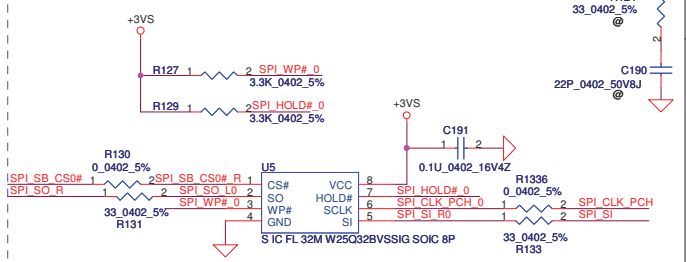
6/30 update R121, R122, R123



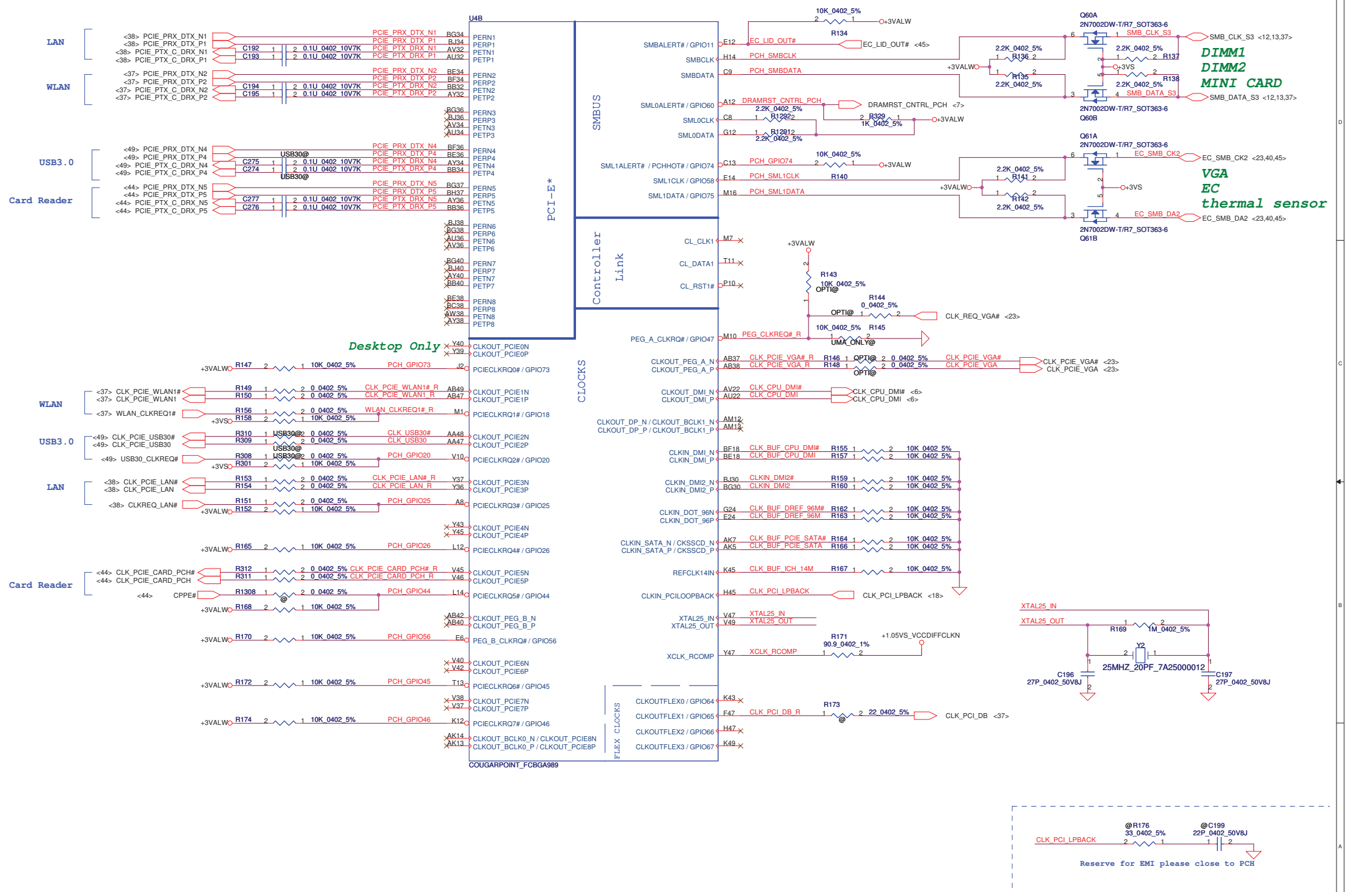
6/17 follow module design



4MB SPI ROM FOR ME & Non-share ROM.

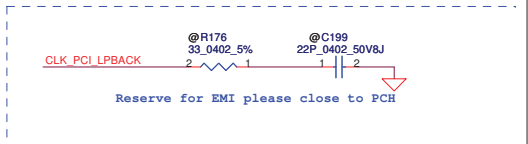


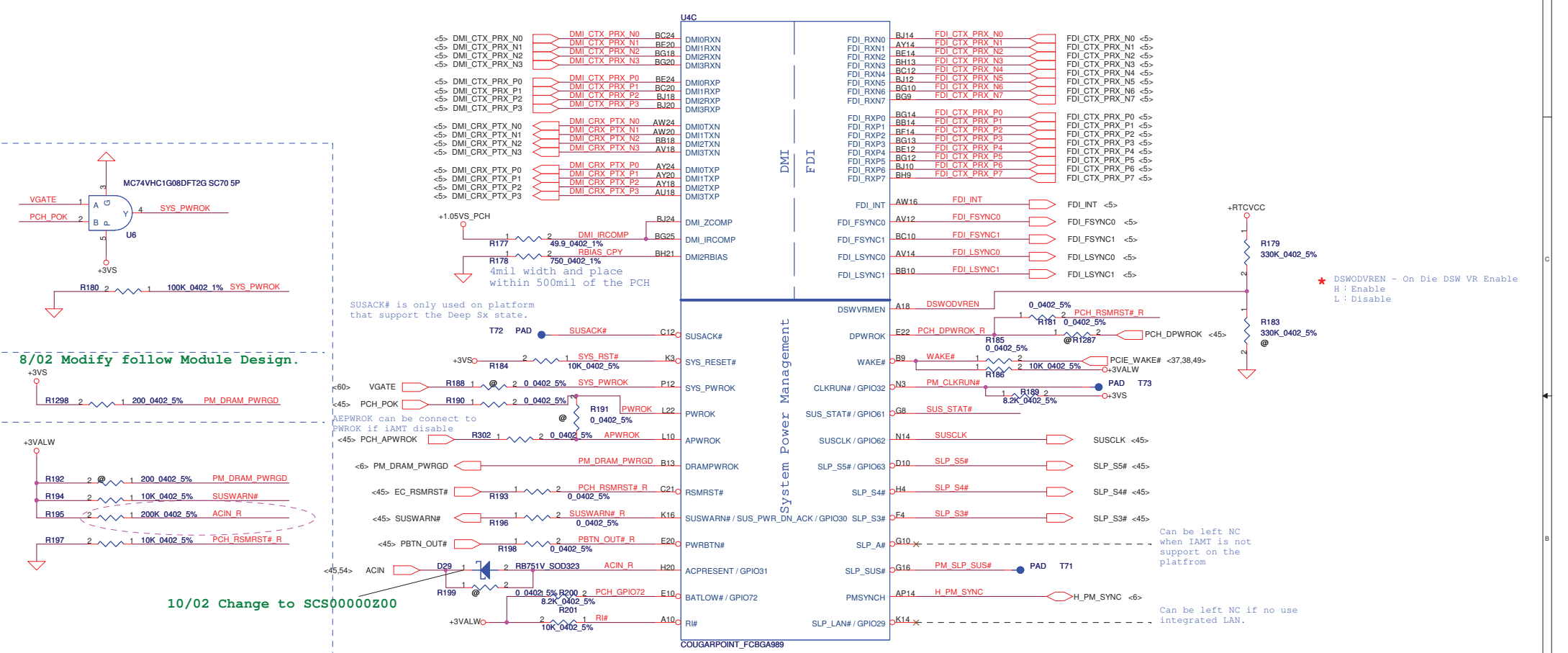
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Issued Date	2010/11/30	Deciphered Date	2011/08	Compal Electronics, Inc.	
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Size	Document Number	Date		Sheet	
Custom	PIQY0 LA6881P	Wednesday, January 05, 2011		14 of 63	
				Rev 1.0	



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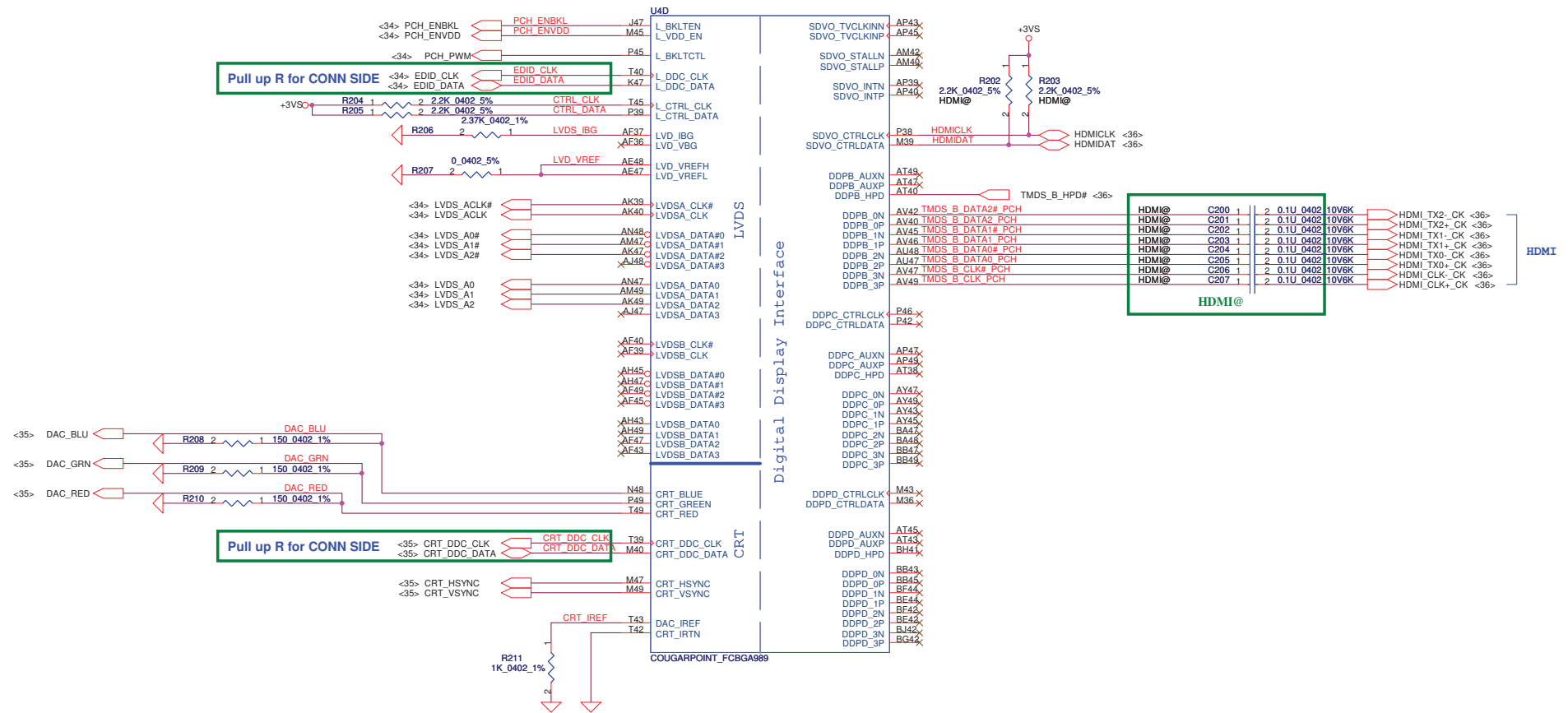
Compal Electronics, Inc.			
PCH (2/8) PCIE, SMBUS, CLK			
Size	Document Number		Rev
Customer	PIQYO LA6881P		1.0
Date:	Wednesday, January 05, 2011	Sheet	15 of 63



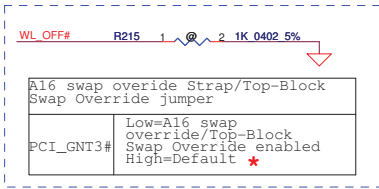
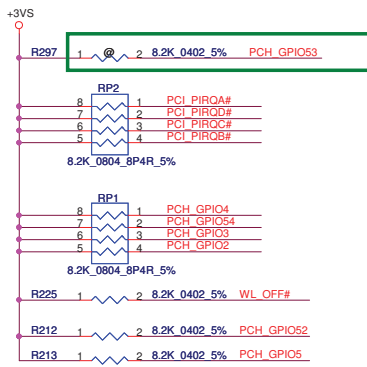


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<p align="right">Compal Electronics, Inc.</p> <p align="center">PCH (3/8) DMI, FDI, PM,</p>			
Size	Document Number	Rev	
Custom	PIQYO LA6881P	1.0	
Date:	Wednesday, January 05, 2011	Sheet	16 of 63

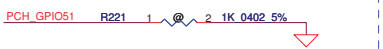


Security Classification	Compal Secret Data			Title				
Issued Date	2010/11/30	Deciphered Date	2011/08	Compal Electronics, Inc.				
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				Size	Document Number	Rev	1.0	
				Customer	PIQYO LA6881P	Date	Wednesday, January 05, 2011	Sheet

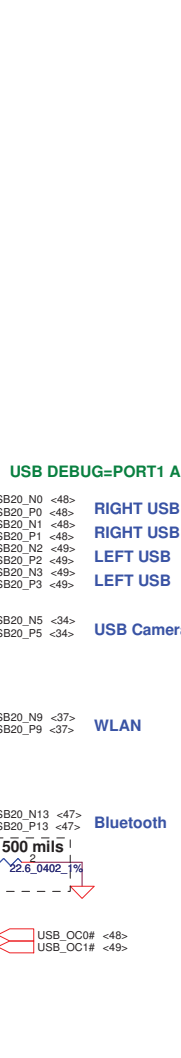
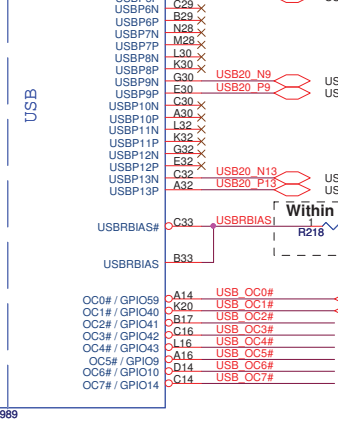
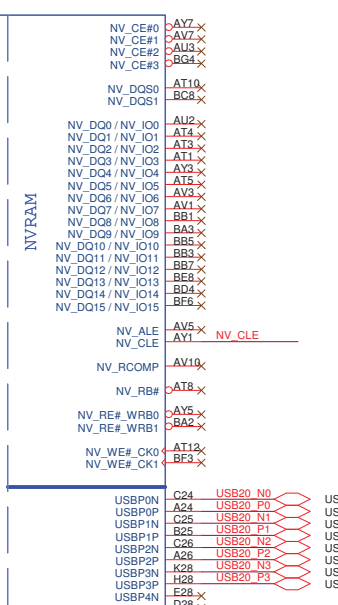
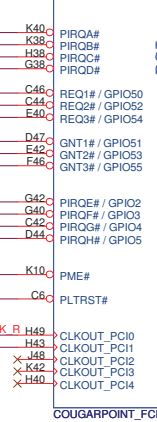


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

GPI053=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
	0	1	Reserved
GNT1#/ GPIO51	1	0	Reserved
	1	1	* SPI (Default)
	0	0	LPC



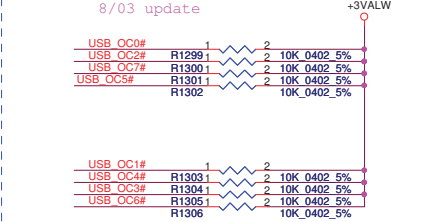
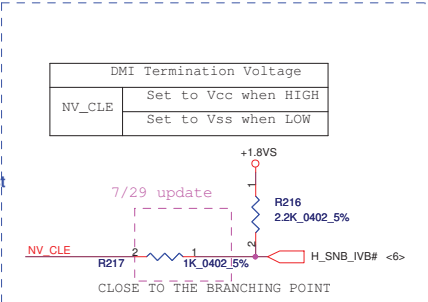
USB DEBUG=PORT1 AND PORT9

- RIGHT USB (CABLE) for SW request
- RIGHT USB (COMBO)
- LEFT USB
- LEFT USB

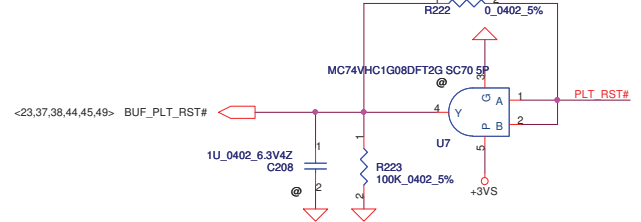
USB Camera

WLAN

Bluetooth



Within 500 mils!
 R216 22.6 0402 5%



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Title		Compal Electronics, Inc.	
PCH (5/9) PCI, USB		PIQY0 LA6881P	
Size	Document Number	Rev	1.0
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6/24 Change to @ follow module design and double check on module design meeting

ICC_EN#
Integrated Clock Chip Enable

H ; Disable
L ; Enable

★ ; Enable

R235 1 @ 2 1K 0402 5% EC_SMI# <37,38,44> DEVICE_RST#

Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator

This signal has a weak internal pull up

H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

★ ; Enable

R240 1 @ 2 1K 0402 5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)

★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 1K 0402 5% PCH_GPIO27

7/29 update for ESATA detect

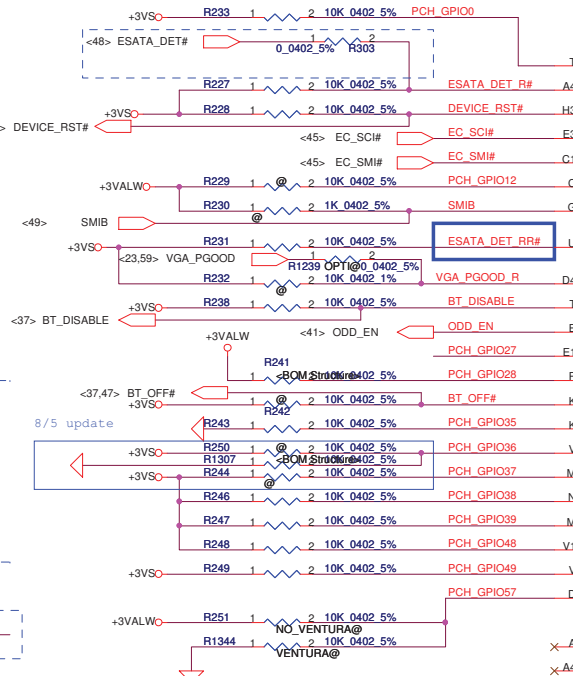
<48> ESATA_DET#

R1294 1 @ 2 0.0402 5% ESATA_DET RR#

0812 Checklist Rev.1.2
When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground.

R1311 1 @ 2 10K 0402 5% PCH_GPIO37

7/29 update for ESATA detect



U4F

BMBUS# / GPIO0	T7
TACH1 / GPIO1	A42
TACH2 / GPIO6	H36
TACH3 / GPIO7	E38
GPIO8	C10
LAN_PHY_PWR_CTRL / GPIO12	C4
GPIO15	G2
SATA4GP / GPIO16	U2
TACH0 / GPIO17	D40
SCLOCK / GPIO22	T5
GPIO24 / MEM_LED	E8
GPIO27	E16
GPIO28	P8
STP_PCIF / GPIO34	K1
GPIO35	K4
SATA2GP / GPIO36	V8
SATA3GP / GPIO37	M5
SLOAD / GPIO38	N2
SDATAOUT0 / GPIO39	M3
SDATAOUT1 / GPIO48	V13
SATA5GP / GPIO49	V3
GPIO57	D6
VSS_NCTF_1	A4
VSS_NCTF_2	A44
VSS_NCTF_3	A45
VSS_NCTF_4	A46
VSS_NCTF_5	A5
VSS_NCTF_6	A6
VSS_NCTF_7	B3
VSS_NCTF_8	B47
VSS_NCTF_9	BD1
VSS_NCTF_10	BD49
VSS_NCTF_11	BE1
VSS_NCTF_12	BE49
VSS_NCTF_13	BF1
VSS_NCTF_14	BE49

COUGARPOINT_FCBGA989

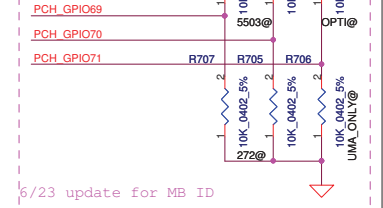
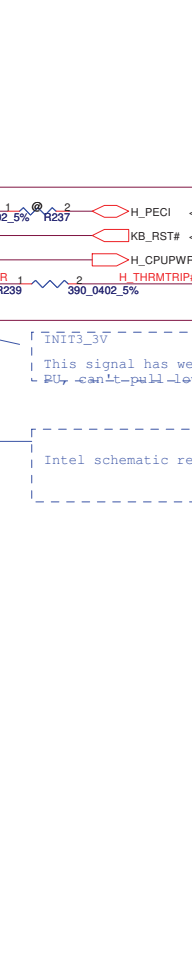
GPIO

CPU/MISC

TACH4 / GPIO68	C40
TACH5 / GPIO69	B41
TACH6 / GPIO70	C41
TACH7 / GPIO71	A40
A20GATE	P4
PECI	AU16
RCIN#	P5
PROCPWRGD	AY11
THRMTTRIP#	AY10
INIT3_3V#	T14
NC_1	AH8
NC_2	AK11
NC_3	AH10
NC_4	AK10
NC_5	P37
VSS_NCTF_15	BG2
VSS_NCTF_16	BG48
VSS_NCTF_17	BH3
VSS_NCTF_18	BH47
VSS_NCTF_19	BJ4
VSS_NCTF_20	BJ44
VSS_NCTF_21	BJ45
VSS_NCTF_22	BJ46
VSS_NCTF_23	BJ5
VSS_NCTF_24	BJ6
VSS_NCTF_25	C2
VSS_NCTF_26	C48
VSS_NCTF_27	D1
VSS_NCTF_28	D49
VSS_NCTF_29	E1
VSS_NCTF_30	E49
VSS_NCTF_31	F1
VSS_NCTF_32	F49

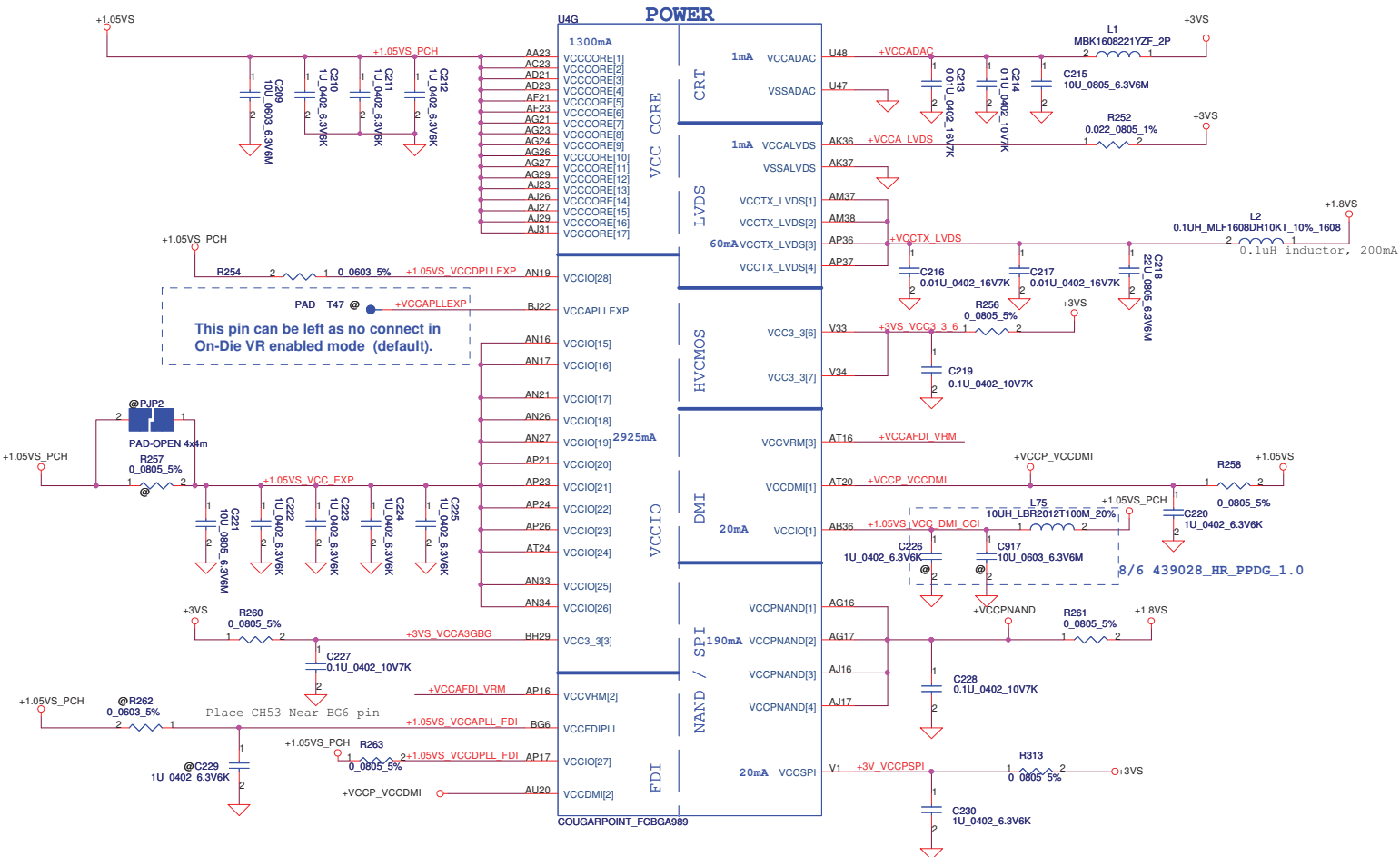
NCTF

PCH_GPIO68	C40
PCH_GPIO69	B41
PCH_GPIO70	C41
PCH_GPIO71	A40
PCH_PECI_R	AU16
KB_RST#	P5
PCH_THRMTRIP#_R	AY10
H_THRMTRIP#	AY10
H_THRMTRIP#_R	T14
AH8	AH8
AK11	AK11
AH10	AH10
AK10	AK10
BG2	BG2
BG48	BG48
BH3	BH3
BH47	BH47
BJ4	BJ4
BJ44	BJ44
BJ45	BJ45
BJ46	BJ46
BJ5	BJ5
BJ6	BJ6
C2	C2
C48	C48
D1	D1
D49	D49
E1	E1
E49	E49
F1	F1
F49	F49



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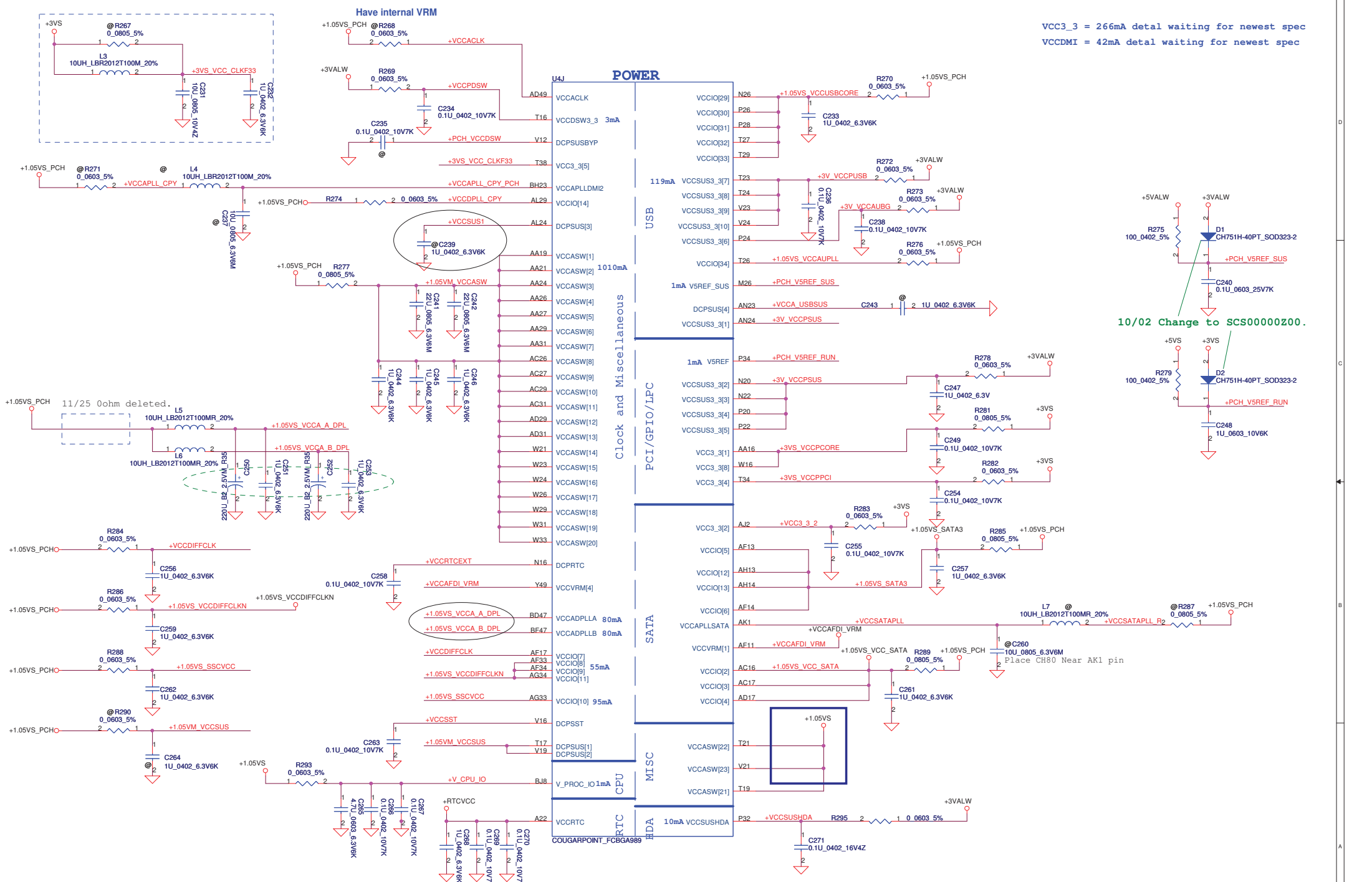
Compal Electronics, Inc.		
Title PCH (6/9) GPIO, CPU, MISC		
Size	Document Number PIQYO LA6881P	Rev 1.0
Date	Wednesday, January 05, 2011	Sheet 19 of 63



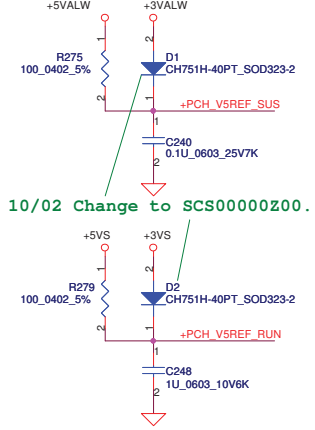
This pin can be left as no connect in On-Die VR enabled mode (default).

+1.5VS +VCCAFDL_VRM
 R265 2 0.0603 5% +VCCAFDI_VRM
 Intel HR_PDDG_1.21
 1.5S rail. Default is to populate to enable VccVRM.
 VCCVRM = 160mA detail waiting for newest spec

PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

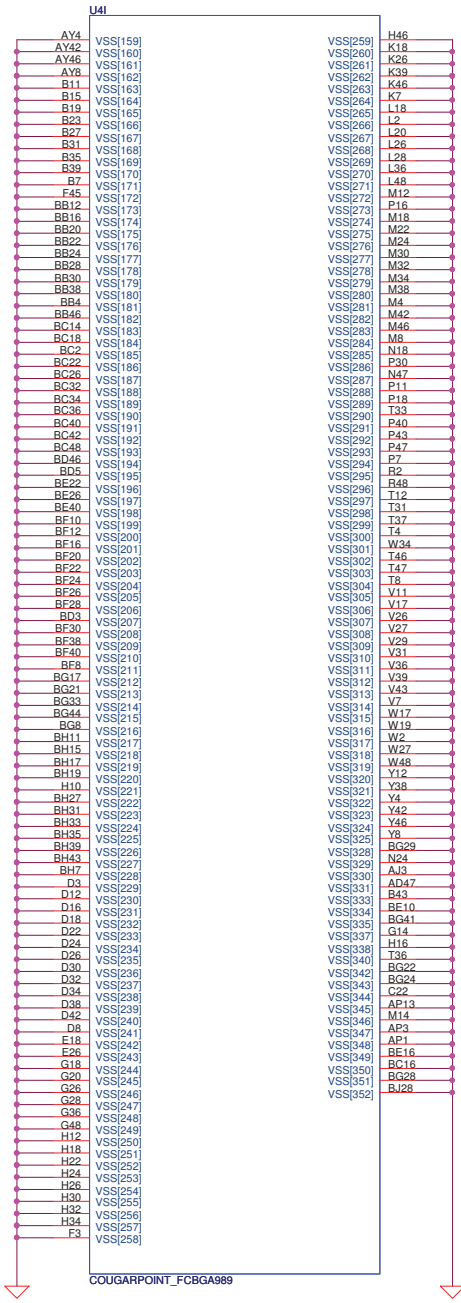
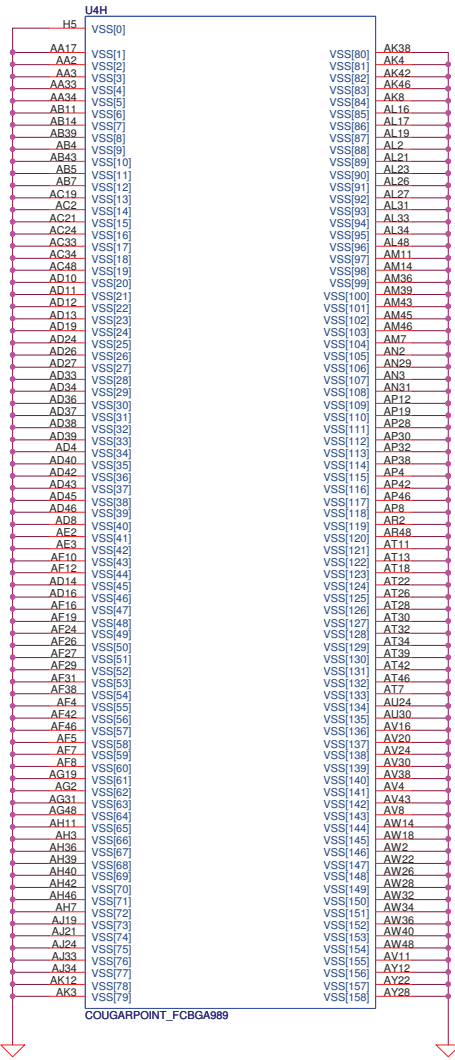


VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

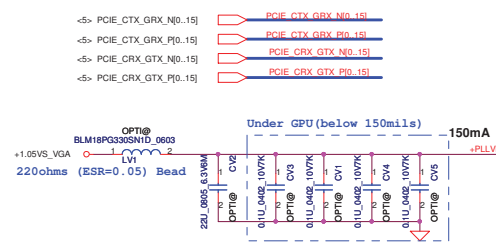


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Title			PCH (8/9) PWR	
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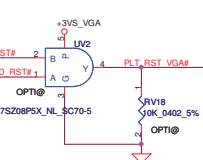


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				Date:	Wednesday, January 05, 2011 Sheet 22 of 63

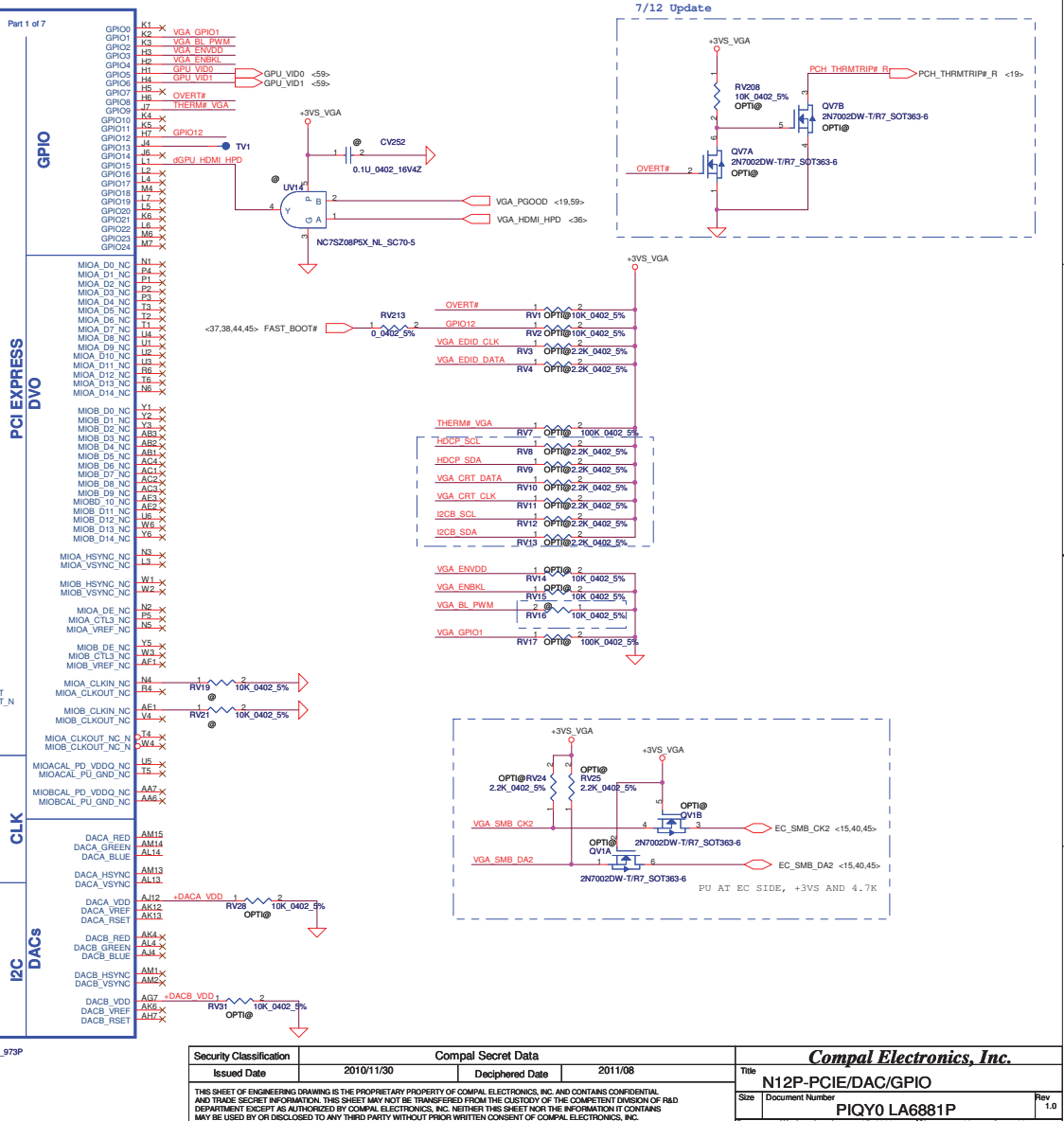
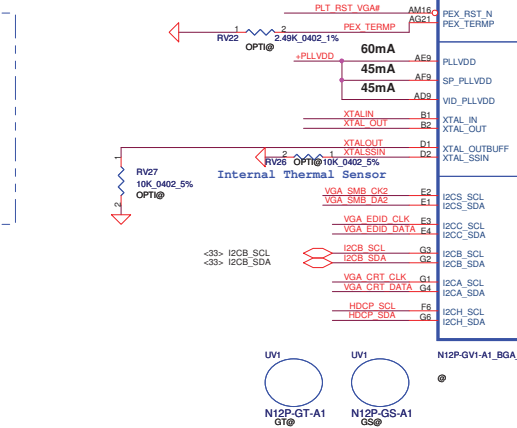
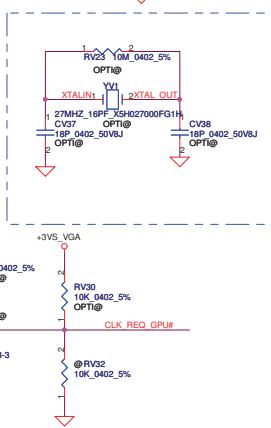


PCIE CTX GRX P0	AP17	PCIE CTX GRX N0	AN17
PCIE CTX GRX P1	AP19	PCIE CTX GRX N1	AN19
PCIE CTX GRX P2	AP19	PCIE CTX GRX N2	AN19
PCIE CTX GRX P3	AP20	PCIE CTX GRX N3	AN20
PCIE CTX GRX P4	AP22	PCIE CTX GRX N4	AN22
PCIE CTX GRX P5	AP22	PCIE CTX GRX N5	AN22
PCIE CTX GRX P6	AP23	PCIE CTX GRX N6	AN23
PCIE CTX GRX P7	AP25	PCIE CTX GRX N7	AN25
PCIE CTX GRX P8	AP25	PCIE CTX GRX N8	AN25
PCIE CTX GRX P9	AP26	PCIE CTX GRX N9	AN26
PCIE CTX GRX P10	AP26	PCIE CTX GRX N10	AN26
PCIE CTX GRX P11	AP28	PCIE CTX GRX N11	AN28
PCIE CTX GRX P12	AP29	PCIE CTX GRX N12	AN29
PCIE CTX GRX P13	AP31	PCIE CTX GRX N13	AN31
PCIE CTX GRX P14	AP32	PCIE CTX GRX N14	AN32
PCIE CTX GRX P15	AP34	PCIE CTX GRX N15	AN34

PCIE CRX GTX P0	CV8	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P0	AL17	PEX TX0
PCIE CRX GTX P1	CV9	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P1	AL19	PEX TX1
PCIE CRX GTX P2	CV10	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P2	AL19	PEX TX2
PCIE CRX GTX P3	CV11	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P3	AL20	PEX TX3
PCIE CRX GTX P4	CV14	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P4	AL21	PEX TX4
PCIE CRX GTX P5	CV16	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P5	AL22	PEX TX5
PCIE CRX GTX P6	CV17	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P6	AL23	PEX TX6
PCIE CRX GTX P7	CV18	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P7	AL23	PEX TX7
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PCIE CRX GTX P9	CV21	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P9	AL25	PEX TX9
PCIE CRX GTX P10	CV22	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P10	AL26	PEX TX10
PCIE CRX GTX P11	CV24	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P11	AL28	PEX TX11
PCIE CRX GTX P12	CV26	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P12	AL29	PEX TX12
PCIE CRX GTX P13	CV29	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P13	AL30	PEX TX13
PCIE CRX GTX P14	CV33	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P14	AL31	PEX TX14
PCIE CRX GTX P15	CV35	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX P15	AL32	PEX TX15
PCIE CRX GTX N15	CV36	OPTI@	1	2	0.1U	0402	10V8K	PCIE CRX C GTX N15	AP33	PEX TX15_N



Differential signal, Default can be unstaffed.

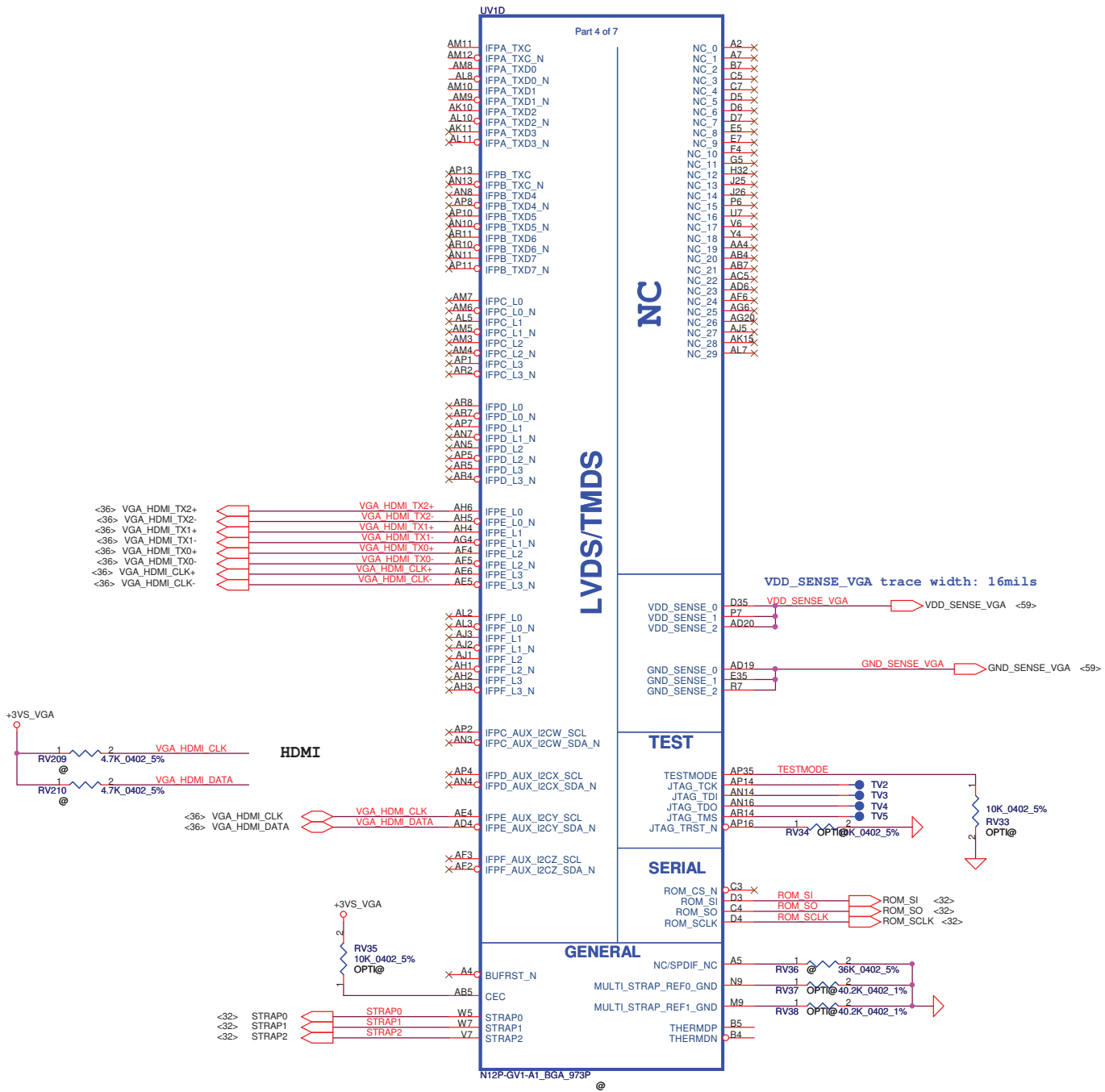


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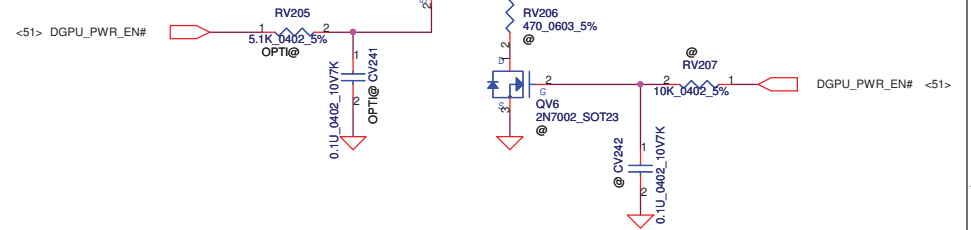
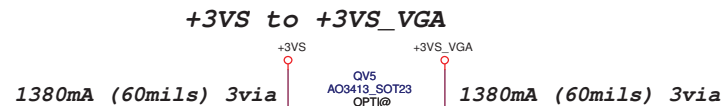
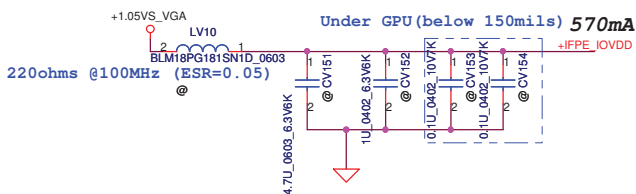
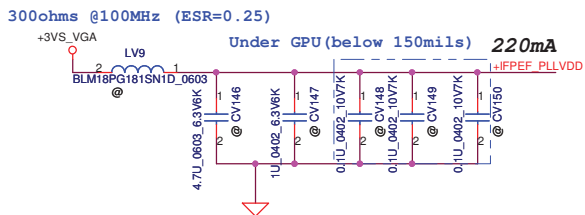
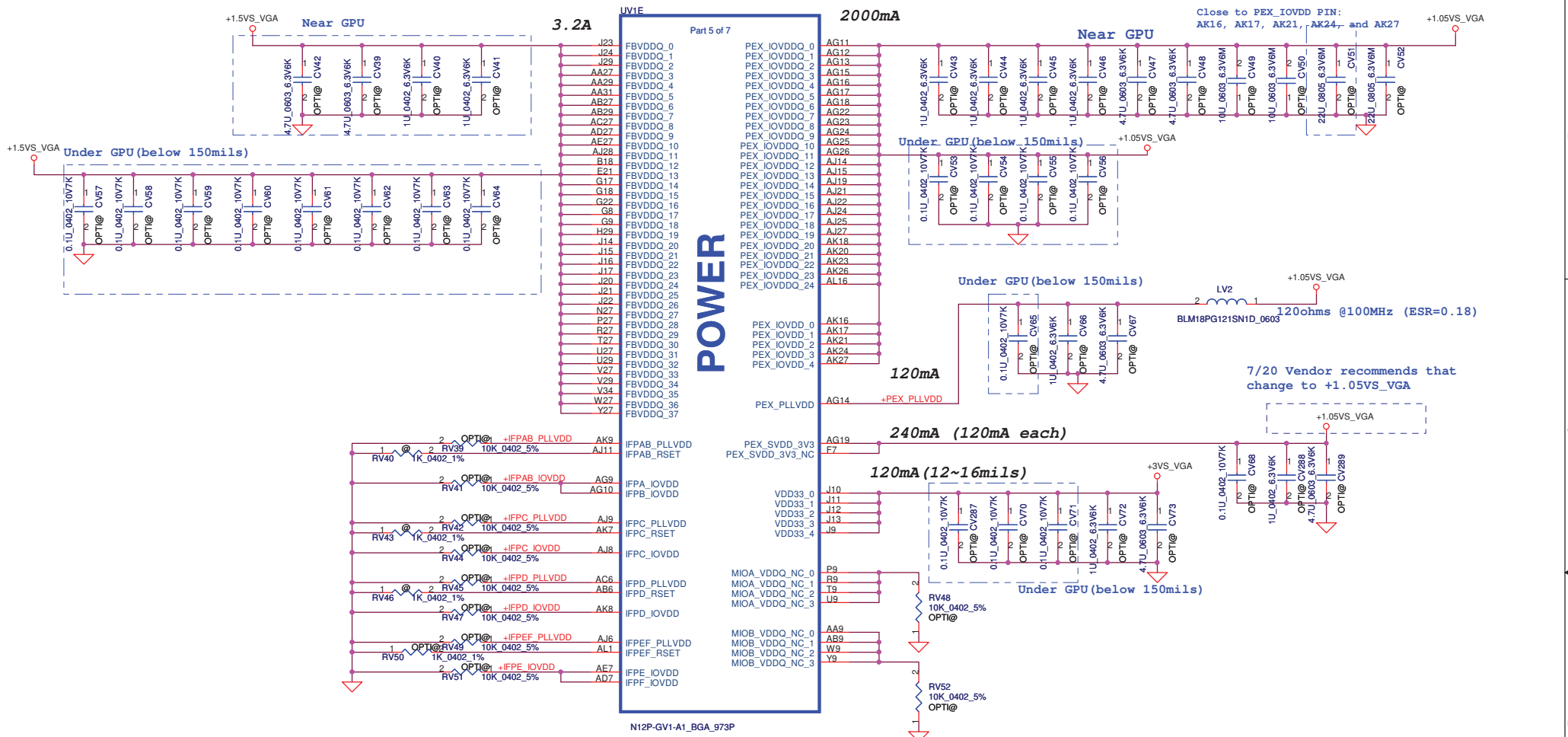
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Rev: **1.0**



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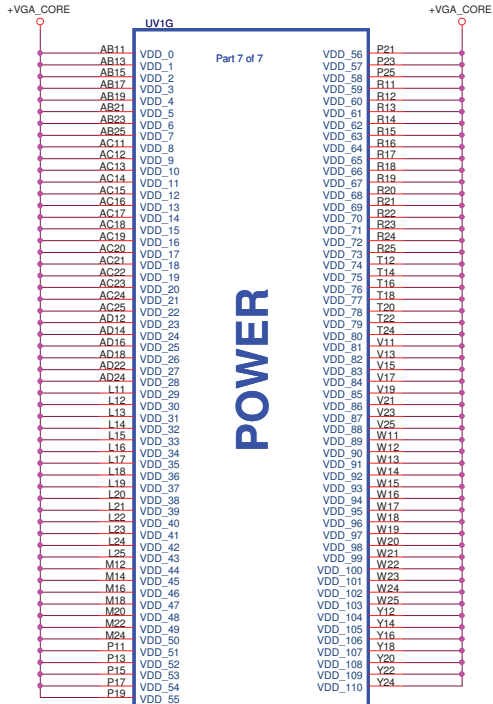
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Title N12P-LVDS/HDMI/DP/THM		
Size	Document Number PIQY0 LA6881P	Rev 1.0
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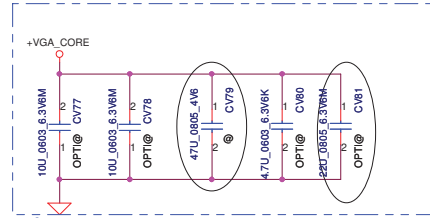
Compal Electronics, Inc.		
Title		
N12P-POWER		
Size	Document Number	Rev
	PIQY0 LA6881P	1.0
Date:	Wednesday, January 05, 2011	Sheet 25 of 63

30.54A (41.02A Peak)

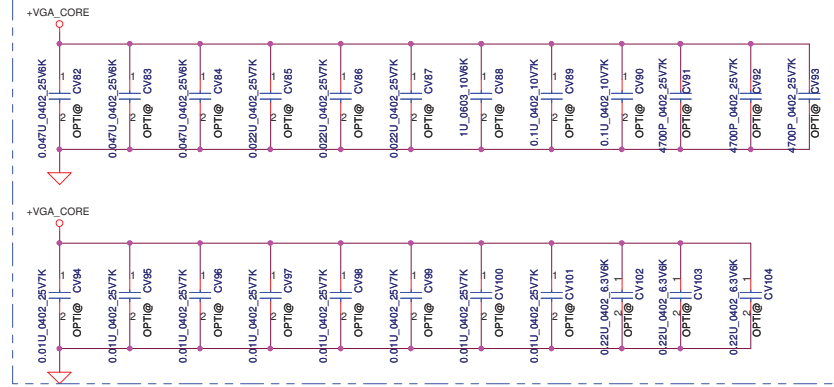


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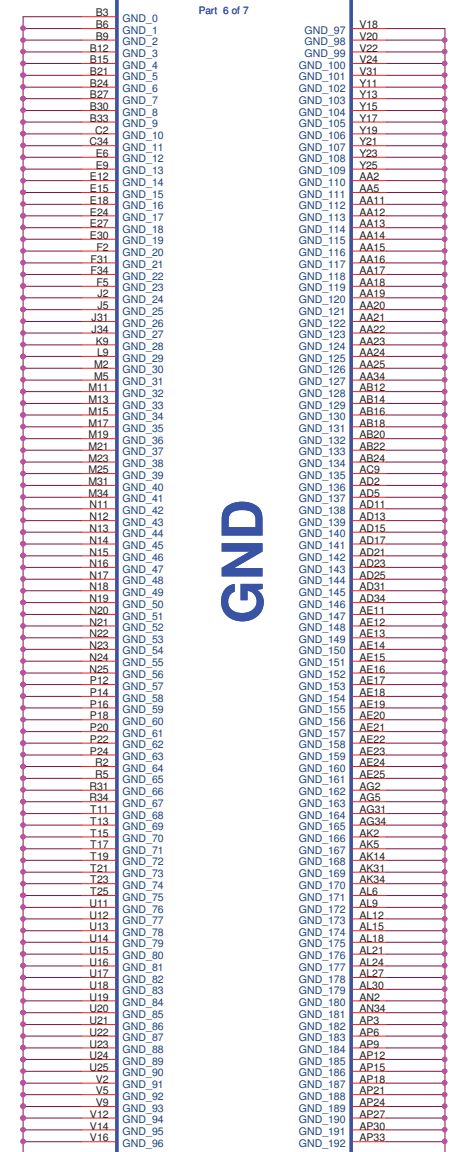
Near GPU



Under GPU

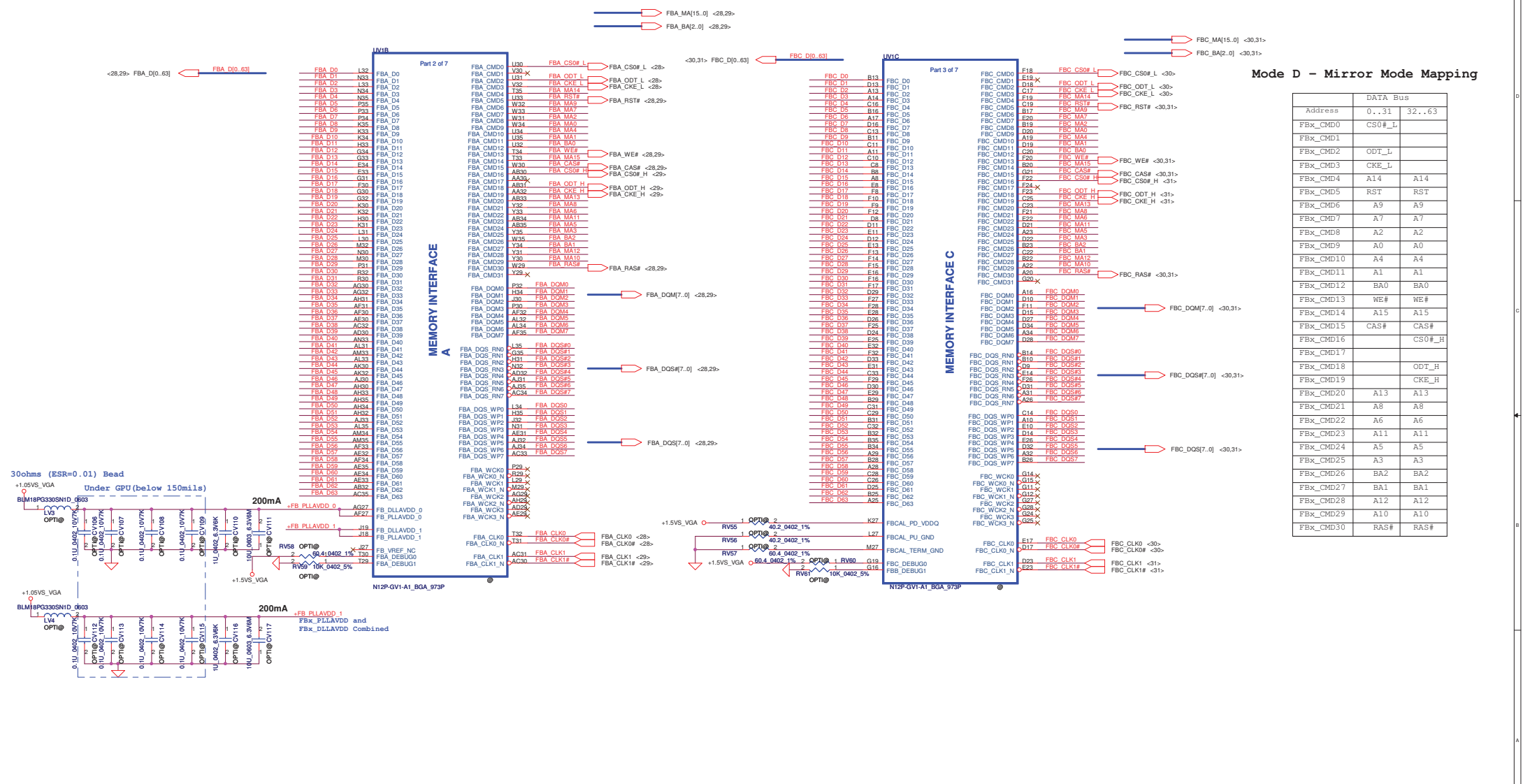


UVIF



N12P-GV1-A1_BGA_973P

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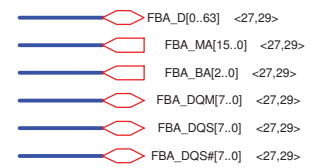


Mode D - Mirror Mode Mapping

Address	DATA Bus
0..31	32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

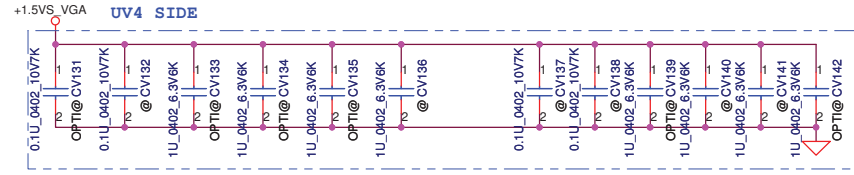
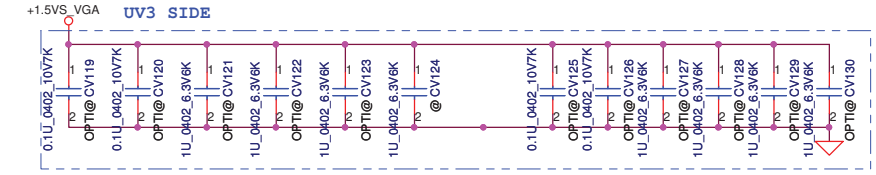
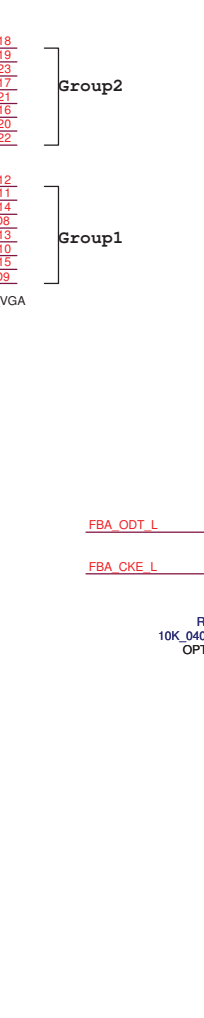
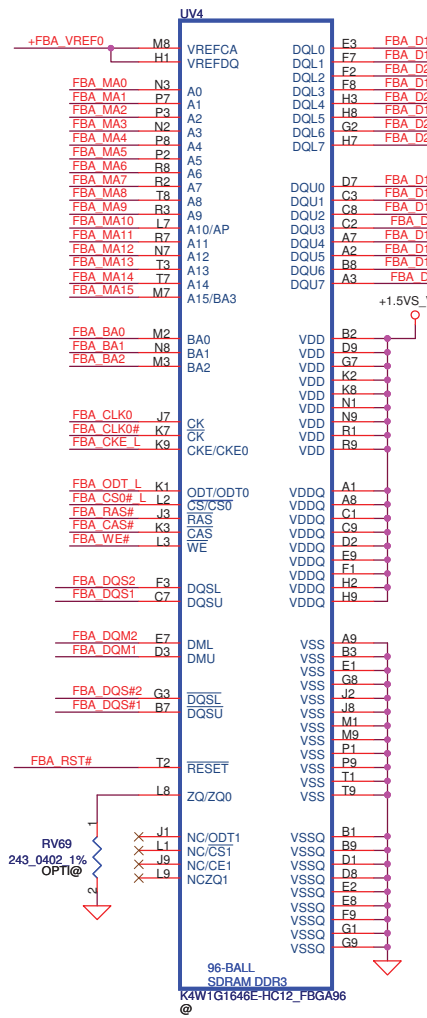
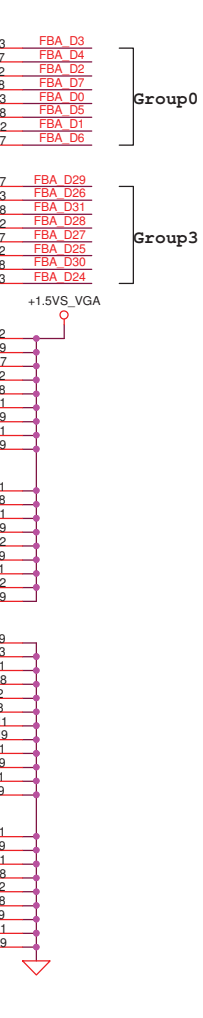
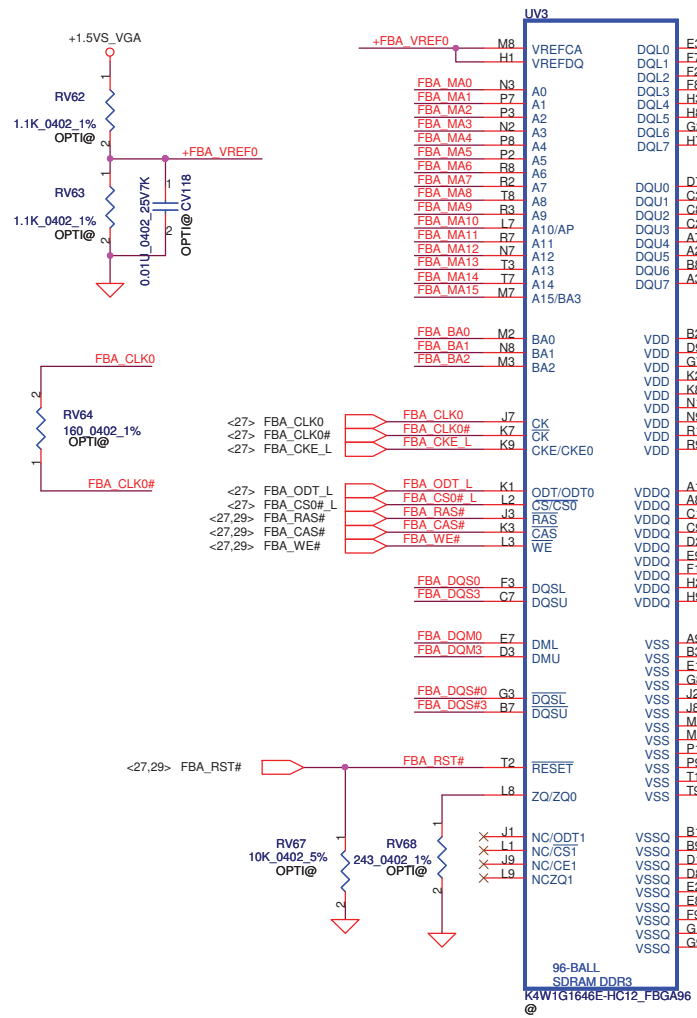
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Memory Partition A - Lower 32 bits



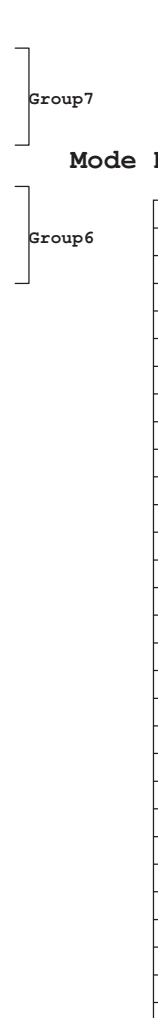
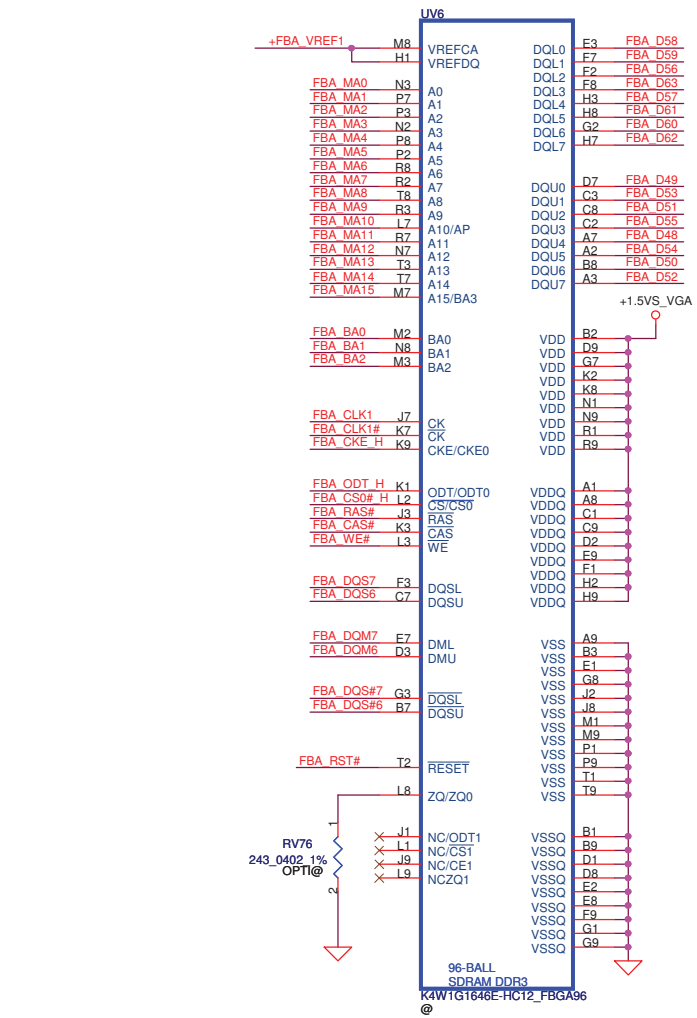
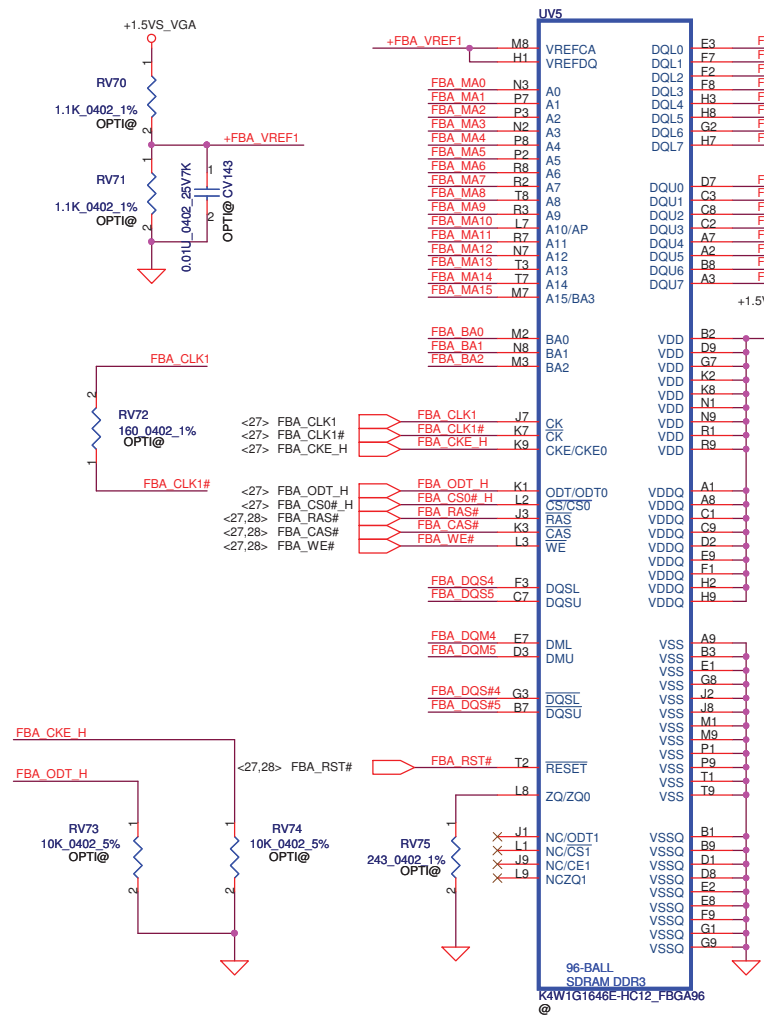
Mode D - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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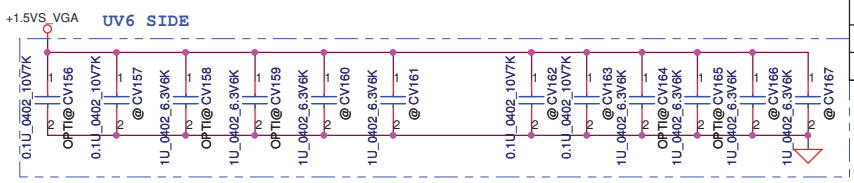
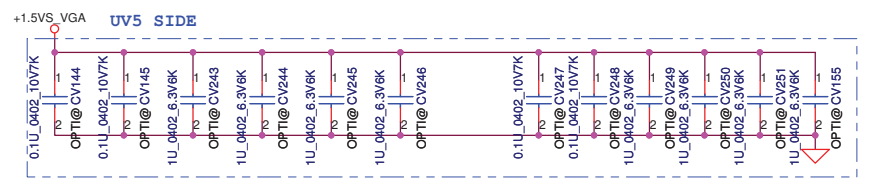
Memory Partition A - Upper 32 bits



- FBA_D[0..63] <27..28>
- FBA_MA[15..0] <27..28>
- FBA_BA[2..0] <27..28>
- FBA_DOM[7..0] <27..28>
- FBA_DQS[7..0] <27..28>
- FBA_DQS#[7..0] <27..28>

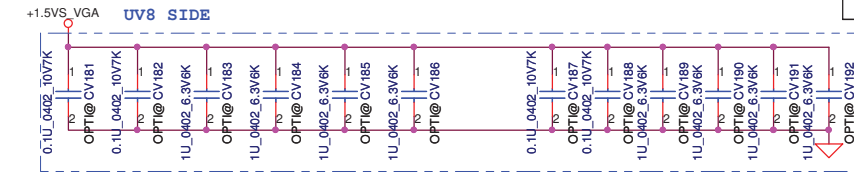
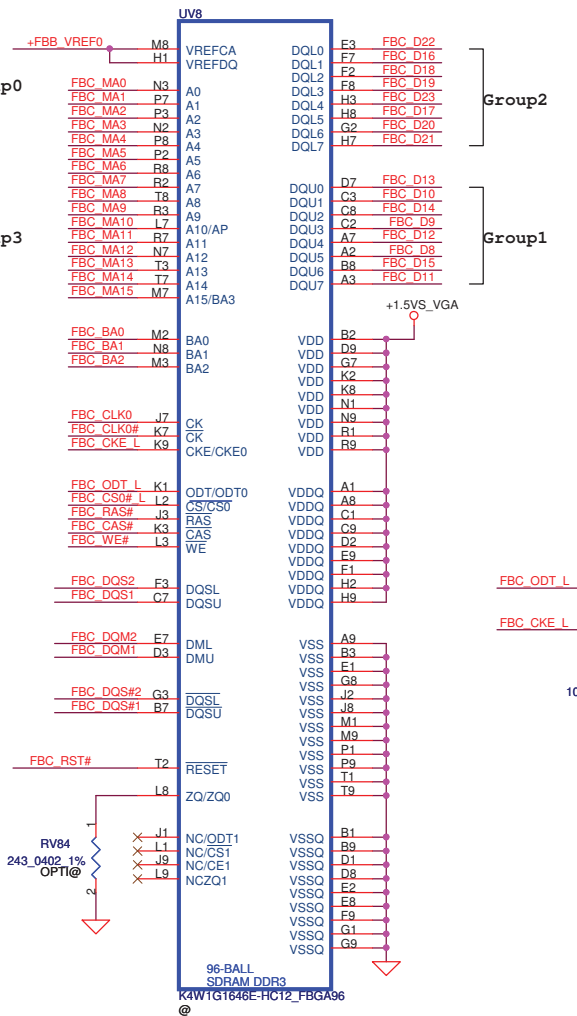
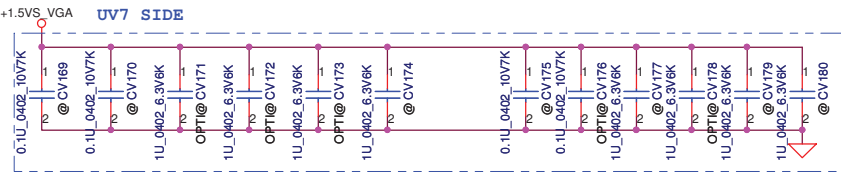
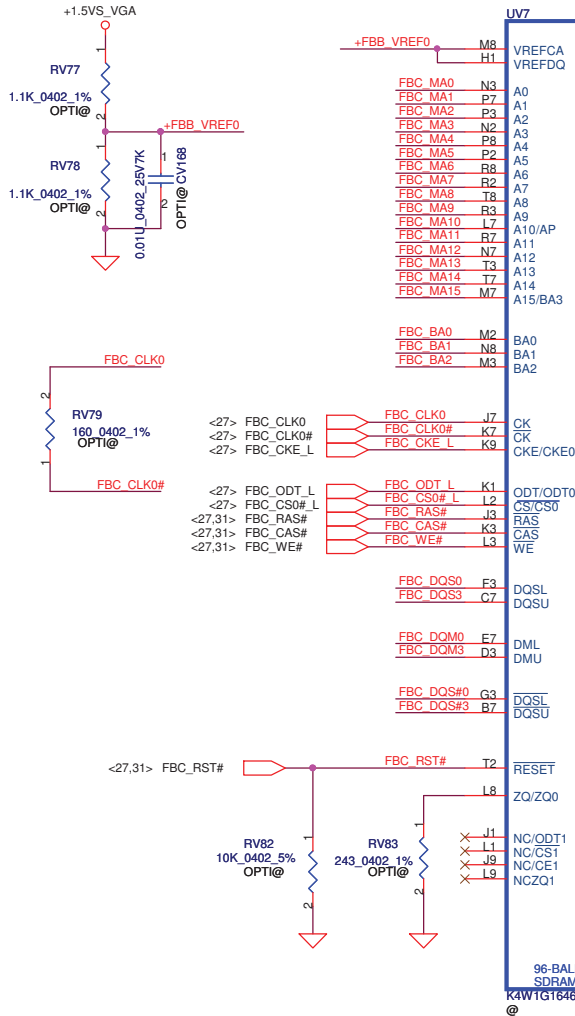
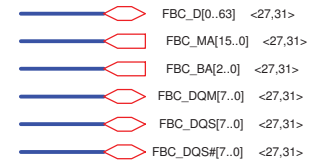
Mode D - Mirror Mode Mapping

Address	DATA Bus	DATA Bus
FBx_CMD0	CS0#_L	32..63
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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				Date:	Wednesday, January 05, 2011

Memory Partition C - Lower 32 bits



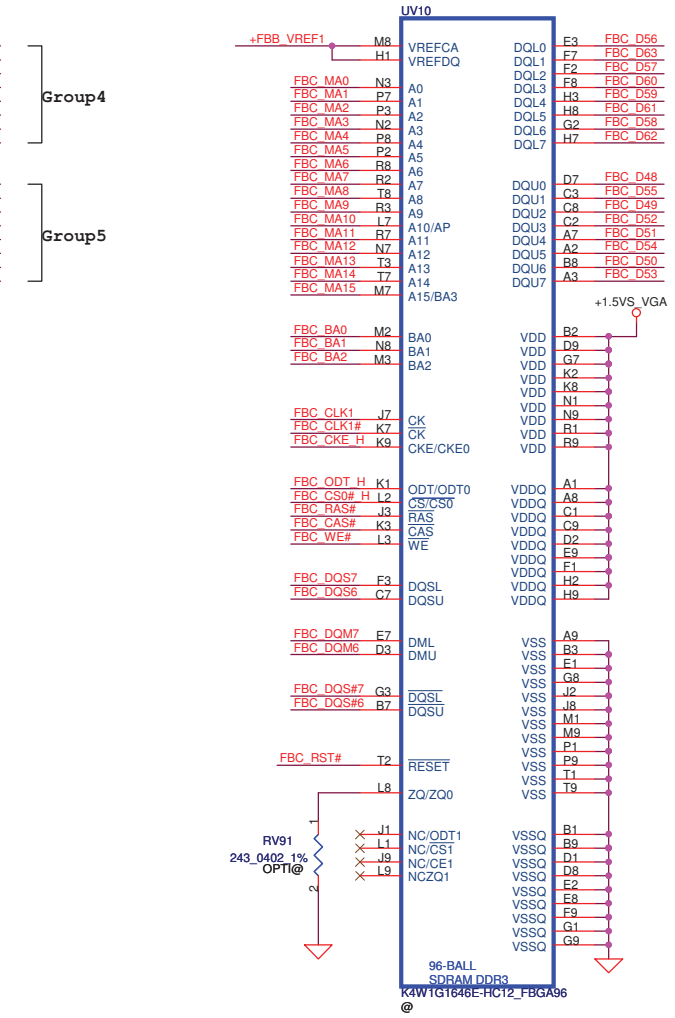
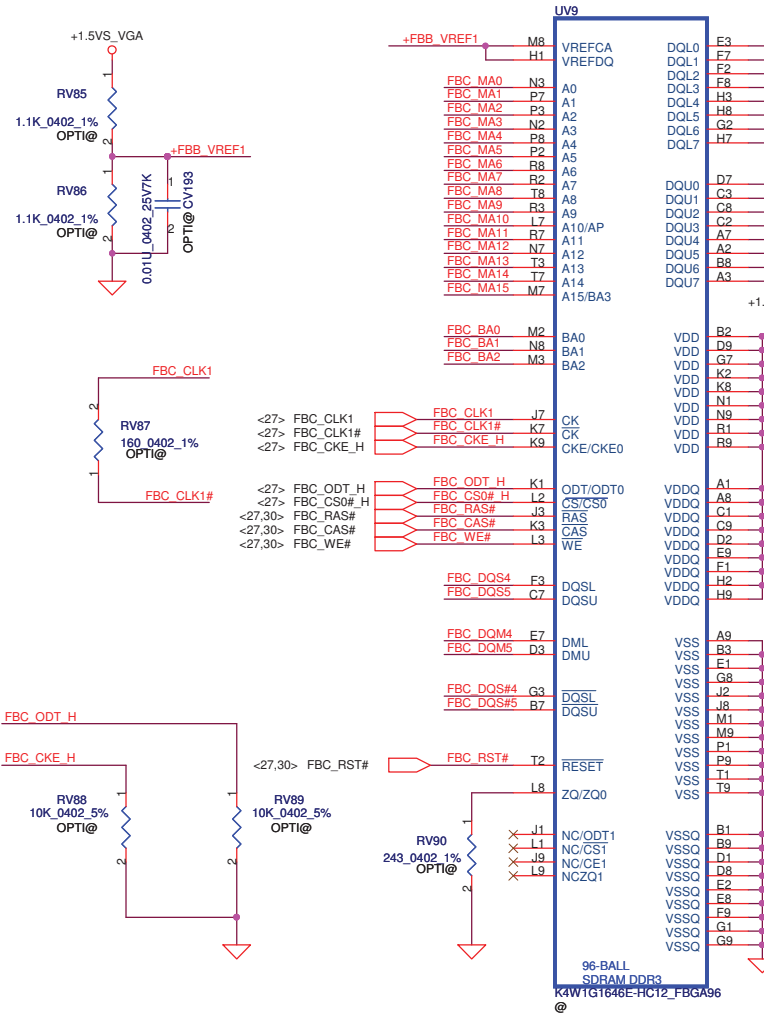
Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Issued Date	2010/11/30	Deciphered Date	2011/08		
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Date:	Wednesday, January 05, 2011	Sheet	30	of	63

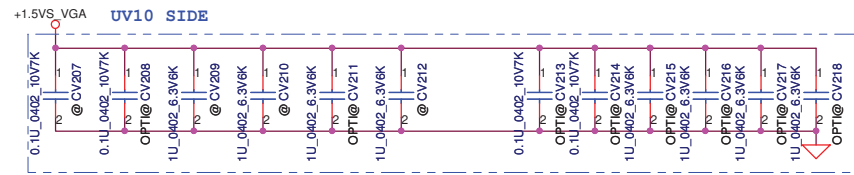
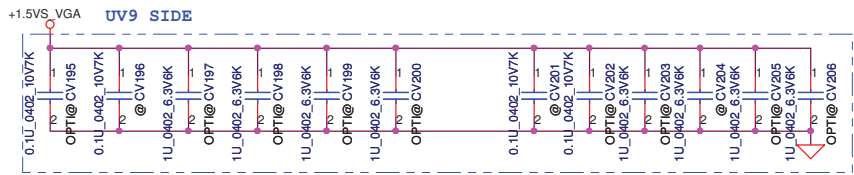
Memory Partition C - Upper 32 bits

- FBC_D[0..63] <27,30>
- FBC_MA[15..0] <27,30>
- FBC_BA[2..0] <27,30>
- FBC_DQM[7..0] <27,30>
- FBC_DQS[7..0] <27,30>
- FBC_DQS#[7..0] <27,30>

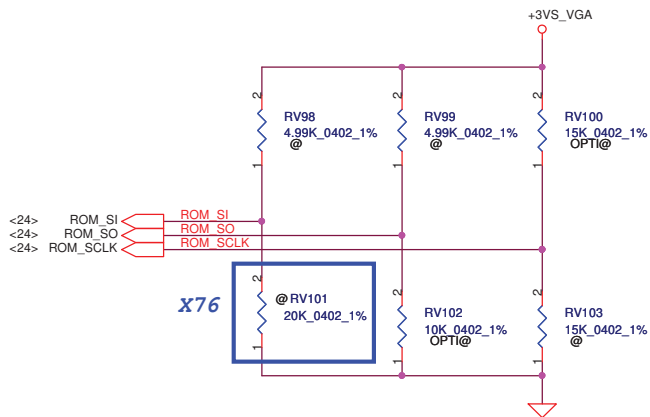
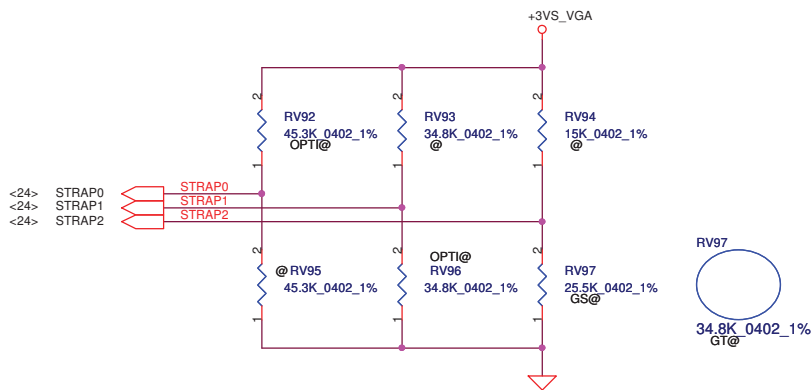


Mode D - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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ROM_SO : PD-10K
 ROM_SCLK : PH-15K
 ROM_SI : PD20K (Samsung)
 Strap 2 : N12P-GS, PD-25K,
 N12P-GT, PD35K,
 Strap 1 : PD-35K
 Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Hynix	H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
		128Mx16	0110	PD 35K	SA00003Y000
Samsung	K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
		128Mx16	0111	PD 45K	SA000047Q10

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

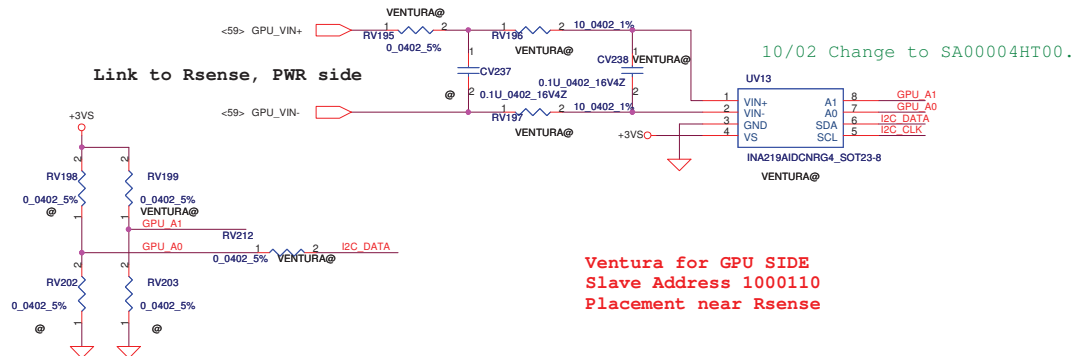
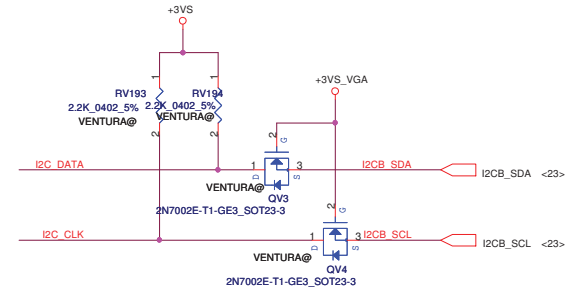
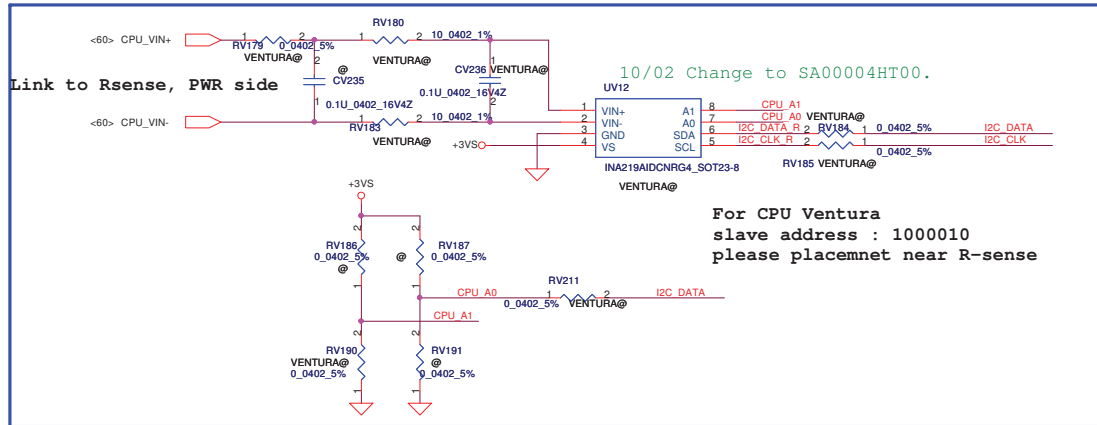
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

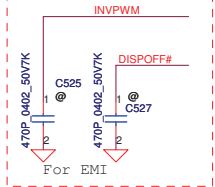
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

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				Rev 1.0 Sheet 32 of 63

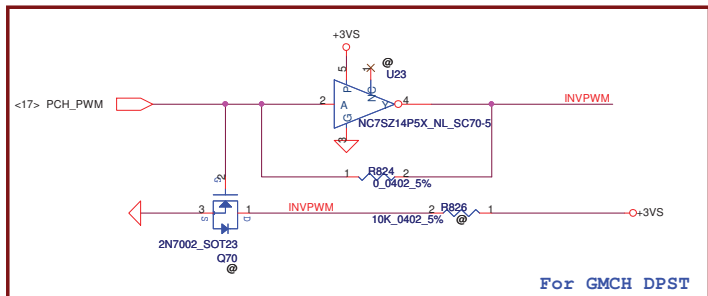
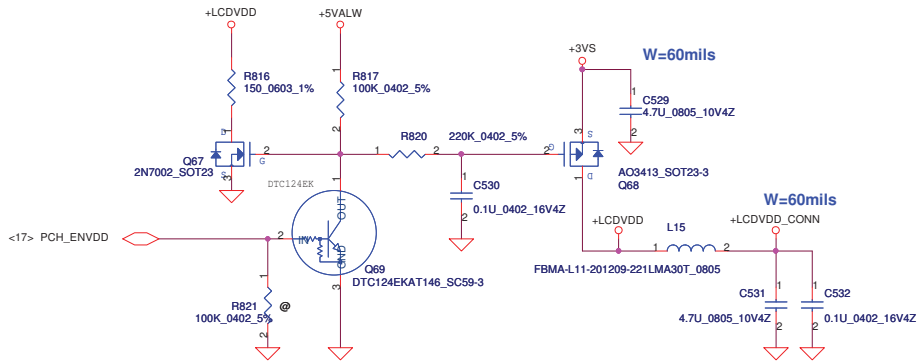
TOP side (under inductor)



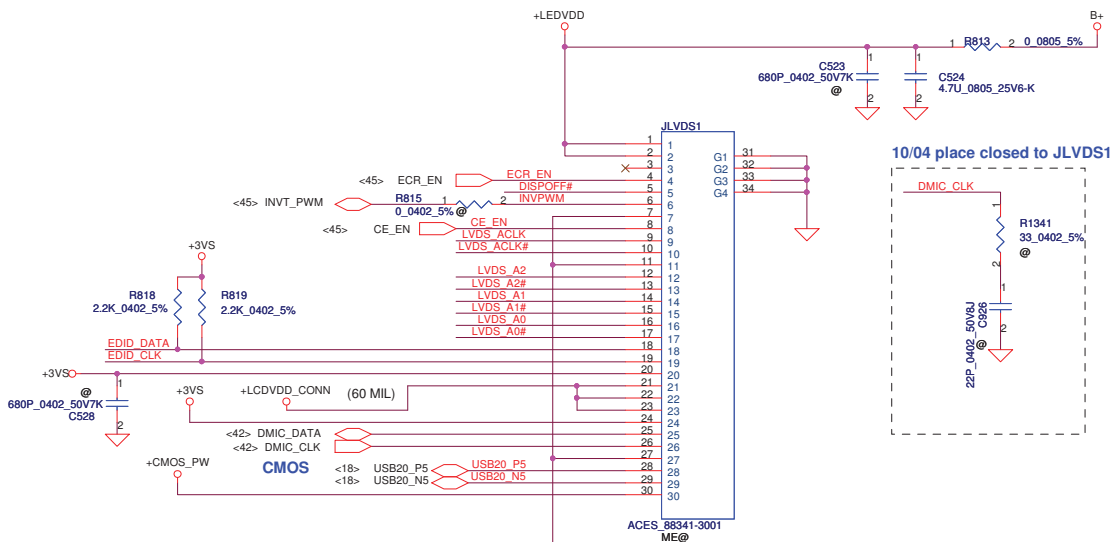
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Issued Date	2010/11/30	Deciphered Date	2011/08				Size
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						Date:	Wednesday, January 05, 2011



LCD POWER CIRCUIT

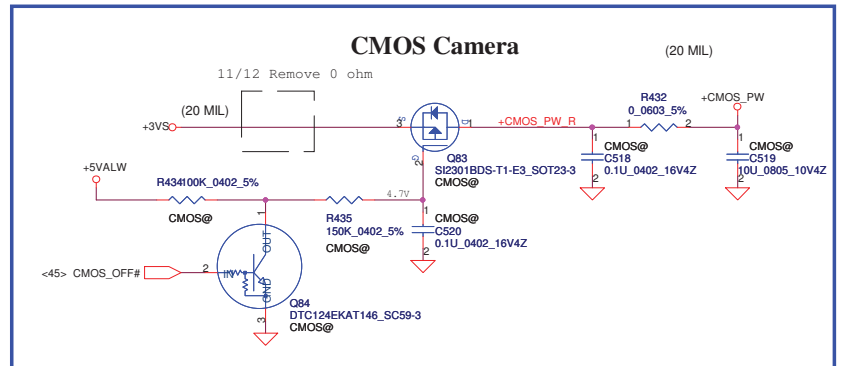
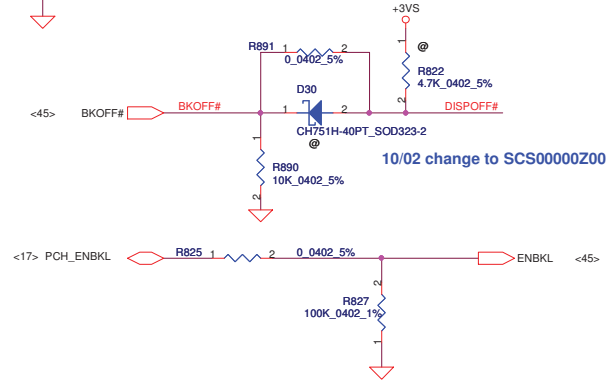
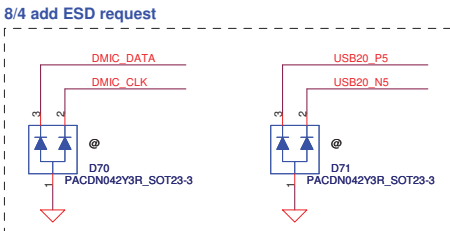


- <17> EDID_CLK <=> EDID_CLK
- <17> EDID_DATA <=> EDID_DATA
- <17> LVDS_A0 <=> LVDS_A0
- <17> LVDS_A0# <=> LVDS_A0#
- <17> LVDS_A1 <=> LVDS_A1
- <17> LVDS_A1# <=> LVDS_A1#
- <17> LVDS_A2 <=> LVDS_A2
- <17> LVDS_A2# <=> LVDS_A2#
- <17> LVDS_ACLK <=> LVDS_ACLK
- <17> LVDS_ACLK# <=> LVDS_ACLK#

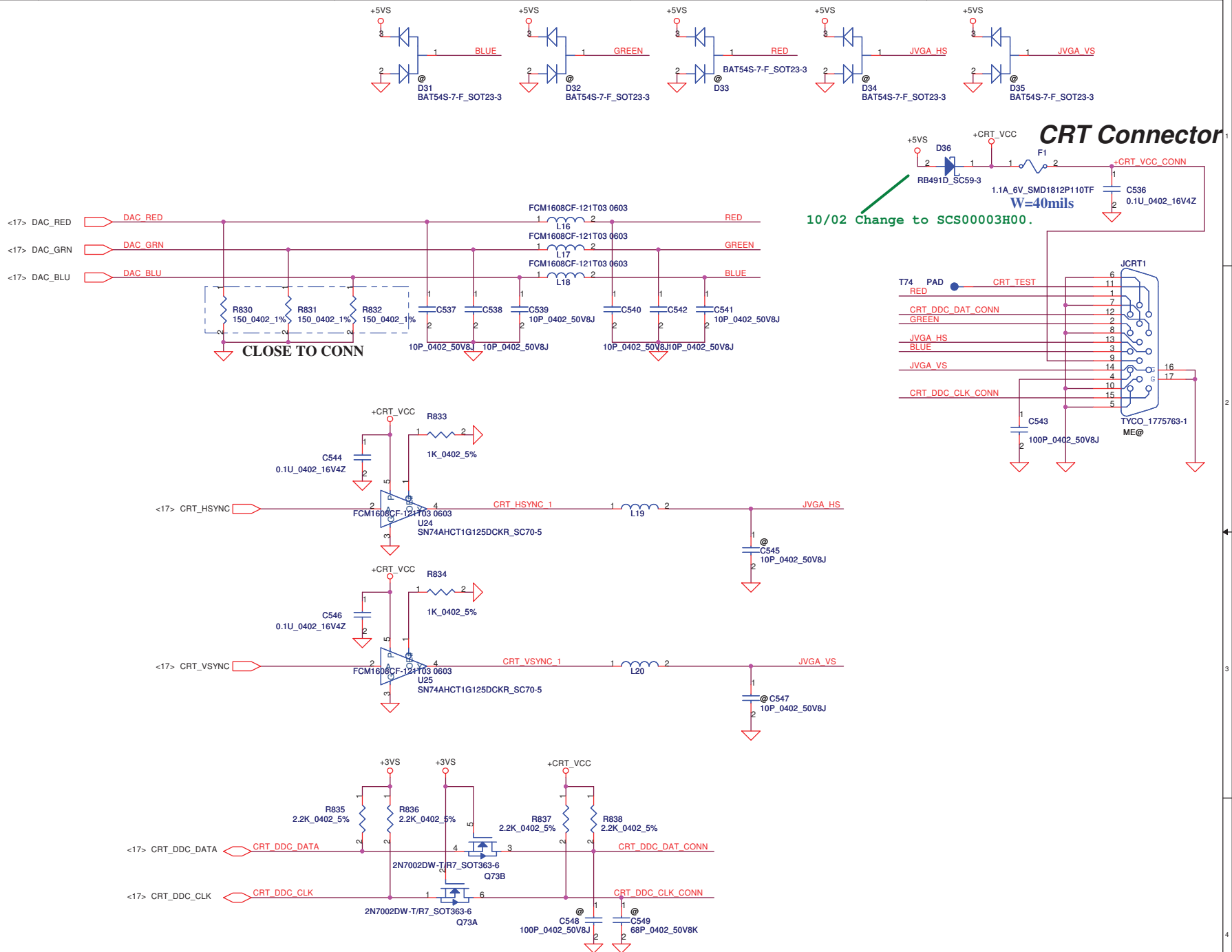


10/04 place closed to JLVD51

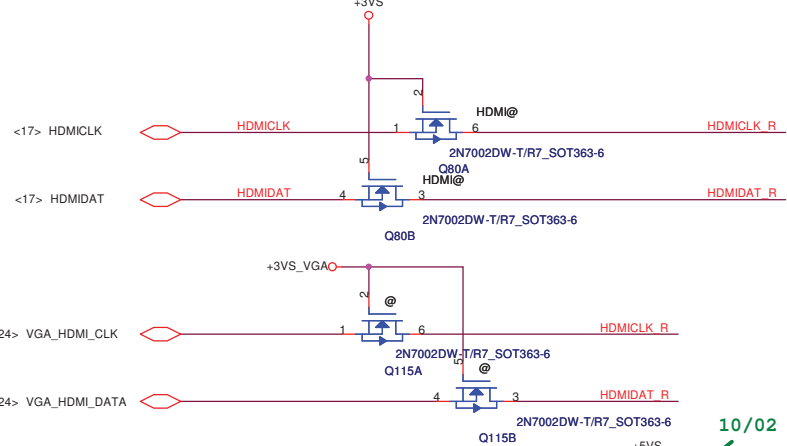
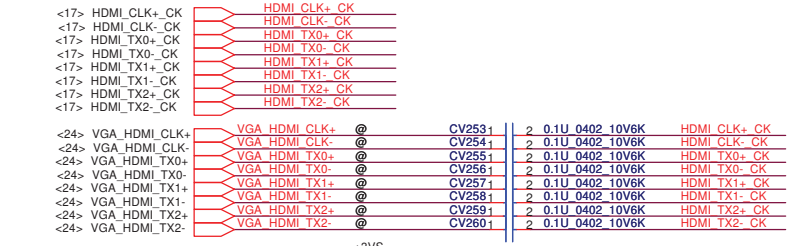
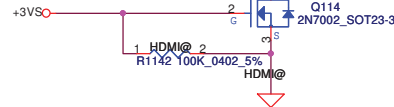
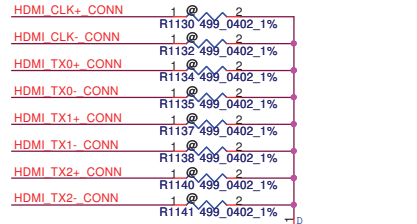
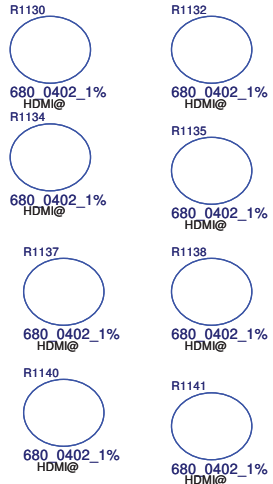
9/21 Rev0.2 update from 40 to 30 pin.



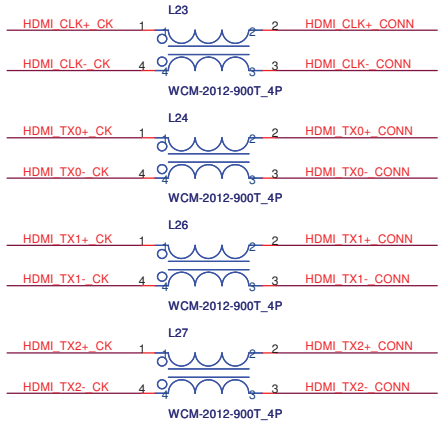
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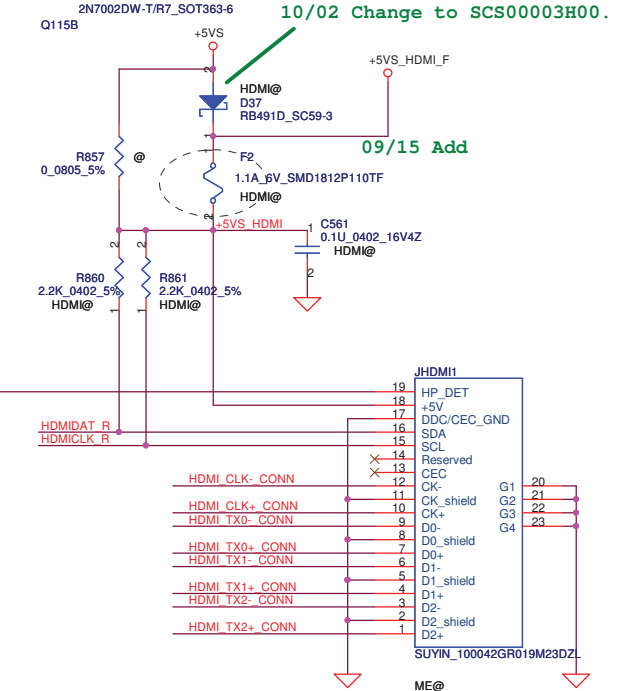
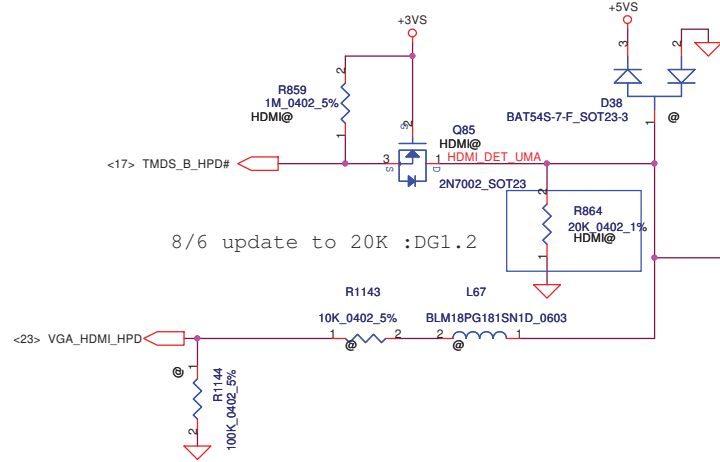
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DVT, Change to SM07000I00 for EMI request.



HDMI_CLK+_CK	R885	1	2	0	0402_5%	HDMI_CLK+_CONN
HDMI_CLK-_CK	R886	1	2	0	0402_5%	HDMI_CLK-_CONN
HDMI_TX0+_CK	R867	1	2	0	0402_5%	HDMI_TX0+_CONN
HDMI_TX0-_CK	R868	1	2	0	0402_5%	HDMI_TX0-_CONN
HDMI_TX1+_CK	R869	1	2	0	0402_5%	HDMI_TX1+_CONN
HDMI_TX1-_CK	R870	1	2	0	0402_5%	HDMI_TX1-_CONN
HDMI_TX2+_CK	R871	1	2	0	0402_5%	HDMI_TX2+_CONN
HDMI_TX2-_CK	R872	1	2	0	0402_5%	HDMI_TX2-_CONN



10/02 Change to SCS00003H00.

09/15 Add

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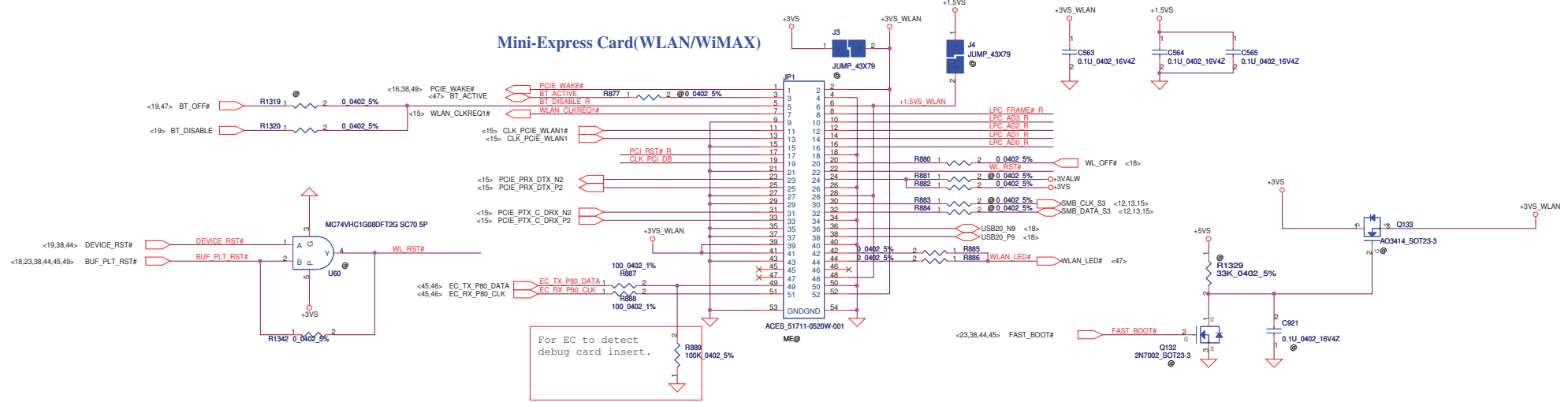
PIQY0 LA6881P

Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

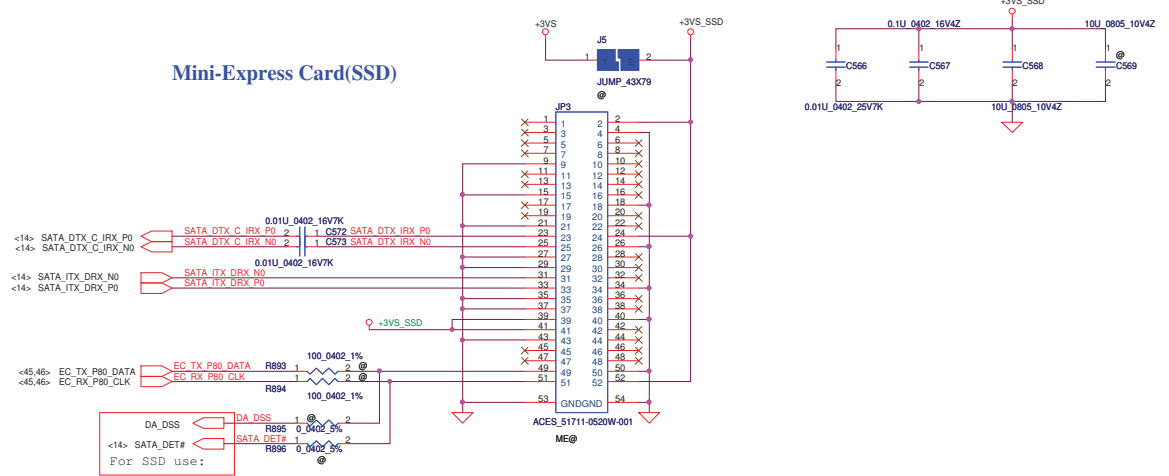
LPC_FRAME# R	R873	1	2	0	0402_5%	LPC_FRAME#	LPC_FRAME#	<14,45>
LPC_AD3 R	R874	1	2	0	0402_5%	LPC_AD3	LPC_AD3	<14,45>
LPC_AD2 R	R875	1	2	0	0402_5%	LPC_AD2	LPC_AD2	<14,45>
LPC_AD1 R	R876	1	2	0	0402_5%	LPC_AD1	LPC_AD1	<14,45>
LPC_AD0 R	R877	1	2	0	0402_5%	LPC_AD0	LPC_AD0	<14,45>
PCI_RST# R	R878	1	2	0	0402_5%	PCI_RST#	PCI_RST#	<14,45>
CLK_PCI_DB	R879	1	2	0	0402_5%	CLK_PCI_DB	CLK_PCI_DB	<15>

Mini-Express Card(WLAN/WiMAX)

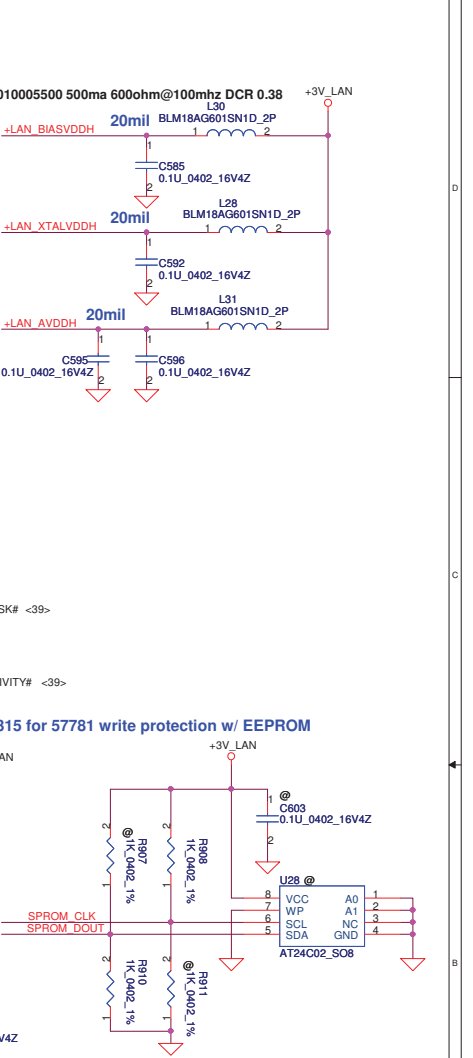
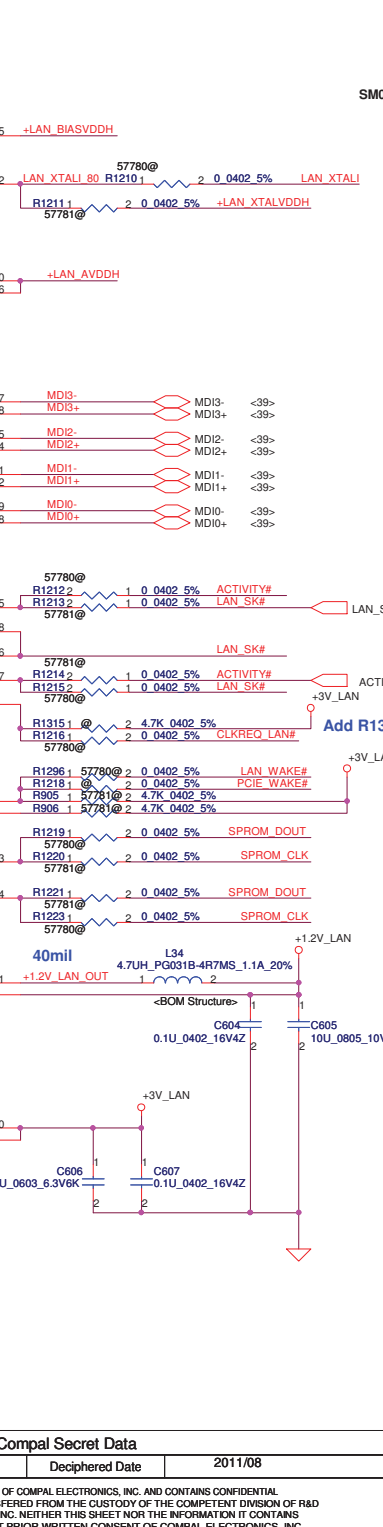
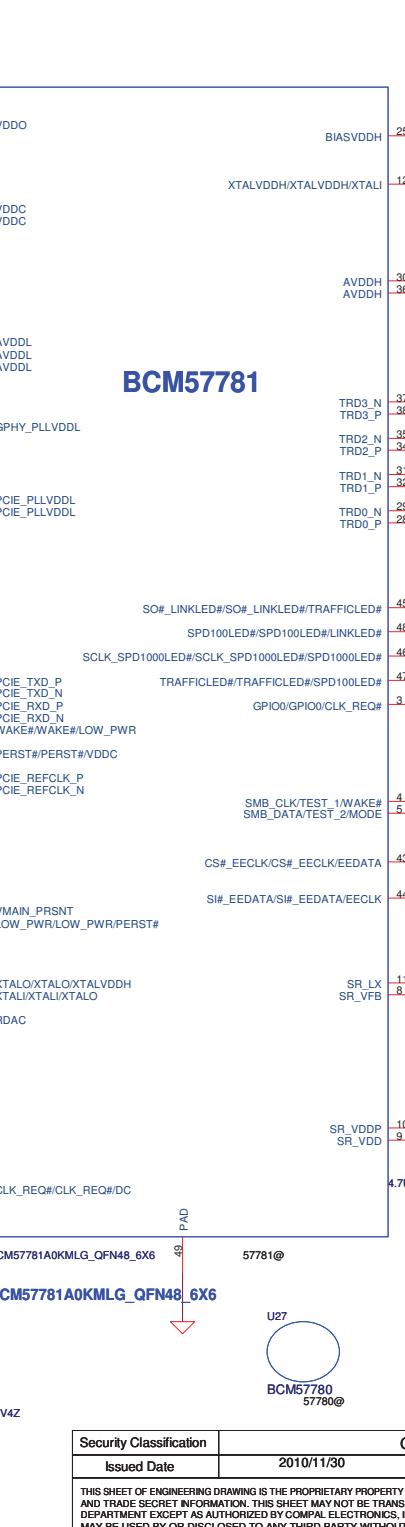
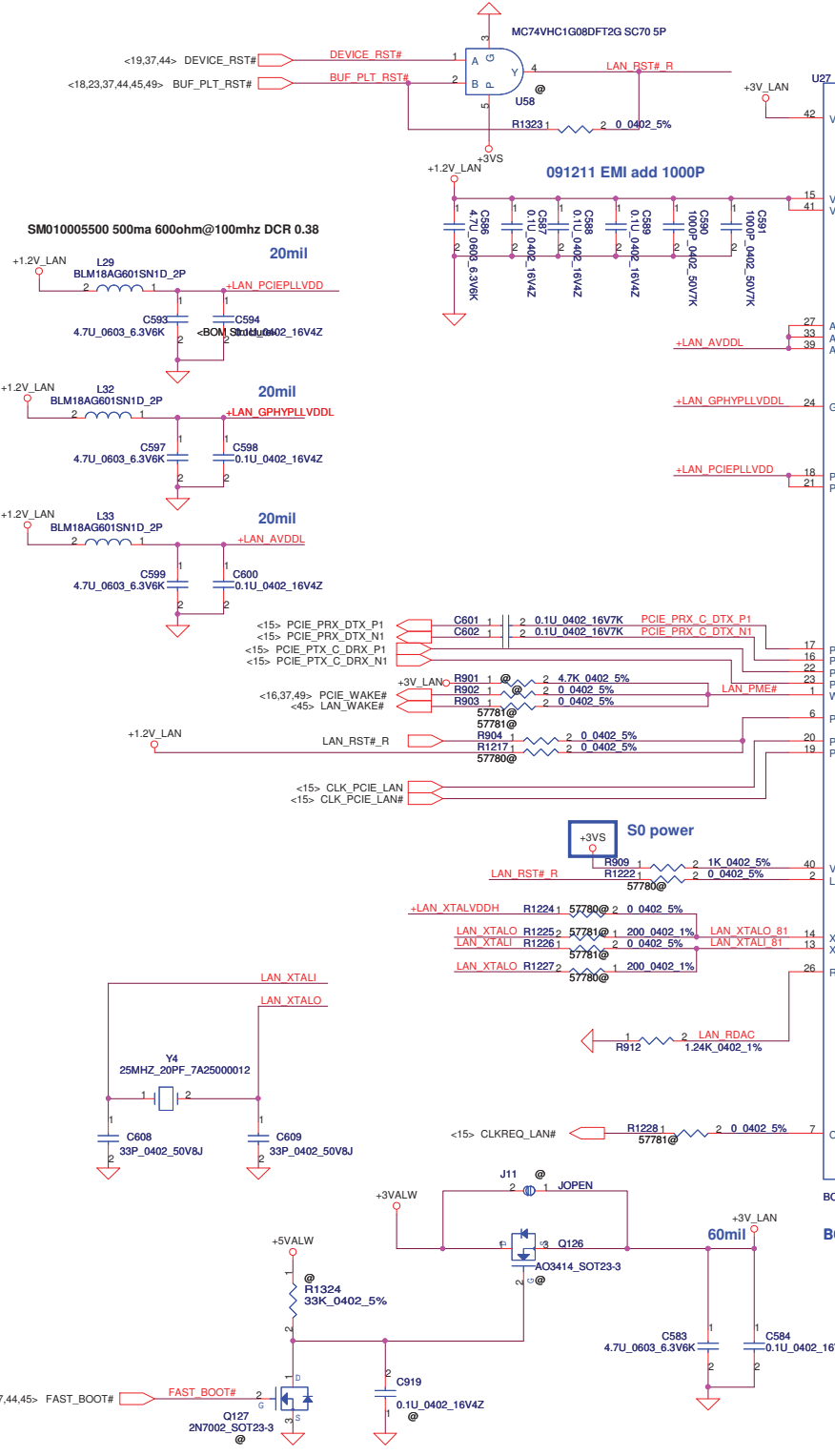


SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)



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Size	Document Number	PIQY0 LA6881P		Rev 1.0
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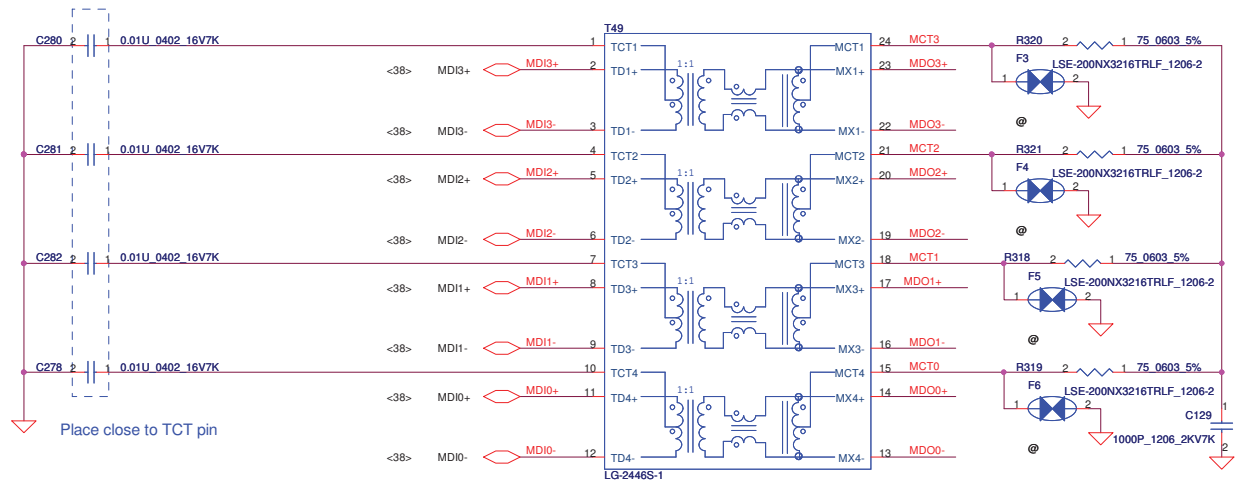
	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data	
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		2011/08

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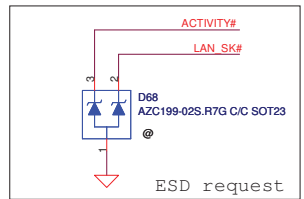
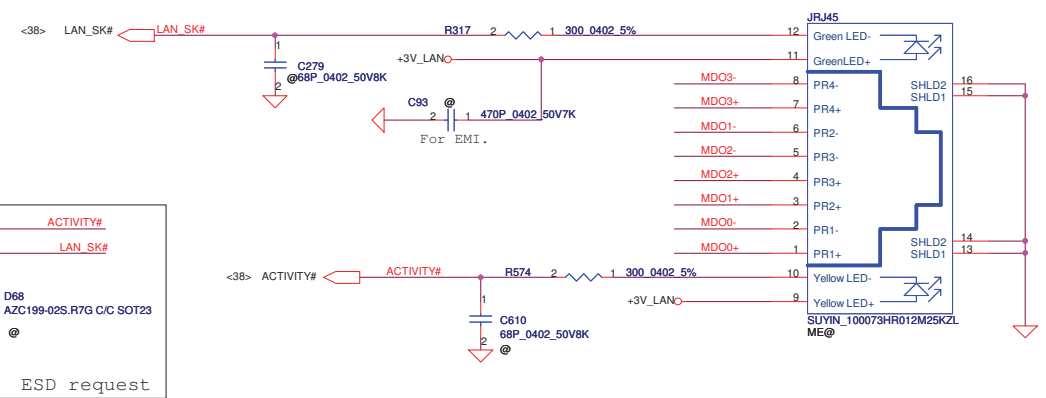
Compal Electronics, Inc.			
Broadcom BCM57781			
Title	Size	Document Number	Rev
	Customer	PIQY0 LA6881P	1.0
Date	Wednesday, January 05, 2011		Sheet 38 of 63

Close to T14

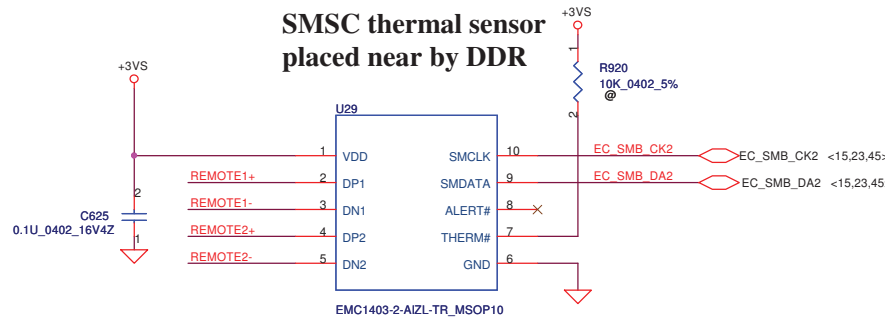
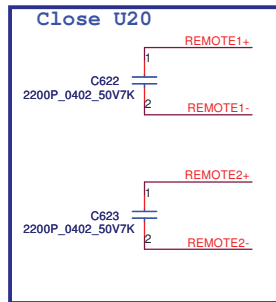


Place close to TCT pin

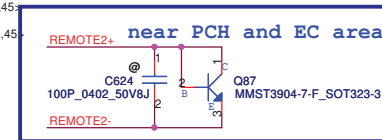
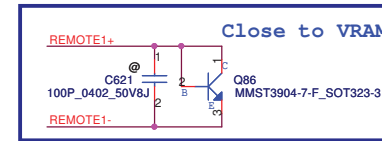
RJ45 Conn.



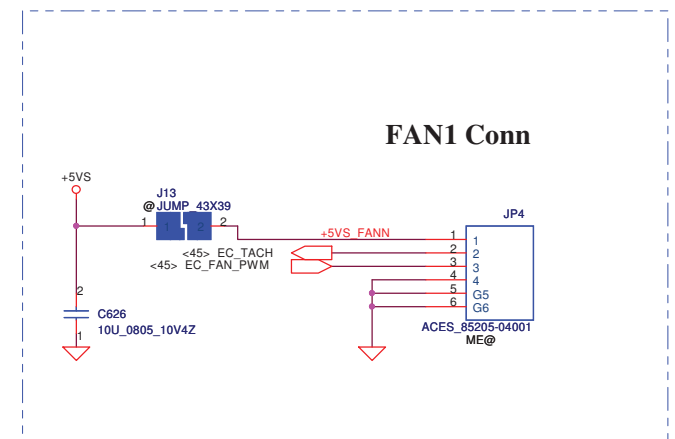
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Size	Document Number	Rev		Date	
Custom	PIQY0 LA6881P	1.0		Wednesday, January 05, 2011	
			Sheet	39	of 63



Address 1001_101xb
8/02 Change PN to SA000046C00, Fintek.

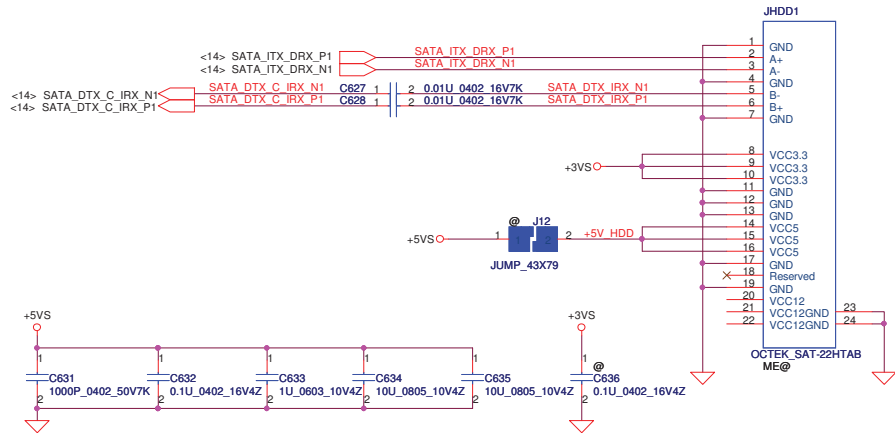


REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

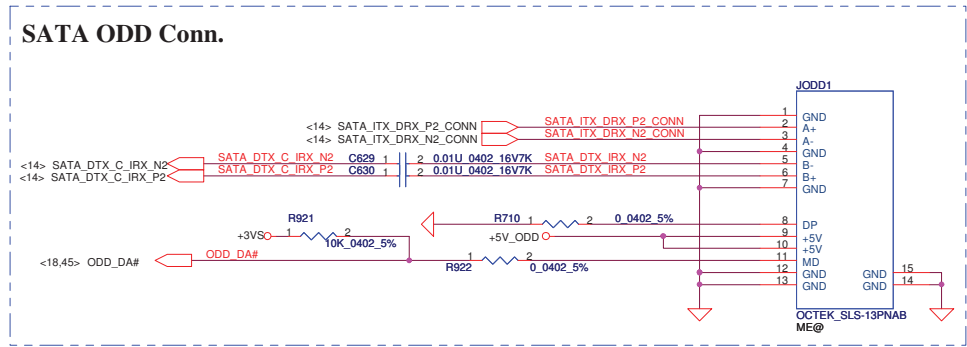


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				Date: Wednesday, January 05, 2011	Rev 1.0
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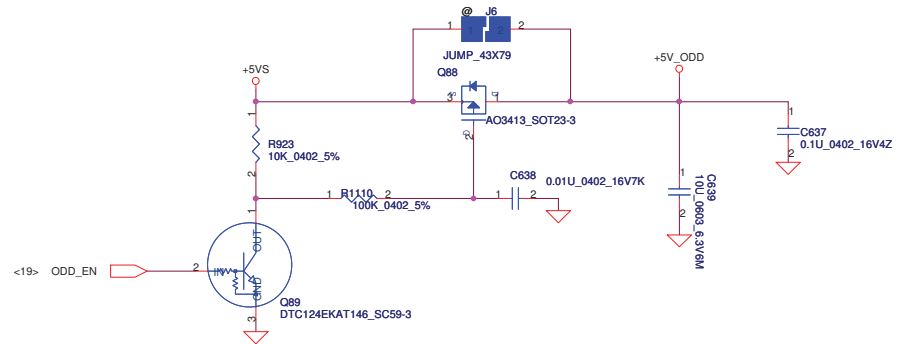
SATA HDD Conn.



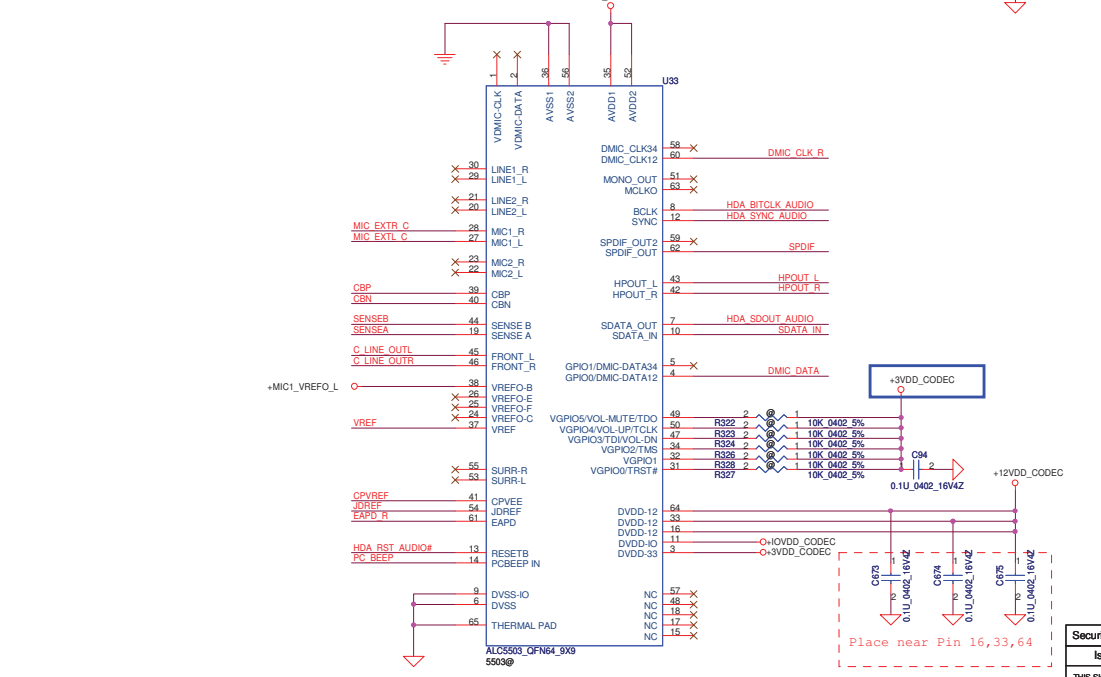
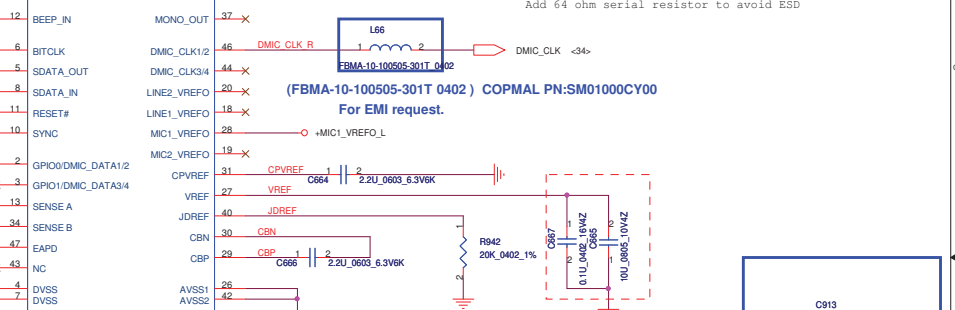
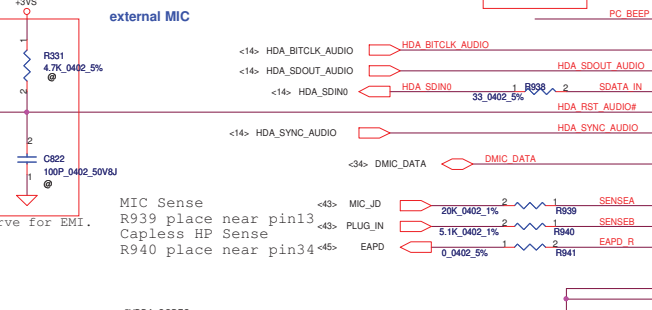
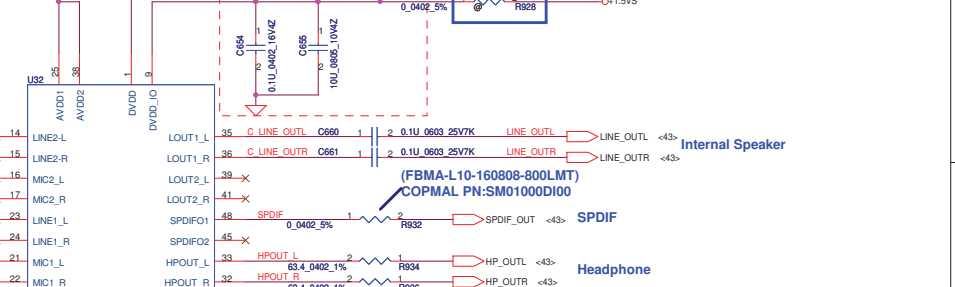
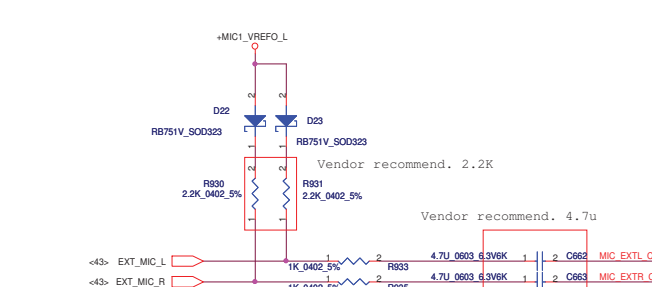
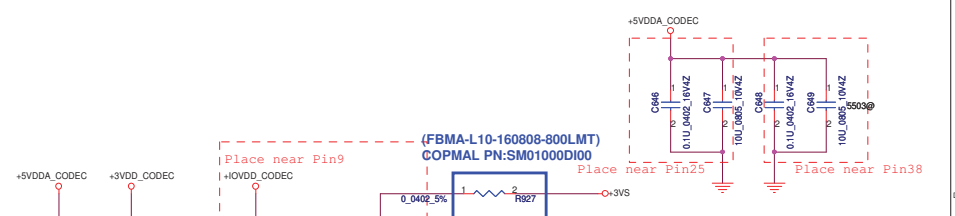
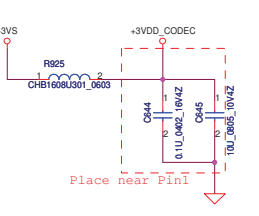
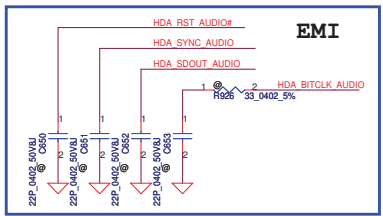
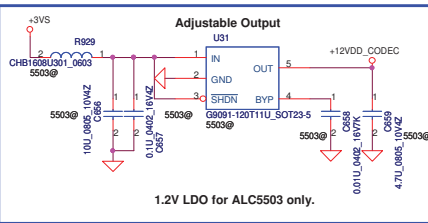
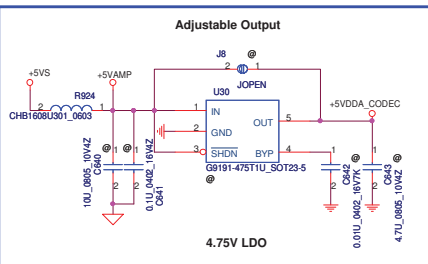
SATA ODD Conn.



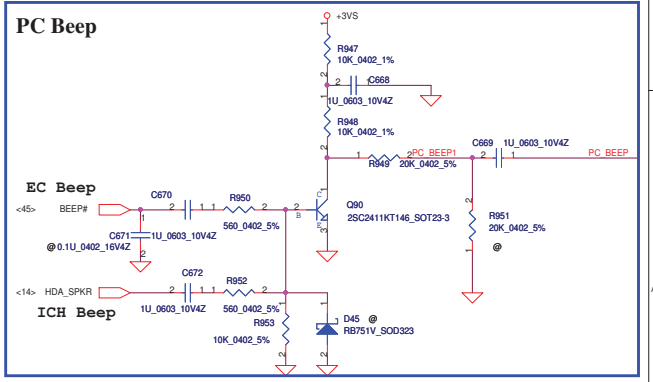
ODD Power Control



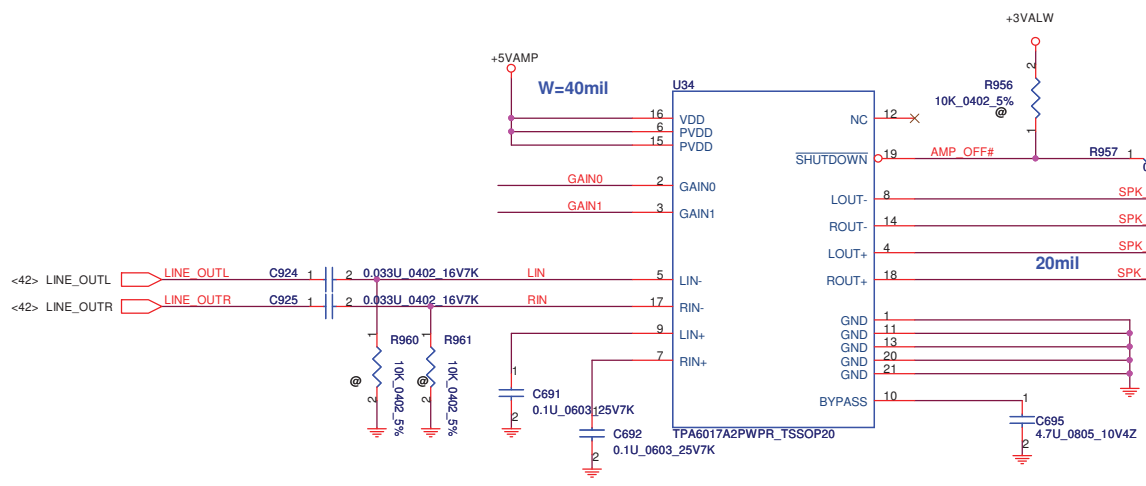
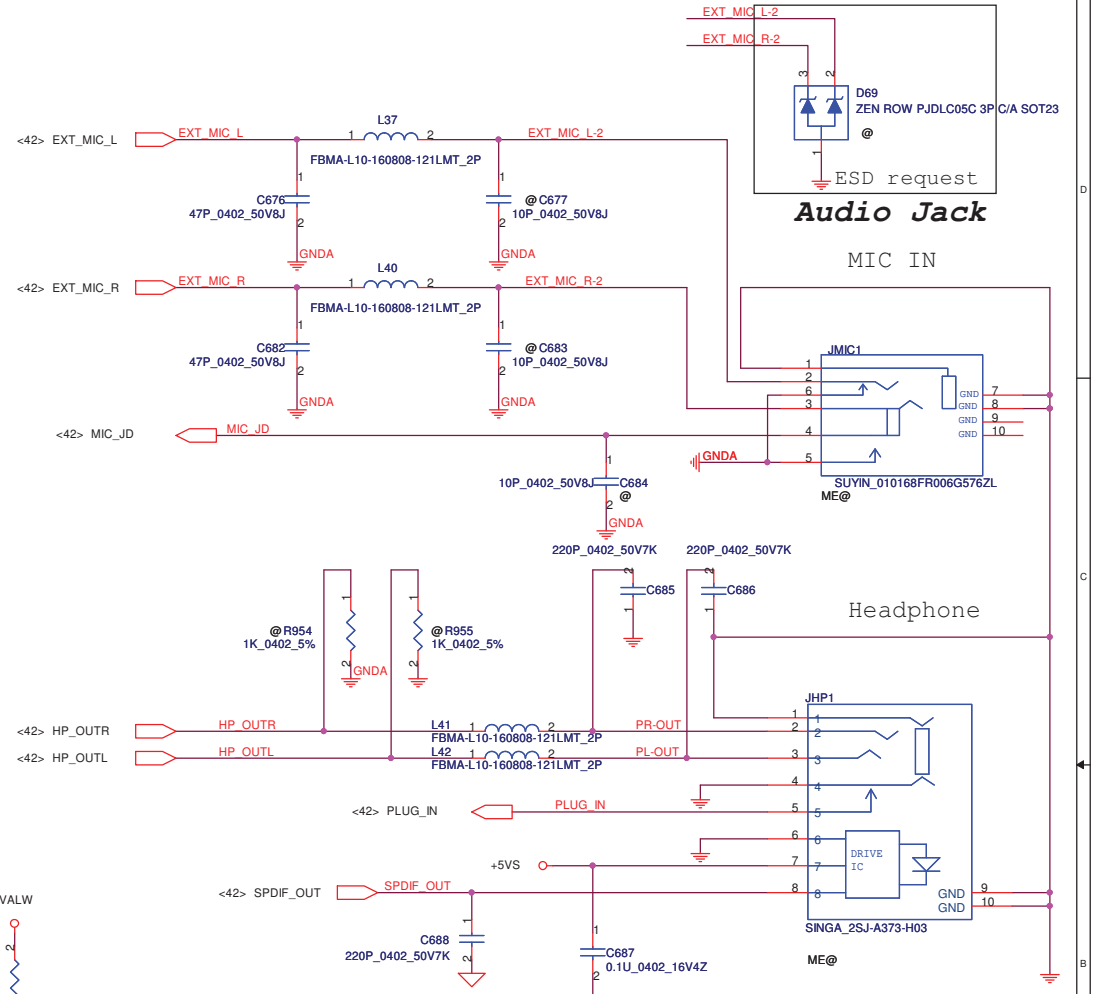
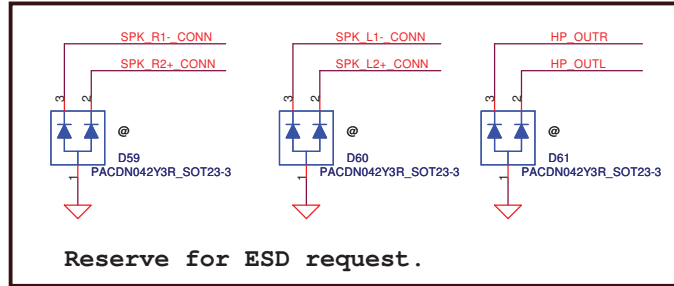
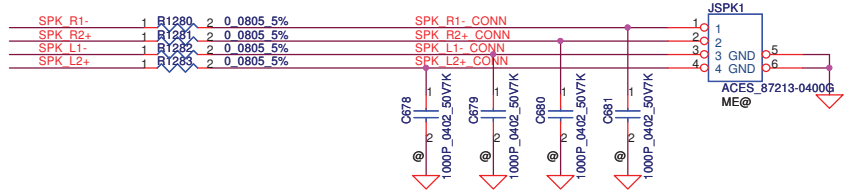
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				Size B	Document Number	Rev 1.0
				PIQY0 LA6881P		
				Date:	Wednesday, January 05, 2011	Sheet 41 of 63



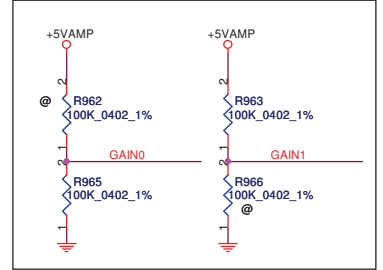
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MIC2 (Pin16/17)	Internal	Internal Mic



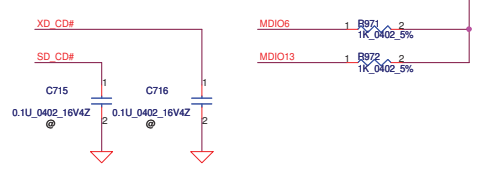
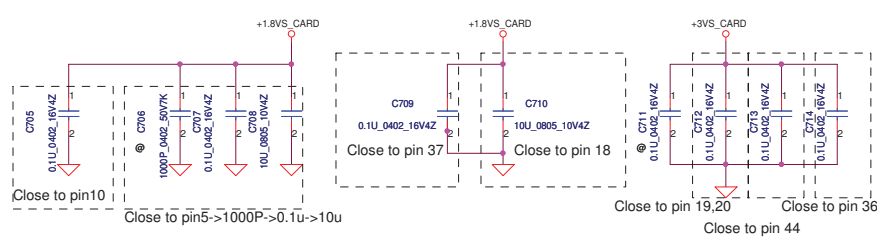
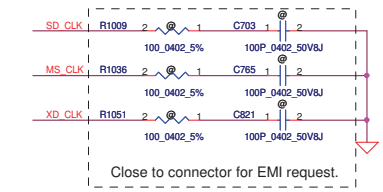
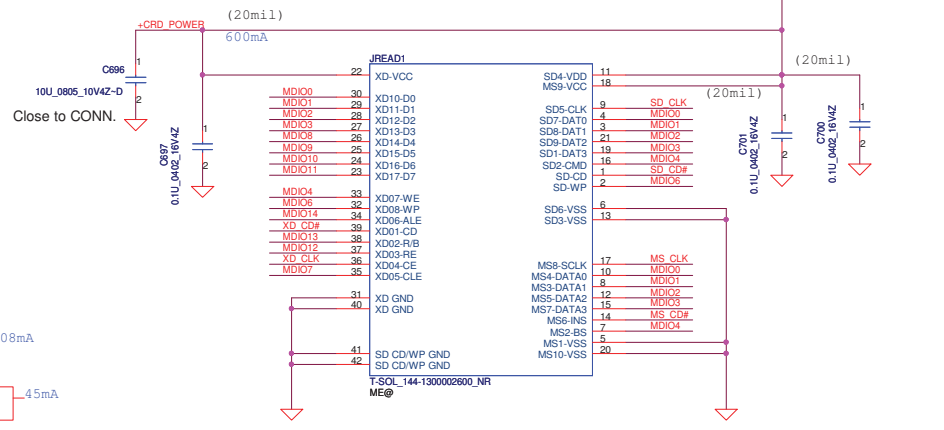
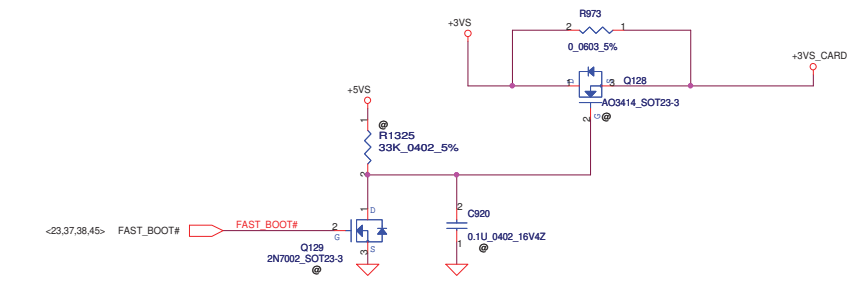
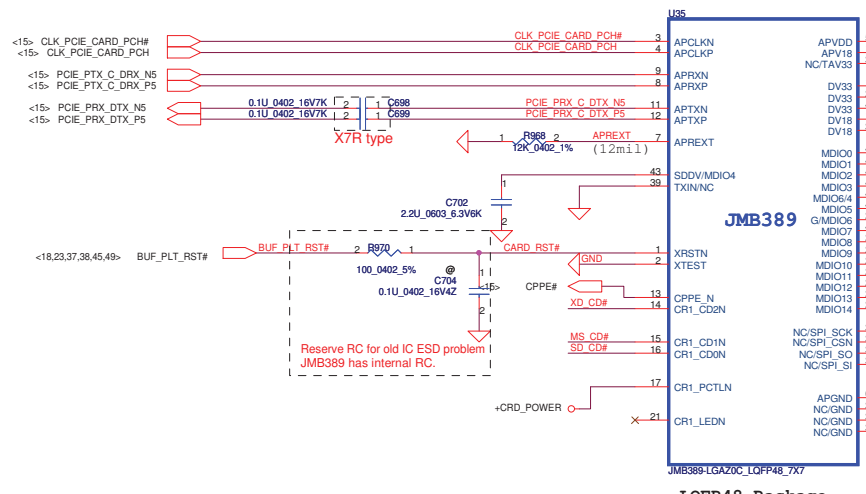
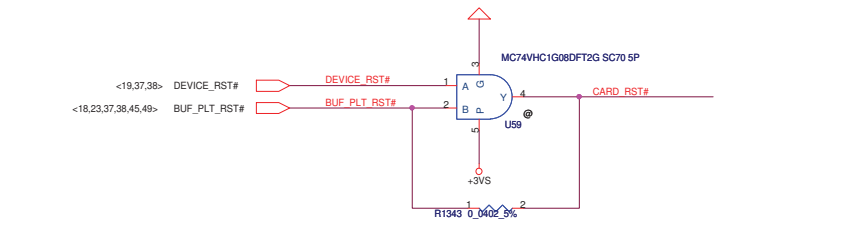
wide 20MIL



GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

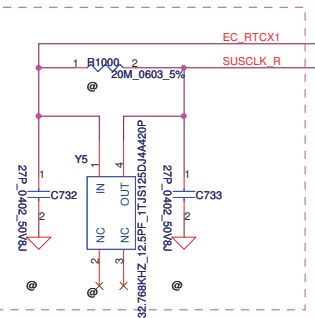
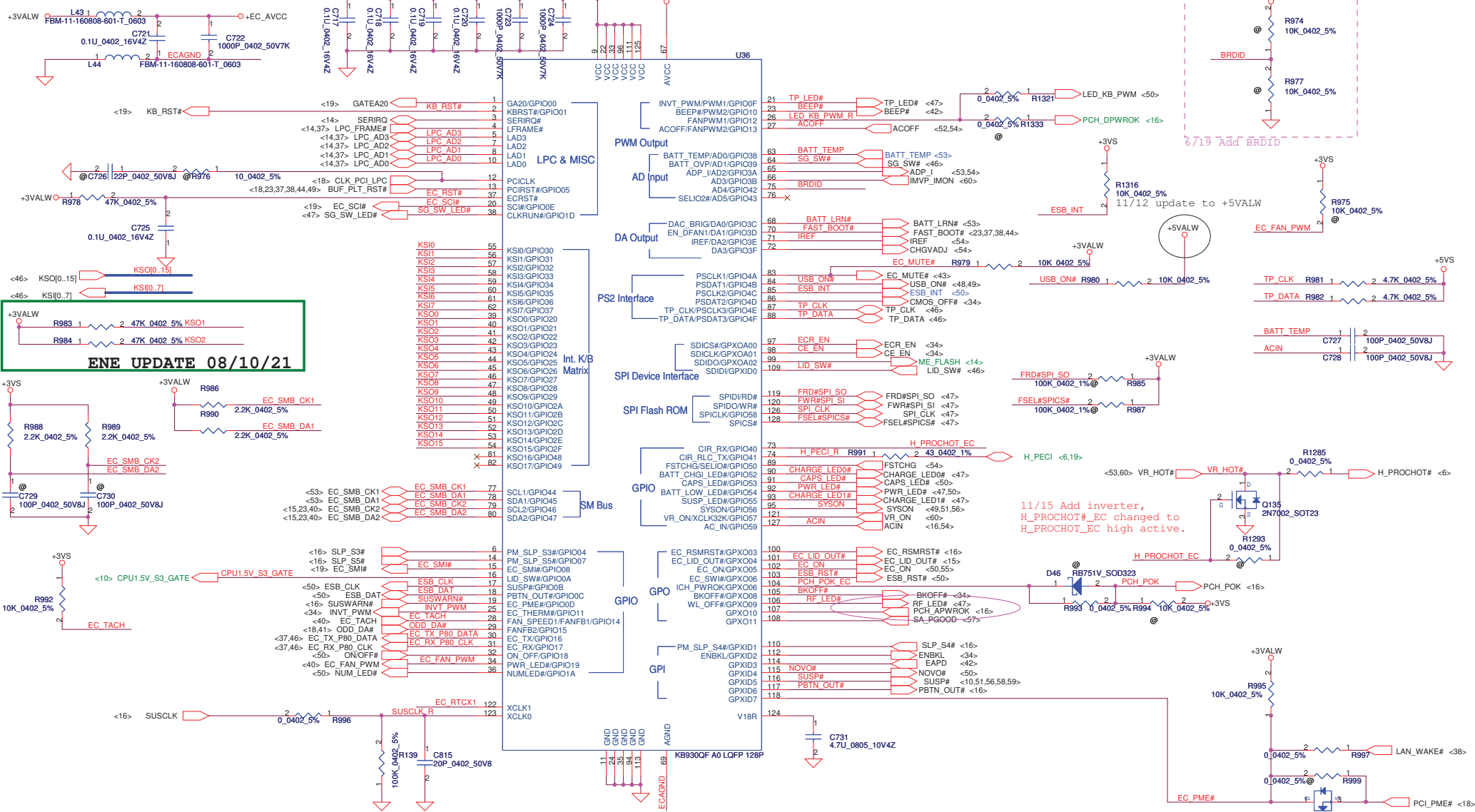


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Size	Document Number			Rev	1.0
Custom	KIWB1/B2_LA4601P			Date	Wednesday, January 05, 2011
				Sheet	43 of 63

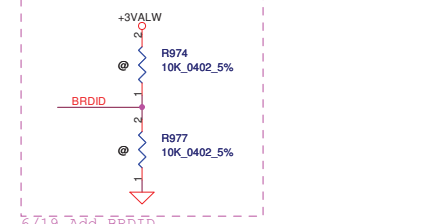


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Size	Document Number	Rev	PIQY0 LA6881P	
Custom		1.0		
Date:	Wednesday, January 05, 2011	Sheet	44	of 63

10/2 Change to SM01000550.



6/15 add XTAL

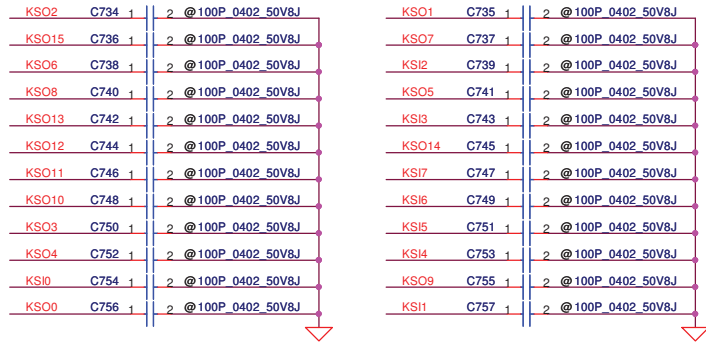
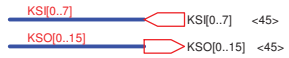


6/19 Add BRDID

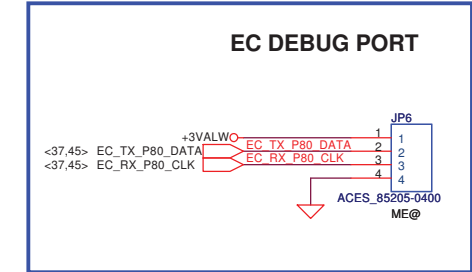
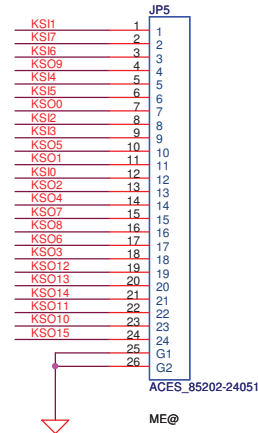
11/15 Add inverter, H_PROCHOT#_EC changed to H_PROCHOT_EC high active.

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				Custar	PIQY0 LA6881P	1.0
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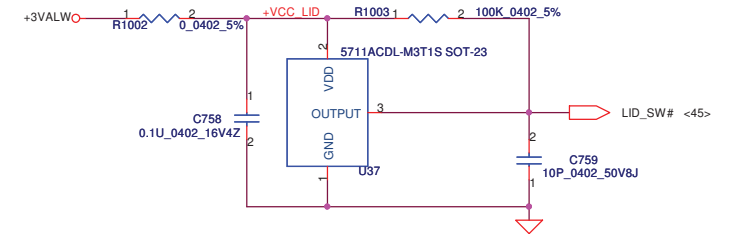
INT_KBD Conn.



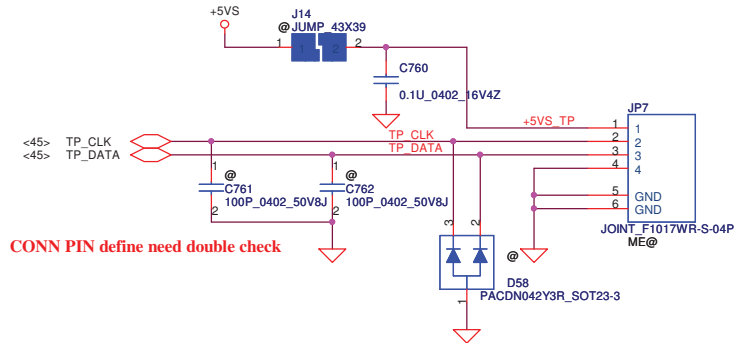
CONN PIN define need double check



Lid Switch

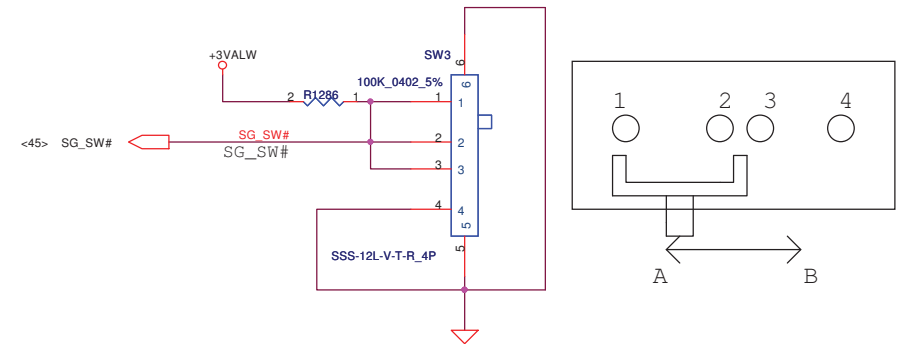
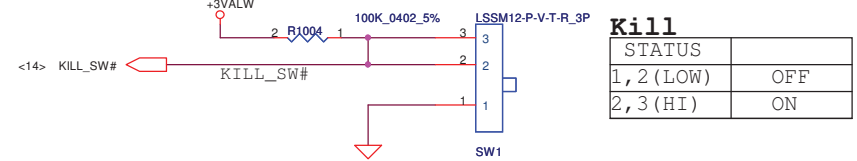


To TP/B Conn.



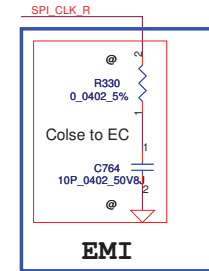
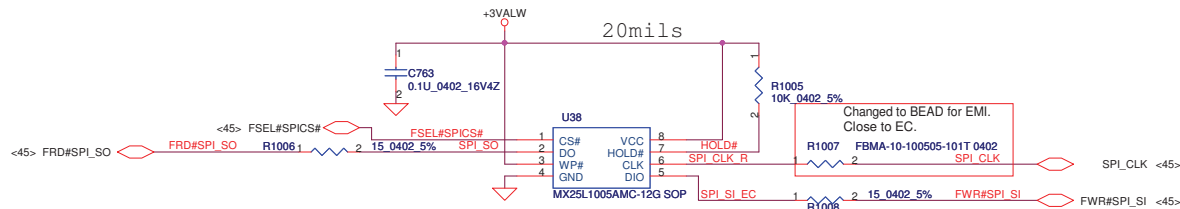
CONN PIN define need double check

Kill Switch

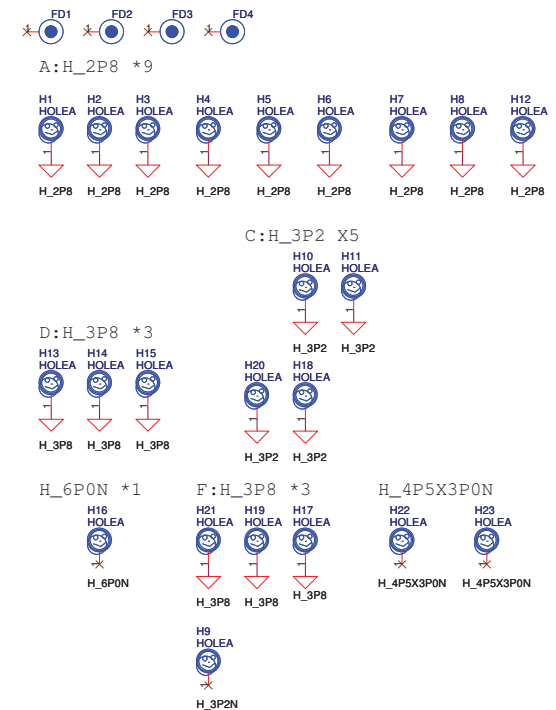
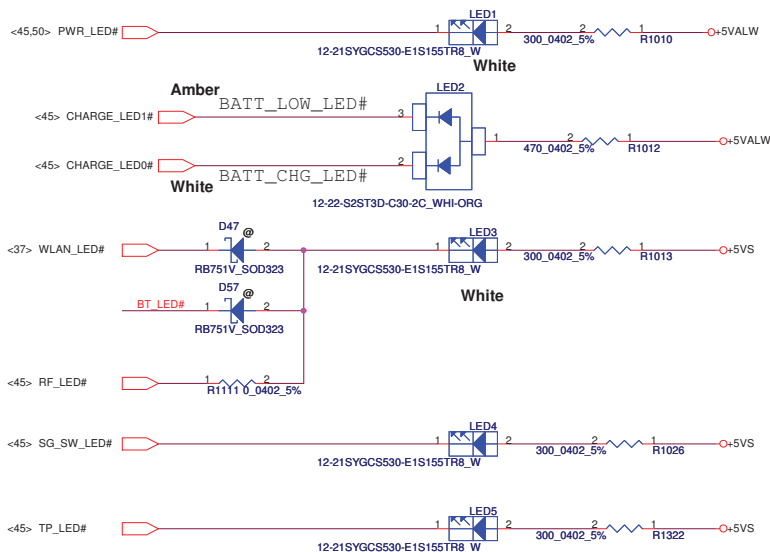


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Size	Document Number		Rev	
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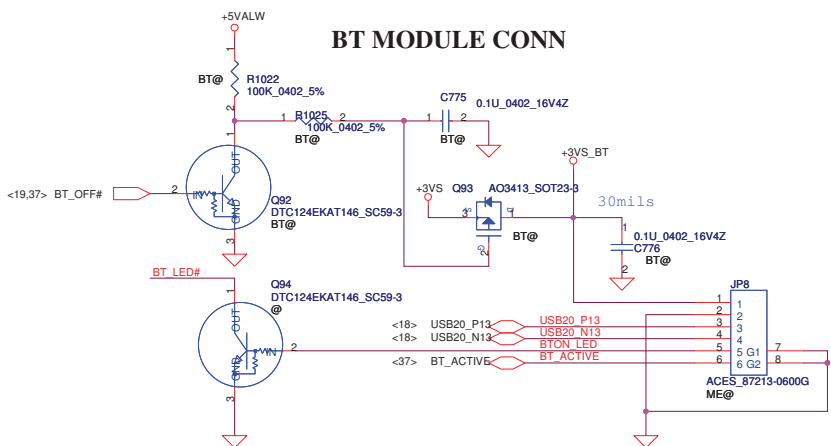
**FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100**



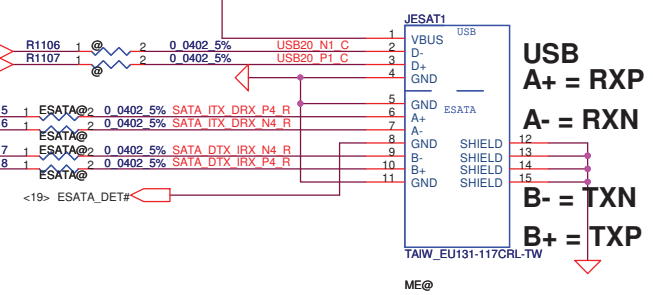
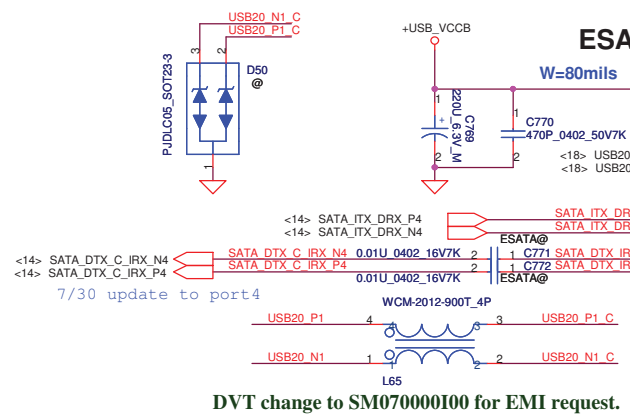
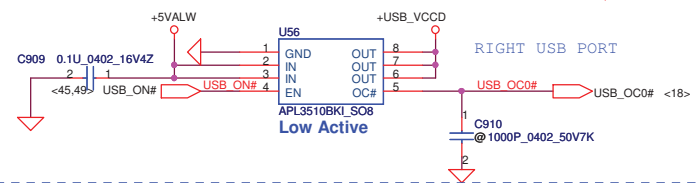
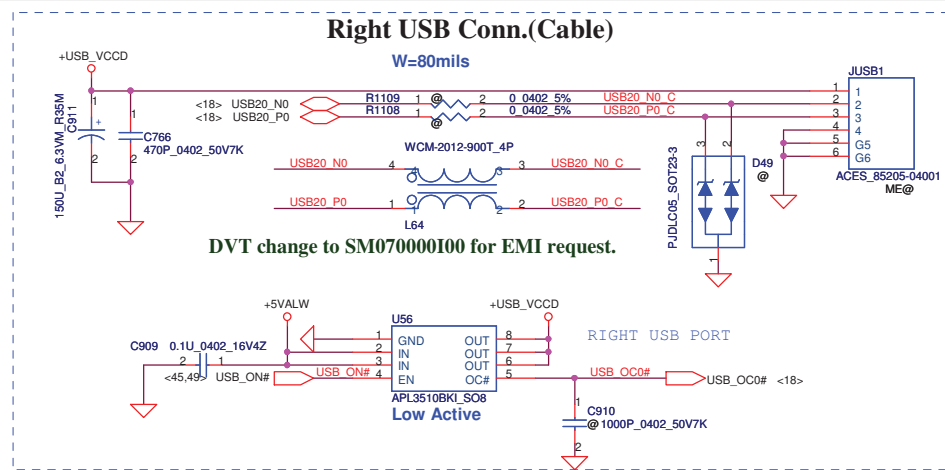
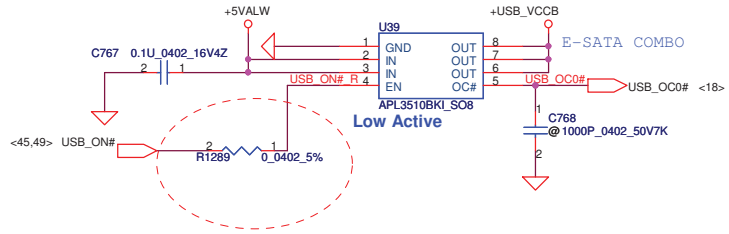
LED



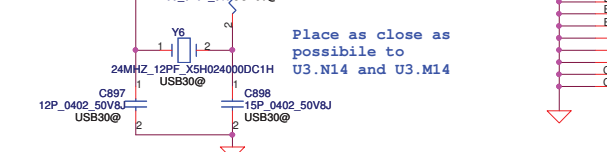
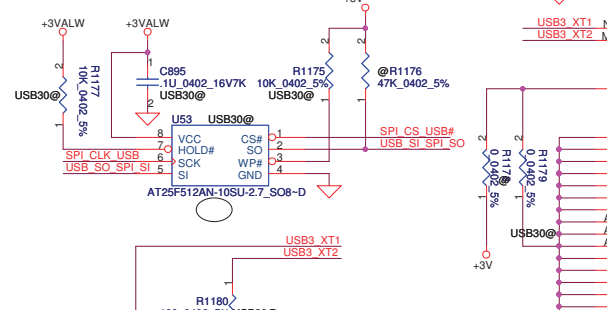
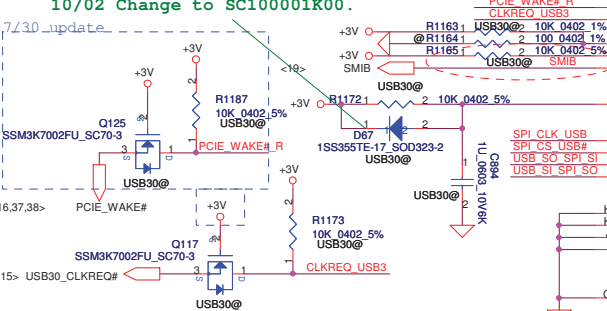
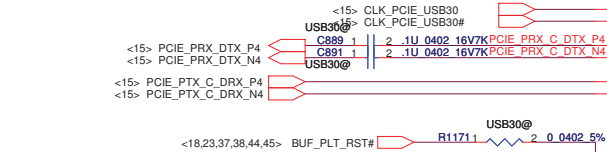
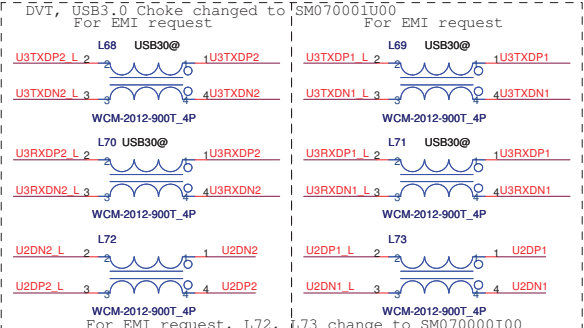
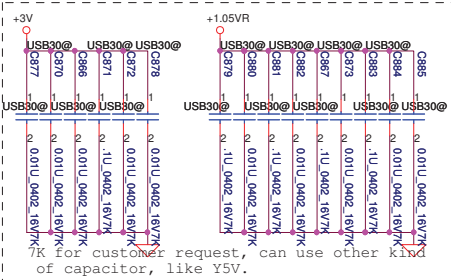
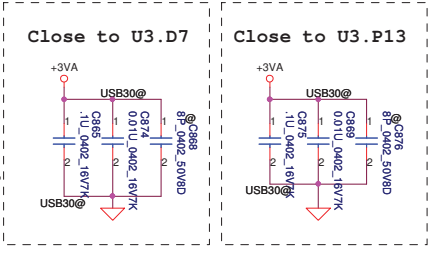
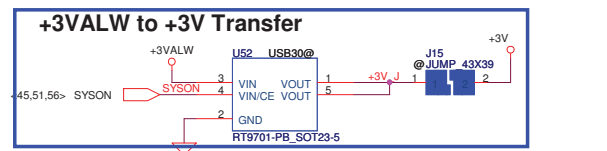
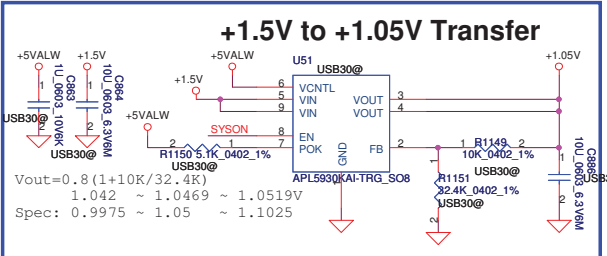
BT MODULE CONN



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SPEC Max: +3V---200mA; +1.05V---800mA
Idle mode: 0.489W; +3V---43mA; +1.05V---328mA
D3 mode: 0.066W; +3V---5.4mA; +1.05V---45mA

Can be attach to EC, either.

PCI Express/ExpressCard select signal 1:others
 0:Express Card or Mini card

As short as possible

Place as close as possible to U3.N14 and U3.M14

W=60mils

09/15 Reserve inverter.

For ESD Request +USB3 VCCA

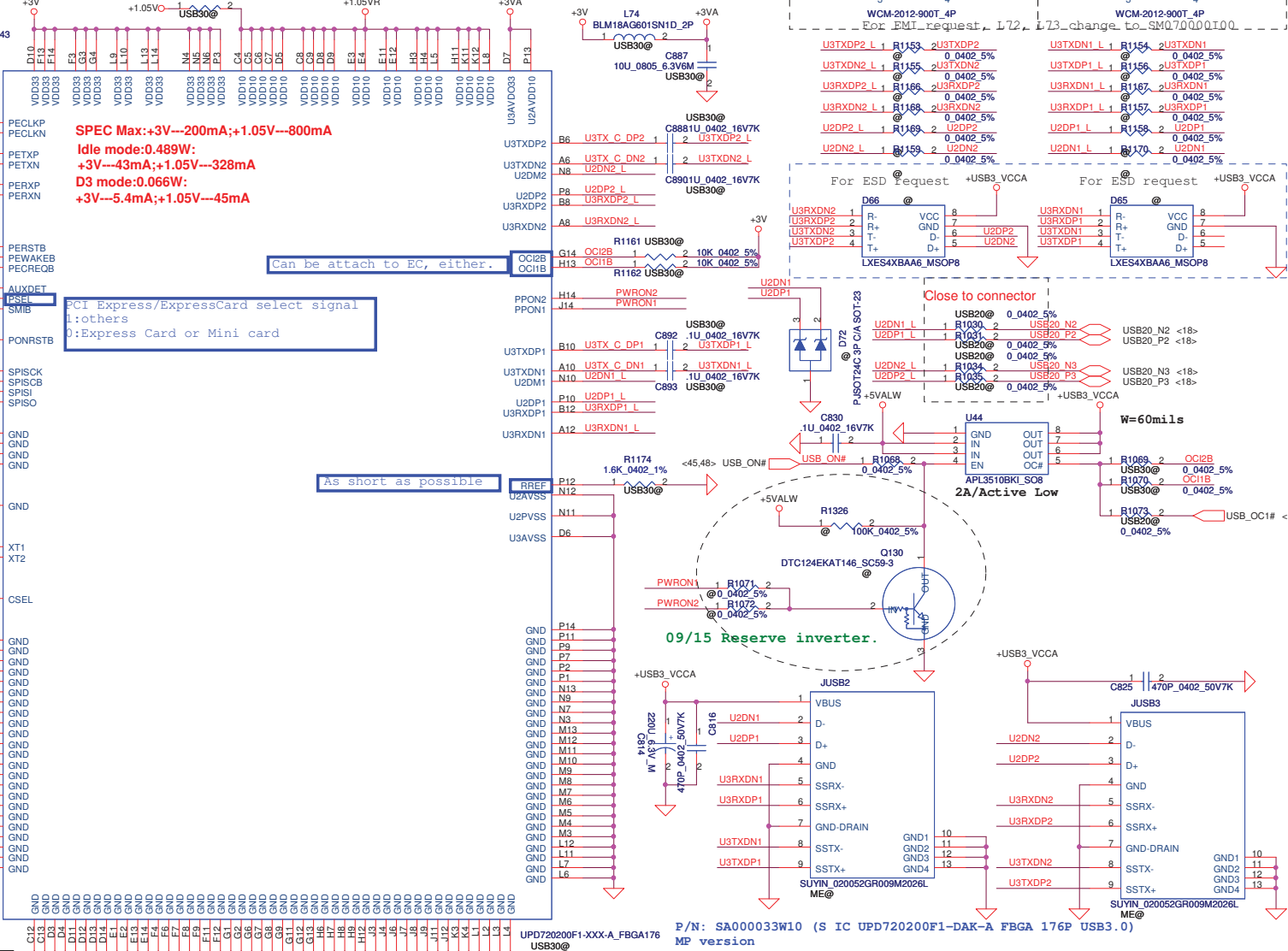
Close to connector

For ESD request +USB3 VCCA

Close to connector

Pin compare table for support USB remote wakeup or not

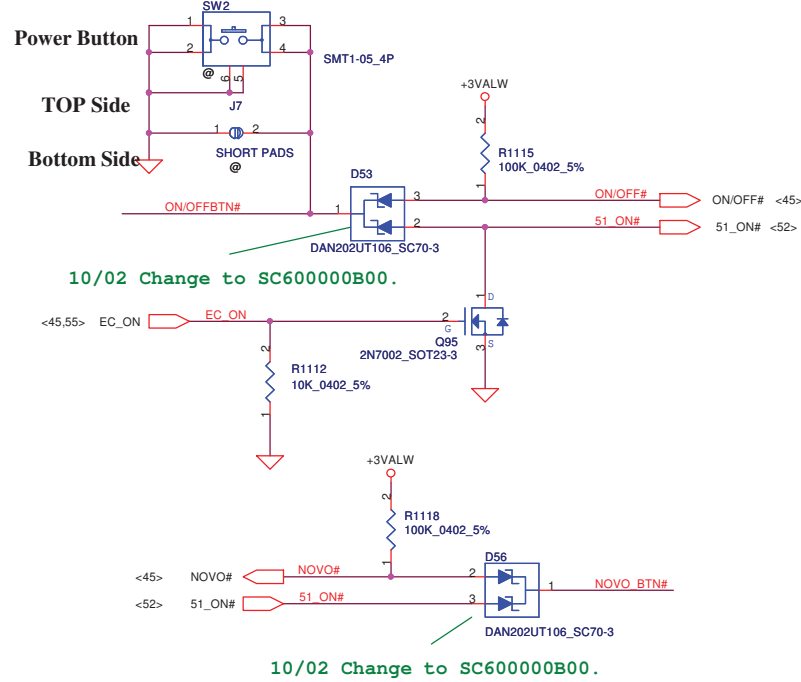
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25



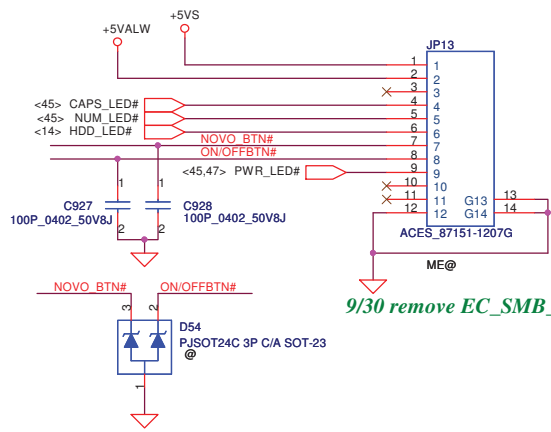
P/N: SA00033W10 (S IC UPD720200F1-DAK-A FBGA 176P USB3.0) MP version

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ON/OFF switch

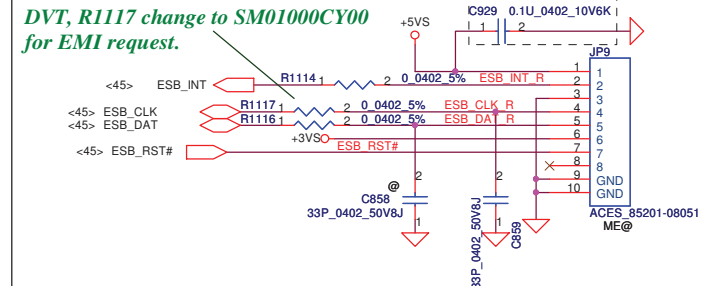


Power Bottom Board Conn. 10pin

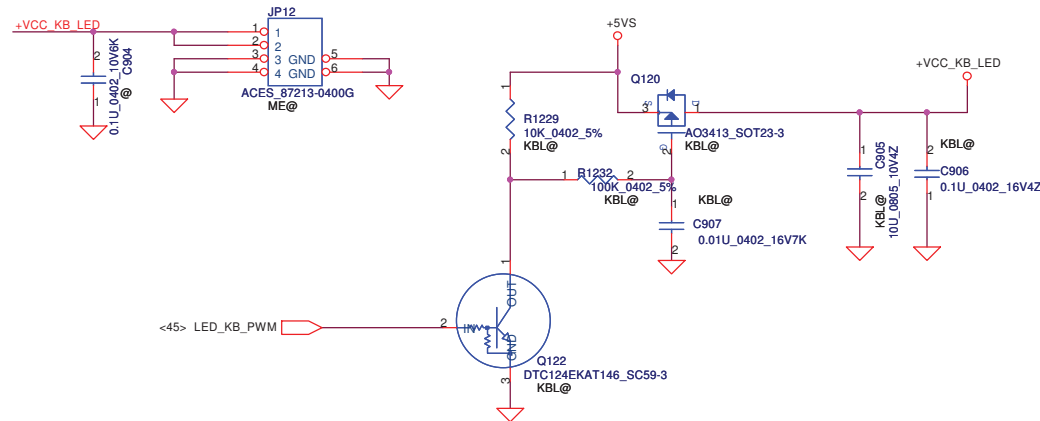


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Slider Bar Board Module Conn. 6pin

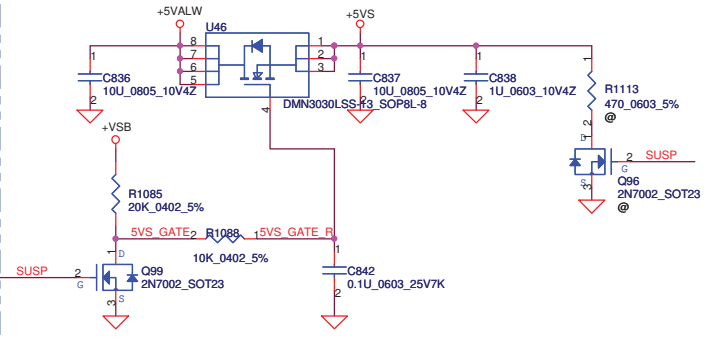


KB Lighting CONN.4pin

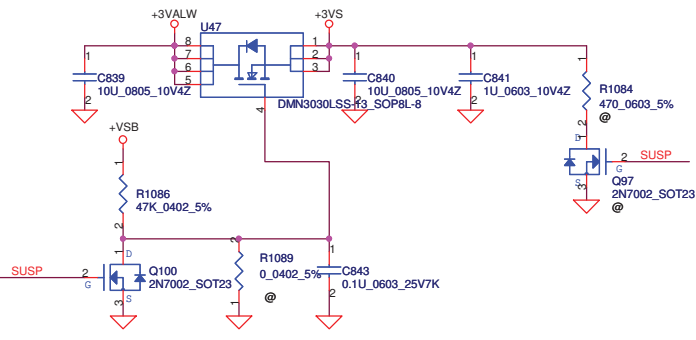


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Size Custom	Document Number	PIQY0 LA6881P		Rev 1.0
Date: Wednesday, January 05, 2011	Sheet	50	of	63

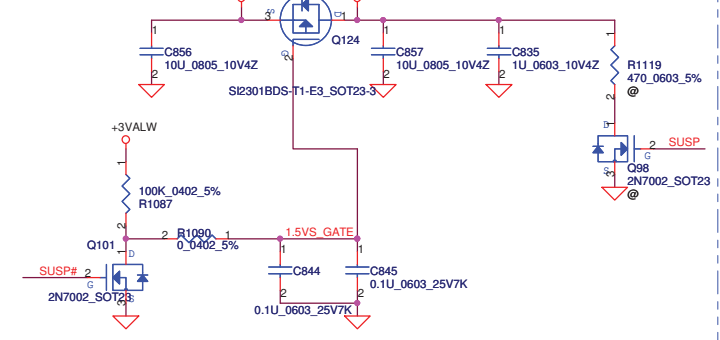
+5VALW TO +5VS



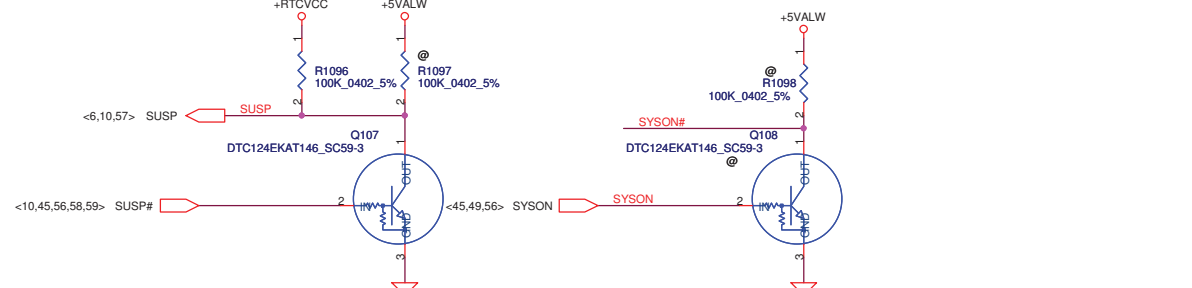
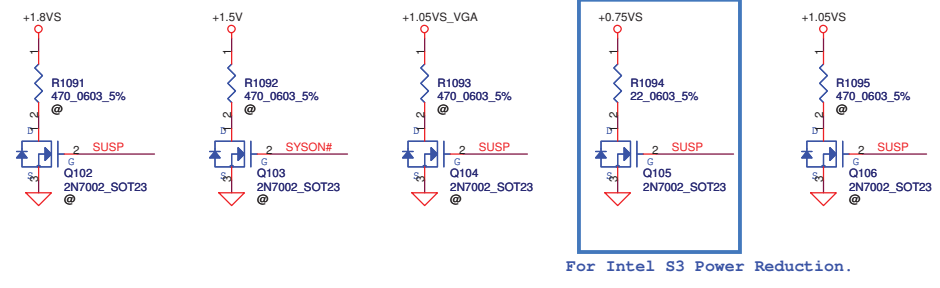
+3VALW TO +3VS



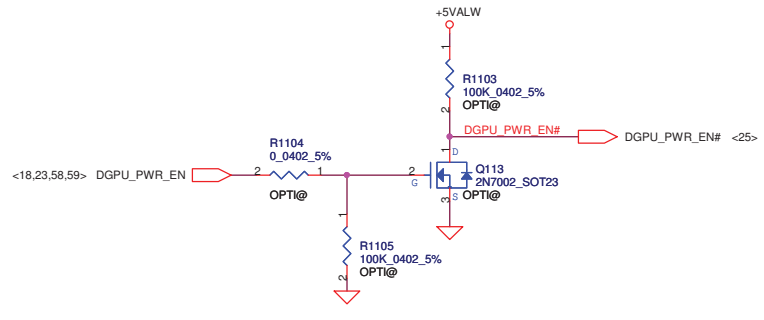
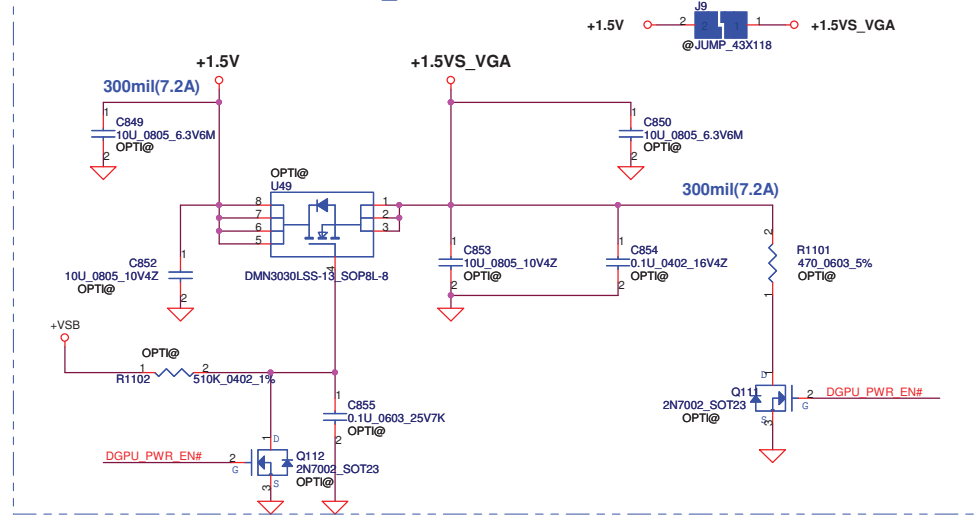
+1.5V to +1.5VS



7/26 change SI4800 to SI2301

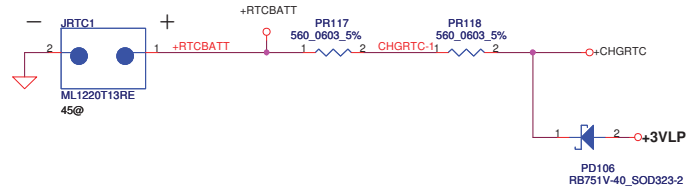
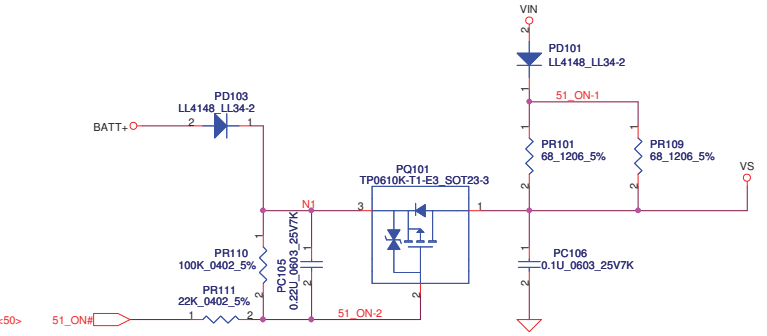
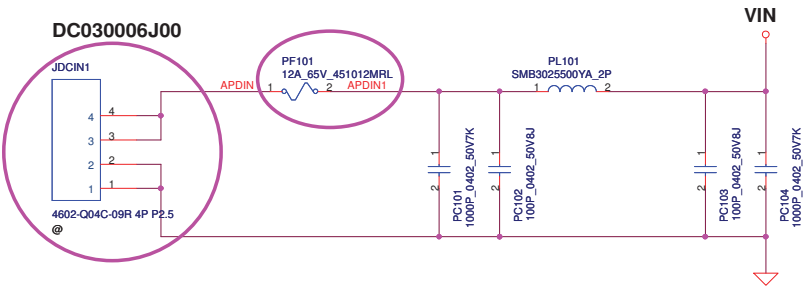


+1.5V to +1.5VS_VGA Transfer

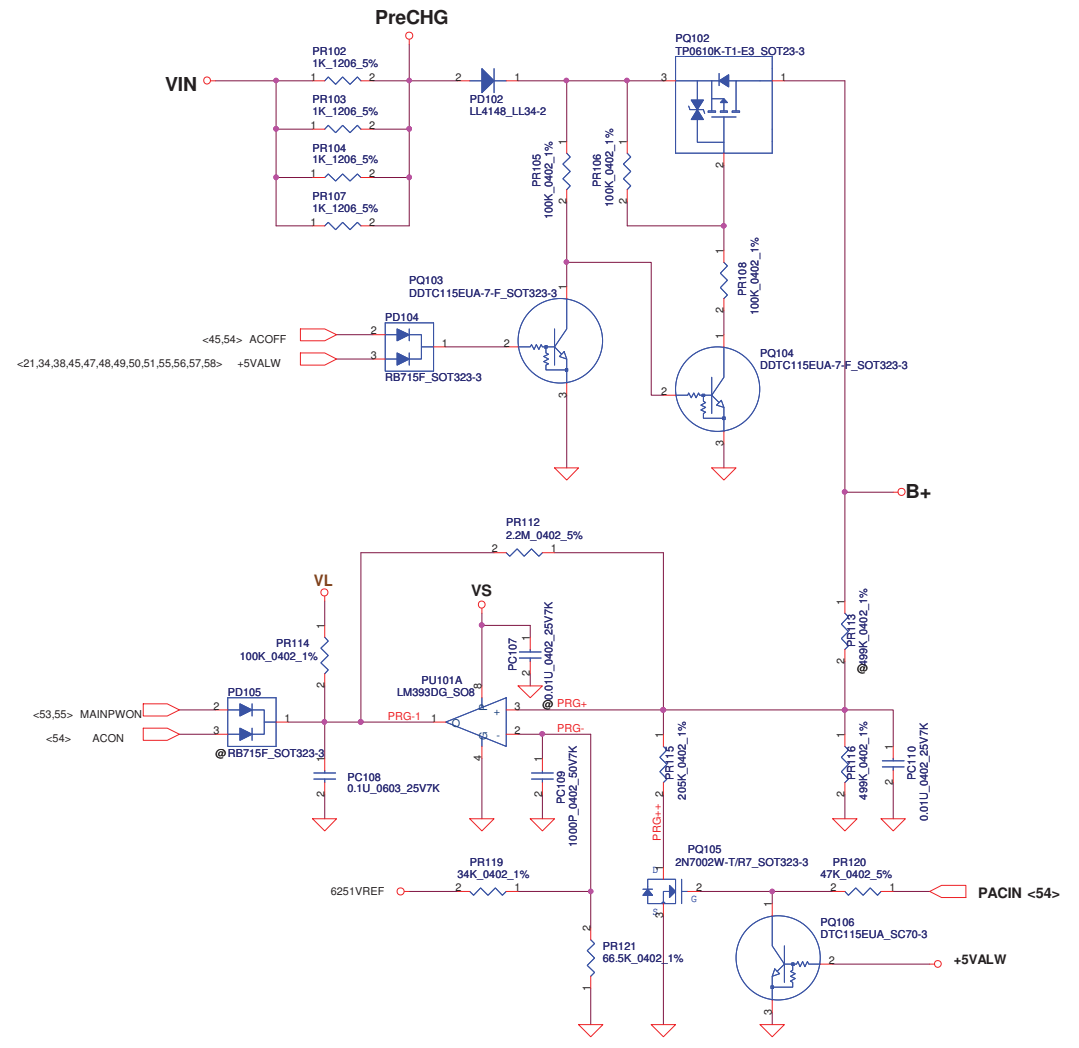


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Size	Document Number	Date		Sheet	Rev
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				of	63

DC030006J00



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**



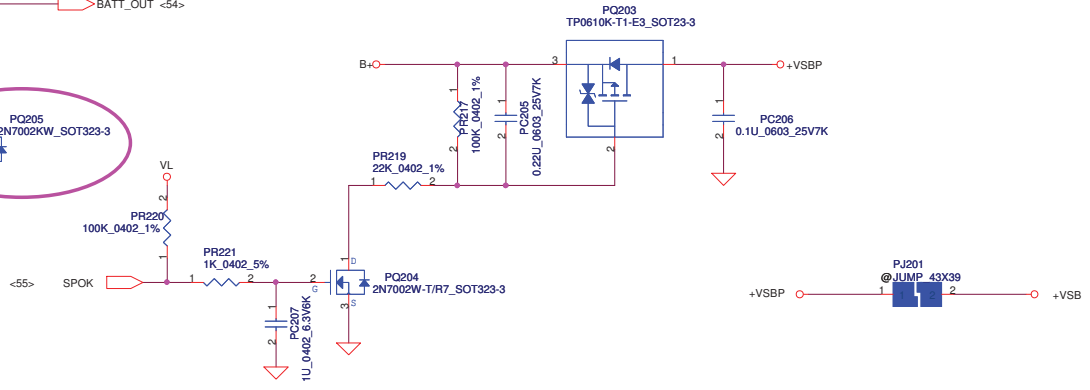
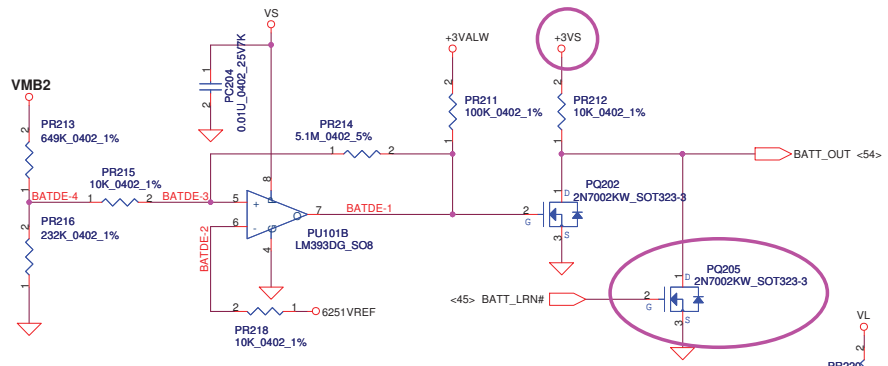
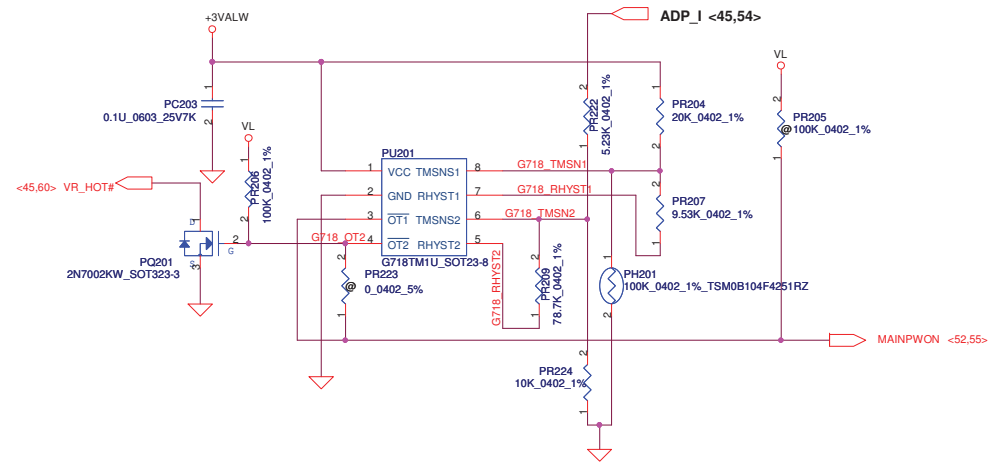
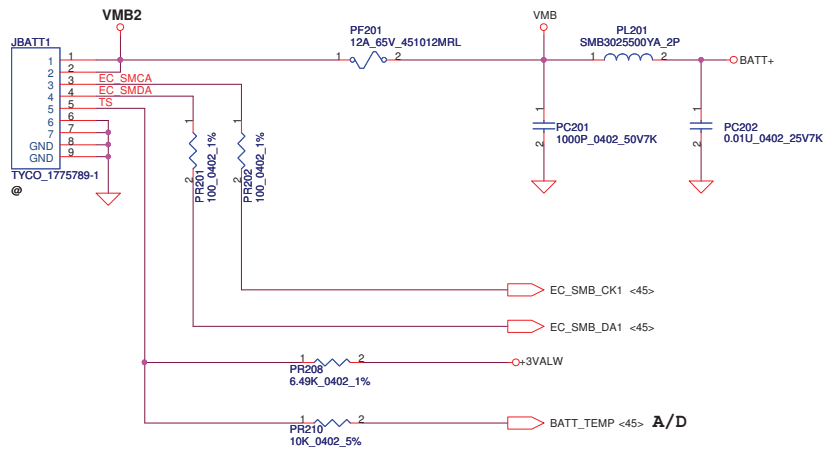
ACIN

Precharge detector		
Min.	typ.	Max.
L-->H	14.991V	15.381V
H-->L	13.860V	14.247V

BATT ONLY

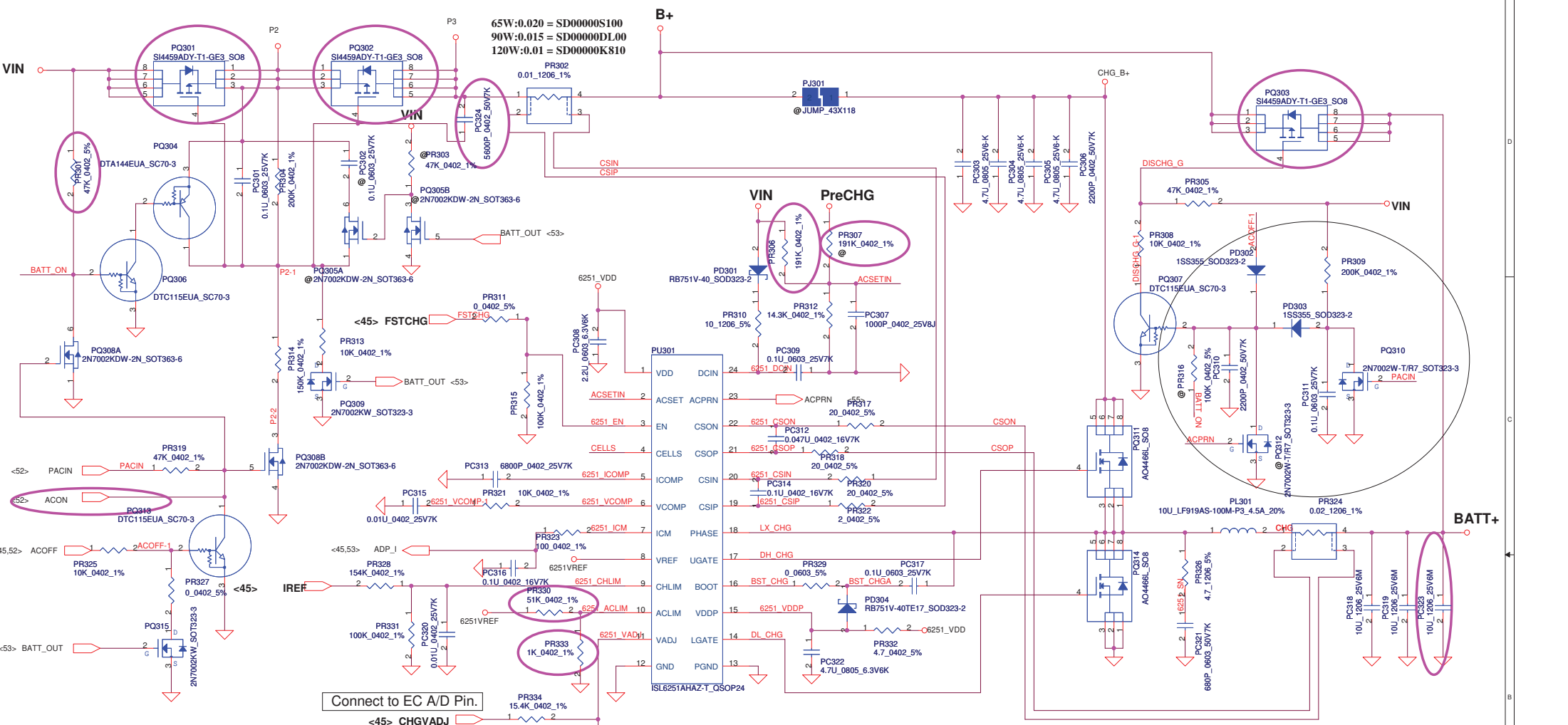
Precharge detector		
Min.	typ.	Max.
L-->H	7.196V	7.349V
H-->L	6.138V	6.214V

PH201 under CPU bottom side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



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Compal Electronics, Inc. PWR-BATTERY CONN/OTP		
Title	PIQY0/Y1	
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65W:0.020 = SD00000S100
 90W:0.015 = SD00000DL00
 120W:0.01 = SD00000K810

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

65W Adapter
 $V_{aLim}=2.39 \times (1.96K / (1.96K + 16.9K)) = 0.2484V$
 $I_{inPut} = (1/0.02) \times ((0.05 \times V_{aLim}) / (2.39 + 0.05))$
 where $V_{aLim} = 0.2484V$, $I_{inPut} = 2.76A$

90W Adapter
 $V_{aLim} = 2.39 \times (2.87K / (2.87K + 16.9K)) = 0.347V$
 $I_{inPut} = (1/0.015) \times ((0.05 \times V_{aLim}) / (2.39 + 0.05))$
 where $V_{aLim} = 0.347V$, $I_{inPut} = 3.82A$

120W Adapter
 $V_{aLim} = 2.39 \times (1K / (1K + 50K)) = 0.047V$
 $I_{inPut} = (1/0.01) \times ((0.05 \times V_{aLim}) / (2.39 + 0.05))$
 where $V_{aLim} = 0.047V$, $I_{inPut} = 5.1A$

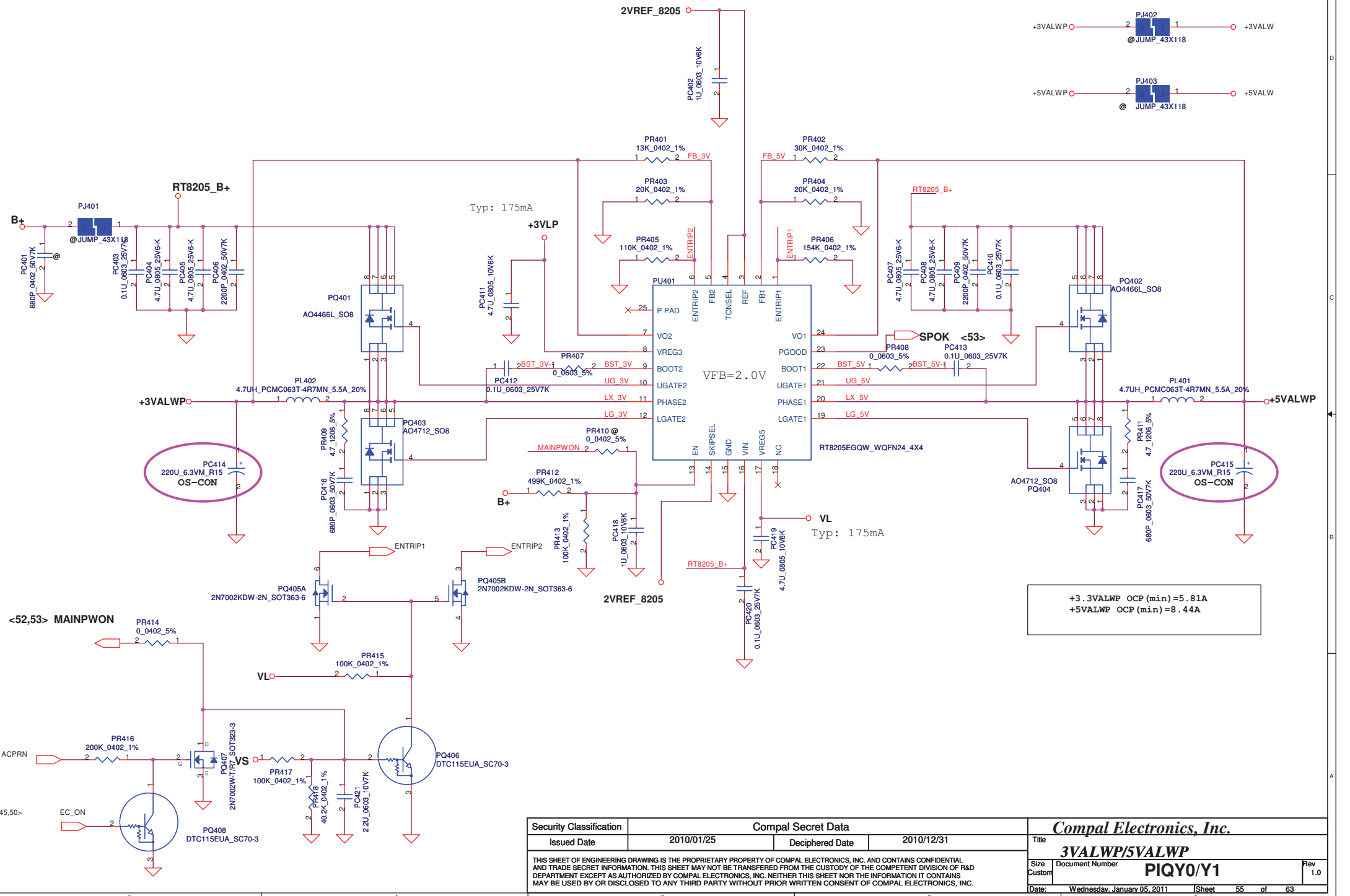
65W : PR330=16.9K, PR333=1.96K
 90W : PR330=16.9K, PR333=2.87K
 120W : PR330=50K, PR333=1K

Connect to EC A/D Pin.

3cell : GND
 4cell : VDD

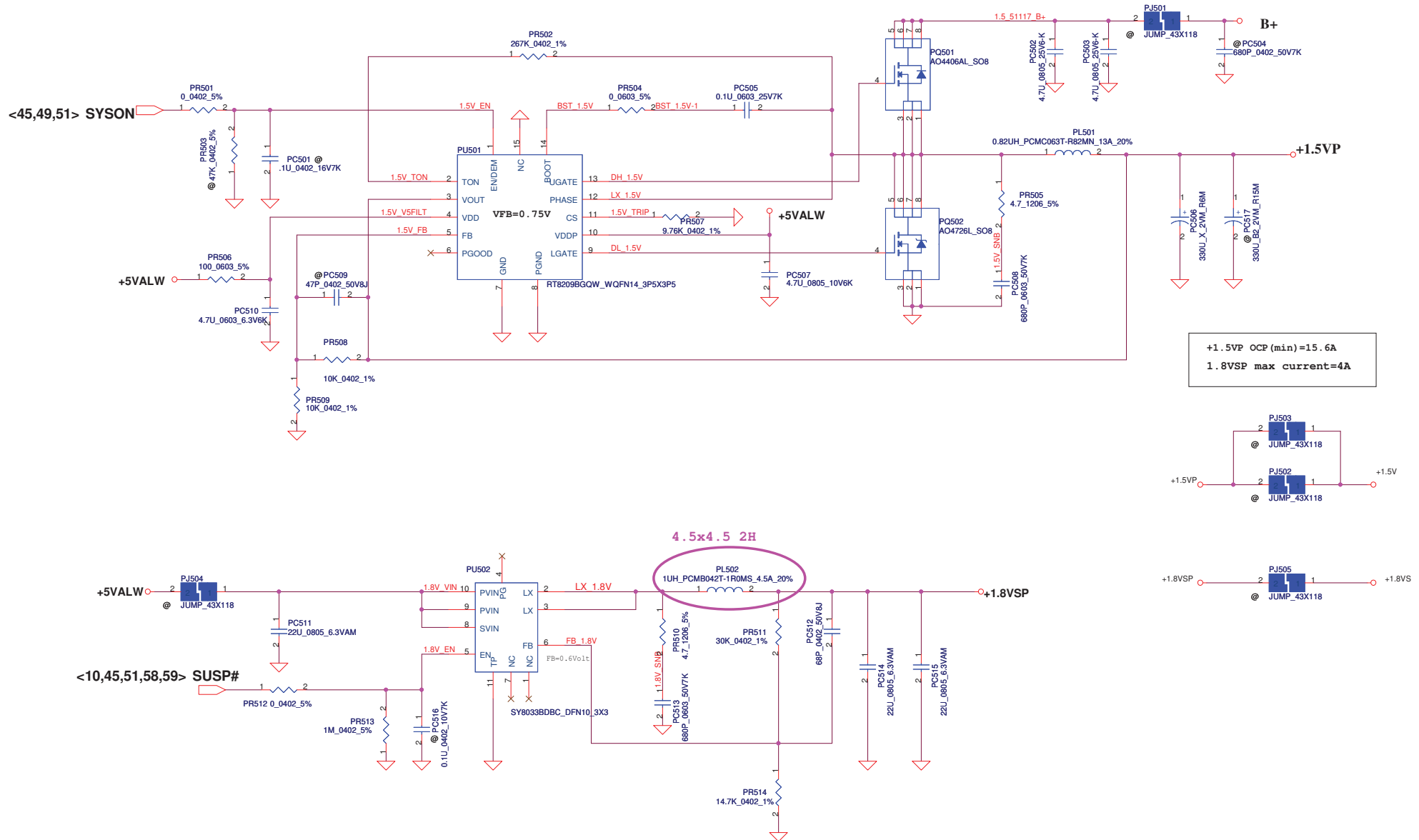
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				PIQY0/Y1	Rev 1.0
				Date: Wednesday, January 05, 2011	Sheet 54 of 63

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO

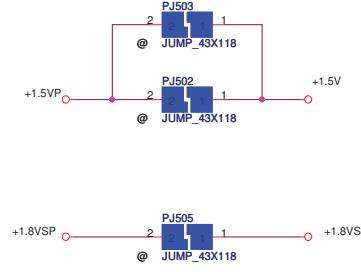


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Compal Electronics, Inc.			
Title	3VALWP/5VALWP		
Size	Document Number	PIQY0/Y1	
Custom			
Date:	Wednesday, January 05, 2011	Sheet	55 of 63
			Rev 1.0

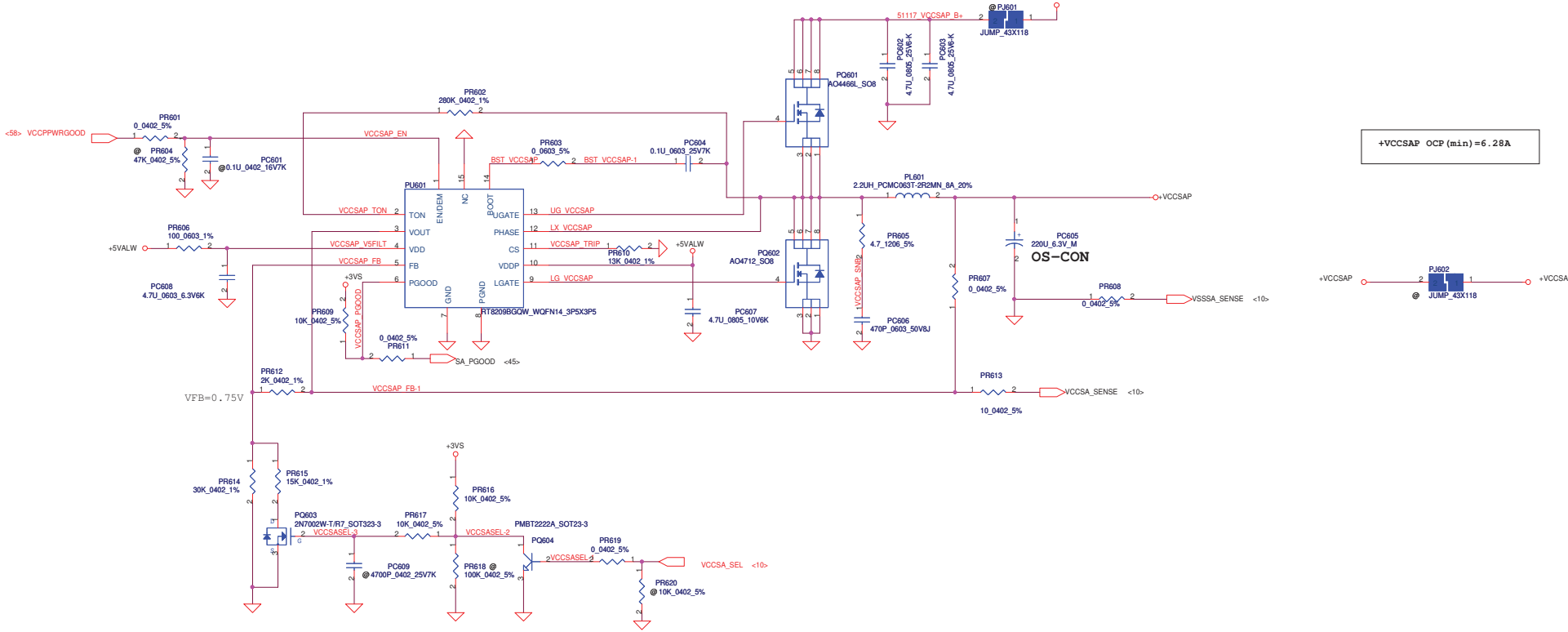


+1.5VP OCP (min)=15.6A
1.8VSP max current=4A



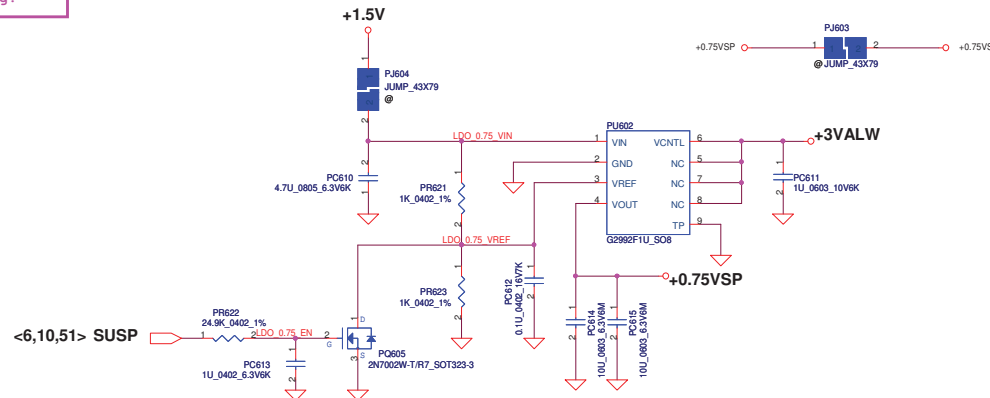
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-+1.5VP/+1.8VSP
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Customer		Rev	1.0	Date:	Wednesday, January 05, 2011
Sheet	56	of	63		

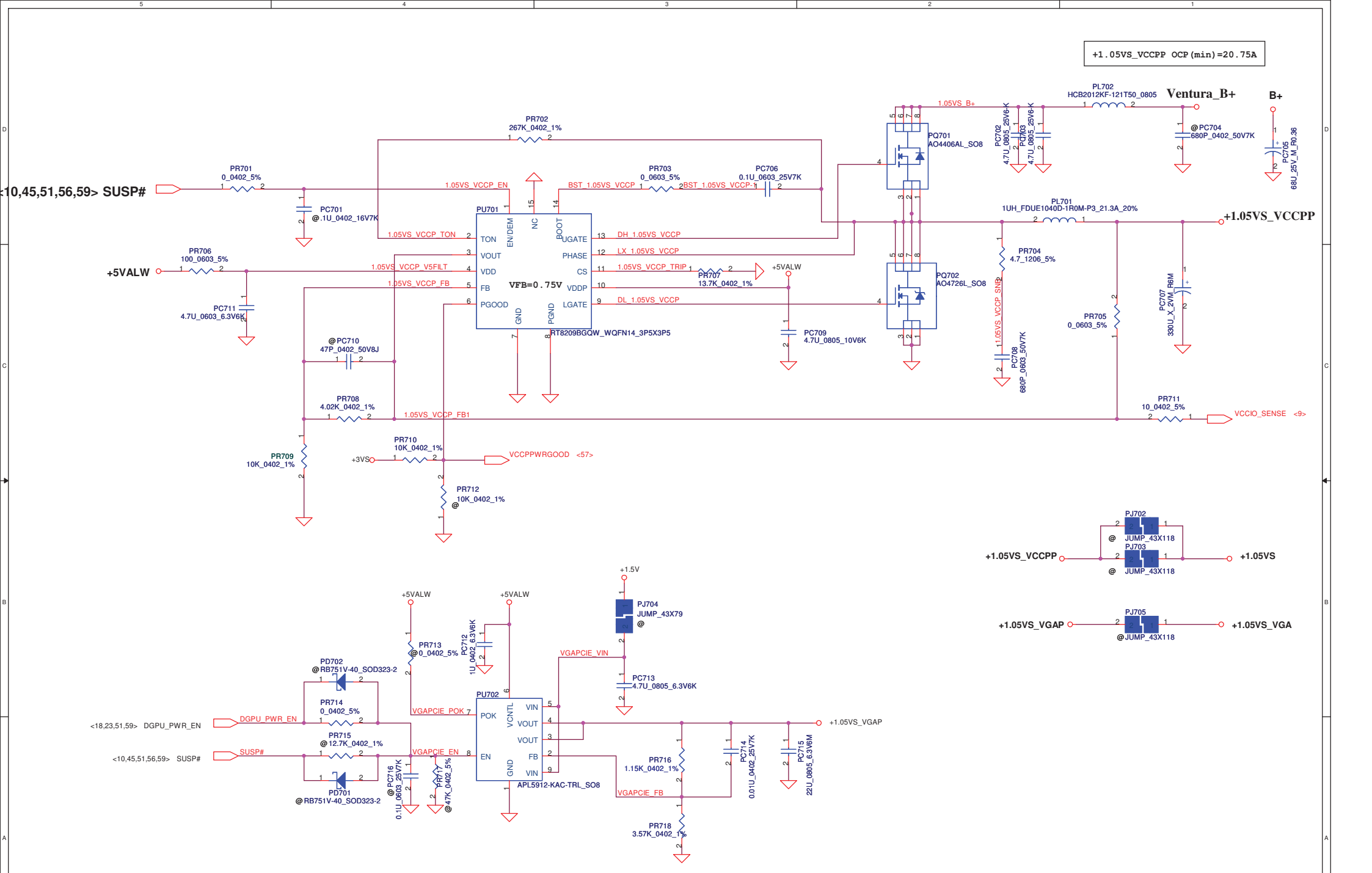
Ventura_B+



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.





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				Date: Wednesday, January 05, 2011	Sheet 58 of 63

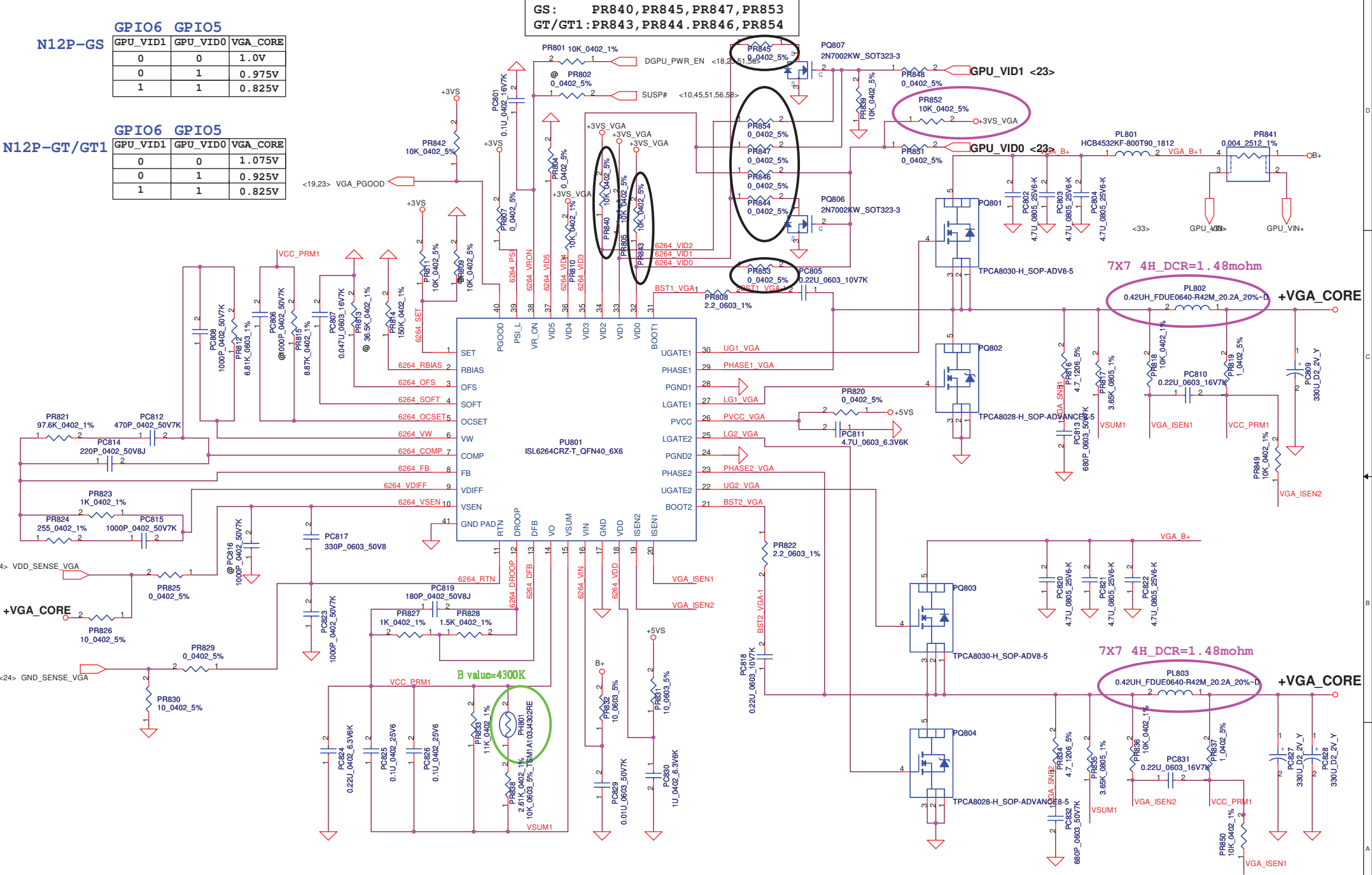
GS: PR840, PR845, PR847, PR853
 GT/GT1: PR843, PR844, PR846, PR854

N12P-GS

GPIO6	GPIO5	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V

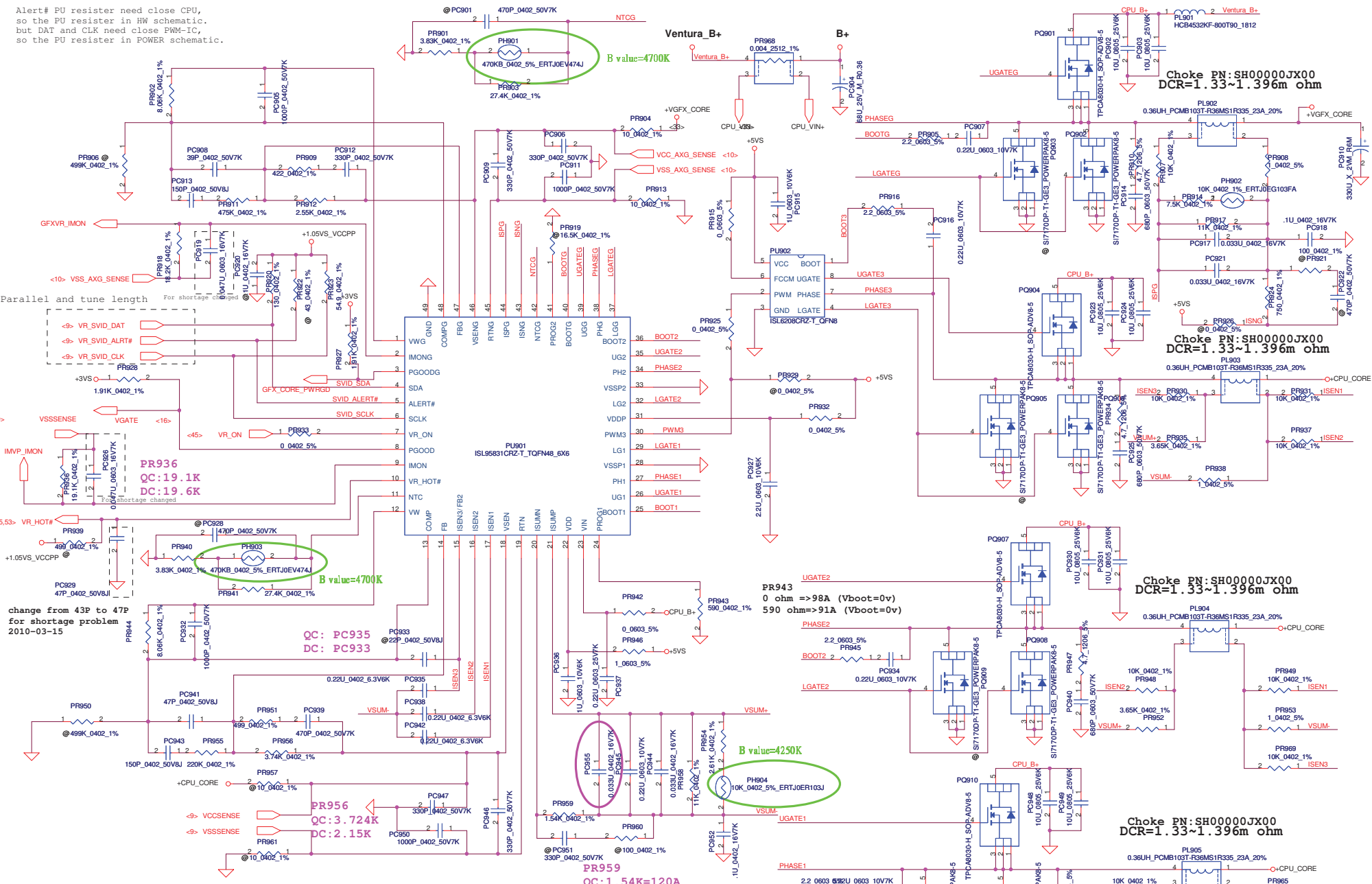


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		2007/12/12

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Compal Electronics, Inc.		
Title		
Power-VGA_CORE		
Size	Document Number	Rev
Custom	PIQY0/Y1	1.0
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Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



Parallel and tune length
For shortage changed

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE	Icc-max=53A
	Rdson=3.6~4.5m ohm
	DCR=1.1m ohm
	HW output cap:
	(1) 10U_0805_4V *10
	(2) 22U_0805_6.3V *15
	(3) 470U_D2_2V *4 (ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP	Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
	Rdson=3.6~4.5m ohm
	DCR=1.1m ohm
	HW output cap:
	(1) 22U_0805_6.3V *12
	(2) 470U_D2_2V *2 (ESR=4.5m ohm)

*OCP setting value=37A

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Compal Electronics, Inc.	
Title PWR+CPU_CORE+VGFX_CORE	
Size Custom	Document Number PIQY0/Y1
Date: Wednesday, January 05, 2011	Sheet 60 of 63

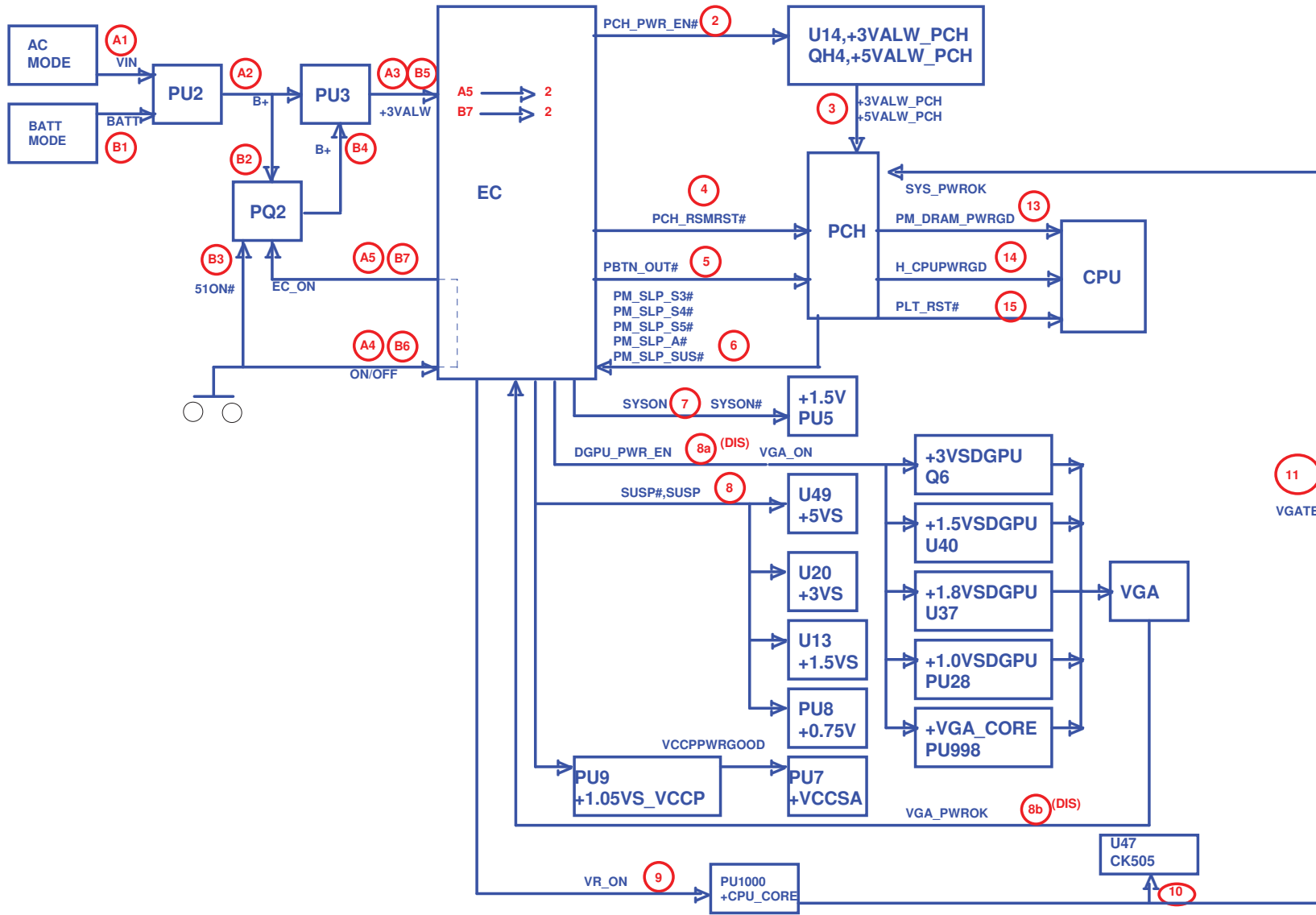
Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/06	Deciphered Date	2009/01/06	PIR (PWR)	
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				Custom	PIQY0/Y1
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				Rev	1.0

PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- DVT TO DVT				
1		P18	Reserve R297	Reserve pull down for PCH GPIO53.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
			Delete U55, C908, R1233, R1235, R1236, 1238, R1230, R1231, Q121	
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GPIO1.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swich control inverter circuit.
7		P48	Add R1327	For CHG_ON# pull down.
8		P45	Stuff R996, R139, C815, unstuff R1000, C732, C733, Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GPIO12.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342, R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
----- DVT TO PVT				
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail
----- PVT TO SVT				
1		P23, P45	FAST_BOOT#	Link FAST_BOOT# to VGA GPIO12
2		P50	Add C929	EMI Request
2		P14	Add R1348	INTEL Design Guide update

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				Size Custom	Document Number
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Title		Compal Electronics, Inc.	
		Power sequence	
Size	Document Number	Rev	
Custom	PIQY0 LA6881P	1.0	
Date:	Wednesday, January 05, 2011	Sheet	63 of 63