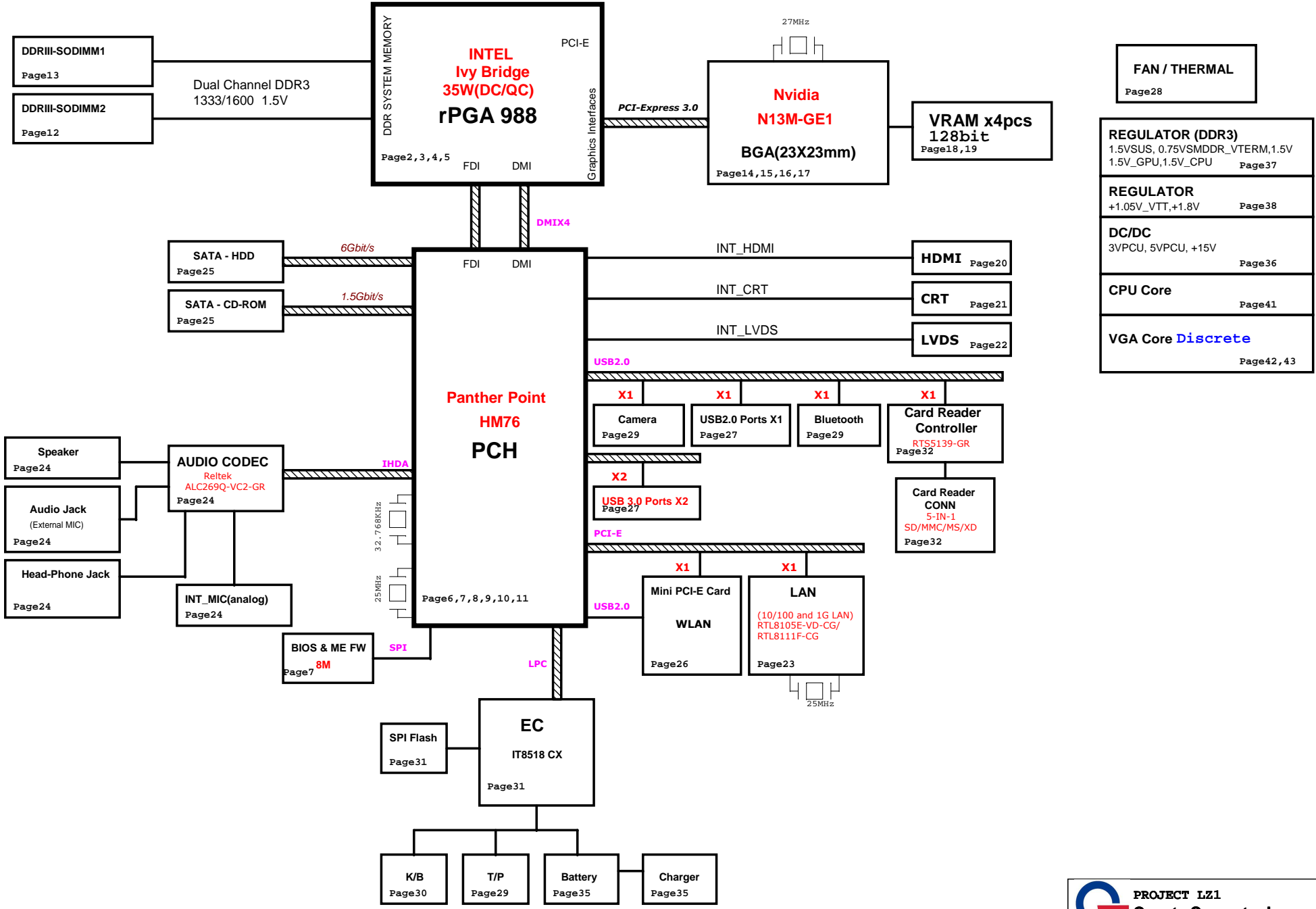
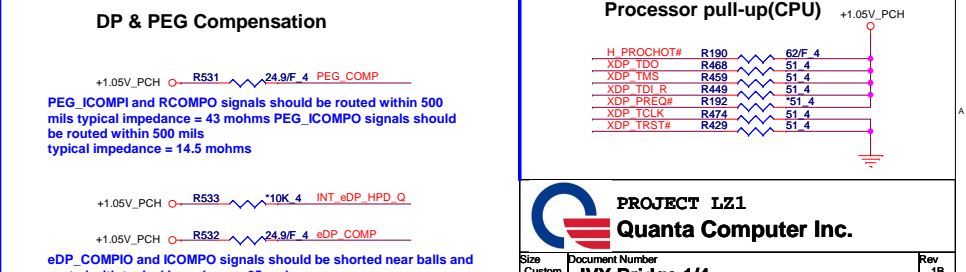
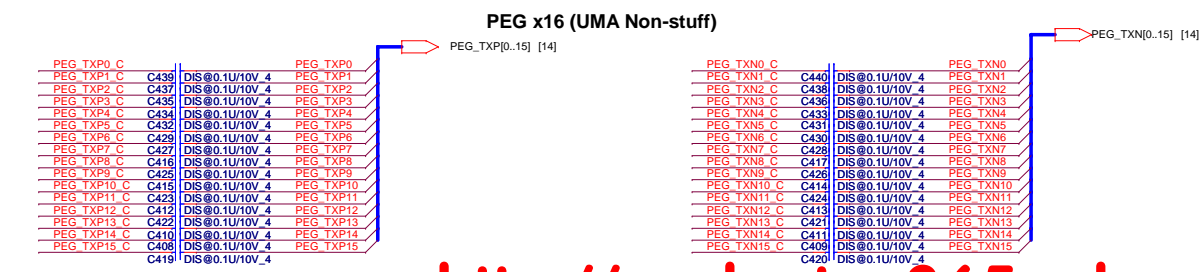
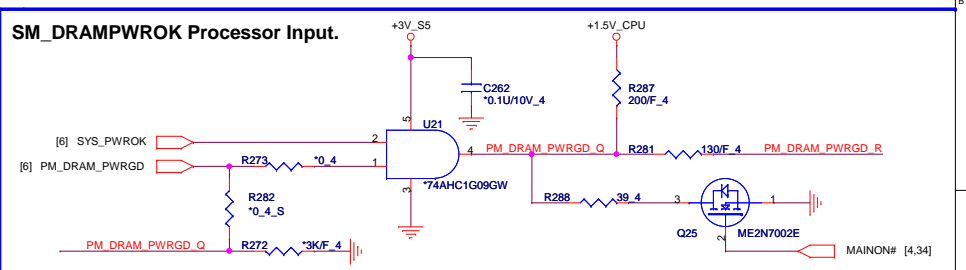
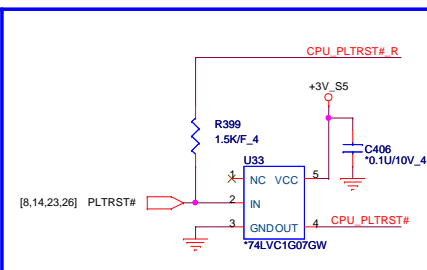
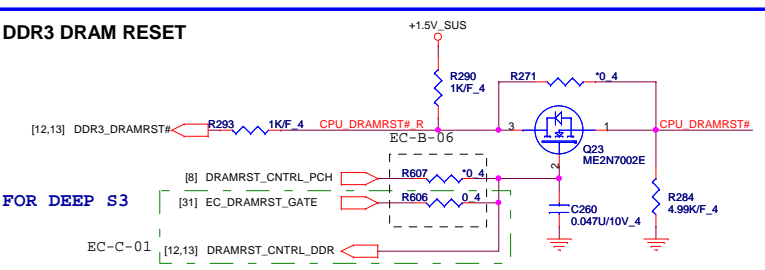
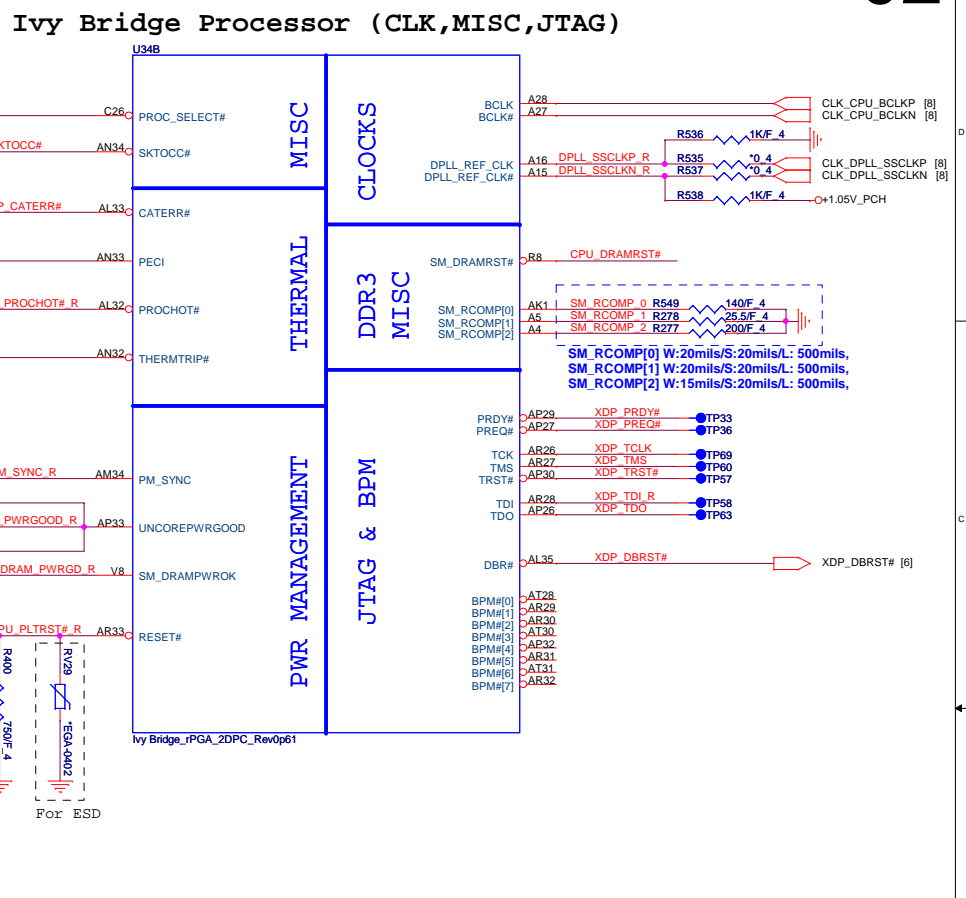
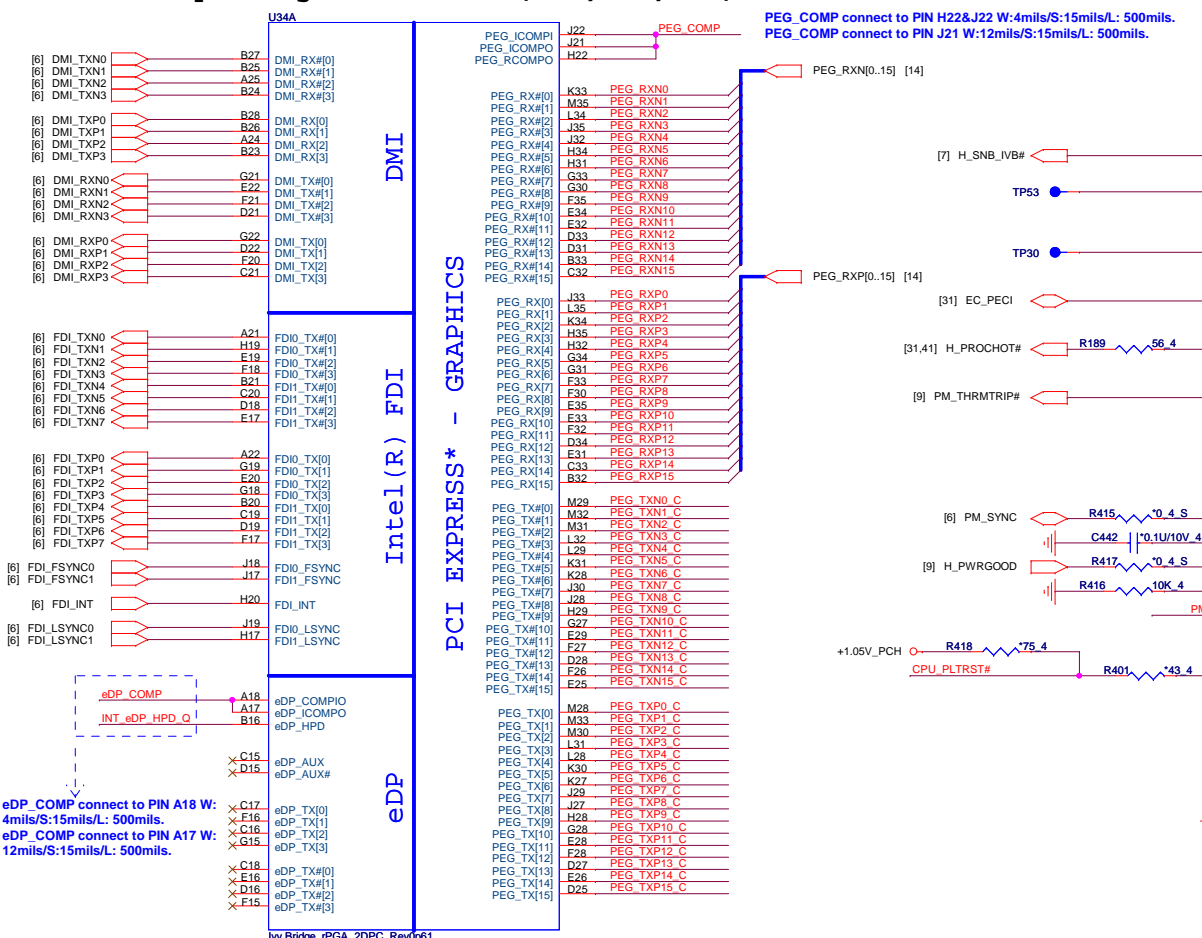


LZ1/LZ1A(Z380) Intel Chief River Platform (Optimus) Block Diagram

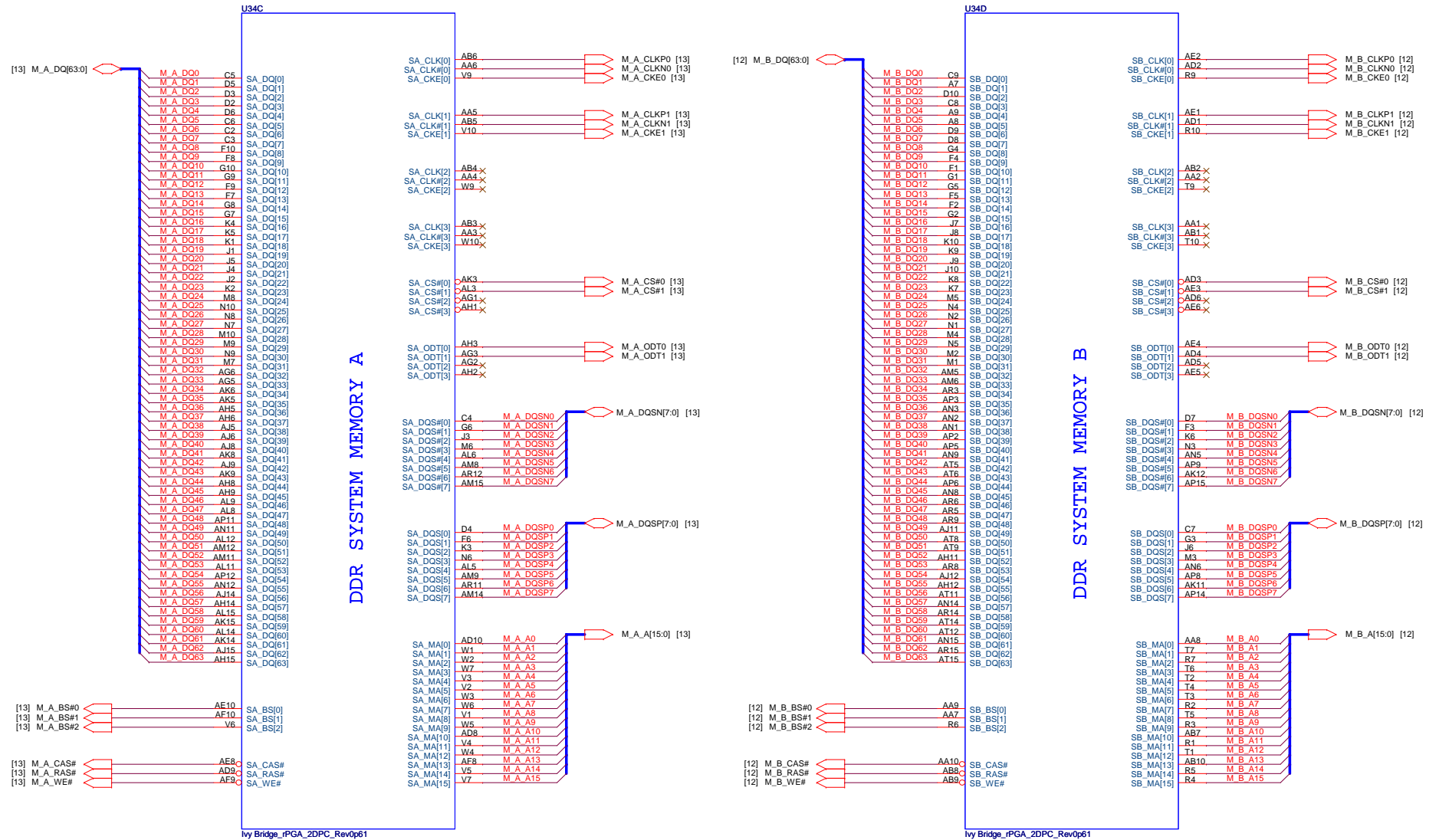


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Ivy Bridge Processor (DDR3)

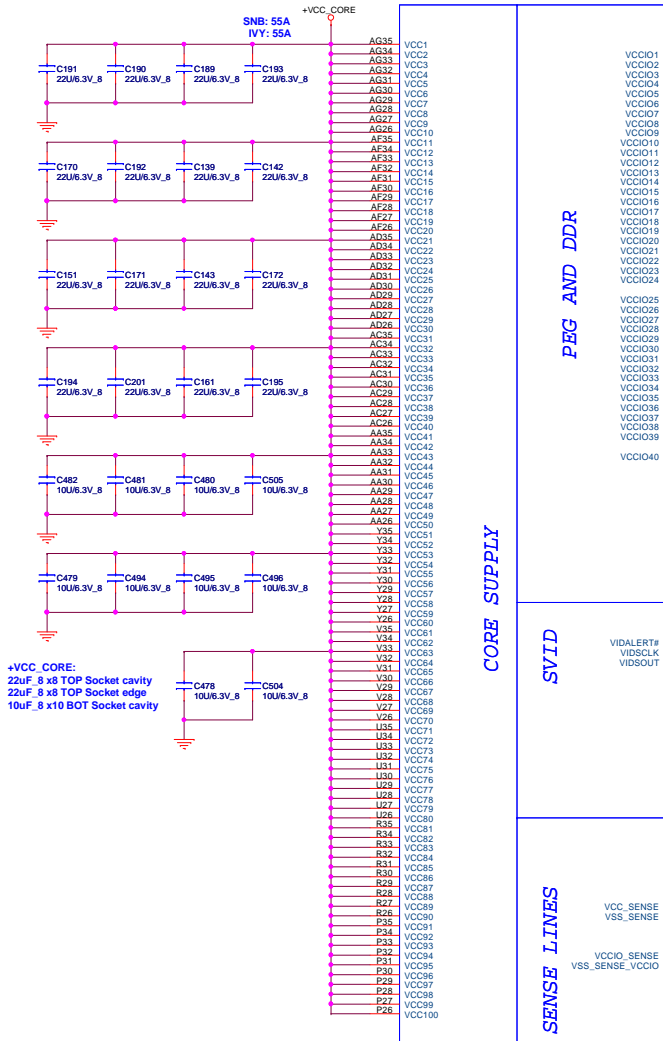


Ivy Bridge_rPGA_2DPC_Rev0p61

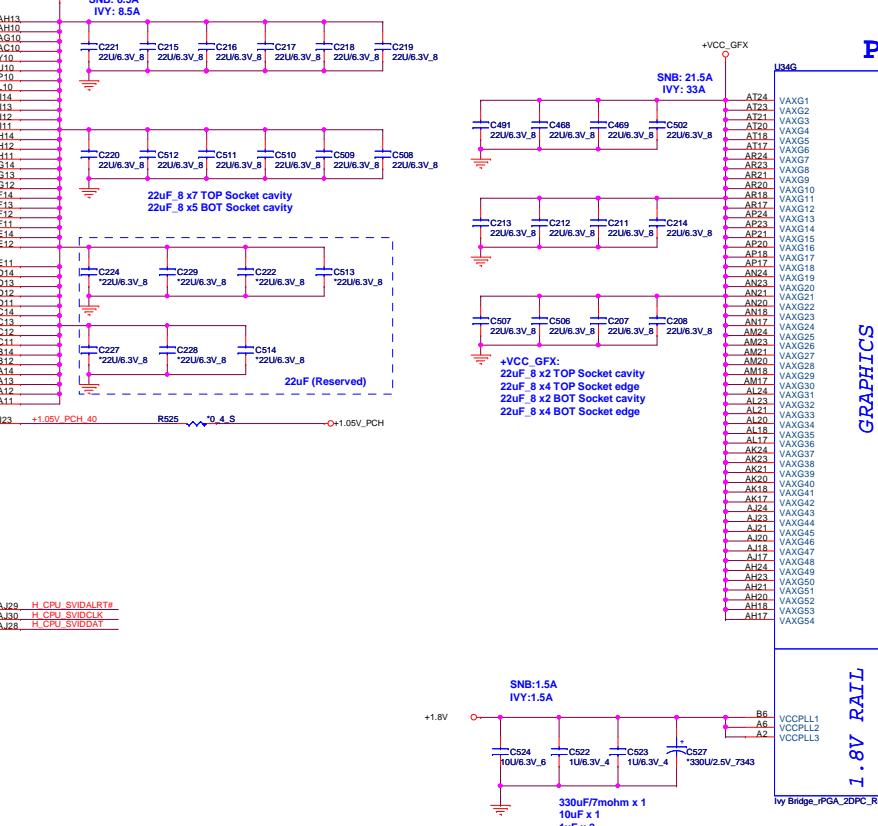
Ivy Bridge_rPGA_2DPC_Rev0p61

[33.41] +VCC_CORE
 [2,10,12,13,33,34,37,43] +1.05V_PCH
 [P] +1.5V_CPU
 [10,26] +1.5V
 [7,10,34,40] +1.8V
 [34,39] +0.85V
 [33.41] +VCC_GFX

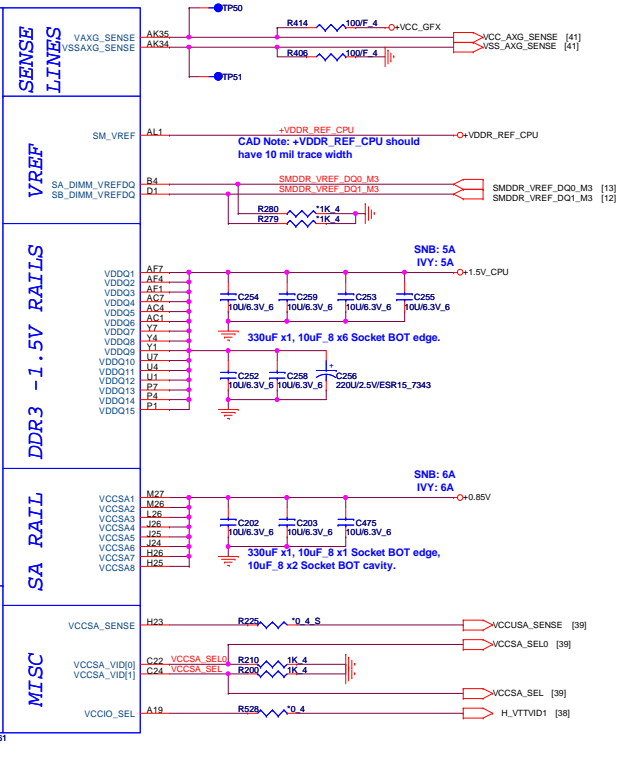
POWER



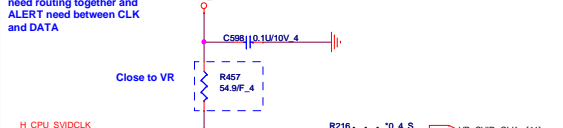
Ivy Bridge Processor (GRAPHIC POWER)



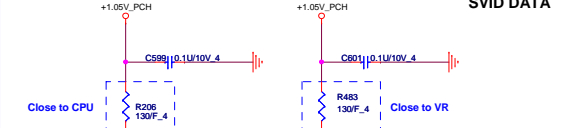
POWER



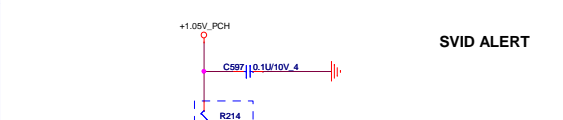
SVID CLK



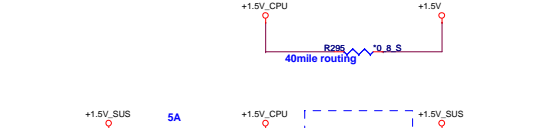
SVID DATA



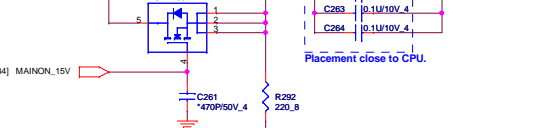
SVID ALERT



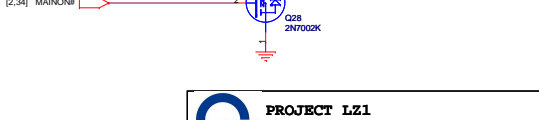
SVID CLK



SVID DATA



SVID ALERT



+VCC_CORE:
 22uF_8 x8 TOP Socket cavity
 22uF_8 x8 TOP Socket edge
 10uF_8 x10 BOT Socket cavity

Trace Route to Power IC area.

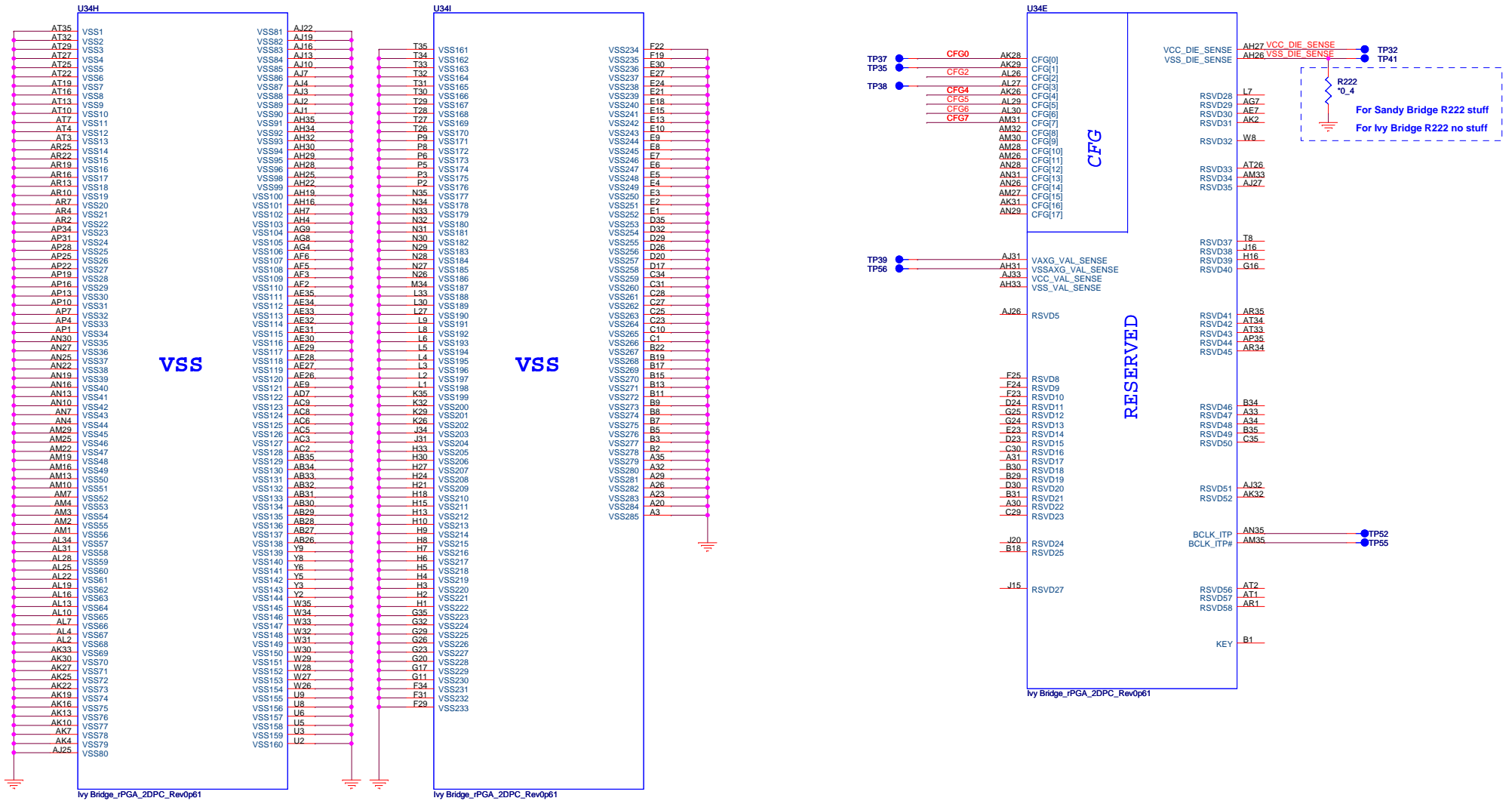
VTT_SENSE R276 10F_4
 VSSP_SENSE R275 10F_4

Layout note:
 need routing together and
 ALERT need between CLK
 and DATA

Close to VR

Close to CPU

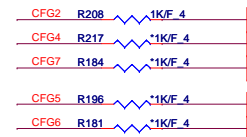
Close to CPU



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

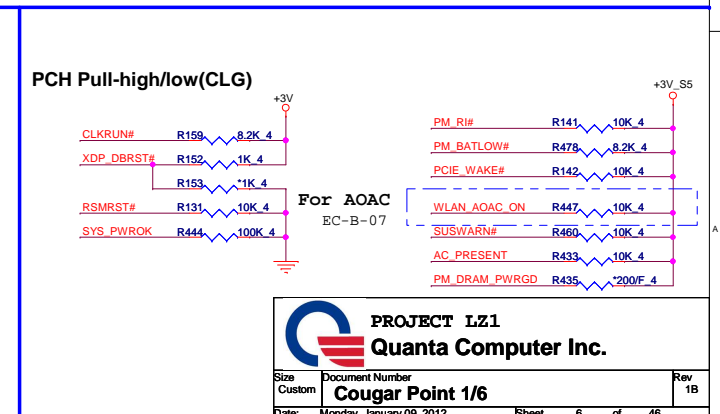
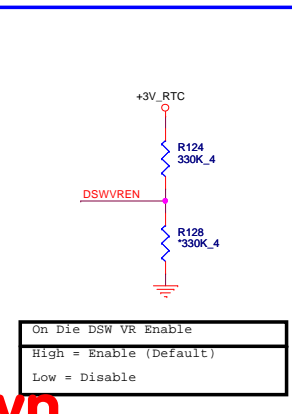
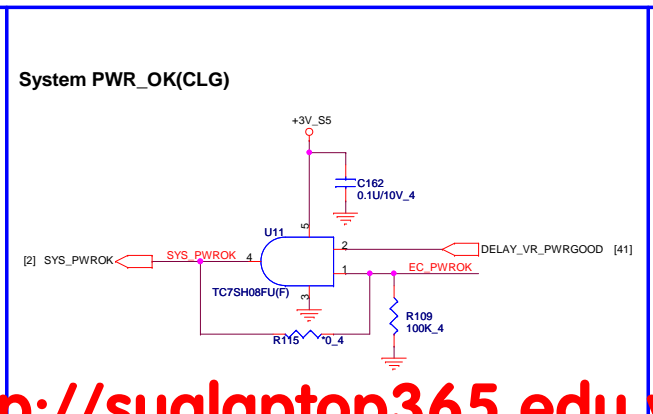
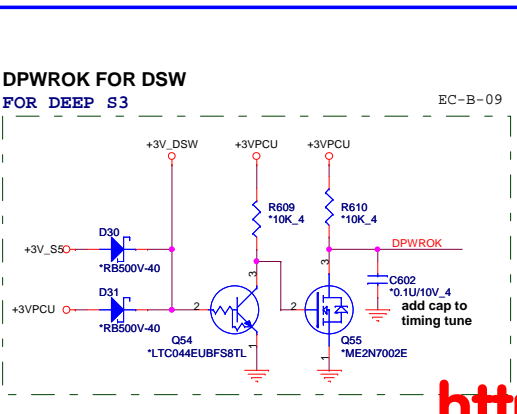
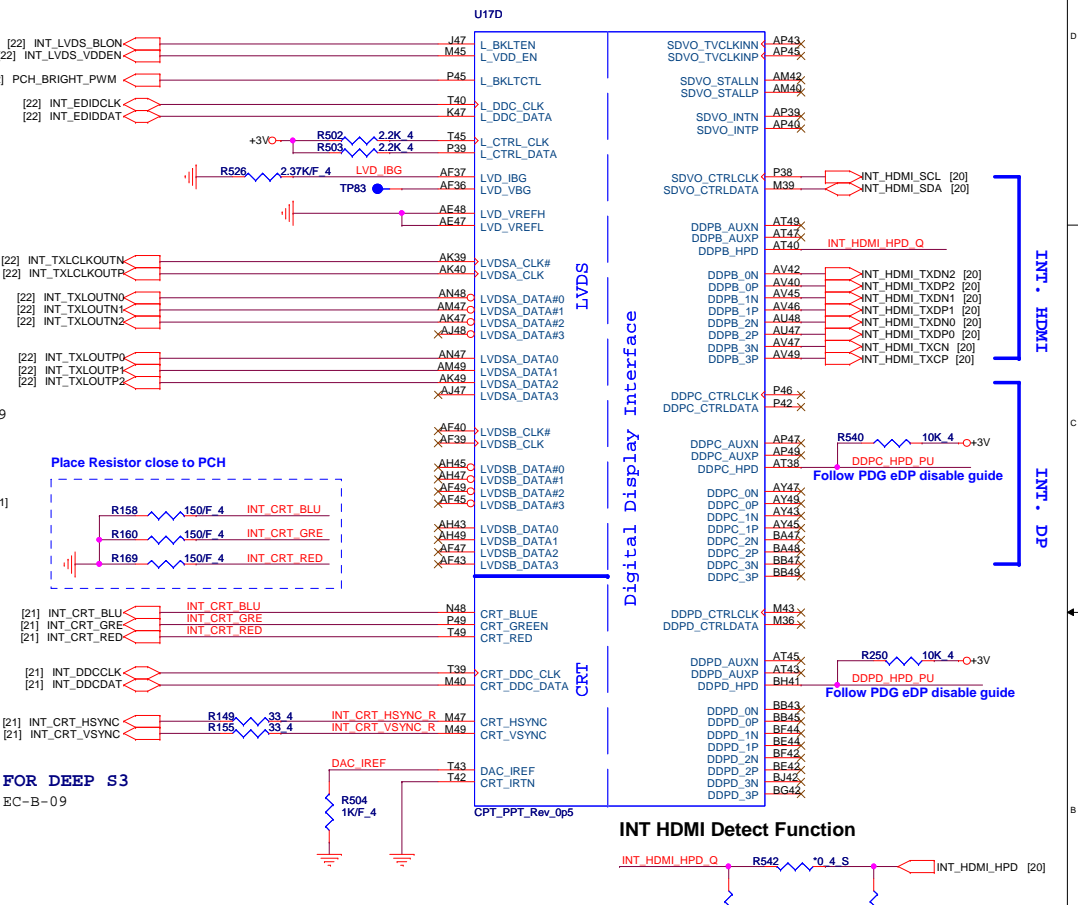
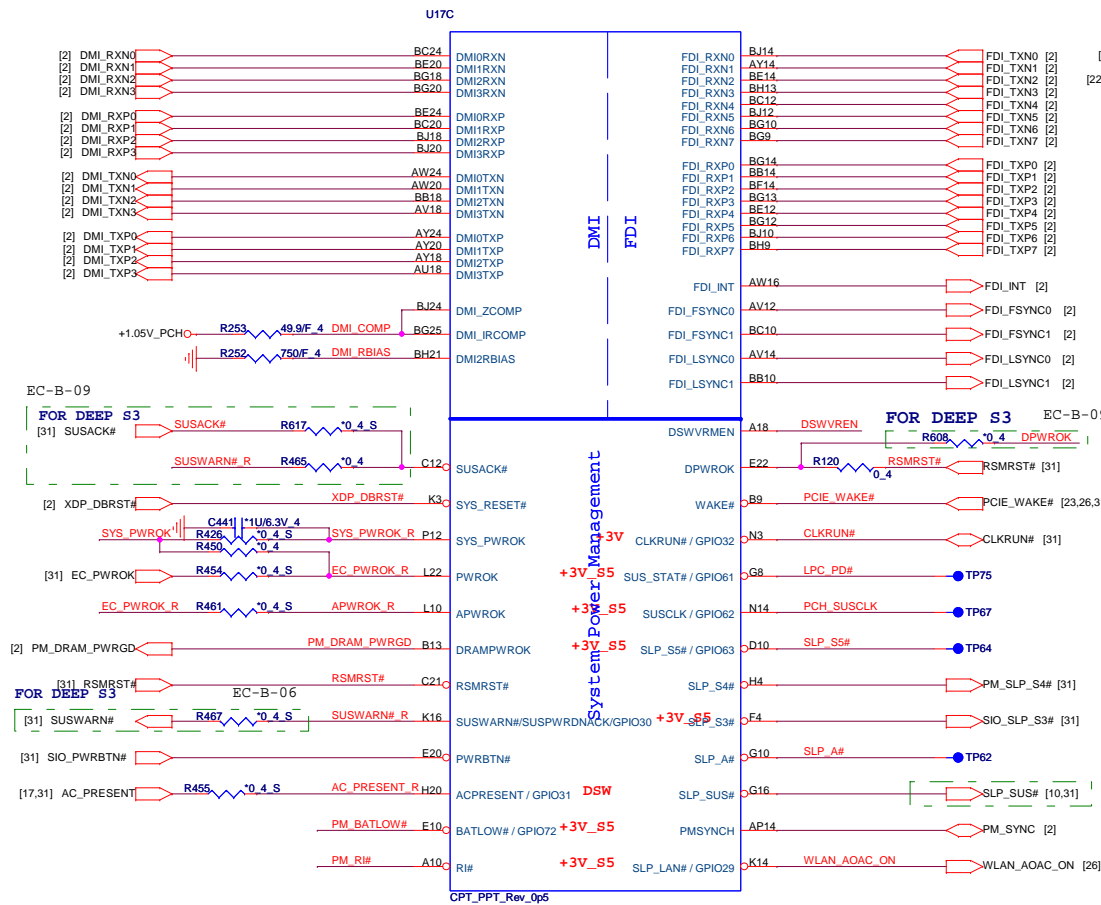
- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
- 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT LZ1
Quanta Computer Inc.

Size: Custom Document Number: **IVY Bridge 4/4** Rev: 1B
 Date: Monday, January 09, 2012 Sheet: 5 of 46

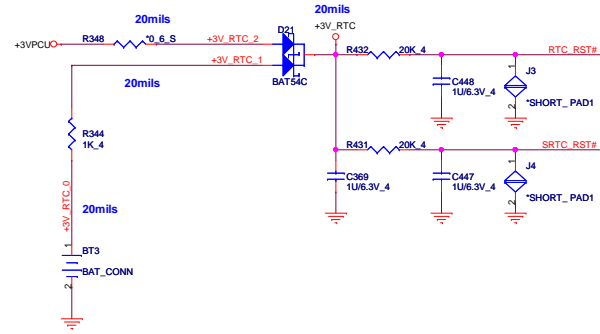
Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

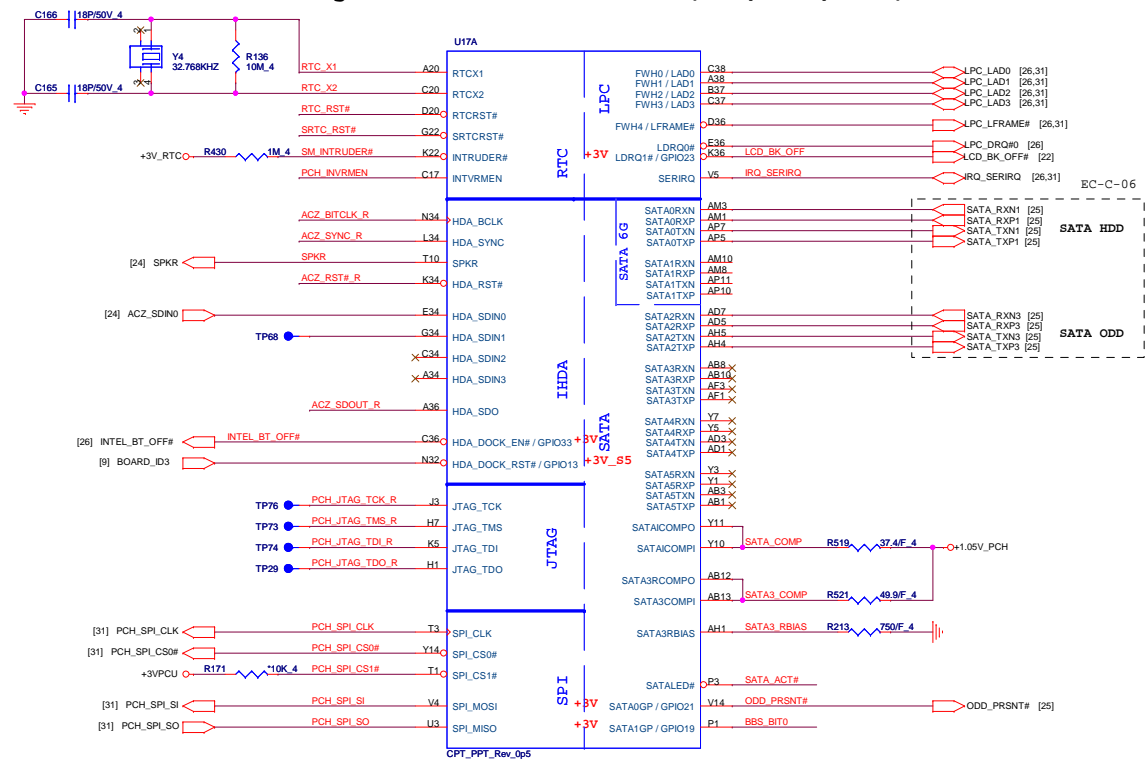


On Die DSW VR Enable
 High = Enable (Default)
 Low = Disable

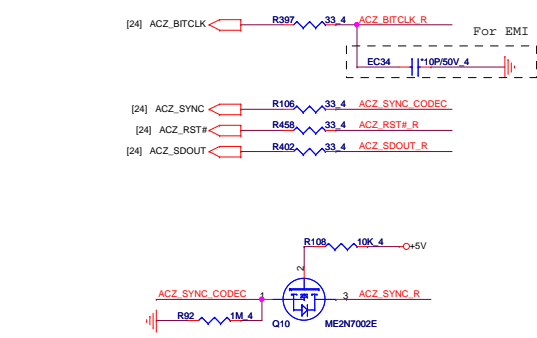
RTC Circuitry(RTC)



PCH2(CLG)

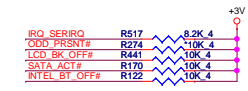


HDA Bus(CLG)

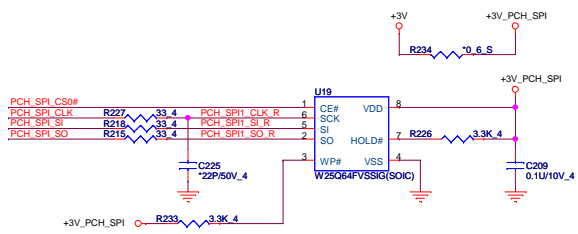


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V _{PCU} - R515 - *1K_4 - SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R486 - *1K_4 - PCH_GNT3# [8]									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R129 - 330K_4 - PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R479 - *1K_4 - BBS_BIT1 [8] R167 - *1K_4 - BBS_BIT0									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 - R413 - *1K_4 - ACZ_SDOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R251 - 2.2K_4 - +1.8V R250 - *1K_4 - DF_TVS [9] R_SAB_VB# [2]									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R496 - *1K_4 - PLL_ODDR_EN [9]									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 - R90 - *1K_4 - ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V _{PCU} - R209 - *1K_4 - PCH_SPL_SI									
INV_ALIVE	Intel Anti-Theft HDD protect	PWROK	0 = Disable (Internal pull-down 20kohm)										



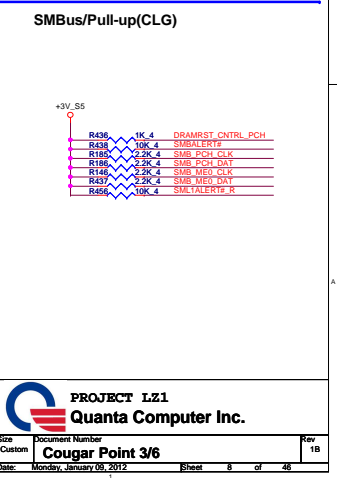
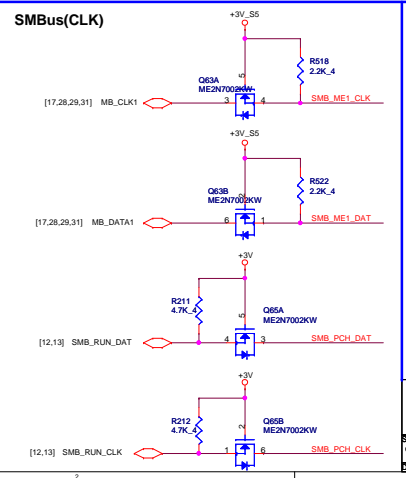
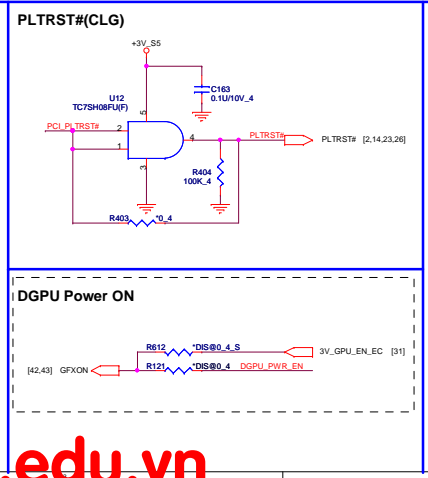
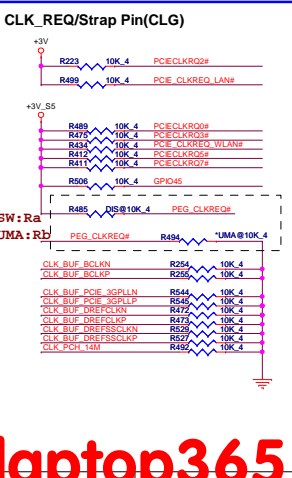
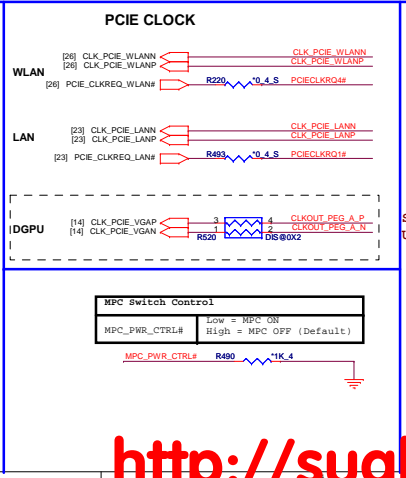
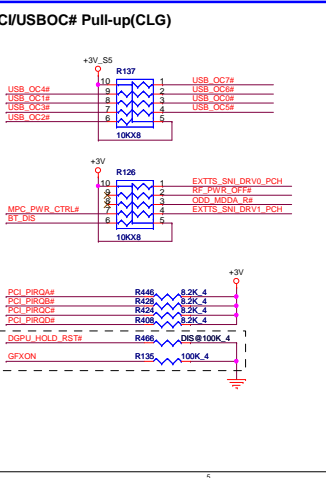
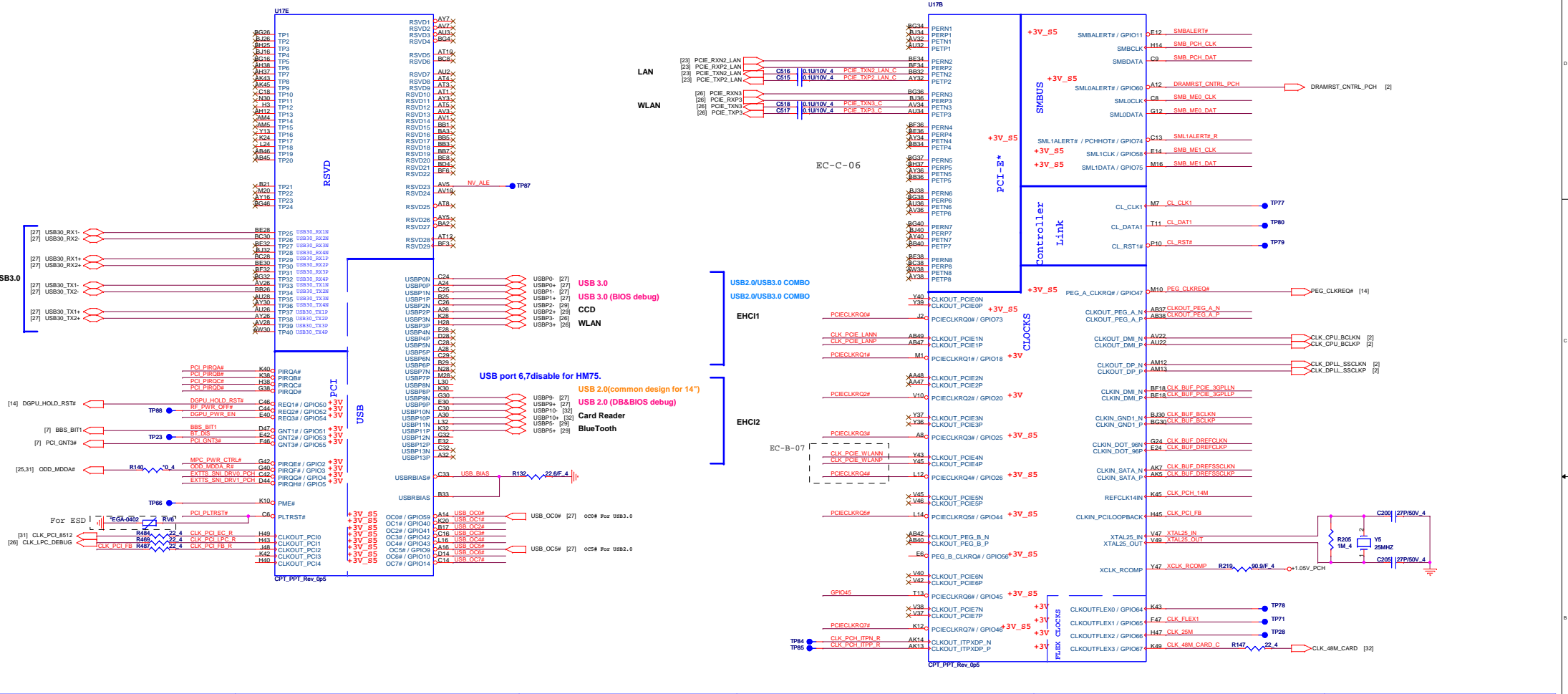
PCH Dual SPI (CLG)



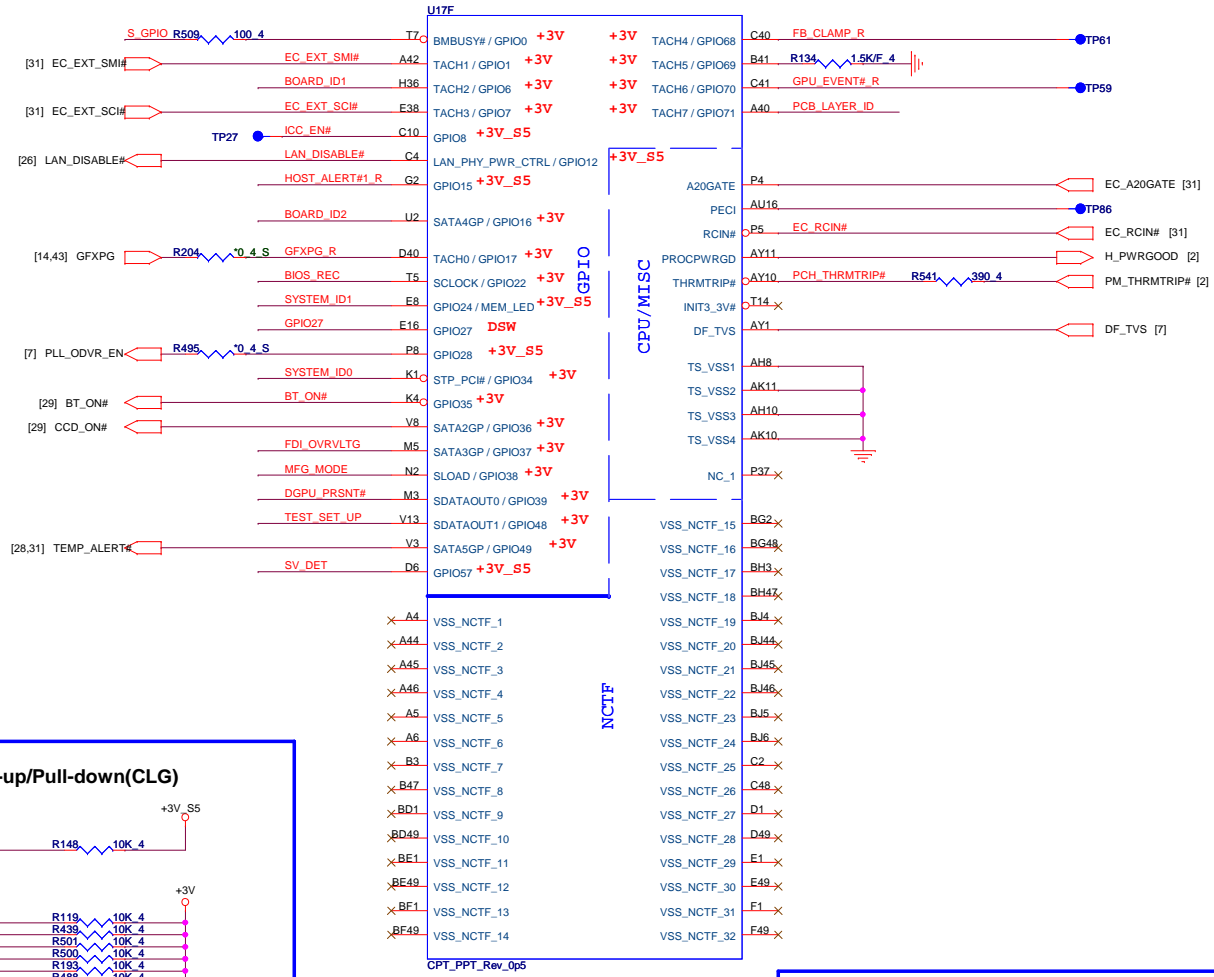
32Mbit (8M Byte), SPI

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

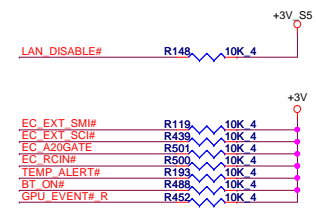
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down (CLG)



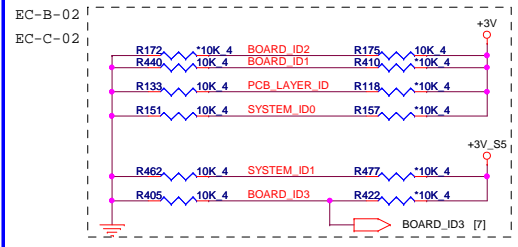
Board ID

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

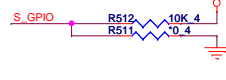
Board ID:
 BOARD_ID1
 BOARD_ID2
 BOARD_ID3

PCB LAYER ID:
 6 layer-->0
 8 layer-->1

System ID[0.1]:
 -->LZ1 [0.0]
 -->LZ2 [0.1]
 -->LZ3 [1.0]



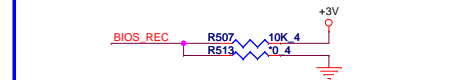
SGPIO



SV_SET_UP
 High = Strong (Default)



SATA2GP/GPIO36 Reserved Rising edge of PWROK
 NOTES:
 1. The internal pull-down is disabled after PLTRST# deasserts.
 2. This signal should not be pulled high when strap is sampled.



HOST_ALERT#1_R R143 1K 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
 Low = Disable (Default)
 High = Enable

	Optimus	UMA
Stuff	R498	R497
No Stuff	R497	R498

DMI TERMINATION VOLTAGE OVERRIDE
 Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE
 Low = Tx, Rx terminated to same voltage

BIOS RECOVERY
 High = Disable (Default)
 Low = Enable

MFG-TEST

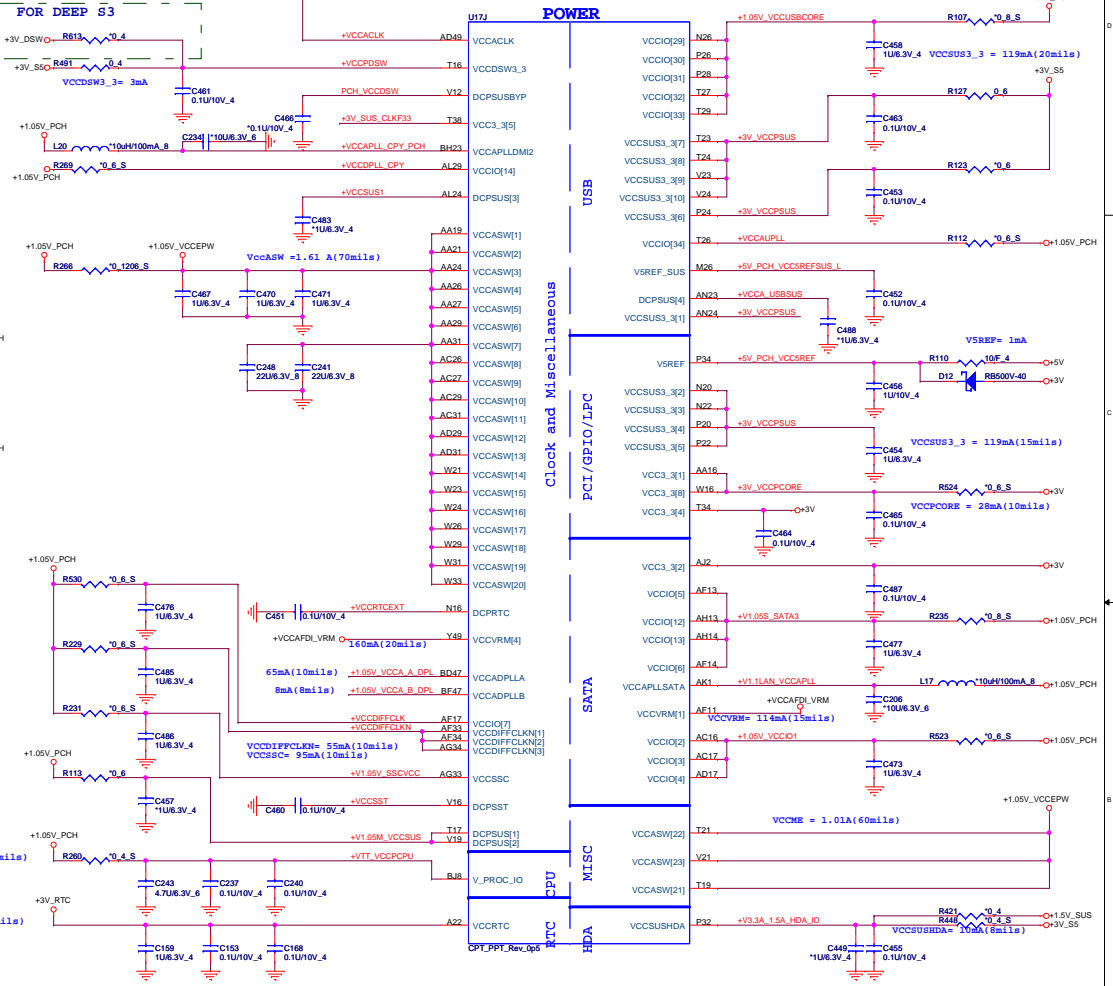
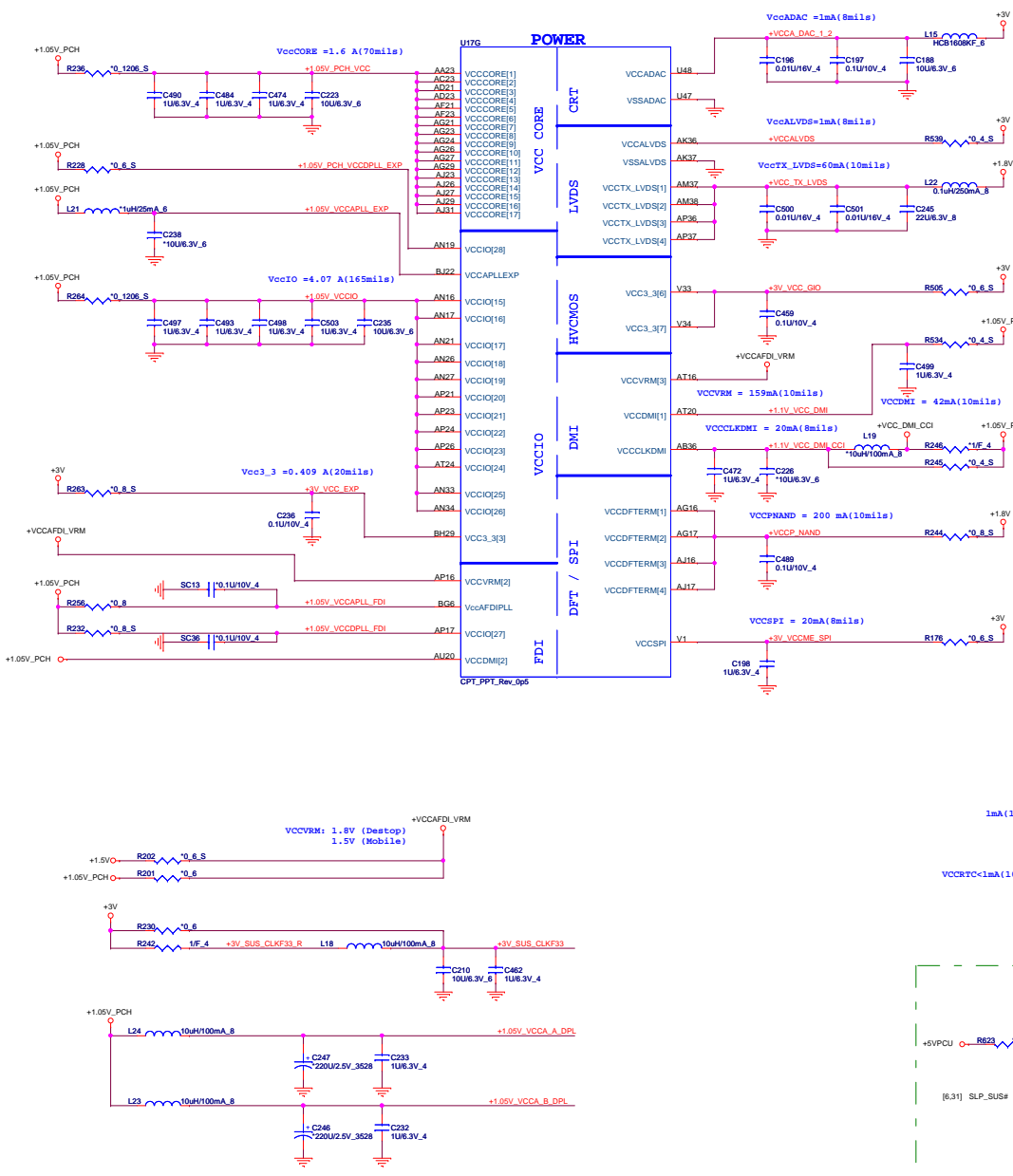


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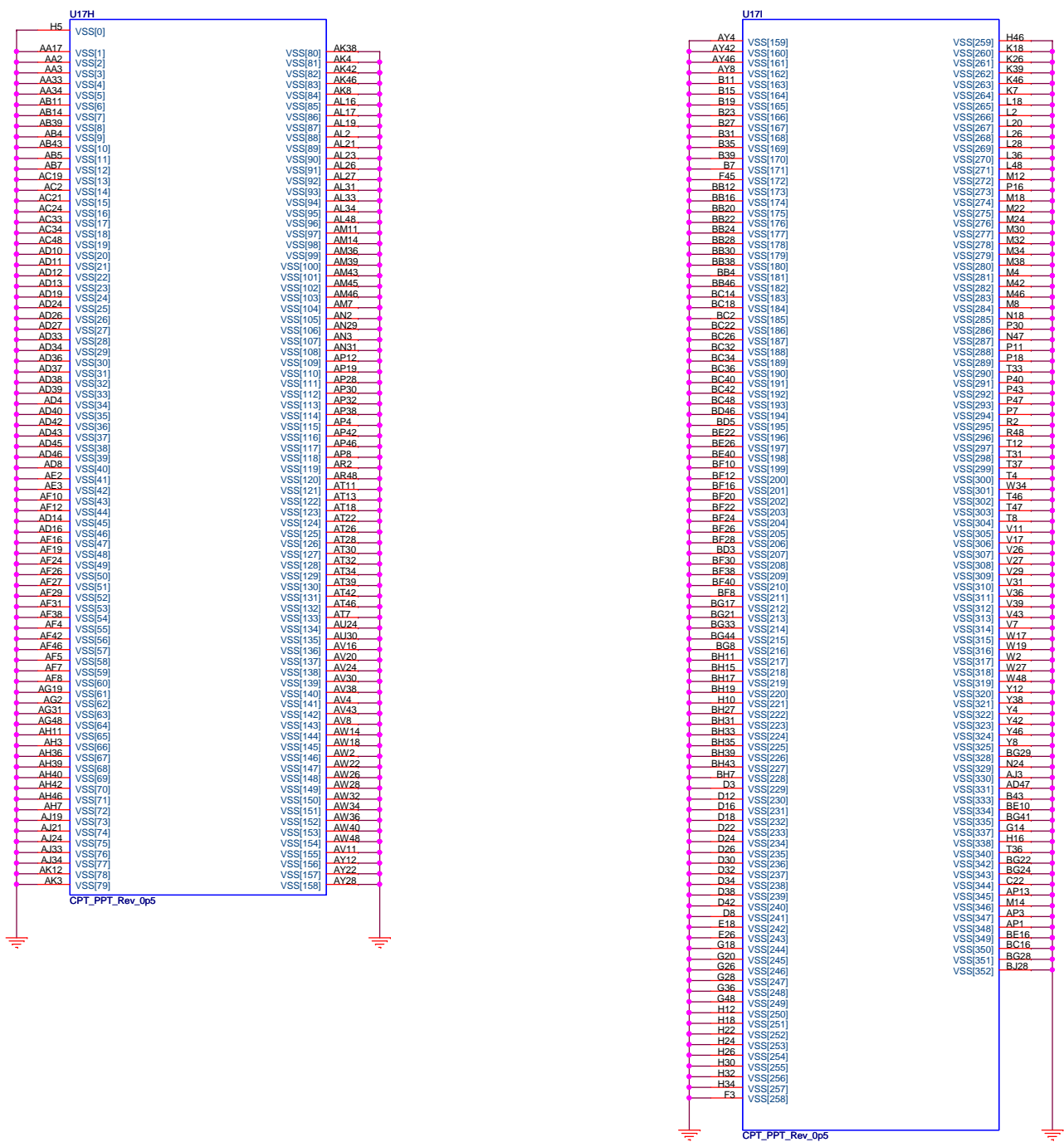
Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)

[6,7,8,9,12,13,14,20,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43]	+1.05V_PCH
[2,4,6,7,33,34,36,43]	+3V
[6,7,31]	+3V_RTC
[2,6,7,8,9,30,34]	+3V_S5
[22,25,27,33,34]	+3V_S5
[7,20,21,24,25,26,29,30,34]	+3V_S5
[4,7,34,40]	+1.5V
[4,26]	+1.5V
[2,4,12,13,33,34,37,40]	+1.5V_SUS



Cougar Point/Panther Point (GND)

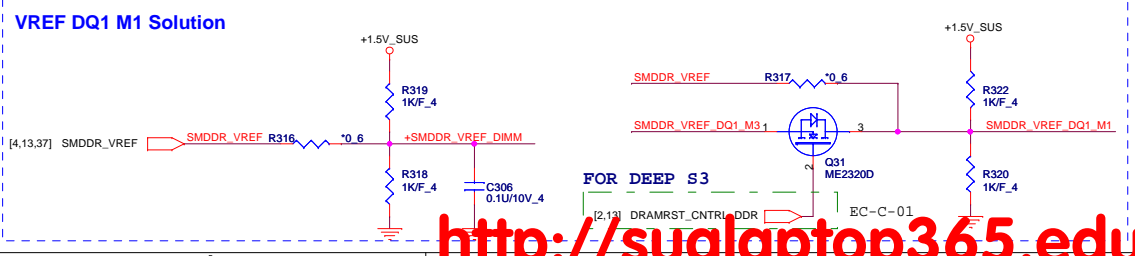
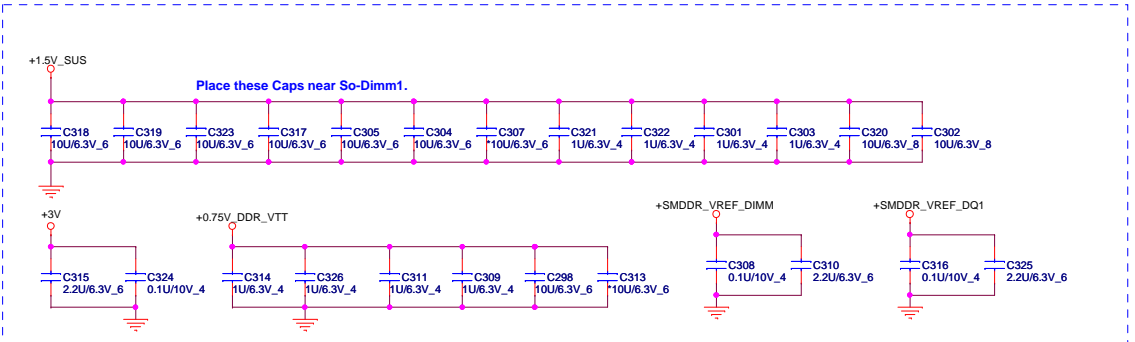
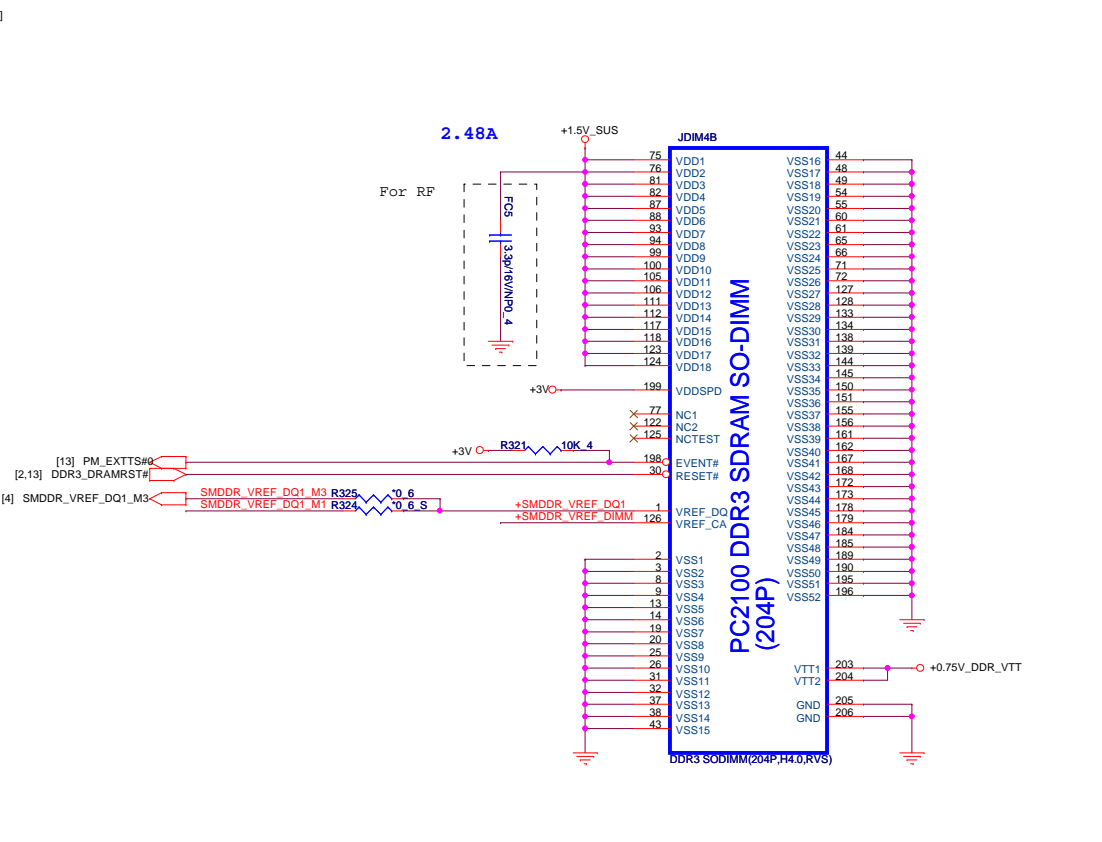
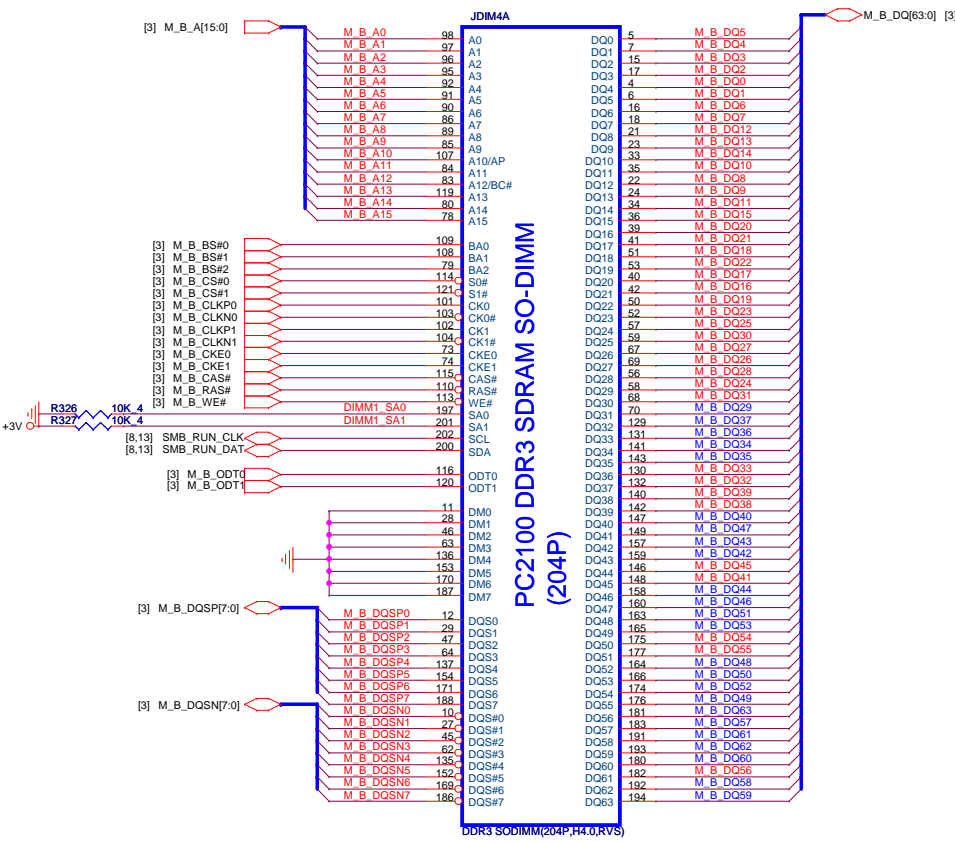


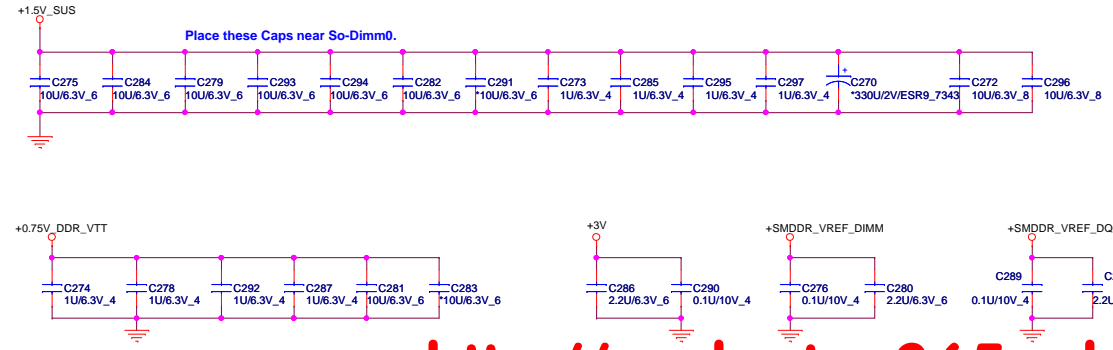
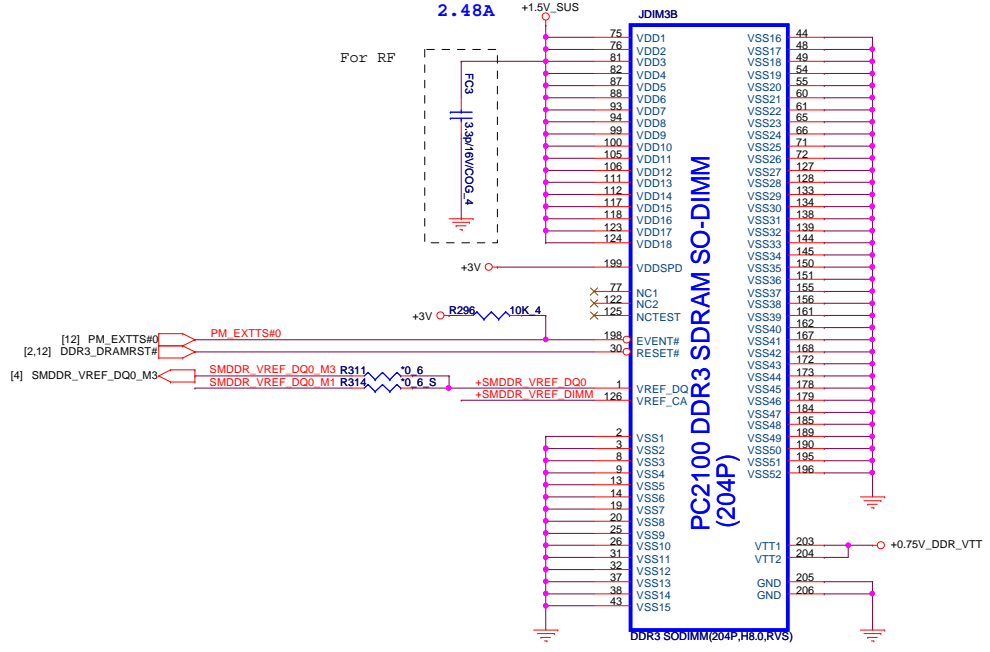
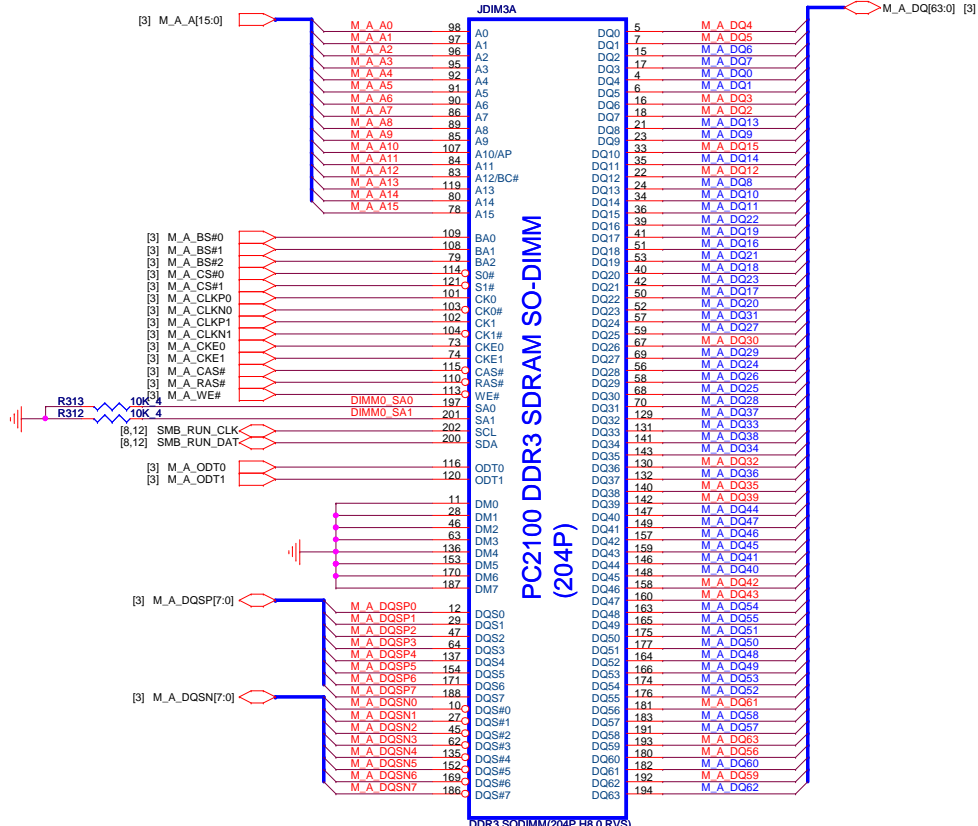
<http://sualaptop365.edu.vn>

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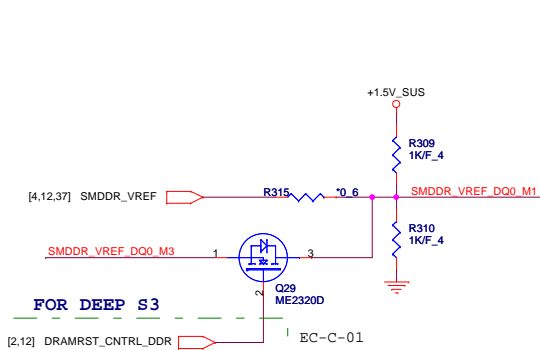
Size Custom Document Number **Cougar Point 6/6** Rev 1B

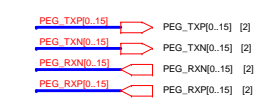
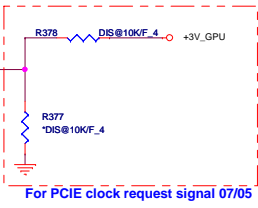
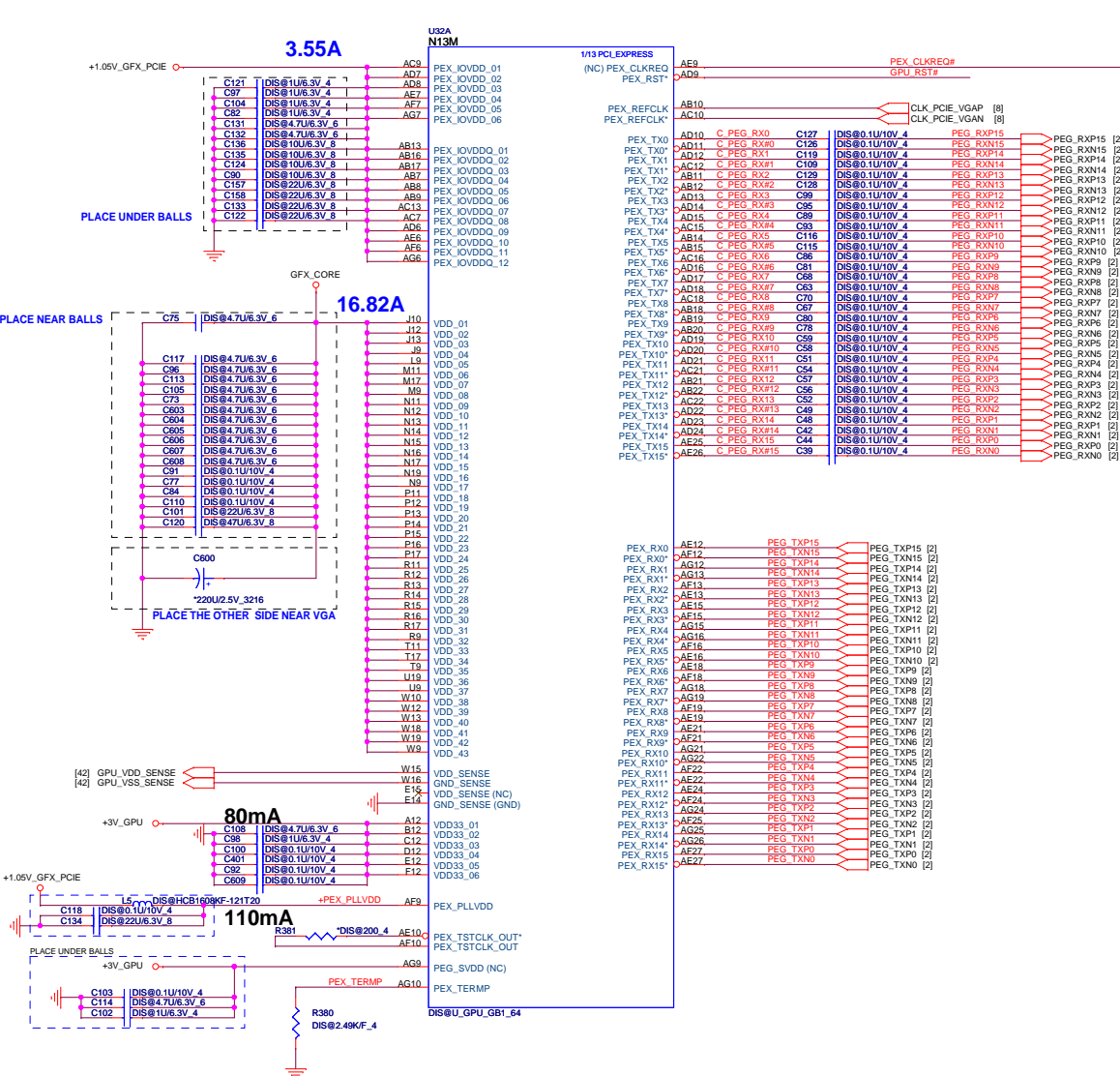
Date: Monday, January 09, 2012 Sheet 11 of 46





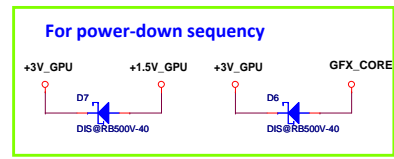
VREF DQ0 M1 Solution





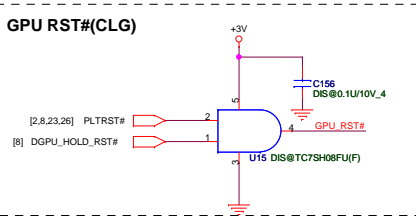
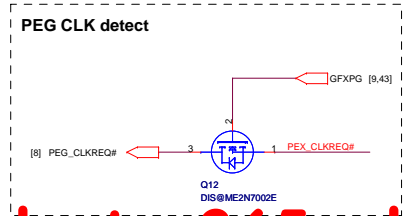
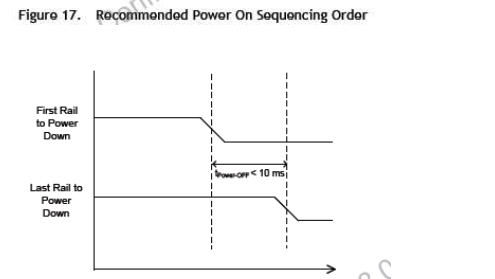
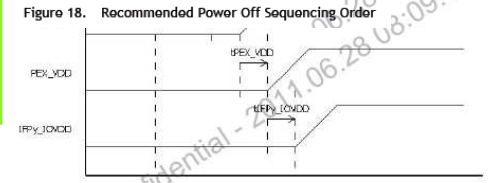
power up sequence

- All GPU power rails must ramp up after VDD33. The following conditions must be met:
- ▶ tNVVDD > 0
 - ▶ tFBVDDQ > 0
 - ▶ tPEX_VDD > 0
 - ▶ tFFPx_IOVDD ≥ 0
 - ▶ tFFPy_IOVDD ≥ 0
 - ▶ The ramp time for any rail must be more than 40 us.

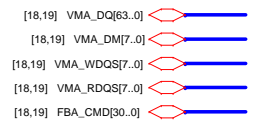
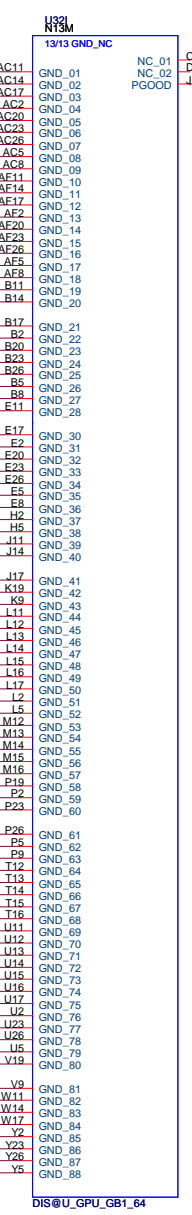
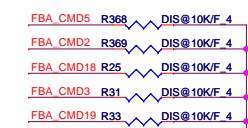
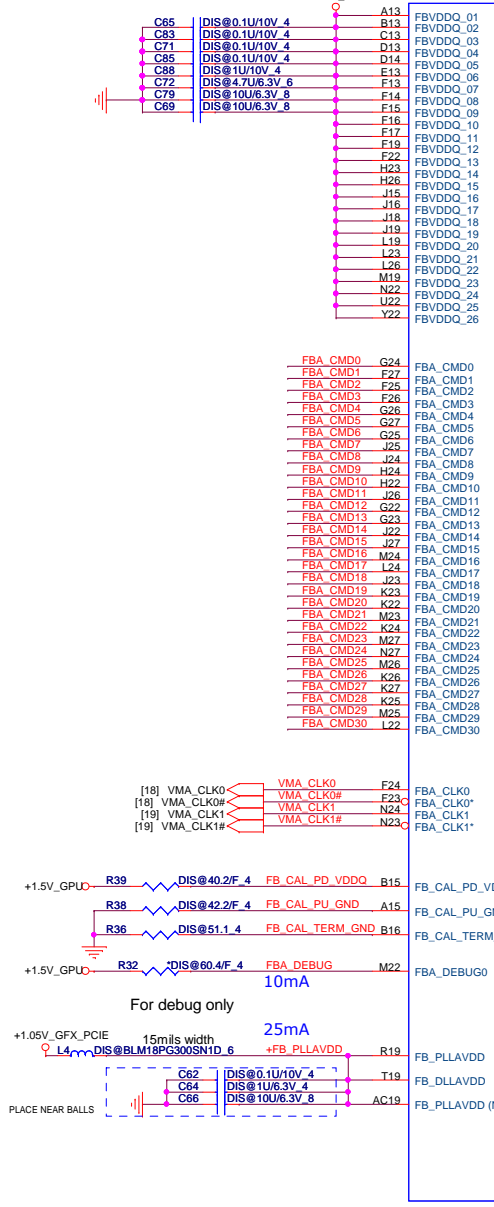


The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

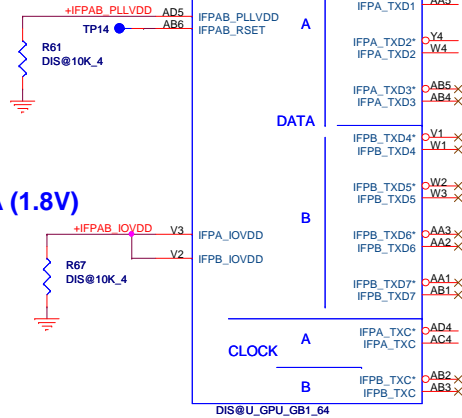
- ▶ NVVDD ≤ VDD33+0.5 V
- ▶ FBVDDQ ≤ VDD33-0.5 V



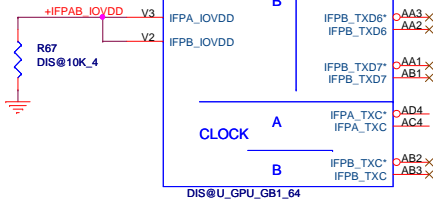
2.63A
+1.5V_GPU



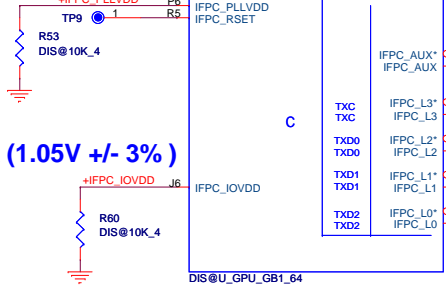
220 mA (1.05V +/- 3%)



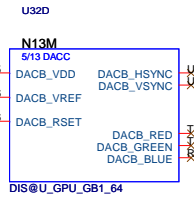
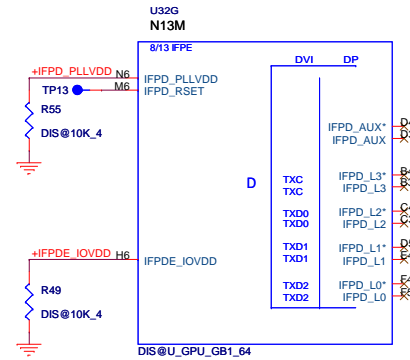
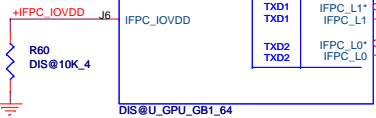
220 mA (1.8V)



220 mA



285 mA (1.05V +/- 3%)



The following guidelines only apply to a fully unused IFP macro:

- ▶ Pull down IFPxy_IOVDD with 10 kΩ resistor
- ▶ Pull down IFPxy_PLLVDD with 10 kΩ resistor
- ▶ The other IO pins can be NC
- ▶ It is also recommended that footprints for both a 10 kΩ resistor to ground and a 10 kΩ resistor to power be implemented as stuffing options to allow for flexibility in design options

The circuit shown in Figure 6.12 shows the connection for an unused IFP macro.

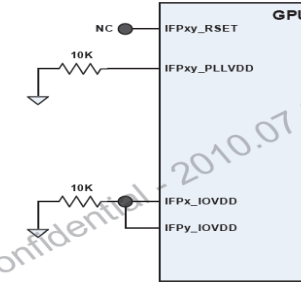
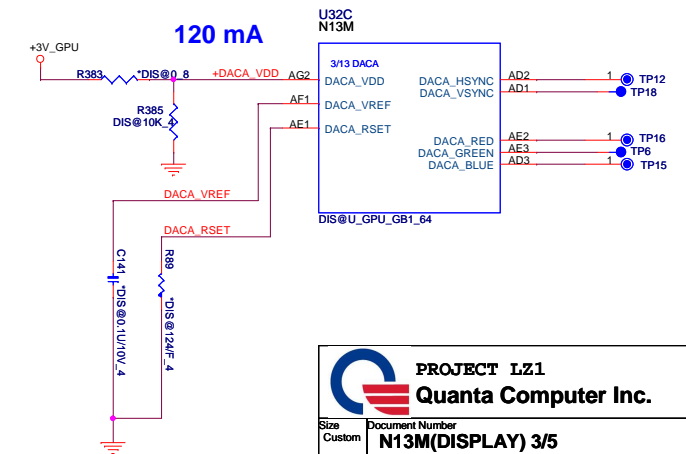
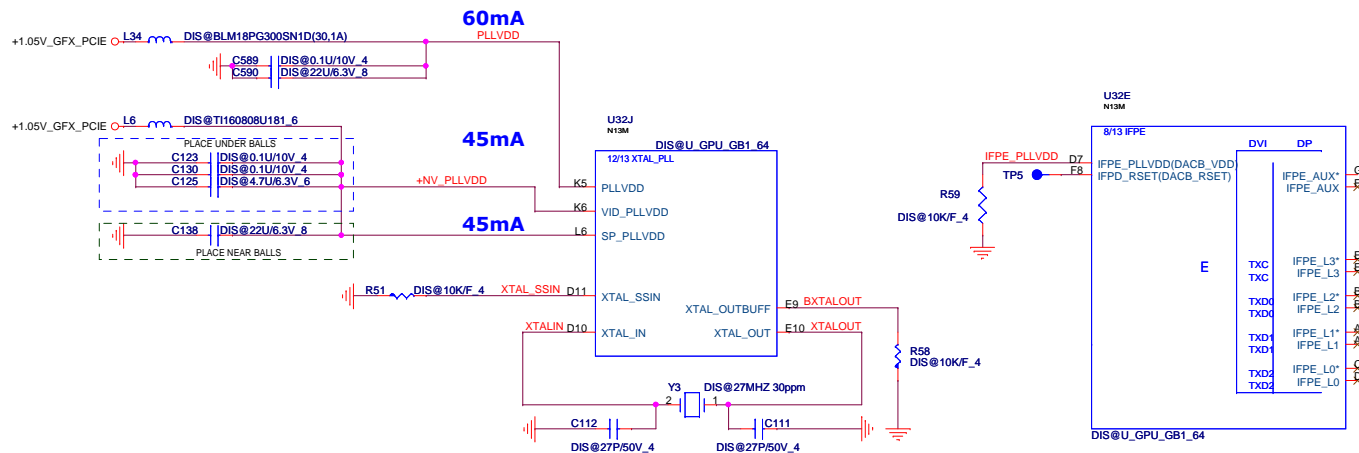


Figure 6.12 Unused IFP Interface

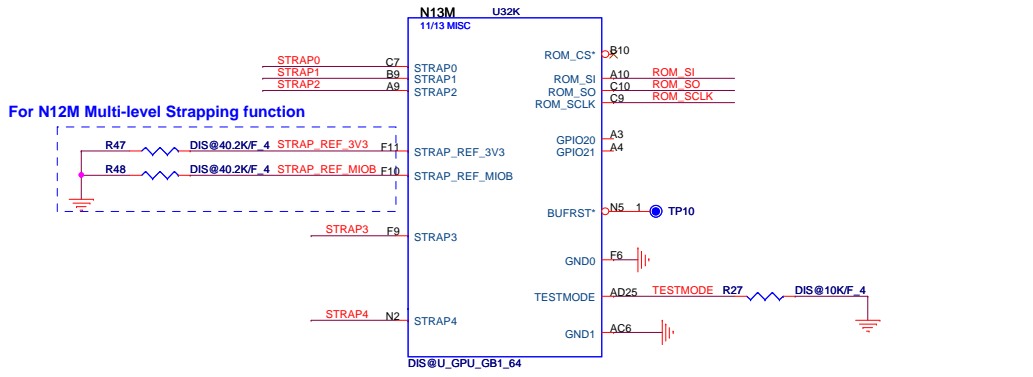
7.4 Unused DAC Interface

To disable a DAC interface:

- ▶ Pull down the DACx_VDD with a 10 kΩ resistor
- ▶ The other DAC IO pins (including DACx_VREF, DACx_RSET) can be NC

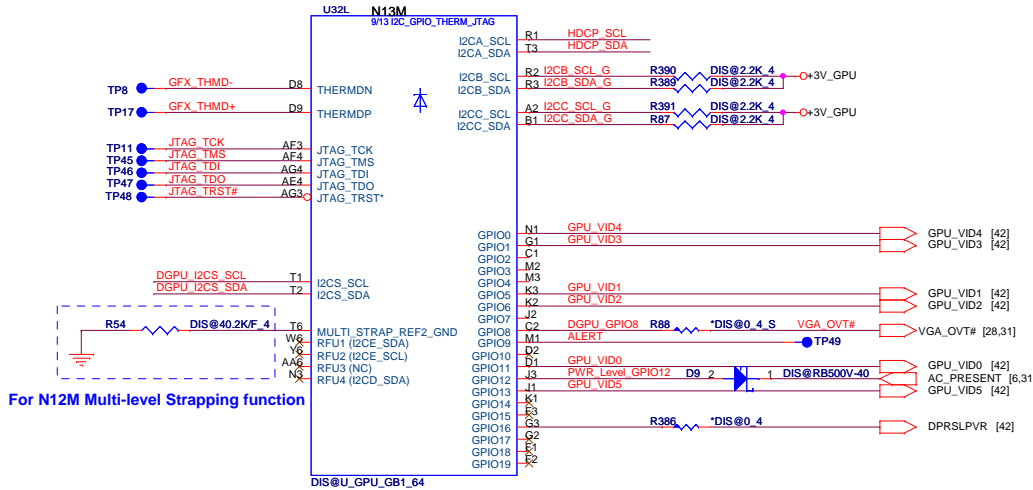


STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS Install it when not connected to Spread spectrum device

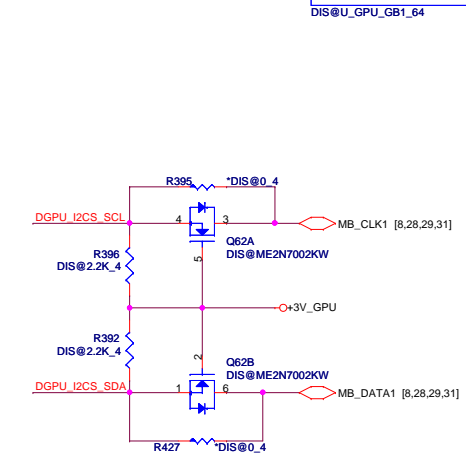


9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 k Ω resistors routing.



For N12M Multi-level Strapping function



nV FAB suggest that the device ID for N13M-GE1 is 0x1058

N13M-GE1

Logical Strap Bit Mapping

Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

(Ra)

- 4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
- 10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
- 15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
- 30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +1%(0402)]
- 34.8K/F_4: CS33482FB22 [RES CHIP 34.8K 1/16W +1%(0402)]
- 45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

Default: Hynix VRAM

- 24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +1%(0402)]
- 20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]

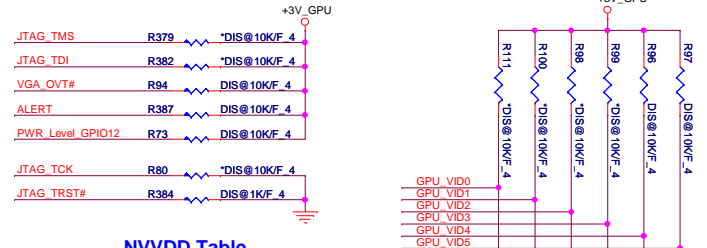
Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N13M-GE1 FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK PCI_DEVICE[4]	SUB_VENDOR	PCI_DEVICE[5]	PEX_PLL_EN_TERM	1010
ROM_SI RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP0 USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1 3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2 PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]	1000
STRAP3 SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4 RESERVED	RESERVED	PCI_MAX_SPEED	DP_PLL_VDD33V	0001

(Ra)

AKD5MGWU00
AKD5MGWT500

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	Reserved	Reserved		
0001	Reserved	Reserved		
0010	Reserved	Reserved		
0011	Reserved	Reserved		
0101	Reserved	Reserved		
0110	Reserved	Reserved		
0111	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	PD 34.8K/F PD 45.3K/F
0111	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	



NVDD Table

N13M-GE1 (GF119)	NVDD (0.9V)
GPU_VID0	0 (R116)
GPU_VID1	0 (R85)
GPU_VID2	0 (R83)
GPU_VID3	0 (R84)
GPU_VID4	1 (R96)
GPU_VID5	1 (R97)

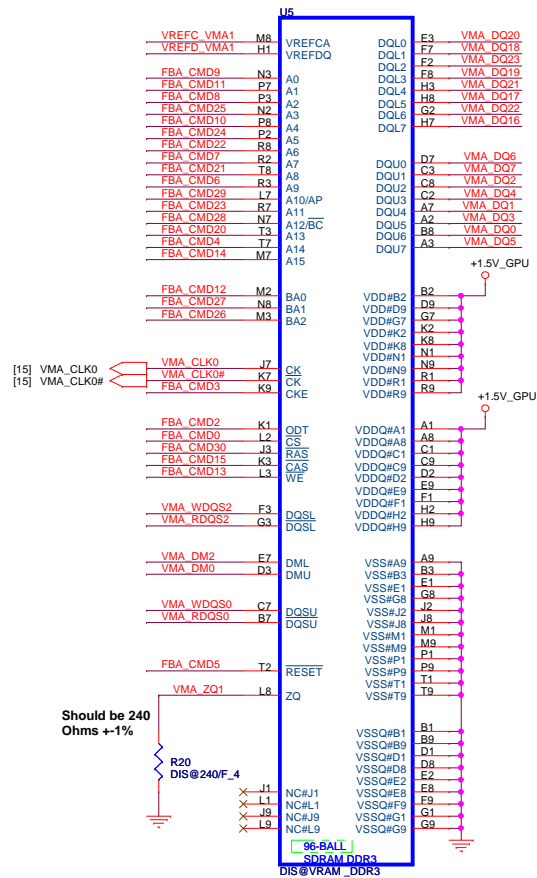
GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	0	GPU Core VDD VID4
GPIO1	GPU_VID3	0	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	0	Panel Power Enable
GPIO4	LCD_BLEN	0	Panel Backlight Enable
GPIO5	GPU_VID0	0	GPU Core VDD VID0
GPIO6	GPU_VID2	0	GPU Core VDD VID2
GPIO7	3D_Vision	0	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	0	Memory VREF Control
GPIO11	GPU_VID0	0	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	0	GPU Core VDD VID5
GPIO14	HPU_AB	I	Hot Plug Detect for HPA8
GPIO15	HPU_C	I	Hot Plug Detect for HPC
GPIO16	MEM_VDD_CTL	0	Memory VDD VIO
GPIO17	HPU_D	I	Hot Plug Detect for HFD
GPIO18	HPU_E	I	Hot Plug Detect for HFE
GPIO19	HPU_F	I	Hot Plug Detect for HFF
GPIO20	Reserved		
GPIO21	Reserved		

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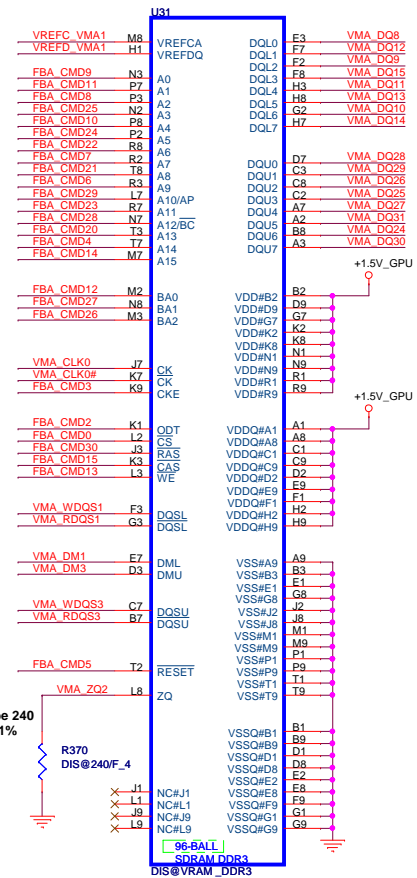
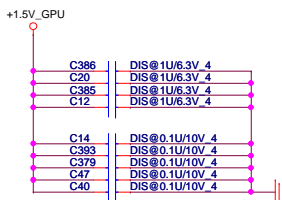
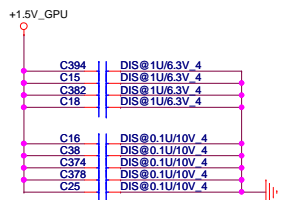
Size: Custom Document Number: **N13M(GPIO & STRAPS) 4/5** Rev 1B

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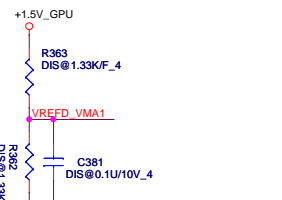
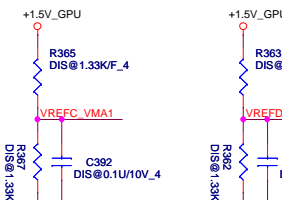
CHANNEL A: 1024MB DDR3



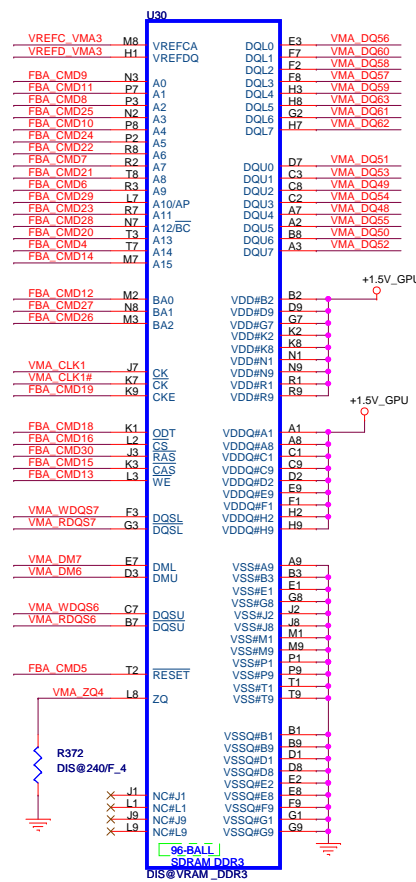
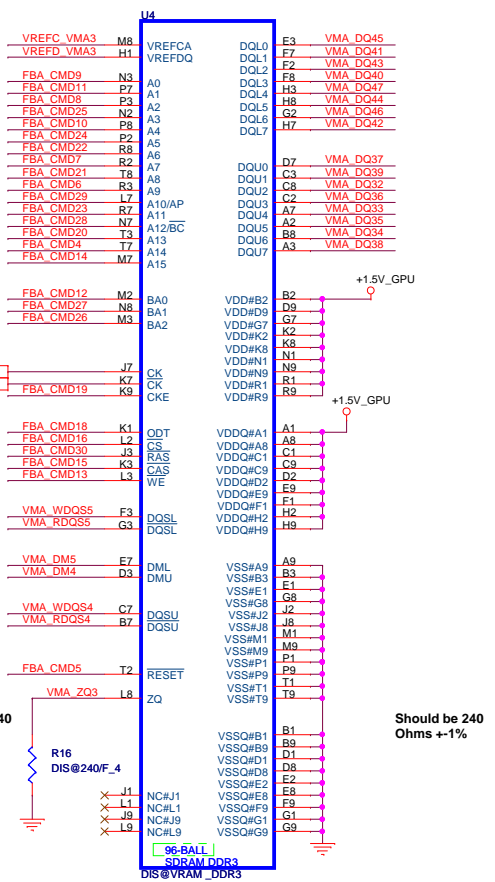
Should be 240 Ohms +-1%



Should be 240 Ohms +-1%



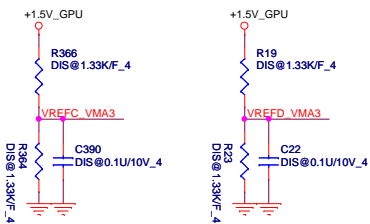
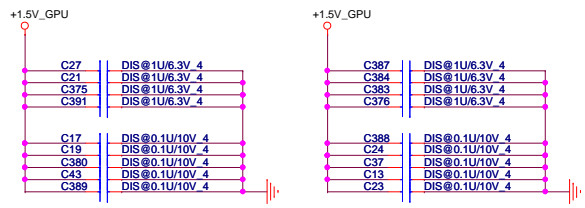
CHANNEL A: 1024MB DDR3



[15] VMA_CLK1#
 [15] VMA_CLK1#

Should be 240 Ohms +/-1%

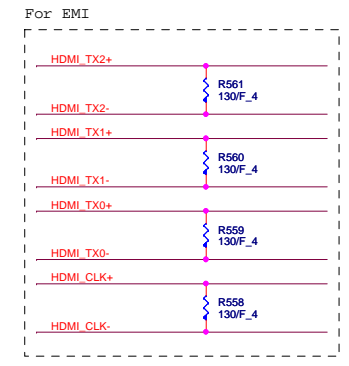
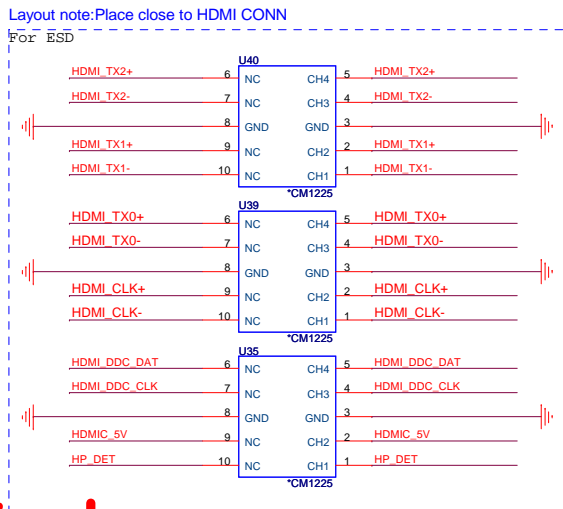
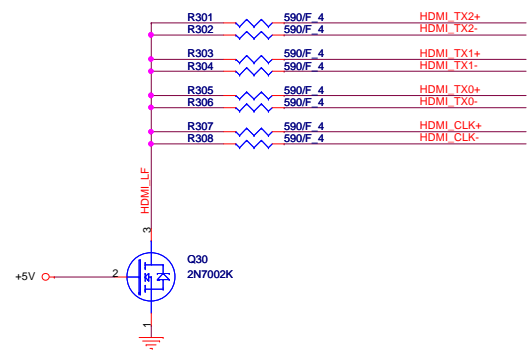
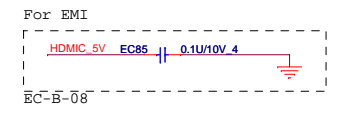
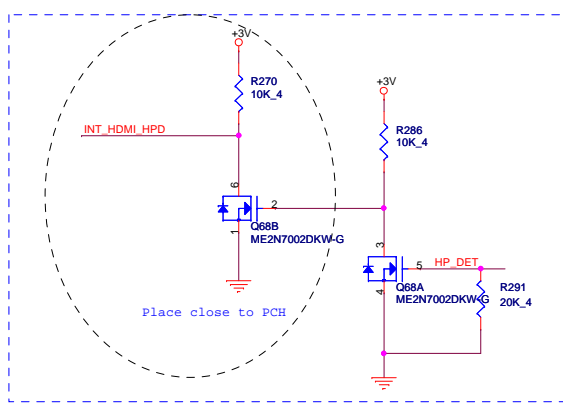
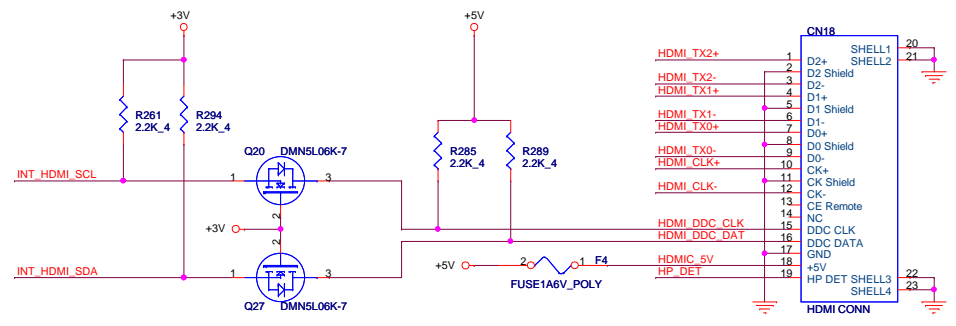
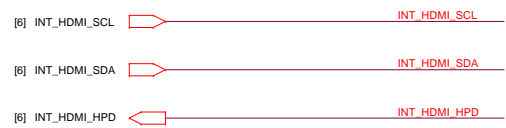
Should be 240 Ohms +/-1%

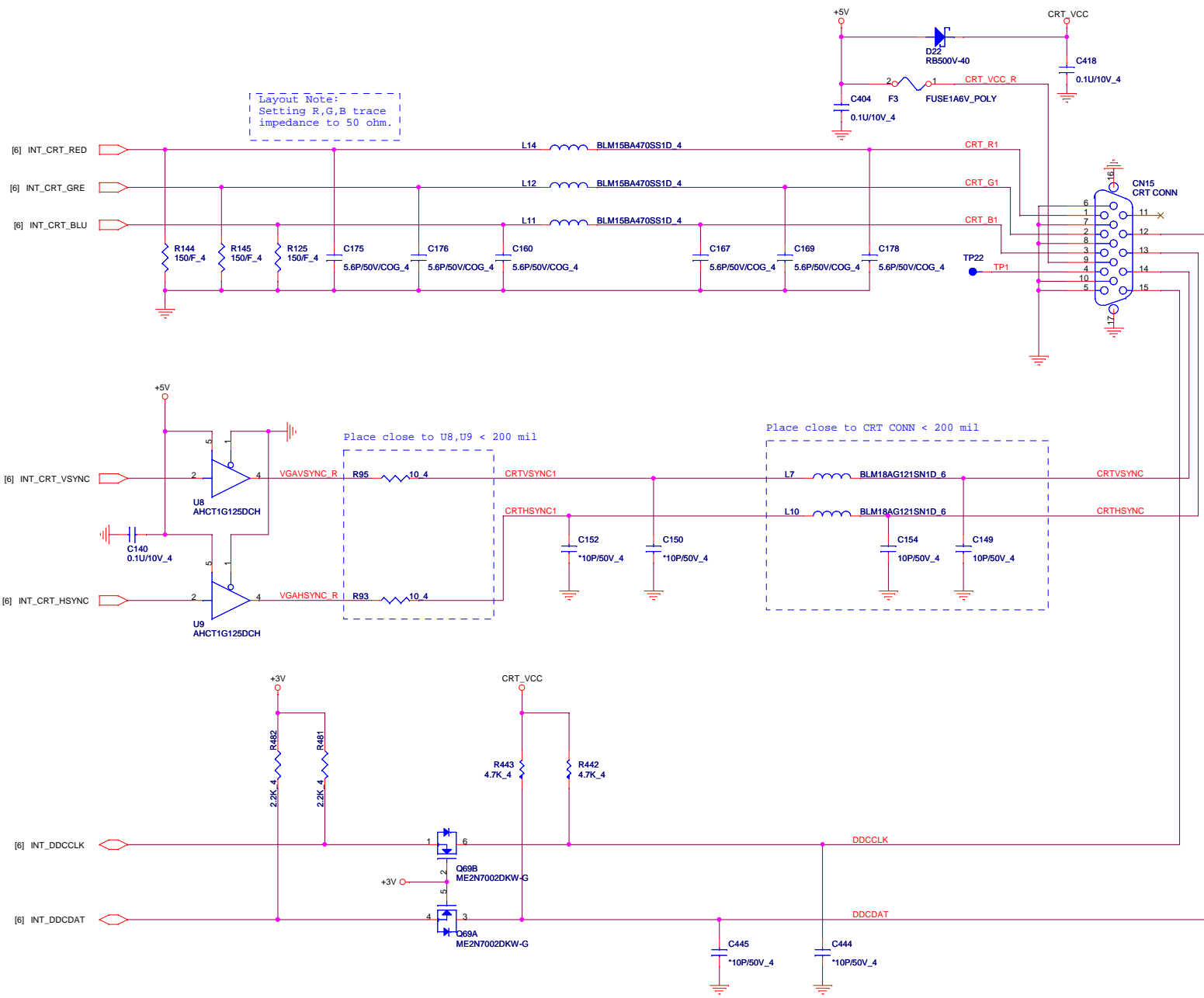


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Size	Document Number	Rev
Custom	N13M (DDR3) 6/6	1B
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[6] INT_HDMI_TXDN2	C534	0.1u/10V_4	HDMI TX2-
[6] INT_HDMI_TXDP1	C533	0.1u/10V_4	HDMI TX1+
[6] INT_HDMI_TXDN1	C532	0.1u/10V_4	HDMI TX1-
[6] INT_HDMI_TXDP0	C531	0.1u/10V_4	HDMI TX0+
[6] INT_HDMI_TXDN0	C530	0.1u/10V_4	HDMI TX0-
[6] INT_HDMI_TXCP	C529	0.1u/10V_4	HDMI CLK+
[6] INT_HDMI_TXCN	C528	0.1u/10V_4	HDMI CLK-

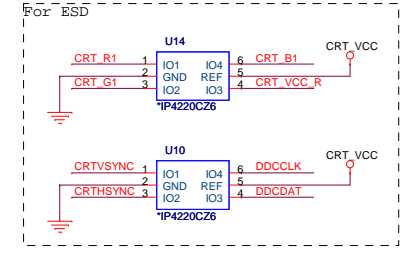


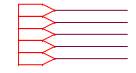


Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

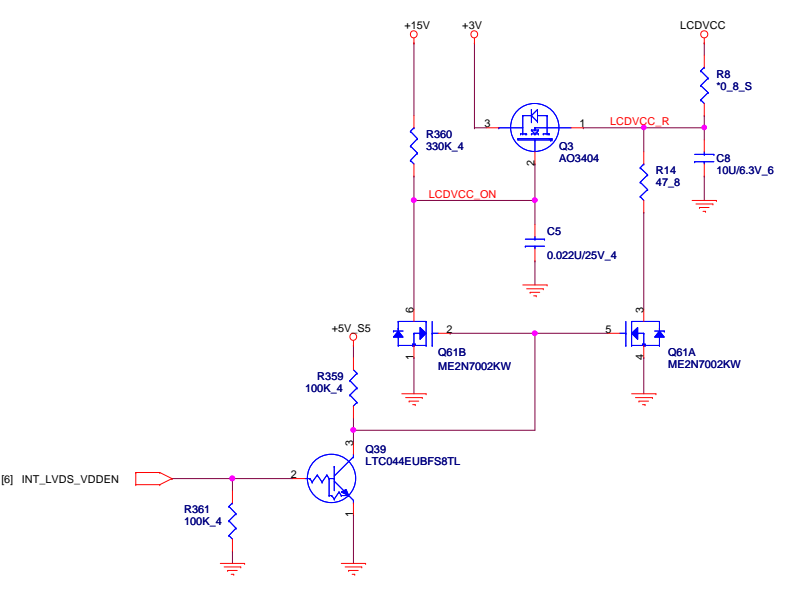
Place close to U8,U9 < 200 mil

Place close to CRT CONN < 200 mil

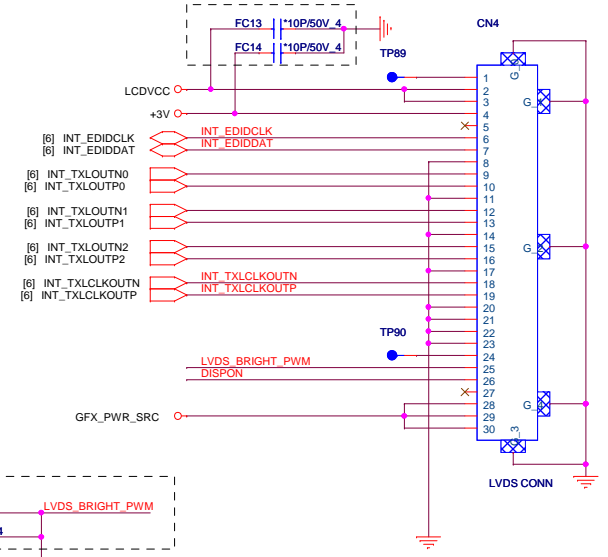




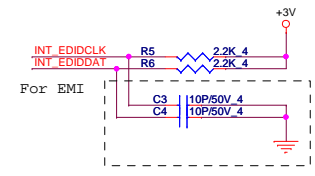
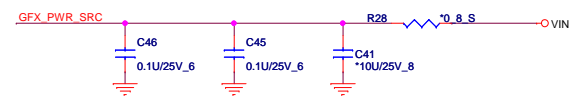
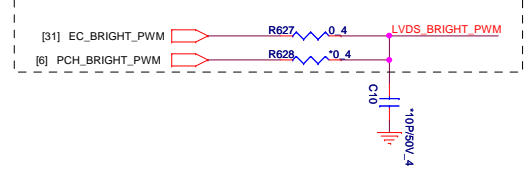
LCDVCC



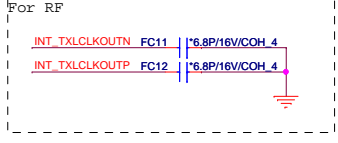
For RF EC-C-05



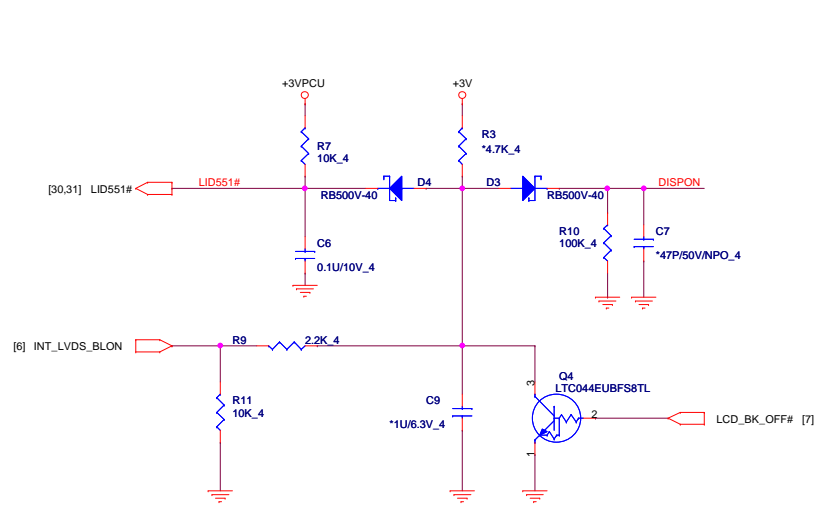
EC-C-08

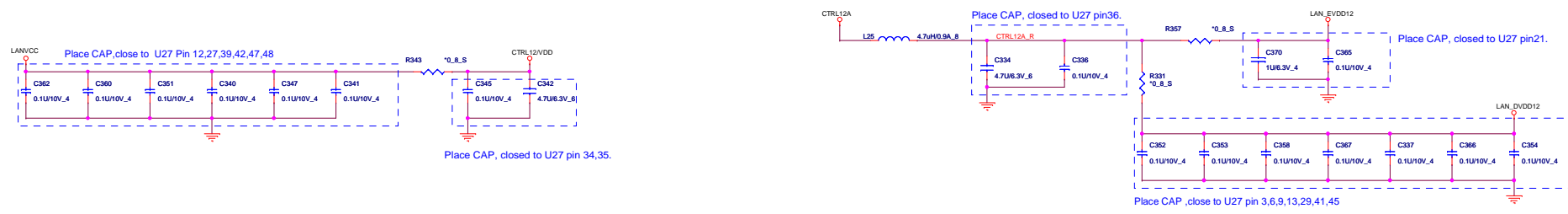
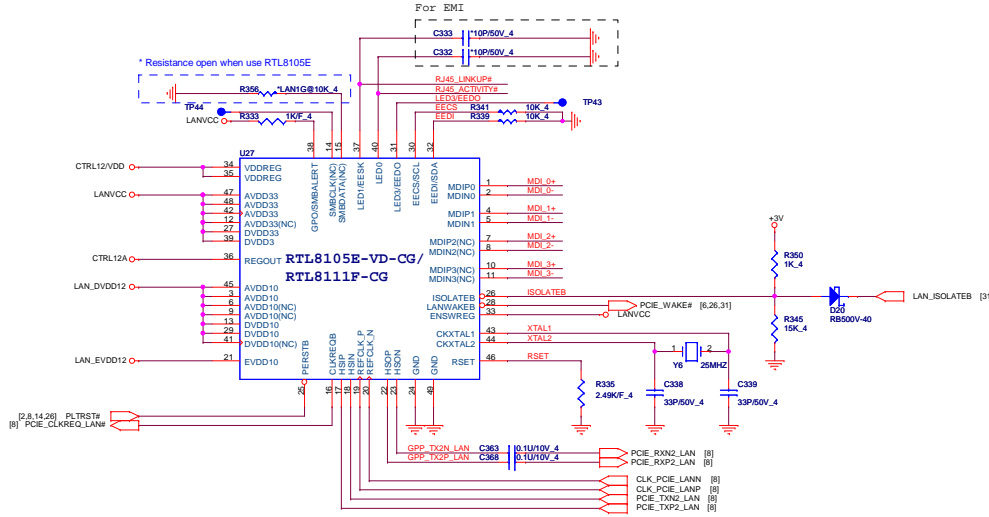
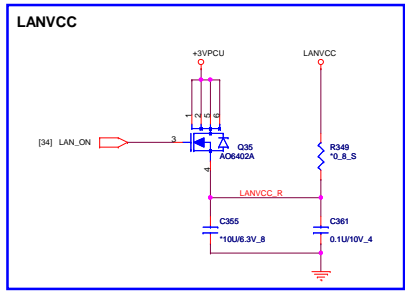


EC-B-03

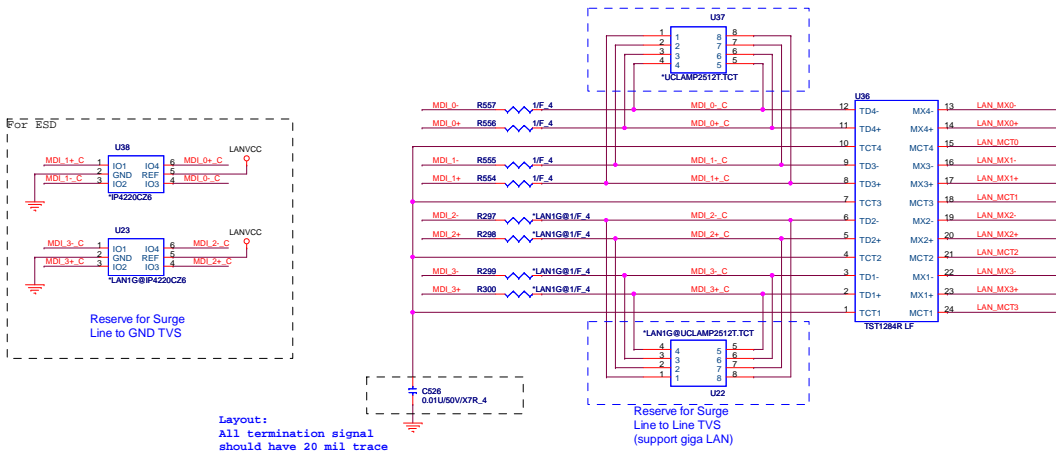


Back light

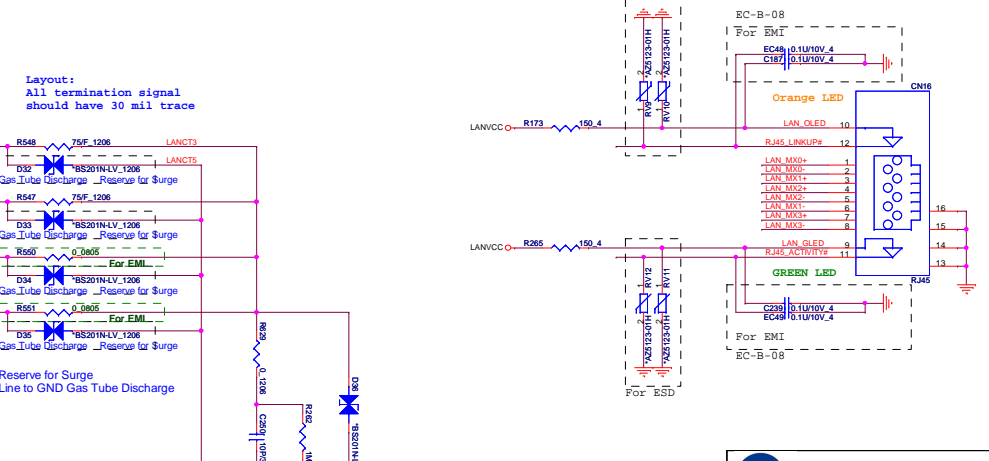




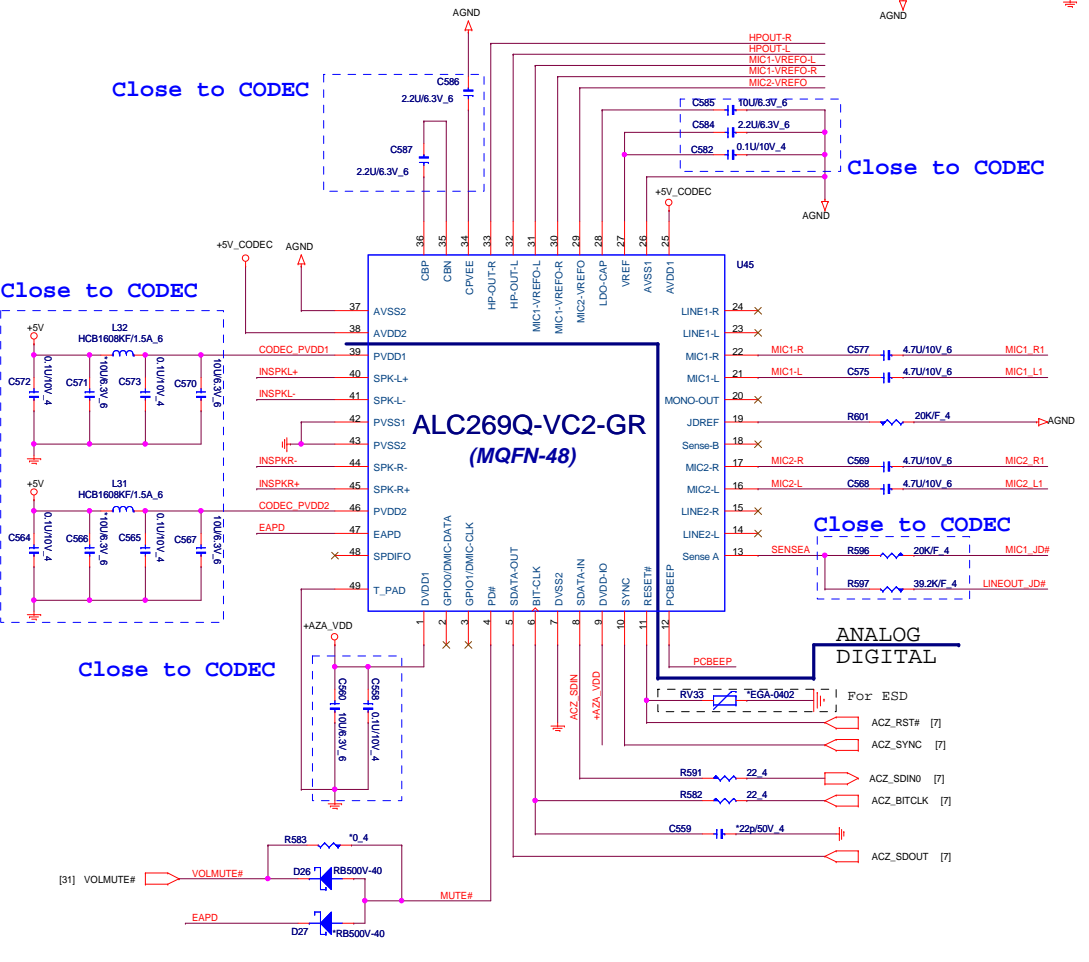
Transformer



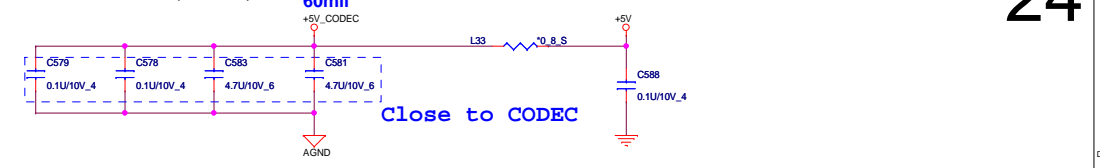
RJ45 Connector



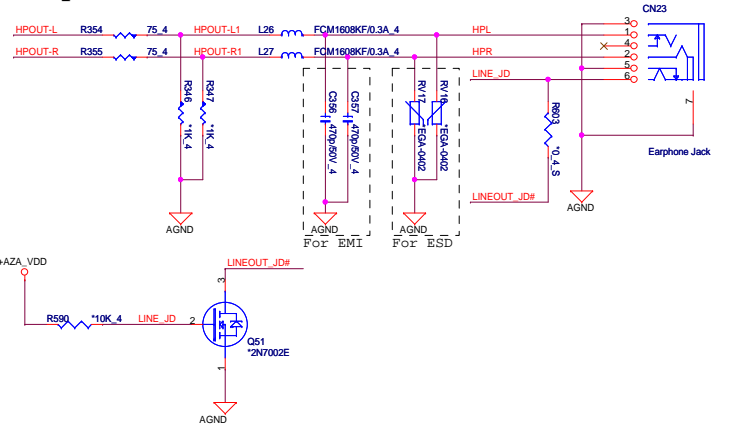
CODEC(ADO)



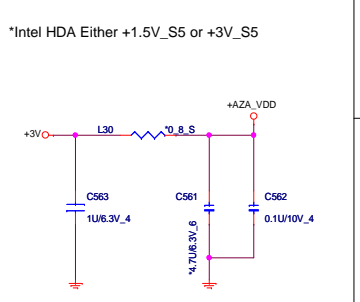
Codec Power(ADO)



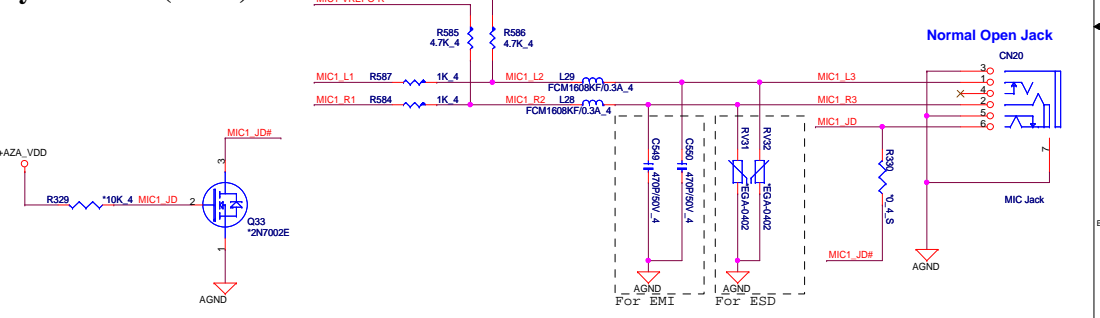
Earphone(AMP)



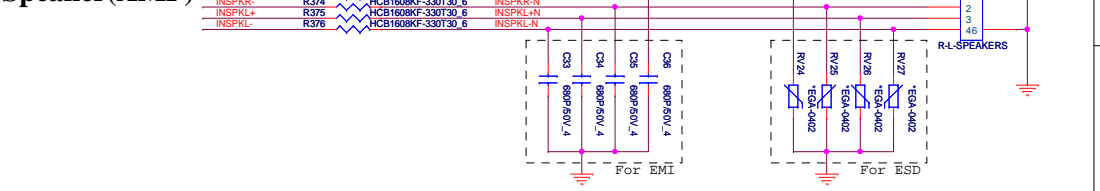
HDA Power(ADO)



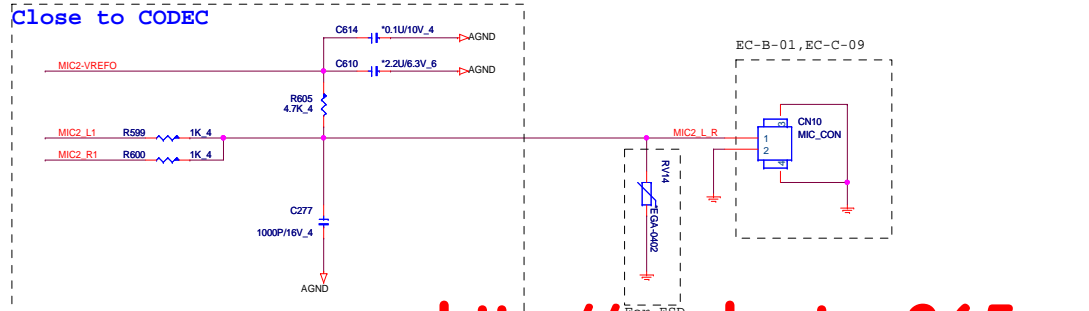
System MIC(AMP)



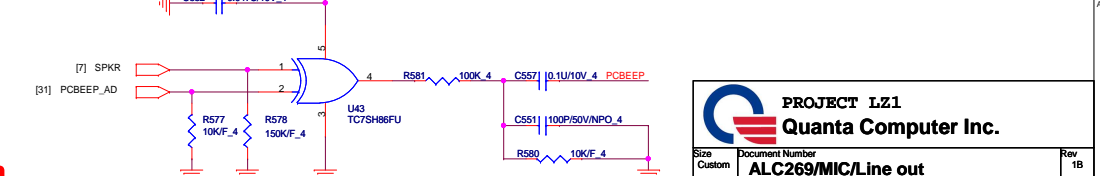
Speaker(AMP)



INTERNAL MIC



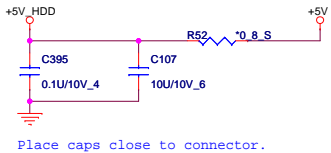
PC BEEP



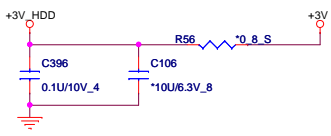
PROJECT LZ1
Quanta Computer Inc.
 Size: Custom Document Number: **ALC269/MIC/Line out** Rev: 1B
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SATA HDD

HDD-->1A
HDD-->1.5A(burning)

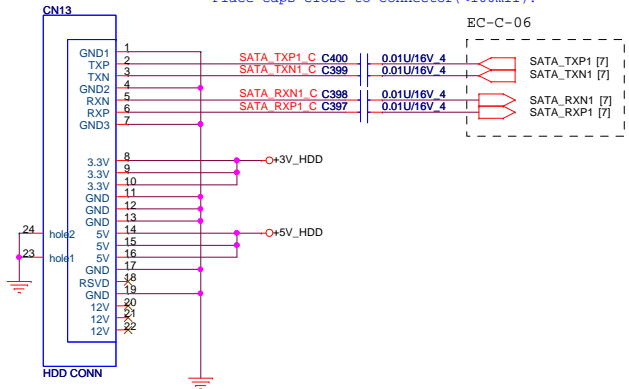


Place caps close to connector.



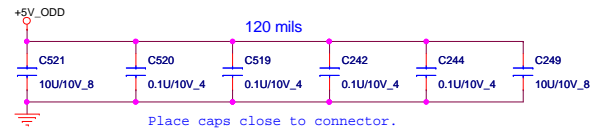
Place caps close to connector.

Place caps close to connector(<100mil).

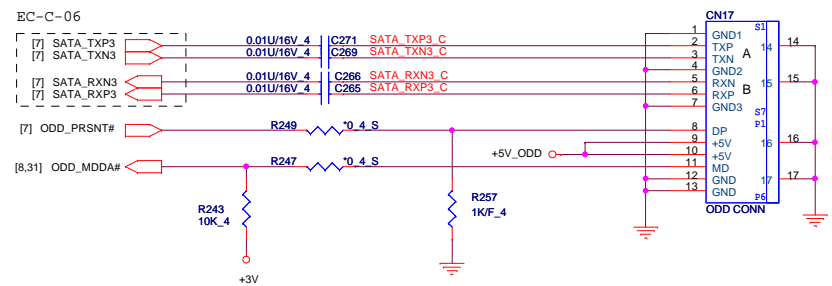
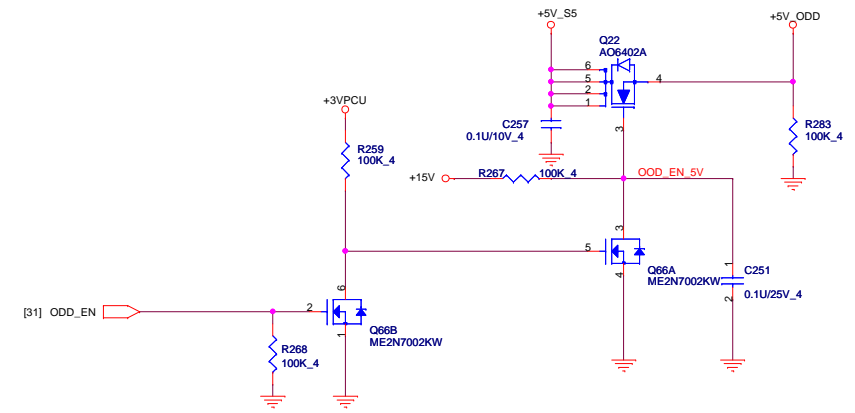


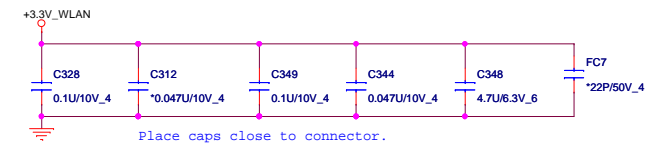
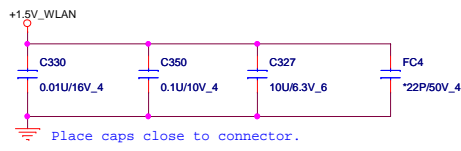
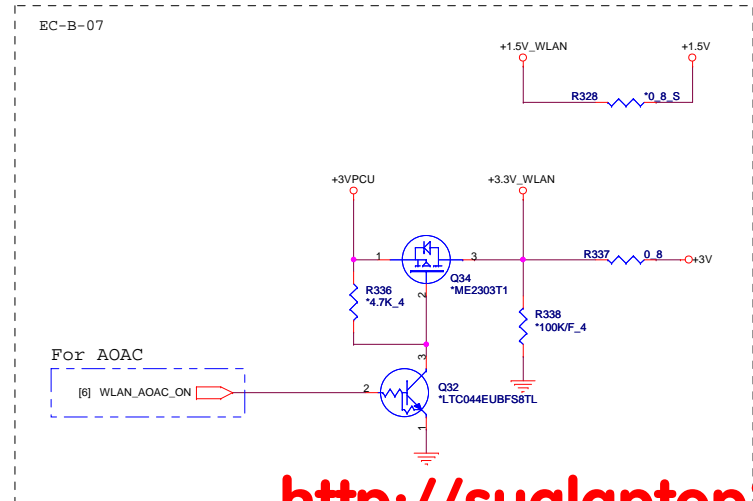
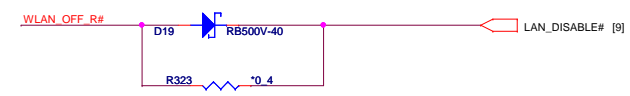
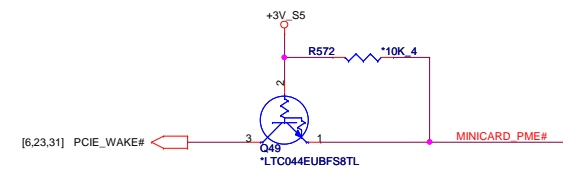
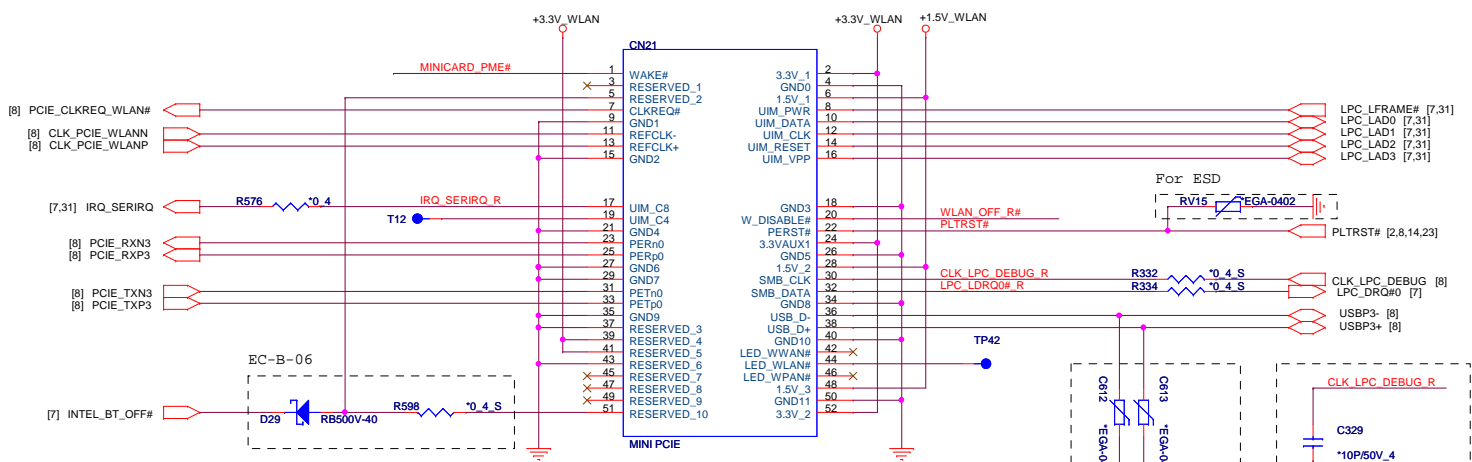
SATA ODD

[7,10,20,21,24,28,29,33,34] +5V
[6,7,8,9,10,12,13,14,20,21,22,23,24,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,22,27,33,34] +5V_SS
[6,7,22,23,26,30,31,34,35,36,40] +3VPCU
[22,29,34,36,43] +15V

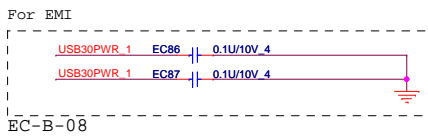
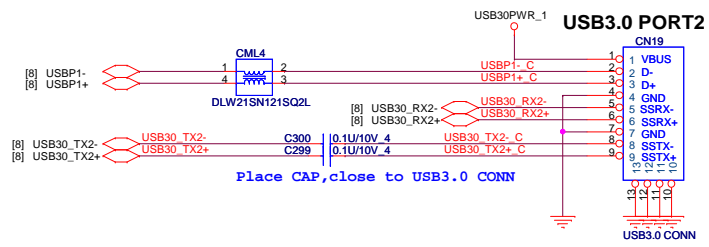
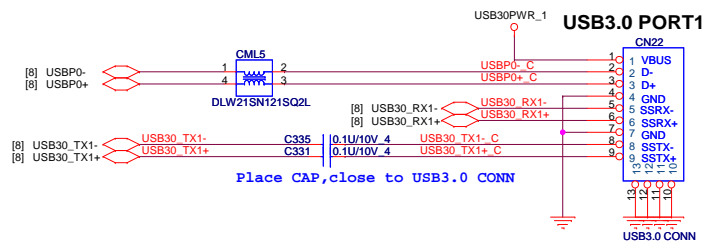
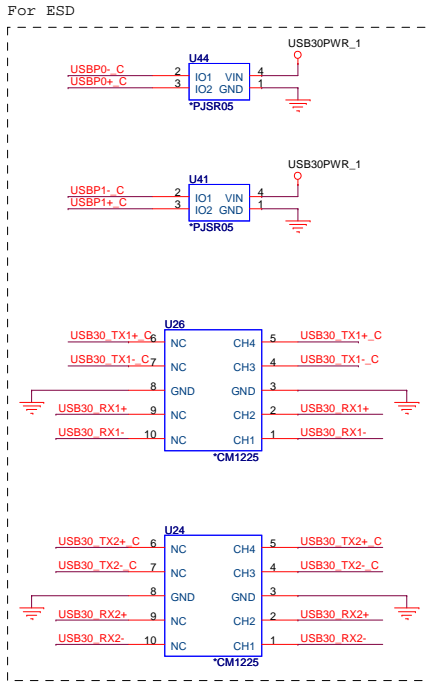
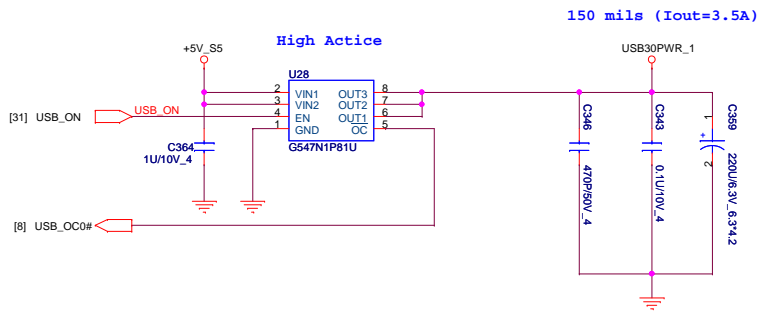


Place caps close to connector.

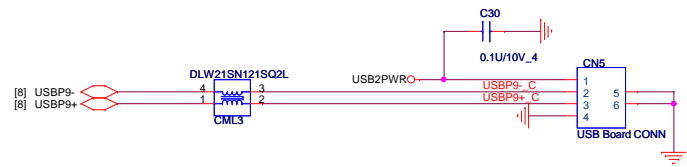
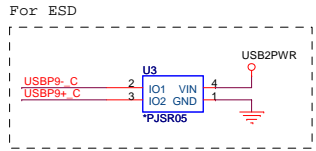
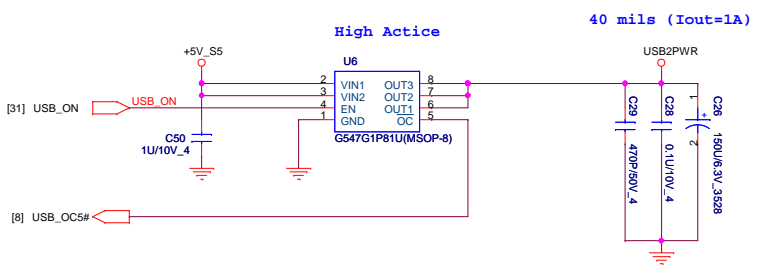


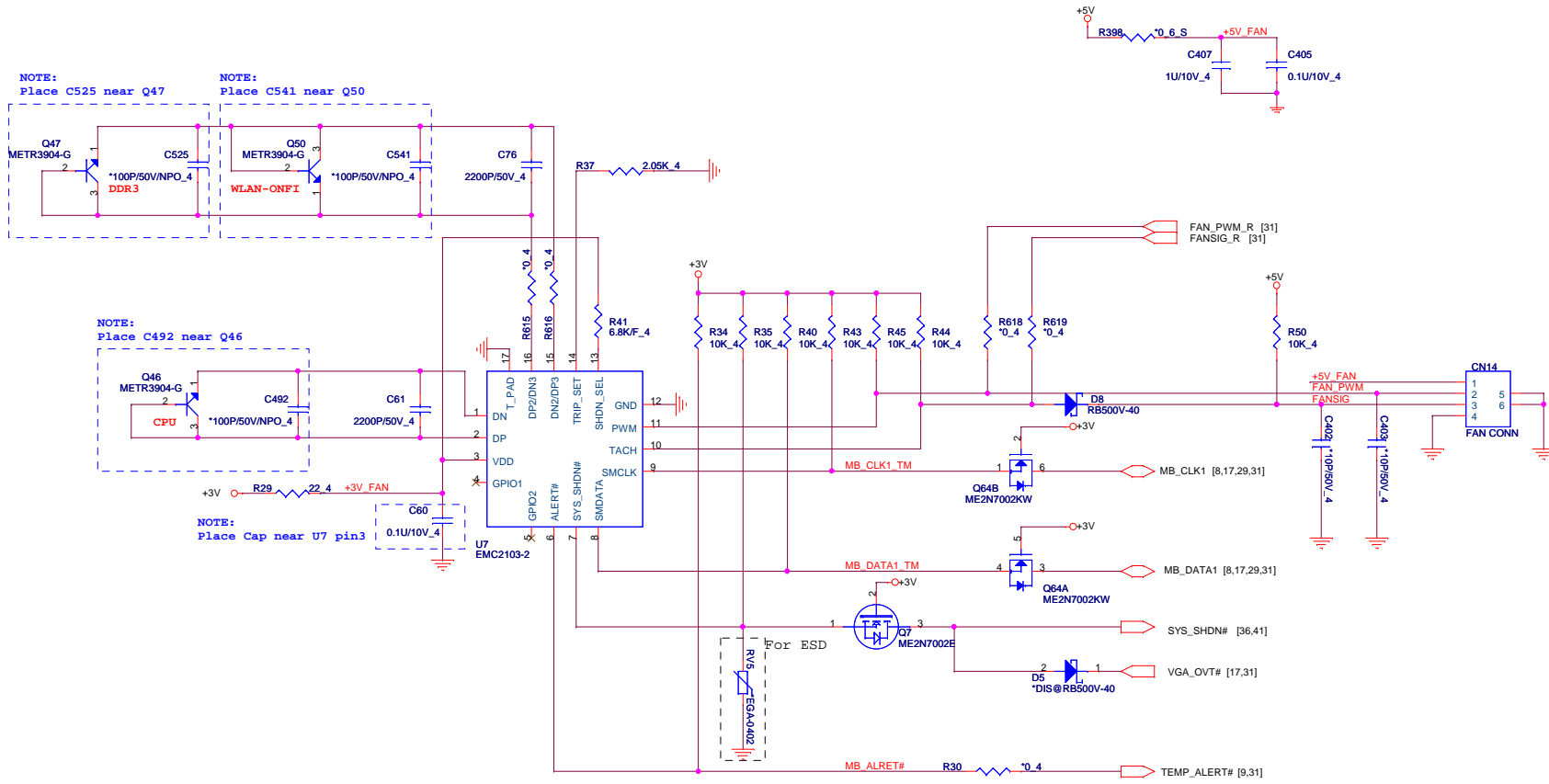


USB3.0

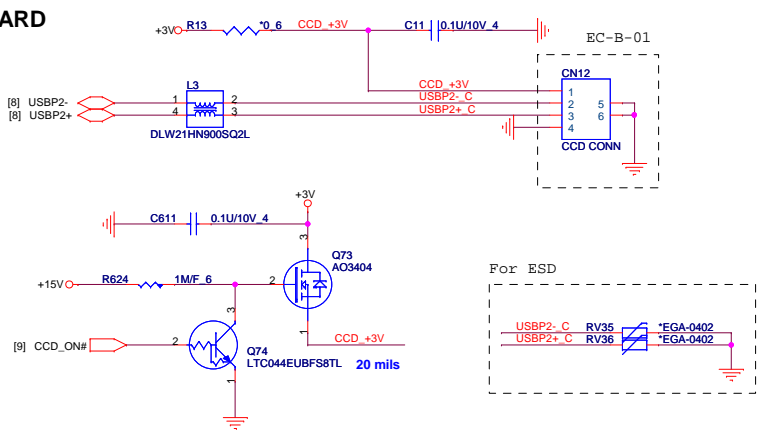


USB 2.0 BOARD UP Right

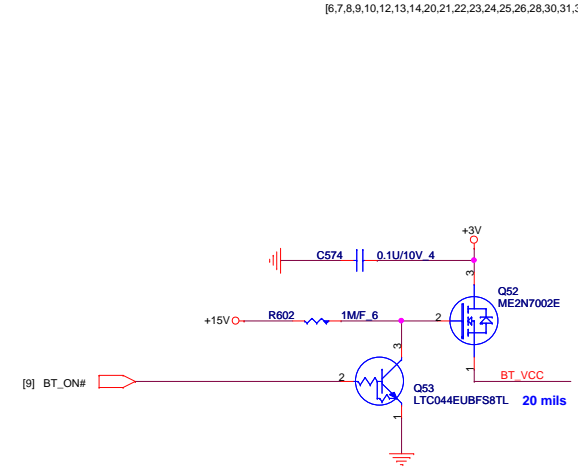




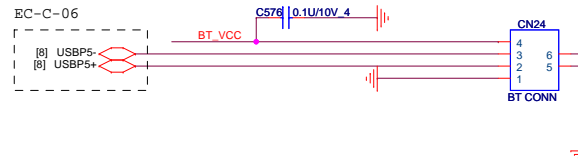
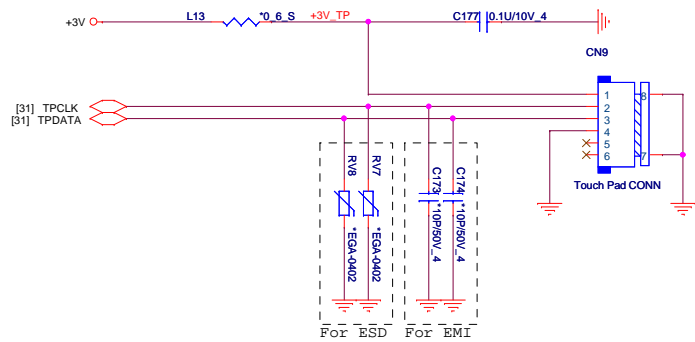
CCD BOARD



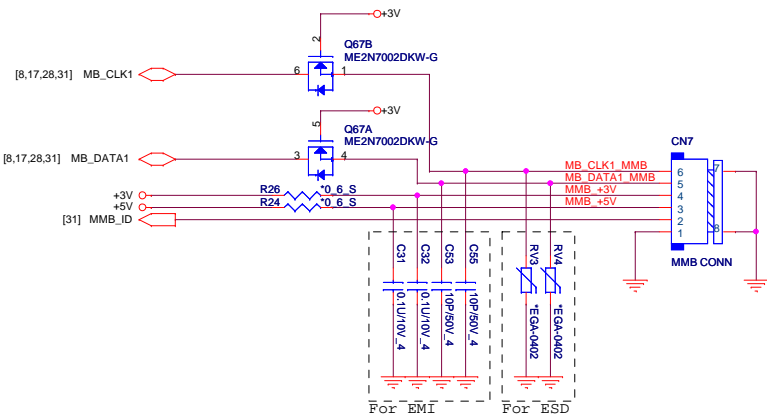
BLUETOOTH



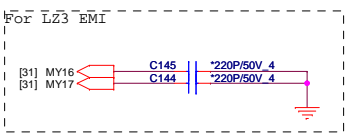
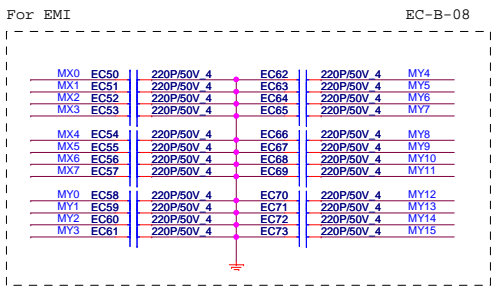
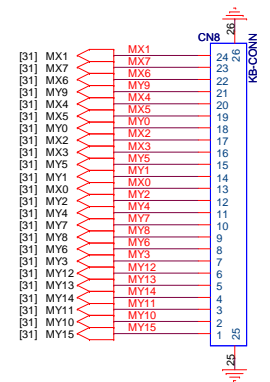
Touch pad



MMB



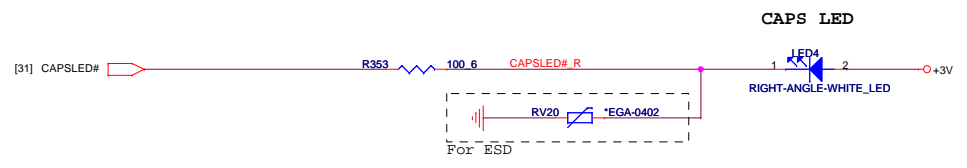
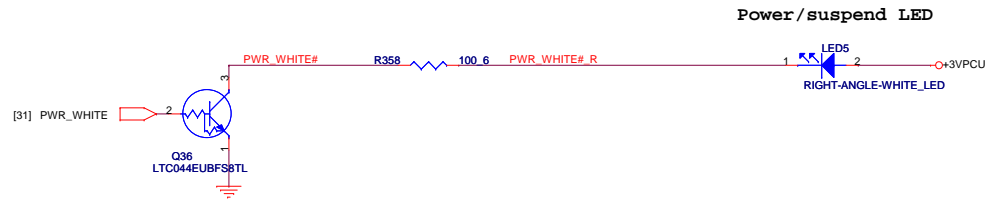
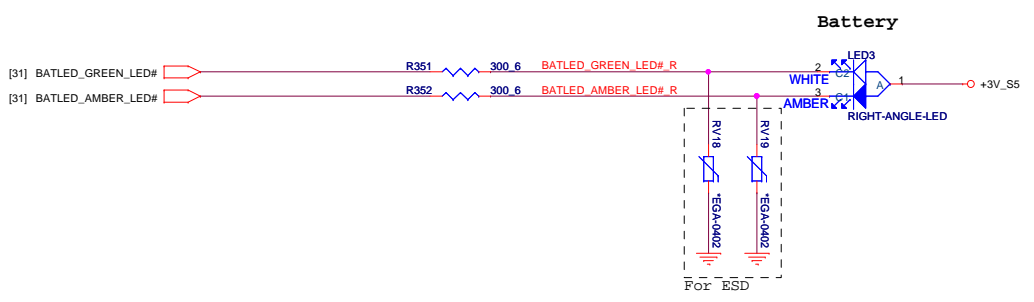
KEYBOARD



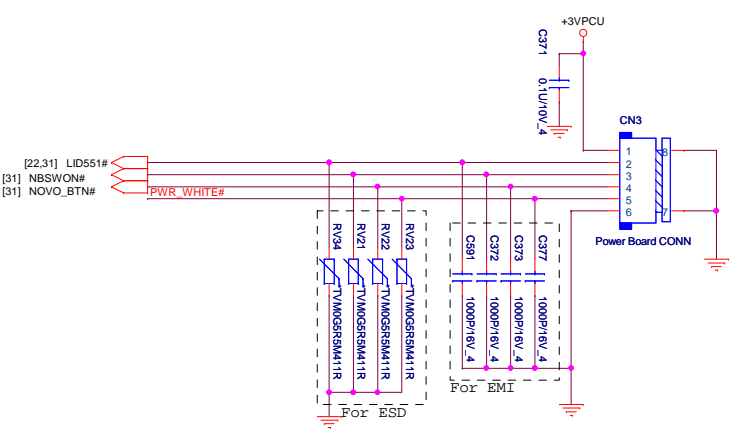
LEDs

[6,7,8,9,10,12,13,14,20,21,22,23,24,25,26,28,29,31,32,33,34,37,38,41,42,43] +3VPCU
 [2,6,7,8,9,10,26,34] +3V
 +3V_SS

30



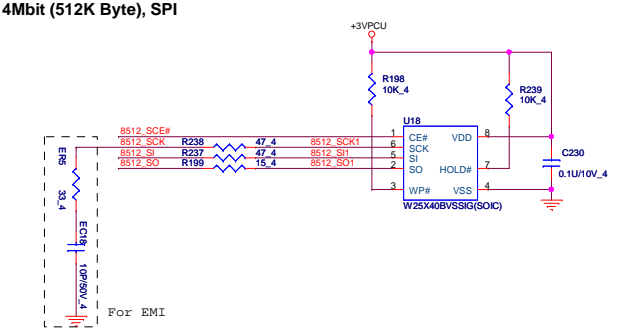
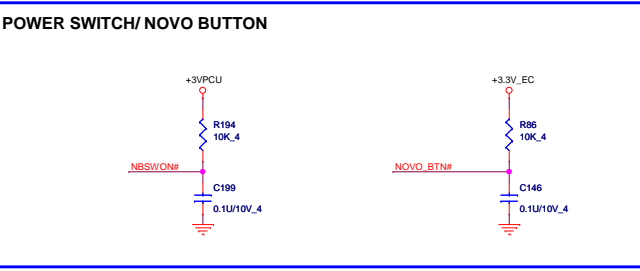
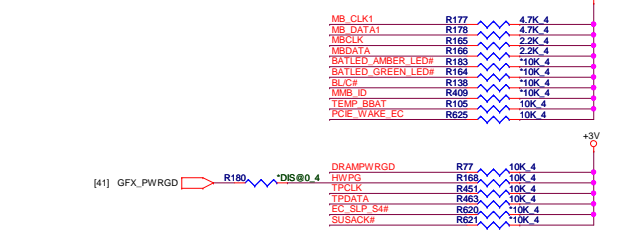
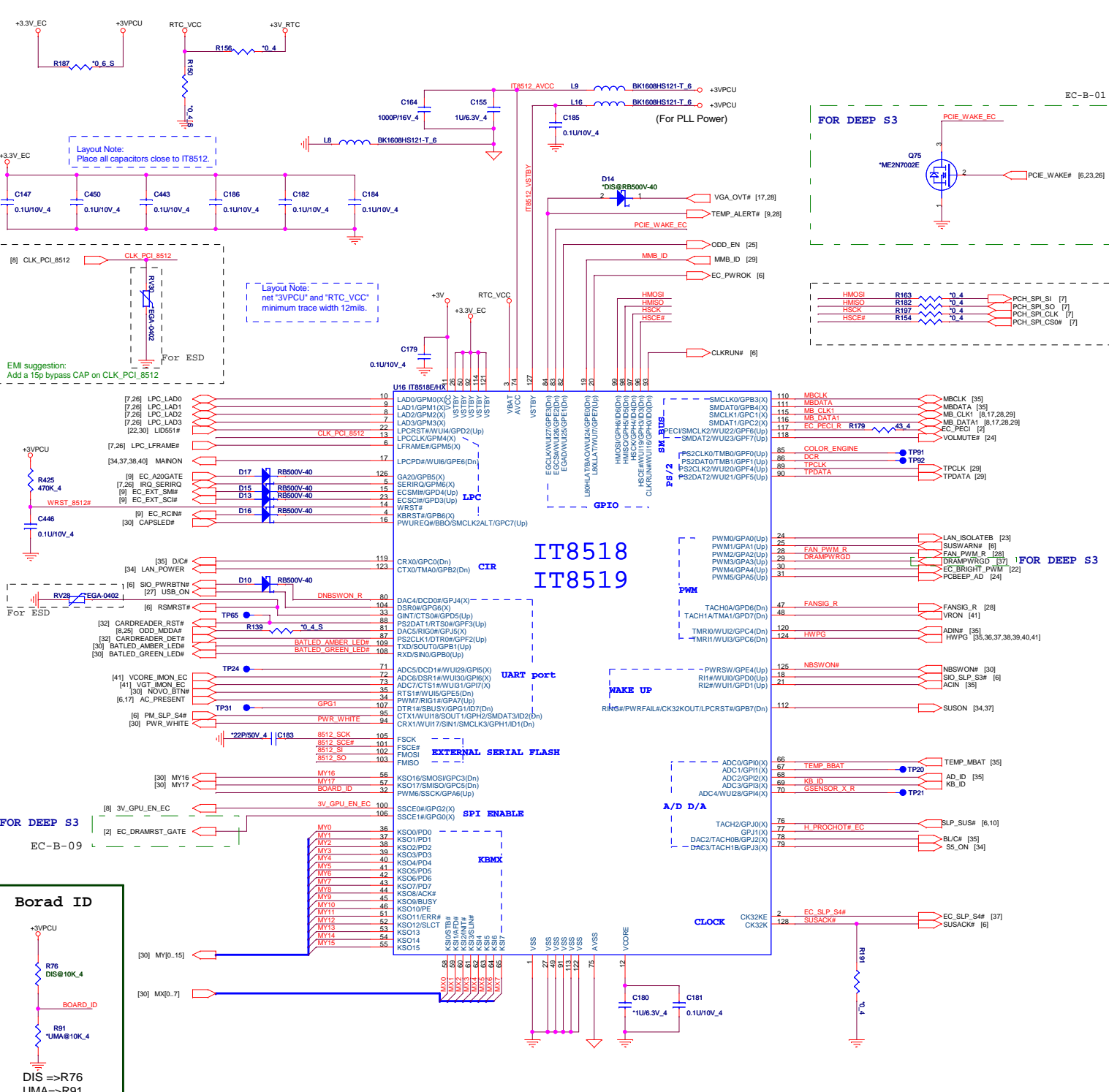
POWER BOARD



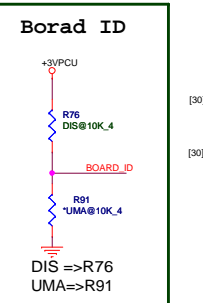
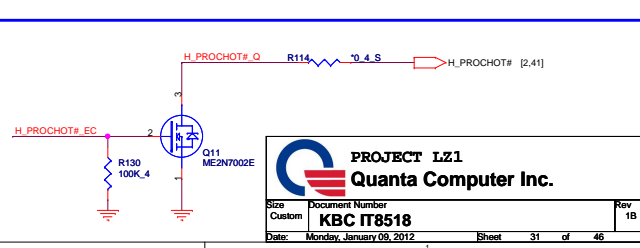
<http://sualaptop365.edu.vn>

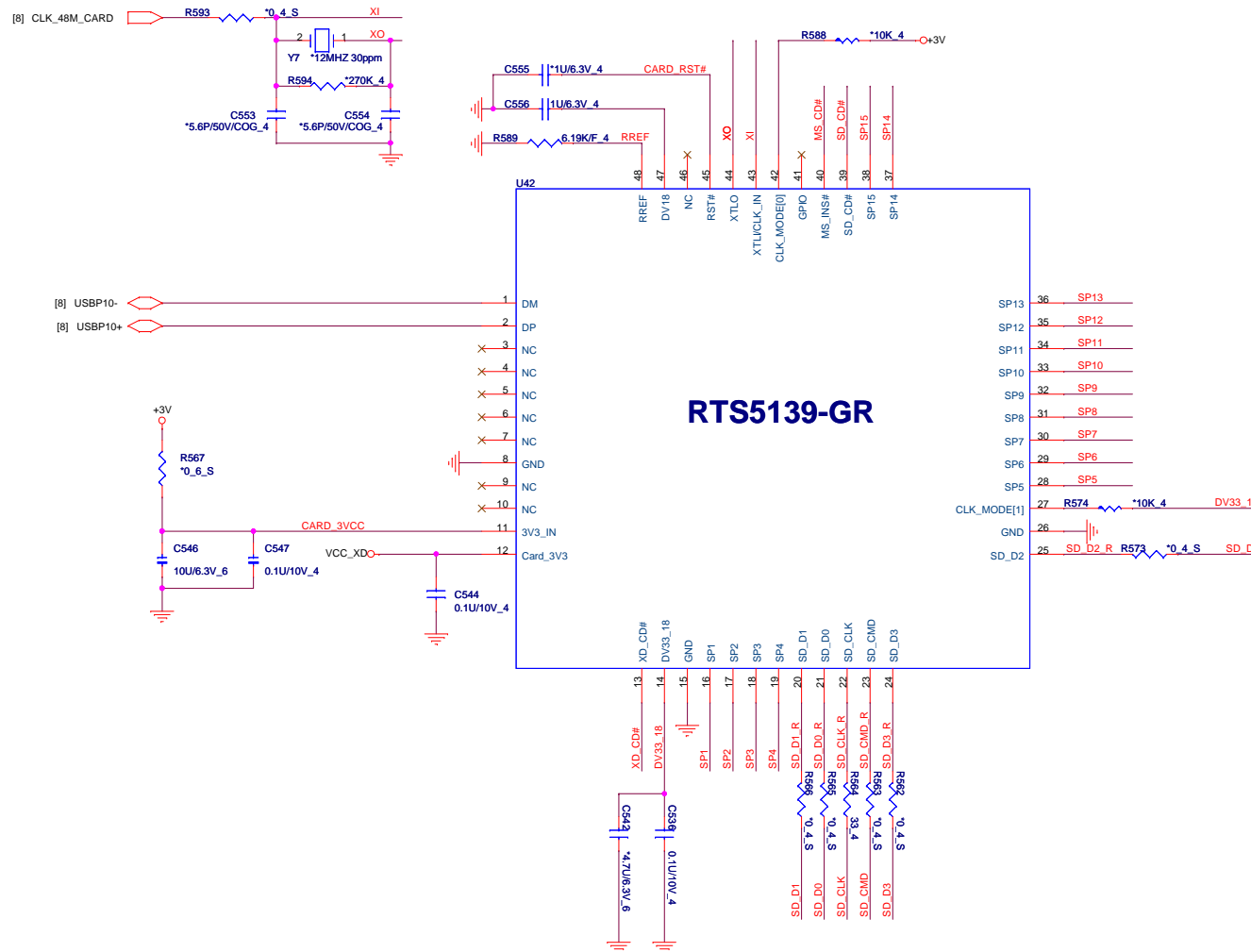
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Quanta Computer Inc.

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Project	PU/PD
Z380 (LZ1) - INTL	PU
Z480 (LZ2) - INTL	PU
Z485 (LZ2) - AMD	PU
Z580 (LZ3) - INTL	PD
Z585 (LZ3) - AMD	PD

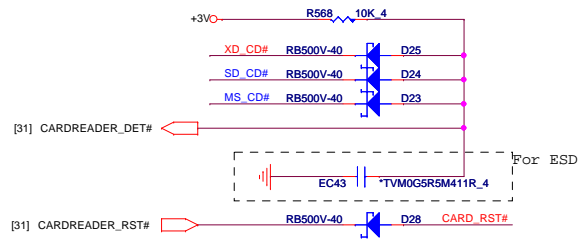
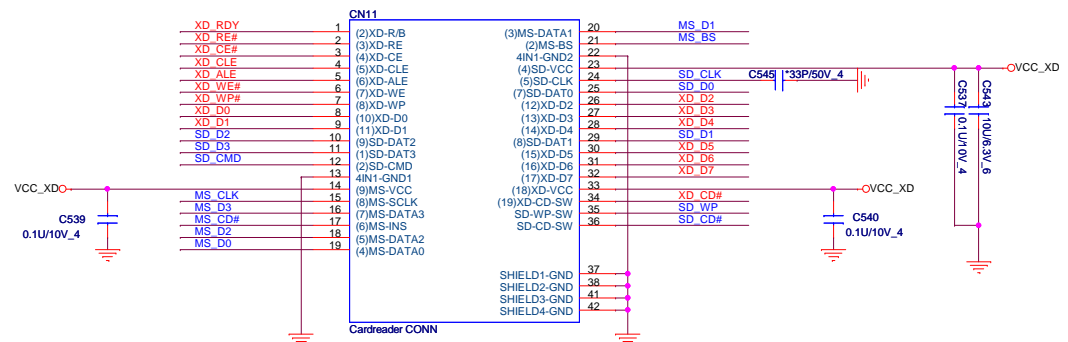




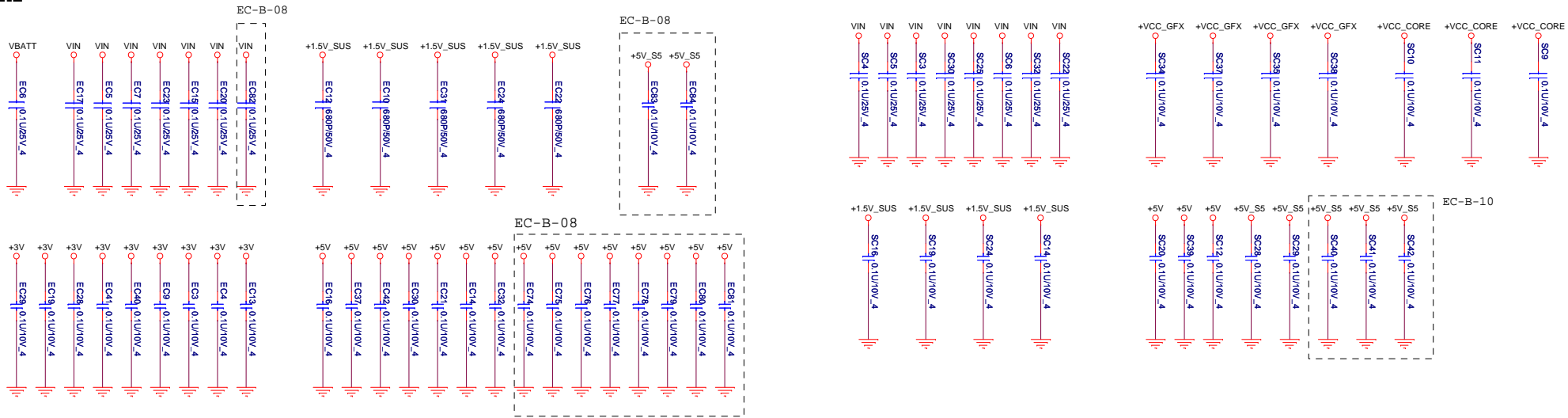
Note:

	SD/MMC	MS	XD
SP1	SD D7		XD RDY
SP2	SD D6		XD RE#
SP3	SD D5		XD CE#
SP4	SD D4		XD WE#
SP5		MS BS	XD CLE
SP6		MS D5	XD ALE
SP7		MS D1	XD WP#
SP8		MS D4	XD D0
SP9		MS D0	XD D1
SP10		MS D2	XD D2
SP11		MS D6	XD D3
SP12		MS D3	XD D4
SP13		MS D7	XD D5
SP14		MS D6	XD D6
SP15	SD WP	MS CLK	XD D7

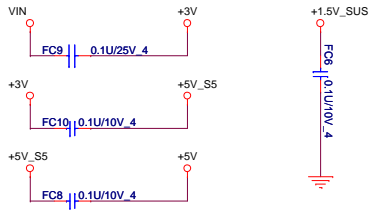
7 IN1 CARD CONN
XD, MMC/SD, MS/MSP



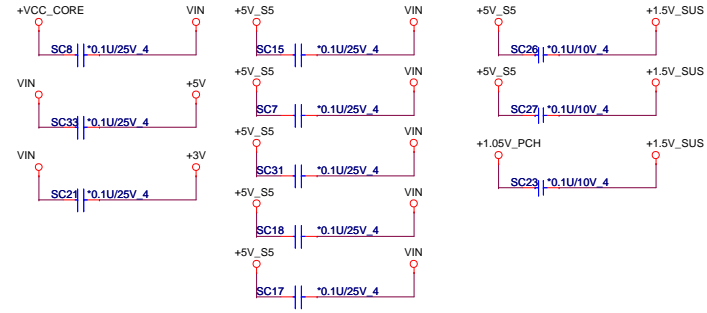
EMI



RF

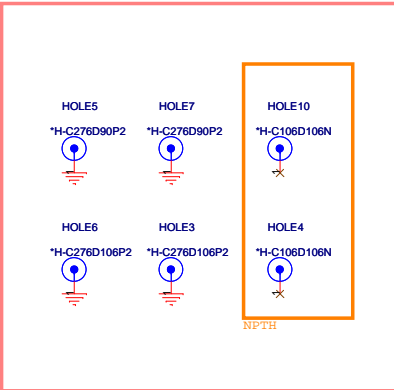
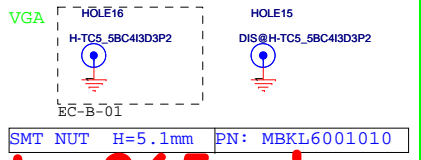
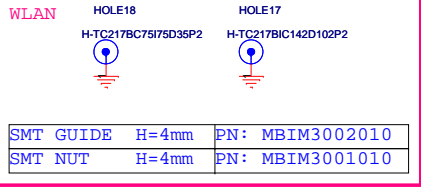
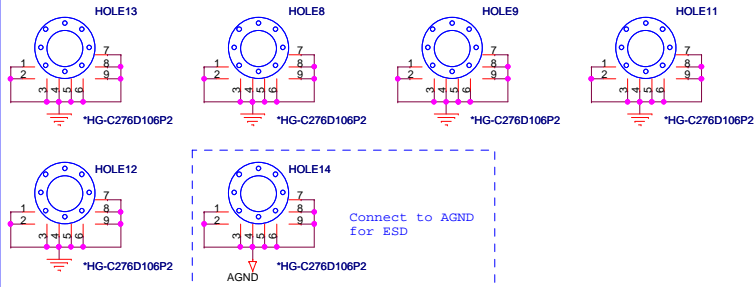


ESD

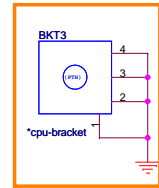


Screw For ME

ME-other holes
Round screw hole(8 guard hole)*7 for ESD



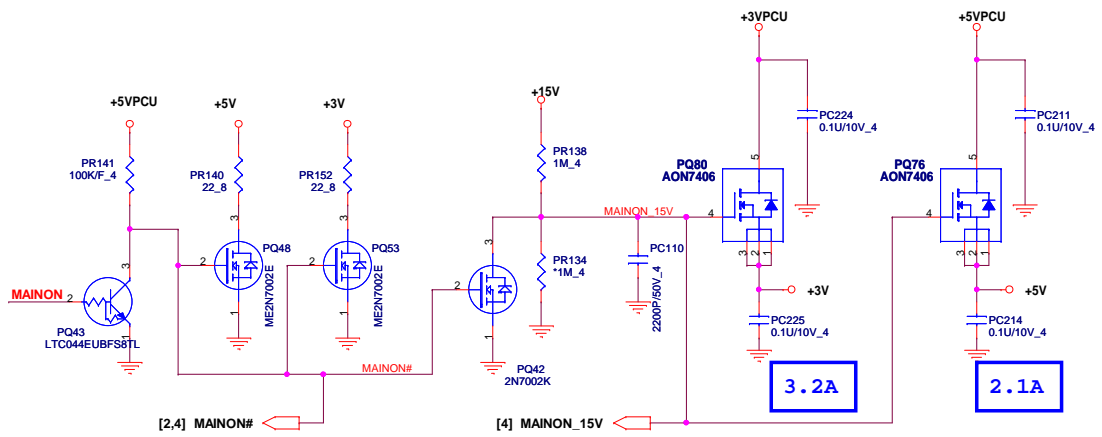
CPU BKT



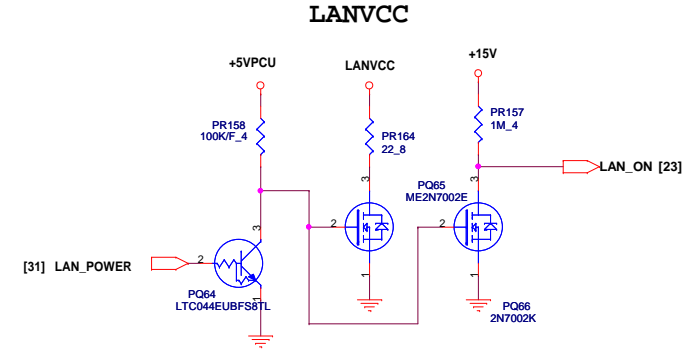
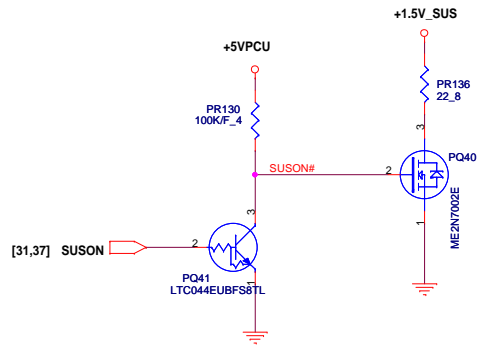
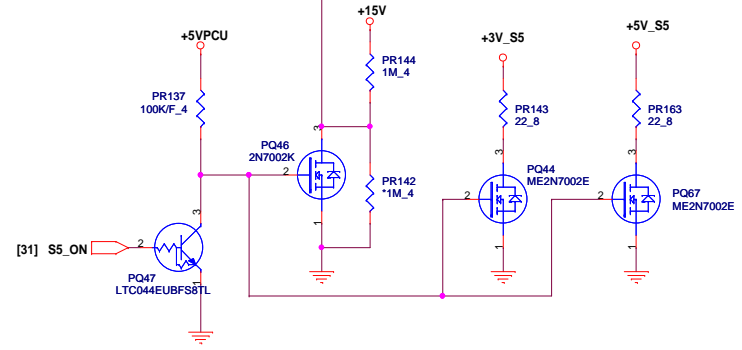
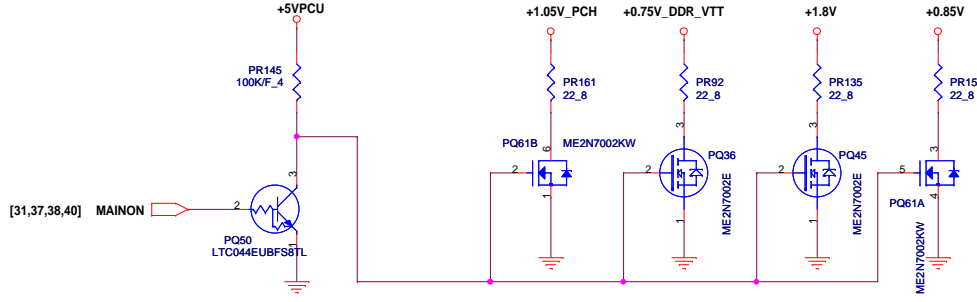
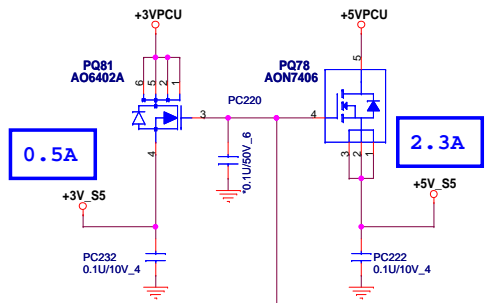
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Quanta Computer Inc.

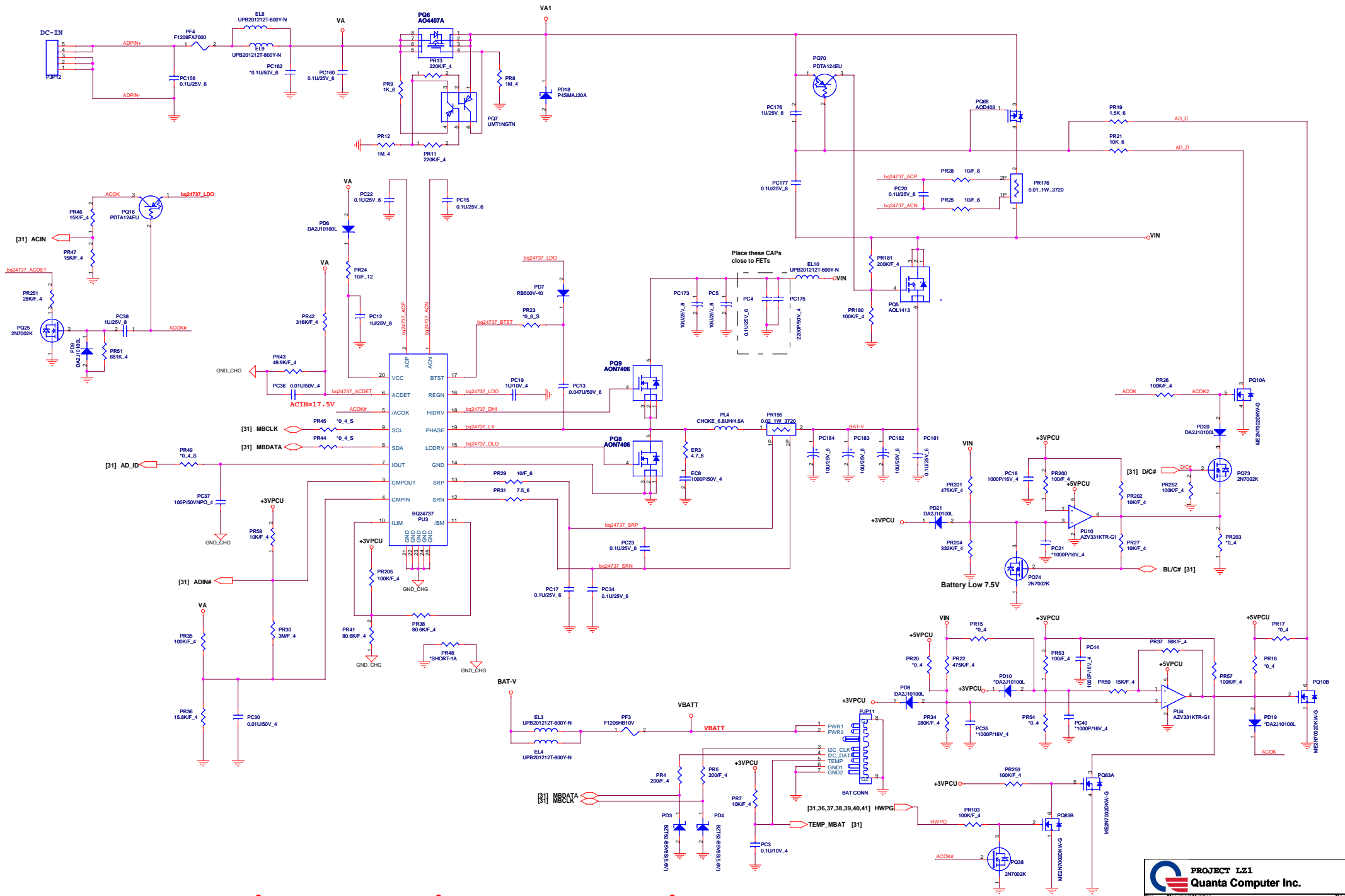
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+3V, +5V, +1.5V

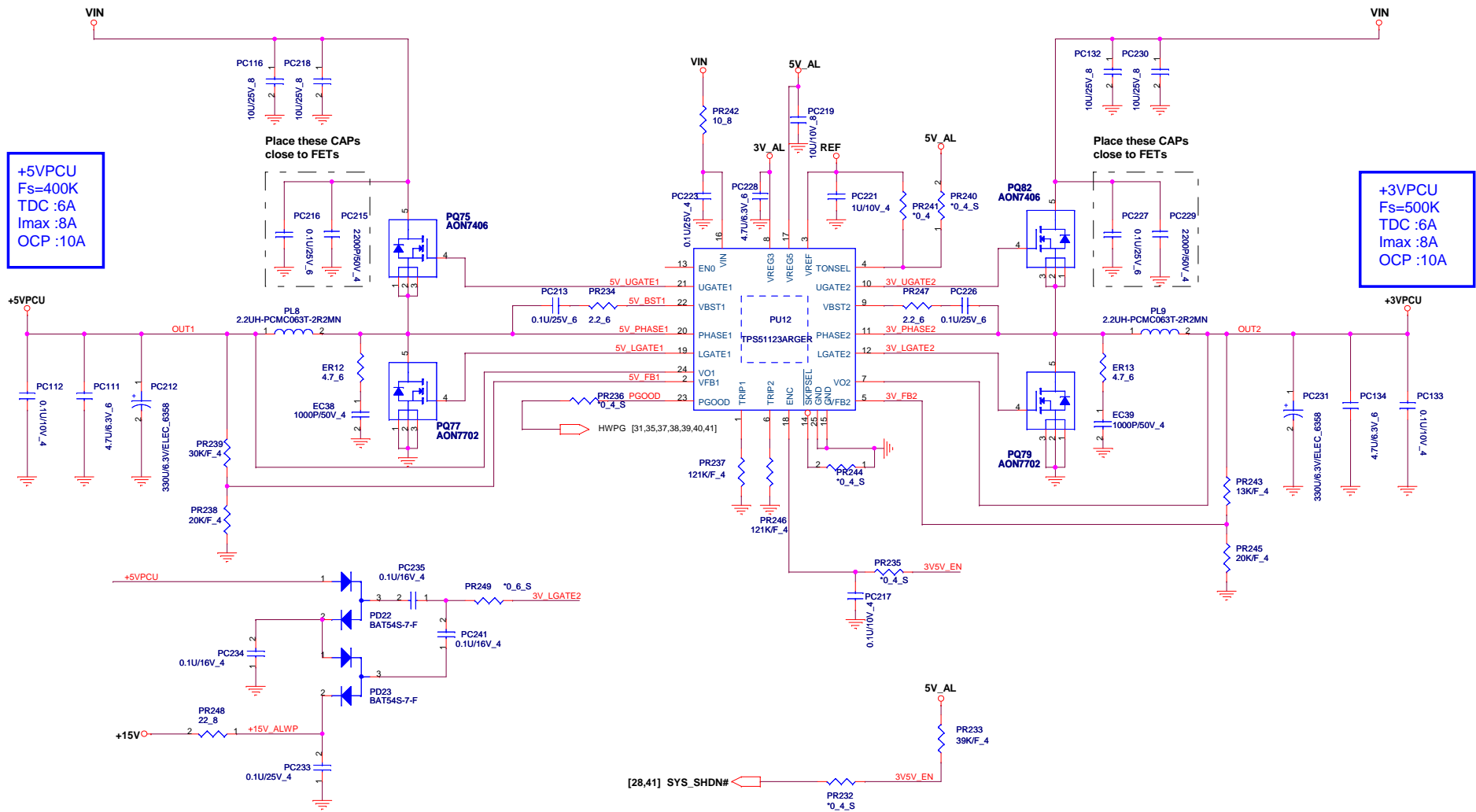


3V_S5, 5V_S5



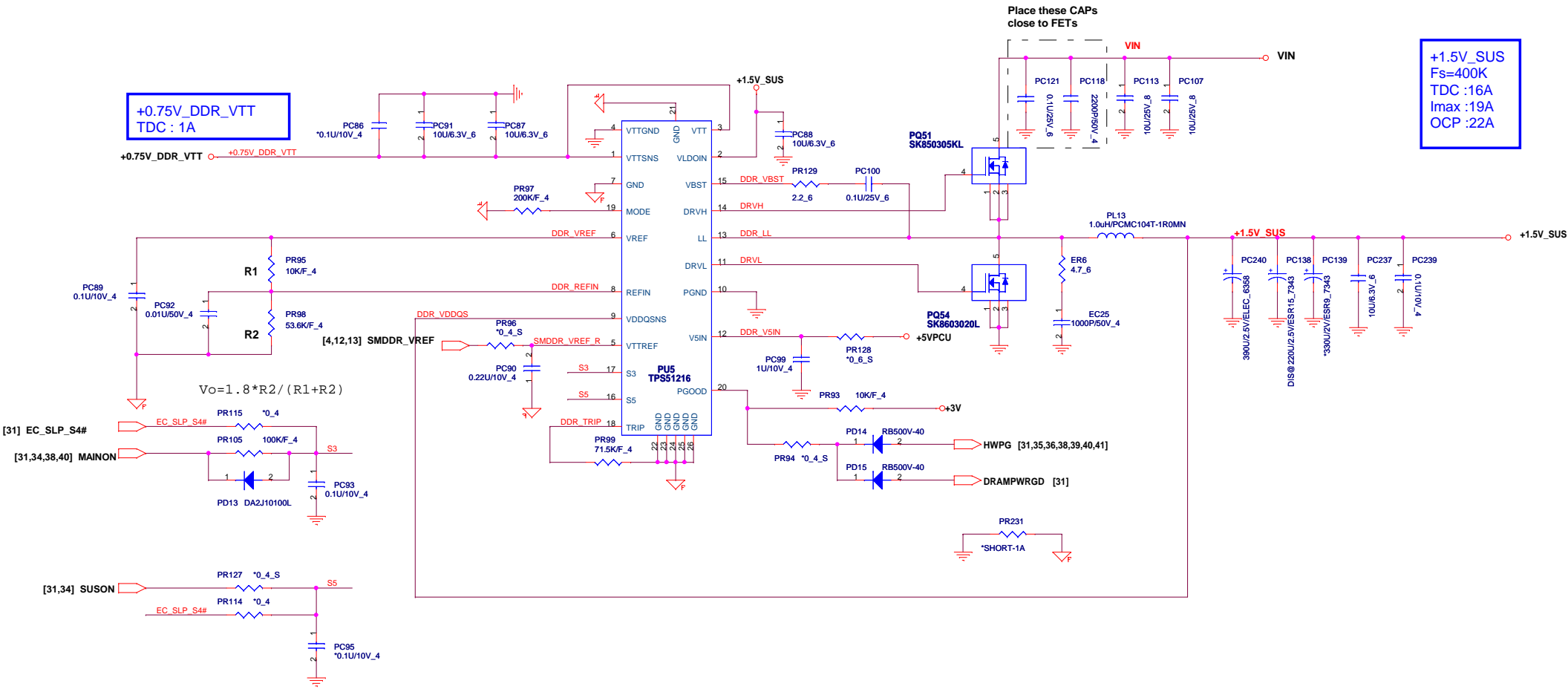


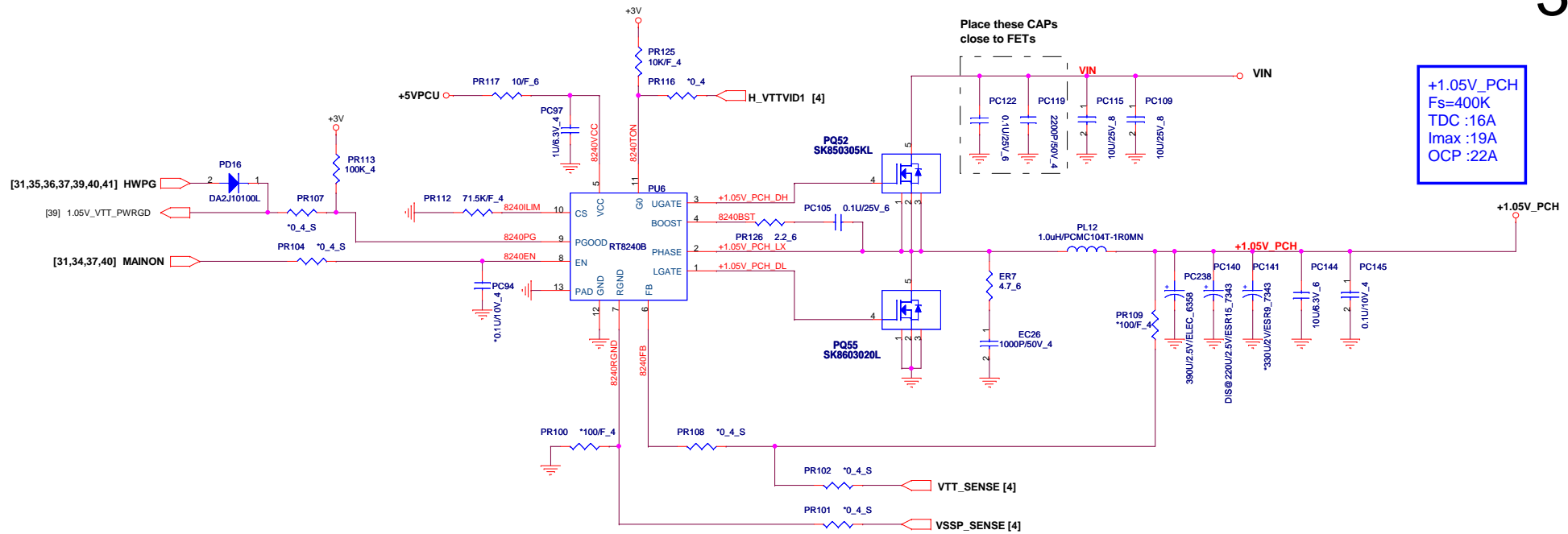
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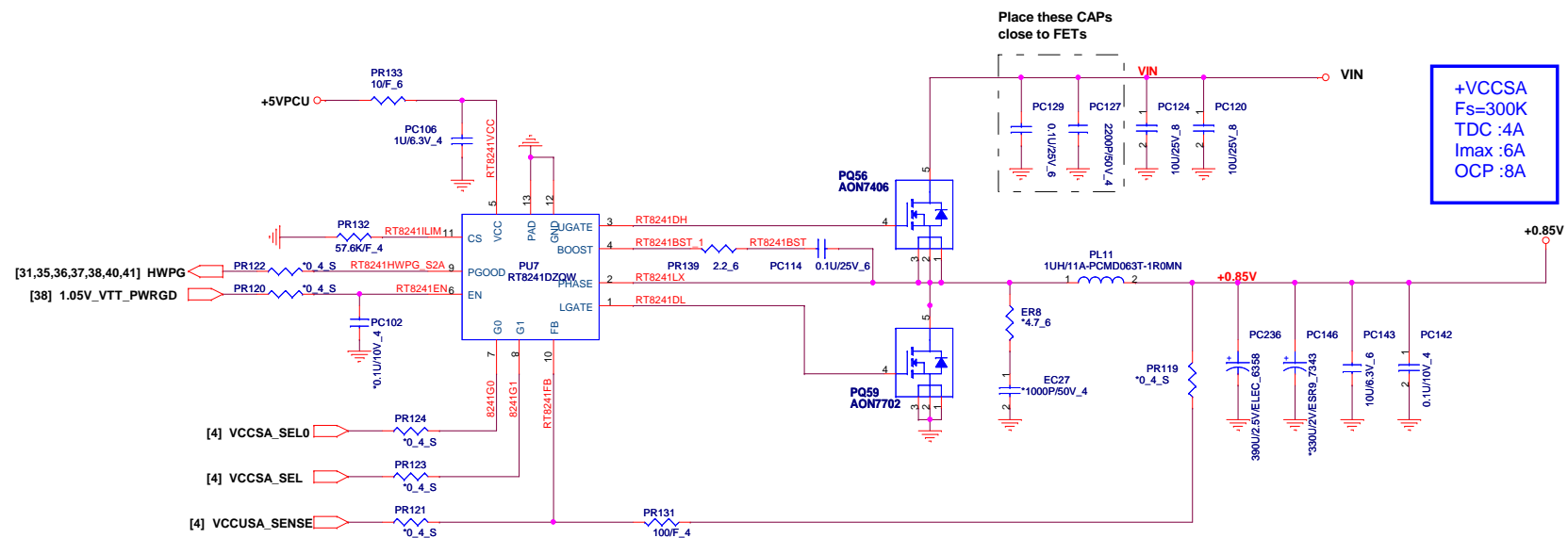
+0.75V_DDR_VTT
TDC : 1A

+1.5V_SUS
Fs=400K
TDC :16A
Imax :19A
OCP :22A





+1.05V_PCH
 Fs=400K
 TDC:16A
 Imax:19A
 OCP:22A

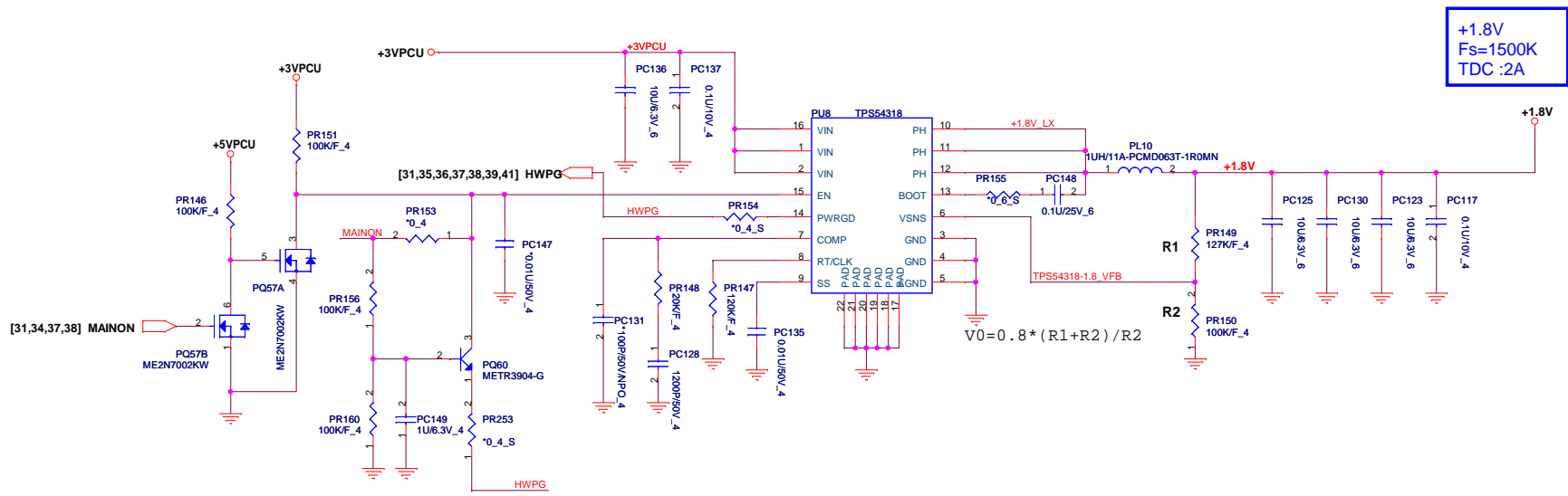


+VCCSA
 Fs=300K
 TDC :4A
 I_{max} :6A
 OCP :8A

Place these CAPs
 close to FETs

G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

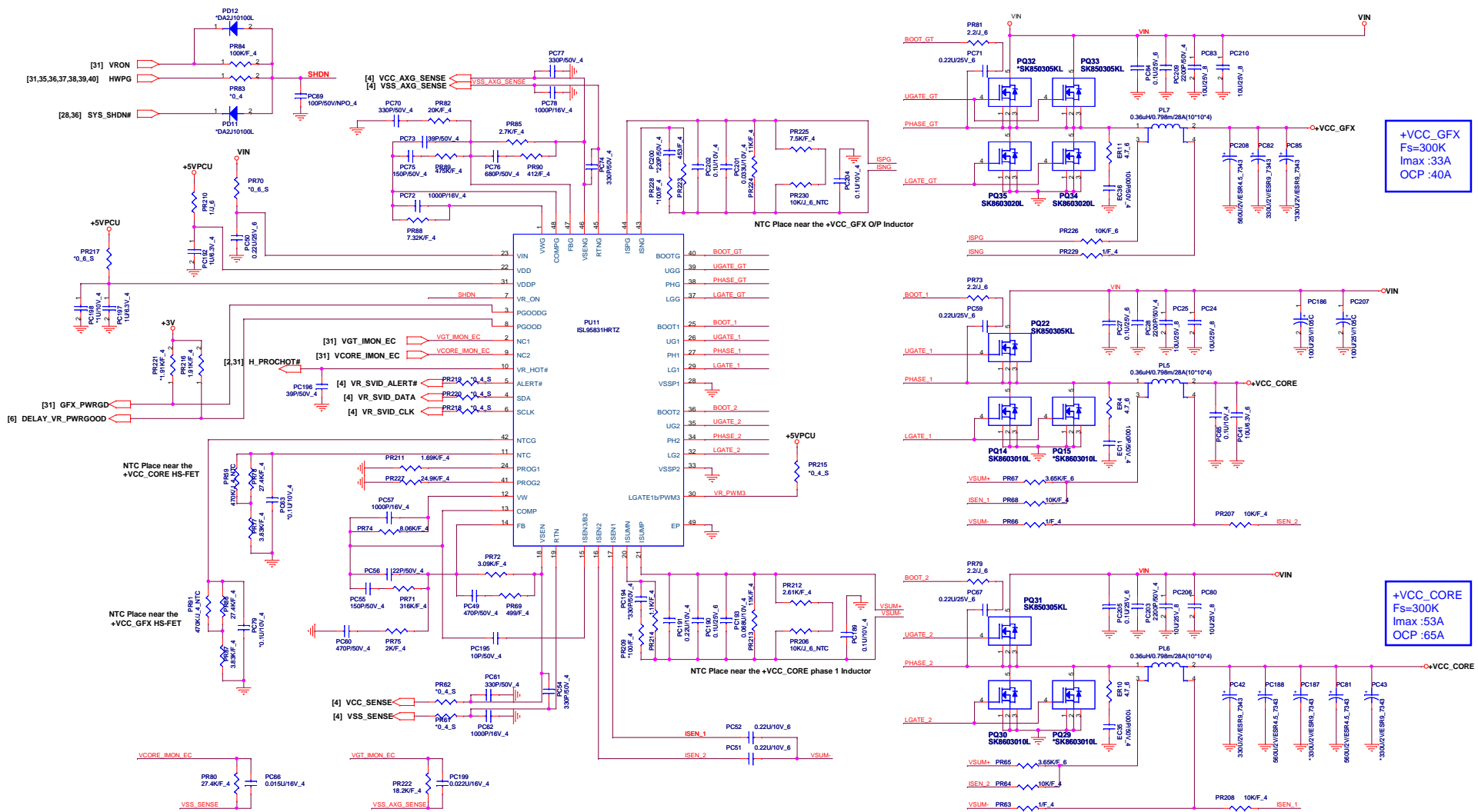


+1.8V
Fs=1500K
TDC :2A

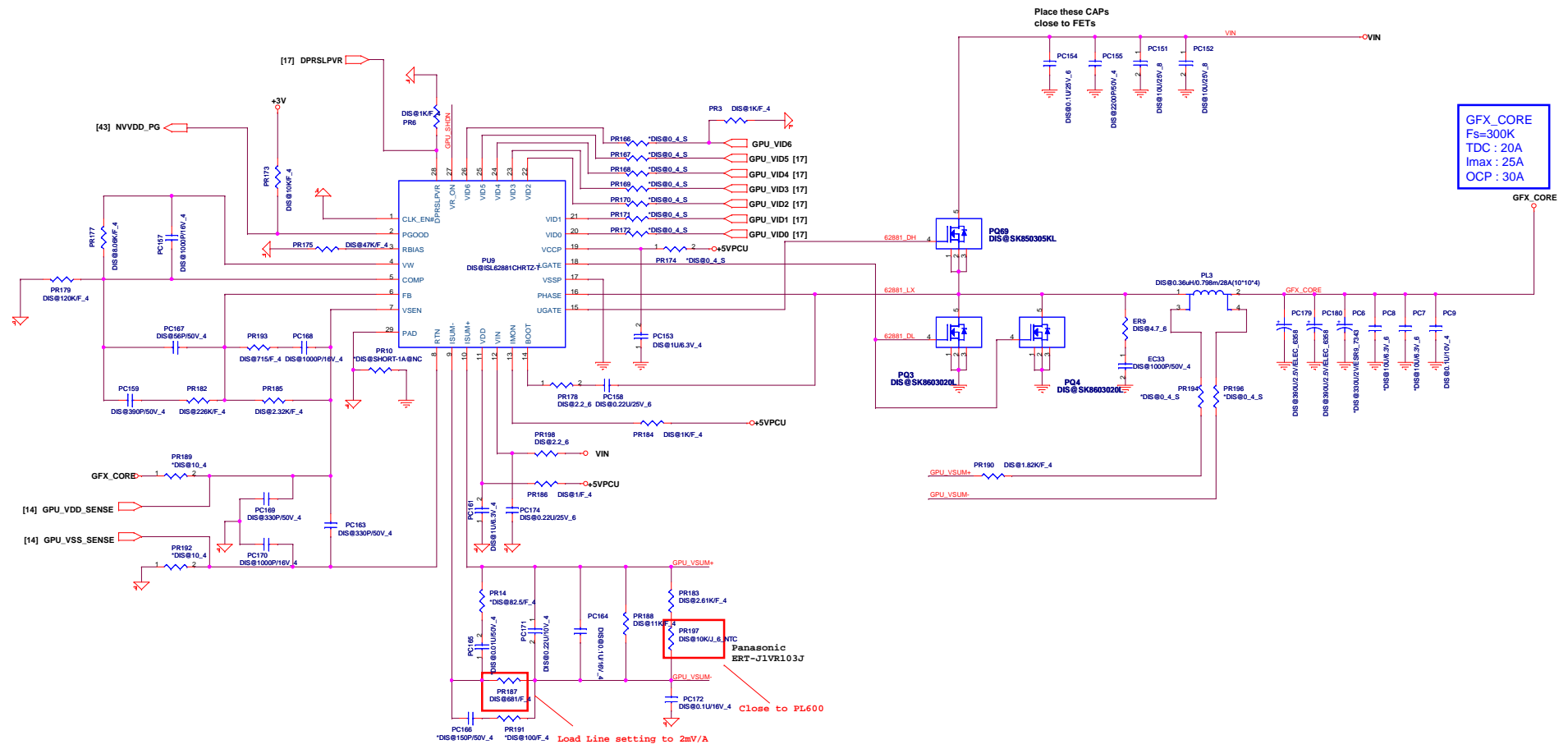
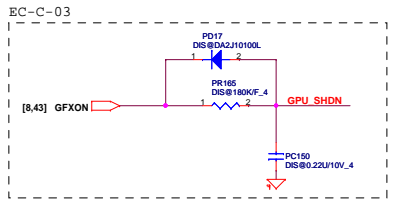
$$V0 = 0.8 * (R1 + R2) / R2$$

[31,34,37,38] MAINON

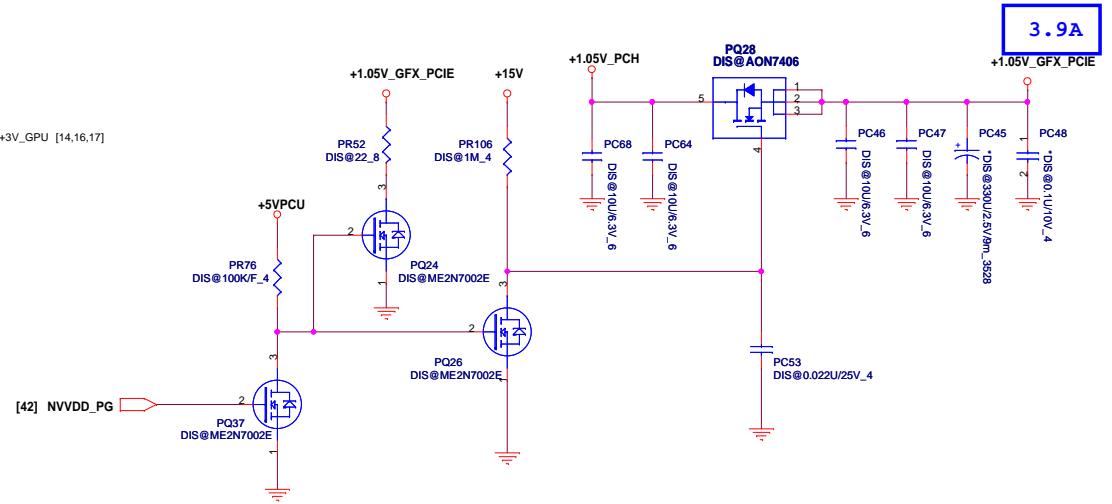
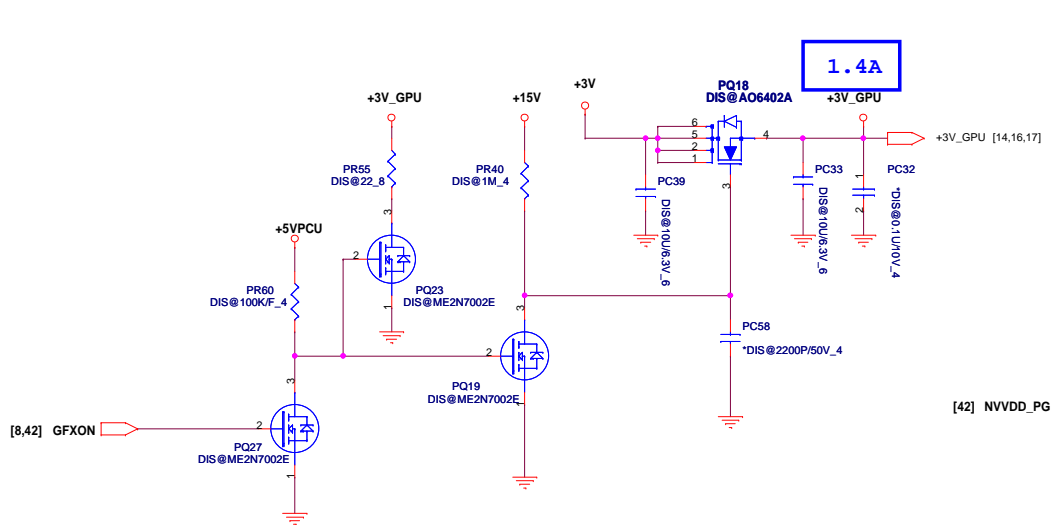
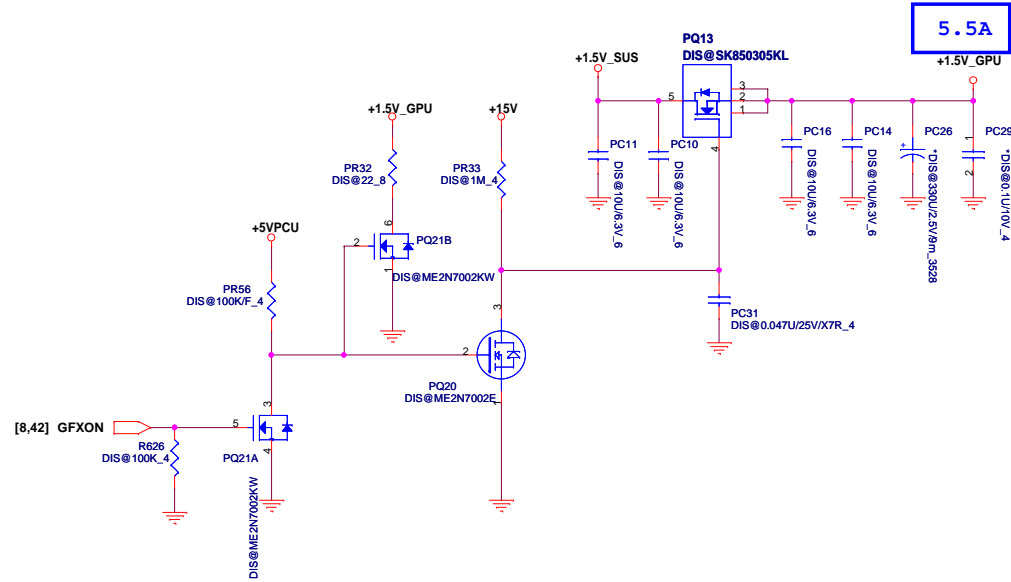
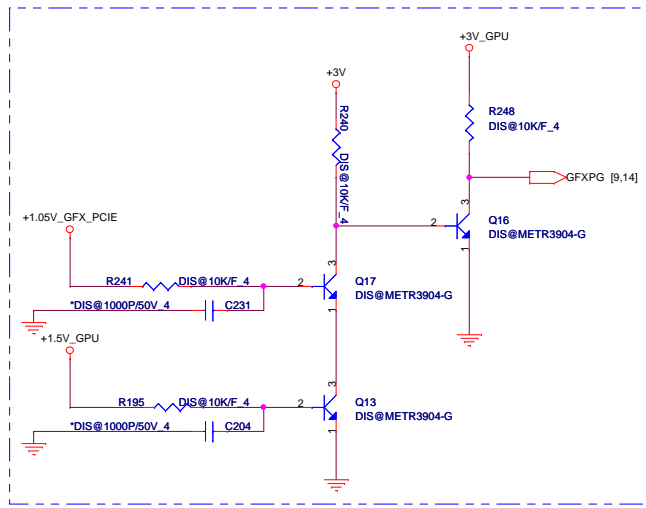
[31,35,36,37,38,39,41] HWPG

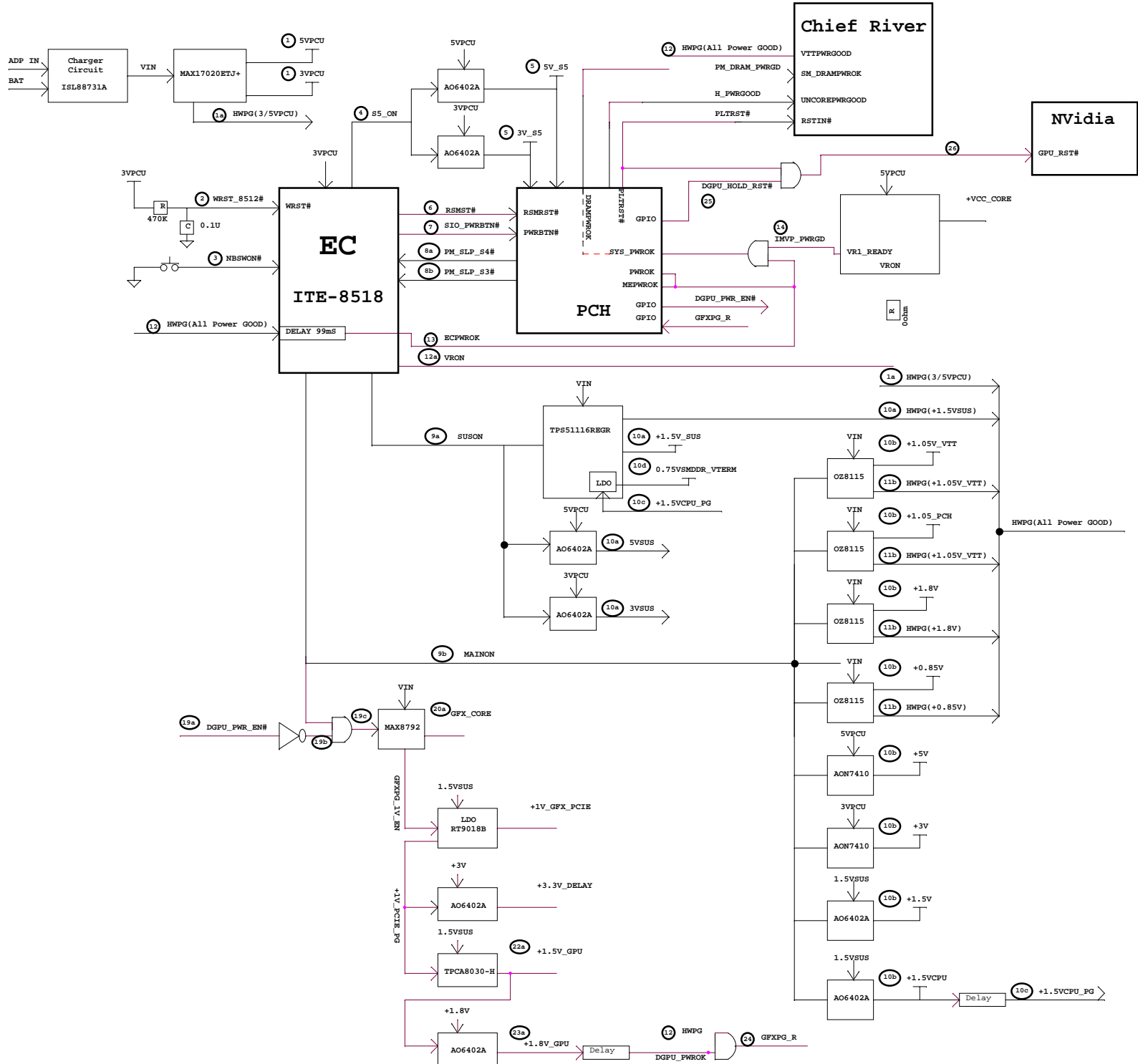


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GFX_CORE
 Fs=300K
 TDC : 20A
 I_{max} : 25A
 OCP : 30A






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LZ1 / Z380 Chief River Schematic EC Tracking Record B (for SDV,A --> SIV,B)OCT. 07, 2011

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EC #	Page	Description	Date
EC-B-01	24	Change INT_MIC type from DIP to Cable.	2011.09.14A
	33	Change VGA NUT P/N type for ME request.	2011.09.28A
EC-B-02	09	Modify Syatem ID & Board ID.	2011.09.19A
EC-B-03	22	Add and reverse 6.8pf to GND for RF request.	2011.09.20A
EC-B-05	30	Setting K/B ID.	2011.09.21A
EC-B-06	26	Modify WLAN & BT COMBO function.	2011.09.22A
EC-B-07	26	Modify AOAC function.	2011.09.22A
EC-B-08	20,23,27,30,33	Add and reverse 0.1uf to GND for EMI Request.	2011.09.22A
EC-B-09	2,6,7,10,31	Add and reverse some material for Deep S3 function.	2011.09.23A
EC-B-10	33	Reverse 0.1uf to GND for ESD Request.	2011.09.25A
EC-B-11	28,31	Change and reverse FAN control from EC .	2011.09.29A

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LZ1 / Z380 Chief River Schematic EC Tracking Record B (for SIV,B --> SIT1,C1) NOV. 07, 2011

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EC #	Page	Description	Date
EC-B-01	2,7,10,12,13,31	Modify schematoc for Deep S3 function.	2011.11.07A
EC-B-02	09	Modify Board ID.	2011.11.16A
EC-B-03	42,43	Tune GPU Sequence from Nvidia request.	2011.11.17A
EC-B-05	12,22	Add 3.3pf & 6.8pf to GND For RF Request.	2011.11.17B
EC-B-06	7,8	Modify schematic for support HM70.	2011.11.28A
EC-B-07	23	Change Transformer type for 家電下鄉surge.	2011.11.28A
EC-B-08	22	Modify brightness control from EC or PCH.	2011.11.28A
EC-B-09	24	Change INT_MIC footprint.	2011.11.28A

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		1B
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