ZZZ1
LA5971P LS5971P

ZZZ3
LA5971P
DAZ@

ZZZ4
LS5971P
DAZ@

Compal Confidential

NAWA1 Schematics Document

AMD Tigris: Caspian Processor with RS880M/SB710/Park-S3 & M93-S3

2009-11-26

Security Classification	Compal Secret Data		
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Title: Cover Page

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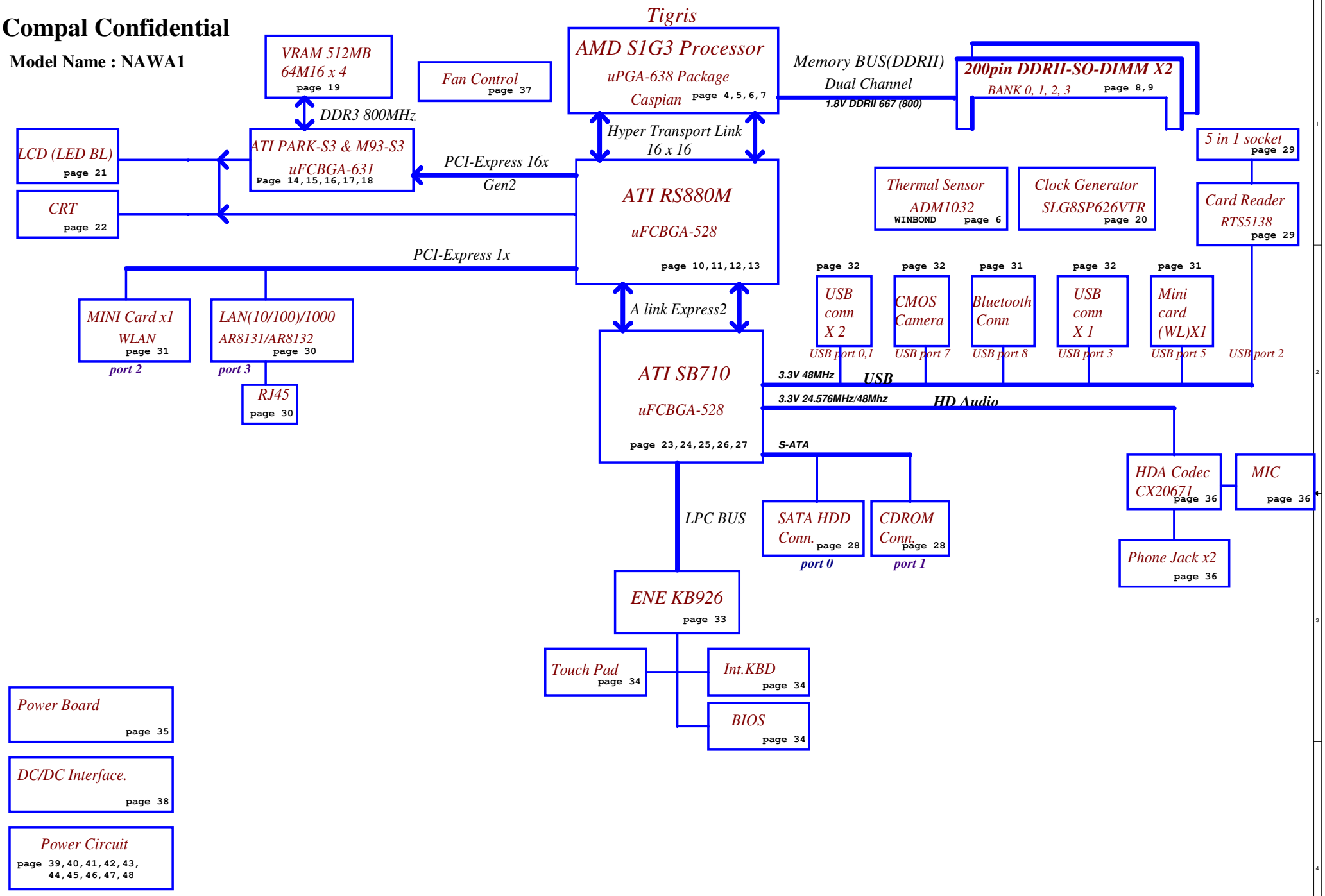
Model Name : NAWA1



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Title: Block Diagrams

Size	Document Number	Rev
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

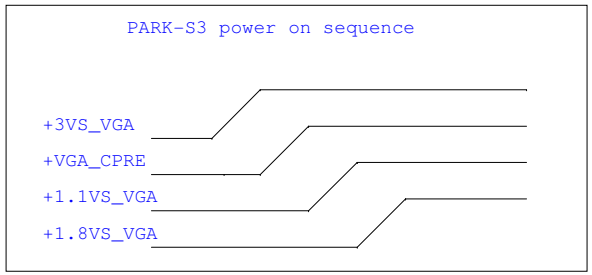
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

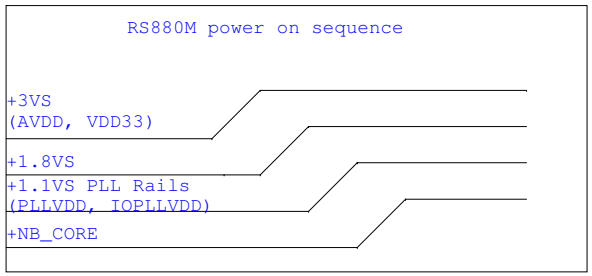
BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
PARK	PARK@
M93	M93@
HDT debug	HDT@
UMA	UMA@
Wireless LAN	WLAN@
Blue Tooth	BT@
Camera	CMOS@
New Card	New Card@
VRAM	X76@
UNPON	@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

NAWA1_UMA : UMA@/WLAN@/BT@/CMOS@/NEW CARD@
NAWA1_DIS : VGA@/M93@/WLAN@/BT@/NEW CARD@/CMOS@/X76@





External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
GMT G781-1 (GPU)	1001 101X b	9AH
SB-Temp Sensor		9CH

SB710 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB710 SM Bus 1 address

Device	Address
New card	

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Title: Notes List

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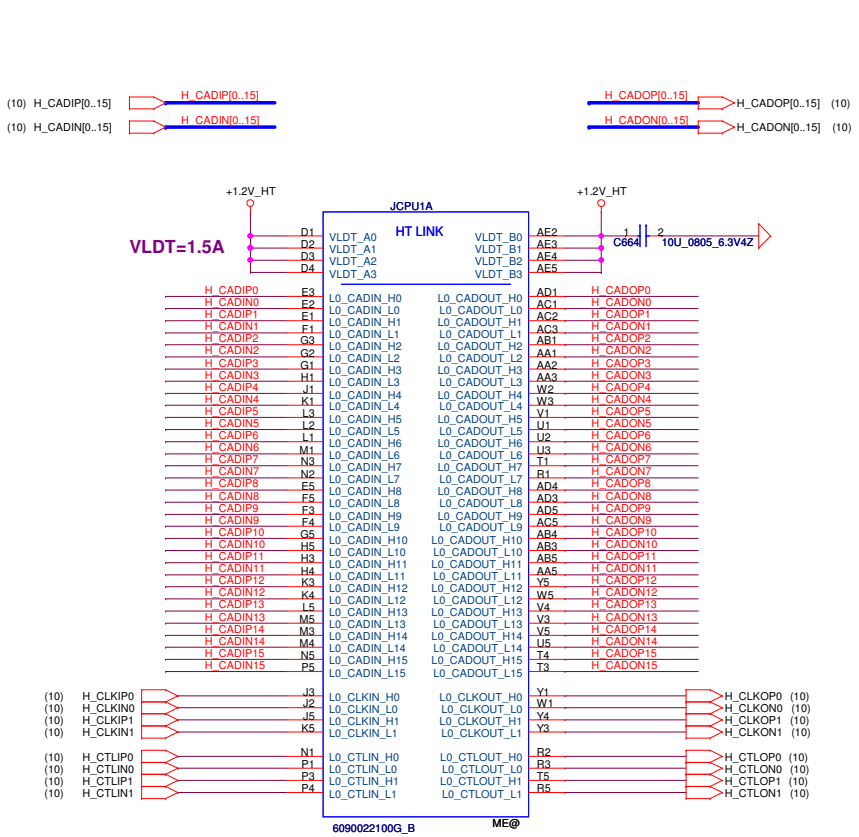

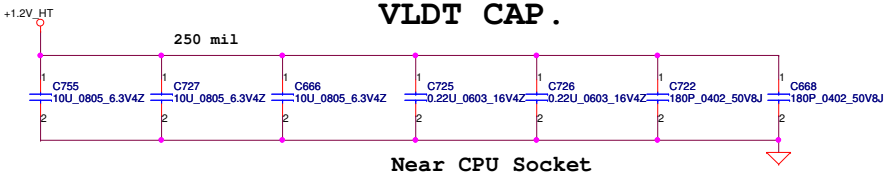

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Title: AMD CPU S1G3 HT I/F

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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.2 INCH

+1.8V
R78 1K_0402_1%
R79 1K_0402_1%
+MCH_REF
C178 0.1U_0402_16V4Z
C177 1000P_0402_25V8J

DDRA_CLK0 — C888 1.5P_0402_50V9C
DDRA_CLK0#
DDRA_CLK1 — C891 1.5P_0402_50V9C
DDRA_CLK1#
DDRB_CLK0 — C890 1.5P_0402_50V9C
DDRB_CLK0#
DDRB_CLK1 — C889 1.5P_0402_50V9C
DDRB_CLK1#

VTT=0.75A
Place them close to CPU within 1"
+0.9V
R77 39.2_0402_1%
R76 39.2_0402_1%

JCPU1B
MEM:CMD/CTRL/CLK

D10	VTT1	VTT5	W10
C10	VTT2	VTT6	AC10
B10	VTT3	VTT7	AB10
AD10	VTT4	VTT8	AA10
		VTT9	A10
AF10	MEMZP		
AE10	MEMZN	VTT_SENSE	Y10 — VTT_SENSE — PAD T4
H16	RSVD_M1	MEMVREF	W17 — +MCH_REF
T19 — DDRA_ODT0 — (8) DDRA_ODT0	MA0_ODT0	RSVD_M2	B18
V22 — DDRA_ODT1 — (8) DDRA_ODT1	MA0_ODT1		
U21	MA1_ODT0	MB0_ODT0	W26 — DDRB_ODT0 — DDRB_ODT0 (9)
V19	MA1_ODT1	MB0_ODT1	W23 — DDRB_ODT1 — DDRB_ODT1 (9)
		MB1_ODT0	Y26
T20 — DDRA_SCS0# — (8) DDRA_SCS0#	MA0_CS_L0	MB0_CS_L0	V26 — DDRB_SCS0# — DDRB_SCS0# (9)
U19 — DDRA_SCS1# — (8) DDRA_SCS1#	MA0_CS_L1	MB0_CS_L1	W25 — DDRB_SCS1# — DDRB_SCS1# (9)
U20	MA1_CS_L0	MB1_CS_L0	U22
V20	MA1_CS_L1		
J22 — DDRA_CKE0 — (8) DDRA_CKE0	MA_CKE0	MB_CKE0	J25 — DDRB_CKE0 — DDRB_CKE0 (9)
J20 — DDRA_CKE1 — (8) DDRA_CKE1	MA_CKE1	MB_CKE1	H26 — DDRB_CKE1 — DDRB_CKE1 (9)
N19	MA_CLK_H0	MB_CLK_H0	P22
N20	MA_CLK_L0	MB_CLK_L0	R22
E16 — DDRA_CLK0 — (8) DDRA_CLK0	MA_CLK_H1	MB_CLK_H1	A17 — DDRB_CLK0 — DDRB_CLK0 (9)
F16 — DDRA_CLK0# — (8) DDRA_CLK0#	MA_CLK_L1	MB_CLK_L1	A18 — DDRB_CLK0# — DDRB_CLK0# (9)
Y16 — DDRA_CLK1 — (8) DDRA_CLK1	MA_CLK_H2	MB_CLK_H2	AF18 — DDRB_CLK1 — DDRB_CLK1 (9)
AA16 — DDRA_CLK1# — (8) DDRA_CLK1#	MA_CLK_L2	MB_CLK_L2	AF17 — DDRB_CLK1# — DDRB_CLK1# (9)
P19	MA_CLK_H3	MB_CLK_H3	R26
P20	MA_CLK_L3	MB_CLK_L3	R25

(8) DDRA_SMA[15..0] — DDRB_SMA[15..0] (9)

N21 — DDRA_SMA0	MA_ADD0	MB_ADD0	P24 — DDRB_SMA0
M20 — DDRA_SMA1	MA_ADD1	MB_ADD1	N24 — DDRB_SMA1
N22 — DDRA_SMA2	MA_ADD2	MB_ADD2	P26 — DDRB_SMA2
M19 — DDRA_SMA3	MA_ADD3	MB_ADD3	N23 — DDRB_SMA3
M22 — DDRA_SMA4	MA_ADD4	MB_ADD4	N26 — DDRB_SMA4
L20 — DDRA_SMA5	MA_ADD5	MB_ADD5	L23 — DDRB_SMA5
M24 — DDRA_SMA6	MA_ADD6	MB_ADD6	L24 — DDRB_SMA6
L21 — DDRA_SMA7	MA_ADD7	MB_ADD7	M26 — DDRB_SMA7
L19 — DDRA_SMA8	MA_ADD8	MB_ADD8	K26 — DDRB_SMA8
K22 — DDRA_SMA9	MA_ADD9	MB_ADD9	T26 — DDRB_SMA9
R21 — DDRA_SMA10	MA_ADD10	MB_ADD10	L26 — DDRB_SMA10
L22 — DDRA_SMA11	MA_ADD11	MB_ADD11	L25 — DDRB_SMA11
K20 — DDRA_SMA12	MA_ADD12	MB_ADD12	W24 — DDRB_SMA12
V24 — DDRA_SMA13	MA_ADD13	MB_ADD13	J23 — DDRB_SMA13
K24 — DDRA_SMA14	MA_ADD14	MB_ADD14	J24 — DDRB_SMA14
K19 — DDRA_SMA15	MA_ADD15	MB_ADD15	DDRB_SMA15

R20 — DDRA_SBS0# — (8) DDRA_SBS0#	MA_BANK0	MB_BANK0	R24 — DDRB_SBS0# — DDRB_SBS0# (9)
R23 — DDRA_SBS1# — (8) DDRA_SBS1#	MA_BANK1	MB_BANK1	U26 — DDRB_SBS1# — DDRB_SBS1# (9)
J21 — DDRA_SBS2# — (8) DDRA_SBS2#	MA_BANK2	MB_BANK2	J26 — DDRB_SBS2# — DDRB_SBS2# (9)
R19 — DDRA_SRAS# — (8) DDRA_SRAS#	MA_RAS_L	MB_RAS_L	U25 — DDRB_SRAS# — DDRB_SRAS# (9)
T22 — DDRA_SCAS# — (8) DDRA_SCAS#	MA_CAS_L	MB_CAS_L	U24 — DDRB_SCAS# — DDRB_SCAS# (9)
T24 — DDRA_SWE# — (8) DDRA_SWE#	MA_WE_L	MB_WE_L	U23 — DDRB_SWE# — DDRB_SWE# (9)

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ME@

(9) DDRB_SDQ[63..0]

JCPU1C
MEM:DATA

DDRB_SDQ0	C11	MB_DATA0	MA_DATA0	G12 — DDRA_SDQ0
DDRB_SDQ1	A11	MB_DATA1	MA_DATA1	F12 — DDRA_SDQ1
DDRB_SDQ2	A14	MB_DATA2	MA_DATA2	H14 — DDRA_SDQ2
DDRB_SDQ3	B14	MB_DATA3	MA_DATA3	G14 — DDRA_SDQ3
DDRB_SDQ4	G11	MB_DATA4	MA_DATA4	H11 — DDRA_SDQ4
DDRB_SDQ5	E11	MB_DATA5	MA_DATA5	H12 — DDRA_SDQ5
DDRB_SDQ6	D12	MB_DATA6	MA_DATA6	C13 — DDRA_SDQ6
DDRB_SDQ7	A13	MB_DATA7	MA_DATA7	E13 — DDRA_SDQ7
DDRB_SDQ8	A15	MB_DATA8	MA_DATA8	H15 — DDRA_SDQ8
DDRB_SDQ9	A16	MB_DATA9	MA_DATA9	E15 — DDRA_SDQ9
DDRB_SDQ10	A19	MB_DATA10	MA_DATA10	E17 — DDRA_SDQ10
DDRB_SDQ11	A20	MB_DATA11	MA_DATA11	H17 — DDRA_SDQ11
DDRB_SDQ12	C14	MB_DATA12	MA_DATA12	E14 — DDRA_SDQ12
DDRB_SDQ13	D14	MB_DATA13	MA_DATA13	F14 — DDRA_SDQ13
DDRB_SDQ14	C18	MB_DATA14	MA_DATA14	C17 — DDRA_SDQ14
DDRB_SDQ15	D18	MB_DATA15	MA_DATA15	G17 — DDRA_SDQ15
DDRB_SDQ16	D20	MB_DATA16	MA_DATA16	G18 — DDRA_SDQ16
DDRB_SDQ17	A21	MB_DATA17	MA_DATA17	C19 — DDRA_SDQ17
DDRB_SDQ18	D24	MB_DATA18	MA_DATA18	D22 — DDRA_SDQ18
DDRB_SDQ19	C25	MB_DATA19	MA_DATA19	E20 — DDRA_SDQ19
DDRB_SDQ20	B20	MB_DATA20	MA_DATA20	E18 — DDRA_SDQ20
DDRB_SDQ21	C20	MB_DATA21	MA_DATA21	F18 — DDRA_SDQ21
DDRB_SDQ22	B24	MB_DATA22	MA_DATA22	B22 — DDRA_SDQ22
DDRB_SDQ23	C24	MB_DATA23	MA_DATA23	C23 — DDRA_SDQ23
DDRB_SDQ24	E23	MB_DATA24	MA_DATA24	F20 — DDRA_SDQ24
DDRB_SDQ25	E24	MB_DATA25	MA_DATA25	F22 — DDRA_SDQ25
DDRB_SDQ26	G25	MB_DATA26	MA_DATA26	H24 — DDRA_SDQ26
DDRB_SDQ27	G26	MB_DATA27	MA_DATA27	J19 — DDRA_SDQ27
DDRB_SDQ28	C26	MB_DATA28	MA_DATA28	E21 — DDRA_SDQ28
DDRB_SDQ29	D26	MB_DATA29	MA_DATA29	E22 — DDRA_SDQ29
DDRB_SDQ30	G23	MB_DATA30	MA_DATA30	H20 — DDRA_SDQ30
DDRB_SDQ31	G24	MB_DATA31	MA_DATA31	H22 — DDRA_SDQ31
DDRB_SDQ32	AA24	MB_DATA32	MA_DATA32	Y24 — DDRA_SDQ32
DDRB_SDQ33	AA23	MB_DATA33	MA_DATA33	AB24 — DDRA_SDQ33
DDRB_SDQ34	AD24	MB_DATA34	MA_DATA34	AB22 — DDRA_SDQ34
DDRB_SDQ35	AE24	MB_DATA35	MA_DATA35	AA21 — DDRA_SDQ35
DDRB_SDQ36	AA26	MB_DATA36	MA_DATA36	W22 — DDRA_SDQ36
DDRB_SDQ37	AA25	MB_DATA37	MA_DATA37	W21 — DDRA_SDQ37
DDRB_SDQ38	AD26	MB_DATA38	MA_DATA38	Y22 — DDRA_SDQ38
DDRB_SDQ39	AE25	MB_DATA39	MA_DATA39	AA22 — DDRA_SDQ39
DDRB_SDQ40	AC22	MB_DATA40	MA_DATA40	Y20 — DDRA_SDQ40
DDRB_SDQ41	AD22	MB_DATA41	MA_DATA41	AA20 — DDRA_SDQ41
DDRB_SDQ42	AE20	MB_DATA42	MA_DATA42	AA18 — DDRA_SDQ42
DDRB_SDQ43	AF20	MB_DATA43	MA_DATA43	AB18 — DDRA_SDQ43
DDRB_SDQ44	AF24	MB_DATA44	MA_DATA44	AB21 — DDRA_SDQ44
DDRB_SDQ45	AF23	MB_DATA45	MA_DATA45	AD21 — DDRA_SDQ45
DDRB_SDQ46	AC20	MB_DATA46	MA_DATA46	AD19 — DDRA_SDQ46
DDRB_SDQ47	AD20	MB_DATA47	MA_DATA47	Y18 — DDRA_SDQ47
DDRB_SDQ48	AD18	MB_DATA48	MA_DATA48	AD17 — DDRA_SDQ48
DDRB_SDQ49	AE18	MB_DATA49	MA_DATA49	W16 — DDRA_SDQ49
DDRB_SDQ50	AC14	MB_DATA50	MA_DATA50	W14 — DDRA_SDQ50
DDRB_SDQ51	AD14	MB_DATA51	MA_DATA51	Y14 — DDRA_SDQ51
DDRB_SDQ52	AF19	MB_DATA52	MA_DATA52	Y17 — DDRA_SDQ52
DDRB_SDQ53	AC18	MB_DATA53	MA_DATA53	AB17 — DDRA_SDQ53
DDRB_SDQ54	AF16	MB_DATA54	MA_DATA54	AB15 — DDRA_SDQ54
DDRB_SDQ55	AF15	MB_DATA55	MA_DATA55	AD15 — DDRA_SDQ55
DDRB_SDQ56	AF13	MB_DATA56	MA_DATA56	AB13 — DDRA_SDQ56
DDRB_SDQ57	AC12	MB_DATA57	MA_DATA57	AD13 — DDRA_SDQ57
DDRB_SDQ58	AB11	MB_DATA58	MA_DATA58	Y12 — DDRA_SDQ58
DDRB_SDQ59	Y11	MB_DATA59	MA_DATA59	W11 — DDRA_SDQ59
DDRB_SDQ60	AE14	MB_DATA60	MA_DATA60	AB14 — DDRA_SDQ60
DDRB_SDQ61	AF14	MB_DATA61	MA_DATA61	AA14 — DDRA_SDQ61
DDRB_SDQ62	AF11	MB_DATA62	MA_DATA62	AB12 — DDRA_SDQ62
DDRB_SDQ63	AD11	MB_DATA63	MA_DATA63	AA12 — DDRA_SDQ63

DDRA_SDQ[63..0] (8)

(9) DDRB_SDM[7..0]

DDRB_SDM0	A12	MB_DM0	MA_DM0	E12 — DDRA_SDM0
DDRB_SDM1	B16	MB_DM1	MA_DM1	C15 — DDRA_SDM1
DDRB_SDM2	A22	MB_DM2	MA_DM2	E19 — DDRA_SDM2
DDRB_SDM3	E25	MB_DM3	MA_DM3	F24 — DDRA_SDM3
DDRB_SDM4	AB26	MB_DM4	MA_DM4	AC24 — DDRA_SDM4
DDRB_SDM5	AE22	MB_DM5	MA_DM5	Y19 — DDRA_SDM5
DDRB_SDM6	AC16	MB_DM6	MA_DM6	AB16 — DDRA_SDM6
DDRB_SDM7	AD12	MB_DM7	MA_DM7	Y13 — DDRA_SDM7

DDRA_SDM[7..0] (8)

(9) DDRB_SDQS0	DDRB_SDQS0	C12	MB_DQS_H0	MA_DQS_H0 — G13 — DDRA_SDQS0 (8)
(9) DDRB_SDQS0#	DDRB_SDQS0#	B12	MB_DQS_L0	MA_DQS_L0 — H13 — DDRA_SDQS0# (8)
(9) DDRB_SDQS1	DDRB_SDQS1	D16	MB_DQS_H1	MA_DQS_H1 — G16 — DDRA_SDQS1 (8)
(9) DDRB_SDQS1#	DDRB_SDQS1#	C16	MB_DQS_L1	MA_DQS_L1 — G15 — DDRA_SDQS1# (8)
(9) DDRB_SDQS2	DDRB_SDQS2	A24	MB_DQS_H2	MA_DQS_H2 — C22 — DDRA_SDQS2 (8)
(9) DDRB_SDQS2#	DDRB_SDQS2#	A23	MB_DQS_L2	MA_DQS_L2 — C21 — DDRA_SDQS2# (8)
(9) DDRB_SDQS3	DDRB_SDQS3	F26	MB_DQS_H3	MA_DQS_H3 — G22 — DDRA_SDQS3 (8)
(9) DDRB_SDQS3#	DDRB_SDQS3#	F26	MB_DQS_L3	MA_DQS_L3 — G21 — DDRA_SDQS3# (8)
(9) DDRB_SDQS4	DDRB_SDQS4	AC25	MB_DQS_H4	MA_DQS_H4 — AD23 — DDRA_SDQS4 (8)
(9) DDRB_SDQS4#	DDRB_SDQS4#	AC26	MB_DQS_L4	MA_DQS_L4 — AC23 — DDRA_SDQS4# (8)
(9) DDRB_SDQS5	DDRB_SDQS5	AF21	MB_DQS_H5	MA_DQS_H5 — AB19 — DDRA_SDQS5 (8)
(9) DDRB_SDQS5#	DDRB_SDQS5#	AF22	MB_DQS_L5	MA_DQS_L5 — AB20 — DDRA_SDQS5# (8)
(9) DDRB_SDQS6	DDRB_SDQS6	AE16	MB_DQS_H6	MA_DQS_H6 — Y15 — DDRA_SDQS6 (8)
(9) DDRB_SDQS6#	DDRB_SDQS6#	AD16	MB_DQS_L6	MA_DQS_L6 — W15 — DDRA_SDQS6# (8)
(9) DDRB_SDQS7	DDRB_SDQS7	AF12	MB_DQS_H7	MA_DQS_H7 — W12 — DDRA_SDQS7 (8)
(9) DDRB_SDQS7#	DDRB_SDQS7#	AE12	MB_DQS_L7	MA_DQS_L7 — W13 — DDRA_SDQS7# (8)

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ME@

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Title: AMD CPU S1G3 DDRII I/F

Size	Document Number	Rev
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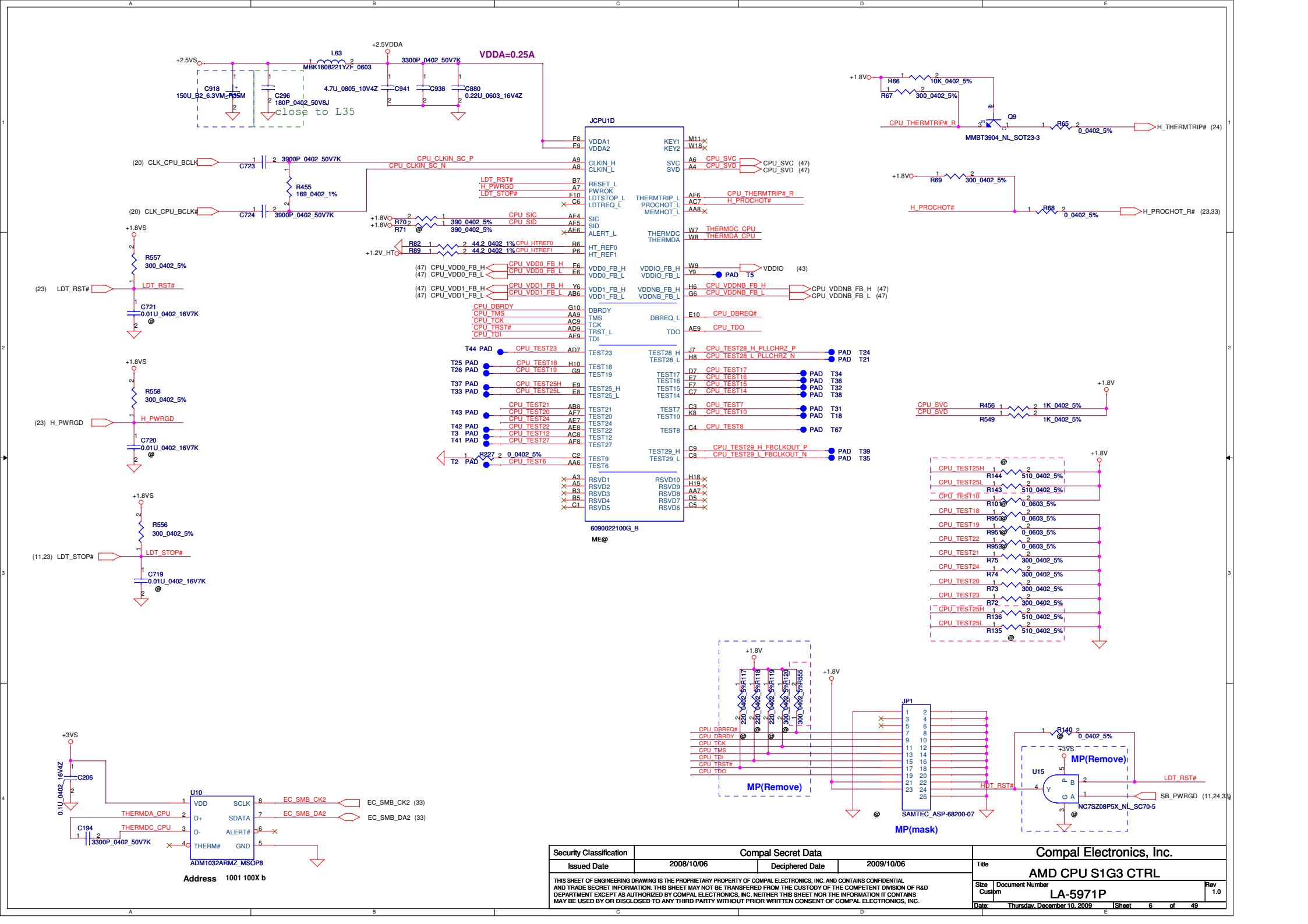

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Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: AMD CPU S1G3 CTRL

Size	Document Number	Rev
Custom	LA-5971P	1.0

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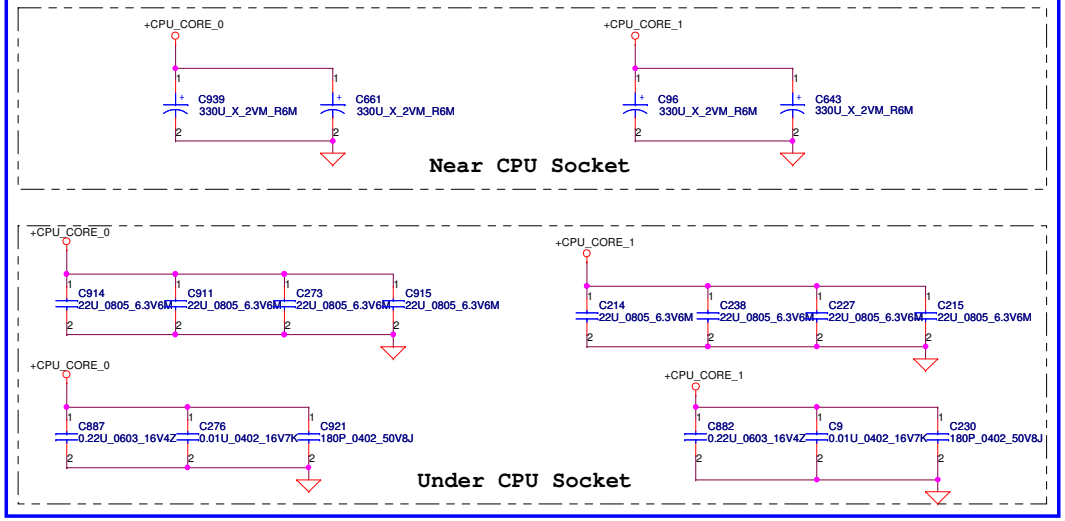
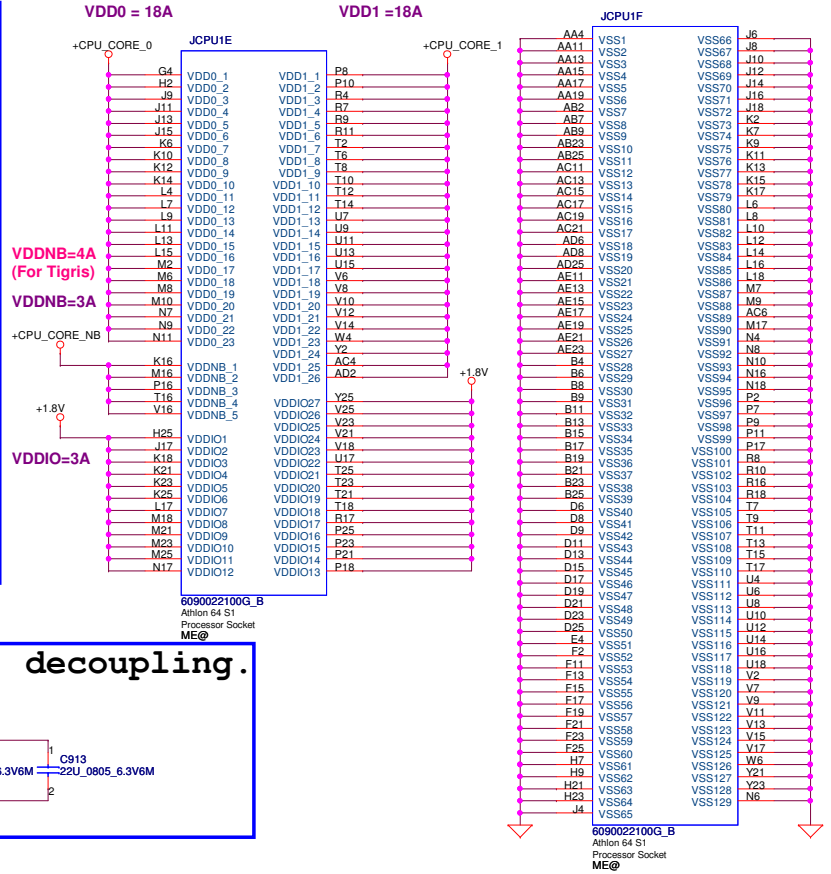
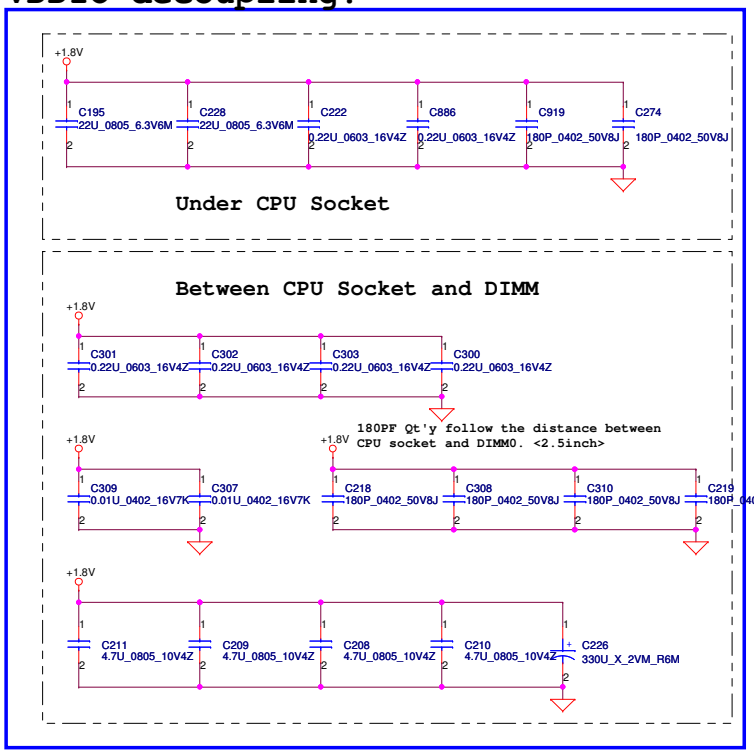
VDD (+CPU_CORE) decoupling.

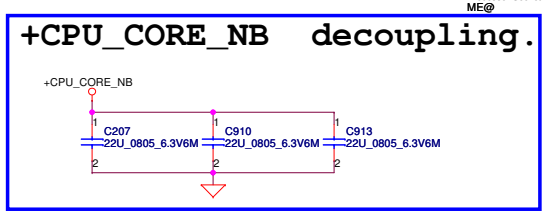




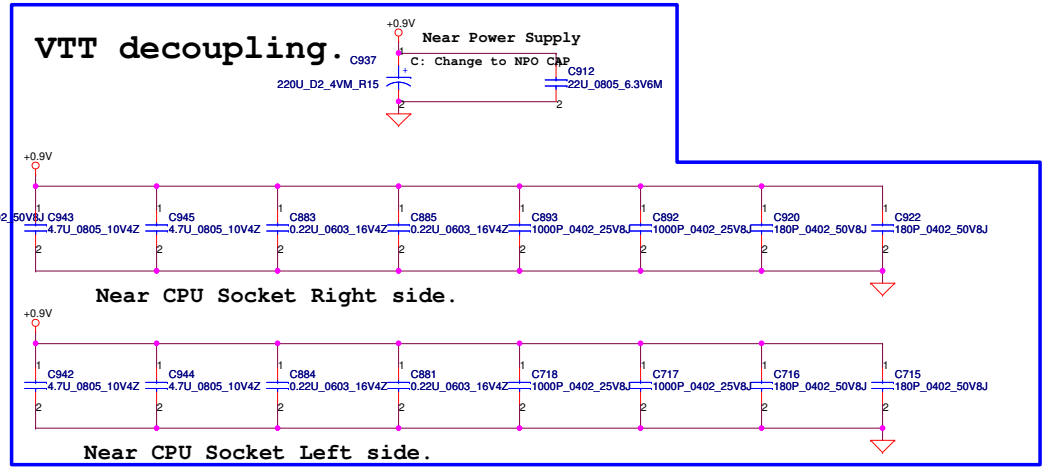
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



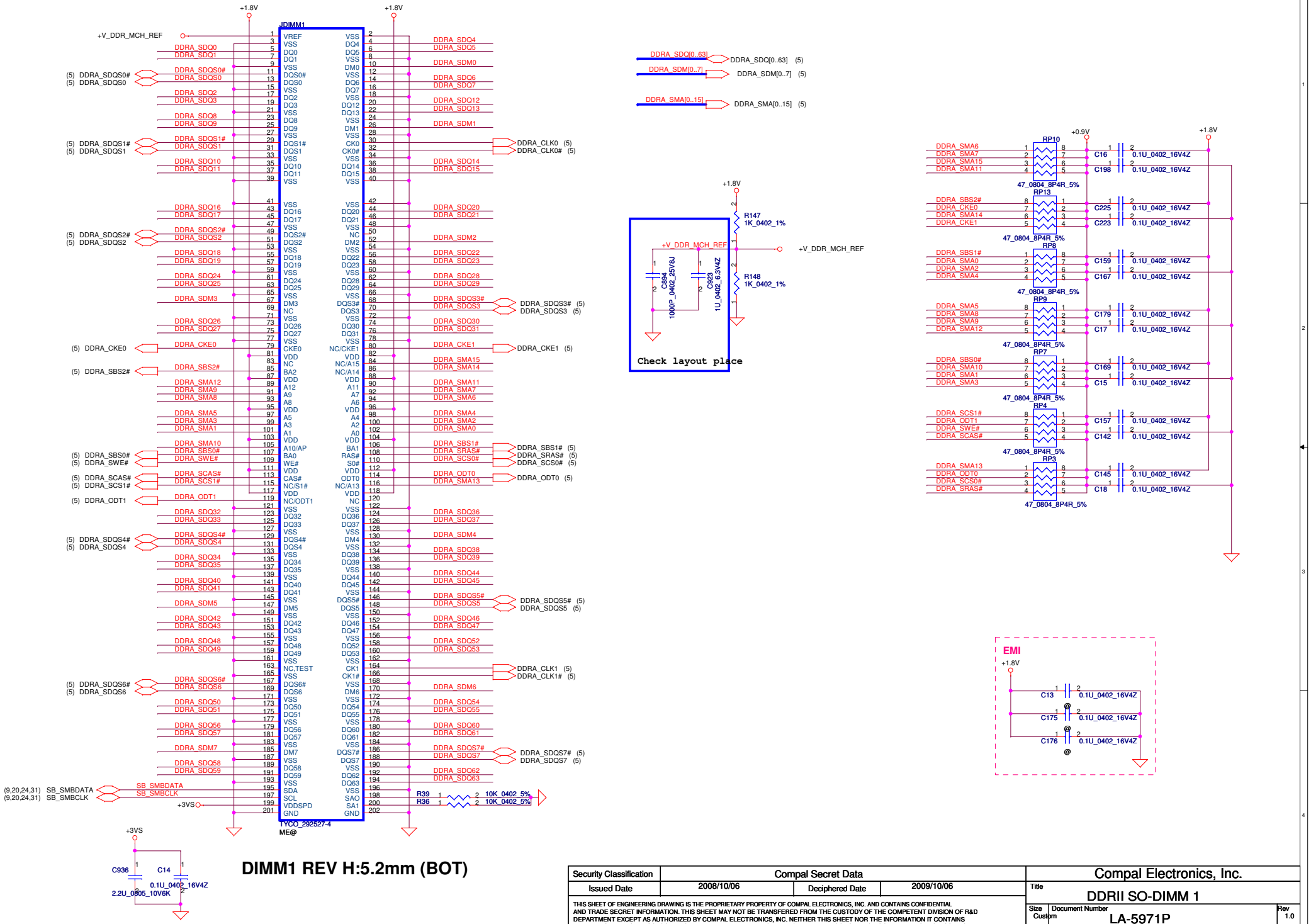
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: AMD CPU S1G3 PWR & GND

Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 7 of 49



DIMM1 REV H:5.2mm (BOT)

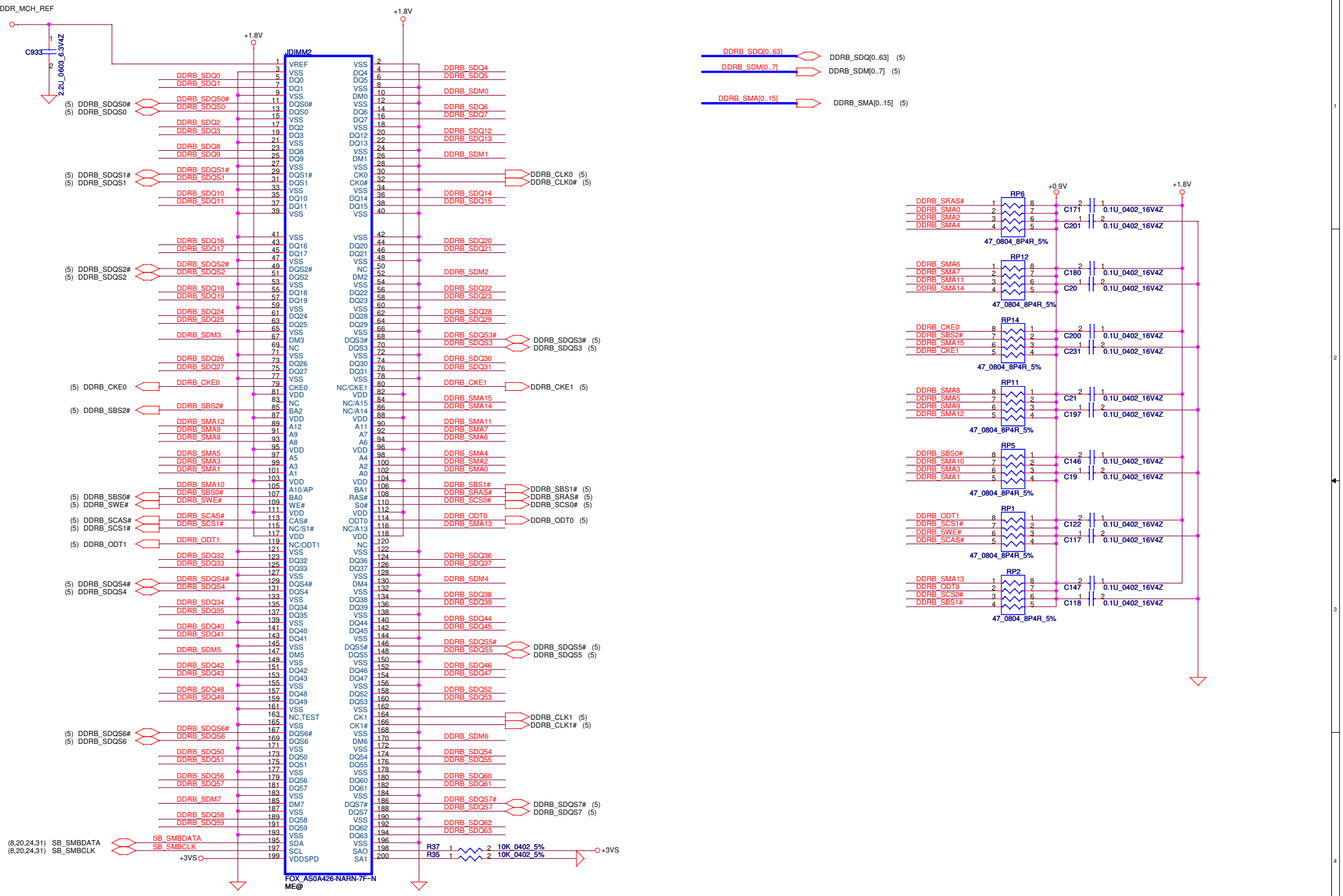
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: DDRII SO-DIMM 1

Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 8 of 49



DIMM2 REV H:9.2mm (BOT)

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: DDRII SO-DIMM 2

Size	Document Number	Rev
Custom	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 9 of 49

(14) PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]
(14) PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] (14)
PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] (14)

U20B

PART 2 OF 6

PCIE I/F GFX

PCIE_GTX_C_MRX_P0	D4	GFX_RX0P	GFX_TX0P	A5	PCIE_MTX_GRX_P0		C358 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P0
PCIE_GTX_C_MRX_N0	C4	GFX_RX0N	GFX_TX0N	B5	PCIE_MTX_GRX_N0	C646 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N0
PCIE_GTX_C_MRX_P1	A3	GFX_RX1P	GFX_TX1P	A4	PCIE_MTX_GRX_P1		C649 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P1
PCIE_GTX_C_MRX_N1	B3	GFX_RX1N	GFX_TX1N	B4	PCIE_MTX_GRX_N1	C648 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N1
PCIE_GTX_C_MRX_P2	C2	GFX_RX2P	GFX_TX2P	C3	PCIE_MTX_GRX_P2		C651 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P2
PCIE_GTX_C_MRX_N2	C1	GFX_RX2N	GFX_TX2N	B2	PCIE_MTX_GRX_N2	C650 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N2
PCIE_GTX_C_MRX_P3	E5	GFX_RX3P	GFX_TX3P	D1	PCIE_MTX_GRX_P3		C653 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P3
PCIE_GTX_C_MRX_N3	F5	GFX_RX3N	GFX_TX3N	D2	PCIE_MTX_GRX_N3	C652 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N3
PCIE_GTX_C_MRX_P4	G5	GFX_RX4P	GFX_TX4P	E2	PCIE_MTX_GRX_P4		C366 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P4
PCIE_GTX_C_MRX_N4	G6	GFX_RX4N	GFX_TX4N	E1	PCIE_MTX_GRX_N4	C356 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N4
PCIE_GTX_C_MRX_P5	H5	GFX_RX5P	GFX_TX5P	F4	PCIE_MTX_GRX_P5		C876 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P5
PCIE_GTX_C_MRX_N5	H6	GFX_RX5N	GFX_TX5N	F3	PCIE_MTX_GRX_N5	C657 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N5
PCIE_GTX_C_MRX_P6	J6	GFX_RX6P	GFX_TX6P	F1	PCIE_MTX_GRX_P6		C658 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P6
PCIE_GTX_C_MRX_N6	J5	GFX_RX6N	GFX_TX6N	F2	PCIE_MTX_GRX_N6	C365 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N6
PCIE_GTX_C_MRX_P7	J7	GFX_RX7P	GFX_TX7P	H4	PCIE_MTX_GRX_P7		C364 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P7
PCIE_GTX_C_MRX_N7	J8	GFX_RX7N	GFX_TX7N	H3	PCIE_MTX_GRX_N7	C641 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N7
PCIE_GTX_C_MRX_P8	L5	GFX_RX8P	GFX_TX8P	H1	PCIE_MTX_GRX_P8		C638 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P8
PCIE_GTX_C_MRX_N8	L6	GFX_RX8N	GFX_TX8N	H2	PCIE_MTX_GRX_N8	C636 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N8
PCIE_GTX_C_MRX_P9	M8	GFX_RX9P	GFX_TX9P	J2	PCIE_MTX_GRX_P9		C637 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P9
PCIE_GTX_C_MRX_N9	L8	GFX_RX9N	GFX_TX9N	J1	PCIE_MTX_GRX_N9	C635 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N9
PCIE_GTX_C_MRX_P10	P7	GFX_RX10P	GFX_TX10P	K4	PCIE_MTX_GRX_P10		C634 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P10
PCIE_GTX_C_MRX_N10	M7	GFX_RX10N	GFX_TX10N	K3	PCIE_MTX_GRX_N10	C632 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N10
PCIE_GTX_C_MRX_P11	P5	GFX_RX11P	GFX_TX11P	K1	PCIE_MTX_GRX_P11		C631 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P11
PCIE_GTX_C_MRX_N11	M5	GFX_RX11N	GFX_TX11N	K2	PCIE_MTX_GRX_N11	C360 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N11
PCIE_GTX_C_MRX_P12	R8	GFX_RX12P	GFX_TX12P	M4	PCIE_MTX_GRX_P12		C629 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P12
PCIE_GTX_C_MRX_N12	P8	GFX_RX12N	GFX_TX12N	M3	PCIE_MTX_GRX_N12	C627 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N12
PCIE_GTX_C_MRX_P13	R6	GFX_RX13P	GFX_TX13P	M1	PCIE_MTX_GRX_P13		C363 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P13
PCIE_GTX_C_MRX_N13	R5	GFX_RX13N	GFX_TX13N	M2	PCIE_MTX_GRX_N13	C623 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N13
PCIE_GTX_C_MRX_P14	P4	GFX_RX14P	GFX_TX14P	N2	PCIE_MTX_GRX_P14		C359 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P14
PCIE_GTX_C_MRX_N14	P3	GFX_RX14N	GFX_TX14N	N1	PCIE_MTX_GRX_N14	C624 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N14
PCIE_GTX_C_MRX_P15	T4	GFX_RX15P	GFX_TX15P	P1	PCIE_MTX_GRX_P15		C621 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P15
PCIE_GTX_C_MRX_N15	T3	GFX_RX15N	GFX_TX15N	P2	PCIE_MTX_GRX_N15	C361 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N15

PCIE I/F GPP

WLAN@ WLAN@

AE3	GPP_RX0P	GPP_TX0P	AC1			
AD4	GPP_RX0N	GPP_TX0N	AC2			
(31) PCIE_PTX_C_IRX_P1 AE2	GPP_RX1P	GPP_TX1P	AB4	PCIE_ITX_PRX_P1	C614 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_P1 (31)
(31) PCIE_PTX_C_IRX_N1 AD3	GPP_RX1N	GPP_TX1N	AB3	PCIE_ITX_PRX_N1	C362 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_N1 (31)
(30) PCIE_PTX_C_IRX_P2 AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_ITX_PRX_P2	C357 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_P2 (30)
(30) PCIE_PTX_C_IRX_N2 AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_ITX_PRX_N2	C618 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_N2 (30)
V5	GPP_RX3P	GPP_TX3P	Y1			
W6	GPP_RX3N	GPP_TX3N	Y2			
(31) PCIE_PTX_C_IRX_P4 U5	GPP_RX4P	GPP_TX4P	Y4	PCIE_ITX_PRX_P4	C964 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_P4 (31)
(31) PCIE_PTX_C_IRX_N4 U6	GPP_RX4N	GPP_TX4N	Y3	PCIE_ITX_PRX_N4	C965 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_N4 (31)
U8	GPP_RX5P	GPP_TX5P	V1		NEWCARD@	
U7	GPP_RX5N	GPP_TX5N	V2		NEWCARD@	

WLAN
LAN

New Card
(4) H_CADOP[0..15] → H_CADOP[0..15] → H_CADIP[0..15] → H_CADIP[0..15] (4)
(4) H_CADON[0..15] → H_CADON[0..15] → H_CADIN[0..15] → H_CADIN[0..15] (4)

PCIE I/F SB

(23) SB_RX0P AA8	SB_RX0P	SB_TX0P	AD7	SB_TX0P_C	C352 1 2	0.1U 0402 10V7K SB_TX0P (23)
(23) SB_RX0N Y8	SB_RX0N	SB_TX0N	AE7	SB_TX0N_C	C609 1 2	0.1U 0402 10V7K SB_TX0N (23)
(23) SB_RX1P AA7	SB_RX1P	SB_TX1P	AE6	SB_TX1P_C	C38 1 2	0.1U 0402 10V7K SB_TX1P (23)
(23) SB_RX1N Y7	SB_RX1N	SB_TX1N	AD6	SB_TX1N_C	C33 1 2	0.1U 0402 10V7K SB_TX1N (23)
(23) SB_RX2P AA5	SB_RX2P	SB_TX2P	AB6	SB_TX2P_C	C37 1 2	0.1U 0402 10V7K SB_TX2P (23)
(23) SB_RX2N AA6	SB_RX2N	SB_TX2N	AC6	SB_TX2N_C	C32 1 2	0.1U 0402 10V7K SB_TX2N (23)
(23) SB_RX3P W5	SB_RX3P	SB_TX3P	AD5	SB_TX3P_C	C610 1 2	0.1U 0402 10V7K SB_TX3P (23)
(23) SB_RX3N Y5	SB_RX3N	SB_TX3N	AE5	SB_TX3N_C	C616 1 2	0.1U 0402 10V7K SB_TX3N (23)

	PCE_CALRP(PCE_BCALRP)	AC8	R32 1 2	1.27K 0402 1%	
	PCE_CALRN(PCE_BCALRN)	AB8	R267 1 2	2K 0402 1%	+1.1VS

RS880M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

U20A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

H_CADOP0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	H_CADIP0
H_CADON0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	H_CADIN0
H_CADOP1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	H_CADIP1
H_CADON1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	H_CADIN1
H_CADOP2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	H_CADIP2
H_CADON2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	H_CADIN2
H_CADOP3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	H_CADIP3
H_CADON3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	H_CADIN3
H_CADOP4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	H_CADIP4
H_CADON4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	H_CADIN4
H_CADOP5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	H_CADIP5
H_CADON5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	H_CADIN5
H_CADOP6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	H_CADIP6
H_CADON6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	H_CADIN6
H_CADOP7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	H_CADIP7
H_CADON7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	H_CADIN7
H_CADOP8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	H_CADIP8
H_CADON8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	H_CADIN8
H_CADOP9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	H_CADIP9
H_CADON9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	H_CADIN9
H_CADOP10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	H_CADIP10
H_CADON10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	H_CADIN10
H_CADOP11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	H_CADIP11
H_CADON11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	H_CADIN11
H_CADOP12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	H_CADIP12
H_CADON12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	H_CADIN12
H_CADOP13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	H_CADIP13
H_CADON13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	H_CADIN13
H_CADOP14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	H_CADIP14
H_CADON14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	H_CADIN14
H_CADOP15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	H_CADIP15
H_CADON15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	H_CADIN15

(4) H_CLKOP0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	H_CLKIP0 (4)
(4) H_CLKON0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	H_CLKIN0 (4)
(4) H_CLKOP1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	H_CLKIP1 (4)
(4) H_CLKON1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	H_CLKIN1 (4)
(4) H_CTLOP0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	H_CTLIP0 (4)
(4) H_CTLON0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	H_CTLIN0 (4)
(4) H_CTLOP1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	H_CTLIP1 (4)
(4) H_CTLON1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	H_CTLIN1 (4)
	C23	HT_RXCALP	HT_TXCALP	B24	R51 1 2 301_0402_1%
	A24	HT_RXCALN	HT_TXCALN	B25	

R56 1 2 301_0402_1%
0718 Place within 1" layout 1:2

RS880M_FCBGA528

0718 Place within 1" layout 1:2

SA00002DR30 S IC 216-0674026 A13 RS780MN FCBGA 0FA
SA000032710 S IC 216-0752001 A11 RS880M FCBGA528 0FA

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

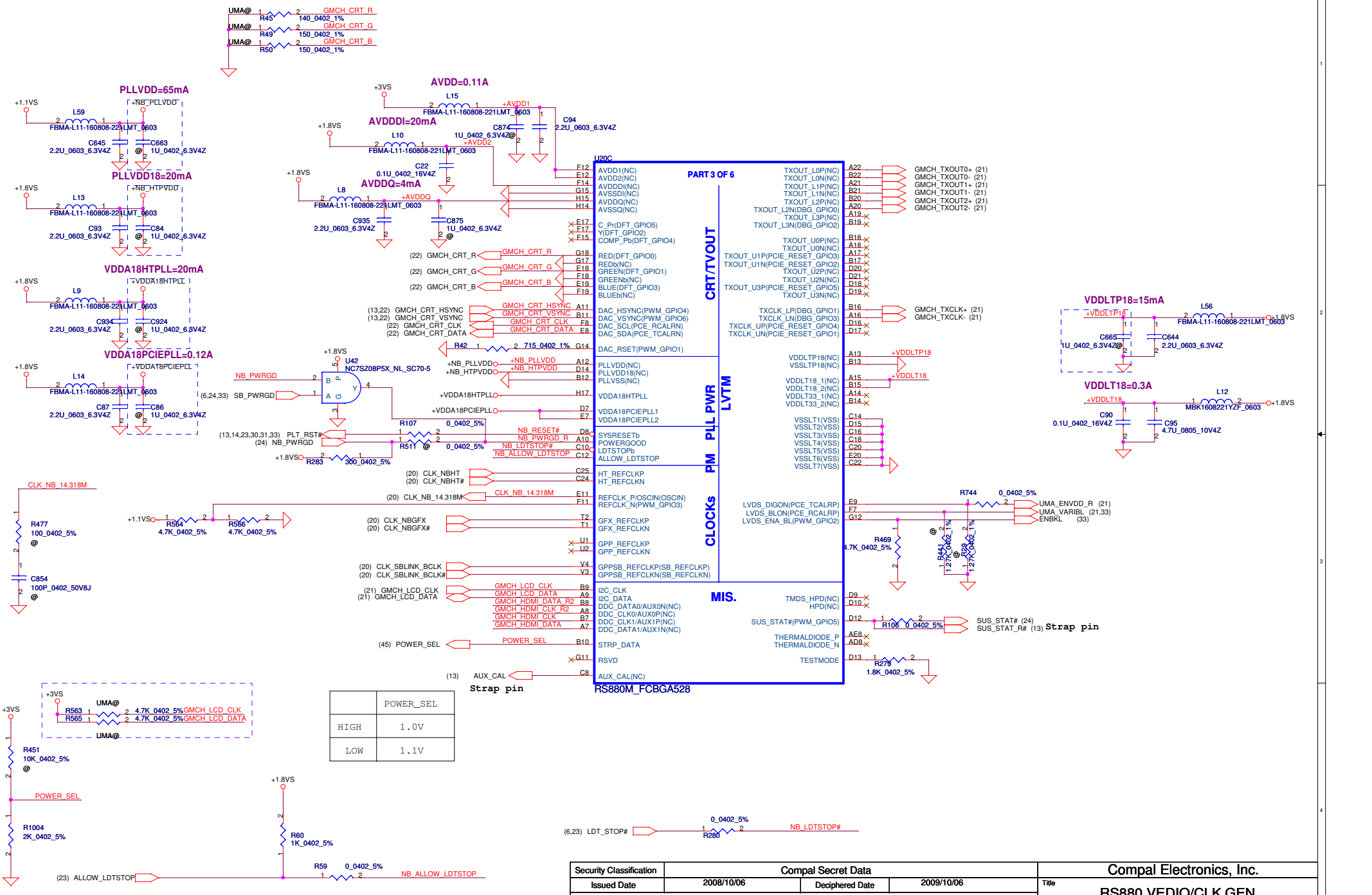
Compal Electronics, Inc.

Title: RS880-HT/PCIE

Size	Document Number	Rev
Custom	LA-5971P	1.0

Date: Thursday, December 10, 2009 Sheet 10 of 49

For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor



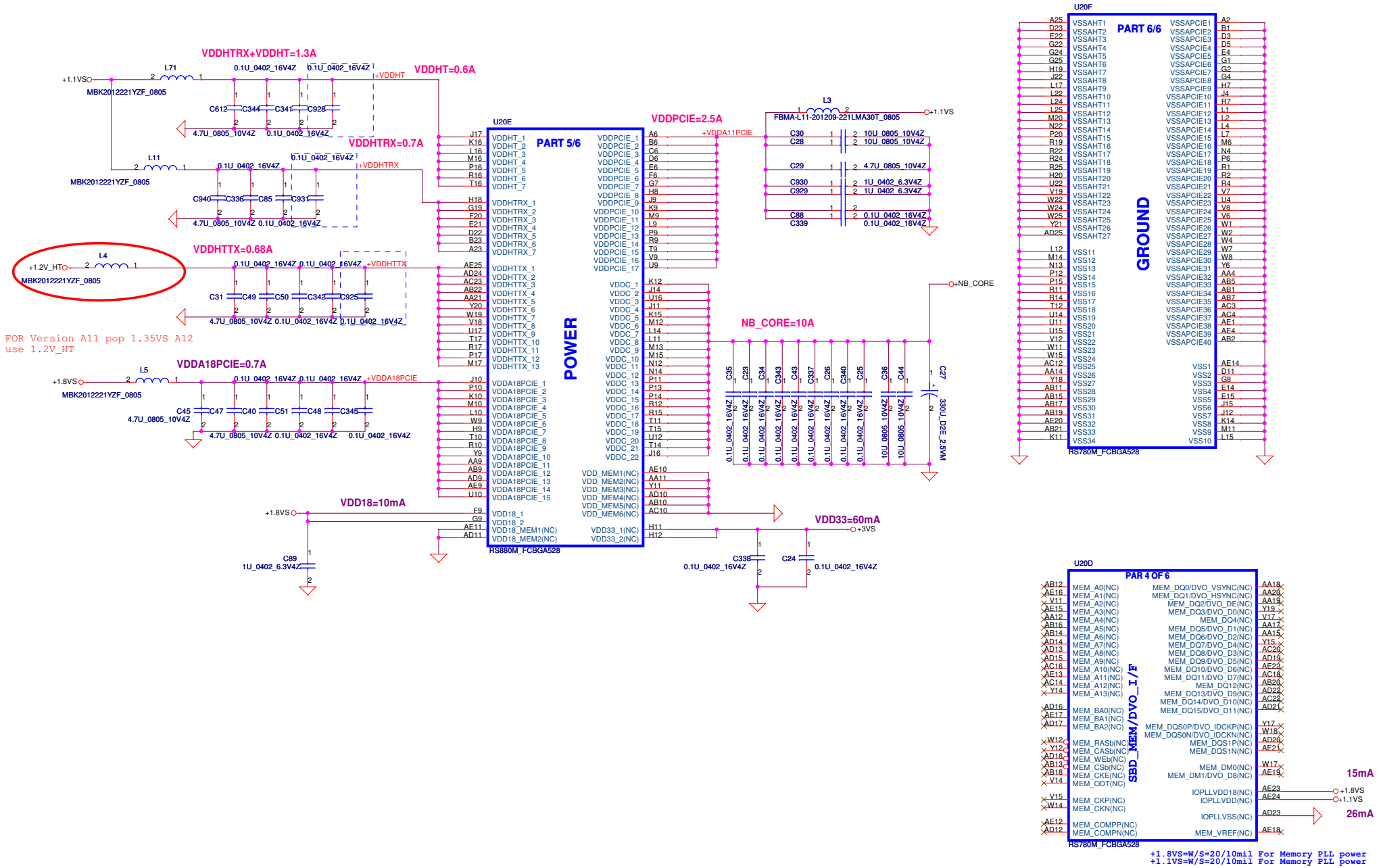
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: RS880 VEDIO/CLK GEN

Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 11 of 49



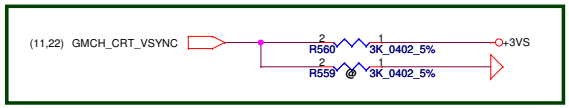
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: RS880 PWR/GND

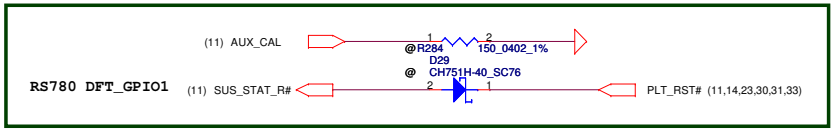
Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 12 of 49



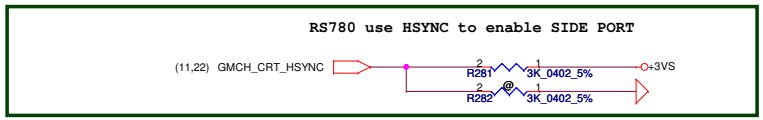
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS880m)
0 : Enable (RS880M)
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```



RS780 use HSYNC to enable SIDE PORT

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.   Enable (RS880M)
1 :  Disable(RS880M)
```

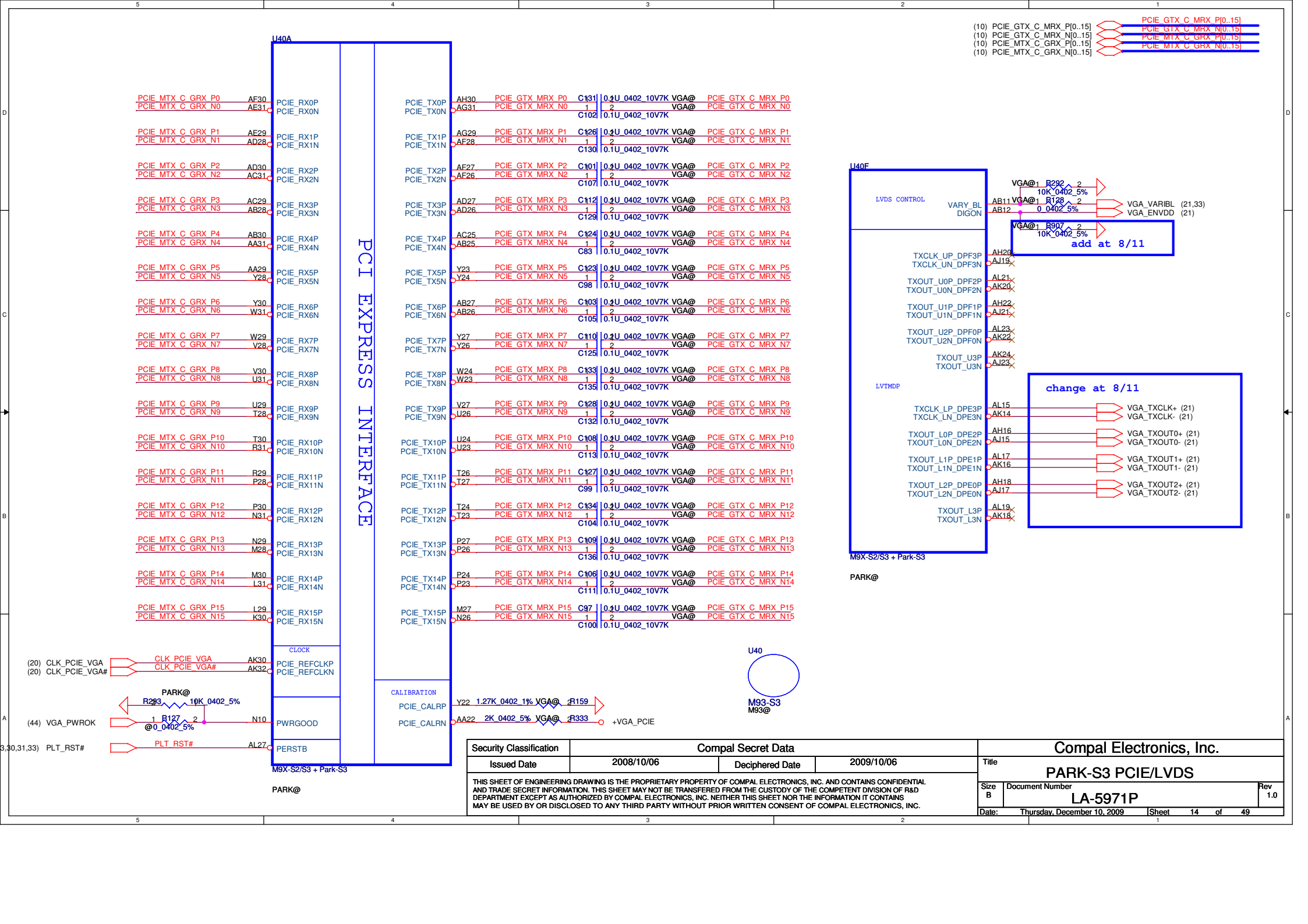
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: RS880 STRAPS

Size	Document Number	Rev
Custom	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 13 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 PCIE/LVDS

Size	Document Number	Rev
B	LA-5971P	1.0

Date: Thursday, December 10, 2009 Sheet 14 of 49

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
	GPIO8		0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

STRAPS

GPU_GPIO0 R232 @ 10K_0402_5%
GPU_GPIO1 @R228 10K_0402_5%
GPU_GPIO2 @R215 10K_0402_5%
GPU_GPIO8 @R233 10K_0402_5%
GPU_GPIO9 @R231 10K_0402_5%
GPIO21_BBEN @R216 10K_0402_5%
GPU_GPIO11 R217 @ 10K_0402_5%
GPU_GPIO12 @R236 10K_0402_5%
GPU_GPIO13 @R234 10K_0402_5%
VGA_CRT_HSYNC @R229 10K_0402_5%
VGA_CRT_VSYNC @R230 10K_0402_5%
VGA_CRT_VSYNC2 @R235 10K_0402_5%
VGA_CRT_HSYNC2 @R108 10K_0402_5%
GPU_GPIO8 R1014 @ 10K_0402_5%

VGA Thermal Sensor G781-1P8F

Closed to GPU

U26 G780P81U_MSOP8
VDD1 SCLK VGA_SMB_CK2_R
D+ SDATA VGA_SMB_DA2_R
D- ALERT#
THERM# GND THM_ALERT#
GPU_THERMAL_D+ C708VGA@ 2200P_0402_50V7K GPU_THERMAL_D-
C137 0.1U_0402_16V4Z VGA@
4.7K_0402_5% R340 +3VS_VGA

add at 8/11
+VGA_PCIE L101 BLM15BD121SN1D_0402 +DPLL_VDDC
C1015 10U_0603_6.3V6M C1014 1U_0402_6.3V4Z C1013 0.1U_0402_10V6K

EMI request add at 8/17
CLK_XTALIN R972 1M_0402_5% CLK_XTALOUT
Y6 27MHZ_20P_7A27000010
C1021 22P_0402_50V8J C1022 22P_0402_50V8J

U40B
M93-S3/M92-S2
DVCNTL_0/ DVPDATA_18
DVCNTL_1 / NC
DVCNTL_2 / TESTEN#2
DVDATA_12 / DVPDATA_16
DVDATA_11 / DVPDATA_20
DVDATA_10 / DVPDATA_22
DVDATA_9 / DVPDATA_12
DVDATA_8 / DVPDATA_14
DVDATA_7 / DVPCNTL_0
DVDATA_6 / DVPDATA_8
DVDATA_5 / DVPDATA_6
DVDATA_4 DVPDATA_4
DVDATA_3 / DVPDATA_19
DVDATA_2 / DVPDATA_21
DVDATA_1 / DVPDATA_2
DVDATA_0 / DVPDATA_0
DVO
DPA: TXCAP_DPA3P TXCAM_DPA3N; TX0P_DPA2P TX0M_DPA2N; TX1P_DPA1P TX1M_DPA1N; TX2P_DPA0P TX2M_DPA0N
DPB: TXCBP_DPB3P TXCBM_DPB3N; TX3P_DPB2P TX3M_DPB2N; TX4P_DPB1P TX4M_DPB1N; TX5P_DPB0P TX5M_DPB0N
M93-S3/M92-S2
DPC_PVDD / DVPDATA_11
DPC_PVSS / GND
DPC_VDD18#1/DVPDAT10
DPC_VDD18#2/DVPDAT23
DPC_VDD10#1/DVPDAT15
DPC_VDD10#2/DVPDAT17
DPC_VSSR#1 / DVPCLK
DPC_VSSR#2 / DVPDAT5
DPC_VSSR#3 / GND
DPC_VSSR#4 / GND
DPC_VSSR#5/ DVPCNTL_MV0
M92-S2/M93-S3
DVPDATA_3/TXCCP_DPC3P
DVPCNTL_2/TXCCM_DPC3N
DVPDATA_7 / TX0P_DPC2P
DVPDATA_1 / TX0M_DPC2N
DVPCNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPCNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR
DPC
R310 150_0402_1% VGA@
I2C: SCL SDA
GENERAL PURPOSE I/O
GPIO_0 GPIO_1 GPIO_2 GPIO_3_SMBDATA GPIO_4_SMBCLK GPIO_5_AC_BATT GPIO_6 GPIO_7_BLON GPIO_8_ROMSO GPIO_9_ROMSI GPIO_10_ROMSCK GPIO_11 GPIO_12 GPIO_13 GPIO_14_HPD2 GPIO_15_PWRCNTL_0 GPIO_16_SSIN GPIO_17_THERMAL_INT GPIO_18_HPD3 GPIO_19_CTF GPIO_20_PWRCNTL_1 GPIO_21_BB_EN GPIO_22_ROMCSB GPIO_23_CLKREQB
JTAG_TRSTB JTAG_TDI JTAG_TCK JTAG_TMS JTAG_TDO TESTEN
GENERICA GENERICB GENERICC GENERICD GENERICE_HPD4
HPD1
VREFG
M92-S2/M93-S3
PLL/CLOCK
DPLL_PVDD DPLL_PVSS DPLL_VDDC XTALIN XTALOUT NC#2/XO_IN NC#1/XO_IN2
THERMAL
DPLUS DMINUS TS_FDO TSVDD TSVSS
M9X-S2/S3 + Park-S3
PARK@
DAC1: R/RB G/GB B/BB HSYNC VSYNC RSET AVDD AVSSQ VDD1DI VSS1DI
DAC2: R2 / NC R2B / NC G2 / NC G2B / NC B2 / NC B2B / NC C / NC Y / NC COMP / NC H2SYNC V2SYNC VDD2DI / NC VSS2DI / NC A2VDD / NC A2VDDQ / NC A2VSSQ R2SET / NC
M92-S2/M93-S3
DDC1CLK DDC1DATA AUX1P AUX1N DDC/AUX
DDC2CLK DDC2DATA AUX2P AUX2N
DDCCLK_AUX5P DDCDATA_AUX5N DDC6CLK DDC6DATA NC/DDCCLK_AUX3P NC/DDCDATA_AUX3N
M92-S2/M93-S3

VGA_CRT_R (22) VGA_CRT_G (22) VGA_CRT_B (22) VGA_CRT_HSYNC (22) VGA_CRT_VSYNC (22) VGA_CRT_CLK (22) VGA_CRT_DATA (22)
R482 499_0402_1% VGA@ 70mA +AVDD
45mA +VDD1DI
50mA +VDD2DI
130mA +A2VDD
1.5mA +A2VDDQ
120mA +DPLL_PVDD
300mA +DPLL_VDDC
R481 499_0402_1% VGA@ +VREFG_GPU
R908 715_0402_1%

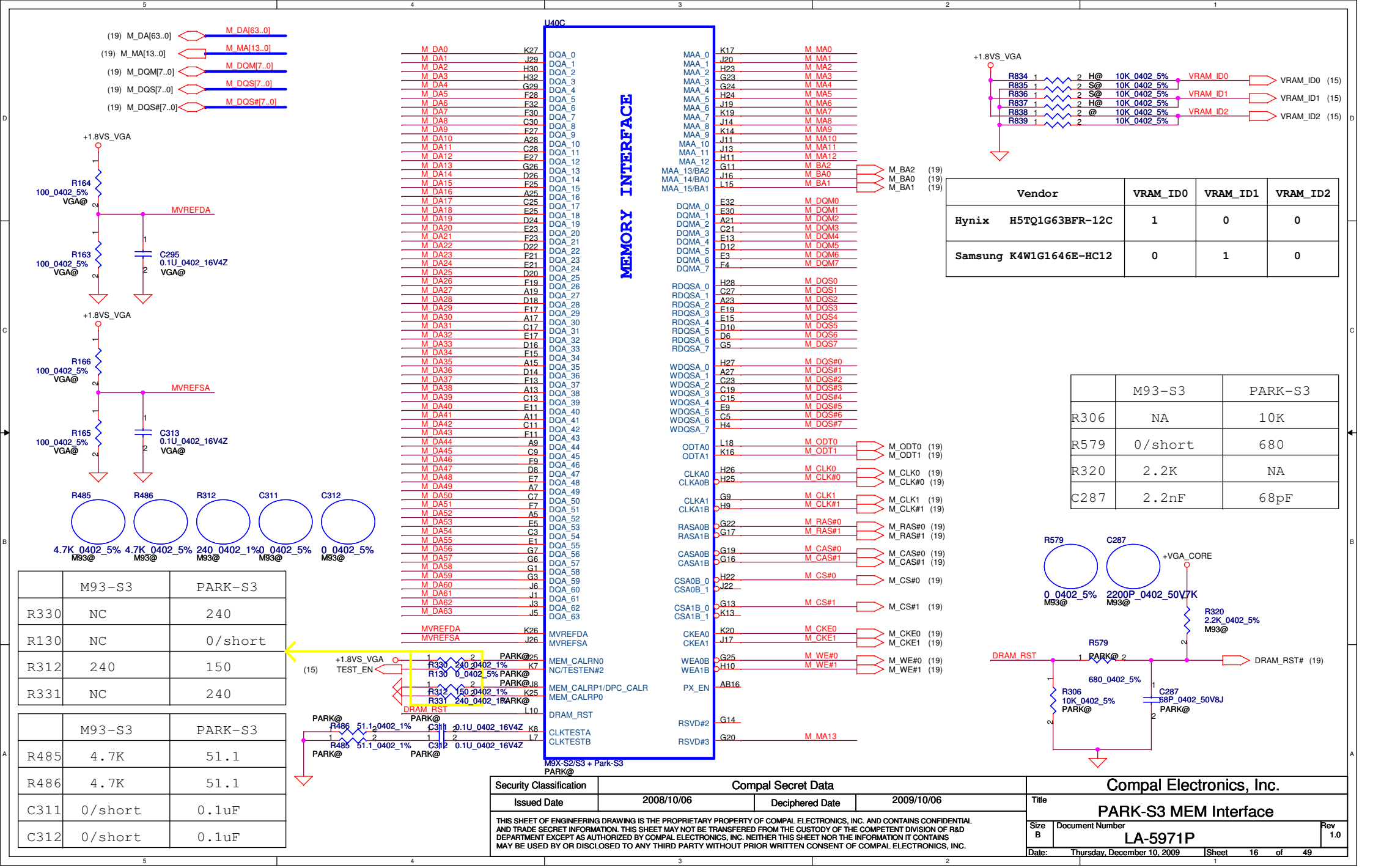
L96 L97 L99 L98 L100 BLM15BD121SN1D_0402 PARK@
C1001 10U_0603_6.3V6M C999 1U_0402_6.3V4Z C998 0.1U_0402_10V6K
C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1002 C1003
+1.8VS_VGA +3VS_VGA +AVDD +VDD1DI +VDD2DI +A2VDD +A2VDDQ
add at 8/11

R303 R297 R287 R302 R305 R294 R299 R298 R483 @10K_0402_5% GPU_GPIO3 GPU_GPIO4 VGA_PWRSEL GPIO24_TRSTB GPIO25_TDI GPIO26_TCK GPIO27_TMS GPIO28_TDO
R341 R342 @4.7K_0402_5% VGA_LCD_DATA VGA_LCD_CLK
@5.11K_0402_1% TEST_EN
R315 10K_0402_5% VGA@
R714 R713 10K_0402_5% VGA@
VGA_SMB_CK2_R VGA_SMB_DA2_R Q54A Q54B 2N7002DW-T/R7_SOT363-6 VGA@
VGA_SMB_CK2 (33) VGA_SMB_DA2 (33)
R341 R338 R336 150_0402_1% VGA@

L83 BLM15BD121SN1D_0402 VGA@ +DPLL_PVDD
C951 10U_0603_6.3V6M C952 1U_0402_6.3V4Z C953 0.1U_0402_10V6K
R332 249_0402_1% VGA@
C958 0.1U_0402_10V6K
R843 @0_0402_5% 27MCLK_SSIC
R582 @0_0402_5% XTALOUT_XTL
82.5_0402_1% CLK_XTALIN
R160 100_0402_1% @
U46 ASM3P2872AF-06OR_TSOT-23-6
REFOUT VSS XOUT MODOUT XIN/CLKIN VDD
27MCLK_SSIC XTALOUT_XTL R_27M_SSC R841 @ 33_0402_1%
C949 0.1U_0402_10V6K C950 1U_0402_6.3V4Z
T69 PAD
C1040 10U_0603_6.3V6M C1041 1U_0402_6.3V4Z C1042 0.1U_0402_10V6K
08/11
Spread Spectrum For EMI

L40 L23 L24 BLM15BD121SN1D_0402 PARK@ VGA@
C322 C324 C323 10U_0603_6.3V6M C288 C294 C286 1U_0402_6.3V4Z C56 C57 C55 0.1U_0402_10V6K
+1.8VS_VGA +PCIE_VGA +DPC_VDD18 130mA +DPC_VDD10 200mA +DPC_PVDD 20mA

(16) VRAM_ID2 (16) VRAM_ID1 (16) VRAM_ID0
VRAM_ID2 VRAM_ID1 VRAM_ID0
GPU_GPIO0 GPU_GPIO1 GPU_GPIO2 GPU_GPIO3 GPU_GPIO4
(25,33,39) ACIN
(33) VGA_ENBKL
GPU_GPIO8 GPU_GPIO9 GPU_GPIO11 GPU_GPIO12 GPU_GPIO13
(44) VGA_PWRSEL (20) 27M_SSC
THM_ALERT#
(17) GPIO21_BBEN
R300 @ 10K_0402_5% D4 @ RB751V_SOD323
R301 @ 10K_0402_5%
R840 @ 2R_27M_SSC
(21) VGA_LCD_CLK (21) VGA_LCD_DATA
GPIO24_TRSTB GPIO25_TDI GPIO26_TCK GPIO27_TMS GPIO28_TDO
(16) TEST_EN
GPU_THERMAL_D+ GPU_THERMAL_D-



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix H5TQ1G63BFR-12C	1	0	0
Samsung K4W1G1646E-HC12	0	1	0

	M93-S3	PARK-S3
R306	NA	10K
R579	0/short	680
R320	2.2K	NA
C287	2.2nF	68pF

	M93-S3	PARK-S3
R330	NC	240
R130	NC	0/short
R312	240	150
R331	NC	240

	M93-S3	PARK-S3
R485	4.7K	51.1
R486	4.7K	51.1
C311	0/short	0.1uF
C312	0/short	0.1uF

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

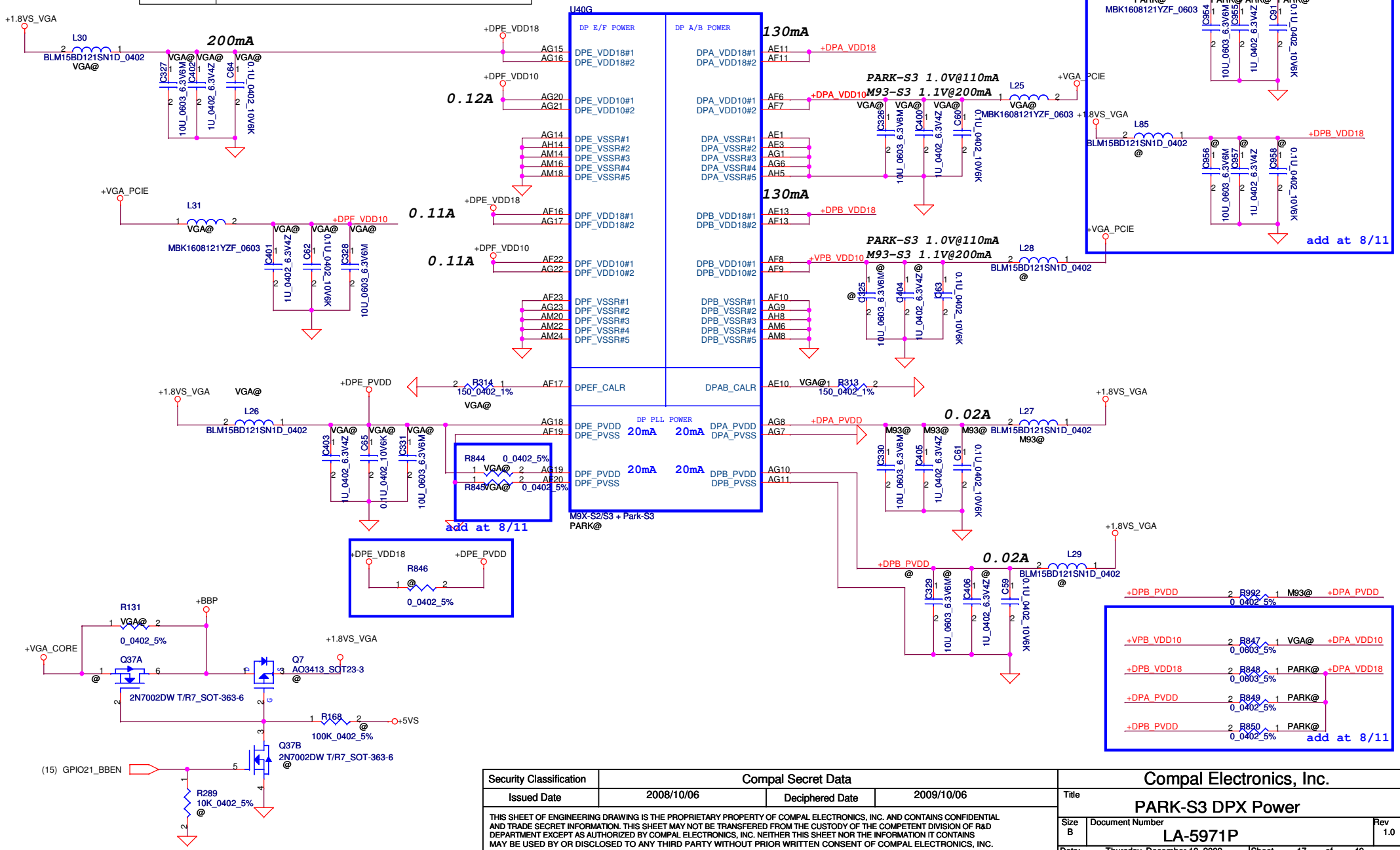
Compal Electronics, Inc.

Title: PARK-S3 MEM Interface

Size	Document Number	Rev
B	LA-5971P	1.0

Date: Thursday, December 10, 2009 Sheet 16 of 49

DPE_VDD10	Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V
DPF_VDD10	M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V



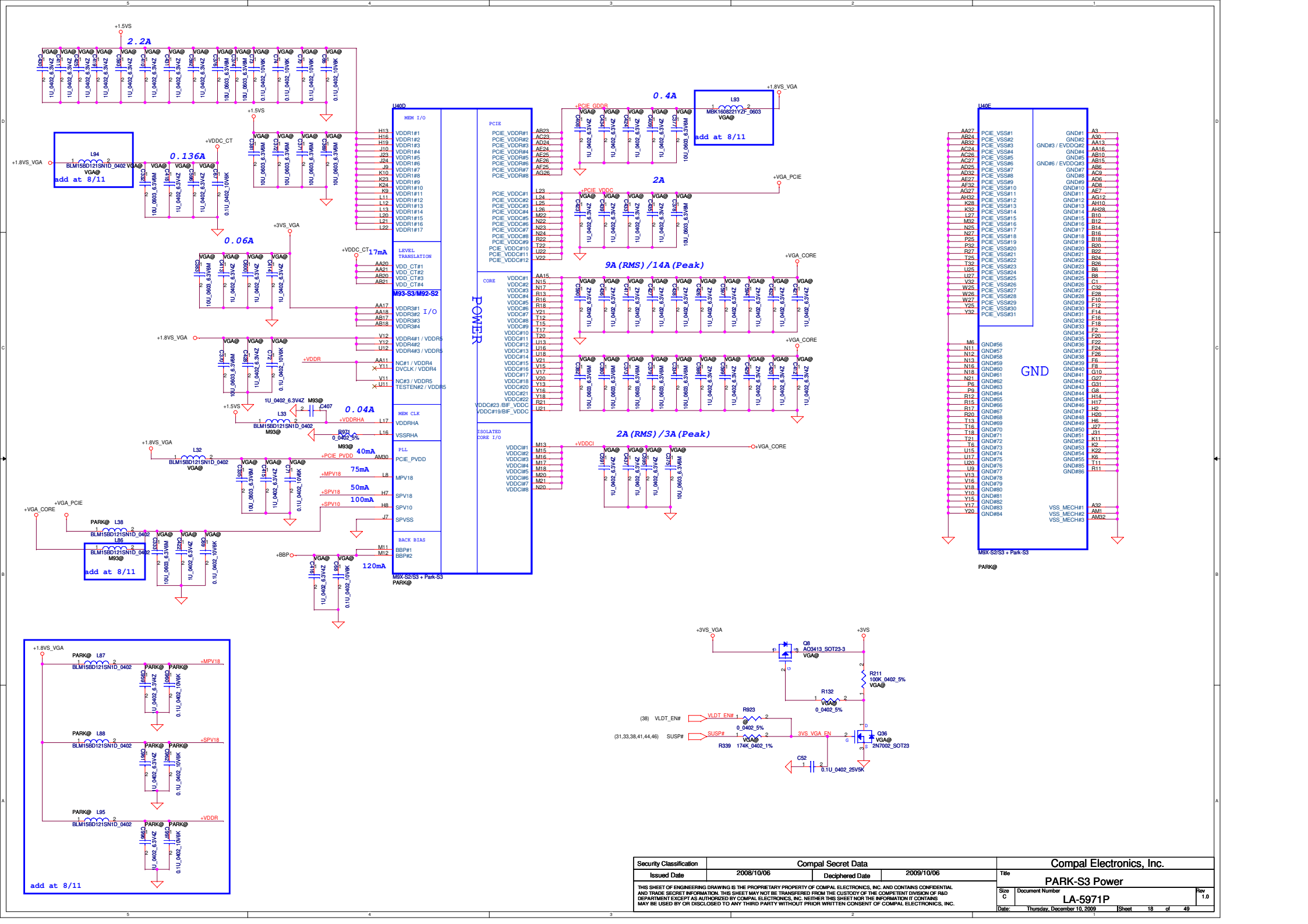
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 DPX Power

Size	Document Number	Rev
B	LA-5971P	1.0

Date: Thursday, December 10, 2009 Sheet 17 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 Power

Size	Document Number	Rev
C	LA-5971P	1.0

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(16) M_DA[63..0] — M_DA[0..63]
(16) M_MA[13..0] — M_MA[13..0]
(16) M_DQM[7..0] — M_DQM[7..0]
(16) M_DQS[7..0] — M_DQS[7..0]
(16) M_DQS#[7..0] — M_DQS#[7..0]

ZZZ2 X76-S
Hynix X76H@ Samsung X76S@

U21 U22
SAMSUNG VRAM S@ SAMSUNG VRAM S@

U23 U24
SAMSUNG VRAM S@ SAMSUNG VRAM S@

U21 — U22 — U23 — U24

VREFC_A1 VREFD_Q1 VREFC_A2 VREFD_Q2 VREFC_A3 VREFD_Q3 VREFC_A4 VREFD_Q4
VREFCA VREFDQ
M_MA0 M_MA1 M_MA2 M_MA3 M_MA4 M_MA5 M_MA6 M_MA7 M_MA8 M_MA9 M_MA10 M_MA11 M_MA12 M_MA13
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15/BA3
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
M_DA16 M_DA23 M_DA19 M_DA21 M_DA17 M_DA18 M_DA22 M_DA20 M_DA0 M_DA4 M_DA1 M_DA6 M_DA3 M_DA7 M_DA2 M_DA5
M_DA25 M_DA27 M_DA24 M_DA31 M_DA26 M_DA30 M_DA28 M_DA29 M_DA14 M_DA10 M_DA15 M_DA11 M_DA12 M_DA8 M_DA13 M_DA9
M_DA38 M_DA34 M_DA33 M_DA37 M_DA35 M_DA39 M_DA32 M_DA36 M_DA44 M_DA42 M_DA47 M_DA40 M_DA45 M_DA43 M_DA46 M_DA41
M_DA54 M_DA52 M_DA53 M_DA49 M_DA51 M_DA50 M_DA55 M_DA48 M_DA57 M_DA58 M_DA60 M_DA61 M_DA63 M_DA62 M_DA56 M_DA59
BA0 BA1 BA2
M_BA0 M_BA1 M_BA2
M_CLK0 M_CLK#0 M_CKE0
M_CLK1 M_CLK#1 M_CKE1
CK CK CKE/CKE0
M_ODT0 M_CS#0 M_RAS#0 M_CAS#0 M_WE#0
M_ODT1 M_CS#1 M_RAS#1 M_CAS#1 M_WE#1
ODT/ODT0 CS RAS CAS WE
M_DQS2 M_DQS0 M_DQS3 M_DQS1 M_DQS4 M_DQS5 M_DQS6 M_DQS7
DQSL DQSU
M_DQM2 M_DQM0 M_DQM3 M_DQM1 M_DQM4 M_DQM5 M_DQM6 M_DQM7
DML DMU
M_DQS#2 M_DQS#0 M_DQS#3 M_DQS#1 M_DQS#4 M_DQS#5 M_DQS#6 M_DQS#7
DRAM_RST#
RESET
ZQ/ZQ0
NC/ODT1 NC/CS1 NC/CE1 NCZQ1
NC
VDD VDDQ VSS VSSQ
+1.5VS
100-BALL SDRAM DDR3
64MX16 H5TQ1G63BFR-12C FBGA
H@

R329 R326 R328 R327
240_0402_1% VGA@

R356 R355 R345 R351 R354 R350 R352 R359
4.99K_0402_1% VGA@
R346 R347 R348 R349 R358 R353 R357 R344
C90 C91 C92 C79 C78 C81 C95 C77
0.1U_0402_10V6K VGA@

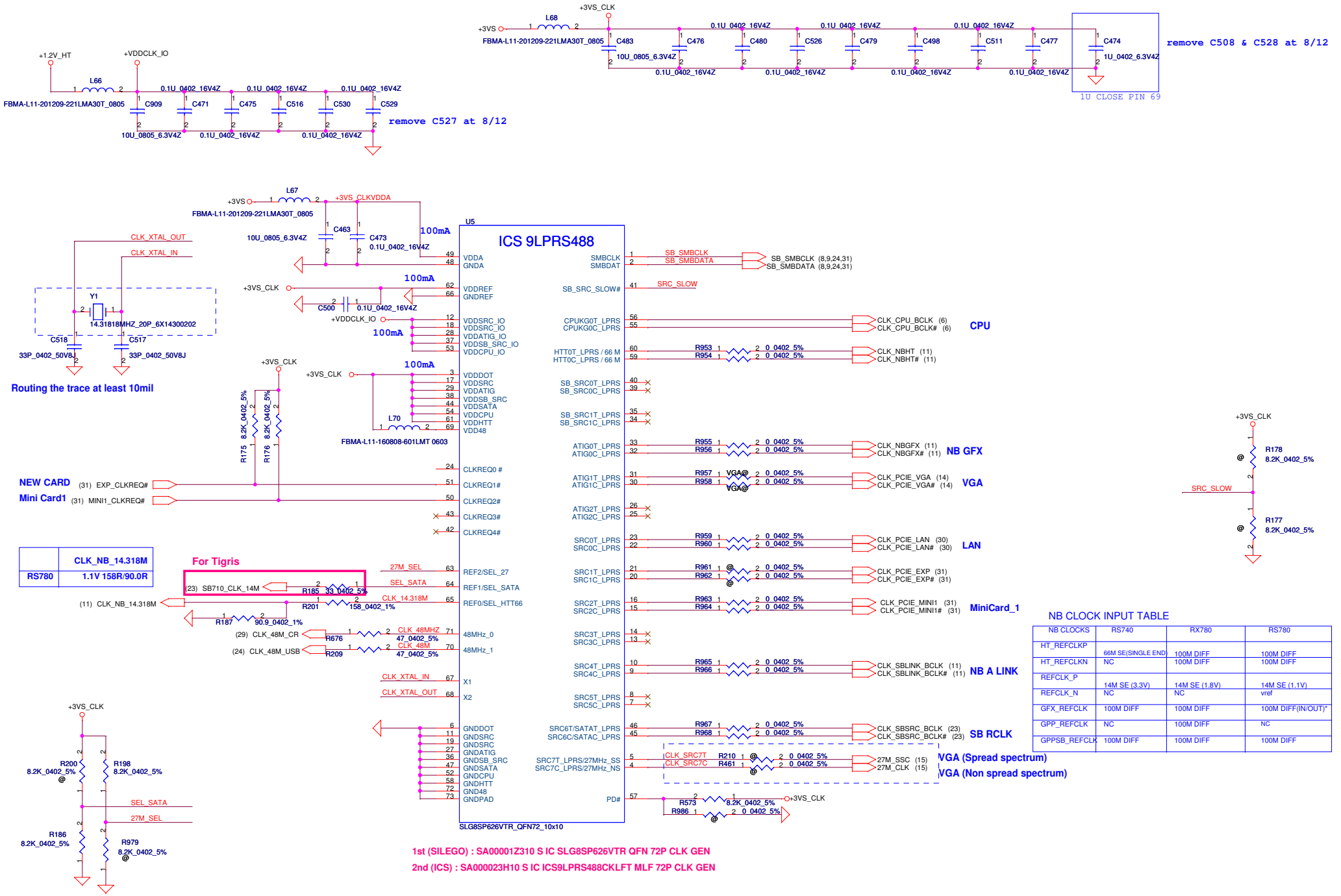
M_CLK0_1 M_CLK#0_1 R576 R489 56_0402_1%
C53 0.01U_0402_16V7K VGA@
M_CLK1_1 M_CLK#1_1 R574 R575 56_0402_1%
C54 0.01U_0402_16V7K VGA@

10U_0603_6.3V6M VGA@
C386 C387 C389 C385 C388 C384

1U_0402_6.3V4Z VGA@
C681 C682 C681 C676 C688 C680 C687 C686 C687 C682
C684 C675 C685 C683 C680 C679 C683 C674 C685 C678

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.
Title: PARK-S3 DDR3 VRAM
Size: C | Document Number: LA-5971P | Rev: 1.0
Date: Thursday, December 10, 2009 | Sheet 19 of 49



	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1	NON SPREAD 100M_SATA SRC6 output
	0*	SPREAD 100M_SATA SRC6 output

* default

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

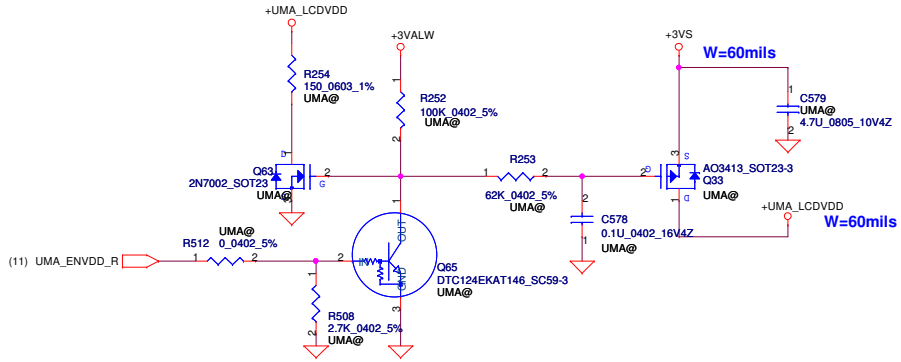
Compal Electronics, Inc.

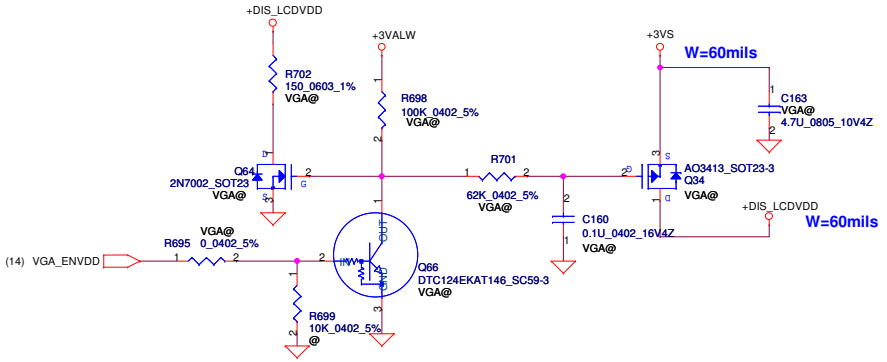
Title: Clock generator

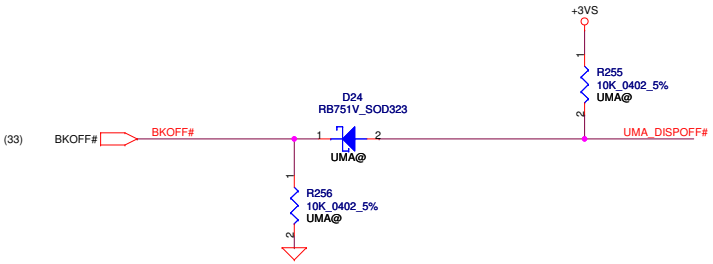
Size: Custom | Document Number: LA-5971P | Rev: 1.0

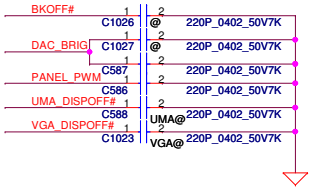
Date: Thursday, December 10, 2009 | Sheet 20 of 49

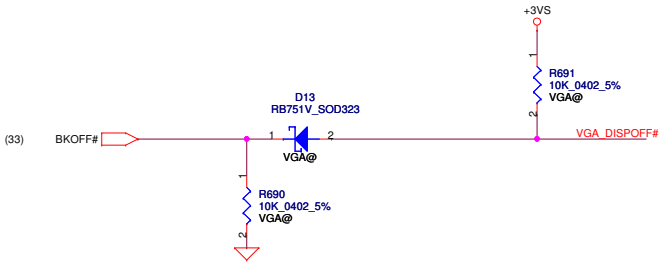
LCD POWER CIRCUIT

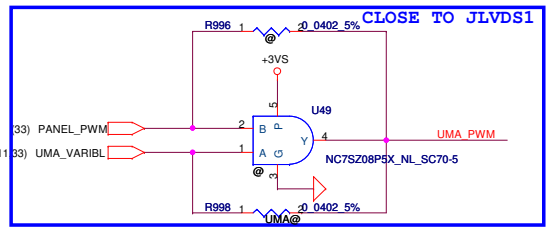


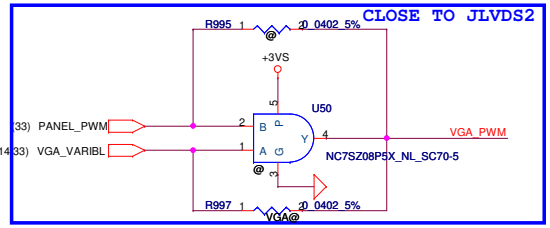




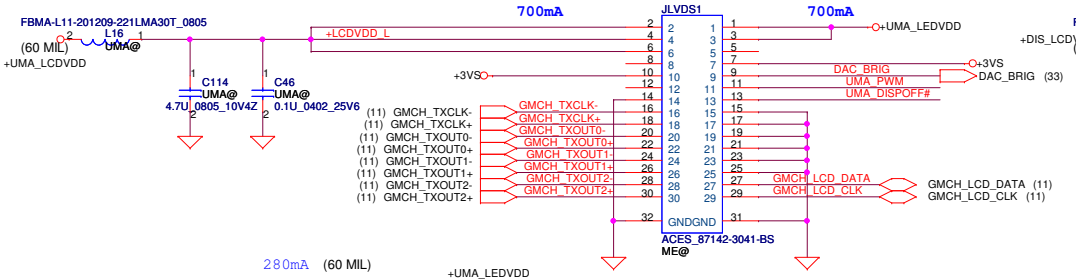


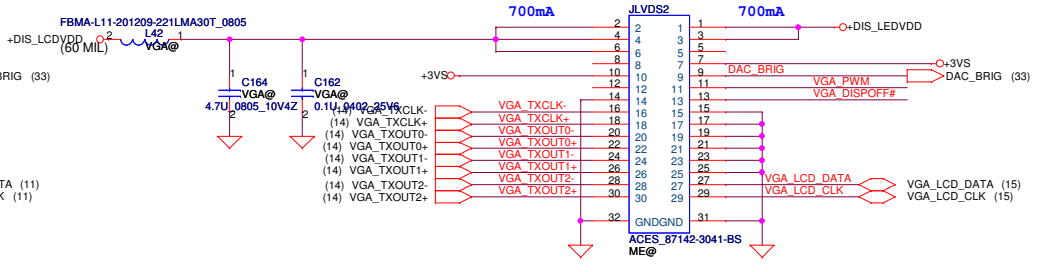


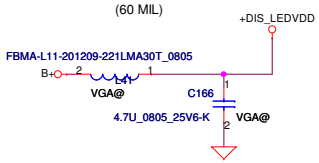




LCD/PANEL BD. Conn.







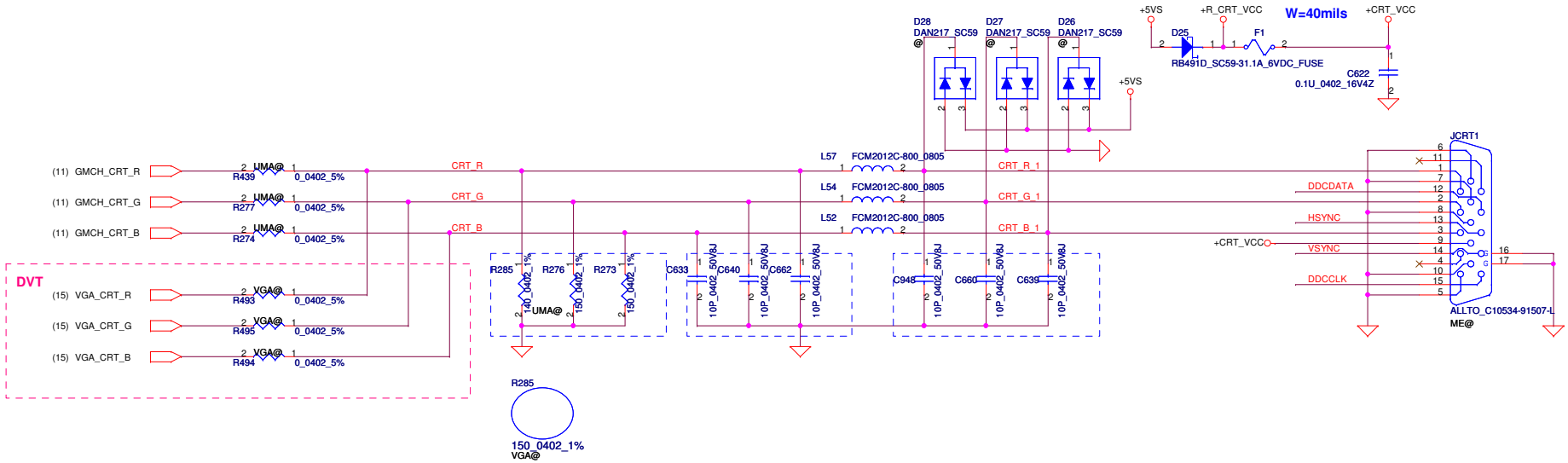
Compal Electronics, Inc.

Title: LVDS Connector

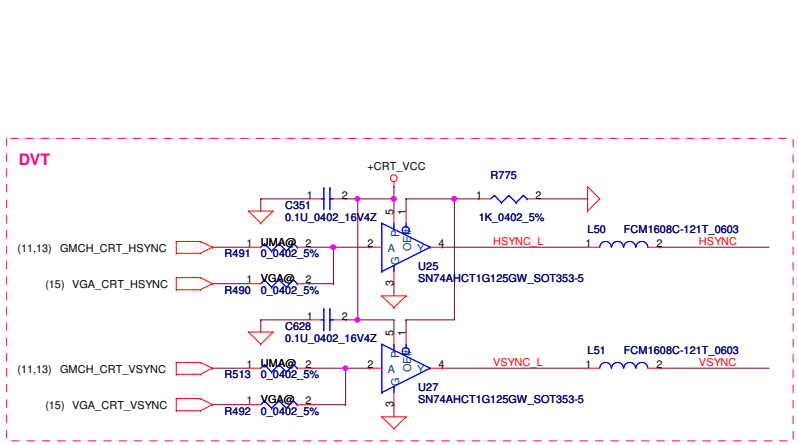
Size: B | Document Number: LA-5971P | Rev: 1.0

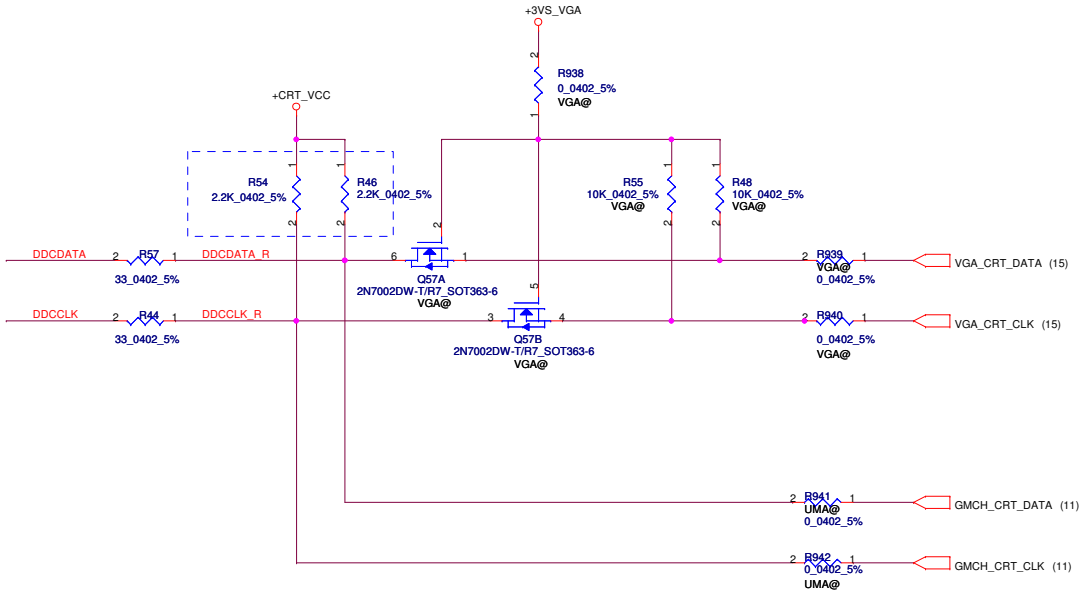
Date: Thursday, December 10, 2009 | Sheet 21 of 49

CRT CONNECTOR



Place closed to chipset





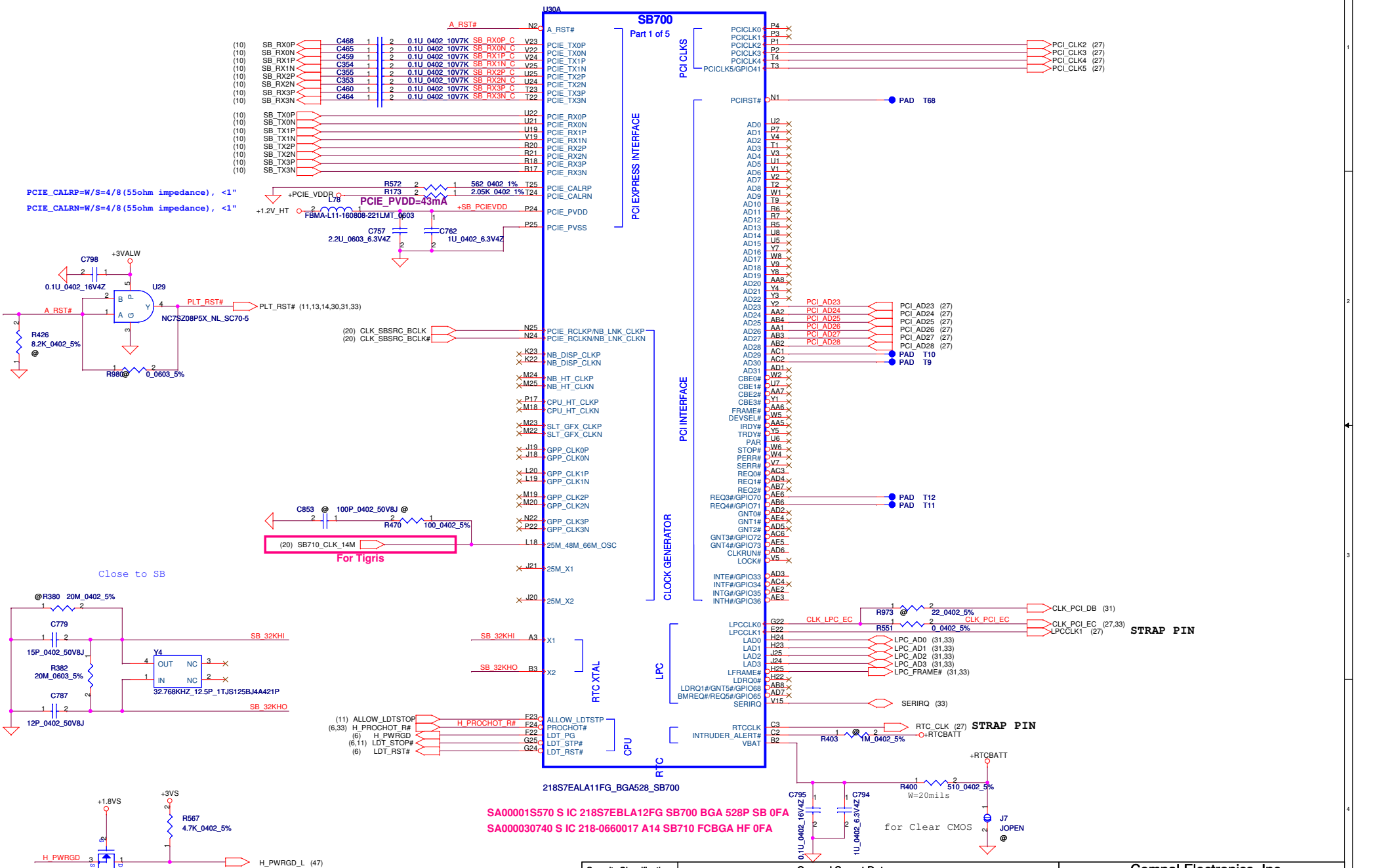
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
B	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 22 of 49



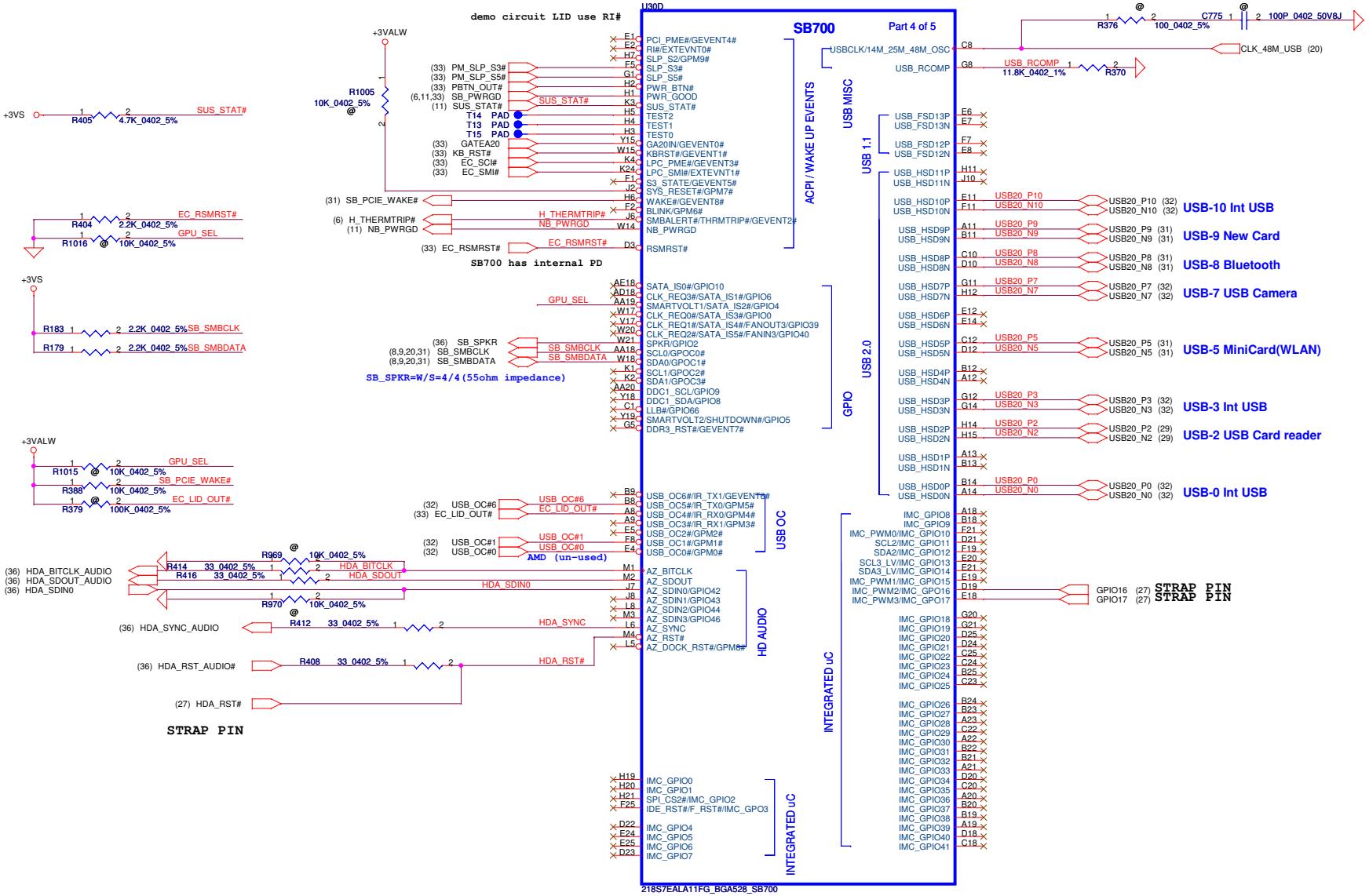
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: SB710-PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 23 of 49



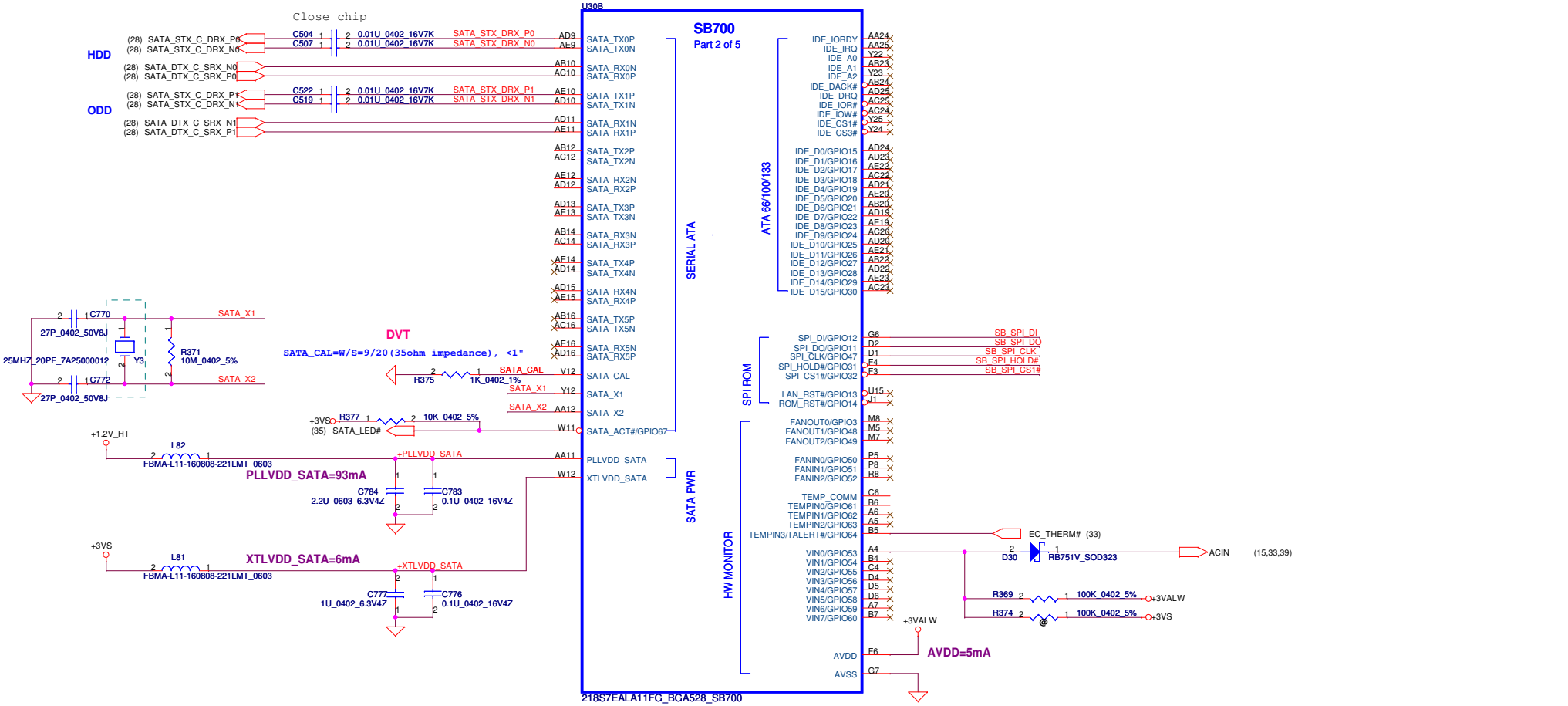
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: SB710 USB/HD audio

Size	Document Number	Rev
Custom	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 24 of 49



Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler

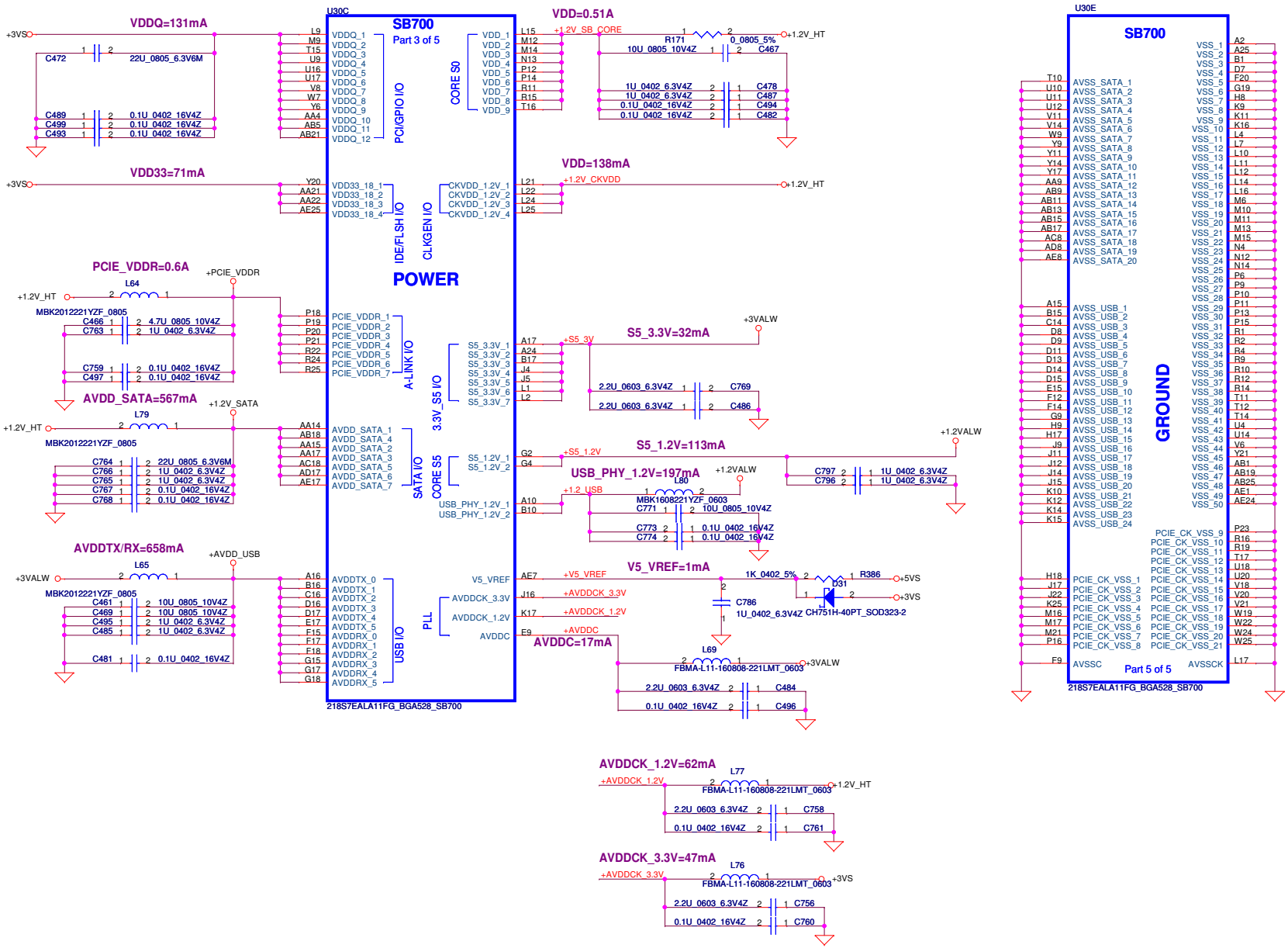
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: SB710 SATA/IDE/SPI

Size	Document Number	Rev
Custom	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 25 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: SB710 power/GND

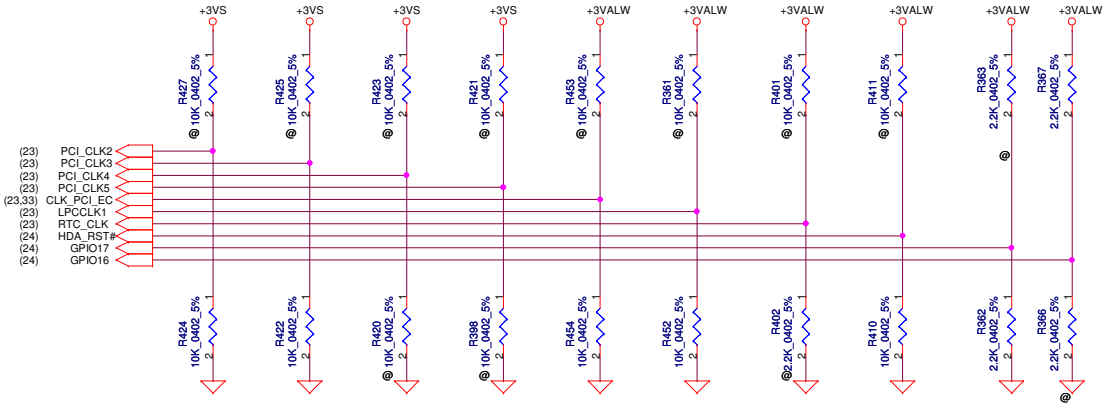
Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 26 of 49

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

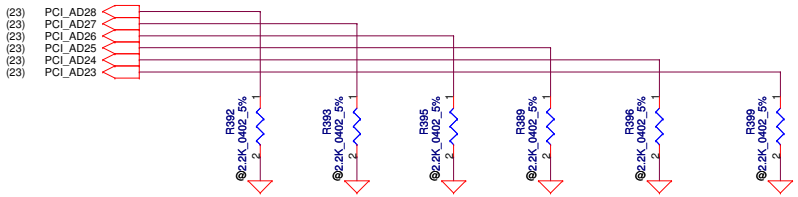
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	**INTERNAL RTC** DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	**BOOTFAIL TIMER DISABLED** DEFAULT	**IGNORE DEBUG STRAPS** DEFAULT			**DISABLE PCI MEM BOOT** DEFAULT	**CLKGEN DISABLED** DEFAULT	**EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK)	**EC DISABLED** DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	**USE LONG RESET** DEFAULT	**USE PCI PLL** DEFAULT	**USE ACPI BCLK** DEFAULT	**USE IDE PLL** DEFAULT	**USE DEFAULT PCIE STRAPS** DEFAULT	**RESERVED**
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



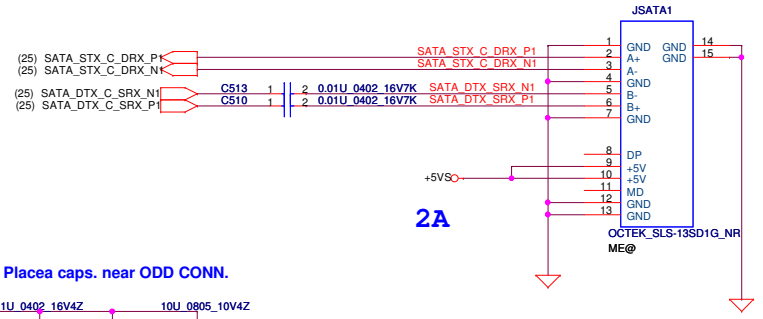
Compal Electronics, Inc.

Title: SB710 STRAPS

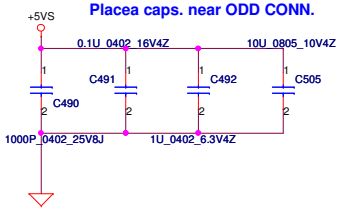
Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 27 of 49

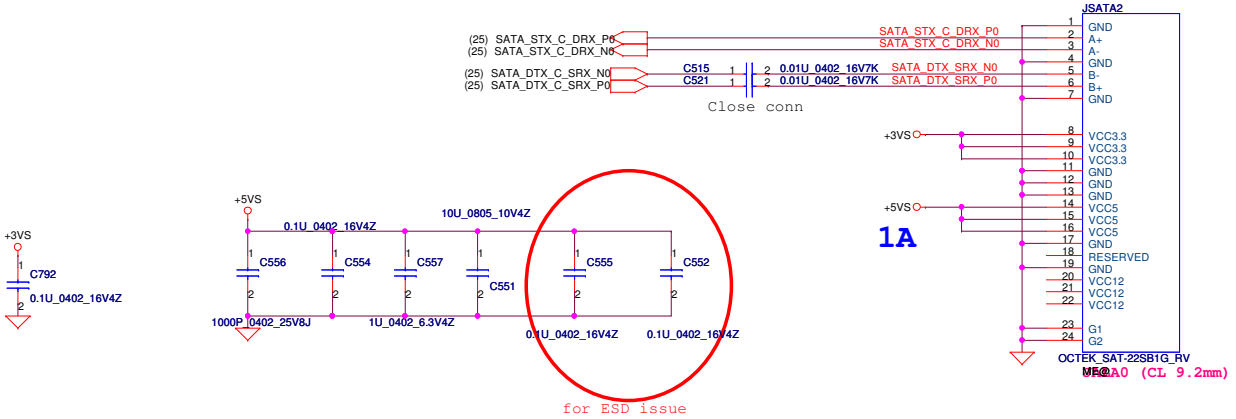
SATA ODD Conn.



Placea caps. near ODD CONN.



SATA HDD Conn.



VGA0 (CL 9.2mm)

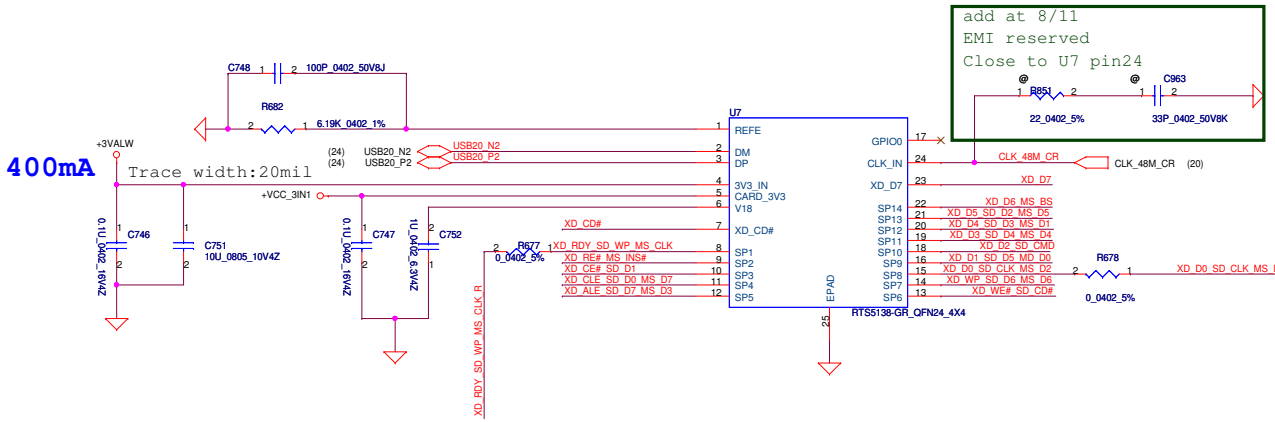
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

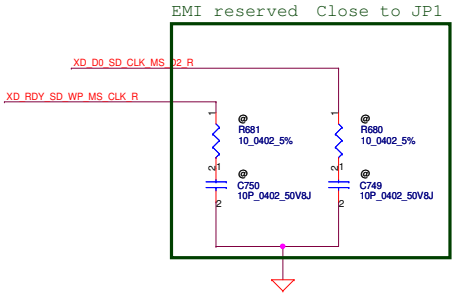
Compal Electronics, Inc.

Title: HDD & ODD Connector

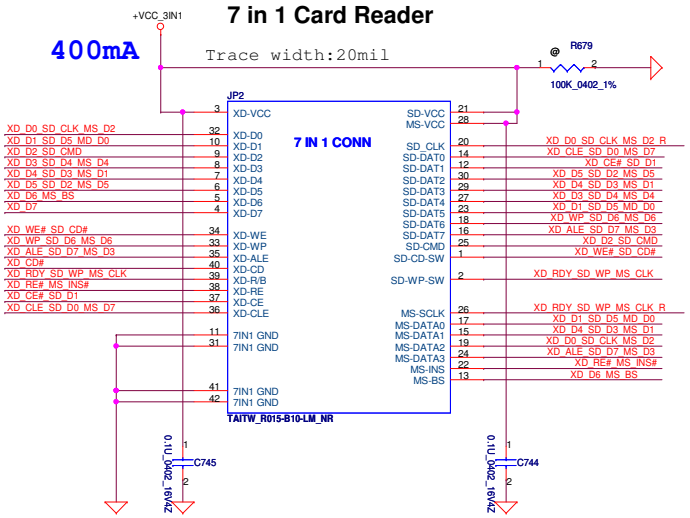
Size	Document Number	Rev
B	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 28 of 49





Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



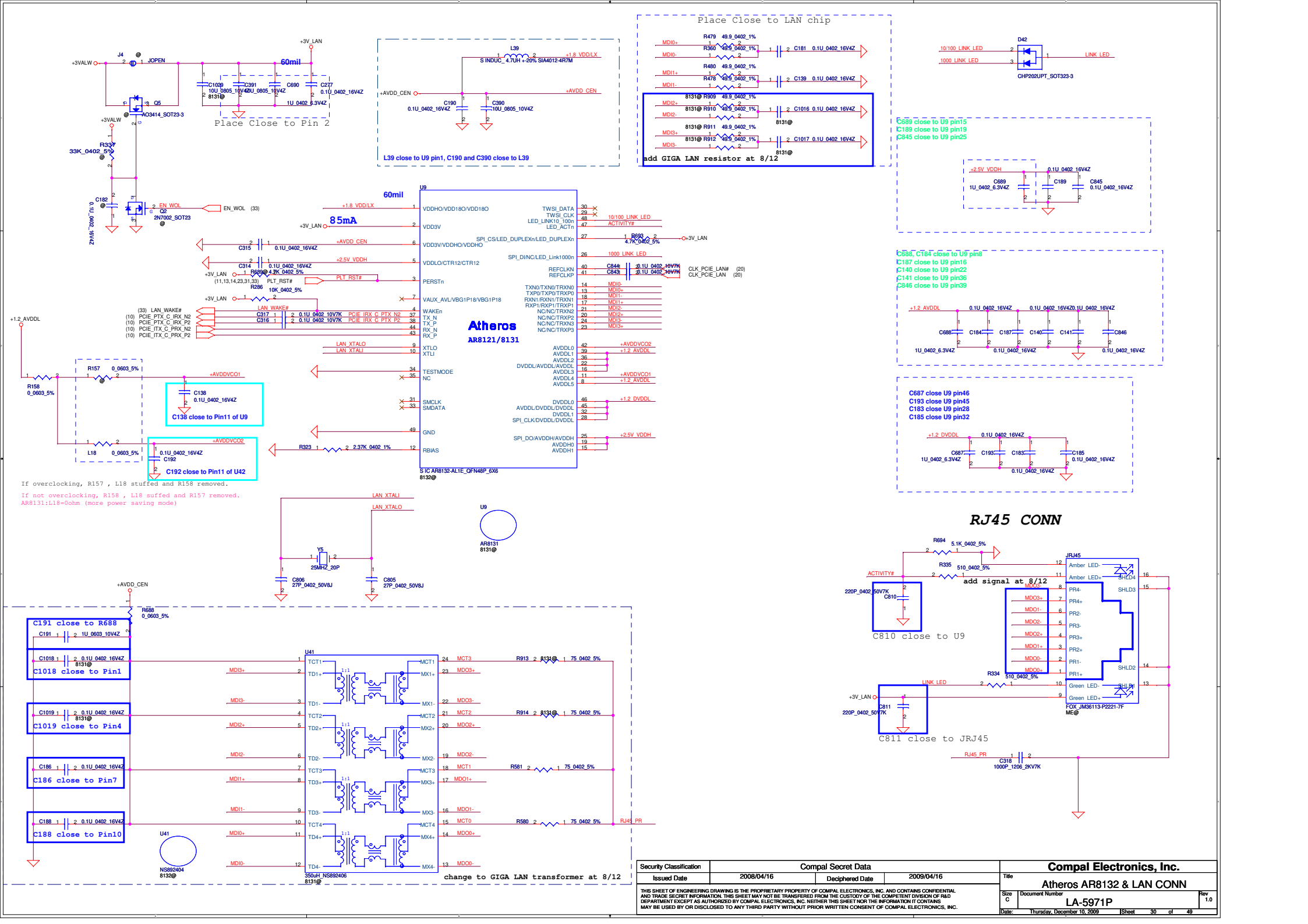
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: RTS5138 Card Reader

Size: Custom | Document Number: LA-5971P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 29 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

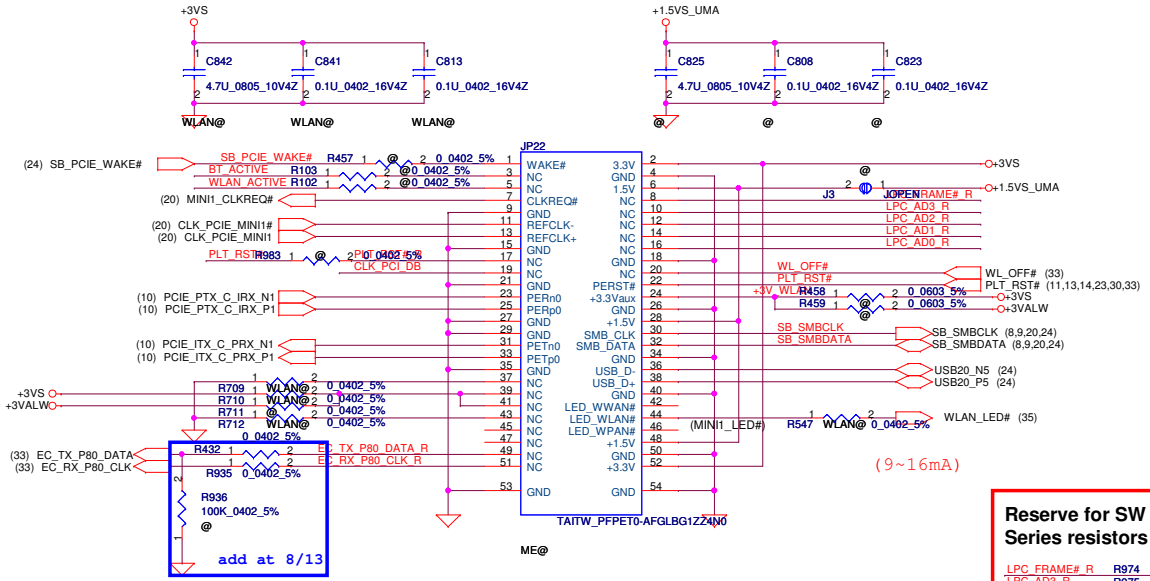
Compal Electronics, Inc.

Title: Atheros AR8132 & LAN CONN

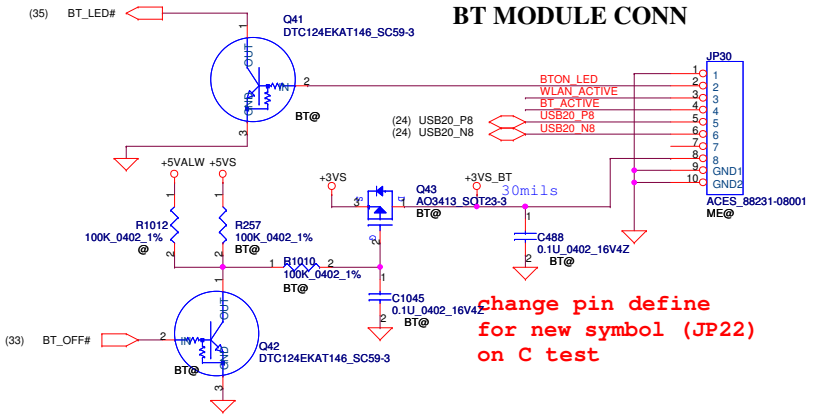
Size	Document Number	Rev
C	LA-5971P	1.0

Date: Thursday, December 10, 2009 | Sheet 30 of 49

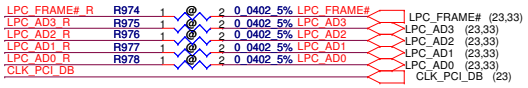
For Wireless LAN



BT MODULE CONN

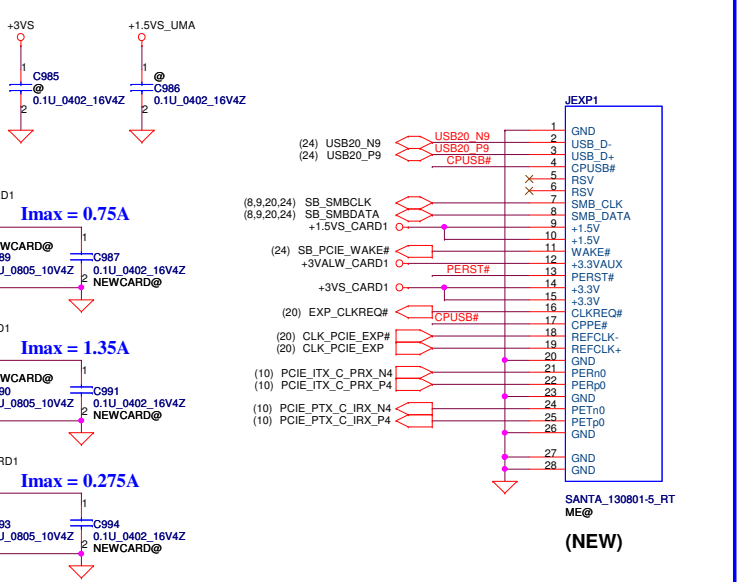


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



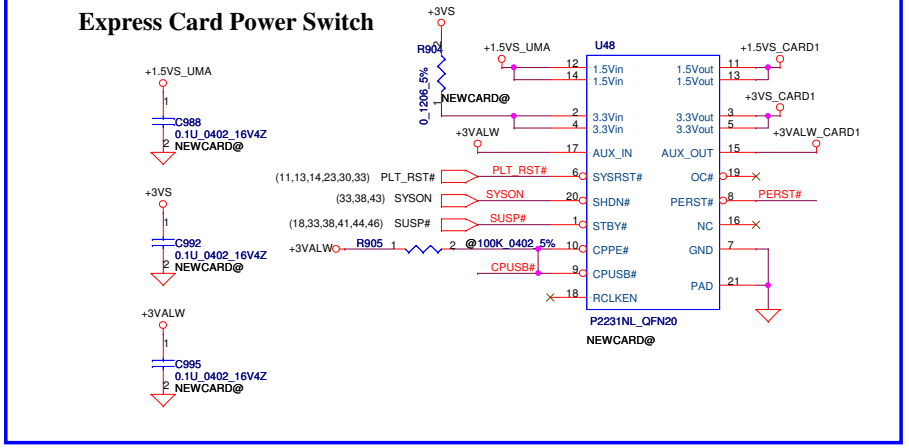
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

add at 8/11



add at 8/11

Express Card Power Switch



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: MINI CARD/BT/ NEW CARD

Size	Document Number	Rev
B	LA-5971P	1.0

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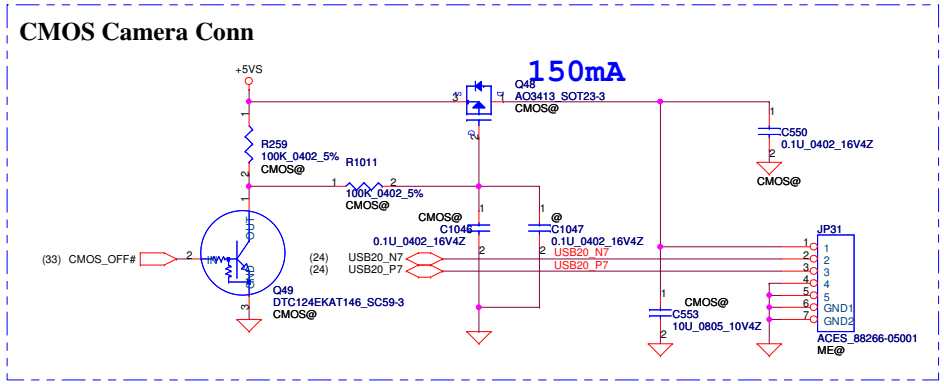

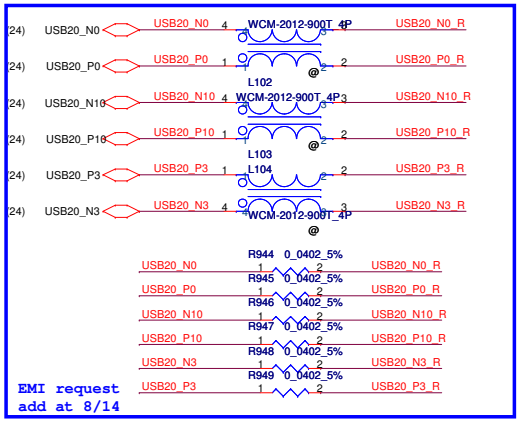

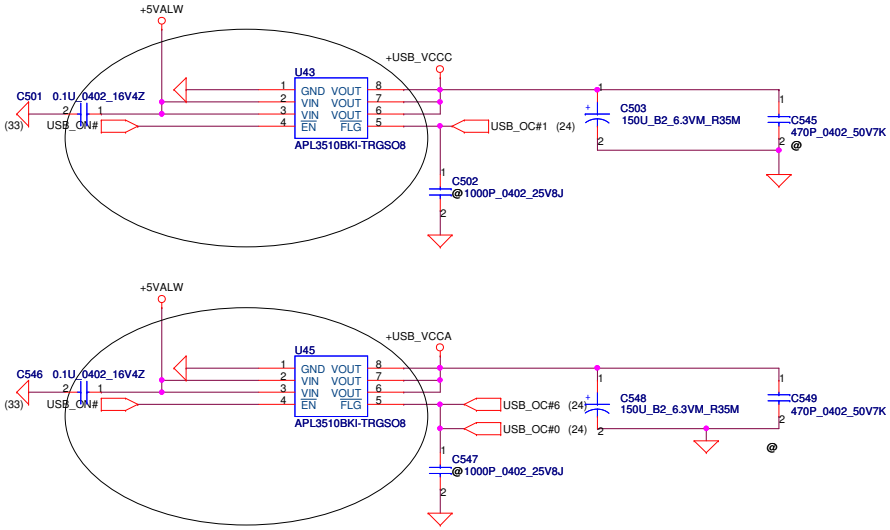

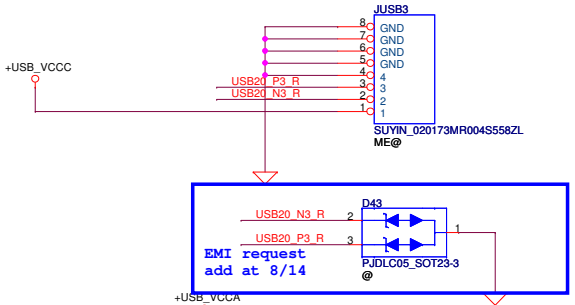

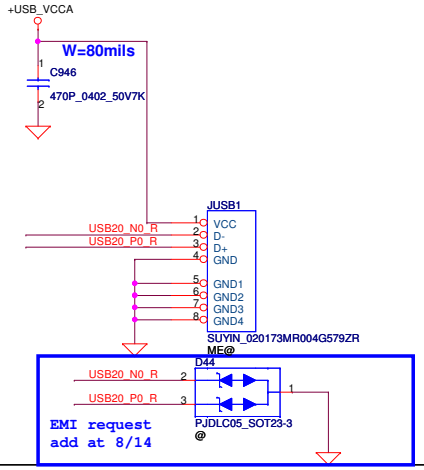

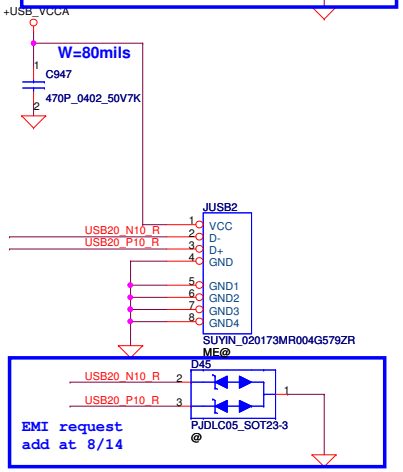

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: BlueTooth / Int USB x2 /eSATA

Size	Document Number	Rev
B	LA-5971P	1.0

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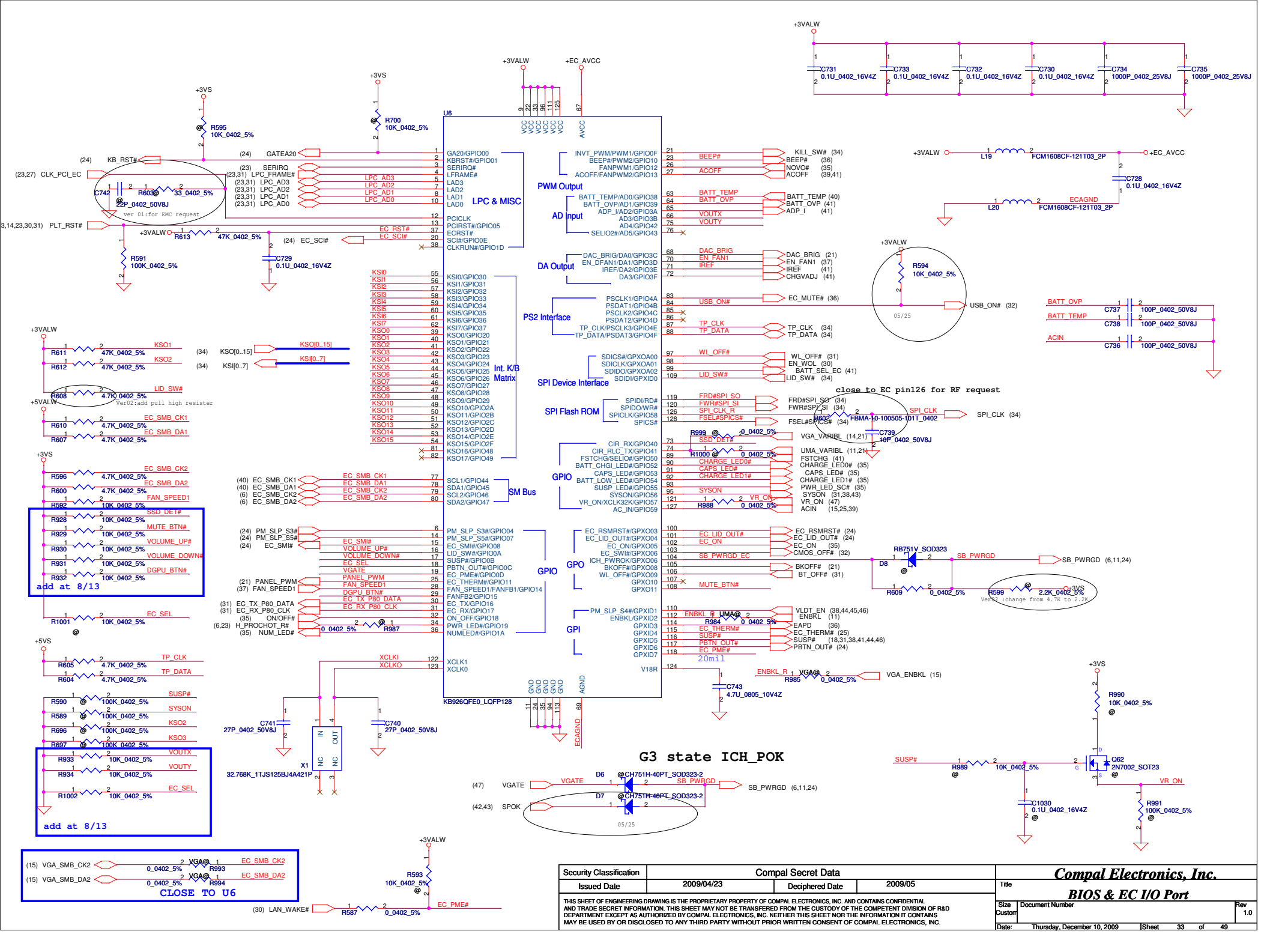

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2009/05

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom		1.0

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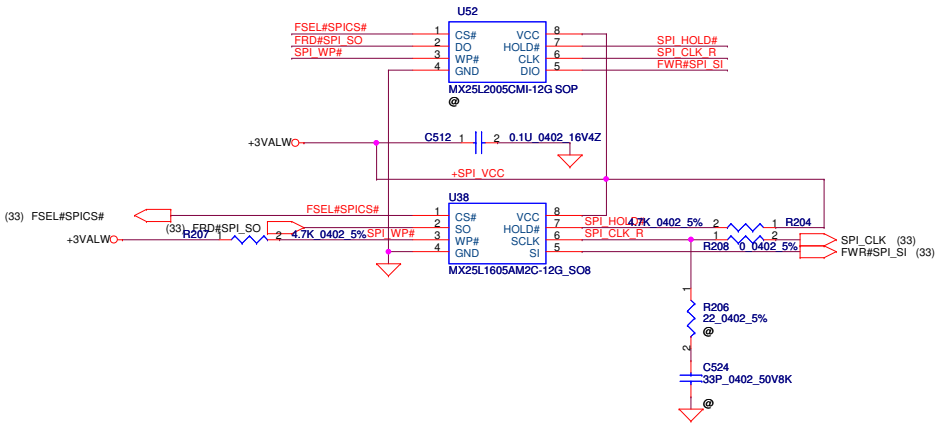
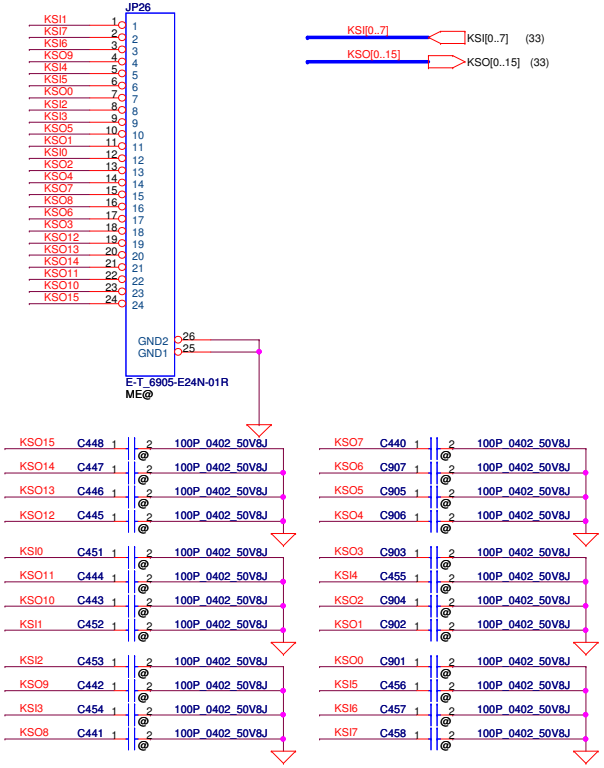
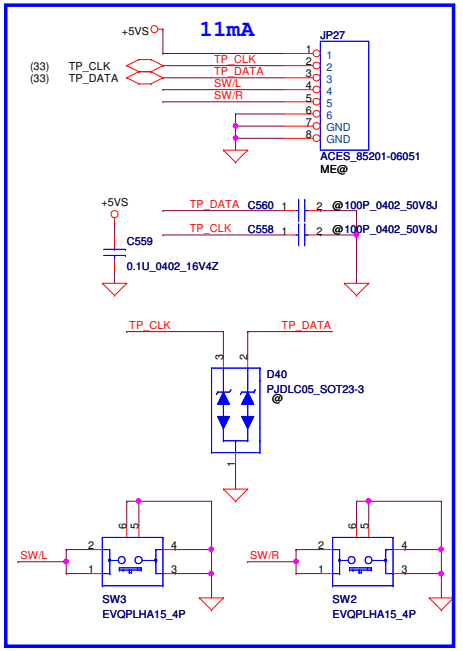
BIOS(SYS / EC / VGA)

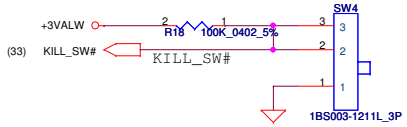


INT_KBD Conn.

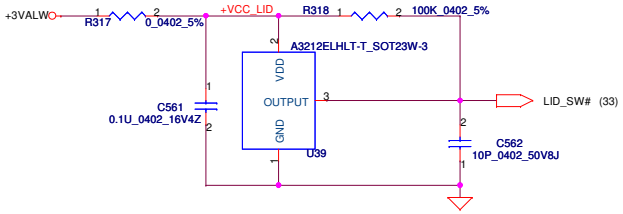




Kill Switch



Lid Switch



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
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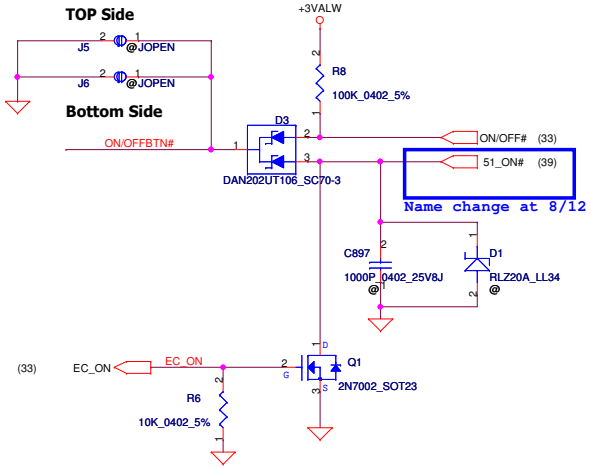
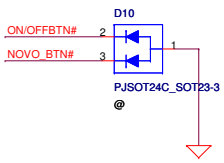
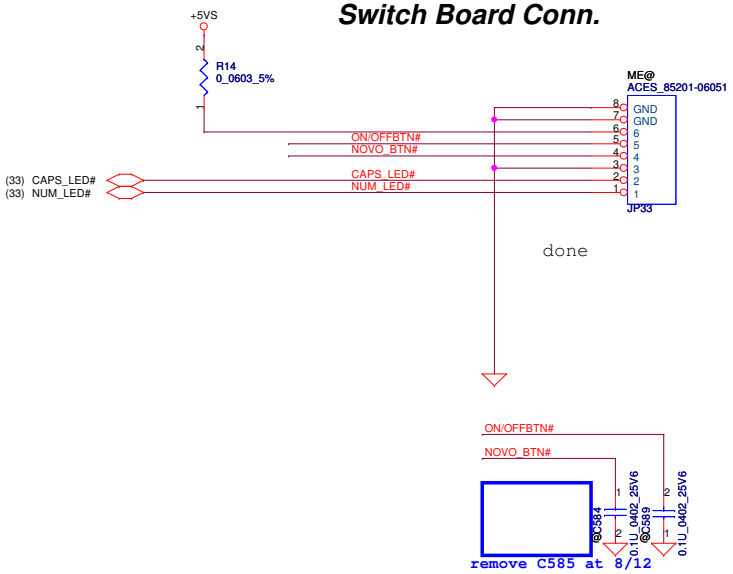
Power Button

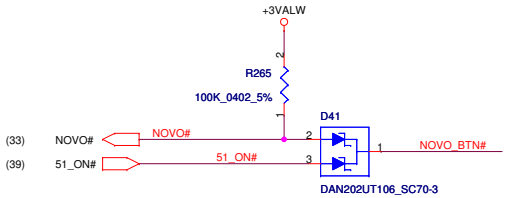
ON/OFF switch



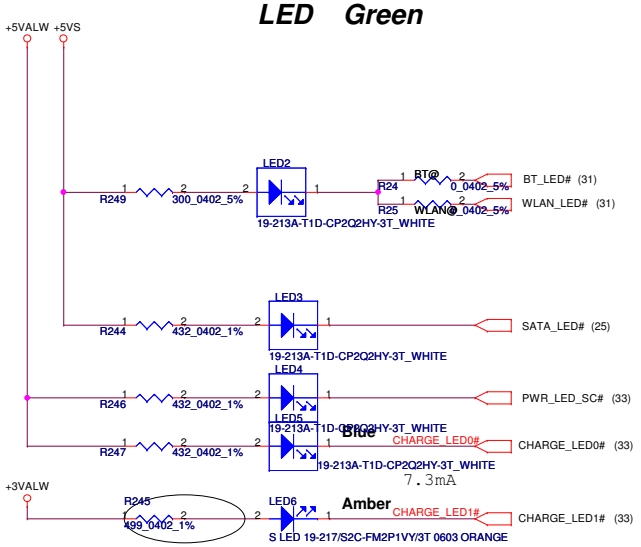


Switch Board Conn.





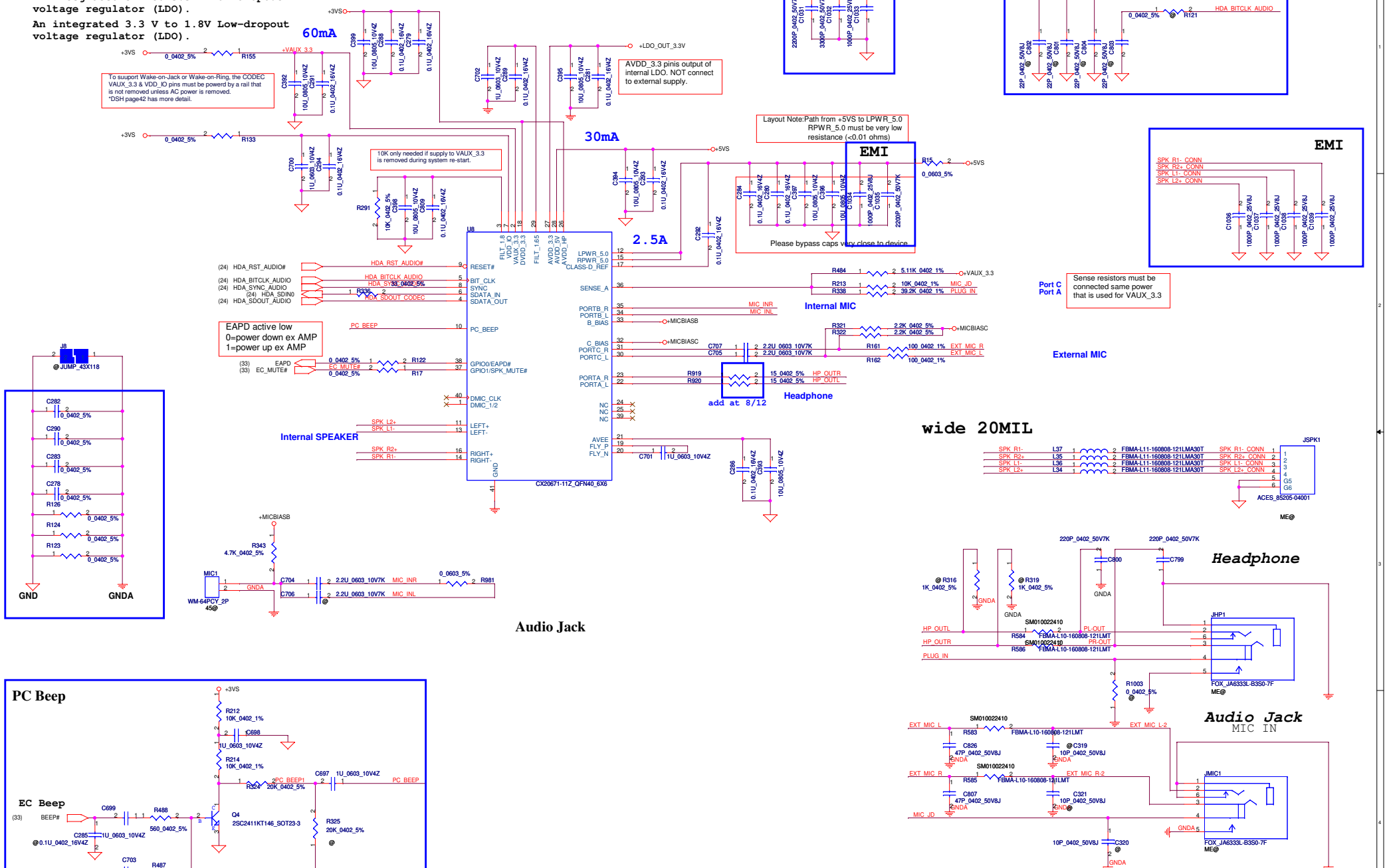
LED Green



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

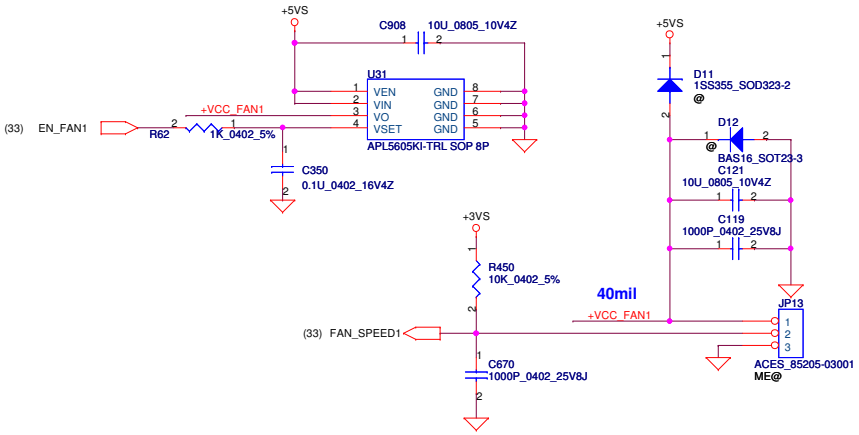
Compal Electronics, Inc.			
Title	Power BTN/LED		
Size B	Document Number LA-5971P		Rev 1.0
Date: Thursday, December 10, 2009	Sheet 35 of 49		

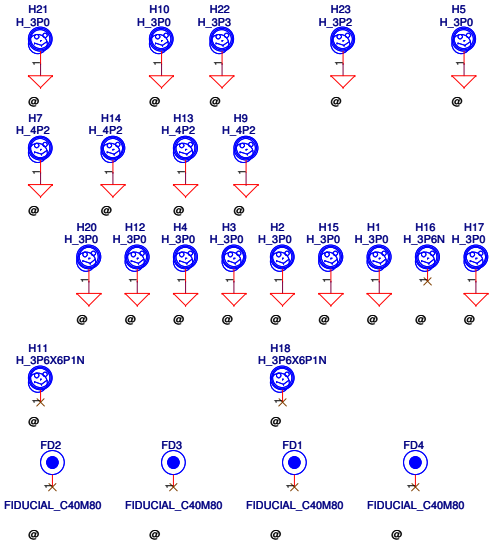
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2009/10/06
Title	HD Audio Codec ALC888S-VC		
Size C	Document Number LA-5971P		Rev 1.0
Date: Thursday, December 10, 2009	Sheet 36 of 49		

FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
B	LA-5971P	1.0

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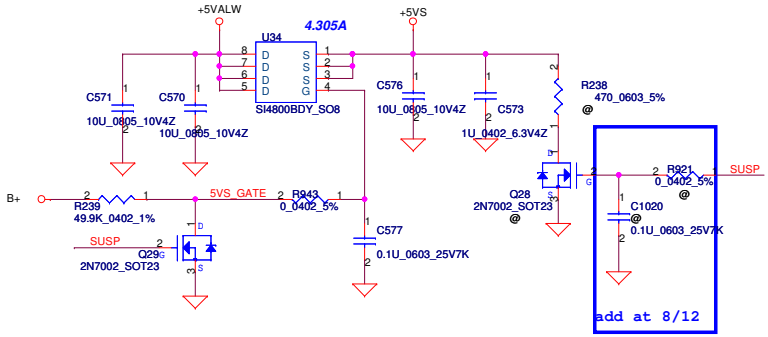
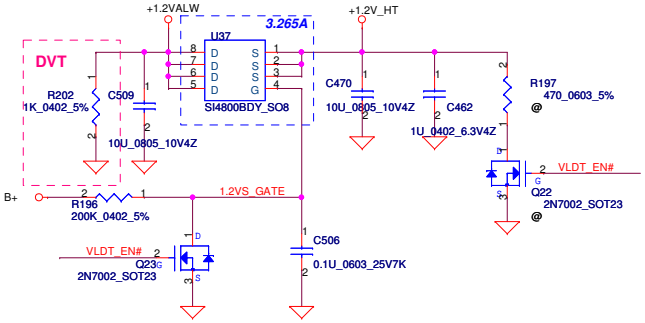
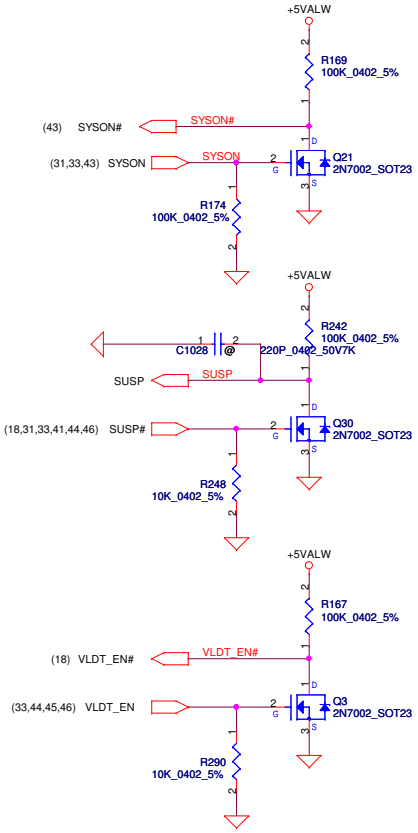
+5VALW TO +5VS

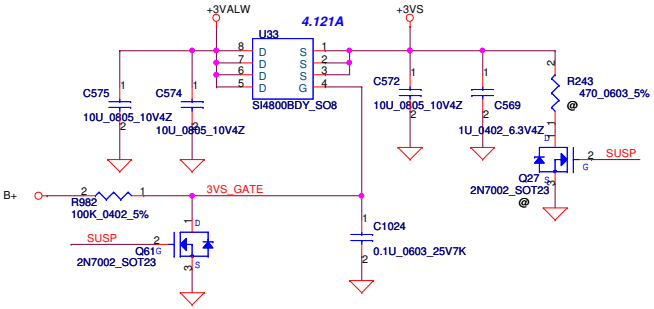


+1.2VALW TO +1.2V_HT

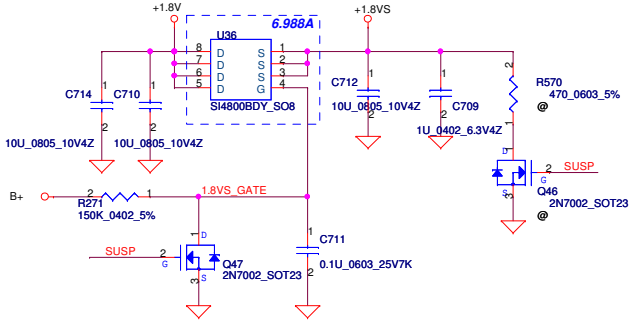


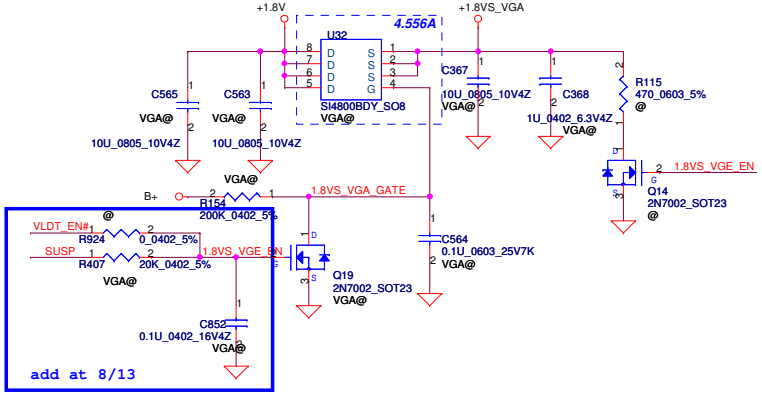


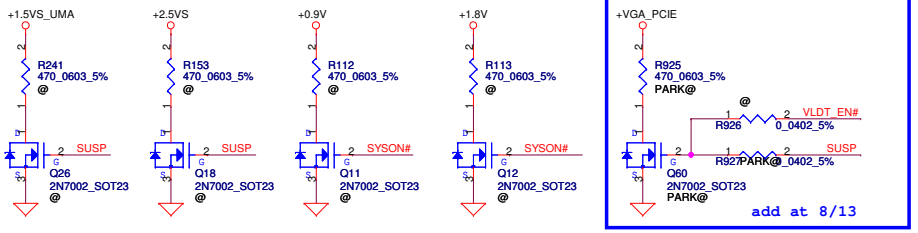
+3VALW TO +3VS



+1.8V to +1.8VS







Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	LA-5971P	1.0

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DC030006J00

VIN

PF101 7A_24VDC_429007.WRML

PL101 SMB3025500YA_2P

APDIN APDIN1

@4602-Q04C-09R 4P P2.5 JDCIN

PC101 @ 0.1U_0603_25V7K
PC102 1000P_0402_50V7K
PC103 100P_0402_50V8J
PC104 @ 0.1U_0603_25V7K
PC105 100P_0402_50V8J
PC106 1000P_0402_50V7K

Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

PR107 1M_0402_1%
VINDE-2
VS
VIN
PR108 84.5K_0402_1%
PR111 22K_0402_1%
VINDE-1
VINDE-3
PC107 0.01U_0402_25V7K
PR109 10K_0805_5%
PR110 10K_0402_1%
ACIN (15,25,33)
PACIN
PACIN (41)
PU101A LM393DG_SO8
PC108 0.068U_0603_16V7K
PR112 20K_0402_1%
PC109 0.1U_0402_16V7K
PR115 10K_0402_5%
PD102 LLZ4V3B_LL34-2
PR114 10K_0402_5%
RTCVREF 3.3V

VIN
PD104 LL4148_LL34-2
51ON-1
BATT+
PD105 LL4148_LL34-2
PR121 68_1206_5%
PR122 68_1206_5%
PQ104 TP0610K-T1-E3_SOT23-3
PR123 200_0603_5%
CHGRTCP
51ON-2
VS
PR126 100K_0402_1%
PR127 22K_0402_1%
PC114 0.22U_0603_25V7K
51ON-3
PC115 0.1U_0603_25V7K
(35) 51_ON#

RTCVREF
+CHGRTC
PR130 560_0603_5%
3.3V
PU102 G920AT24U_SOT89-3
OUT IN GND
PR128 200_0603_5%
CHGRTCIN
PC116 10U_0603_6.3V6M
PC117 1U_0805_25V4Z

ACIN

Precharge detector

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

VIN
PD101 LL4148_LL34-2
PR101 1K_1206_5%
PR102 1K_1206_5%
PR103 1K_1206_5%
PQ101 TP0610K-T1-E3_SOT23-3
PR104 100K_0402_1%
PR105 100K_0402_1%
PR106 100K_0402_1%
(33,41) ACOFF
PQ102 DTC115EUA_SC70-3
PQ103 DTC115EUA_SC70-3
B+

VL
PR113 2.2M_0402_5%
PR117 100K_0402_1%
PD103 RB715F_SOT323-3
(40,42) MAINPWON
(41) ACON
PU101B LM393DG_SO8
PC113 0.1U_0603_25V7K
PC111 1000P_0402_50V7K
PR116 499K_0402_1%
PR118 205K_0402_1%
PR119 499K_0402_1%
PC112 0.01U_0402_25V7K
PRG++
PR124 10K_0402_5%
RTCVREF
PQ105 SSM3K7002F_SC59-3
PR125 47K_0402_5%
PACIN (41)
+5VALW
PQ106 DTC115EUA_SC70-3

JRTC
@MAXEL_ML1220T10
PR129 560_0603_5%
+RTCBATT
PD106 RB751V-40_SOD323-2
+CHGRTC

RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: Custom | Document Number | Rev: 1.0

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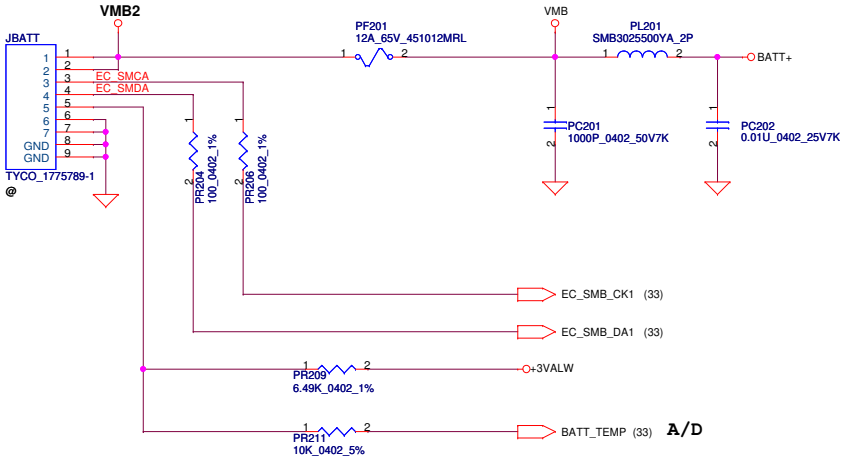
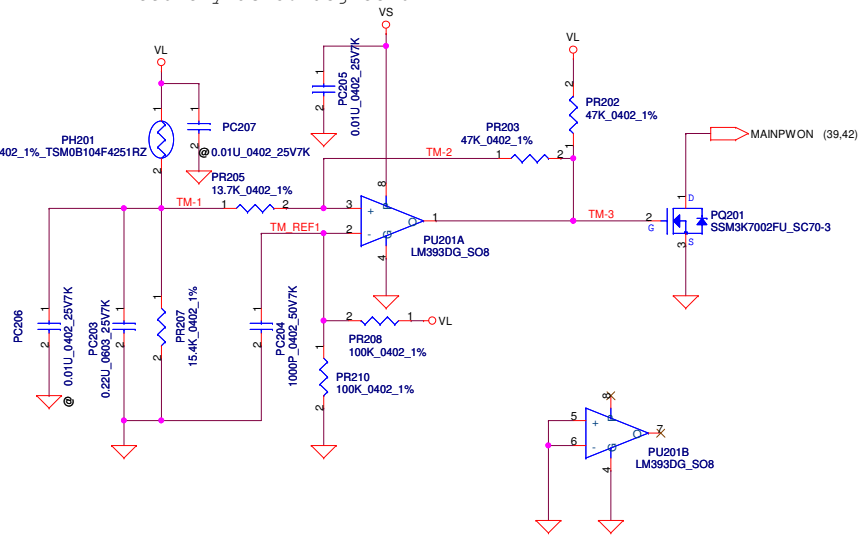
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





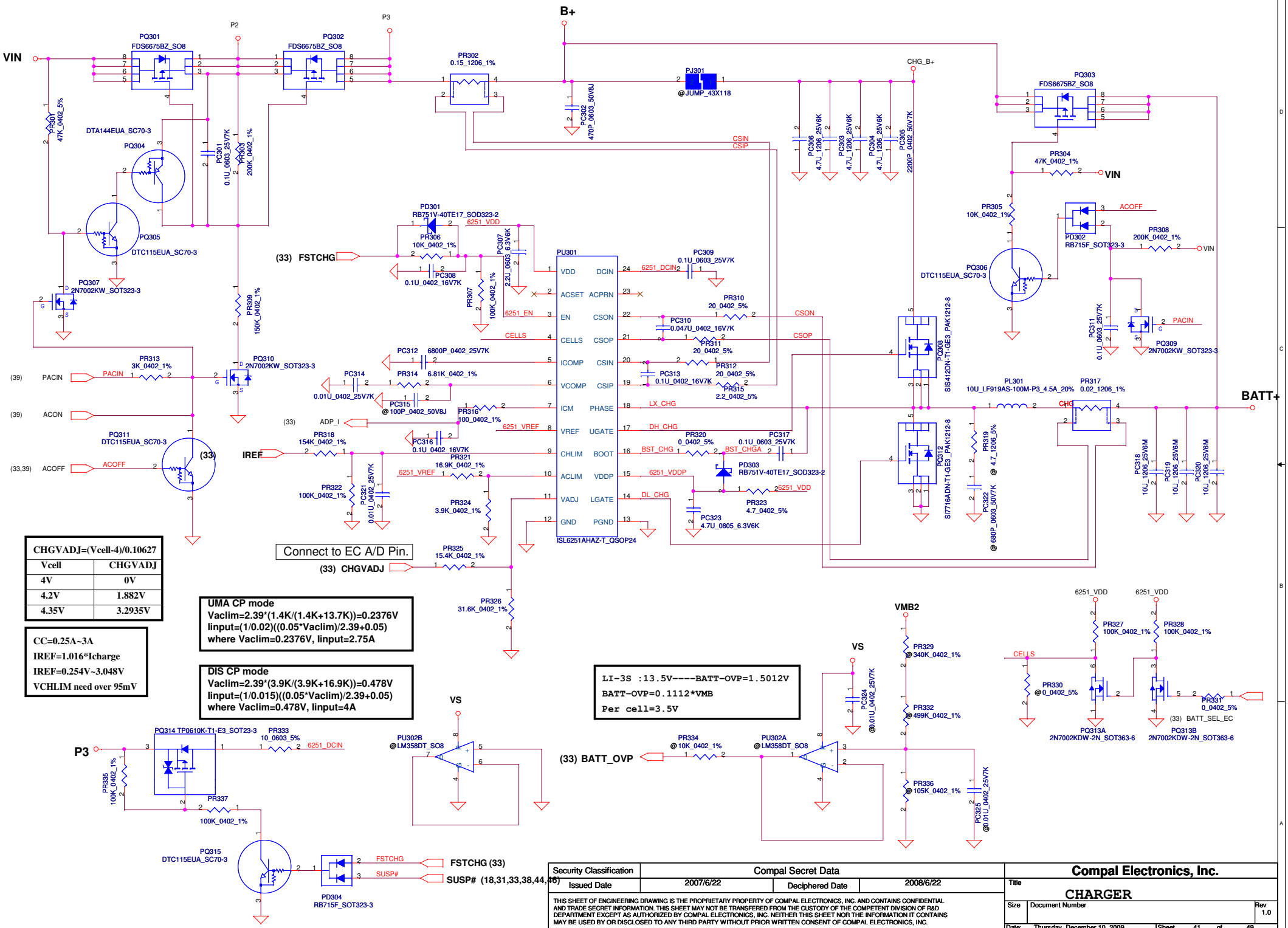
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		1.0

Date: Thursday, December 10, 2009 | Sheet 40 of 49



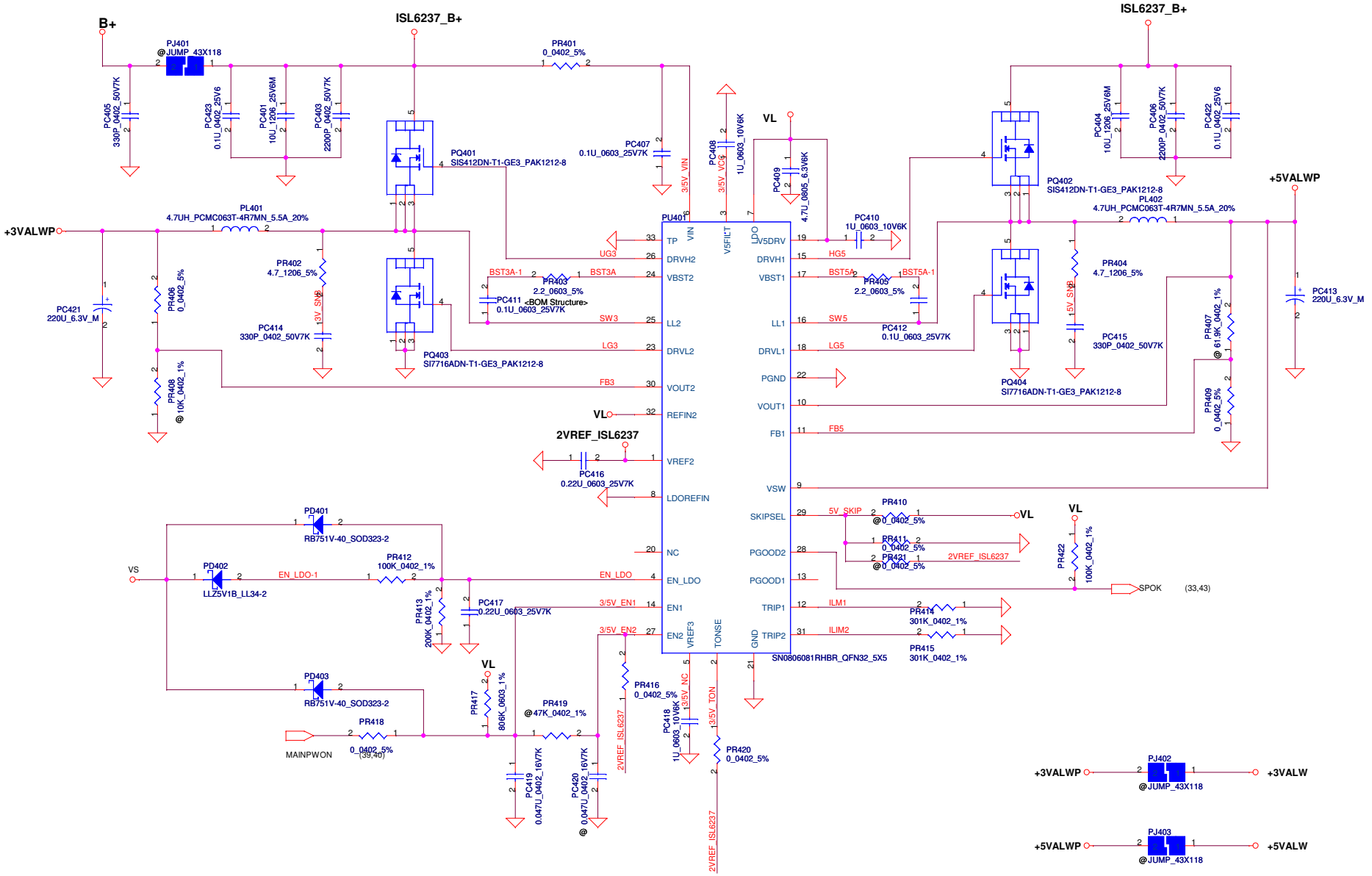
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
		1.0

Date: Thursday, December 10, 2009 | Sheet 41 of 49



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		1.0

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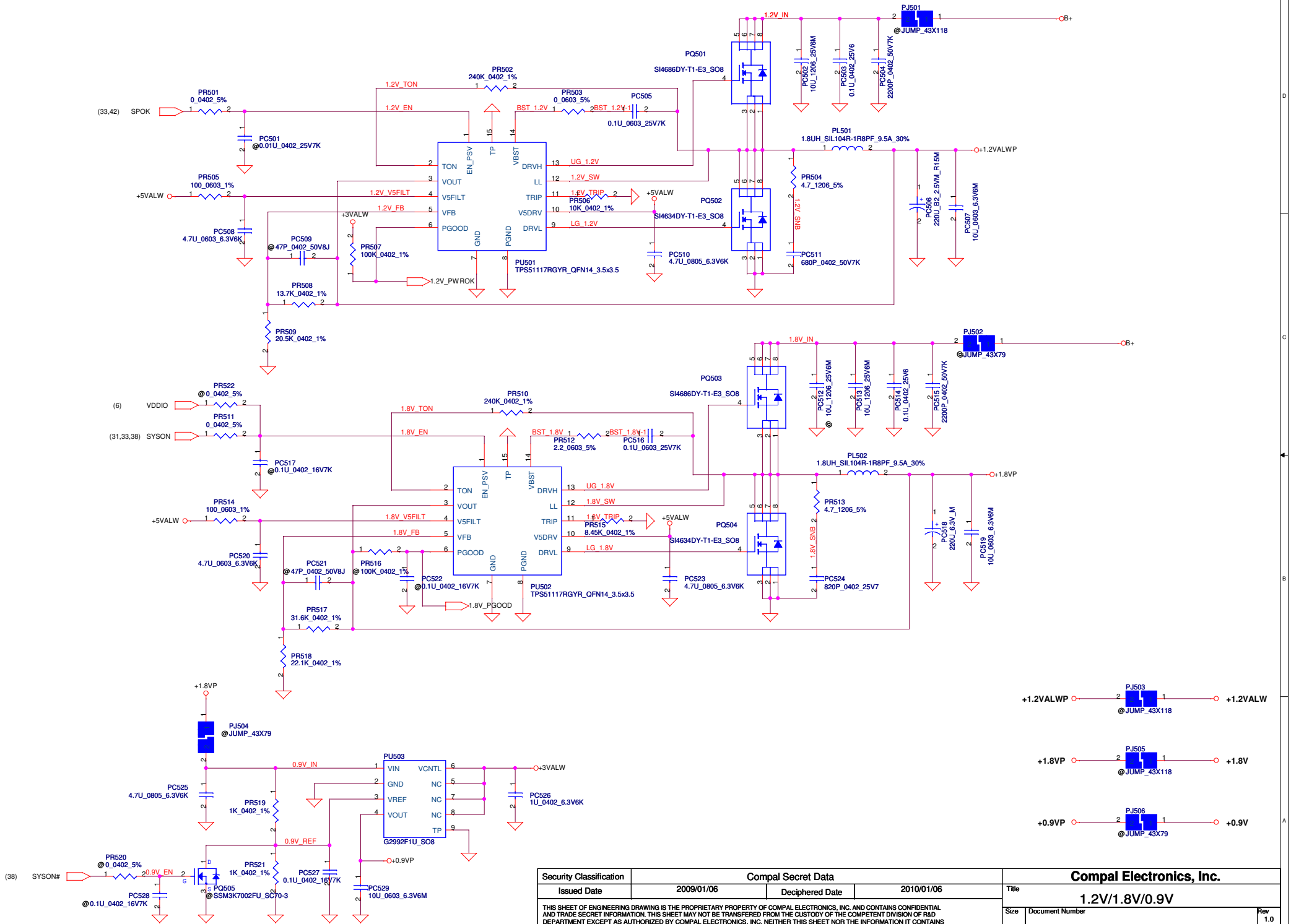


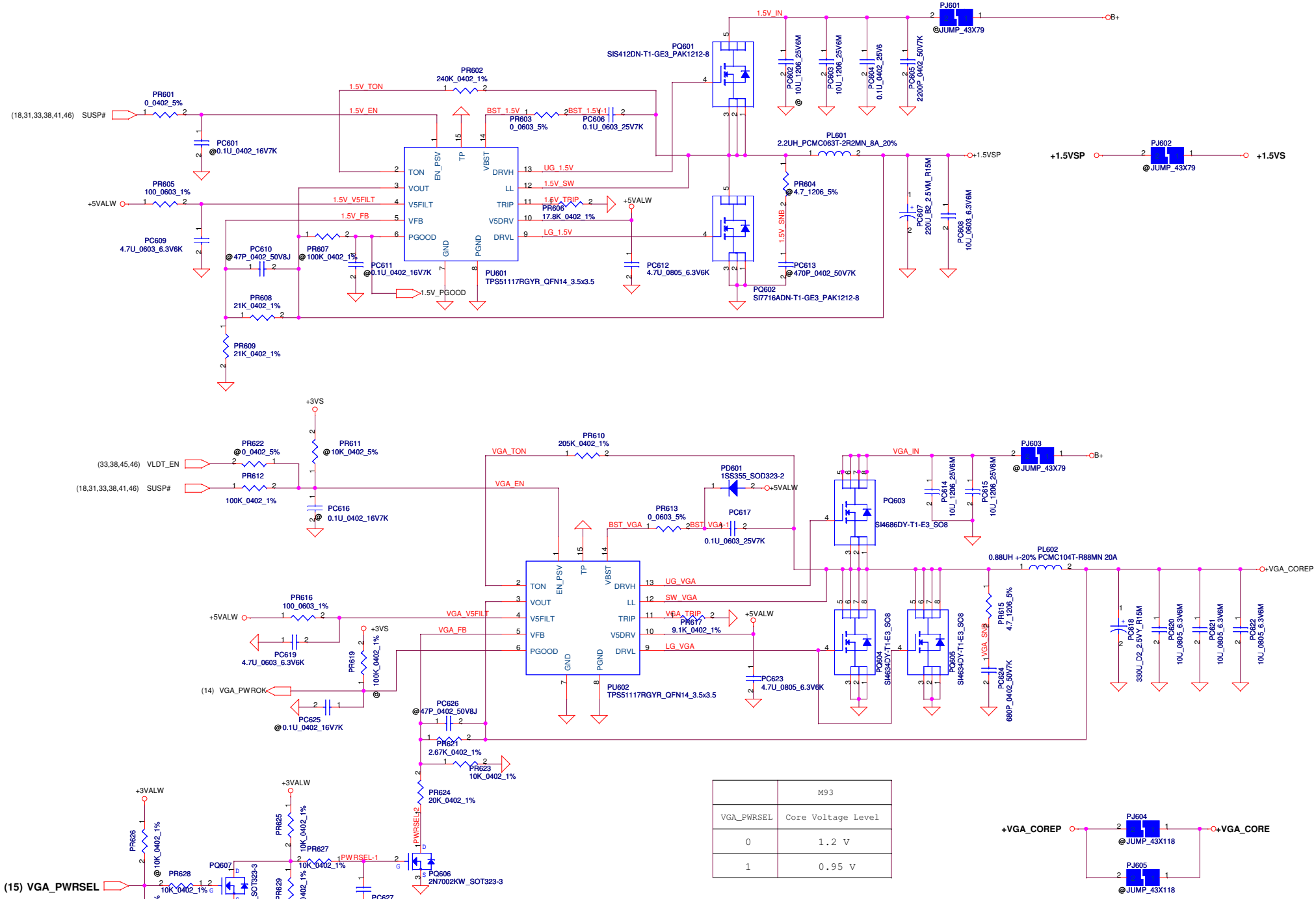
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.2V/1.8V/0.9V

Size	Document Number	Rev
		1.0

Date: Thursday, December 10, 2009 | Sheet 43 of 49



	M93
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V

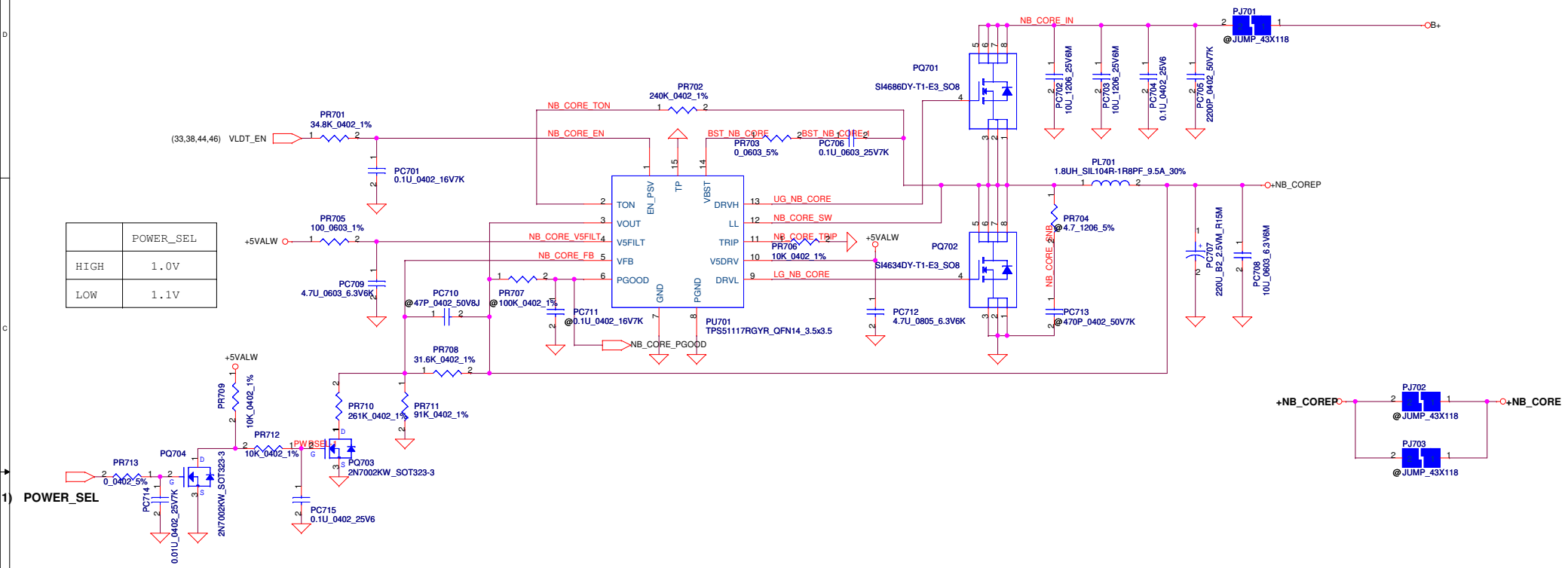
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/VGA_CORE

Size	Document Number	Rev
		1.0

Date: Thursday, December 10, 2009 | Sheet 44 of 49



Security Classification	Compal Secret Data
Issued Date	2009/01/06
Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: +NB_CORE

Size	Document Number	Rev
Custom		1.0

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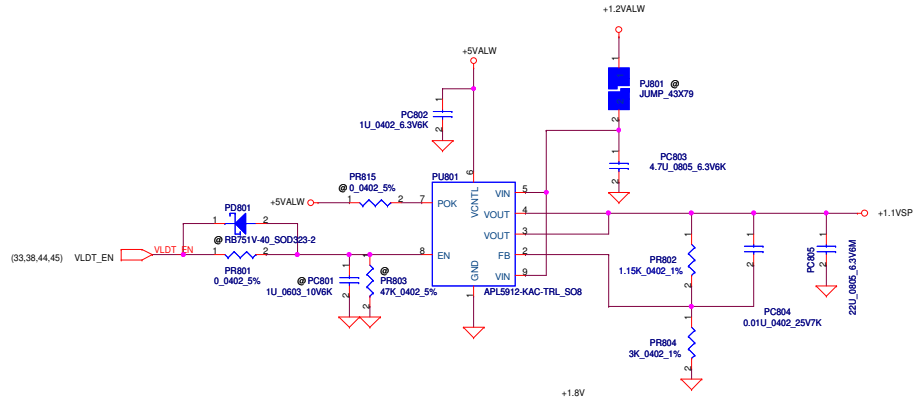
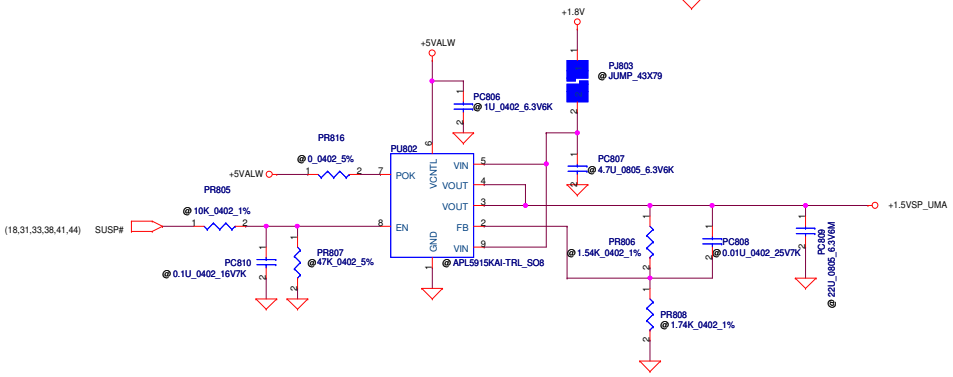
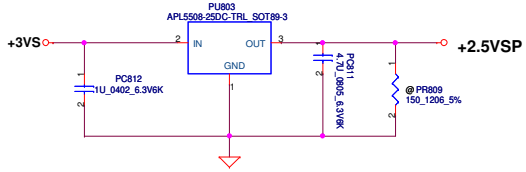
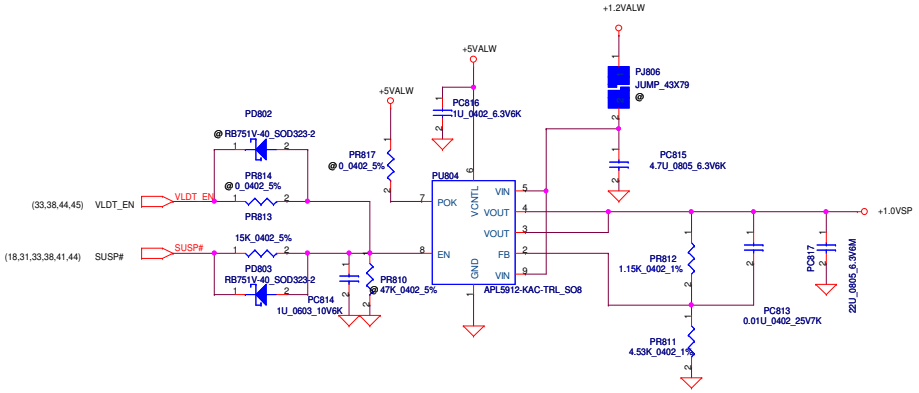
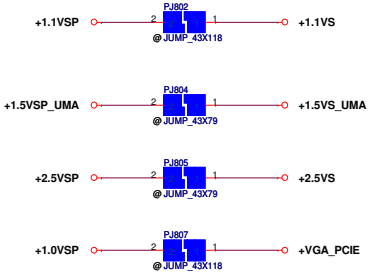










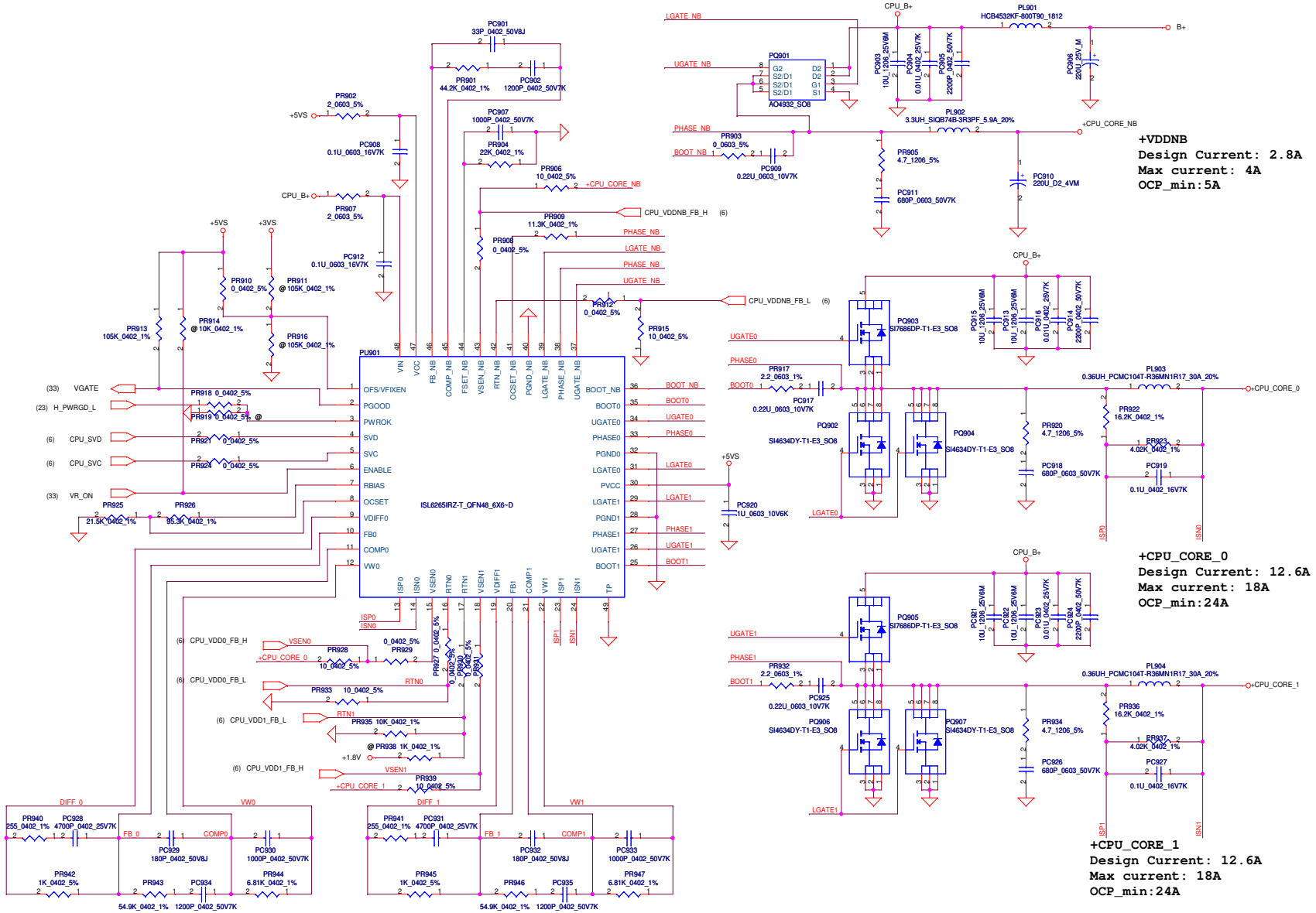
	Park	M93
VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K

Compal Electronics, Inc.

Title: 1.1V/1.5V/2.5V/1.0V

Size	Document Number	Rev
		1.0

Date: Thursday, December 10, 2009 | Sheet 46 of 49



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Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
		1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adjust power sequence for VGA_PCIE by HW request	P46	PR831=15K	2009.10.27	EVT
2	Change PC108 from 1000pF to 0.068uF for issue solution	P39	PC108=0.068uF	2009.11.17	PVT
3	Add snubber R & C and modify boost resistor for 1.8VP	P43	PR512=2.2 ohm;PR513=4.7 ohm;PC524=820pF	2009.11.17	PVT
4	Adjust power sequence	P45	PR701=34.8K,PC701=0.1uF Un-pop PR520,PQ505	2009.12.03	PVT
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: LA-5971P | Rev: 1.0

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1. change component AP2301GN to AO3413

2. remove R521, R517, R520 and R518, and reserve U49 , U50, R995, R996, R997 and R998 for experiment Vari-bright function.

3. U6.18 add a pull up resistor R1001 and pull down resistor R1002 for check ENE KB926 version.

4. reserve R999 and R1000 for Vari-bright test.

5. add J8, C1031, C1032, C1033, C1034, C1035, C1036, C1037, C1038 and C1039 for EMI request.

6. Change R583, R584, R585 and R586 Bead from SM010018110 to SM010022410.

7. reserve R1003 for EMI request.

8. Change C633, C640, C662, C948, C660 and C639 to 10pF for EMI rquest.

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: HW PIR

Size	Document Number	Rev
B	LA-5971P	1.0

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