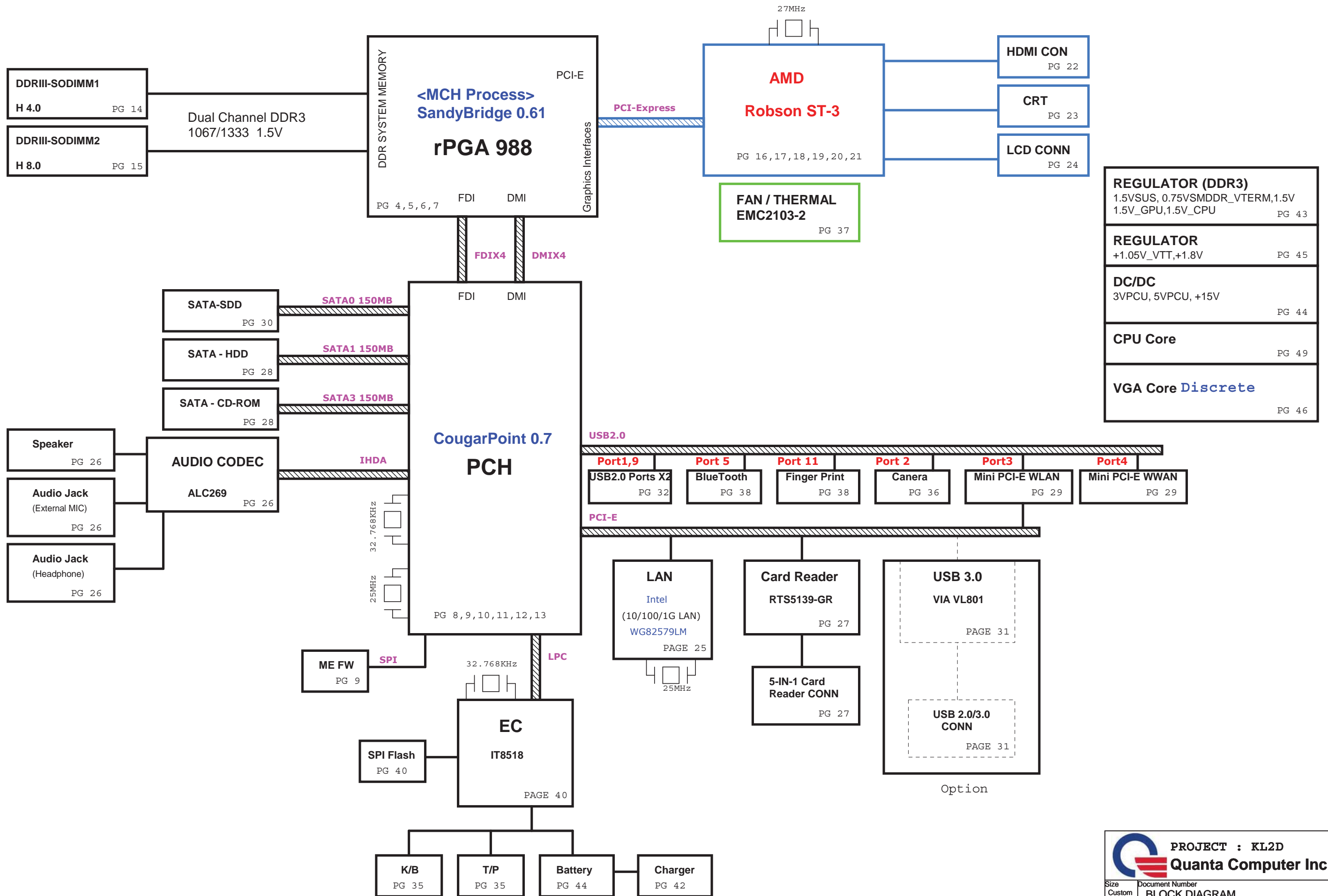
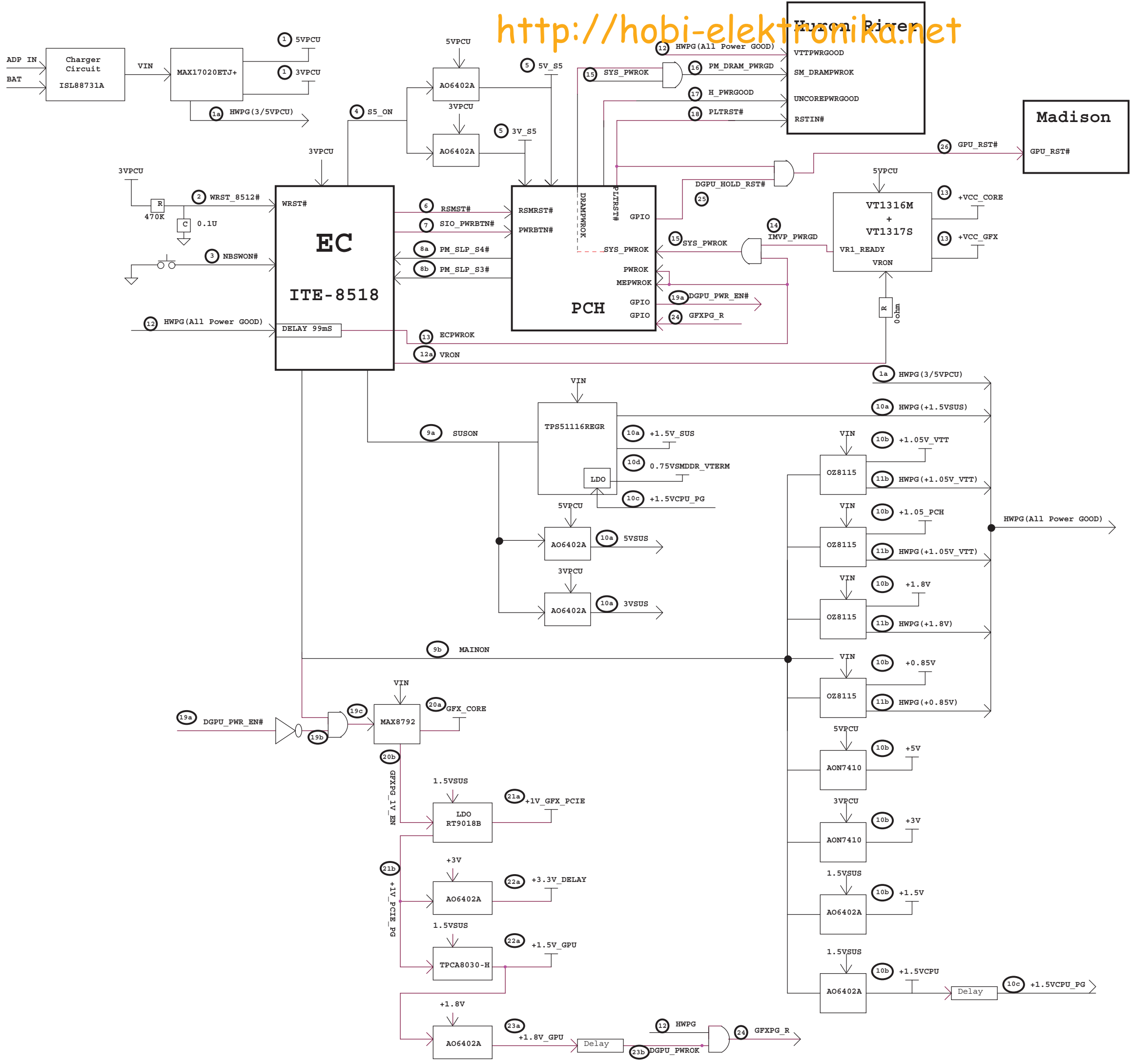


KL9A Intel Huron River Platform with AMD Discrete GFX






02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

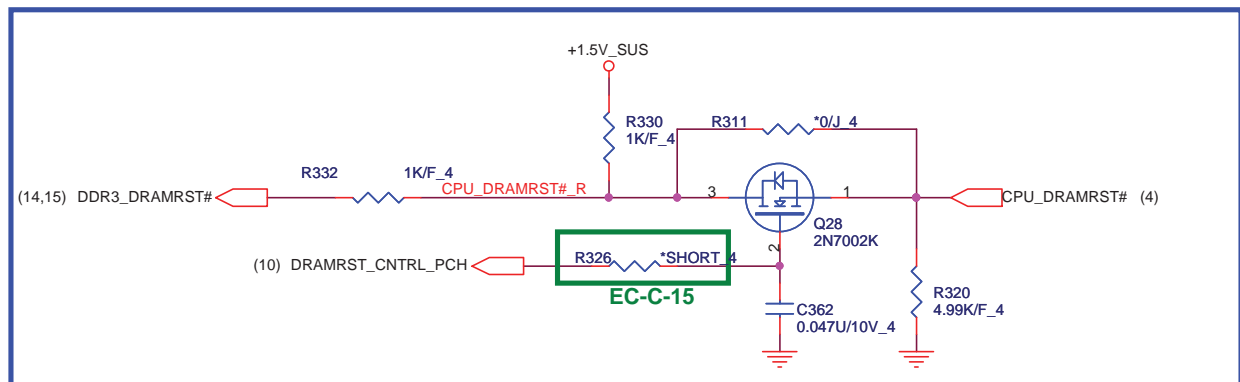
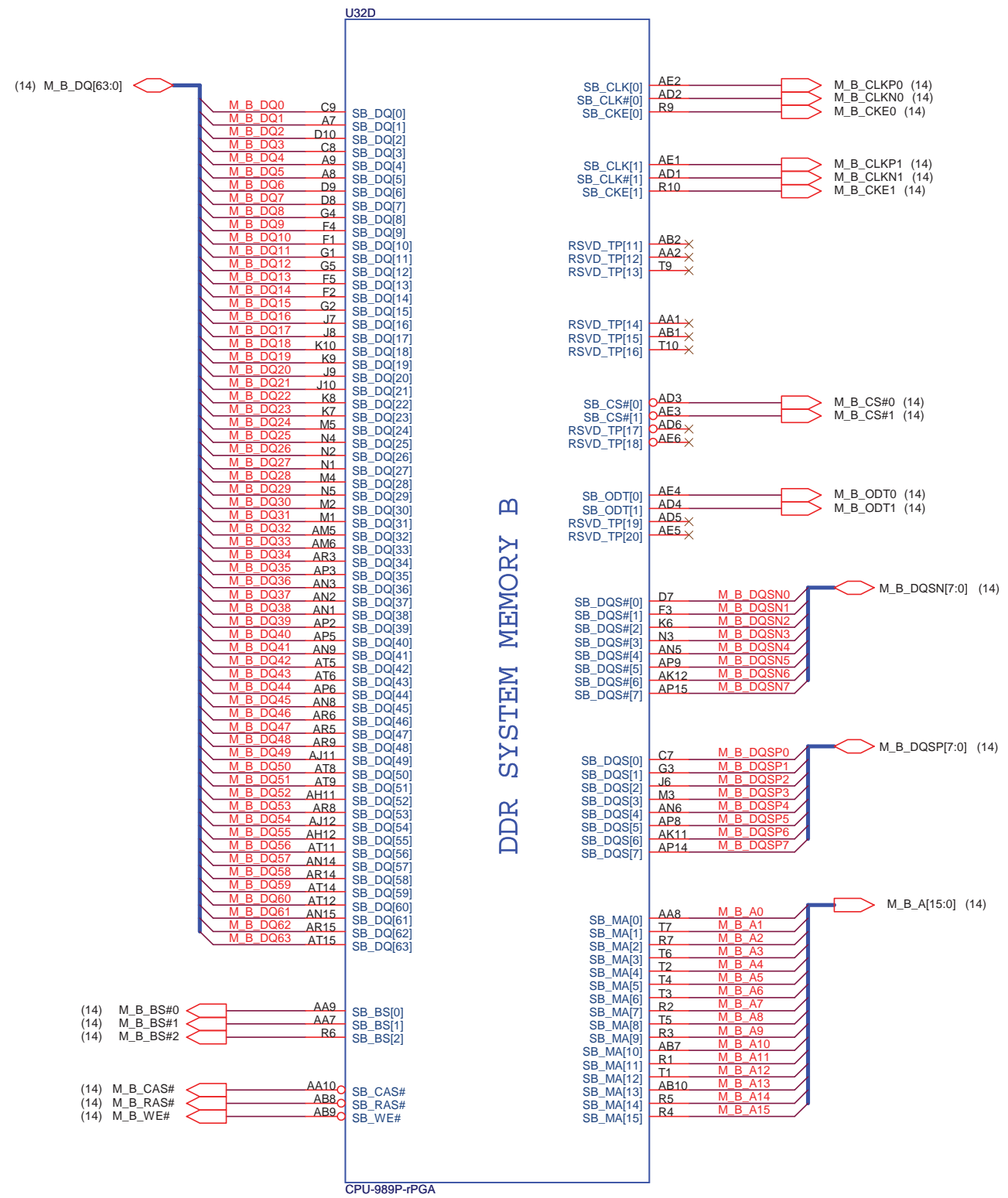
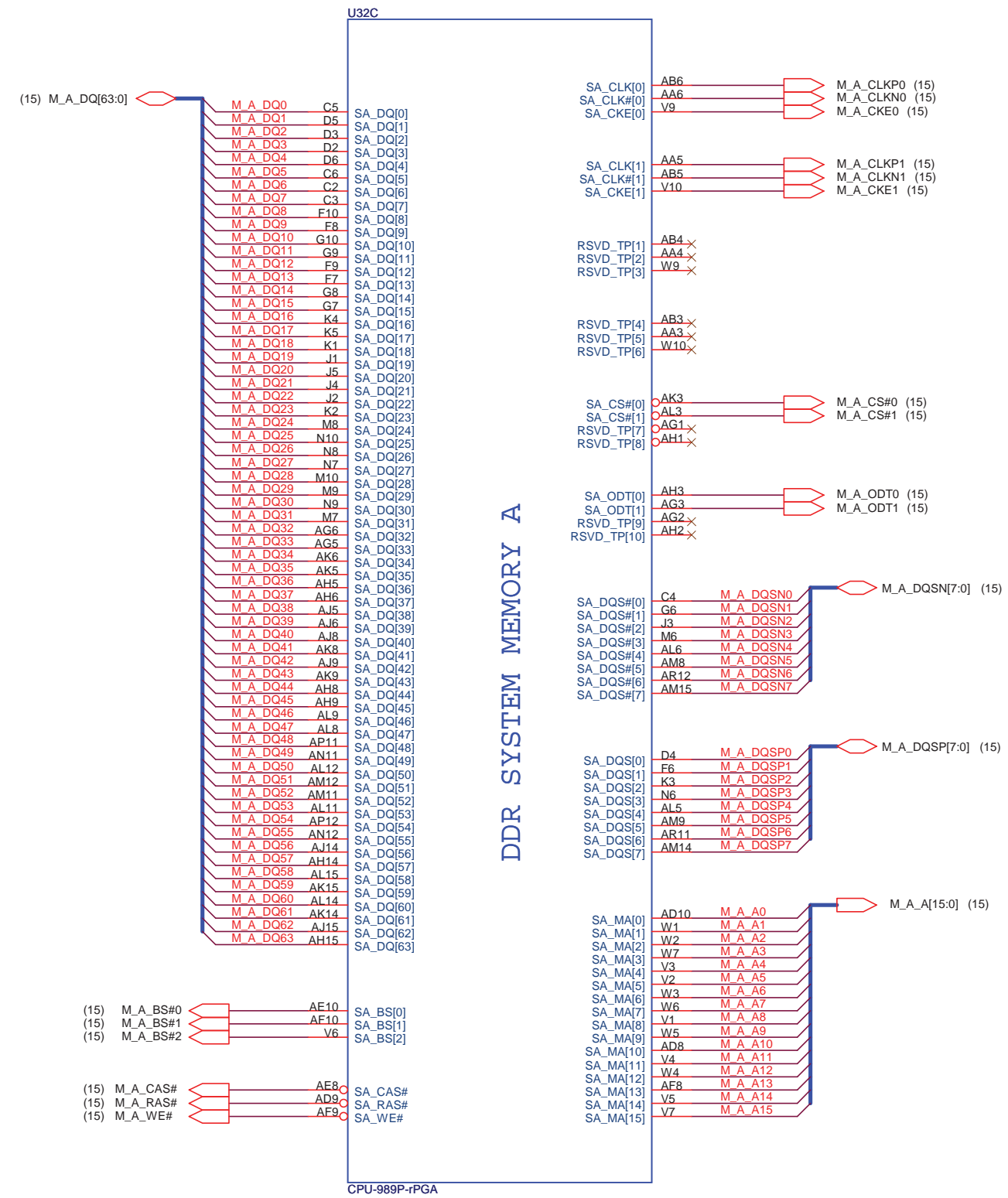
02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Clock Generator	1A
Date:	Thursday, November 04, 2010	Sheet 3 of 53

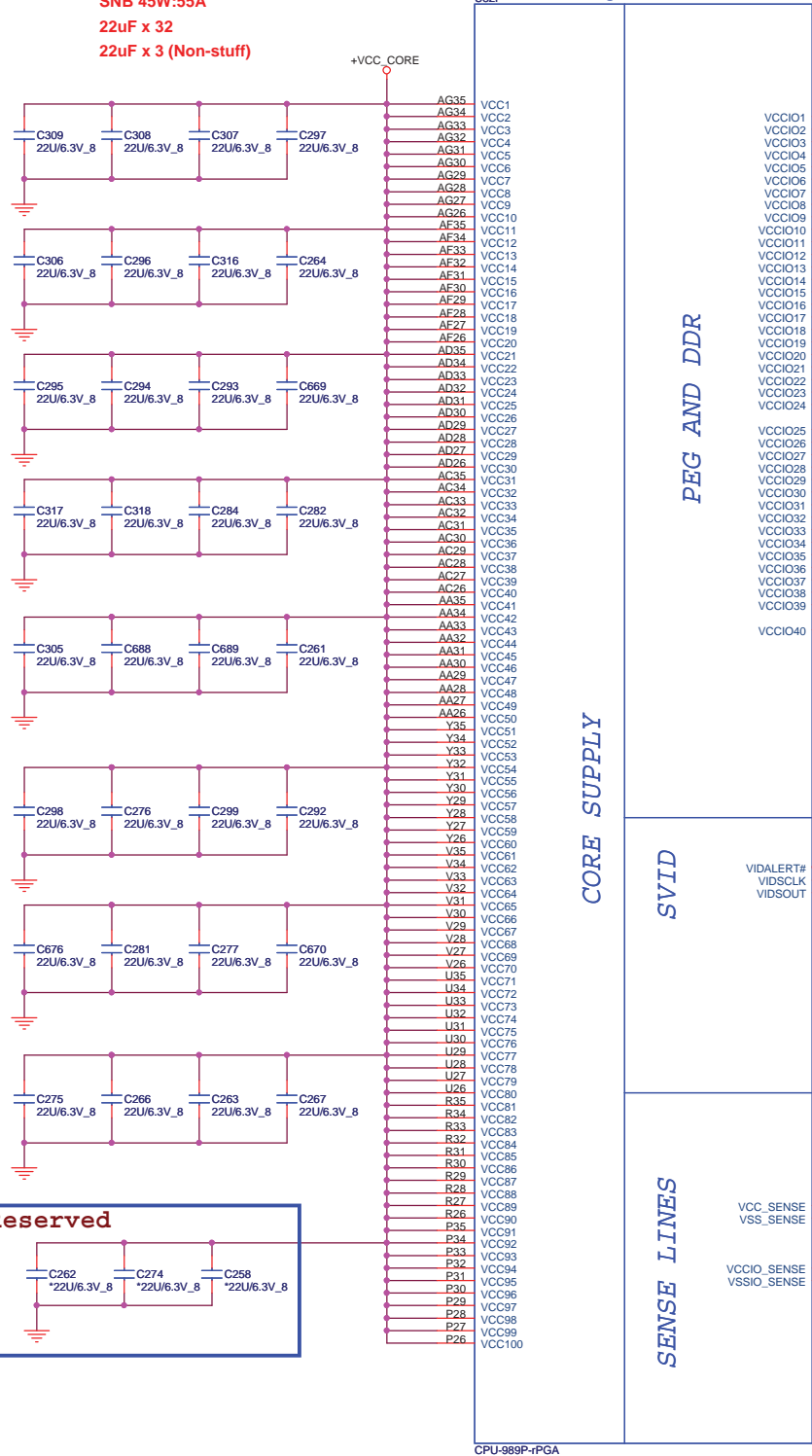


PROJECT : KL2D
Quanta Computer Inc.

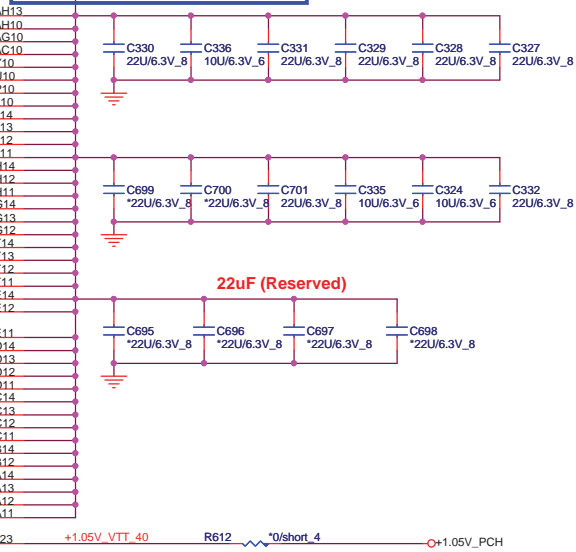
Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date:	Tuesday, January 04, 2011	Sheet 5 of 53

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

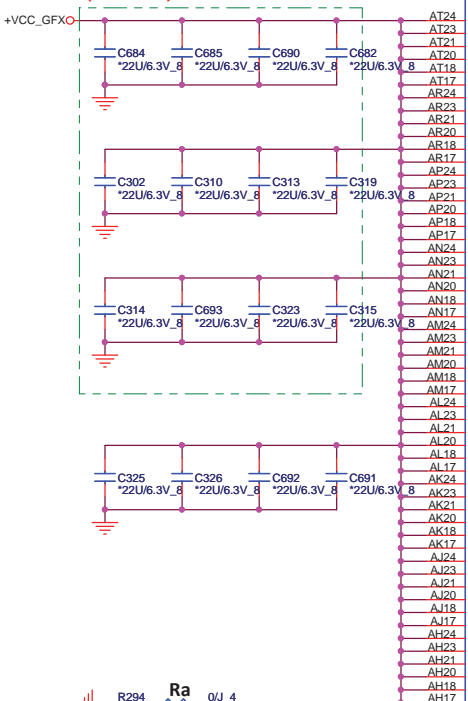
POWER



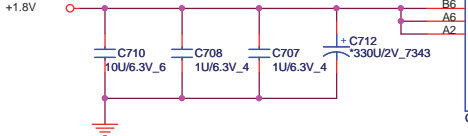
CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)



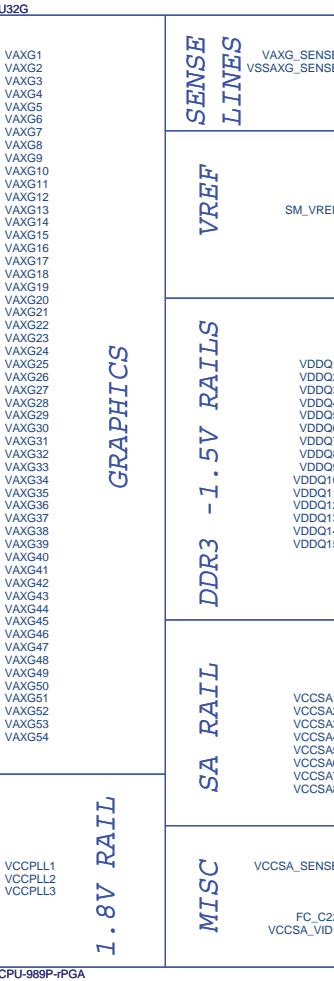
CPU VG1
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)



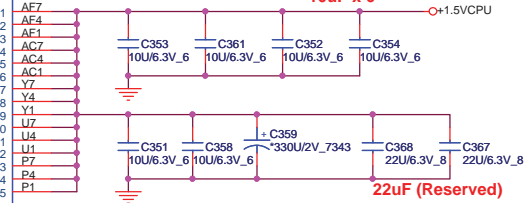
CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2



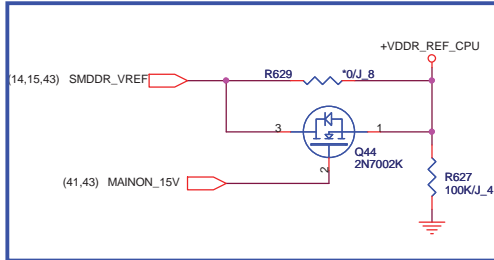
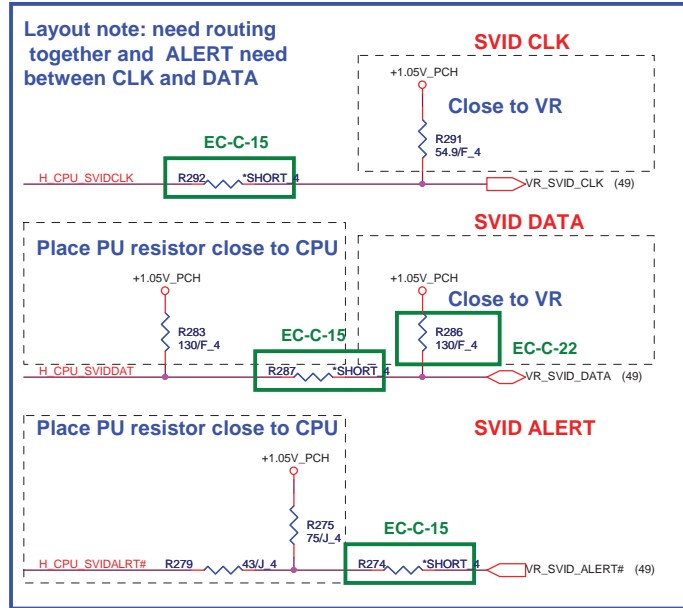
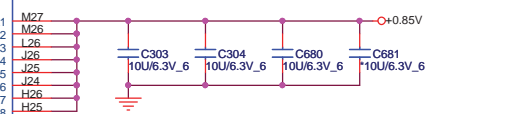
POWER



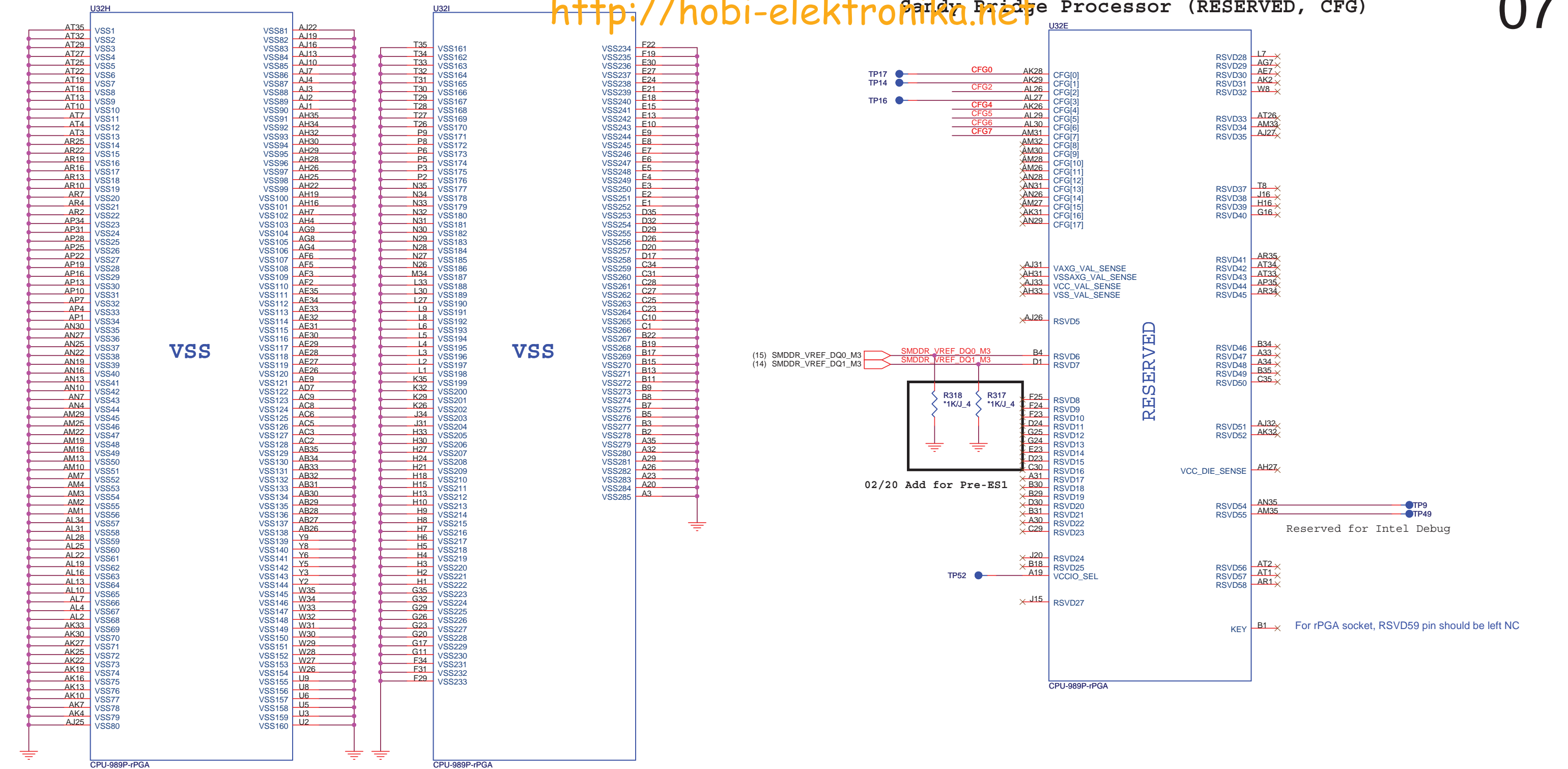
CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6



CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3



<http://hobi-elektronika.net>



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

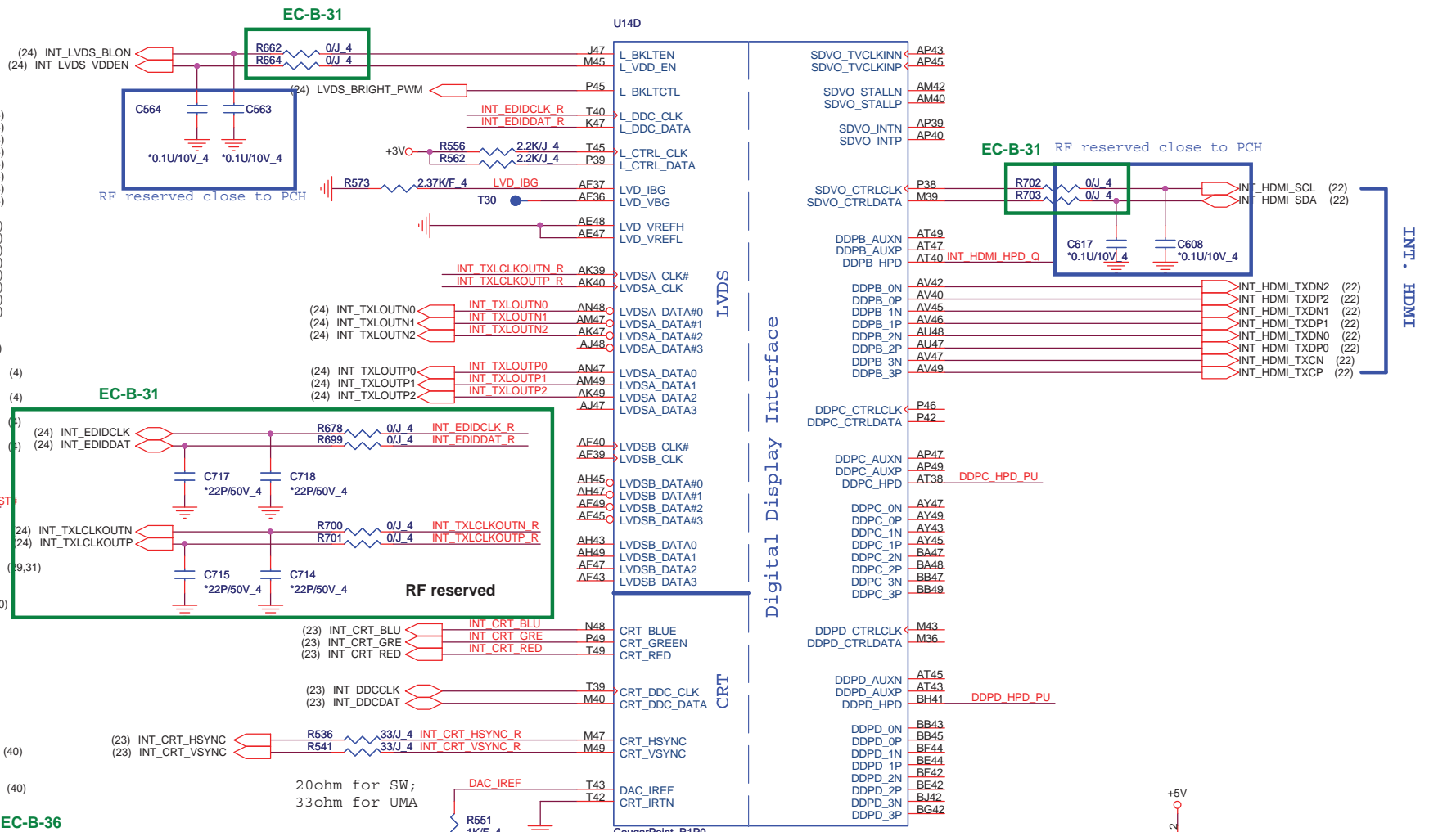
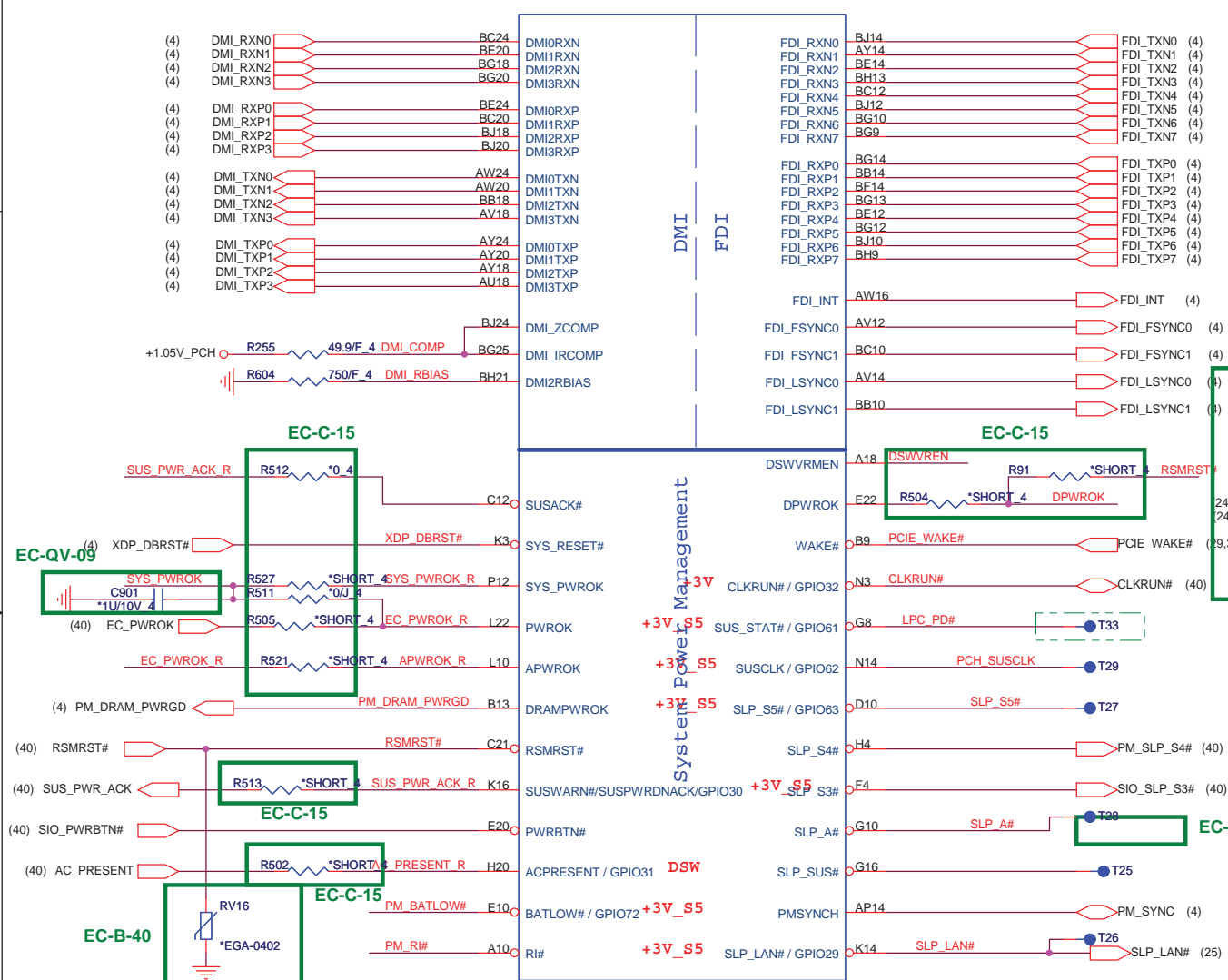
PROJECT : KL2D
Quanta Computer Inc.

Size Document Number Rev 1A
Sandy Bridge 4/4

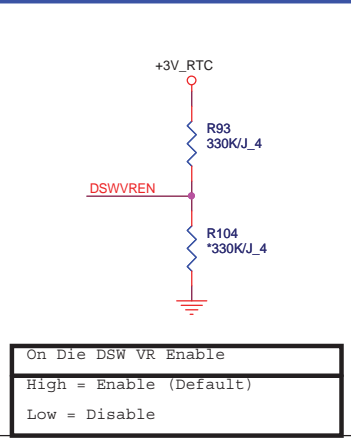
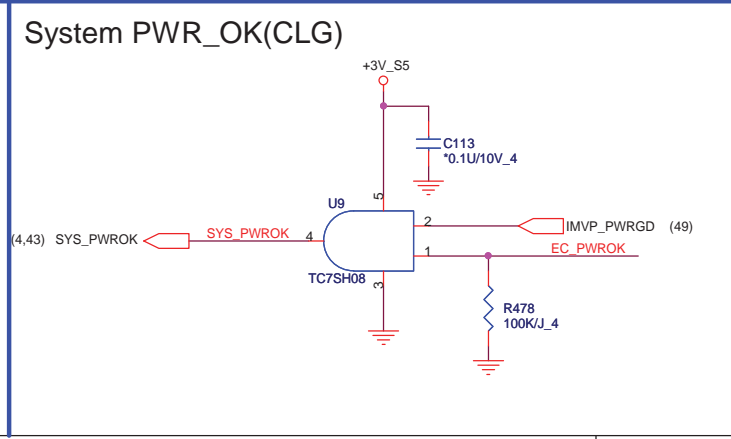
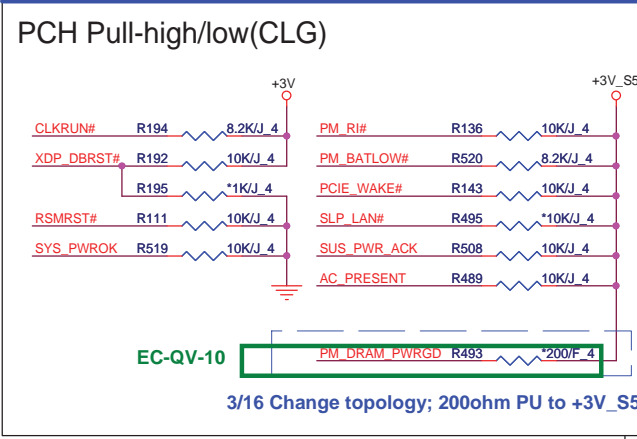
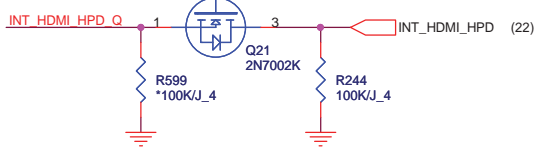
Date: Tuesday, January 04, 2011 Sheet 7 of 53

Cougar Point (DMI, FDI, PM)

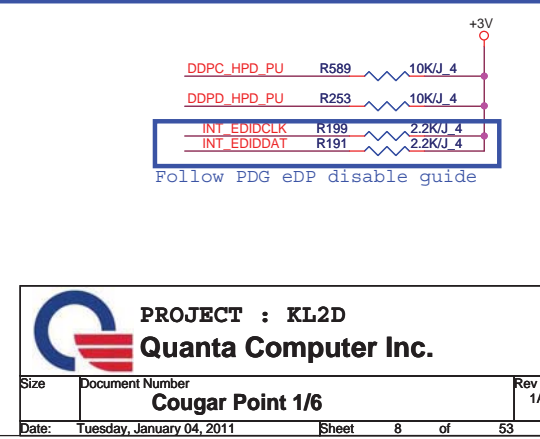
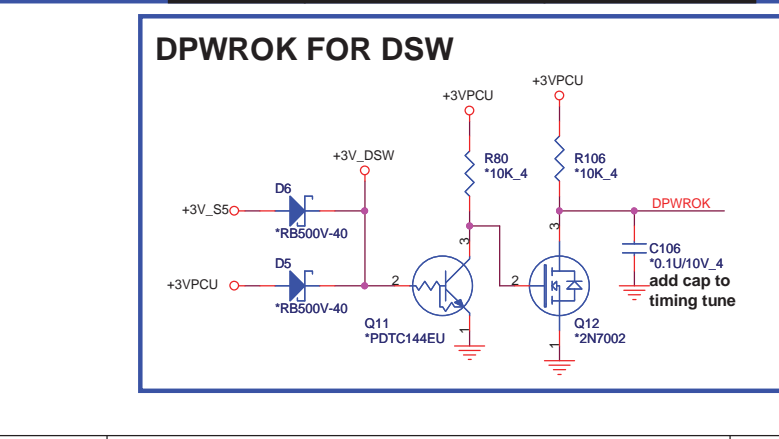
U14C

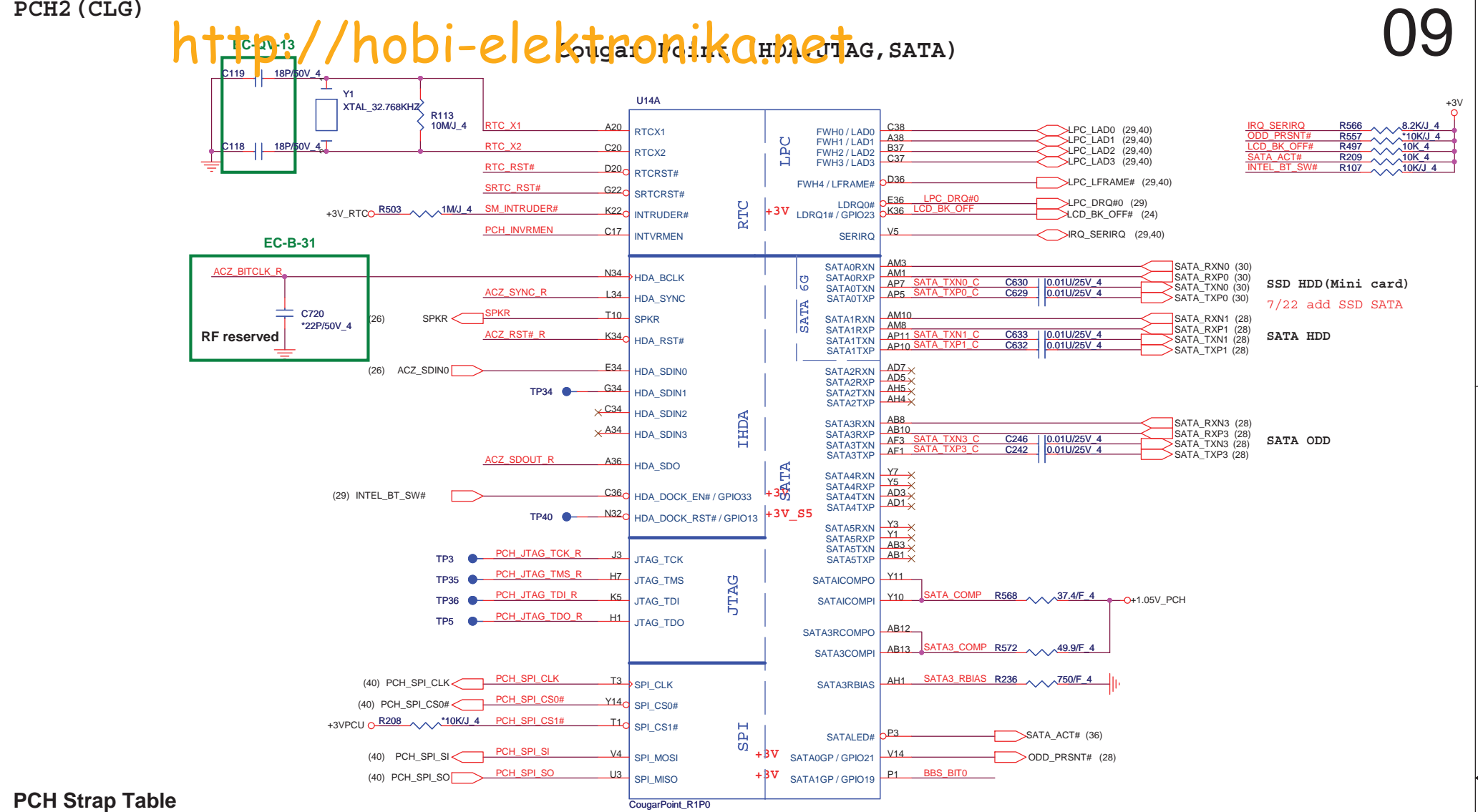
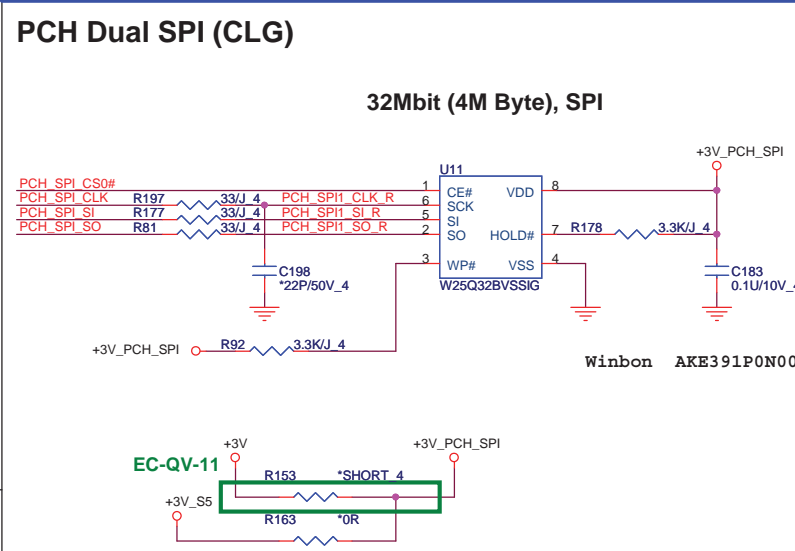
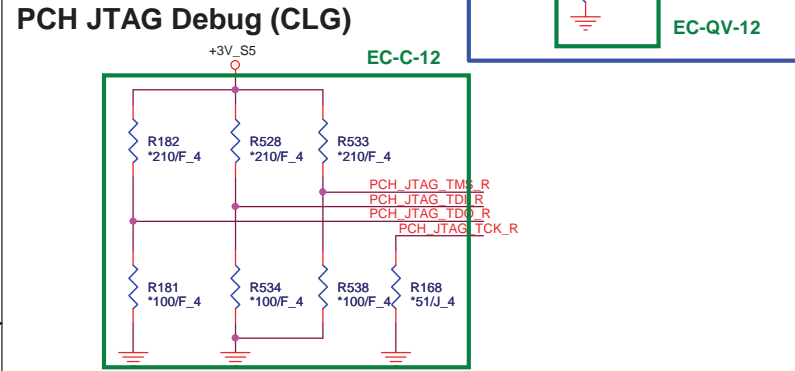
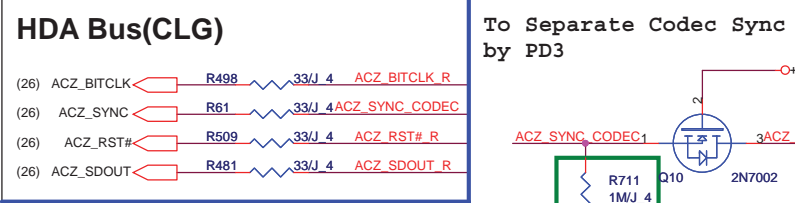
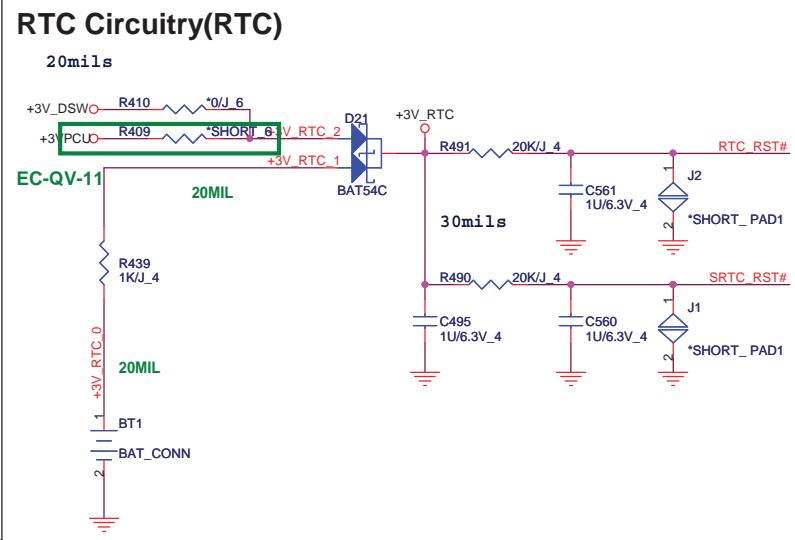


Deep sleep option	Support	Not support
SUS_PWR_ACK	To PCH SUSACK# (Pop R597)	EC or NC (Non-pop R597)
DPWROK	DSWPWRGD (Pop Q54, R663, Q55, R677)	RSMRST (Pop R639)
SLP_SUS	EC	NC

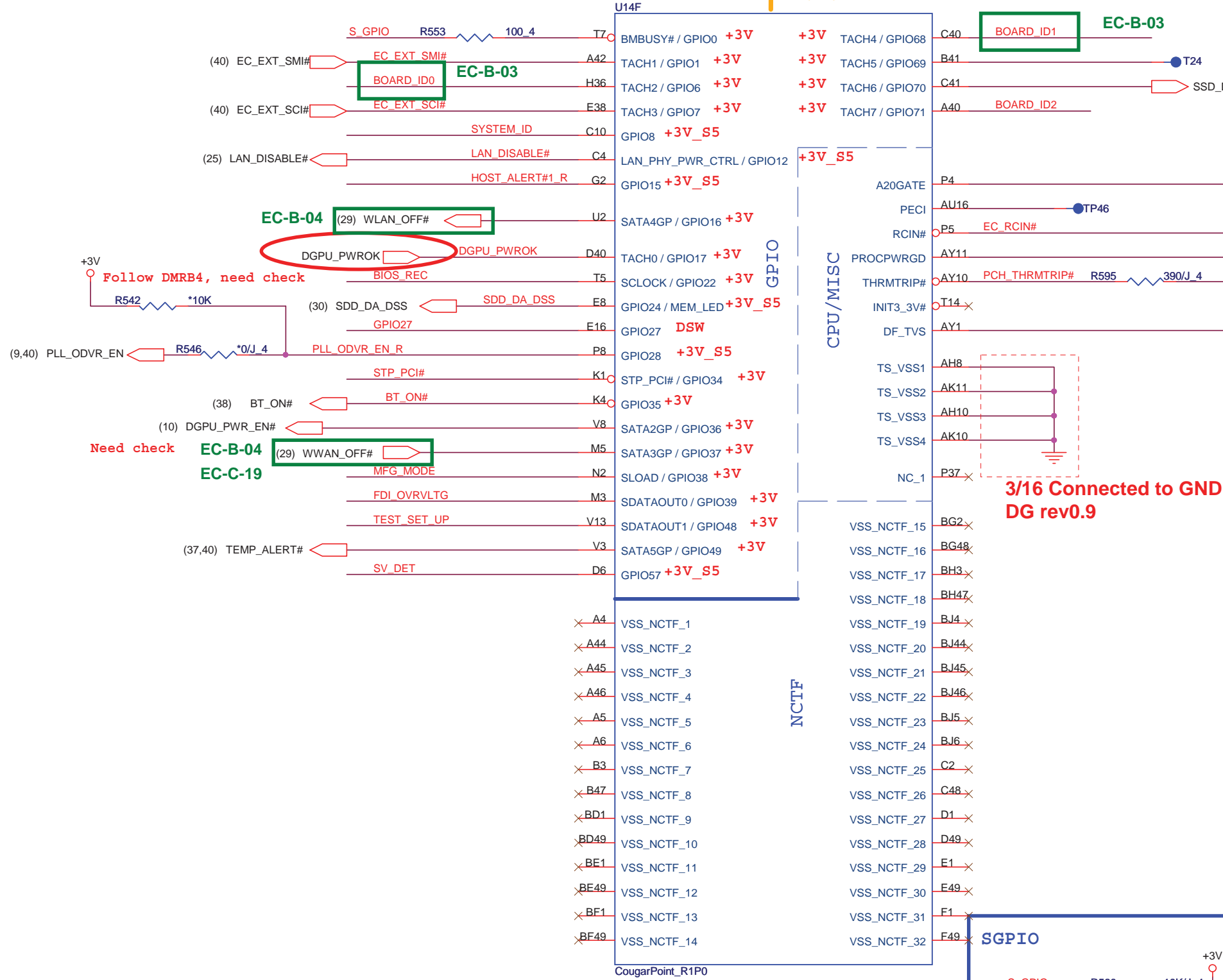


On Die DSW VR Enable
High = Enable (Default)
Low = Disable

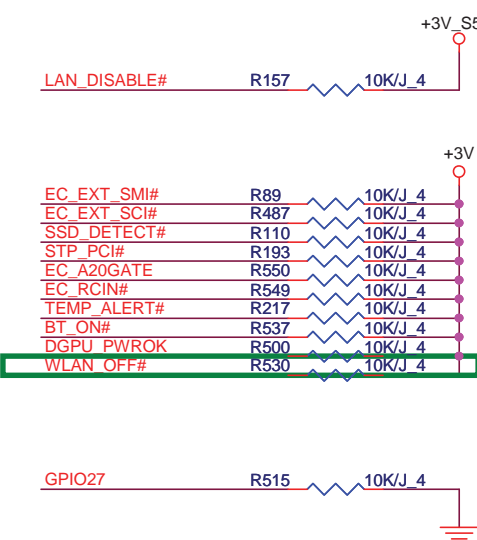




PCH Strap Table

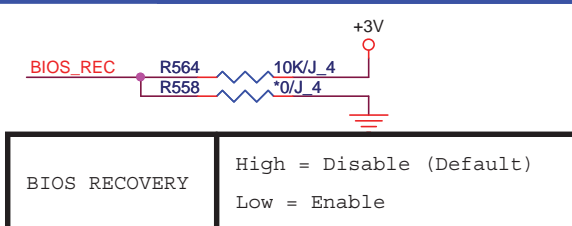
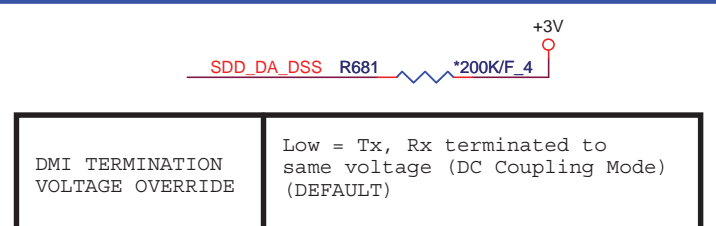
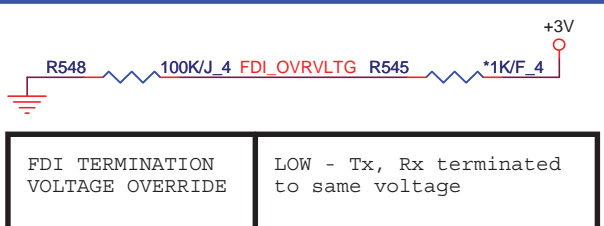
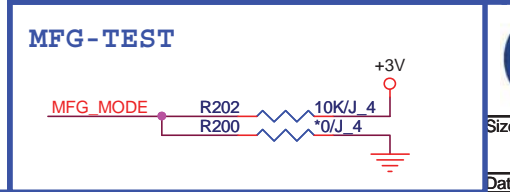
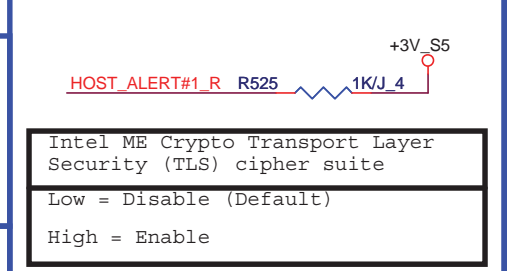
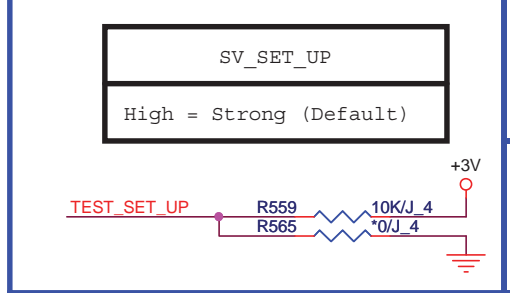
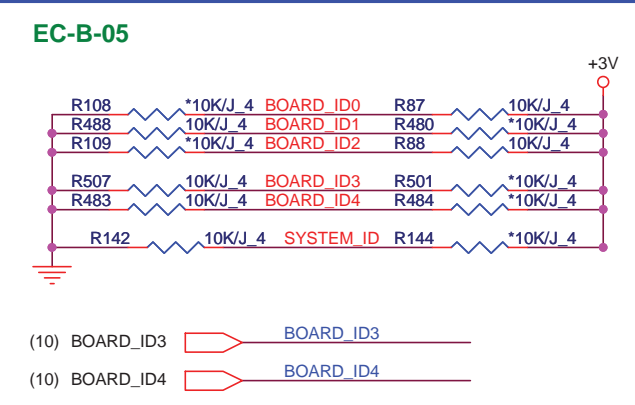


GPIO Pull-up/Pull-down(CLG)



3/16 Connected to GND
DG rev0.9

	GPIO71	GPIO68	GPIO6
	BOARD_ID2	BOARD_ID1	BOARD_ID0
KL7	0	0	0
KL8	0	1	0
KL9	1	0	0
KL8A	0	1	1
KL9A	1	0	1

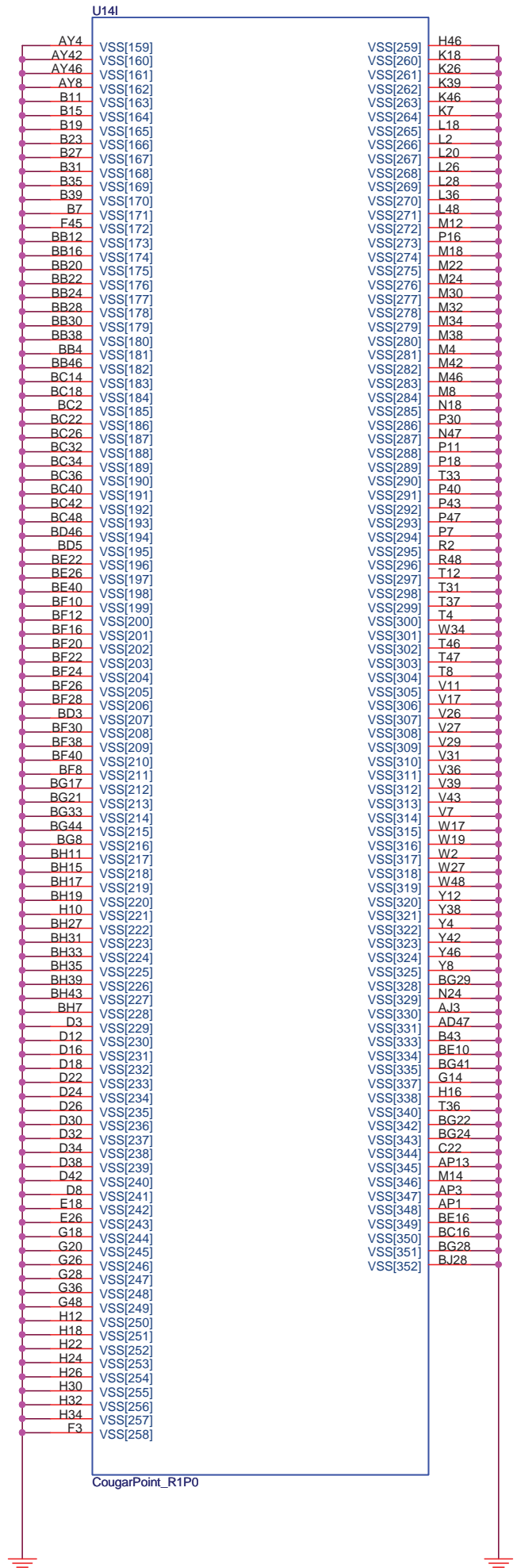
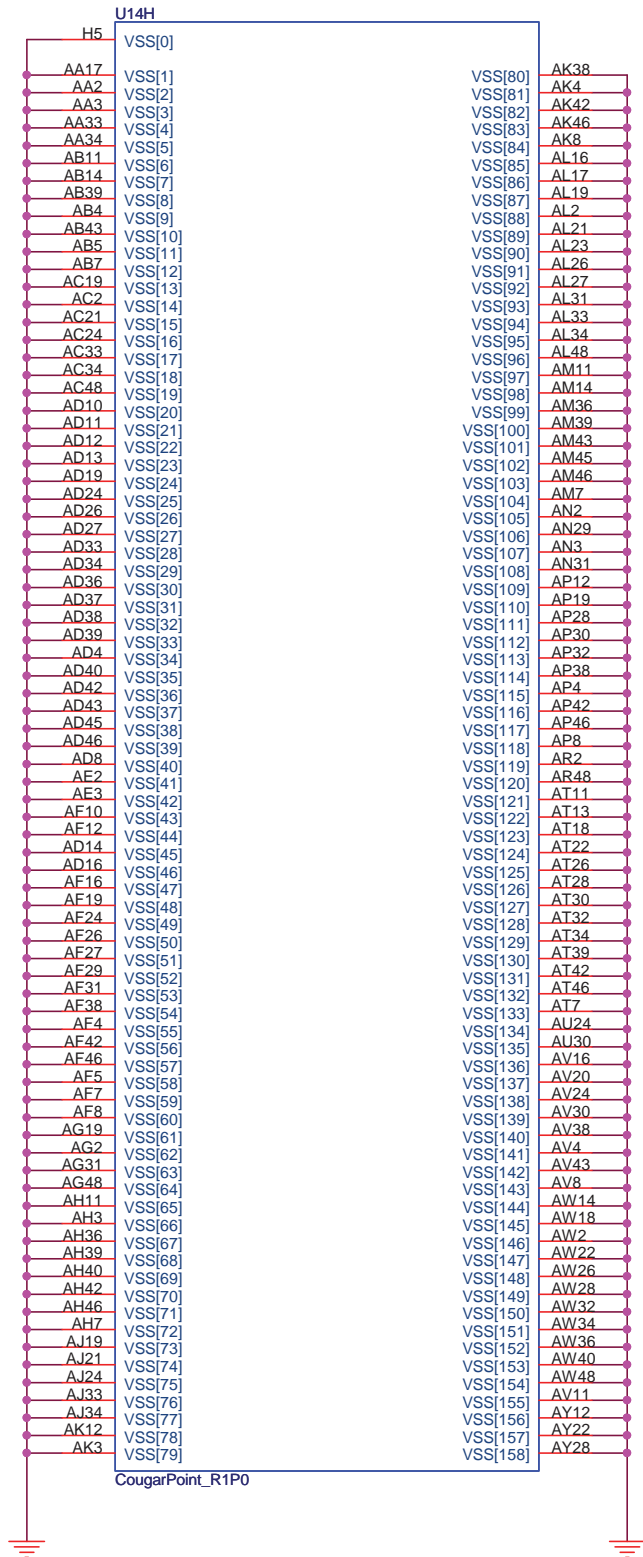


PROJECT : KL2D
Quanta Computer Inc.

Size: Document Number
Cougar Point 4/6
Rev 1A

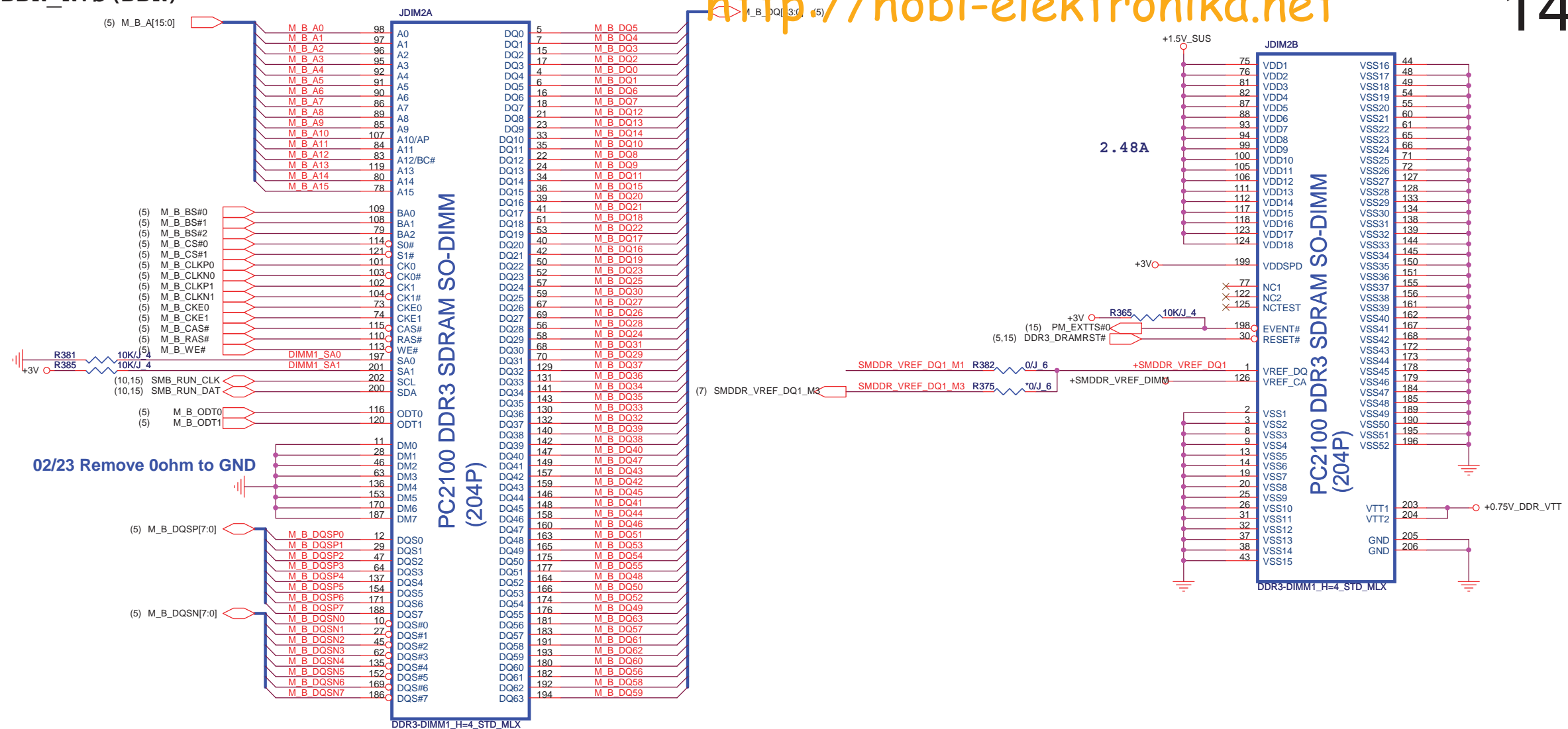
Date: Tuesday, January 04, 2011 Sheet 11 of 53

IBEX PEAK-M (GND)



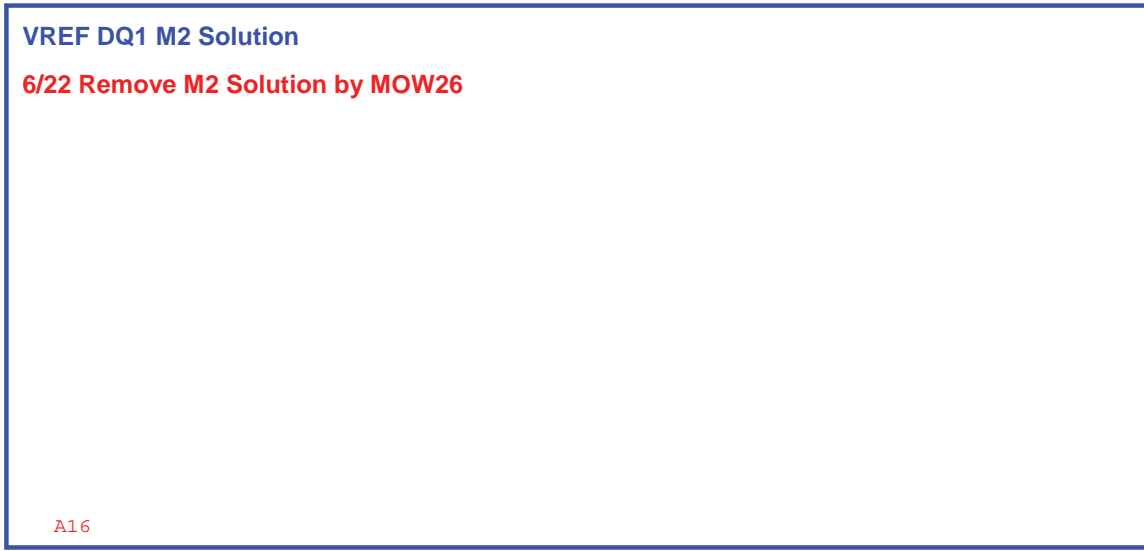
PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 6/6	1A
Date:	Thursday, November 04, 2010	Sheet 13 of 53

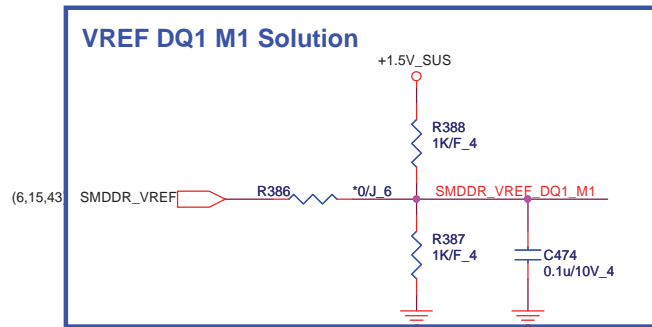
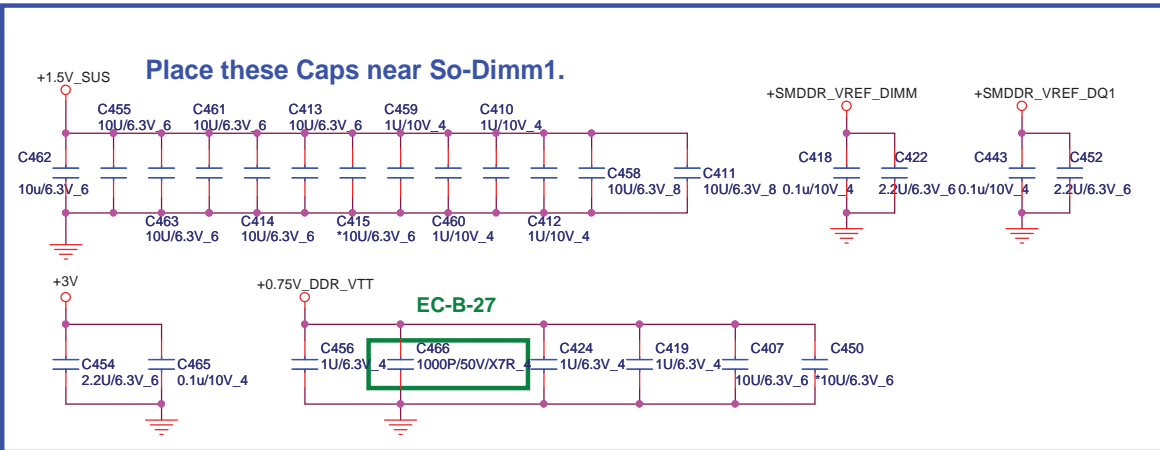


02/23 Remove 0ohm to GND

2.48A



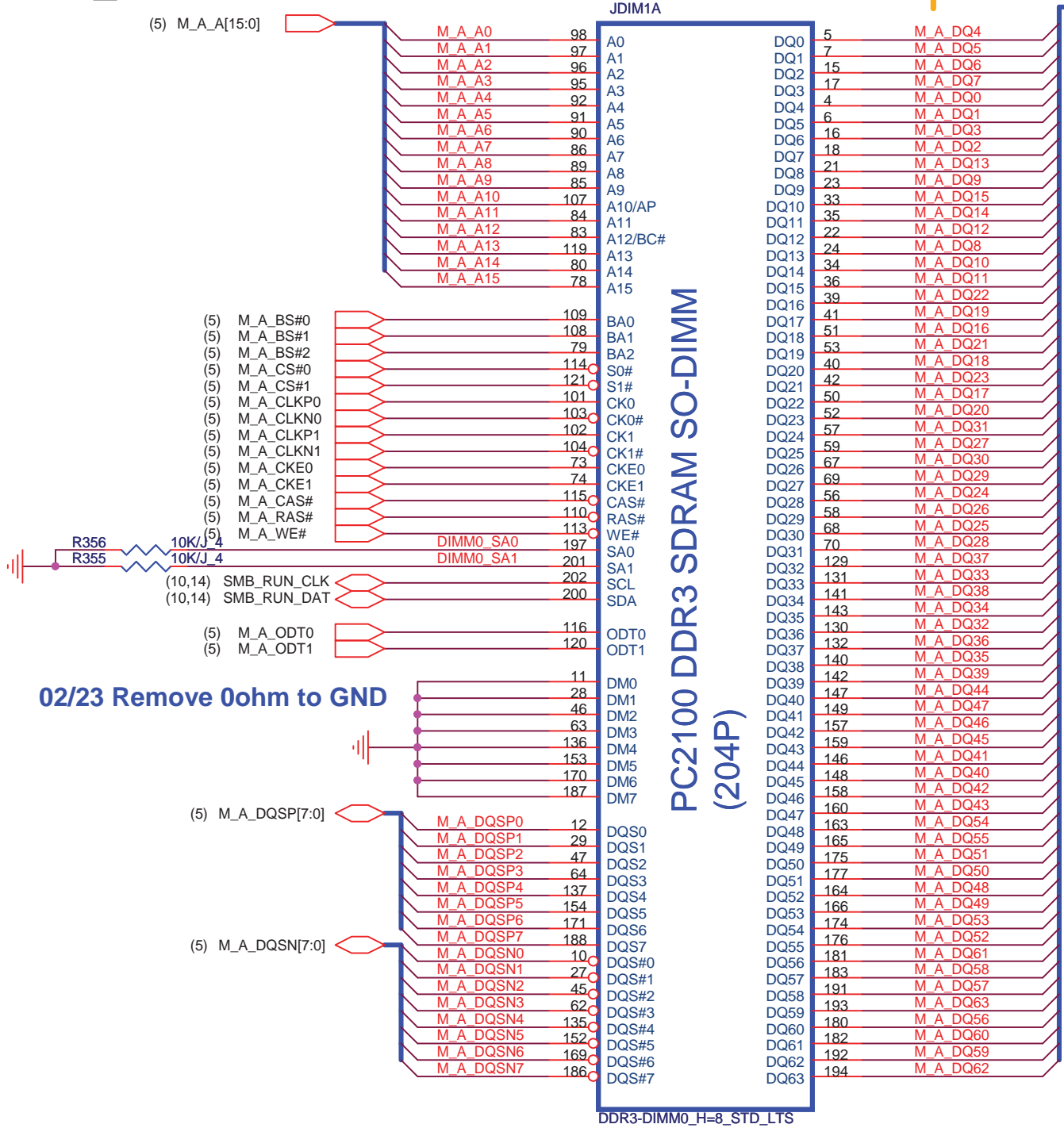
A16



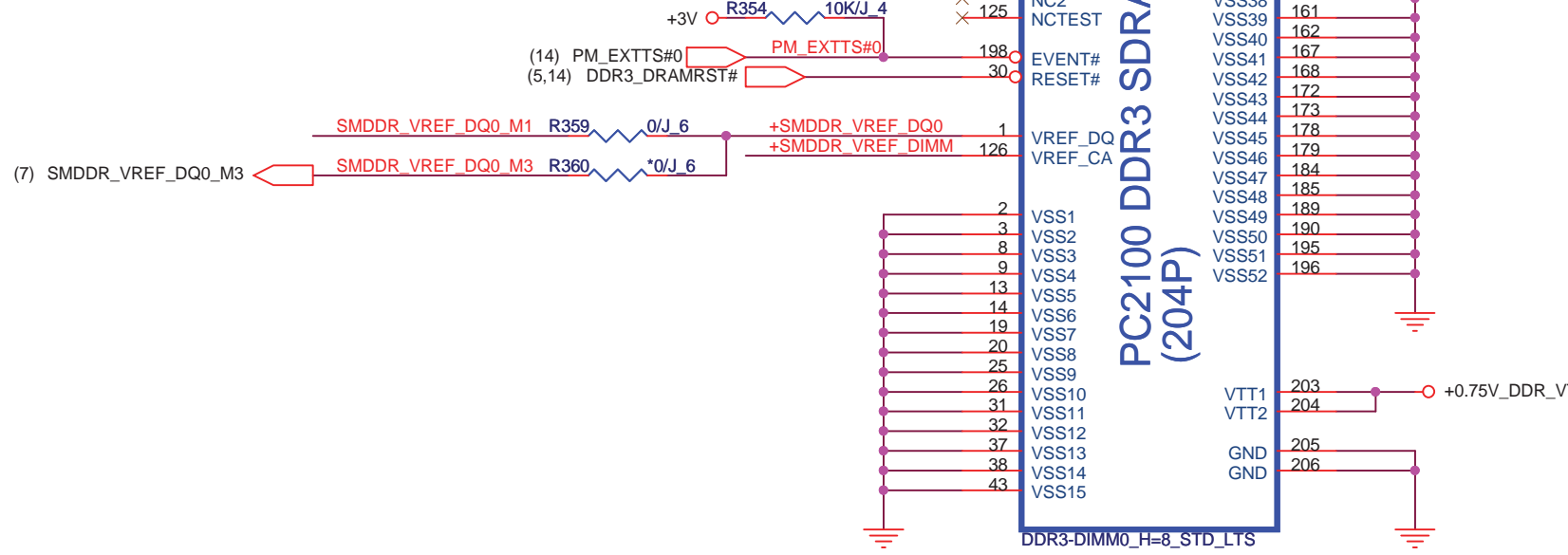
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

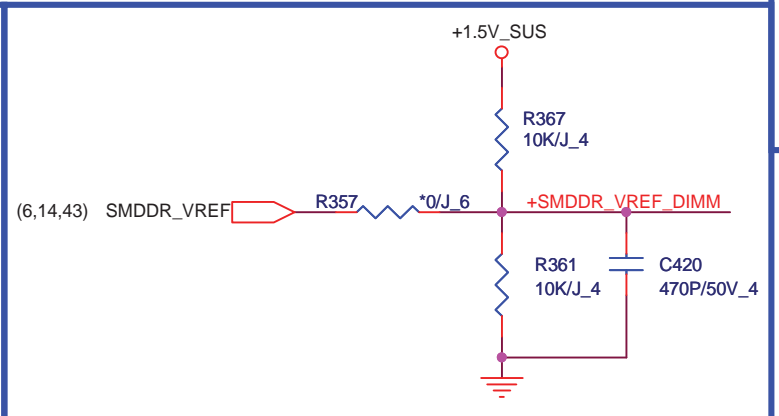
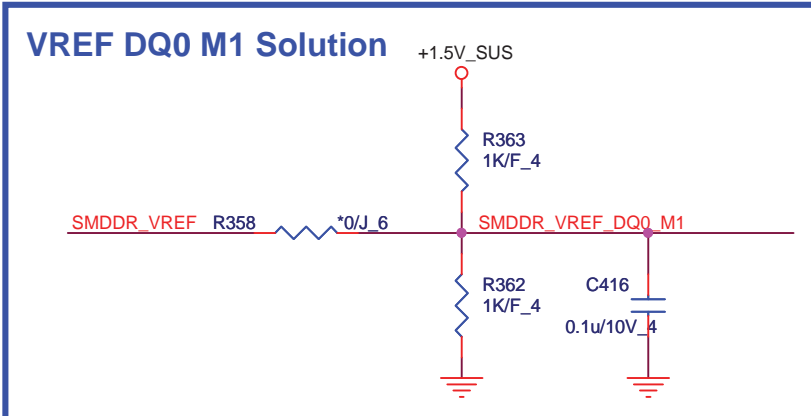
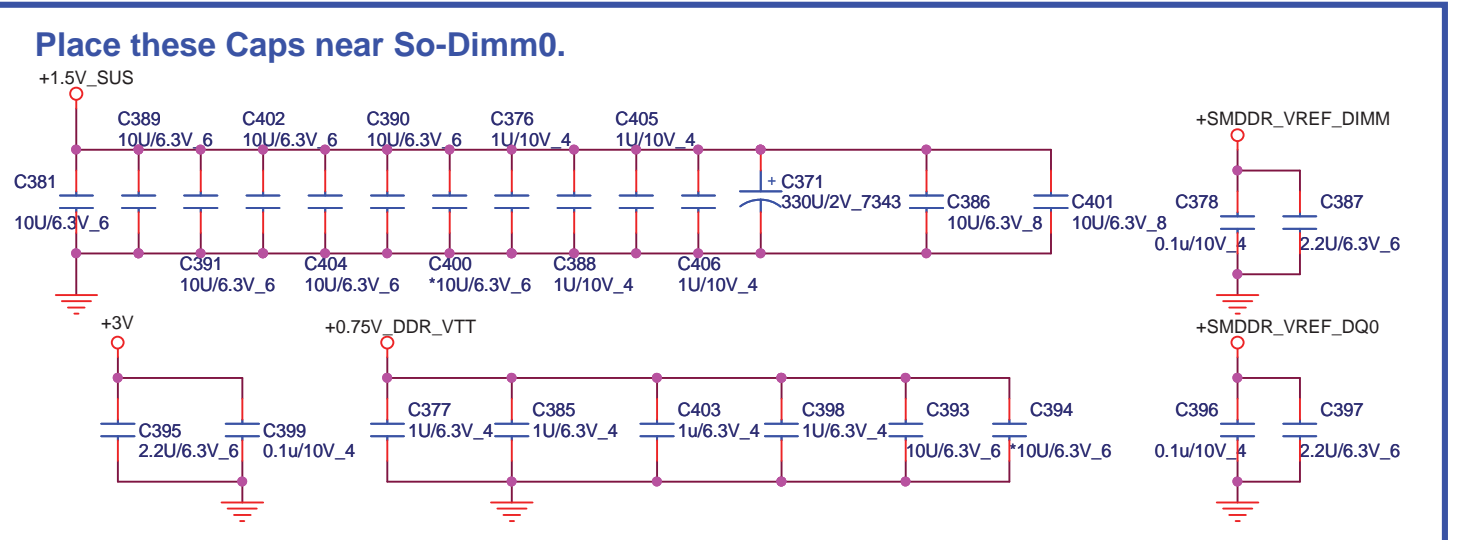
DDR_RVS (DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		



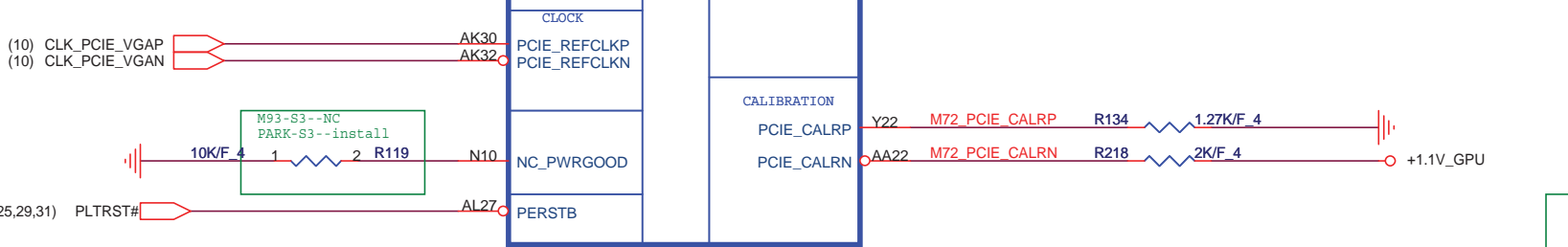
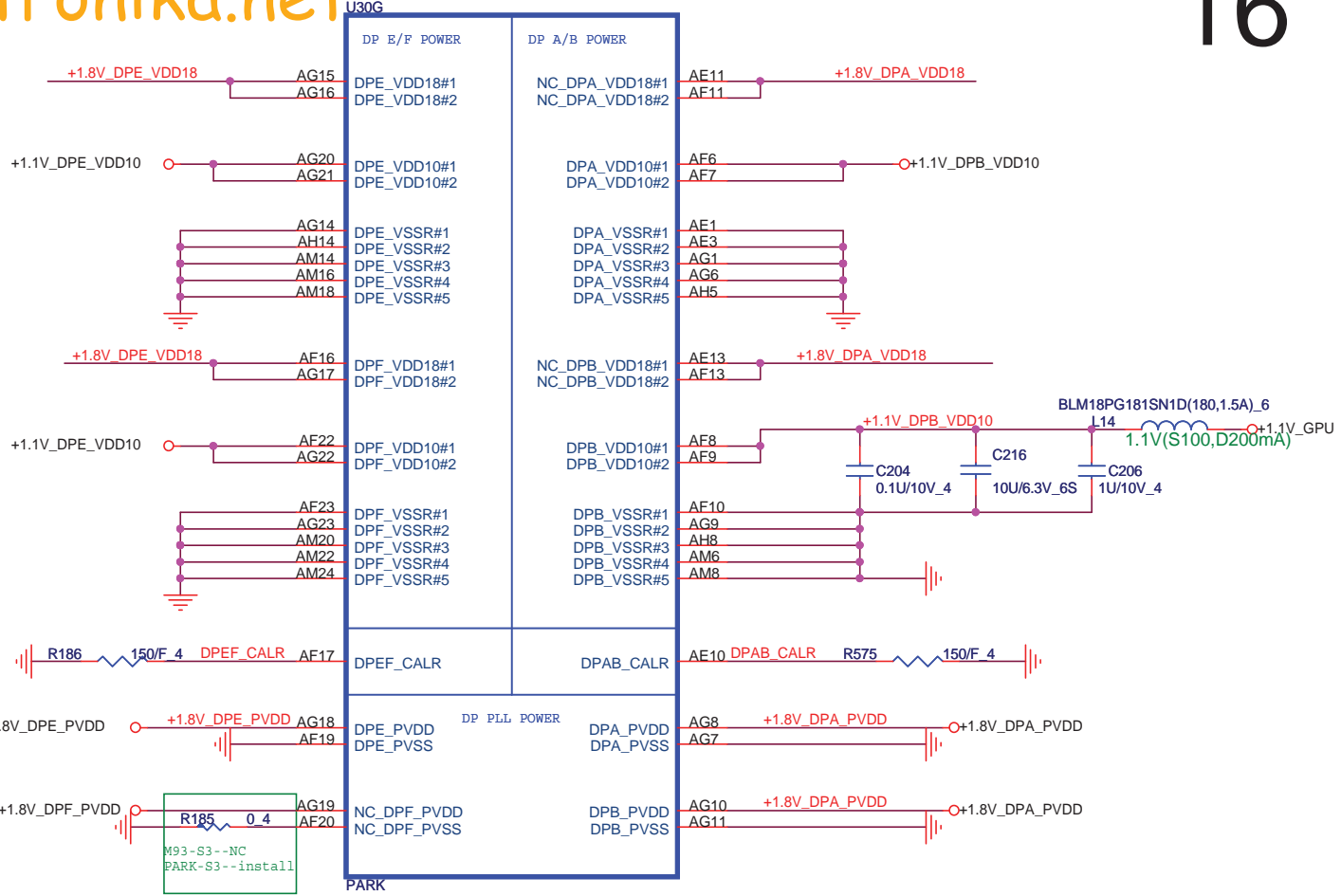
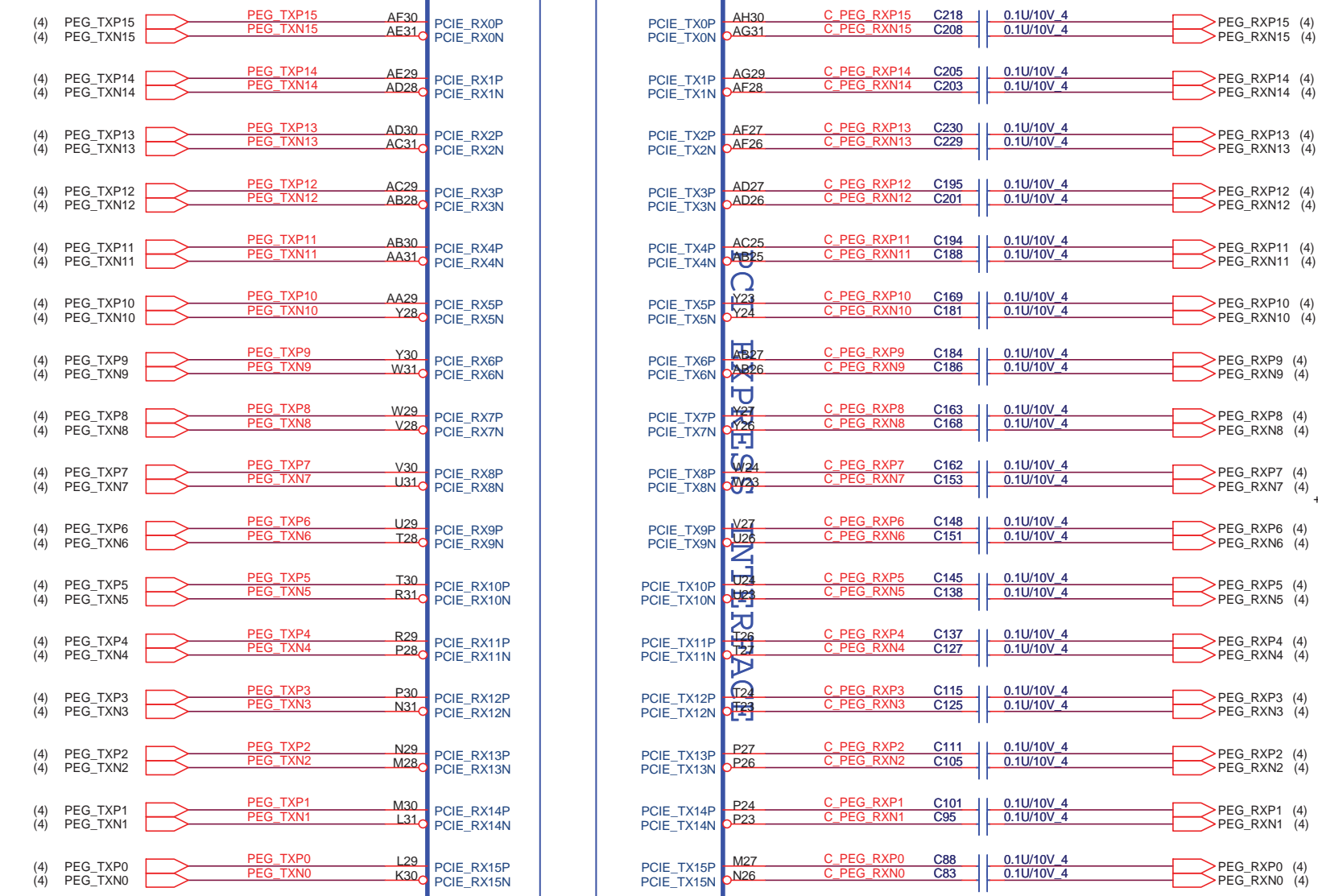
02/23 Remove 0ohm to GND



2.5GT/s bit rate

U30A

POWER
+PCIE_VDDR=1.0V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

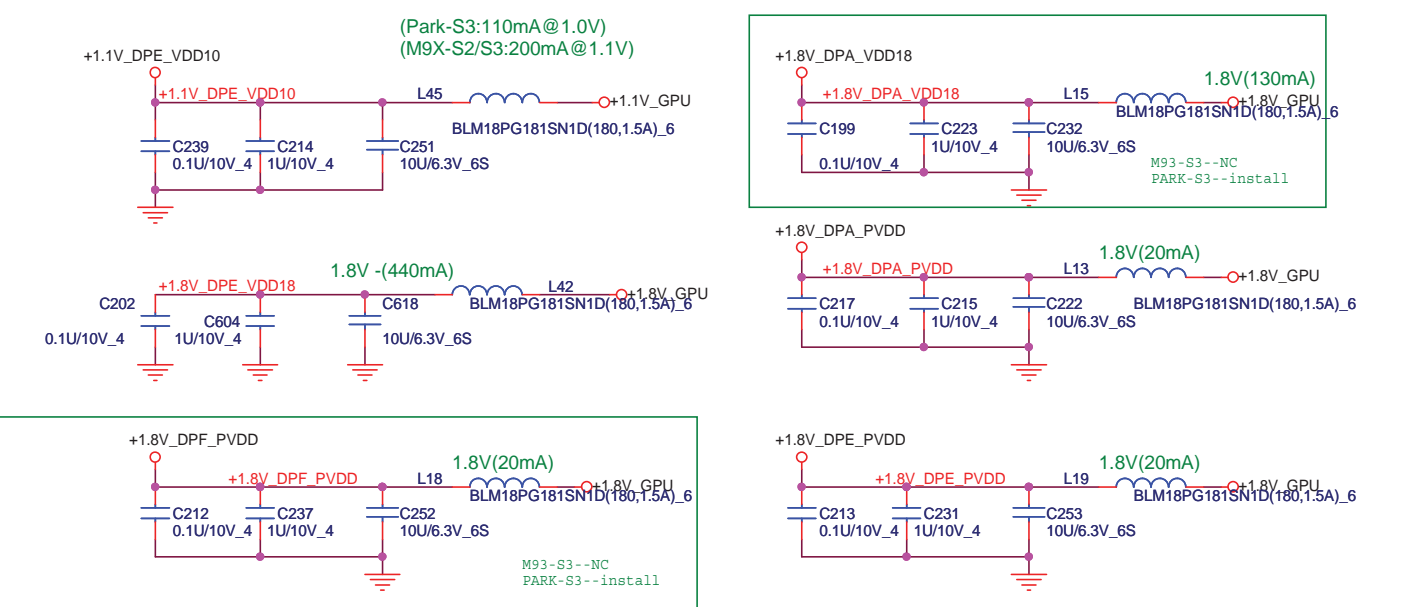
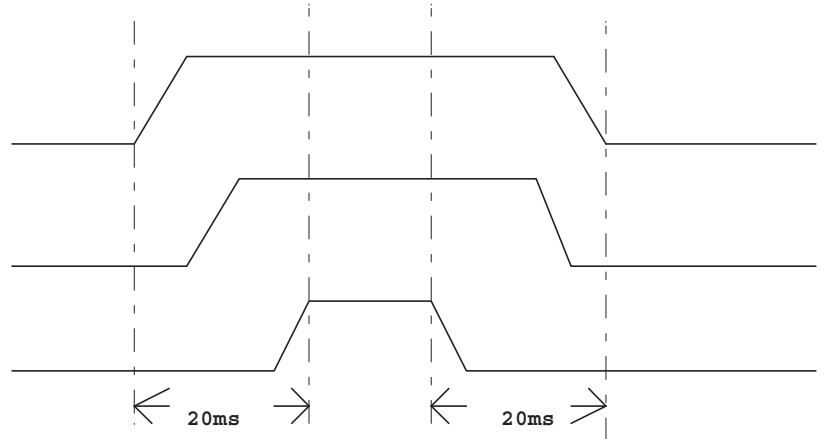


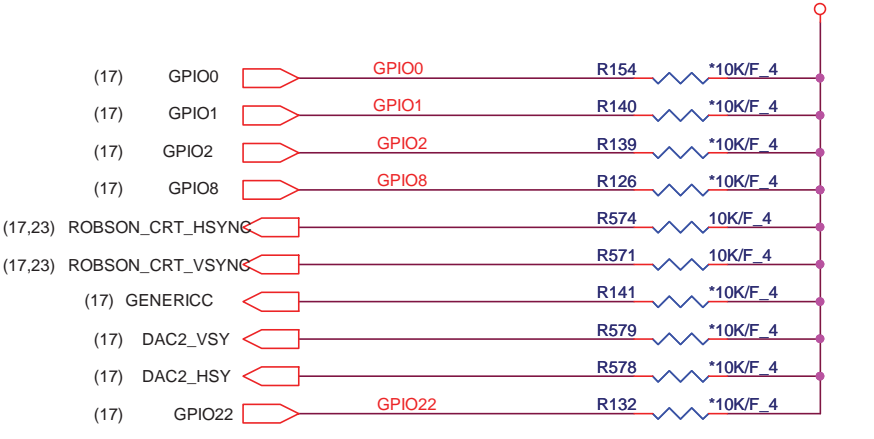
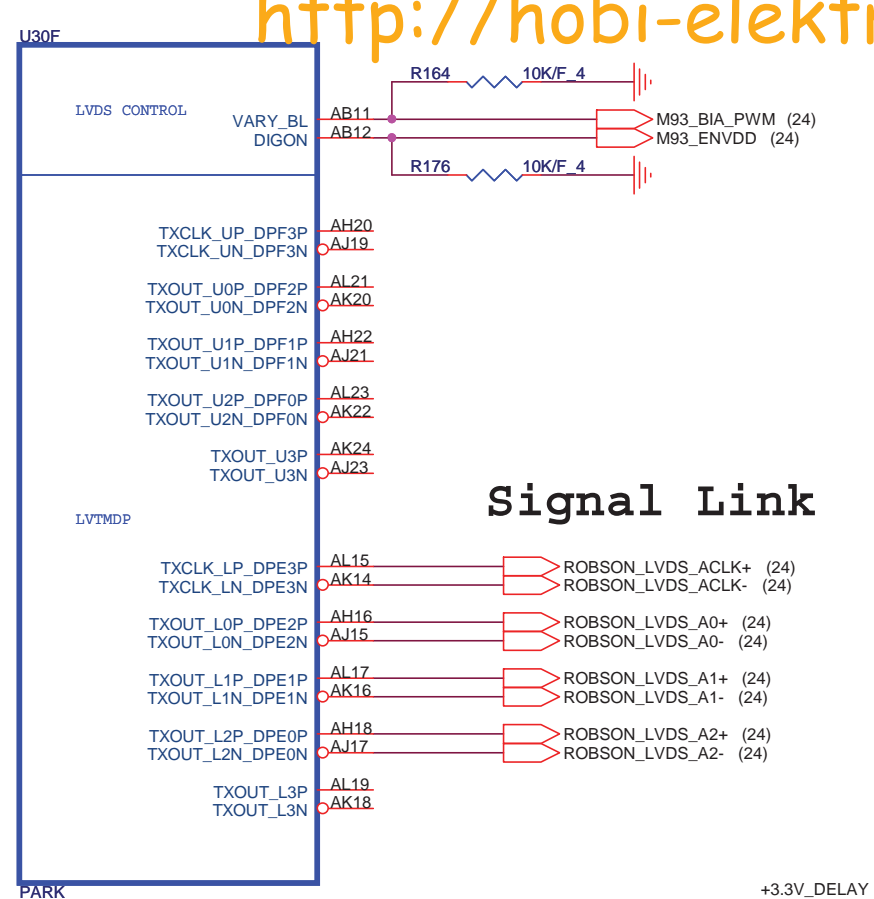
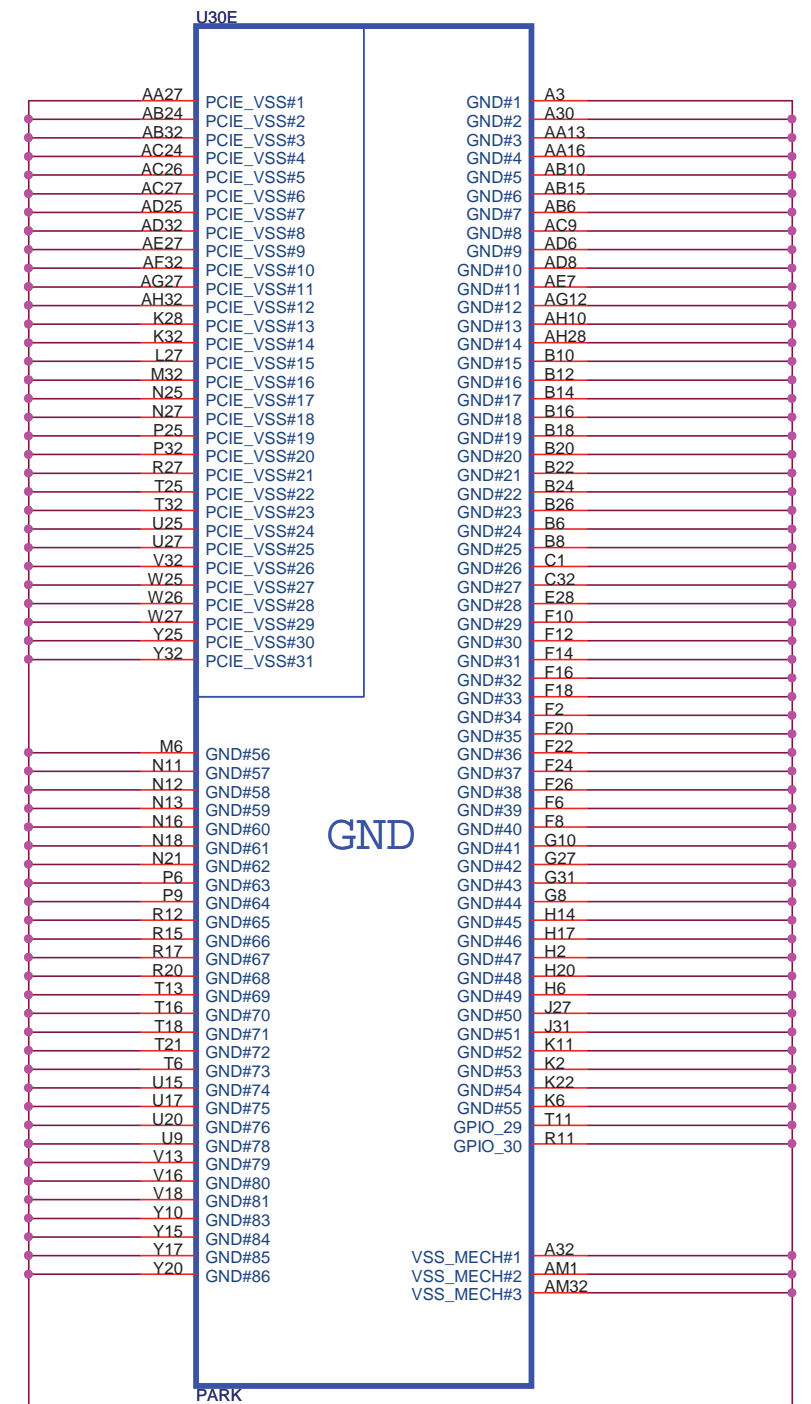
100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing

VGA Core BPP
VGA Core VDDC

+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1

+3V_VGA VDDR3





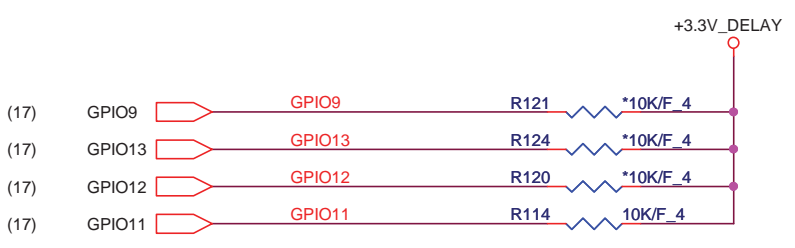
Memory Aperture size

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

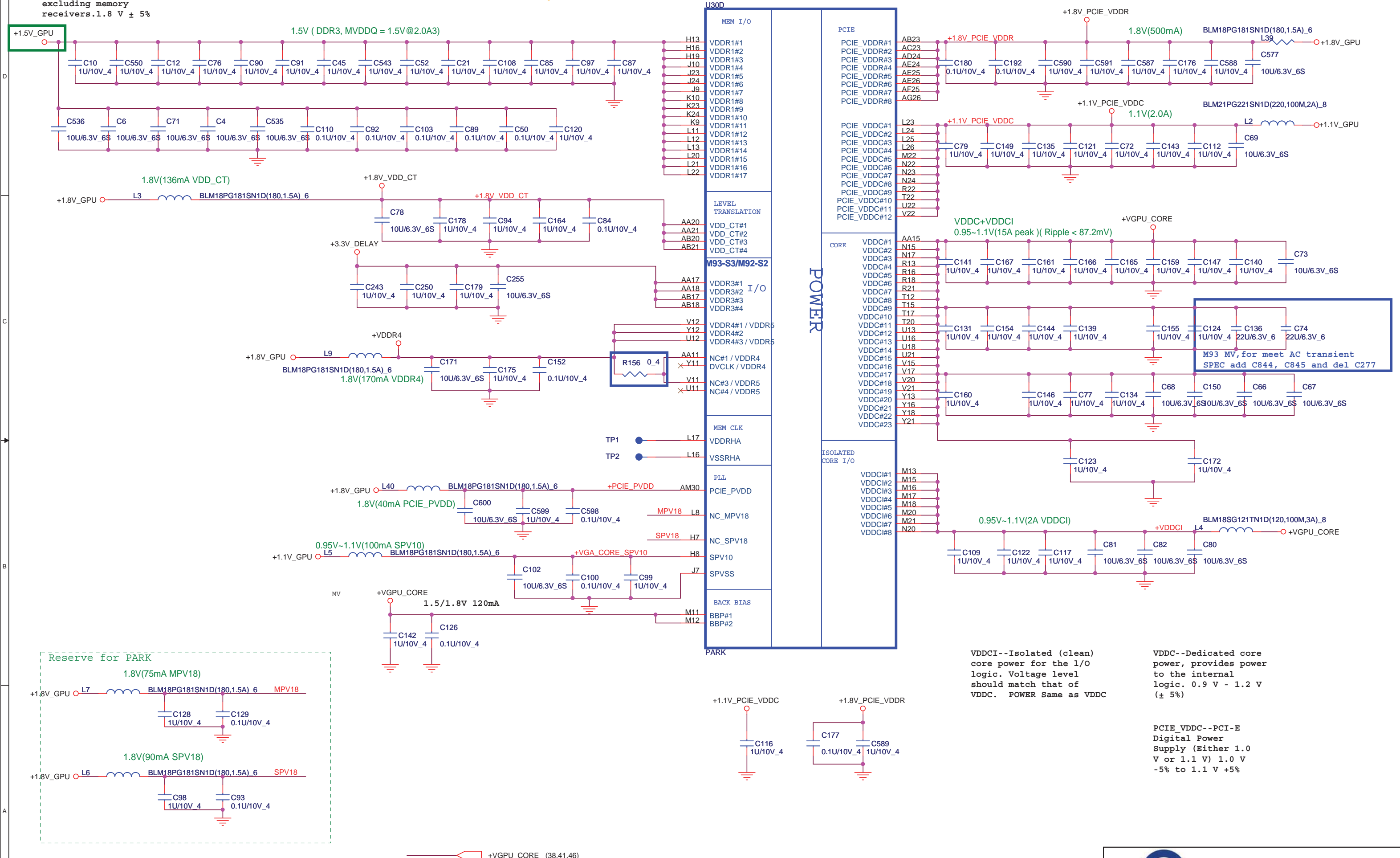


Quanta Computer Inc.
PROJECT :DM4/RB4

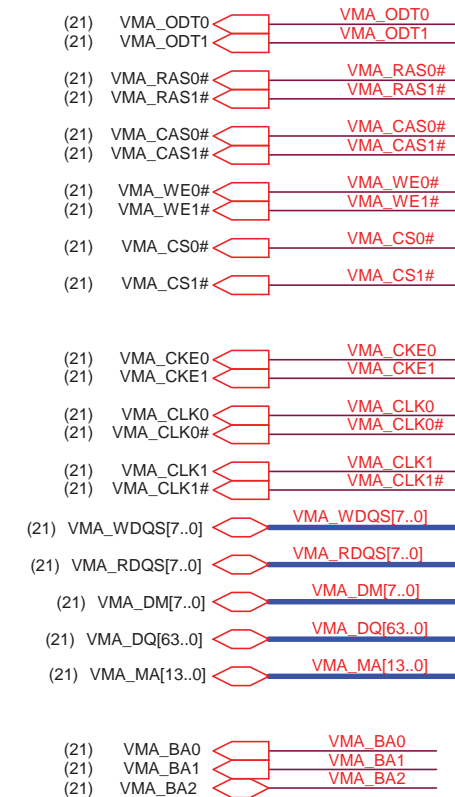
Size: Document Number: **Robson_GND / LVDS / Straps** Rev 1A
Date: Friday, November 19, 2010 Sheet 18 of 53

VDD_CT -- Level translation between core and I/O, excluding memory receivers. 1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

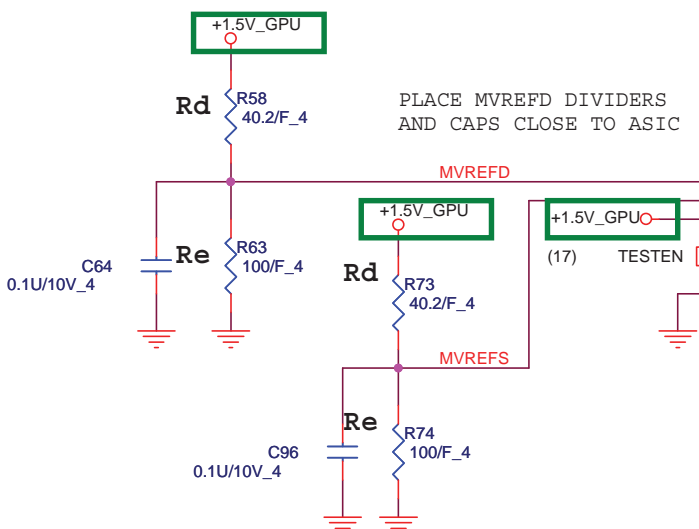
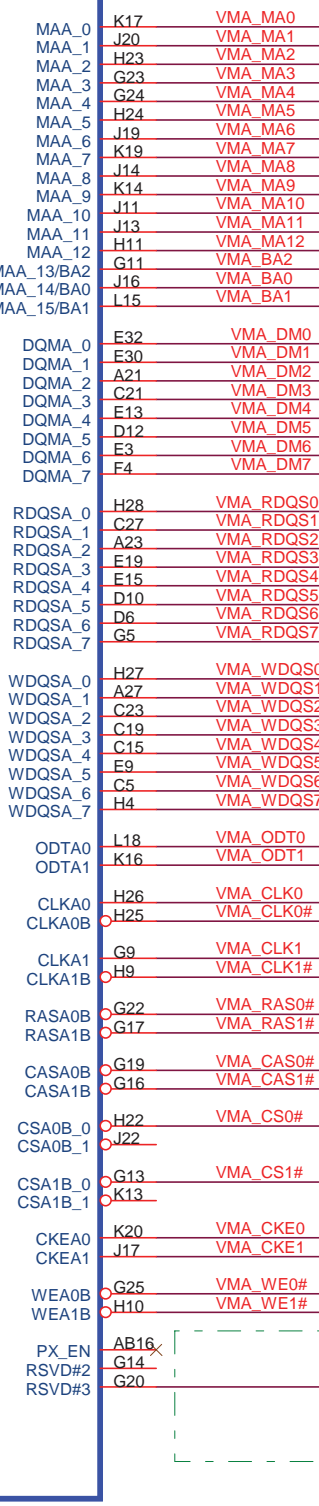
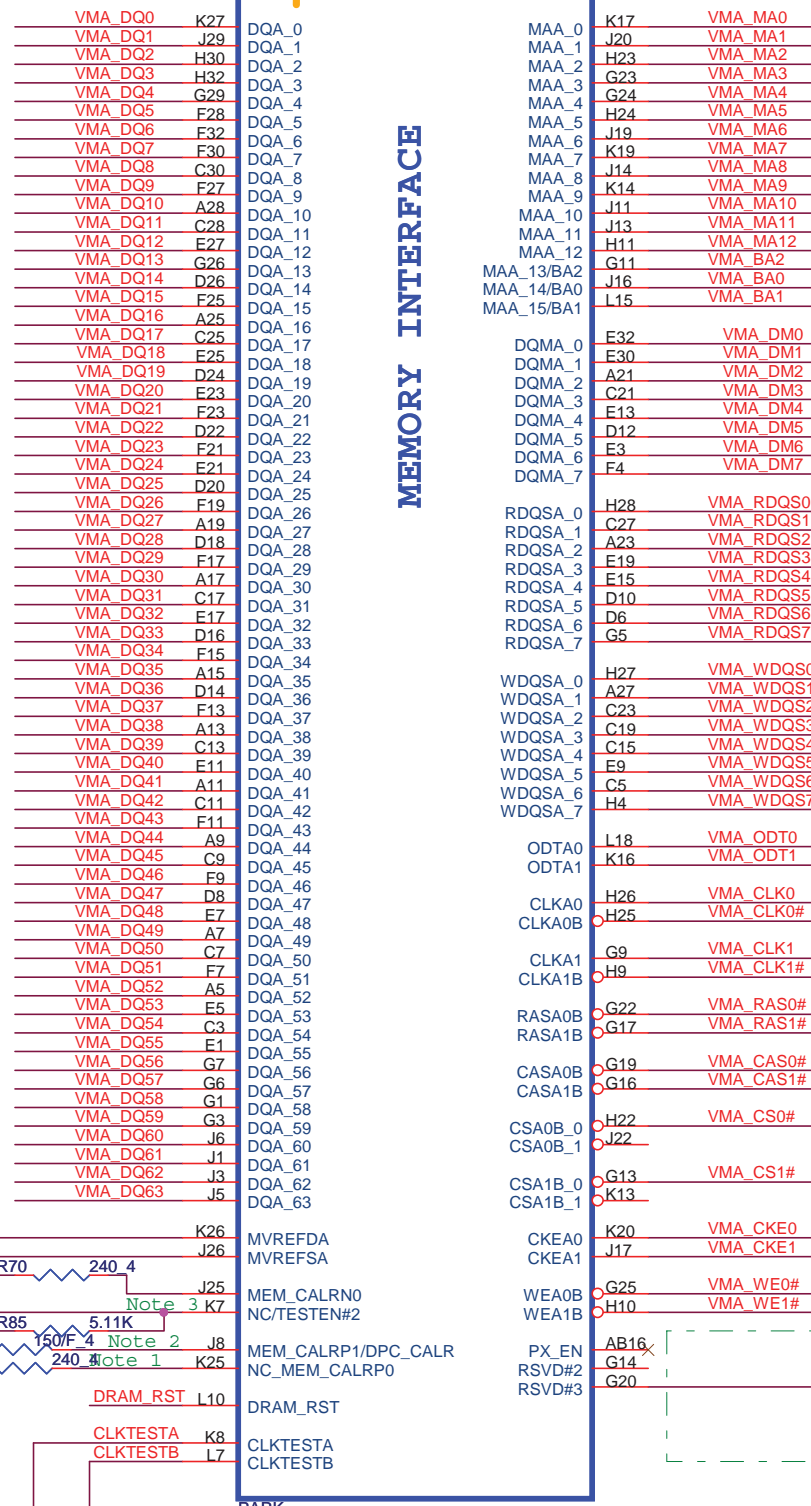


MEMORY INTERFACE

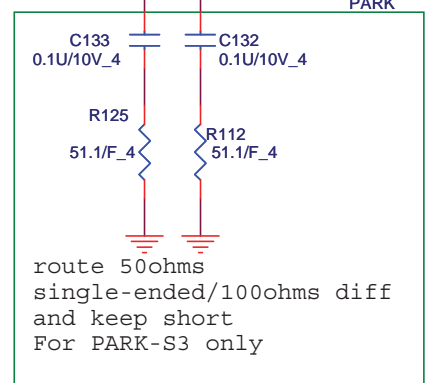


support 1Gbit
VRAM (64M X 16)

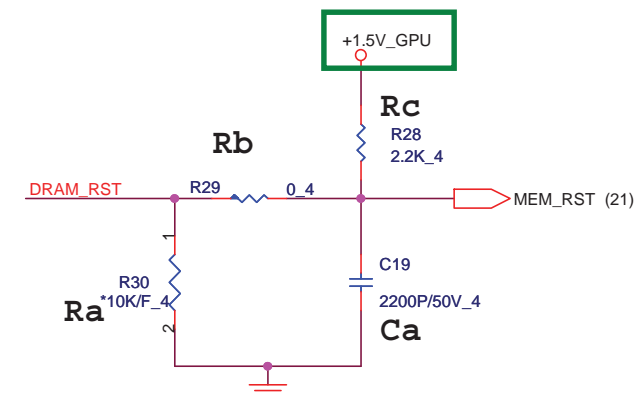
DIVIDER RESISTORS	ROBSON
MVREF TO 1.8V (Rd)	40.2R
MVREF TO GND (Re)	100R



PLACE MVREFD DIVIDERS AND CAPS CLOSE TO ASIC



route 50ohms single-ended/100ohms diff and keep short For PARK-S3 only



Ra Rb Rc Rd

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

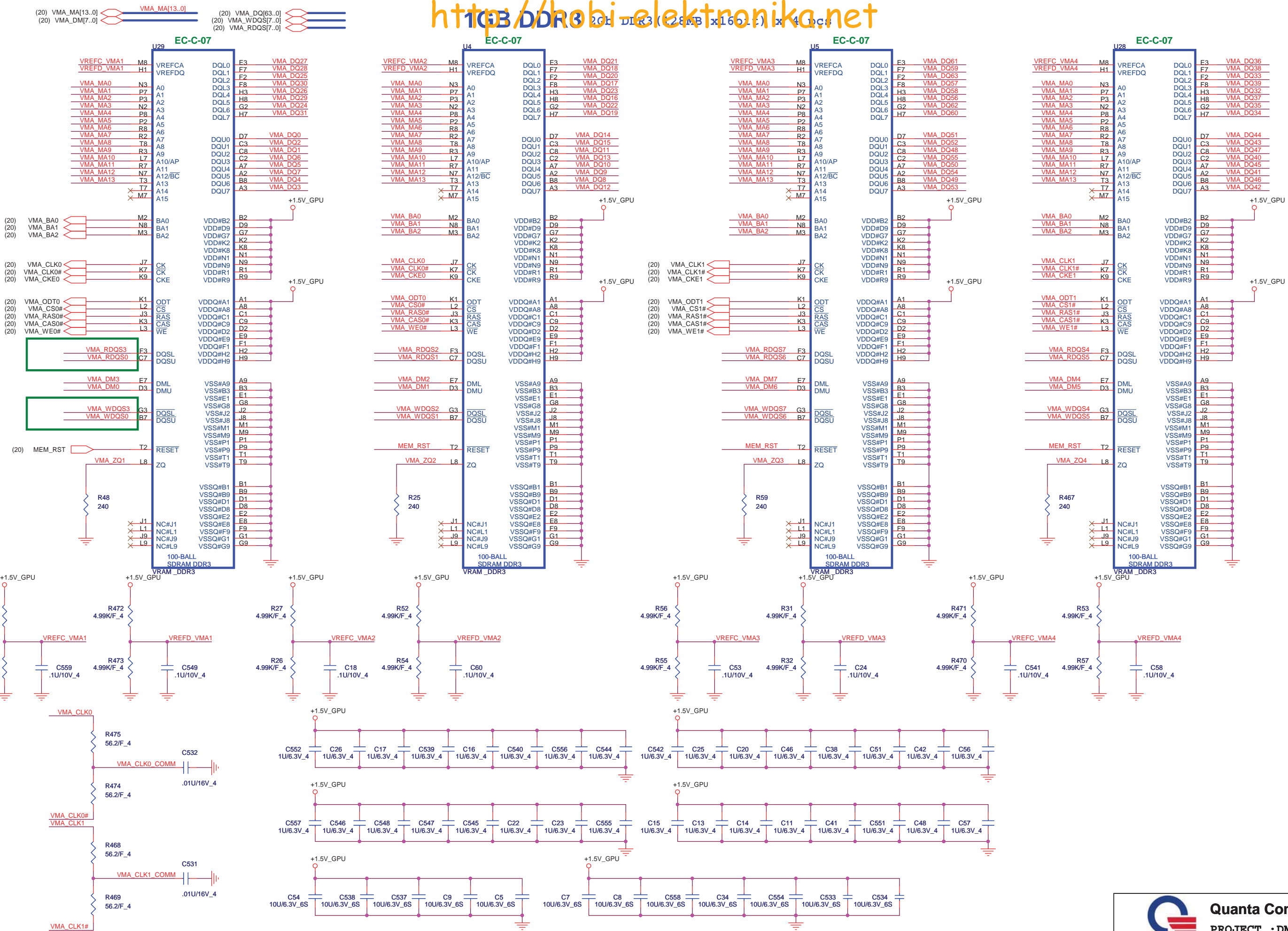
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

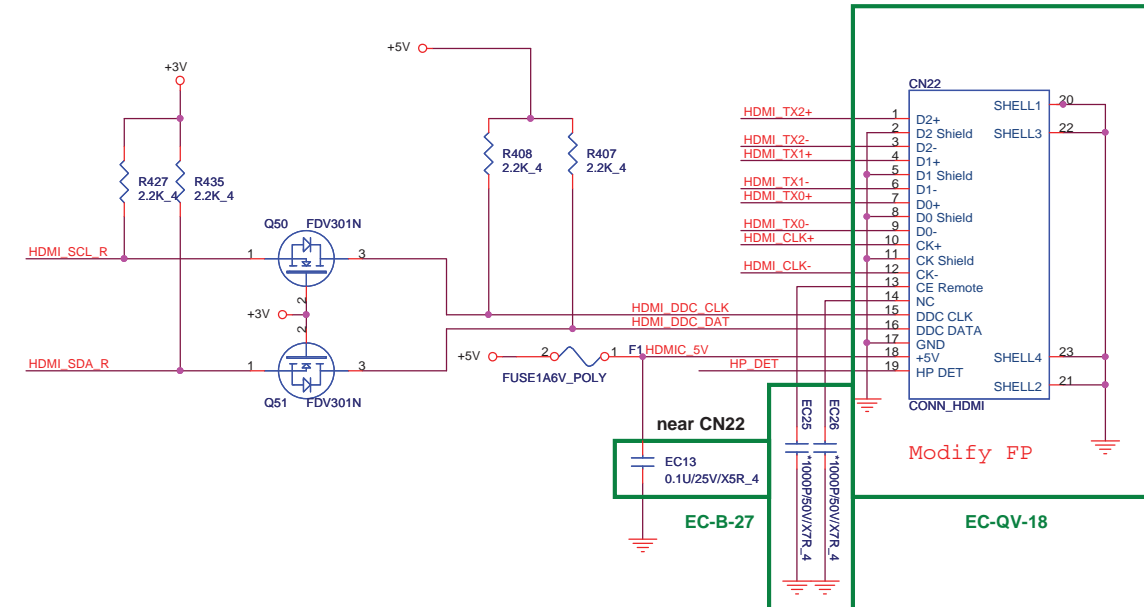
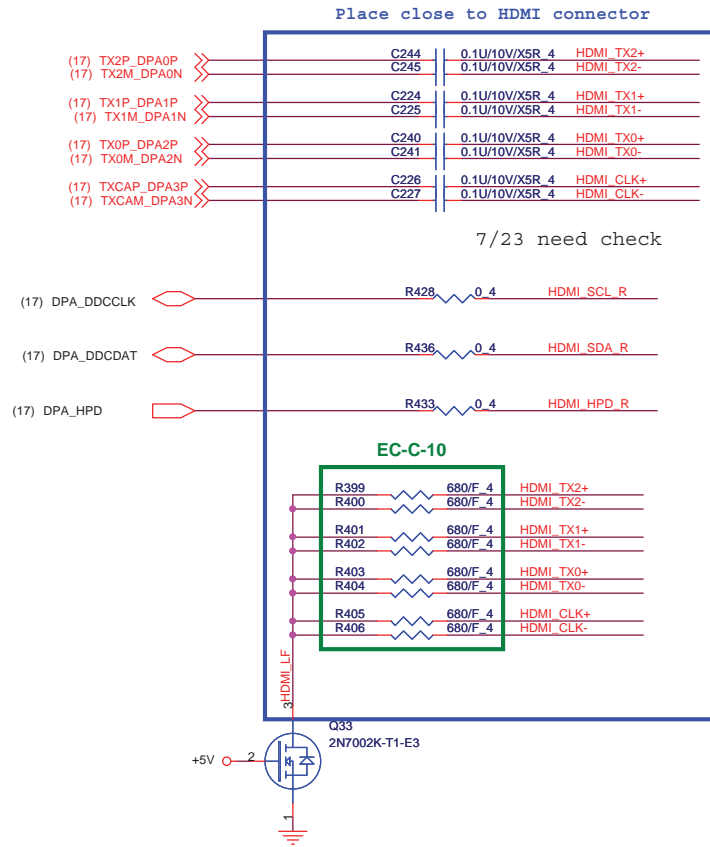
For PARK-S3 only For M9X-S2/S3 with DDR3: this pin is not in use.

- Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
- Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor. For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
- Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected. For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24 R575 for Robson only

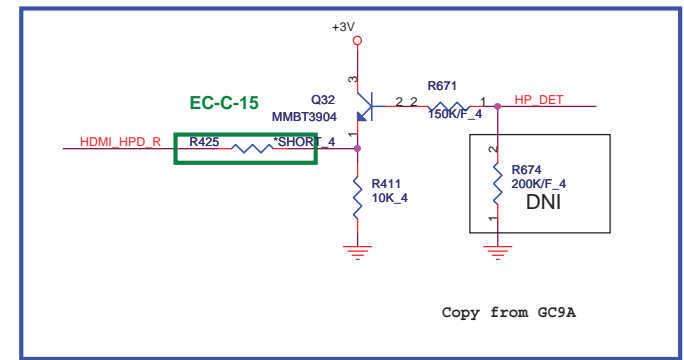
Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	Robson_MEM_Interface	1A
Date:	Tuesday, January 04, 2011	Sheet 20 of 53

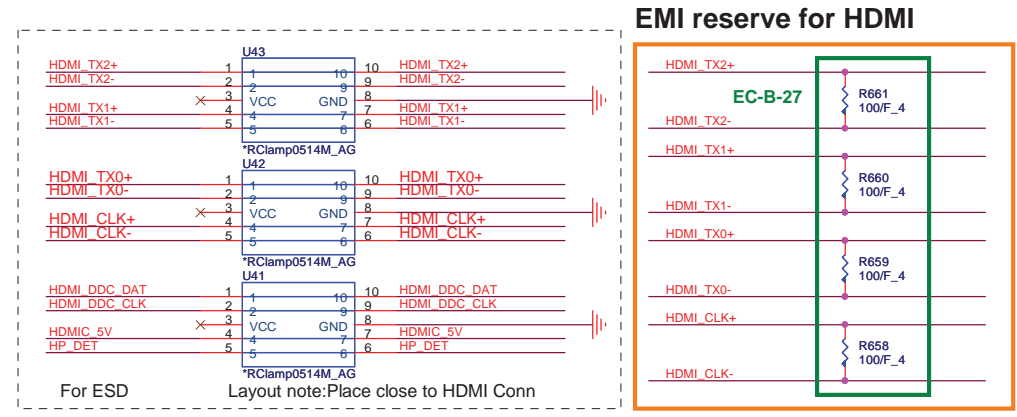
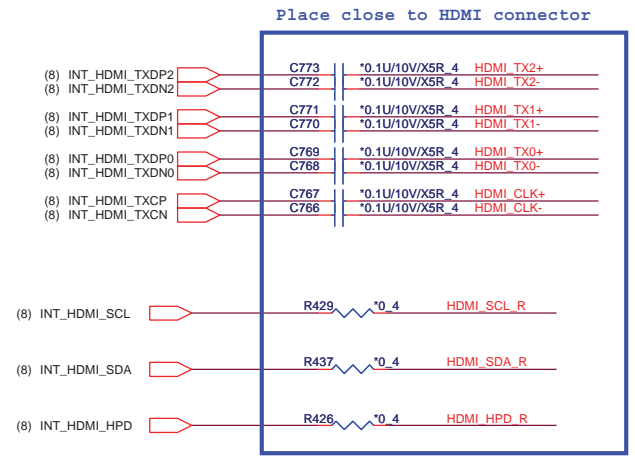




HDMI Hot-PLUG to EC and GPU

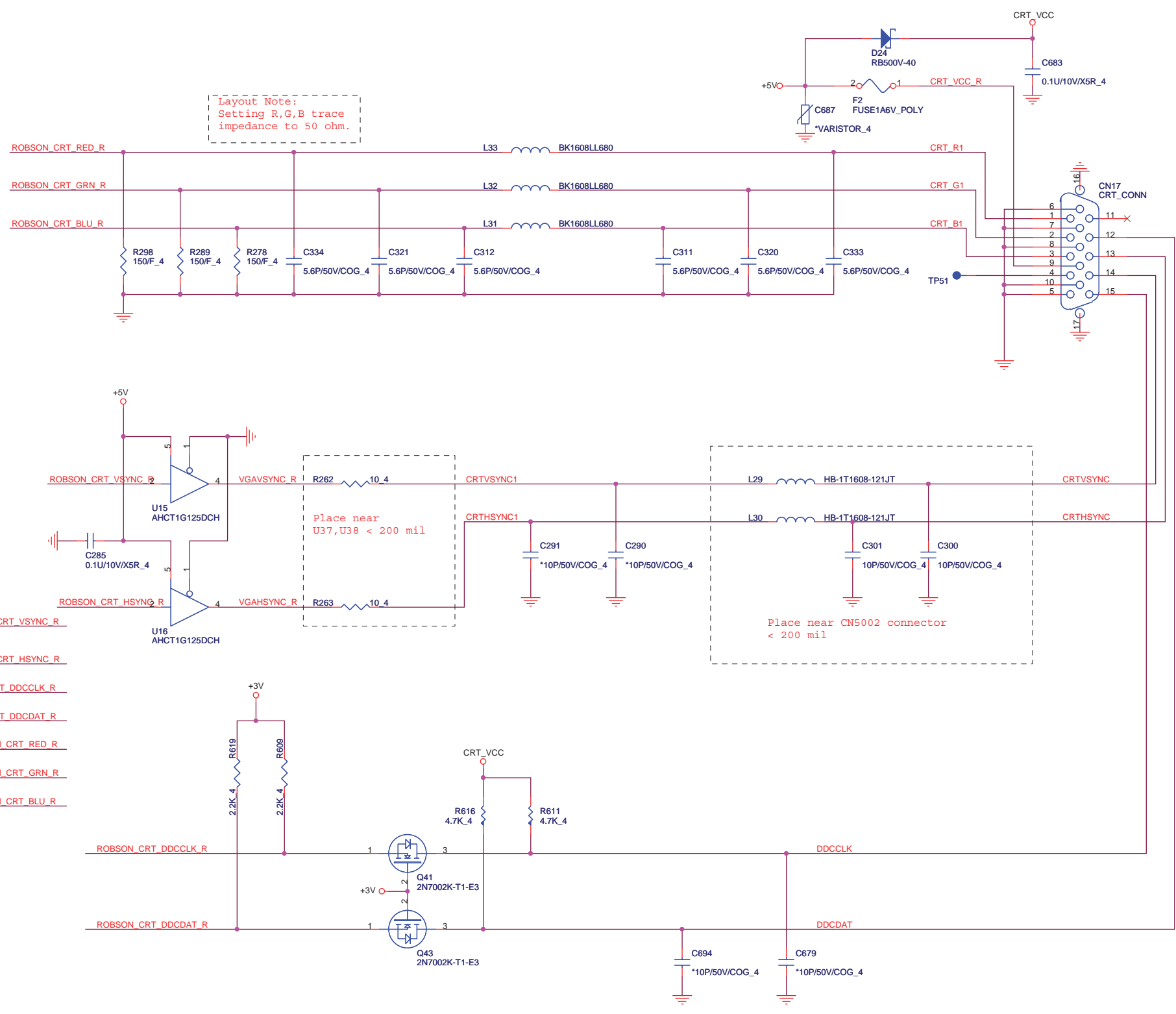
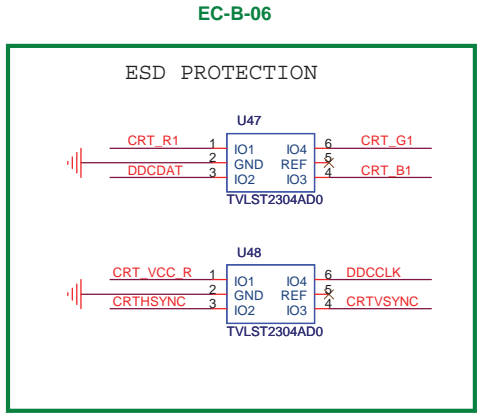


UMA Only

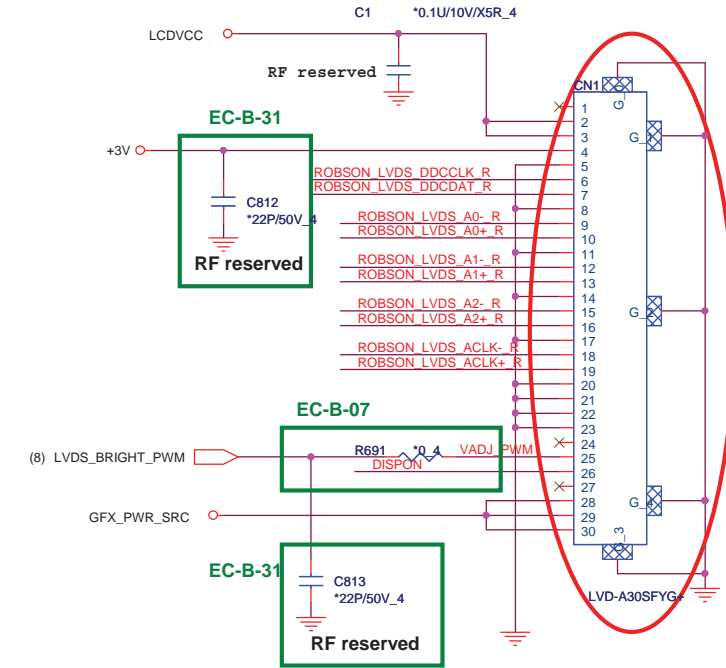
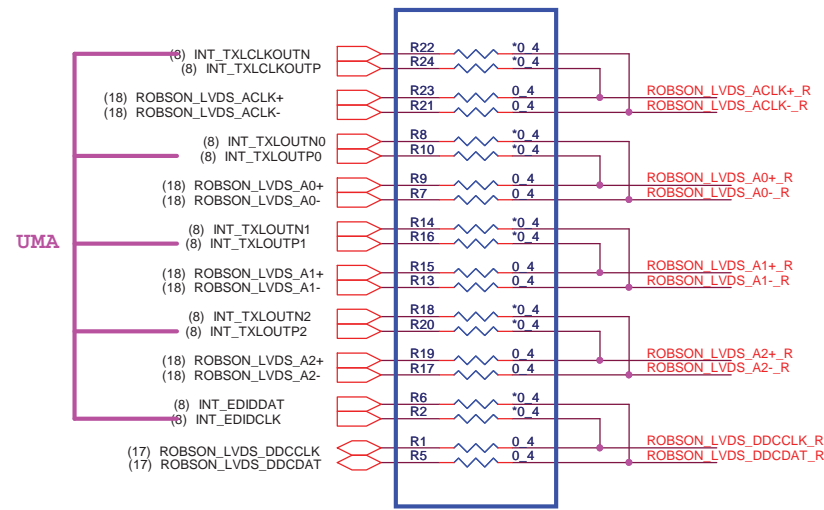
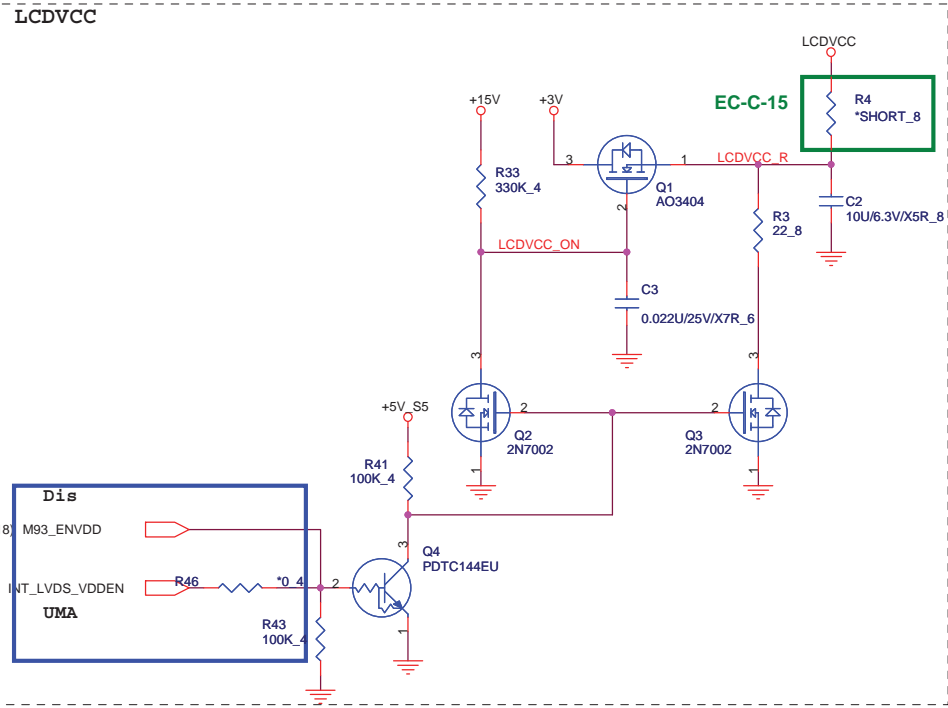


(8,9,10,11,12,14,15,17,22,24,26,27,28,29,30,31,36,37,38,41,41,42,46,47,48,49) +5V
(8,9,10,11,12,14,15,17,22,24,26,27,28,29,30,31,36,37,38,41,41,42,46,47,48,49) +3V

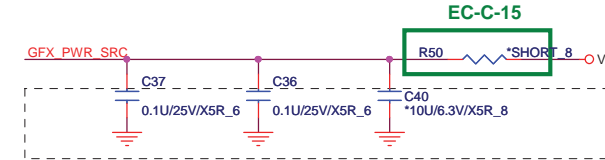
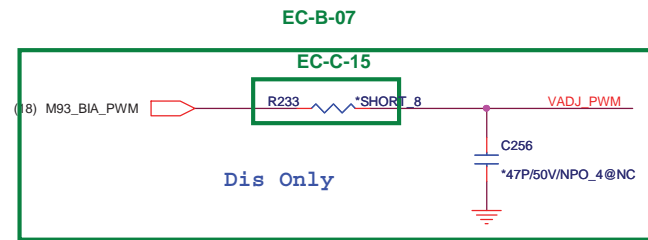
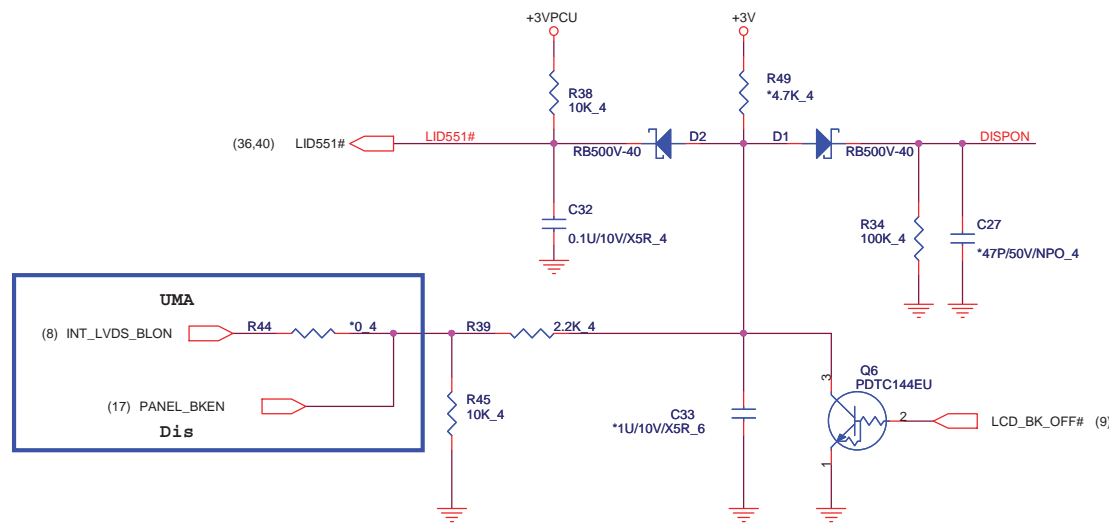
Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

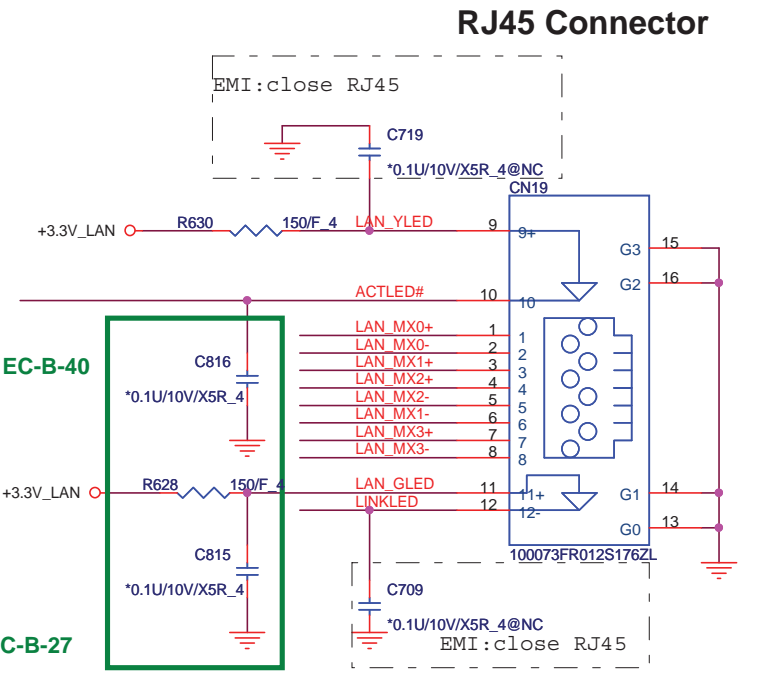
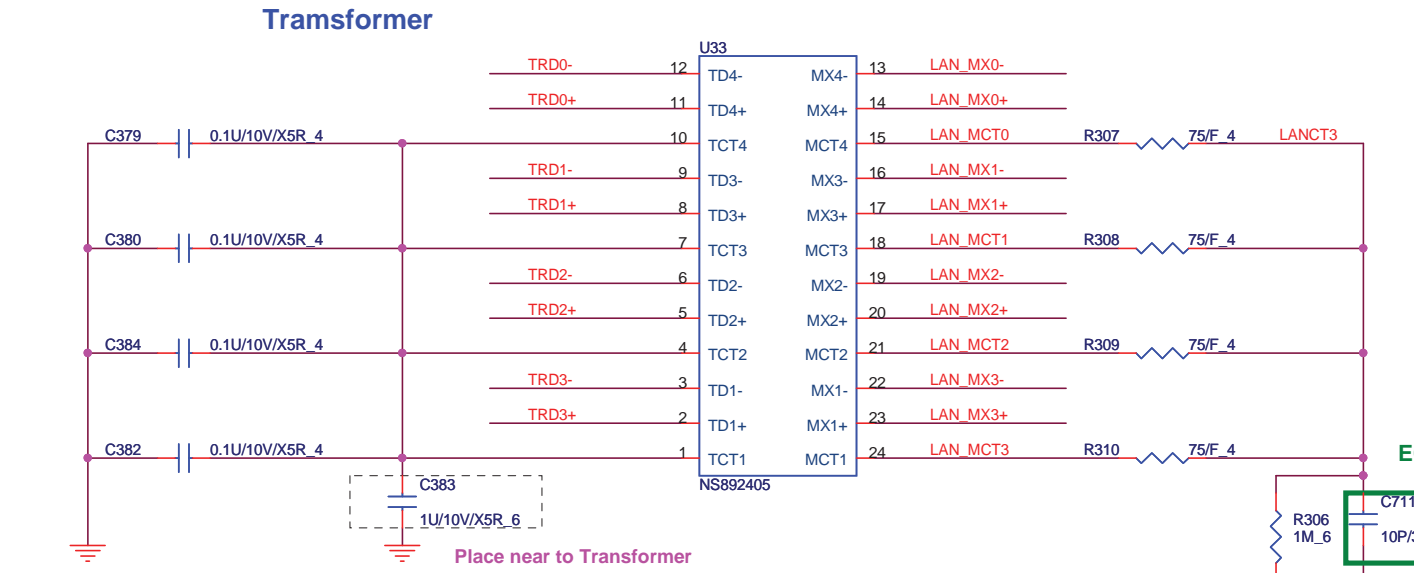
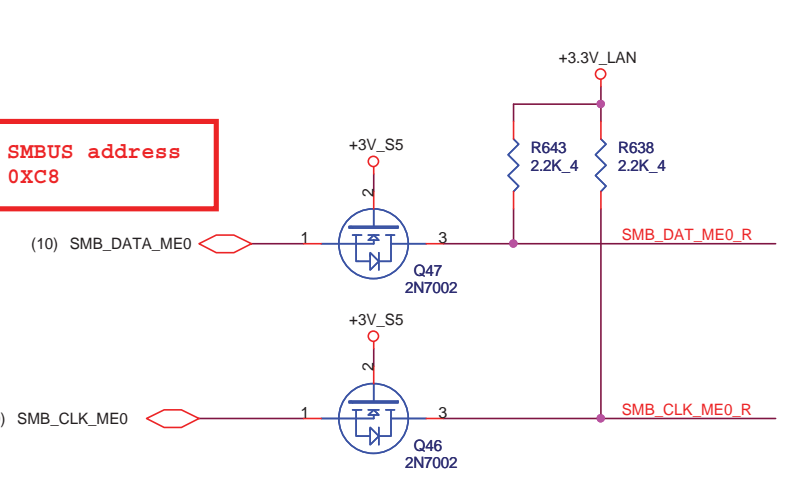
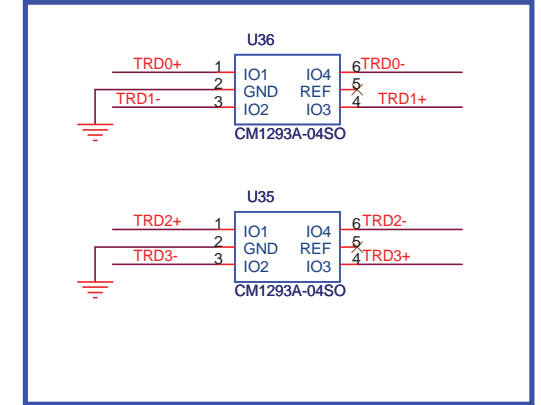
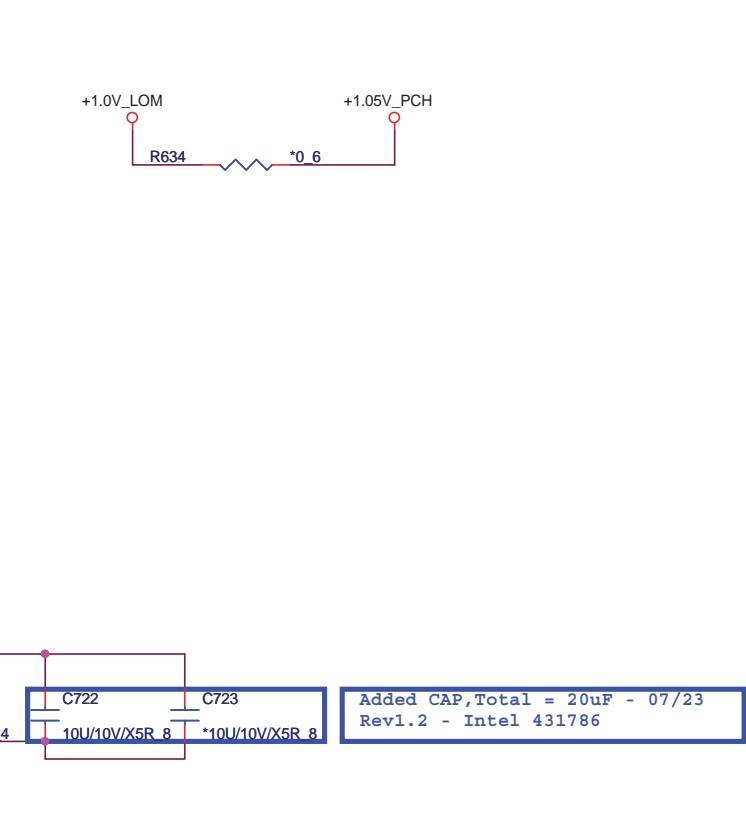
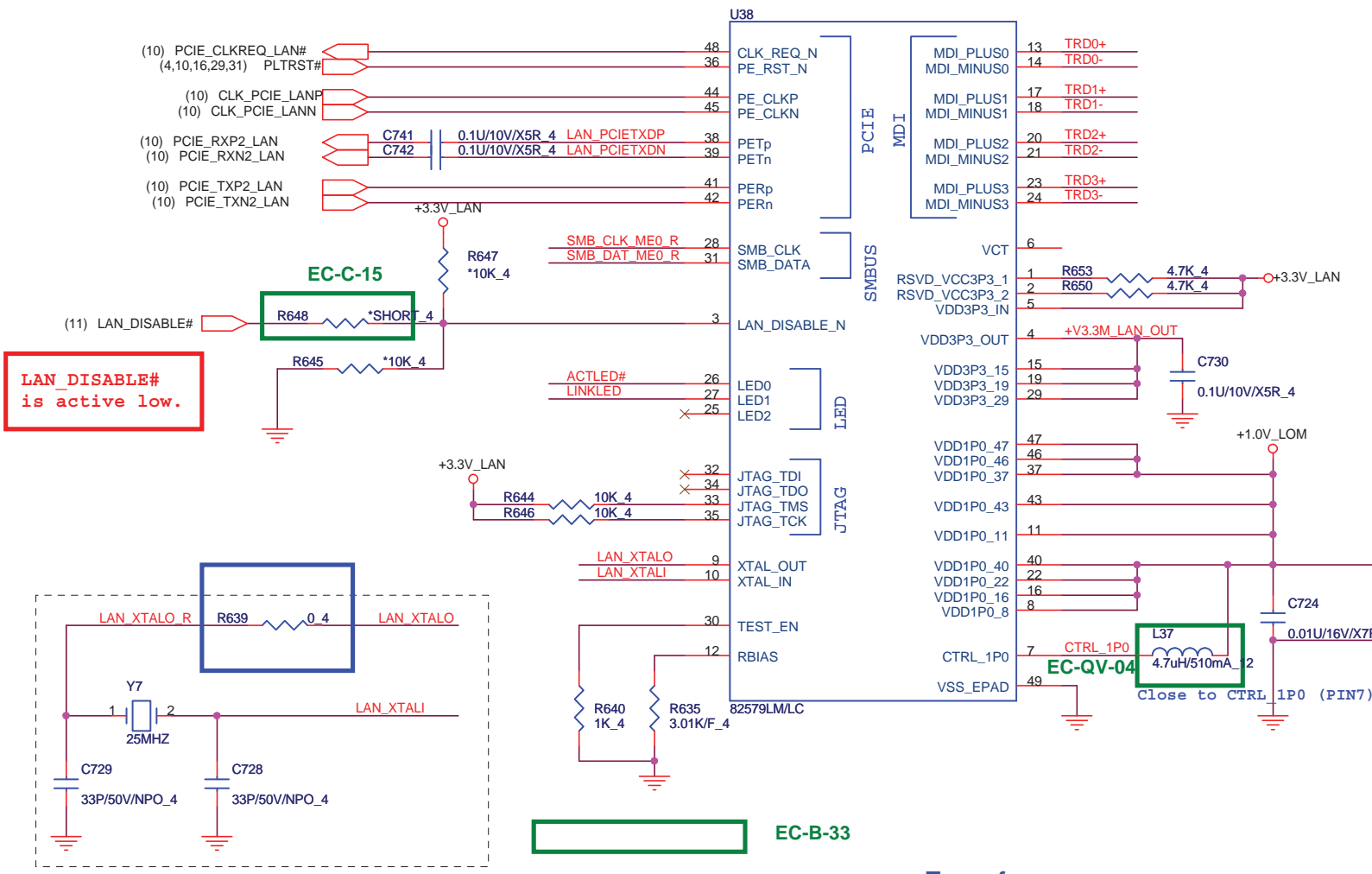
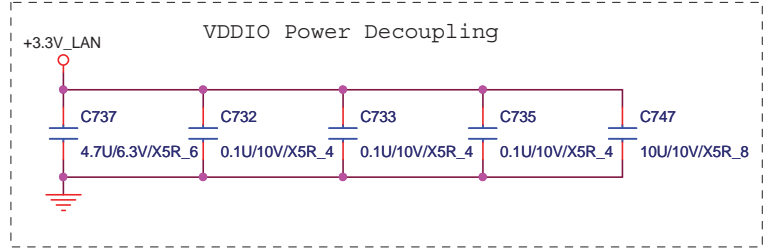
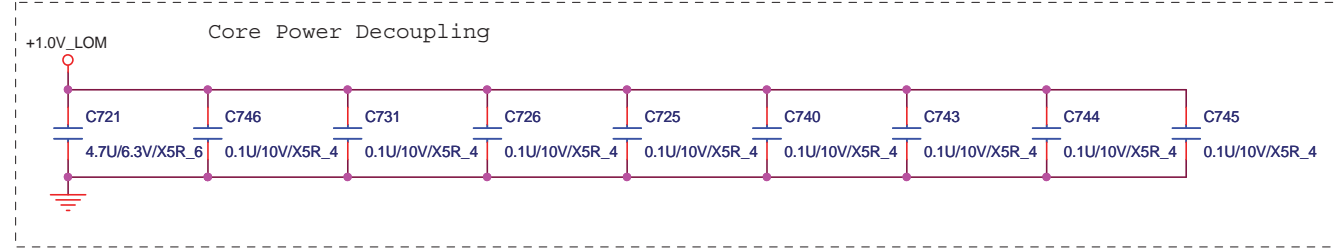
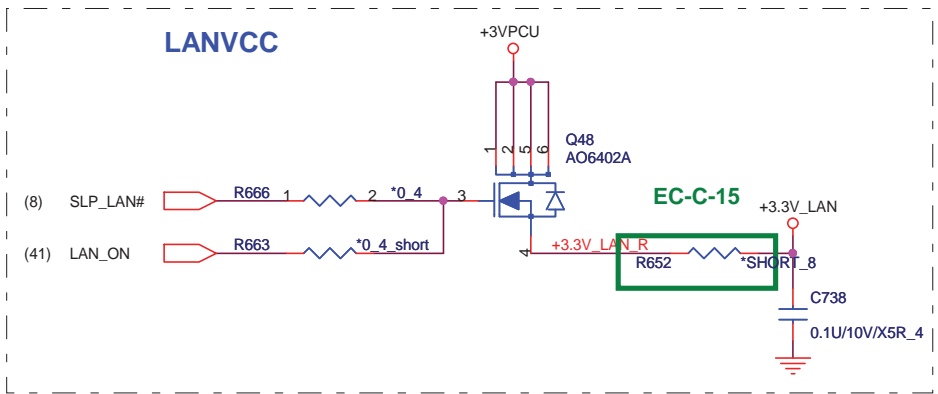


DIS



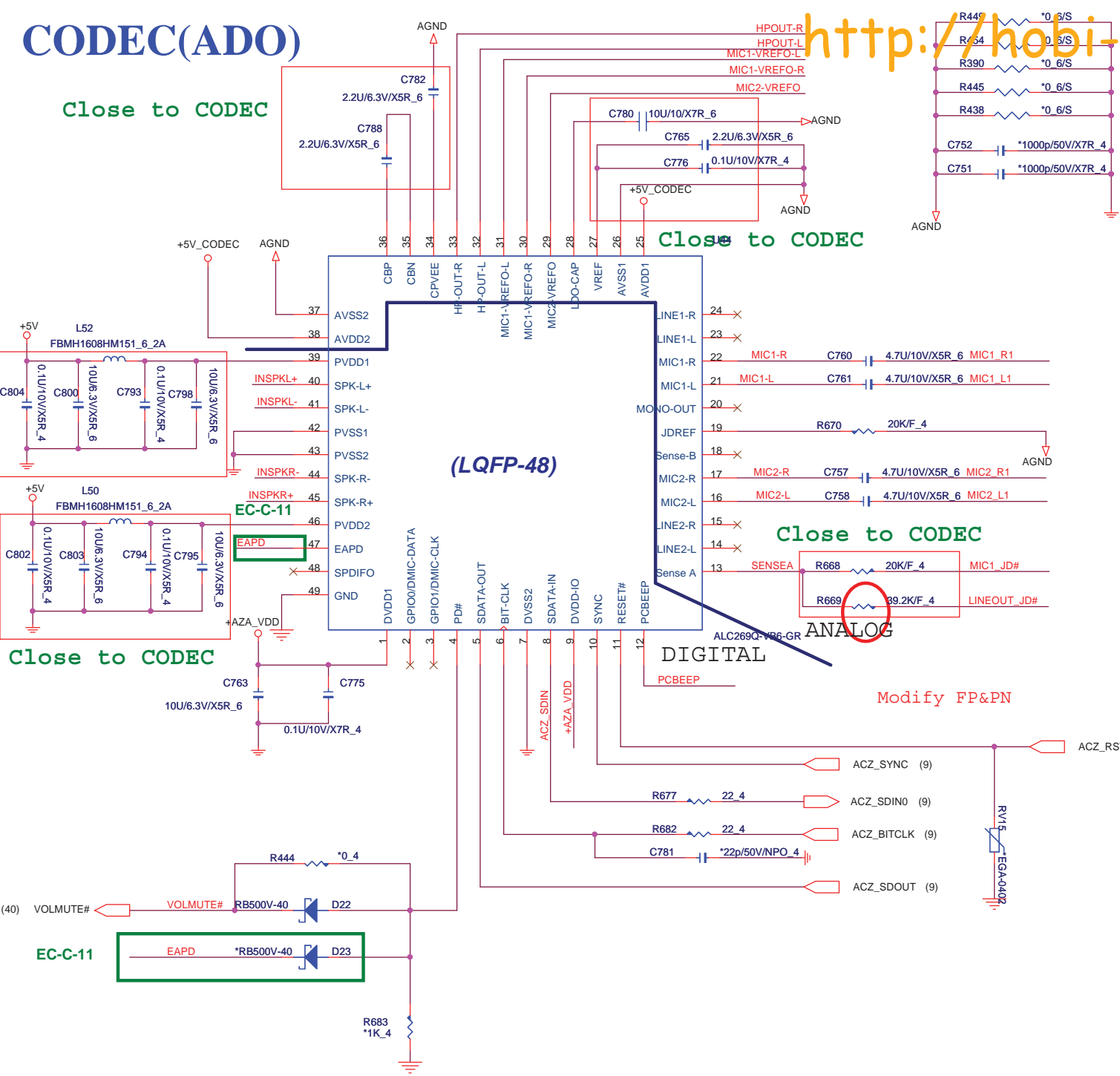
Back light





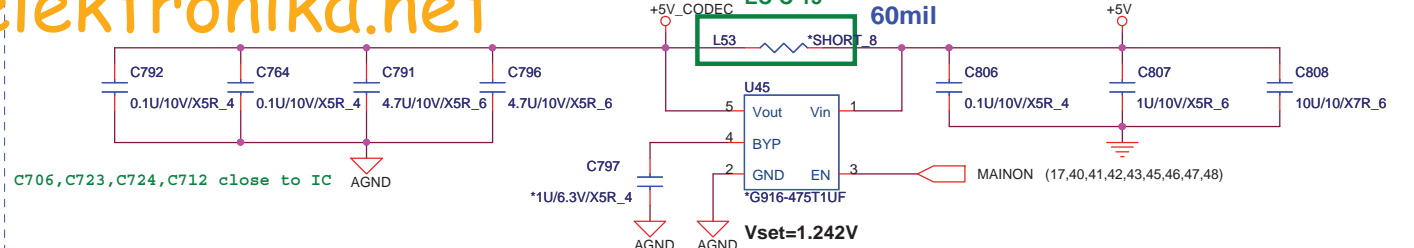
CODEC(ADO)

Close to CODEC

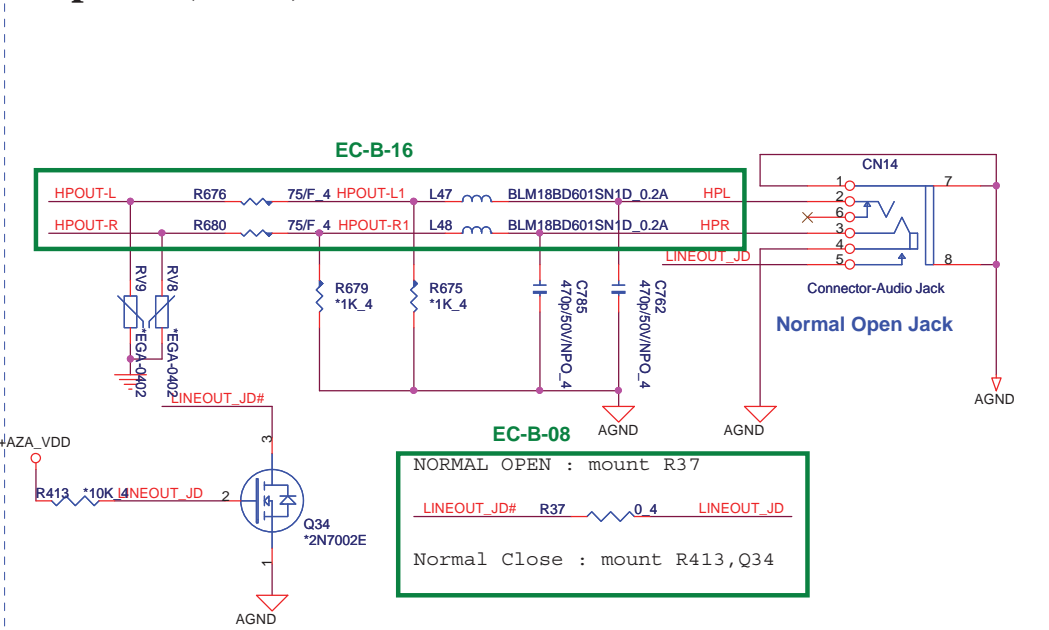


<http://hobi-elektronika.net>

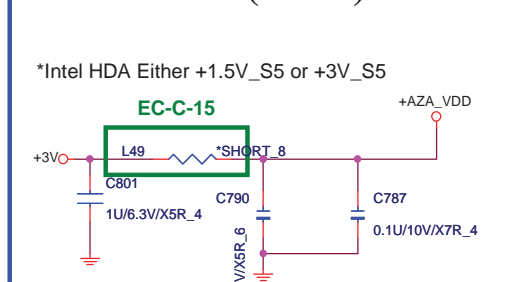
Codec Power(ADO)



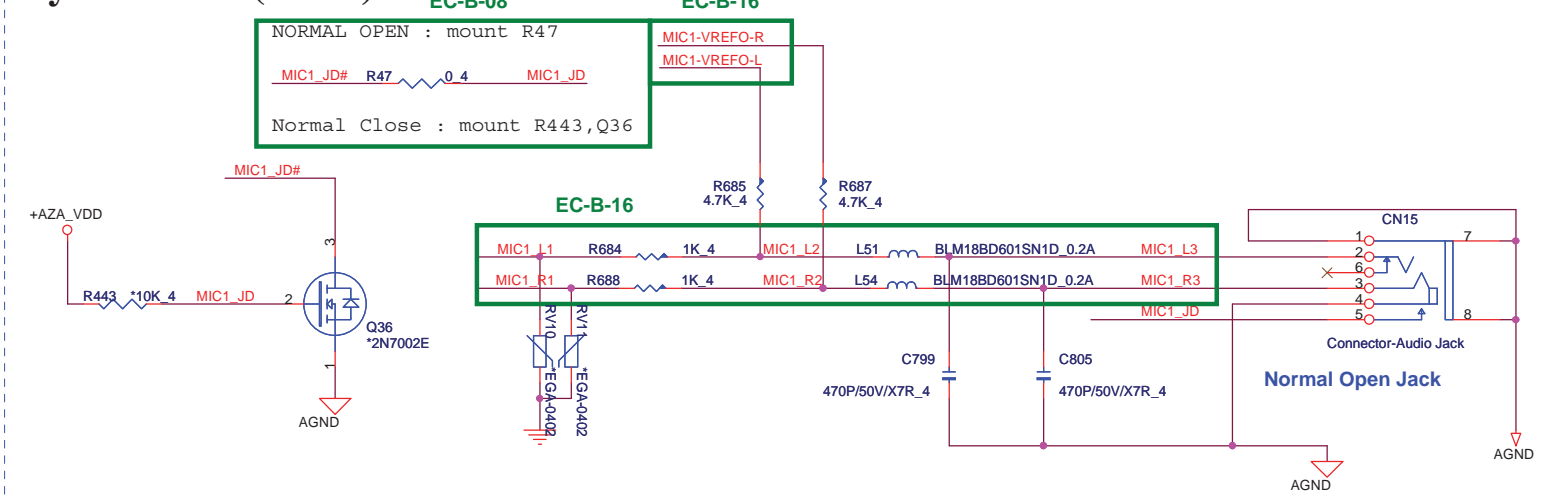
Earphone(AMP)

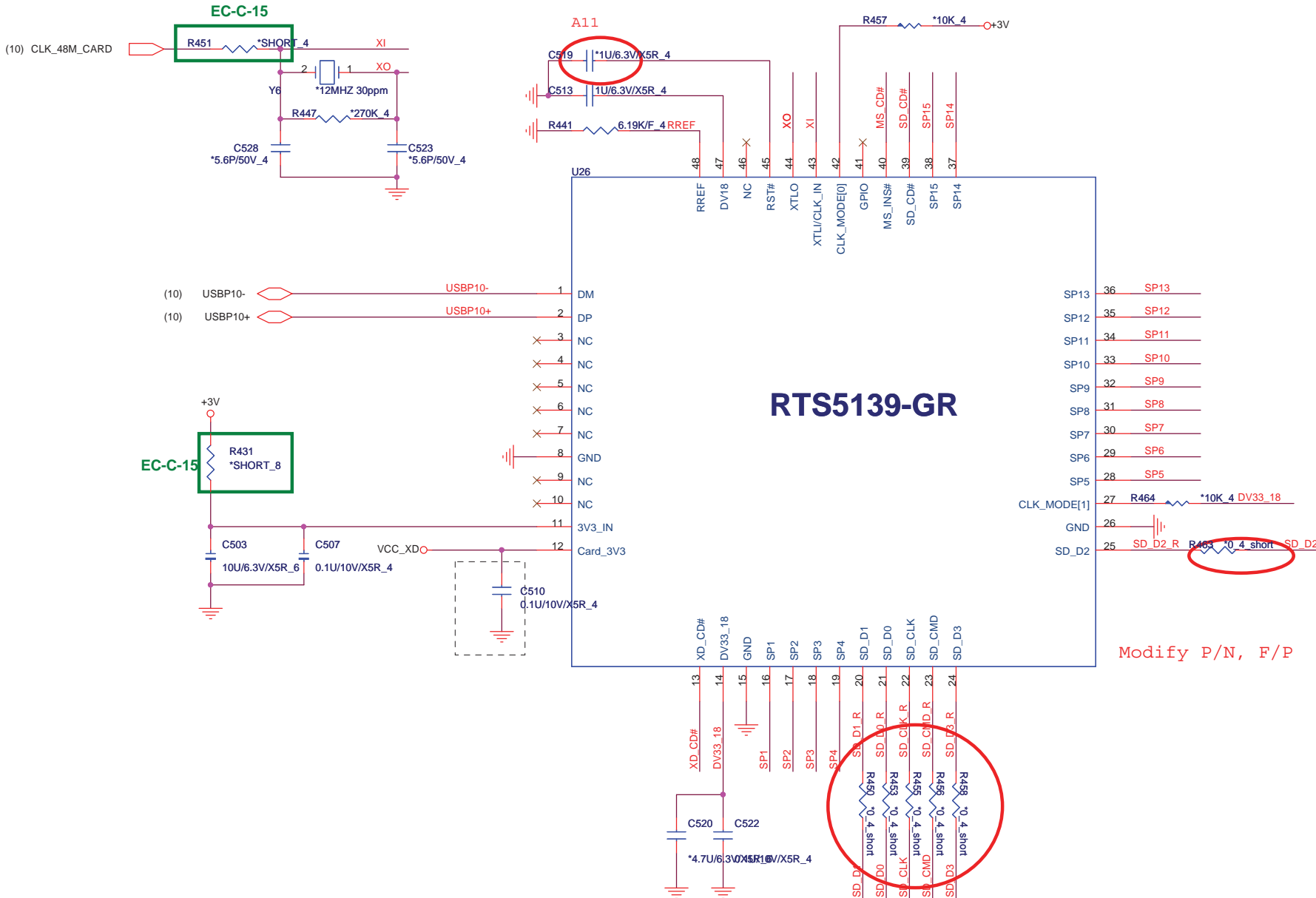


HDA Power(ADO)



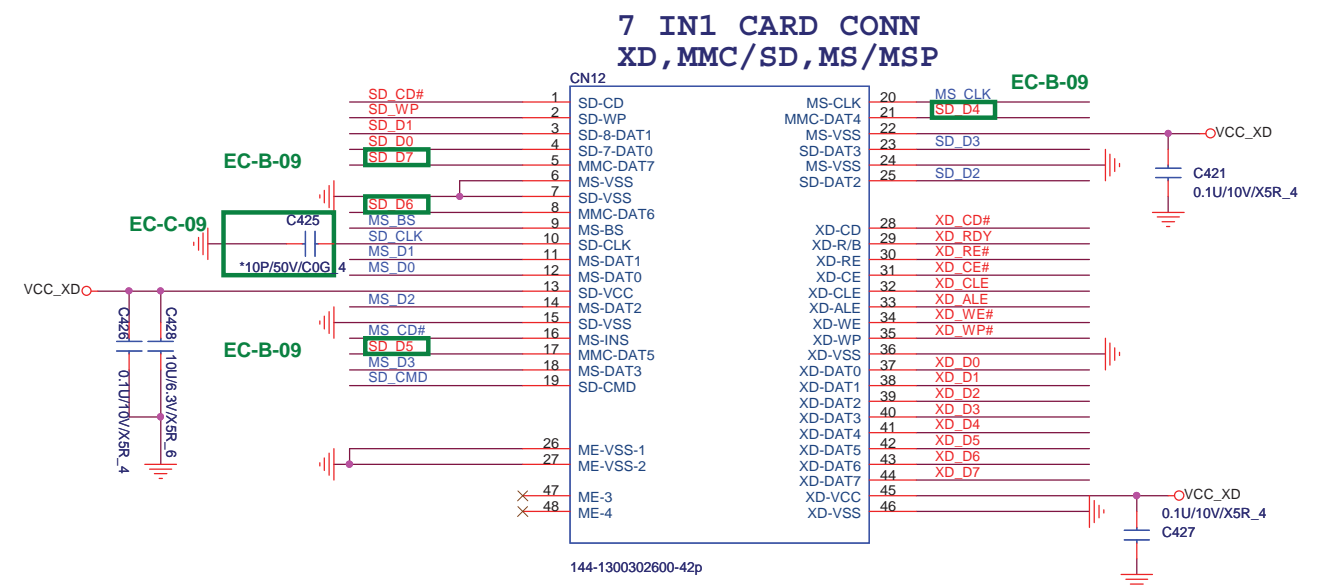
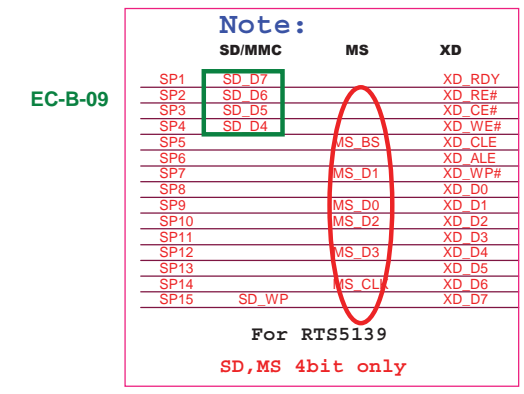
System MIC(AMP)

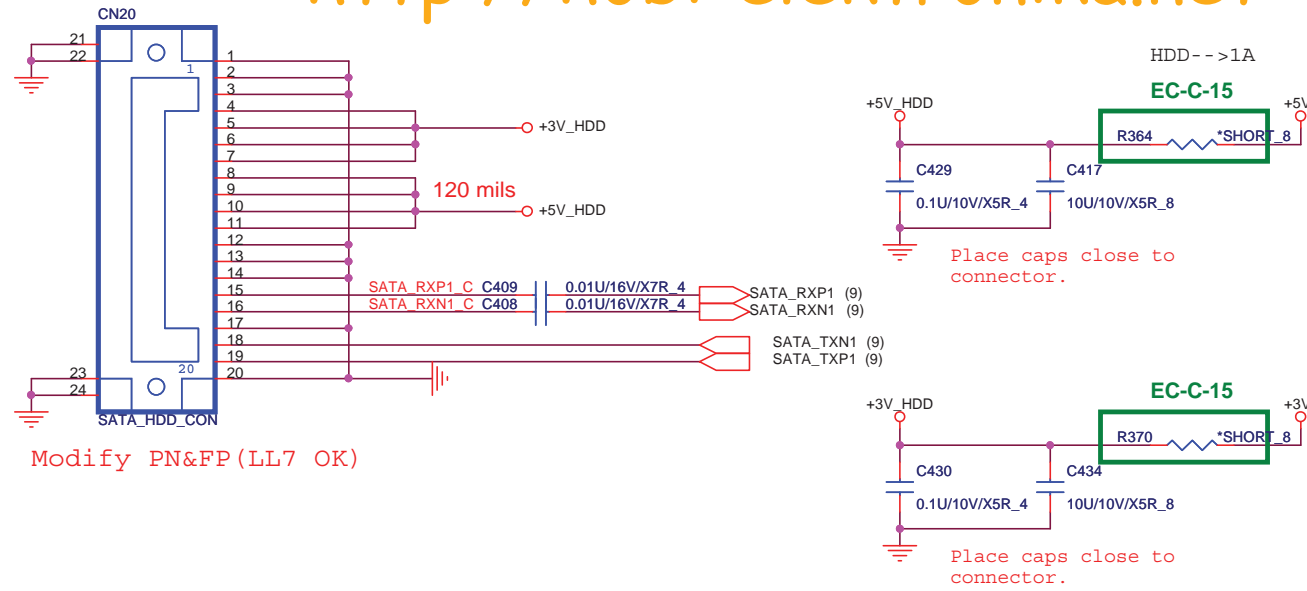




Modify P/N, F/P

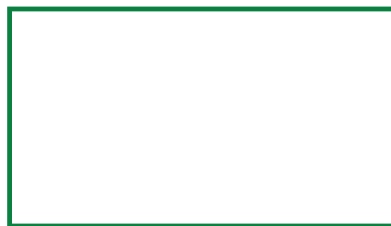
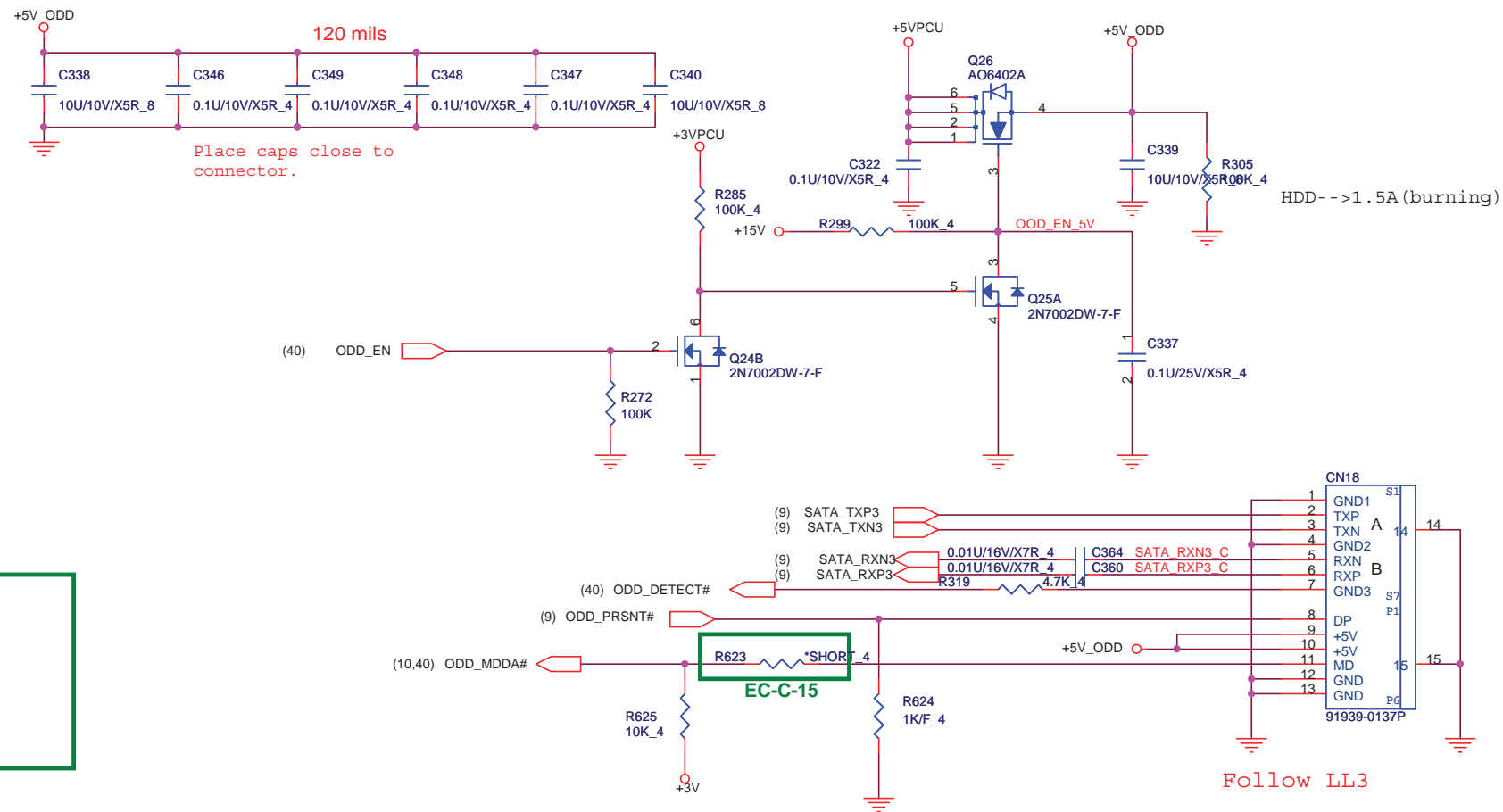
Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

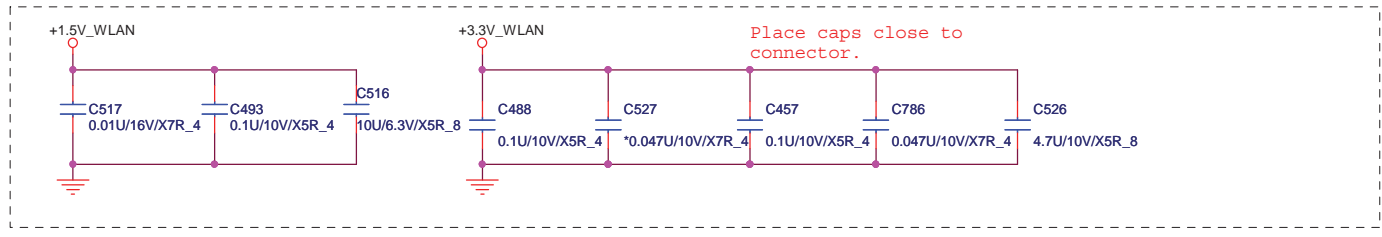
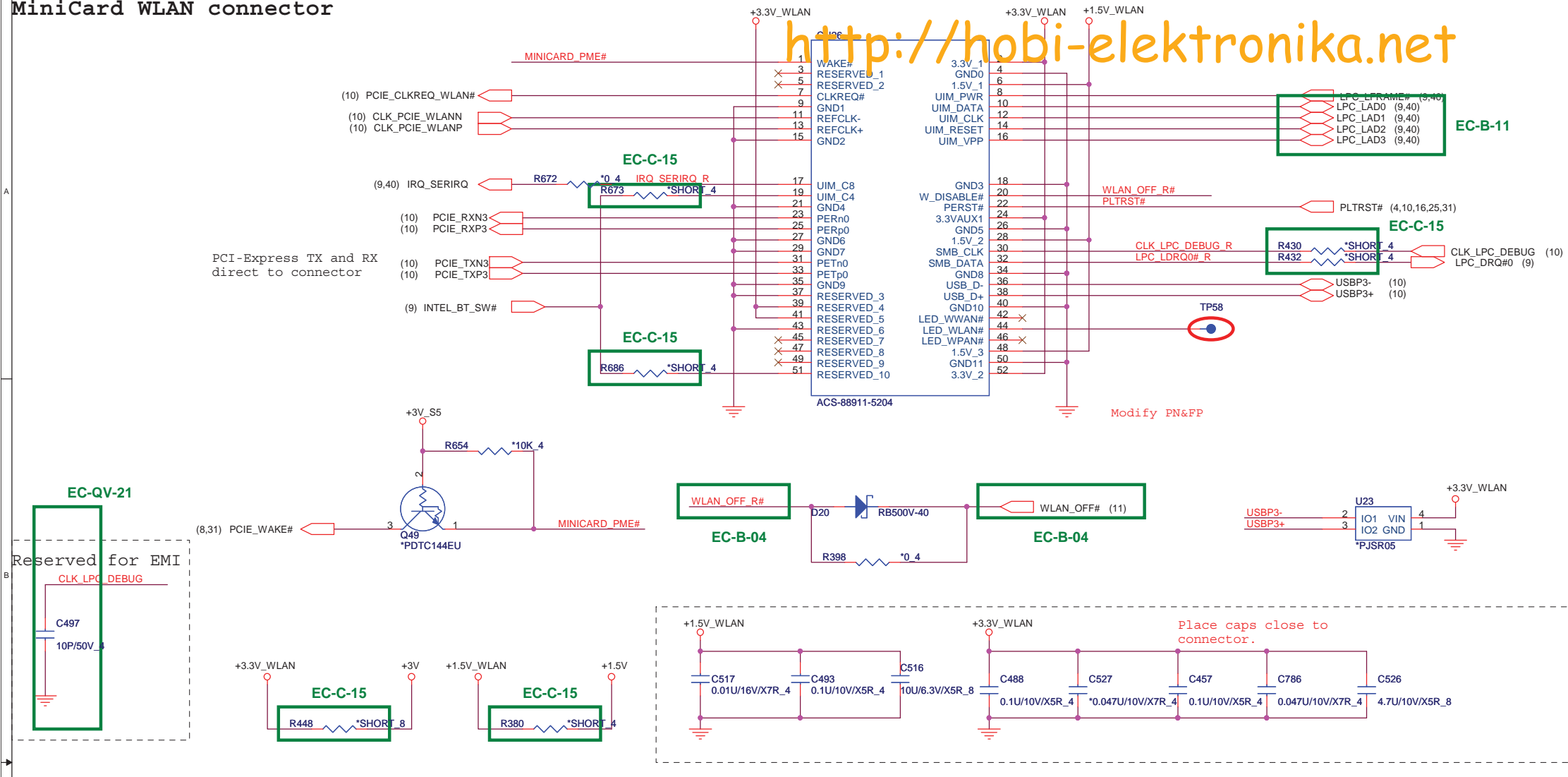




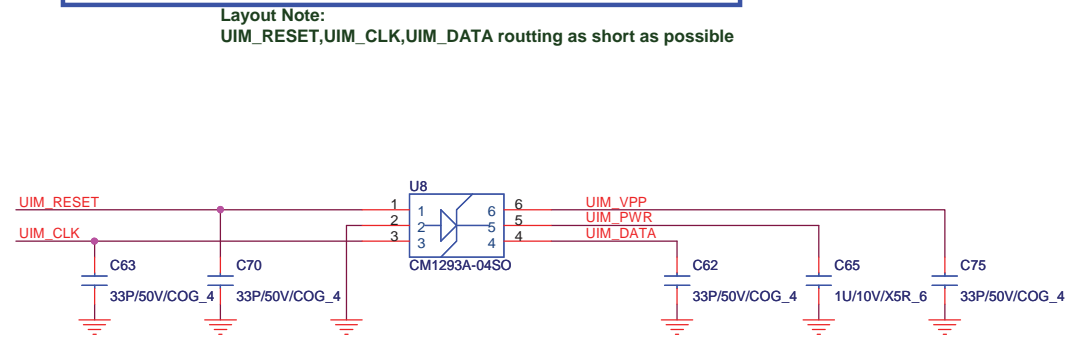
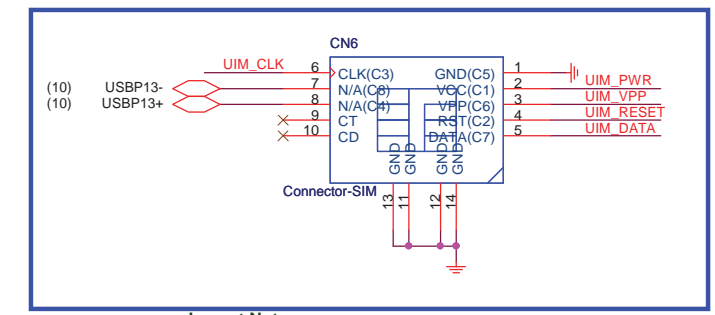
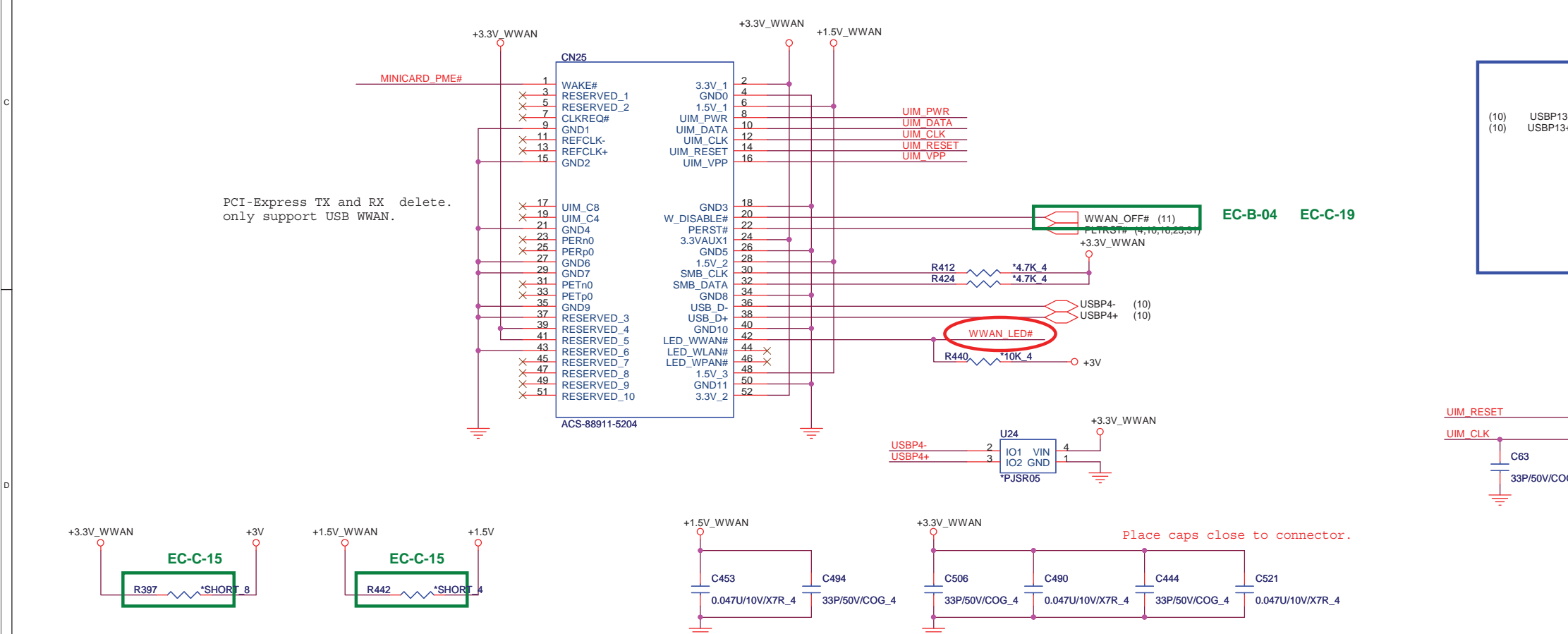
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

SATA ODD Connector.





MiniCard WWAN (Reserved for KL9)



Mini PCI-E Card 3 SSD

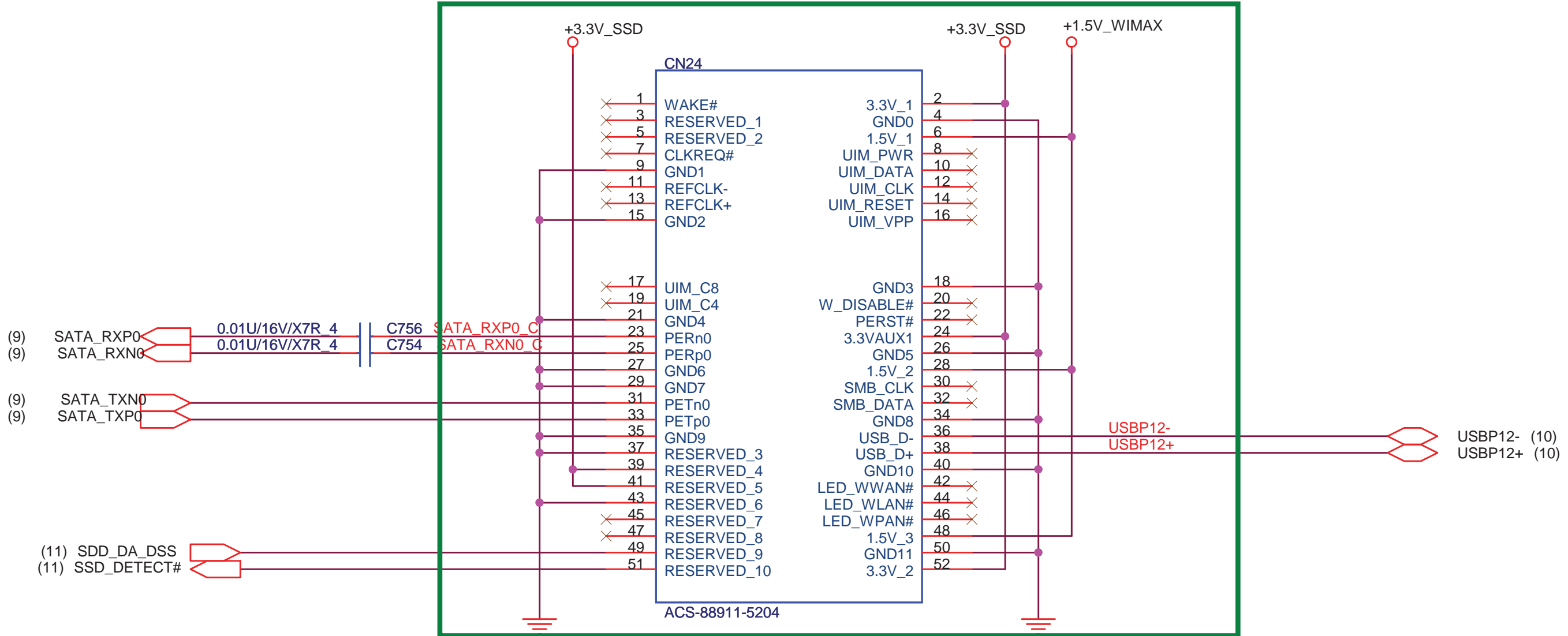
<http://hobi-elektronika.net>

(8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,31,36,37,38,40,41,42,46,47,48,49)

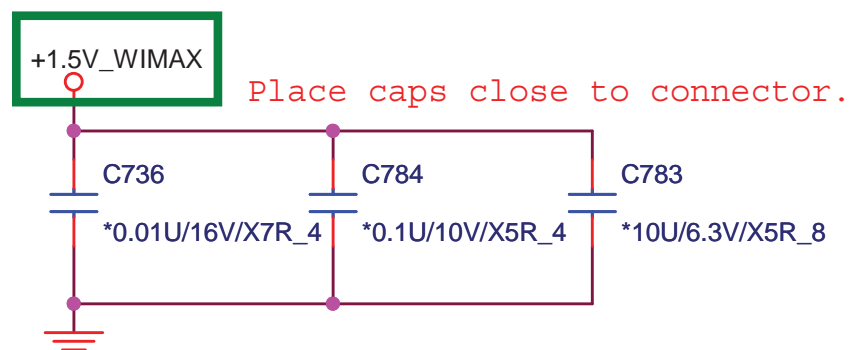
(12,29,38,41,43) +1.5V
+3V

32

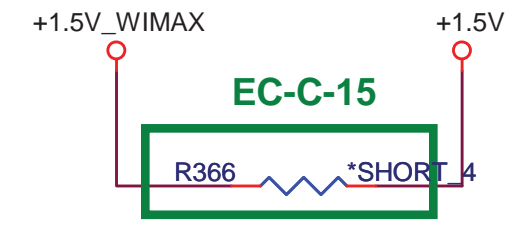
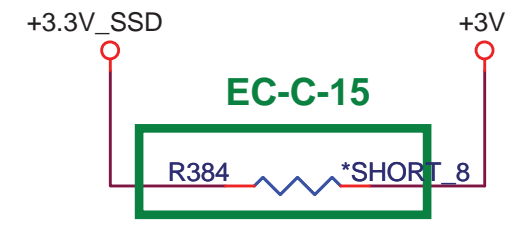
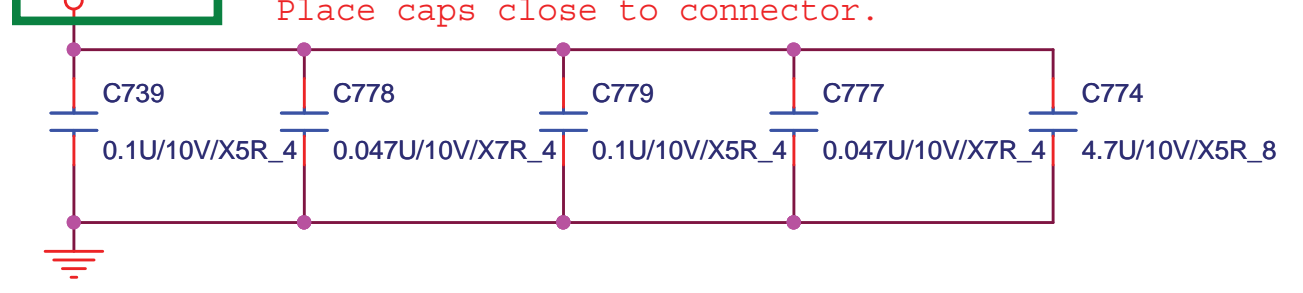
EC-B-13




EC-B-12



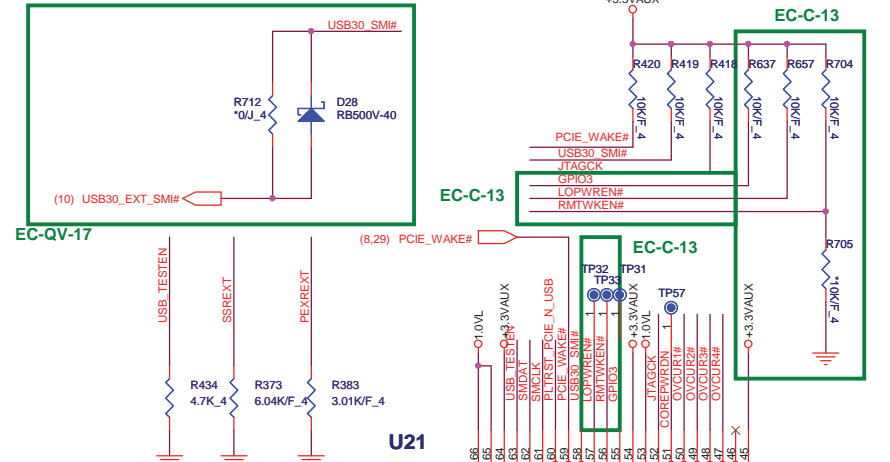
EC-B-12



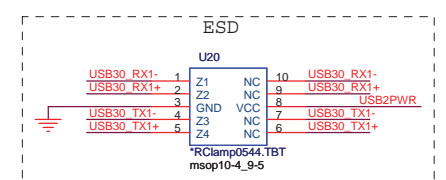
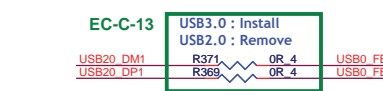


PROJECT :LL3A
Quanta Computer Inc.

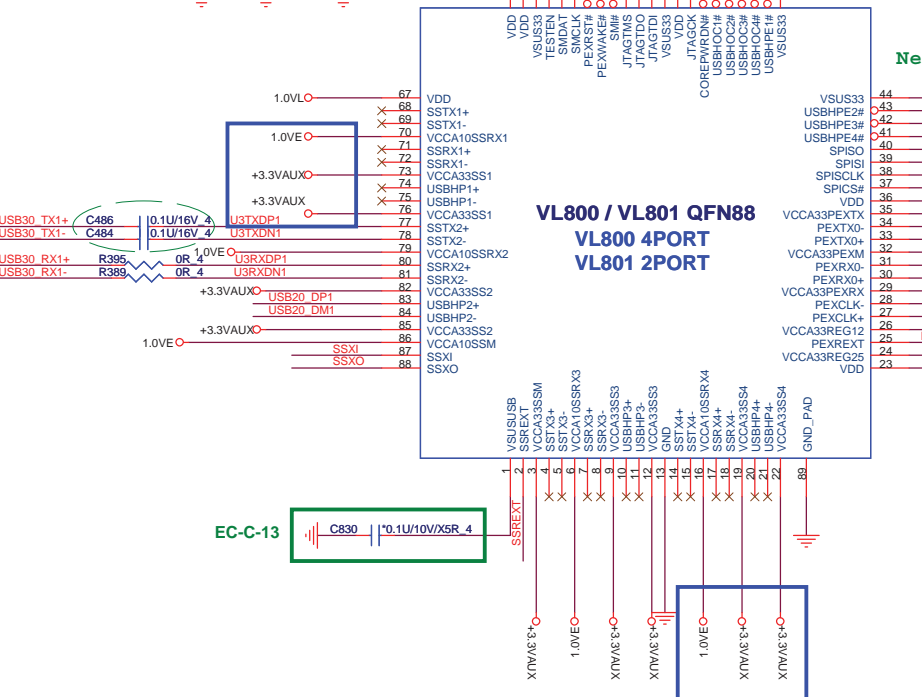
Size Custom	Document Number MINI Card (SSD)	Rev 1E
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For debug only.
Don't connect to
system SMBus

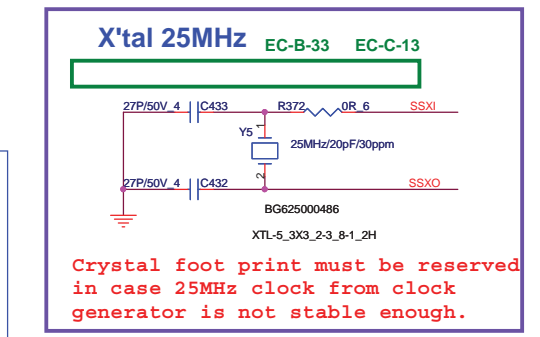
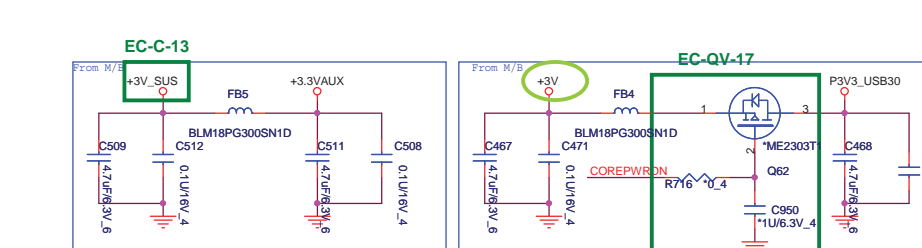
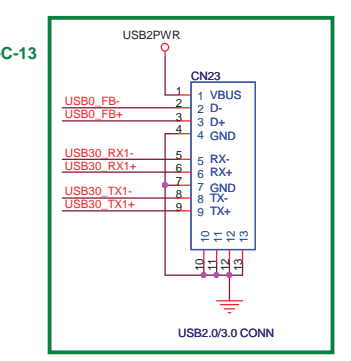
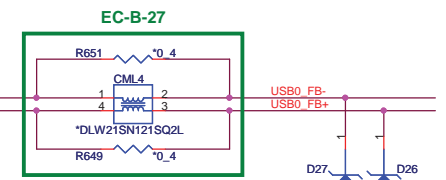


Co-layout USB
PORT for 2.0&3.0
USB 3.0 function reserved

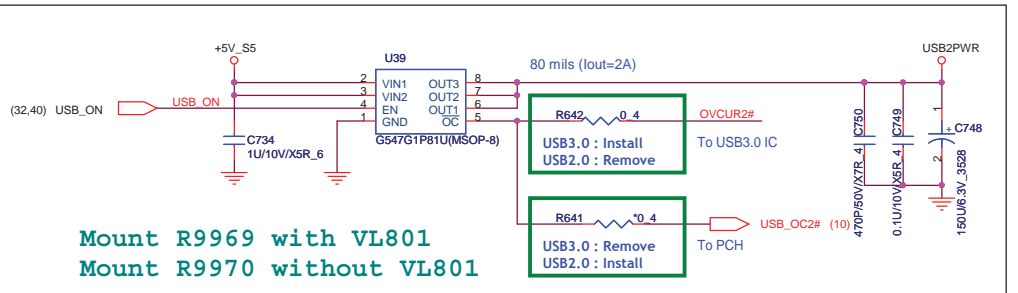


Near PCIe Slot

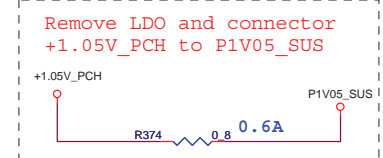
	USB3.0	USB2.0
R651	No-ASM	No-ASM
R649	No-ASM	No-ASM
CML4	No-ASM	ASM



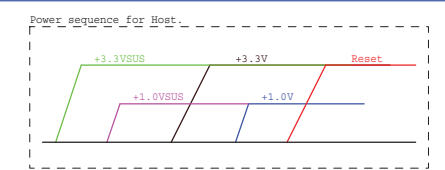
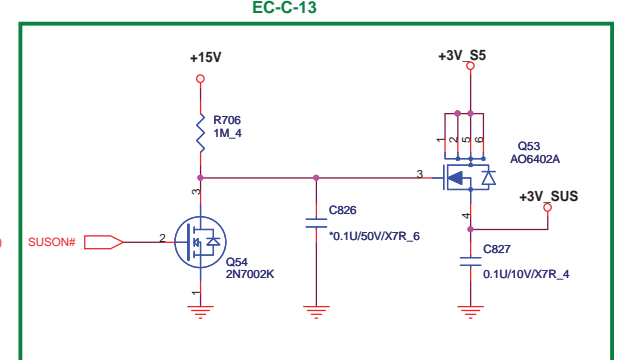
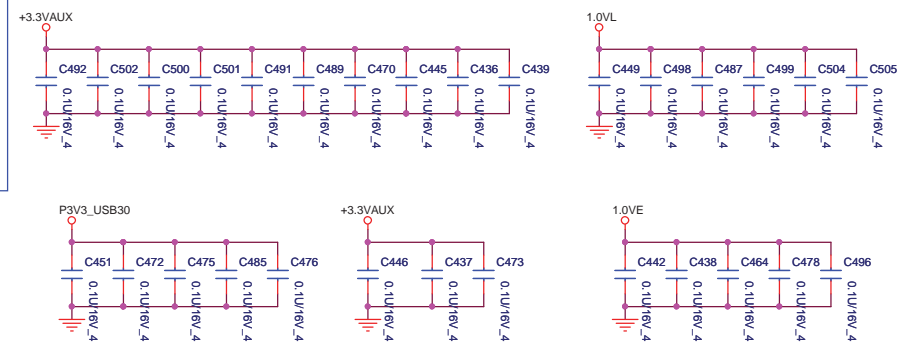
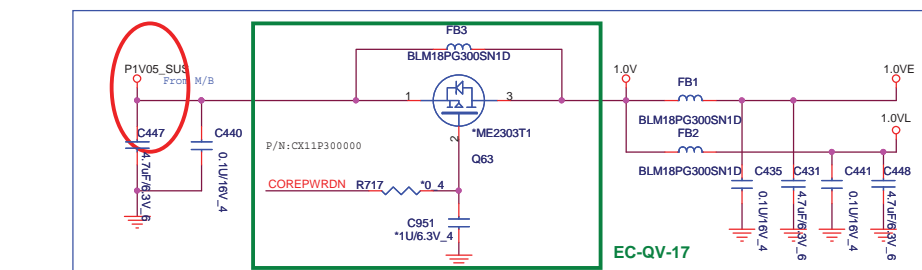
Crystal foot print must be reserved
in case 25MHz clock from clock
generator is not stable enough.



Mount R9969 with VL801
Mount R9970 without VL801

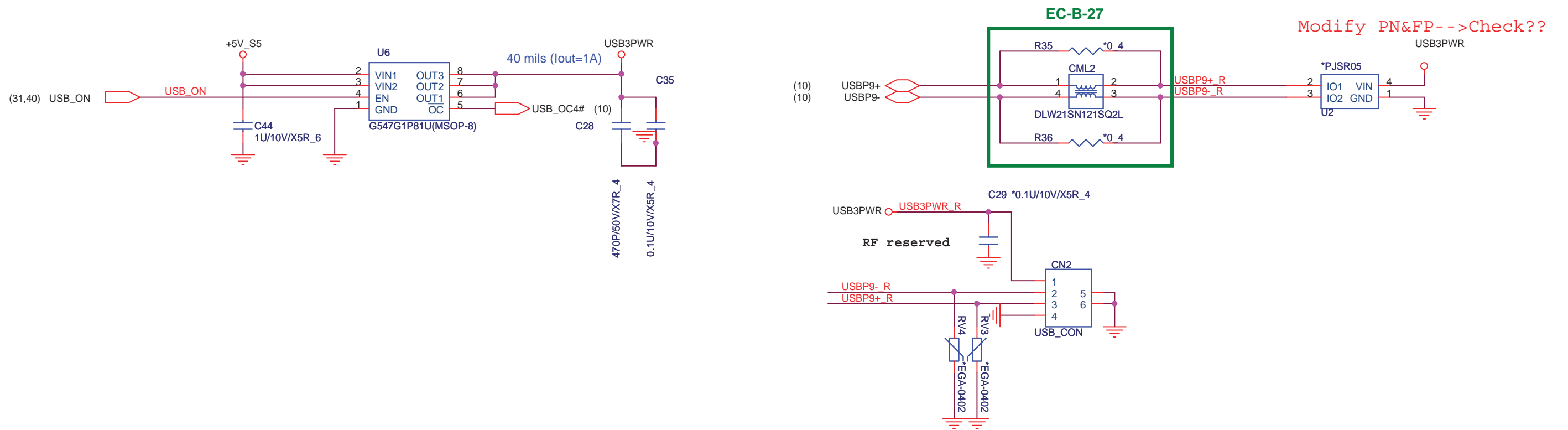


Remove LDO and connector
+1.05V_PCH to P1V05_SUS

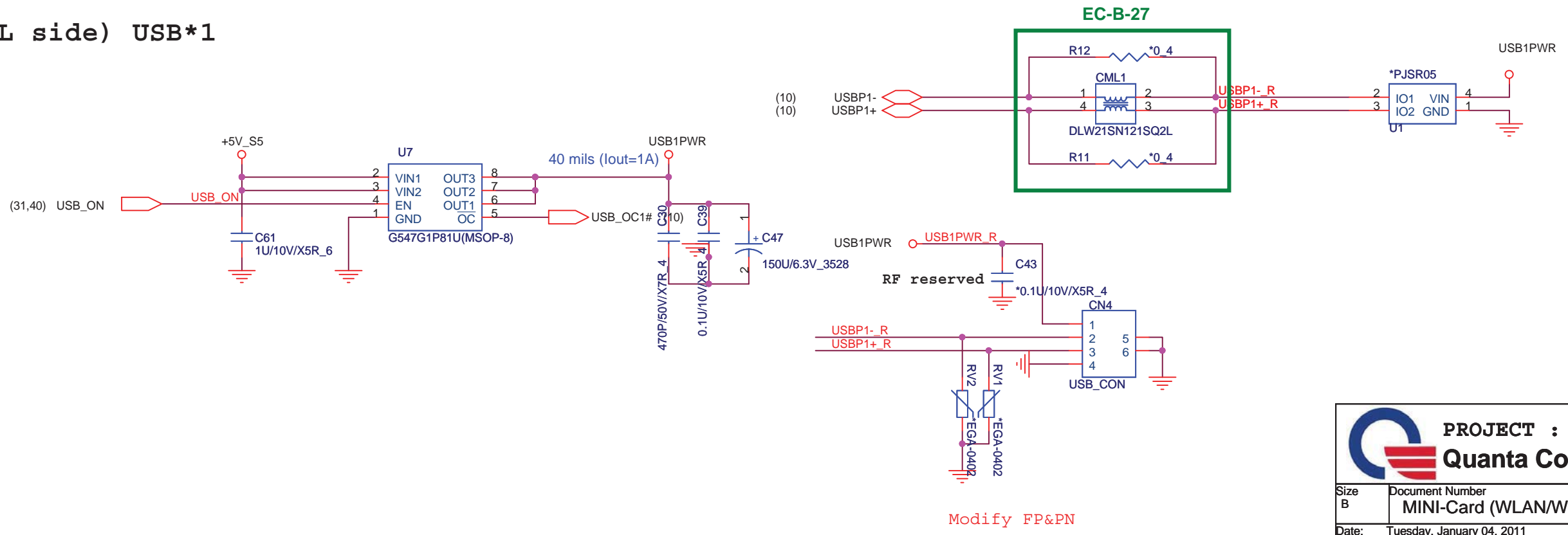


USB2.0*2

External (R side) USB*1



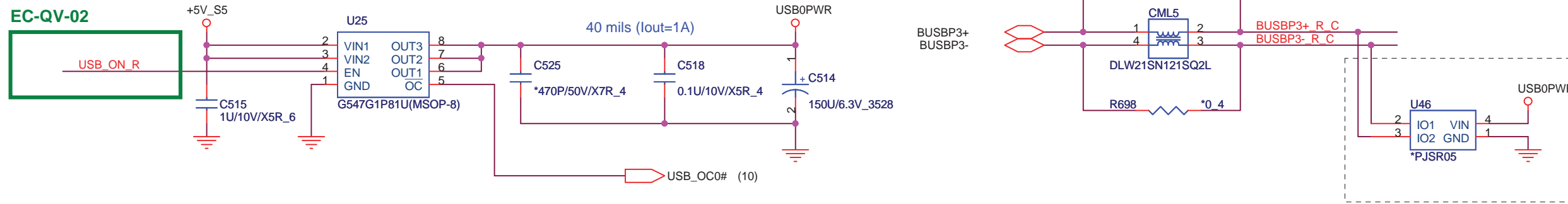
External (L side) USB*1



PROJECT : KL2D
Quanta Computer Inc.

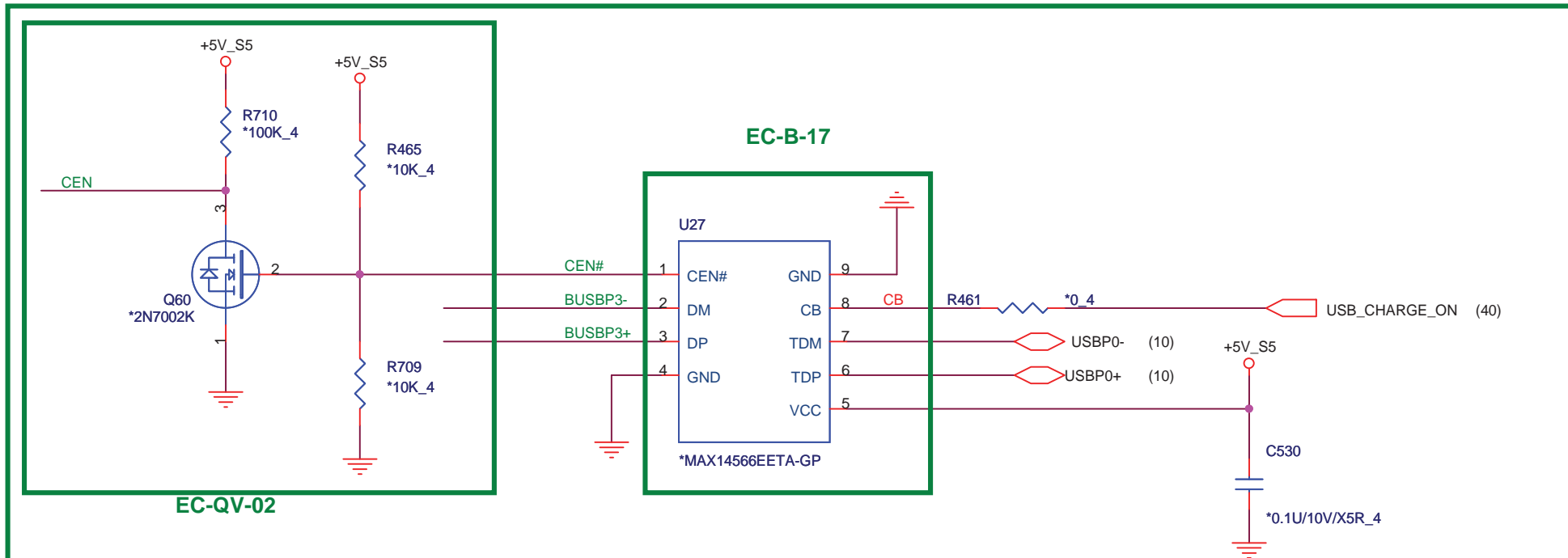
Size B	Document Number MINI-Card (WLAN/WWAN)	Rev 1A
Date: Tuesday, January 04, 2011	Sheet 32 of 53	

EC-QV-02



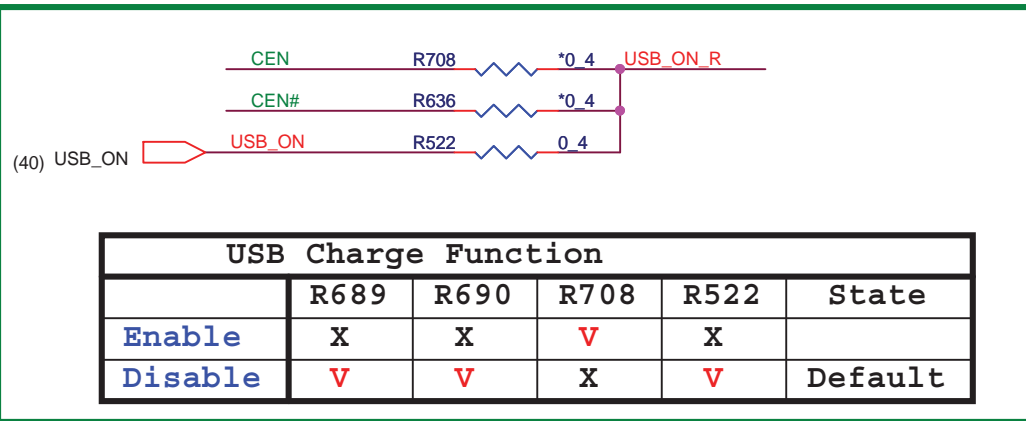
USB charger

EC-B-38

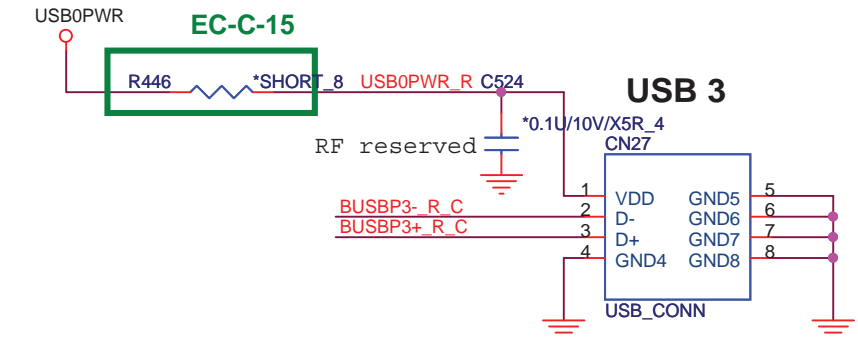


EC-QV-02

EC-QV-02



Stuff for bypass USB charger



G-SENSOR (3-Axial)

<http://hobi-elektronika.net>

(8,9,10,11,12,13,15,17,22,31,24,26,27,28,29,30,31,36,37,38,40,41,42,46,47,48,49) +3V
(24,28,31,38,41,43,44,45) +15V

+3V
+15V



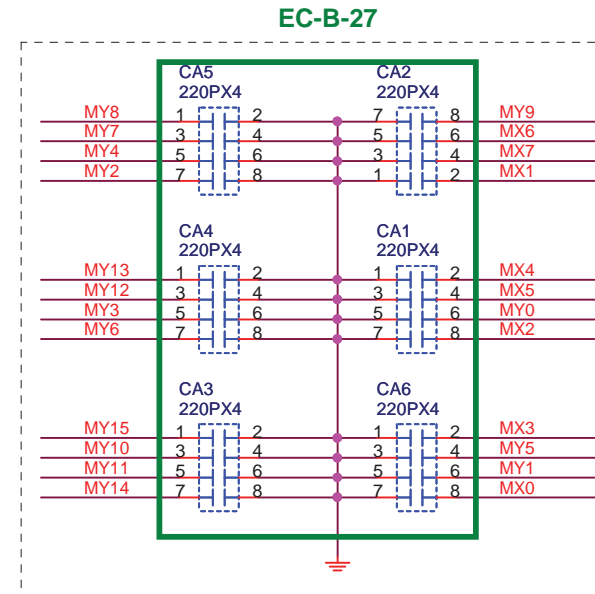
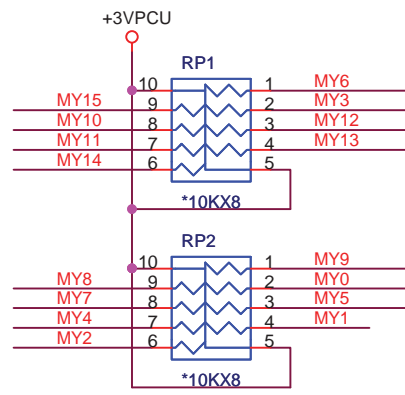
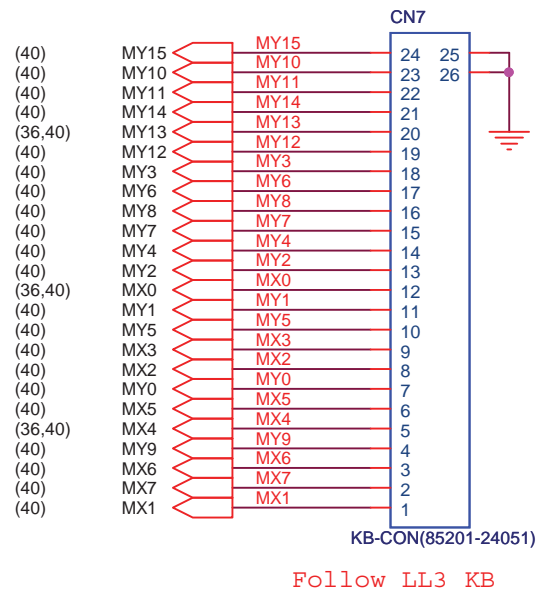
36

EC-B-18



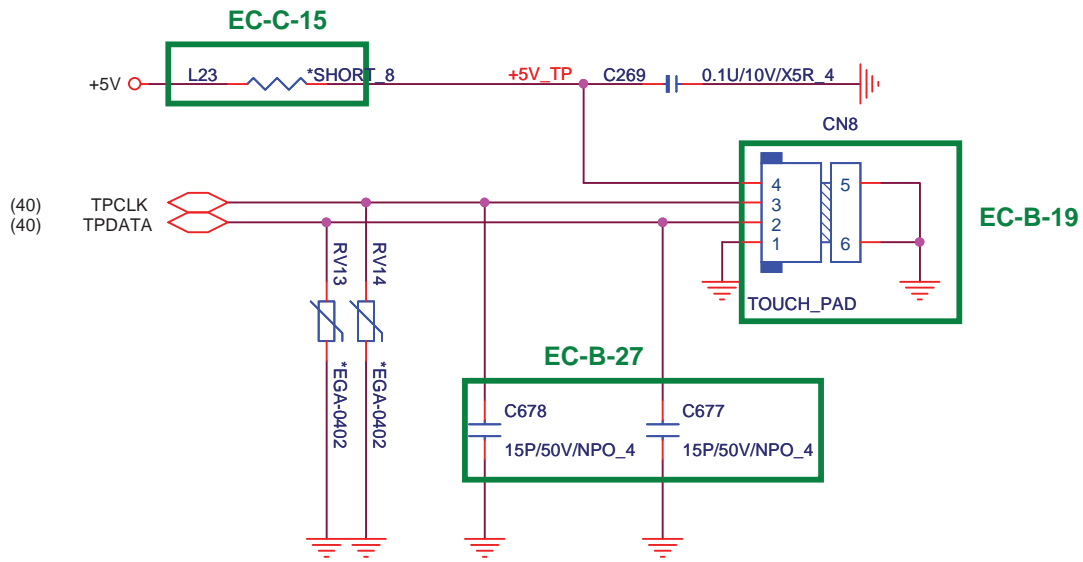
PROJECT : LL3A
Quanta Computer Inc.

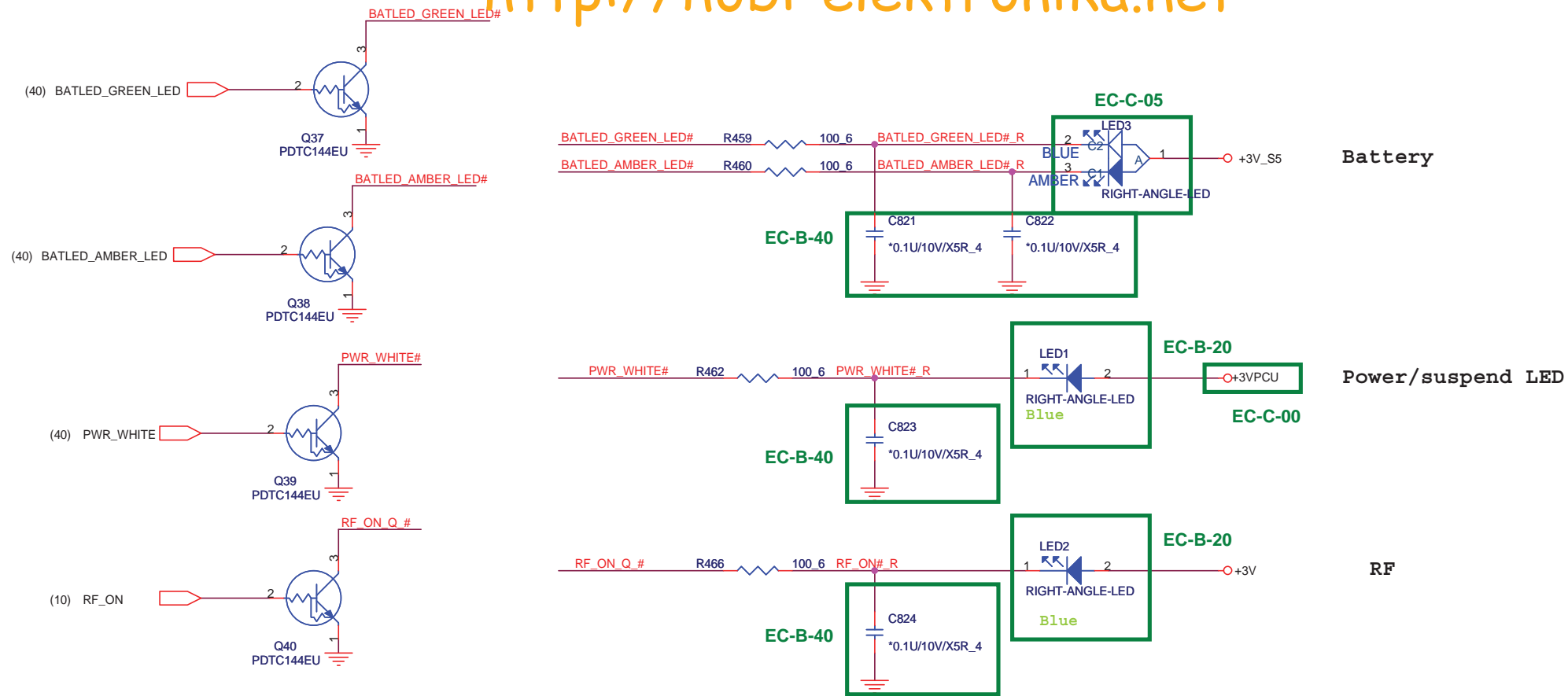
Size Custom	Document Number G-SENSOR	Rev 1E
Date: Tuesday, January 04, 2011	Sheet 34	of 53



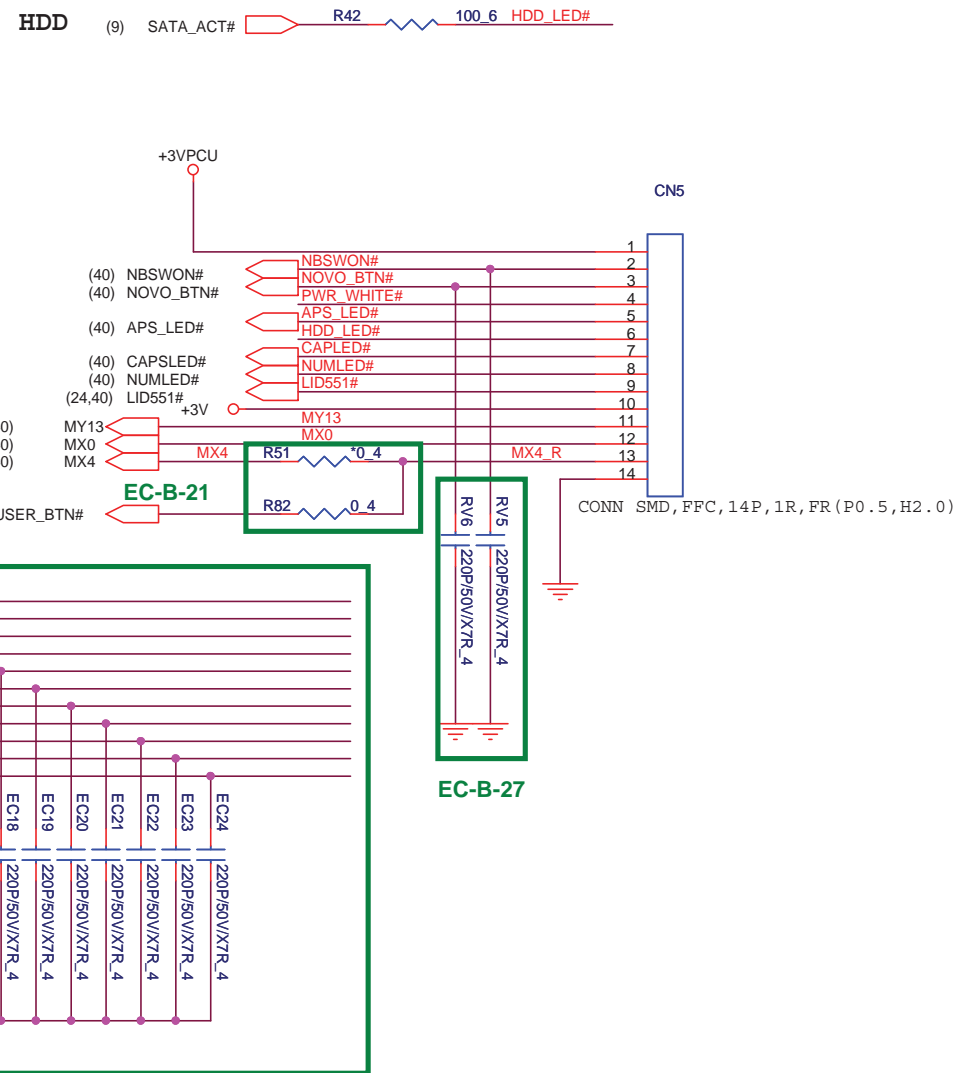
For EMI request

Touch pad

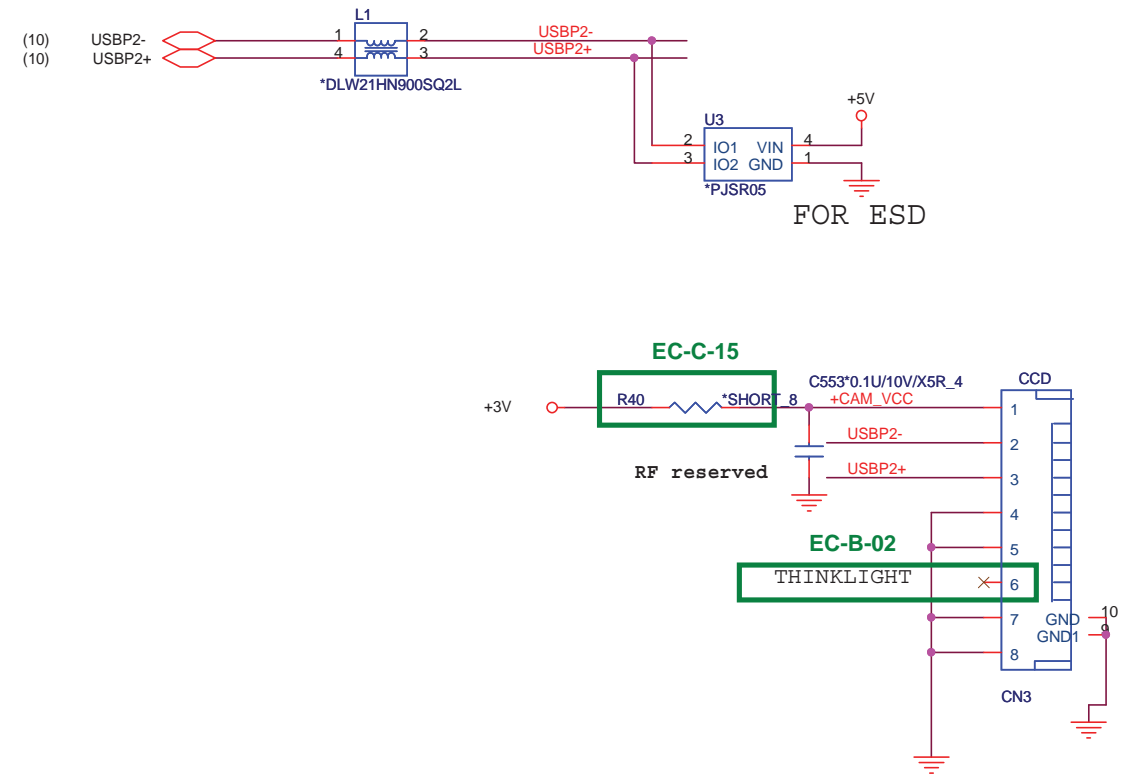


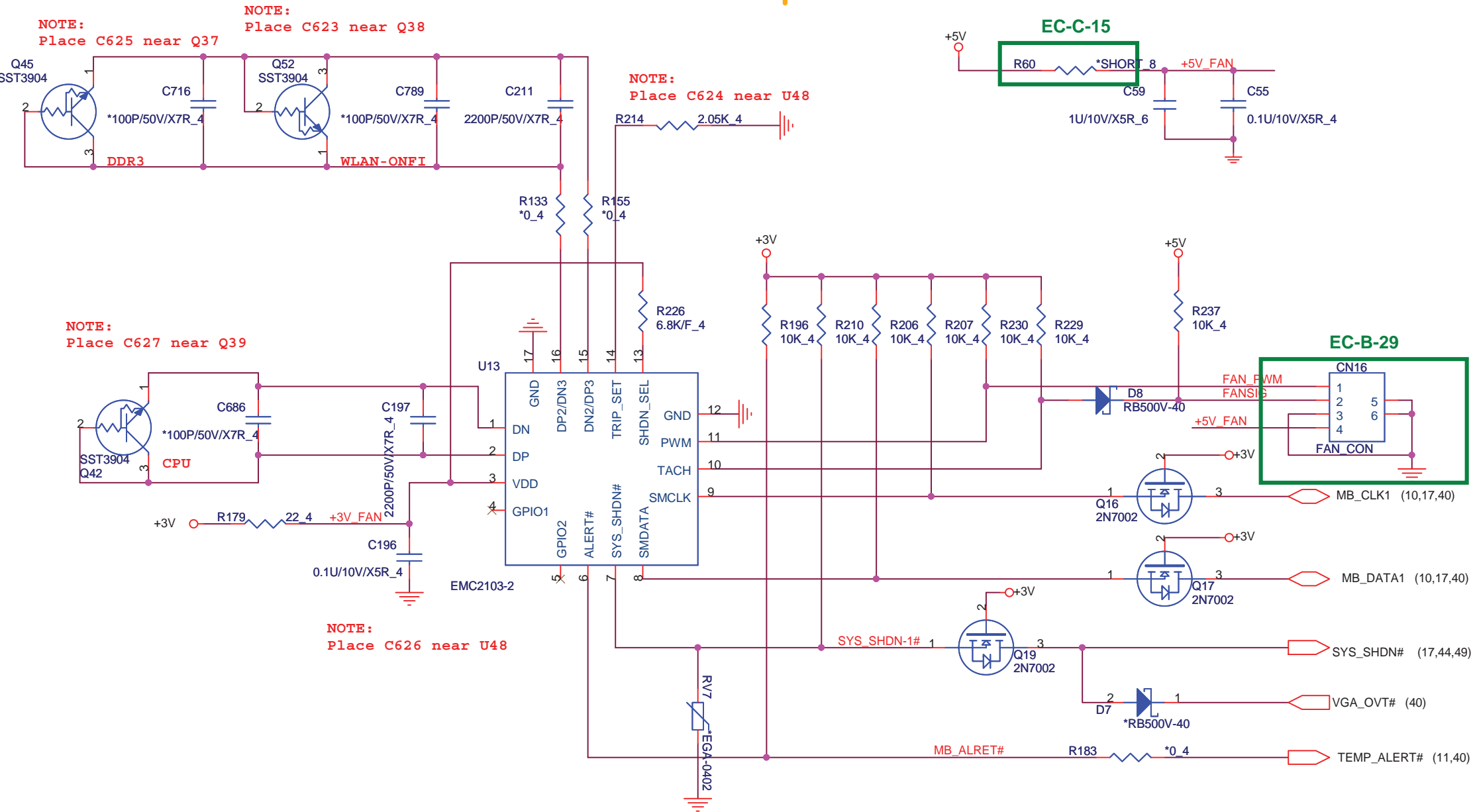


B to B connector



CAMERA & Keyboard light






NOTE: Place C625 near Q37

NOTE: Place C623 near Q38

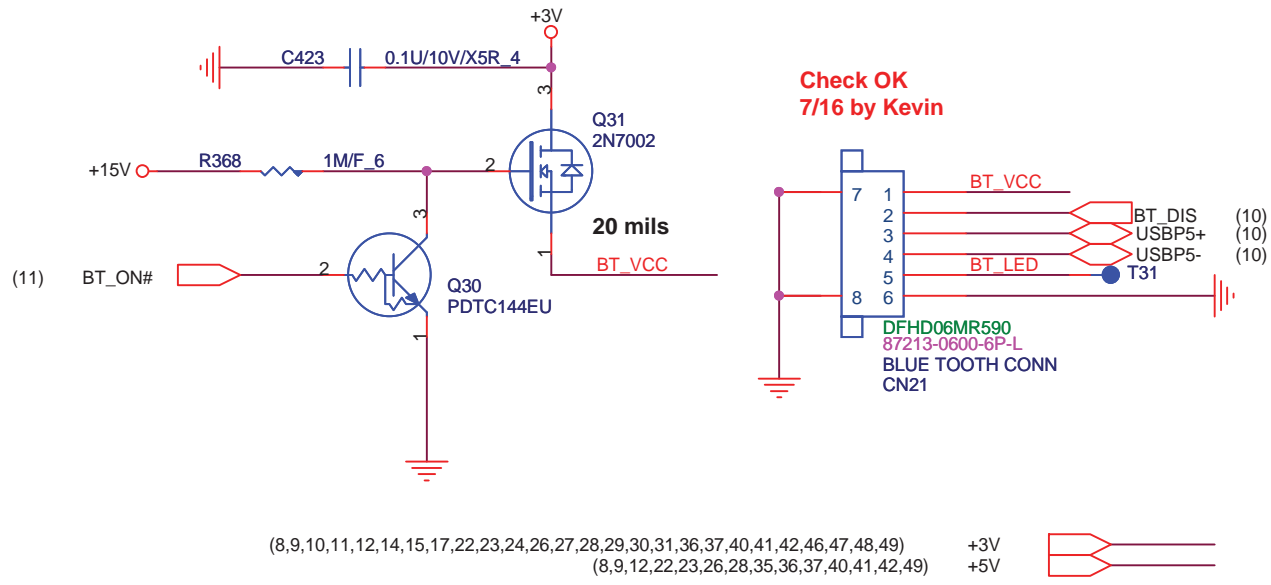
NOTE: Place C624 near U48

NOTE: Place C627 near Q39

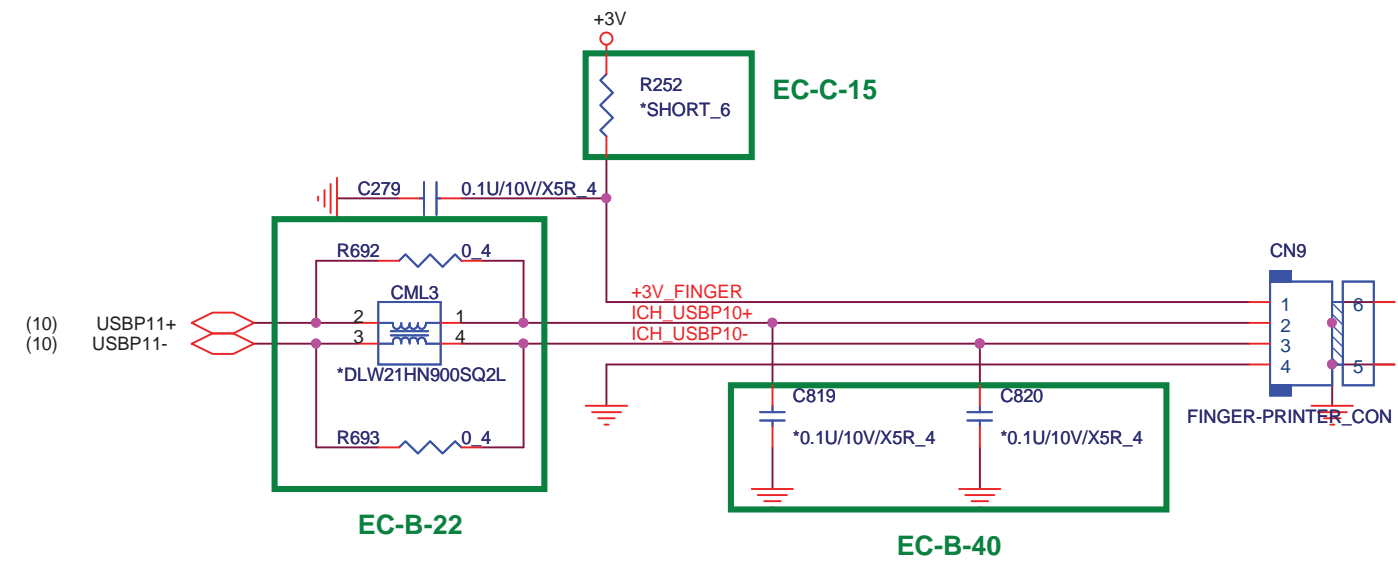
NOTE: Place C626 near U48

 PROJECT KL5A Quanta Computer Inc.		
Size B	Document Number FAN / THERMAL	Rev 1A
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Sheet 37 of 53		

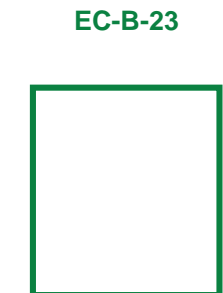
BLUETOOTH



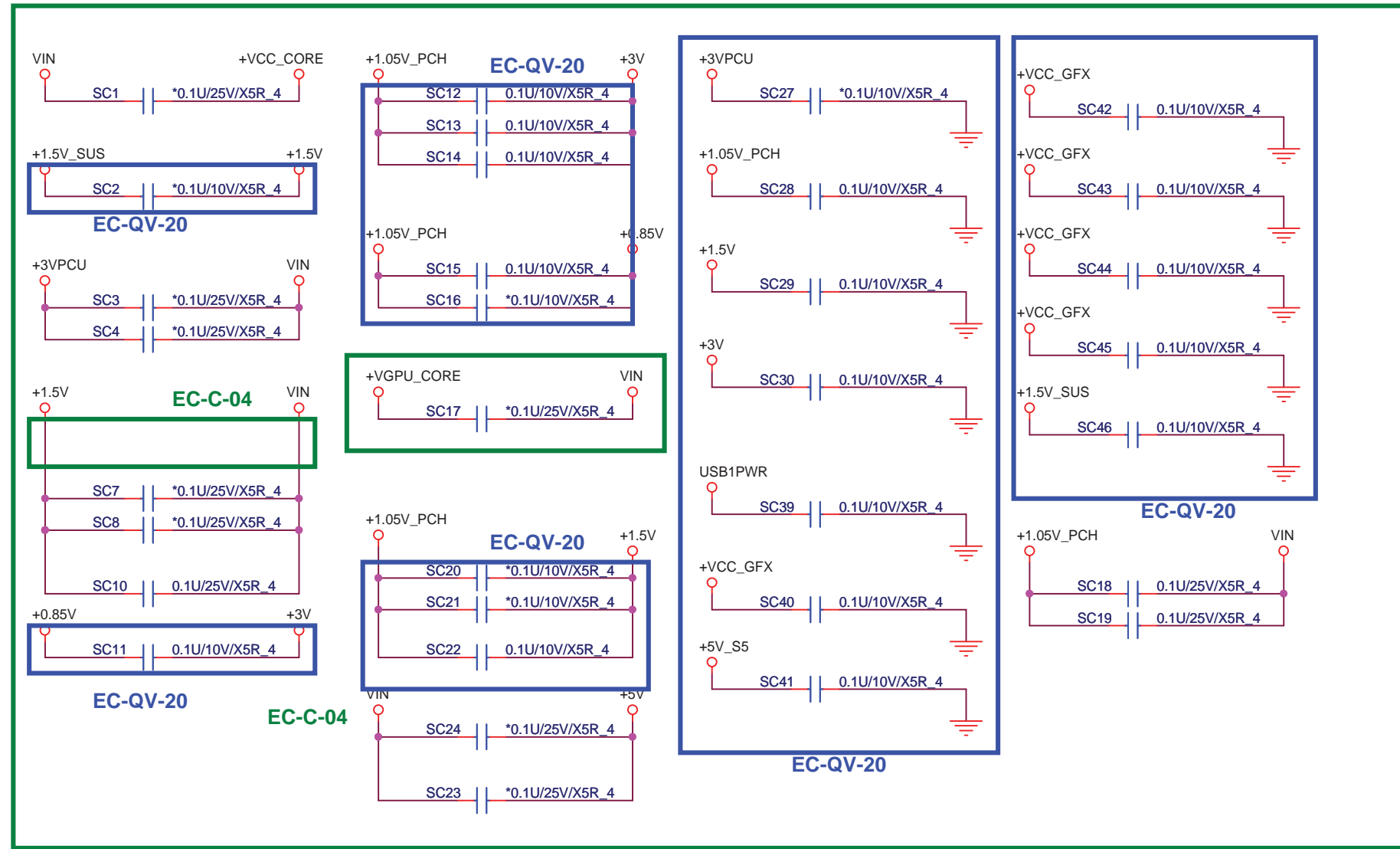
FINGER PRINTER



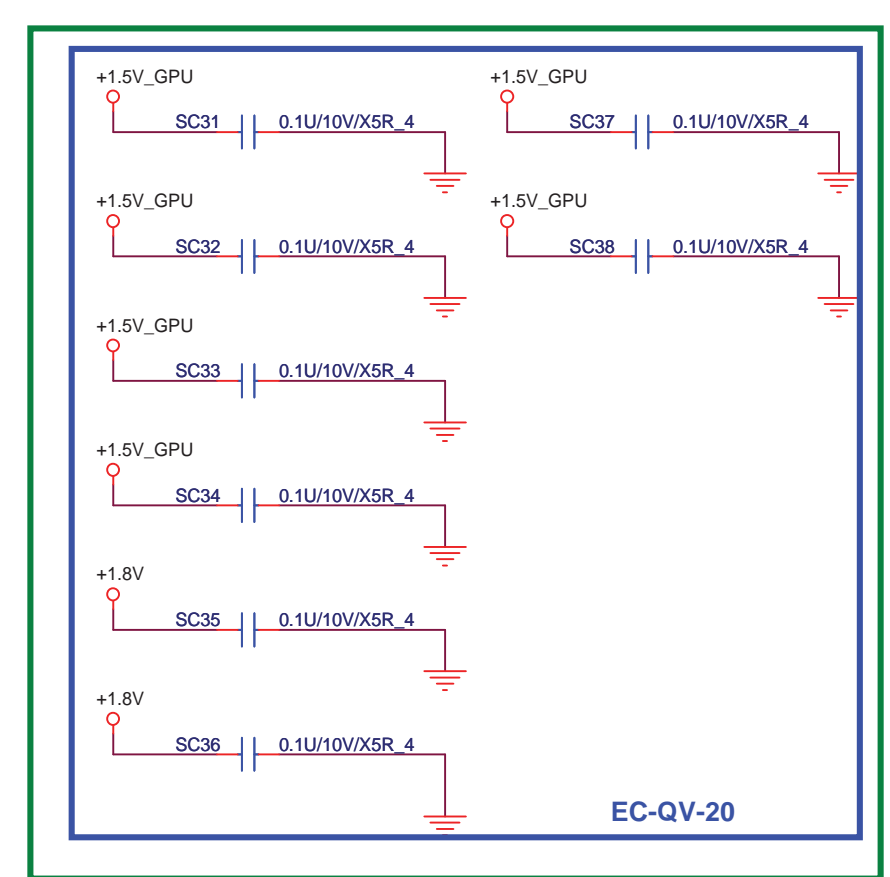
TPM



ESD suggestions

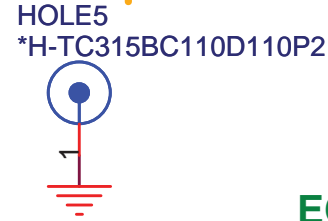
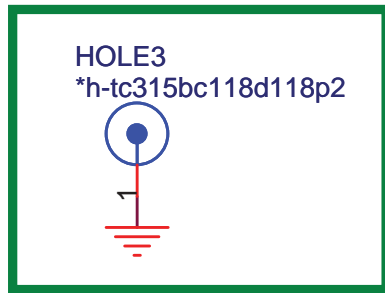


EMI suggestions

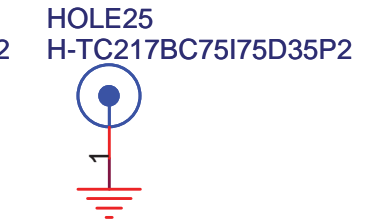
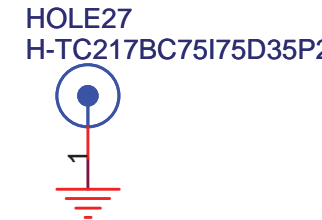
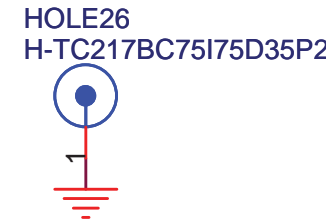
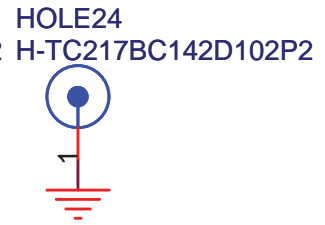
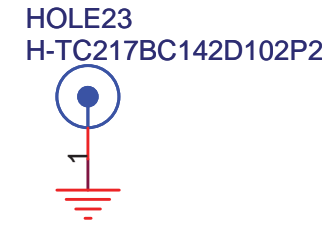
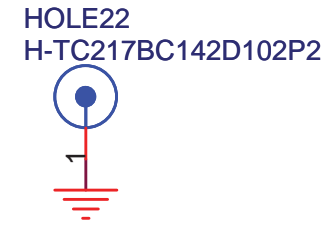
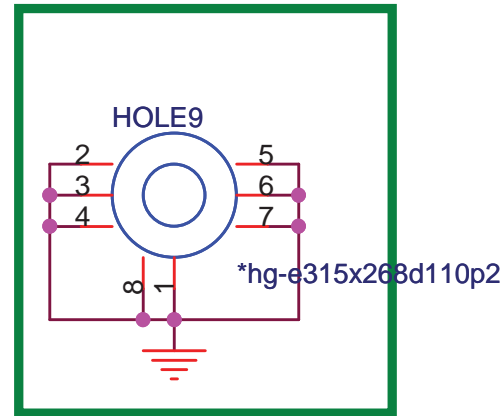


WLAN/WWAN/Mini-SSD Nuts

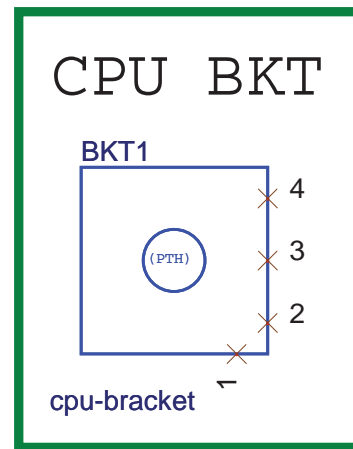
EC-B-37



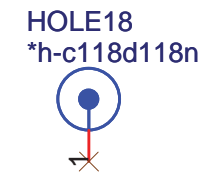
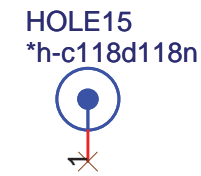
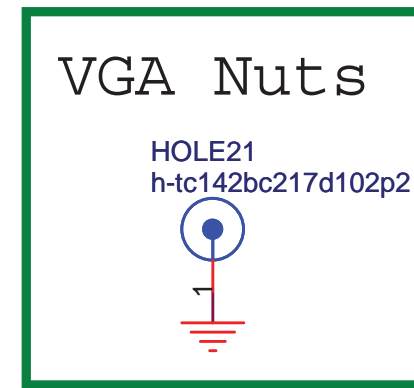
EC-C-02



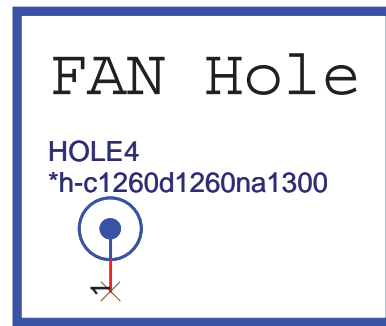
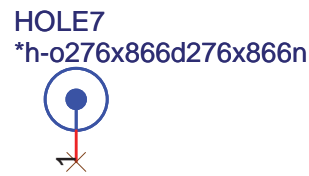
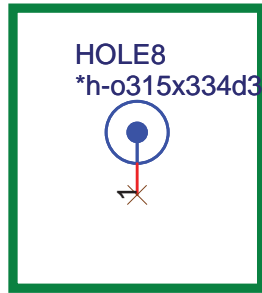
EC-B-40



EC-B-37

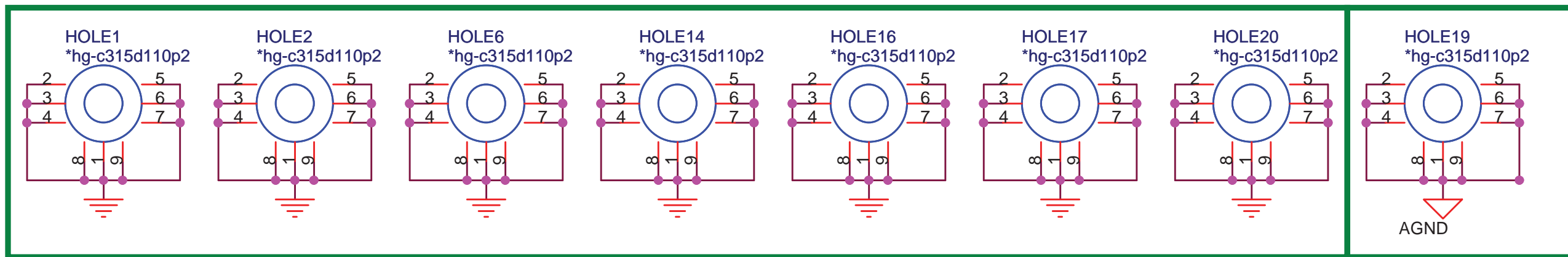



EC-QV-16

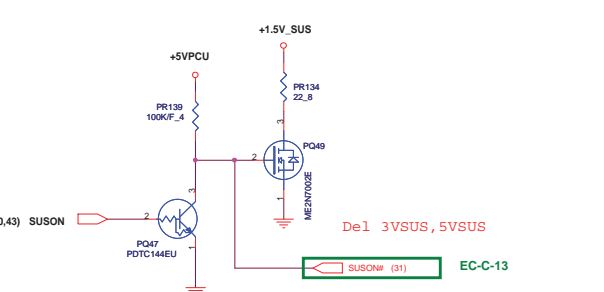
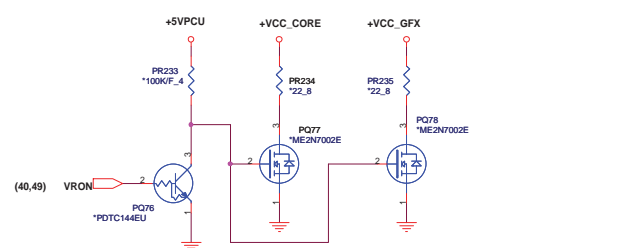
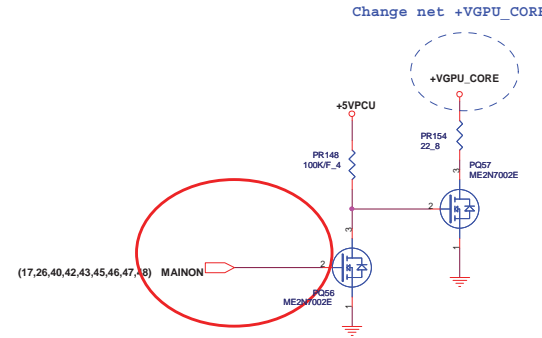
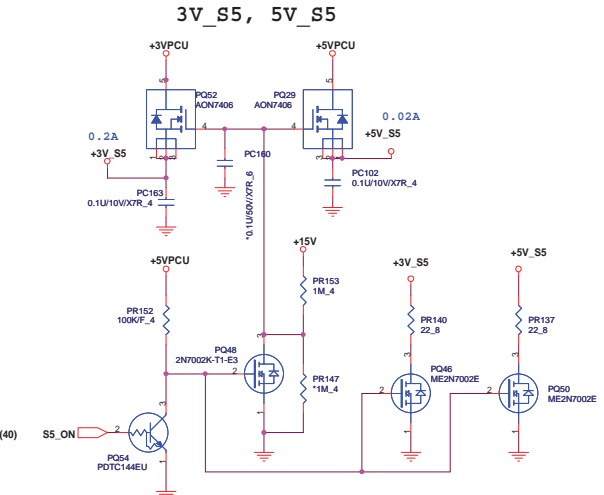
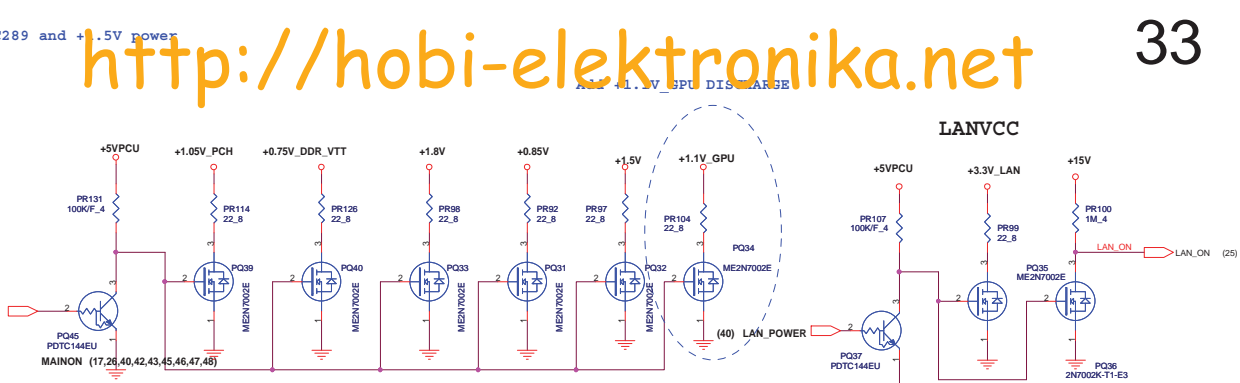
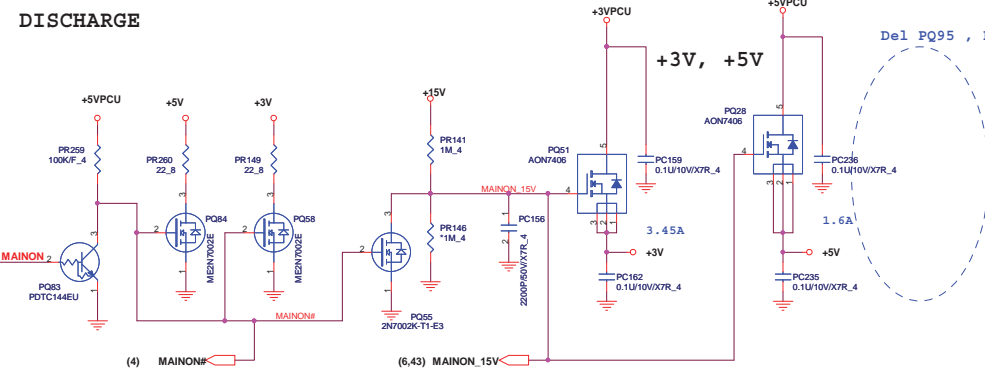


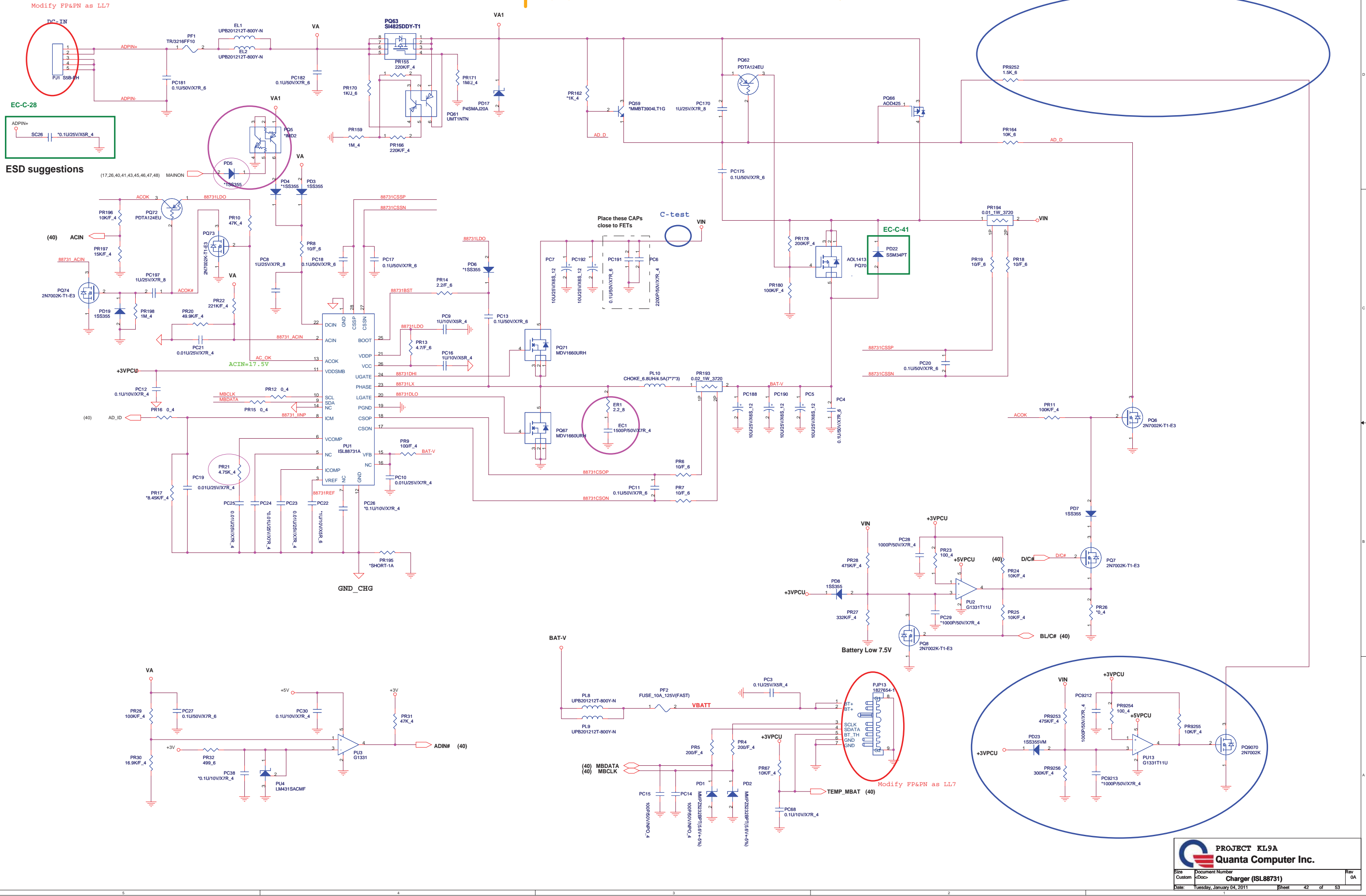
EC-C-02

EC-B-40 EC-C-02



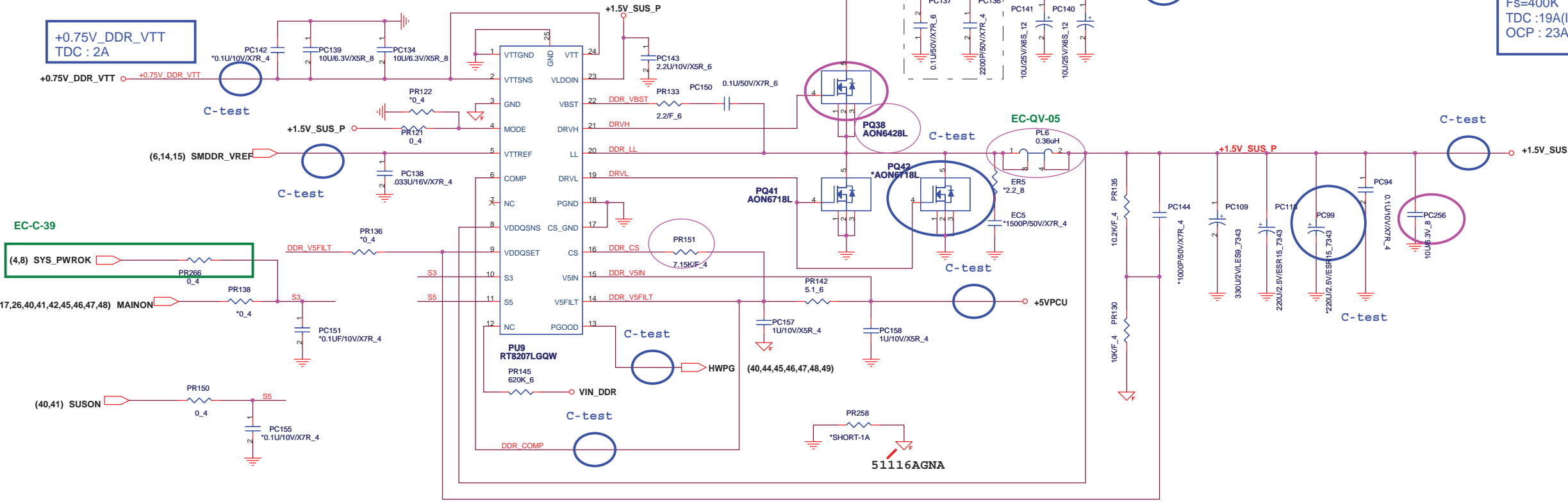
 PROJECT : KL2D Quanta Computer Inc.		
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Place these CAPS close to FETs

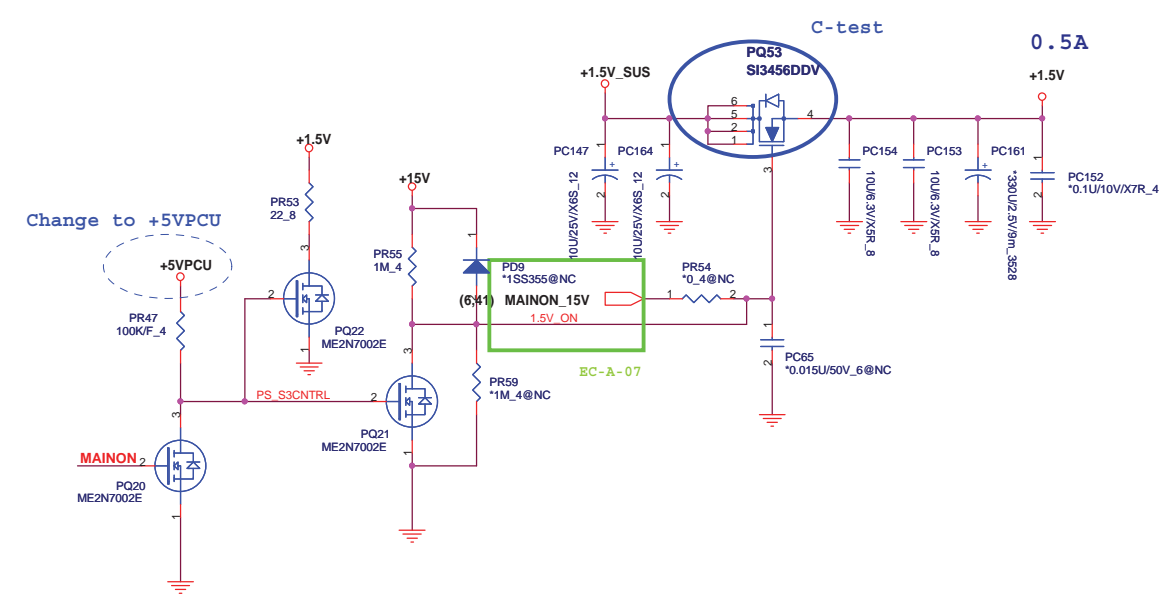
+1.5V_SUS
Fs=400K
TDC :19A(I_{max})
OCP : 23A



EC-C-39
(4,8) SYS_PWROK

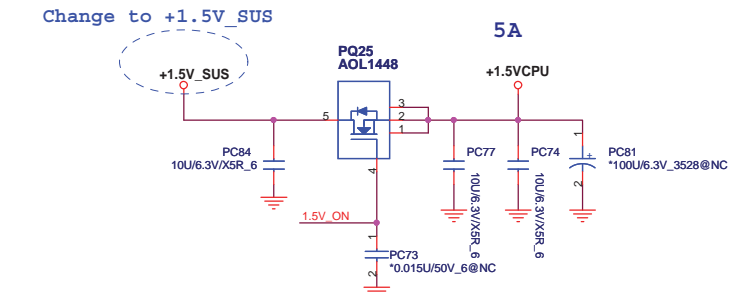
(17,26,40,41,42,45,46,47,48) MAINON

(40,41) SUSON



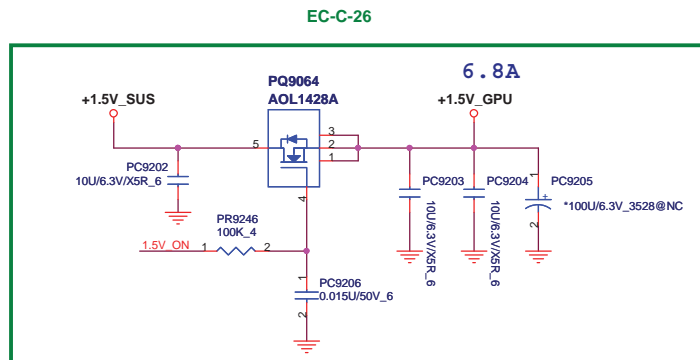
Change to +5VPCU

MAINON₂



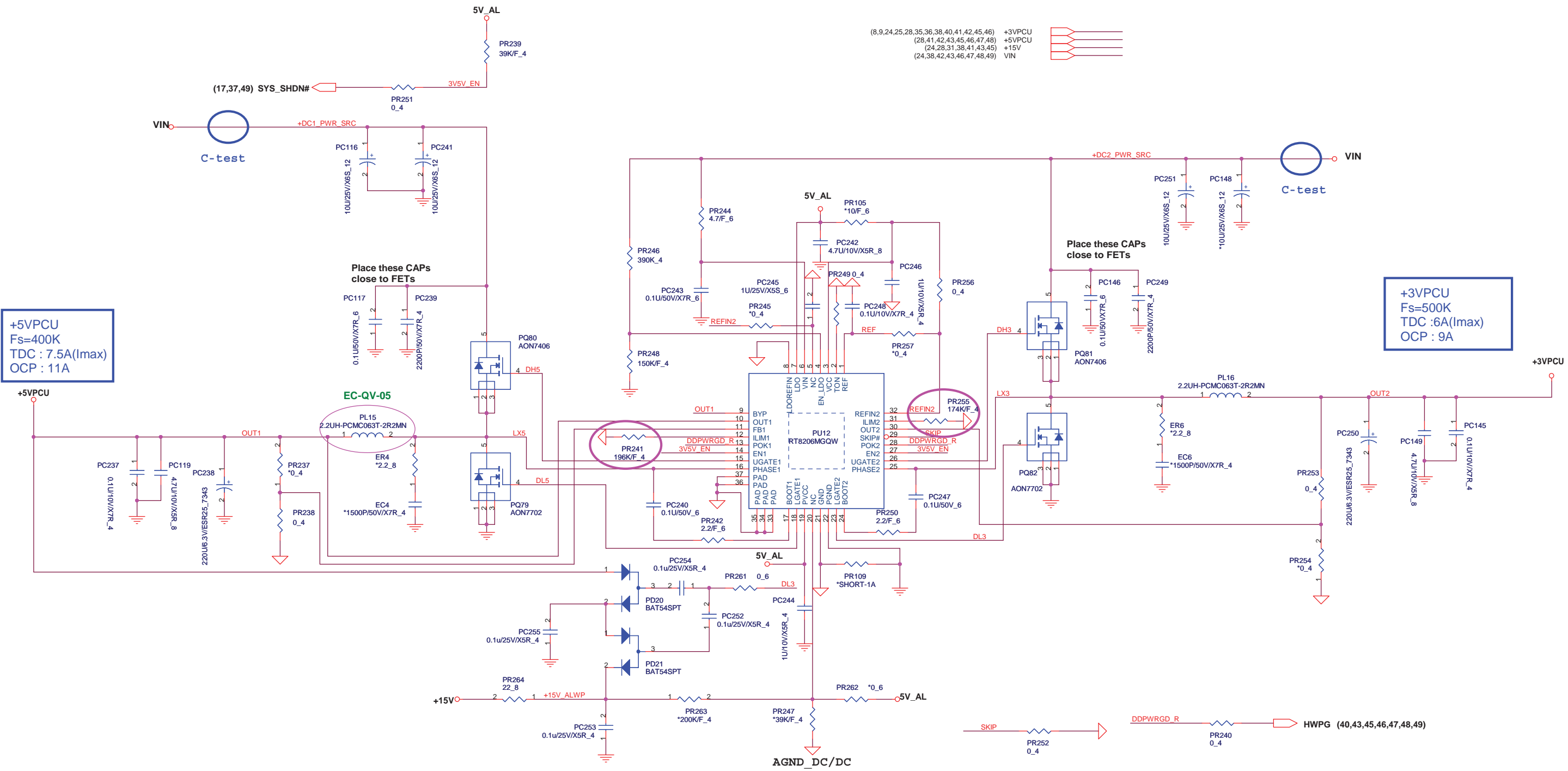
Change to +1.5V_SUS

5A

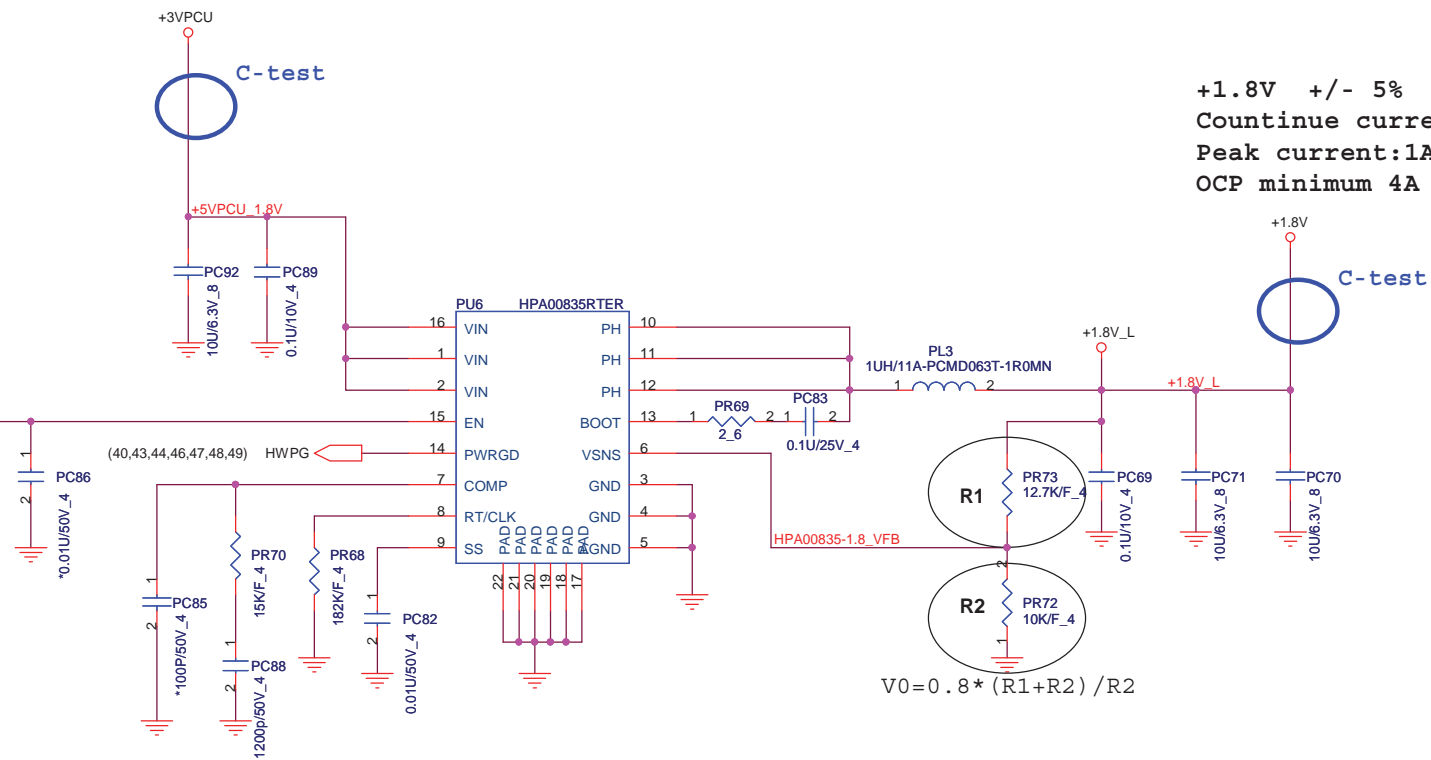


EC-C-26

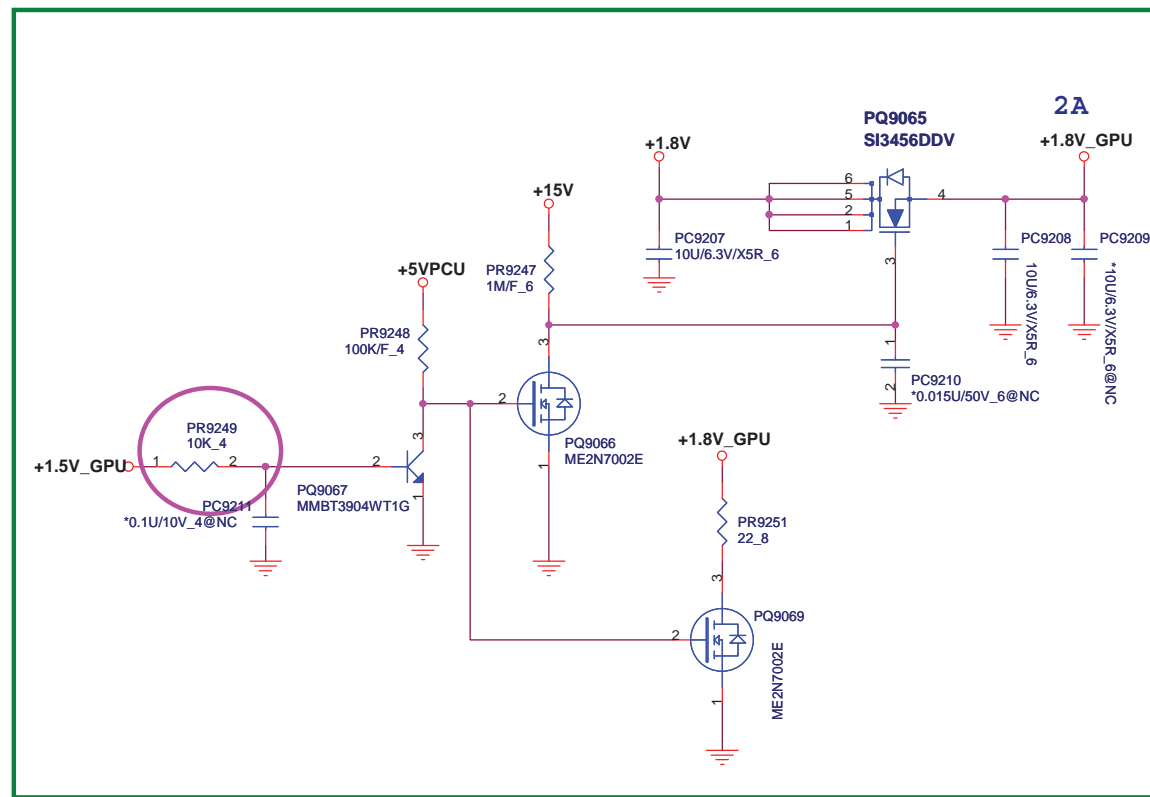
6.8A



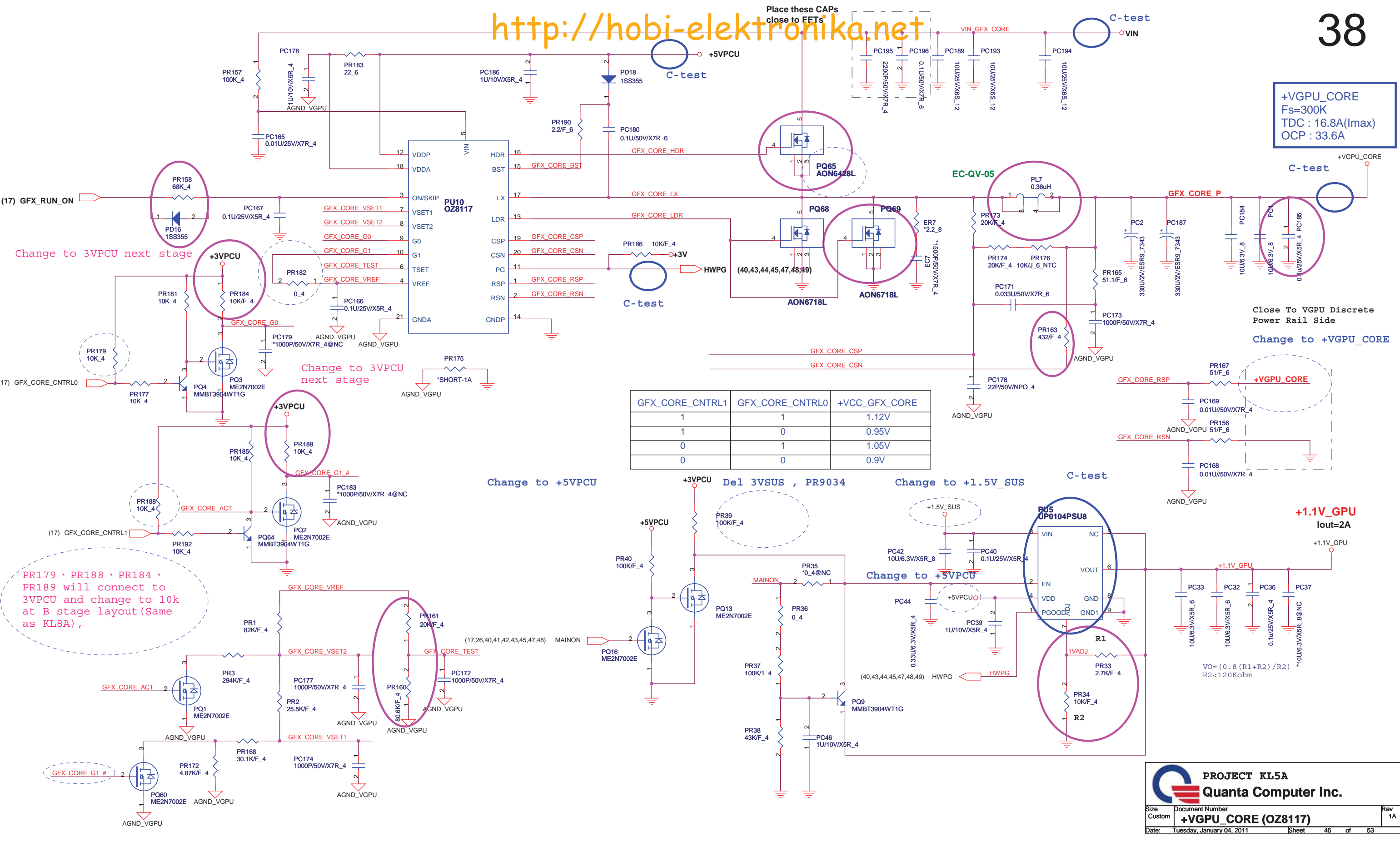
+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A
OCP minimum 4A



EC-C-26



Place these CAPs close to FETs



+VGPU_CORE
 Fs=300K
 TDC : 16.8A(I_{max})
 OCP : 33.6A

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
1	1	1.12V
1	0	0.95V
0	1	1.05V
0	0	0.9V

Change to 3VPCU next stage

Change to 3VPCU next stage

Change to +5VPCU

Del 3VSUS , PR9034

Change to +1.5V_SUS

Change to +5VPCU

PR179 , PR188 , PR184 , PR189 will connect to 3VPCU and change to 10k at B stage layout (Same as KL8A) ,

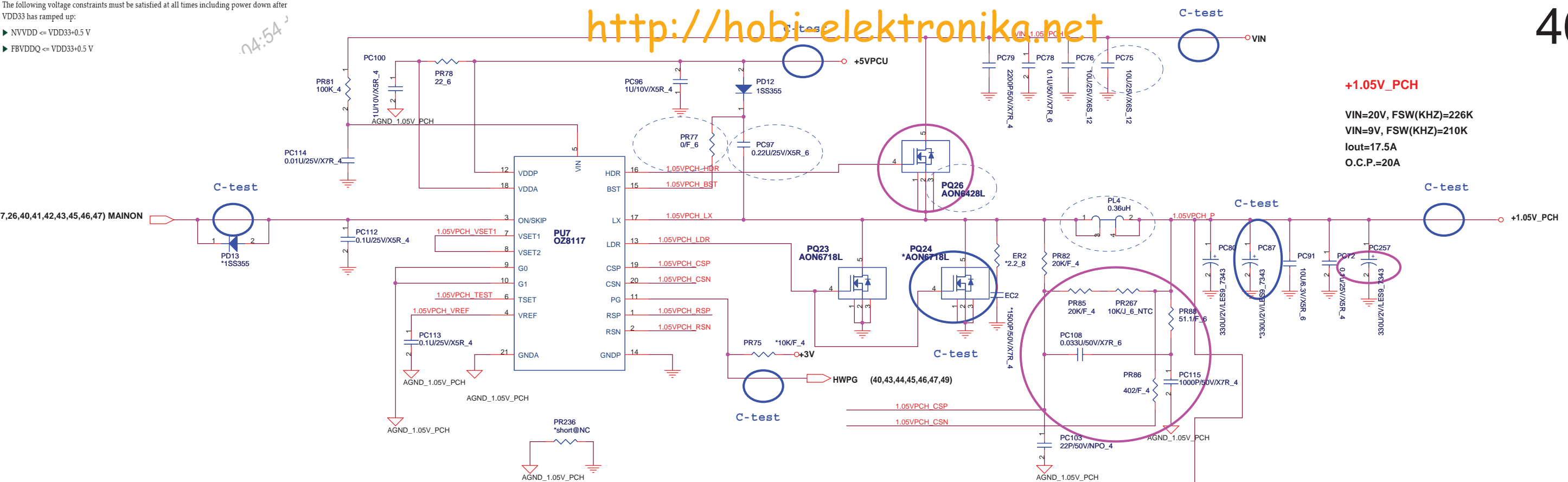
Close To VGPU Discrete Power Rail Side

Change to +VGPU_CORE

The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

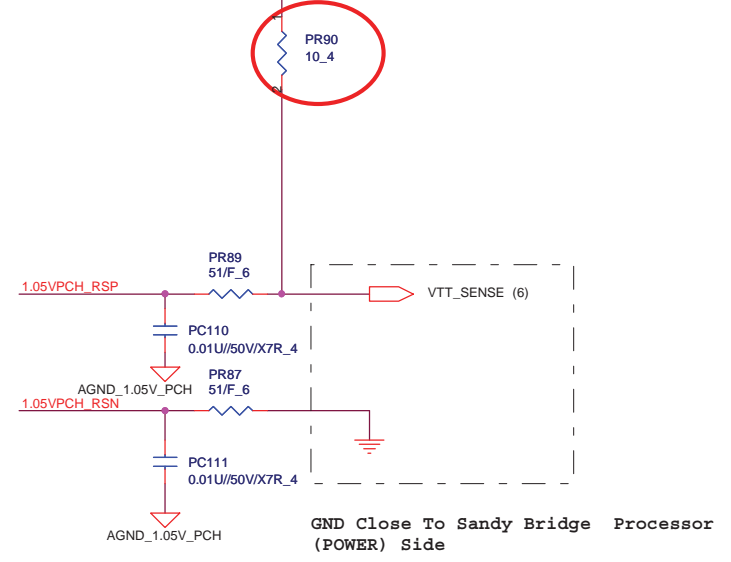
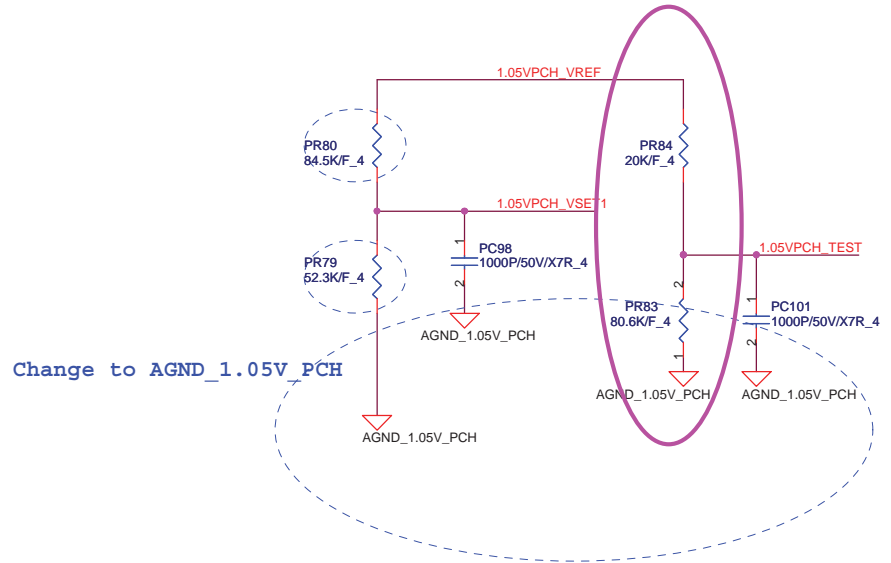
- ▶ NVVDD <= VDD33+0.5 V
- ▶ FBVDDQ <= VDD33+0.5 V

04:54



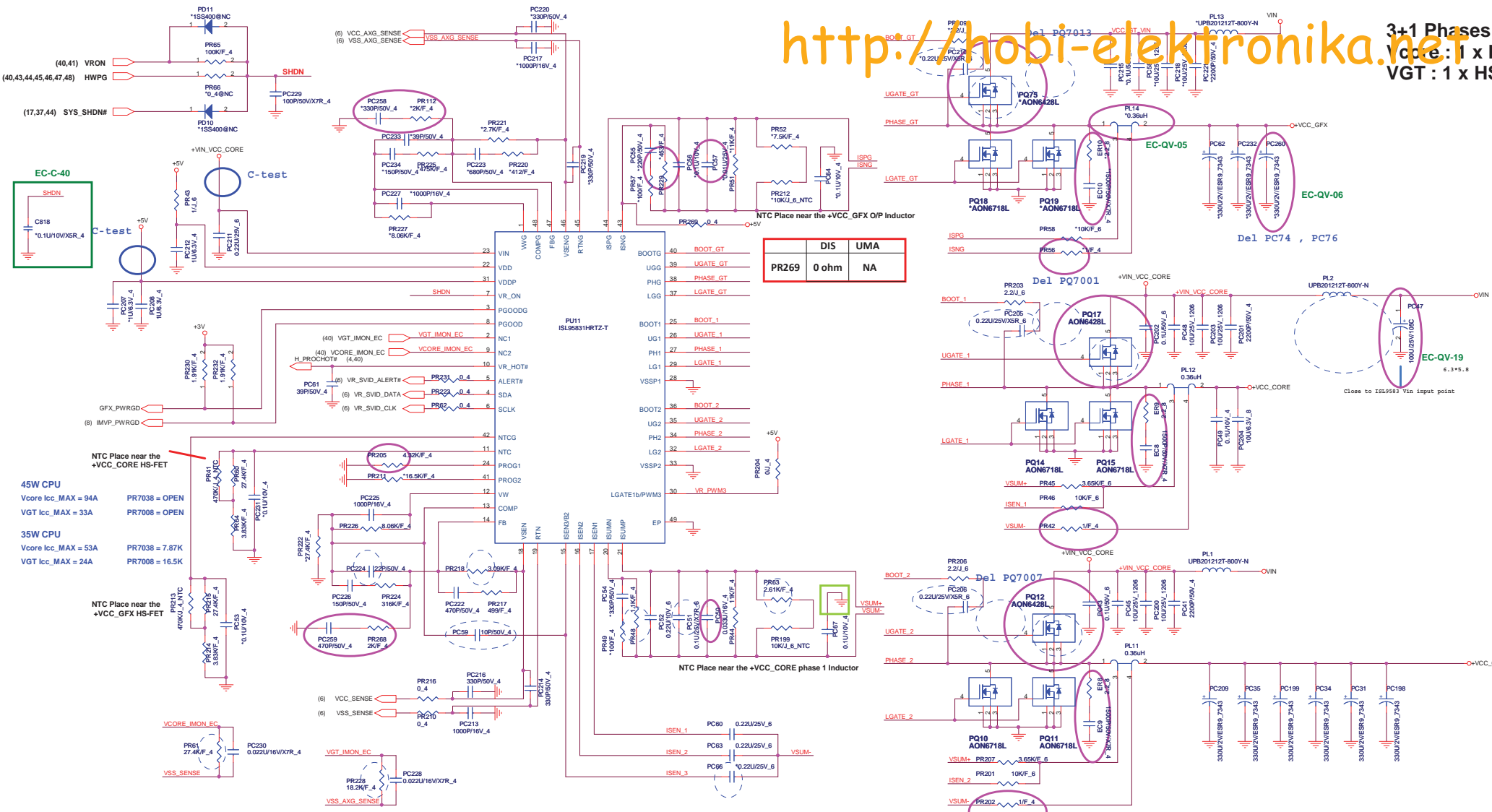
+1.05V_PCH

VIN=20V, FSW(KHZ)=226K
 VIN=9V, FSW(KHZ)=210K
 Iout=17.5A
 O.C.P.=20A



Del +1.5V SW

3+1 Phases design (45W CPU)
 Vcore: 1 x HS-FET, 2 x LS-FET
 VGT: 1 x HS-FET, 2 x LS-FET




	DIS	UMA
PR269	0 ohm	NA

45W CPU
 Vcore Icc_MAX = 94A
 VGT Icc_MAX = 33A

35W CPU
 Vcore Icc_MAX = 53A
 VGT Icc_MAX = 24A

VCCORE_IMON_EC
 VSS_SENSE
 VGT_IMON_EC
 VSS_AWG_SENSE

EC #	Page	Description	Part Affected
EC-B-00	4	Change U18 output type from coms to open-drain.	U18
EC-B-01	10	Remove TPM funtion. (LPC interface)	U14
EC-B-02	10,38	Remove keyboard light funtion.	U14,CN3
EC-B-03	11	Switch pins between BOARD_ID0 and BOARD_ID1.	U14
EC-B-04	11,31	Change net name from WIMAX_OFF# TO WLAN_OFF#, also add pull high 10K with GPIO16	U14,R530
EC-B-05	11	Add board id table.	
EC-B-06	25	Change ESD protection components.	U47,U48
EC-B-07	26	Modify the DIS backlight pin connecting to LVDS connector.	CN1
EC-B-08	28	Add R37 and R47 for normal-open audio jack.	R37,R47
EC-B-09	29	Add SD_4~SD_7 to support SD 3.0	CN12
EC-B-10	30	Remove 2nd battery switch.It is only for KL8/8A.	
EC-B-11	31	Correct the LPC connection for debug card.	CN26
EC-C-12	32	change capacitors connection from +3V to +3.3V_SSD,+1.5V to +1.5V_WIMAX	
EC-B-13	32	Remove unused nets in SSD connector.	CN24
EC-B-14	33	Switch the PCIE_TXN5 , PCIE_TXP5 for the right connection.	U21
EC-B-15	35	Change control signal of U25 enable pin from USB_ON to USB_CHARGE_ON for usb charge function.	U25
EC-B-16	28	Modify left & right sound reverse issue	
EC-B-17	35	Correct USB charge IC footprint.	U27
EC-B-18	36,42	Remove G-sensor circuits.	U17
EC-B-19	37	Correct the pin connection of CN8.	CN8
EC-B-20	38	Correct LED footprint.	LED1,LED2
EC-B-21	38	Add R51,R82 for user button defined as a power button function.	R51,R82,R378
EC-B-22	40	Add R692,R693 and disable EMI solution "CML3".	R692,R693,CML3
EC-B-23	40	Remove TPM circuits.	
EC-B-24	42	Correct connection and net name of NOVO_BTN#	
EC-B-25	42	Add KB_MATRIX signal for different keyboard matrix selection between KL7 and KL9.	R376,R377
EC-B-26	46,48	Add a +1.5V_GPU and +1.8V_GPU circuits for GPU power sequence tuning.	PQ9064,PC9202,PC9203,P9204,PC9205,PC9206,PR9246
EC-B-27	10,24,27 33,34,14 37,38	Add EMI solution	EC11,EC12,R658,R659,R660,R661,EC13,C711,CML1,R11,R12,CML2,R35,R36,CML4,R649,R651,C677,C678 CA1,CA2,CA3,CA4,CA5,CA6,EC14~EC26,C466
EC-B-28	40	Add ESD solution	SC1~SC30
EC-B-29	39	Follow PDC standard parts pin definition	CN16

 **PROJECT : KL2D**
Quanta Computer Inc.

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EC #	Page	Description	Part Affected
EC-C-00	36	Change power LED pull high power plane to +3VPCU to fix system enter S3 can't flicker issue	LED1
EC-C-01	38	Add EMI solution	SC31,SC32,SC33,SC34,SC35,SC36,SC37,SC38
EC-C-02	39	Modify Hole footprint	Hole1,Hole2,Hole6,Hole14,Hole16,Hole17,Hole20,Hole19,Hole9,Hole8
EC-C-03	12	Reserve CAP for +VCCAFDI_VRM	C825
EC-C-04	38	Delete ESD solution SC9 due to +1.5V power plane was deleted & change SC17 power plane bridge, add some component	SC9,SC17,SC25,SC39,SC40,SC41,SC42,SC43,SC44,SC45,SC14,SC18,SC19,SC28,SC29,SC30,SC10,SC11 SC12,SC13,SC15,SC22,SC46
EC-C-05	36	Modify LED footprint to fix SMT issue	LED3
EC-C-06	25	Modify bead footprint to fix SMT issue	L37
EC-C-07	21	Modify VRAM footprint to fix SMT issue	U4,U5,U28,U29
EC-C-08	4	Un-stuff AND gate component	U18,C366,R314,R313
EC-C-09	27	Change SD_CLK CAP from 33p to 10p	C425
EC-C-10	22	Change RES value to fix HDMI test fail item	R399,R400,R401,R402,R403,R404,R405,R406
EC-C-11	26	Reserve diode for EAPD pin	D23
EC-C-12	9	Un-stuff JTAG RES	R181,R182,R528,R534,R533,R538,R168
EC-C-13	31	Add USB3.0 schematic	CN23,R369,R371,CML4,R637,R657,R704,R705,Q53,Q54,C706,C826,C827,C828,R636,R155,R707,C829,Q58,C830
EC-C-14	31	Modify TP footprint to 3050	TP20,TP21,TP22,TP23
EC-C-15		Modify 0 ohm RES to short pad	R592,R608,R326,R274,R287,R292,R502,R504,R505,R512,R513,R521,R527,R91,R245,R258,R587,R301 R648,R451,R380,R442,R366,R425,R623,R673,R686,R77,R430,R432,R101,R212,R221,R232,R235,R239 R563,R586,R588,R600,R66,R71,R94,R391,R392,R393,R394,R252,R242,R248,R250,R603,R65,R233 R4,R50,R652,L49,L53,R431,R364,R370,R397,R448,R384,R446,L23,R40,R60,R349
EC-C-16	12	Change 0.002 ohm RES to 0 ohm	R247,R261,R254
EC-C-17	26	Stuff ESD solution	C480,C481,C482,C483
EC-C-18	10	Remove RF_ON pull down RES	R522
EC-C-19	29	Add net WWAN_OFF# to disable WWAN function	
EC-C-20	12	Change 0 ohm RES to bead	R222
EC-C-21	4	For INTEL design guide definition and material shortage, will change to 25.5ohm	R315
EC-C-22	6	Stuff SVID DATA pull high RES	R286

EC #	Page	Description	Part Affected
EC-QV-00	42	Add power circuit for charge issue.	PR9252,PR9253,PR9254,PR9255,PR9256,PC9212,PC9213,PD23,PU13,PQ9070
EC-QV-01	37	Add 0 Ohm for thermal sensor of DDR & WWAN	R133,R155
EC-QV-02	33	Modify the USB charge circuit(Add option and reverse circuit, change the USB switch EN to USB_ON_R)	R522,R636,R708,R709,R710,Q60
EC-QV-03	11	Change the SV_DET pull high to +3V_S5 from +3V	
EC-QV-04	25	Change footprint of L37 for SMT request	L37
EC-QV-05	43	Change footprint of PL4, PL6, PL7, PL15, PL16	PL4, PL6, PL7, PL15, PL16
EC-QV-06	49	Add capacitor in +VCC_GFX	PC260
EC-QV-07	4	Add un-stuff capacitor on H_PWRGOOD_R	C900
EC-QV-08	4	Change to component stuff	R325,Q29
EC-QV-09	8	Add un-stuff capacitor on SYS_PWROK	C901
EC-QV-10	8	Change R493 to un-stuff	R493
EC-QV-11	9	Change footprint to shortpad	R409,R153
EC-QV-12	9	Add 1M ohm on ACZ_SYNC_CODEC	R711
EC-QV-13	9	Change C119,C118 to 18p from 6p for RTC issue	C118,C119
EC-QV-14	30	Change component to un-stuff.	C783,C784,C736
EC-QV-15	26	Change the footprint for EMI solution stuff BEAD	R391,R392,R393,R394
EC-QV-16	39	Change HOLE8 to NTPH	
EC-QV-17	31	Modify USB3.0 circuit for power saving.	Q35,R414,R415, D28,R712,Q62,R716,C950,Q63,R717,C951,C952,R713,R714,Q61,C953,R715,R421
EC-QV-18	22	Change the footprint to 4 GND PIN for HDMI	CN22
EC-QV-19	49	Change PC47 to stuff	PC47
EC-QV-20	38	Change the P/N for cost saving	SC2,SC11,SC12,SC13,SC14,SC15,SC16,SC20,SC21,SC22,SC27,SC28,SC29,SC30,SC39,SC40,SC41,SC42,SC43,SC44,SC45,SC46,SC31,SC32,SC33,SC34,SC35,SC36,SC37,SC38
EC-QV-21	29	Change C497 to stuff	C497