CPU Plate

H1 Do Not Stuff — Do Not Stuff
H2 Do Not Stuff — Do Not Stuff
H3 Do Not Stuff — Do Not Stuff

VGA Std-Off

H4 STF237R128H42-1-GP — 34.4GD01.001
H5 STF237R128H42-1-GP — 34.4GD01.001

Structure boss

H7 Do Not Stuff — Do Not Stuff
H9 Do Not Stuff — Do Not Stuff
H10 Do Not Stuff — Do Not Stuff
H11 Do Not Stuff — Do Not Stuff
H8 Do Not Stuff — Do Not Stuff
H12 Do Not Stuff — Do Not Stuff
H13 Do Not Stuff — Do Not Stuff
H15 Do Not Stuff — Do Not Stuff

Check test point

5,11,18,27,31,36,65,66,71,83 PLT_RST# — AFTP13

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
11,19,27 PM_PWRBTN#	AFTP10
5,11,22,36 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12

Test Point放在Dimm Door打開可量測處

MiniPCI Std-Off

H14 STF256R89H178-GP — 34.4B417.001

1D05V_VTT

R9701 Do Not Stuff DY — VTT_RUNPWR
Q9701 Do Not Stuff DY
16,31,33,40,42 PS_S3CNTRL — PS_S3CNTRL

1D8V_S0

R9702 Do Not Stuff DY — 1D8V_RUNPWR
Q9702 Do Not Stuff DY
PS_S3CNTRL

1D5V_S0

R9703 Do Not Stuff DY — 1D5V_RUNPWR
Q9703 Do Not Stuff DY
PS_S3CNTRL

3D3V_S0

R9704 Do Not Stuff DY — 3D3V_RUNPWR
Q9704 Do Not Stuff DY
PS_S3CNTRL

5V_S0

R9705 Do Not Stuff DY — 5V_RUNPWR
Q9705 Do Not Stuff DY
PS_S3CNTRL

VCC_CORE

R9706 Do Not Stuff DY — CORE_RUNPWR
Q9706 Do Not Stuff DY
PS_S3CNTRL

VCC_GFXCORE

R9707 Do Not Stuff DY — GFX_RUNPWR
Q9707 Do Not Stuff DY
PS_S3CNTRL

0D75V_S0

R9708 Do Not Stuff DY — 0D75V_RUNPWR
Q9708 Do Not Stuff DY
PS_S3CNTRL

0D85V_S0

R9709 Do Not Stuff DY — 1D05V_RUNPWR
Q9709 Do Not Stuff DY
PS_S3CNTRL

For Discharge

3D3V_S5 — R9710 Do Not Stuff DY — Q9710 Do Not Stuff DY
1D5V_S3 — R9711 Do Not Stuff DY — 3D3V_RUNPWR — Q9711 Do Not Stuff DY
PM_SLP_S4
16,31,33,40,42 PM_SLP_S4#

AD+ — EC9702 SCD1U25V2KX-GP — EC9703 SCD1U25V2KX-GP — EC9704 DY Do Not Stuff

DCBATOUT — EC9705 SCD1U25V2KX-GP

55.4KZ01.S18G S19G

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Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: LA470 | Rev: -1
Date: Thursday, November 04, 2010 | Sheet 1 of 103

UMA & Optimus Schematics Document

Sandy Bridge

Intel PCH

2010-10-27

REV : -1

DY :None Installed
UMA:UMA platform installed
OPS:Optimus

55.4KZ01.S18G S19G

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Title		
	Cover Page	
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 1 of 103	

Block Diagram (UMA/Optimus co-lay)

##OnMainBoard

POWER BD

Finger Printer BD

IO BD (Cardreader+Audio+USB)

LED BD

USB

VRAM 2GB/1GB/512MB 88,89,90,91

DDR3 800MHz

NVIDIA N12P-GE/GV N12M-GE 83.84,85,86,87

PCIe x 16 (Discrete only)

Intel CPU

Sandy Bridge

DDRIII: 1066/1333/1666 MHz

4,5,6,7,8,9,10

DDRIII 1066/1333/1666 Channel A

DDRIII 1066/1333/1666 Channel B

DDRIII Slot 0 1066/1333/1666 14

DDRIII Slot 1 1066/1333/1666 15

Project code : 91.4KZ01.001
PCB P/N : 48.4KZ01.011
Revision : 10250-1

HDMI 51

LCD 49

CRT 50

FDI x 4 x 2 (UMA only)

DMI x 4

HDMI

LVDS

RGB CRT

Intel PCH Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25

Bluetooth 63

CAMERA 49

Finger Print BD

Finger Print 64

USB2.0 x 3

I/O BD

SD/MMC+/MS/ MS Pro/xD 74

CardReader Realtek RTS5139

USB 2.0 x 1

AZALIA

PCIE x 1

GLAN RTL8111E 31

RJ45 CONN 59

PCIE x 1/USB2.0 x 1

Mini-Card WLAN 65

SATA x 1/USB2.0 x 1

Mini-Card WWAN 66

SIM 66

USB 2.0 x 3

MB USB x 3

USB 2.0 x 1/SATA x 1

E-SATA/USB comb 57

SATA x 2

HDD 56

ODD 56

SPI

Flash ROM 4MB 60

LPC Bus

LPC debug port 71

Internal DMIC

HP1

MIC IN

I/O BD

Azalia CODEC Codec_ALC272 29

2CH SPEAKER

KBC NUVOTON NPCE795G 27

SMBus

G-Sensor 79

Touch PAD 69

Int. KB 69

Thermal EMC2103-2-AP 28

Fan 28

SYSTEM DC/DC RT8208A 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51218 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208A 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8015B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

55.4KZ01.S18G S19G

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Title: Block Diagram

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA Pair	SATA Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

55.4KZ01.S18G S19G

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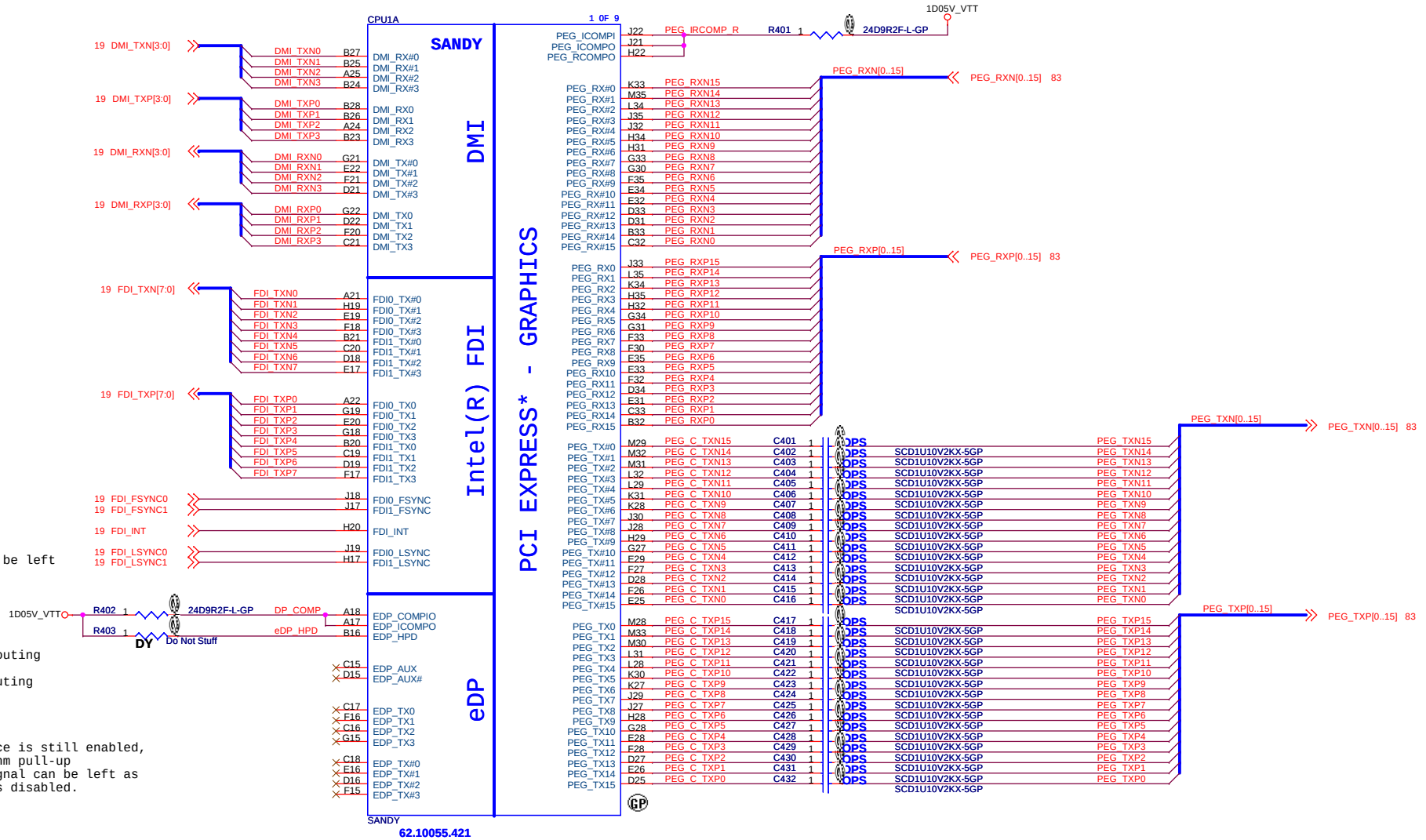
Title: **Table of Content**

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 3 of 103

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-k ohm pull-up resistor on the motherboard. This signal can be left as no connect if entire eDP interface is disabled.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

55.4KZ01.S18G S19G

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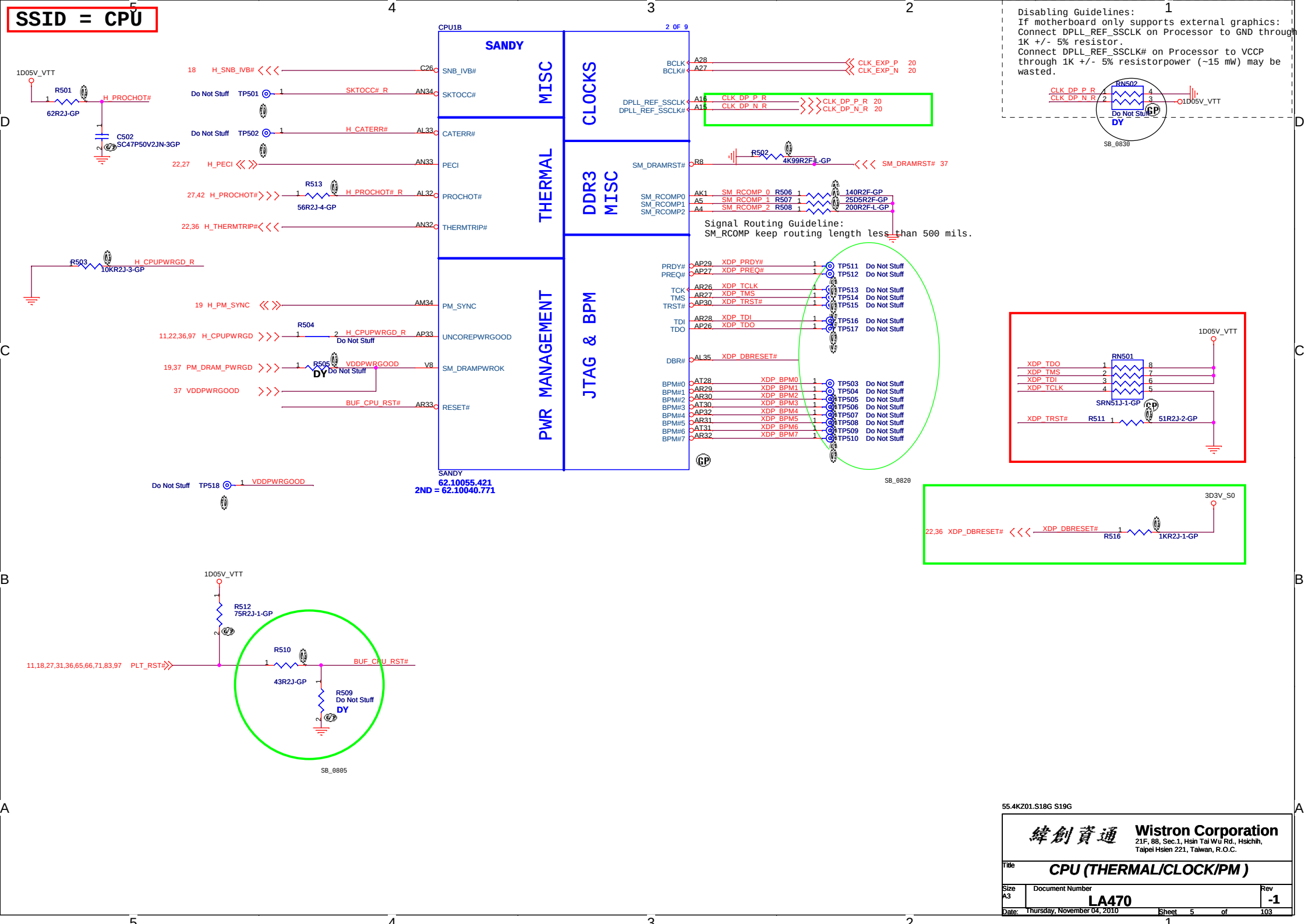
Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 4 of 103

SSID = CPU



55.4KZ01.S18G S19G

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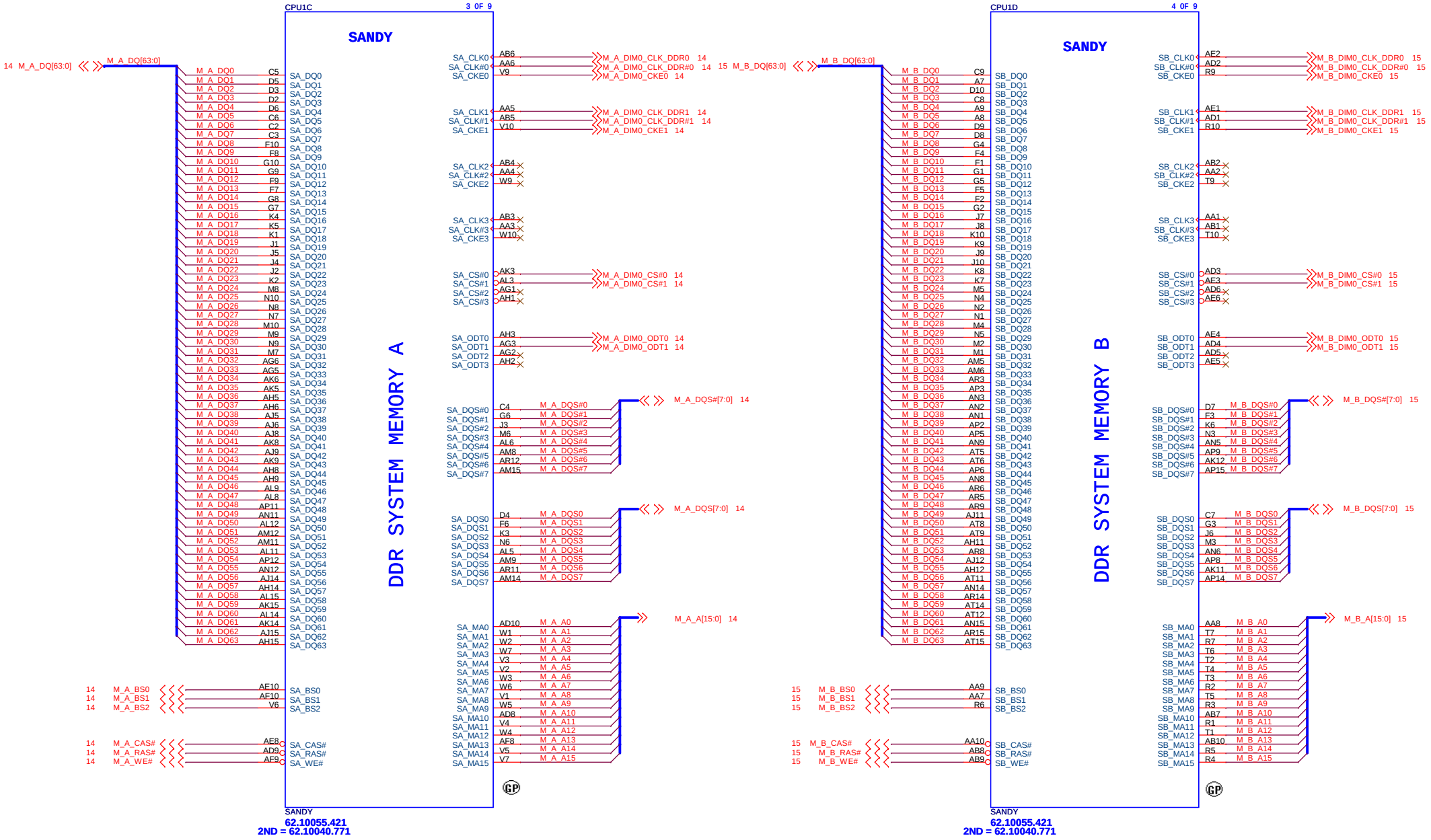
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 5 of 103

SSID = CPU



55.4KZ01.S18G S19G

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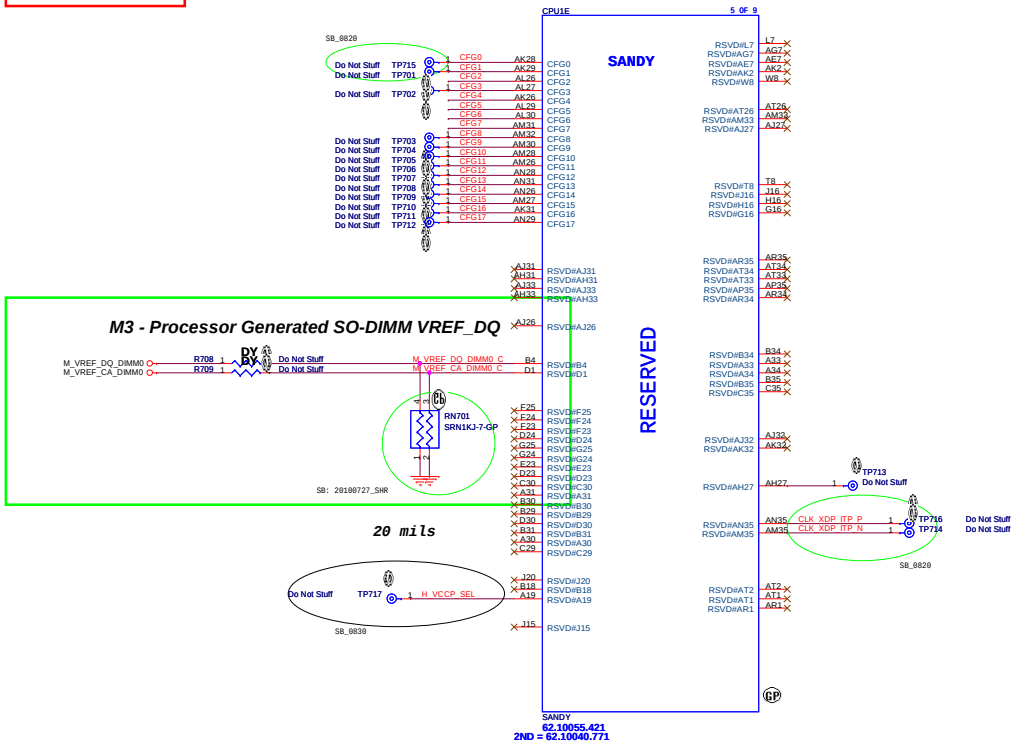
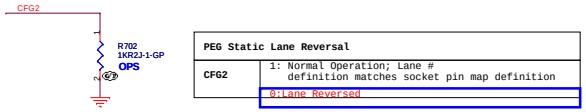
Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	LA470	-1

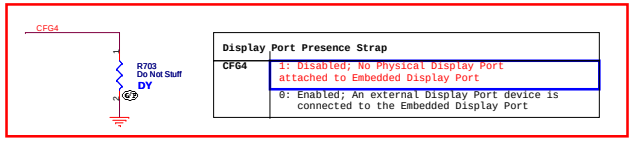
Date: Thursday, November 04, 2010 Sheet 6 of 103

SSID = CPU

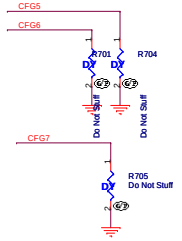




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

Size	Document Number	Rev
A2	LA470	-1

Date: Thursday, November 04, 2010 Sheet 7 of 103

SSID = CPU

POWER

PROCESSOR CORE POWER

53A

CPU1F

6 OF 9

SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCC_CORE

1D05V_VTT

R804 need to close to CPU

R801, R802 need to close to CPU

55.4KZ01.S18G S19G

SANDY

62.10055.421

2ND = 62.10040.771

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Title: CPU (VCC_CORE)

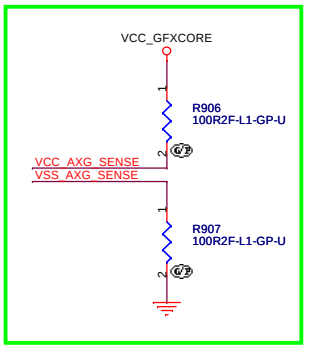
Size: Custom | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 8 of 103

SSID = CPU

POWER

Close to CPU



VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 C902 C903 C904 C905 C906 SC10U6D3V5KX-1GP

RC901 Not Stuff DY

C907 C908 C918 C919 C920 C921 SC10U6D3V5KX-1GP

RC902 Not Stuff DY

SB_0831

CPU1G

SANDY

GRAPHICS

VAXG: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

7 OF 9

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 42

VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

VREF

SM_VREF AL1 → +V_SM_VREF_CNT → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 C910 C911 C912 C913 C914 SC10U6D3V5KX-1GP

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

C916 C915 C917 SC10U6D3V5KX-1GP

TC903 Do Not Stuff DY

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

0D85V_S0

R902 Do Not Stuff DY

R902 need be close to pin H23.

MISC

VCCSA_SENSE H23 → VCCSA_SENSE 48

FC_C22 C22 → H_FC_C22 48

VCCSA_VID1 C24 → VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C925 SC10U6D3V5KX-1GP

C923 SC10U6D3V5KX-1GP

C922 C924 SC1U10V2KX-1GP

VCCPLL: B6 A6 A2

SANDY

62.10055.421

2ND = 62.10040.771

55.4KZ01.S18G S19G

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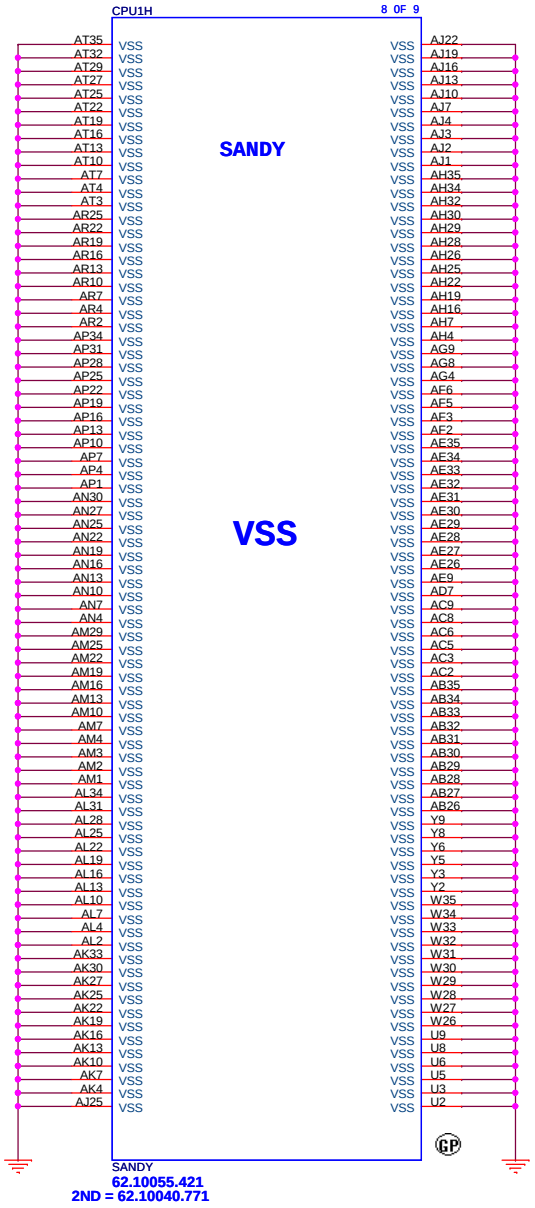
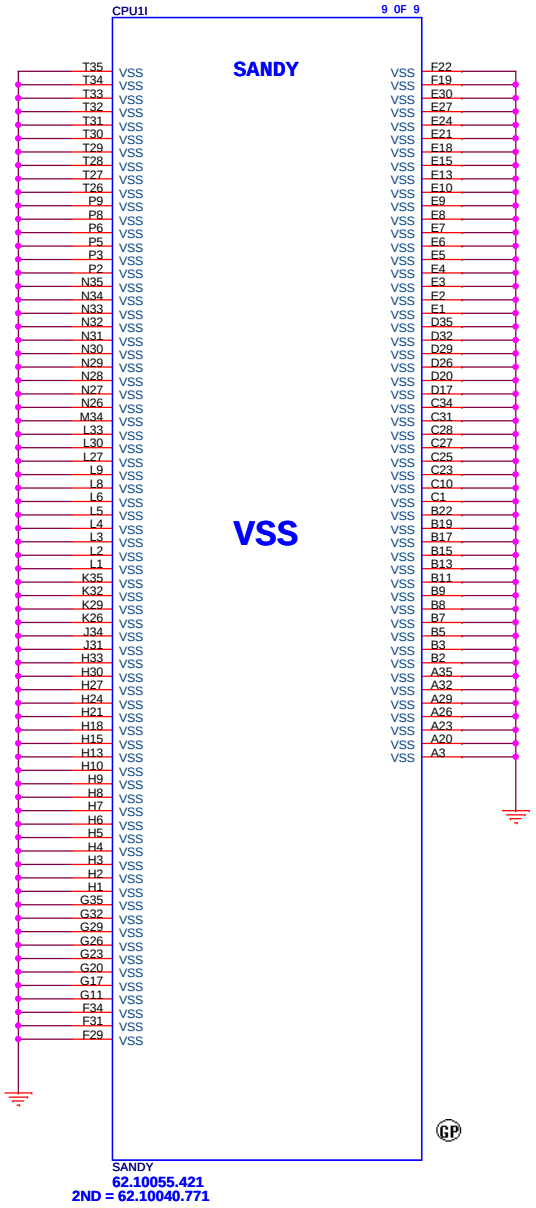
Title: CPU (VCC_GFXCORE)

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 9 of 103

SSID = CPU





55.4KZ01.S18G S19G

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***CPU (VSS)***	
Size A3	Document Number **LA470**	Rev **-1**
Date: Thursday, November 04, 2010	Sheet 10 of 103	

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***

Size	Document Number	Rev
A3	**LA470**	**-1**

Date: Thursday, November 04, 2010 Sheet 11 of 103

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 12 of 103

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **LA470**	Rev: **-1**
Date: Thursday, November 04, 2010	Sheet 13 of 103	

SSID = MEMORY

DM1

DDR_VREF_S3

R1405 Do Not Stuff

M_VREF_CA_DIMM0

C1423 SCD1U10V2KX-5GP

C1425 DY Do Not Stuff

C1424 SCD1U10V2KX-5GP

DDR_VREF_S3

R1404 Do Not Stuff

M_VREF_DQ_DIMM0

C1411 SCD1U10V2KX-5GP

C1412 DY Do Not Stuff

C1413 SCD1U10V2KX-5GP

0D75V_S0

Place these caps close to VTT1 and VTT2.

C1419 SC1U6D3V2KX-GP

C1420 DY Do Not Stuff

C1421 SC1U6D3V2KX-GP

C1422 DY Do Not Stuff

C1418 DY Do Not Stuff

M_A_A[15:0] 6

M_A_BS2 6

M_A_BS0 6

M_A_BS1 6

M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6

M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6

M_A_DIM0_ODT1 6

M_VREF_CA_DIMM0

M_VREF_DQ_DIMM0

15,37 DDR3_DRAMRST#

0D75V_S0

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
	79	A16/BA2	
	109	BA0	
	108	BA1	
M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	
M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
M_A_DQS#7	186	DQS7#	
M_A_DQS0	12	DQS0	
M_A_DQS1	29	DQS1	
M_A_DQS2	47	DQS2	
M_A_DQS3	64	DQS3	
M_A_DQS4	137	DQS4	
M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	
	116	ODT0	
	120	ODT1	
M_VREF_CA_DIMM0	126	VREF_CA	
M_VREF_DQ_DIMM0	1	VREF_DQ	
	30	RESET#	
0D75V_S0	203	VTT1	
	204	VTT2	

NP1	NP1	
NP2	NP2	
RAS#	110	M_A_RAS# 6
WE#	113	M_A_WE# 6
CAS#	115	M_A_CAS# 6
CS0#	114	M_A_DIM0_CS#0 6
CS1#	121	M_A_DIM0_CS#1 6
CKE0	73	M_A_DIM0_CKE0 6
CKE1	74	M_A_DIM0_CKE1 6
CK0	101	M_A_DIM0_CLK_DDR0 6
CK0#	103	M_A_DIM0_CLK_DDR#0 6
CK1	102	M_A_DIM0_CLK_DDR1 6
CK1#	104	M_A_DIM0_CLK_DDR#1 6
DM0	11	
DM1	28	
DM2	46	
DM3	63	
DM4	136	
DM5	153	
DM6	170	
DM7	187	
SDA	200	PCH_SMBDATA 15,20,65,66
SCL	202	PCH_SMBCLK 15,20,65,66
EVENT#	198	TS#_DIMM0_1 15
VDDSPD	199	
SA0	197	SA0_DIM0
SA1	201	SA1_DIM0
NC#1	77	
NC#2	122	
NC#/TEST	125	
VDD1	75	
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	118	
VDD17	123	
VDD18	124	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	13	
VSS	14	
VSS	19	
VSS	20	
VSS	25	
VSS	26	
VSS	31	
VSS	32	
VSS	37	
VSS	38	
VSS	43	
VSS	44	
VSS	48	
VSS	49	
VSS	54	
VSS	55	
VSS	60	
VSS	61	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	127	
VSS	128	
VSS	133	
VSS	134	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	150	
VSS	151	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	167	
VSS	168	
VSS	172	
VSS	173	
VSS	178	
VSS	179	
VSS	184	
VSS	185	
VSS	189	
VSS	190	
VSS	195	
VSS	196	
VSS	205	
VSS	206	

DDR3-204P-109-GP

62.10017.XS1

2nd = 62.10017.R91

3rd = 62.10017.V61

SB_0819

3D3V_S0

C1401 SCD1U10V2KX-5GP

C1402 DY Do Not Stuff

1D5V_S3

SODIMM A DECOUPLING

TC1401 ST330U2VDM4-GP

C1403 SC10U6D3V5KX-1GP

C1404 SC10U6D3V5KX-1GP

C1405 DY Do Not Stuff

C1406 SC10U6D3V5KX-1GP

C1407 SC10U6D3V5KX-1GP

C1408 DY Do Not Stuff

C1409 DY Do Not Stuff

C1410 DY Do Not Stuff

C1414 SCD1U10V2KX-5GP

C1415 SCD1U10V2KX-5GP

C1416 SCD1U10V2KX-5GP

C1417 SCD1U10V2KX-5GP

SA0_DIM0

SA1_DIM0

R1401 10KR2J-3-GP

R1402 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

3D3V_S0

TS#_DIMM0_1

R1403 10KR2J-3-GP

55.4KZ01.S18G S19G

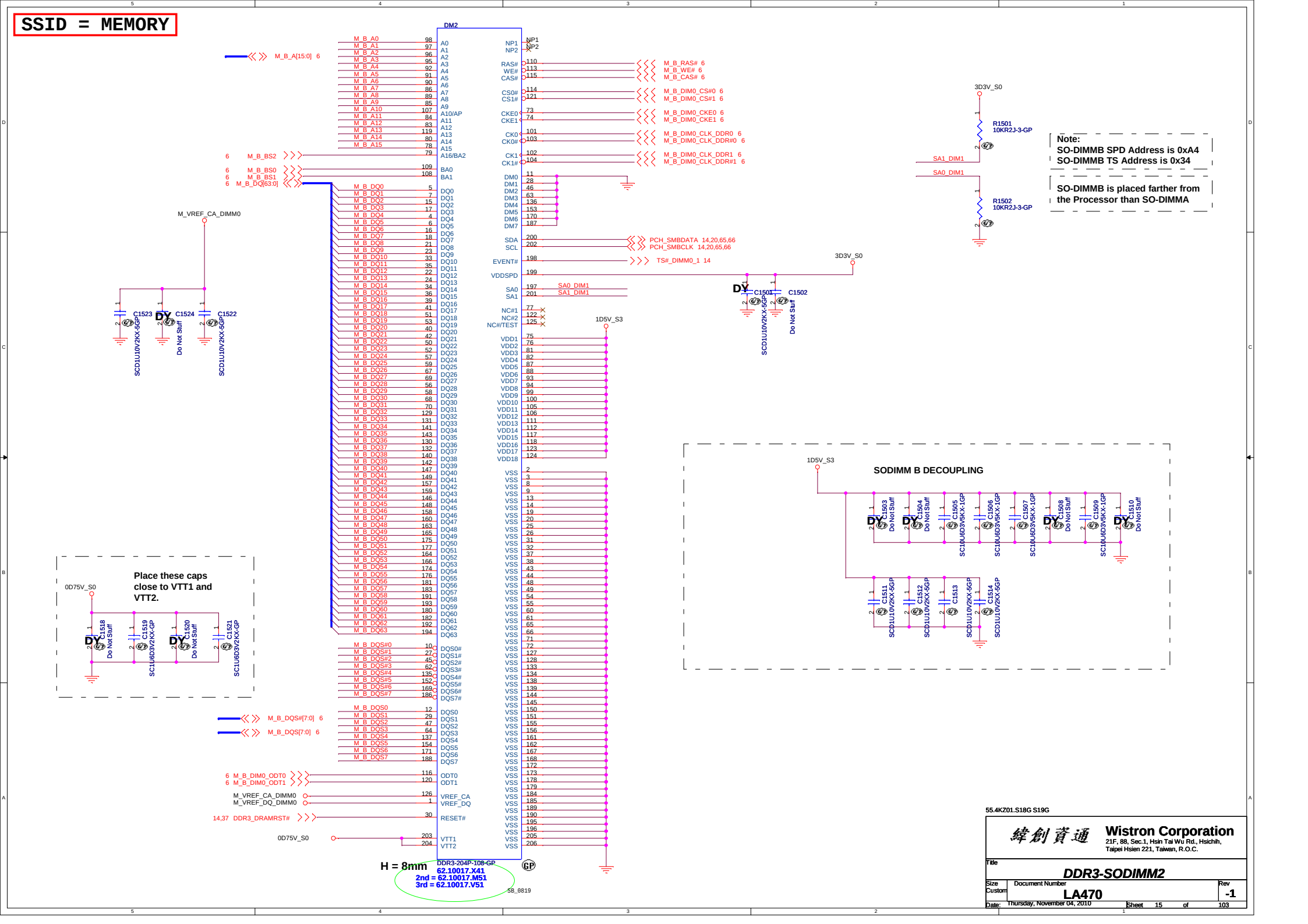
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
Custom	LA470	-1

Date: Thursday, November 04, 2010 Sheet 14 of 103

SSID = MEMORY



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	LA470	-1

Date: Thursday, November 04, 2010 Sheet 15 of 103

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
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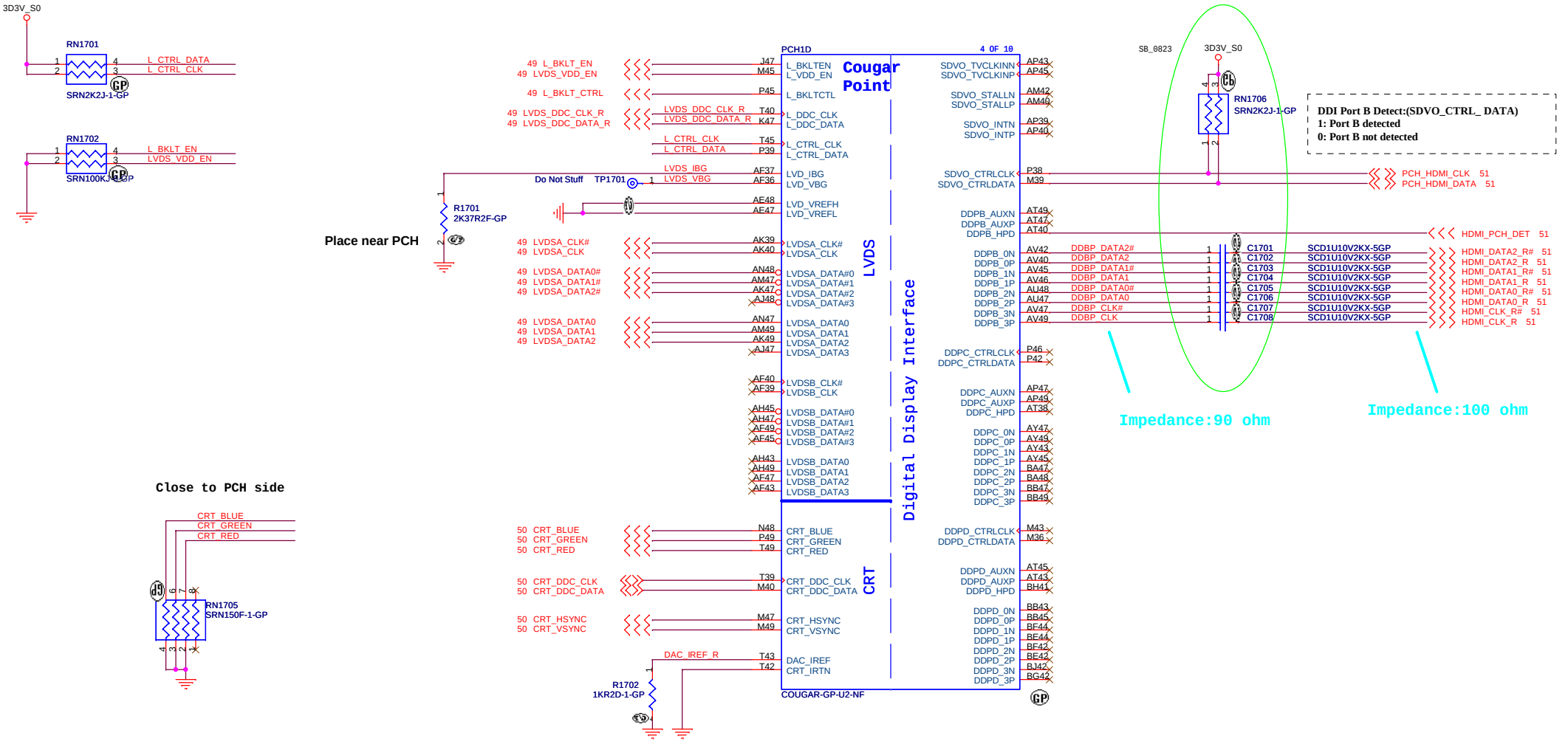
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 16 of 103



55.4KZ01.S18G S19G

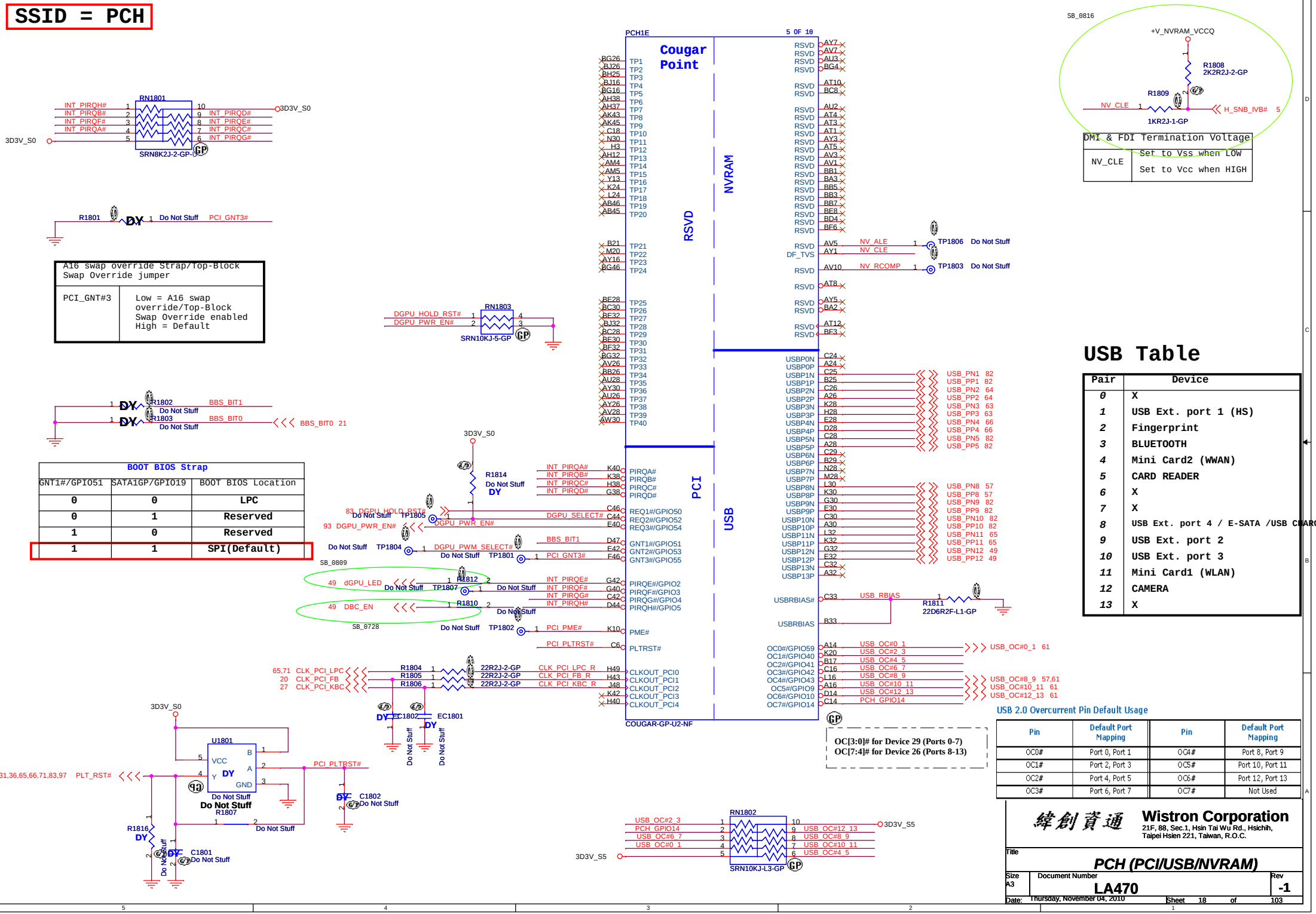
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 17 of 103

SSID = PCH



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

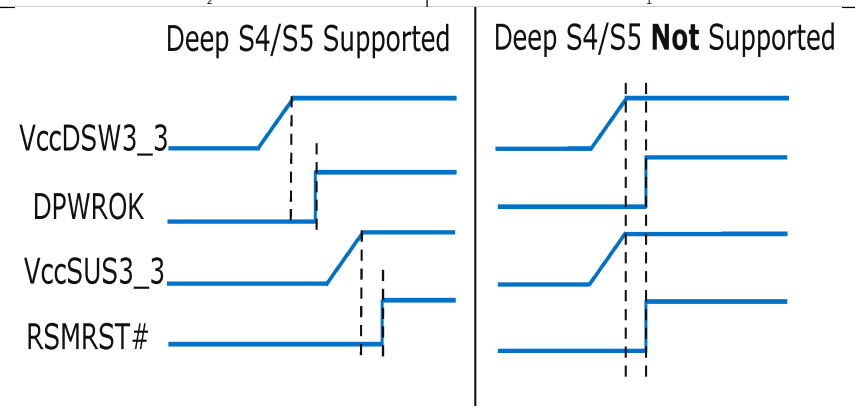
Title: PCH (PCI/USB/NVRAM)

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

This signal has an internal pull-up resistor

1st = 84.DM601.03F
2nd = 84.2N702.A3F

55.4KZ01.S18G S19G

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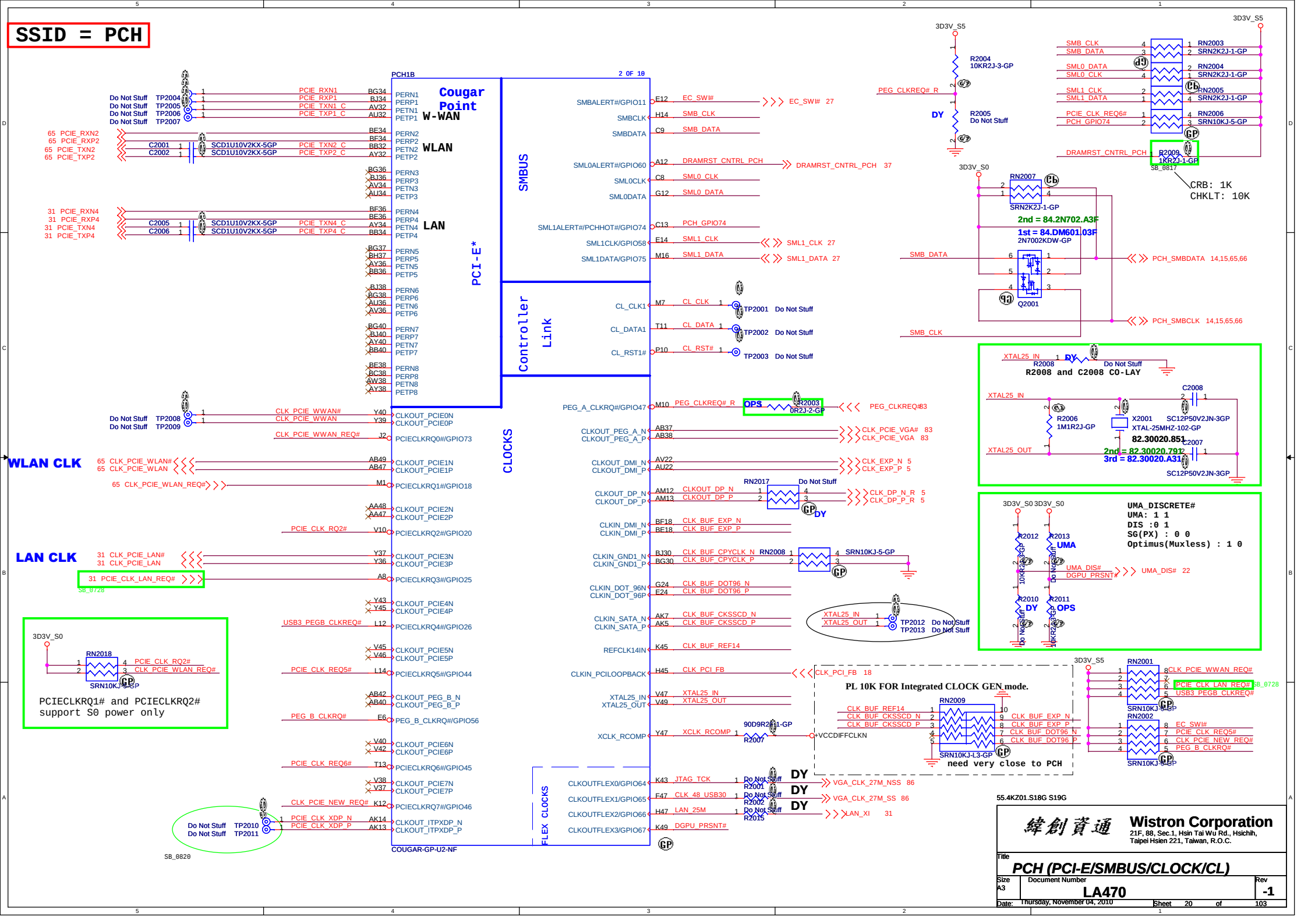
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: LA470 | Rev: -1
Date: Thursday, November 04, 2010 | Sheet 19 of 103

SSID = PCH


PCH1B
2 OF 10
Cougar Point
W-WAN
WLAN
LAN
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR-GP-U2-NF
WLAN CLK
LAN CLK
PCIECLKRQ1# and PCIECLKRQ2# support S0 power only
PL 10K FOR Integrated CLOCK GEN mode.
need very close to PCH
R2008 and C2008 CO-LAY
UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0
CRB: 1K
CHKLT: 10K
2nd = 84.2N702.A3F
1st = 84.DM601.03F
82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31
55.4KZ01.S18G S19G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (PCI-E/SMBUS/CLOCK/CL)
LA470
-1
Thursday, November 04, 2010
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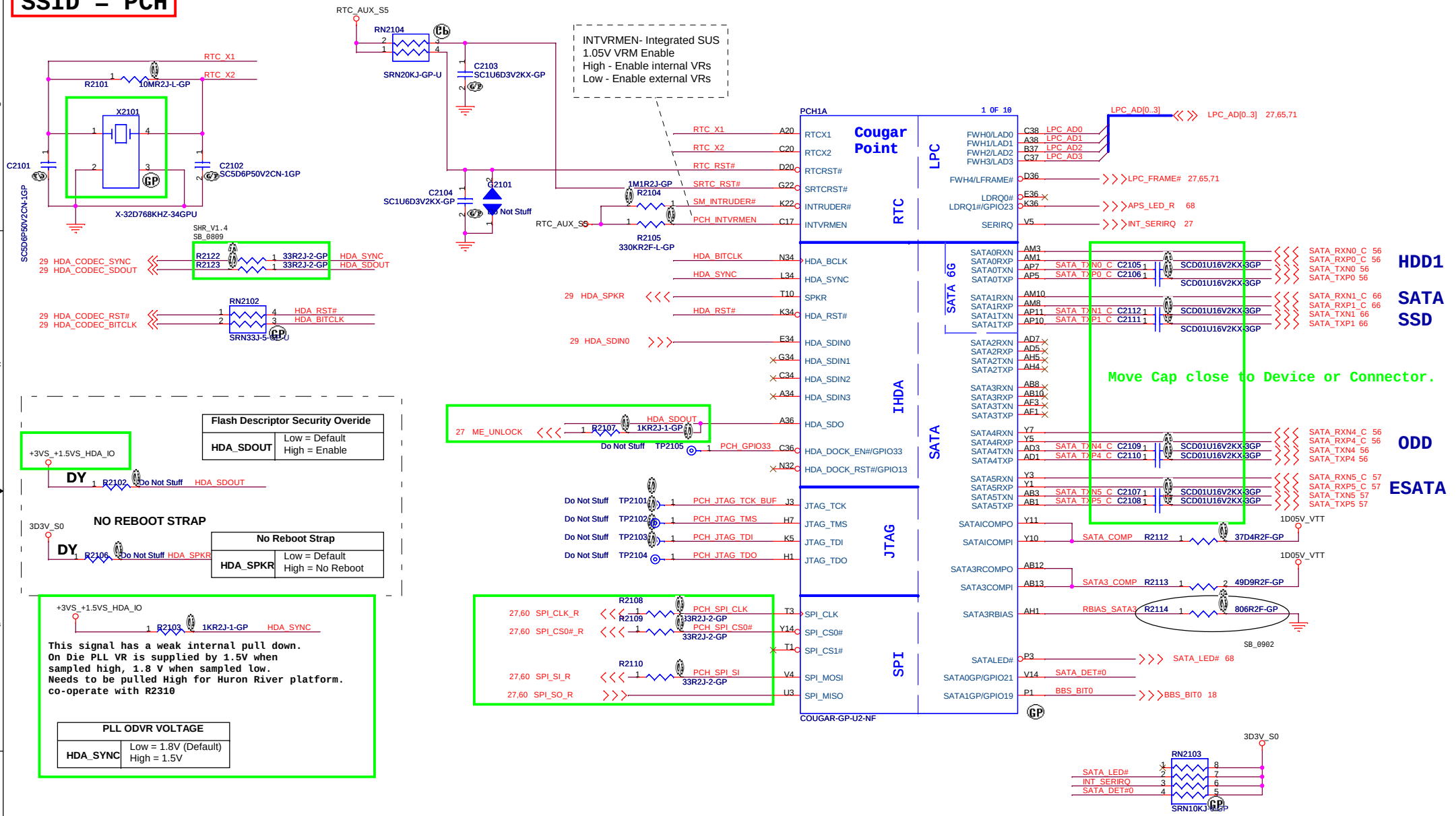
SSID = PCH



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (SPI/RTC/LPC/SATA/IHDA)		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 21 of 103	

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2202 1 — 200KR2F-L-GP — SATA_ODD_PRSNT#

20100625 V1.2

3D3V_S0 — RN2203 — H_A20GATE, H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S0 — R2224 10KR2J-3-GP — PCH_TEMP_ALERT#
PCH_GPIO27 — DY R2223 Do Not Stuff
DY R2225 Do Not Stuff

3D3V_S0 — RN2201 — PSW_CLR#, DGPU_HPD_INTR#, EC_SCI# — SRN10KJ-8-GP

RN2202 — MFG_MODE, S_GPIO, EC_SCI#, PCH_GPIO22 — SRN10KJ-8-GP
PCH_GPIO48 — R2227 10KR2J-3-GP

3D3V_S5 — RN2205 — PCH_GPIO12, USB3_PWR_ON — SRN10KJ-8-GP
PCH_GPIO15 — R2201 1KR2J-1-GP
PCH_GPIO24 — R2221 10KR2J-3-GP
20100625 V1.2
PLL_ODVR_EN — R2226 10KR2J-3-GP

NC_FP_DET# — R2220 10KR2J-3-GP
20100705

PCH1F — 6 OF 10 — Cougar Point

S_GPIO — R2218 100R2J-2-GP	GPIO0	T7	BMBUSY#/GPIO0
	EC_SMI#	A42	TACH1/GPIO1
	DGPU_HPD_INTR#	H36	TACH2/GPIO6
27 EC_SCI#	EC_SCI#	E38	TACH3/GPIO7
	ICC_EN#	C10	GPIO8
	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL/GPIO12
	PCH_GPIO15	G2	GPIO15
56 SATA_ODD_PRSNT# — R2213 Do Not Stuff	PCH_GPIO16	U2	SATA4GP/GPIO16
92,93 DGPU_PWROK	DGPU_PWROK	D40	TACH0/GPIO17
49 Color_Engine# — R2228 Do Not Stuff — TP2202	PCH_GPIO22	T5	SCLOCK/GPIO22
	PCH_GPIO24	E8	GPIO24/MEM_LED
	PCH_GPIO27	E16	GPIO27
	PLL_ODVR_EN	P8	GPIO28
	PSW_CLR#	K1	STP_PCI#/GPIO34
Do Not Stuff TP2204 — G2201	NC_FP_DET#	K4	GPIO35
	DMI_OVRVLTG	V8	SATA2GP/GPIO36
	FDI_OVRVLTG	M5	SATA3GP/GPIO37
	MFG_MODE	N2	SLOAD/GPIO38
	GFX_CRB_DET	M3	SDATAOUT0/GPIO39
TP2209	PCH_GPIO48	V13	SDATAOUT1/GPIO48
	PCH_TEMP_ALERT#	V3	SATA5GP/GPIO49
Do Not Stuff	USB3_PWR_ON	D6	GPIO57

GPIO

	TACH4/GPIO68	C40	SATA_ODD_PWRGT 56
	TACH5/GPIO69	B41	UMA_DIS# 20
	TACH6/GPIO70	C41	VRAM_SIZE1
	TACH7/GPIO71	A40	VRAM_SIZE2
	A20GATE	P4	H_A20GATE 27
	PECI	AU16	H_PECI_R — DY R2203 Do Not Stuff — H_PECI 5,27
	RCIN#	P5	H_RCIN# 27
	PROCPWRGD	AY11	H_CPUPWRGD 5,11,36,97
	THRMTRIP#	AY10	PCH_THERMTRIP_R R2204 390R2J-1-GP — H_THERMTRIP# 5,36
	INIT3_3V#	T14	INIT3_3V# — TP2201 Do Not Stuff

CPU/MISC

	TS_VSS1	AH8	
	TS_VSS2	AK11	
	TS_VSS3	AH10	
	TS_VSS4	AK10	TS_VSS1 R2219 Do Not Stuff
	NC_1	P37	

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

NCTF

	NCTF_VSS#A4	A4	
Do Not Stuff TP2205	NCTF_VSS#A44	A44	
	NCTF_VSS#A45	A45	
TP2206 Do Not Stuff	NCTF_VSS#A46	A46	
	NCTF_VSS#A5	A5	
	NCTF_VSS#A6	A6	
	NCTF_VSS#B3	B3	
	NCTF_VSS#B47	B47	
	NCTF_VSS#BD1	BD1	
	NCTF_VSS#BD49	BD49	
	NCTF_VSS#BE1	BE1	
	NCTF_VSS#BE49	BE49	
	NCTF_VSS#BF1	BF1	
	NCTF_VSS#BF49	BF49	
	NCTF_VSS#BG2	BG2	
	NCTF_VSS#BG48	BG48	
	NCTF_VSS#BH3	BH3	
	NCTF_VSS#BH47	BH47	
	NCTF_VSS#BJ4	BJ4	
	NCTF_VSS#BJ44	BJ44	
	NCTF_VSS#BJ45	BJ45	
	NCTF_VSS#BJ46	BJ46	
	NCTF_VSS#BJ5	BJ5	
	NCTF_VSS#BJ6	BJ6	
	NCTF_VSS#C2	C2	
	NCTF_VSS#C48	C48	
	NCTF_VSS#D1	D1	
	NCTF_VSS#D49	D49	
	NCTF_VSS#E1	E1	
	NCTF_VSS#E49	E49	
	NCTF_VSS#F1	F1	
	NCTF_VSS#F49	F49	

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

COUGAR-GP-U2-NF

SB_0811
SHR_V1.5

Do Not Stuff TP2210
Do Not Stuff TP2211
Do Not Stuff TP2212

3D3V_S0 — R2207 Do Not Stuff — DY — FDI_OVRVLTG
TP2207 Do Not Stuff
R2208 10KR2J-3-GP
TP2208 Do Not Stuff

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2209 Do Not Stuff — DY — DMI_OVRVLTG
R2210 10KR2J-3-GP

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — DY R2205 Do Not Stuff — GFX_CRB_DET
R2206 100KR2J-1-GP

PCH_THERMTRIP_R — R2222 — 1D05V_VTT
DY Do Not Stuff

3D3V_S0 — R2214 2G Do Not Stuff — R2216 1G 10KR2J-3-GP
VRAM_SIZE1
VRAM_SIZE2
R2215 1G_512M_UMA — R2217 2G_512M_UMA

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — DY R2212 Do Not Stuff

55.4KZ01.S18G S19G

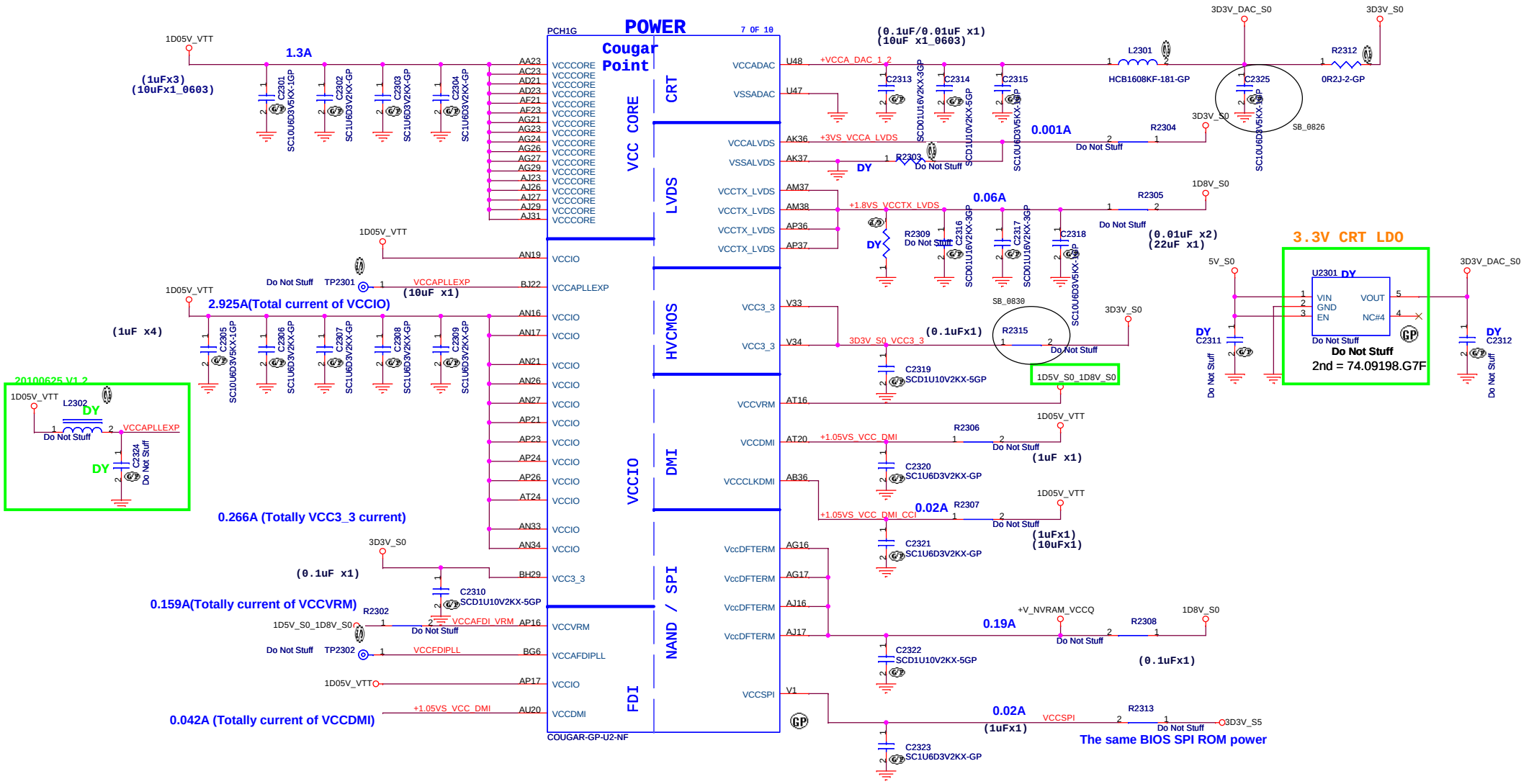
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 — Sheet 22 of 103

SSID = PCH 6A



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (POWER1)		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 23 of 103	

SSID = PCH

POWER

PCH1J

10 OF 10

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

1.01A (Total current of VCCASW)

0.08A

0.16A (Totally current of VCCVRM)

0.055A

0.095A

0.001A

6uA

0.01A

+3VS_+1.5VS_HDA_IO

55.4KZ01.S18G S19G

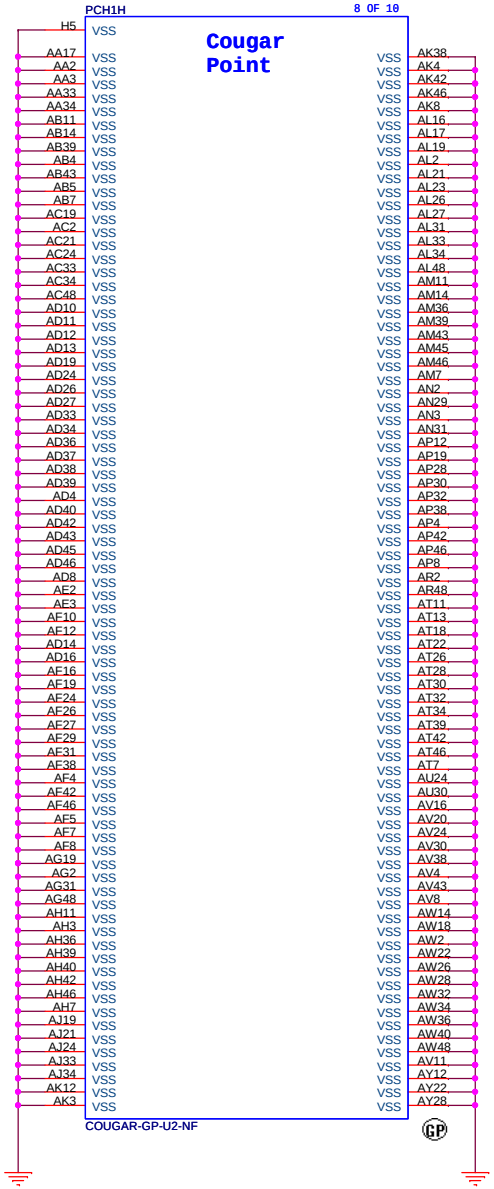
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

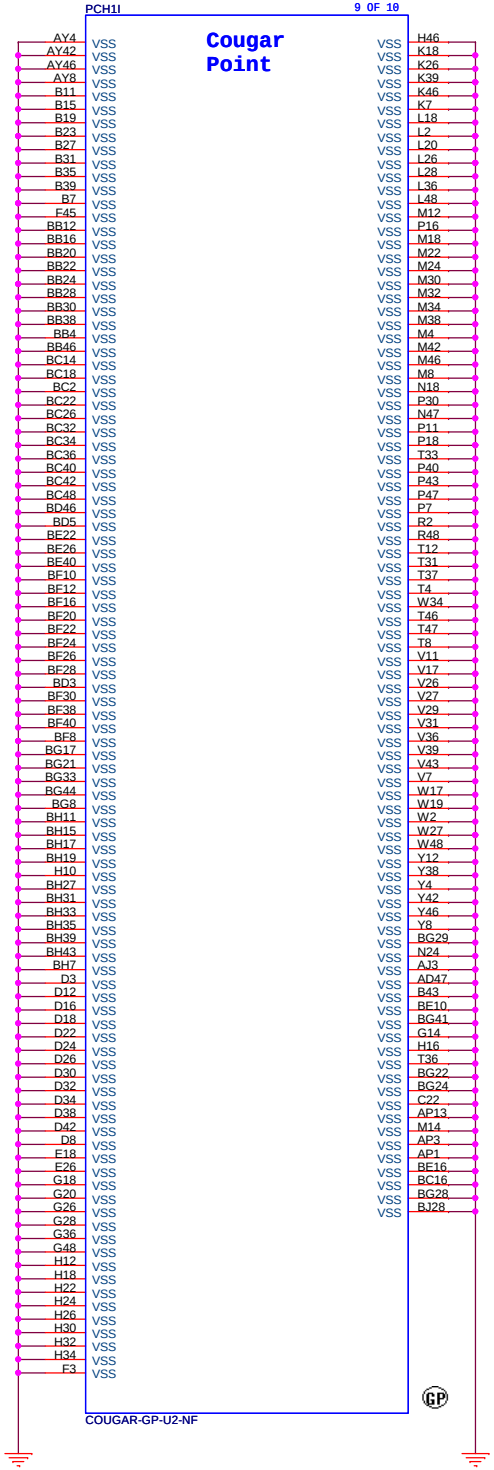
Title: PCH (POWER2)

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 24 of 103

SSID = PCH





55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 25 of 103

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 26 of 103

SSID = KBC

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

65W_90W#
High: 65W / Low 90W

G Sensor ID:
High: ST
Low:ADI

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L..

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

R2701 and C2716
Need very close to EC

EC GPIO standard PH/PL

EC_GPIO47 High Active

Prevent BIOS data loss solution

Do Not Stuff

LILI Multi GPIO setting

MODEL_ID_A0 (Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/B 47 UMA	100.0 K	33.0 K (63.33334 1.0L)	2.481 V
V/B 47 OPTIMUS	100.0 K	47.0 K (63.47334 1.0L)	2.245 V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795
Size: A1 | Document Number: LA470 | Rev: -1
Date: Thursday, November 08, 2012 | Sheet 22 of 103

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA_0905 change to 390p

3

C183 SC390P50V2KX-GP

Q6 MMBT3904WT1G-GP

2200p close to smsc2103 chip

2

C434 Do Not Stuff DY

Q42 MMBT3904WT1G-GP

REMOTE2-

C569 SC2200P50V2KX-2GP

REMOTE2+

between CPU, VGA and DIMM on bottom side

T8

1

Q9 MMBT3904WT1G-GP

2200p close to smsc2103 chip

H_THERMDA

C389 SC2200P50V2KX-2GP

H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit

Close to connector

5V_S0

SA_0905

D2801 Do Not Stuff

Do Not Stuff

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

DY

C39 SC4D7U6D3V3KX-GP

R2801 Do Not Stuff

R426 10KR2J-3-GP

SB_0819

FAN_TACH

FAN_PWM

R427 Do Not Stuff

5V_S0_FAN

FAN_PWM_C

FAN1 ACES-CON4-4-GP

20.F0765.004

2nd = 20.F1808.004

EC2801 DY Do Not Stuff

EC2802 DY Do Not Stuff

20100707_EMI

3D3V_S0

R280 6K8R2J-GP

SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0

R260 68R2-GP

C388 SCD1U10V2KX-4GP

2103_VDD

U31

H_THERMDA

H_THERMDC

REMOTE2+

REMOTE2-

SC 1203

THERM_SCI#

TP66 Do Not Stuff

R272 Do Not Stuff

THERM_SYS_SHDN#

THERM_SCI# R

27,86 SMBC_THERM

27,86 SMBD_THERM

VDD

DP1

DN1

DP2/DN3

ND2/DP3

SYS_SHDN#

ALERT#

SMCLK

SMDATA

GPIO1

GPIO2

TACH

PWM

TRIP_SET

SHDN_SEL

GND

GND

EMC2103-2-AP-GP

2103_4

2103_5

TP65 Do Not Stuff

TP67 Do Not Stuff

TRIP_SET_R276

649R2F-GP

T8 = 98

TRIP_SET: 649 ohm => 87 dgree C

RN49

SRN10KJ-5-GP

3D3V_S0

D2802

CH551H-30PT-GP

FAN_TACH

FAN_PWM

2ND = 83.5R003.08F

3rd = 83.R5003.G8F

83.R5003.C8F

AFTP2803

AFTP2802

AFTP2801

FAN_PWM_C

FAN_TACH

5V_S0_FAN

SB_0825

pin6, ALERT# OD

pin7, SYS_SHDN# OD

3D3V_AUX_S5

D2803 Do Not Stuff

Do Not Stuff

2ND = 83.BAT54.D81

3rd = 83.BAT54.S81

DY

27,36,86 PURE_HW_SHUTDOWN#

R2812 DY Do Not Stuff

C2811 DY Do Not Stuff

Q2802

2N7002K-2-GP

1st = 84.2N702.031

2ND = 84.2N702.J31

THERM_SYS_SHDN#

R2809 100KR2J-1-GP

R2810 DY Do Not Stuff

R2811 0R2J-2-GP

3D3V_S0

IMVP_PWRGD 36,42

SB_0812

55.4KZ01.S18G S19G

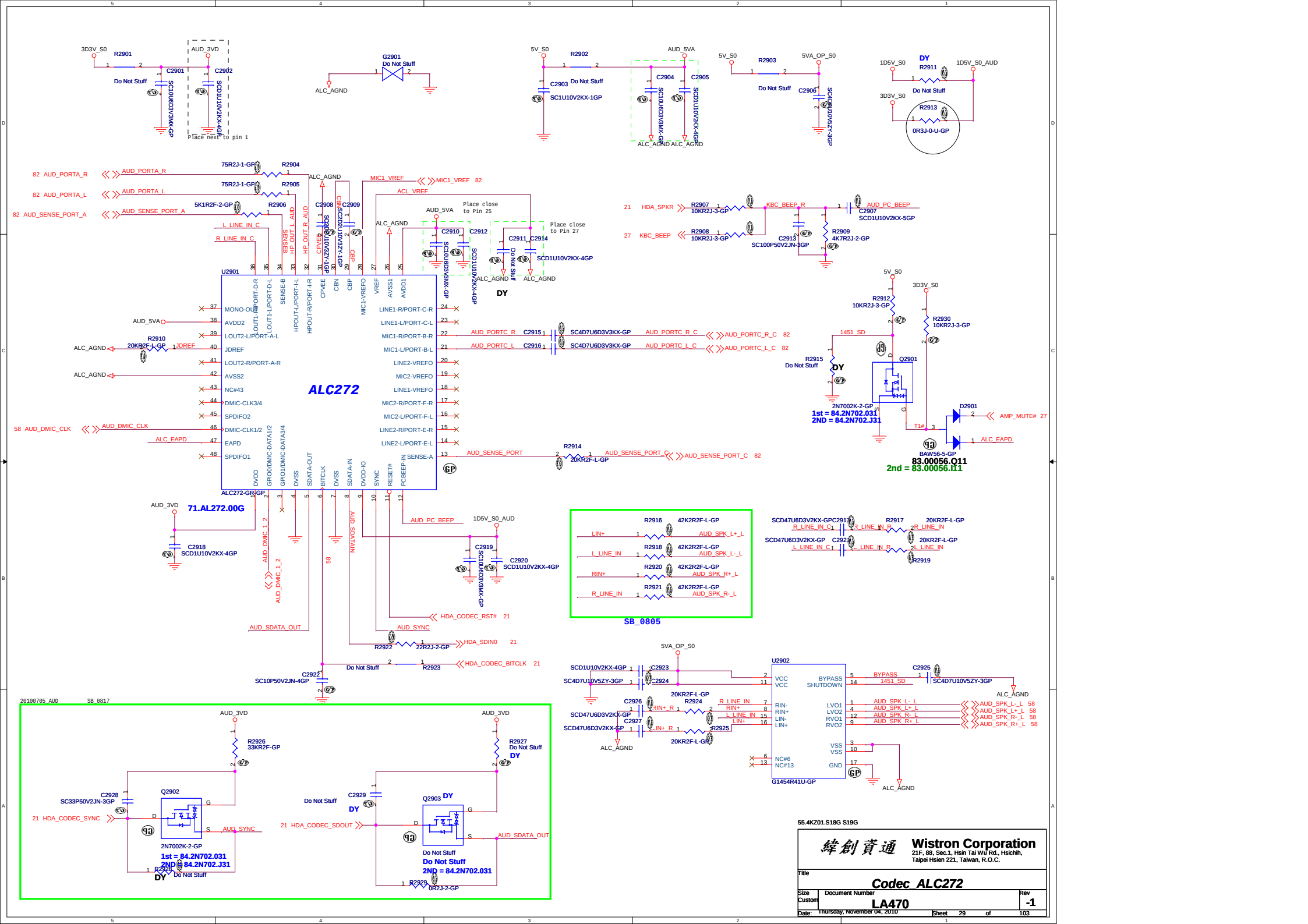
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 28 of 103


ALC272
ALC272-GR-GP
71.AL272.00G
83.00056.Q11
2nd = 83.00056.I11
1st = 84.2N702.031
2ND = 84.2N702.J31
SB_0805
20100705_AUD SB_0817
Do Not Stuff
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Codec_ALC272
LA470
Rev -1
Thursday, November 04, 2010
Sheet 29 of 103

55.4KZ01.S18G S19G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

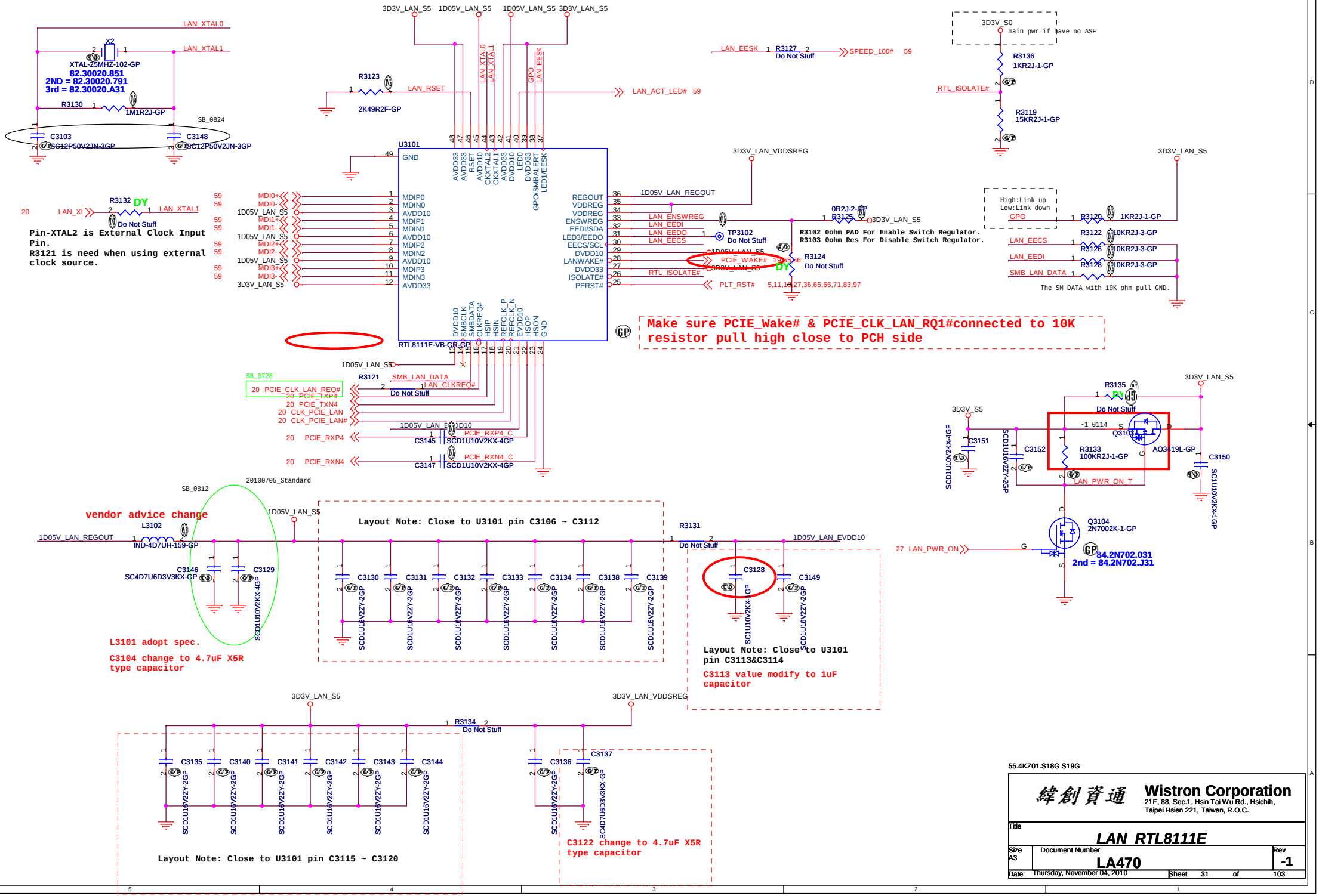
Title

Audio AMP

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 30 of 103

25MHz XTAL



55.4KZ01.S18G S19G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111E

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 31 of 103

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A3	**LA470**	**-1**

Date: Thursday, November 04, 2010 Sheet 32 of 103

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **LA470**	Rev: **-1**
Date: Thursday, November 04, 2010	Sheet 33 of 103	

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 34 of 103

55.4KZ01.S18G S19G

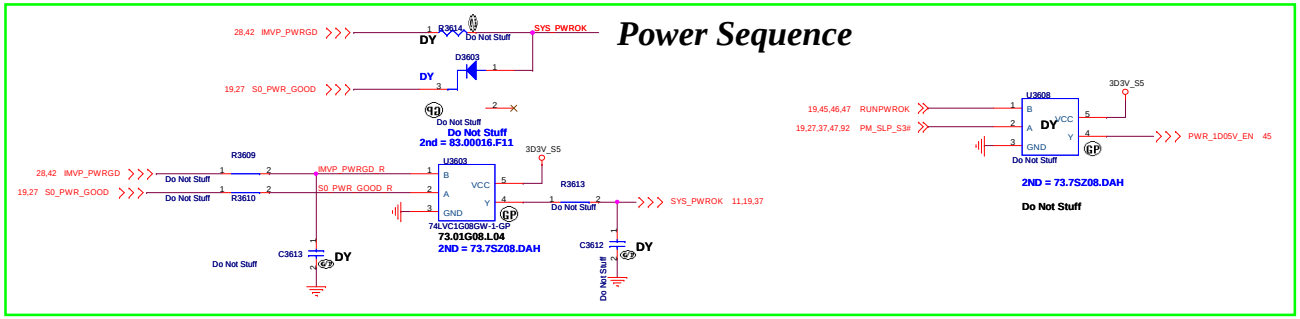
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

Size	Document Number	Rev
A3	LA470	-1

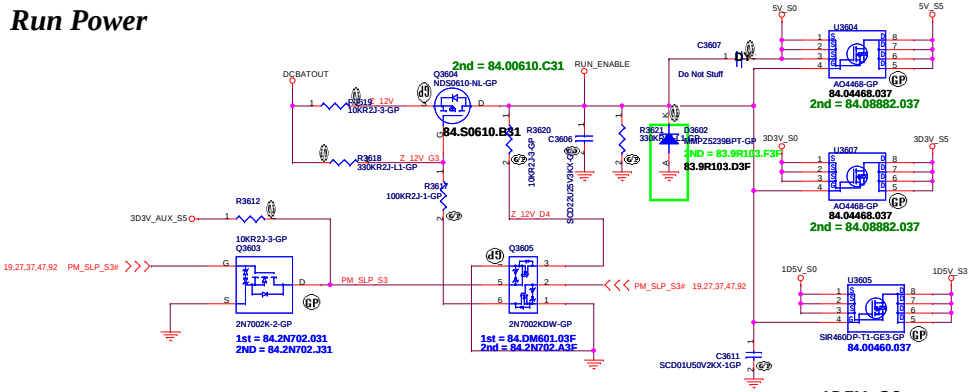
Date: Thursday, November 04, 2010 Sheet 35 of 103

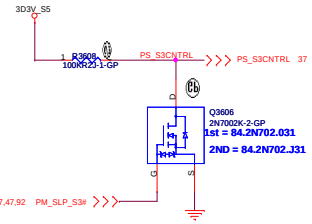
Power Sequence

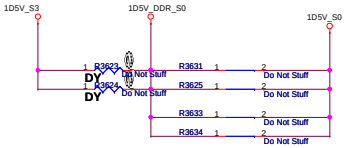


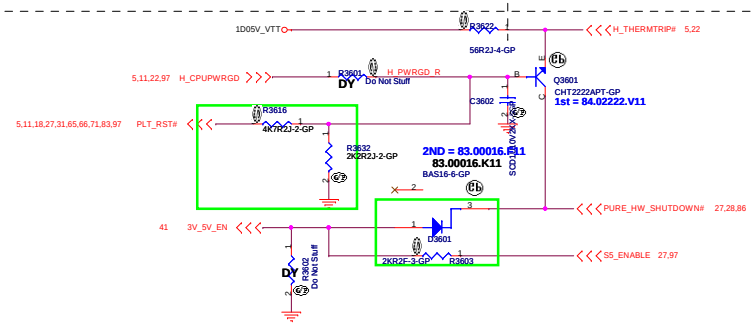
SSID = Reset.Suspend

Run Power









55.4KZ01.S18G S19G

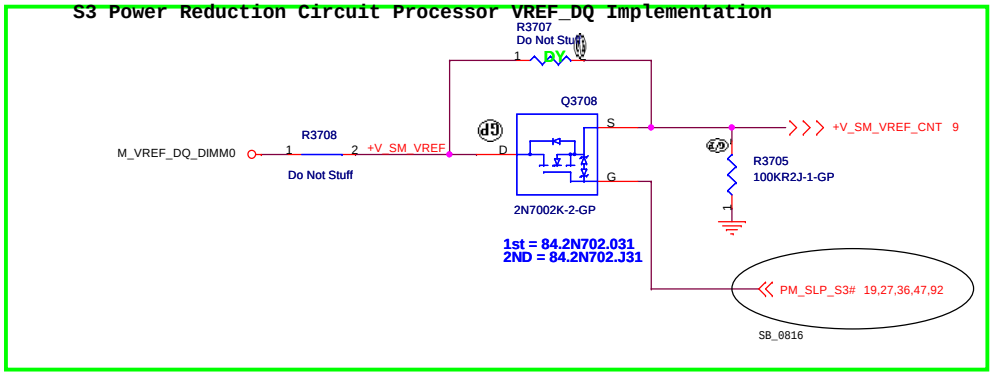
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

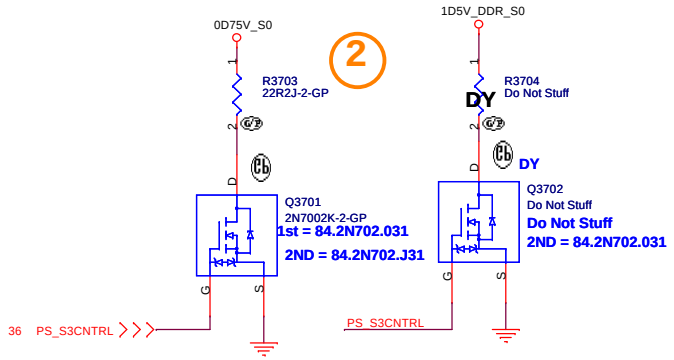
Size	Document Number	Rev
A2	LA470	-1

Date: Thursday, November 04, 2010 Sheet 36 of 103

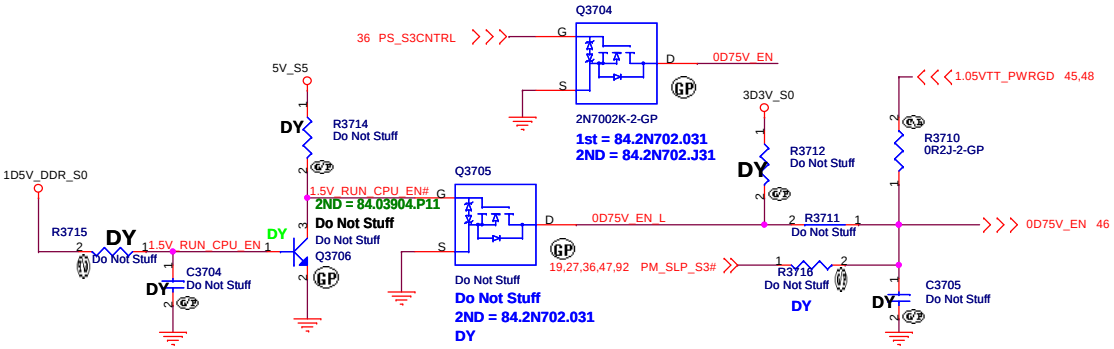
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



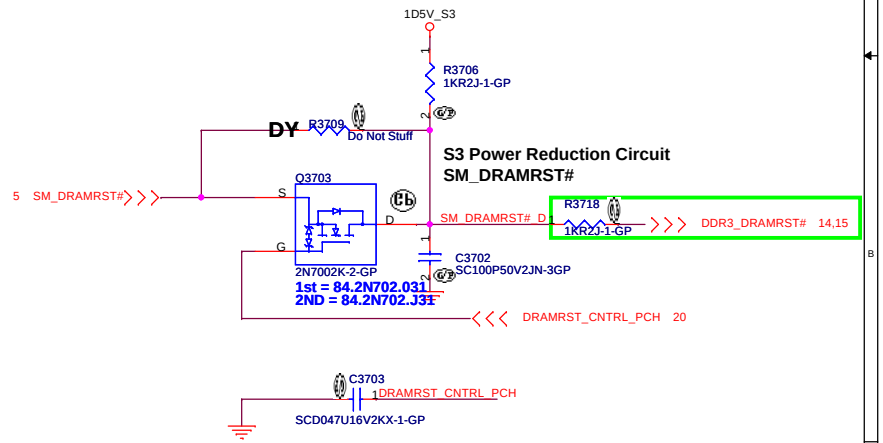
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



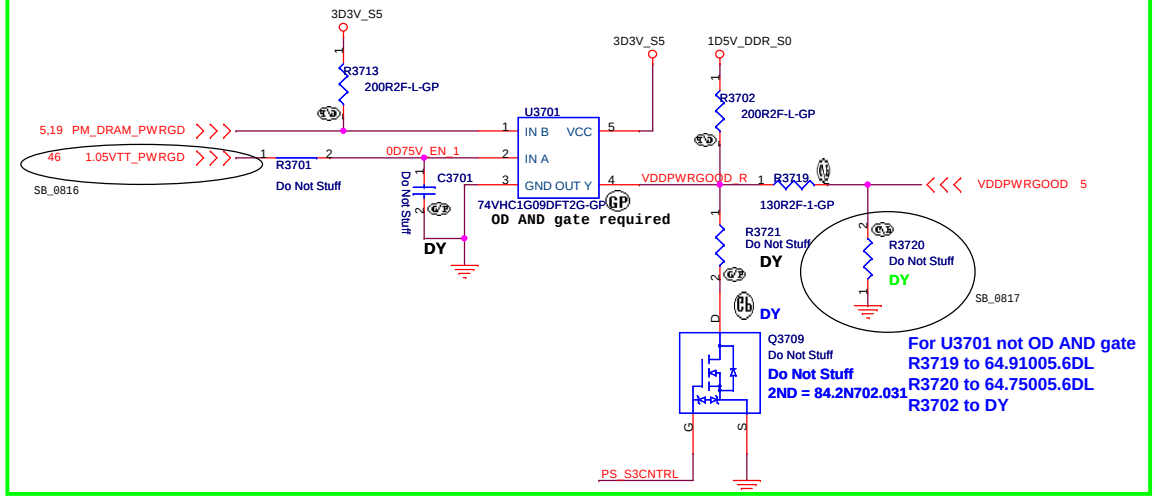
5 S3 Power Reduction X01 20091111



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



55.4KZ01.S18G S19G

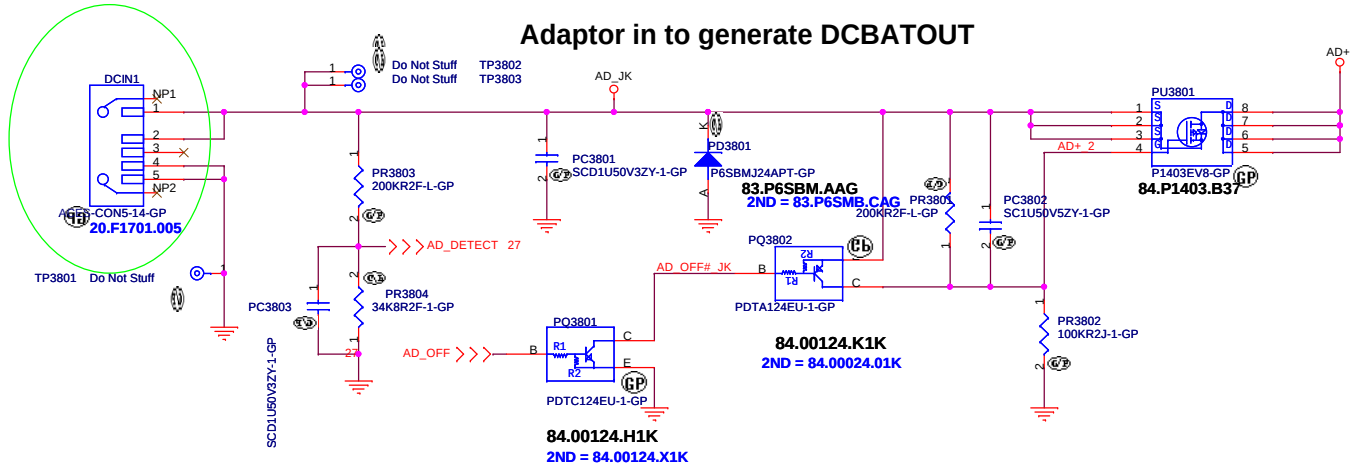
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 37 of 103

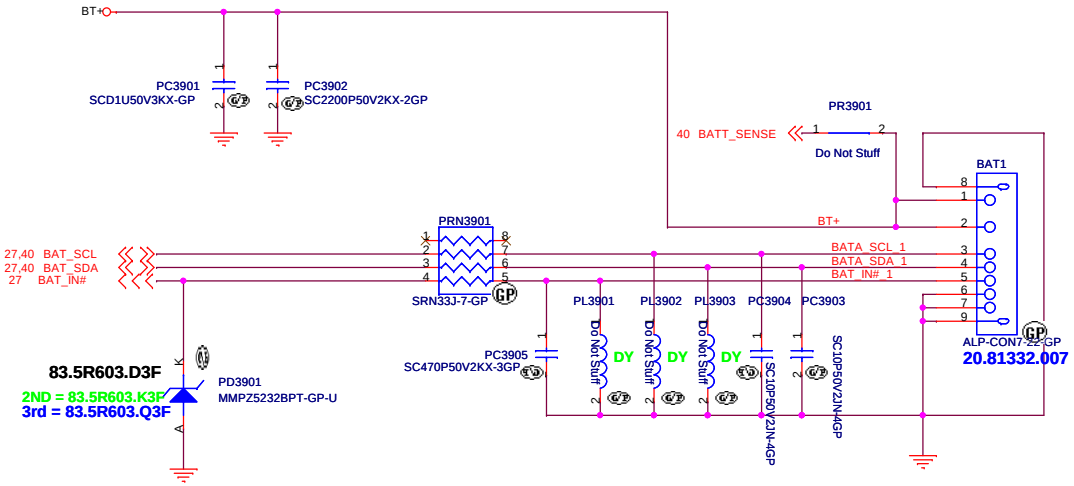
Adaptor in to generate DCBATOUT



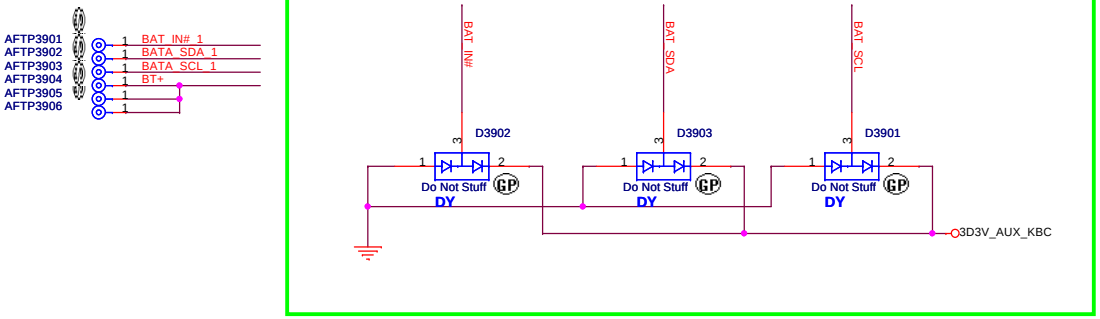
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN_JACK*		
Size	Document Number: **LA470**	Rev: **-1**
Date: Thursday, November 04, 2010	Sheet 38 of 103	

BATTERY CONNECTOR



SB_0818



DY ???

55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT_CONN		
Size	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 39 of 103	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

AD+

PU4001 P1403EV8-GP 84.P1403.B37

PR4002 100KR2J-1-GP

AD+_G_2

PR4001 10KR2F-2-GP

PR4003 49K9R2F-L-GP

AD+_G_1

DC_IN_D

PQ4001 2N7002KDW-GP

1st = 84.DM601.03F
2nd = 84.2N702.A3F

BQ24745_ACOK

AD+_TO_SYS

PR4004 D01R3721F-GP-U

DCBATOUT

BT+

PU4002 P1403EV8-GP 84.P1403.B37

PD4002 SMF18A-GP 83.SMF18.AAH

PR4005 470KR2J-2GP

20100518 WAYNE

PG4001 Do Not Stuff

PG4002 Do Not Stuff

STOP_CHG# connects to KBC

3D3V_AUX_S5

PR4009 10KR2F-2-GP

STOP_CHG#

27 STOP_CHG

PD4001 1SS400GPT-GP 83.00400.C1F 2nd = 83.1S400.B2F

BQ24745_VREF

R1 PR4007 121KR2F-L-GP BOM Ctrl

20100707

R2 PR4008 49K9R2F-L-GP

CHG_AGND

CHG_ICREF

PC4002 SCD1U50V3KX-GP

BQ24745_CSSP

PC4003 SCD1U50V3KX-GP

PC4004 SCD1U25V3KX-GP

PC4001 SC1U25V3KX-1GP

PR4006 316KR3F-2-GP

PU4003 BQ24745RHDR-GP

74.24745.073

BQ24745_DCIN	22	DCIN	
BQ24745_ACIN	2	ACIN	
	11	VDDSMB	
	13	ACOK	
	10	SCL	
	9	SDA	
	14	NC#14	
BQ24745_IINP	8	VICM	
	6	FBO	
	5	EAI	
	4	EAO	
	3	VREF	
	7	CE	
	12	GND	
ICREF			
CSSP	28		
BQ24745_CSSN	27	CSSN	
BQ24745_ICOUT	26	ICOUT	
BQ24745_BST	25	BOOT	
BQ24745_VDDP	21	VDDP	
24745_HIGH_G	24	UGATE	
BQ24745_LX1	23	PHASE	
24745_LOW_G	20	LGATE	
	19	PGND	
	18	CSOP	
	17	CSON	
	16	NC#16	
BATT_SENSE	15	VFB	
GND	29		

PR4012 Do Not Stuff

PD4003 CH520S-30PT-GP

PC4009 SC1U10V3KX-3GP

PU4004 SIS412DN-T1-GE3-GP

83.R0203.08F
2nd = 83.1R003.I8F

Do Not Stuff

PC4025 DY Do Not Stuff

PC4023 SC1U25V6KX-1GP

PC4005 SC1U25V6KX-1GP

PC4006 SCD1U25V2ZY-1GP

PL4001 IND-5D6UH-39-GP 68.5R610.10P

PR4017 D01R3721F-GP-U

BT+_R

SC_1021

PU4005 SIS412DN-T1-GE3-GP

PC4016 SCD1U50V3KX-GP

PG4003 Do Not Stuff

PG4004 Do Not Stuff

20100518 WAYNE

PC4020 SC1U25V6KX-1GP

PC4021 SC1U25V6KX-1GP

PC4022 SCD1U50V3KX-GP

PR4010 49K9R2F-L-GP

PC4007 SCD01U50V2KX-1GP

AC_IN

PR4011 Do Not Stuff

BQ24745_ACOK

27,39 BAT_SCL

27,39 BAT_SDA

PC4008 SC1U10V3KX-3GP

PR4013 Do Not Stuff

27 AD_IA

SC150P50V2JN-3GP

PC4010

BQ24745_FBO_RC

PR4014 4K7R2J-2-GP

BQ24745_FBO

PR4015 200KR2F-L-GP

BQ24745_EAI

BQ24745_EAO

BQ24745_VREF

BQ24745_CHG_ON

PC401 SC220P50V2KX-3GP

PC4012 SC2200P50V2KX-2GP

BQ24745_EAO_RC

PR4016 7K5R2F-1-GP

PC4013 SC56P50V2JN-2GP

PC4014 SC1U10V3KX-3GP

BATT_SENSE 39

MAX8731A_CSIP

MAX8731A_CSIN

PC4015 SCD1U25V2ZY-1GP

PR4018 Do Not Stuff

BQ24745_VREF

PRN4001 SRN100KJ-5-GP

AC_IN

CHG_ON#

BQ24745_CHG_ON

3D3V_AUX_S5

SC_1019

SB_0812

PQ4002 2N7002K-2-GP

1st = 84.2N702.031
2ND = 84.2N702.J31

BQ24745_CHG_ON

DY C4001

Do Not Stuff

CHG_ON#

CHG_ON# 27

AC_IN to KBC

55.4KZ01.S18G S19G

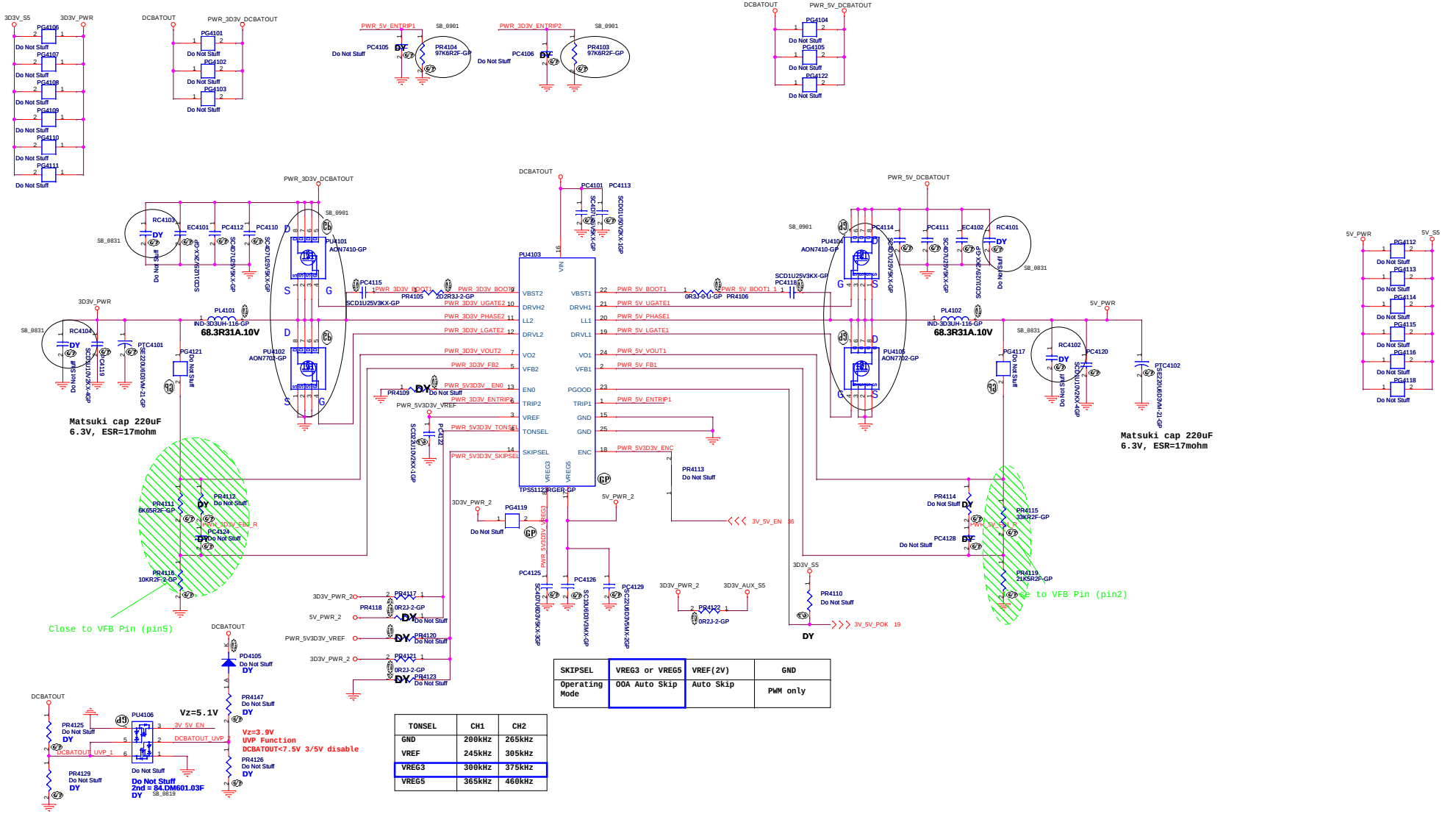
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24745

Size: | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v

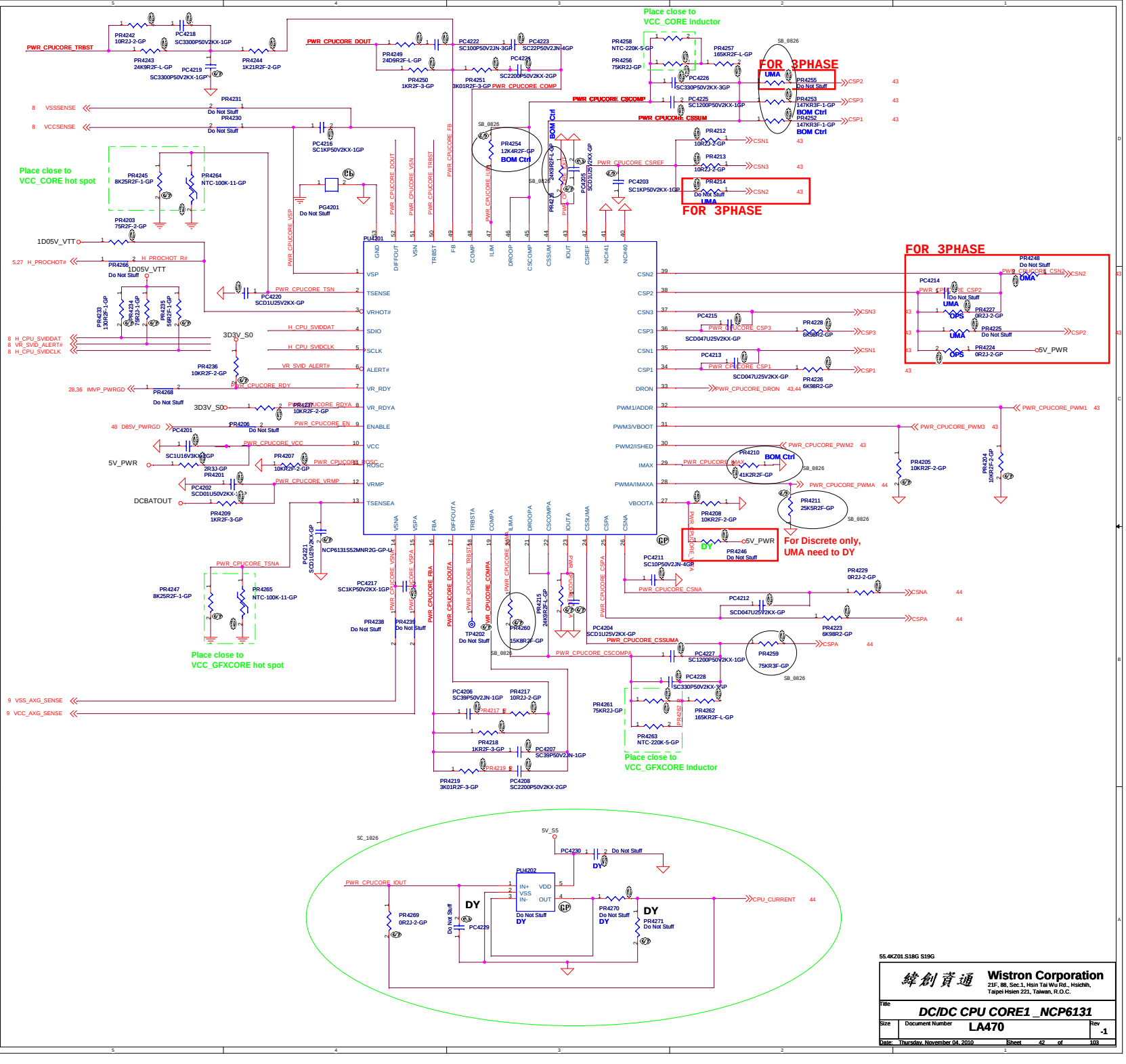


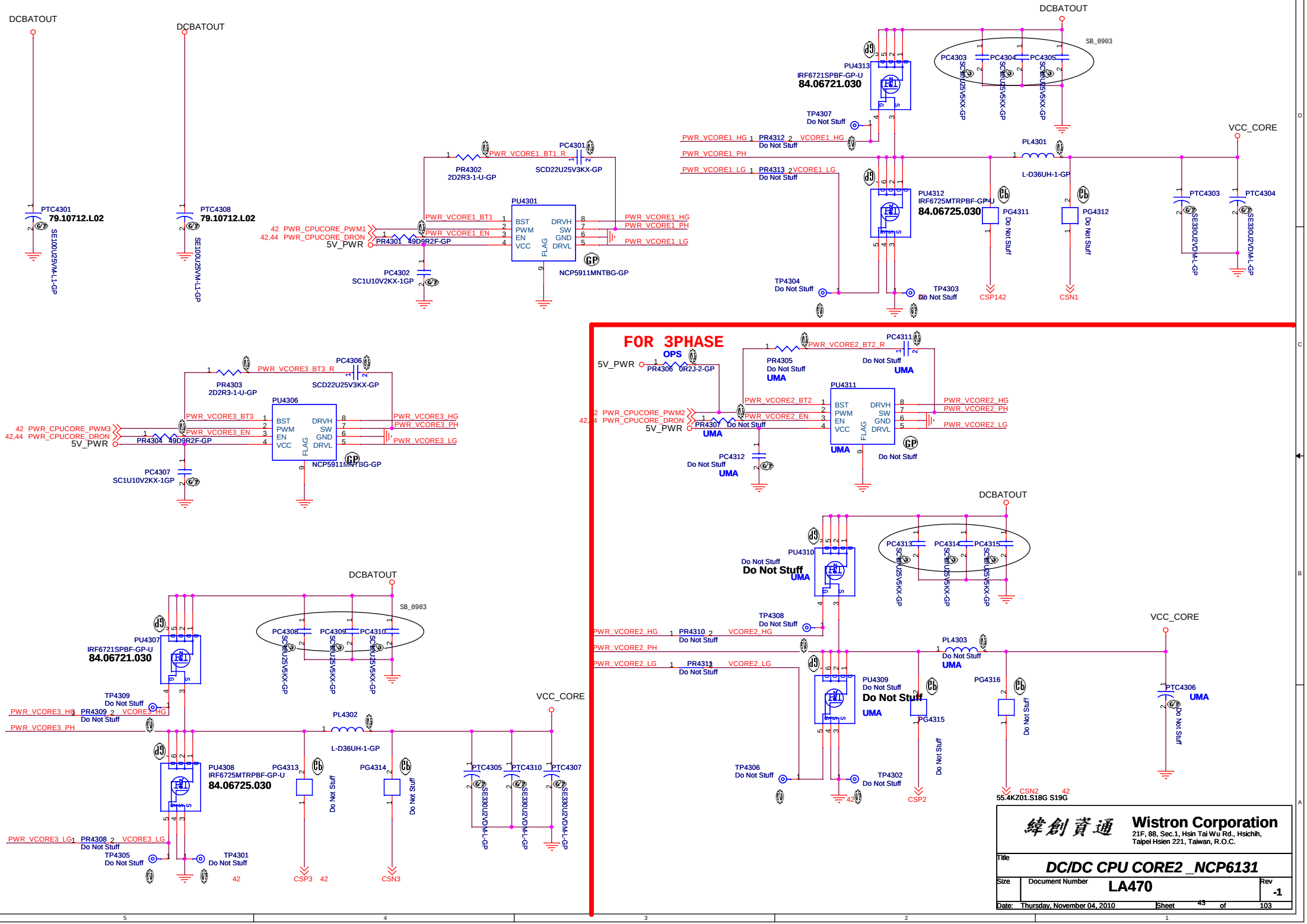
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

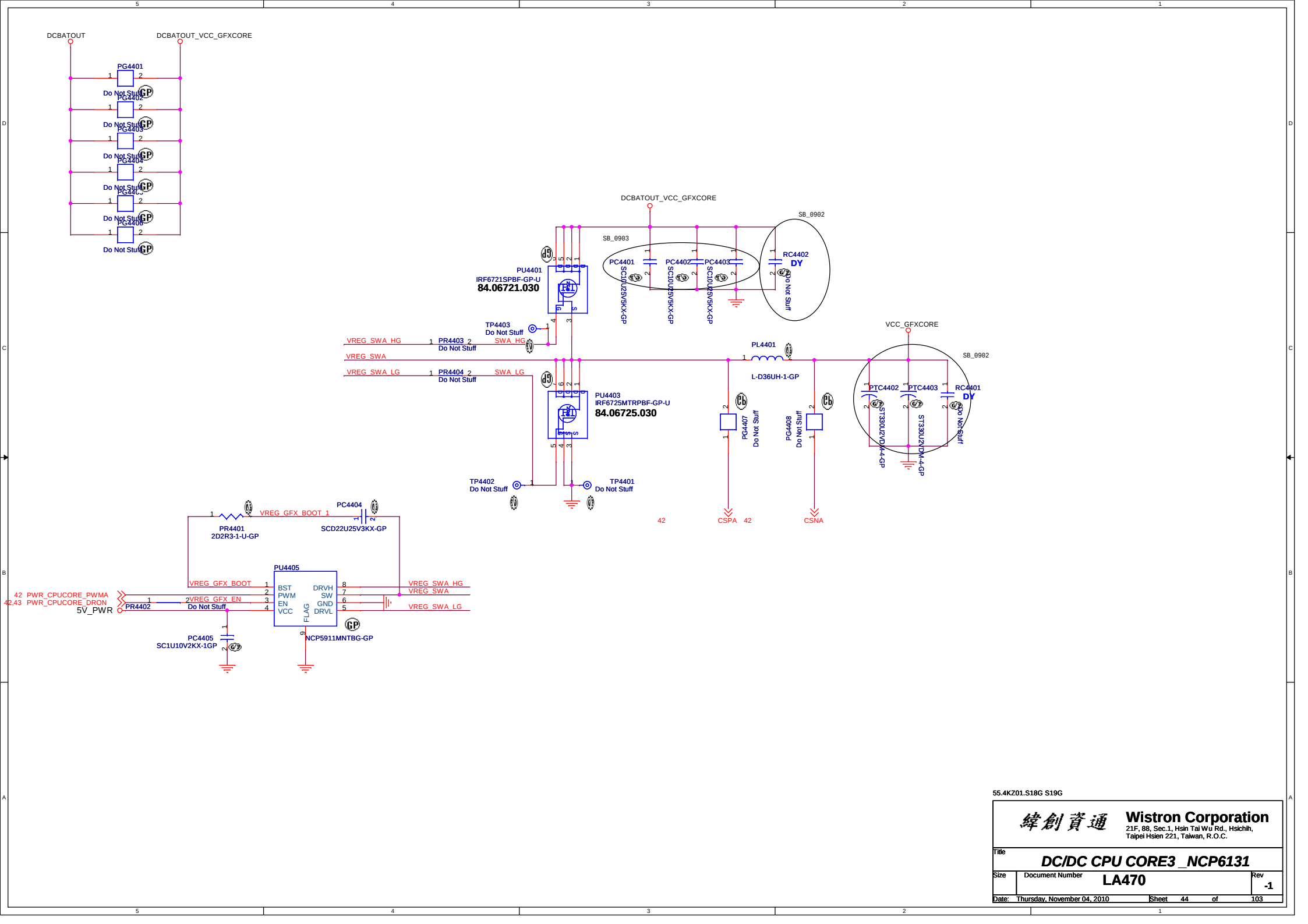
55.4KZ01.S18G S19G

緯創資通	Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC/DC 3D3V5V
Size	Document Number: LA470 — Rev: -1
Date: Thursday, November 04, 2010	Sheet 41 of 103


Place close to
VCC_CORE Inductor
FOR 3PHASE
UMA
Do Not Stuff
BOM Ctrl
PWR_CPUCORE_TRBST
PWR_CPUCORE_DOUT
PWR_CPUCORE_CSCOMP
PWR_CPUCORE_CSSUM
PWR_CPUCORE_CSREF
PWR_CPUCORE_COMP
VSSSENSE
VCCSENSE
Place close to
VCC_CORE hot spot
1D05V_VTT
H_PROCHOT#
PU4201
VSP
TSENSE
VRHOT#
SDIO
SCLK
ALERT#
VR_RDY
VR_RDYA
ENABLE
VCC
ROSC
VRMP
TSENSEA
3D3V_S0
5V_PWR
DCBATOUT
PWR_CPUCORE_TSNA
Place close to
VCC_GFXCORE hot spot
VSS_AXG_SENSE
VCC_AXG_SENSE
For Discrete only,
UMA need to DY
Place close to
VCC_GFXCORE Inductor
SC_1026
PU4202
PWR_CPUCORE_IOUT
CPU_CURRENT
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC/DC CPU CORE1 _NCP6131
LA470
-1
Thursday, November 04, 2010
42
103



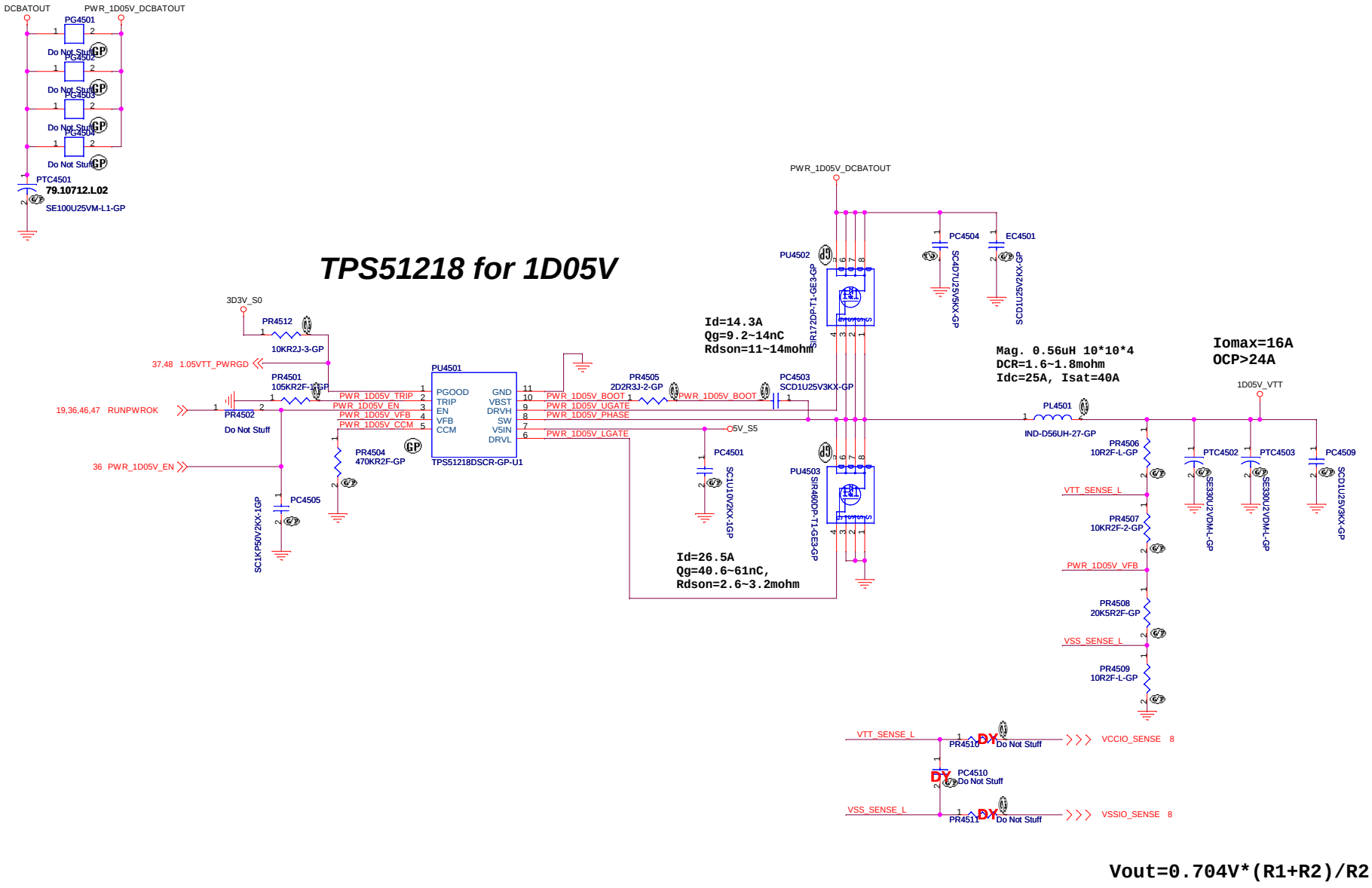
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***DC/DC CPU CORE2 _NCP6131***		
Size	Document Number **LA470**		Rev **-1**
Date: Thursday, November 04, 2010		Sheet 43 of 103	



55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

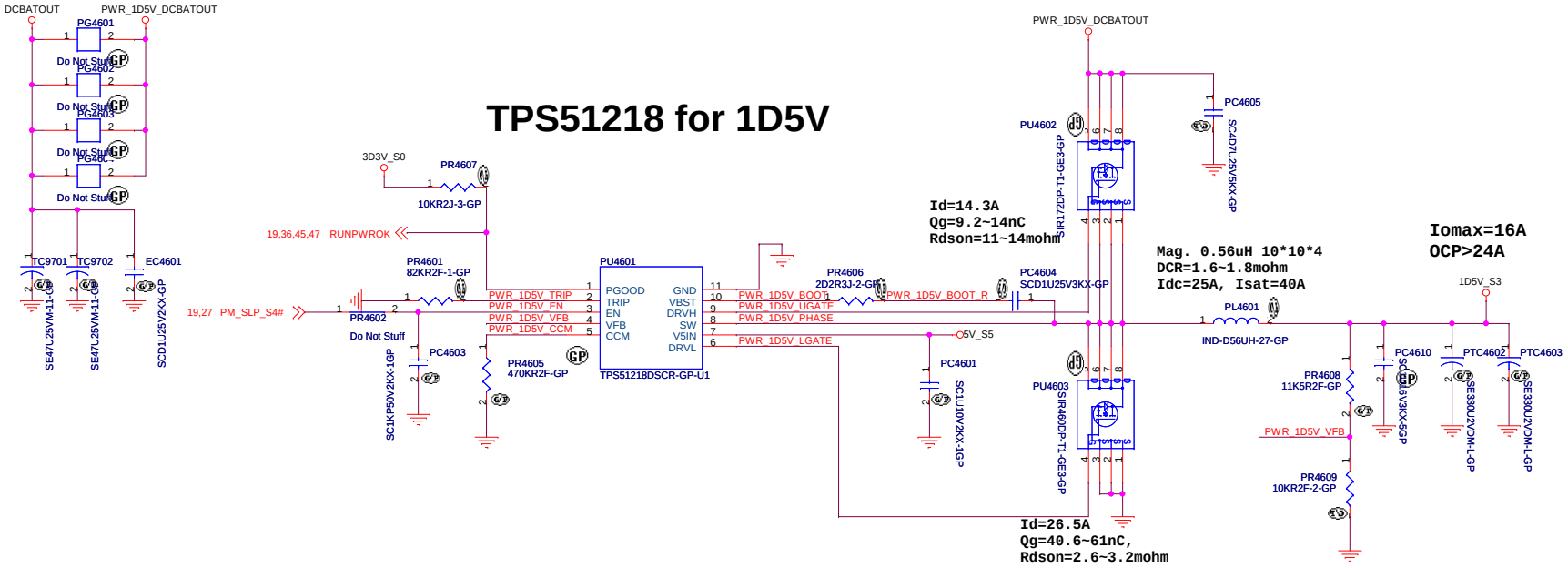
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LA470**	Rev **-1**
Date: Thursday, November 04, 2010	Sheet 44 of 103	

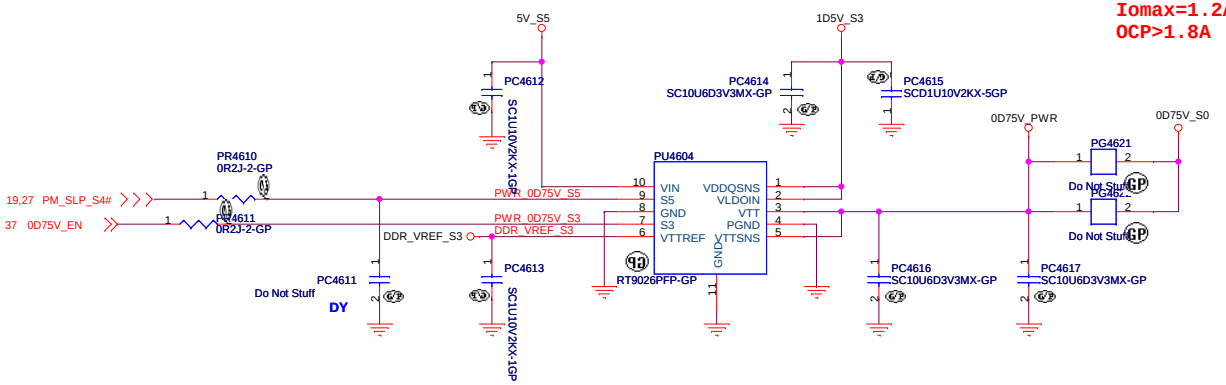


55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***TPS51218_1D05V***	
Size	Document Number	Rev -1
Date: Thursday, November 04, 2010	Sheet 45 of 103	





55.4KZ01.S18G S19G

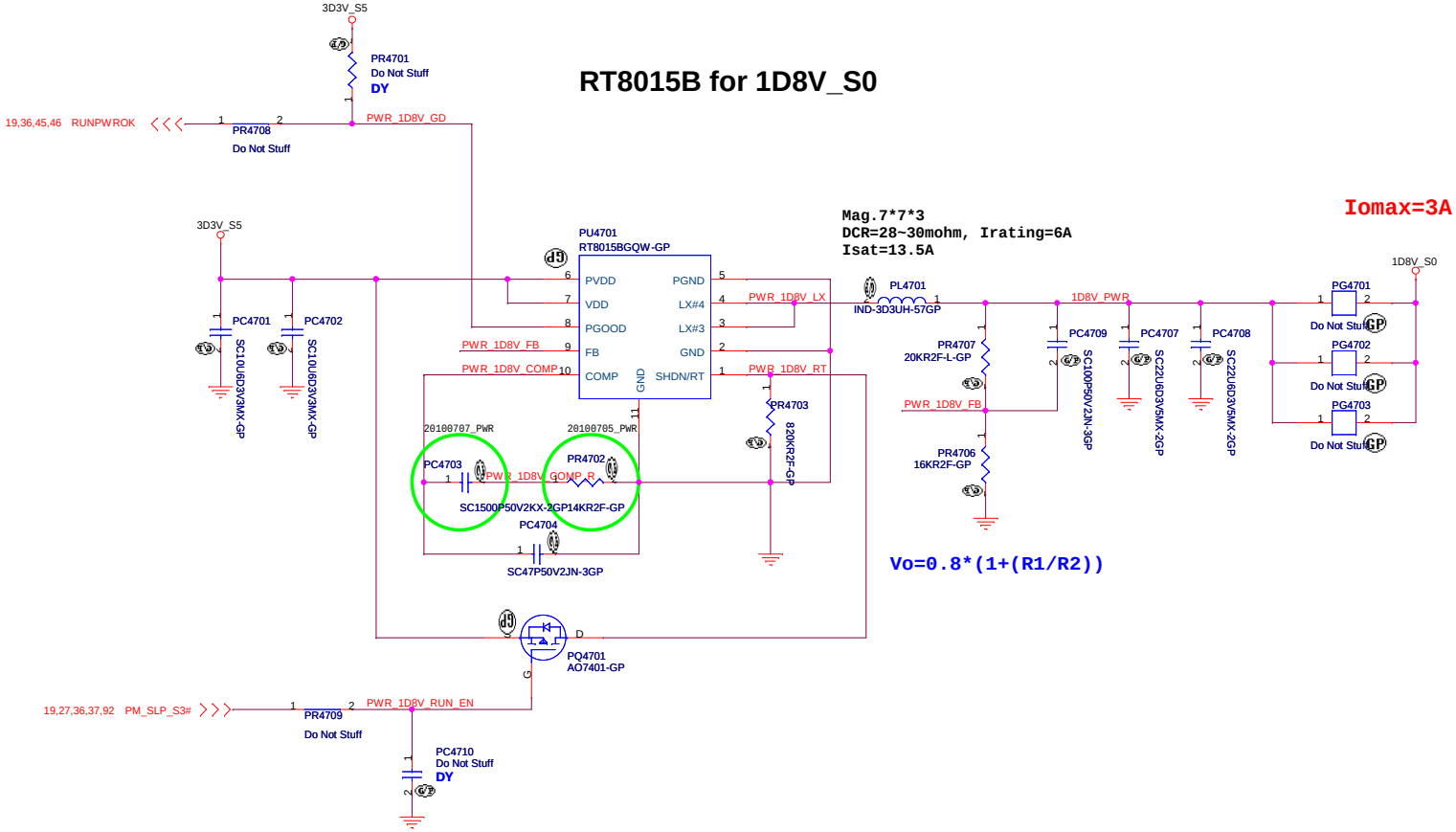
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		-1

Date: Thursday, November 04, 2010 Sheet 46 of 103

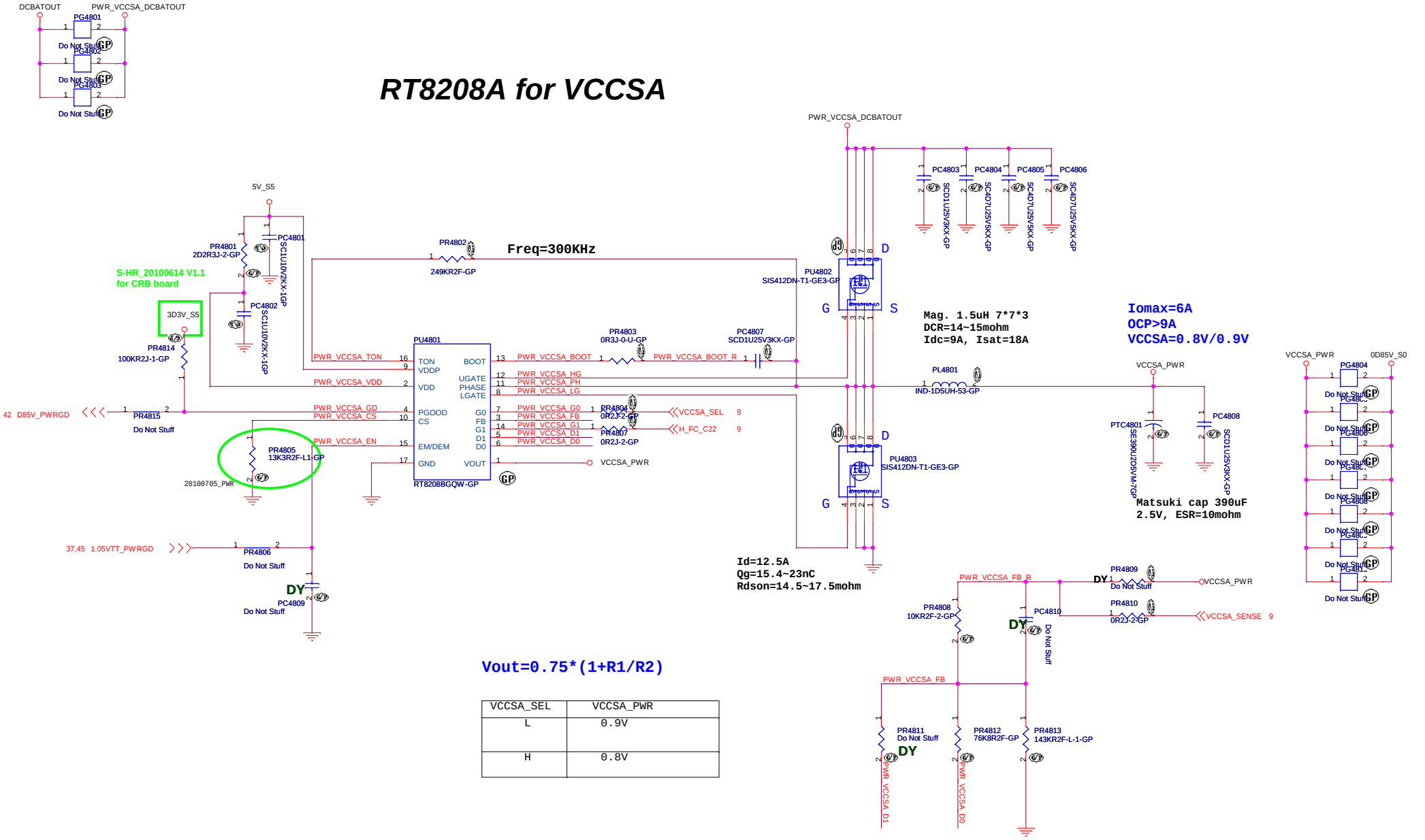
RT8015B for 1D8V_S0



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	PWM_1D8V_RT8015B	
Size	Document Number LA470	Rev -1
Date: Thursday, November 04, 2010	Sheet 47 of 103	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

55.4KZ01.S18G S19G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

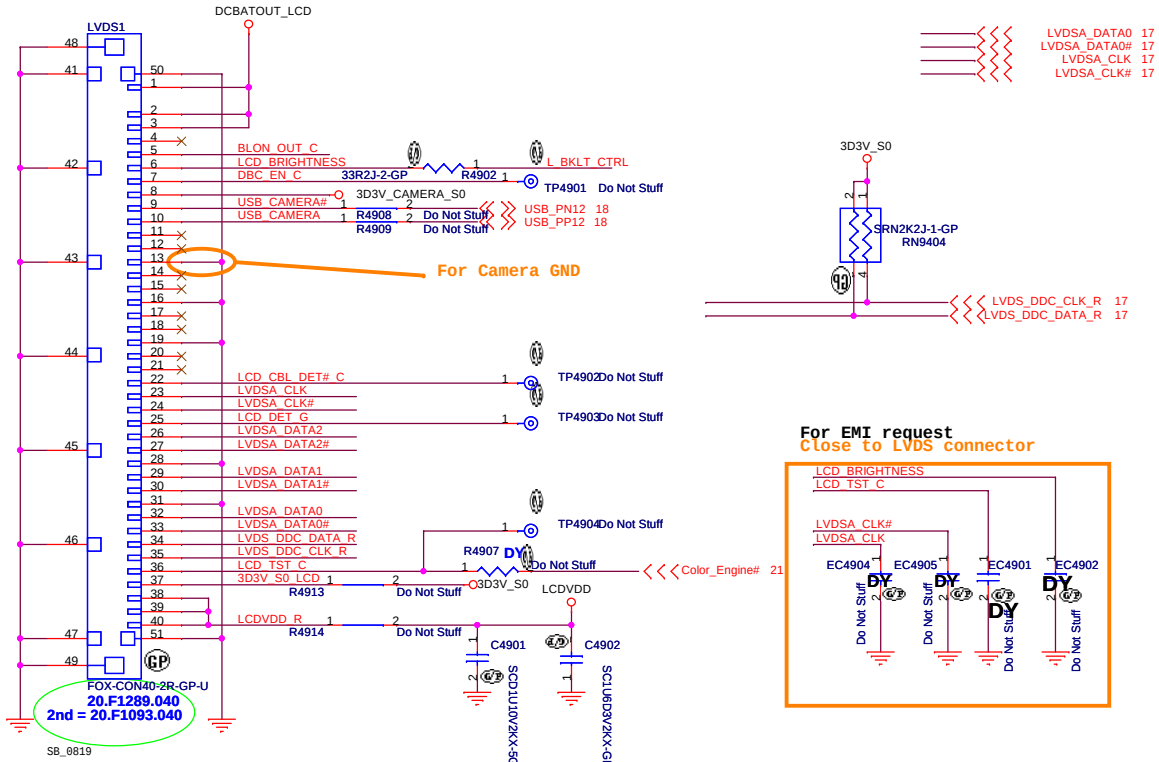
Title: RT8208B_VCCSA

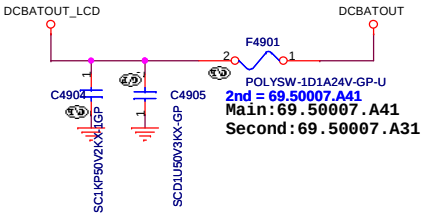
Size | Document Number: LA470 | Rev: -1

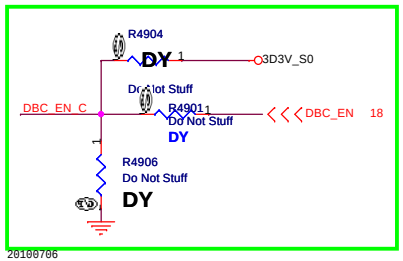
Date: Thursday, November 04, 2010 | Sheet 48 of 103

SSID = VIDEO

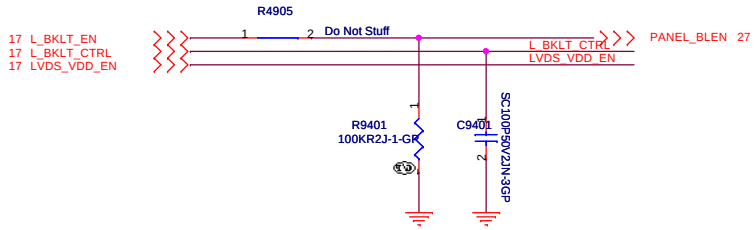
LVDS CONNECTOR



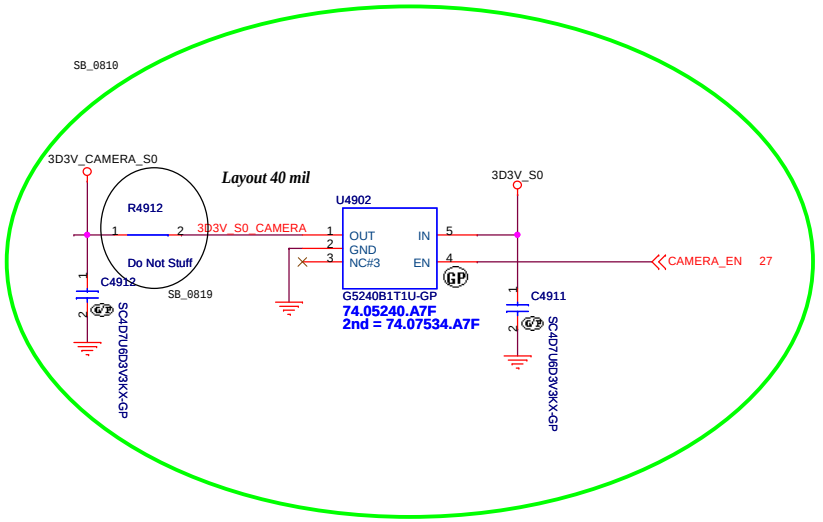




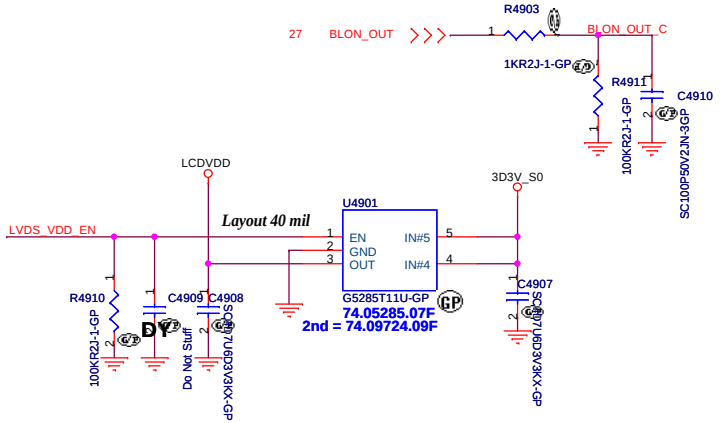
Panel BL brightness/Power En/BL En



CAMERA POWER



SSID = VIDEO



55.4KZ01.S18G S19G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
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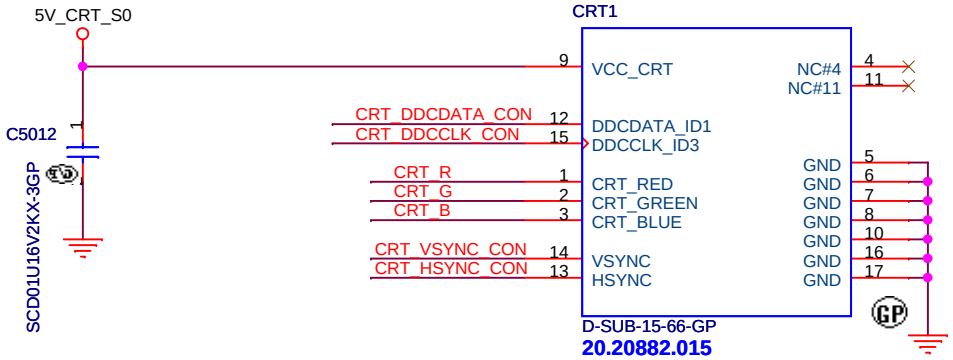
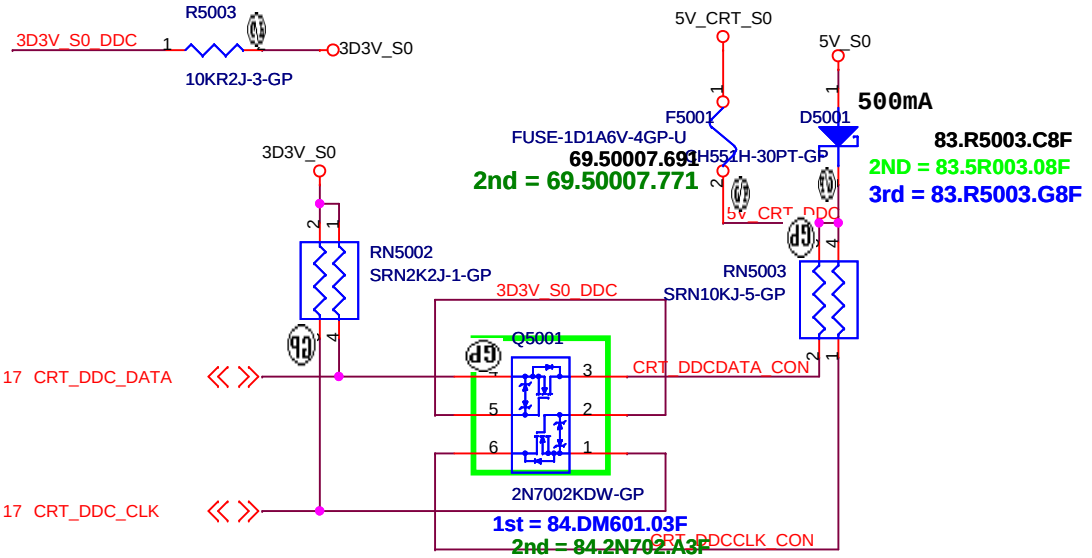
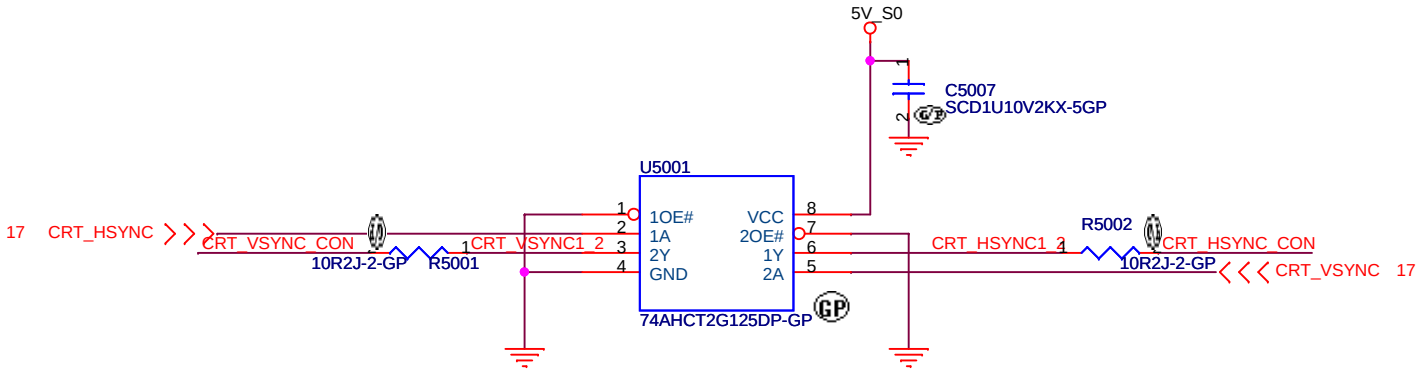


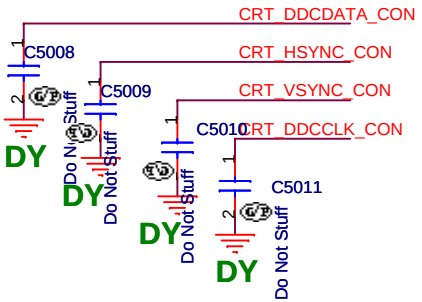
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board

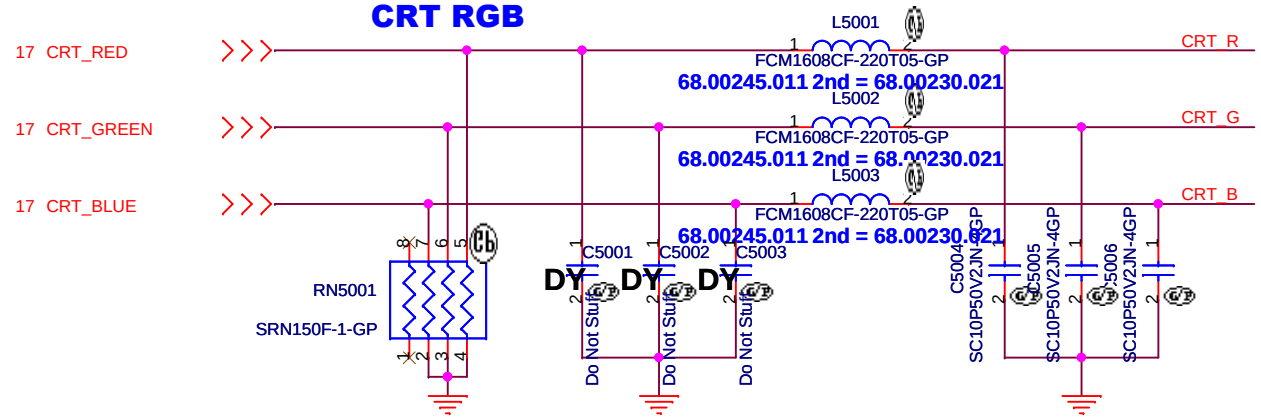


CRT Hsync & Vsync level shift





CRT RGB



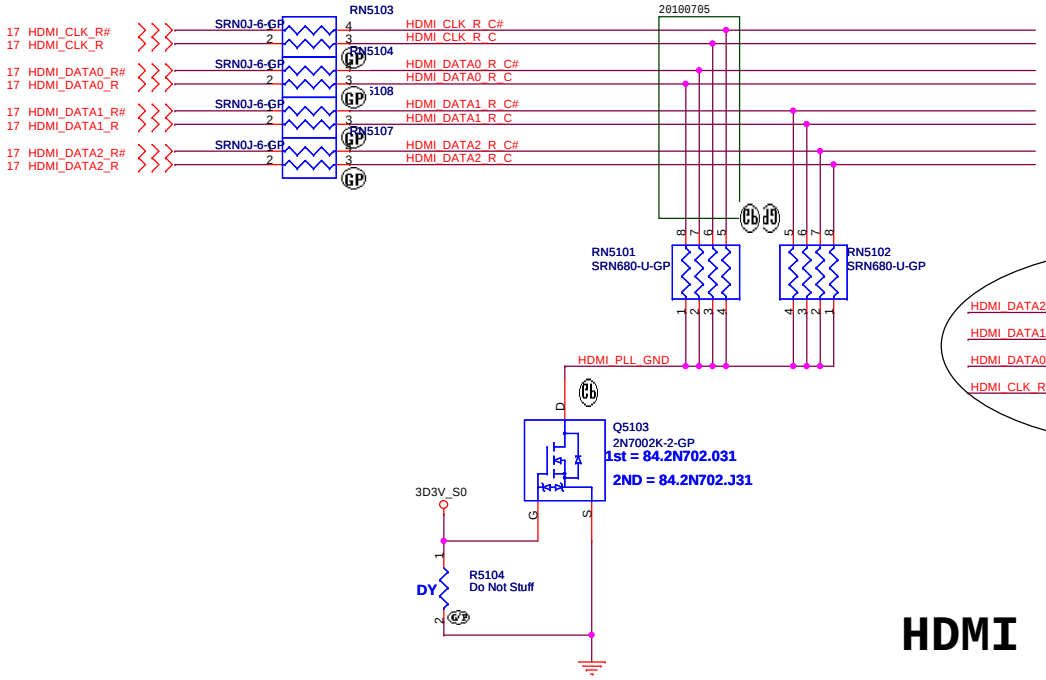
55.4KZ01.S18G S19G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Connector***	
Size A4	Document Number **LA470**	Rev **-1**
Date: Thursday, November 04, 2010	Sheet 50 of 103	

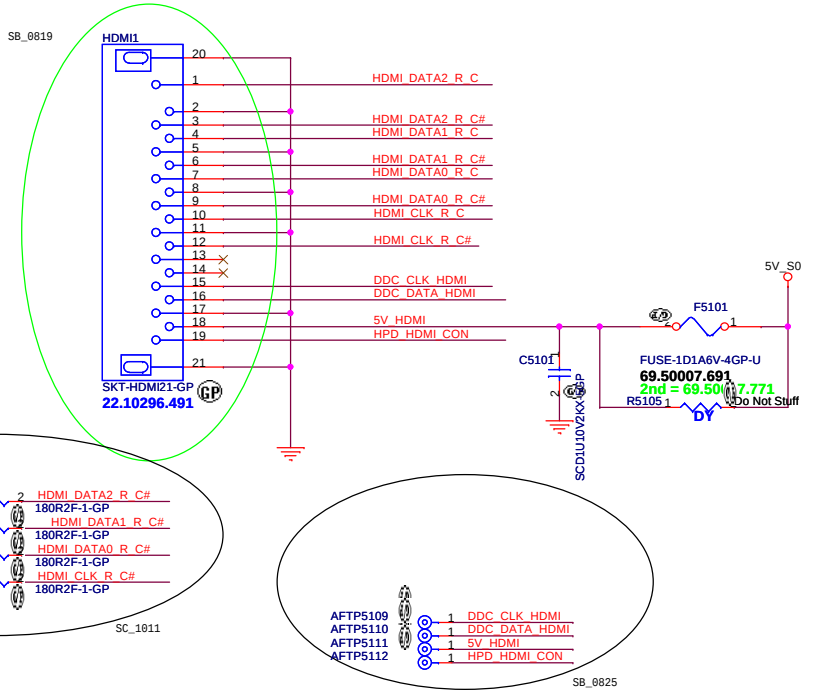
SSID = VIDEO

HDMI CONNECTOR

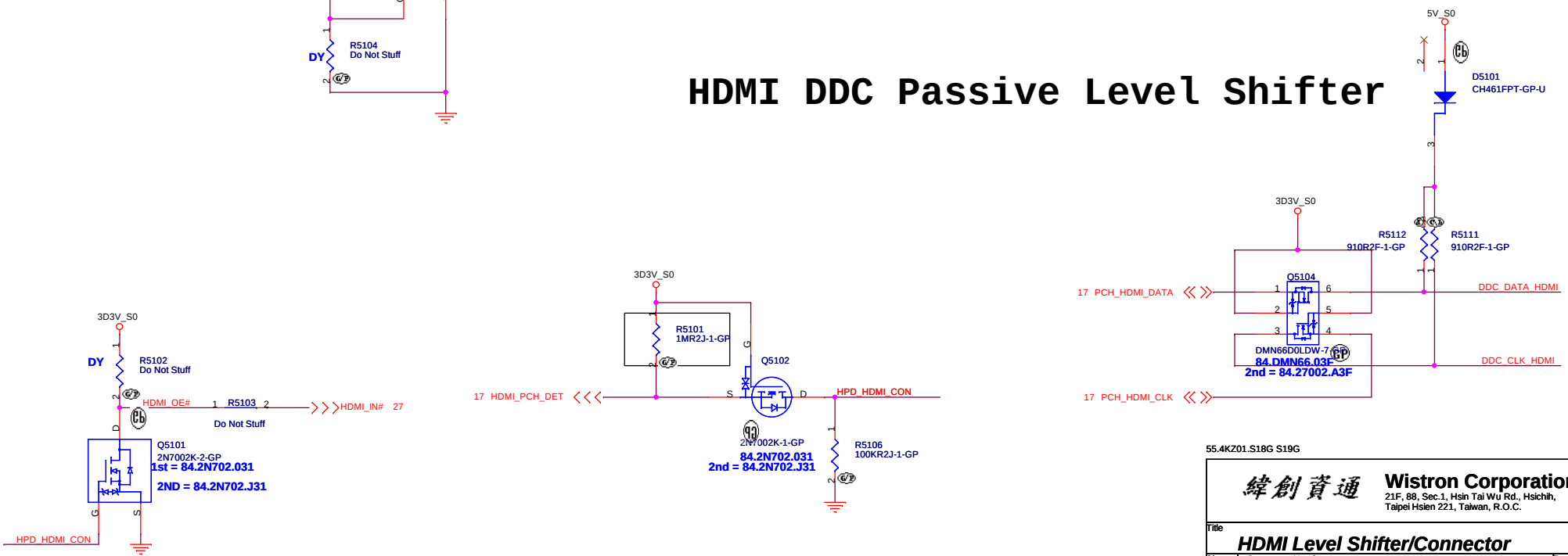
HDMI Passive Level Shifter



HDMI CONN



HDMI DDC Passive Level Shifter



55.4KZ01.S18G S19G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDMI Level Shifter/Connector		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 51 of 103	

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 52 of 103	

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 53 of 103

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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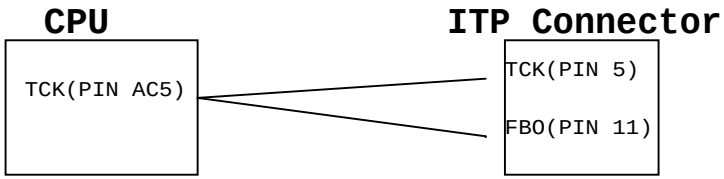
Date: Thursday, November 04, 2010 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



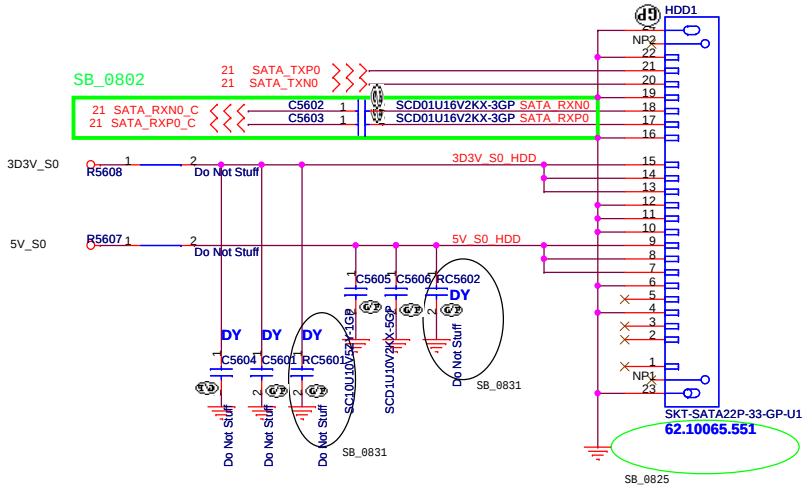
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

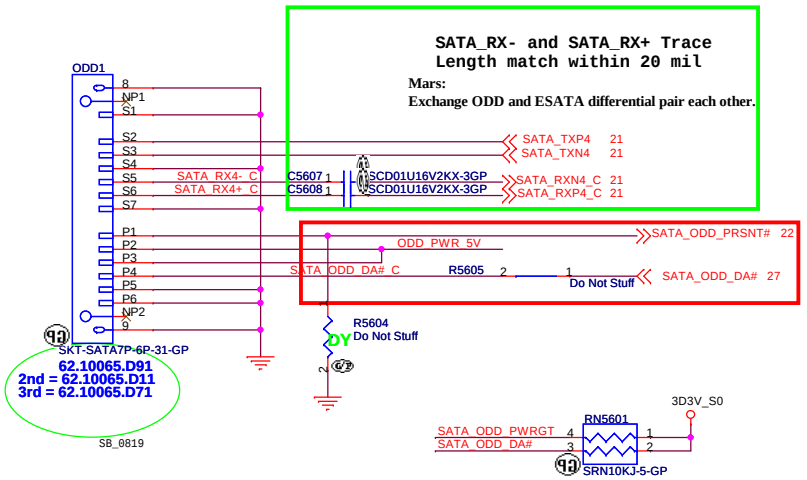
Title: ITP		
Size: A4	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 55 of 103	

SSID = SATA

SATA HDD Connector

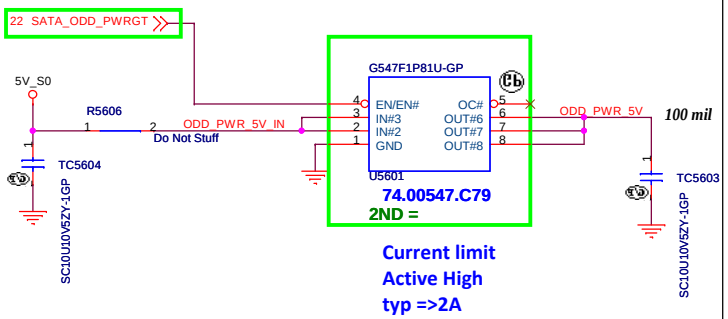


ODD Connector



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



55.4KZ01.S18G S19G

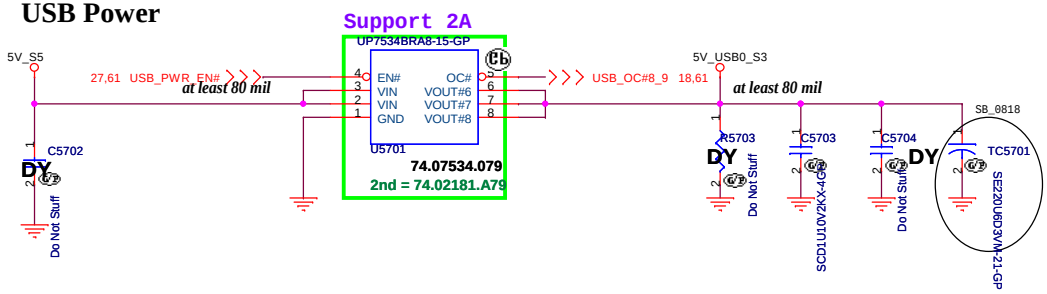
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

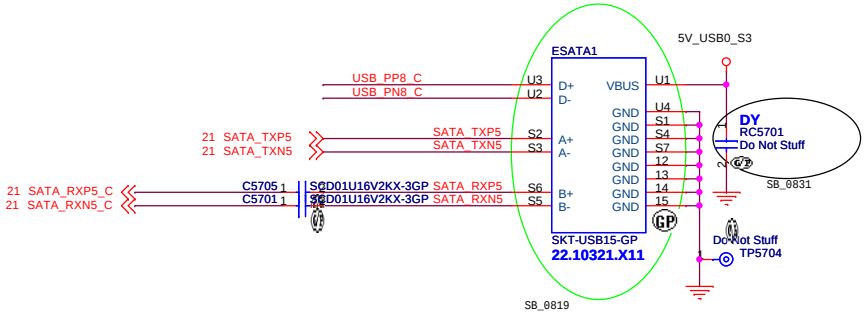
Title: HDD/ODD

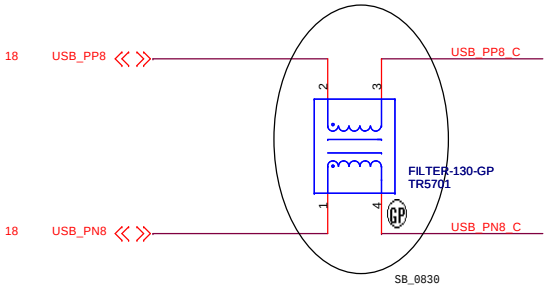
Size	Document Number	Rev
A3	LA470	-1

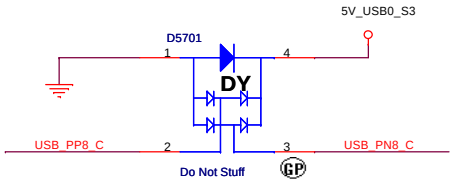
Date: Thursday, November 04, 2010 Sheet 56 of 103

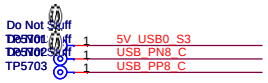
USB Power





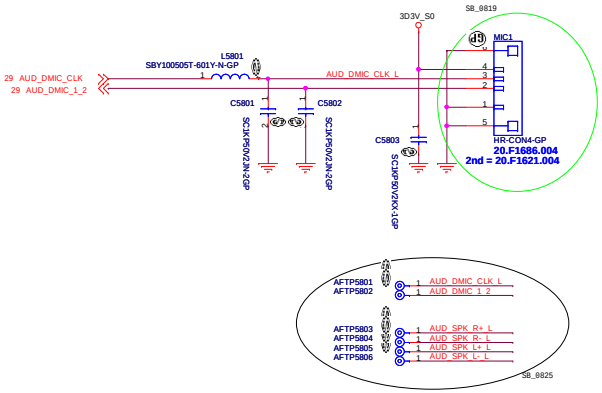






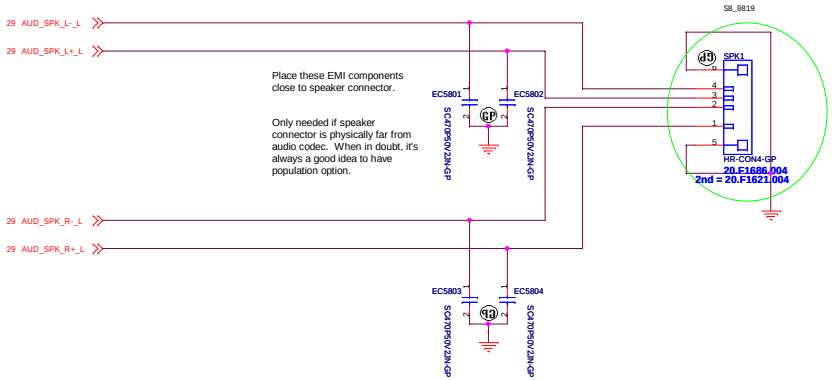
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: E-SATA		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 57 of 103	



INTERNAL STEREO SPEAKERS

Port G



55.4KZ01.S18G S19G

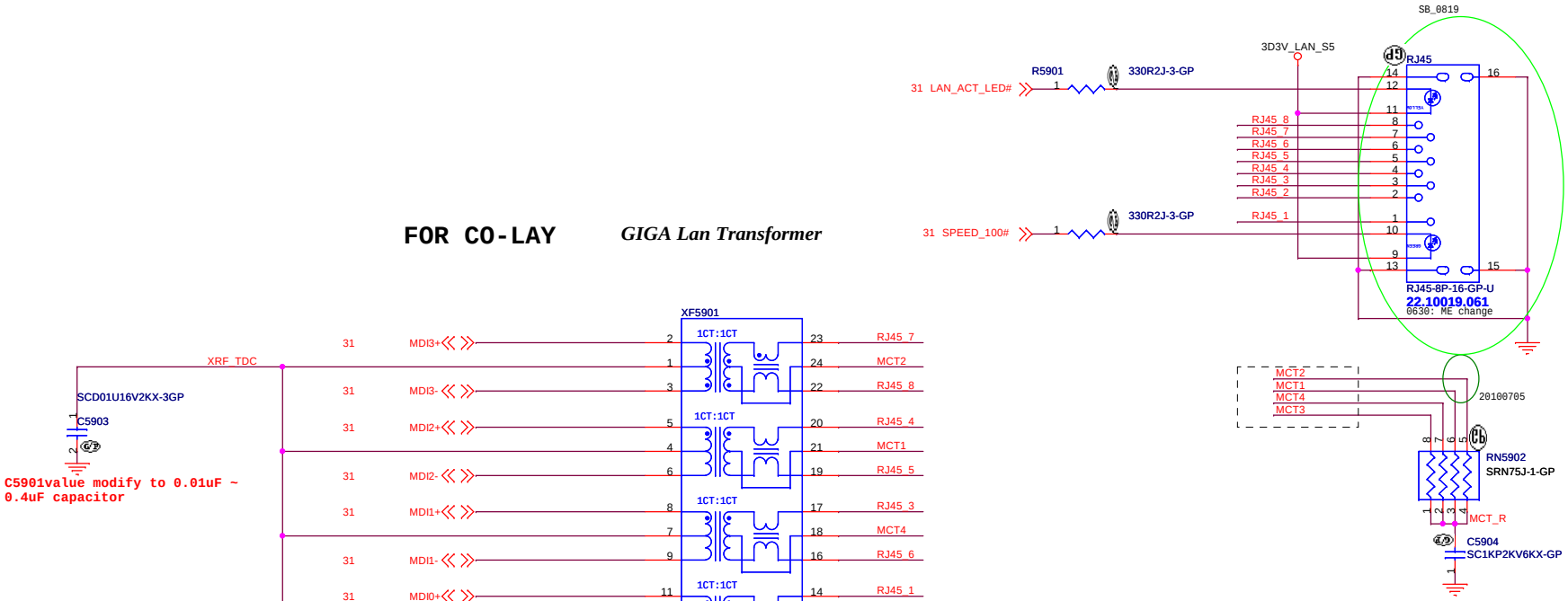
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
A2	LA470	-1

Date: Thursday, November 04, 2010 Sheet 58 of 103

LAN Connector

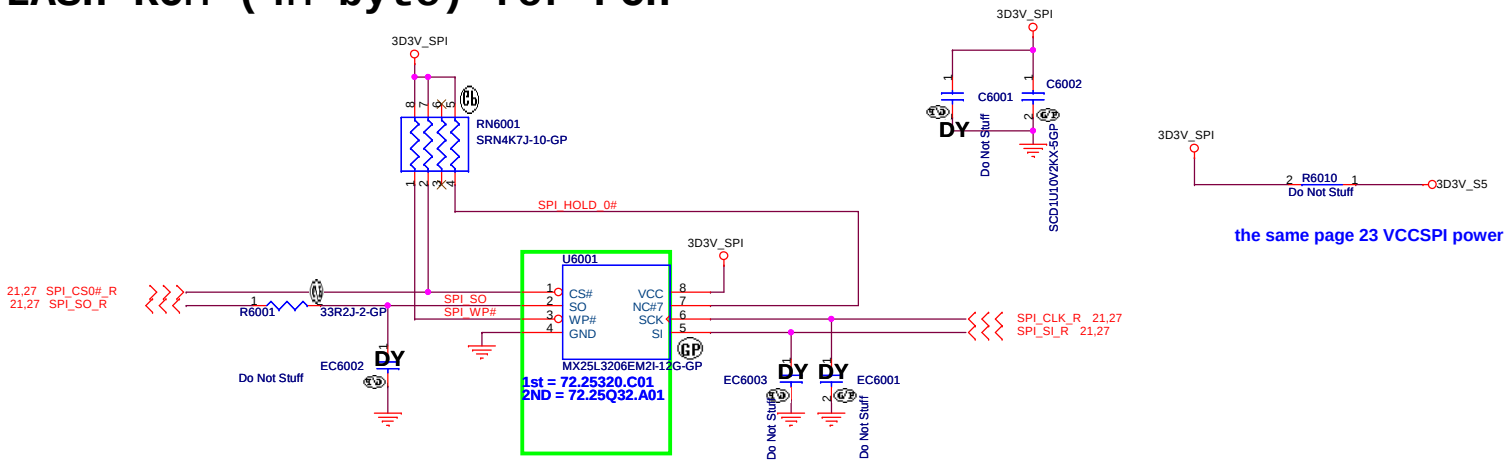


55.4KZ01.S18G S19G

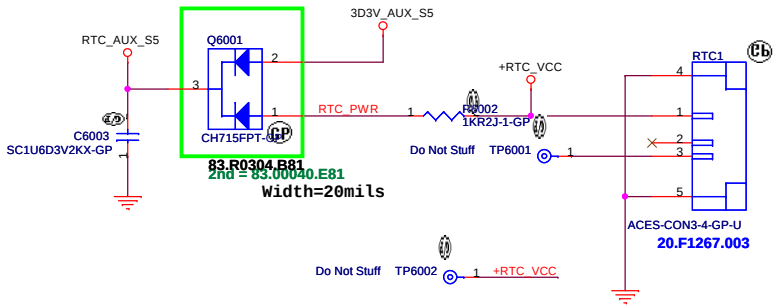
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RJ45 / Transformer*		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



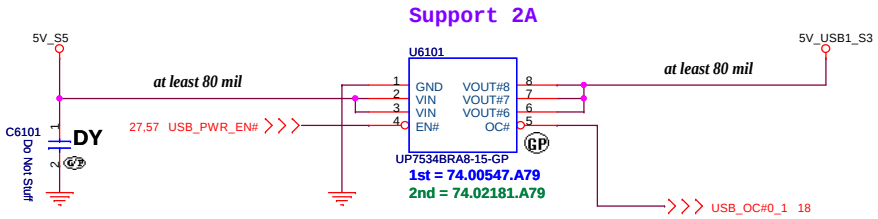
55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

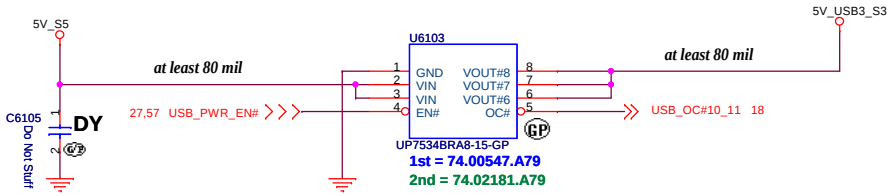
Title	***Flash/RTC***	
Size A3	Document Number **LA470**	Rev **-1**
Date: Thursday, November 04, 2010	Sheet 60 of 103	

SSID = USB

IO Board USB Power



Sub-USB Board Power



55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 61 of 103

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Port***

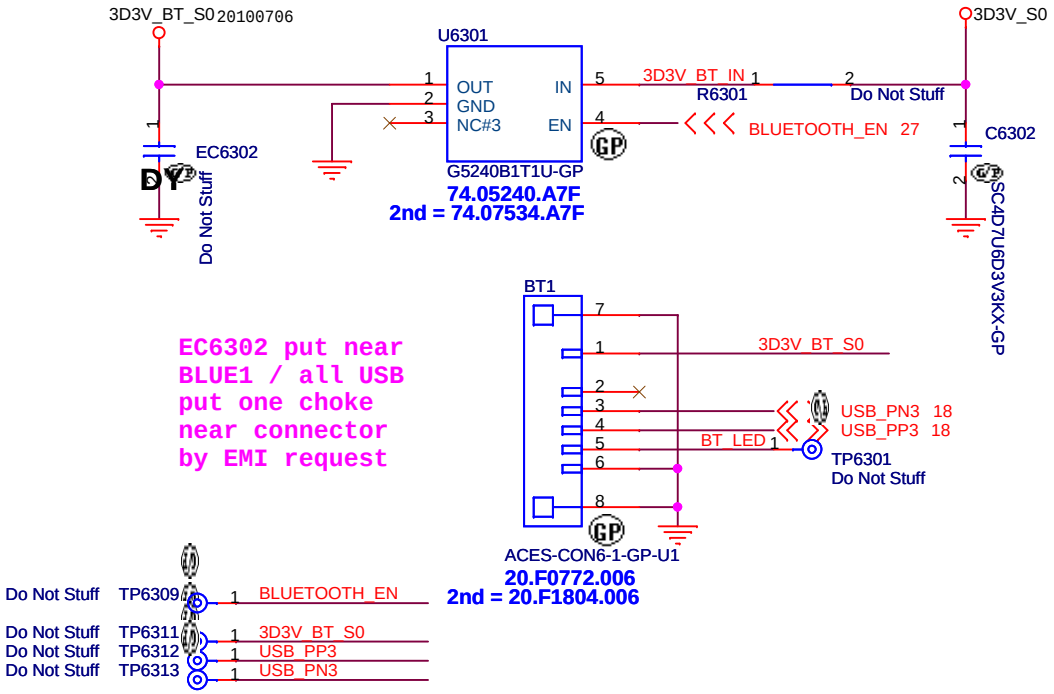
Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

Bluetooth Module

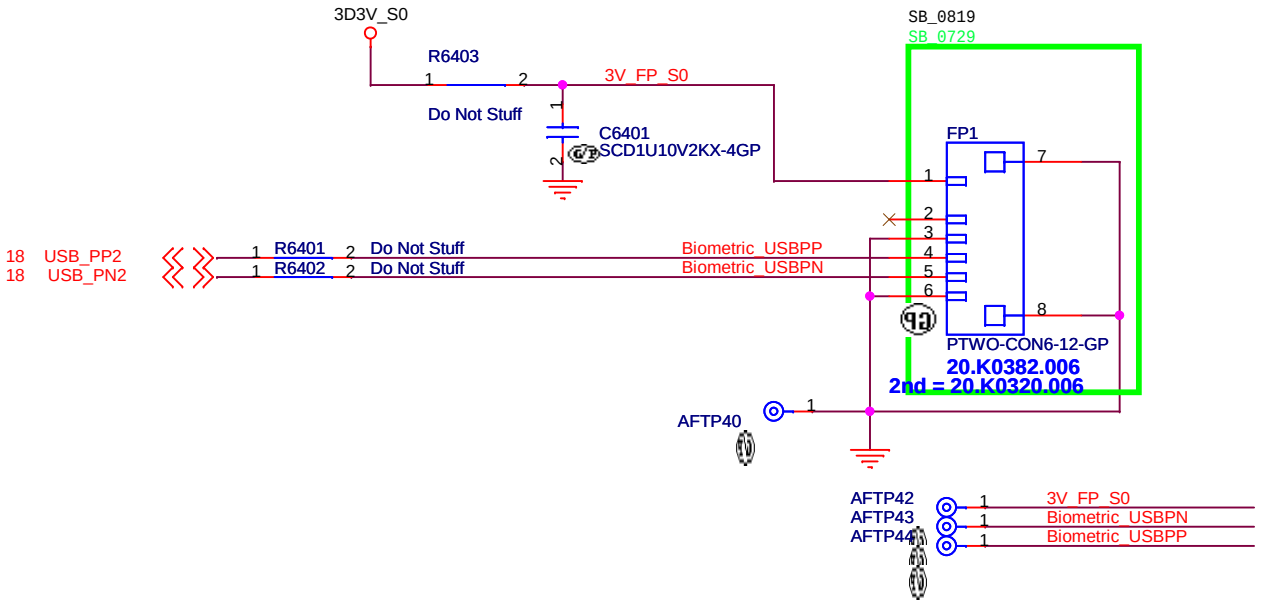


55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***		
Size: A4	Document Number: **LA470**	Rev: **-1**
Date: Thursday, November 04, 2010	Sheet 63 of 103	

Finger Printer Connector

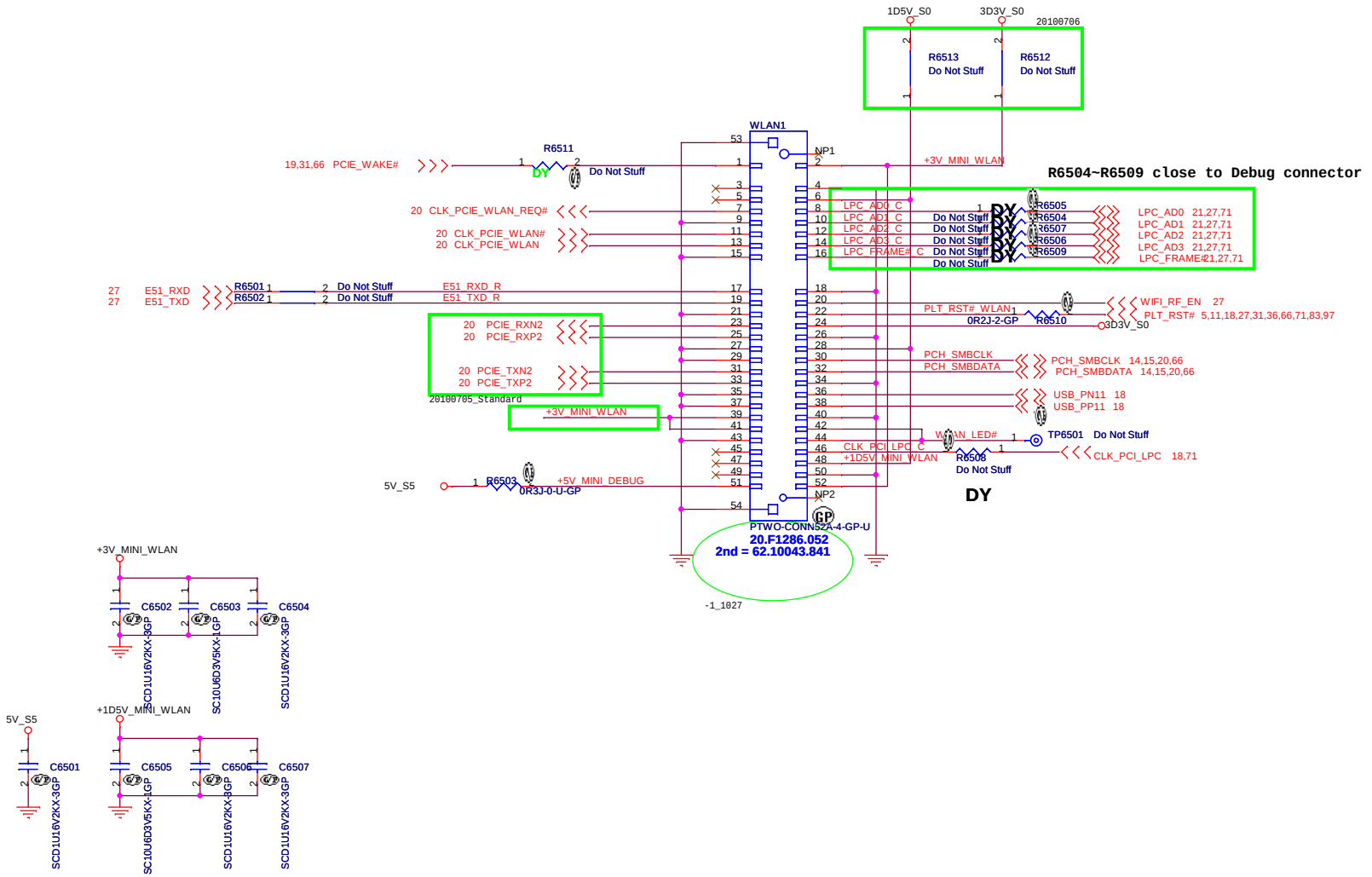


55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LA470**	Rev: **-1**
Date: Thursday, November 04, 2010	Sheet 64 of 103	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

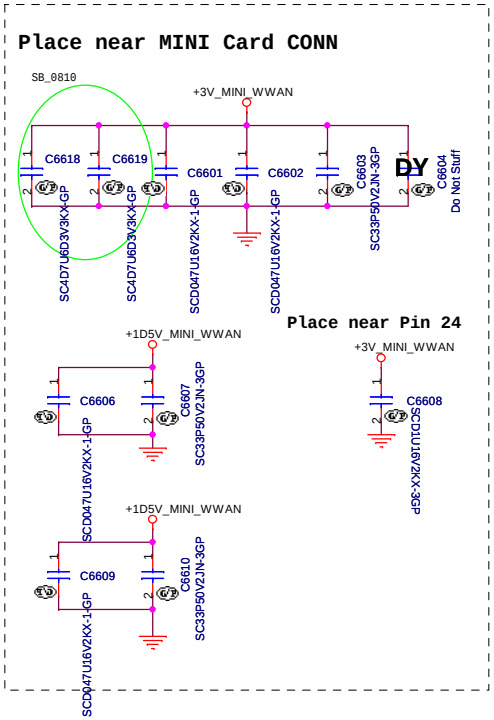
Title: MINICARD(WLAN)/ITP CONN

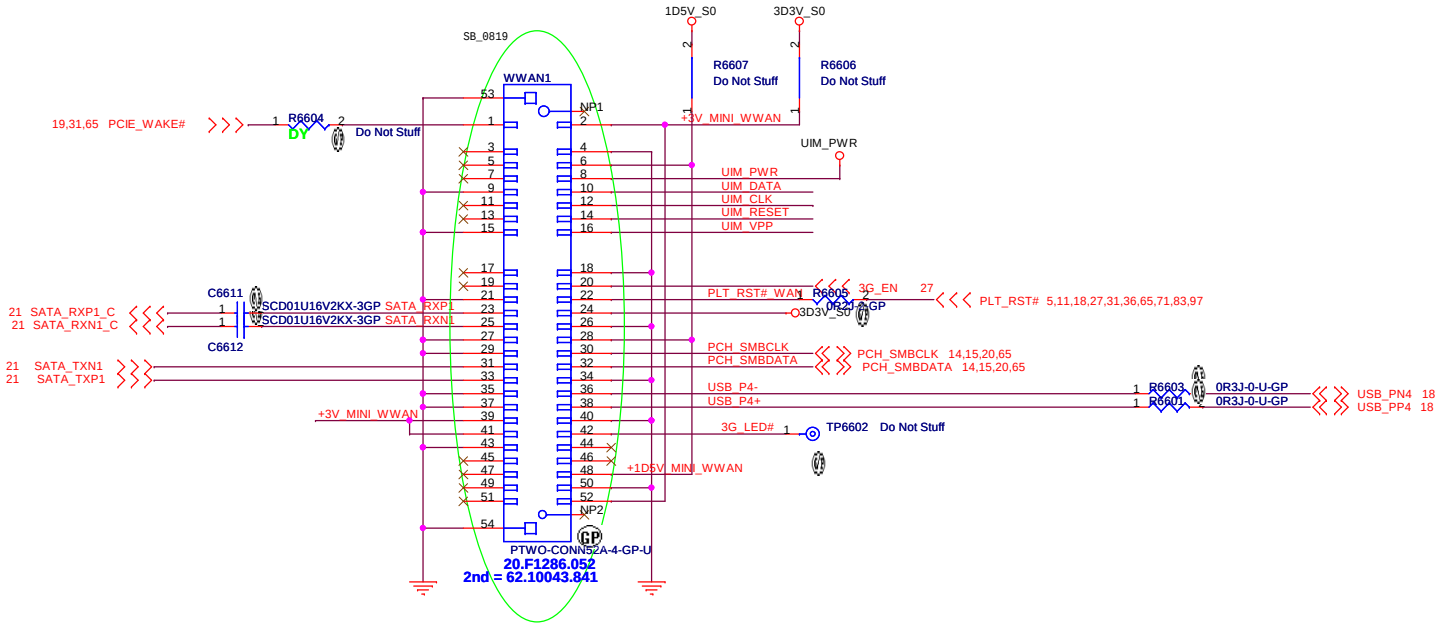
Size	Document Number	Rev
A3	LA470	-1

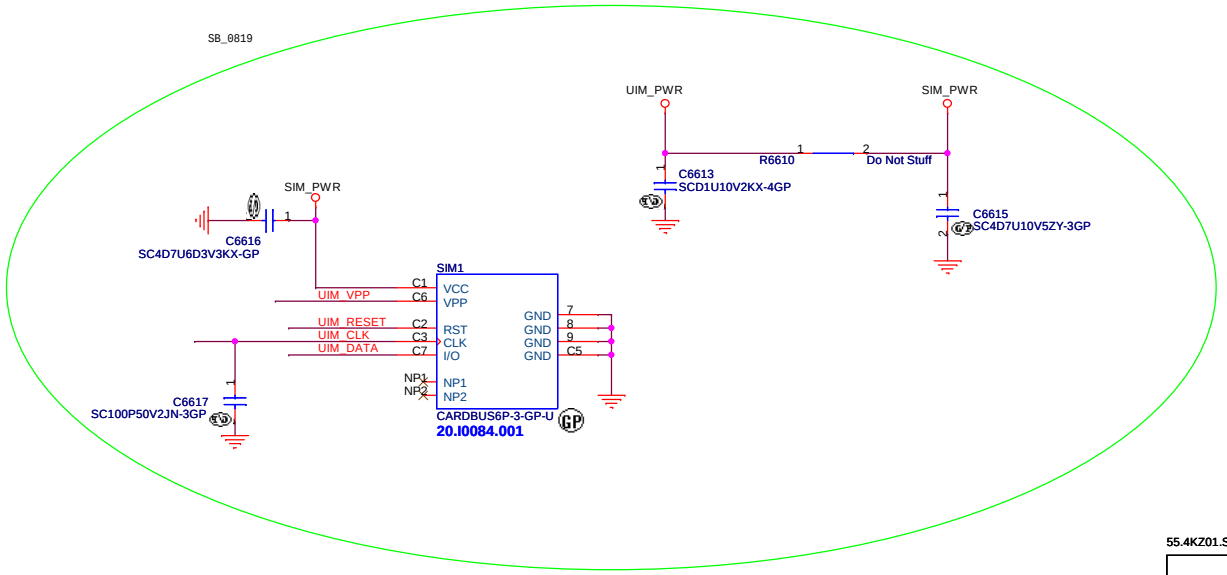
Date: Thursday, November 04, 2010 Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)







55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***WWAN Connector***	
Size A3	Document Number **LA470**	Rev **-1**
Date: Thursday, November 04, 2010	Sheet 66 of 103	

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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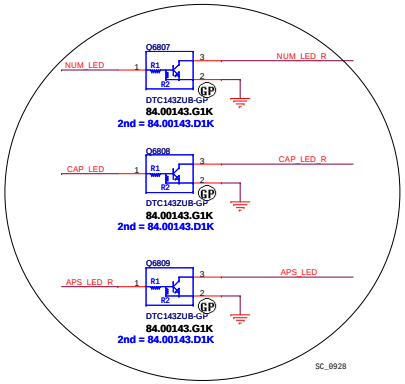
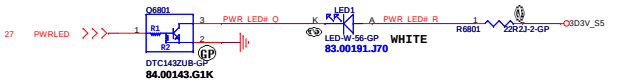
Date: Thursday, November 04, 2010 Sheet 67 of 103

SSID = User.Interface

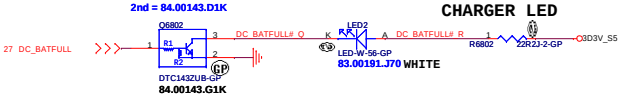
Power button LED



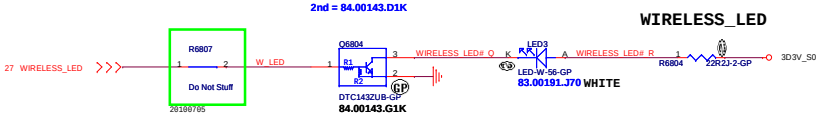
POWER LED



CHARGER LED

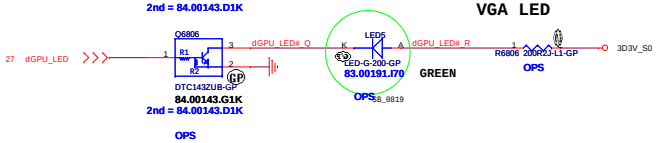


WIRELESS_LED

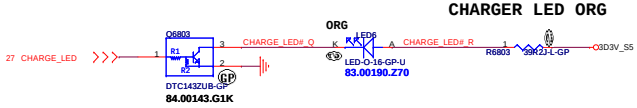


TP LED

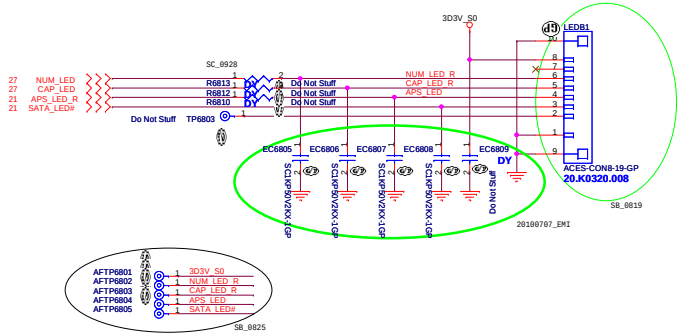
VGA LED

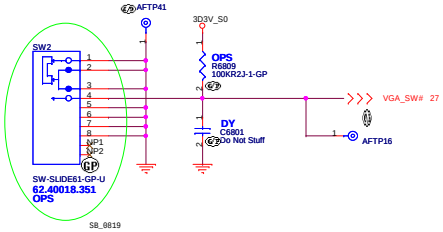


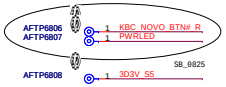
CHARGER LED ORG



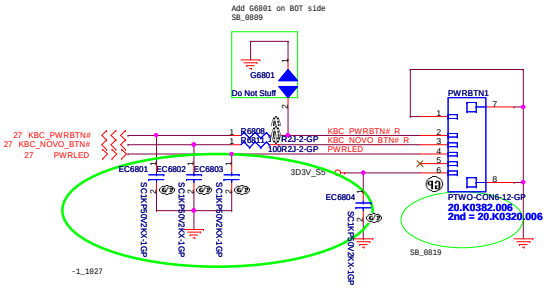
LED Bord CONN.







Power button LED(White)



55.4KZ01.S18G S19G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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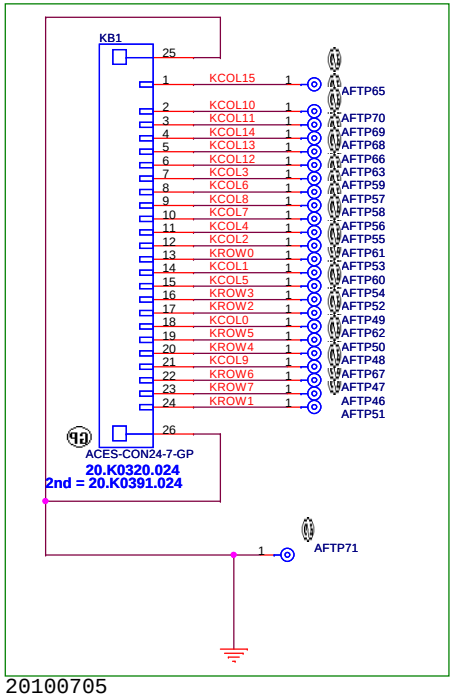
SSID = KBC

Internal KeyBoard Connector

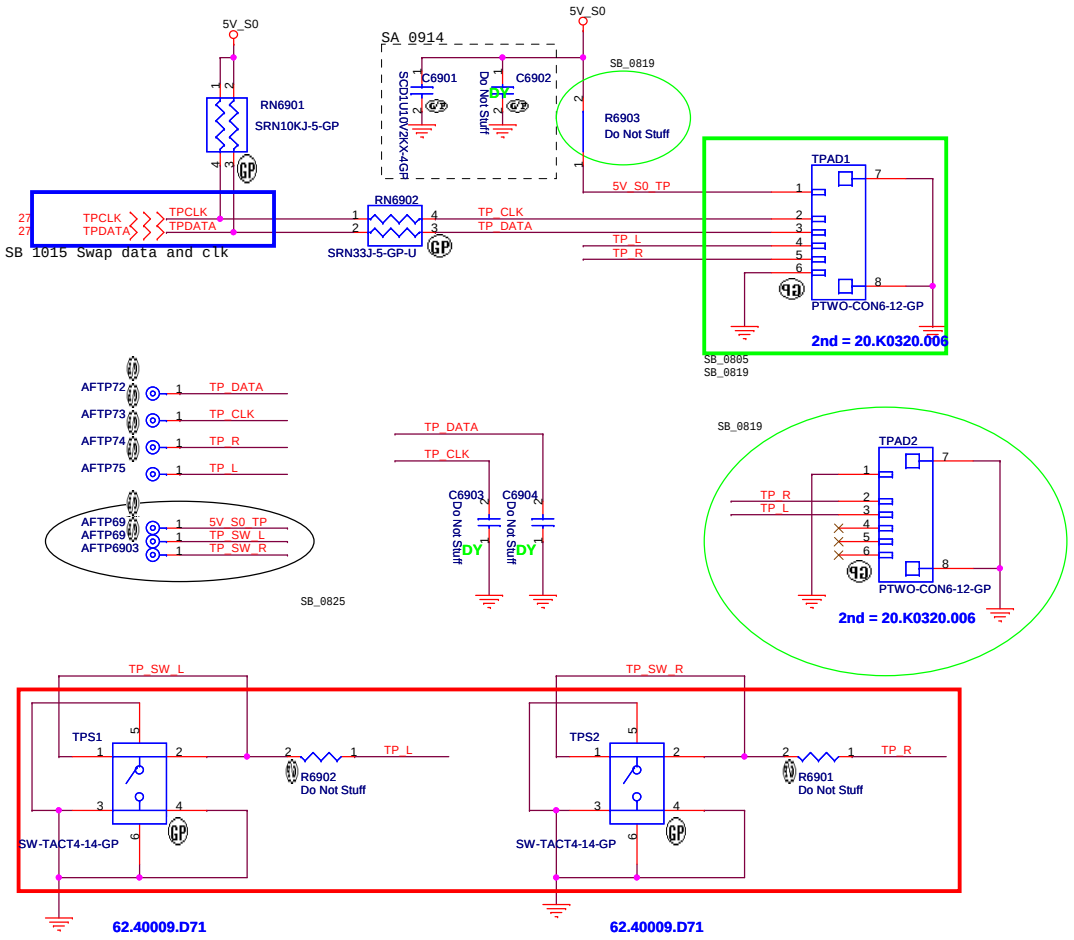


20100705

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



55.4KZ01.S18G S19G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Key Board/Touch Pad	
Size A3	Document Number LA470	Rev -1
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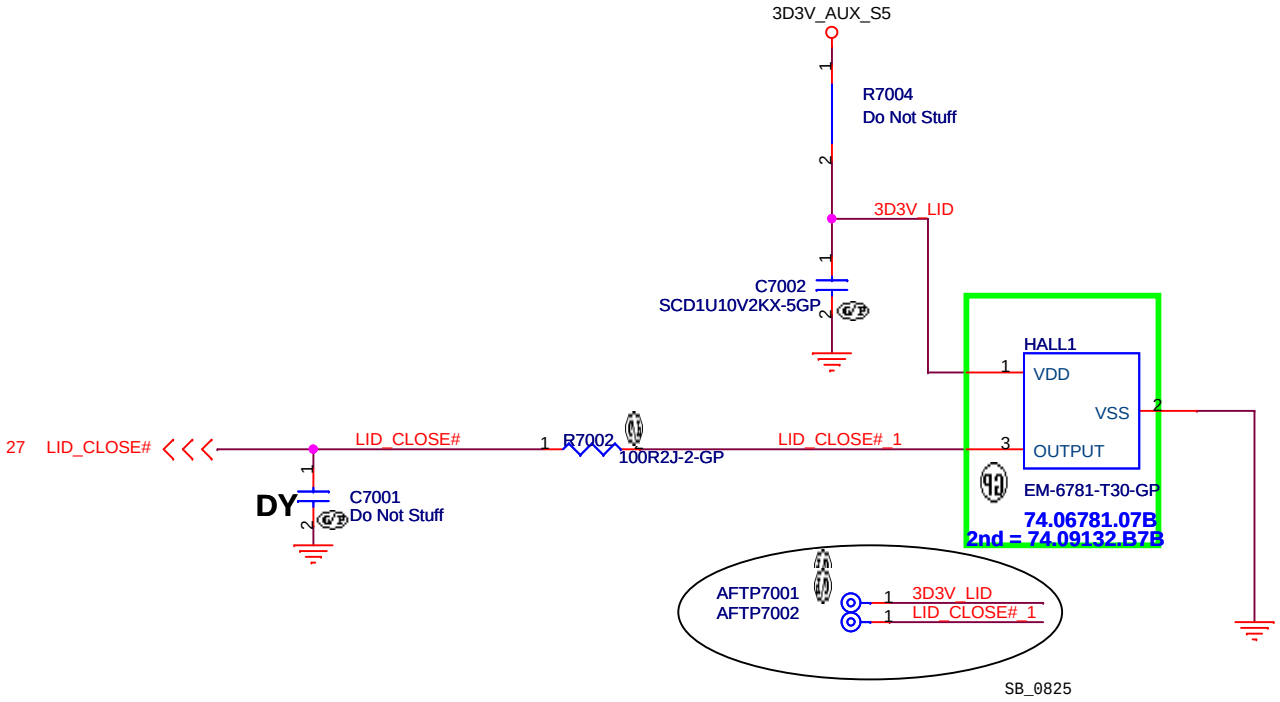

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
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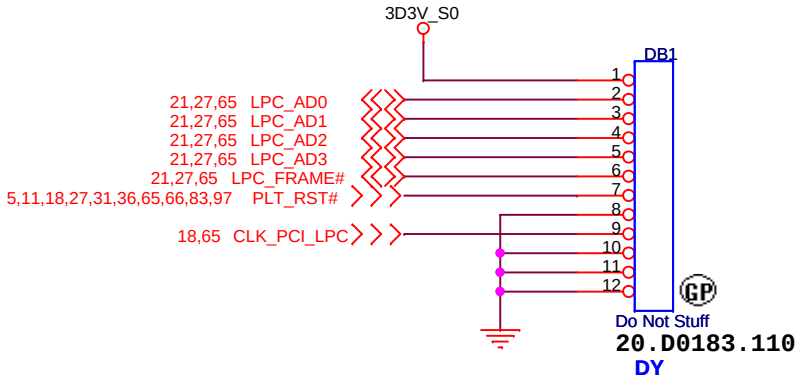
Date: Thursday, November 04, 2010 Sheet 70 of 103



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

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Date: Thursday, November 04, 2010 Sheet 71 of 103

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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Date: Thursday, November 04, 2010 Sheet 72 of 103

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A3	Document Number: **LA470**	Rev: **-1**
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, November 04, 2010 Sheet 75 of 103

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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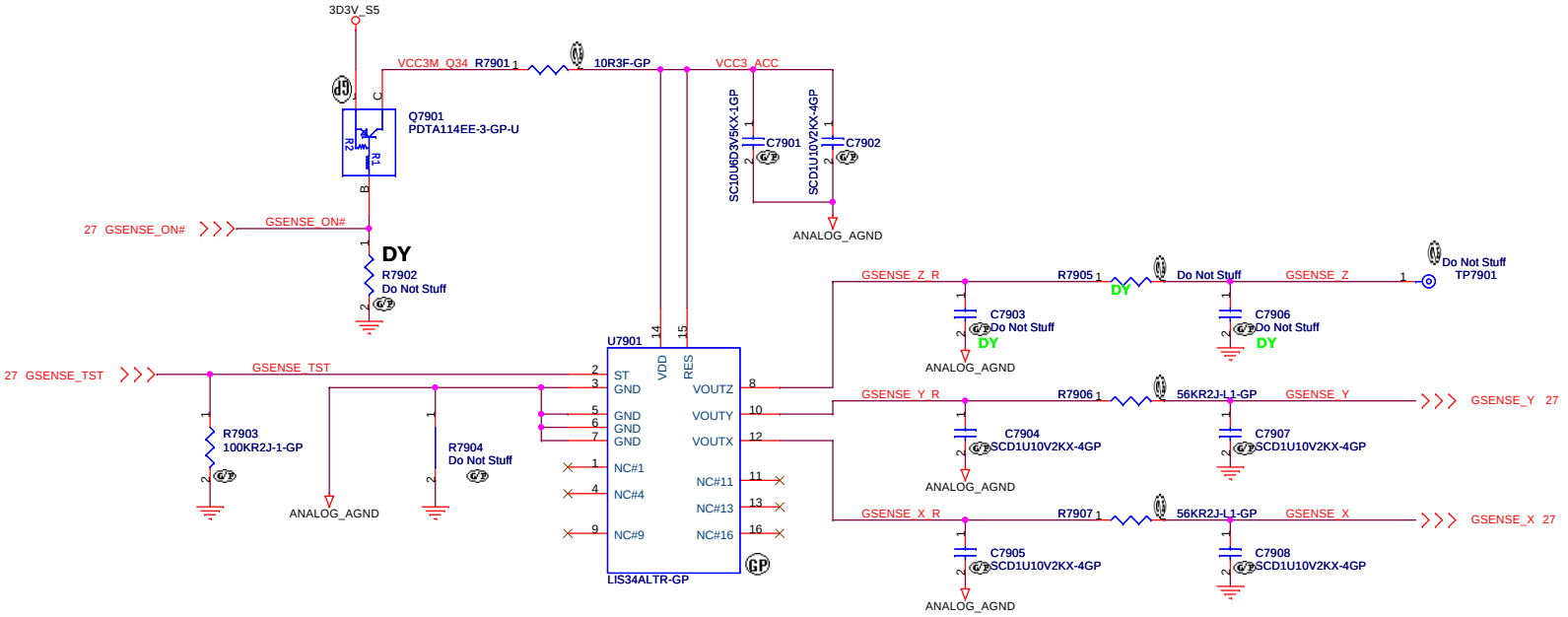
G-Sensor



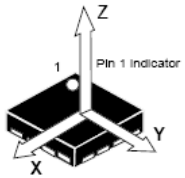
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***G-Sensor***	
Size: Custom	Document Number: **LA470**	Rev: **-1**
Date: Thursday, November 04, 2010	Sheet 79 of 103	

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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Date: Thursday, November 04, 2010 Sheet 80 of 103

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55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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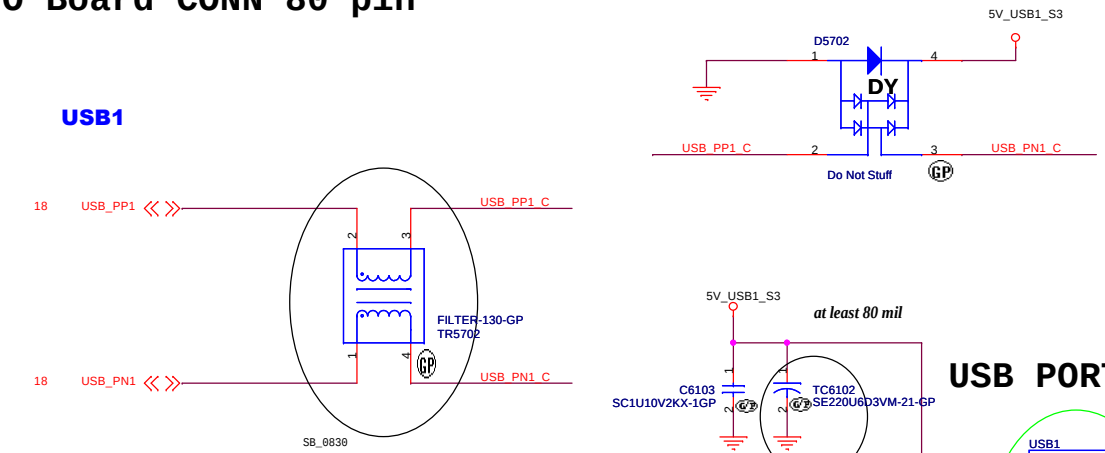
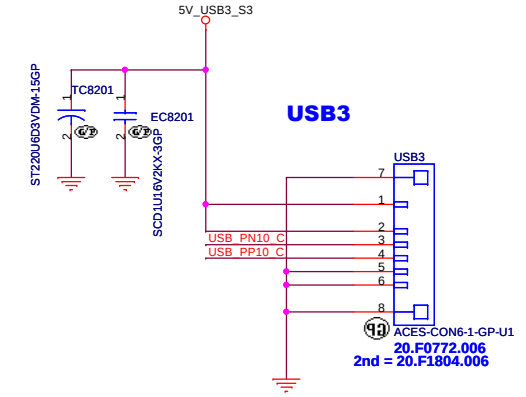
IO Board CONN 80 pin

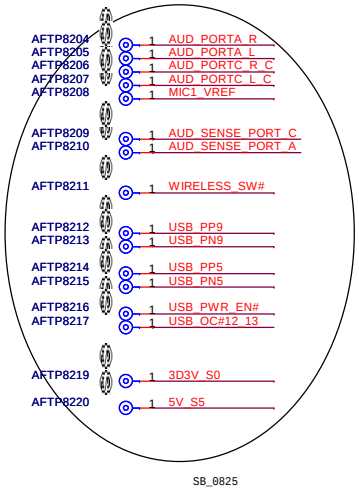


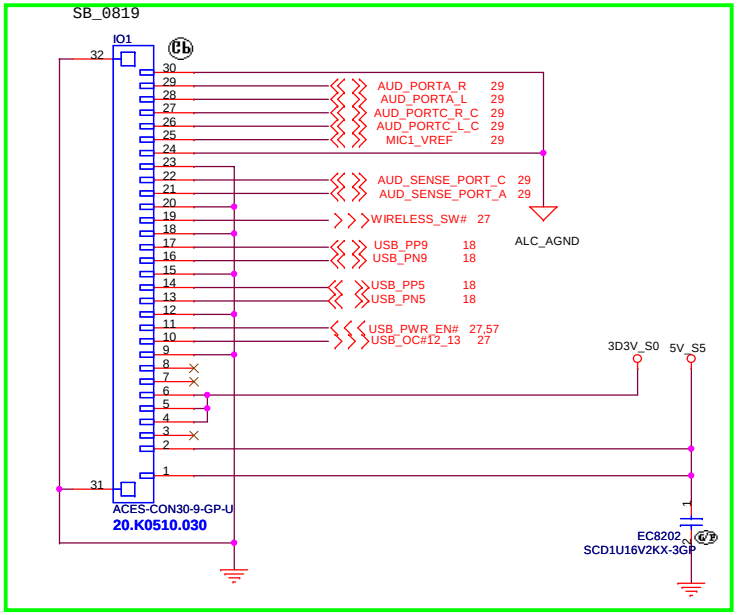
Mars:
Exchange ODD and ESATA differential pair each other.

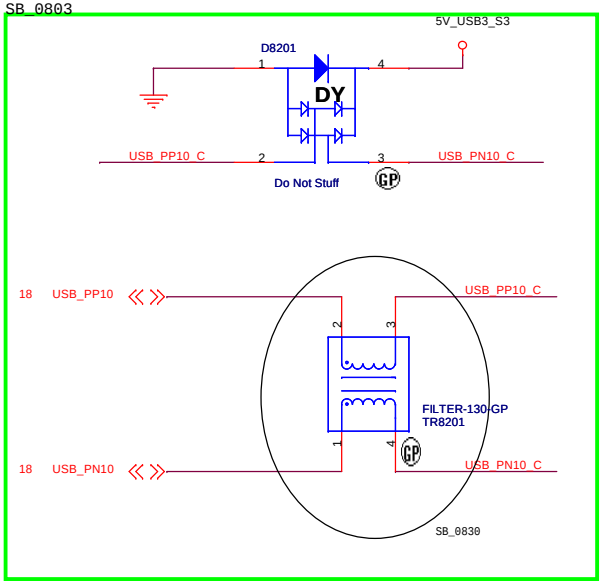
USB Board CONN.

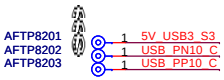


I/O Board CONN.



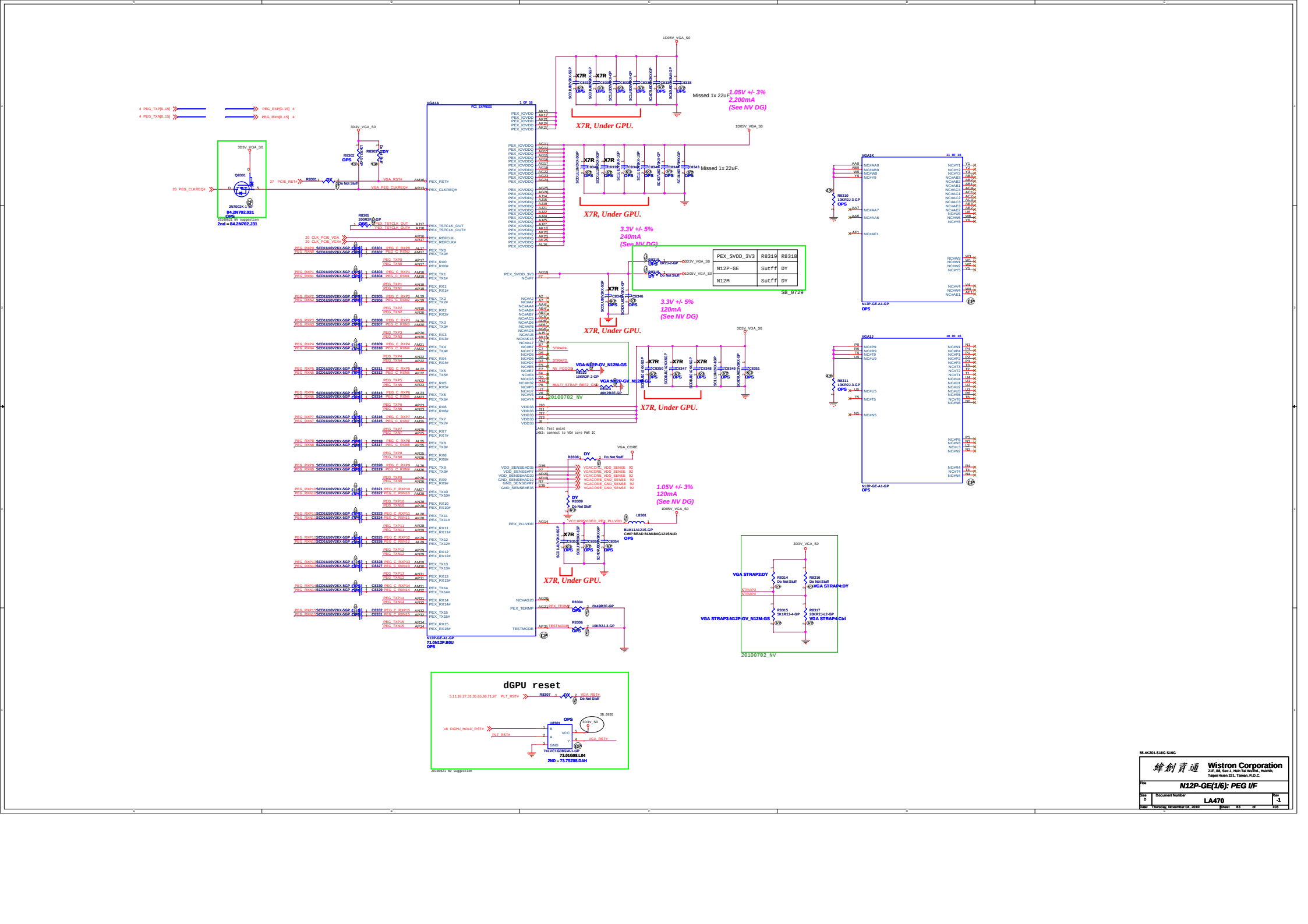




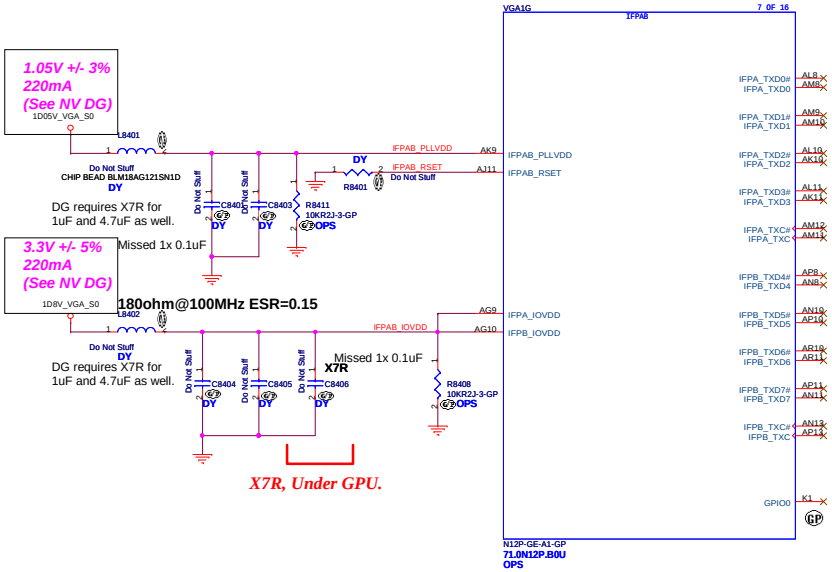


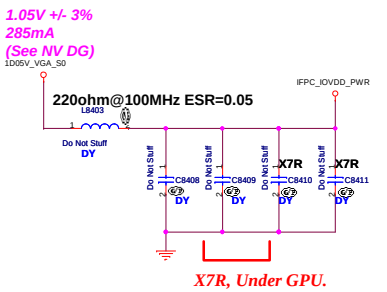
55.4KZ01.S18G S19G

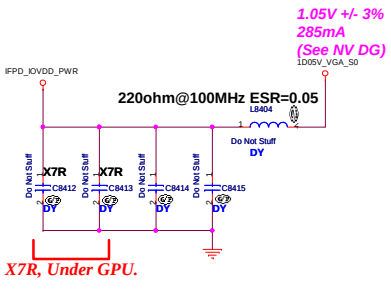
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: IO Board Connector		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 82 of 103	

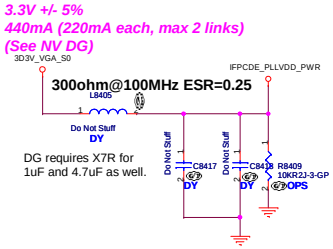

VGA1A
PCI_EXPRESS
1 OF 16
N12P-GE-A1-GP
71.0N12P.B0U
OPS
VGA1K
11 OF 16
VGA1J
10 OF 16
N12P-GE-A1-GP
OPS
1D05V_VGA_S0
3D3V_VGA_S0
VGA_CORE
X7R, Under GPU.
Missed 1x 22uF.
1.05V +/- 3%
2,200mA
(See NV DG)
3.3V +/- 5%
240mA
(See NV DG)
3.3V +/- 5%
120mA
(See NV DG)
1.05V +/- 3%
120mA
(See NV DG)
PEX_SVDD_3V3 | R8319 | R8318
N12P-GE | Stuff | DY
N12M | Stuff | DY
SB_8729
20100702_NV
dGPU reset
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
SB_8826
20100621 NV suggestion
55.4K201.S18G S19G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
N12P-GE(1/6): PEG I/F
LA470
Rev -1
Date: Thursday, November 04, 2010
Sheet 03 of 103

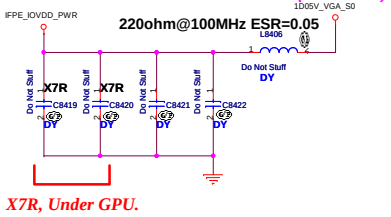
LVDS Interface

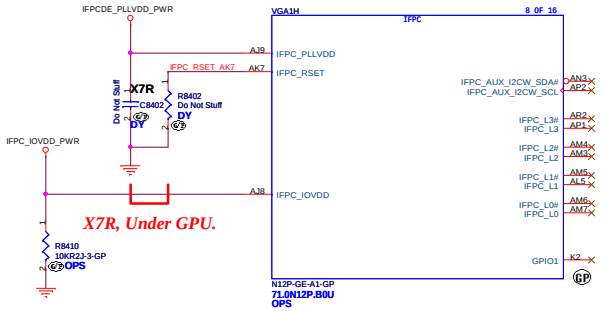




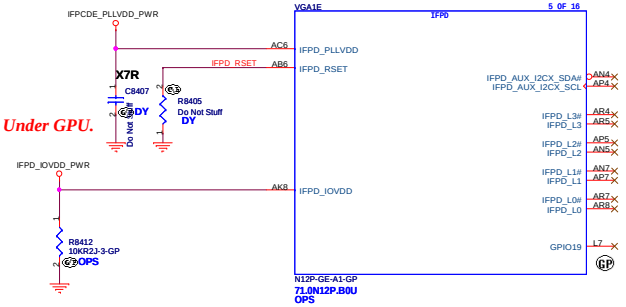


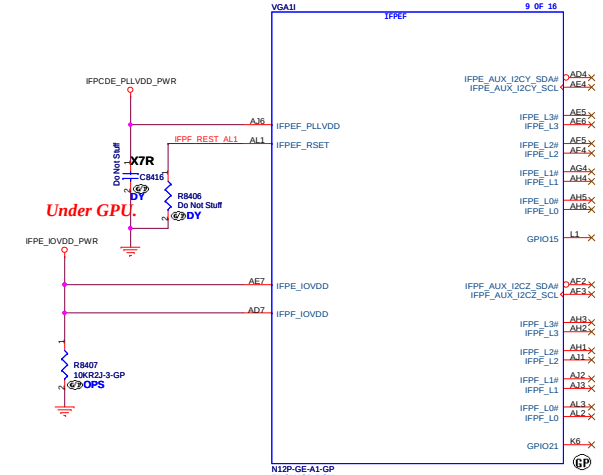






HDMI Interface





55.4KZ01.S18G S19G

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Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

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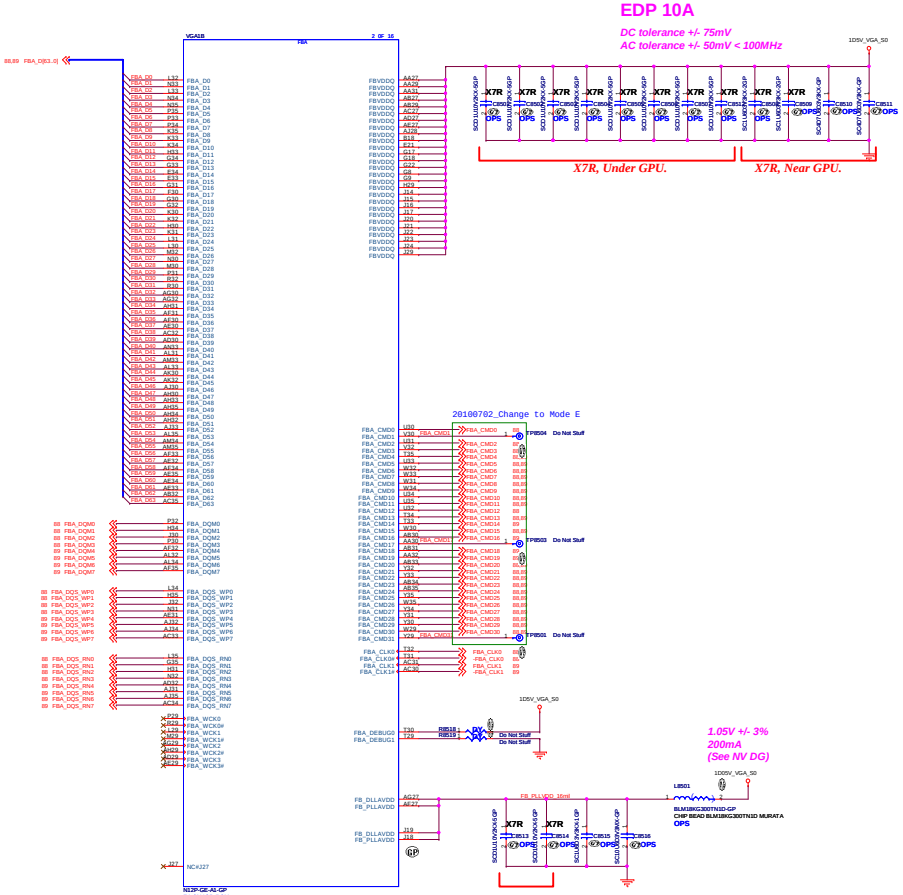
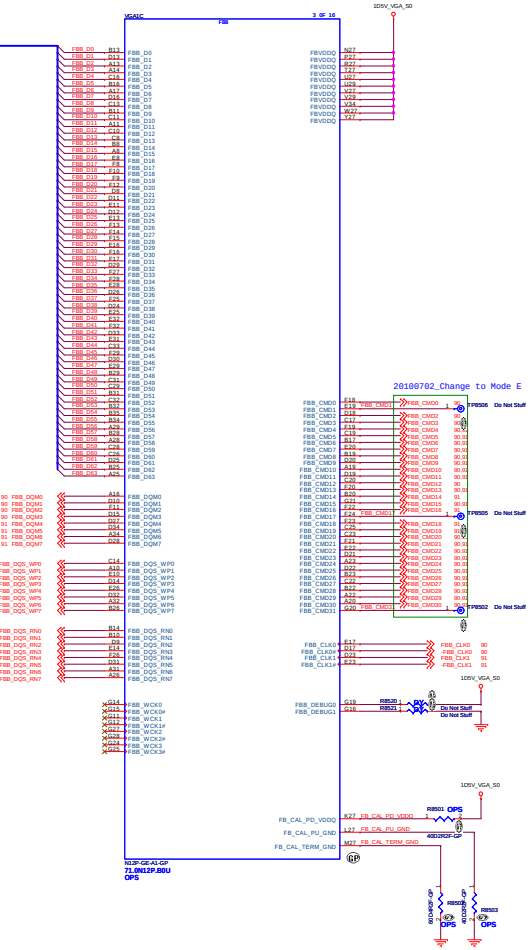
Date: Thursday, November 04, 2010 Sheet 84 of 103

EDP 10A

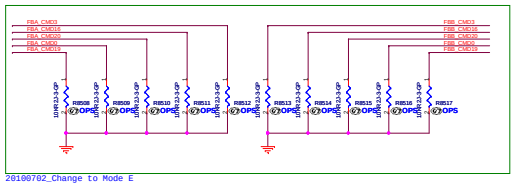
DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz





FBCLK Termination place on VRAM side

FBCLK Termination	R8504~R8507
N12P	Stuff 162 ohm 64.16205.6DL
N12M	Stuff 243 ohm 64.24305.6DL



FBCLK Termination place on VRAM side

S5.4K201.S18G S19G

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *N12P-Q1/Q3 (3/6): VRAM I/F*

Size	Document Number	Rev
A1	LA470	-1

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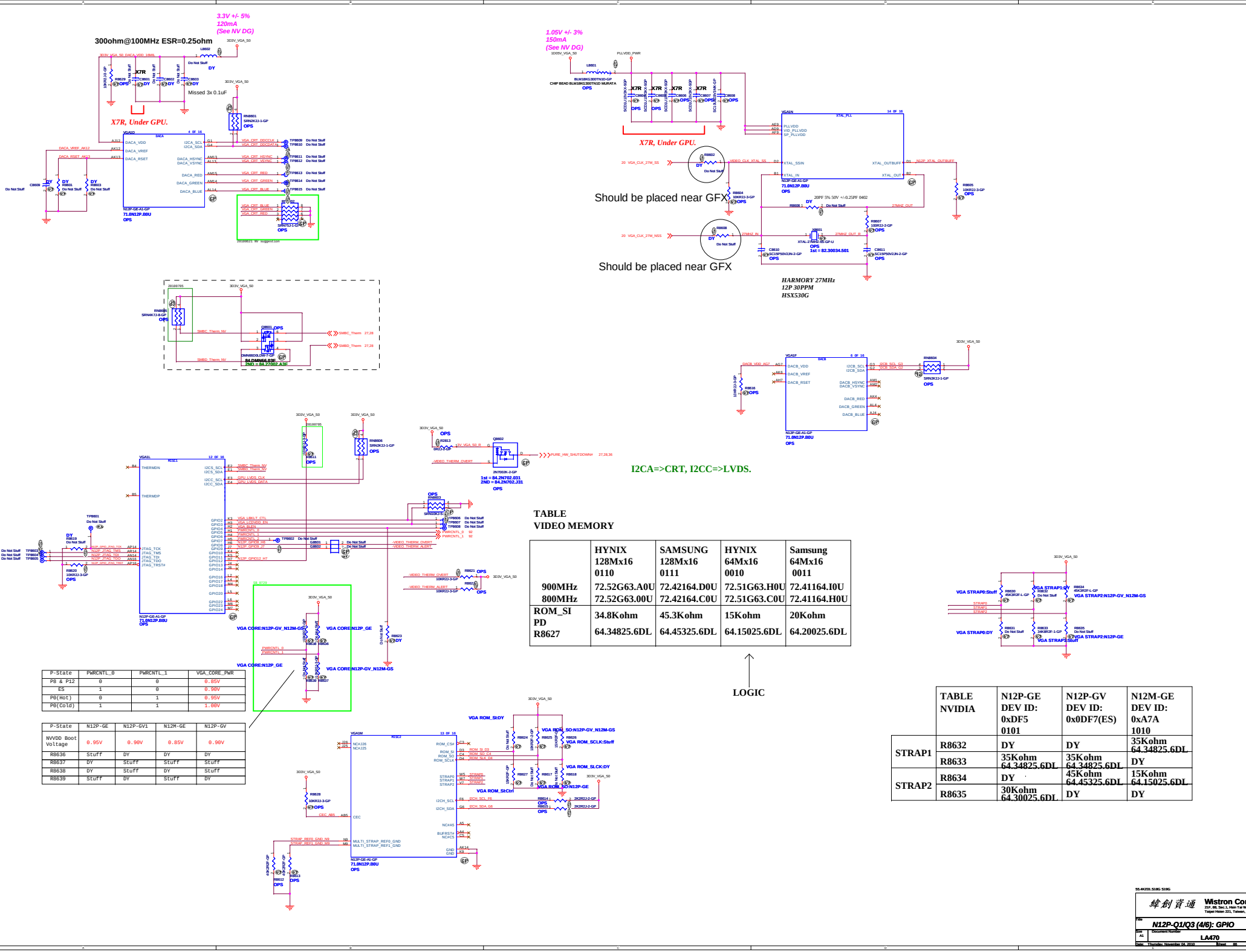

TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
900MHz	72.52G63.A0U	72.42164.D0U	72.51G63.H0U	72.41164.I0U
800MHz	72.52G63.00U	72.42164.C0U	72.51G63.C0U	72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

P-State	PWRCNTL_0	PWRCNTL_1	VGA_CORE_PWR
P8 & P12	0	0	0.85V
ES	1	0	0.90V
P0(Hot)	0	1	0.95V
P0(Cold)	1	1	1.00V

P-State	N12P-GE	N12P-GV1	N12M-GE	N12P-GV
NVVDD Boot Voltage	0.95V	0.90V	0.85V	0.90V
R8636	Stuff	DY	DY	DY
R8637	DY	Stuff	Stuff	Stuff
R8638	DY	Stuff	DY	Stuff
R8639	Stuff	DY	Stuff	DY

TABLE NVIDIA	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: 0x0DF7(ES)	N12M-GE DEV ID: 0xA7A 1010
STRAP1 R8632	DY	DY	35Kohm 64.34825.6DL
STRAP1 R8633	35Kohm 64.34825.6DL	35Kohm 64.34825.6DL	DY
STRAP2 R8634	DY	45Kohm 64.45325.6DL	15Kohm 64.15025.6DL
STRAP2 R8635	30Kohm 64.30025.6DL	DY	DY

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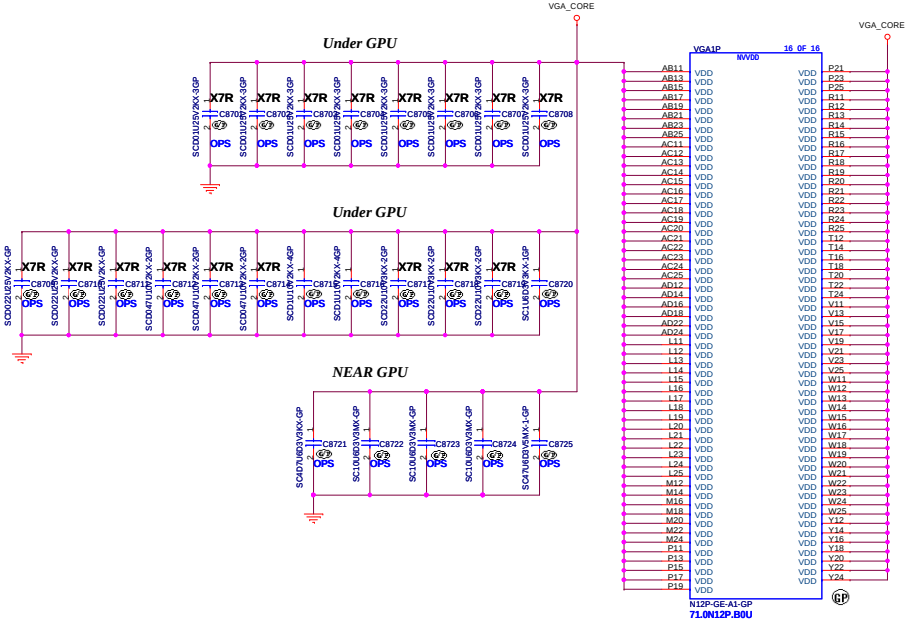
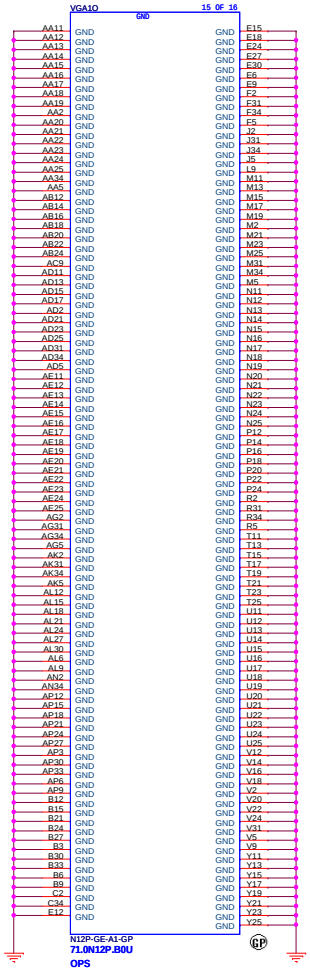
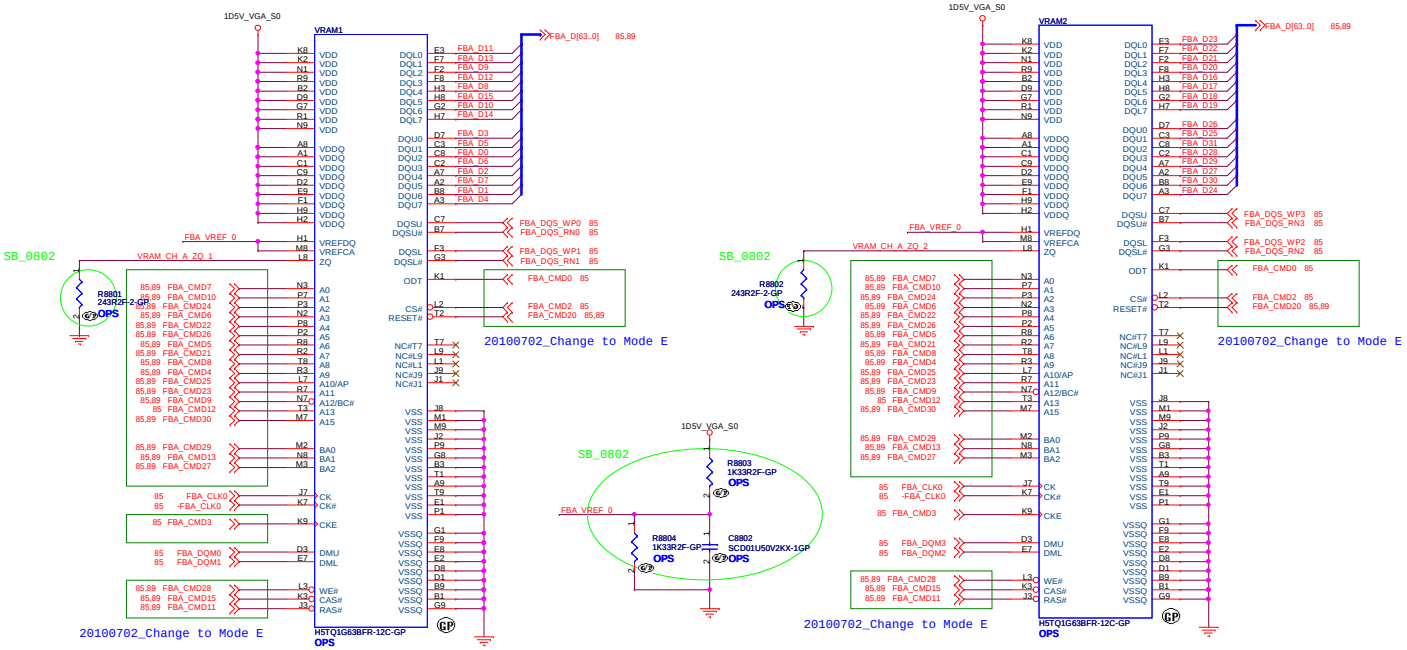
Title: N12P-Q1/Q3 (4/6): GPIO
Size: A1 | Document Number: LA470 | Rev: -1
Date: Thursday, November 04, 2010 | Sheet 86 of 103



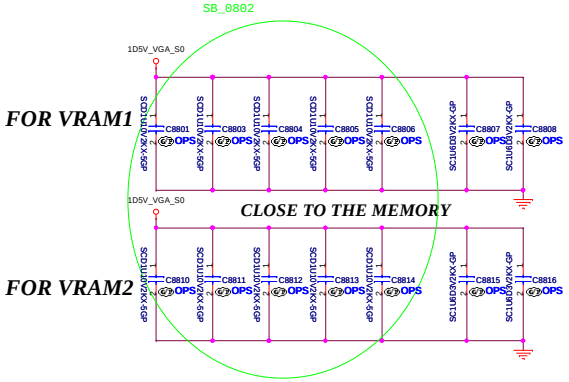


55.4KZ01.S18G S19G

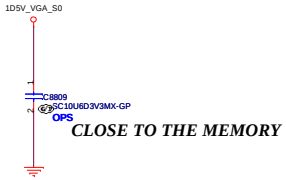
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *N12P-Q1/Q3 (5/6): POWER*		
Size: A2	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 87 of 103	



FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT A

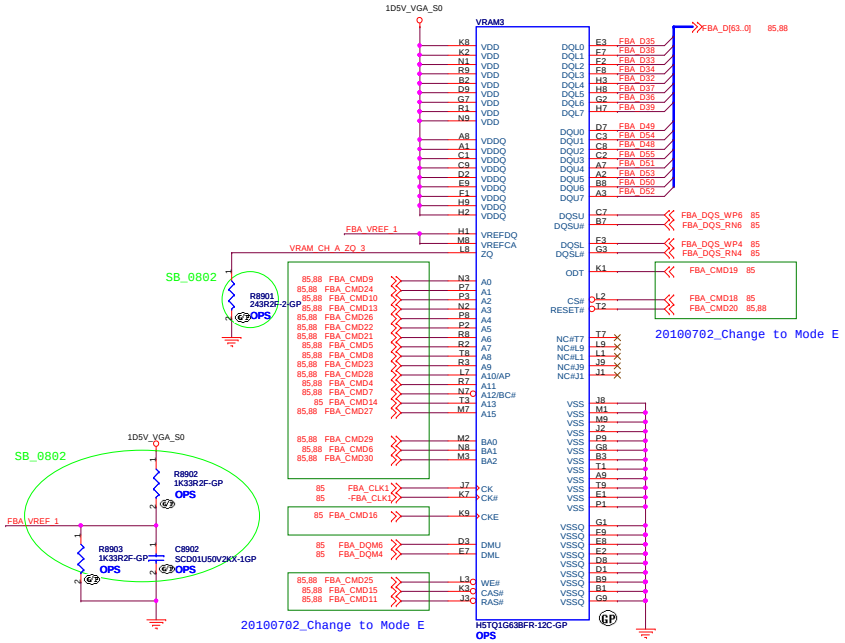
55.4KZ01.S18G S19G

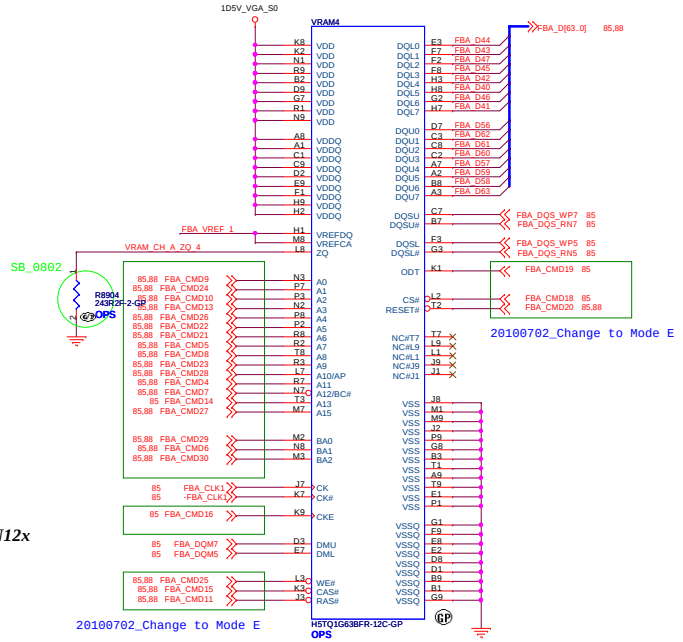
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-A**

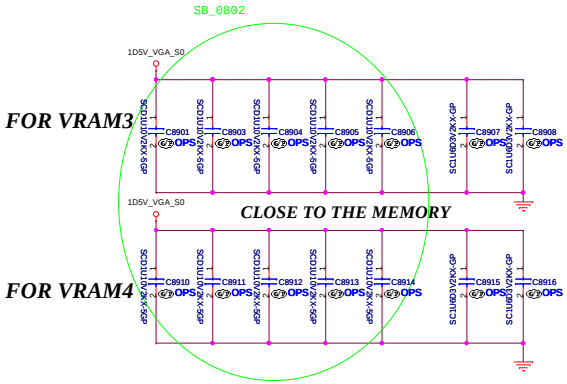
Size	Document Number	Rev
A2	LA470	-1

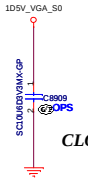
Date: Thursday, November 04, 2010 Sheet 88 of 103





FB CMD mapping Mode D-N12x





CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
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Title: **VRAM CHANNEL-A**

Size	Document Number	Rev
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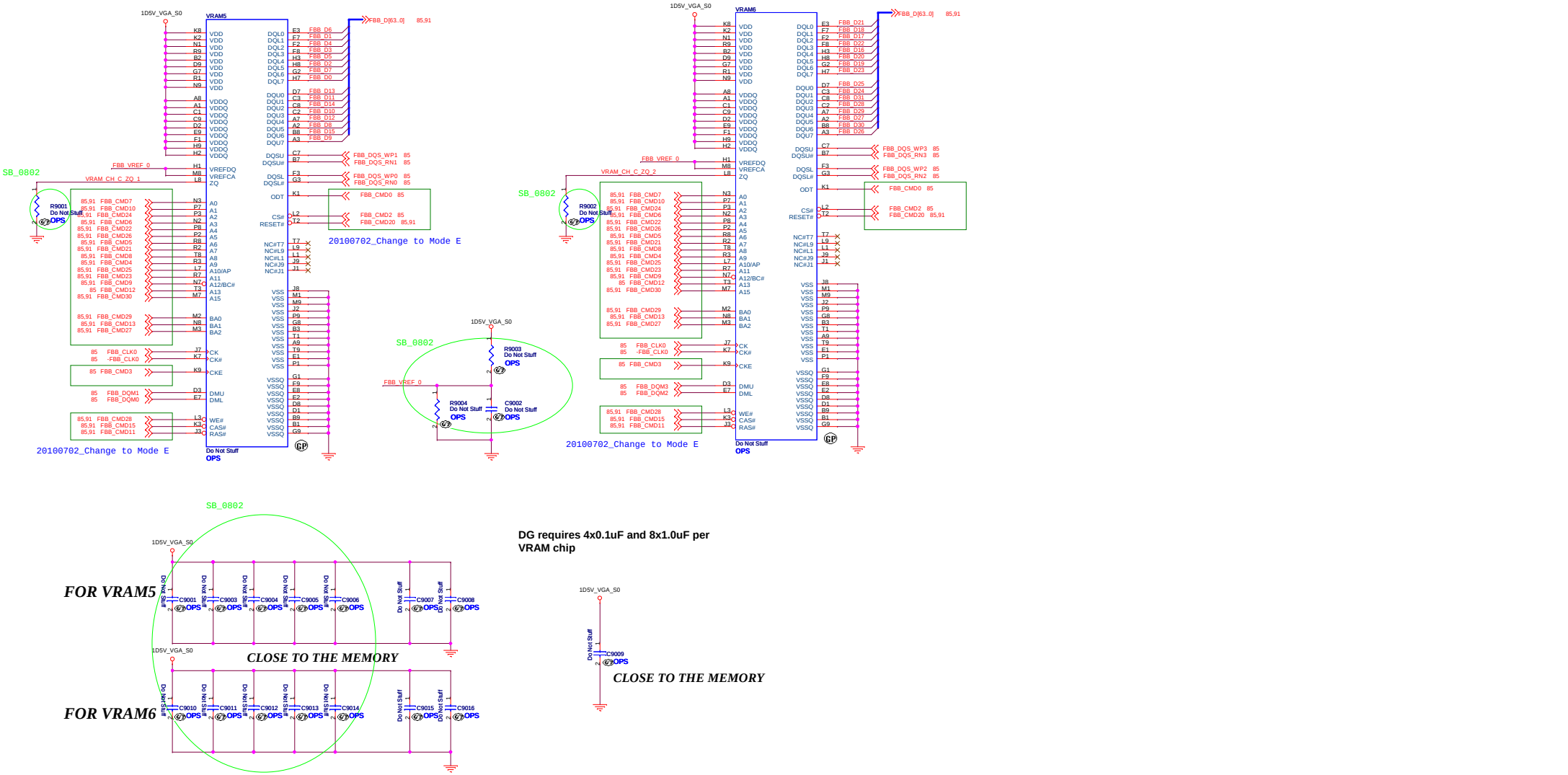
Date: Thursday, November 04, 2010 Sheet 89 of 103



DG requires 4x0.1uF and 8x1.0uF per VRAM chip

CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT C

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
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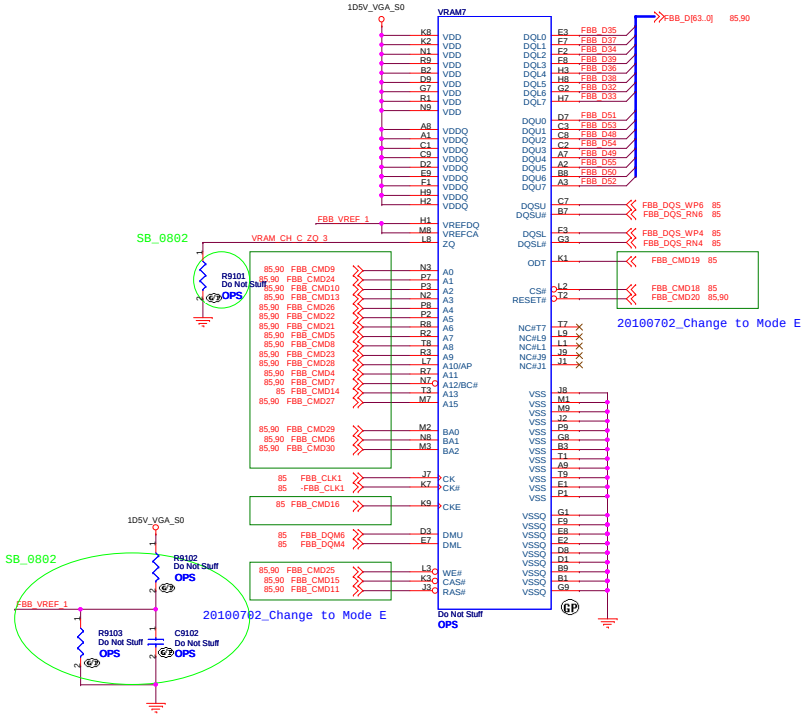
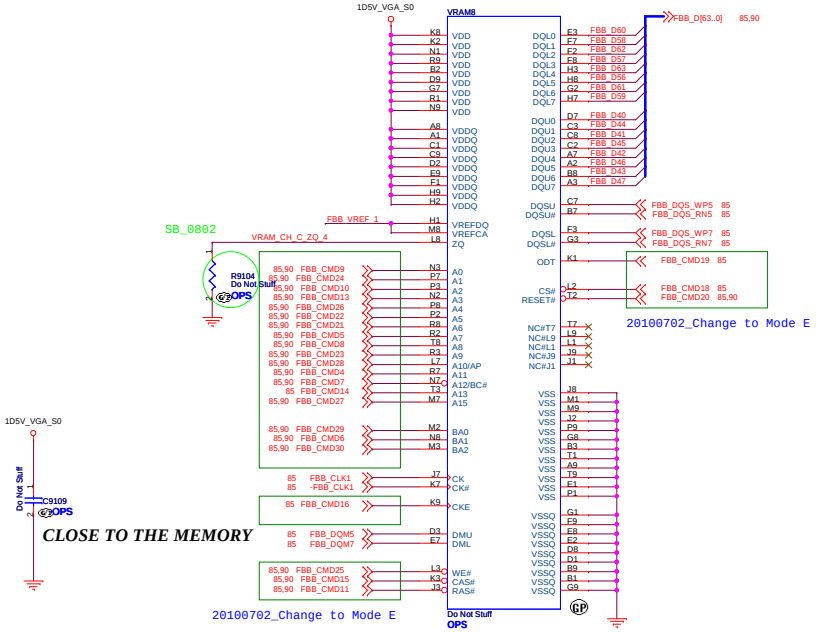
Taipei Hsien 221, Taiwan, R.O.C.

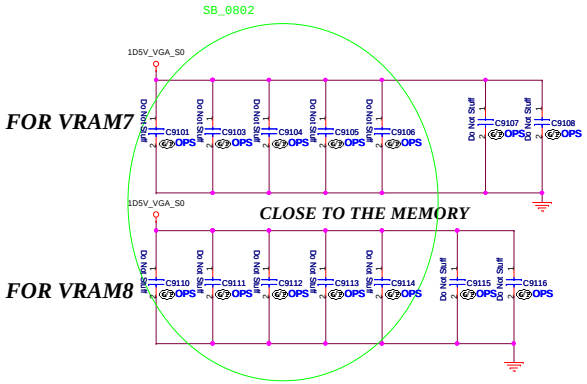
Title: ***VRAM CHANNEL-C***

Size	Document Number	Rev
A2	LA470	-1

Date: Thursday, November 04, 2010 Sheet 90 of 103







VIDEO FRAME BUFFER PORT C

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
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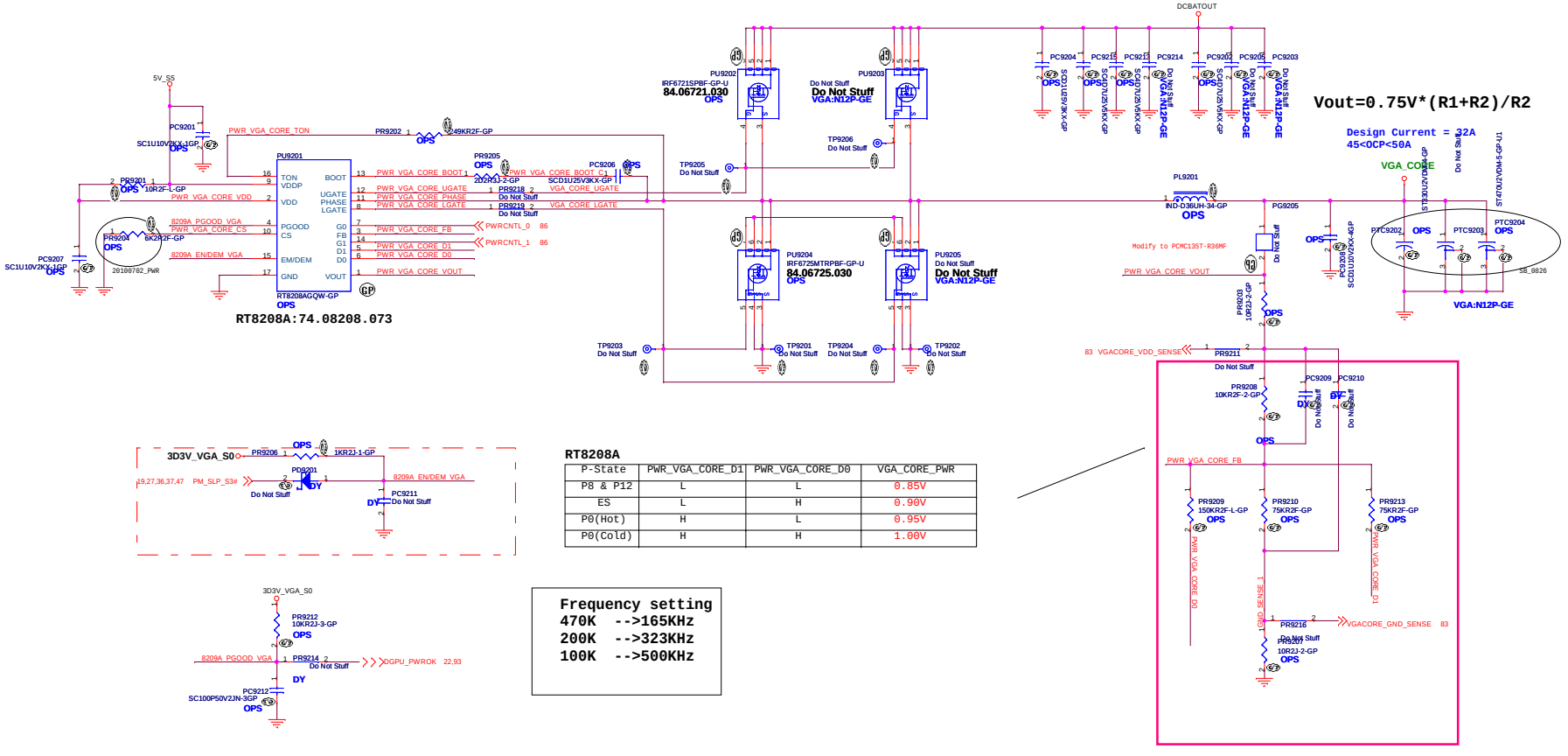
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM CHANNEL-C***

Size	Document Number	Rev
A2	LA470	-1

Date: Thursday, November 04, 2010 Sheet 91 of 103

SSID = PWR.Plane.Regulator_GFX



RT8208A

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 & P12	L	L	0.85V
ES	L	H	0.90V
P0(Hot)	H	L	0.95V
P0(Cold)	H	H	1.00V

55.4KZ01.S18G S19G

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Title: DC/DC_VGA CORE_RT8208A

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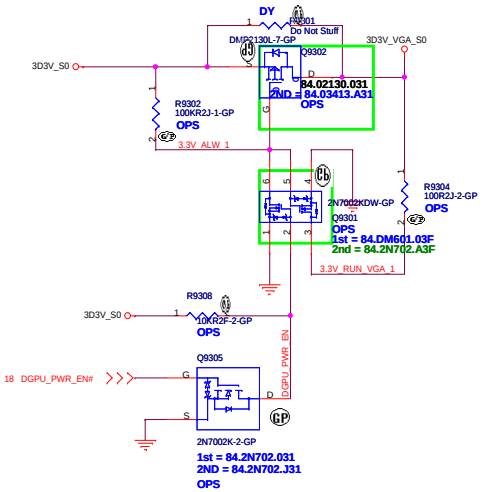
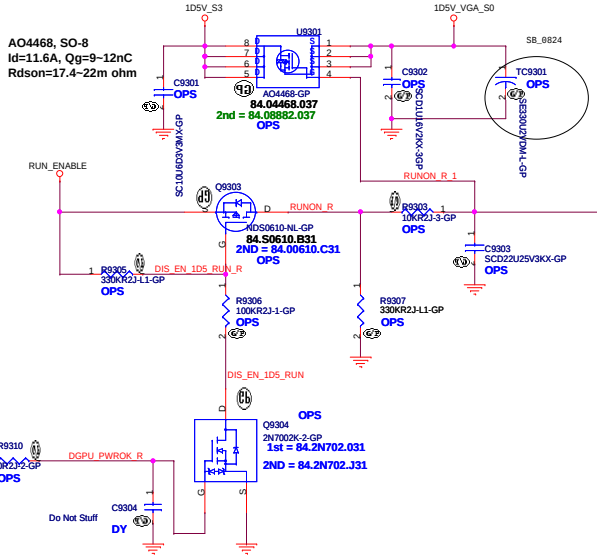
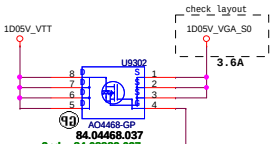
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

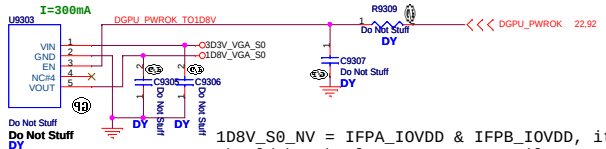


1.05V to 1.05V_VGA_S0 Transfer



20100707

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

55.4KZ01.S18G S19G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size	Document Number LA470	Rev -1
Date: Thursday, November 04, 2010	Sheet 93 of 103	

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55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size: A2 | Document Number: LA470 | Rev: -1

Date: Thursday, November 04, 2010 | Sheet 94 of 103

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT_Switch*		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet 95 of 103	

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, November 04, 2010 Sheet 96 of 103

(Blanking)

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

Size	Document Number	Rev
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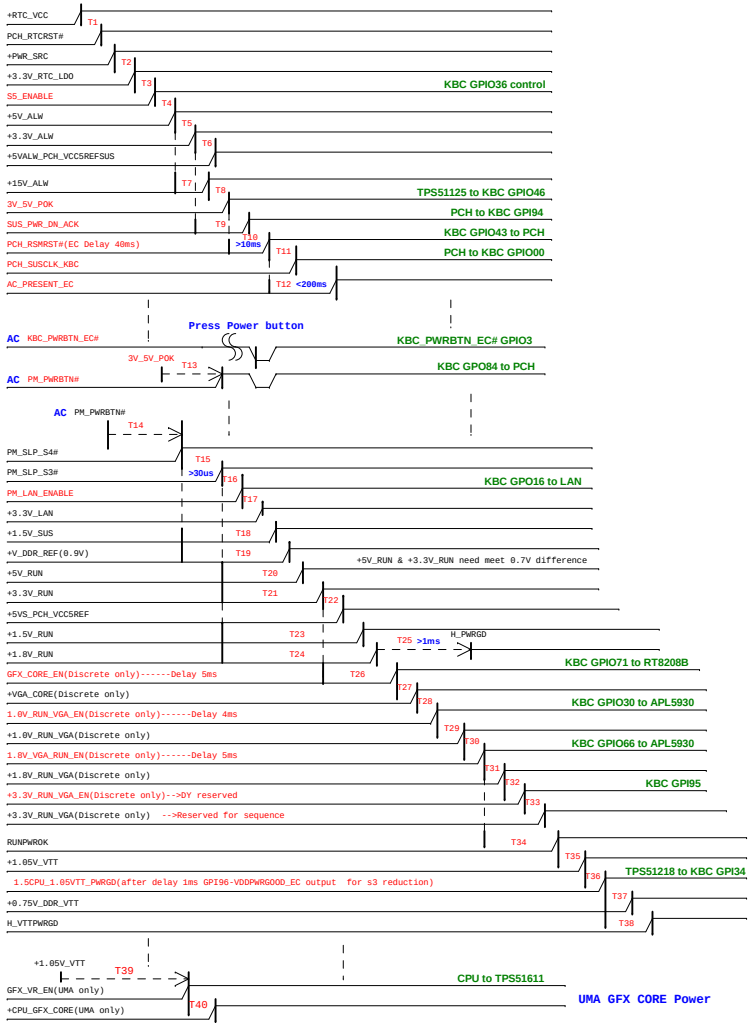
Intel-Power Up Sequence

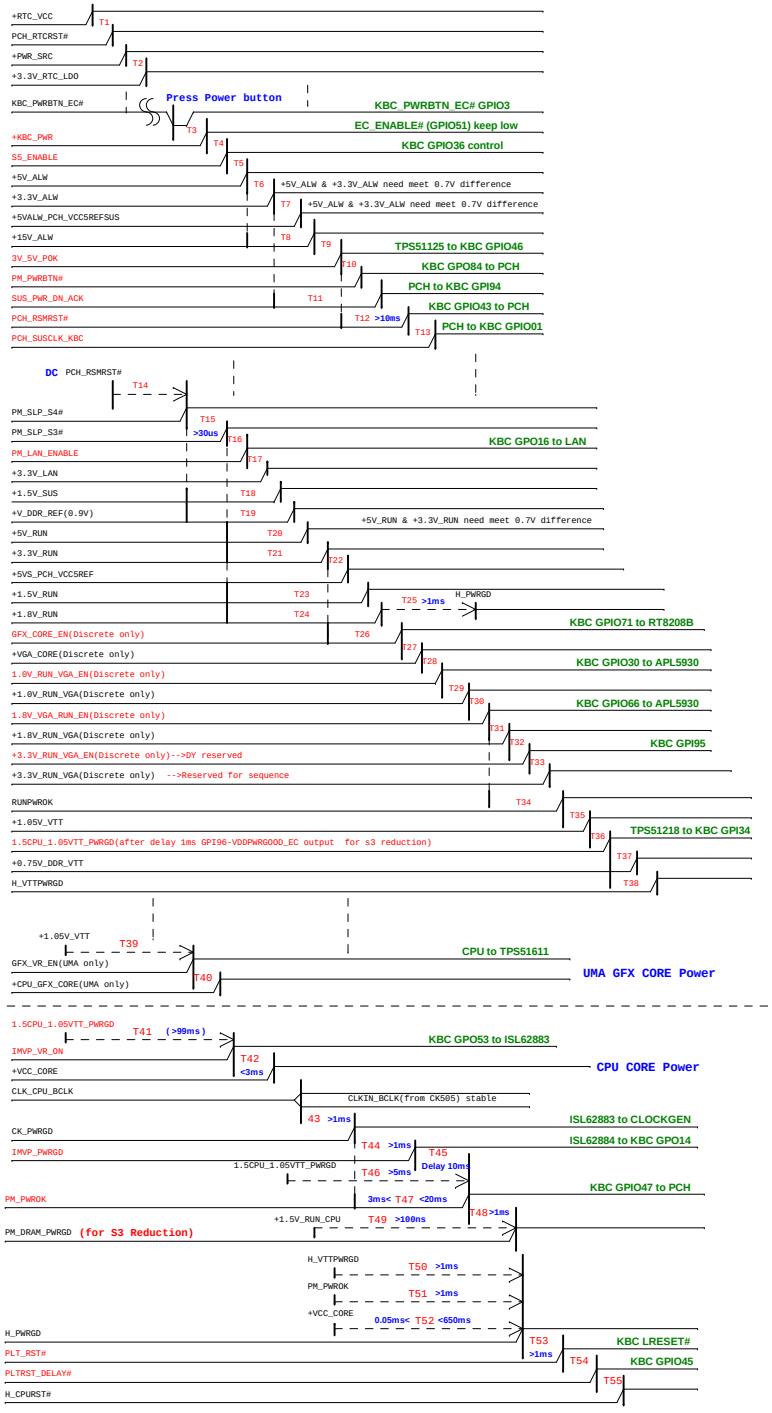
(AC mode)

red word: KBC GPIO

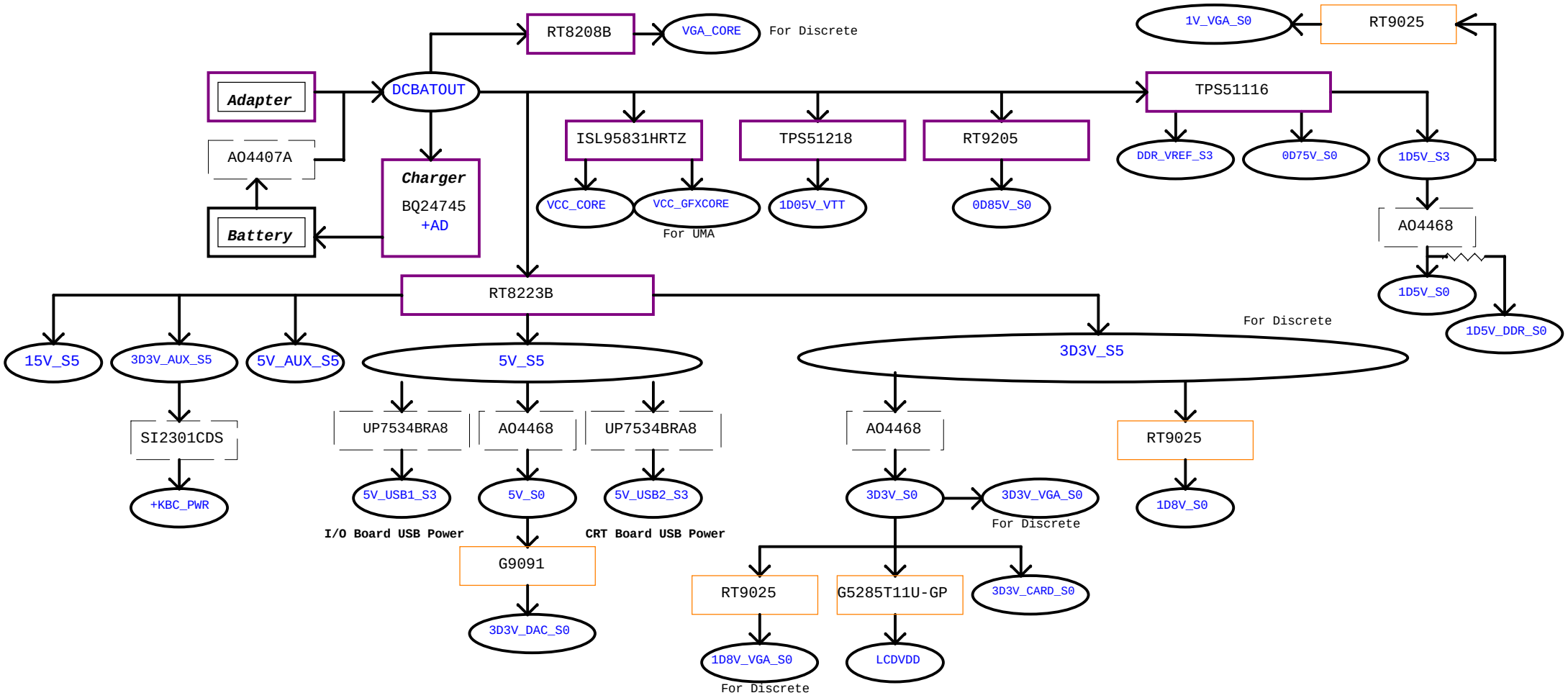


(DC mode)

red word: KBC GPIO



緯創資通	Wistron Corporation		
Title: Power Sequence			
Size: A3	Document Number: LA470	Rev: -1	
Date: Thursday, November 05, 2009	Sheet 59 of 103		



Power Shape

Regulator	LDO	Switch

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
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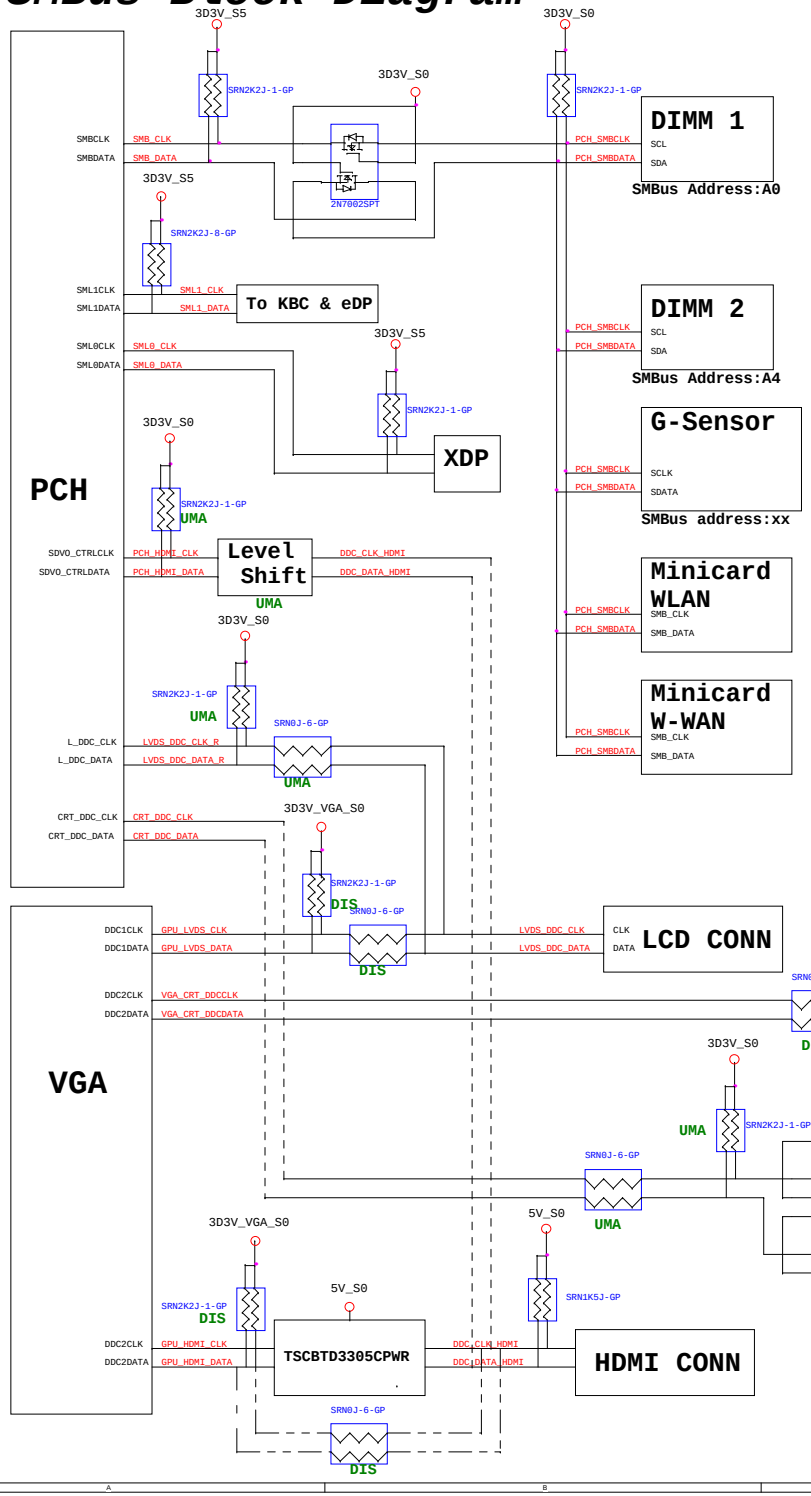
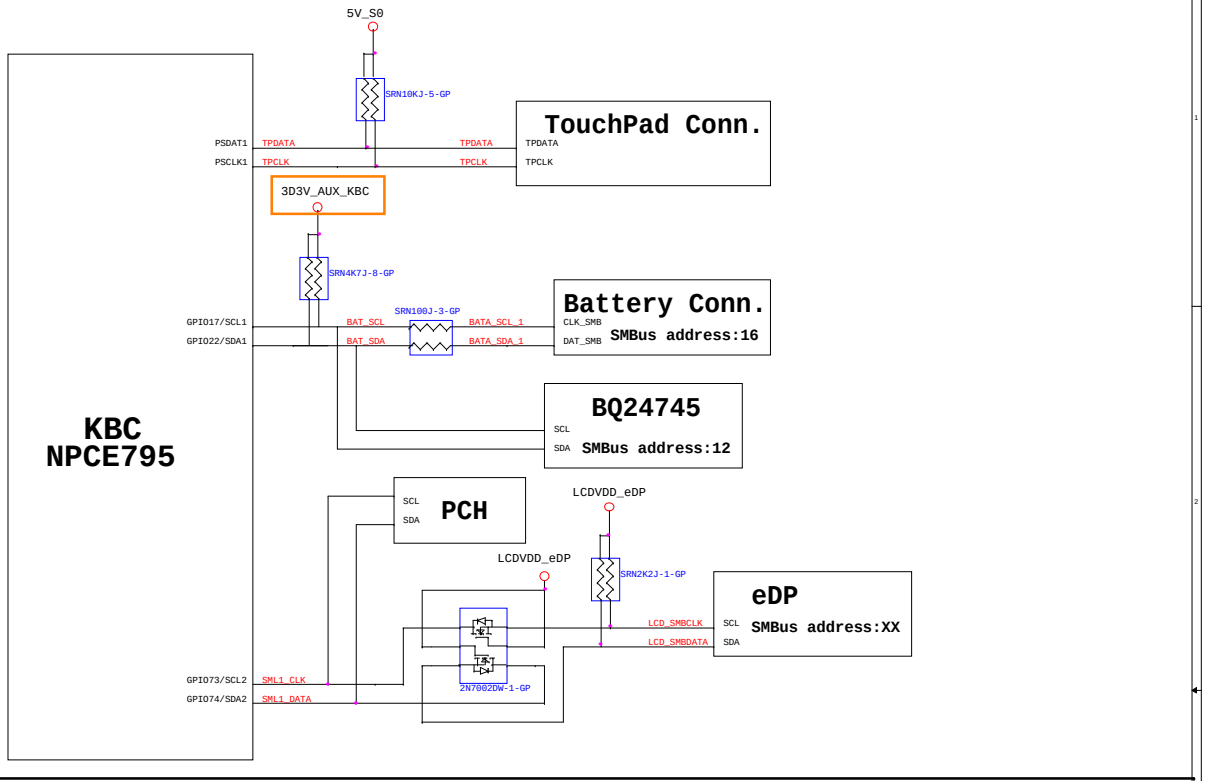
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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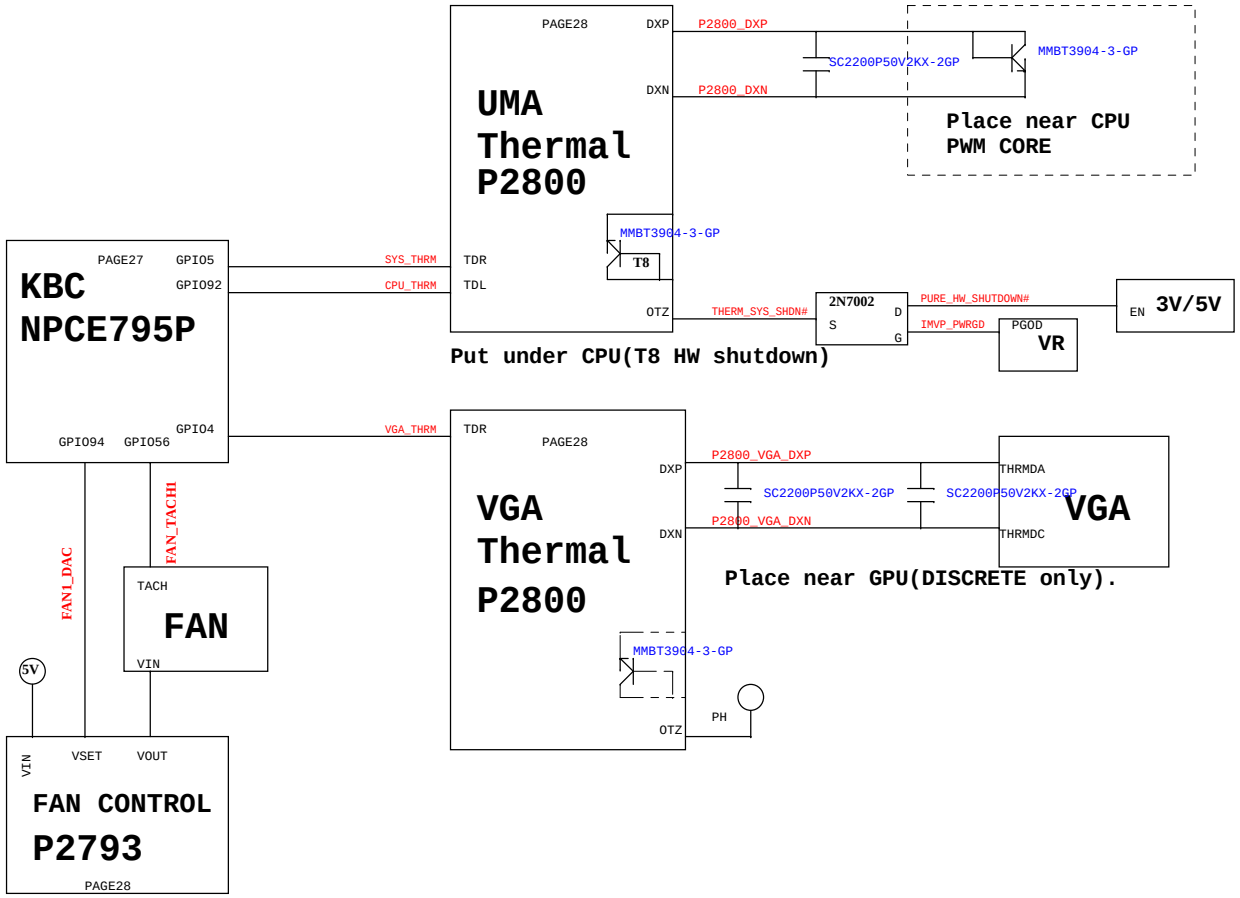
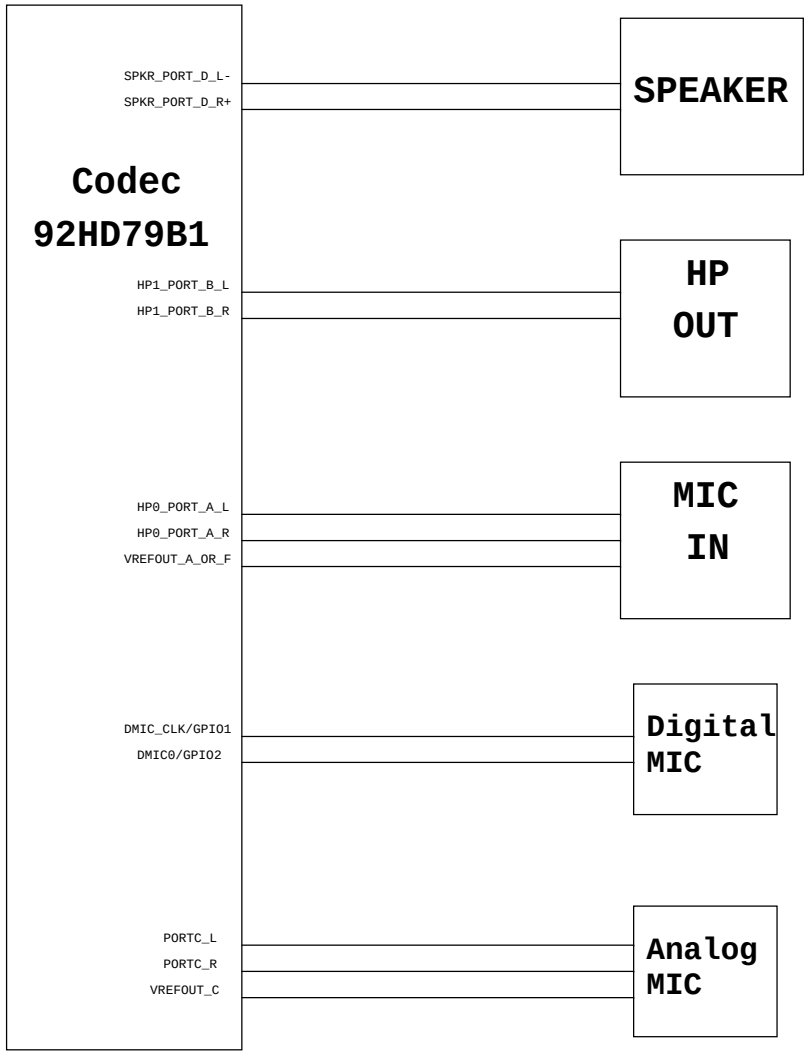
Thermal Block Diagram



Audio Block Diagram



55.4KZ01.S18G S19G

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Title: ***Change History***

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