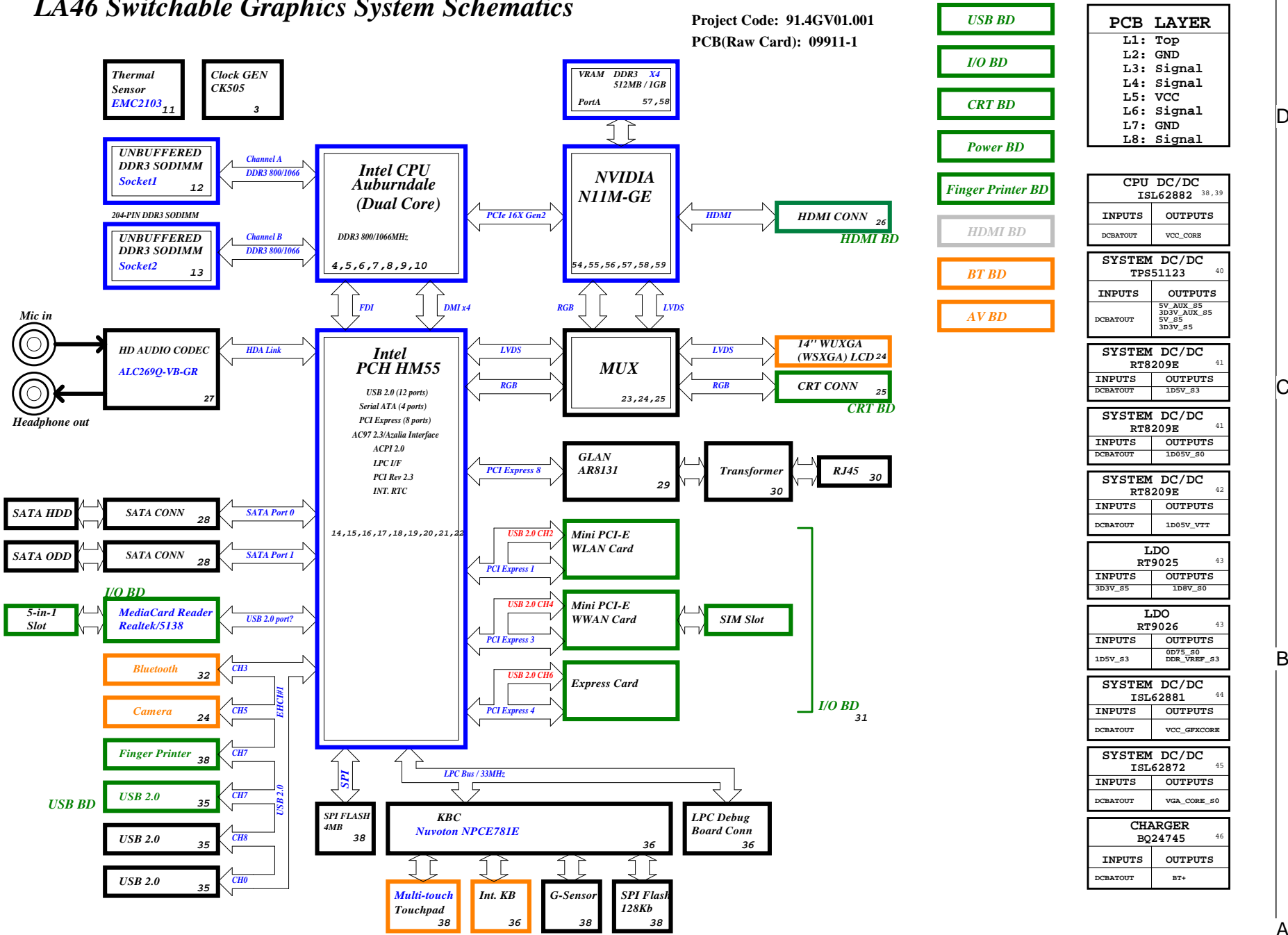


LA46 Switchable Graphics System Schematics

Project Code: 91.4GV01.001
PCB(Raw Card): 09911-1



- USB BD
- I/O BD
- CRT BD
- Power BD
- Finger Printer BD
- HDMI BD
- BT BD
- AV BD

PCB LAYER	
L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Signal

CPU DC/DC	
ISL62882 38, 39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC	
TPS51123 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC	
RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC	
RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC	
RT8209E 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO	
RT9025 43	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO	
RT9026 43	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC	
ISL62881 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC	
ISL62872 45	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER	
BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	BT+

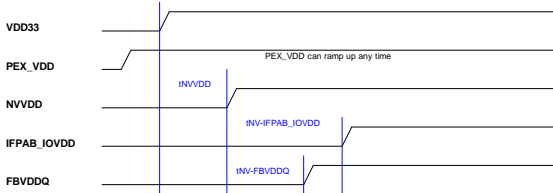
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarkfield samples.	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

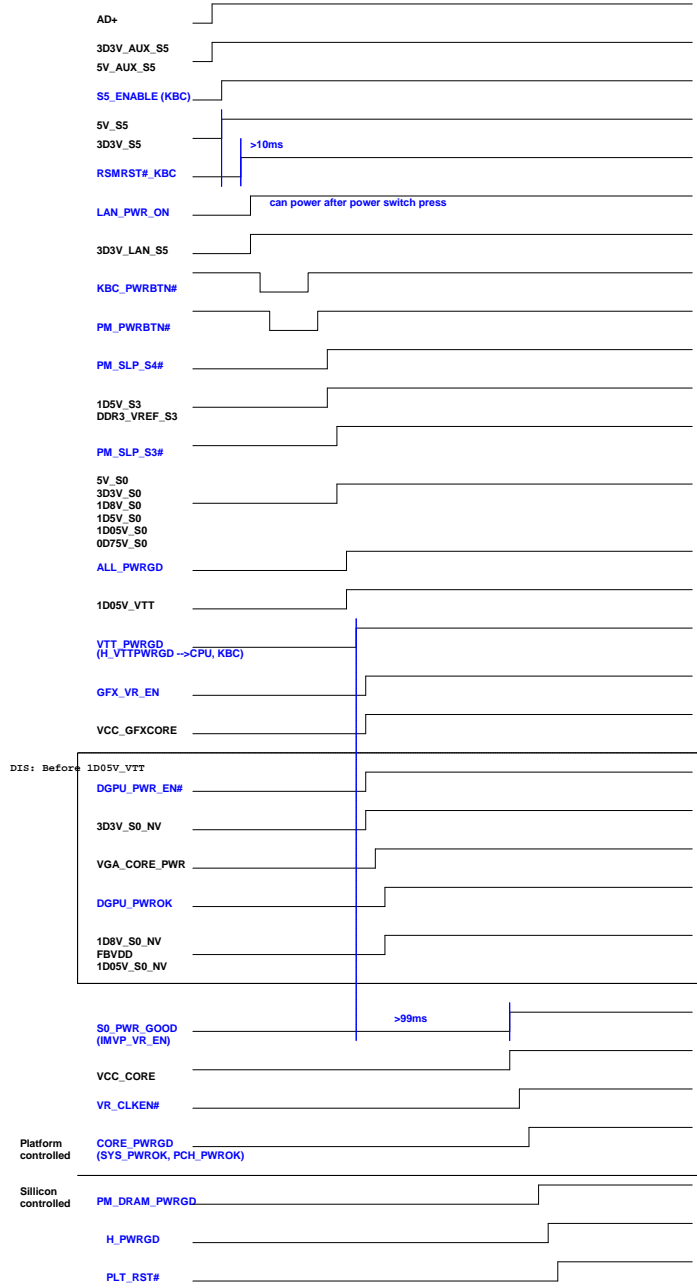
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ES1 compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence

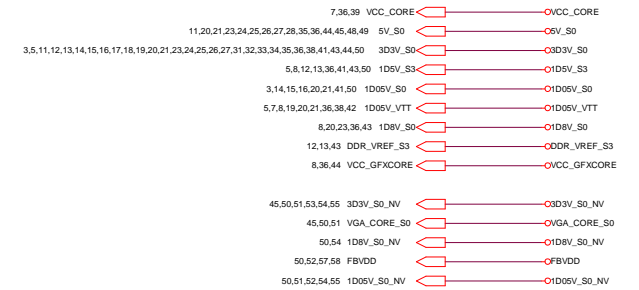


Sequence AC



PLANAR_ID[1..0]

KBC GPin	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0	LA46 - SA	SA
	0	0	LA46 - SB	SB
	0	1	LA46 - SB	SC
	1	0		
	1	1		-1



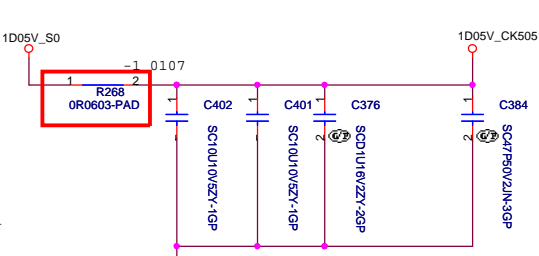
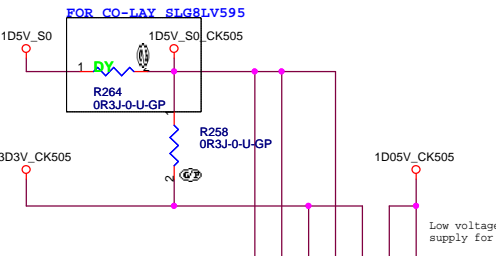
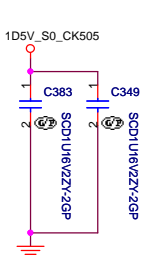
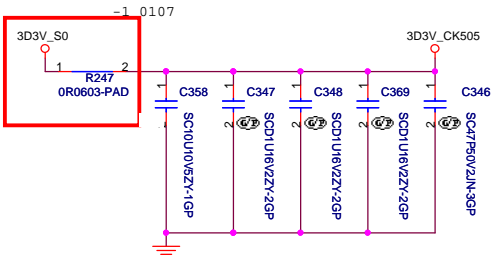
<Core Design>

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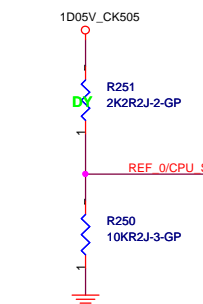
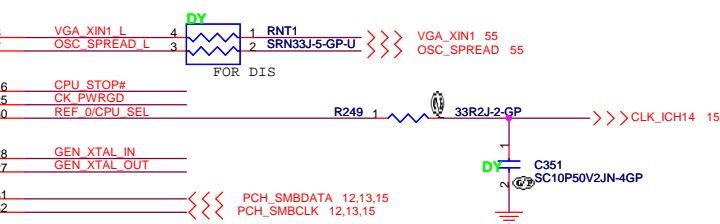
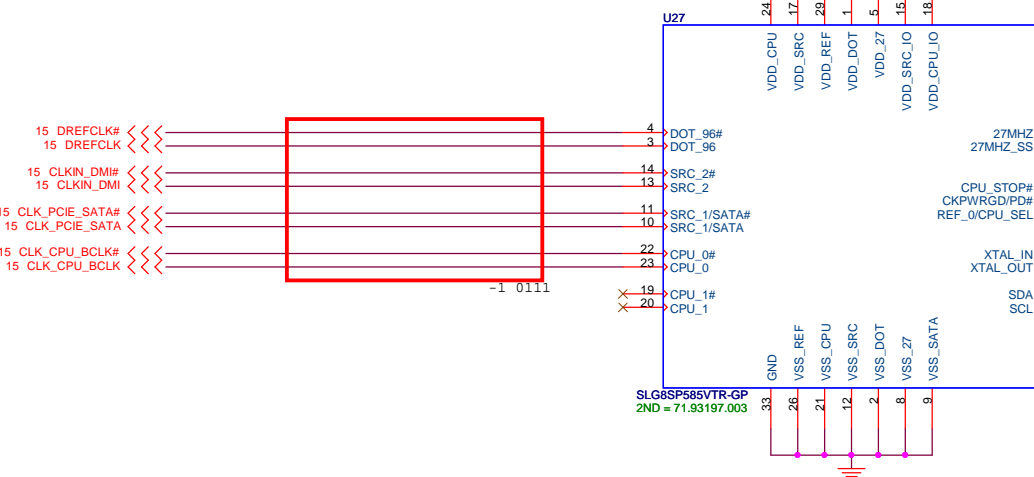
File	Document Number	Rev
A2	LA46 MB	-1

02 Reference

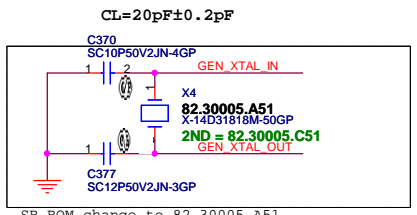
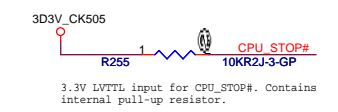
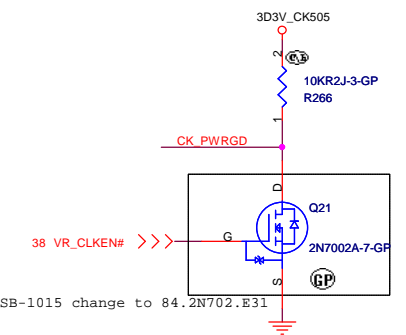
Date: Wednesday, January 27, 2010 Sheet 2 of 58



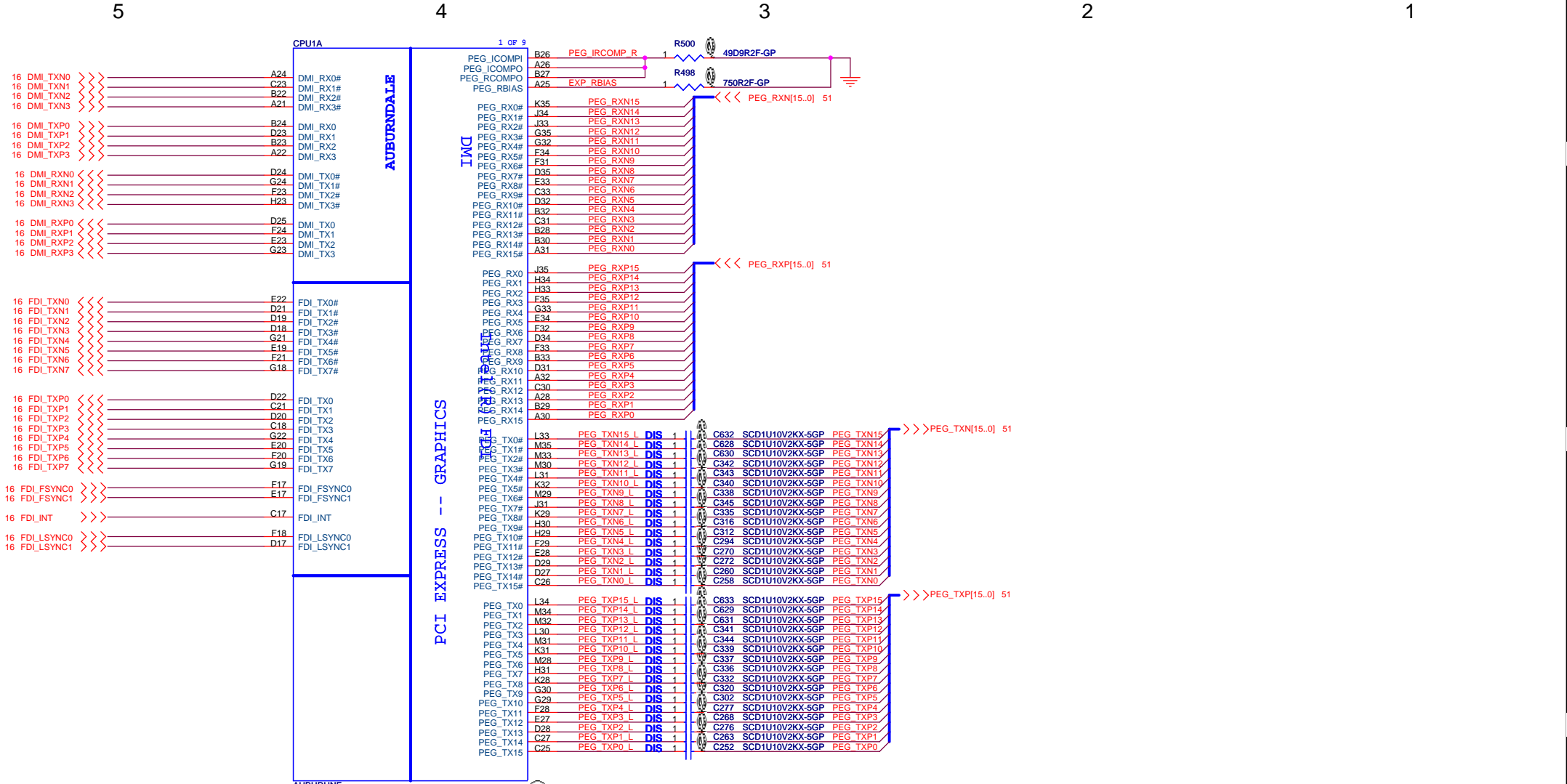
VGA_27M	RNT1	R75	X1	R79	R80	C107	C131
Crystal	DY	DY	Mount	Mount	Mount	Mount	Mount
CLK_GEN	Mount	Mount	DY	DY	DY	DY	DY

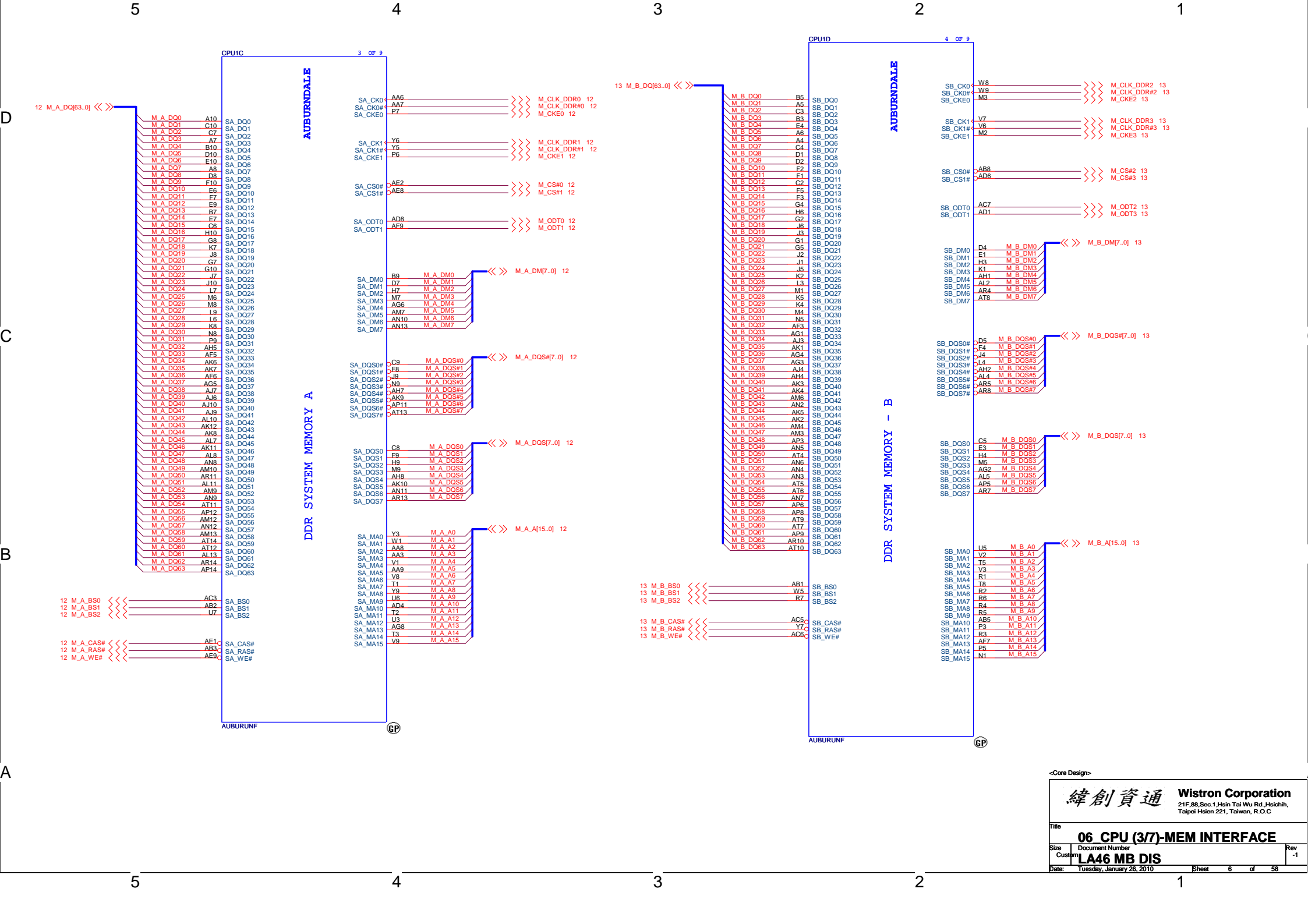


FSC	0	1
SPEED	133MHz (Default)	100MHz



Layout Notes:
 Make sure that the stubs to the test points (CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.



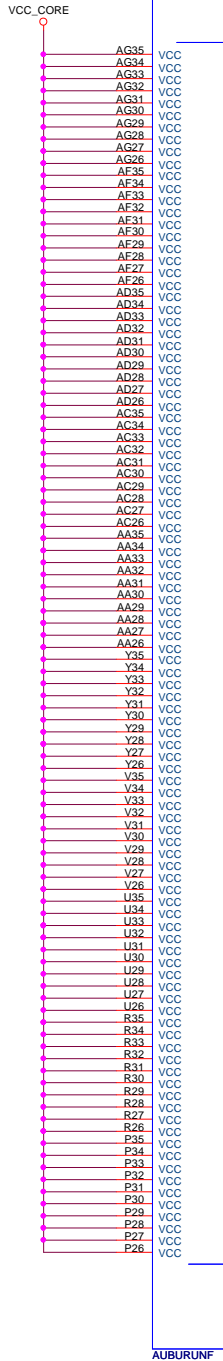
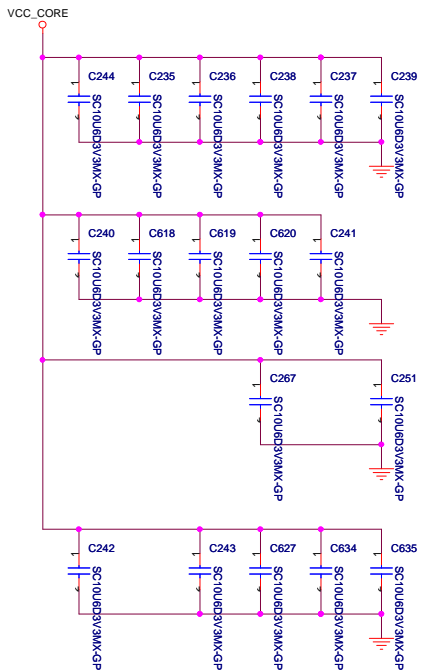


<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C

Title		06 CPU (3/7)-MEM INTERFACE	
Size	Document Number	Sheet	Rev
Custom	LA46 MB DIS	6	-1
Date:	Tuesday, January 28, 2010	Sheet	6 of 58

PROCESSOR CORE POWER
48A -->Arrandale



AUBURNDALE

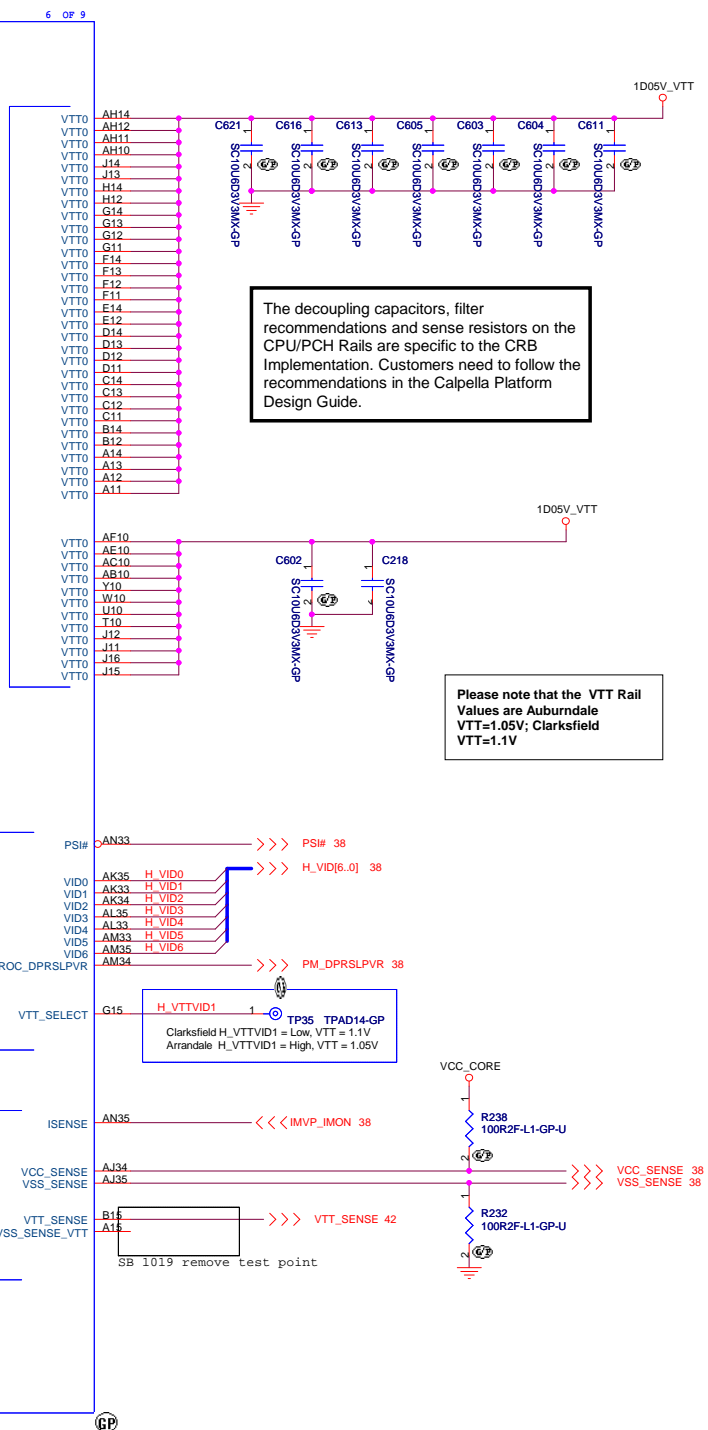
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

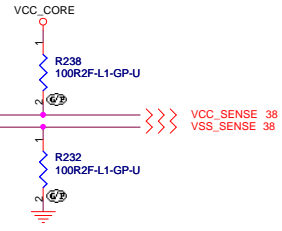
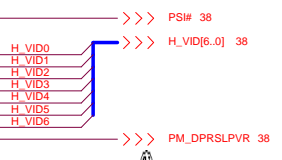
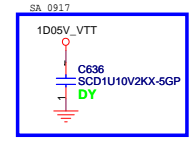
CPU VIDS

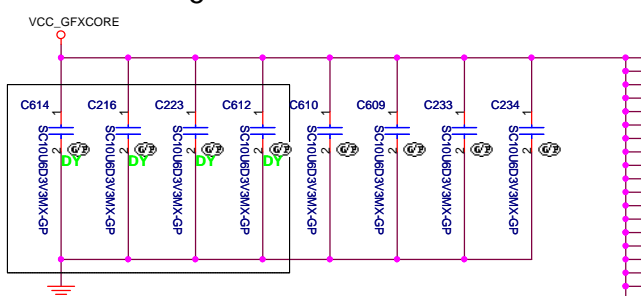
SENSE LINES



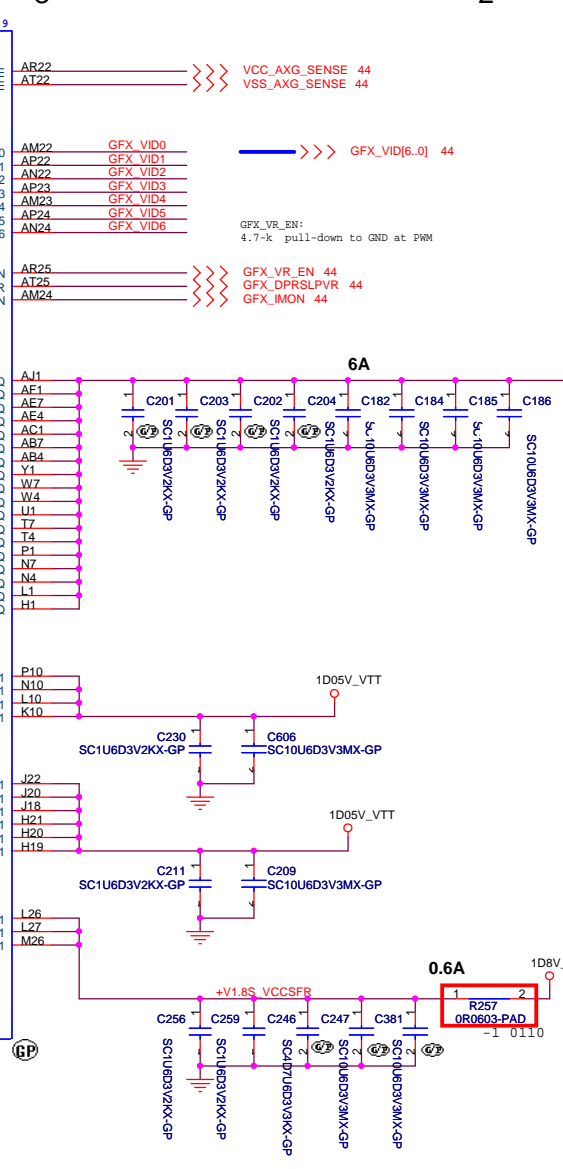
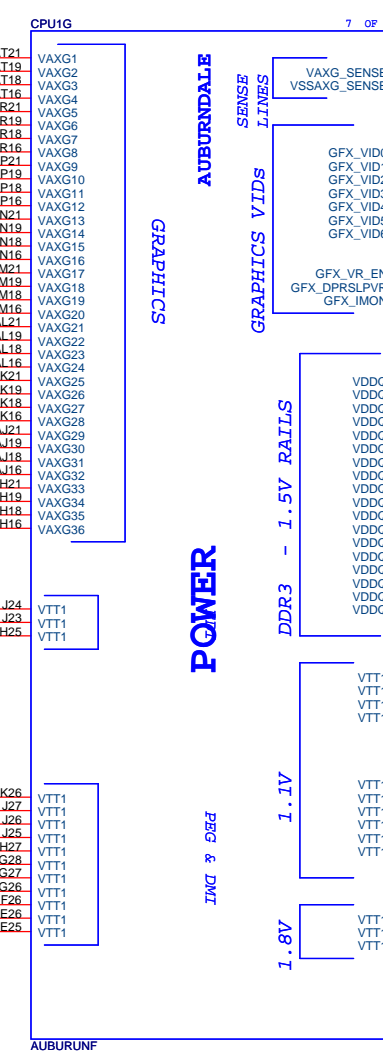
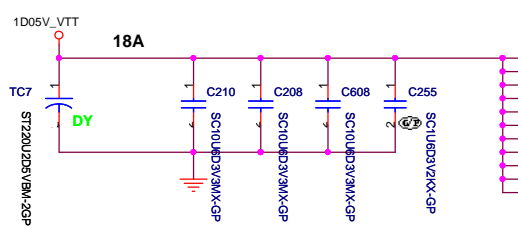
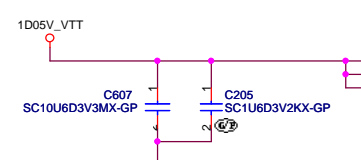
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

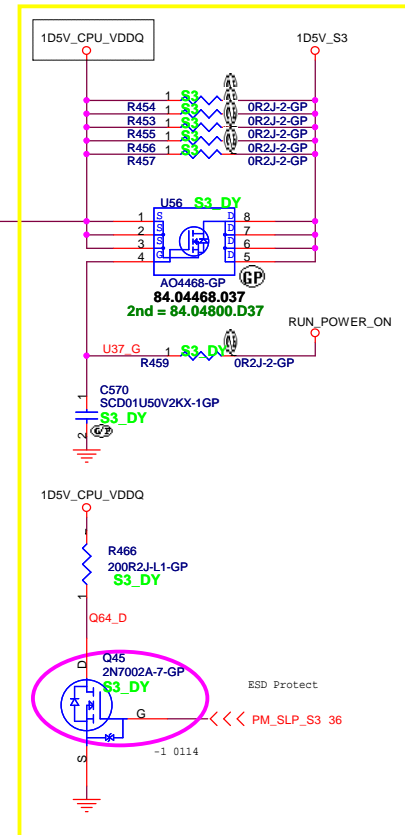




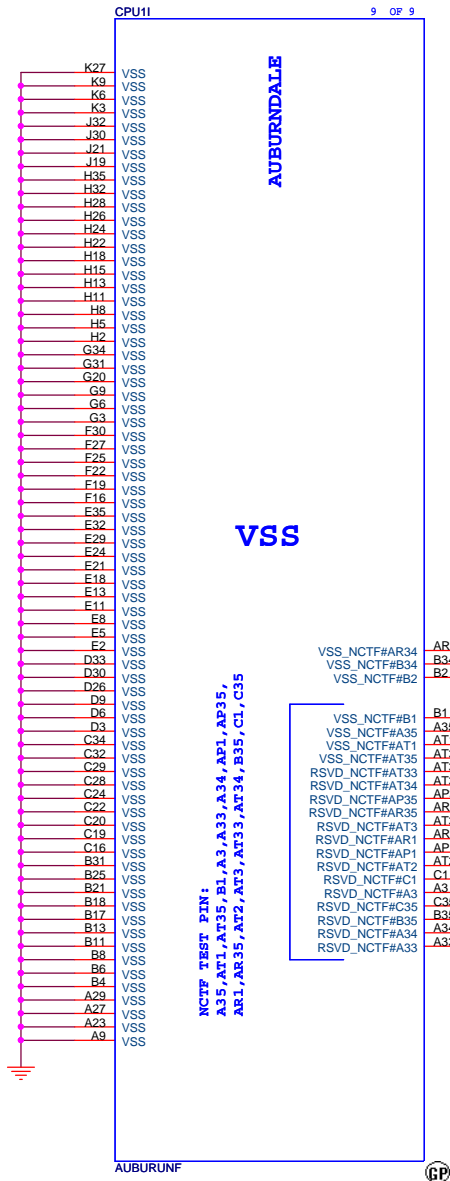
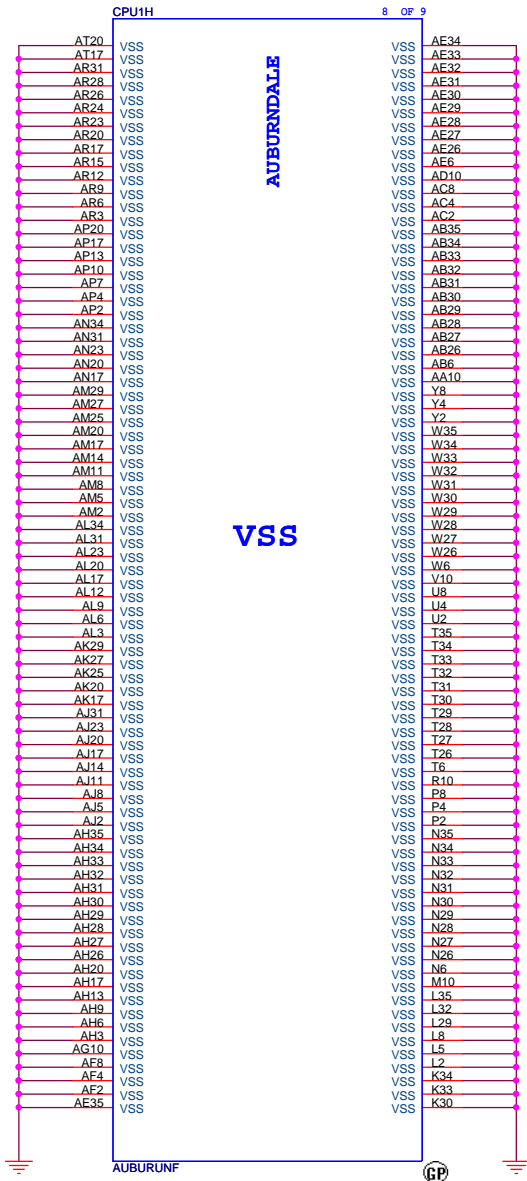
Please note that the VTT Rail Values are Aurburndale
VTT=1.05V; Clarksfield
VTT=1.1V



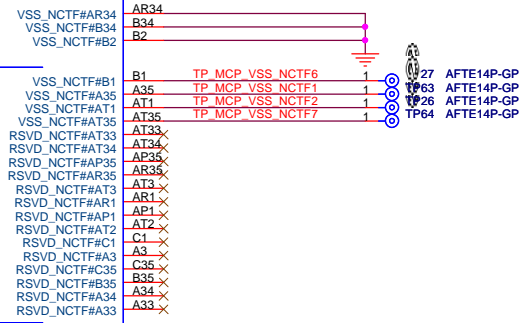
SA 0901: LC require to reserve s3 reduce power circuit

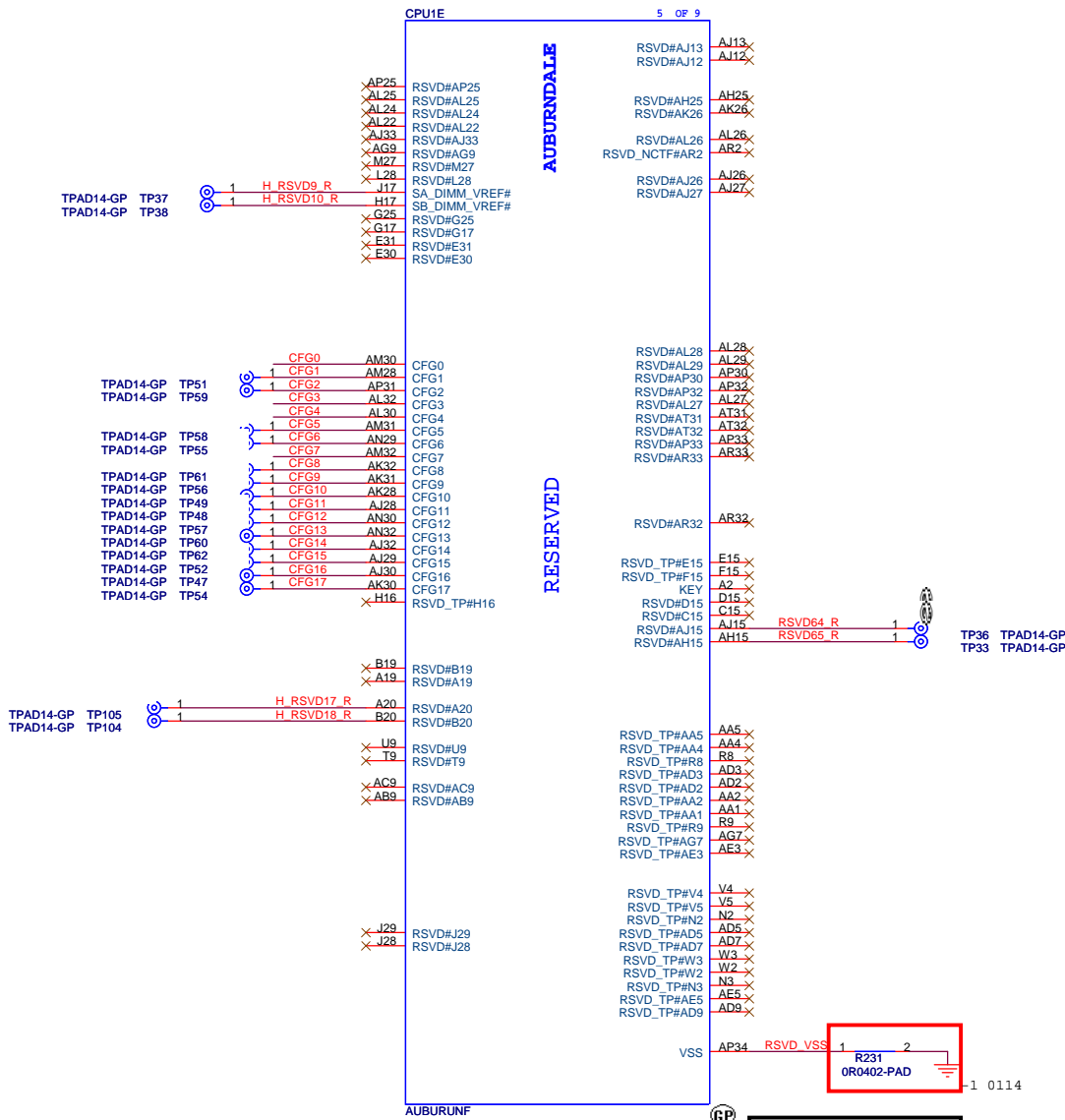


SA 0903: Place across the plane
SB 1022 Remove

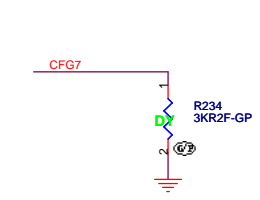
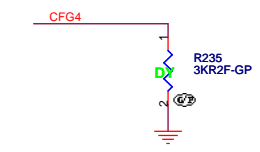
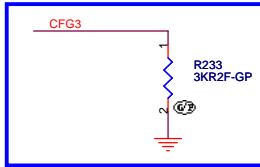
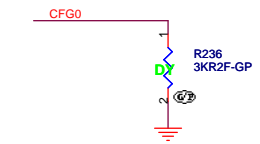


NCTF TEST PIN:
 A35, AT1, AT35, B1, A3, A33, A34, AP1, AP35,
 AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35





VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



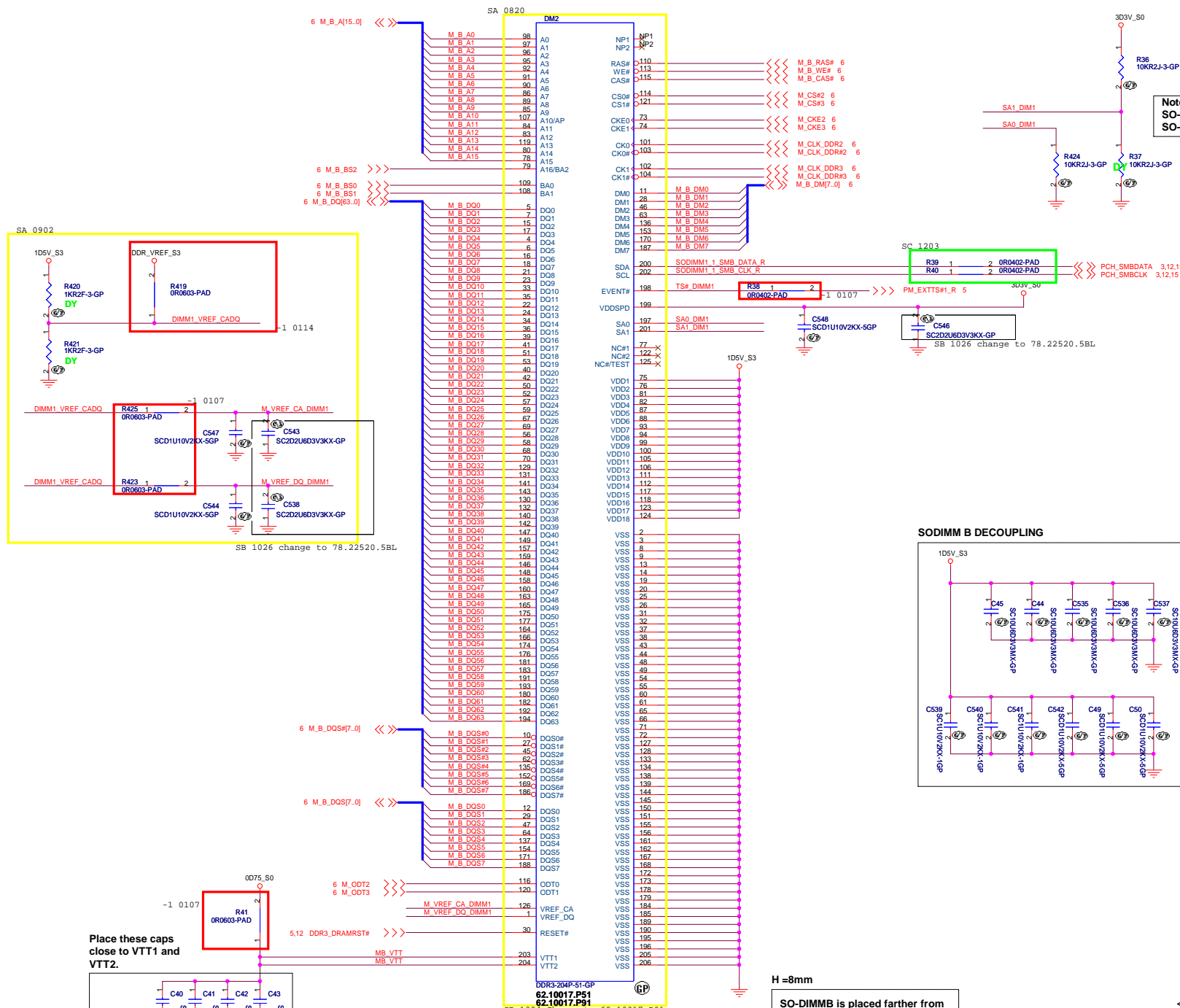
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

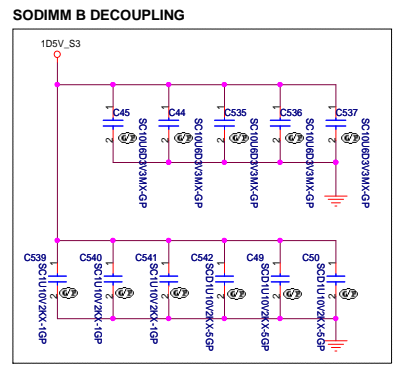
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

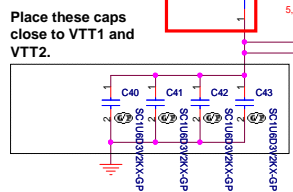
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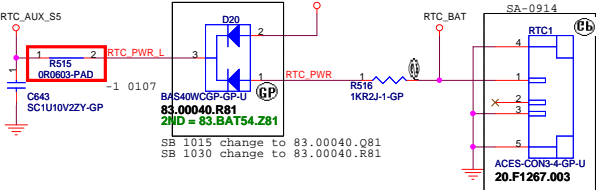
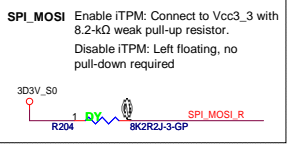
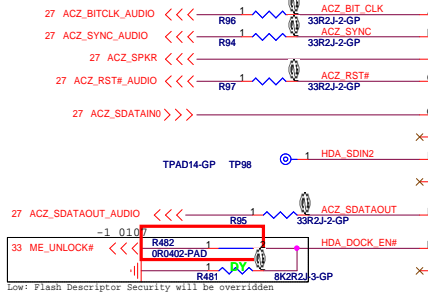
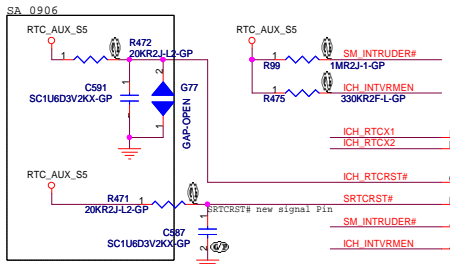
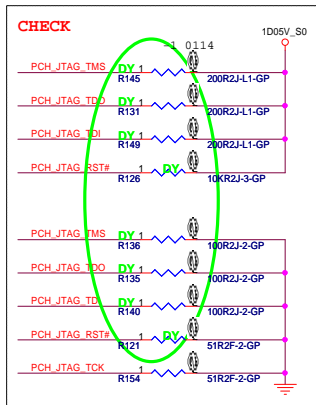
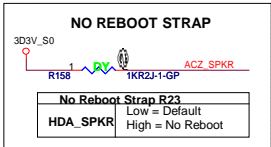
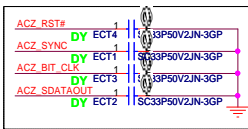
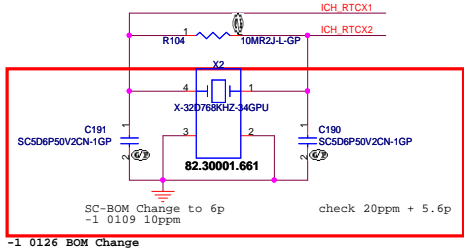


Note:
SO-DIMMB SPD Address is 0x44
SO-DIMMB TS Address is 0x34

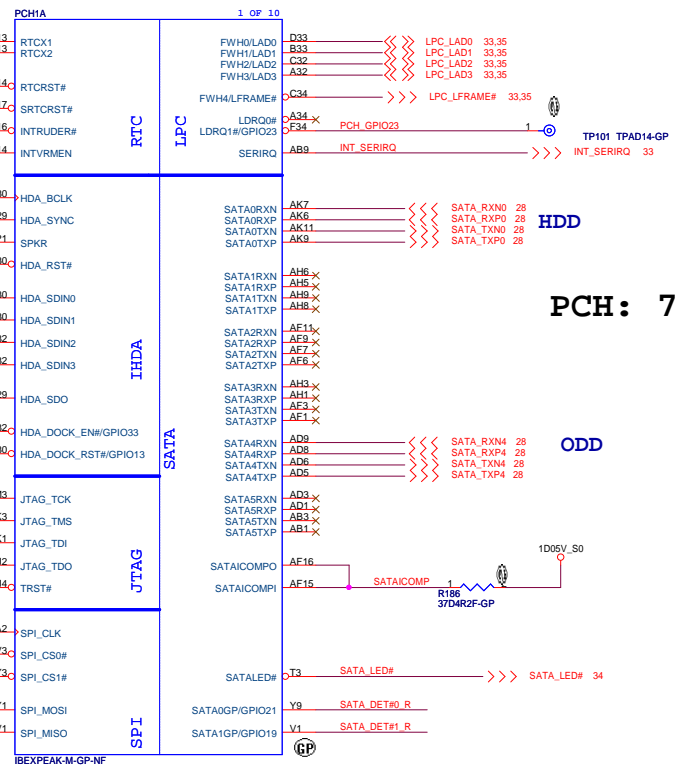


H = 8mm
SO-DIMMB is placed farther from the Processor than SO-DIMMA





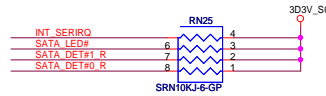
Integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable



PCH: 71.0IBEX.G0U

HDD

ODD



SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SB 1015 change to 83.00040_Q81
SB 1030 change to 83.00040_R81

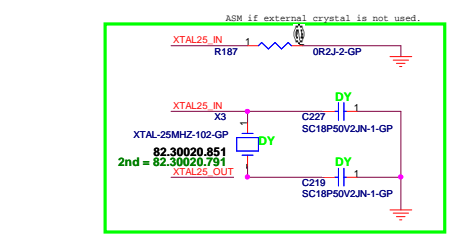
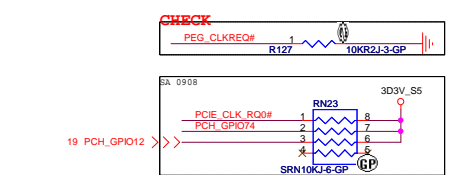
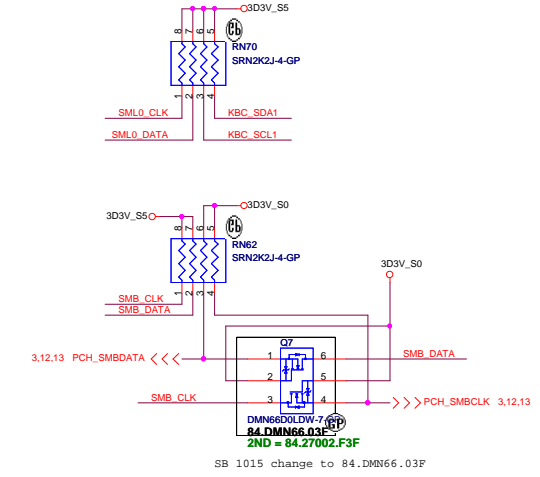
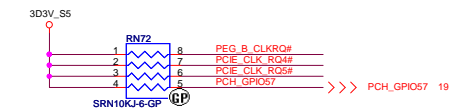
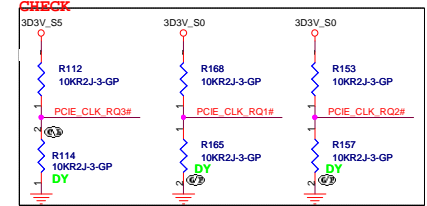
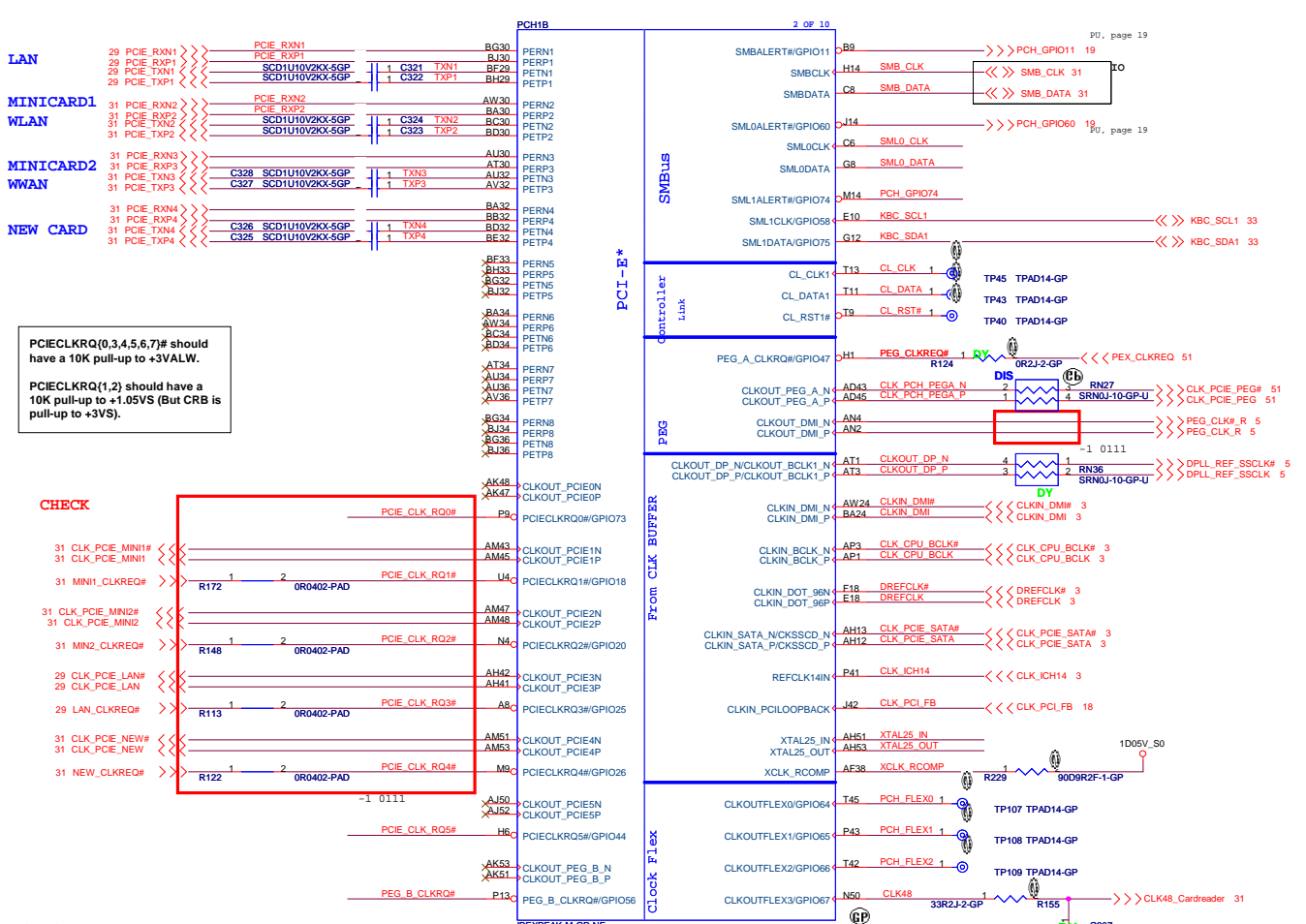
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Title: **14 PCH (1/9)-SATA/SPI/LPC/HDA**

Size: Custom Document Number: **LA46 MB DIS** Rev: -1

Date: Wednesday, January 27, 2010 Sheet: 14 of 58

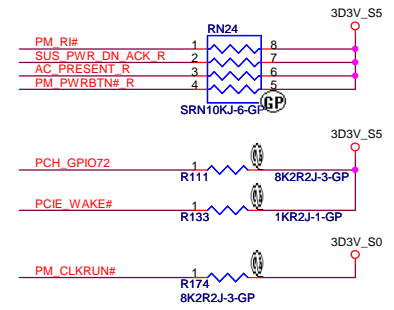
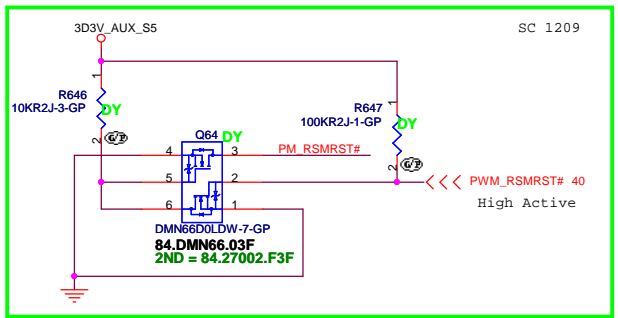
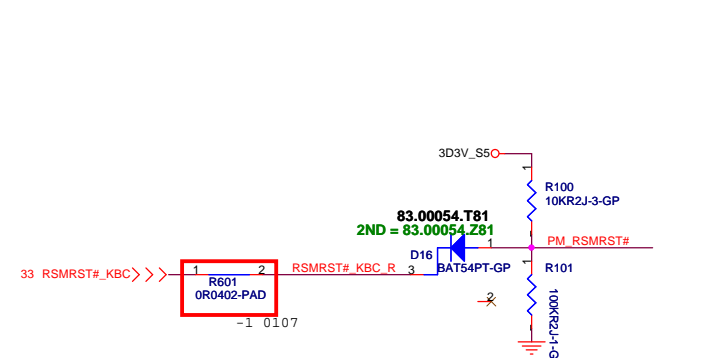
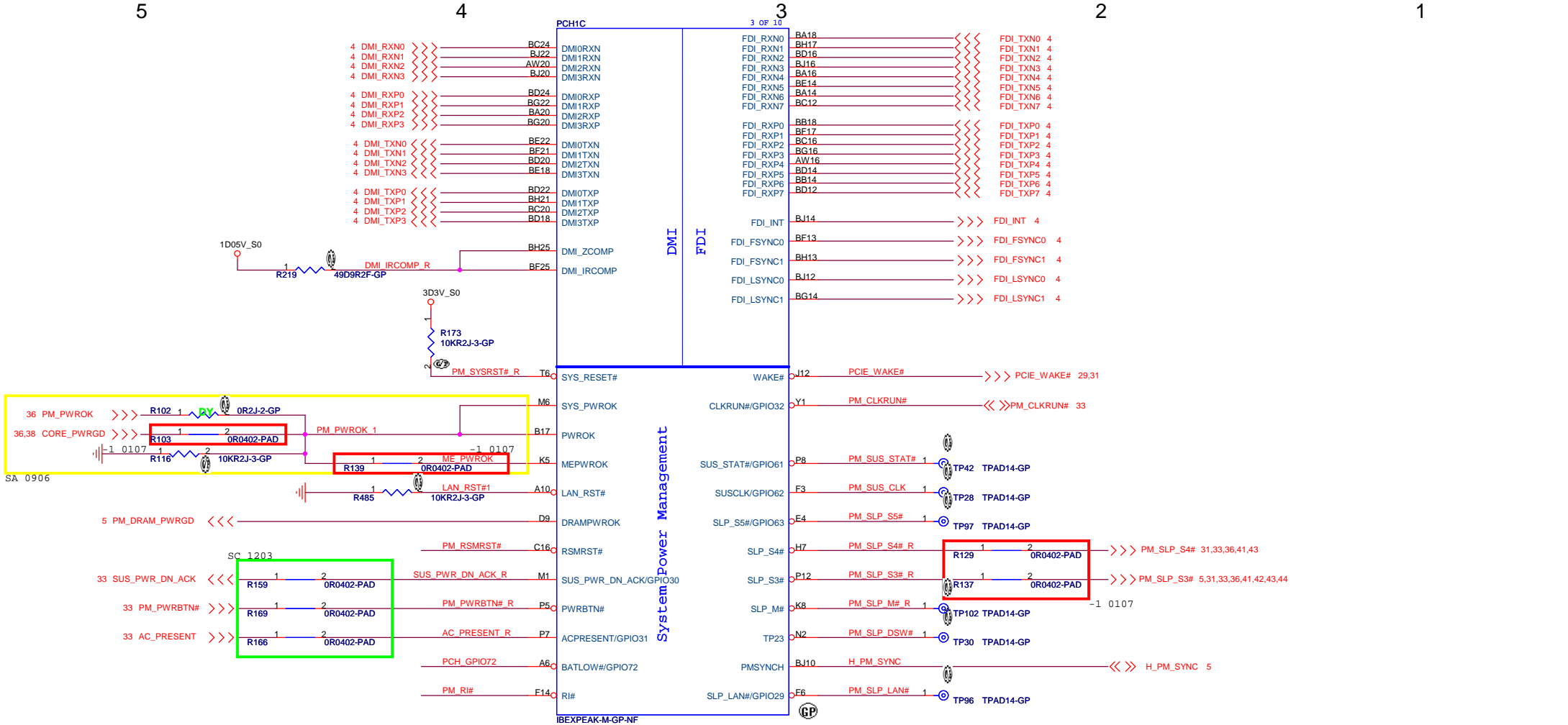


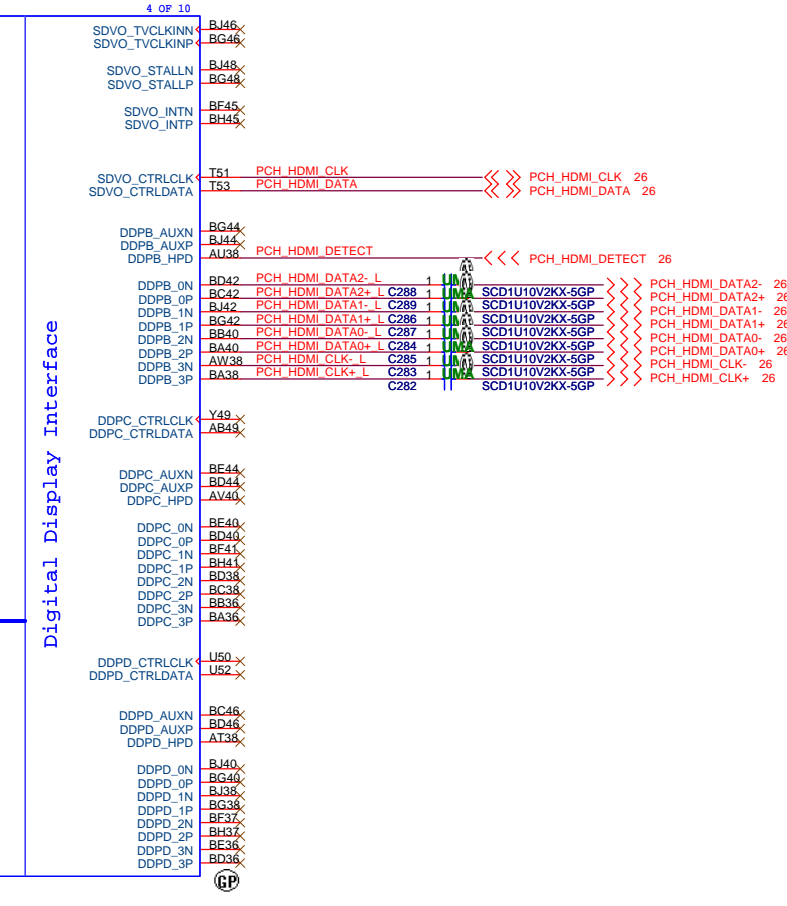
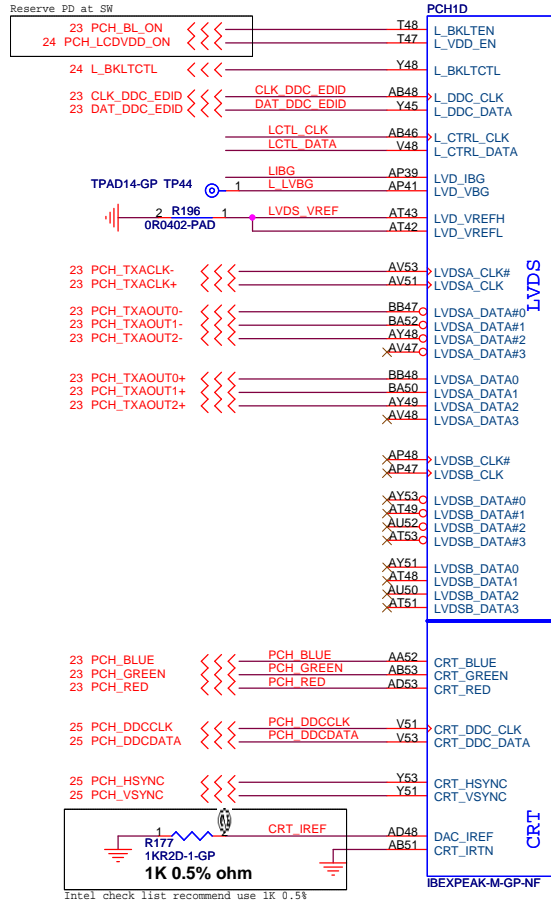
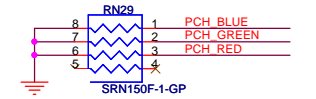
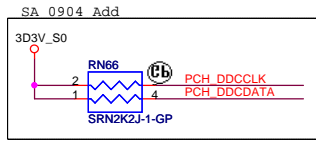
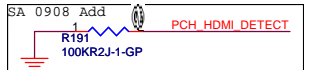
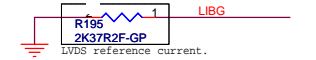
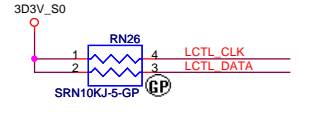
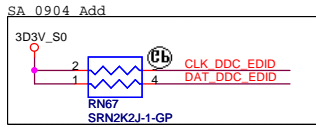
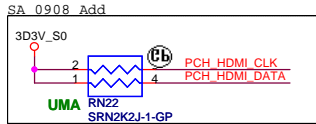
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

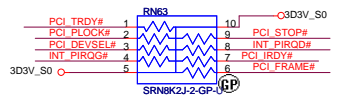
File: **15_PCH (2/9)-PCIE / SMBUS / CLK**

Size: **LA46 MB DIS**

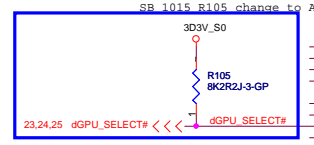
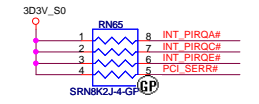
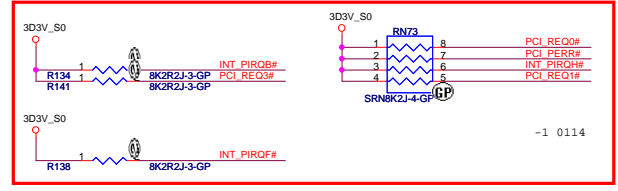
Date: Tuesday, January 26, 2010



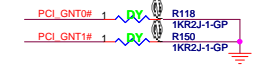




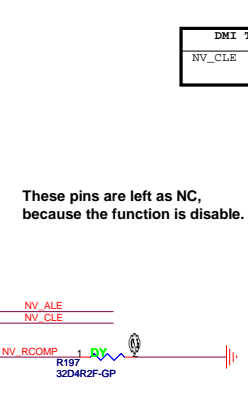
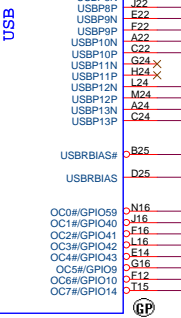
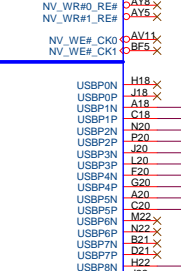
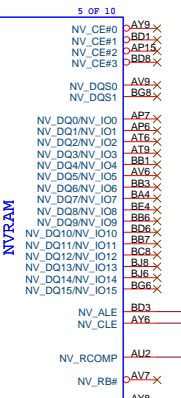
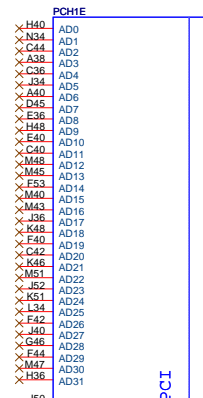
These pins are left as NC, because the function is disable.



24 dGPU_PWM_SELECT# <<<< dGPU_PWM_SELECT#



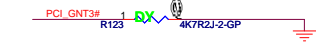
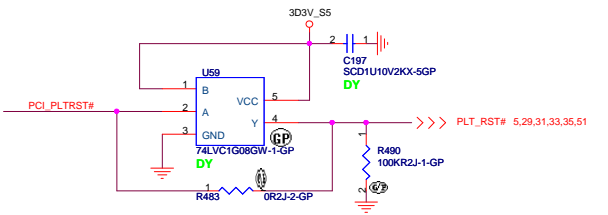
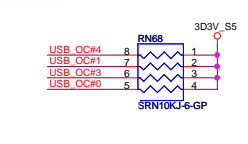
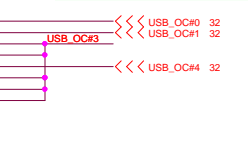
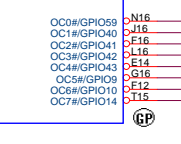
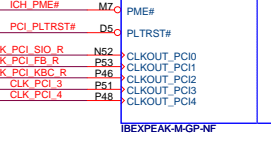
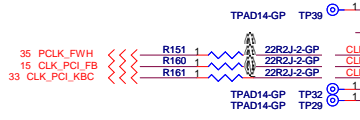
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC (Default)
1	0	Reserved
0	1	PCI
1	1	SPI



These pins are left as NC, because the function is disable.

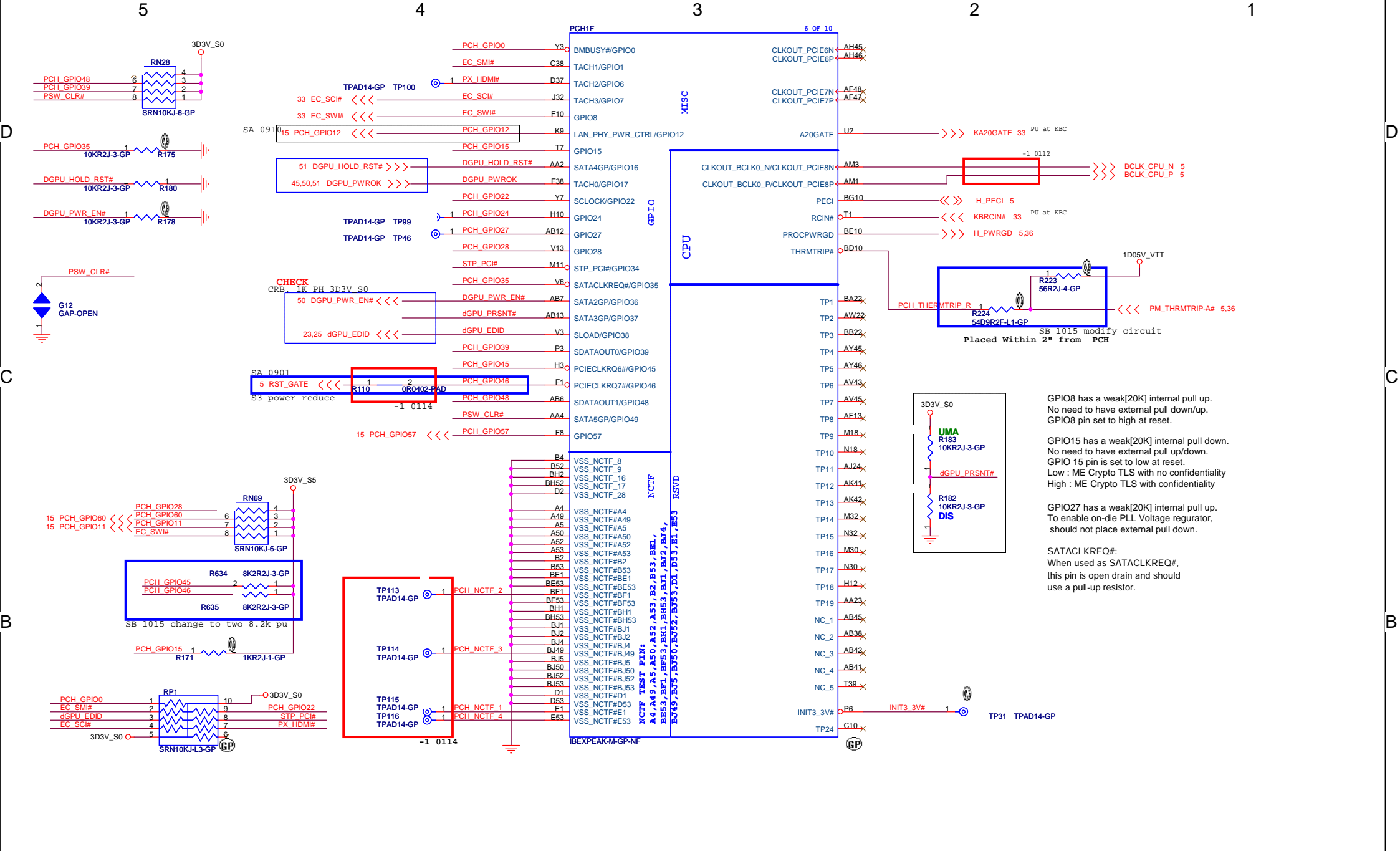
Danbury Technology: Disabled when Low. Enable when High.

Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	Card Reader
5	WWAN
6	Disable (HM55)
7	Disable (HM55)
8	USB2
9	Blue Tooth
10	Finger Print
11	NC
12	Express Card
13	Camera



PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---

OC#0	Port 0 & 1	
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	EHCI 1
OC#3	Port 6 & 7	
OC#4	Port 8 & 9	
OC#5	Port 10 & 11	EHCI 2
OC#6	Port 12 & 13	
OC#7	Floater OC# (not used)	



GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

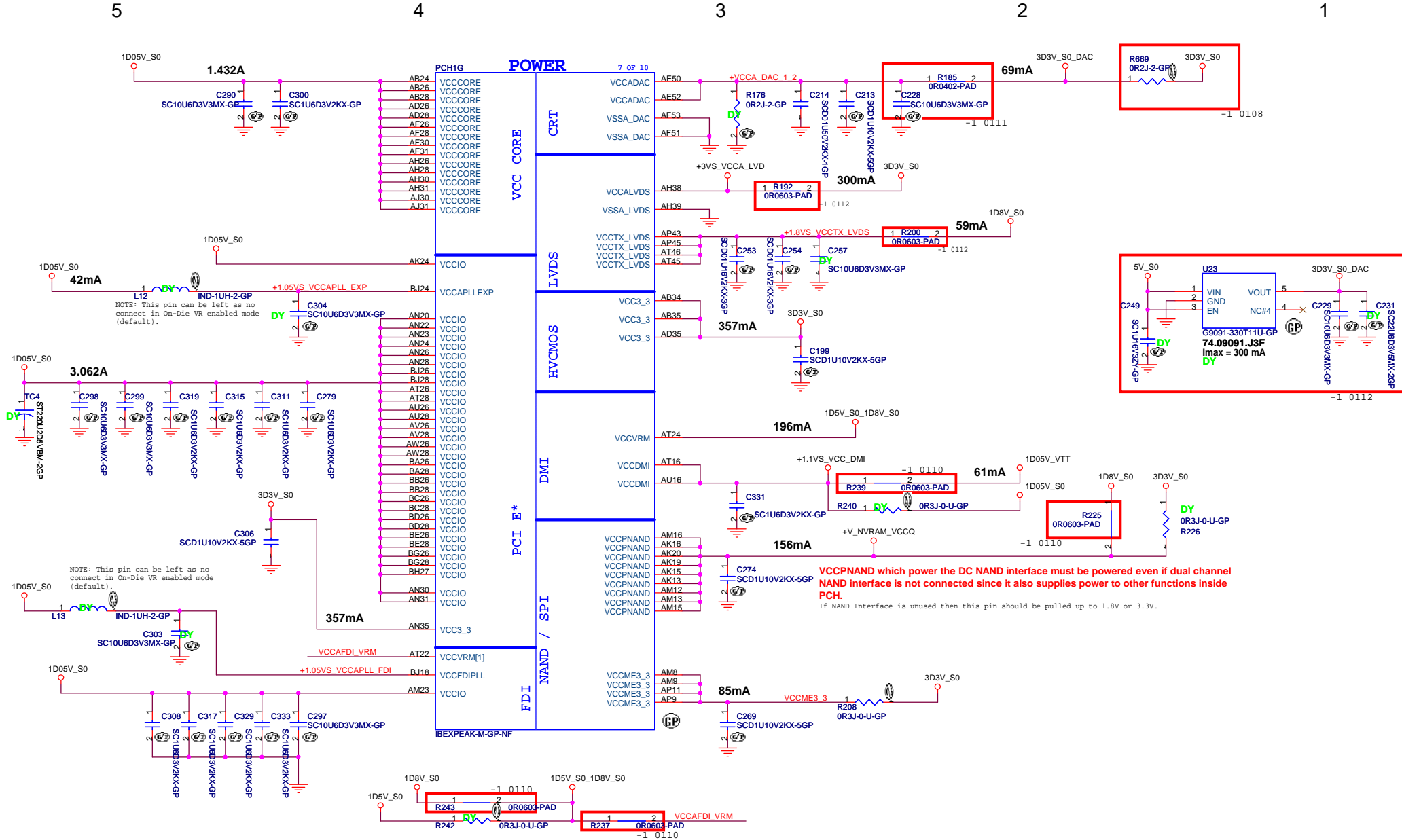
GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

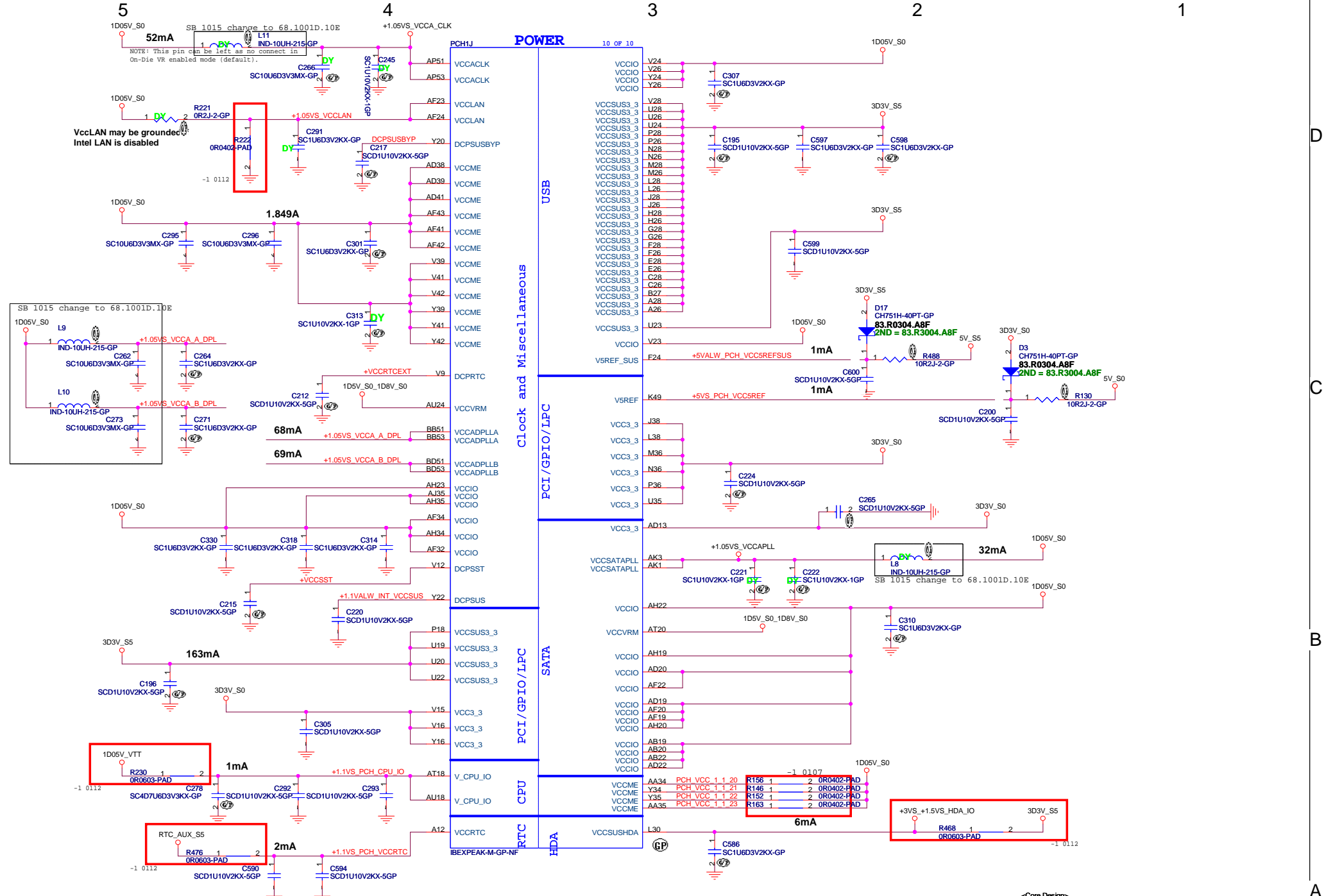
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

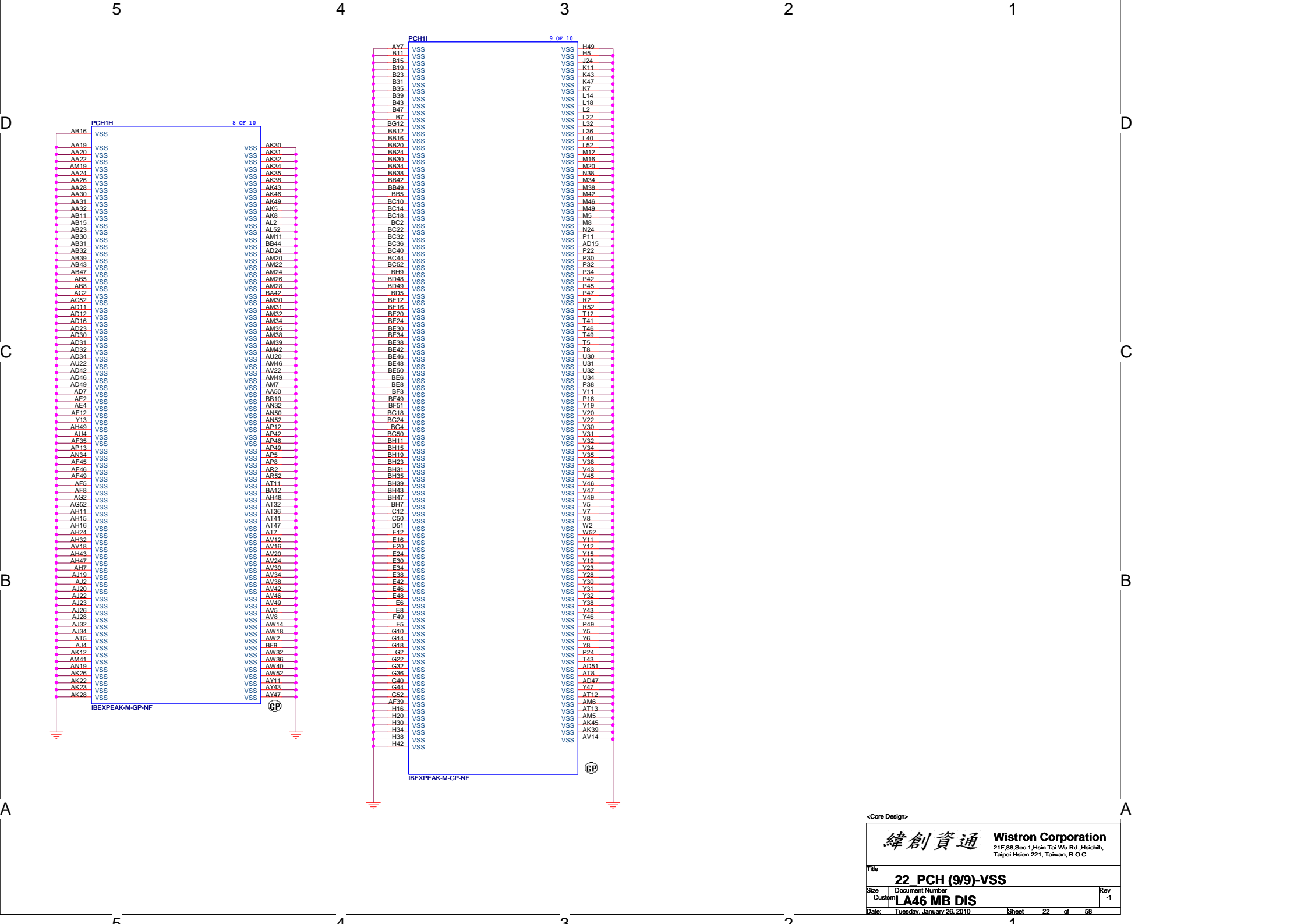
SATACLKREQ#:
When used as SATACLKREQ#,
this pin is open drain and should use
a pull-up resistor.

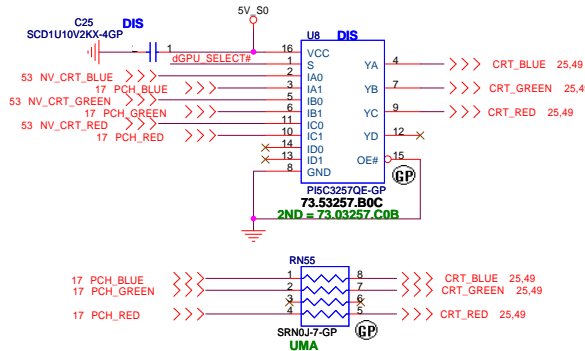
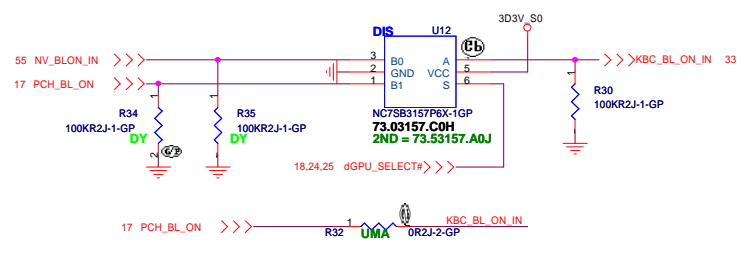
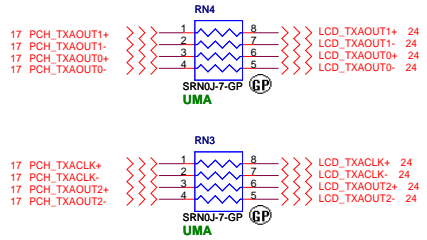
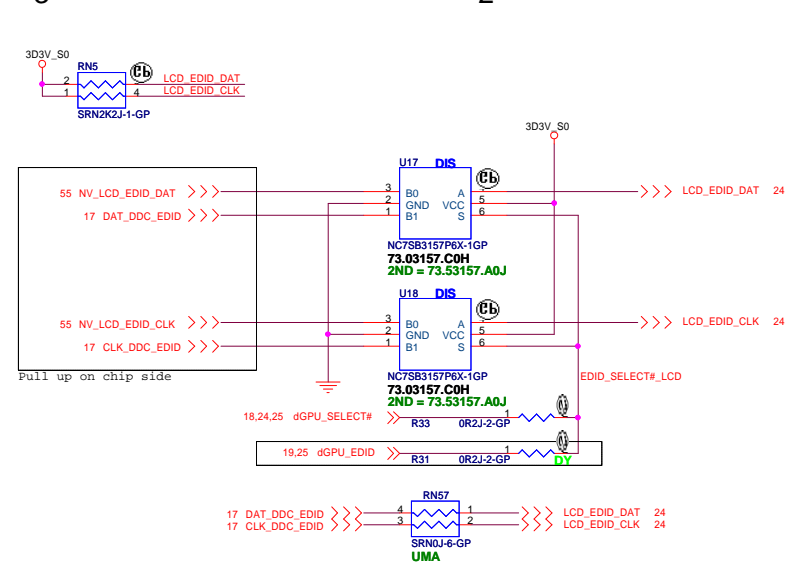
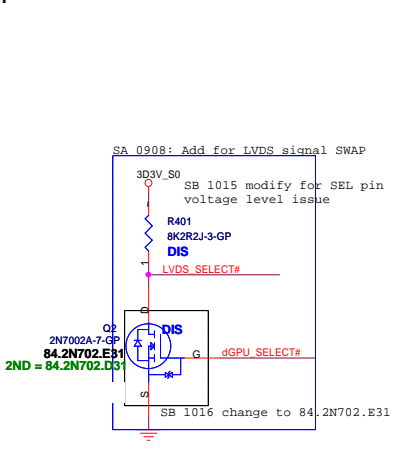
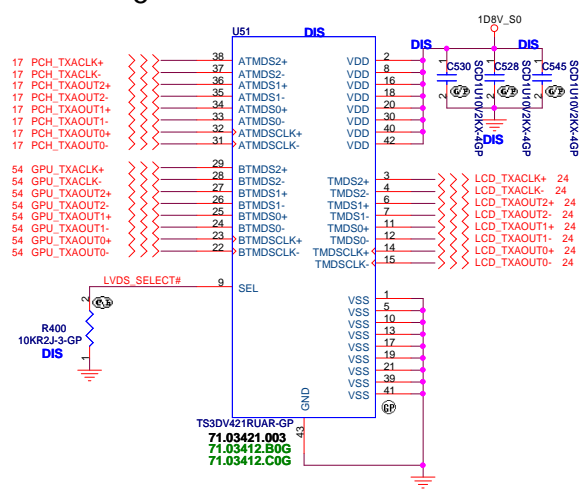
<Core Design>

緯創資通		Wistron Corporation	
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
File			
19 PCH (6/9)-GPIO/VSS NCTF/RSVD			
LA46 MB DIS			
Size	Document Number	Sheet	Rev
A3		19	-1
Date:	Tuesday, January 26, 2010	Sheet	19 of 58









FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

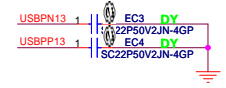
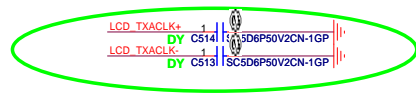
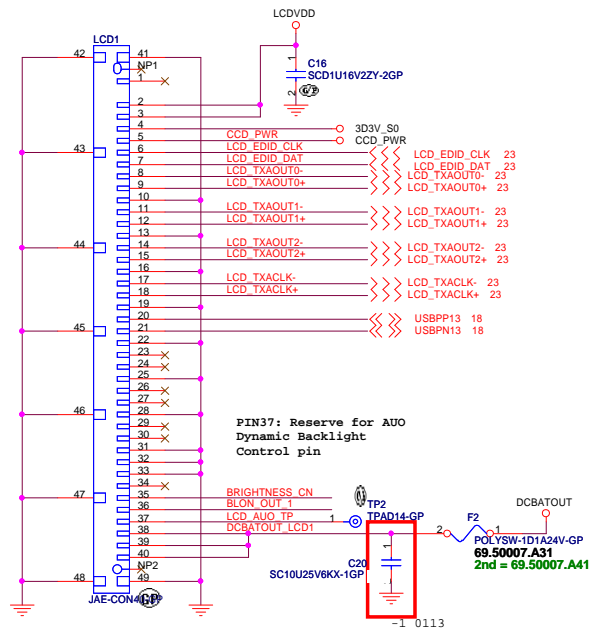
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

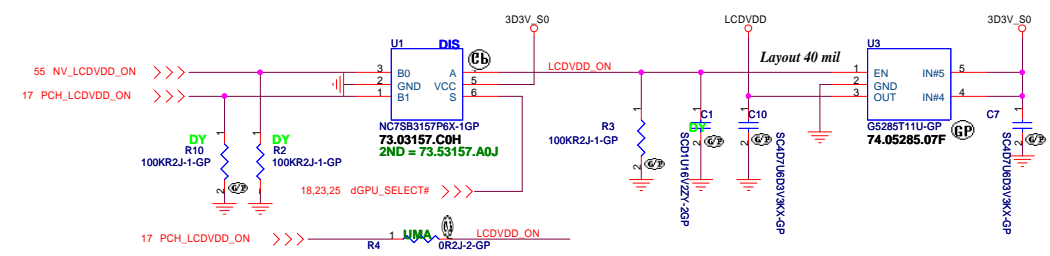
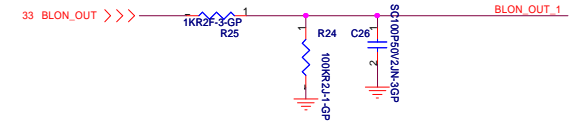
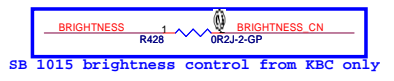
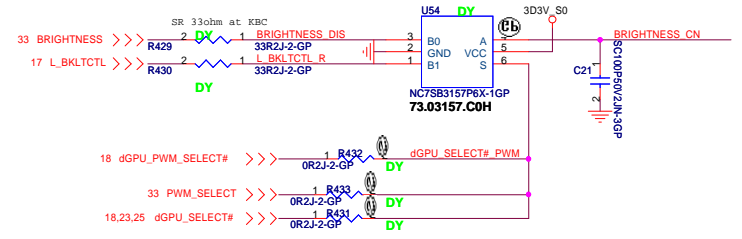
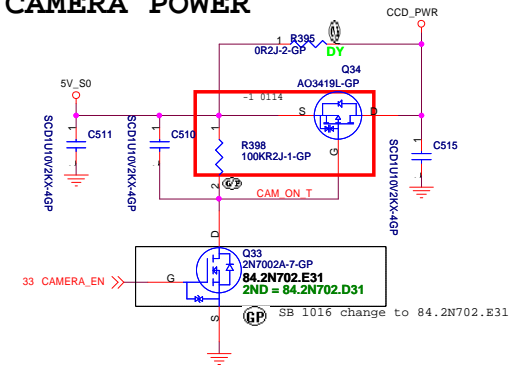
緯創資通 Wistron Corporation
 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C

Title: **23 Display MUX**
 Size: **LA46 MB DIS**
 Date: Tuesday, January 26, 2010 Sheet 23 of 58

LCD/INVERTER/CCD CONN



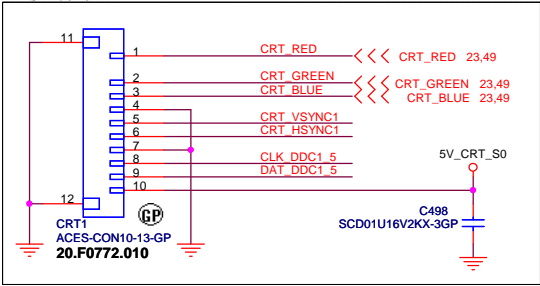
CAMERA POWER



<Core Design>

緯創資通		Wistron Corporation	
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C			
24 LCD & CCD			
Title			
Size	Document Number		
Custom	LA46 MB DIS		
Date:	Tuesday, January 26, 2010	Sheet	24 of 58
			Rev -1

SA-0820 Move pi filter to CRT board.
SA-0823



SB 1024 Add pin to GND (EMI)

CLK_DDC1_5 <<< CLK_DDC1_5 49
DAT_DDC1_5 <<< DAT_DDC1_5 49

CRT_VSYNC1 <<< CRT_VSYNC1 49
CRT_HSYNC1 <<< CRT_HSYNC1 49

L=>B0 -DIS
H=>B1 -UMA

Hsync & Vsync level shift

18,23,24 dGPU_SELECT#>>>

For DIS CRT

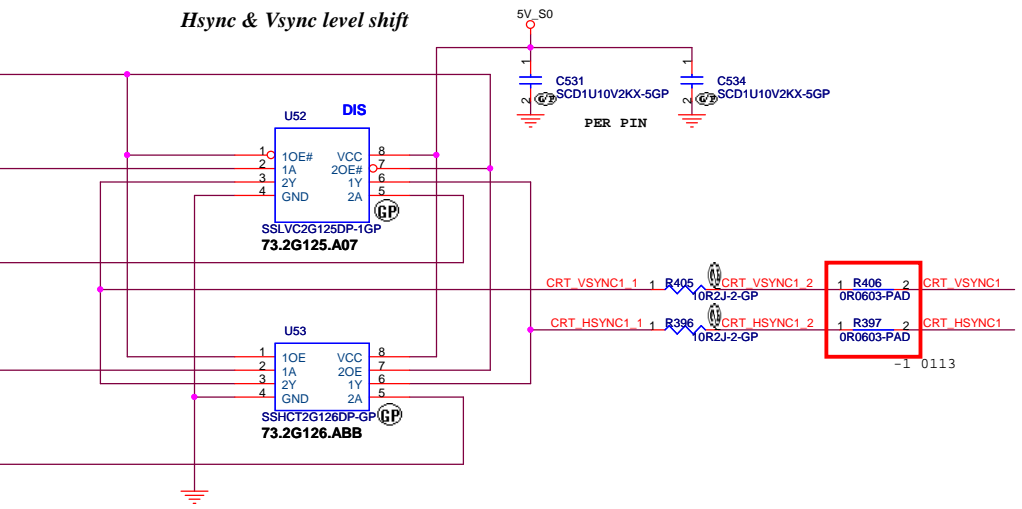
53 NV_CRT_HSYNC >>>

53 NV_CRT_VSYNC >>>

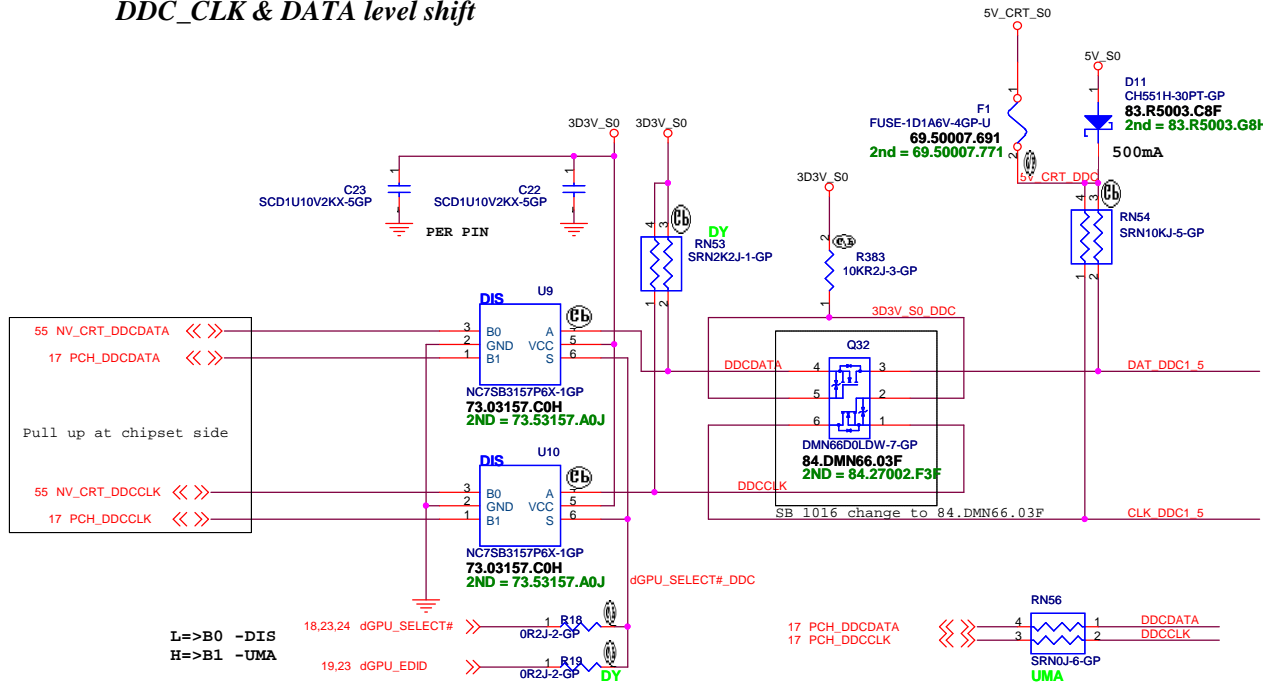
For UMA CRT

17 PCH_HSYNC >>>

17 PCH_VSYNC >>>



DDC_CLK & DATA level shift



L=>B0 -DIS
H=>B1 -UMA

18,23,24 dGPU_SELECT# >>>

19,23 dGPU_EDID >>>

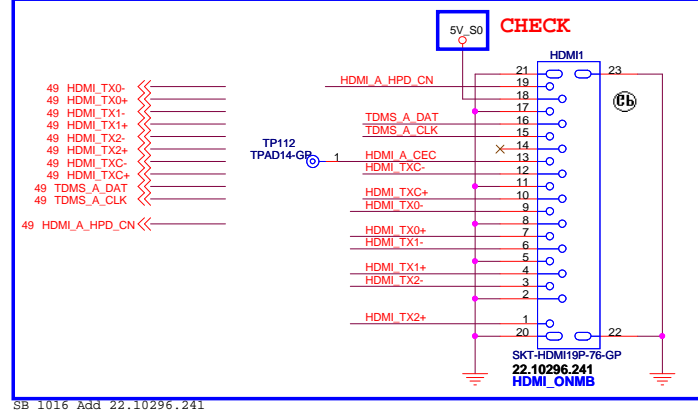
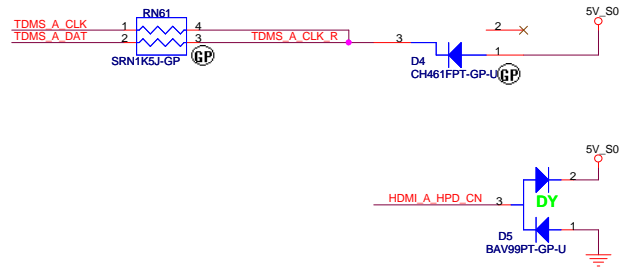
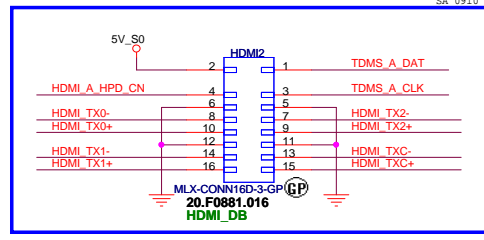
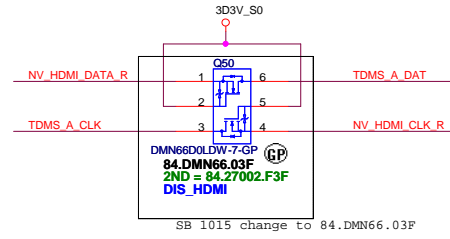
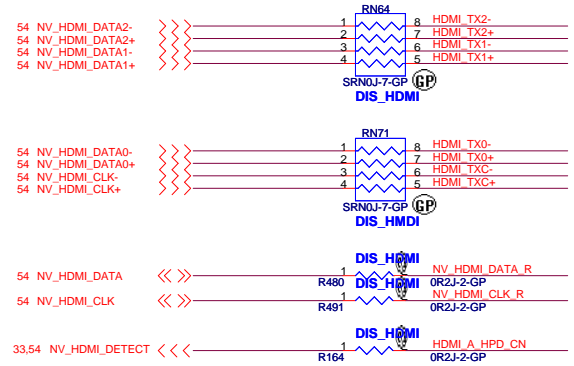
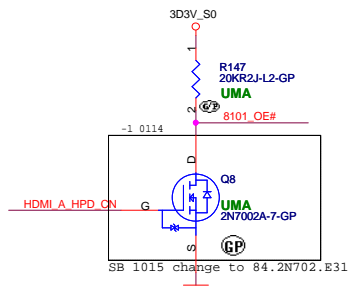
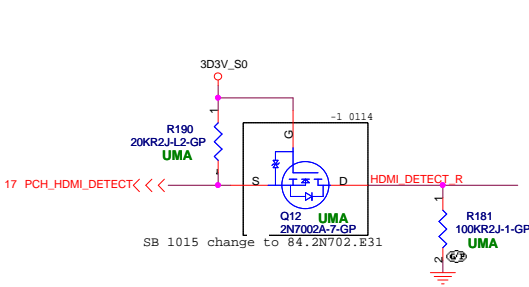
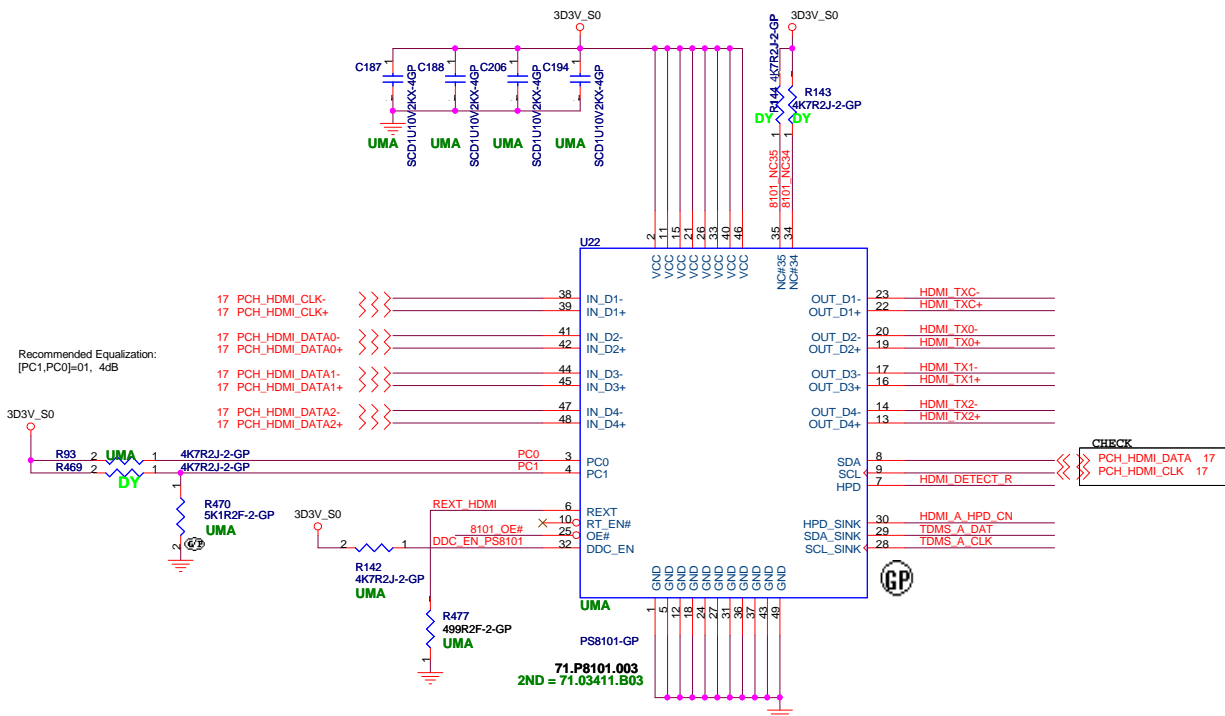
17 PCH_DDCDATA >>>

17 PCH_DDCCLK >>>

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

File	25 CRT	
Size	Document Number	
A3	LA46 MB DIS	
Date:	Tuesday, January 26, 2010	Sheet 25 of 58
Rev	-1	



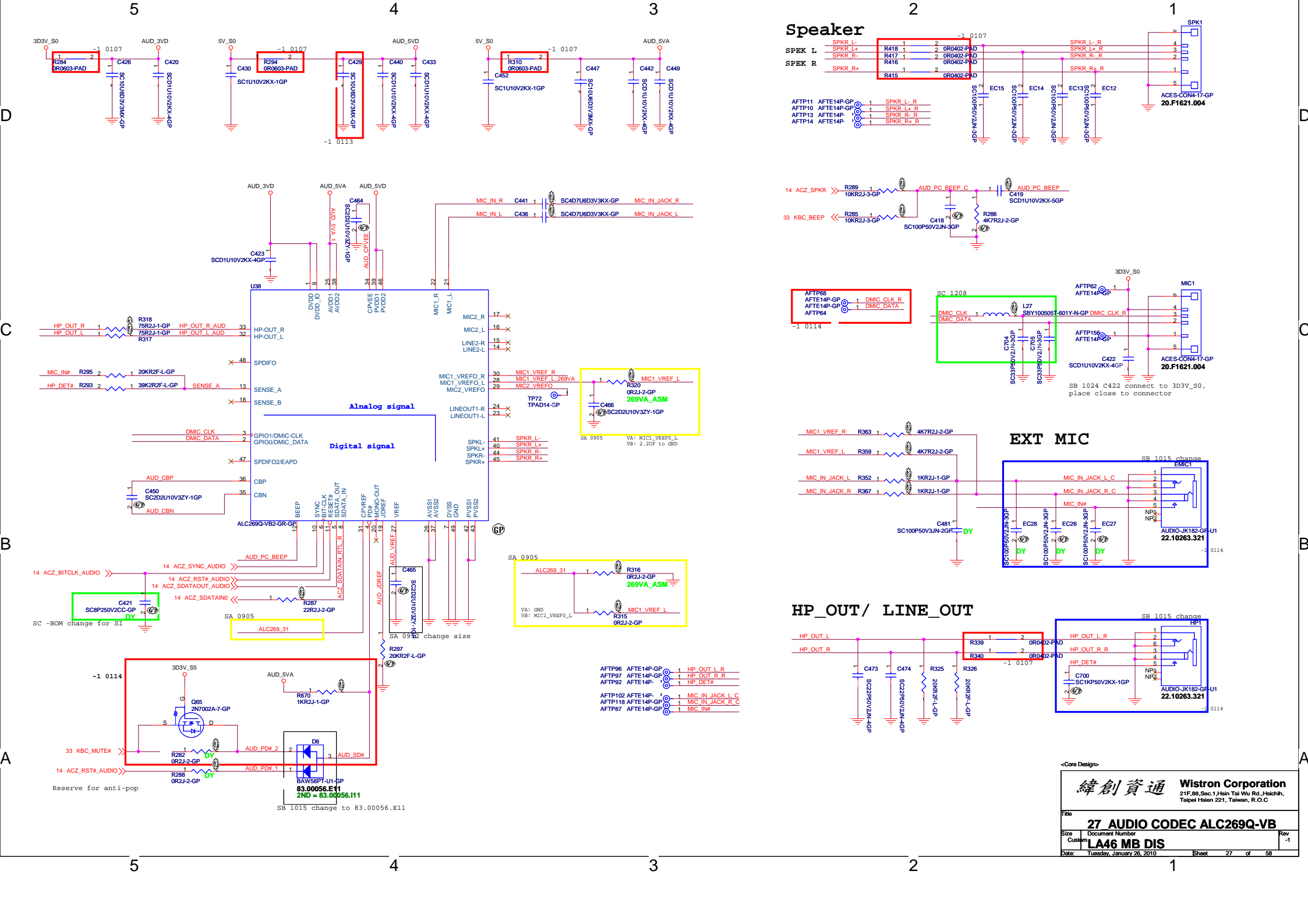
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緯創資通 Wistron Corporation
 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: **26 HDMI**

Size: Custom
 Document Number: **LA46 MB DIS**

Date: Tuesday, January 26, 2010 Sheet 26 of 58



Reserve for anti-pop
 SB 1015 change to 83.00056.E11

- AFTP96 AFTE14P-GP 1 HP_OUT_L_R
- AFTP97 AFTE14P-GP 1 HP_OUT_R_R
- AFTP92 AFTE14P-GP 1 HP_DET#
- AFTP102 AFTE14P-GP 1 MIC_IN_JACK_L_C
- AFTP118 AFTE14P-GP 1 MIC_IN_JACK_R_C
- AFTP87 AFTE14P-GP 1 MIC_IN#

<Core Design>

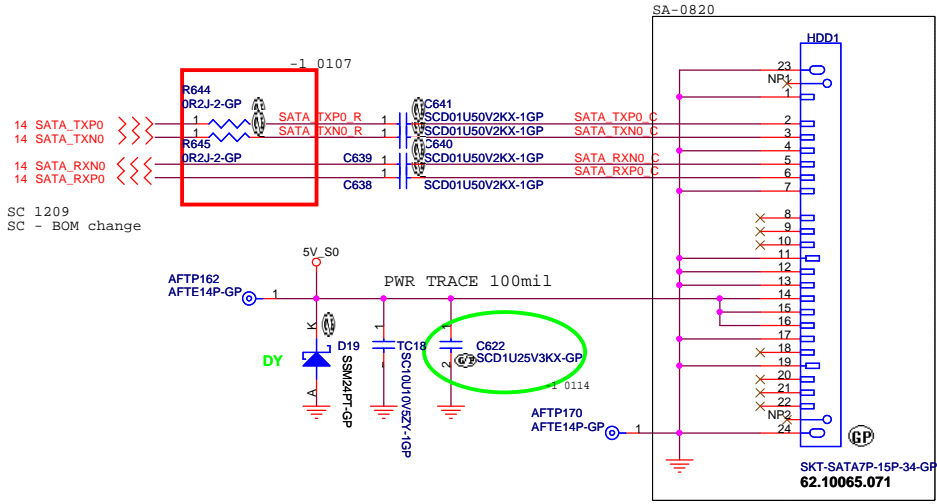
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C

Title: **27 AUDIO CODEC ALC269Q-VB**

Size: Document Number
 Customer: **LA46 MB DIS**

Date: Tuesday, January 26, 2010 Sheet 27 of 58

SATA Connector

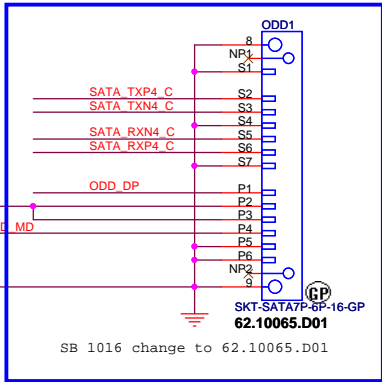
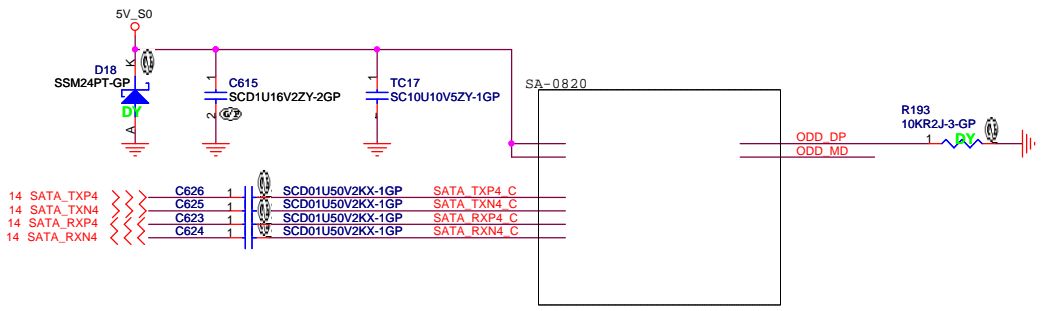


SC 1209
SC - BOM change

AFTP75	AFTE14P-GP	1	SATA TXP0 C
AFTP74	AFTE14P-GP	1	SATA TXN0 C
AFTP73	AFTE14P-GP	1	SATA RXN0 C
AFTP72	AFTE14P-GP	1	SATA RXP0 C

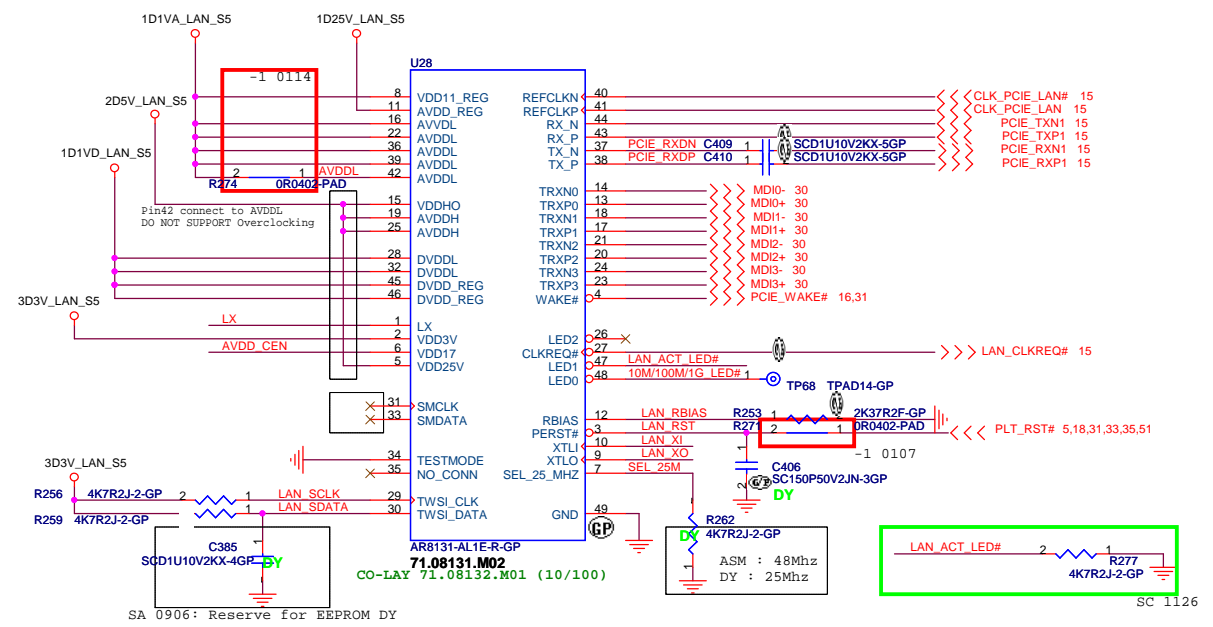
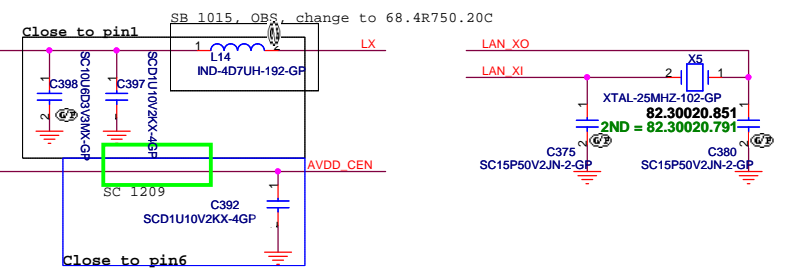
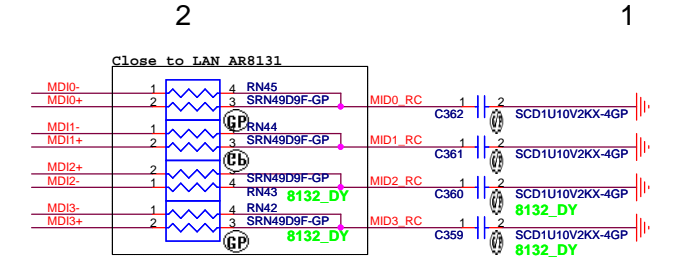
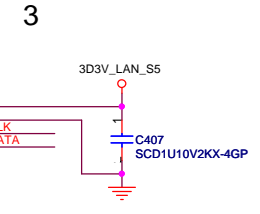
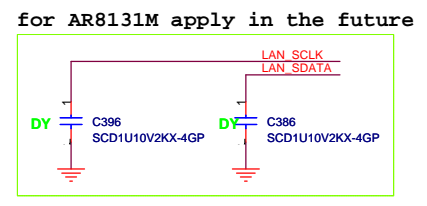
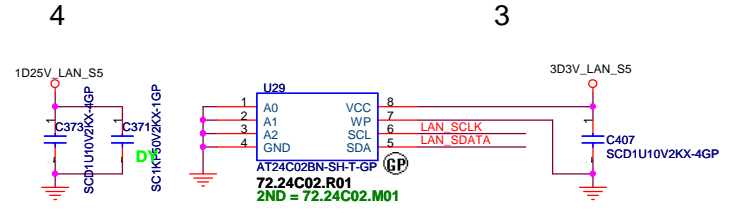
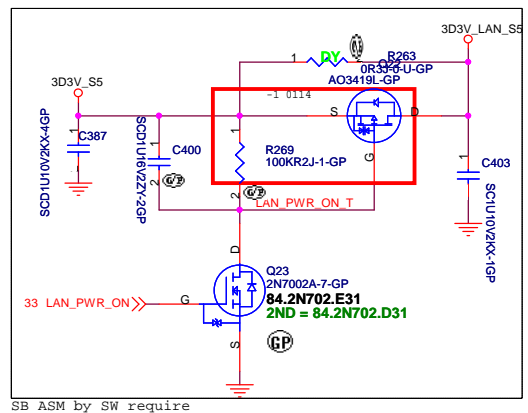
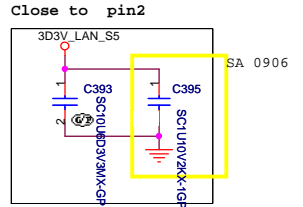
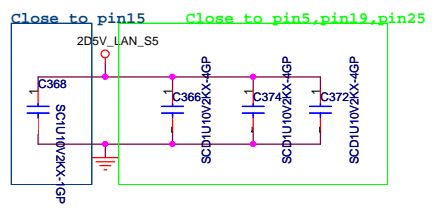
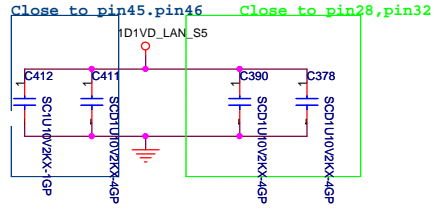
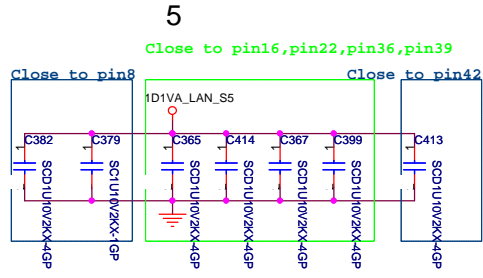
SB 1015 Add AF E

ODD Connector

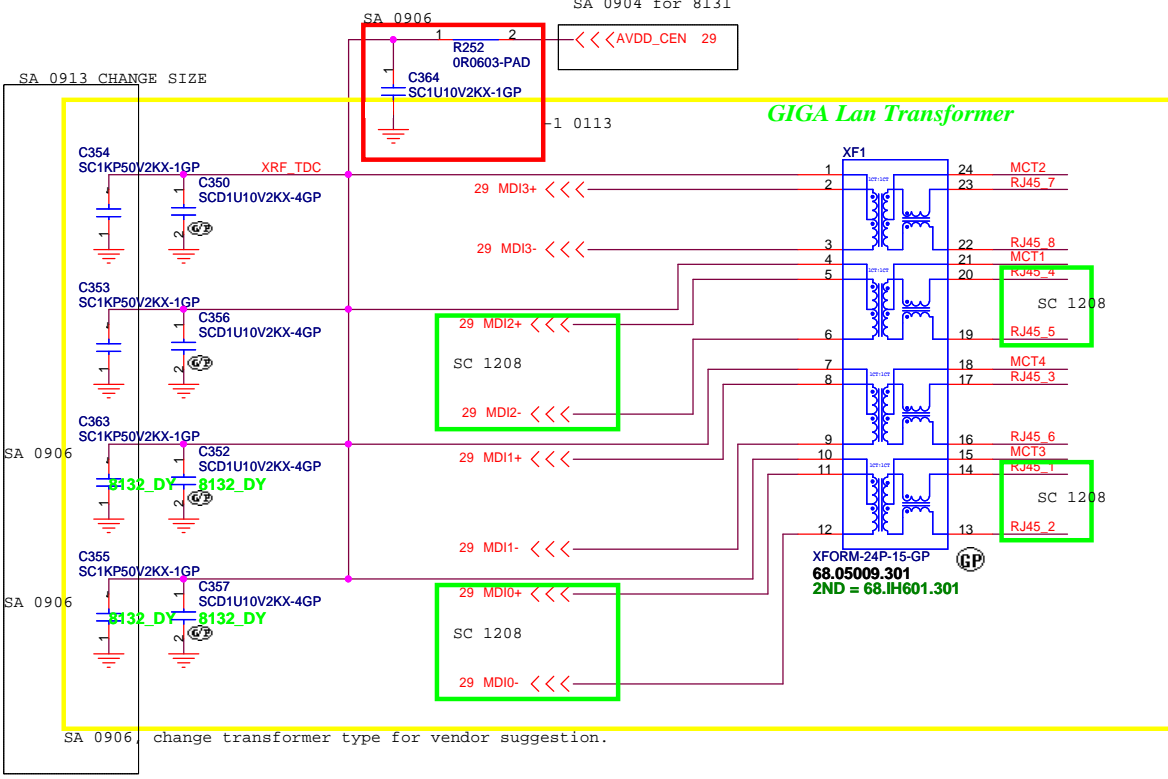


SB 1016 change to 62.10065.D01

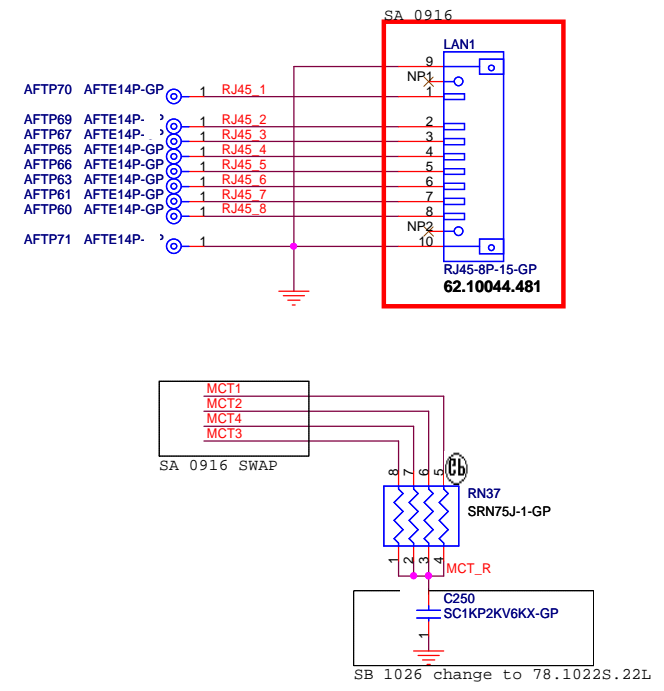
AFTP163	AFTE14P-GP	1	SATA TXP4 C
AFTP161	AFTE14P-GP	1	SATA TXN4 C
AFTP159	AFTE14P-GP	1	SATA RXP4 C
AFTP160	AFTE14P-GP	1	SATA RXN4 C



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

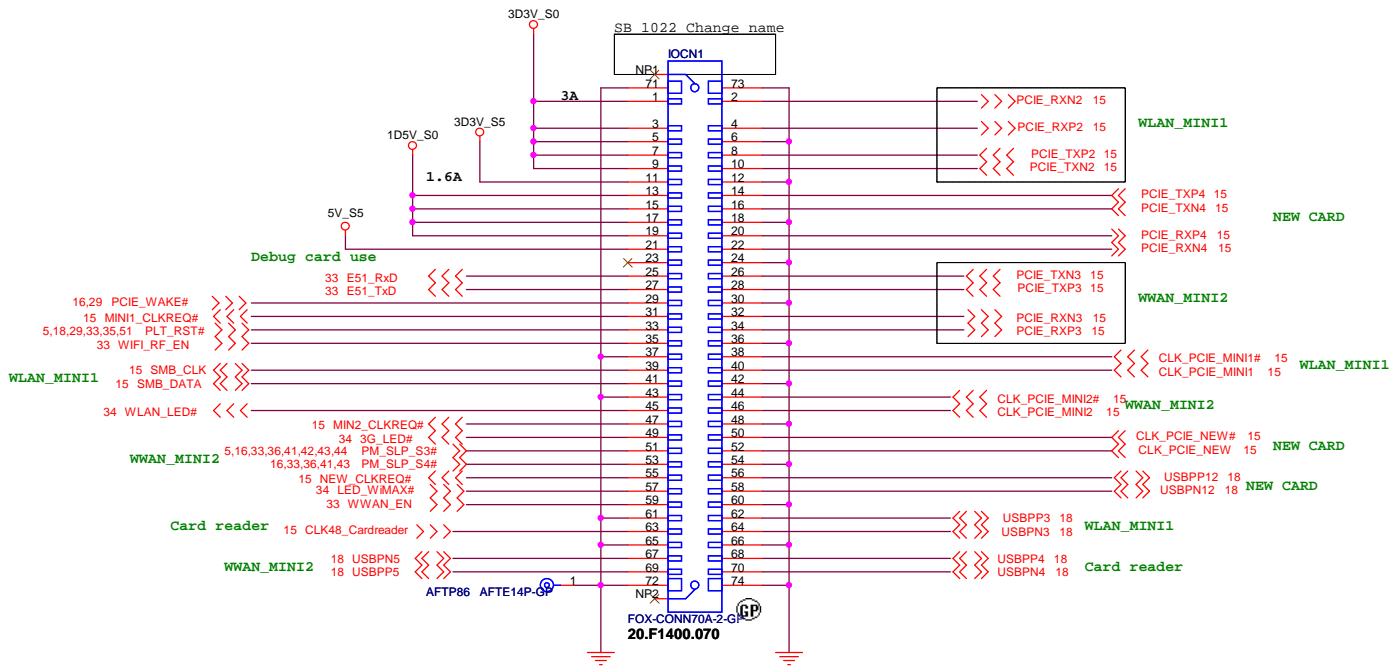


LAN Connector



<Core Design>

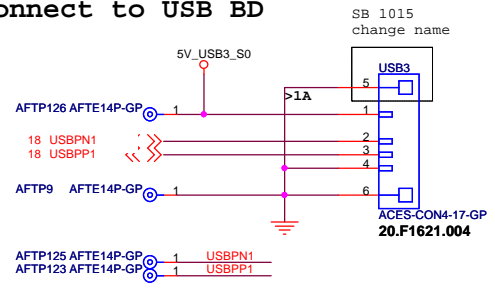
緯創資通		Wistron Corporation	
		21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title			
30 LAN CONN			
Size	Document Number	Rev	
Custom	LA46 MB DIS	-1	
Date:	Tuesday, January 26, 2010	Sheet	30 of 58



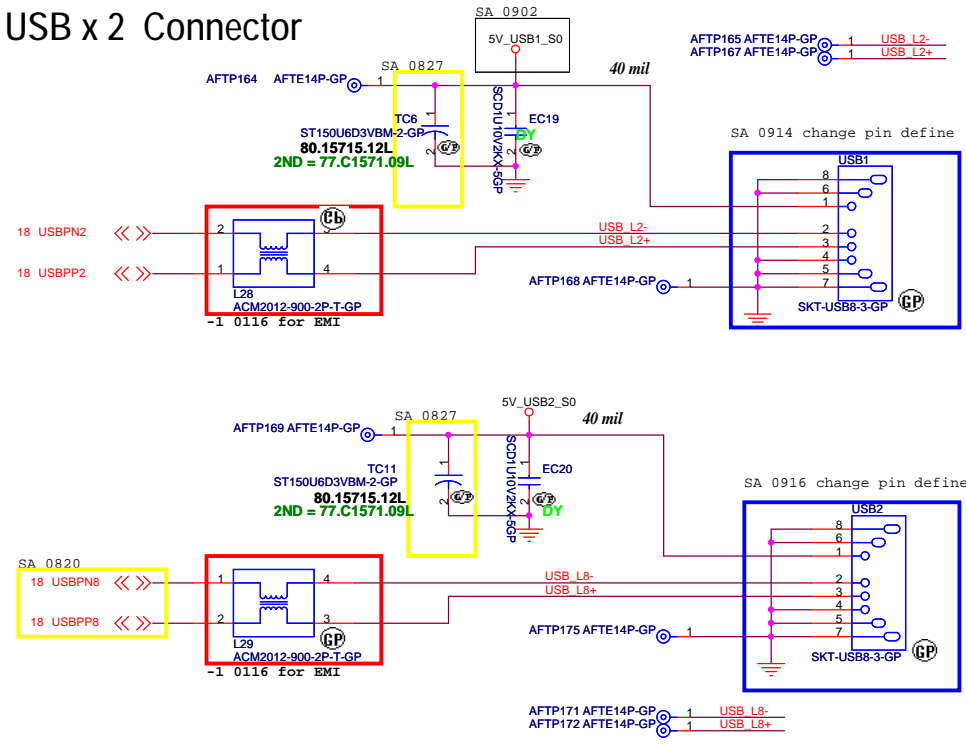
- AFTP107 AFTE14P-GP 1 3D3V_S0
- AFTP103 AFTE14P 1 3D3V_S5
- AFTP104 AFTE14P-GP 1 1D5V_S0
- AFTP99 AFTE14P 1 5V_S5
- AFTP98 AFTE14P-GP 1 E51_RxD
- AFTP93 AFTE14P-GP 1 E51_TxD
- AFTP91 AFTE14P 1 PCIE_WAKE#
- AFTP84 AFTE14P 1 MINI_CLKREQ#
- AFTP190 AFTE14P-GP 1 CLK_PCIE_MINI1#
- AFTP188 AFTE14P 1 CLK_PCIE_MINI1
- AFTP109 AFTE14P 1 PCIE_RXN2
- AFTP108 AFTE14P 1 PCIE_RXP2
- AFTP105 AFTE14P 1 PCIE_TXN2
- AFTP106 AFTE14P-GP 1 PCIE_TXP2
- AFTP185 AFTE14P 1 PLT_RST#
- AFTP184 AFTE14P 1 WIFI_RF_EN
- AFTP182 AFTE14P-GP 1 SMB_CLK
- AFTP181 AFTE14P 1 SMB_DATA
- AFTP180 AFTE14P 1 WLAN_LED#
- AFTP178 AFTE14P 1 MIN2_CLKREQ#
- AFTP187 AFTE14P 1 USBPN3
- AFTP189 AFTE14P-GP 1 USBPP3
- AFTP177 AFTE14P 1 CLK_PCIE_MINI2#
- AFTP179 AFTE14P 1 CLK_PCIE_MINI2
- AFTP194 AFTE14P-GP 1 USBPP4
- AFTP193 AFTE14P-GP 1 USBPN4
- AFTP176 AFTE14P-GP 1 CLK48_Cardreader
- AFTP101 AFTE14P-GP 1 PCIE_TXP4
- AFTP100 AFTE14P 1 PCIE_TXN4
- AFTP95 AFTE14P 1 PCIE_RXP4
- AFTP94 AFTE14P-GP 1 PCIE_RXN4
- AFTP174 AFTE14P-GP 1 CLK_PCIE_NEW
- AFTP173 AFTE14P 1 CLK_PCIE_NEW#
- AFTP80 AFTE14P 1 USBPP12
- AFTP79 AFTE14P 1 USBPN12
- AFTP81 AFTE14P-GP 1 3G_LED#
- AFTP78 AFTE14P 1 PM_SLP_S3#
- AFTP82 AFTE14P 1 PM_SLP_S4#
- AFTP83 AFTE14P 1 NEW_CLKREQ#
- AFTP89 AFTE14P 1 PCIE_TXN3
- AFTP88 AFTE14P-GP 1 PCIE_TXP3
- AFTP90 AFTE14P 1 PCIE_RXN3
- AFTP85 AFTE14P 1 PCIE_RXP3
- AFTP192 AFTE14P 1 USBPN5
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- AFTP76 AFTE14P 1 WWAN_EN

USB3

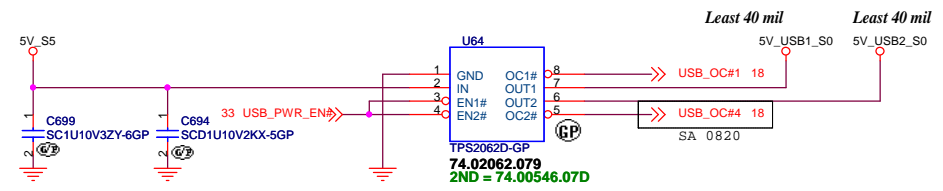
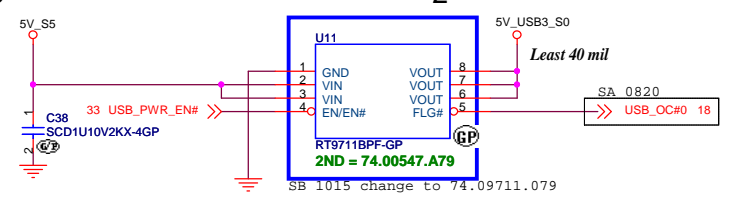
Connect to USB BD



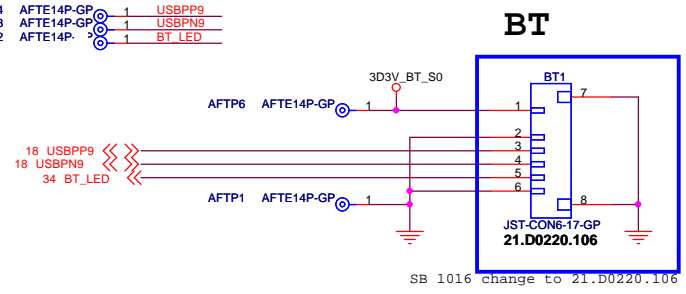
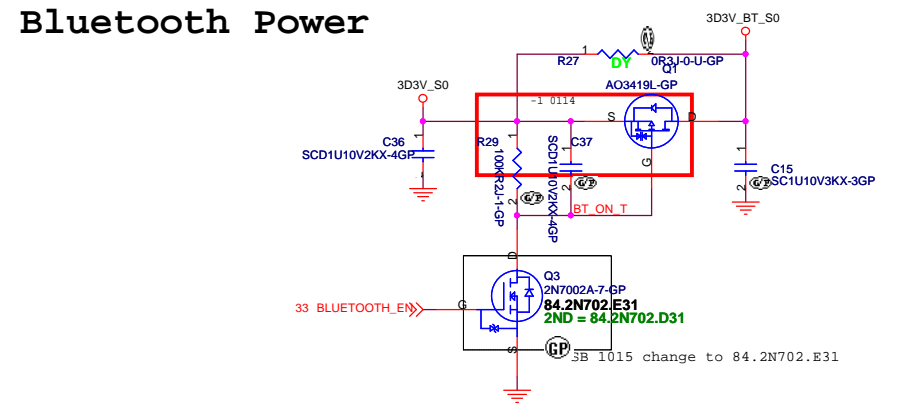
USB x 2 Connector



3



Bluetooth Power

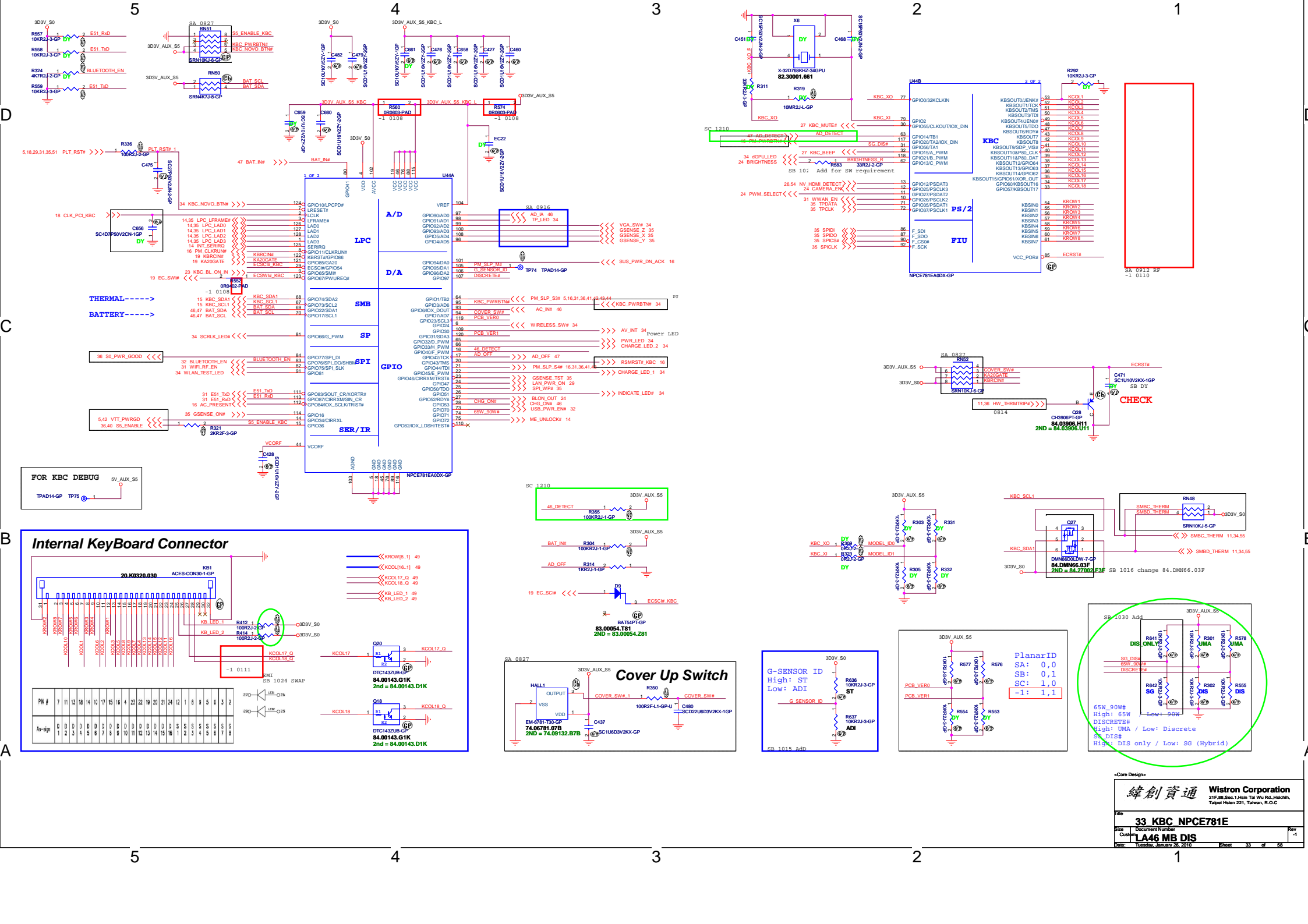


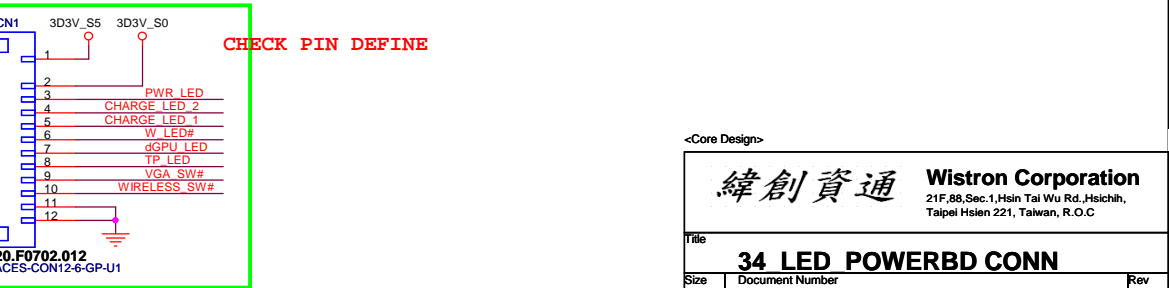
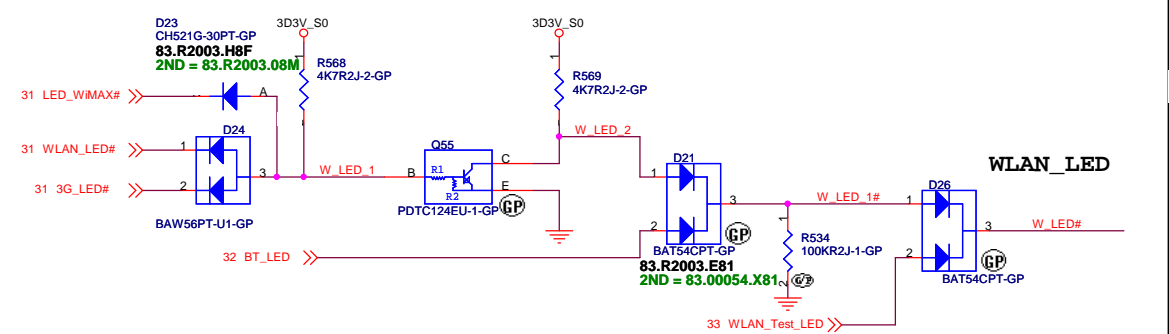
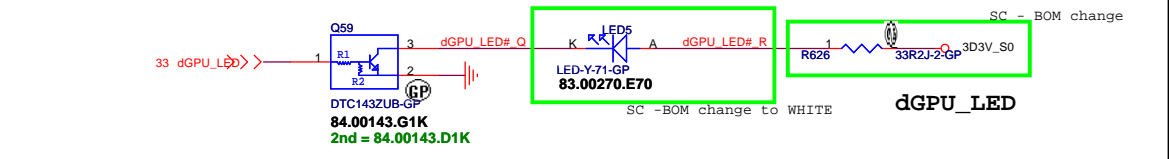
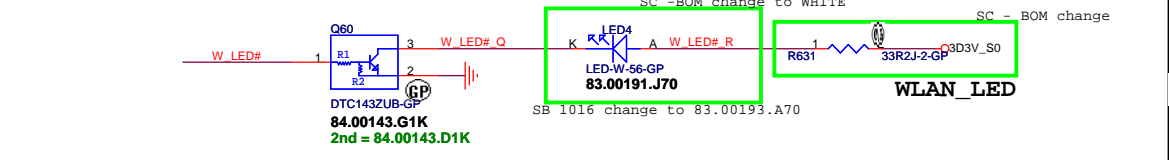
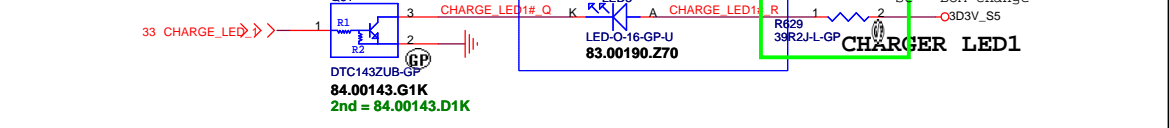
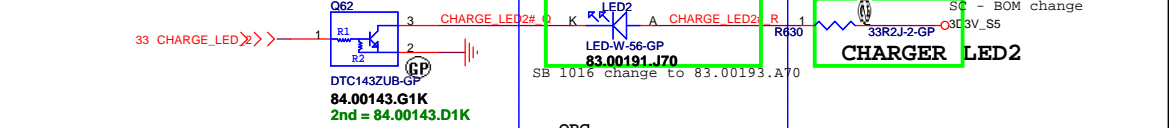
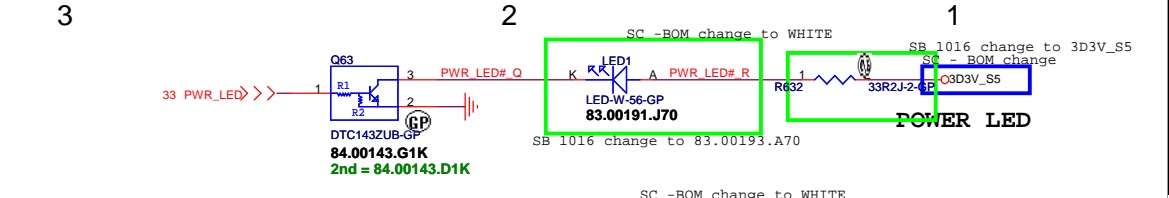
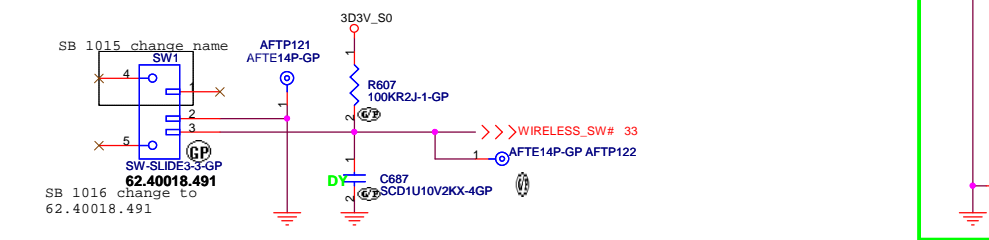
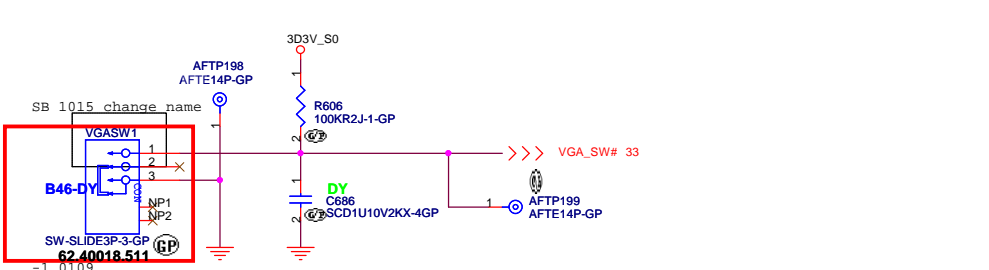
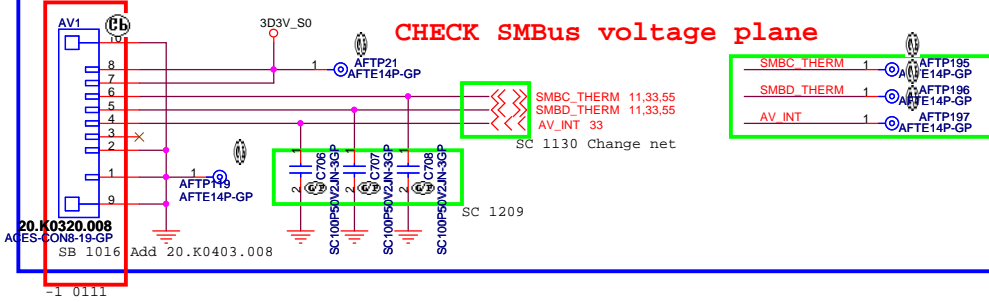
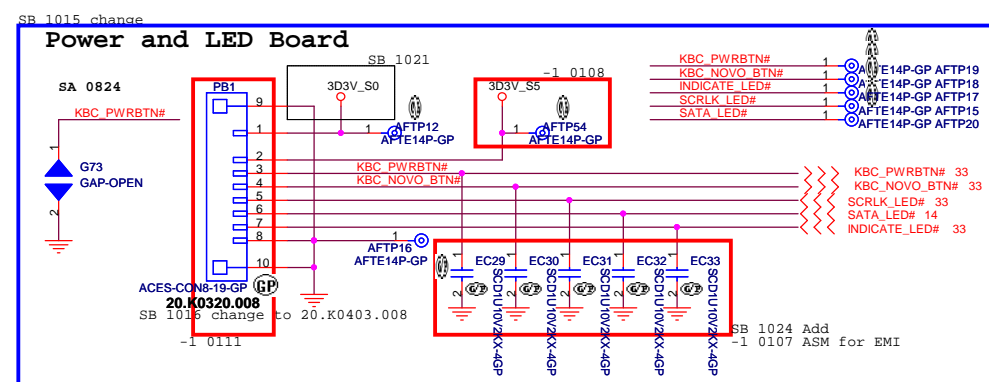
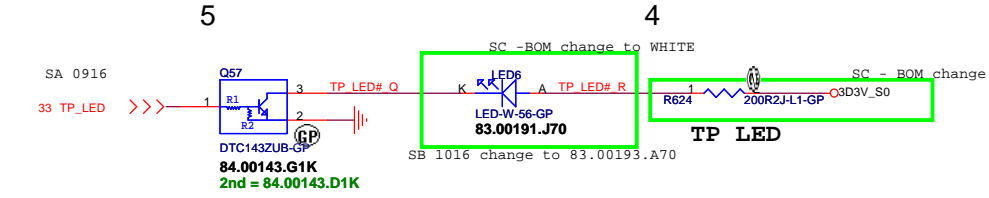
Pin	Pin Name
1	V3V3
2	GND
3	USB D+
4	USB D-
5	LINK_IND

<Core Design>

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File: **32 USB & BT**
 Size: A3 Document Number: **LA46 MB DIS**
 Date: Tuesday, January 26, 2010 Sheet 32 of 58 Rev -1



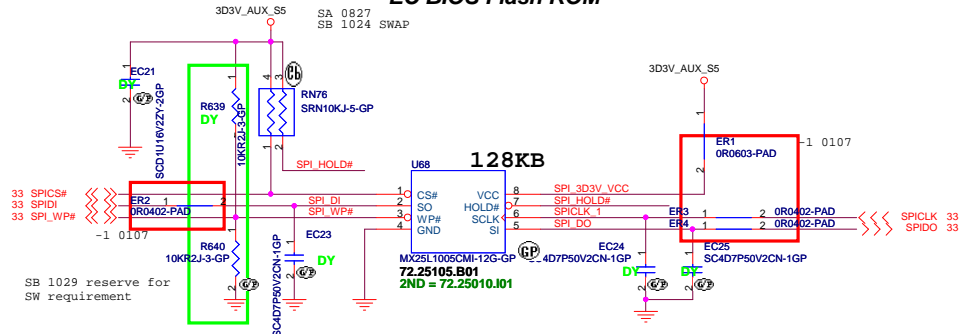


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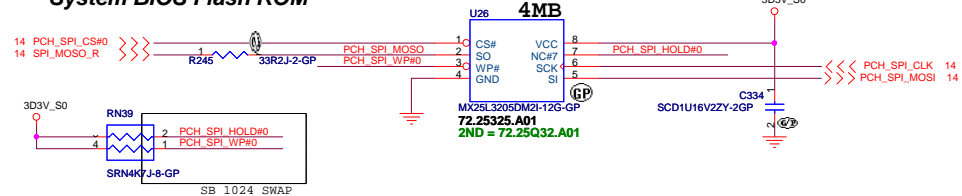
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C

File	34 LED POWERBD CONN	
Size	Document Number	Rev
A3	LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet 34 of 58

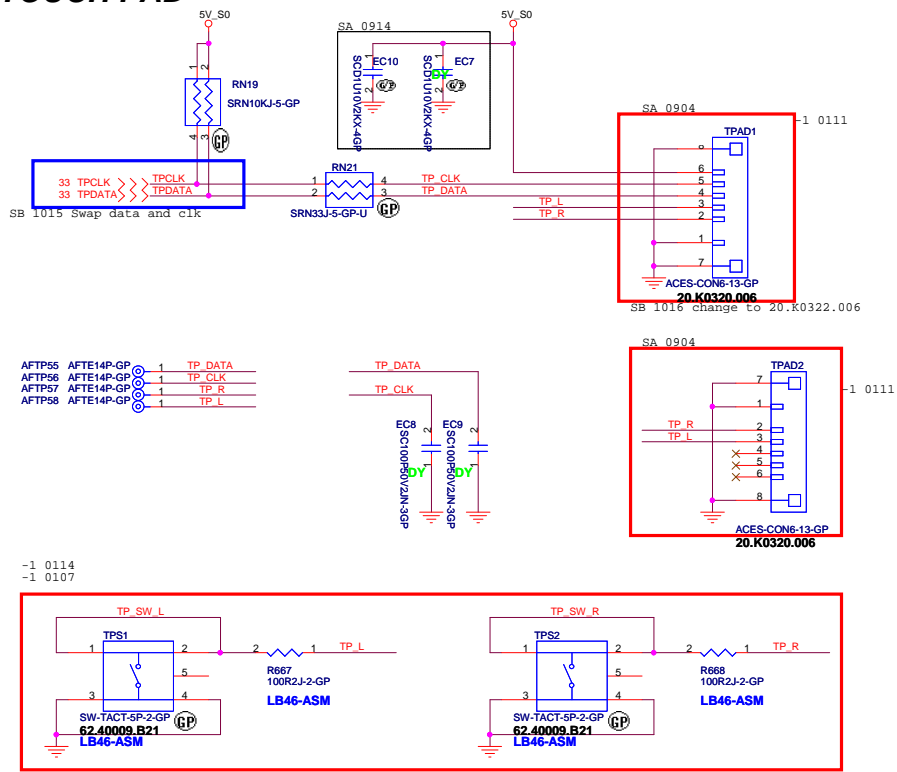
EC BIOS Flash ROM



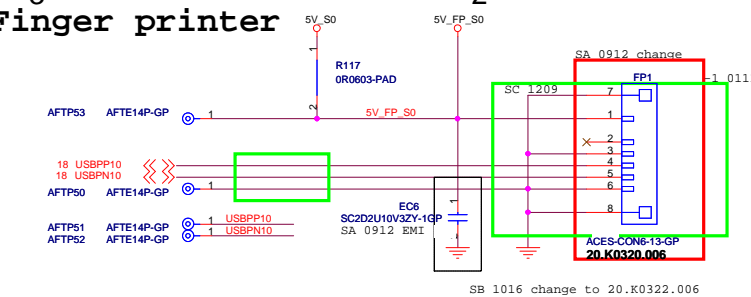
System BIOS Flash ROM



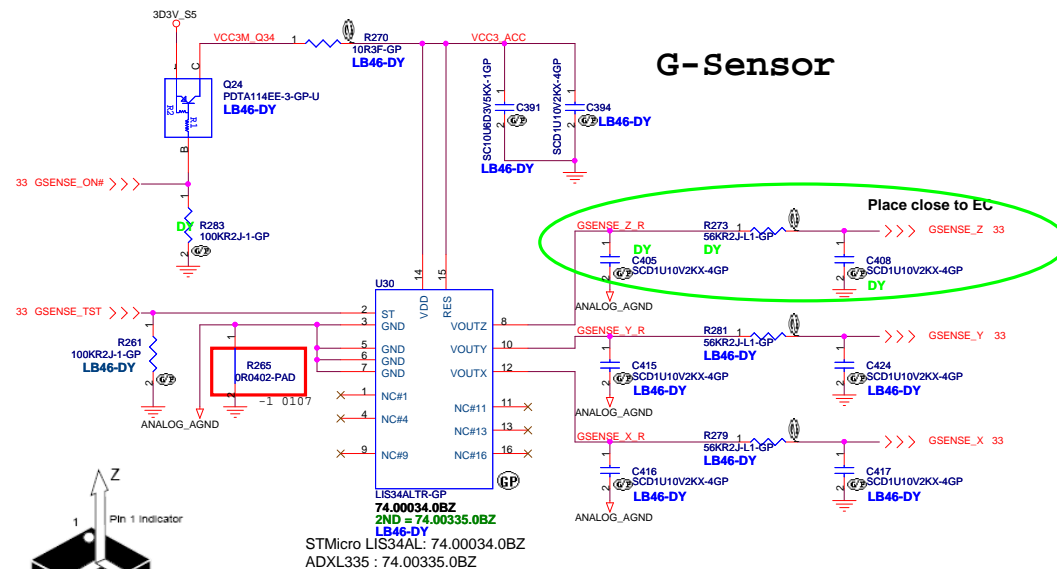
TOUCH PAD



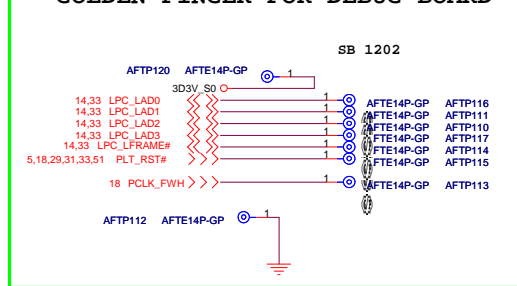
Finger printer

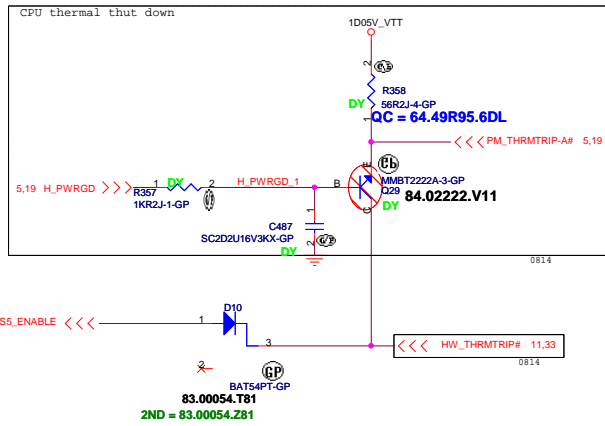


G-Sensor

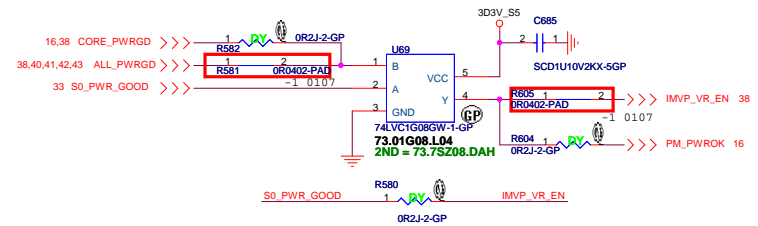
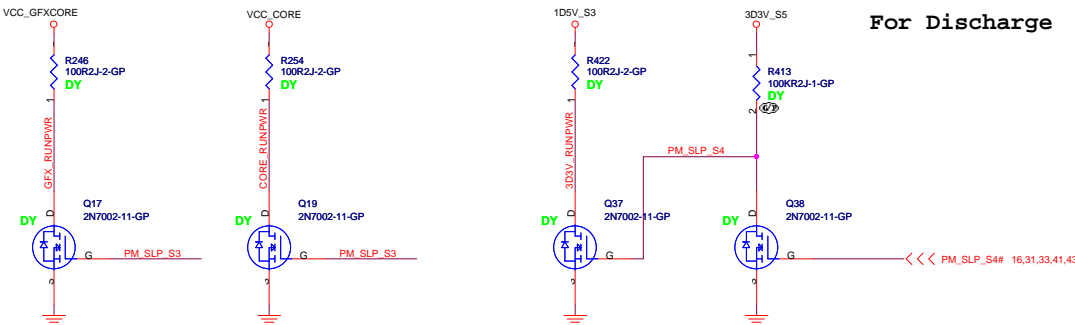
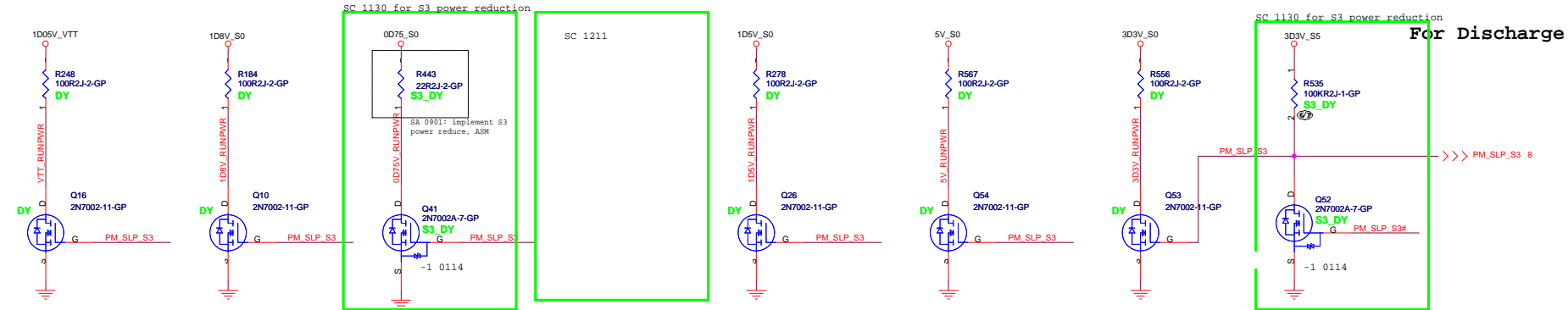
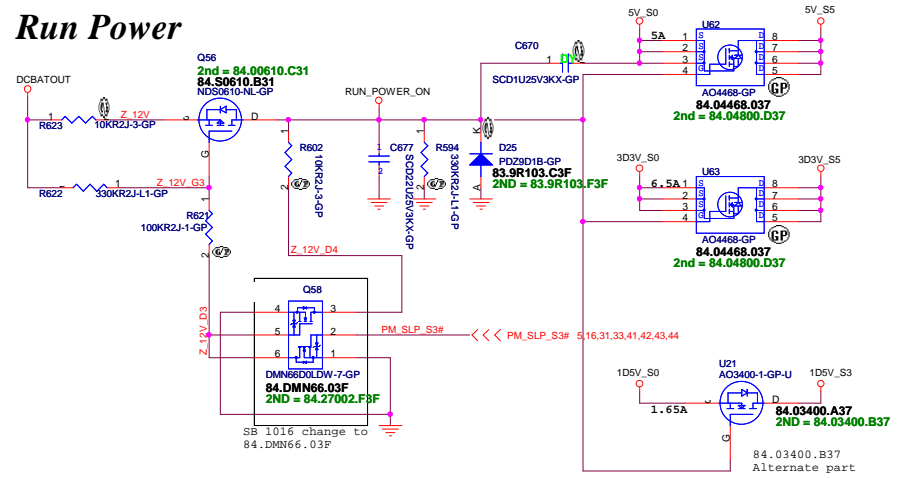


GOLDEN FINGER FOR DEBUG BOARD





Run Power



<p>Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C</p>	
<p>36 Run PWR</p>	
<p>Size: 11.5x17.5</p>	<p>Document Number: LA46 MB DIS</p>
<p>Date: Tuesday, January 26, 2010</p>	<p>Sheet 36 of 58</p>

5

4

3

2

1

D

D

C

C

B

B

A

A

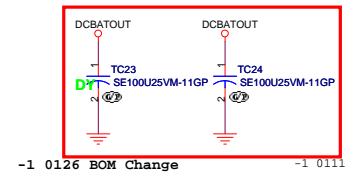
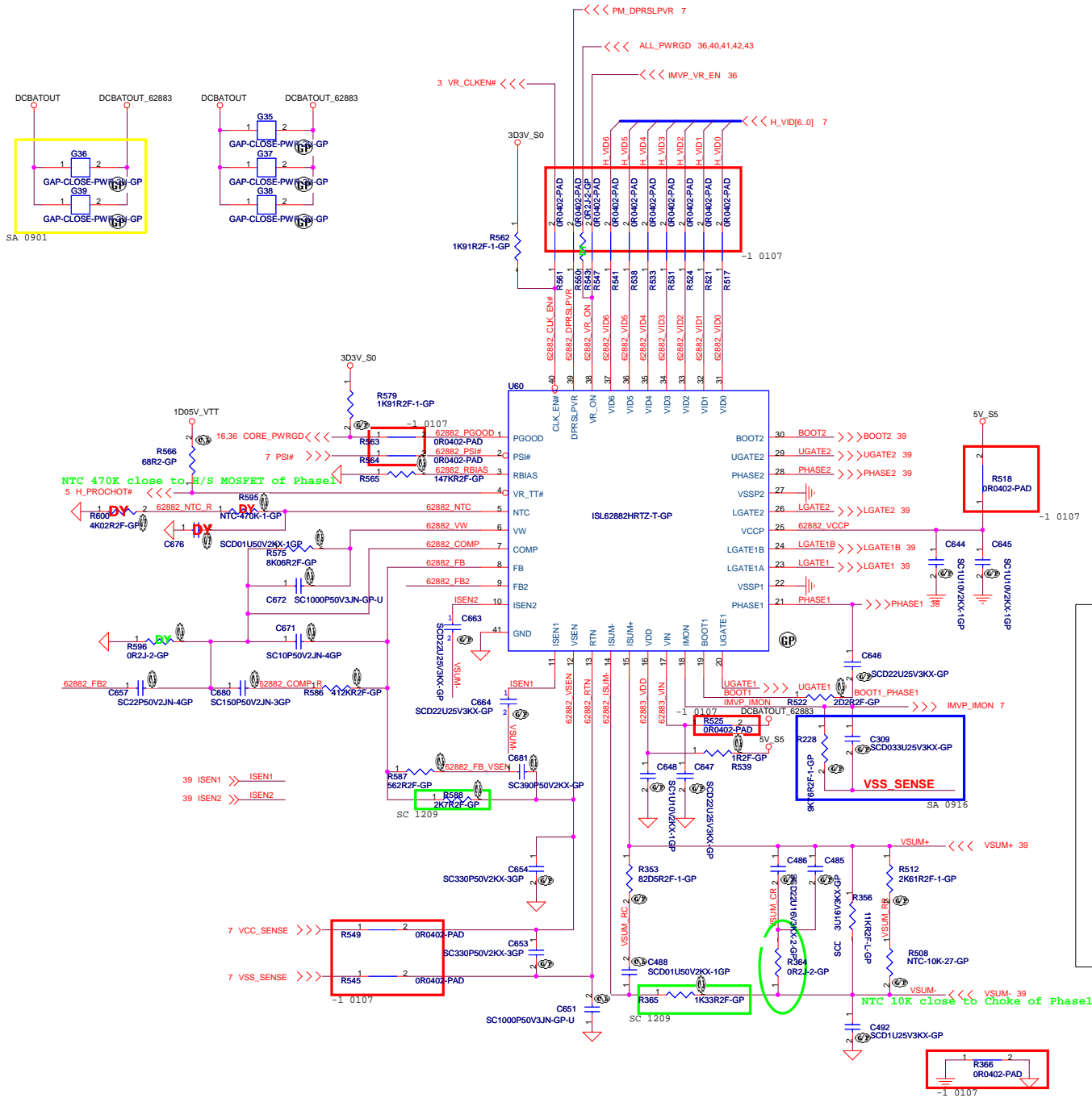
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緯創資通 **Wistron Corporation**
 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C

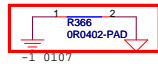
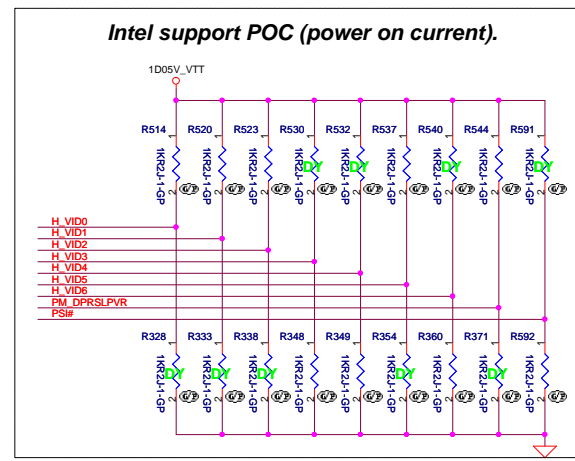
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37 BLANK		

Size	Document Number	Rev
A3	LA46 MB	SA

Date: Tuesday, January 26, 2010	Sheet 37 of 58
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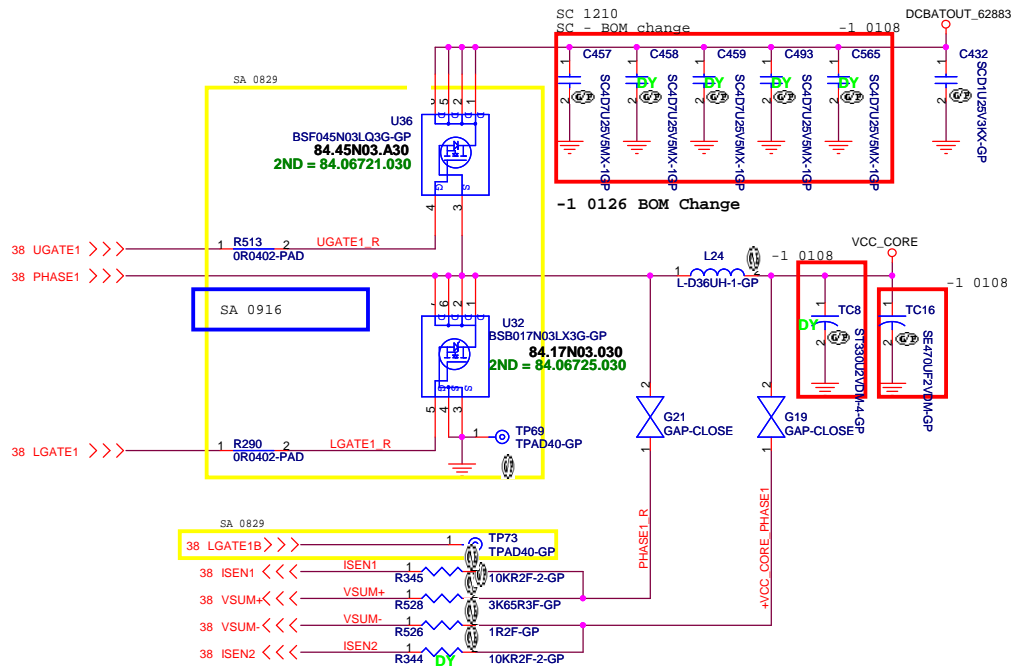
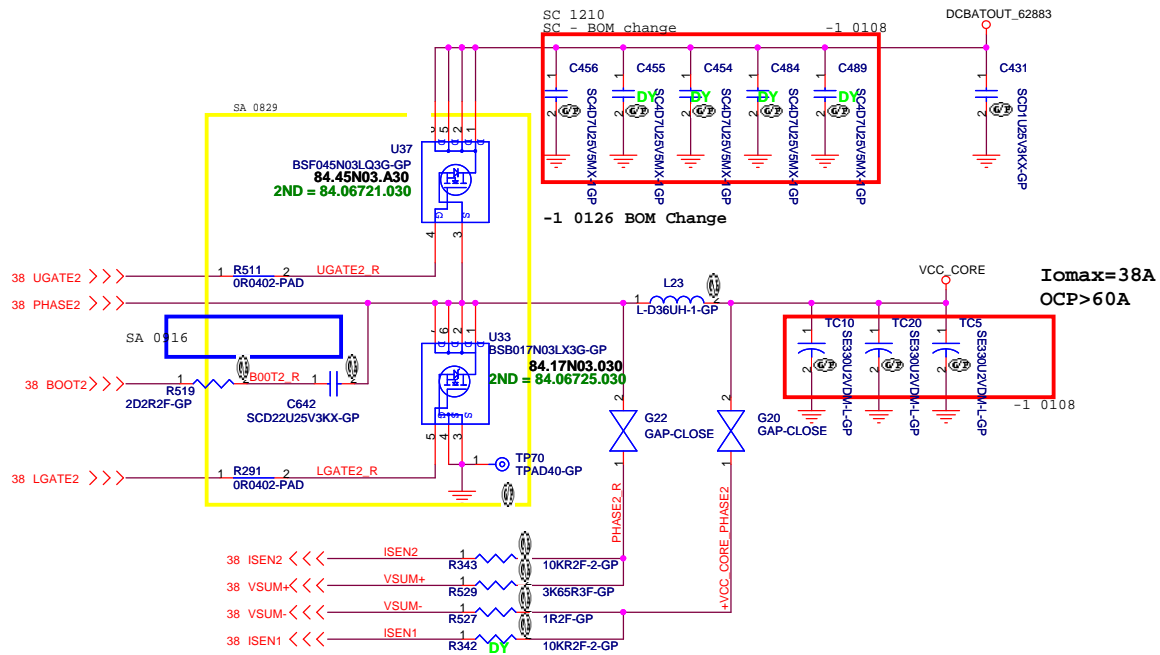


-1 0126 BOM Change -1 0111



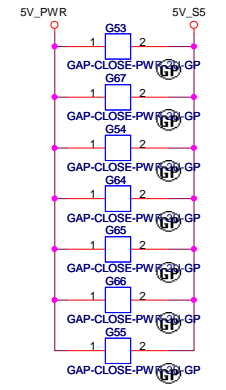
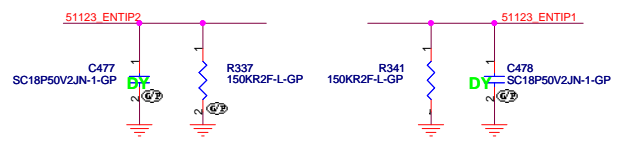
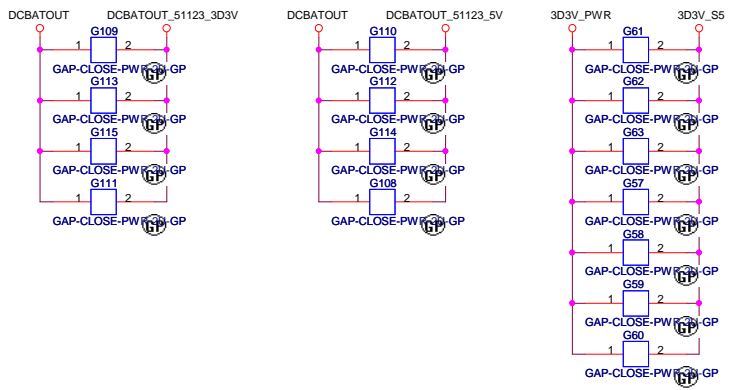
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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C

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Size	Document Number	LA46 MB DIS	
Custom	Rev	-1	
Date	Wednesday, January 27, 2010	Sheet	38 of 58

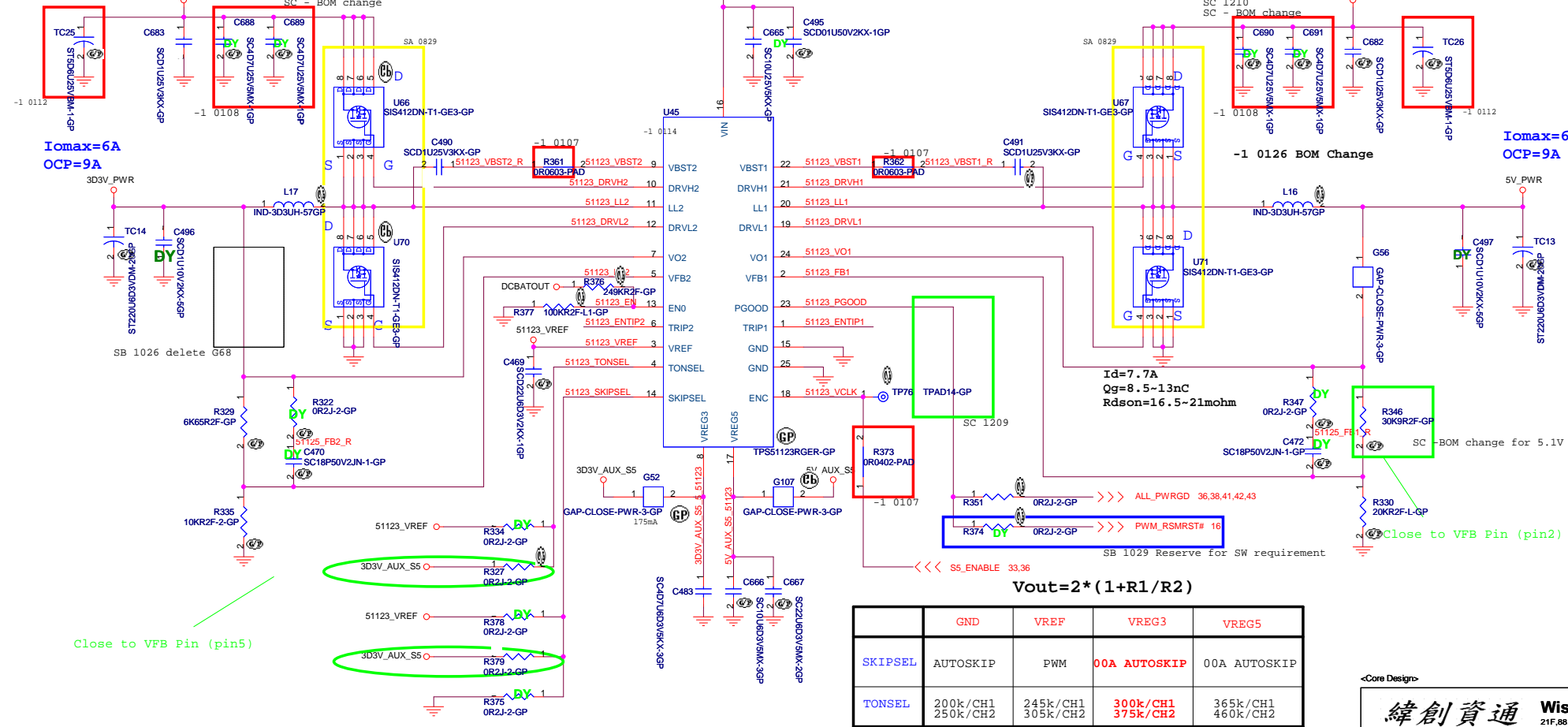


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緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
File	39 ISL62882 CPU CORE (2 of 2)		
Size	Document Number		
A3	LA46 MB DIS		
Date:	Wednesday, January 27, 2010	Sheet	39 of 58
			Rev -1



-1 0126 BOM Change



I_{omax}=6A
OCp=9A

I_{omax}=6A
OCp=9A

I_d=7.7A
Q_g=8.5-13nC
R_{dson}=16.5-21mohm

$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

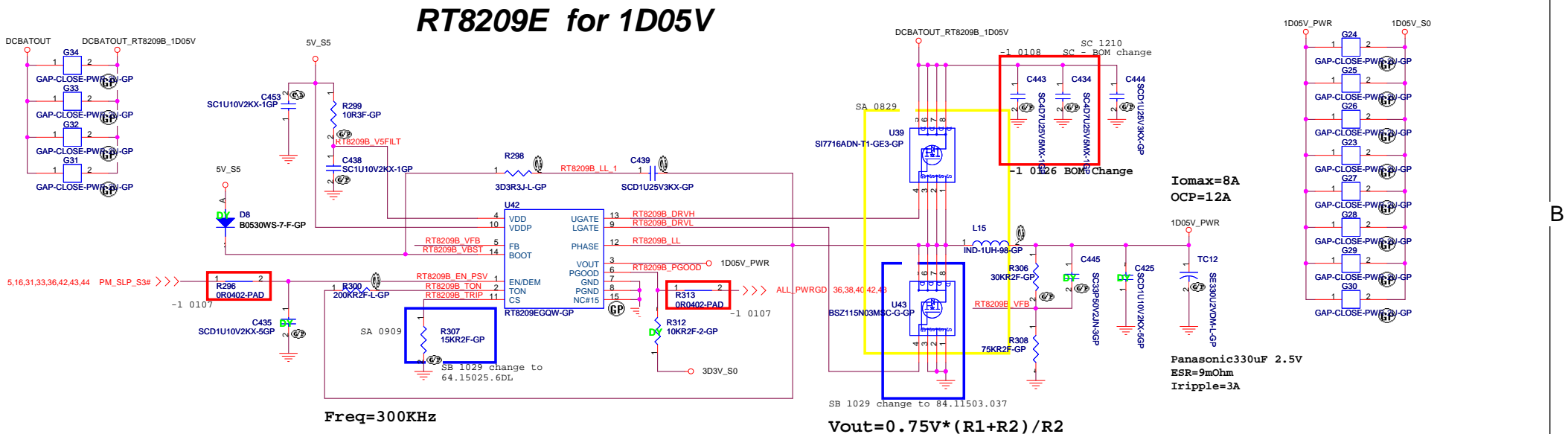
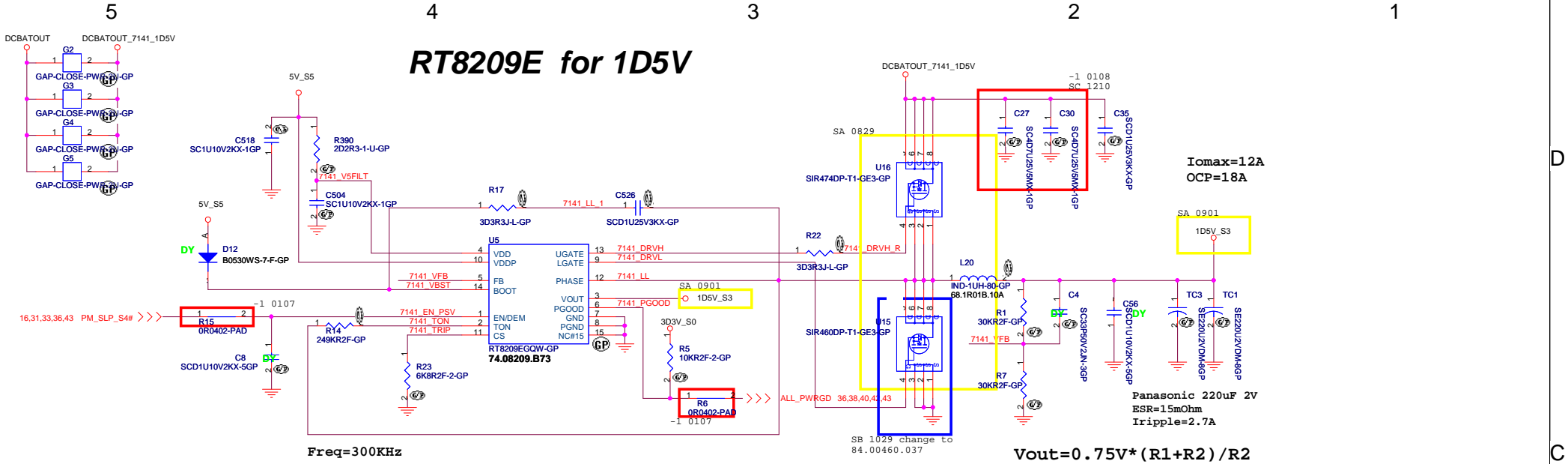
Close to VFB Pin (pin5)

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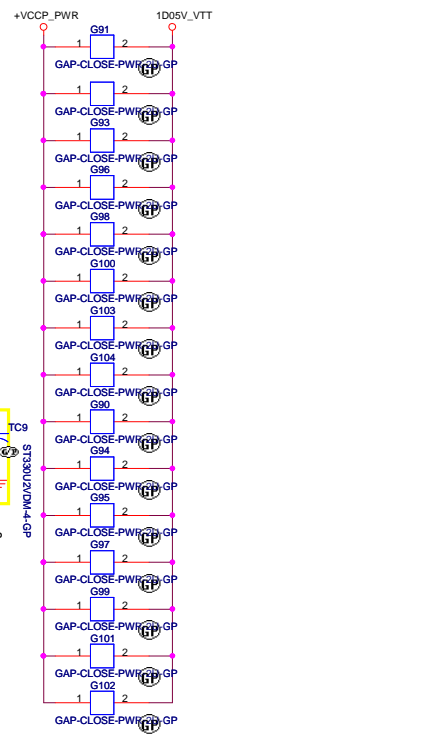
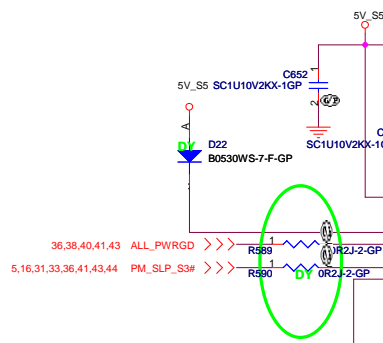
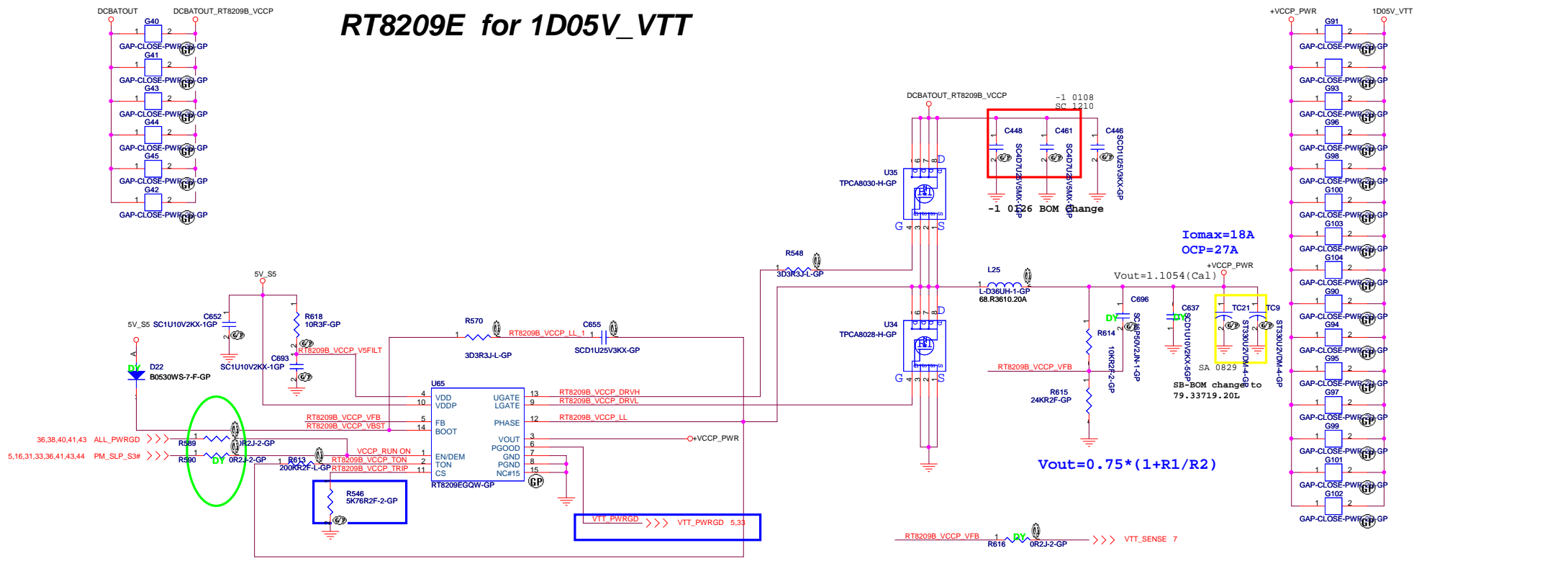
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Title: **40 TPS51123 5V/3D3V**
Document Number: **LA46 MB DIS**

Size: **LA46 MB DIS**
Date: Wednesday, January 27, 2010 Sheet 40 of 58



RT8209E for 1D05V_VTT



<Core Design>

緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C

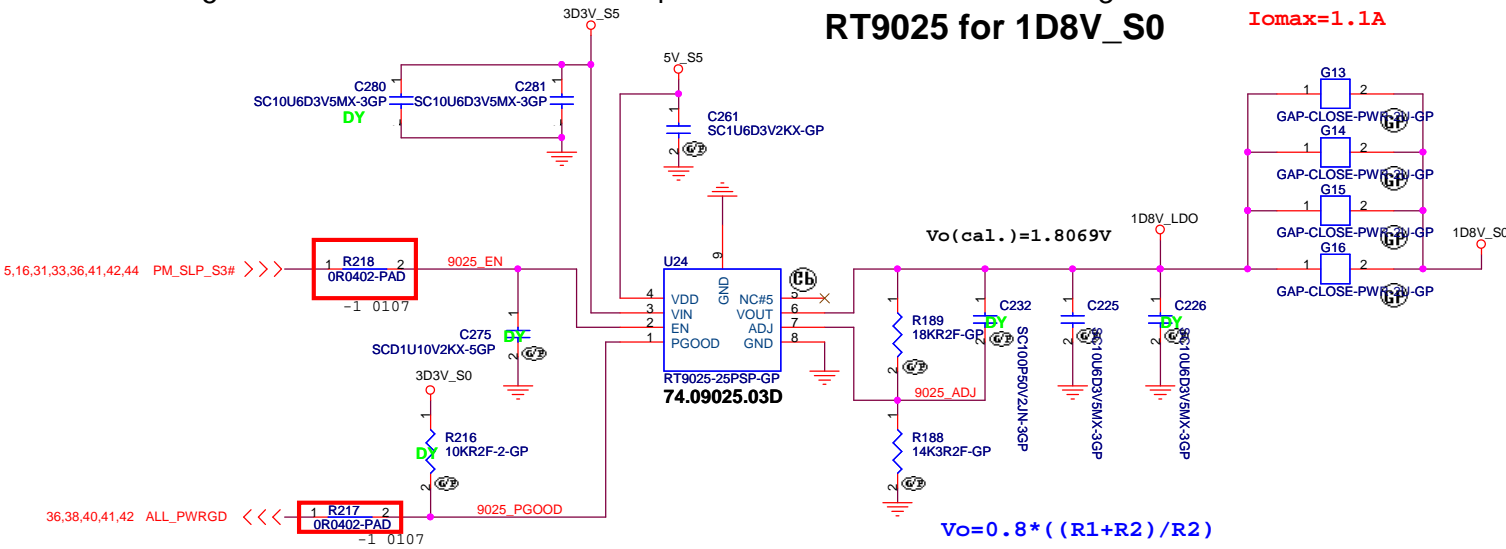
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Size	Document Number	Rev
Custom	LA46 MB DIS	-1

Date: Wednesday, January 27, 2010 Sheet 42 of 58

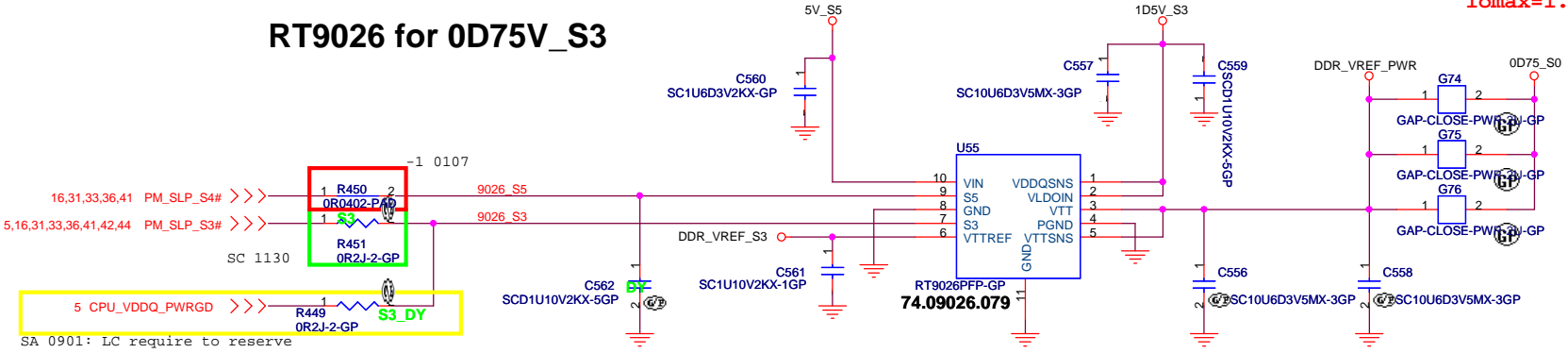
RT9025 for 1D8V_S0

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RT9026 for 0D75V_S3

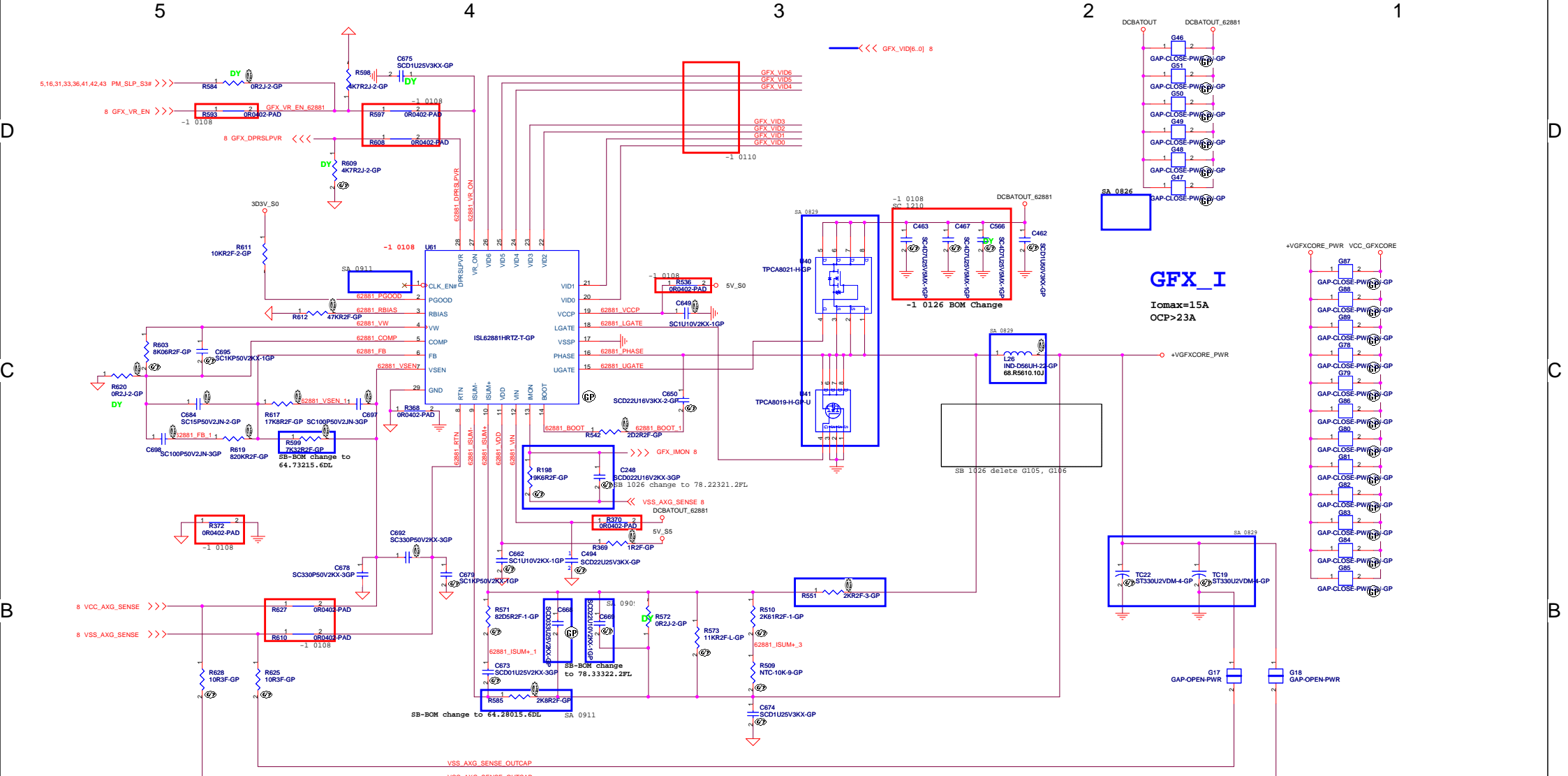
Iomax=1.2A



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Taipei Hsien 221, Taiwan, R.O.C

Title		
43 RT9025 1D8V/ RT9026 0D75		
Size	Document Number	Rev
Custom	LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet 43 of 58



GFX_I
 Iomax=1.5A
 OCR>2.3A

<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	44 ISL62881 +VCC GFXCORE		
Size	Document Number	Rev	
Customer	LA46 MB DIS	-1	
Date	Wednesday, January 27, 2010	Sheet	44 of 58

5

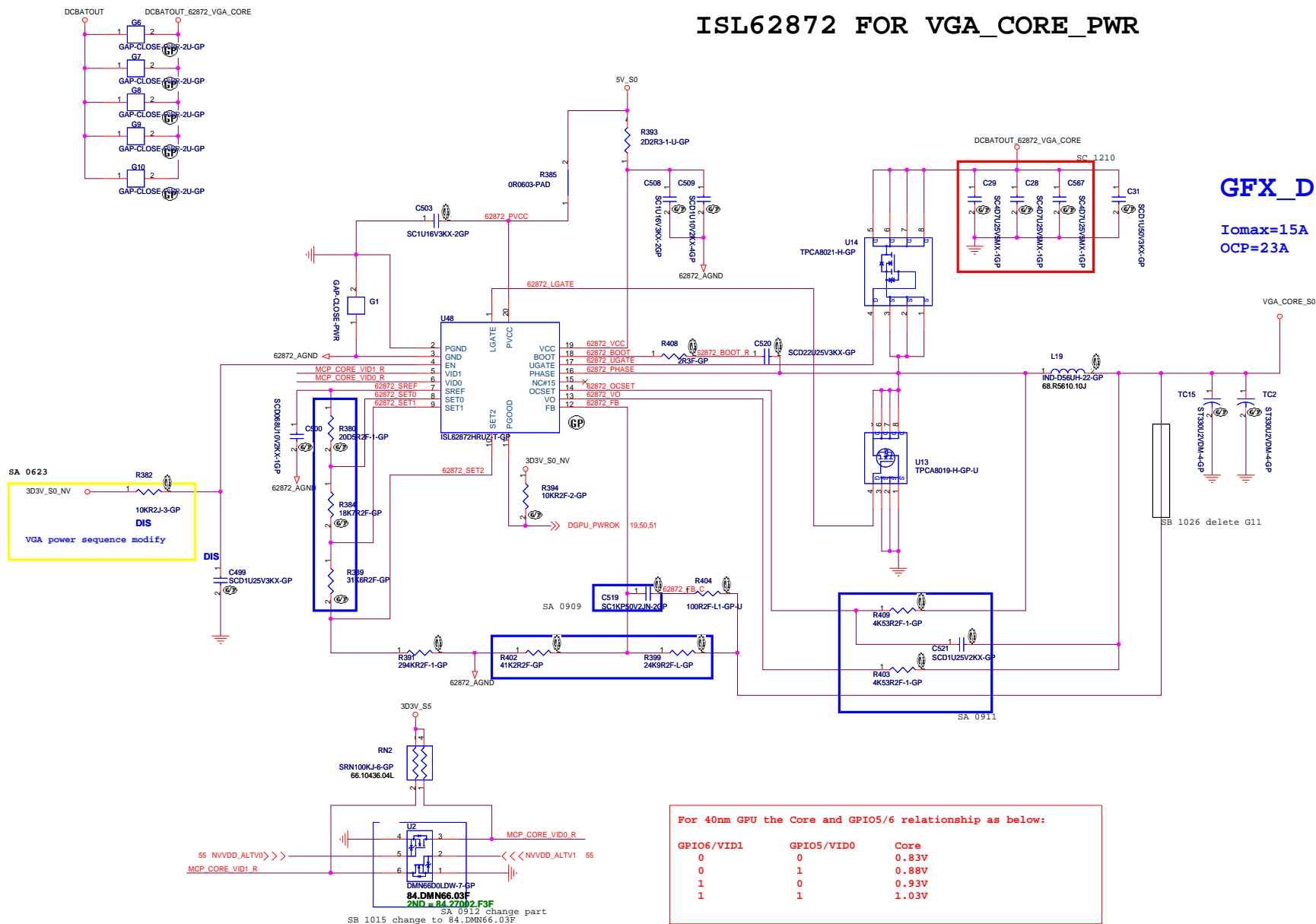
4

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2

1

ISL62872 FOR VGA_CORE_PWR



GFX_D

Iomax=1.5A
OCP=23A

For 40nm GPU the Core and GPIO5/6 relationship as below:

GPIO6/VID1	GPIO5/VID0	Core
0	0	0.83V
0	1	0.88V
1	0	0.93V
1	1	1.03V

SB 1031 R380 Change to 64.20R55.6DL
R384 Change to 64.18725.6DL
R389 Change to 64.31625.6DL
to rise up VGA voltage for NV suggestion.

SA 0623
3D3V_S0_NV
10KR2J-3-GP
DIS
VGA power sequence modify

SB 1026 delete G11

55 NVDD_ALTVO >>>
MCP_CORE_VID1_R <<< NVDD_ALTVO 55
U2
DMN66D0LW-7-GP
84.DMN66.03F
2ND = 84.27002.F3F
SB 0912 change part
SB 1015 change to 84.DMN66.03F

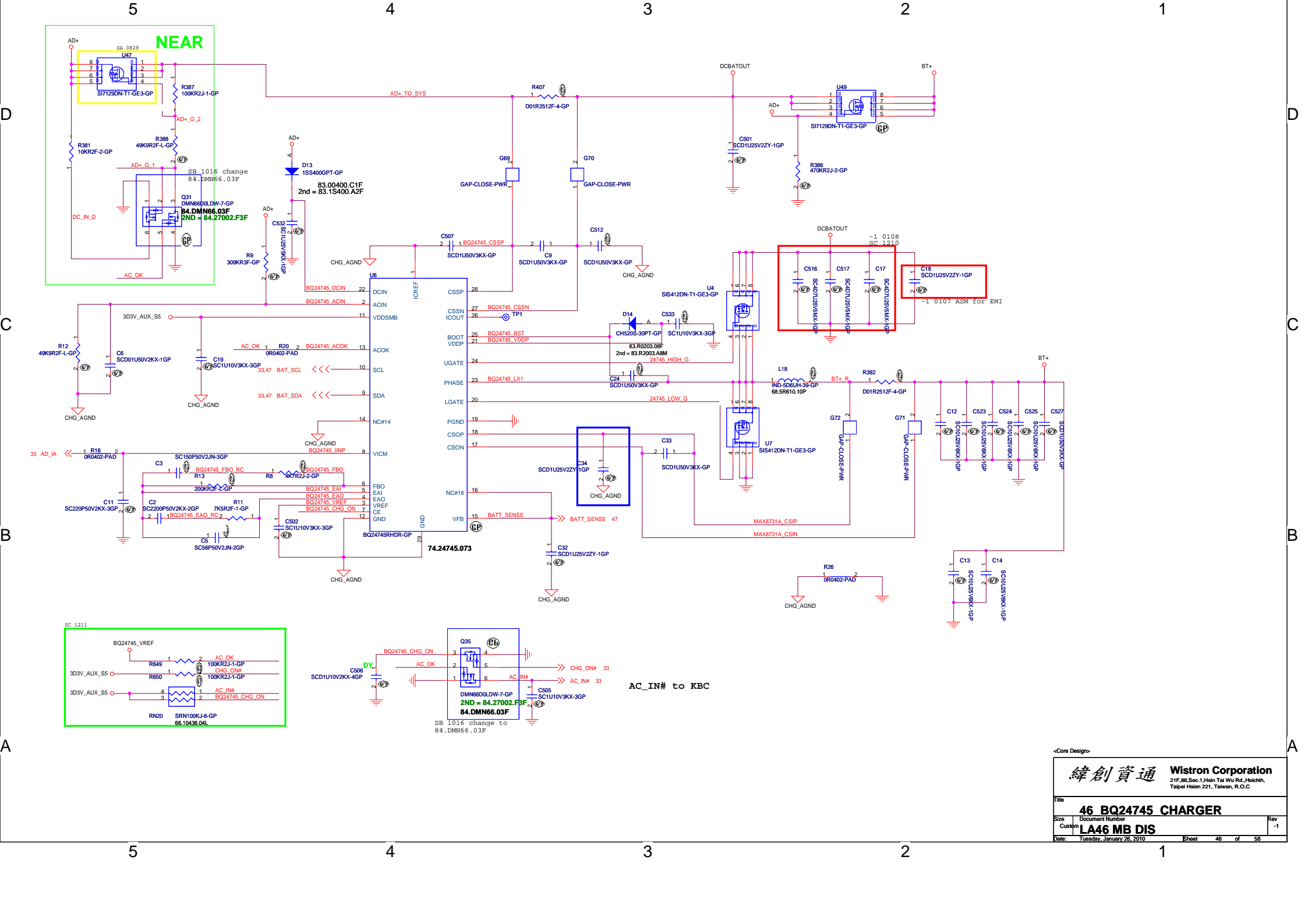
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C

Title: **45 ISL62872 VGA CORE**

Size: Customer Document Number: **LA46 MB DIS**

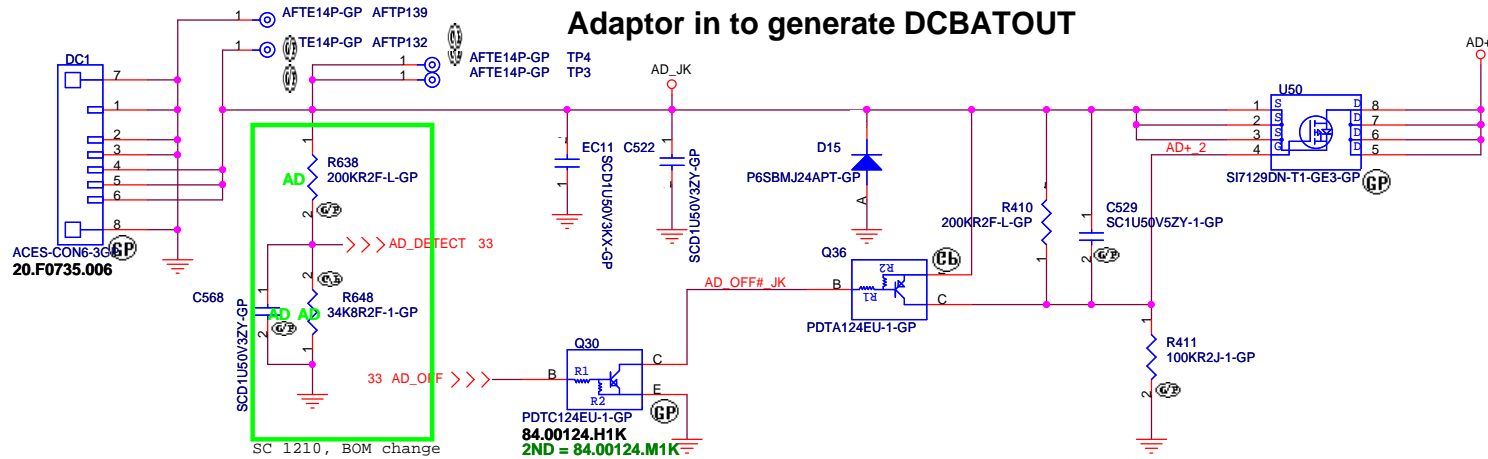
Date: Tuesday, January 26, 2010 Sheet 45 of 58



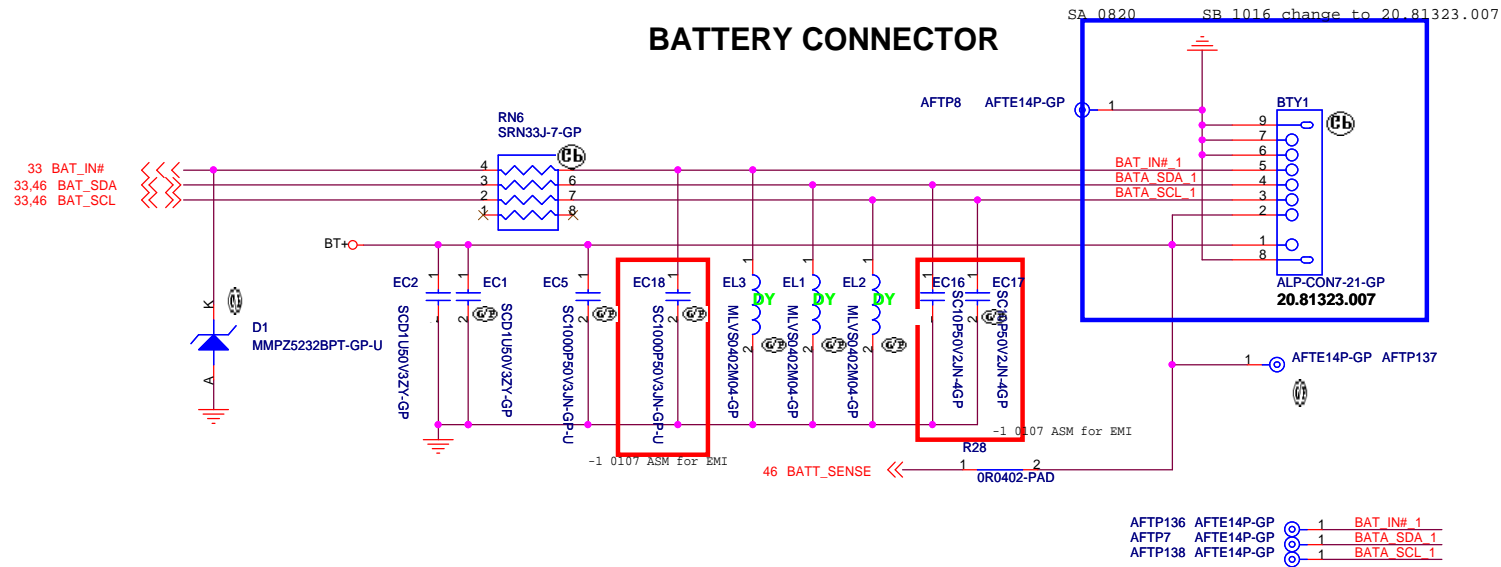
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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Size	Customer	Document Number	Rev
		LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet	46 of 58

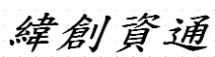
Adaptor in to generate DCBATOUT

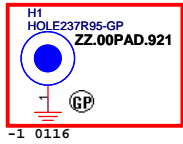


BATTERY CONNECTOR

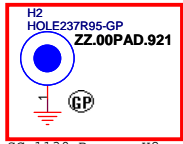


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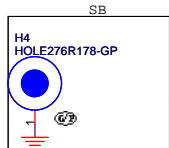
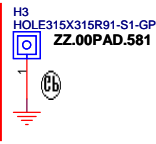
 Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title 47 AD / BATT CONN	
Size	Document Number
Custom	LA46 MB DIS
Date:	Tuesday, January 26, 2010
Sheet	47 of 58
Rev	-1



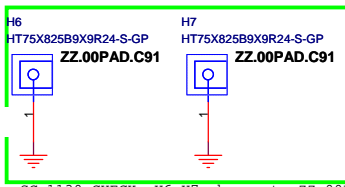
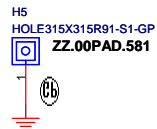
-1 0116



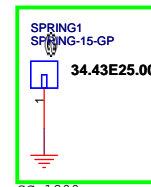
SC 1130 Remove H2
-1 0110



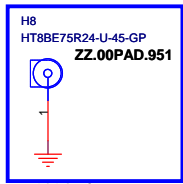
ZZ.00PAD.N11



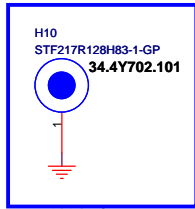
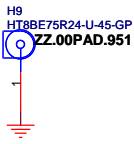
SC 1130 CHECK, H6,H7 change to ZZ.00PAD.C91



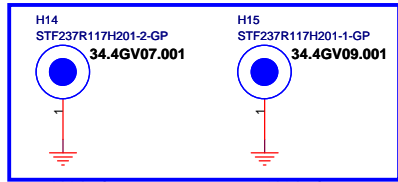
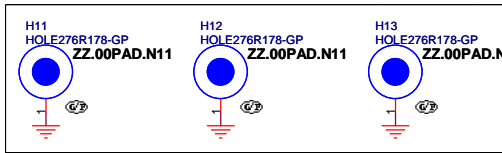
SC 1209



SB 1016 change to
ZZ.00PAD.951

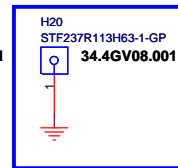
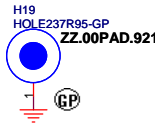
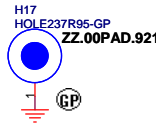
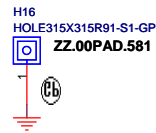


SB 1016 change to
34.4Y702.101

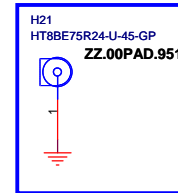


SB 1016 change to
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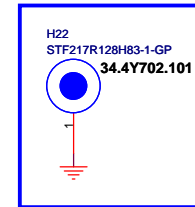
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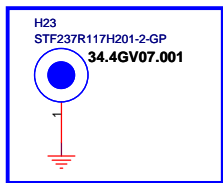
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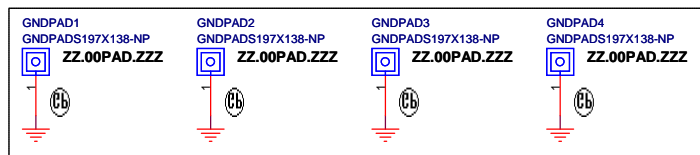
SB 1016 change
to ZZ.00PAD.951



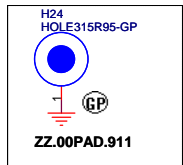
SB 1016 change to
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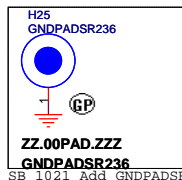
SB 1016 Add 34.4GV07.001



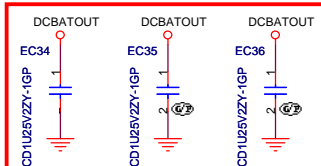
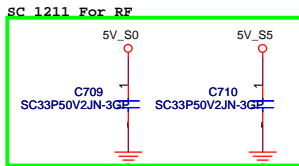
SB 1019 Add GND PAD



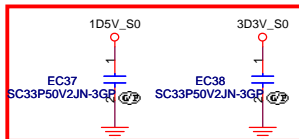
SB 1021 Add ZZ.00PAD.911



SB 1021 Add GNDPADSR236



-1 0107 ASM for EMI



-1 0116

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title

48 EMI/Spring/Boss

Size A3 Document Number

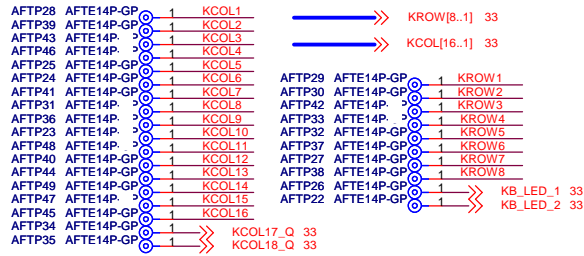
LA46 MB DIS

Rev

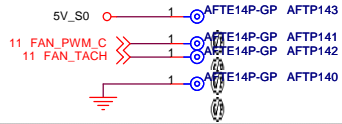
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Date: Tuesday, January 26, 2010 Sheet 48 of 58

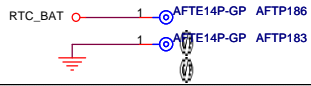
Near KB1 Keyboard



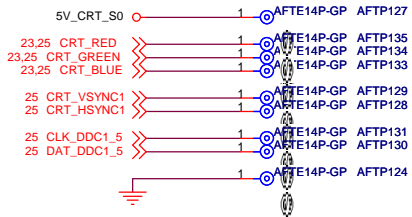
Near FAN1



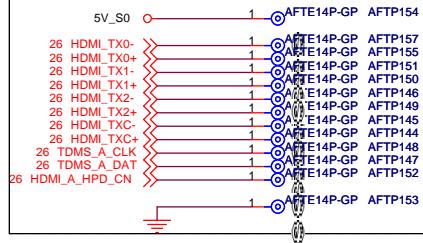
Near RTC1



Near CRT_CN1



Near HDMI_CN1



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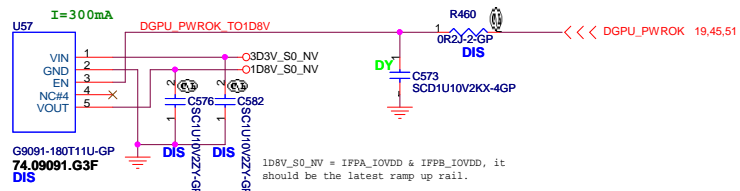
緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C

Title		
49 AFTE TP		
Size	Document Number	Rev
A3	LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet 49 of 58

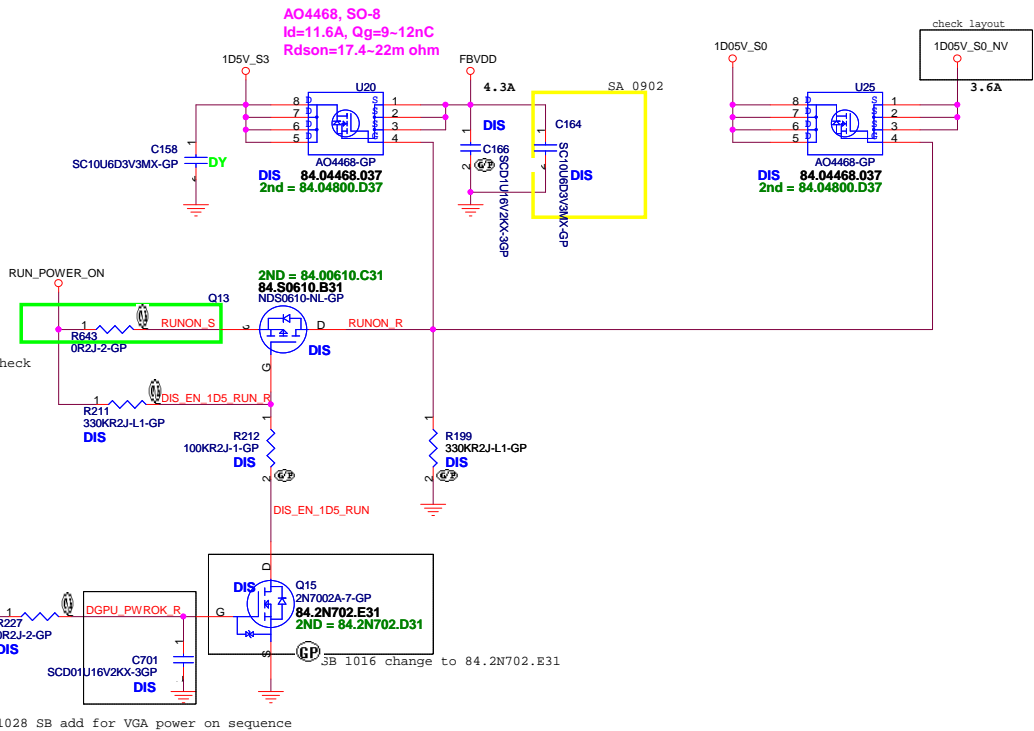
+1.5V to FBVDD Transfer

+1.05V to +1.05V_NV Transfer

+3VS to 1.8V Transfer



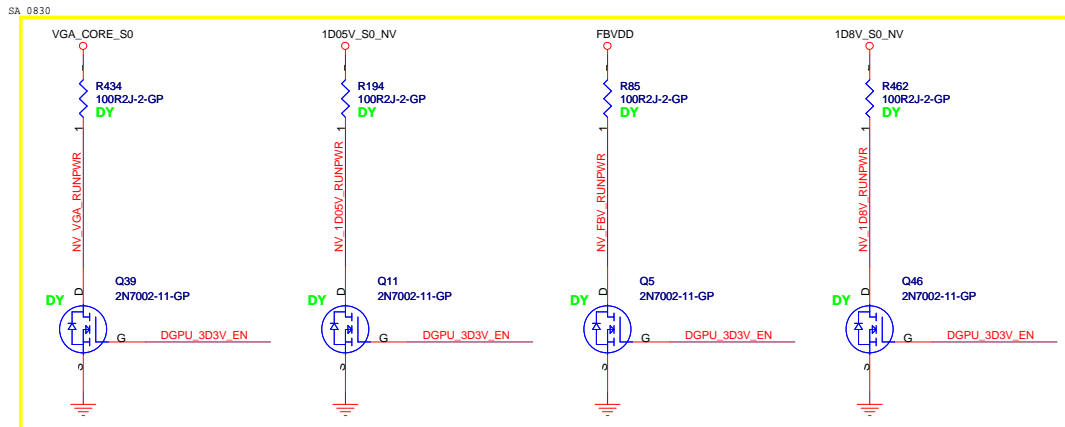
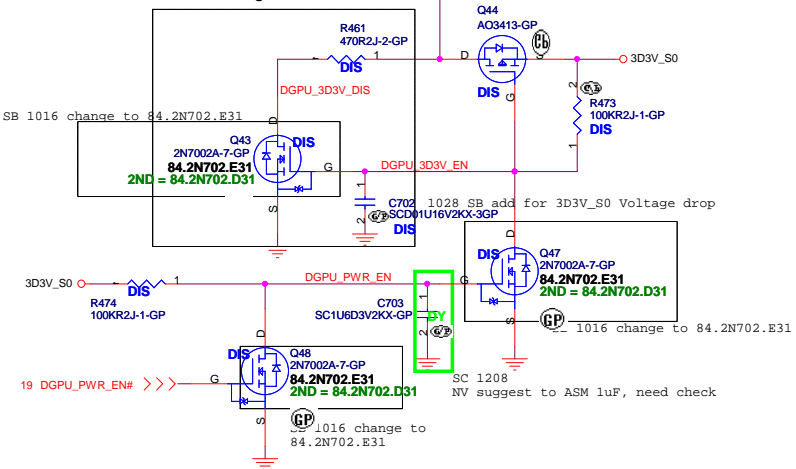
SC 1208
NV suggest to use 200K, need check



+3VS to 3.3V_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT



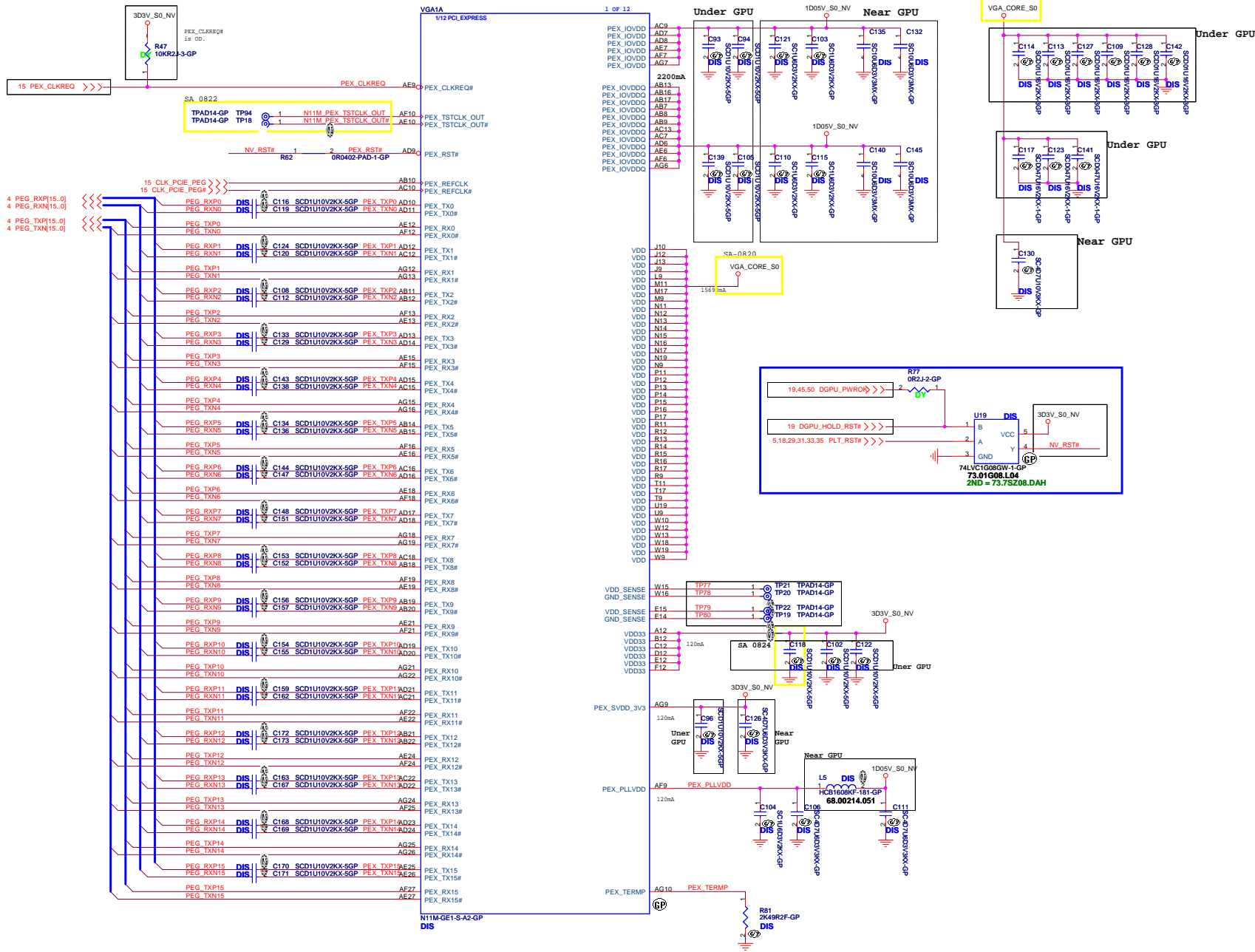
system turn on 3D3V_S0_NV --> VGA_CORE_S0
DGPU_PWROK --> FBVDD, 1D05V_S0_NV, 1D8V_S0_NV

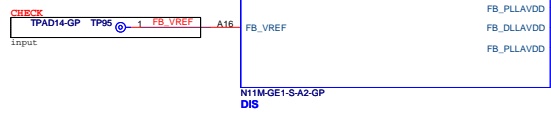
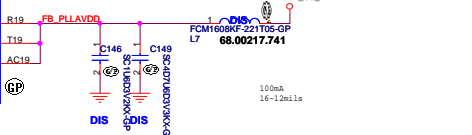
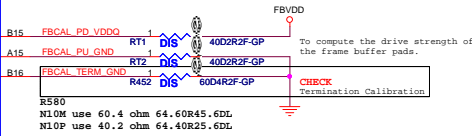
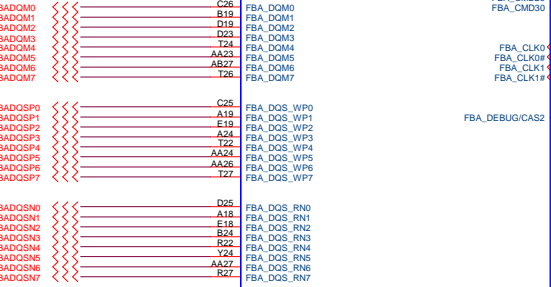
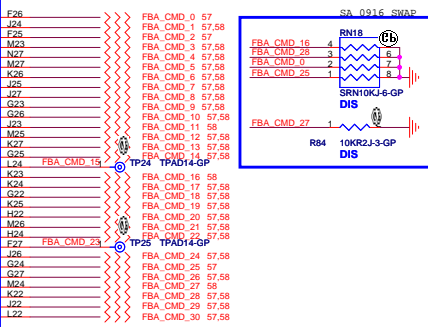
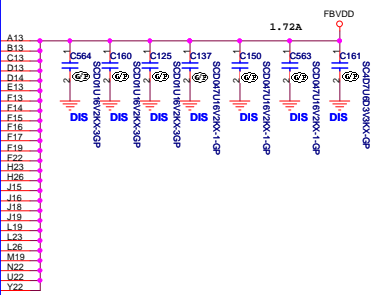
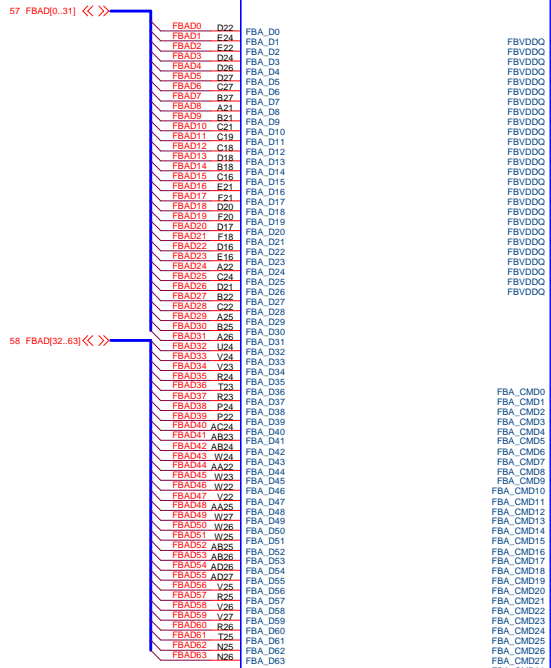
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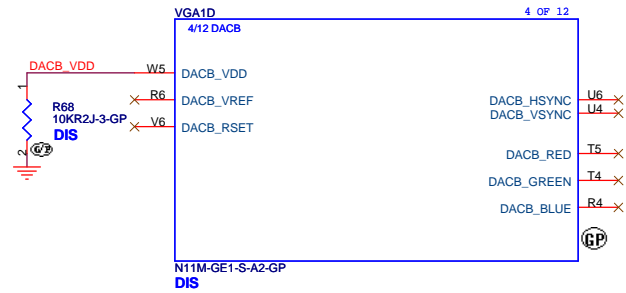
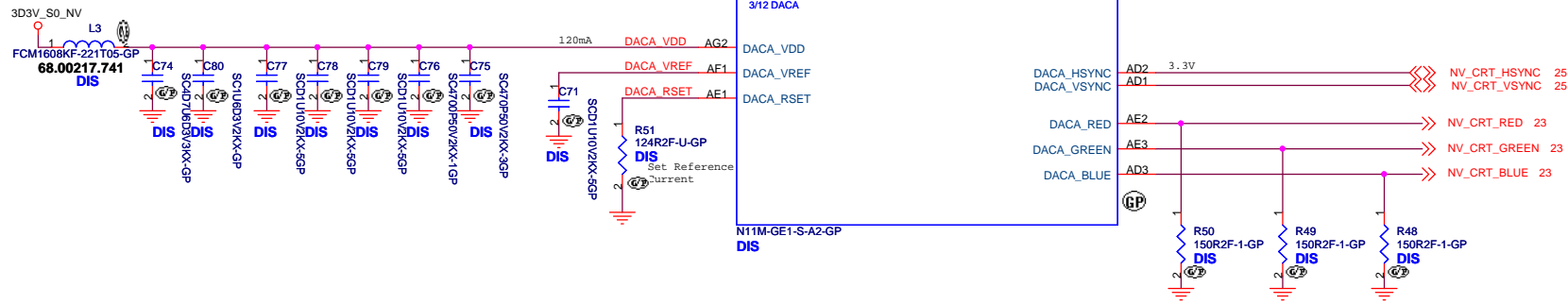
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Title		50 NV power	
Size	Document Number	LA46 MB DIS	
Customer	Date:	Tuesday, January 26, 2010	Sheet 50 of 58
Rev	-1		

A3? 71.0N11M.CO.U

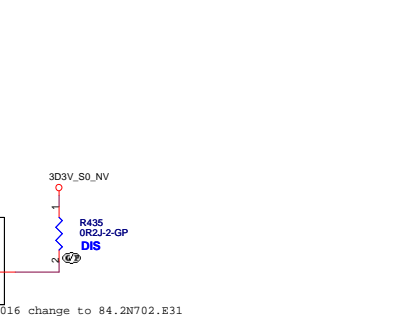
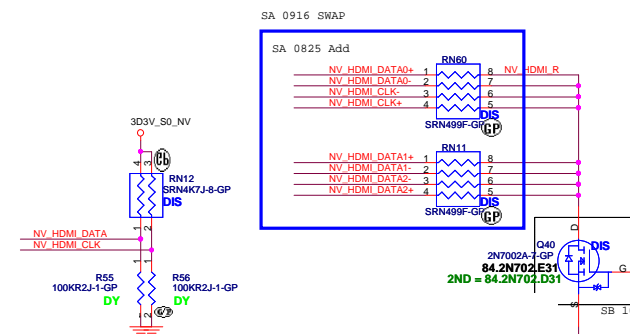
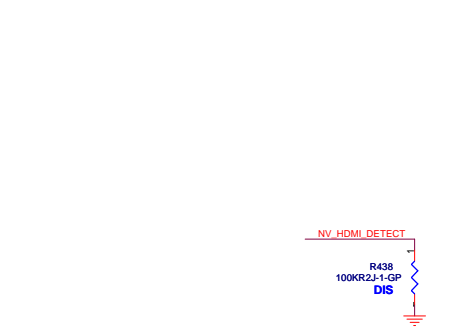
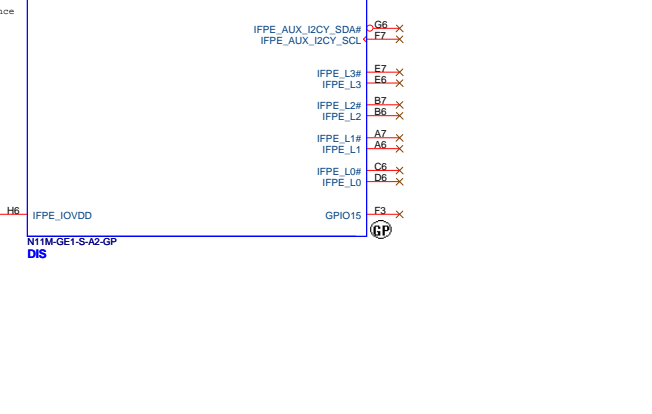
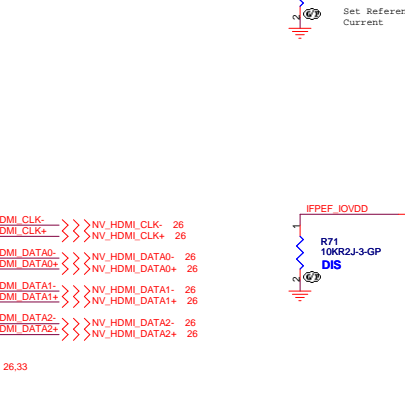
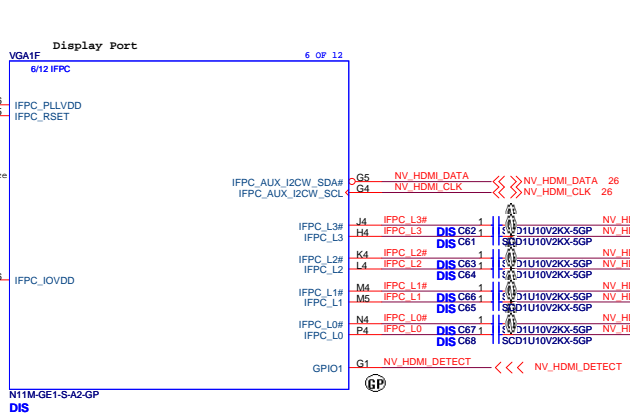
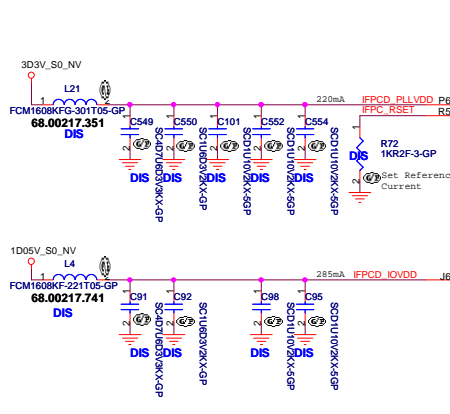
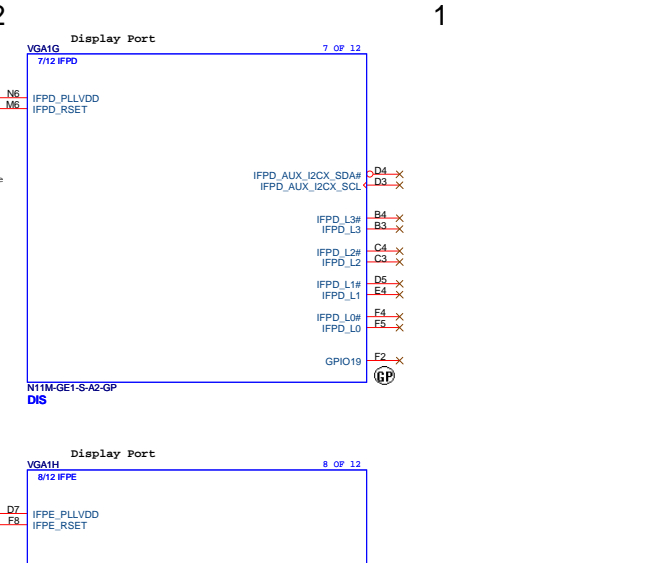
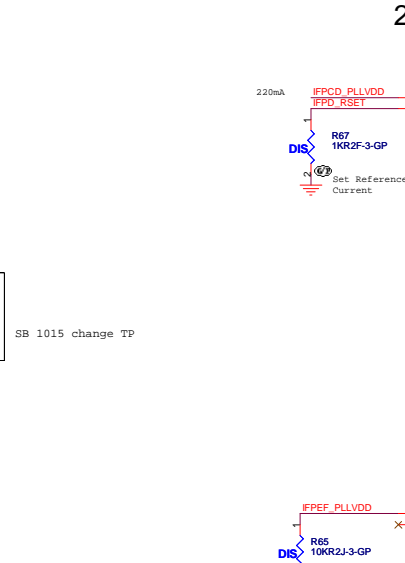
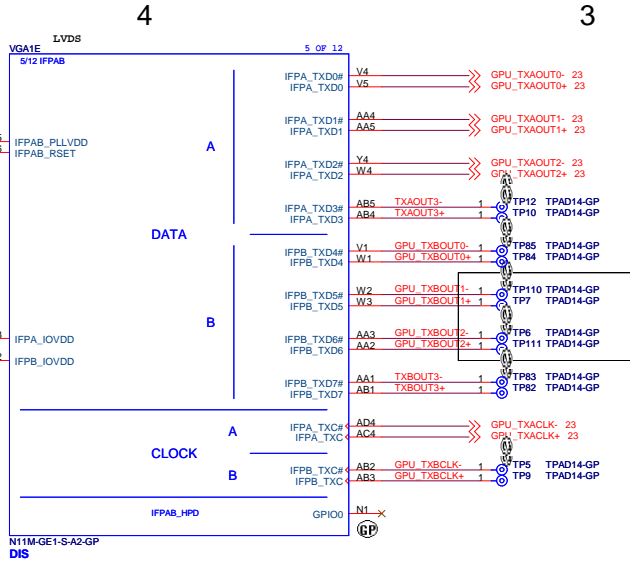
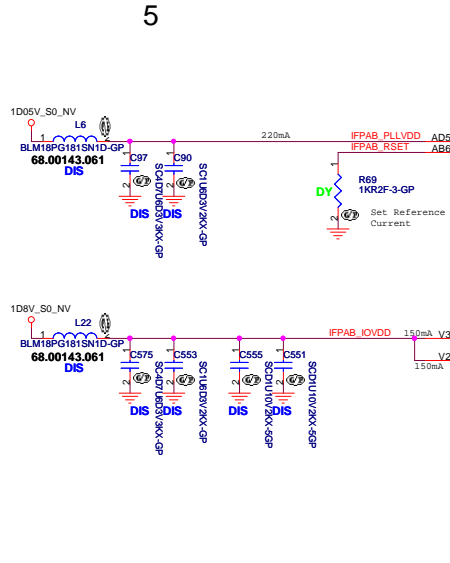




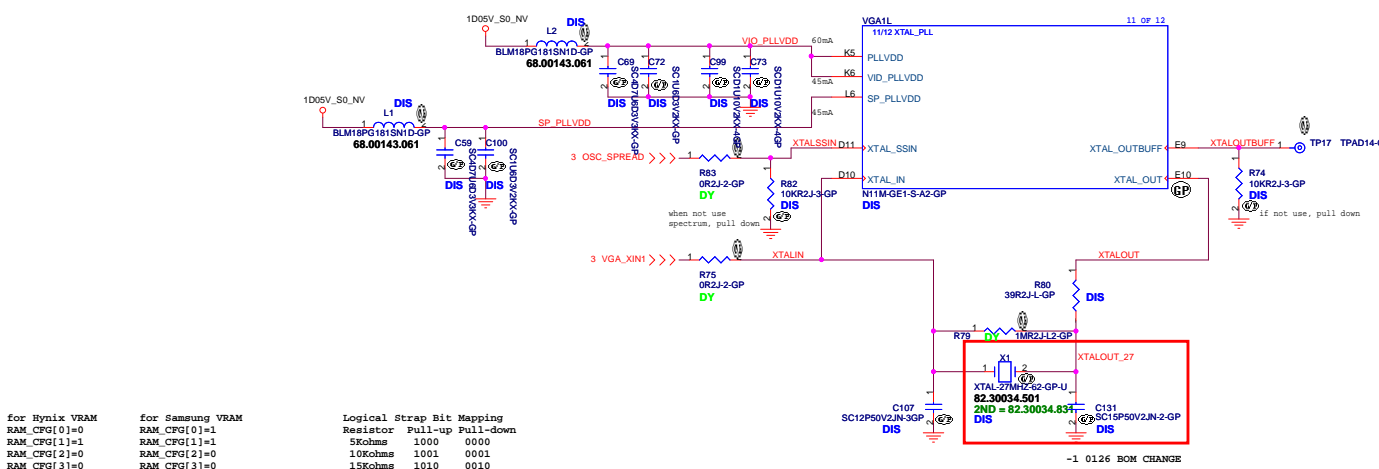
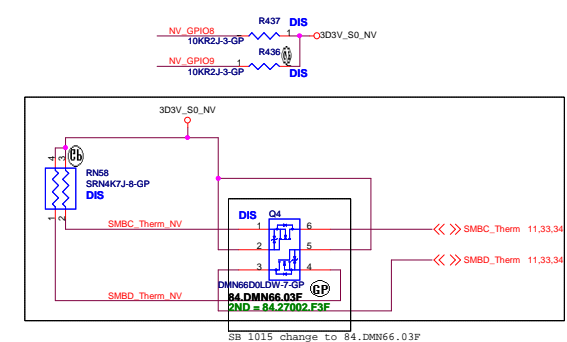
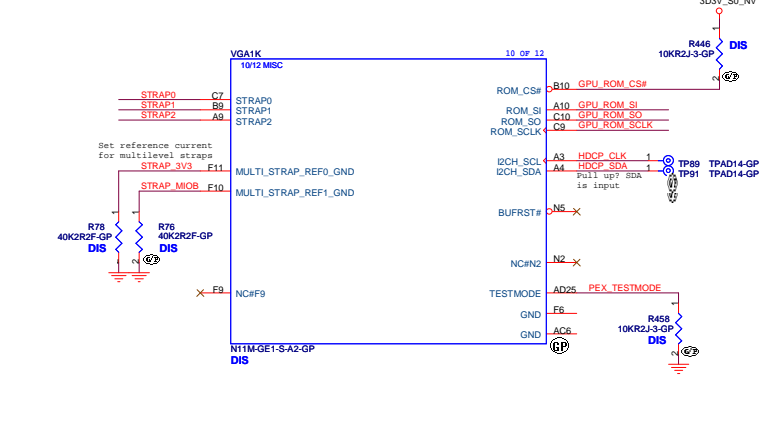
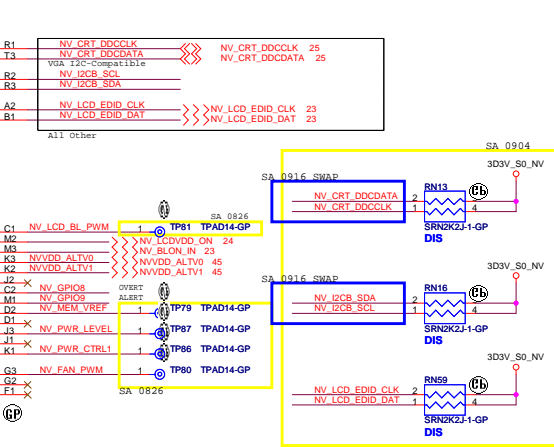
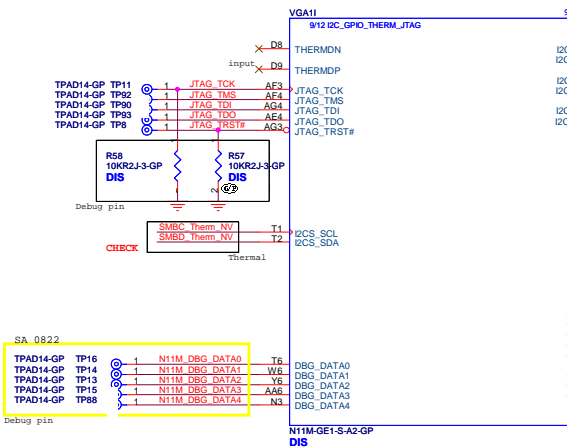


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Title	
53 N11M(3/6) DAC	
Size	Document Number
Customer	LA46 MB DIS
Date:	Tuesday, January 26, 2010
Sheet	53 of 58
Rev	-1



Direct HDMI Connection



```

DeviceID
USER[0]=1          N11P-LMI (0x0A2B) ?
USER[1]=1          N11M-LP1 (0x0A75) 1-0101
USER[2]=1
USER[3]=1

GPU_ROM_SI for Hynix VRAM  for Samsung VRAM
RAM_CFG[0]=0 RAM_CFG[0]=1
RAM_CFG[1]=1 RAM_CFG[1]=1
RAM_CFG[2]=0 RAM_CFG[2]=0
RAM_CFG[3]=0 RAM_CFG[3]=0

GPU_ROM_SI for Hynix VRAM  for Samsung VRAM
RAM_CFG[0]=0 RAM_CFG[0]=1
RAM_CFG[1]=1 RAM_CFG[1]=1
RAM_CFG[2]=0 RAM_CFG[2]=0
RAM_CFG[3]=0 RAM_CFG[3]=0

GPU_ROM_SO VGA_DEVICE =1
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0

GPU_ROM_SCLK PEX_PLL_BN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 [4] 0 1
  
```

Logical Strap Bit Mapping	
Resistor	Pull-up Pull-down
5Kohms 1000 0000	
10Kohms 1001 0001	
15Kohms 1010 0010	
20Kohms 1011 0011	
25Kohms 1100 0100	
30Kohms 1101 0101	
35Kohms 1110 0110	
45Kohms 1111 0111	

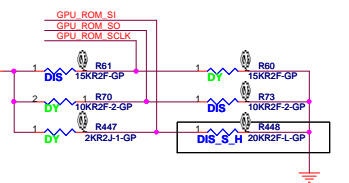
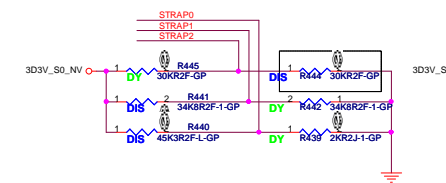


TABLE KENDO VIDEO MEMORY

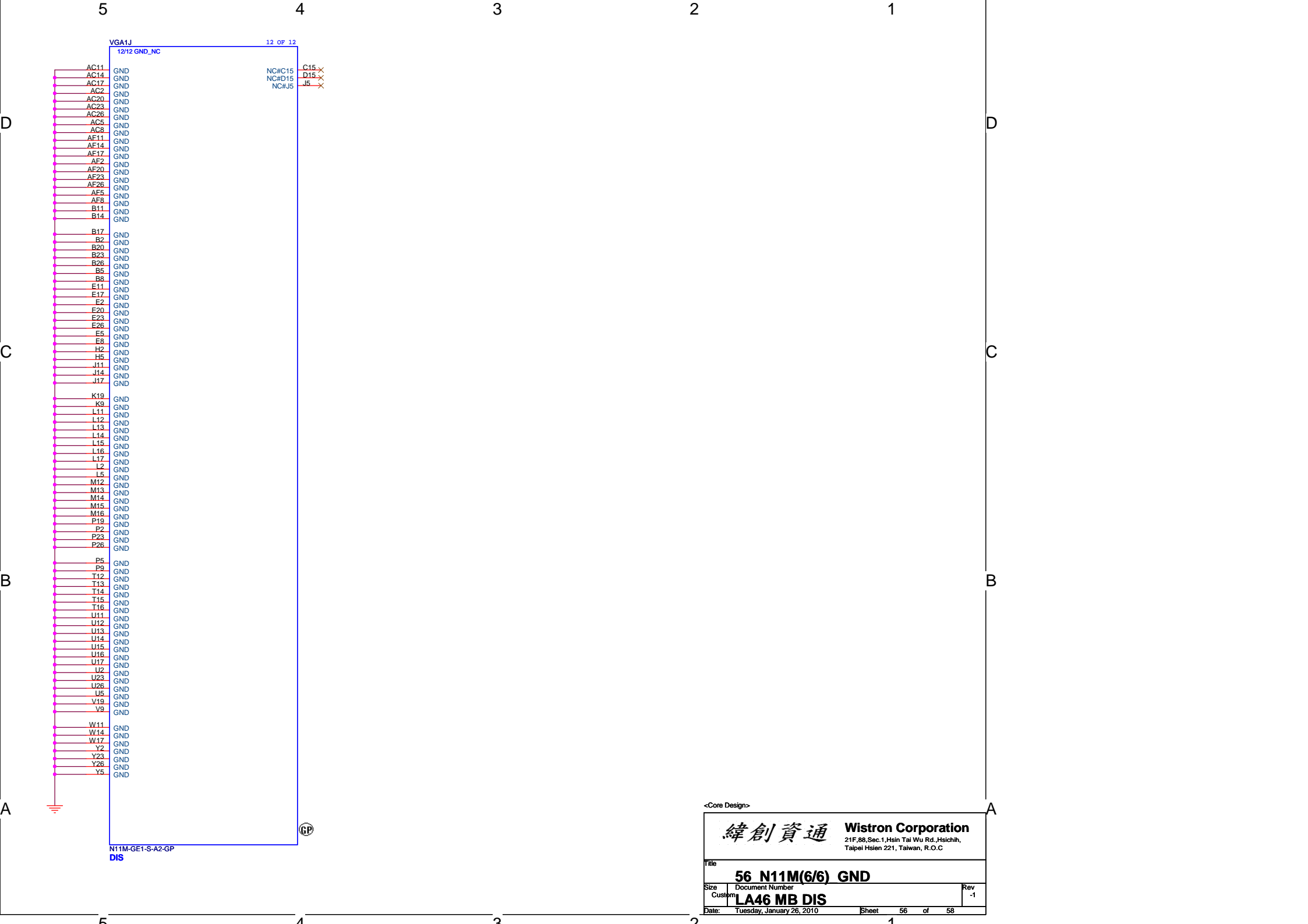
	SAMSUNG	HYNIX
R448	64.20025.6DL	64.15025.6DL

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 21F, 88, Sec. 1, Main Tai Wu Rd, Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

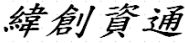
55 N11M(5/6) STRAP/ GPIO
 LA46 MB DIS

Rev: 1

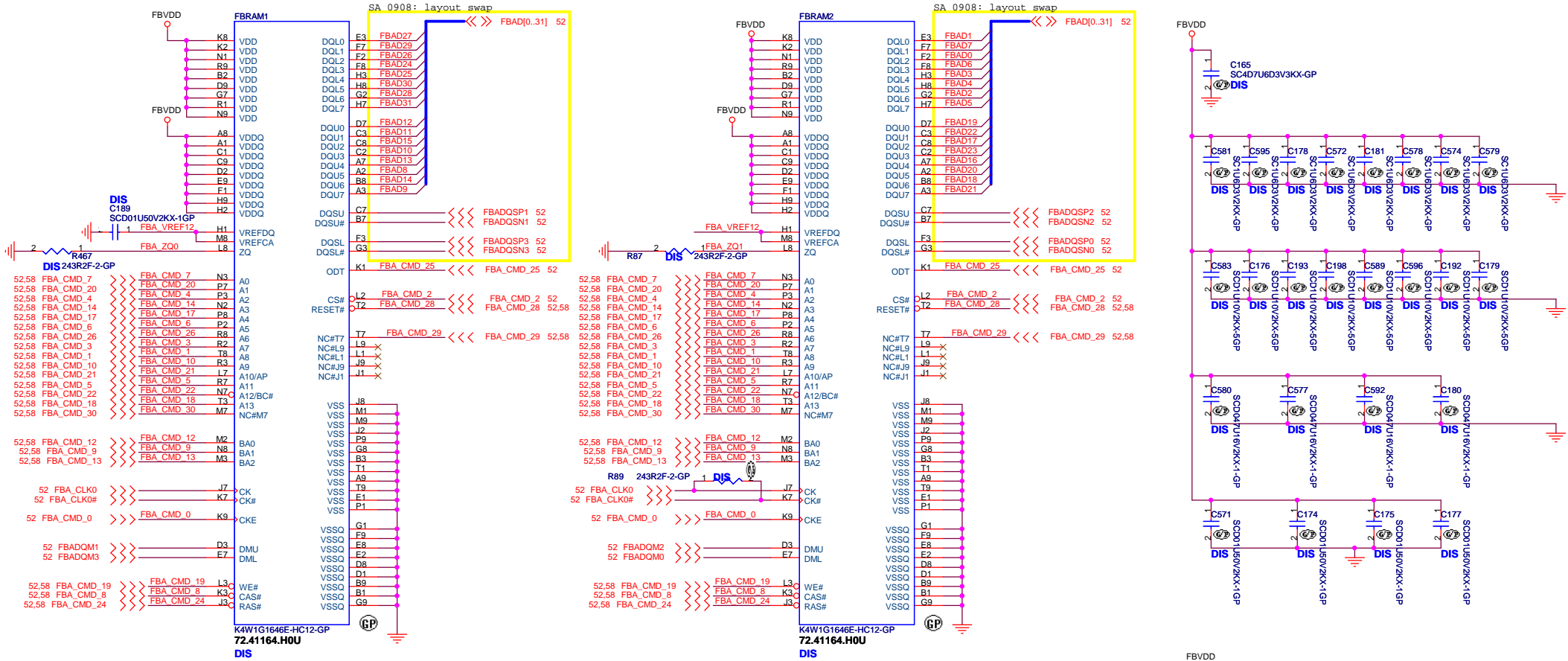
Date: Wednesday, January 27, 2010 Sheet 55 of 58



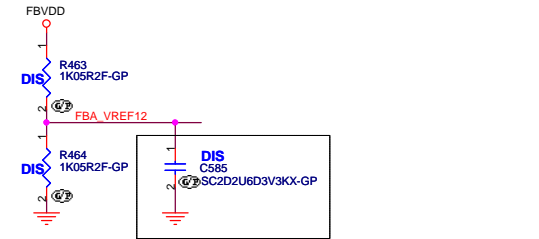
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File	
56 N11M(6/6) GND	
Size	Document Number
Custom	LA46 MB DIS
Date:	Tuesday, January 26, 2010
Sheet	56 of 58
Rev	-1

Mode C Command Mapping

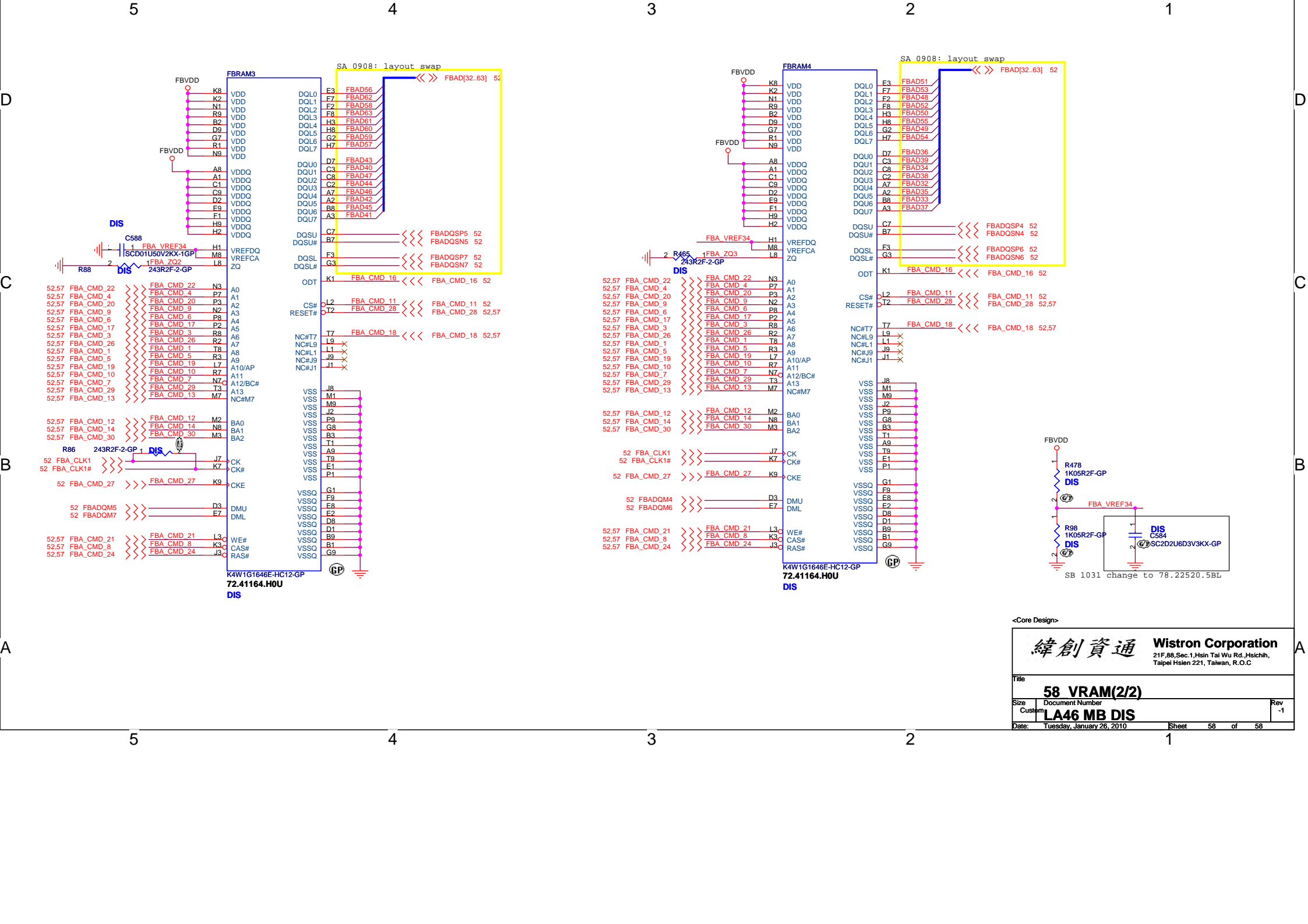


2nd: 72.51G63.C0U (IC SDRAM H5TQ1G63BFR-12C FBGA)



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Title 57 VRAM(1/2)	
Size Custom	Document Number LA46 MB DIS
Date: Tuesday, January 26, 2010	
Sheet 57 of 58	



<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C

File: **58 VRAM(2/2)**

Size: Document Number
 Customer: **LA46 MB DIS**

Date: Tuesday, January 26, 2010 Sheet 58 of 58

Rev: -1