COMPAL CONFIDENTIAL

MODEL NAME : BAL20

PCB NO : DAZ1P600100

BOM P/N : 431A2K31L01

SKL-U+MEC1404 board
2016-06-21

REV : 1.0 (A00)

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
KBL@/SKL@ : CPU Type
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
3D@/3D@EMI@ : 3D Camera
@3D@ : 3D Camera Un-POP Component

M1_70R1@ : GPU R1
M1_70R3@ : GPU R3
2G@/2G_H@/2G_S@/2G_M@ : VRAM type
4G@/4G_H@/4G_S@/4G_M@ : VRAM type

ZZZ

PCB

DAZ1P600100

PCB@

PCB BAL20 LA-D801P LS-D801P/D802P/D803P

KBL R3

UC1

i7-R1

SA0000A344L

i7KBL2.7G_R3@

S IC FJ8067702739740 SR2ZV H0 2.7G A31!

UC1

i5-R1

SA0000A374L

i5KBL2.5G_R3@

S IC FJ8067702739739 SR2ZU H0 2.5G A31!

SKL R3

UC1

i7-R3

SA000092P3L

i7SKL2.5G_R3@

FJ8066201930408 SR2EZ D1 2.5G A31!

UC1

i5-R3

SA000092O3L

i5SKL2.3G_R3@

FJ8066201930409 SR2EY D1 2.3G A31!

Layout Dell logo

REV: X00
PWB: 9HTP8

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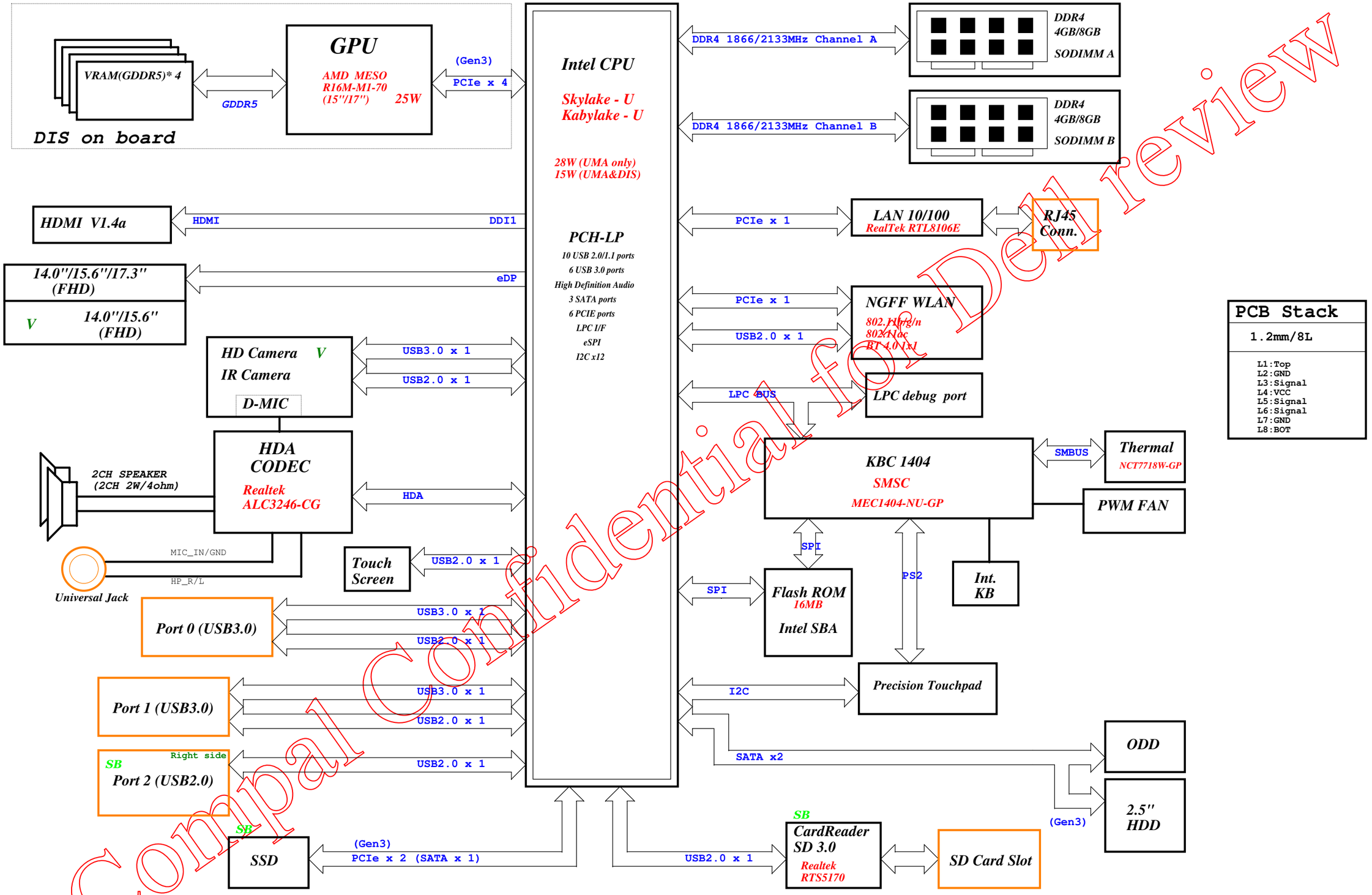
Compal Electronics, Inc.		
Title: Cover Page		
Size	Document Number: LA-D801P	Rev: A00
Date: Tuesday, June 21, 2016	Sheet 1 of 61	

Block Diagram



PCB Stack
1.2mm/8L
L1:Top L2:GND L3:Signal L4:VCC L5:Signal L6:Signal L7:GND L8:BOT

Title	Block Diagram	
Size C	Document Number LA-D801P	Rev A00
Date: Tuesday, June 21, 2016	Sheet 2 of 61	

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB3.0 Port1
2	USB3.0 Port2
3	IO/DB
4	N/A
5	CCD
6	Card Reader
7	Touch Screen
8	BT
9	N/A
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port1
USB3.0-2	SSIC-1			USB3.0 Port2
USB3.0-3	SSIC-2			3D Camera
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		10/100M LAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	SATA ODD
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	N/A

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	DVT1
3	100	17.8	2.801	DVT2
4	100	22.1	2.703	
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

Compal Electronics, Inc.

Title: Index and Configuration

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CPU PWR
GPU PWR
Peripheral Device PWR

ADAPTER
CHARGER ISL95521HRZ (PU703)
BATTERY
+PWR_SRC (+19VB)

PJP206 RT8207PGQW (PU200)
SIO_SLP_S4#
+1.2VP
PJP200
+1.2V_DDR
0.6V_DDR_VTT_ON
+0.6VSP
PJP203
+0.6V_DDR_VTT

PJP301 SYX196DQNC (PU301)
@SIO_SLP_SUS#
POK
+1VALWP
PJP302
+1.0V_PRIM

TPS22961 (UZ2)
SIO_SLP_S3#
SIO_SLP_S0#
+1.0V_VCCSTG 3.5A
JP1
Volume
+1.0VS_VCCIO 3.4A

0ohm 0603 (RC174)
+1.0V_MPHYGT 2.8A
P.18

TPS22967 (UZ1)
SIO_SLP_S4#
+1.0V_VCCST 240mA

EM5209VF (UZ5)
JP7
DGPU_PWR_EN
+0.95VSDGPU

PJP1401 SYX196DQNC (PU1400)
DGPU_PWROK
+1.35VGPUP
PJP1402
+1.35V_MEM_GFX

PJP106 SY8286CRAC (PU102)
EN_5V
ENLDO_3V5V
+5VALWP
PJP103
+5VALW
VL

AP22802BW5 (UU1)
USB_EN#
USB30_VCCA

AP22802BW5 (UU3)
USB_EN#
USB20_VCCA

EM5209VF (UZ3)
JP4
SIO_SLP_S3#
+5VS

TPS22967DSGR (UX1)
JP14
3D_CAM_EN
+5V_CAM

0ohm 0805 (RA1) → +5V_PVDD
0ohm 0805 (RS2) → +5V_HDD_S0
0ohm 0805 (RS3) → +5V_ODD_S0
FUSE 1.1A_6V (FI1) → +5V_HDMI
FUSE 0.5A_13.2V (F3) → +5V_KB_BL

PJP105 SY8286BRAC (PU100)
EN_3V
ENLDO_3V5V
+3VALWP
PJP102
+3VALW
+3VLP
BAS40C (D1)
+RTC_CELL
+RTC_VCC

EM5209VF (UZ3)
JP5
SIO_SLP_S3#
+3VS

RT9724GB (U1)
EDP_VDD_EN or LCD_TST
+LCDVDD

0ohm 0805 (RW3) → +3.3V_WLAN

EM5209VF (UZ4)
DGPU_PWR_EN
JP6
+3VGS

JP9
+3VALW_PCH

PJP501 RT8061AZQW (PU500)
(NON-DS3) POK
(DS3) @SIO_SLP_SUS#
+1.8VALWP
PJP502
+1.8V_PRIM
EM5209VF (UZ5)
JP8
DGPU_PWR_EN
+1.8VGS

PJP801 RT9059GSP (PU800)
SIO_SLP_S4#
+2.5VP
PJP802
+2.5V_MEM

PJP1201 NB681GD-Z (PU1200) U23@
SIO_SLP_S3#
+1.0VS_VCCOPCP
PJP1202
+1.0VS_VCCOPC

ISL95859HRTZ (PU602)
ISL95808HRZ (PU606)
IMVP_VR_ON
+VCC_SA

AOZ5019QI (PU604) U23@
AOZ5019QI (PU603)
IMVP_VR_ON
+VCC_CORE

AOZ5019QI (PU605)
DRMOS_EN
+VCC_GT

ISL62771HRTZ (PU1100)
DGPU_PWR_EN
+VGA_CORE

Compal Electronics, Inc.

Title: Power Rail

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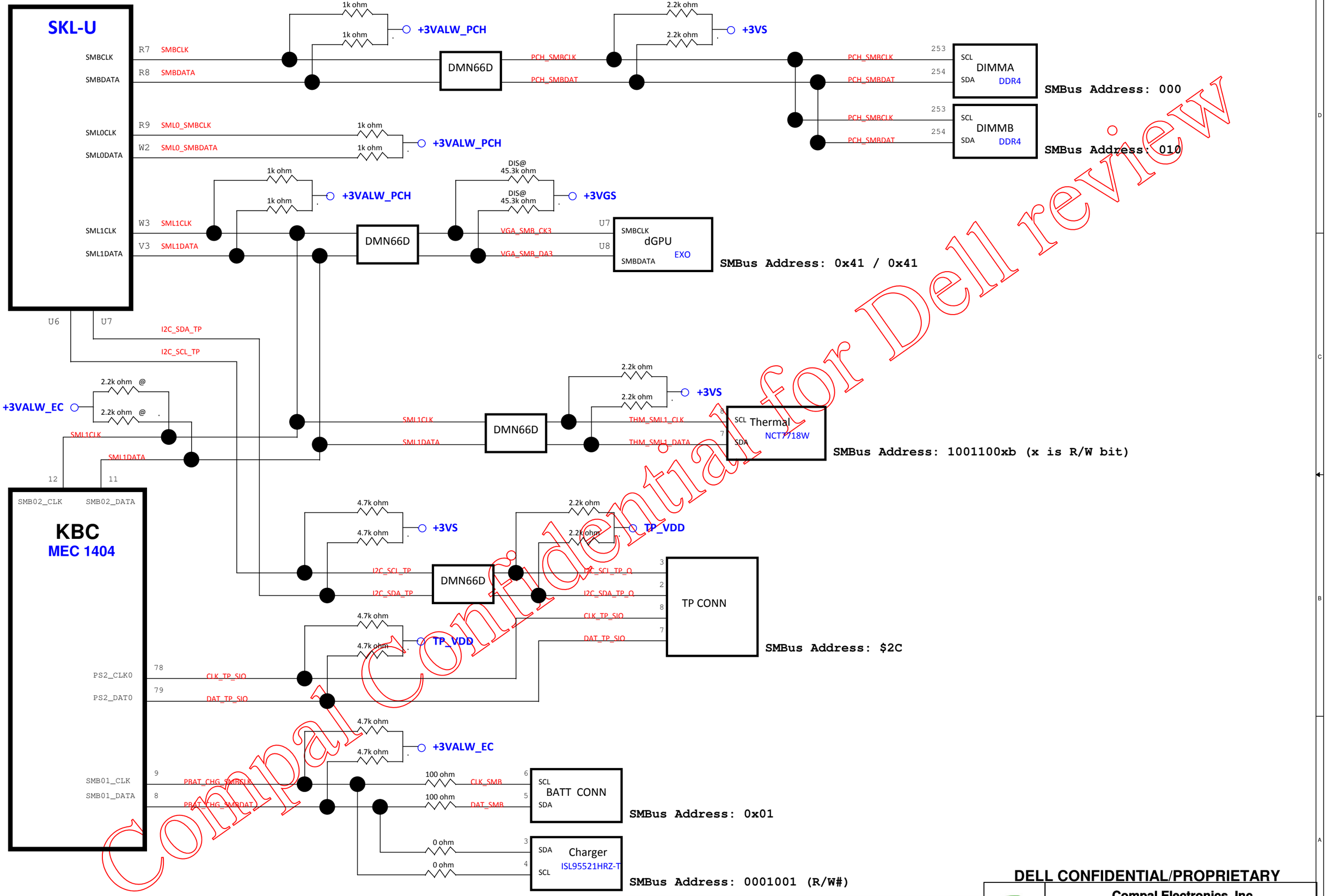

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Title: SMbus Block diagram

Size | Document Number: LA-D801P | Rev: A00

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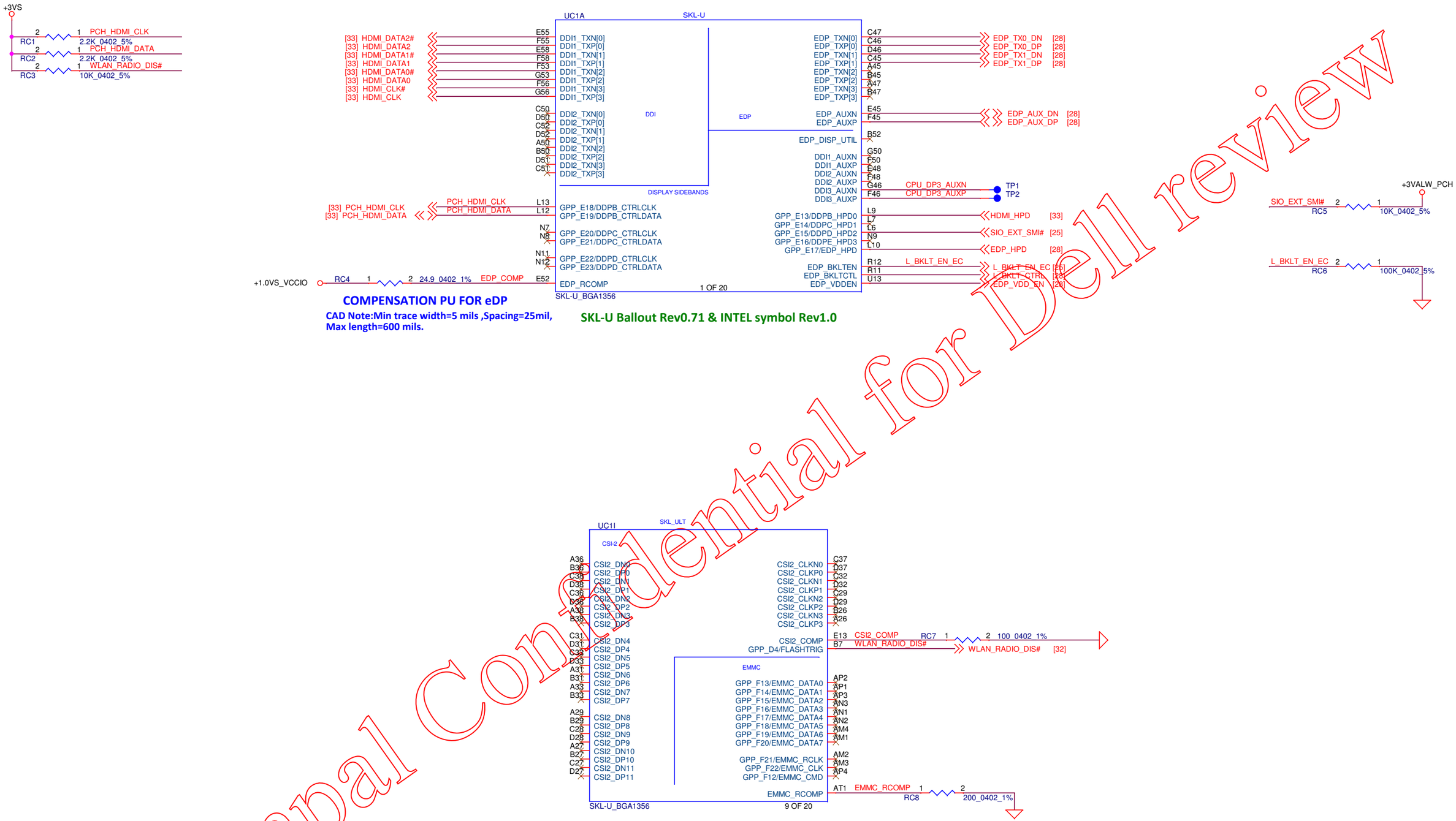

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Compal Electronics, Inc.

Title: MCP(1/14)DDI,EDP,CSI2,EMMC

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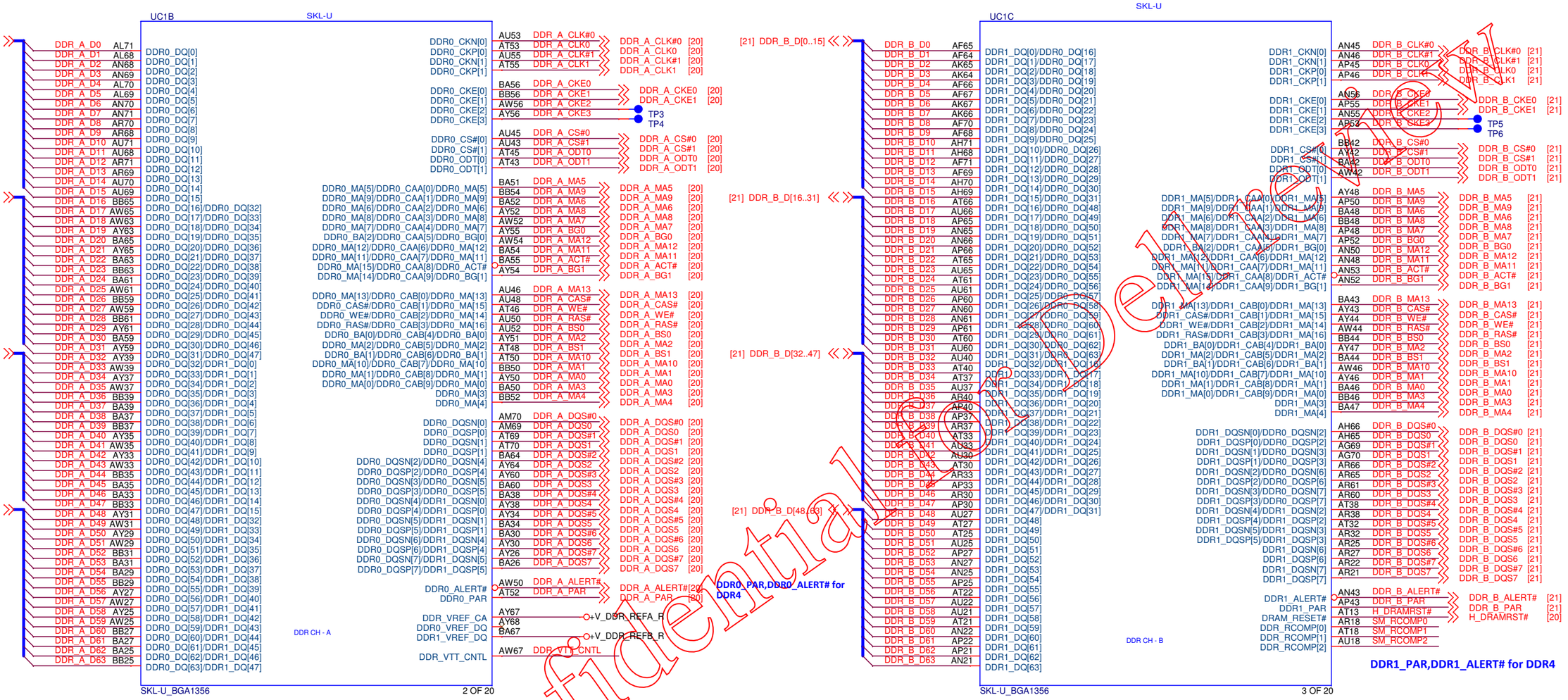
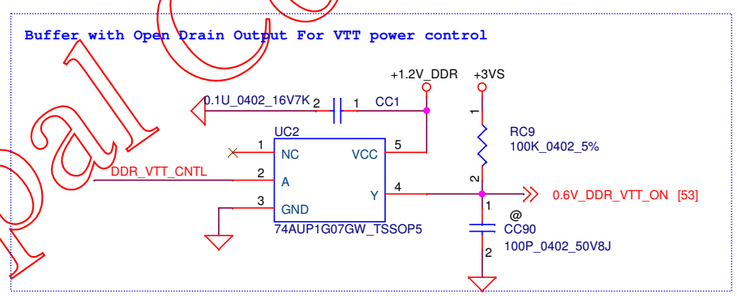
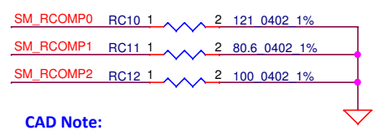
DDR4 Interleaved Memory





BUFFER
Main: SA00005U600
2nd: SA00007UR00

DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

Compal Electronics, Inc.			
Title: MCP(2/14)DDR4			
Size	Document Number: LA-D801P		Rev: A00
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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

+3VS
RC181 @ 10K_0402_5%
ONE_DIMM#
RC182 10K_0402_5%

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

UC1E SKL-U

SPI - FLASH
PCH_SPI_CLK_R1 AV2 SPI0_CLK
PCH_SPI_D1_R1 AW3 SPI0_MISO
PCH_SPI_D0_R1 AV3 SPI0_MOSI
PCH_SPI_D2_R1 AW2 SPI0_IO2
PCH_SPI_D3_R1 AU4 SPI0_IO3
PCH_SPI_CS#0_R1 AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#
[25] PCH_SPI_CS#0_R1

SPI - TOUCH
ONE_DIMM# M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK
G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

LPC
AW13 GPP_A0/RCIN#
AY11 GPP_A6/SERIRQ

SMBUS, SMLINK
GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 PCH_SMB_ALERT#
GPP_C3/SML0CLK R9 SML0_SMBCLK
GPP_C4/SML0DATA W2 SML0_SMBDATA
GPP_C5/SML0ALERT# W1 GPP_C5
GPP_C6/SML1CLK W3 SML1CLK → SML1CLK [25,30,41]
GPP_C7/SML1DATA V3 SML1DATA → SML1DATA [25,30,41]
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23

LPC
GPP_A1/LAD0/ESPI_IO0 AY13 → LPC_LAD0 [25]
GPP_A2/LAD1/ESPI_IO1 BA13 → LPC_LAD1 [25]
GPP_A3/LAD2/ESPI_IO2 BB13 → LPC_LAD2 [25]
GPP_A4/LAD3/ESPI_IO3 AY12 → LPC_LAD3 [25]
GPP_A5/LFRAME#/ESPI_CS# BA12 → LPC_LFRAME# [25]
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT#/LPCPD#

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 PCI_CLK_LPC1 → EMI@ RC15 1 2 22_0402_5% → CLK_PCI_LPC_MEC [25]
GPP_A10/CLKOUT_LPC1 AY9 → EMI@ RC16 1 2 22_0402_5% → CLK_PCI_LPDEBUG [25]
GPP_A8/CLKRUN# AW11 CLKRUN# → CLKRUN# [25]

SKL-U_BGA1356 5 OF 20

+3VS
RC13 10K_0402_5%
[25] SIO_RCIN#
[25] SERIRQ
+3VS RC14 10K_0402_5%

+3VS
QC1A DMN66D0LDW-7_SOT363-6
SMBCLK → PCH_SMBCLK [20,21]
QC1B DMN66D0LDW-7_SOT363-6
SMBDATA → PCH_SMBDATA [20,21]

SMB -> DDR4

SML1 -> EC,DGPU,THM
SML1CLK => GPU_THM_SMBCLK
SML1DATA => GPU_THM_SMBDAT

+3VS
PCH_SMBDATA RC27 2.2K_0402_5%
PCH_SMBCLK RC28 2.2K_0402_5%

+3VALW_PCH
SMBCLK RC29 1K_0402_5%
SMBDATA RC30 1K_0402_5%
SML1CLK RC31 1K_0402_5%
SML1DATA RC32 1K_0402_5%
SML0_SMBCLK RC33 1K_0402_5%
SML0_SMBDATA RC34 1K_0402_5%
SUS_STAT#/LPCPD# RC35 @ 8.2K_0402_5%

+3VS
CLKRUN# RC36 8.2K_0402_5%

Int. PD.
+3VALW_PCH
PCH_SMB_ALERT# RC37 @ 8.2K_0402_5%

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Int. PD.
+3VALW_PCH
GPP_C5 RC38 @ 10K_0402_5%

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

+3VALW_PCH
Modify Value to 150k for WW52 MOW 2015/03/03 Jason
GPP_B23 RC39 CMC@ 150K_0402_5%

EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

+3VALW_PCH
RC17 @ 0_0603_5%
+3.3V_SPI

+3.3V_SPI
RC18 PCH_SPI_CS#0_R1 4.7K_0402_5%

+3.3V_SPI MOW WW06
RC19 PCH_SPI_D2_R1 1K_0402_5%
RC20 @ PCH_SPI_D3_R1 1K_0402_5%

[14] XDP_SPI_SI RC40 CMC@ PCH_SPI_D0_R1
[14] XDP_SPI_IO2 RC41 CMC@ PCH_SPI_D2_R1
RC40/41 place to within 1100 mil of SPIO_MOSI/SPI0_IO2 pin for XDP

PCH
PCH_SPI_D1_R1 RC22 33_0402_5% PCH_SPI_D1_R → PCH_SPI_D1_R [25]
PCH_SPI_D0_R1 RC23 33_0402_5% PCH_SPI_D0_R → PCH_SPI_D0_R [25]
PCH_SPI_CLK_R1 RC24 33_0402_5% PCH_SPI_CLK_R → PCH_SPI_CLK_R [25]
PCH_SPI_D3_R1 RC25 33_0402_5% PCH_SPI_D3_R
PCH_SPI_D2_R1 RC26 33_0402_5% PCH_SPI_D2_R

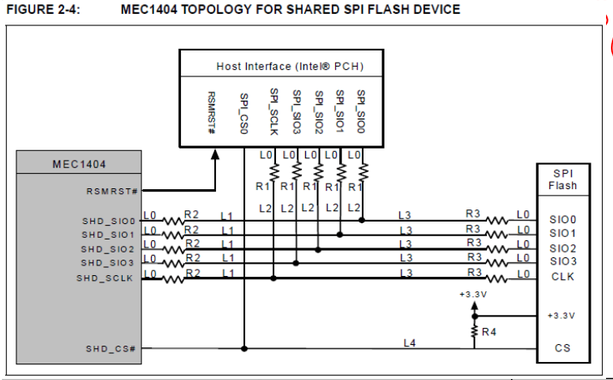
+3.3V_SPI
CC3 0.1U_0402_25V6

UC3 W25Q128FVSIQ_SO8
PCH_SPI_CS#0_R1 → CS#
PCH_SPI_D2_R RC176 15_0402_1% PCH_SPI_D2_0_R → WP#
PCH_SPI_D3_R RC177 15_0402_1% PCH_SPI_D3_0_R → HOLD#
GND
VCC
PCH_SPI_CLK_0_R RC178 15_0402_1% PCH_SPI_CLK_R → SCLK
PCH_SPI_D0_0_R RC179 15_0402_1% PCH_SPI_D0_R → SI/SIO0
PCH_SPI_D1_0_R RC180 15_0402_1% PCH_SPI_D1_R → SO/SIO1

128Mb Flash ROM

PCH_SPI_CLK_R
@EMI@ RC21 33_0402_5%
@EMI@ CC2 33P_0402_50V8J

FIGURE 2-4: MEC1404 TOPOLOGY FOR SHARED SPI FLASH DEVICE



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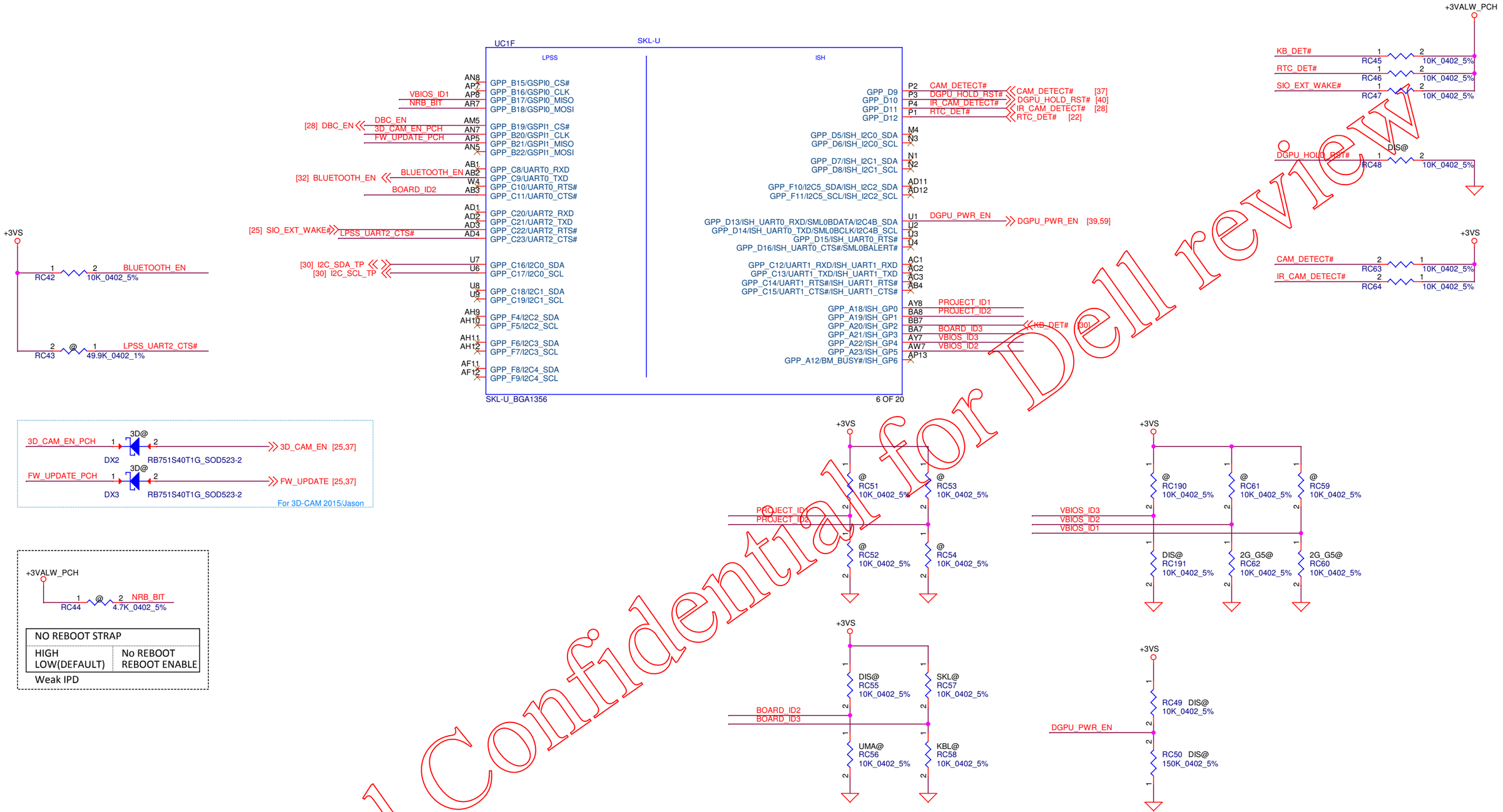
Compal Electronics, Inc.
Title: MCP(3/14)SPI,SMB,LPC
Size: Document Number: LA-D801P
Rev: A00
Date: Tuesday, June 21, 2016 Sheet 8 of 61



VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID3 (GPP_A22)	VBIOS_ID2 (GPP_A23)	VBIOS_ID1 (GPP_B17)
2G GDDR5	0	0	0
4G GDDR5	0	0	1
2G DDR3	0	1	0
Reserved	0	1	1

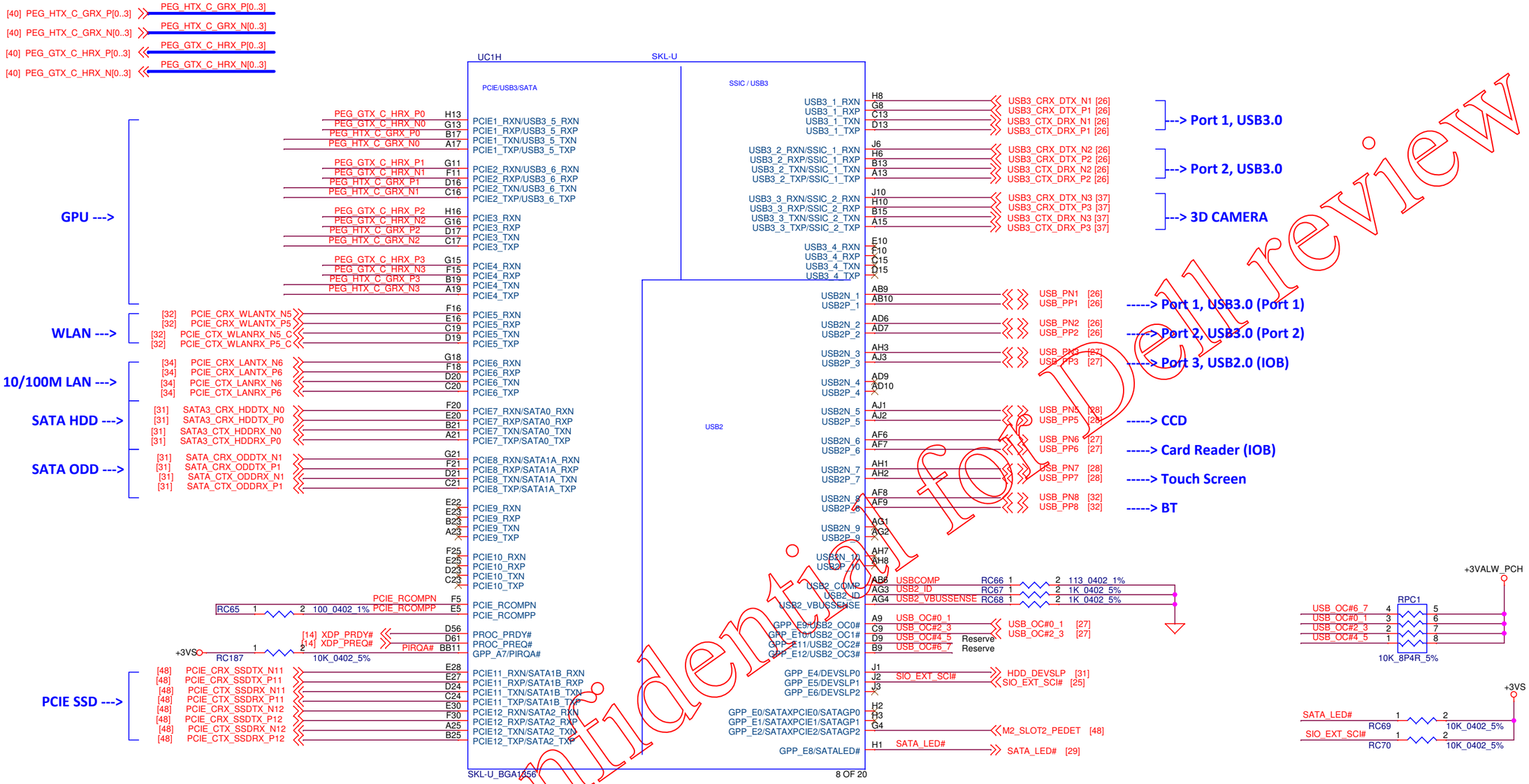
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: MCP(4/14)GSPI,I2C,UART,ISH

Size | Document Number: LA-D805P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 9 of 61

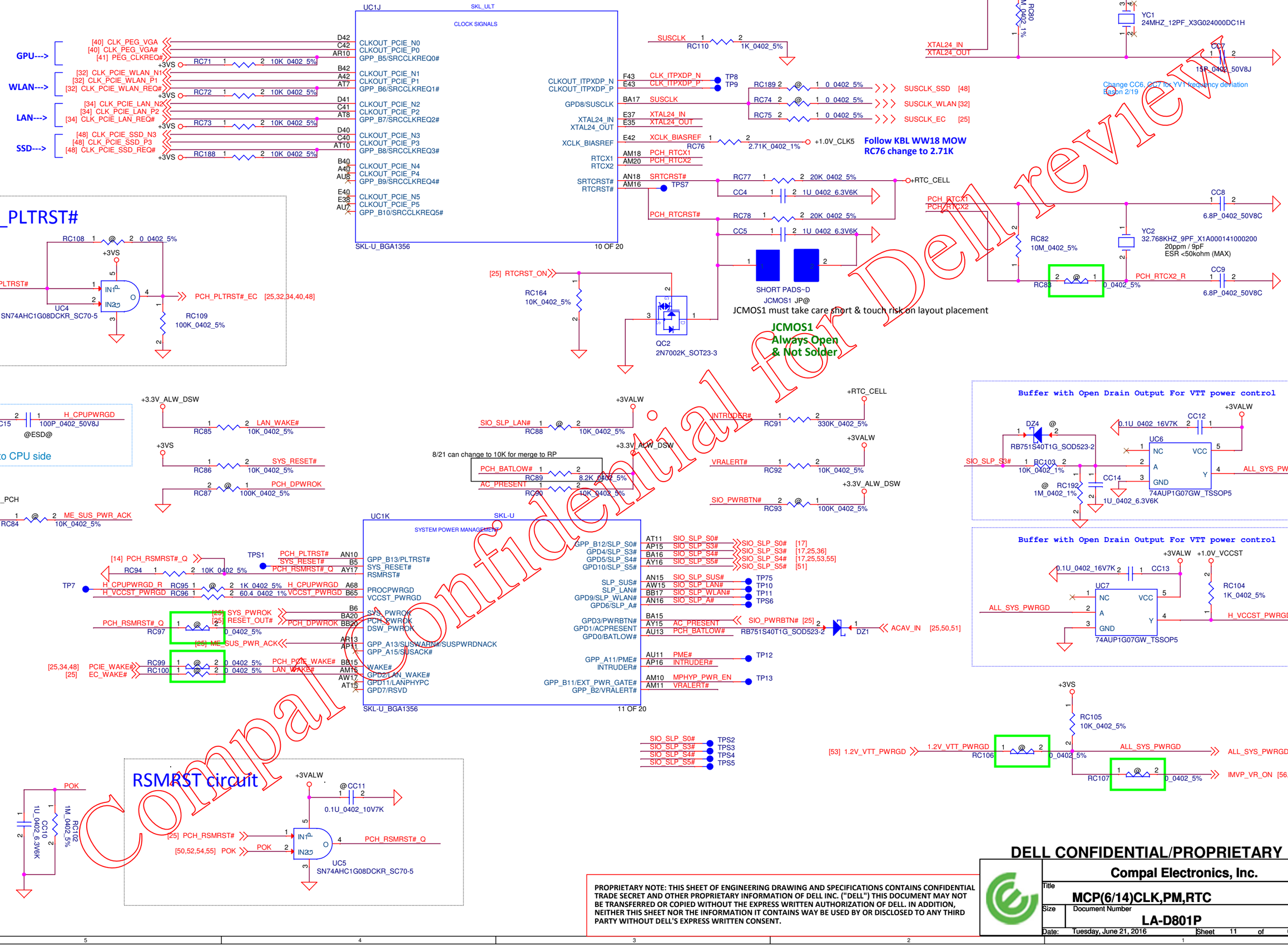


Compal Electronics, Inc.

Title: MCP(5/14)PCIE,USB,SATA

Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 10 of 61



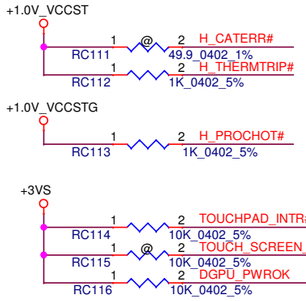
DELL CONFIDENTIAL/PROPRIETARY

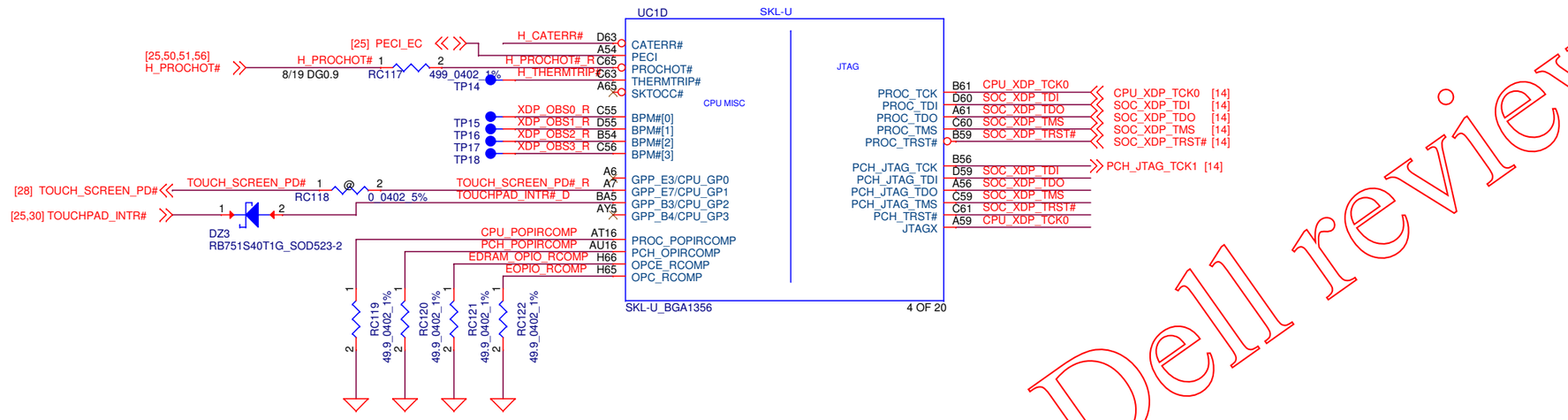
Compal Electronics, Inc.

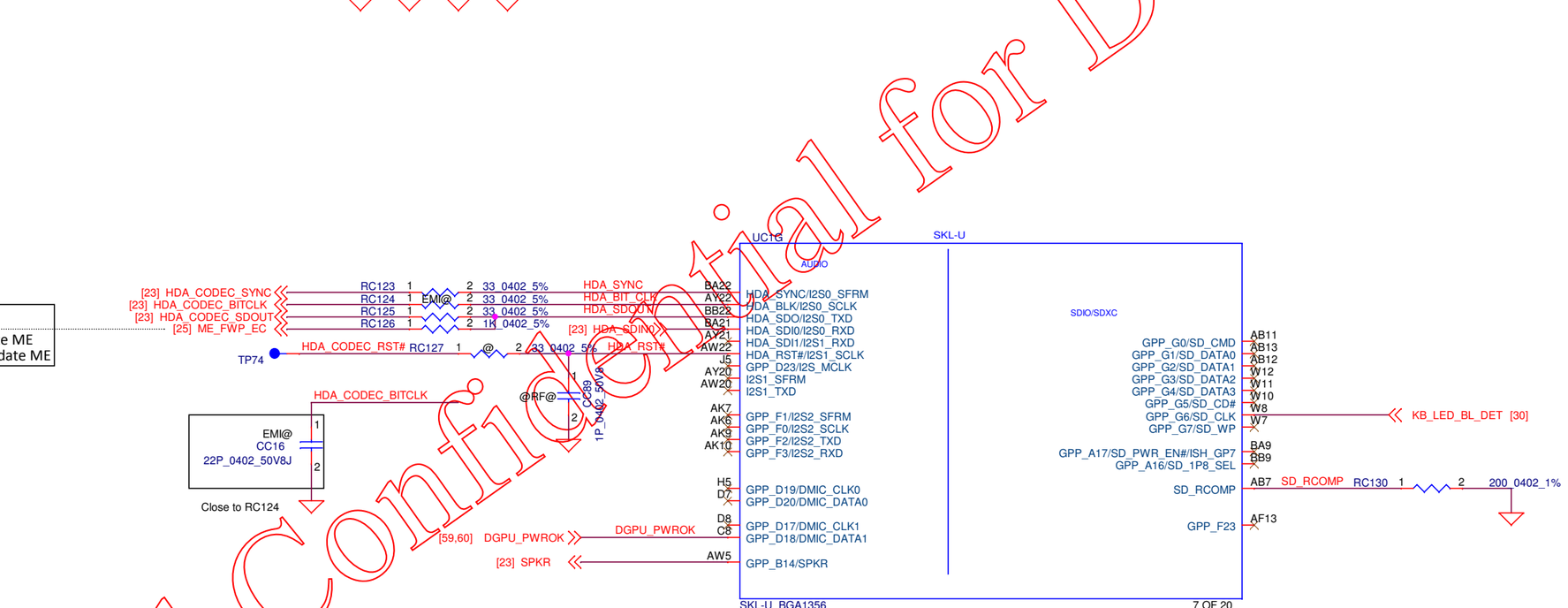
Title: MCP(6/14)CLK,PM,RTC

Size: | Document Number: LA-D801P | Rev: A00

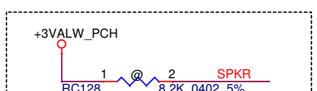
Date: Tuesday, June 21, 2016 | Sheet 11 of 61



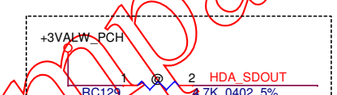




ME_FWP_EC
- LOW = ENABLE -->ME lock, can't update ME
- HIGH = DISABLE -->ME un-lock, can update ME



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE



Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

Compal Electronics, Inc.

Title: MCP(7/14)MISC,JTAG,HDA,SDIO

Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 12 of 61

RC131 1 @ 2 CFG0 10K_0402_1%

Stall reset sequence	
HIGH(DEFAULT)	No stall(Normal Operation)
LOW	stall

RC136 1 @ 2 CFG4 10K_0402_1%

eDP enable	
HIGH	Disabled
LOW(DEFAULT)	Enabled

CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin

RC132 1 @ 2 CFG1 10K_0402_1%
RC133 1 @ 2 CFG3 10K_0402_1%

RC134 2 1 CFG_RCOMP 49.9_0402_1%

UC1S SKL-U

RESERVED SIGNALS-1

[14] CFG0	CFG0 E68	CFG[0]
[14] CFG1	CFG1 B67	CFG[1]
[14] CFG2	D65	CFG[2]
[14] CFG3	CFG3 D67	CFG[3]
[14] CFG4	CFG4 E70	CFG[4]
[14] CFG5	C68	CFG[5]
[14] CFG6	D68	CFG[6]
[14] CFG7	C67	CFG[7]
[14] CFG8	F71	CFG[8]
[14] CFG9	G69	CFG[9]
[14] CFG10	F70	CFG[10]
[14] CFG11	G68	CFG[11]
[14] CFG12	H70	CFG[12]
[14] CFG13	G71	CFG[13]
[14] CFG14	H69	CFG[14]
[14] CFG15	G70	CFG[15]
[14] CFG16	E63	CFG[16]
[14] CFG17	F63	CFG[17]
[14] CFG18	E66	CFG[18]
[14] CFG19	F66	CFG[19]
	E60	CFG_RCOMP
[14] XDP_ITP_PMODE	E8	ITP_PMODE
	AY2	RSVD_AY2
	AY1	RSVD_AY1
	D1	RSVD_D1
	D3	RSVD_D3
	K46	RSVD_K46
	K45	RSVD_K45
	AL25	RSVD_AL25
	AL27	RSVD_AL27
	C71	RSVD_C71
	B70	RSVD_B70
	F60	RSVD_F60
	A52	RSVD_A52
TP19	BA70	RSVD_TP_BA70
TP20	BA68	RSVD_TP_BA68
	J71	RSVD_J71
	J68	RSVD_J68
	F65	VSS_F65
	G65	VSS_G65
	F61	RSVD_F61
	E61	RSVD_E61

SKL-U_BGA1356 19 OF 20

RSVD_TP_BB68	BB68	TP21
RSVD_TP_BB69	BB69	TP22
RSVD_TP_AK13	AK13	TP23
RSVD_TP_AK12	AK12	TP24
RSVD_BB2	BB2	
RSVD_BA3	BA3	
TP5	AU5	TP25
TP6	AT5	TP26
RSVD_D5	D5	
RSVD_D4	D4	
RSVD_B2	B2	
RSVD_C2	C2	
RSVD_B3	B3	
RSVD_A3	A3	
RSVD_AW1	AW1	
RSVD_E1	E1	
RSVD_E2	E2	
RSVD_BA4	BA4	
RSVD_BB4	BB4	
RSVD_A4	A4	
RSVD_C4	C4	
TP4	BB5	TP27
RSVD_A69	A69	
RSVD_B69	B69	
RSVD_AY3	AY3	
RSVD_D71	D71	
RSVD_C70	C70	
RSVD_C54	C54	
RSVD_D54	D54	
TP1	AY4	TP28
TP2	BB3	TP29
VSS_AY71	AY71	
ZVM#	AR56	
RSVD_TP_AW71	AW71	TP30
RSVD_TP_AW70	AW70	TP31
MSM#	AP56	
PROC_SELECT#	C64	

P.AR56 ZVM# for SKYLAKE-U 2+3e only

RC138 1 @ 2 100K_0402_5% +1.0V_VCCST

From WW48 MOW

Stuff 100k(RC138) for Cannonlake

Un-stuff 100k(RC138) for Skylake

+1.8V_PRIM

RC137 1 @ 2 0_0402_5%

UC1T SKL-U

SHARE

AW69	RSVD_AW69	RSVD_F6 F6
AW68	RSVD_AW68	RSVD_E3 E3
AU56	RSVD_AU56	RSVD_C11 C11
AW48	RSVD_AW48	RSVD_B11 B11
C7	RSVD_C7	RSVD_A11 A11
U12	RSVD_U12	RSVD_D12 D12
U11	RSVD_U11	RSVD_C12 C12
H11	RSVD_H11	RSVD_F52 F52

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Compal Electronics, Inc.

Title: MCP(8/14)CFG,RSVD

Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 13 of 61

Connector Less Routing Topology

DCI Link
RC142 need POP
RC146 need POP

+3.3V_SPI

RC139 1 CMC@ 2 1K_0402_5% XDP_SPI_SI

+1.0V_VCCSTG

Place to CPU side

RC140 2 CMC@ 1 51 0402 5% SOC_XDP_TMS
RC141 2 CMC@ 1 51 0402 5% SOC_XDP_TDI
RC142 2 CMC@ 1 51 0402 5% SOC_XDP_TDO

+1.0V_XDP

RC143 1 CMC@ 2 1K 0402 5% XDP_ITP_PMODE

Place to CPU side

RC144 2 @ 1 0 0402 5% XDP_PRSENT_CPU
RC145 2 @ 1 0 0402 5% XDP_PRSENT_PCH
RC146 2 CMC@ 1 51 0402 1% CPU_XDP_TCK0
RC147 2 @ 1 51 0402 5% PCH_JTAG_TCK1

[12] SOC_XDP_TDO → XDP_TDO → TPC1
[12] CPU_XDP_TCK0 → XDP_TCK0 → TPC2
[12] PCH_JTAG_TCK1 → XDP_TCK1 → TPC3
[12] SOC_XDP_TMS → XDP_TMS → TPC4

[12] SOC_XDP_TDI → XDP_TDI → TPC5
[12] SOC_XDP_TRST# → XDP_TRST# → TPC6
[13] XDP_ITP_PMODE → XDP_HOOK6 → TPC7

[8] XDP_SPI_SI → XDP_HOOK3 → TPC8
[8] XDP_SPI_IO2 → XDP_PRSENT_PCH → TPC9

CFG3 — RC175 1 CMC@ 2 0_0402_5% — XDP_PRSENT_CPU

[11] PCH_RSMRST#_Q — RC148 PCH_RSMRST#_Q 1 CMC@ 2 1K_0402_5% — XDP_HOOK0

PRIMARY CMC CONN

+1.0V_PRIM — RC149 1 CMC@ 2 0 0603 5% — +1.0V_XDP

[13] CFG0 → TPC10
[13] CFG1 → TPC11
[13] CFG2 → TPC12
[13] CFG3 → TPC13
[13] CFG4 → TPC14
[13] CFG5 → TPC15
[13] CFG6 → TPC16
[13] CFG7 → TPC17
[13] CFG17 → TPC18
[13] CFG16 → TPC19
[13] CFG8 → TPC20
[13] CFG9 → TPC21
[13] CFG10 → TPC22
[13] CFG11 → TPC23
[13] CFG12 → TPC24
[13] CFG13 → TPC25
[13] CFG14 → TPC26
[13] CFG15 → TPC27
[13] CFG19 → TPC28
[13] CFG18 → TPC29

TPC30 → XDP_PREQ# [10]
TPC31 → XDP_PRDY# [10]
TPC32 → XDP_HOOK0
TPC33 → XDP_PRSENT_CPU

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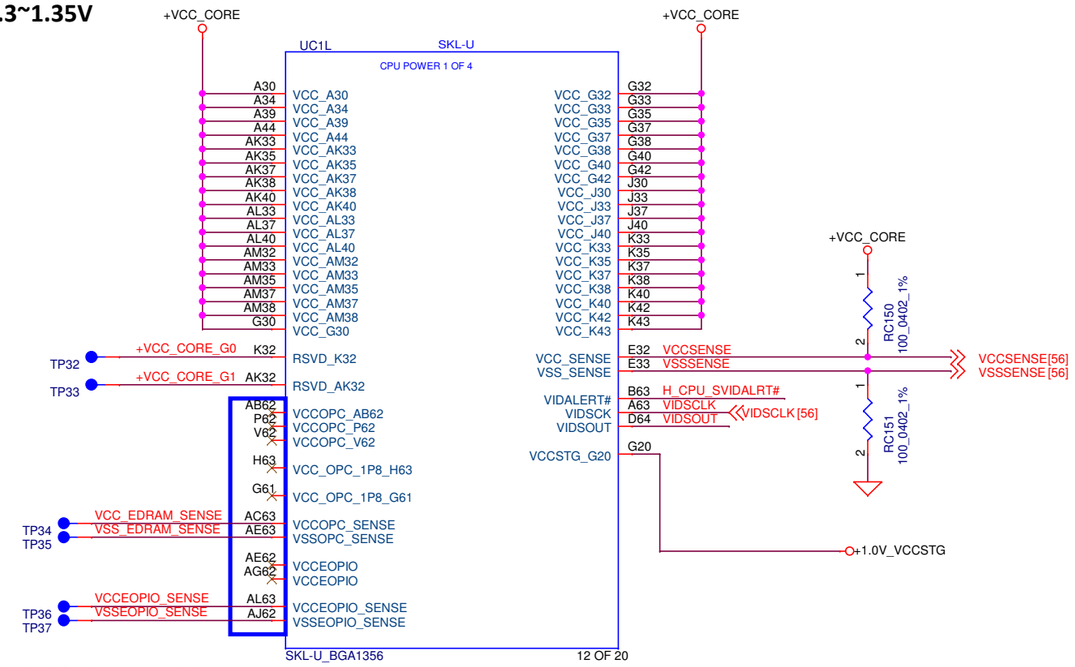
Compal Electronics, Inc.

Title: MCP(9/14)XDP
Size: Document Number: LA-D801P
Rev: A00
Date: Tuesday, June 21, 2016 Sheet 14 of 61

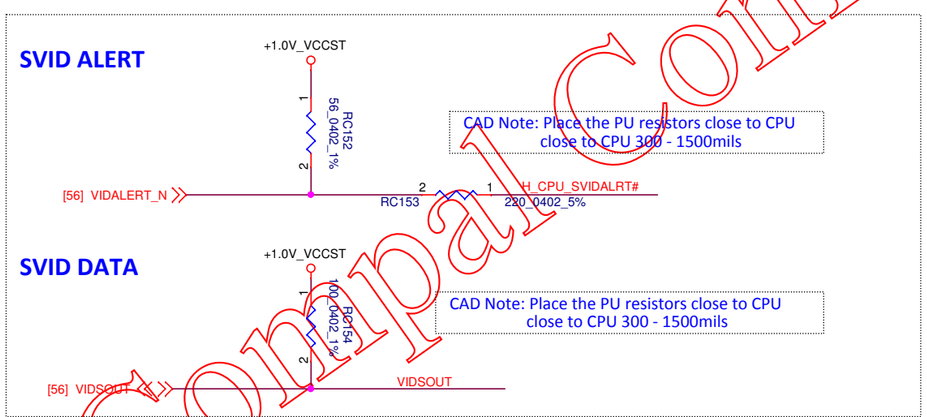
+VCC_CORE: 0.3~1.35V



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

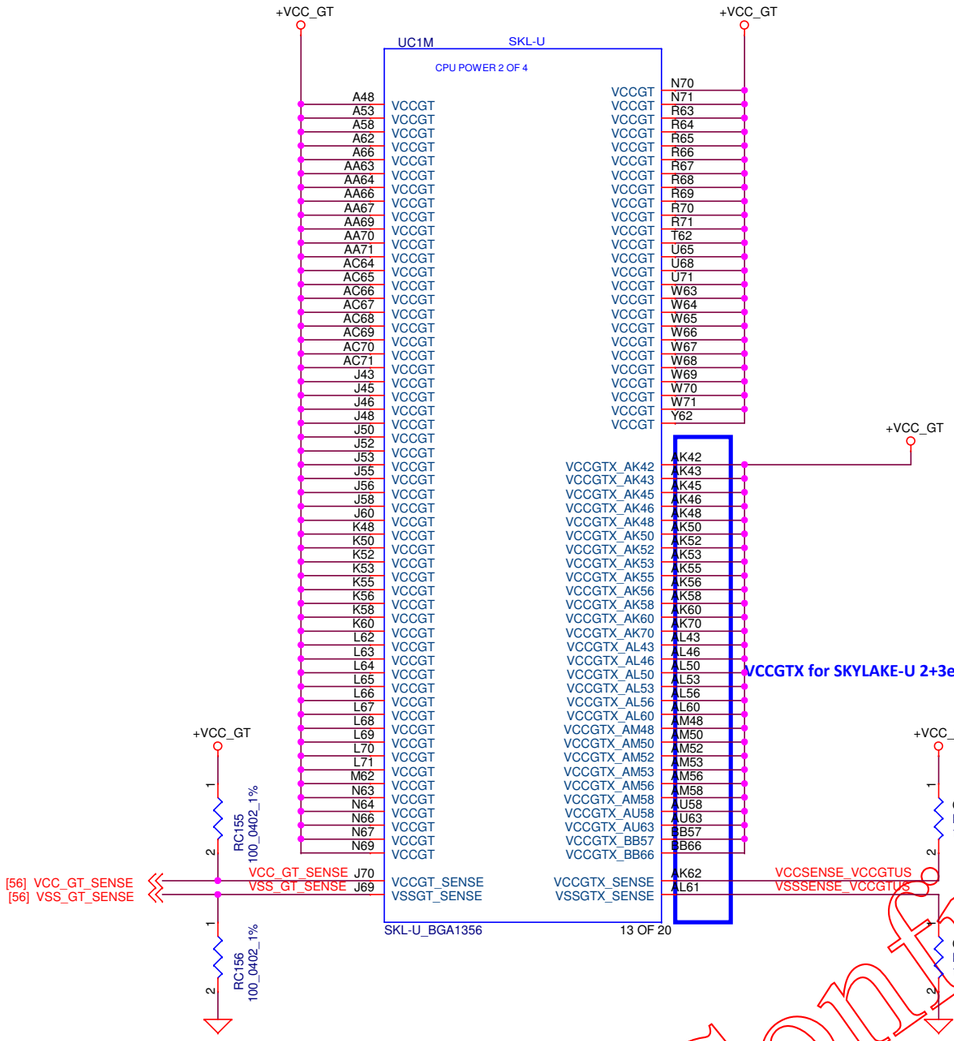
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: MCP(10/14)PWR-VCC CORE		
Size	Document Number: LA-D801P	Rev: A00
Date: Tuesday, June 21, 2016	Sheet 15 of 61	

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



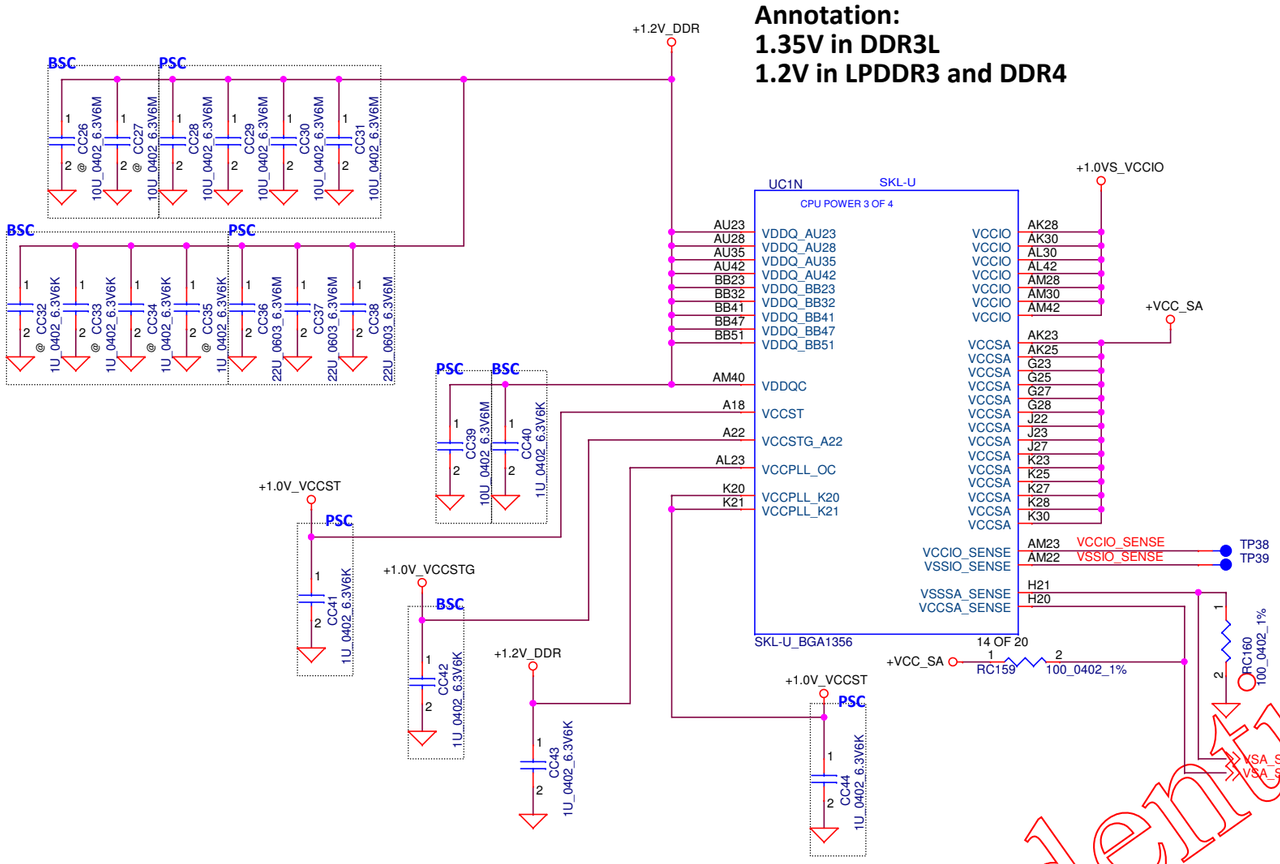
Compal Electronics, Inc.

Title: MCP(11/14)PWR-VCCGT

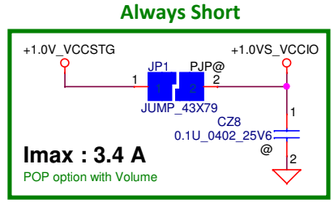
Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 16 of 61

Annotation:
1.35V in DDR3L
1.2V in LPDDR3 and DDR4



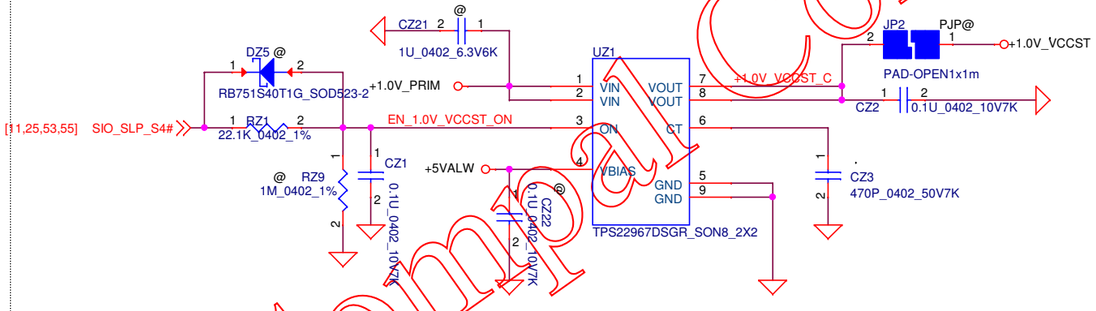
JP1
Always Short



+1.0V_VCCST source

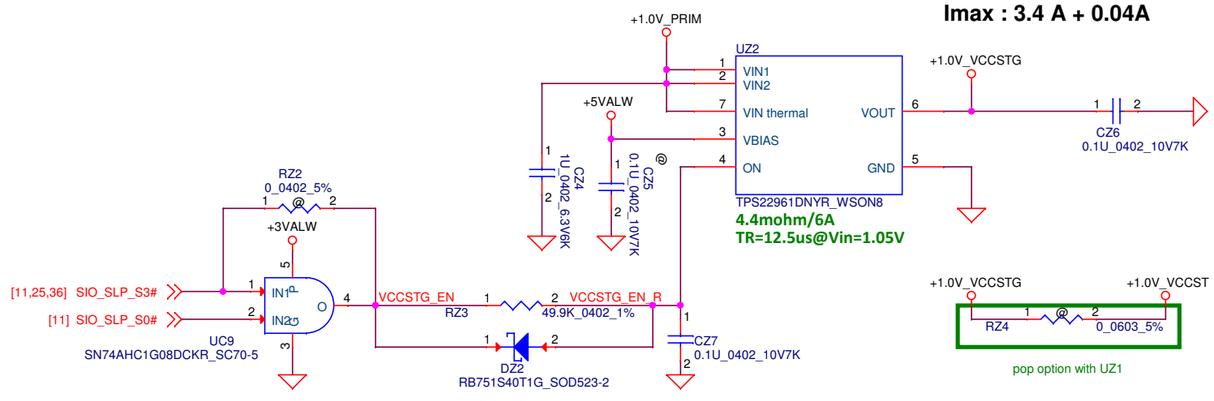
Imax : 0.24 A

JP2
Always Short



+1.0V_VCCSTG source

Imax : 3.4 A + 0.04A



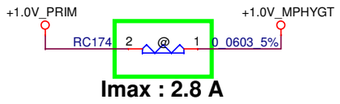
Compal Electronics, Inc.

Title: MCP(12/14)PWR-VCCIO,MEM

Size: | Document Number: LA-D805P | Rev: A00

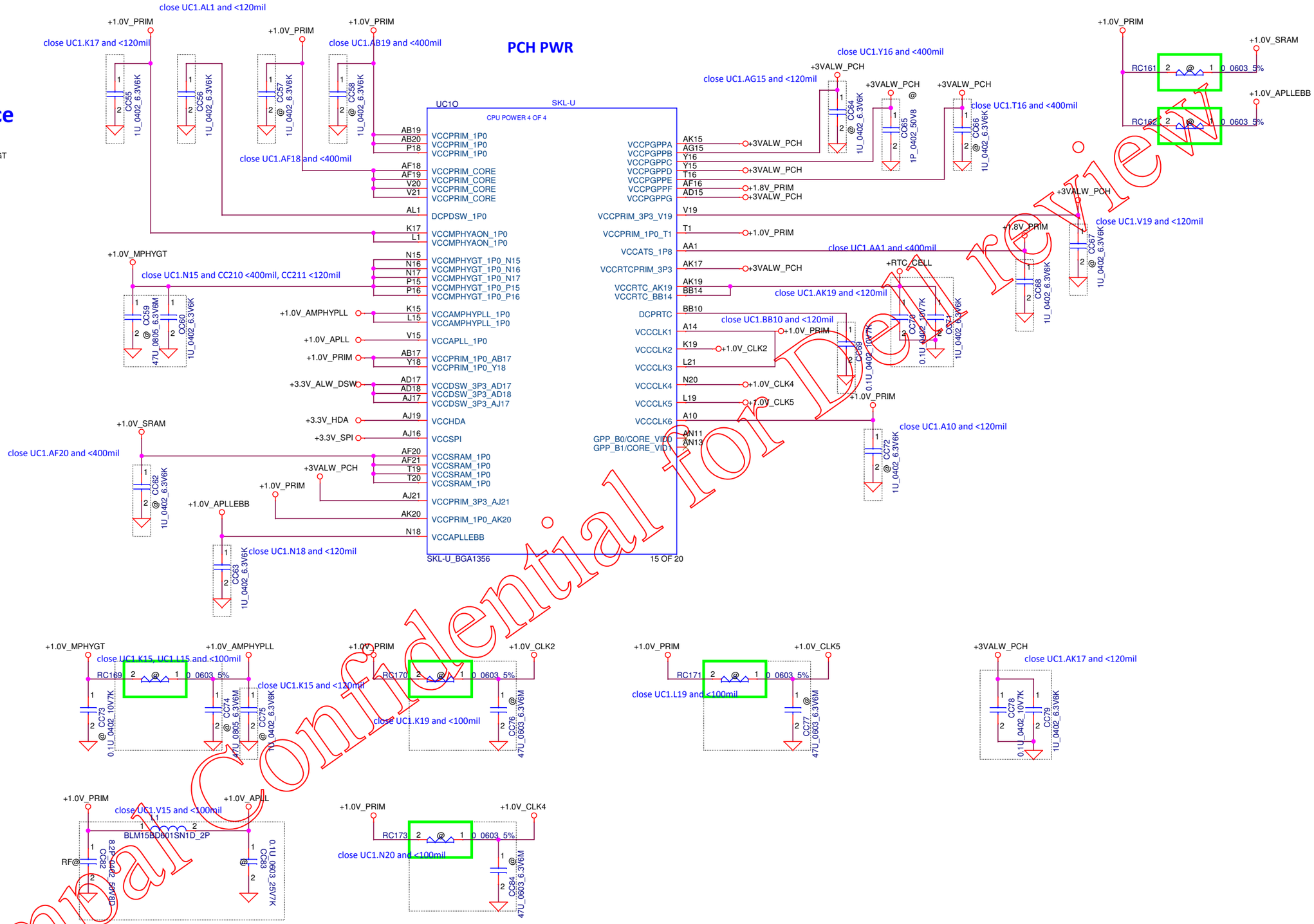
Date: Tuesday, June 21, 2016 | Sheet 17 of 61

+1.0V_MPHYGT source



Imax : 2.8 A

PCH PWR

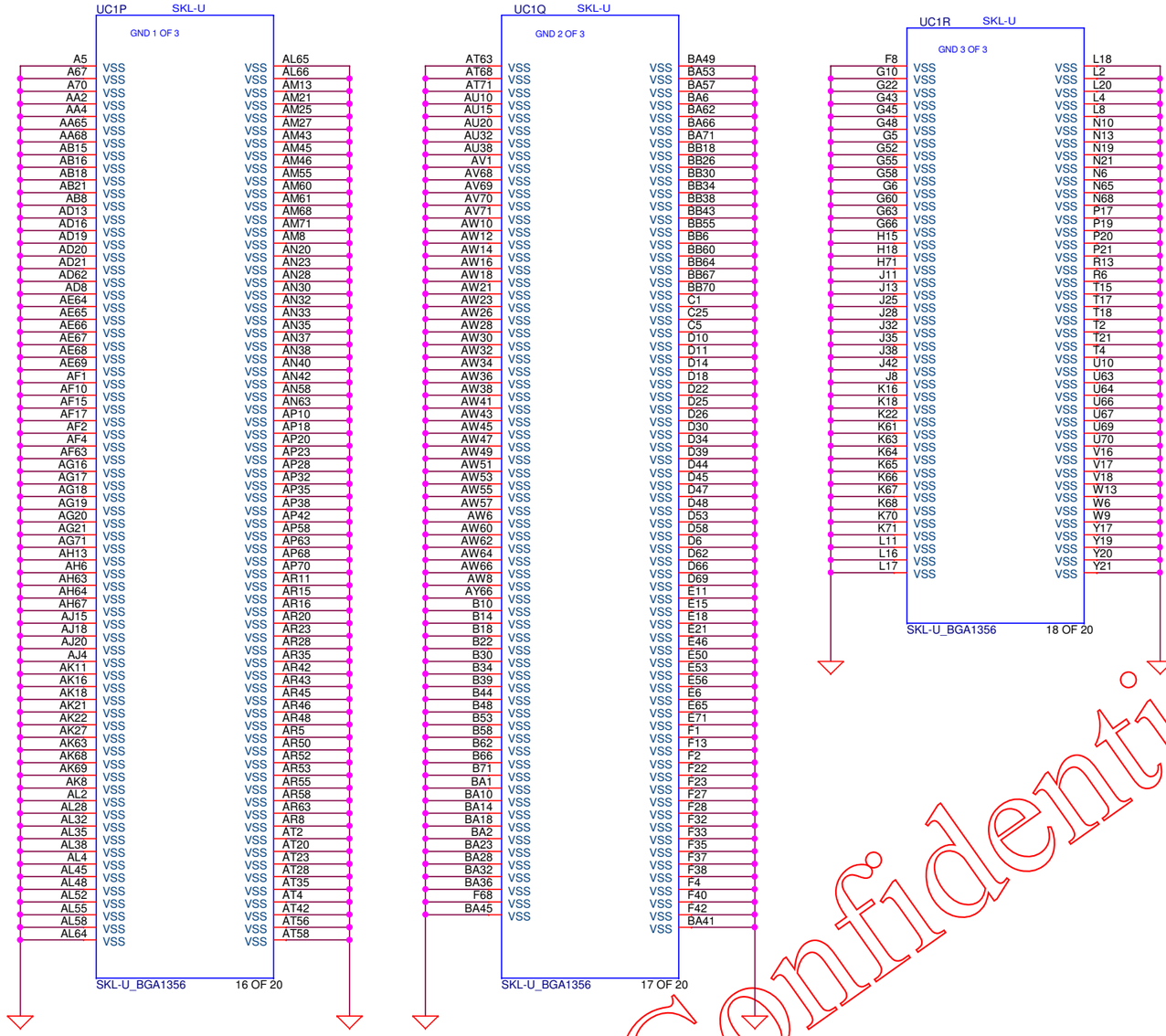


Compal Electronics, Inc.

Title: MCP(13/14)PCH PWR

Size: | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 18 of 61



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

DELL CONFIDENTIAL/PROPRIETARY

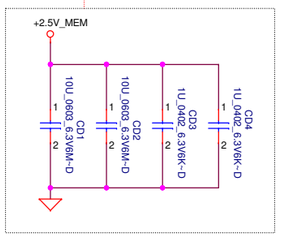
Compal Electronics, Inc.

Title: MCP(14/14)VSS

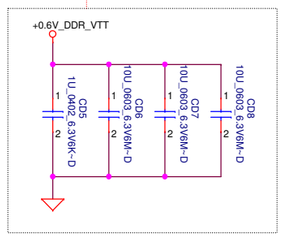
Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 19 of 61

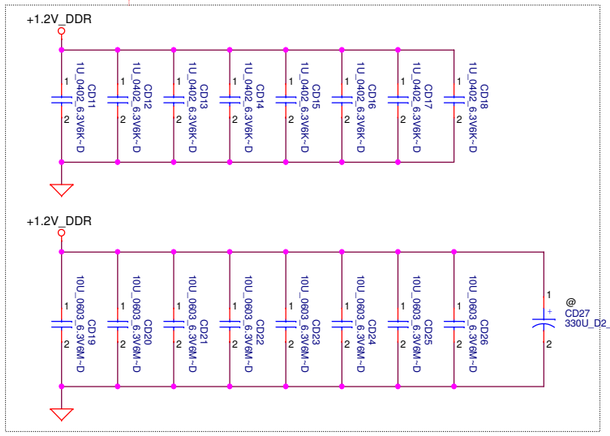
Layout Note:
Place near JDIMM1.257,259



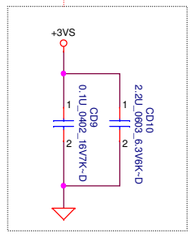
Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1

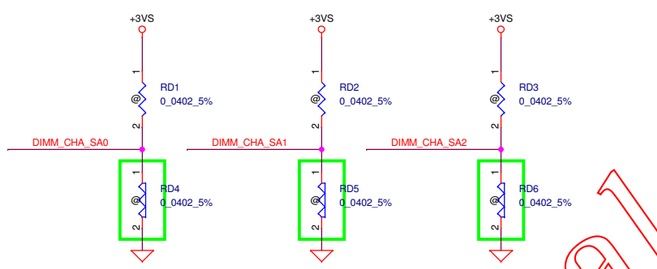


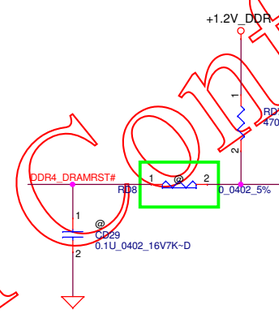
Layout Note:
Place near JDIMM1.255

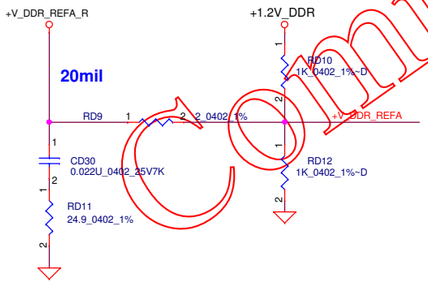


[7] DDR_A_D[0..63]
[7] DDR_A_MA[0..13]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_DQS[0..7]

All VREF traces should have 10 mil trace width







Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **DDR4 DIMMA_RVS**

Size: B | Document Number: **LA-D801P** | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 20 of 61

Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2

[7] DDR_B_D[0..63]
[7] DDR_B_MA[0..13]
[7] DDR_B_DQS#[0..7]
[7] DDR_B_DQS[0..7]

+0.6V_DDR_VTT
CD31 1U_0402_6.3V6K~D
CD32 10U_0603_6.3V6M~D
CD33 10U_0603_6.3V6M~D
CD34 10U_0603_6.3V6M~D

+2.5V_MEM
CD35 1U_0402_6.3V6K~D
CD36 10U_0603_6.3V6M~D
CD37 10U_0603_6.3V6M~D
CD38 10U_0603_6.3V6M~D

+3VS
CD39 0.1U_0402_16V7K~D
CD40 2.2U_0603_6.3V6K~D

+1.2V_DDR
CD41 1U_0402_6.3V6K~D
CD42 1U_0402_6.3V6K~D
CD43 1U_0402_6.3V6K~D
CD44 1U_0402_6.3V6K~D
CD45 1U_0402_6.3V6K~D
CD46 1U_0402_6.3V6K~D
CD47 1U_0402_6.3V6K~D
CD48 1U_0402_6.3V6K~D

+1.2V_DDR
CD49 10U_0603_6.3V6M~D
CD50 10U_0603_6.3V6M~D
CD51 10U_0603_6.3V6M~D
CD52 10U_0603_6.3V6M~D
CD53 10U_0603_6.3V6M~D
CD54 10U_0603_6.3V6M~D
CD55 10U_0603_6.3V6M~D
CD56 10U_0603_6.3V6M~D
CD57 330U_D2_2V_Y

+3VS
RD13 0_0402_5%
RD14 0_0402_5%
RD15 0_0402_5%
DIMM_CHB_SA0
DIMM_CHB_SA1
DIMM_CHB_SA2
RD16 0_0402_5%
RD17 0_0402_5%
RD18 0_0402_5%

+V_DDR_REFB_R
20mil
RD19 2_0402_1%
+1.2V_DDR
RD20 1K_0402_1%~D
+V_DDR_REFB
RD21 1K_0402_1%~D
CD59 0.022U_0402_25V7K
RD22 24.9_0402_1%

+1.2V_DDR
JDIMM2 CONN@
+1.2V_DDR

		1				2	
DDR_B_D13		3	VSS1		VSS2	4	DDR_B_D9
		5	DQ5		DQ4	6	
DDR_B_D12		7	VSS3		VSS4	8	DDR_B_D8
		9	DQ1		DQ0	10	
DDR_B_DQS#1		11	VSS5		VSS6	12	
DDR_B_DQS1		13	DQS0_c	DM0_n/DBI0_n		14	
		15	DQS0_t		VSS7	16	DDR_B_D14
DDR_B_D15		17	VSS8		DQ6	18	
		19	DQ7		VSS9	20	DDR_B_D11
DDR_B_D10		21	VSS10		DQ2	22	
		23	DQ3		VSS11	24	DDR_B_D4
DDR_B_D1		25	VSS12		DQ12	26	
		27	DQ13		VSS13	28	DDR_B_D0
DDR_B_D5		29	VSS14		DQ8	30	
		31	DQ9		VSS15	32	DDR_B_DQS#0
		33	VSS16		DQS1_c	34	DDR_B_DQS0
		35	DM1_n/DBI_n		DQS1_t	36	
DDR_B_D7		37	VSS17		VSS18	38	DDR_B_D3
		39	DQ15		DQ14	40	
DDR_B_D6		41	VSS19		VSS20	42	DDR_B_D2
		43	DQ10		DQ11	44	
DDR_B_D16		45	VSS21		VSS22	46	DDR_B_D21
		47	DQ21		DQ20	48	
DDR_B_D17		49	VSS23		VSS24	50	DDR_B_D20
		51	DQ17		DQ16	52	
DDR_B_DQS#2		53	VSS25		VSS26	54	
DDR_B_DQS2		55	DQS2_c	DM2_n/DBI2_n		56	
		57	DQS2_t		VSS27	58	DDR_B_D23
DDR_B_D19		59	VSS28		DQ22	60	
		61	DQ23		VSS29	62	DDR_B_D18
DDR_B_D22		63	VSS30		DQ18	64	
		65	DQ19		VSS31	66	DDR_B_D25
DDR_B_D29		67	VSS32		DQ28	68	
		69	DQ29		VSS33	70	DDR_B_D28
DDR_B_D24		71	VSS34		DQ24	72	
		73	DQ25		VSS35	74	DDR_B_DQS#3
		75	VSS36		DQS3_c	76	DDR_B_DQS3
		77	DM3_n/DBI3_n		DQS3_t	78	
DDR_B_D26		79	VSS37		VSS38	80	DDR_B_D31
		81	DQ30		DQ31	82	
DDR_B_D30		83	VSS39		VSS40	84	DDR_B_D27
		85	DQ26		DQ27	86	
		87	VSS41		VSS42	88	
		89	CB5/NC		CB4/NC	90	
		91	VSS43		VSS44	92	
		93	CB1/NC		CB0/NC	94	
		95	VSS45		VSS46	96	
		97	DQS8_c	DM8_n/DBI_n/NC		98	
		99	DQS8_t		VSS47	100	
		101	VSS48		CB6/NC	102	
		103	CB2/NC		VSS49	104	
		105	VSS50		CB7/NC	106	
		107	CB3/NC		VSS51	108	
		109	VSS52		RESET_n	110	DDR4_DRAMRST#
[7] DDR_B_CKE0	DDR_B_CKE0	111	CKE0		CKE1	112	DDR_B_CKE1
		113	VDD1		VDD2	114	
[7] DDR_B_BG1	DDR_B_BG1	115	BG1		ACT_n	116	DDR_B_ALERT#
[7] DDR_B_BG0	DDR_B_BG0	117	BG0		ALERT_n	118	
	DDR_B_MA12	119	VDD3		VDD4	120	DDR_B_MA11
	DDR_B_MA9	121	A12		A11	122	DDR_B_MA7
		123	A9		A7	124	
	DDR_B_MA8	125	VDD5		VDD6	126	DDR_B_MA5
	DDR_B_MA6	127	A8		A5	128	DDR_B_MA4
		129	A6		A4	130	
	DDR_B_MA3	131	VDD7		VDD8	132	DDR_B_MA2
	DDR_B_MA1	133	A3		A2	134	
		135	A1		EVENT_n/NF	136	
[7] DDR_B_CLK0	DDR_B_CLK0	137	VDD9		VDD10	138	DDR_B_CLK1
[7] DDR_B_CLK#0	DDR_B_CLK#0	139	CK0_t		CK1_t/NF	140	DDR_B_CLK#1
		141	CK0_c		CK1_c/NF	142	
		143	VDD11		VDD12	144	DDR_B_MA0
[7] DDR_B_PAR	DDR_B_PAR	145	PARITY		A0	146	DDR_B_MA10
[7] DDR_B_BS1	DDR_B_BS1	147	BA1		A10/AP	148	
		149	VDD13		VDD14	150	DDR_B_BS0
[7] DDR_B_CS#0	DDR_B_CS#0	151	CS0_n		BA0	152	DDR_B_RAS#
[7] DDR_B_WE#	DDR_B_WE#	153	WE_n/A14		RAS_n/A16	154	
		155	VDD15		VDD16	156	DDR_B_CAS#
[7] DDR_B_ODT0	DDR_B_ODT0	157	ODT0		CAS_n/A15	158	DDR_B_MA13
[7] DDR_B_CS#1	DDR_B_CS#1	159	CS1_n		A13	160	
		161	VDD17		VDD18	162	
[7] DDR_B_ODT1	DDR_B_ODT1	163	ODT1		C0/CS2_n/NC	164	TP43
		165	VDD19		VREFCA	166	DIMM_CHB_SA2
TP42		167	C1, CS3_n,NC		SA2	168	+V_DDR_REFB
	DDR_B_D32	169	VSS53		VSS54	170	DDR_B_D36
		171	DQ37		DQ36	172	
	DDR_B_D33	173	VSS55		VSS56	174	DDR_B_D37
		175	DQ33		DQ32	176	
	DDR_B_DQS#4	177	VSS57		VSS58	178	
	DDR_B_DQS4	179	DQS4_c	DM4_n/DBI4_n		180	+1.2V_DDR
		181	DQS4_t		VSS59	182	DDR_B_D39
	DDR_B_D34	183	VSS60		DQ39	184	
		185	DQ38		VSS61	186	DDR_B_D38
	DDR_B_D35	187	VSS62		DQ35	188	
		189	DQ34		VSS63	190	DDR_B_D40
	DDR_B_D44	191	VSS64		DQ45	192	
		193	DQ44		VSS65	194	DDR_B_D41
	DDR_B_D45	195	VSS66		DQ41	196	
		197	DQ40		VSS67	198	DDR_B_DQS#5
		199	VSS68		DQS5_c	200	DDR_B_DQS5
+1.2V_DDR		201	DM5_n/DBI5_n		DQS5_t	202	
	DDR_B_D43	203	VSS69		VSS70	204	DDR_B_D46
		205	DQ46		DQ47	206	
	DDR_B_D42	207	VSS71		VSS72	208	DDR_B_D47
		209	DQ42		DQ43	210	
	DDR_B_D52	211	VSS73		VSS74	212	DDR_B_D49
		213	DQ52		DQ53	214	
	DDR_B_D53	215	VSS75		VSS76	216	DDR_B_D48
		217	DQ49		DQ48	218	
	DDR_B_DQS#6	219	VSS77		VSS78	220	
	DDR_B_DQS6	221	DQS6_c	DM6_n/DBI6_n		222	+1.2V_DDR
		223	DQS6_t		VSS79	224	DDR_B_D55
	DDR_B_D50	225	VSS80		DQ54	226	
		227	DQ55		VSS81	228	DDR_B_D54
	DDR_B_D51	229	VSS82		DQ50	230	
		231	DQ51		VSS83	232	DDR_B_D56
	DDR_B_D61	233	VSS84		DQ60	234	
		235	DQ61		VSS85	236	DDR_B_D57
	DDR_B_D60	237	VSS86		DQ57	238	
		239	DQ56		VSS87	240	DDR_B_DQS#7
+1.2V_DDR		241	VSS88		DQS7_c	242	DDR_B_DQS7
		243	DM7_n/DBI7_n		DQS7_t	244	
	DDR_B_D59	245	VSS89		VSS90	246	DDR_B_D63
		247	DQ62		DQ63	248	
	DDR_B_D58	249	VSS91		VSS92	250	DDR_B_D62
		251	DQ58		DQ59	252	
		253	VSS93		VSS94	254	PCH_SMBDATA
[8,20] PCH_SMBCLK	PCH_SMBCLK	255	SCL		SDA	256	DIMM_CHB_SA0
+3VS		257	VDDSPD		SA0	258	
+2.5V_MEM		259	VPP1		VTT	260	DIMM_CHB_SA1
		261	VPP2		SA1	262	
			GND1		GND2		

DEREN_40-42261-26001RHF
DEREN_40-42261-26001RHF

DDR4_DRAMRST# [20]
DDR_B_CKE1 [7]
DDR_B_ACT# [7]
DDR_B_ALERT# [7]
RD24 2_240_0402_1% 1 +1.2V_DDR
DDR_B_CLK1 [7]
DDR_B_CLK#1 [7]
DDR_B_BS0 [7]
DDR_B_RAS# [7]
DDR_B_CAS# [7]
+V_DDR_REFB
CD58 0.1U_0402_16V7K~D
+1.2V_DDR
PCH_SMBDATA [8,20]
+0.6V_DDR_VTT

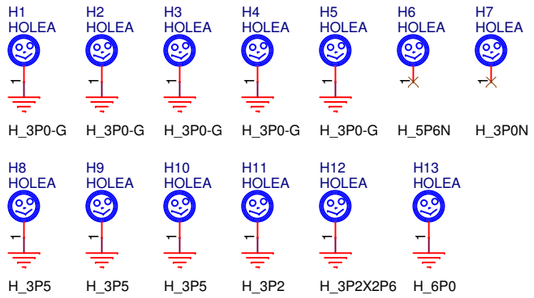
All VREF traces should have 10 mil trace width

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

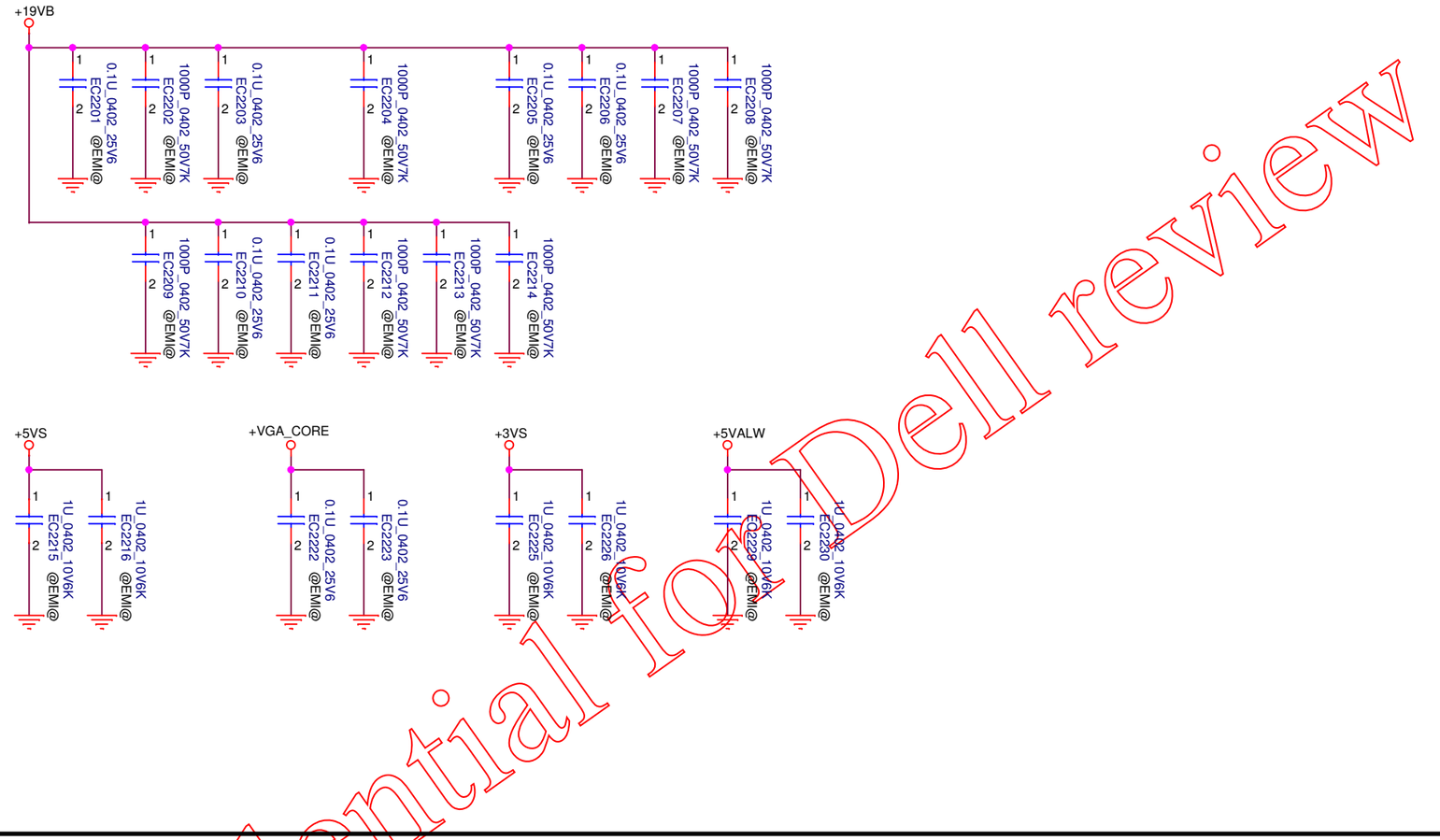
Compal Electronics, Inc.	
Title	DDR4 DIMMB_STD
Size	Document Number: LA-D801P
Rev	A00
Date: Tuesday, June 21, 2016	Sheet 21 of 61

Main Func = Other

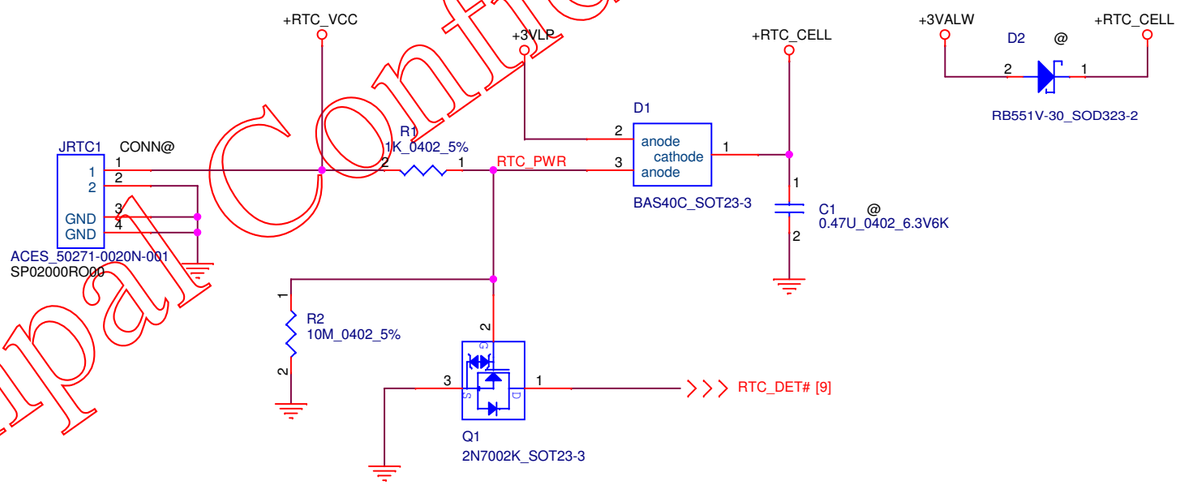
Screw hole/FD



Mind the voltage rating of the caps.



Main Func = RTC



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: RTC/Screw hole/EMI cap			
Size: D	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 22 of 61		

Main Func = Audio

+5VS → RA1 2A 0_0805_5% → +5V_PVDD
CA1 10U_0603_10V6M, CA2 .1U_0402_16V7K, CA3 10U_0603_10V6M, CA4 .1U_0402_16V7K

Layout Note: Close pin41

Layout Note: Close pin46

+3VS → RA2 25mA 0_0402_5% → +3V_DVDD
CA5 4.7U_0603_6.3V6K, CA6 .1U_0402_16V7K

Close pin9

[28] DMIC_DATA_EDP → RA42 33_0402_5% → DMIC_DATA
[28] DMIC_CLK_EDP → L5 EMI@ BLM15PX221SN1D_2P → DMIC_CLK
@EMI@ CA9 6.8P_0402_50V

moat

+5V_AVDD → RA44 0_0603_5% → +5VS
CA10 4.7U_0603_10V6K, CA11 .1U_0402_16V7K → AUD_AGND

Place close to Pin 26

+1.8V_PRIM → QA1 LN2306LT1G_SOT23-3 → +3VS

moat

+1.8V_AVDD → RA5 0_0402_5%
CA12 4.7U_0603_6.3V6K

Close pin40

AUD_AGND

+1.8V_CPVDD → RA6 0_0402_5%
CA13 4.7U_0603_6.3V6K, CA14 .1U_0402_16V7K

Close pin36

CA17 .1U_0402_16V7K → +3V_DVDD → +5V_PVDD
CA15 4.7U_0603_6.3V6K, CA16 .1U_0402_16V7K

+5V_AVDD, +1.8V_AVDD, +1.8V_CPVDD

Delete HDA_RST

UA1 ALC3246-CG_MQFN48_6X6 / ALC3246-CG_MQFN48_6X6-S

Pin	Name
1	DVDD
9	DVDD-IO
41	PVDD1
46	PVDD2
26	AVDD1
40	AVDD2
36	CPVDD
11	I2C_SDA
12	I2C_SCL
10	SYNC
6	BIT-CLK
5	SDATA-OUT
8	SDATA-IN
4	EAPD/DC DET
2	GPIO0/DMIC-DATA12
3	GPIO1/DMIC-CLK
47	PDB
48	SPDIFO/GPIO2/DMIC-DATA-34/DMIC-CLK-In/MIC-OPI
27	LDO1-CAP
39	LDO2-CAP
7	LDO3-CAP
42	SPK-L+
43	SPK-L-
44	SPK-R-
45	SPK-R+
13	HP/LINE1_JD1
14	MIC2/LINE2_JD2
15	SPDIFO/FRONT JD3/GPIO3
31	LINE1-VREFO-L
30	LINE1-VREFO-R
29	MIC2-VREFO
28	VREF
35	CBN
37	CBP
20	5VSTB
34	CPVEE
17	MIC2-L/RING2
18	MIC2-R/SLEEVE
19	MIC_CAP
24	LINE2-L
23	LINE2-R
22	LINE1-L
21	LINE1-R
16	PCBEEP
32	HP-OUT-L
33	HP-OUT-R
25	AVSS1
38	AVSS2
49	THERMAL PAD

[12] HDA_CODEC_SYNC, [12] HDA_CODEC_BITCLK, [12] HDA_CODEC_SDOUT, [12] HDA_SDIN0 → RA7 33_0402_5% → HDA_CODEC_SDIN0

+3V_DVDD → RA8 100K_0402_5%, RA9 0_0402_5% → DMIC_DATA, DMIC_CLK

[25] EC_MUTE#

AUD_AGND → RA41 100K_0402_5%
CA20 4.7U_0603_6.3V6K LDO1_CAP
CA21 10U_0603_6.3V6M LDO2_CAP
CA22 4.7U_0603_6.3V6K LDO3_CAP

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

[23] AUD_SPK_L+ → AUD_SPK_L+
[23] AUD_SPK_L- → AUD_SPK_L-
[23] AUD_SPK_R- → AUD_SPK_R-
[23] AUD_SPK_R+ → AUD_SPK_R+

AUD_SENSE_A

AUD_SENSE → RA10 200K_0402_1%

Layout Note: Place close to Pin 13

+3V_DVDD → RA3 100K_0402_5% AUD_SENSE_A → moat → CA7 .1U_0402_16V7K → AUD_AGND

AUD_SENSE 10 mils → RA39 0_0603_5% → 10 mils → JACK_PLUG [24]

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

[23] AUD_SPK_R+ → RA13 EMI@ BLM15PD800SN1D_2P → AUD_SPK_R+_C
[23] AUD_SPK_R- → RA14 EMI@ BLM15PD800SN1D_2P → AUD_SPK_R-_C
[23] AUD_SPK_L+ → RA15 EMI@ BLM15PD800SN1D_2P → AUD_SPK_L+_C
[23] AUD_SPK_L- → RA16 EMI@ BLM15PD800SN1D_2P → AUD_SPK_L-_C

JSPK1 CONN@ (1, 2, 3, 4, 5 GND1, 6 GND2)
JXT_WB247H-004S10M
SP020017K10

CA27, CA28, CA29, CA30 EMI@ 1000P_0402_50V7K

DA1, DA2 AZ5125-02S.R7G_SOT23-3 @ESD@

ZT4 AUD_SPK_R+_C
ZT5 AUD_SPK_R-_C
ZT6 AUD_SPK_L+_C
ZT7 AUD_SPK_L-_C

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

+3VALW, +RTC_CELL → moat → RA11 0_0402_5%, RA12 0_0402_5% → V3D3_STB

CPVEE → CA25 1U_0603_16V7

AUD_AGND → CA23 2.2U_0603_6.3V6K, CA24 1U_0603_16V7

RING2 [24], SLEEVE [24]

Layout Note:
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

MIC_CAP → CA26 10U_0603_6.3V6M → AUD_AGND

LINE1_L [24], LINE1_R [24]

AUD_PC_BEEP

AUD_HP1_JACK_L [24], AUD_HP1_JACK_R [24]

AUD_AGND

moat

RA17 0_0402_5%, RA18 0_0402_5% → AUD_AGND

RA22 0_0805_5% → AUD_AGND

Layout Note:
Tied at point only under Codec or near the Codec

Place on the moat between GND & GNDA.

AUD_AGND → EC2301 0.1U_0402_25V6 @EMI@, EC2302 0.1U_0402_25V6 @EMI@

[12] SPKR, [25] BEEP → DA3 BAT54C-7-F_SOT23-3

AUD_PC_BEEP_C → RA23 1K_0402_5% → CA31 0.1U_0402_16V7K → AUD_PC_BEEP

RA24 10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

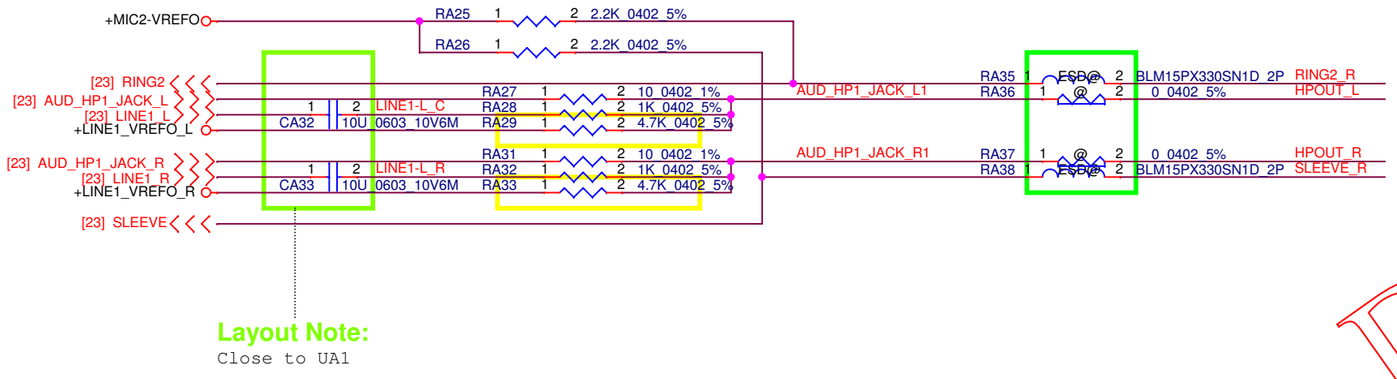
Compal Electronics, Inc.

Title: Audio Codec ALC3246

Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 23 of 61

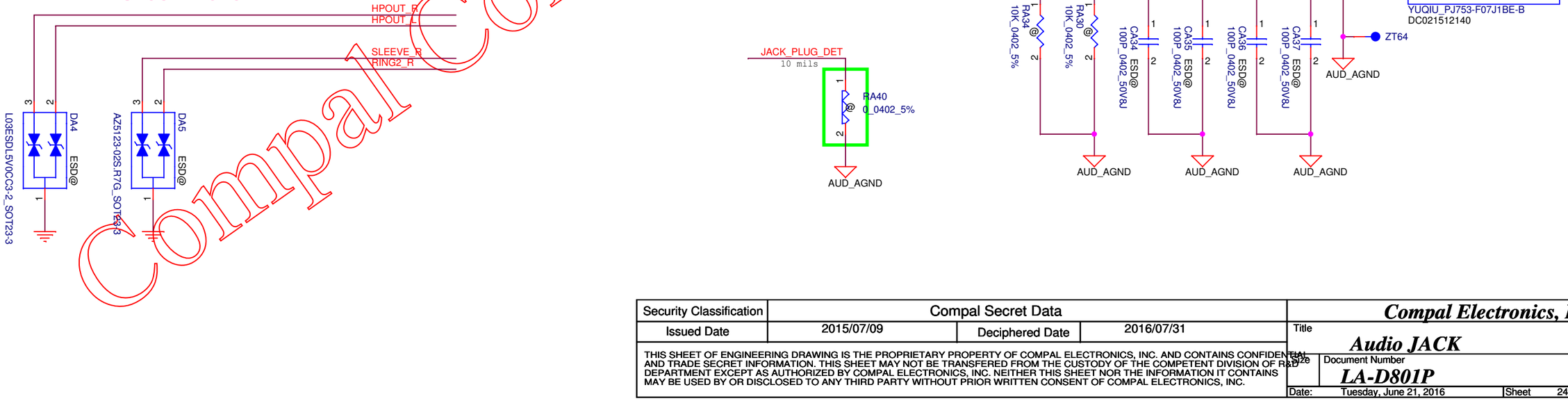
Main Func = Audio Jack



Universal Jack
(Global Headset Jack + mic phone in + line in support)

Layout Note:
Close to UA1

Main Func = Audio Jack



Universal Jack
(Global Headset Jack + mic phone in + line in support)

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: Audio JACK			
Size	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 24 of 61		

EC MEC1404

EC Chip CPN

MEC1404-NU-D0_VTQFP128_14X14

SA000084410

SD034499280

For Board ID Select

EVT	10K
DVT1	13.7K
DVT2	17.8K
Pilot	49.9K

49.9K_0402_1%

SD034100280	10K_0402_1%
SD034137280	13.7K_0402_1%
SD034178280	17.8K_0402_1%
SD034221280	22.1K_0402_1%
SD034270280	27K_0402_1%
SD034324280	32.4K_0402_1%
SD034374280	37.4K_0402_1%
SD034499280	49.9K_0402_1%
SD034576280	57.6K_0402_1%
SD034649280	64.9K_0402_1%
SD00000B180	73.2K_0402_1%
SD000002780	82.5K_0402_1%
SD034931280	93.1K_0402_1%
SD034107380	107K_0402_1%
SD034120380	120K_0402_1%
SD034137380	137K_0402_1%
SD034154380	154K_0402_1%
SD034200380	200K_0402_1%
SD034232380	232K_0402_1%
SD034100380	100K_0402_1%

Model ID

Board ID

32 KHz Clock (Un- POP)

Debug Connector (80 Port)

Pin8 5085_TXD for EC Debug
pin9 5048_TXD for SBIOS debug

Close to UE1 each pin

ESR <100m ohms
Close UE1

SML1DATA => GPU_THM_SMBDAT
SML1CLK => GPU_THM_SMBCLK

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

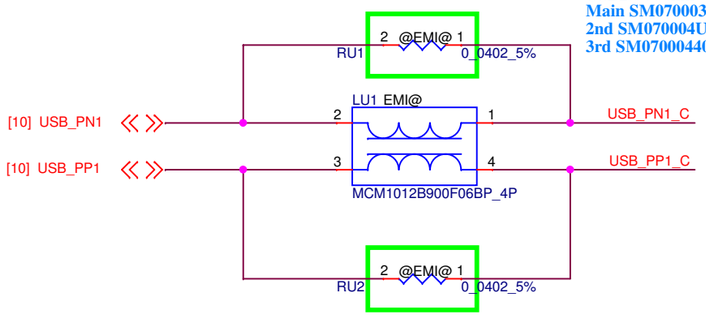
Title: EC MEC1404

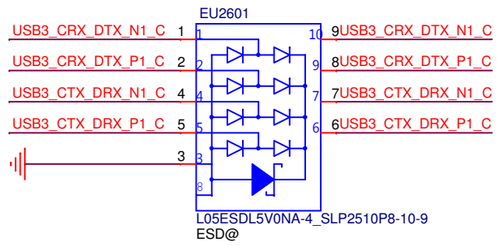
Size: | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 25 of 61

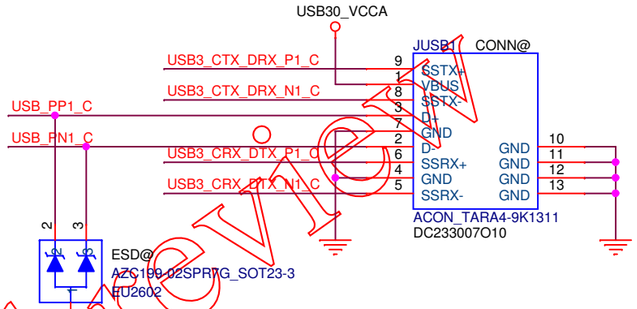
Main Func = USB3.0 Port1

USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)

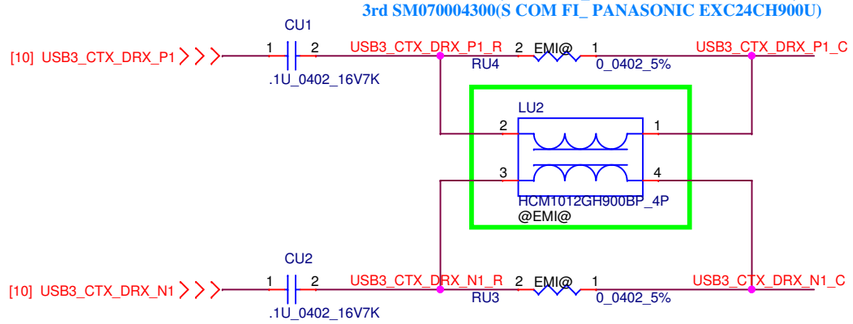




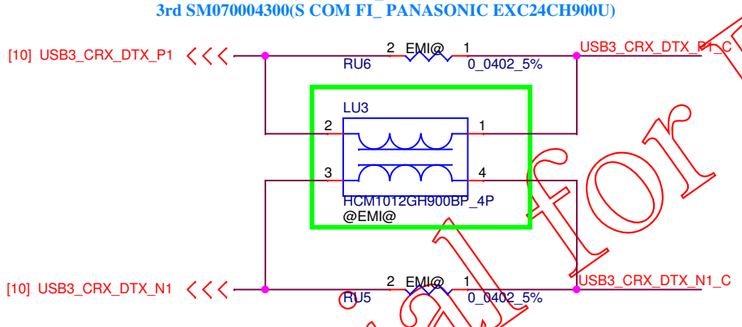
USB3.0 Port1



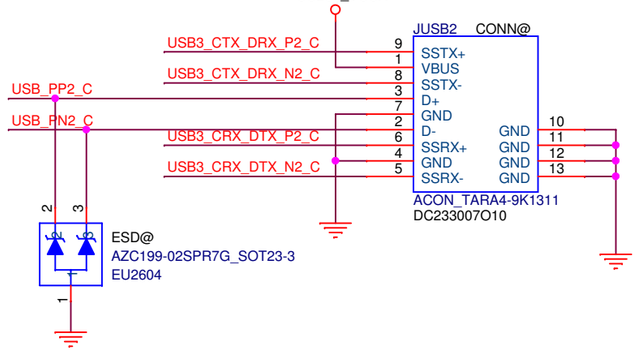
USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)



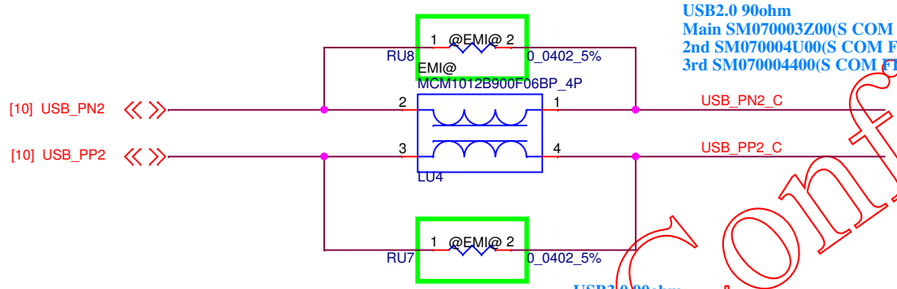
USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

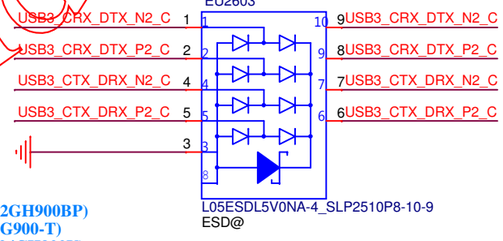


USB3.0 Port2

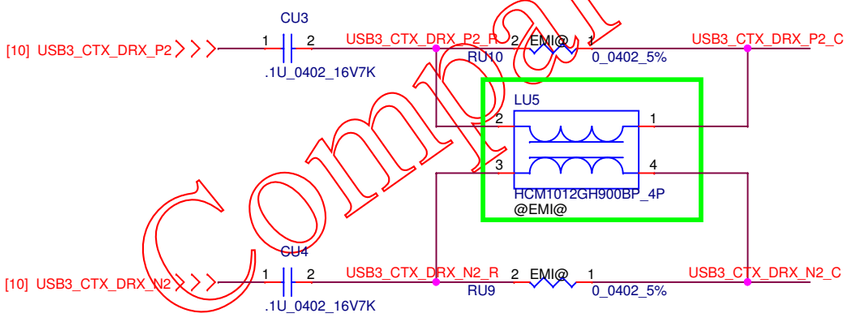


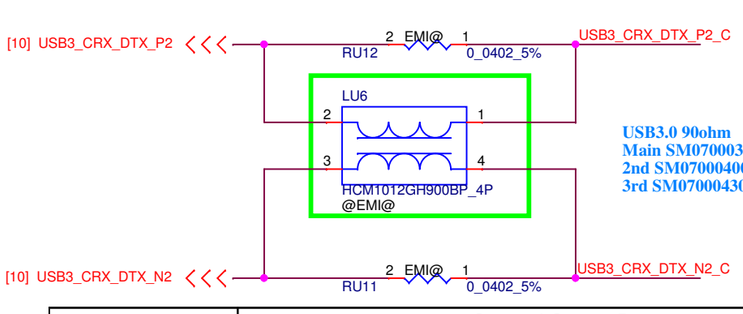
USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)





USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)





USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

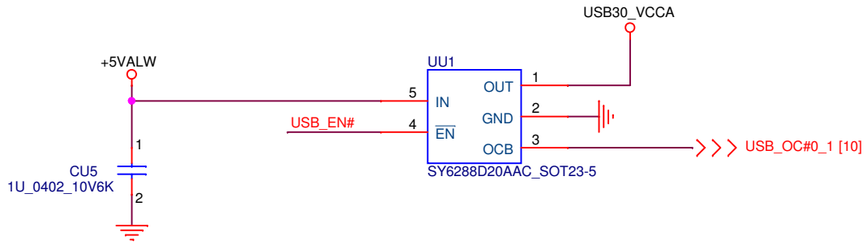
Title: **USB3.0 CONN**

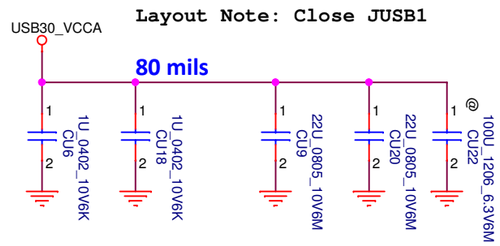
Size | Document Number: **LA-D801P** | Rev: A00

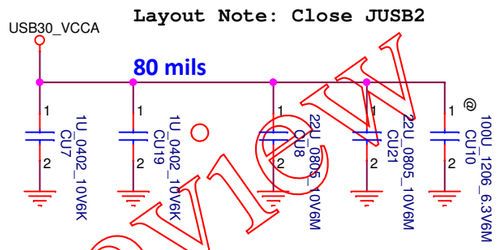
Date: Tuesday, June 21, 2016 | Sheet 26 of 61

Main Func = USB3.0 Port1/Port2

SY6288D Support 2A

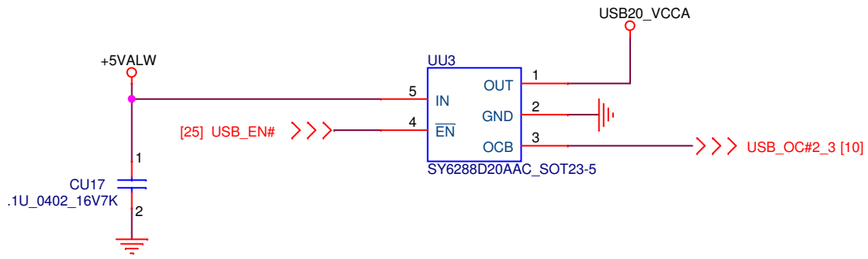




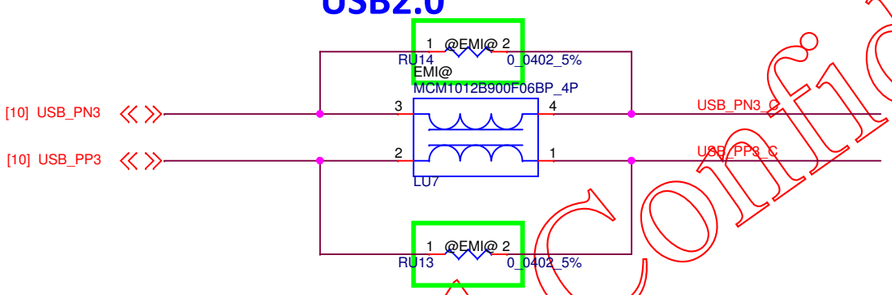


Main Func = USB3.0 Port3

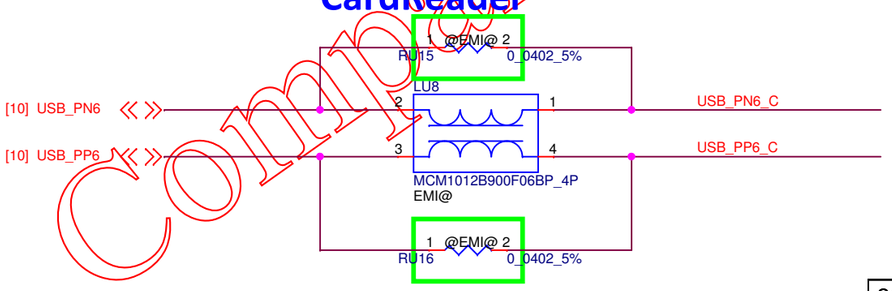
SY6288D Support 2A



USB2.0

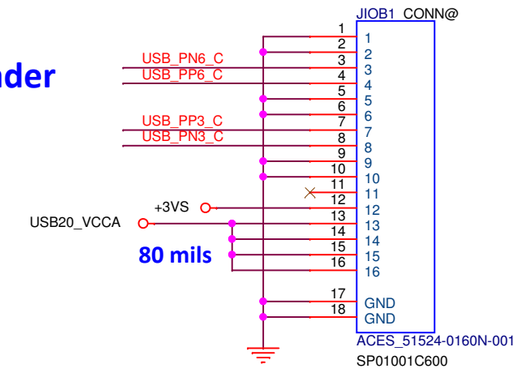


CardReader



I/O Board Connector

CardReader
USB2.0



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

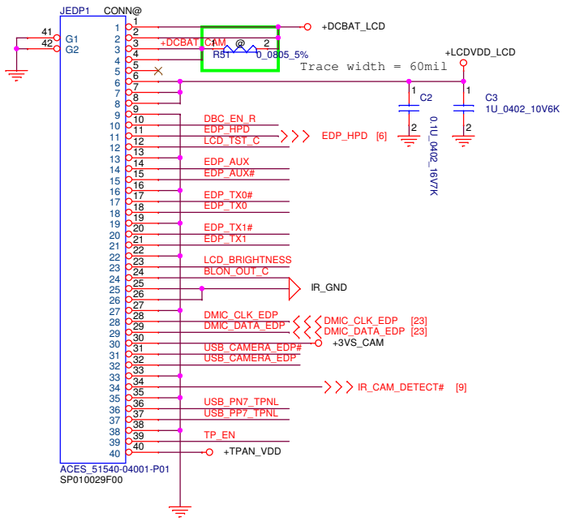
Compal Electronics, Inc.

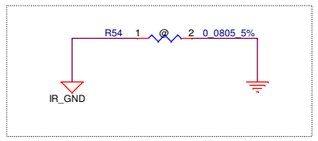
Title: USB Power SW/IO Board

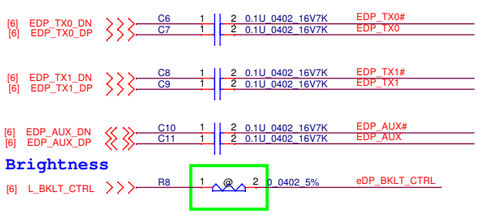
Size | Document Number: LA-D801P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 27 of 61

Main Func = LCD

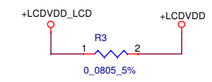




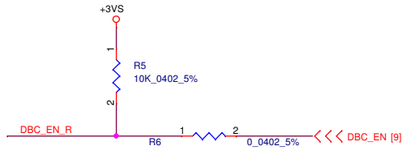


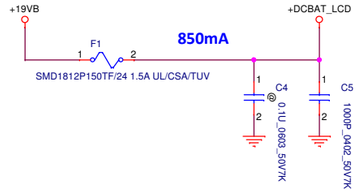
Brightness

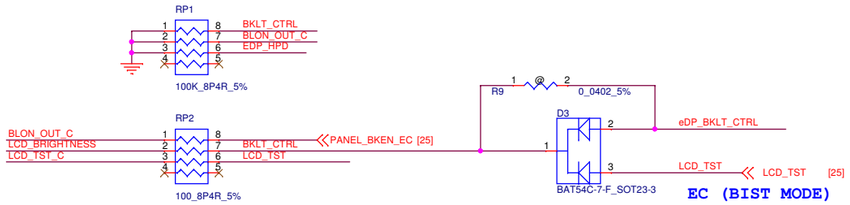
INVERTER POWER



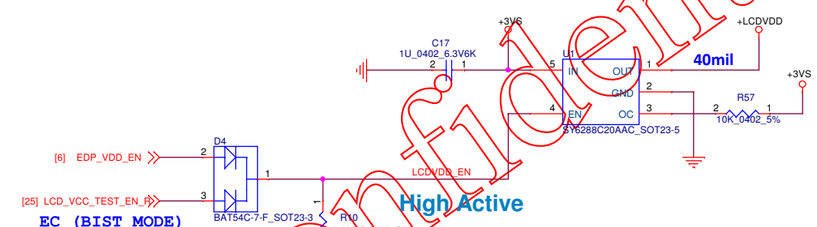
EE note: Never change R3 to short pad after MP





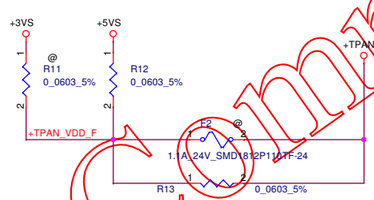


EC (BIST MODE)



High Active

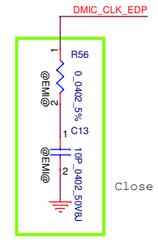
EC (BIST MODE)



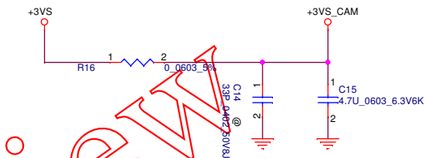
EE note: Never change R12/R13 to short pad after MP

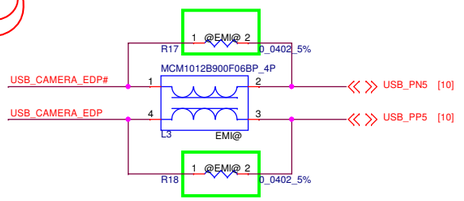
Main Func = CAM

EE note: Never change R16 to short pad after MP



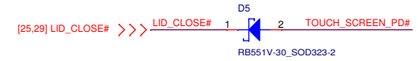
Close JEDP1 Pin28, 29

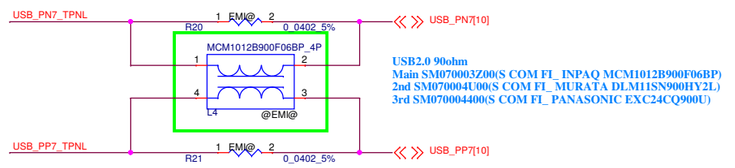




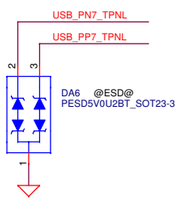
Main Func = TS

Touch Panel





USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/07/09	Deciphered Date 2016/07/31	Title: LCD/Cam/MIC/T.Panel
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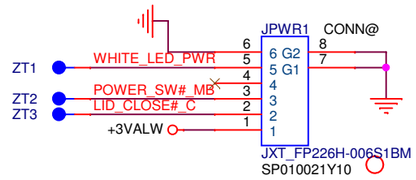
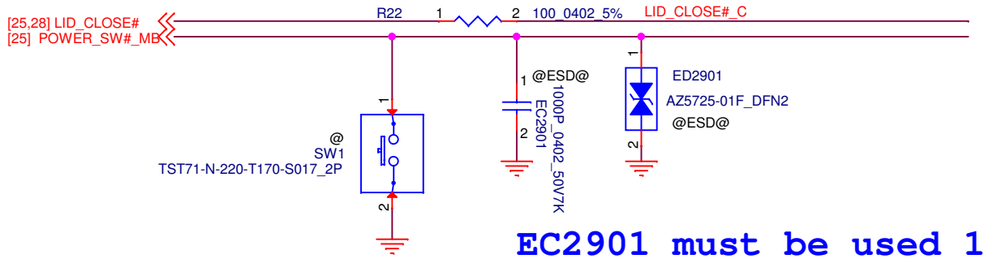
Main Func = Power BTN

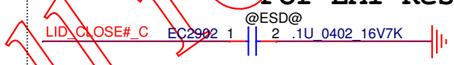
using ZT2 insted of TPS8





EC2901 must be used 1000pF.

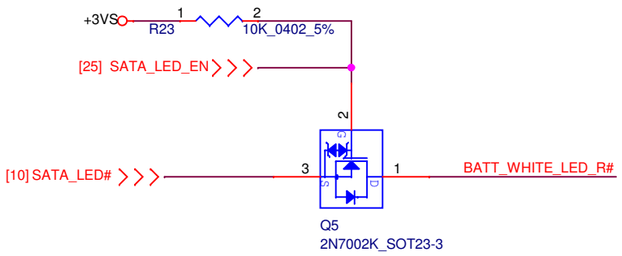
For EMI Reserved

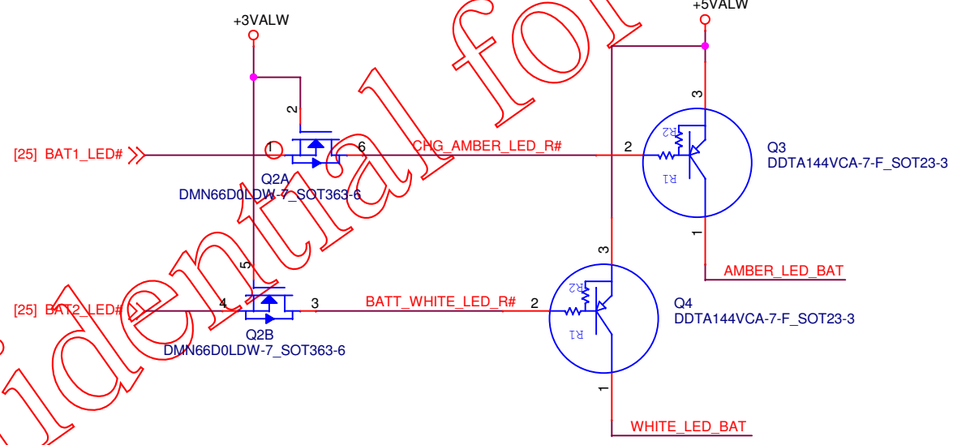


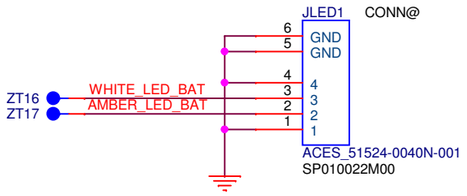
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



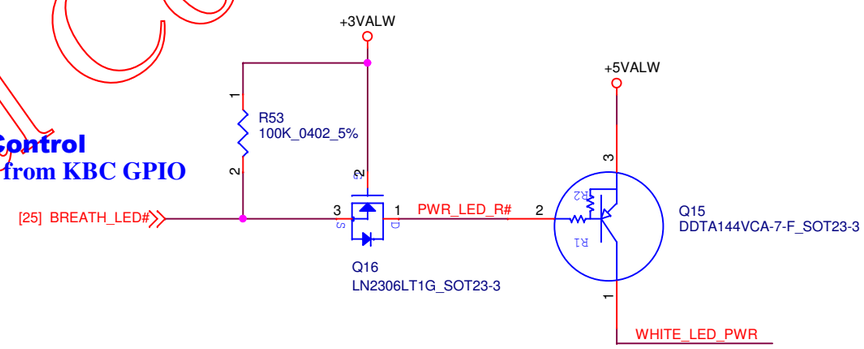




Main Func = PWR LED

Low actived from KBC GPIO

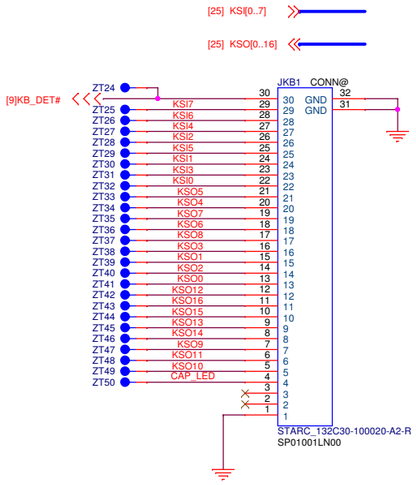
PWR LED Control
LOW actived from KBC GPIO



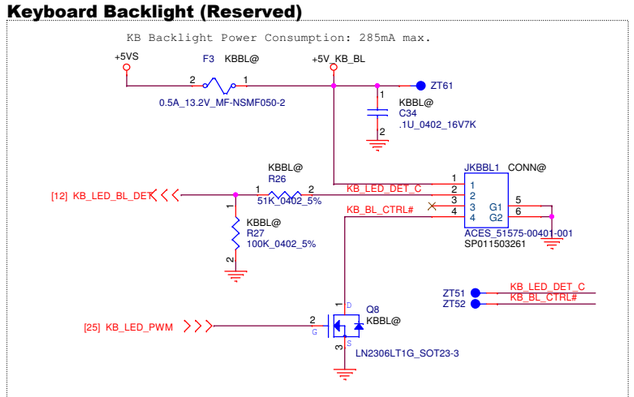
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: LED Board/Power Button			
Size:	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 29 of 61		

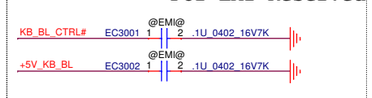
Main Func = KB



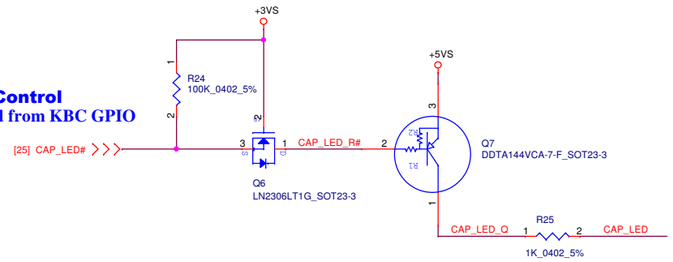
Keyboard Backlight (Reserved)



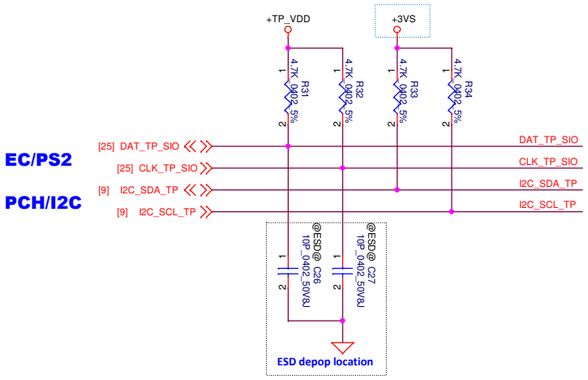
For EMI Reserved

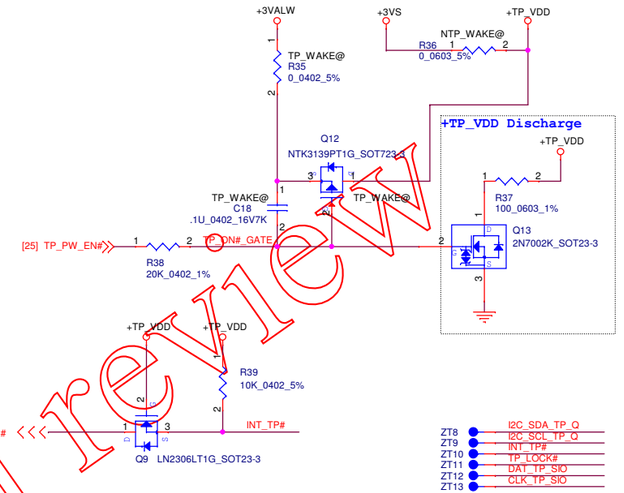


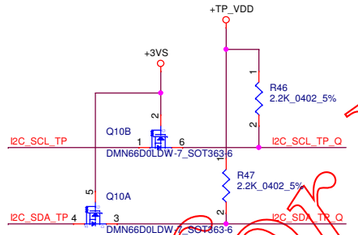
CAP LED Control
LOW actived from KBC GPIO

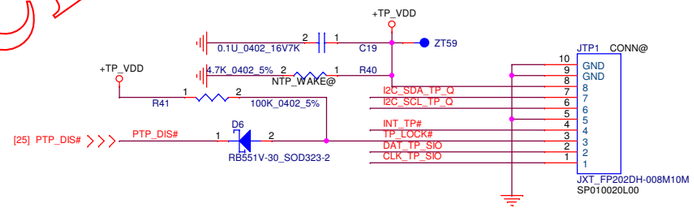


Main Func = TPAD

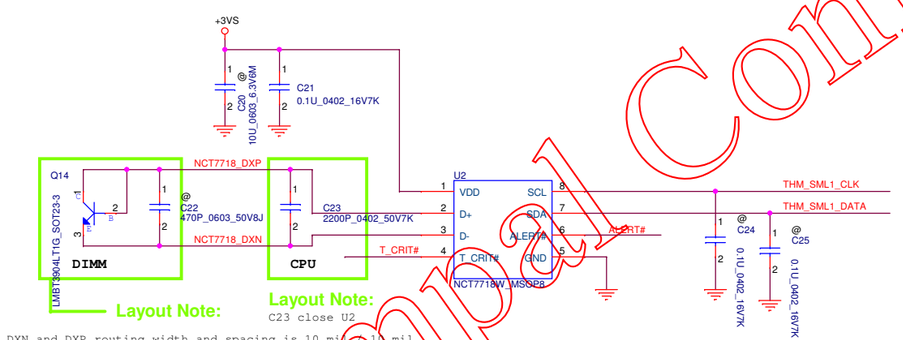


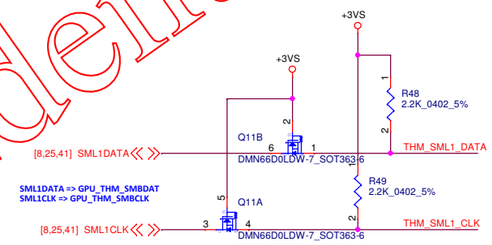


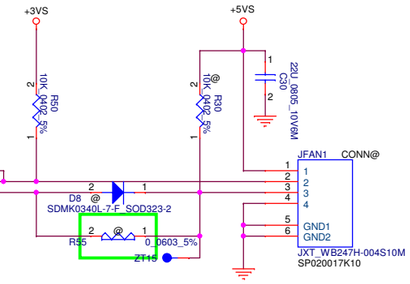




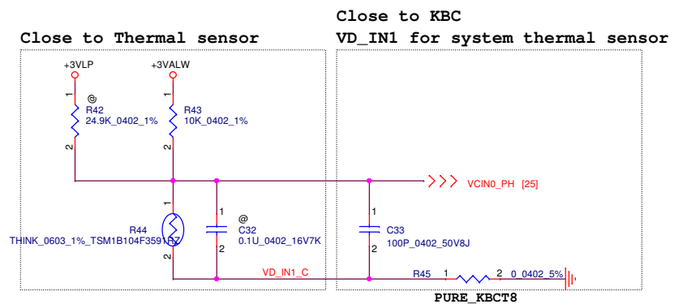
Main Func = Thermal







TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



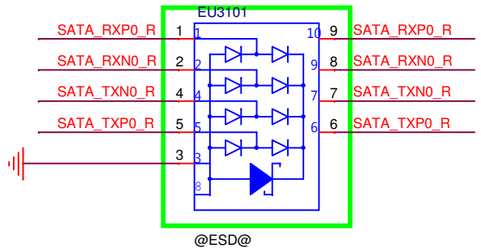
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.	
Title	Keyboard/Touch Pad/Thermal/FAN
Size	Document Number: LA-D801P
Rev	A00
Date: Tuesday, June 21, 2016	Sheet 30 of 61

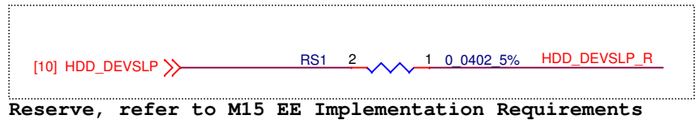
Main Func = HDD

SATA HDD Connector

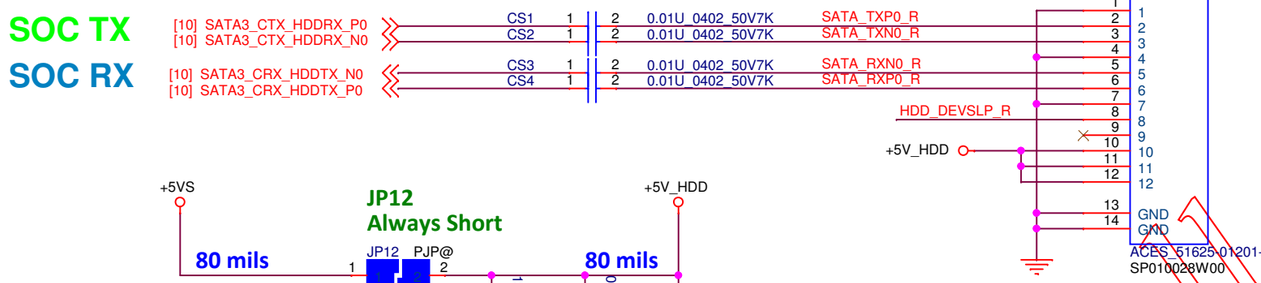
Layout Note:
Place near HDD1

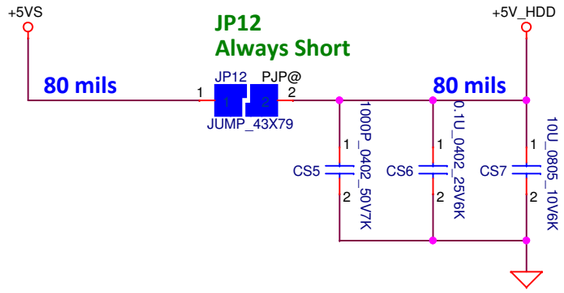


Swap based on the swap report.



Reserve, refer to M15 EE Implementation Requirements

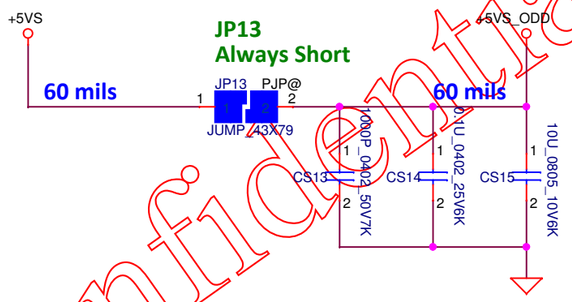


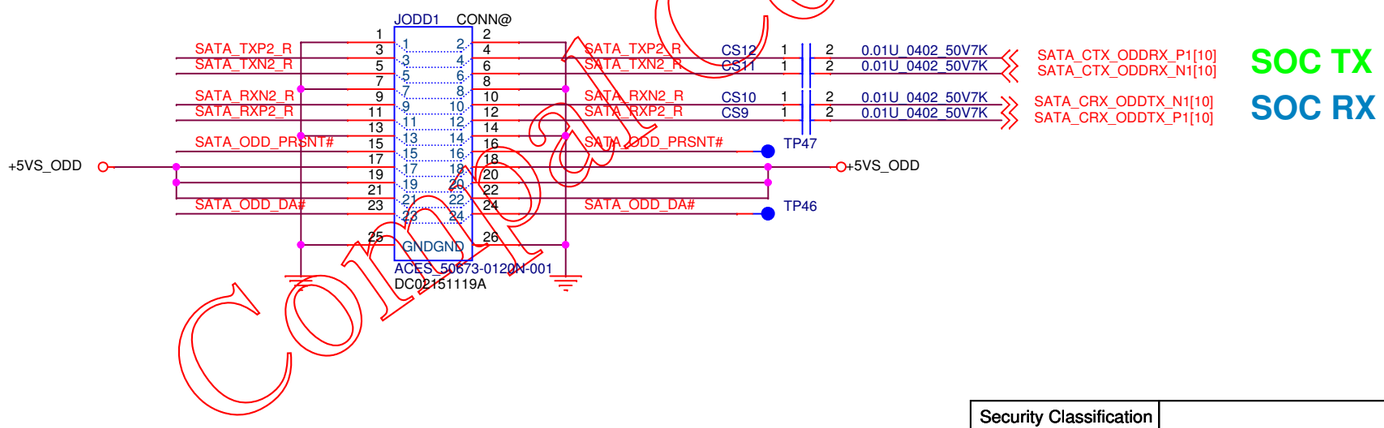


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD ZiF Connector





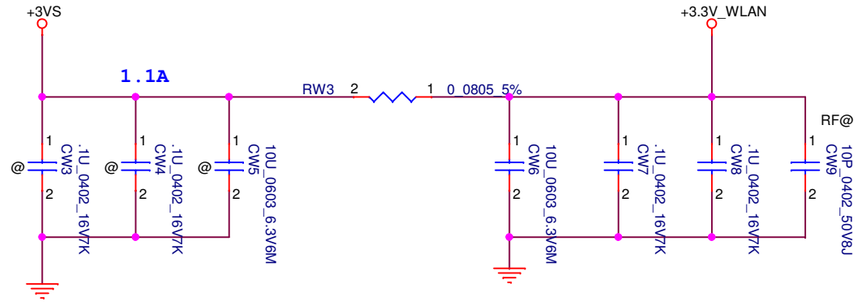
Pin	Signal
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND
8	DP
9	+5V
10	+5V
11	MD
12	GND
13	GND

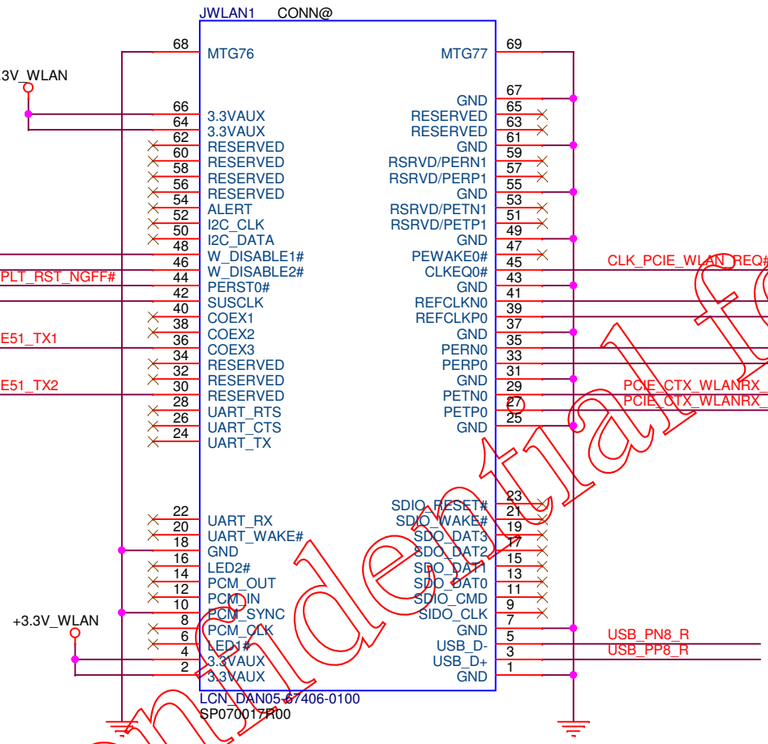
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

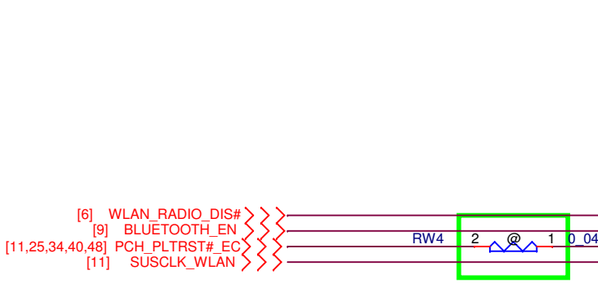
Compal Electronics, Inc.		
Title: HDD/ODD		
Size	Document Number: LA-D801P	Rev: A00
Date: Tuesday, June 21, 2016	Sheet 31 of 61	

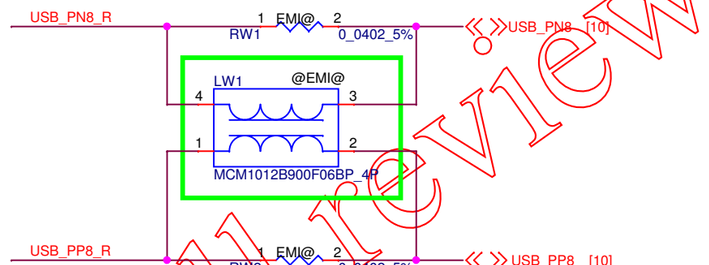
Main Func = WLAN

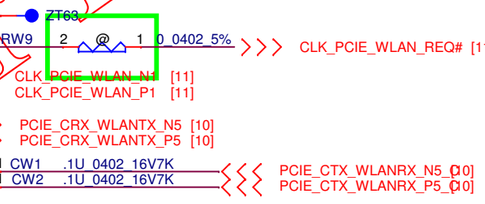
A Key CONN

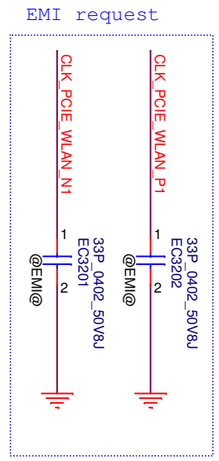




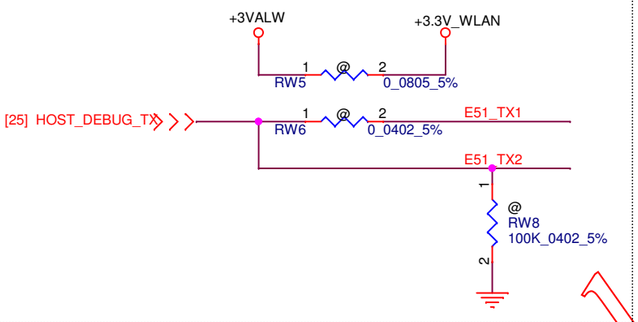








Reserved for NGFF Debug Card



Support: Intel Dual Band Wireless-AC 3160

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/07/09	Deciphered Date 2016/07/31	Title: NGFF_WLAN CONN
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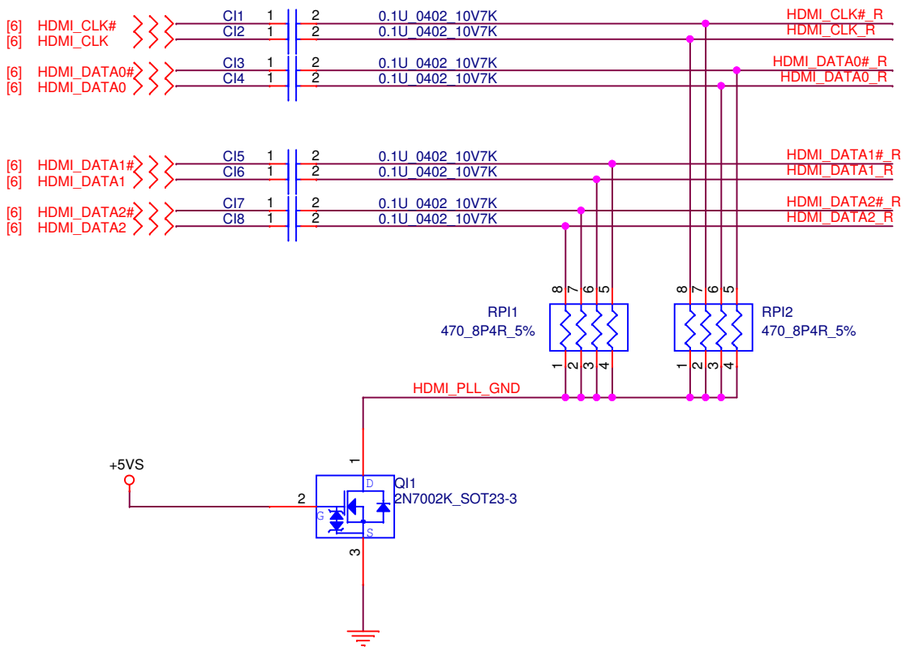
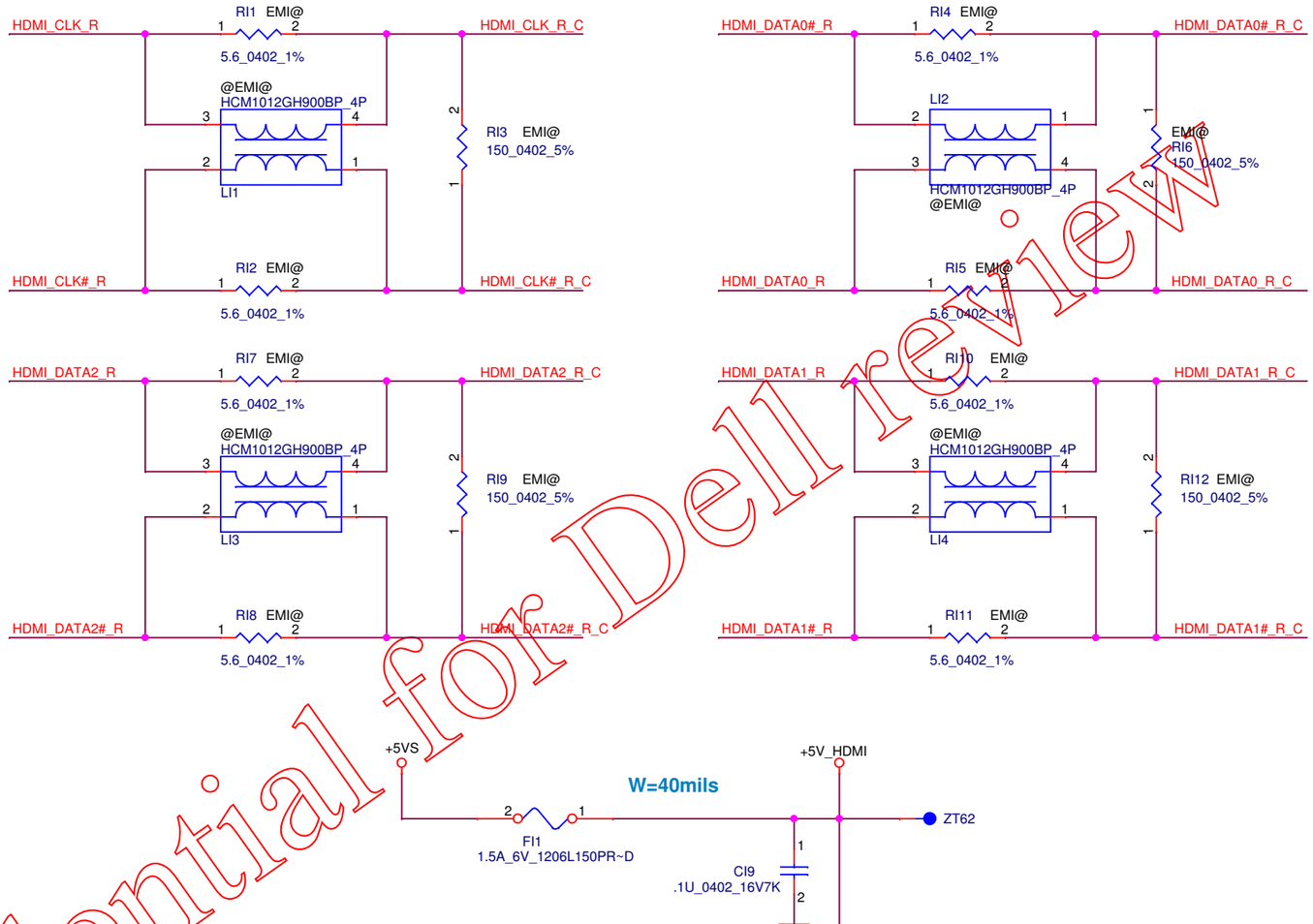
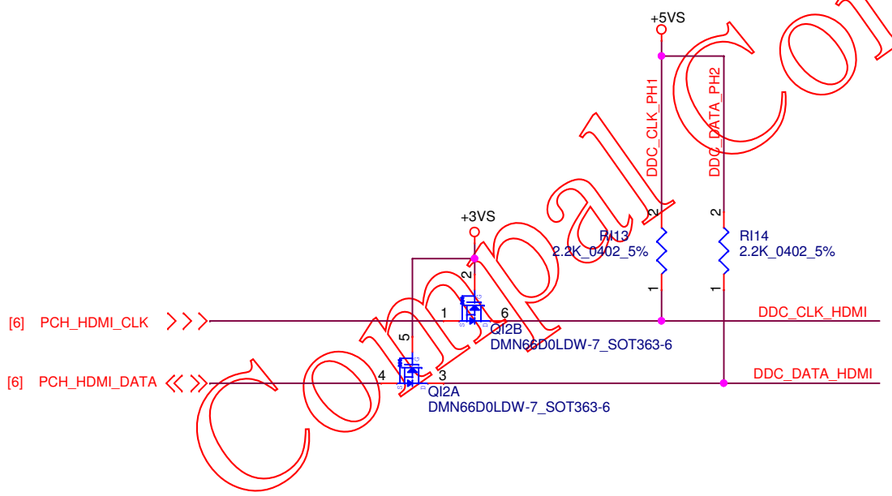
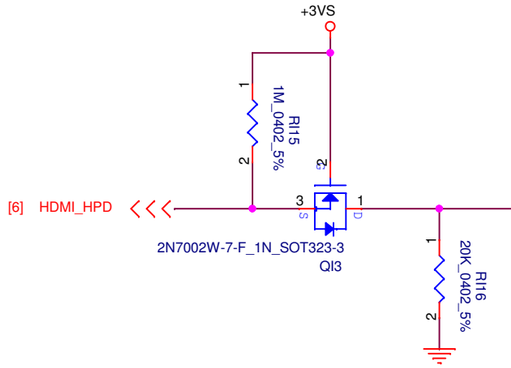
Main Func = HDMI









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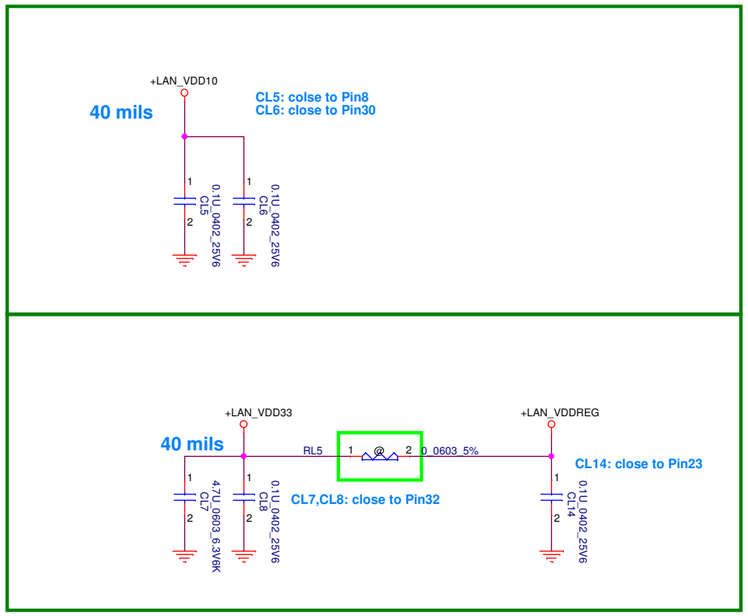
Issued Date	2015/07/09	Deciphered Date	2016/07/31

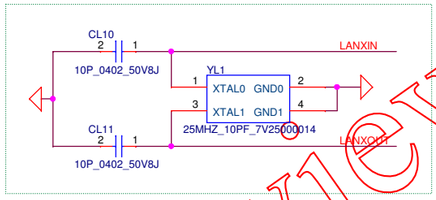
Compal Electronics, Inc.			
Title: HDMI L.Shifter/Conn			
Size	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 33 of 61		

Main Func = LAN

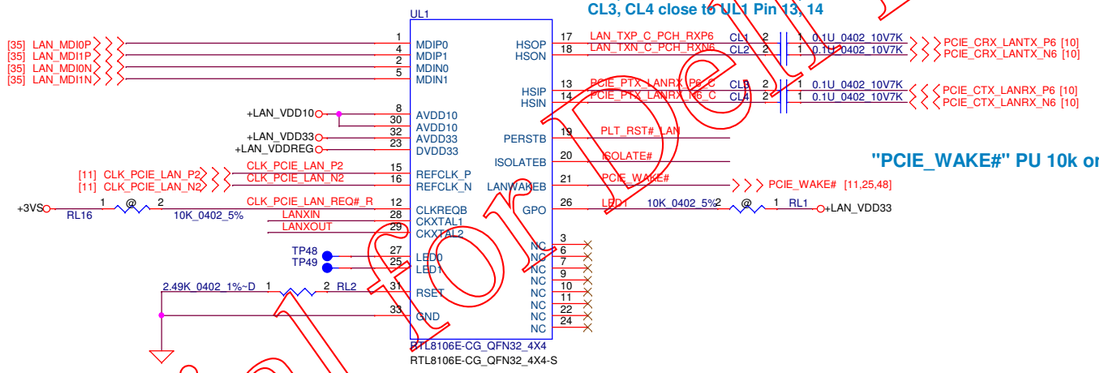
LAN CHIP 10/100M

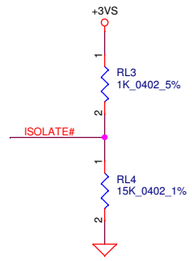
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
			SA000065Y00
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

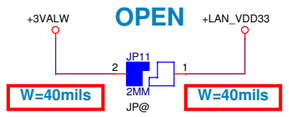




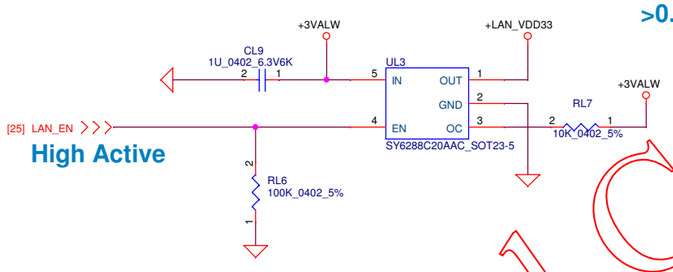
XTAL

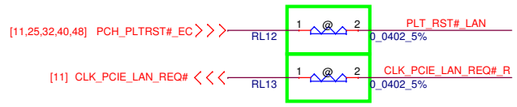






+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



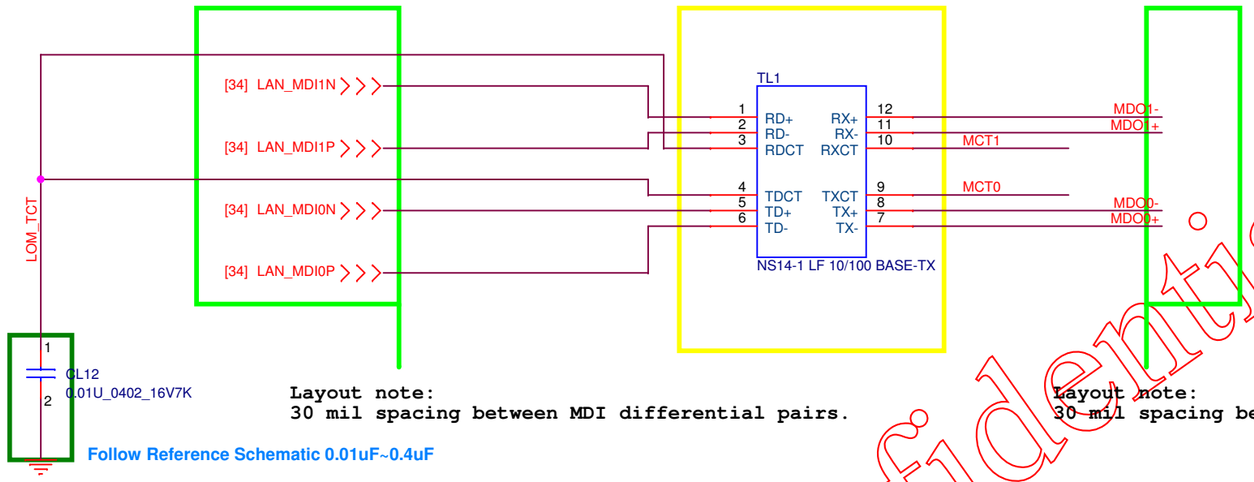


Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: LAN RTL8106			
Size	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 34 of 61		

Main Func = LAN

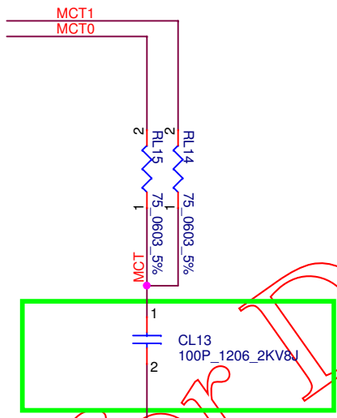
LAN TransFormer 10/100M

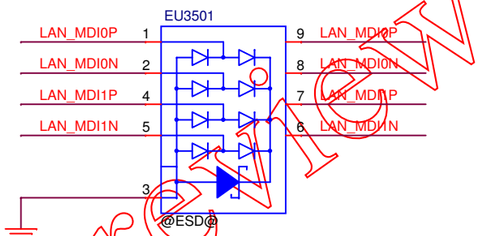


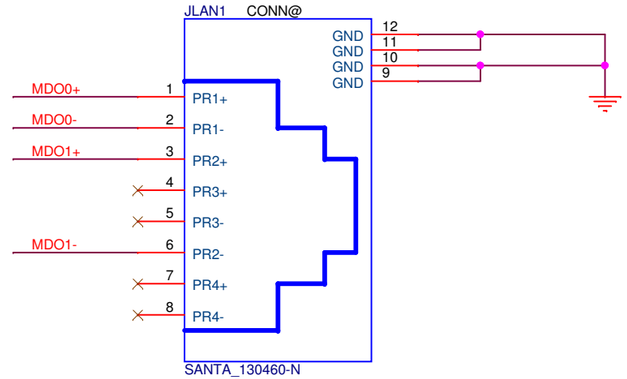
Follow Reference Schematic 0.01uF~0.4uF

Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.







Main:
SP050007K00, S X'FORM_HD-081-A LAN
2nd:
SP050008L00, S X'FORM_ NS681677 LAN
Jason 2015/04/27

Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: XFOM&RJ45			
Size: B2e	Document Number: LA-D801P		Rev: A00
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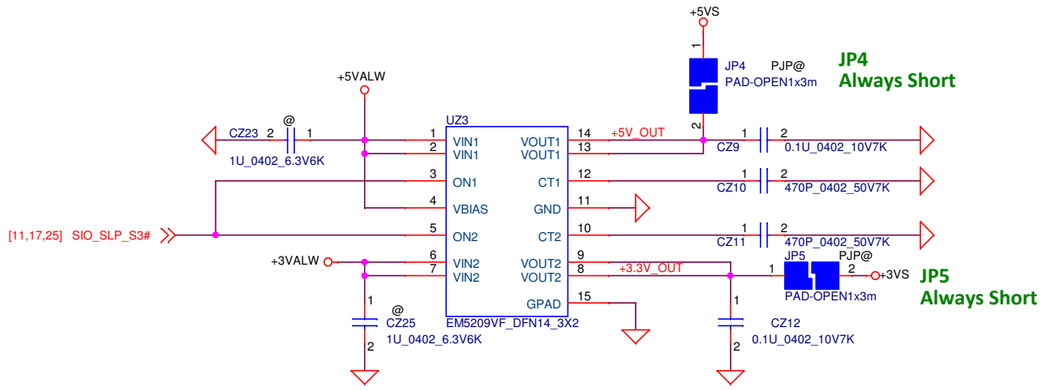
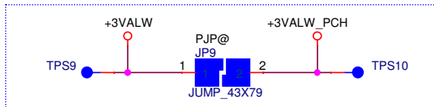
+5VS/+3VS for System



+3VALW_PCH for System



JP9 Short
for NON-DS3

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title: DC to DC	
Size	Document Number: LA-D805P — Rev: A00
Date: Tuesday, June 21, 2016	Sheet 36 of 61

Vendor	PS8713B	TI	Spec				schematic netname	3Vs		GND	
1	VDD	VCC	Same								
2	B_EQ0	EQ1	**LL:** 9.5dB (default)	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_EQ1_P0	RI23	@	RI32	@
3	DE0	DE1	LL: 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE1_P0	RI26	@	RI35	@
4	EQ1	OS1	**LL:** 9.5dB	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_OS1_P0	RI22	@	RI40	@
5	PD#	EN_RXD	it can be left open				USB3_ERD_P0	RI44	@	RI48	@
6	B_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN6	RI53	@	RI49	@
7	REXT	NC		4.99K						RI56	4.99K
8	B_Inn	RX1-	Same								
9	B_Inp	RX1+	Same								
10	GND	GND	Same								
11	A_OUTn	TX2-	Same								
12	A_OUTp	TX2+	Same								
13	VDD	VCC	Same								
14	TST/NC	CM	4.7K ohm resistor for perfomance adjustment				USB3_CM_P0	RI42	@	RI46	@
15	A_EQ1	OS2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_OS2_P0	RI19	@	RI87	@
16	A_DE0	DE2	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE2_P0	RI20	@	RI31	@
17	A_EQ0	EQ2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_EQ2_P0	RI21	@	RI36	@
18	A_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN18	RI52	@	RI50	@
19	A_Inp	RX2+	Same								
20	A_Inn	RX2-	Same								
21	GND	GND	Same								
22	B_OUTp	TX1+	Same								
23	B_OUTn	TX1-	Same								
24	I2C_EN	NC	this pin canbe NC or connected to GND				NC			RI57	@

+5VALW TO +5V_3DCAM

JP10 Always Open

JP10 JP@ JUMP_43X39

CT pin use 2200pf for soft start tuning

TPS22967DSGR_SON8_2X2

PS8713BTQFN24GTR2-A0_TQFN24_4X4

SN65LVPE502CPRGER_VQFN24_4X4-S

MCF12102G900-T_4P

ACES_50463-0104A-001

SP01001G000

S DIO(BR) TVWDF1004AD0 DFN ESD

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Issued Date	2015/07/09	Deciphered Date	2016/07/31

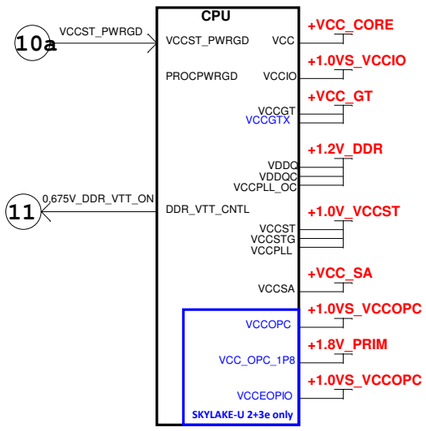
Compal Electronics, Inc.

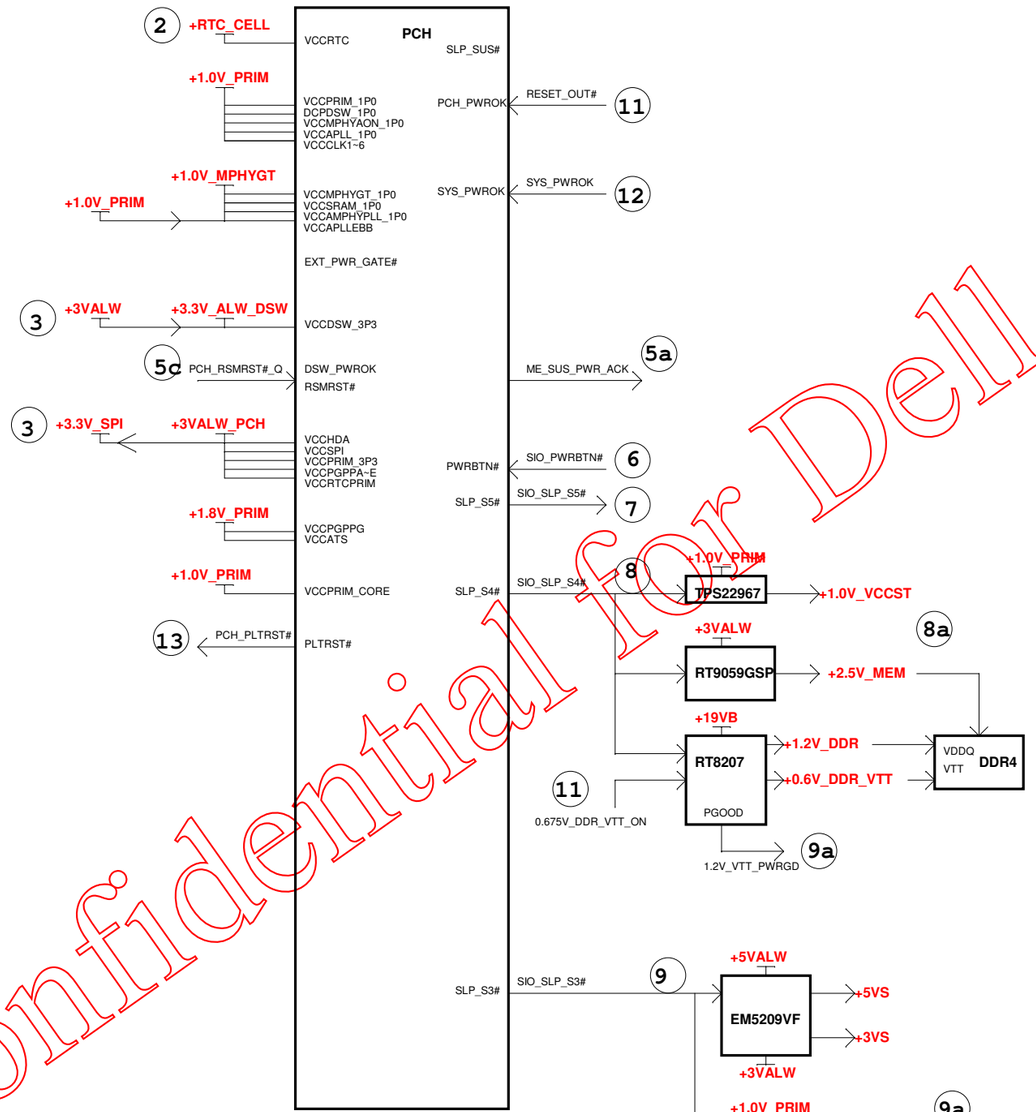
Title: **3D CAMERA**

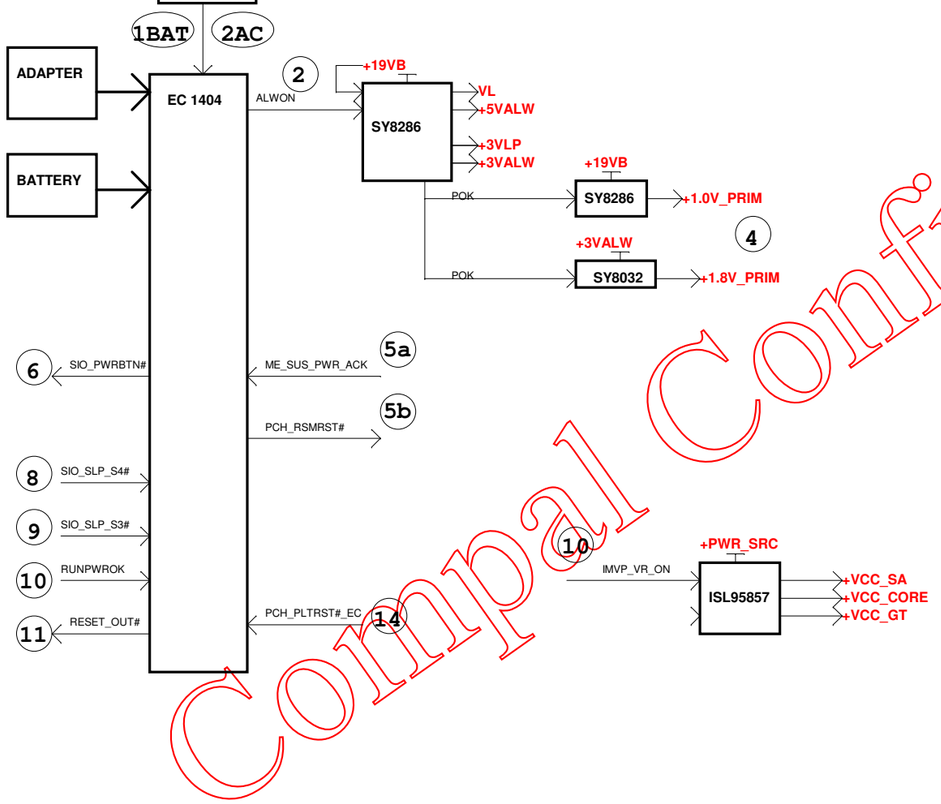
Size | Document Number: **LA-D801P** | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 37 of 61

Timing Diagram for S5 to S0 mode



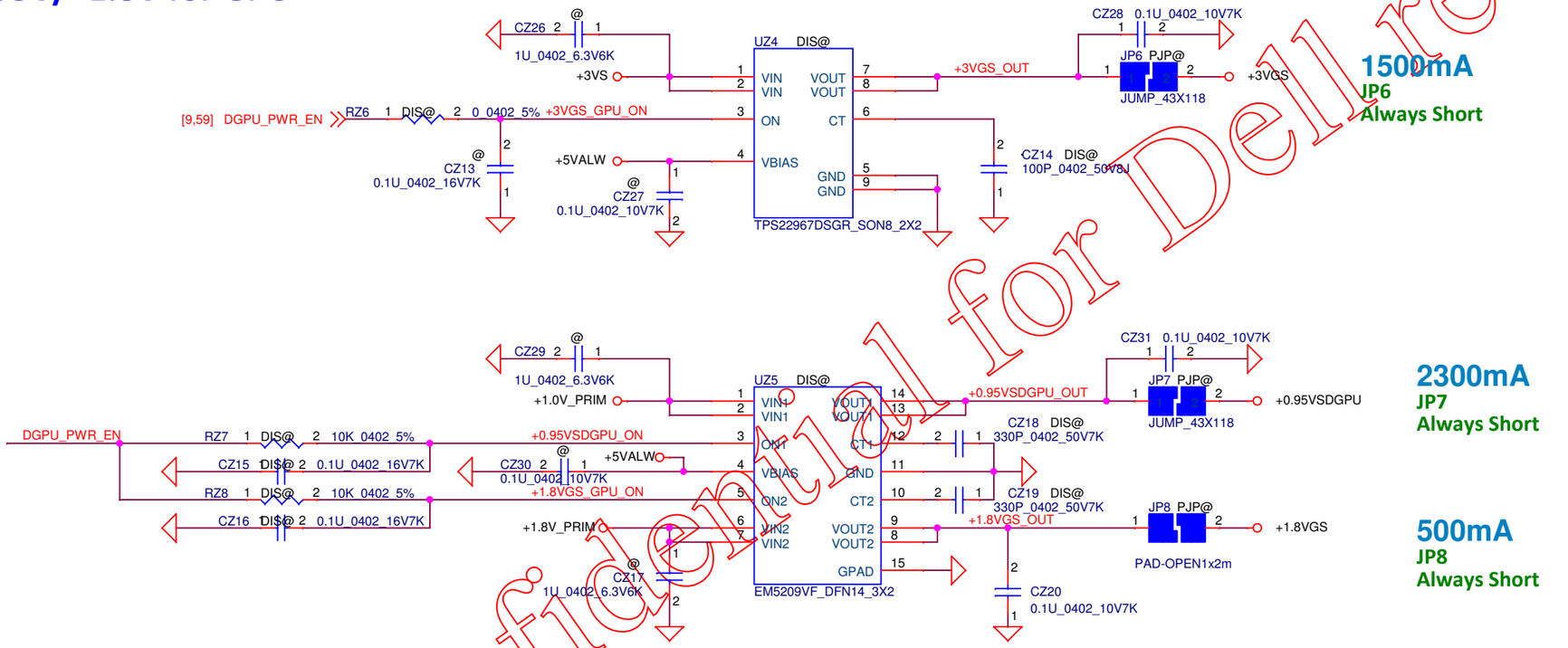




DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Power Sequence		
Size	Document Number: LA-D801P	Rev: A00
Date: Tuesday, June 21, 2016	Sheet 38 of 61	

+3V/+0.95V/+1.8V for GPU



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.		
Title: *GPU Power*		
Size	Document Number: *LA-D805P*	Rev: A00
Date: Tuesday, June 21, 2016	Sheet 39 of 61	

[10] PEG_HTX_C_GRX_P[0..3] → PEG_HTX_C_GRX_P[0..3]
[10] PEG_HTX_C_GRX_N[0..3] → PEG_HTX_C_GRX_N[0..3]
[10] PEG_GTX_C_HRX_P[0..3] → PEG_GTX_C_HRX_P[0..3]
[10] PEG_GTX_C_HRX_N[0..3] → PEG_GTX_C_HRX_N[0..3]

@
UV1A

PEG_HTX_C_GRX_P0	DIS@ 2	1	CV312	0.22U_0402_16V7K	PEG_HTX_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PEG_GTX_HRX_P0	DIS@ 2	1 CV1 0.22U_0402_16V7K PEG_GTX_C_HRX_P0
PEG_HTX_C_GRX_N0	DIS@ 2	1	CV306	0.22U_0402_16V7K	PEG_HTX_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PEG_GTX_HRX_N0	DIS@ 2	1 CV2 0.22U_0402_16V7K PEG_GTX_C_HRX_N0
PEG_HTX_C_GRX_P1	DIS@ 2	1	CV308	0.22U_0402_16V7K	PEG_HTX_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PEG_GTX_HRX_P1	DIS@ 2	1 CV3 0.22U_0402_16V7K PEG_GTX_C_HRX_P1
PEG_HTX_C_GRX_N1	DIS@ 2	1	CV305	0.22U_0402_16V7K	PEG_HTX_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PEG_GTX_HRX_N1	DIS@ 2	1 CV4 0.22U_0402_16V7K PEG_GTX_C_HRX_N1
PEG_HTX_C_GRX_P2	DIS@ 2	1	CV307	0.22U_0402_16V7K	PEG_HTX_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PEG_GTX_HRX_P2	DIS@ 2	1 CV5 0.22U_0402_16V7K PEG_GTX_C_HRX_P2
PEG_HTX_C_GRX_N2	DIS@ 2	1	CV309	0.22U_0402_16V7K	PEG_HTX_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PEG_GTX_HRX_N2	DIS@ 2	1 CV6 0.22U_0402_16V7K PEG_GTX_C_HRX_N2
PEG_HTX_C_GRX_P3	DIS@ 2	1	CV313	0.22U_0402_16V7K	PEG_HTX_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PEG_GTX_HRX_P3	DIS@ 2	1 CV7 0.22U_0402_16V7K PEG_GTX_C_HRX_P3
PEG_HTX_C_GRX_N3	DIS@ 2	1	CV304	0.22U_0402_16V7K	PEG_HTX_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PEG_GTX_HRX_N3	DIS@ 2	1 CV8 0.22U_0402_16V7K PEG_GTX_C_HRX_N3

AB30 / AA31	PCIE_RX4P / PCIE_RX4N	PCIE_TX4P / PCIE_TX4N → AC25 / AB25
AA29 / Y28	PCIE_RX5P / PCIE_RX5N	PCIE_TX5P / PCIE_TX5N → Y23 / Y24
Y30 / W31	PCIE_RX6P / PCIE_RX6N	PCIE_TX6P / PCIE_TX6N → AB27 / AB26
W29 / V28	PCIE_RX7P / PCIE_RX7N	PCIE_TX7P / PCIE_TX7N → V27 / Y26
V30 / U31	NC#V30 / NC#U31	NC#W24 / NC#W23 → W24 / W23
U29 / T28	NC#U29 / NC#T28	NC#V27 / NC#U26 → V27 / U26
T30 / R31	NC#T30 / NC#R31	NC#U24 / NC#U23 → U24 / U23
R29 / P28	NC#R29 / NC#P28	NC#T26 / NC#T27 → T26 / T27
P30 / N31	NC#P30 / NC#N31	NC#T24 / NC#T23 → T24 / T23
N29 / M28	NC#N29 / NC#M28	NC#P27 / NC#P26 → P27 / P26
M30 / L31	NC#M30 / NC#L31	NC#P24 / NC#P23 → P24 / P23
L29 / K30	NC#L29 / NC#K30	NC#M27 / NC#N26 → M27 / N26

PCI EXPRESS INTERFACE

CLOCK

[11] CLK_PEG_VGA → CLK_PEG_VGA AK30 PCIE_REFCLKP
[11] CLK_PEG_VGA# → CLK_PEG_VGA# AK32 PCIE_REFCLKN

CALIBRATION

PCIE_CALR_TX Y22 — RV1 1 DIS@ 2 1.69K_0402_1%
PCIE_CALR_RX AA22 — RV3 1 DIS@ 2 1K_0402_1%

RV2 1 DIS@ 2 1K_0402_1% → N10 TEST_PG

PLT_RST_VGA# → AL27 PERSTB

2160856030-A0_FCBGA631

+0.95VSDGPU

GPU R1/R3

UV1 SA000098V1L M1_70_G5@
S IC 216-0889-018 A0 R16M-M1-70 A31!

UV1 SA000098V2L M1_70_D3@
S IC 216-0864-032 A0 R16M-M1-70 0FD

No Use GPU Display Port outpud

@
UV1F

+VGA_CORE

VARY_BL	AB11	
DIGON	AB12	
TXCAP_DPA3P	AL15	
TXCAM_DPA3N	AK14	
TX0P_DPA2P	AH16	
TX0M_DPA2N	AJ15	
TX1P_DPA1P	AL17	
TX1M_DPA1N	AK16	
TX2P_DPA0P	AH18	
TX2M_DPA0N	AJ17	
NC_TXOUT_L3P	AL19	
NC_TXOUT_L3N	AK18	
TMDP		
TXCBP_DPB3P	AH20	
TXCBM_DPB3N	AJ19	
TX3P_DPB2P	AL21	
TX3M_DPB2N	AK20	
TX4P_DPB1P	AH22	
TX4M_DPB1N	AJ21	
TX5P_DPB0P	AL23	
TX5M_DPB0N	AK22	
NC_TXOUT_U3P	AK24	
NC_TXOUT_U3N	AJ23	

216-0842024-A11-MAR_ECBGA631

PLT_RST#
[11,25,32,34,48] PCH_PLTRST#_EC
[9] DGPU_HOLD_RST#
DGPU_HOLD_RST#(GPP_D10)

+3VGS
UV2 DIS@
MC74VHC1G08DFT2G_SC70-5
IN1 IN2 O
PLT_RST_VGA# [25]
RV4 100K_0402_5% DIS@

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Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title MESO_(1/5)_PCIE/DP
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				Date: Tuesday, June 21, 2016 / Sheet 40 of 61

Resistor Divider Lookup Lable

0402 1% resistors are equired

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :

PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :

PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_FN_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11

Strap Name :

PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :

PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

VRAM Type
Need reference
X76 Schematic

M1-70 use +1.8v

Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

TOPAZ Thermal Address=->0x82

Change CV17, CV18 for YV1 frequency deviation
Eason 2/19

Enable MLPS

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	MESO_(2/5)_MSIC		
Size	Document Number		Rev
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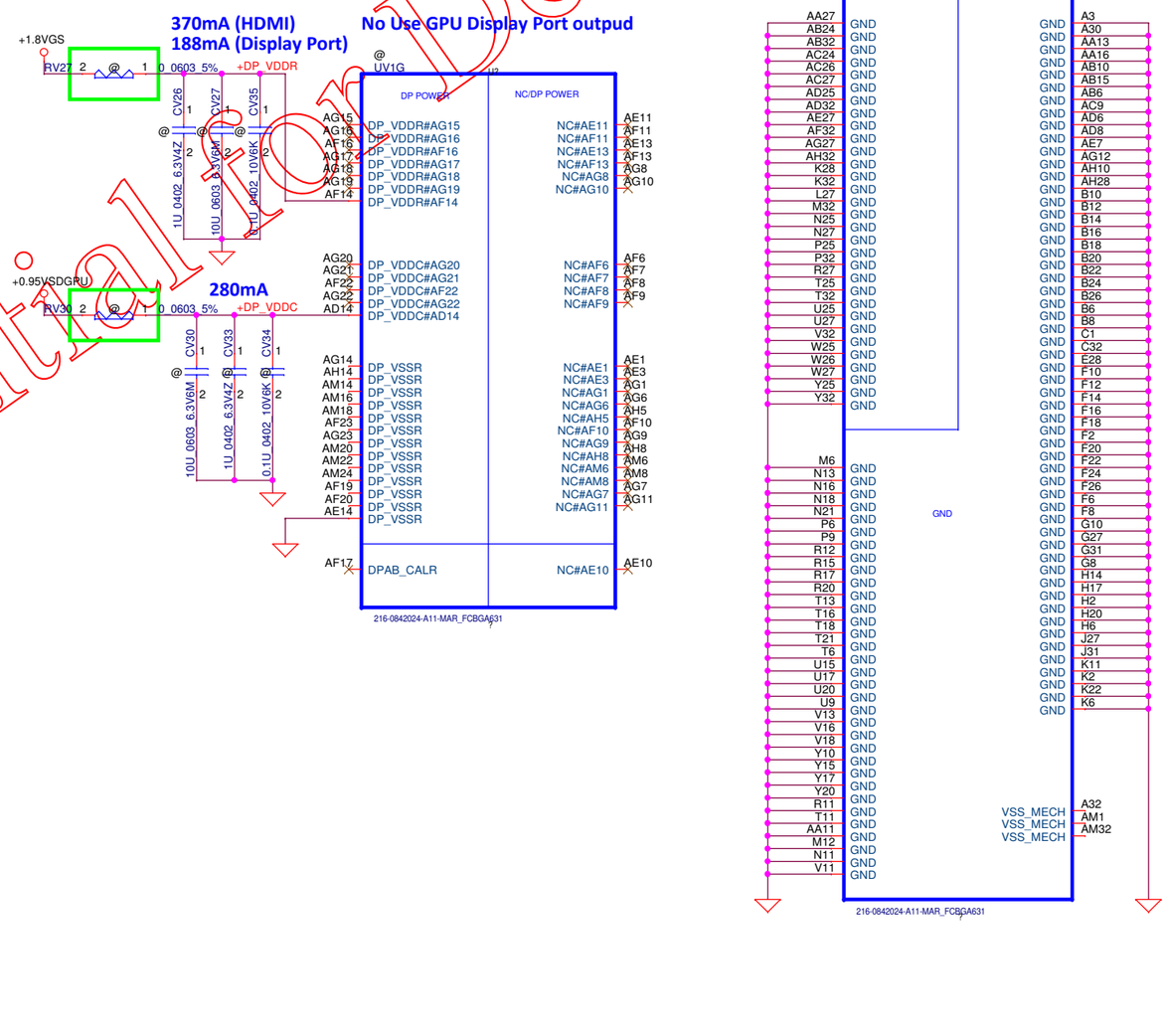

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	MESO_(3/5)_Power/GND		
Size	Document Number		Rev
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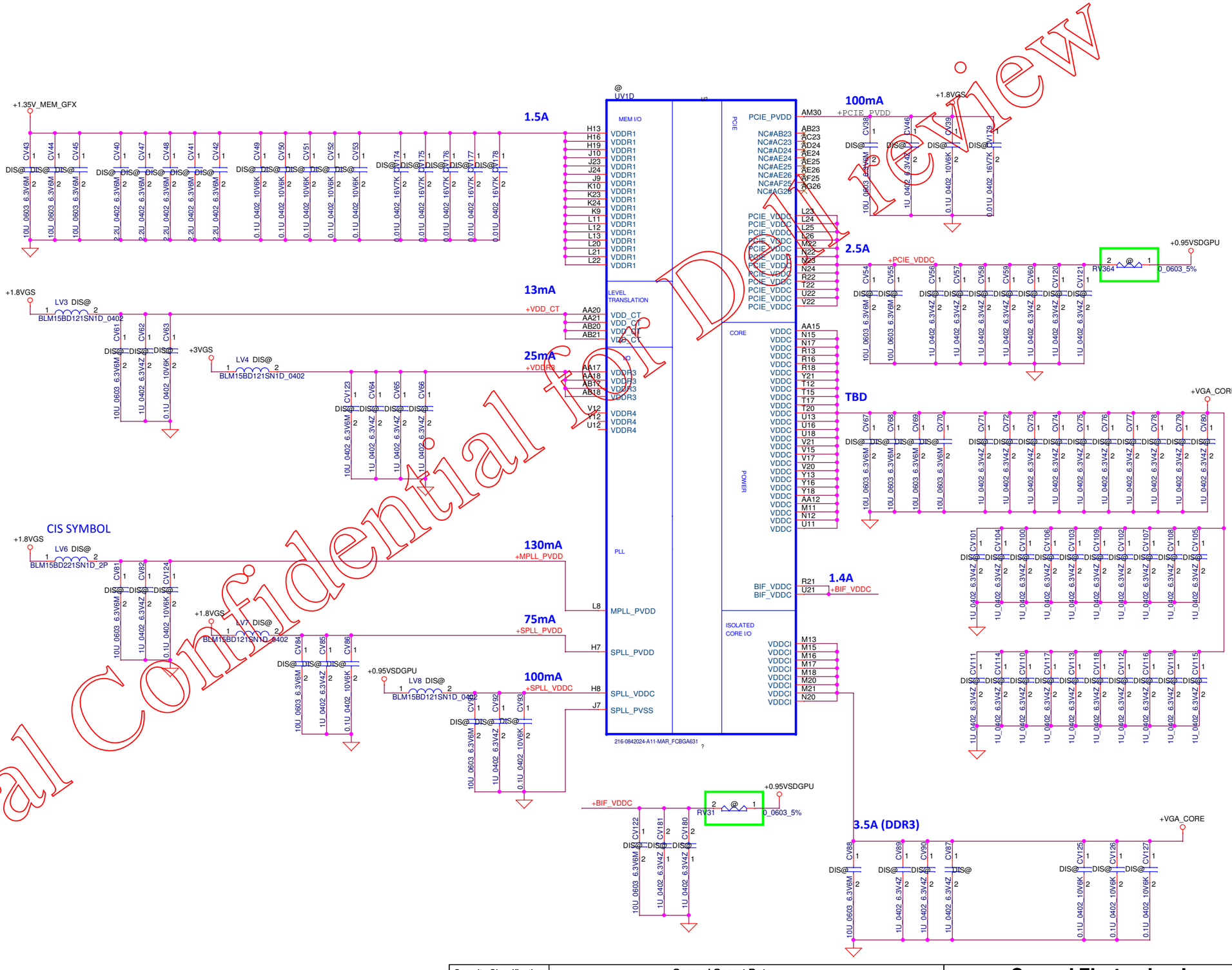
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	4	30	0
VDDCI	3.5A	1	3	3

+0.95VSDGPU		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2	7	0
BIF_VDDC	1.4A	1	2	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	1	3	0



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: MESO_(4/5)_Power			
Size: Custom	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 43 of 61		

[45,46] M_DA[63..0] M_DA[63..0]

[45] M0_MA[8..0] M0_MA[8..0]

[46] M1_MA[8..0] M1_MA[8..0]

+1.35V_MEM_GFX

RV33 40.2_0402_1% DIS@

RV34 100_0402_1% DIS@

+MVREFDA

CV94 1U_0402_6.3V4Z DIS@

+1.35V_MEM_GFX

RV32 40.2_0402_1% DIS@

RV35 100_0402_1% DIS@

+MVREFSA

CV95 1U_0402_6.3V4Z DIS@

[45,46] DRAM_RST

RV36 DIS@ 49.9_0402_1%

RV37 DIS@ 10_0402_1%

DRAM_RST_G

CV96 120P_0402_50V8J DIS@

RV38 5.1K_0402_1% DIS@

@ CV97 68P_0402_50V8J

Place close to GPU (within 25mm) and place componment close to each other

@ UV1C

U2

GDDR5/DDR3

M_DA0	K27	DQA0_0	MAA0_0/MAA_0	K17	M0_MA0	
M_DA1	J29	DQA0_1	MAA0_1/MAA_1	J20	M0_MA1	
M_DA2	H30	DQA0_2	MAA0_2/MAA_2	H23	M0_MA2	
M_DA3	H32	DQA0_3	MAA0_3/MAA_3	G23	M0_MA3	
M_DA4	G29	DQA0_4	MAA0_4/MAA_4	G24	M0_MA4	
M_DA5	F28	DQA0_5	MAA0_5/MAA_5	H24	M0_MA5	
M_DA6	F32	DQA0_6	MAA0_6/MAA_6	J19	M0_MA6	
M_DA7	F30	DQA0_7	MAA0_7/MAA_7	K19	M0_MA7	
M_DA8	C30	DQA0_8	MAA0_8/MAA_13	G20	M0_MA8	
M_DA9	F27	DQA0_9	MAA0_9/MAA_15	L17		
M_DA10	A28	DQA0_10		J14	M1_MA0	
M_DA11	C28	DQA0_11	MAA1_0/MAA_8	K14	M1_MA1	
M_DA12	E27	DQA0_12	MAA1_1/MAA_9	J11	M1_MA2	
M_DA13	G26	DQA0_13	MAA1_2/MAA_10	J13	M1_MA3	
M_DA14	D26	DQA0_14	MAA1_3/MAA_11	H11	M1_MA4	
M_DA15	F25	DQA0_15	MAA1_4/MAA_12	G11	M1_MA5	
M_DA16	A25	DQA0_16	MAA1_5/MAA_BA2	J16	M1_MA6	
M_DA17	C25	DQA0_17	MAA1_6/MAA_BA0	L15	M1_MA7	
M_DA18	E25	DQA0_18	MAA1_7/MAA_BA1	G14	M1_MA8	
M_DA19	D24	DQA0_19	MAA1_8/MAA_14	L16		
M_DA20	E23	DQA0_20	MAA1_9/RSVD			
M_DA21	F23	DQA0_21				
M_DA22	D22	DQA0_22	WCKA0_0/DQMA0_0	E32	M_WCKA0_0	M_WCKA0_0 [45]
M_DA23	F21	DQA0_23	WCKA0B_0/DQMA0_1	E30	M_WCKA0_0#	M_WCKA0_0# [45]
M_DA24	E21	DQA0_24	WCKA0_1/DQMA0_2	A21	M_WCKA0_1	M_WCKA0_1 [45]
M_DA25	D20	DQA0_25	WCKA0B_1/DQMA0_3	C21	M_WCKA0_1#	M_WCKA0_1# [45]
M_DA26	F19	DQA0_26	WCKA1_0/DQMA1_0	E13	M_WCKA1_0	M_WCKA1_0 [46]
M_DA27	A19	DQA0_27	WCKA1B_0/DQMA1_1	D12	M_WCKA1_0#	M_WCKA1_0# [46]
M_DA28	D18	DQA0_28	WCKA1_1/DQMA1_2	E3	M_WCKA1_1	M_WCKA1_1 [46]
M_DA29	F17	DQA0_29	WCKA1B_1/DQMA1_3	F4	M_WCKA1_1#	M_WCKA1_1# [46]
M_DA30	A17	DQA0_30				
M_DA31	C17	DQA0_31		H28	M_EDC_0	
M_DA32	E17	DQA1_0	EDCA0_0/QSA0_0	C27	M_EDC_1	M_EDC_1 [45]
M_DA33	D16	DQA1_1	EDCA0_1/QSA0_1	A23	M_EDC_2	M_EDC_2 [45]
M_DA34	F15	DQA1_2	EDCA0_2/QSA0_2	E19	M_EDC_3	M_EDC_3 [45]
M_DA35	A15	DQA1_3	EDCA0_3/QSA0_3	E15	M_EDC_4	M_EDC_4 [46]
M_DA36	D14	DQA1_4	EDCA1_0/QSA1_0	D10	M_EDC_5	M_EDC_5 [46]
M_DA37	F13	DQA1_5	EDCA1_1/QSA1_1	D6	M_EDC_6	M_EDC_6 [46]
M_DA38	A13	DQA1_6	EDCA1_2/QSA1_2	G5	M_EDC_7	M_EDC_7 [46]
M_DA39	C13	DQA1_7	EDCA1_3/QSA1_3			
M_DA40	E11	DQA1_8		H27	M_DBI0#	
M_DA41	A11	DQA1_9	DDBIA0_0/QSA0_0B	A27	M_DBI1#	M_DBI0# [45]
M_DA42	C11	DQA1_10	DDBIA0_1/QSA0_1B	C23	M_DBI2#	M_DBI1# [45]
M_DA43	F11	DQA1_11	DDBIA0_2/QSA0_2B	C19	M_DBI3#	M_DBI2# [45]
M_DA44	A9	DQA1_12	DDBIA0_3/QSA0_3B	C15	M_DBI4#	M_DBI3# [45]
M_DA45	C9	DQA1_13	DDBIA1_0/QSA1_0B	E9	M_DBI5#	M_DBI4# [46]
M_DA46	F9	DQA1_14	DDBIA1_1/QSA1_1B	C5	M_DBI6#	M_DBI5# [46]
M_DA47	D8	DQA1_15	DDBIA1_2/QSA1_2B	H4	M_DBI7#	M_DBI6# [46]
M_DA48	E7	DQA1_16	DDBIA1_3/QSA1_3B			M_DBI7# [46]
M_DA49	A7	DQA1_17		L18	M_ADBI0	
M_DA50	C7	DQA1_18	ADBIA0/ODTA0	K16	M_ADBI1	M_ADBI0 [45]
M_DA51	F7	DQA1_19	ADBIA1/ODTA1			M_ADBI1 [46]
M_DA52	A5	DQA1_20		H26	M_CLK0	
M_DA53	E5	DQA1_21	CLKA0	H25	M_CLK#0	M_CLK0 [45]
M_DA54	C3	DQA1_22	CLKA0B			M_CLK#0 [45]
M_DA55	E1	DQA1_23		G9	M_CLK1	
M_DA56	G7	DQA1_24	CLKA1	H9	M_CLK#1	M_CLK1 [46]
M_DA57	G6	DQA1_25	CLKA1B			M_CLK#1 [46]
M_DA58	G1	DQA1_26		G22	M_RAS#0	
M_DA59	G3	DQA1_27	RASA0B	G17	M_RAS#1	M_RAS#0 [45]
M_DA60	J6	DQA1_28	RASA1B			M_RAS#1 [46]
M_DA61	J1	DQA1_29		G19	M_CAS#0	
M_DA62	J3	DQA1_30	CASA0B	G16	M_CAS#1	M_CAS#0 [45]
M_DA63	J5	DQA1_31	CASA1B			M_CAS#1 [46]
				H22	M_CS0B#0	
+MVREFDA	K26	MVREFDA	CSA0B_0	J22		M_CS0B#0 [45]
+MVREFSA	J26	MVREFSA	CSA0B_1			
	J25			G13	M_CS1B#0	
RV39 1 DIS@ 2 120_0402_1%	K25	NC#J25 MEM_CALRP0	CSA1B_0	K13		M_CS1B#0 [46]
			CSA1B_1			
				K20	M_CKE0	
			CKEA0	J17	M_CKE1	M_CKE0 [45]
			CKEA1			M_CKE1 [46]
				G25	M_WE#0	
DRAM_RST_G	L10		WEA0B	H10	M_WE#1	M_WE#0 [45]
		DRAM_RST	WEA1B			M_WE#1 [46]
	K8					
	L7	CLKTESTA CLKTESTB				

RV40 @ 1 2 51.1_0402_1% CV98 @1 2 0.1U_0402_16V4Z

RV41 @ 1 2 51.1_0402_1% CV99 @1 2 0.1U_0402_16V4Z

Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation,if not need, DNI.

216-0842024-A11-MAR_FCBGA631

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: MESO_(5/5)_MEM

Size: Custom | Document Number: LA-D801P | Rev: A00

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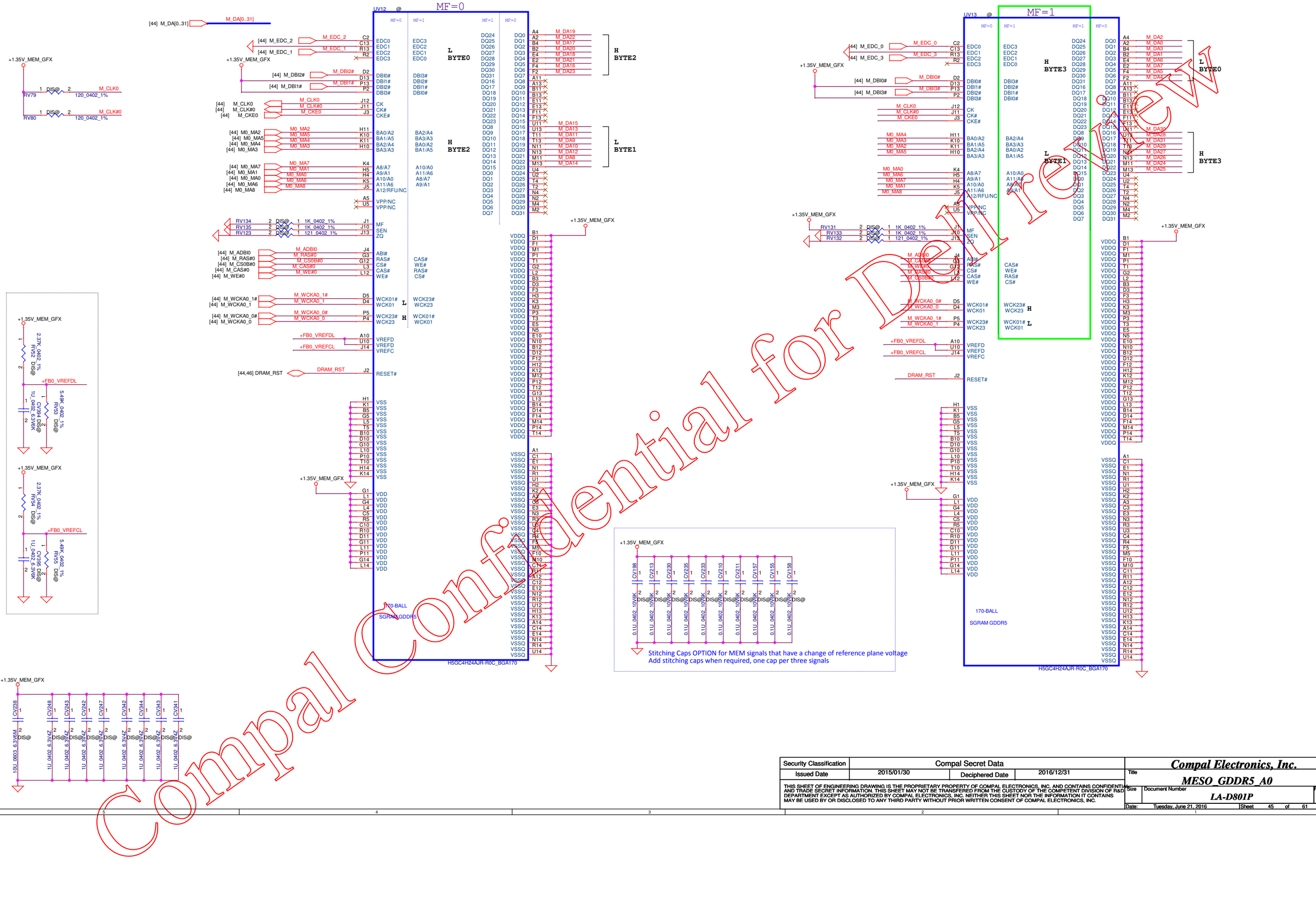

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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Compal Electronics, Inc.			
Title	MESO_GDDR5_A0		
Size	Document Number	LA-D801P	Rev A00
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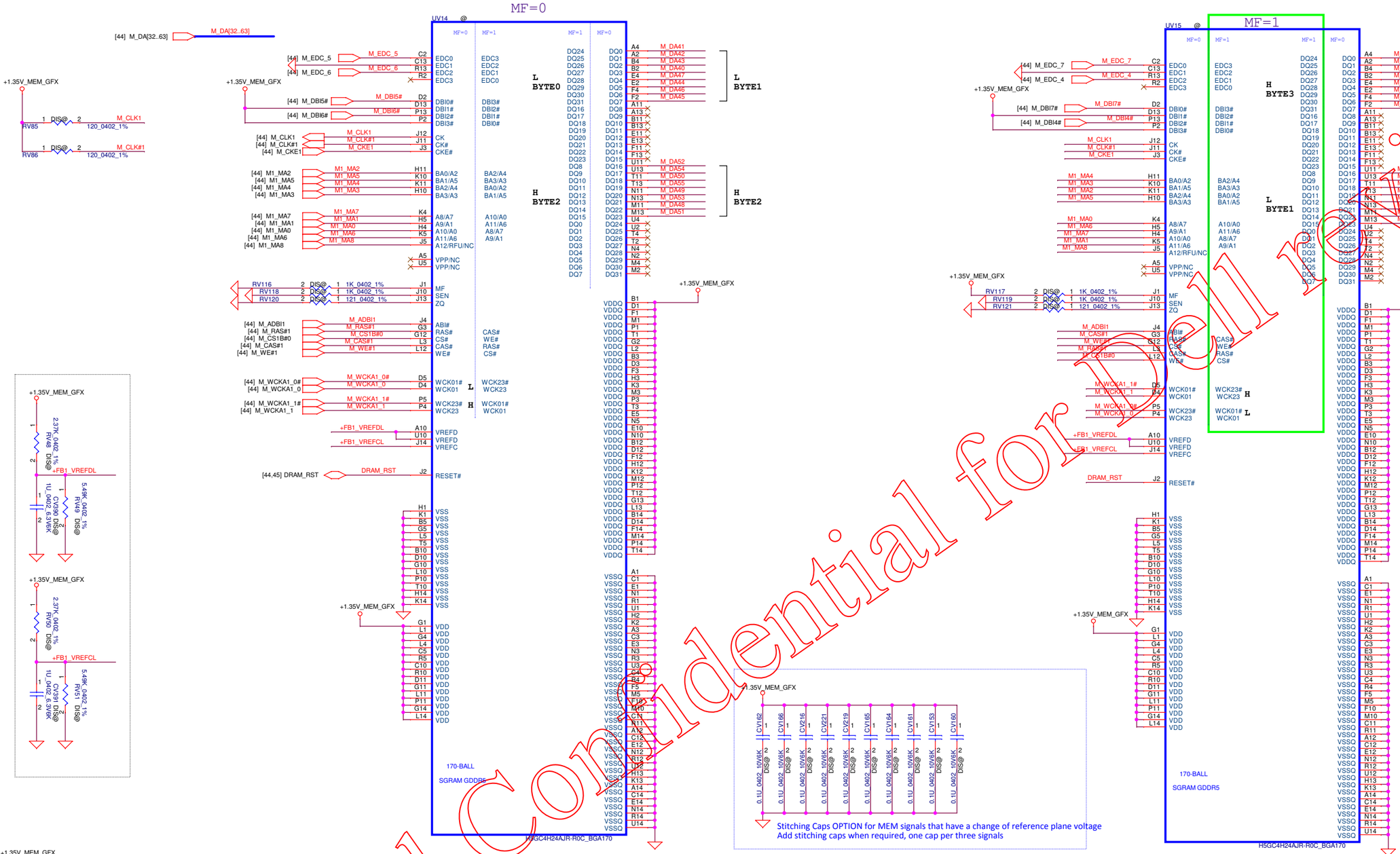
MF=0

MF=1



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	MESO_GDDR5_A1		
Size	Document Number		Rev
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Date: Tuesday, June 21, 2016	Sheet 46 of 61		

Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

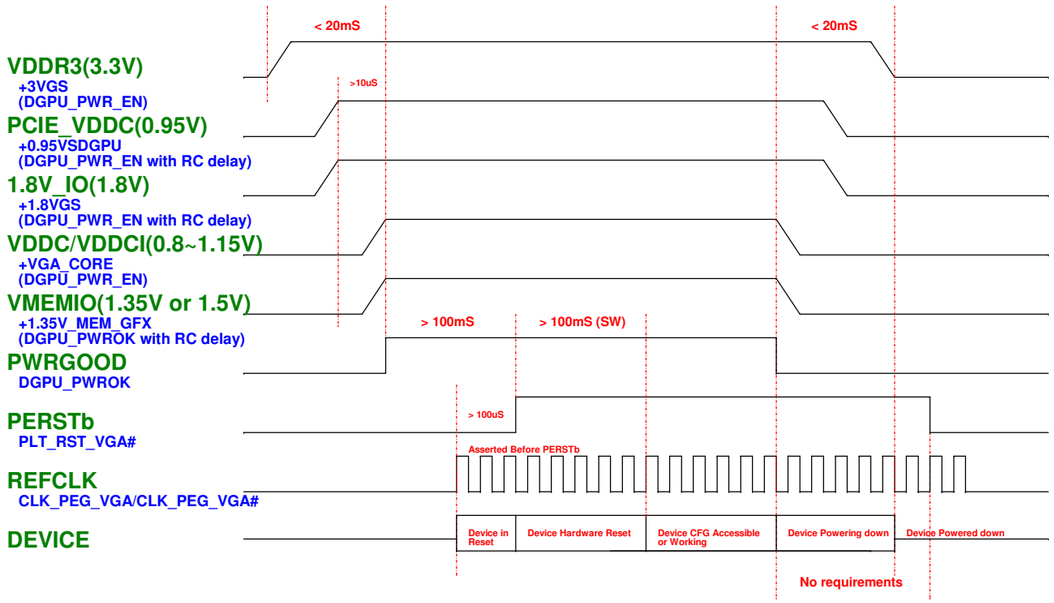
2. It is recommended that the 3.3-V rail ramp up first.

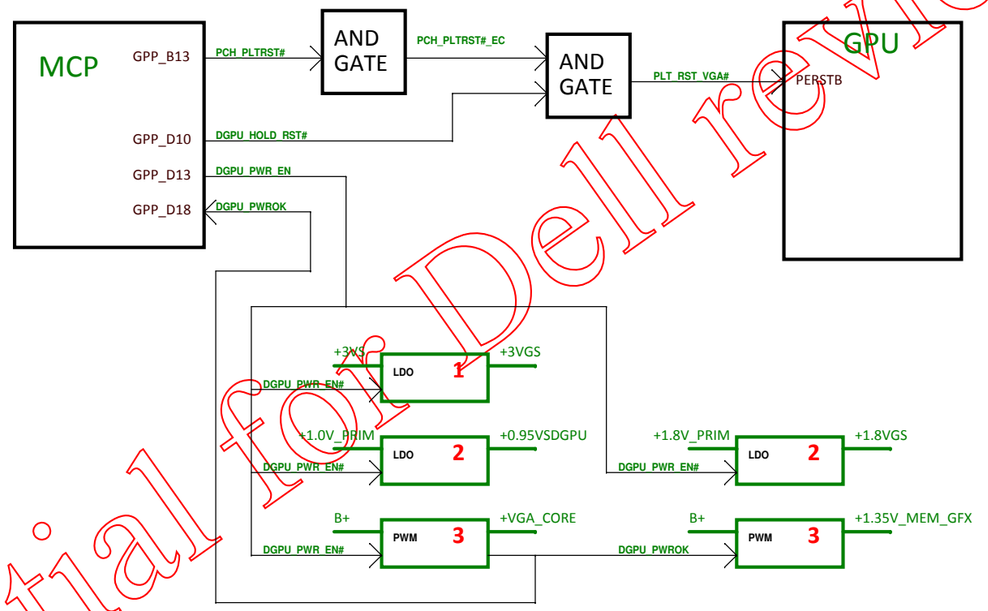
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.

4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µs).

5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

6. For power down, reversing the ramp-up sequence is recommended.





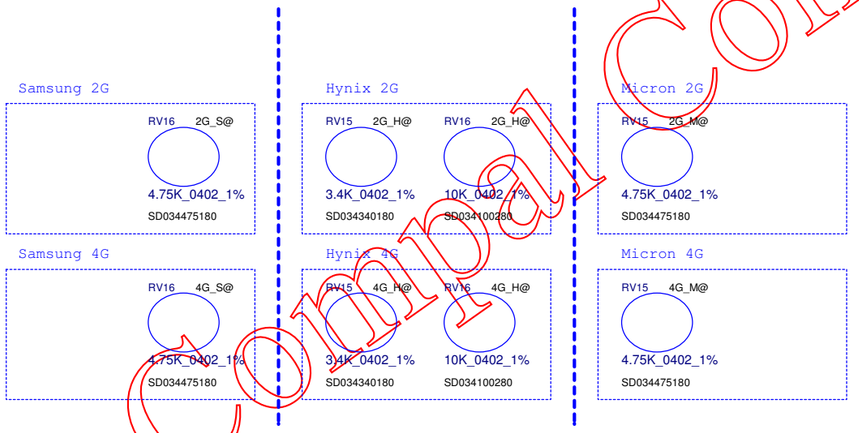


Table 3–21 Resistor Divider Lookup T.

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

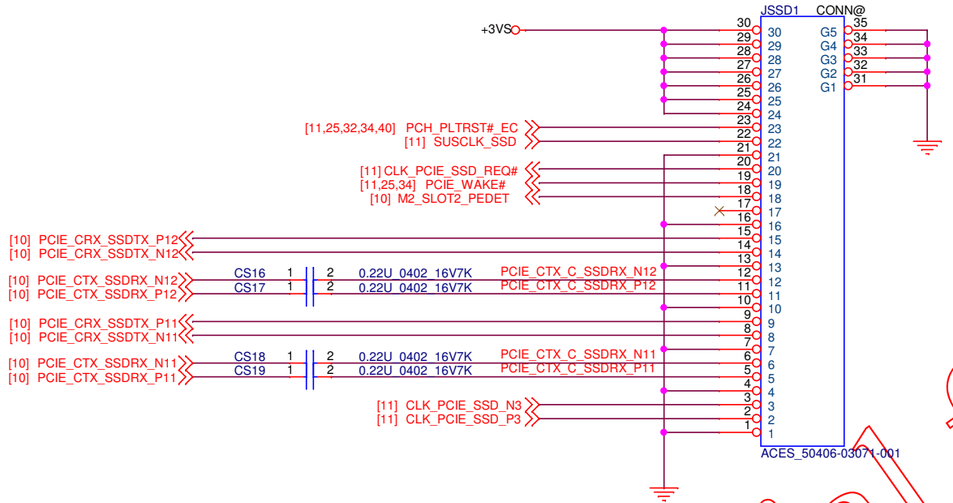
For AMD R16M-M1-70 VRAM Only

Memory ID	4Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70:A A31!	4GB

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: MESO_Note			
Size	Document Number: LA-D801P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 47 of 61		



"M2_SLOT2_PEDET" PU 10k on DB

PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: SSD

Size: Custom | Document Number: LA-D801P | Rev: A00

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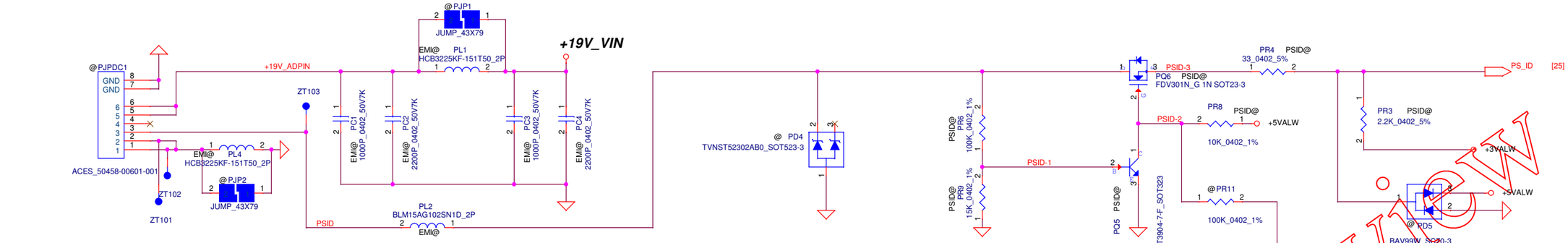
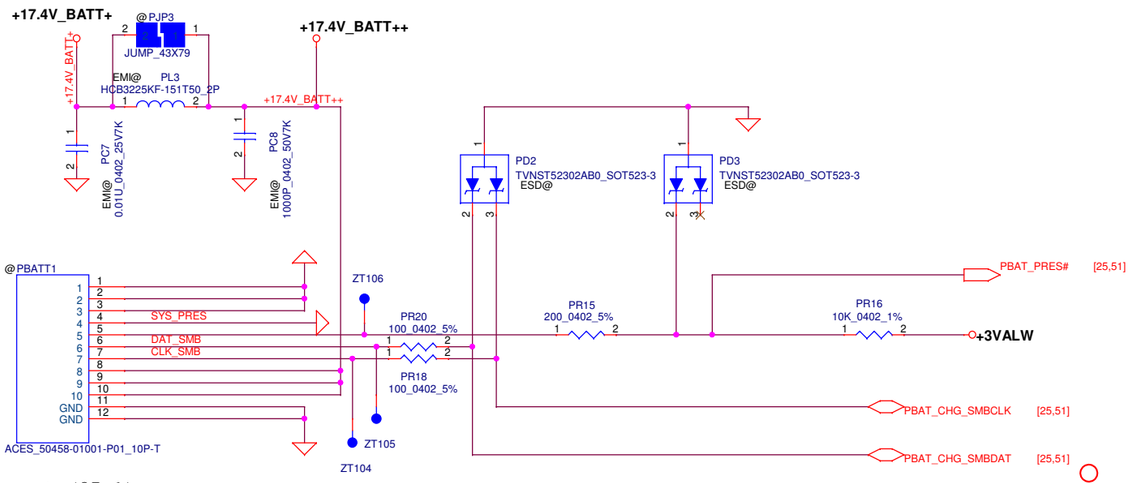
Version Change List (P. I. R. List)

Item	Date	Page	Part reference	change description	Reason
Design Change					
Based on LA-D801P_0106					
1	2016/1/8	20	CD29	Change CD29 Pin1 Net from "H_DRAMRST#" to "DDR4_DRAMRST#"	Modify DDR4_DRAMRST# Sequence
2	2016/1/8	20, 21	CD27,CD57	Change CD27,CD57 Footprint	Material change, D7 H1.1 --> D2 H1.9
3	2016/1/8	22	H8,H9,H10,H11,H13	Modify H8,H9,H10,H11, Add H13	ME change
4	2016/1/8	22	TP27,TP28,TP29	Add TP27,TP28,TP29	CPU Test point
5	2016/1/14	22	U1,C17,R57	Change U1,C17, Add R57	Change to Stand Part
6	2016/1/20	9	~~JWDB1,RC190,RC191~~	~~Add JWDB1,RC190,RC191~~	~~Add Win7 Debug~~
7	2016/2/2	39	CZ20	Change CZ20 Pin1 Net from "+1.8VGS" to "+1.8VGS_OUT"	Layout
8	2016/2/2	18	L1,L2	Change L1,L2 Footprint	Material change, sourcer request
9	2016/2/2	30	F3	Change F3 Footprint	Material change, sourcer request
10	2016/3/2	18	CC61	Change CC61 Pin1 Net from "+3.3V_HDA" to "+3VALW_PCH"	follow RF test result
11	2016/3/2	18	CC82	Change CC82 Pin1 Net from "+1.0V_APLL" to "+1.0V_PRIM"	follow RF test result
12	2016/3/2	48	JSSD1	Swap SSD Pin define and cancel "SSD_DEVSLP"	For cable wiring methods
13	2016/3/4	35	JLAN1	JLAN1.9 --> LANGND1 JLAN1.10 --> LANGND1 JLAN1.11 --> LANGND2 JLAN1.12 --> LANGND2 CL13.2 --> LANGND2	HI-POT modify
14	2016/3/8	25. 28	UEI.113,RB64,D4.3	UEI.113 add 0 ohm then connect to D4.3	Modify LCD BITS Sequence
15	2016/3/10	33	RP12,LI2	HDMI_CLK#_R --> HDMI_CLK_R HDMI_DATA0#_R --> HDMI_DATA0_R HDMI_DATA0#_R_C --> HDMI_DATA0_R_C	HDMI signal Layout modify, EMI request
16	2016/3/16	17, 36, 39	CZ21,CZ22,CZ23,CZ24,CZ25,CZ26,CZ27,CZ28,CZ29,CZ30,CZ31	Add Capacitance close to Vin, Vbias, Vout, CT	Load Switch common design
17	2016/3/16	9	RC190,RC191	Add RC190,RC191 connect to GPP_A22	VRAM ID
18	2016/3/18	35	JLAN1	JLAN1.9 --> GND JLAN1.10 --> GND JLAN1.11 --> GND JLAN1.12 --> GND CL13.2 --> GND	HI-POT modify
19	2016/3/21	11, 17	DZ4,DZ5,RZ9,RC192	Reserve DZ4,DZ5,RZ9,RC192	Speed up SLP_S3# & SLP_S3# power down sequence
20	2016/3/22	29	JPWR1	Change JPWR1 Footprint	ME request
21	2016/3/22	48	JSSD1	PCIE_CRX_SSDTX_P12 --> PCIE_CRX_SSDTX_P11 PCIE_CRX_SSDTX_N12 --> PCIE_CRX_SSDTX_N11 PCIE_CTX_SSDRX_N12 --> PCIE_CTX_SSDRX_N11 PCIE_CTX_SSDRX_P12 --> PCIE_CTX_SSDRX_P11 PCIE_CTX_C_SSDRX_N12 --> PCIE_CTX_C_SSDRX_N11 PCIE_CTX_C_SSDRX_P12 --> PCIE_CTX_C_SSDRX_P11	For cable wiring methods
22	2016/3/22	20	CD29	Change CD29 BOM Config to @	SAMMANG DRAM issue
DVT2					
23	2016/4/22	25	UEI.30	Change LED control signal net name from "SATA_LED#_R" to "SATA_LED_EN"	EC request
24	2016/4/22	29	JPWR1	Change Footprint	ME request
25	2016/4/25	22	H6	Φ5 --> Φ5.6	ME request
26	2016/4/25	24	RA36,RA37	Change footprint from Bead to Resistance	EMI request
27	2016/4/25	45	UV3,UV4,UV5,UV6	Change footprint from "MT41J128M16JT-093_FBGA_96P_A39" to "MT41J256M16LY-091G-N_FBGA_96P"	DFB request, LA-D805P only
28	2016/5/3	29	JPWR1	Change Footprint, E-T_6915K-Q06N-00L --> JXT_FP226H-006S1BM	ME request
29	2016/5/3	12	CC89	Add "1pF_0402" on "HDA_RST#"	RF request
Pilot					
~~30~~	~~2016/5/5~~	~~18~~	~~L2~~	~~Change Footprint, BLM15BD601SN1D --> LQG15HS4N7S02D~~	~~RF request~~
31	2016/5/9		RA1,RA22,RW3,R51	Change Footprint from "R_0805" to "R0805_0ohm"	Change to Short PAD
			RA4,RA39,RC17,RC161,RC1	Change Footprint from "R_0603" to "R0603_0ohm"	
			RA2,RA5,RA17,RA18,RA6,R	Change Footprint from "R_0402" to "R0402_0ohm"	
32	2016/5/10		RE45,RE22,RE28,RE37,RE38	Change Footprint from "R_0402" to "R0402_0ohm"	Change to Short PAD
33	2016/5/20		LW1,L4	Change Footprint from "INPAQ_MCM1012B900F06BP_4P" to "INPAQ_MCM1012B900F06BP_4P	Close solder mask
34	2016/5/20		LU2,LU3,LU5,LU6	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NPI	Close solder mask
35	2016/5/20		RU1,RU2,RX4,RX7,RU7,RX	Change Footprint from "R_0402" to "R0402-NPM"	Close solder mask
36	2016/5/20	30	JKB1	Change Footprint from "ACES_50699-03041-P01_30P" to "STARC_132C30-100020-A2-R_30P"	DFB request
37	2016/5/30	11	RC81	Del RC81	For Layout optimally
38	2016/6/13	33	LI1,LI2,LI3,LI4	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NPI	Close solder mask
39	2016/6/15	7	CC90	Add CC90	Reserve for fine-tune +0.6V_DDR_VTT sequence
40	2016/6/15		RC75,RE45	Change Footprint from "R0402_0ohm" to "R_0402"	Change to 0 Ohm
41	2016/6/15		RW3	Change Footprint from "R0805_0ohm" to "R_0805"	Reserve for BT lose issue
42	2016/6/15		RW5	Change Footprint from "R_0402" to "R_0805"	



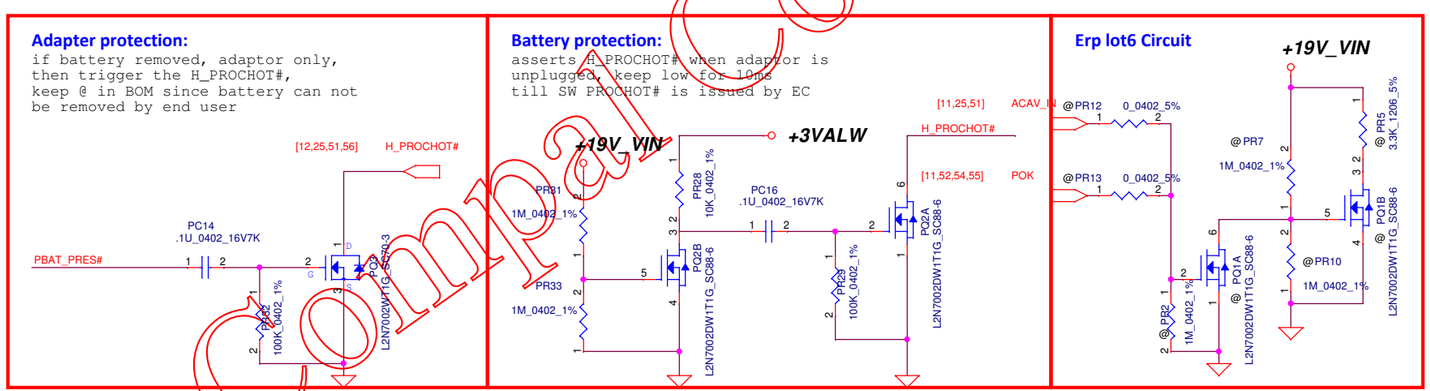


Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

Other component (37_1)

ACES_50458-01001-P01_10P-T



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Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev X00
Date: Tuesday, June 21, 2016	Sheet 50 of 61		

Iada=0~3.33A(65W)
Iada=0~2.30A(45W)

ADP_I = 32*Iadapter*Rsense

+19V_VIN
+19VB
+17.4V_BATT+
+3VALW
+1.8V_VIN

PQ709 L2N7002WT1G_SC70-3
PR738 1M_0402_1%
PR737 3M_0402_5%
PQ718 MDU1512RH_POWERDFN56-8-5
PQ740 MDU1512RH_POWERDFN56-8-5
PR703 0.01_1206_1%
@EMI@ PL704 1UH_PCMB053T-1R0MS_7A_20%
@PJP701 JUMP_43X118
PC760 10U_0805_25V6K
@PC762 10U_0805_25V6K
@PC763 10U_0805_25V6K
PC764 10U_0805_25V6K
PC765 0.1U_0402_25V7K
EMI@ PC705 220P_0402_25V7K
EMI@ PC780 100P_0402_25V8J
EMI@ PC781 100P_0402_25V8J
@ PC742 5600P_0402_25V7K
PC744 0.1U_0402_25V6
@PR778 0_0402_5%
@ PR772 0_0402_5%
PR740 2_0402_5%
PC747 0.1U_0402_25V6
PR762 4.02K_0402_1%
PR763 4.02K_0402_1%
PR745 100_0402_1%
@PR773 0_0603_5%
PC750 0.22U_0603_25V7K
PR739 392K_0402_1%
PR732 53.6K_0402_1%
PC711 0.01UF_0402_25V7K
PR741 100K_0402_1%
PQ712 L2N7002WT1G_SC70-3
[25] AC_DIS
For Learn Mode
CMSRC
ASGATE
VDD_CHG
ACIN_CHG
ACIN
[11,25,50] ACAV_IN
PR731 150K_0402_1%
[25,50] PBAT_CHG_SMBDAT
[25,50] PBAT_CHG_SMBCLK
[25,50,56] H_PROCHOT#
[25] I_ADP
[25] I_BATT
[25,56] I_SYS
PROH
PR777 0_0402_5%
PR774 1K_0402_1%
@PR769 0_0402_5%
@PR770 0_0402_5%
@PR775 0_0402_5%
PU703 ISL88739HRZ-T_QFN32_4X4
ACIN ACOK SDA SCL PROCHOT# AMON BMON PSYS AGND PROG COMP CCLIM FSET BATGONE CSON CSOP ACLIM
BOOT UGATE PHASE LGATE VDOP VDO DCIN NTC VBAT BGATE
UGATE_CHG PHASE_CHG LGATE_CHG VDDP_CHG VDD_CHG
PC748 0.1U_0402_25V7K
PC749 2200P_0402_25V7K
@ PR727 10.5K_0402_1%
@PR771 0_0603_5%
PC721 0.22U_0402_16V7K
@PR761 0_0603_5%
PR760 4.7_0402_5%
PC768 1U_0402_16V6K
PC769 1U_0402_16V6K
PR757 100K_0402_1%
@ PR779 0_0402_5%
PC757 1U_0603_25V6
PR743 10_1206_5%
PD704 LRB715FT1G_SOT323-3
AON7408L_DFN8-5 PQ704
AON7506_DFN33-8-5 PQ708
PL700 4.7UH_5.5A_20%_7X7X3_M
PR765 0.01_1206_1%
@EMI@ PR766 4.7_1206_5%
@EMI@ PC767 680P_0603_50V7K
PC778 10U_0805_25V6K
PC775 10U_0805_25V6K
@ PC776 10U_0805_25V6K
PC777 0.1U_0402_25V7K
PC761 10U_0805_25V6K
PC766 10U_0805_25V6K
PQ710 LMUN5113T1G_SOT323-3
@ PR750 0_0603_5%
SIO_SLP_S5# [11]
PQ711 LTC015EUBFS8TL_UMT3F
PR742 2_0402_5%
PC708 0.1U_0402_25V6
@PR776 0_0402_5%
PR779 392K_0402_1%
PC779 0.1U_0402_25V7K
PQ717 MDU1512RH_POWERDFN56-8-5
PR749 200K_0402_1%
PR750 200K_0402_1%
PR751 75K_0402_1%
PR752 66.5K_0402_1%
PR753 182K_0402_1%
PC751 560P_0402_50V7K
PR754 100_0402_1%
PR755 102K_0402_1%
PC752 0.015U_0402_25V7K
PR764 10K_0402_1%
PC753 10P_0402_50V8J
@ PR756 10K_0402_1%
PBAT_PRES# [25,50]

Delay adaptor OC H_PROCHOT#
2ms while hybrid power transition
VDD_CHG
+3VALW
PR791 10K_0402_5%
PR781 10K_0402_5%
@PR790 160K_0402_1%
PQ721 RUM002N02GT2L_VMT3
PQ720 RUM002N02GT2L_VMT3
PC790 0.01U_0402_16V7K
H_PROCHOT#
PROH

3S1P: CV = 13.05V CC: 1.9A

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/03/23	Deciphered Date 2014/12/15	Title PWR_CHARGER
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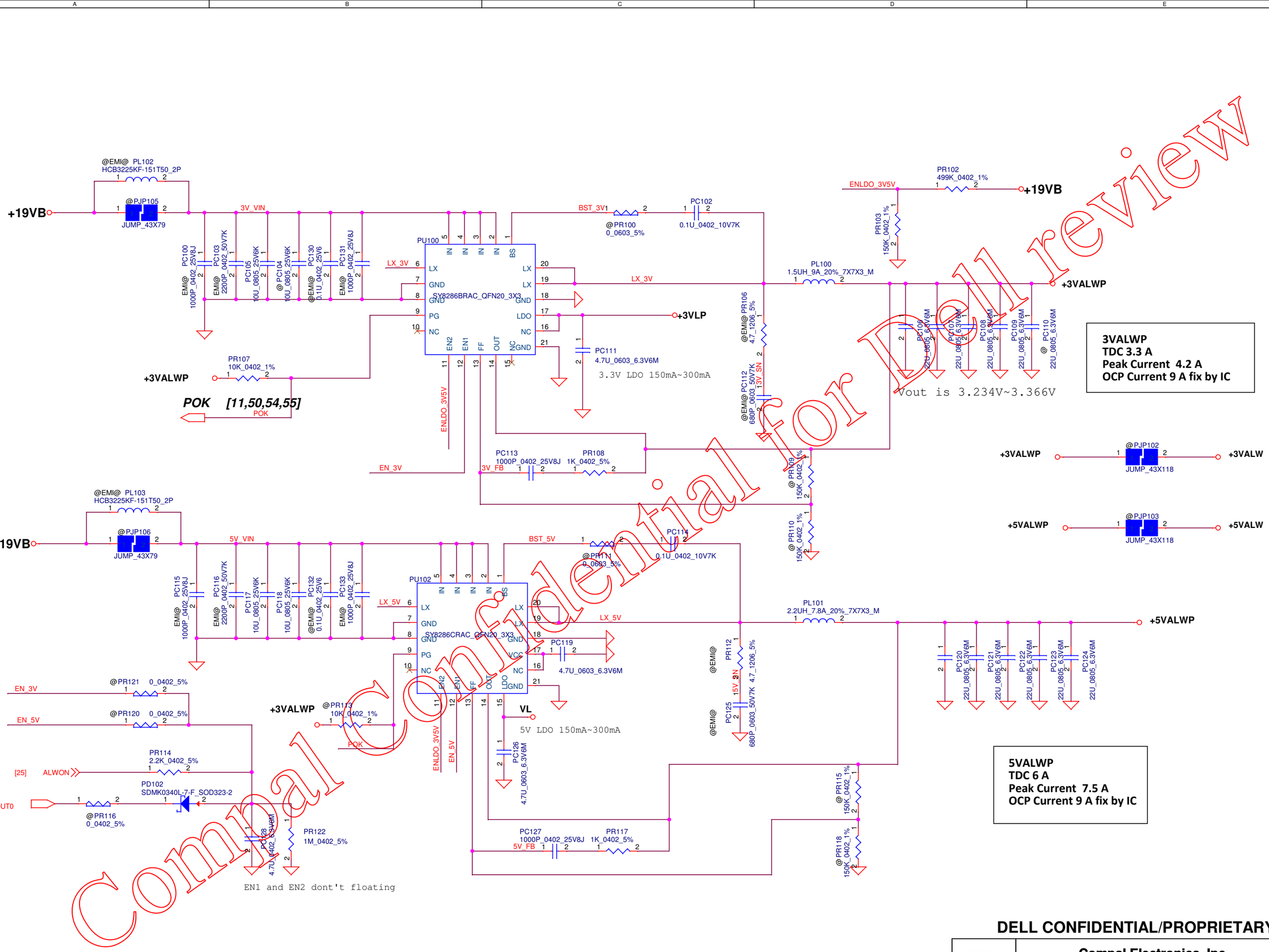
			Date: Tuesday, June 21, 2016 Sheet 51 of 61



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: PWR_3.3VALWP/5VALWP		
Size	Document Number: LA-D801P	Rev: X00
Date: Tuesday, June 21, 2016	Sheet 52 of 61	

0.6Volt +/- 5%
TDC 1.2A
Peak Current 1.5A

+1.2V_MEM
TDC 6.7 A
Peak Current 8.375 A
OCP Current 10.2 A

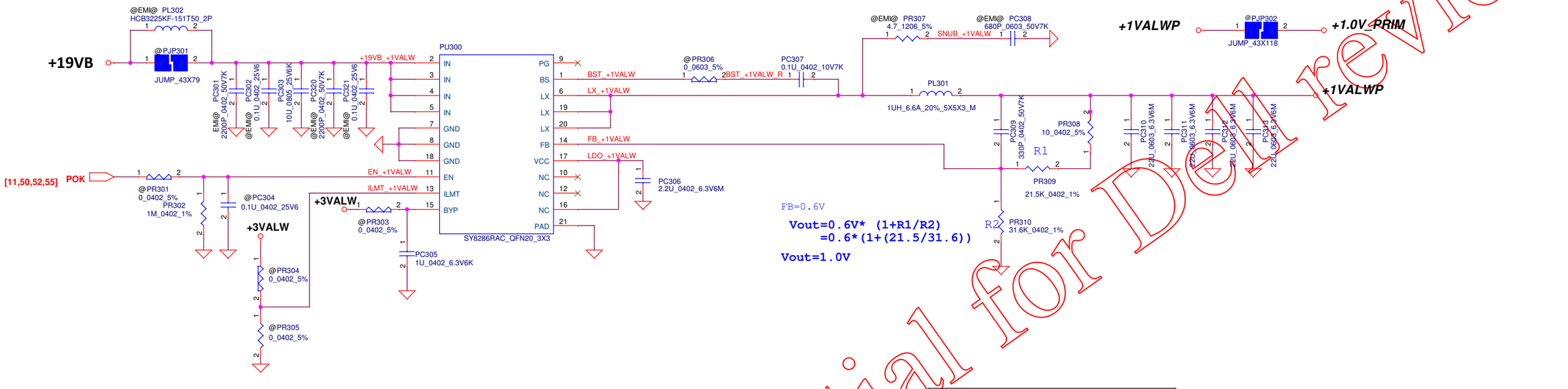
Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

For RT8207P

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT
Size: Custom | Document Number | Rev: X00
Date: Tuesday, June 21, 2016 | Sheet 53 of 61



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

+1.0V_PRIM
TDC 6 A
Peak Current 8.6 A
OCP Current 12 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm , 12.0mohm	

DELL CONFIDENTIAL/PROPRIETARY

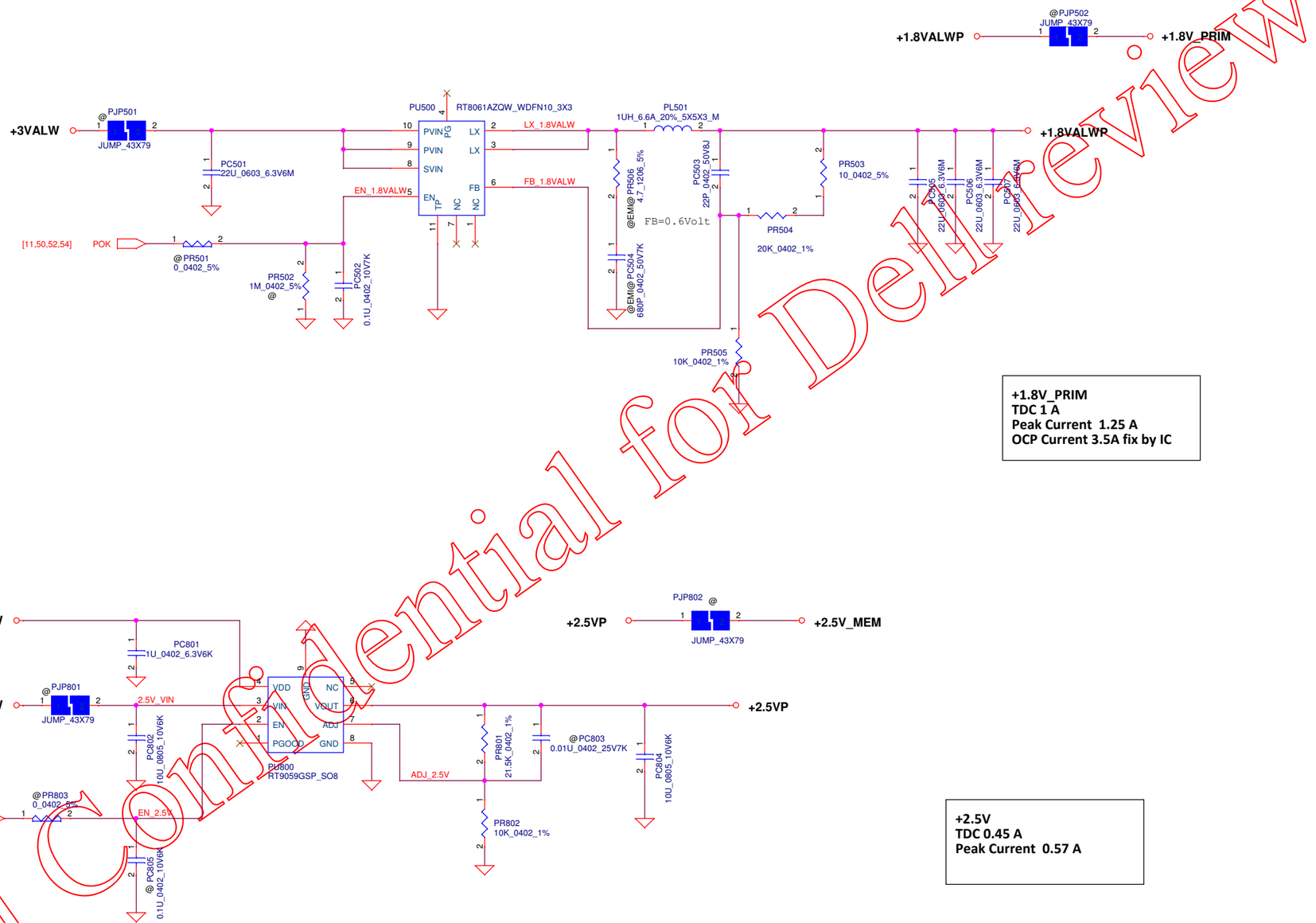
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: ***PWR_+1VALWP***

Size: C | Document Number: *LA-C142P* | Rev: X00

Date: Tuesday, June 21, 2016 | Sheet 54 of 61



Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_+1.8V_PRIM and +2.5V		
Size C	Document Number		Rev X00
Date: Tuesday, June 21, 2016	Sheet 55 of 61		

+1.0V_VCCST

Local sense put on HW site

VCC_SA
Loadline : 10.3m-ohm

TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5%m ohm

VCCSA_B+ — @ PJP603 — PAD-OPEN1x1m — CPU_B+

+5VALW

+3VS

VCCSA_B+

+VCC_SA

ISL95859HRTZ-T_TQFN40_5X5

PU602

PU606 ISL95808HRZ-TS2878_DFN8_2X2

AON7934_DFN3X3A-8-10 PQ601

PL601 0.68UH +-20% 7.9A

	U22@SKL	U22@KBL
PR640	255	280
PR648	1.37K	1.5K
PR629	84.5K	97.6K

PR640 U22@KBL@ 280_0402_1%

PR648 U22@KBL@ 1.5K_0402_1%

PR629 U22@KBL@ 97.6K_0402_1%

Local sense put on HW site

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/03/23	Deciphered Date 2014/12/15	Title PWR_+VCC_SA
			Size Document Number Rev X00
			Date: Tuesday, June 21, 2016 Sheet 56 of 61

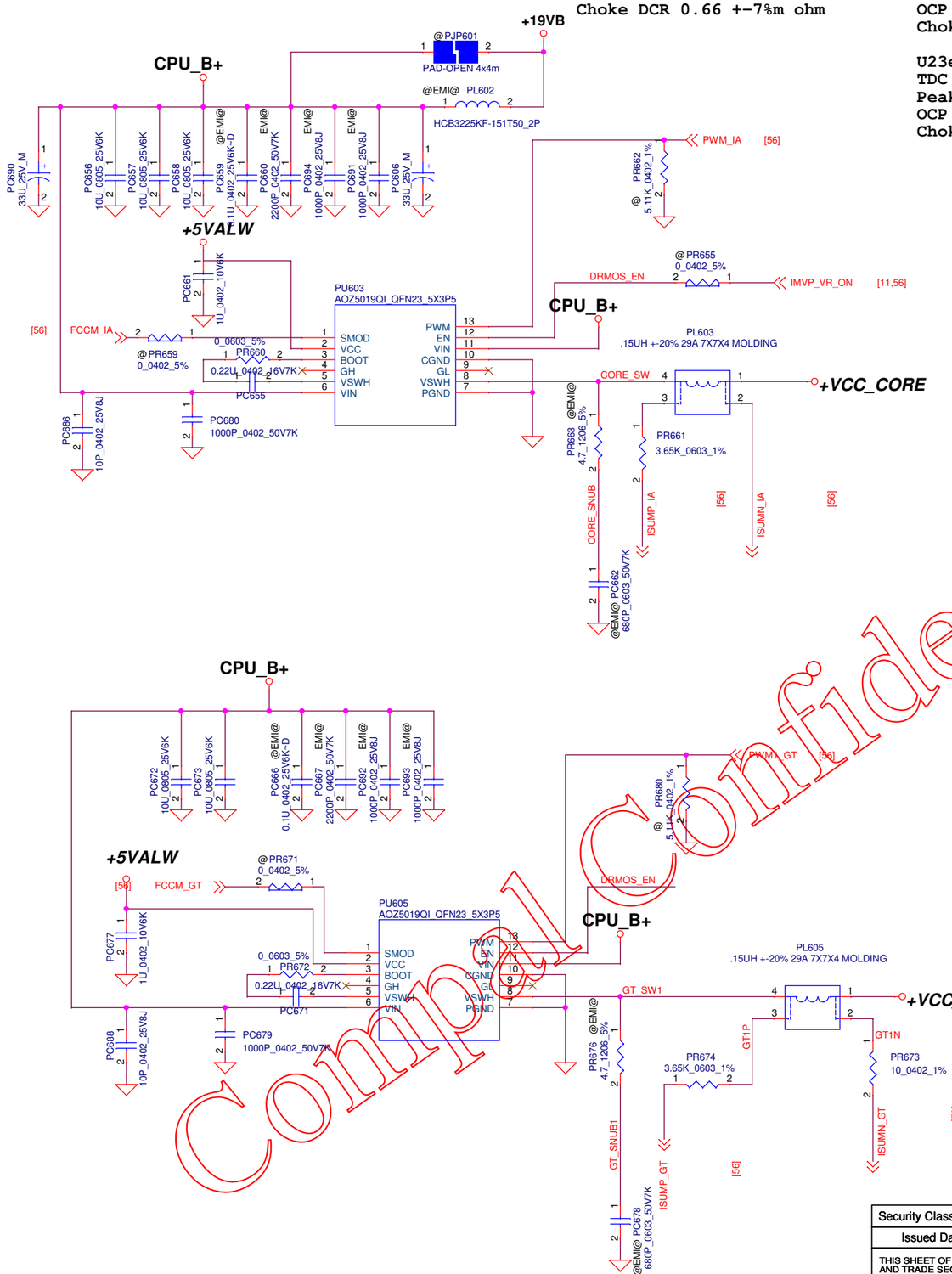
VCC_core
U22 – 15W
Loadline : 2.4m-ohm
U23e – 15W
Loadline : 2.4m-ohm

TDC 21A
Peak Current 29A (KBL : 32A)
OCP current 34A (KBL : 36A)
Choke DCR 0.66 +-7%m ohm

VCC_GT
U22 – 15W
Loadline : 3.1m-ohm
U23e – 15W
Loadline : 2m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7%m ohm

U23e-15W
TDC 36A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7%m ohm



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Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title: PWR_+VCC_core and +VCC_GT			
Size	Document Number		Rev X00
Date: Tuesday, June 21, 2016	Sheet 57 of 61		

SKL :
VCC_CORE Place on CPU
Back Side.
22U_0603 * 15 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 3 pcs+330u_D2*2 pcs

KBL :
VCC_CORE Place on CPU
Back Side.
22U_0603 * 15 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 5 pcs+330u_D2*2 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 19 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 6 pcs +330u*1 pcs

+VCC_CORE

PC1076 PC1078 PC1077 PC1079 PC1001 PC1002 PC1003 PC1004 PC1005 PC1006 PC1007 PC1008 PC1009 PC1010 PC1011 PC1012 PC1013
22U_0603_6.3V6M

PC1081 PC1080 PC1082 PC1067 PC1072 PC1069 PC1074 PC1070 PC1061 PC1071 PC1066 PC1073 PC1068 PC1075 PC1064 PC1065
22U_0603_6.3V6M
U22@KBL@

PC1083 PC1030 PC1031 PC1032 PC1033 PC1034 PC1035 PC1036 PC1037 PC1038 PC1039 PC1084 PC1086 PC1085 PC1088 PC1087 PC1089
1U_0201_6.3V6M

PC1099 PC1095 PC1094 PC1096 PC1090 PC1093 PC1091 PC1097 PC1092 PC1098 PC1050 PC1051 PC1052 PC1053 PC1054 PC1126 PC1164 PC1125
1U_0201_6.3V6M

PC1127 220U_2V_Y_D2
PC1062 220U_2V_Y_D2
PC1170 PC1171 PC1172 PC1173 PC1174
22U_0603_6.3V6M
U22@KBL@

VCC_SA Place on CPU
Back Side.
22U_0603 * 6 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 3 pcs

+VCC_GT

PC1014 PC1015 PC1016 PC1017 PC1018 PC1019 PC1020 PC1021 PC1022 PC1023 PC1024 PC1025 PC1026
22U_0603_6.3V6M

PC1133 PC1137 PC1129 PC1132 PC1136 PC1134 PC1135 PC1138 PC1027 PC1028 PC1130 PC1029 PC1131
22U_0603_6.3V6M

PC1040 PC1041 PC1042 PC1043 PC1044 PC1045 PC1046 PC1047 PC1048 PC1049 PC1055 PC1056
1U_0201_6.3V6M

PC1128 330U_2V_M
PC1063 330U_2V_M
PC1181 PC1180 PC1177 PC1179 PC1176 PC1178 PC1175 PC1182 PC1184 PC1183
22U_0603_6.3V6M

+VCC_SA

PC1057 PC1058 PC1059 PC1060 PC1139 PC1140 PC1141 PC1142 PC1143 PC1144 PC1145 PC1146
22U_0603_6.3V6M

PC1153 PC1147 PC1148 PC1149 PC1150 PC1151 PC1152
1U_0201_6.3V6M

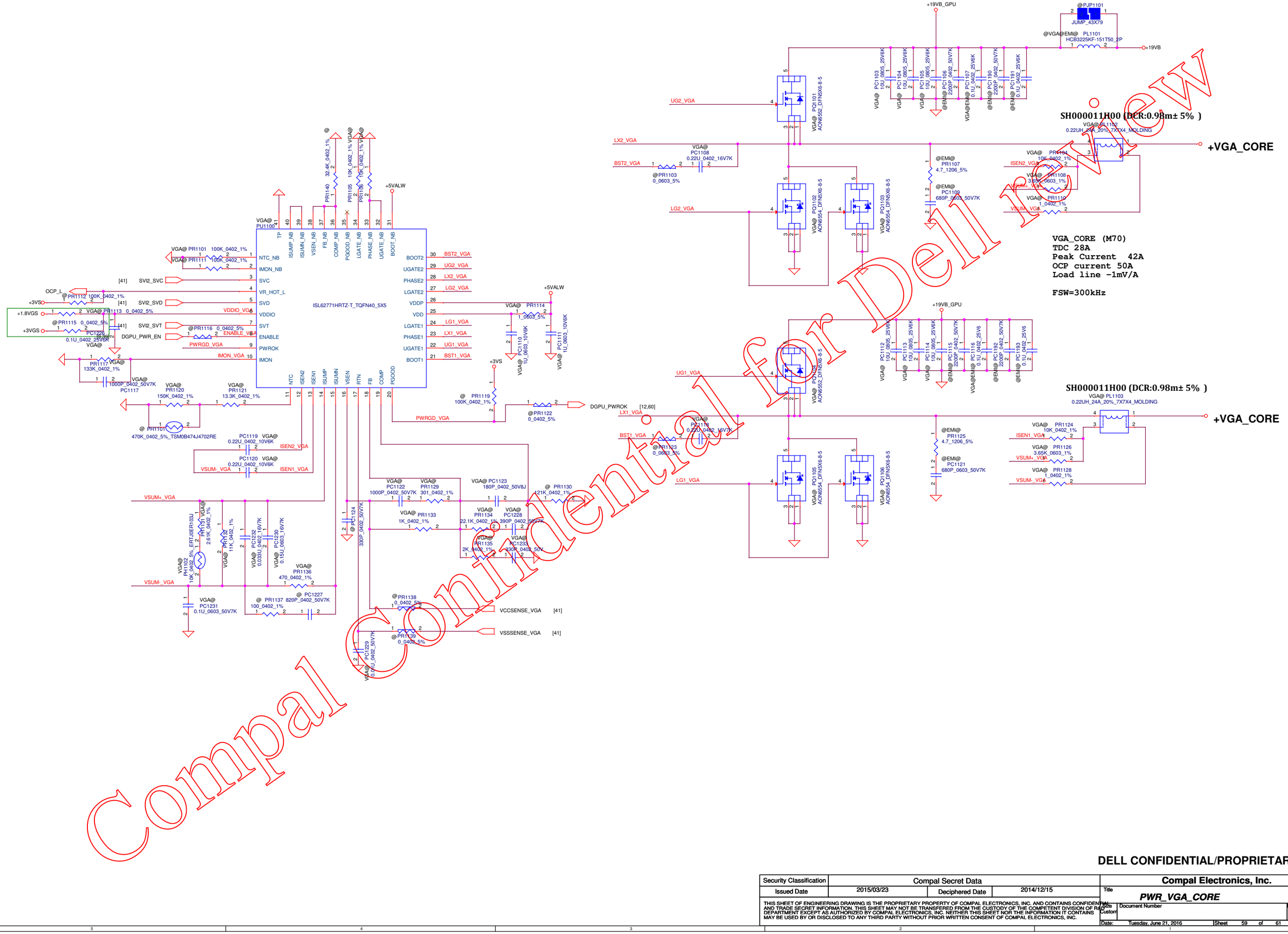
+VGA_CORE

PC836 PC837 PC838 PC839
330U_2V_M
VGA@

For VGACORE

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title: PWR_CPU&VGA bulk and MLCC			
Size	Document Number		Rev X00
Date: Tuesday, June 21, 2016	Sheet 58 of 61		



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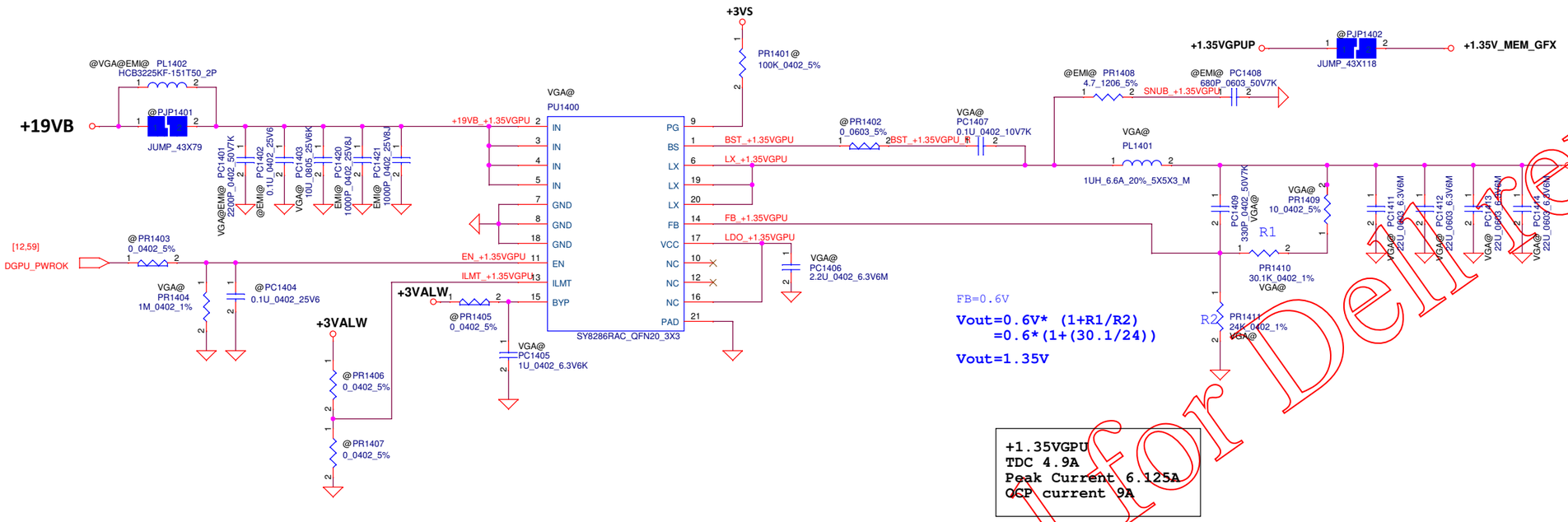
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/03/23	Deciphered Date 2014/12/15	Title: PWR_VGA_CORE

Size: Custom	Document Number		Rev: X00
Date: Tuesday, June 21, 2016	Sheet 59 of 61		



+1.35VGPU
TDC 4.9A
Peak Current 6.125A
OCP current 9A

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin13)
6A	Pull low
9A	Floating
12A	Pull high

Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **PWR_+1.35VGPU**

Size | Document Number: **LA-D801P** | Rev: X00

Date: Tuesday, June 21, 2016 | Sheet 60 of 61

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL	design change charger IC design change	PU706 change to ISL88739 PR732 change to 53.6K PR774 change to 1K PC748 change to 0.1U delete PR727,PC762,PC763,PC776	0.1(X00)
2	P56	PWR	20160321	COMPAL	design change for IA_Core Iccmax 32A	Change the PR640 to 280 Ohm Change the PR648 to 1.5k Change the PR629 to 93.1k	0.1(X00)
3	P58	PWR	20160321	COMPAL	design change	delete PC1003,PC1004,PC1006,PC1012,PC1013,PC1014,PC1015,PC1017,PC1019, PC1020,PC1021,PC1025,PC1027,PC1058,PC1059,PC1060,PC1068,PC1070,PC1071, PC1073,PC1074,PC1075,PC1076,PC1077,PC1078,PC1079,PC1080,PC1081,PC1082 add PC1170,PC1171,PC1172,PC1173,PC1174,PC1175,PC1176,PC1177,PC1180, PC1181,PC1182,PC1183	0.1(X00)
4	P50	PWR	20160504	COMPAL	Reserve Erp lot6	Reserve PR2,PR5 ,PR7,PR10,PQ1	0.3(X02)
5	P51	PWR	20160504	COMPAL	PQ740 damage issue	Change PQ740 to SB00000SY00 (MDU1512R)	0.3(X02)
6	P51	PWR	20160504	COMPAL	EMI solution	Change to SE068102J80 (1000P) Location : PC780,PC781,PC100,PC131,PC115,PC133,PC230,PC231,PC694,PC691, PC692,PC693,PC1420,PC1421	0.3(X02)
7	P51	PWR	20160614	COMPAL	Change SOT23-6P to SOT23-3P	change PQ709 to SB00000ST00 (PQ709,PQ712)	1.0(A00)
8	P51	PWR	20160614	COMPAL	Add pull high resistance	Add PR781	1.0(A00)

Security Classification	Compal Secret Data		
Issued Date	2015/12/22	Deciphered Date	2017/01/31

Compal Electronics, Inc.			
Title: PWR_Change list			
Size	Document Number		Rev X00
Date: Tuesday, June 21, 2016	Sheet 61 of 61		