COMPAL CONFIDENTIAL

MODEL NAME : Goliad MLK 12 UMA ENTRY

PCB NO : LA-A972P

BOM P/N : 4319RK31LXX

GPIO MAP: 3.3b

Goliad MLK 12" UMA ENTRY

Broadwell U Processor

2013-12-23

REV : 0.2 (X01)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

VPRO@ : Vpro Component

NVPRO@ : Non-Vpro Component

Layout Dell logo

REV: X01
PWB: FGFC2
DATE: 1352-01

MB PCB

Part Number	Description
DA80002B000	PCB 14A LA-A972P REV0 MB W/O DOCKING 2

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Title: Cover Sheet

Size: | Document Number: LA-A972P | Rev: 0.1

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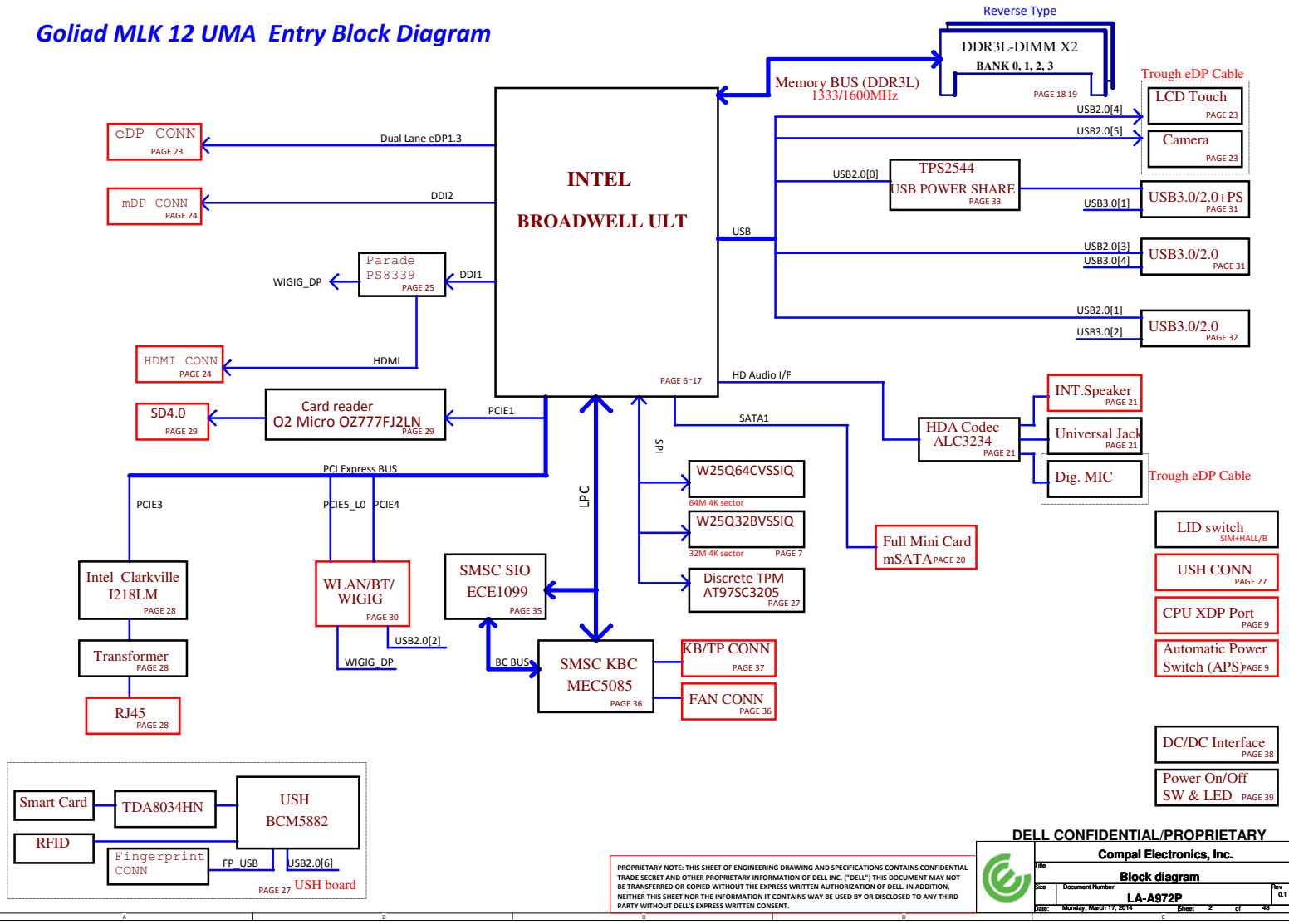
Goliad MLK 12 UMA Entry Block Diagram



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Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

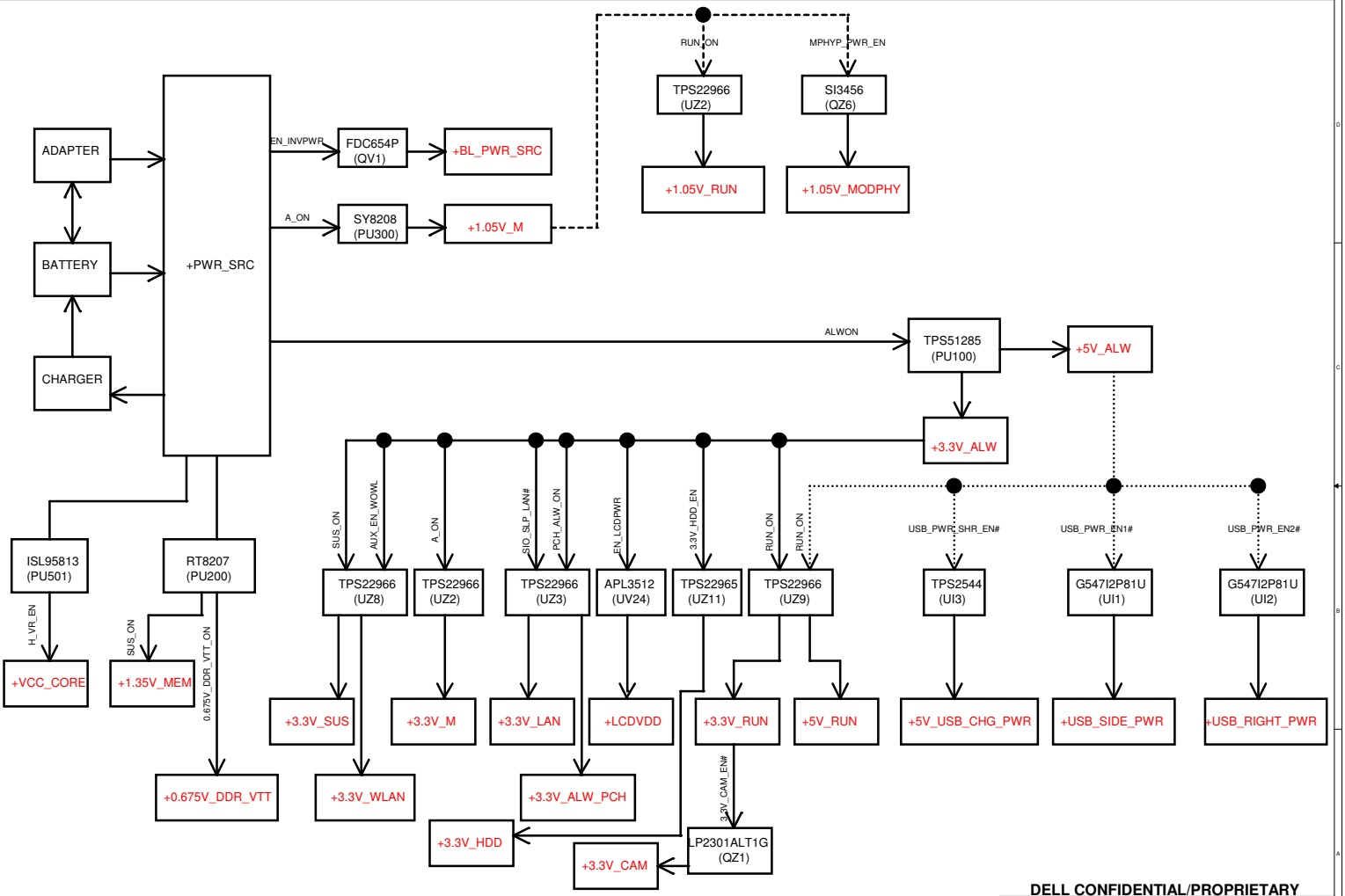
PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	NA
		SATA 2	NA
		SATA 1	JMINI3
		SATA 0	NA

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA



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Title: Power rails

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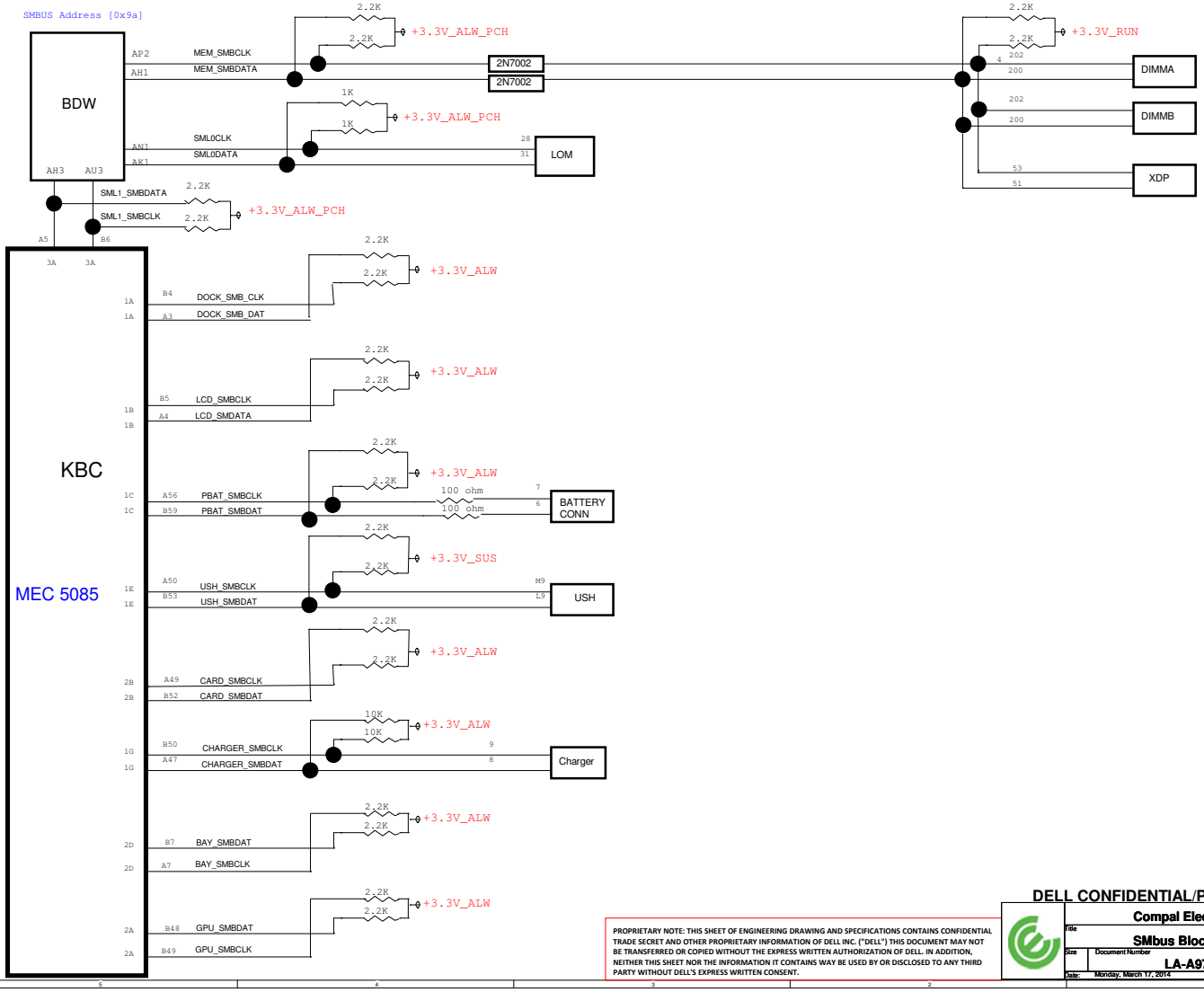

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Title: SMbus Block diagram

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UMA SATA port

SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G12 Entry	NA	NA	
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	G14U_En	NA	NA	

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FRT.

PT, ST pop RC2 & SW1; MP pop RC301.

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CMOS place near DIMM

HDA for Codec

Reserve for EMI

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

for DOCK

SATA HDD

for PCIe Cache (WWAN)

for SATA-CACHE (WWAN)

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Title: CPU (1/12)

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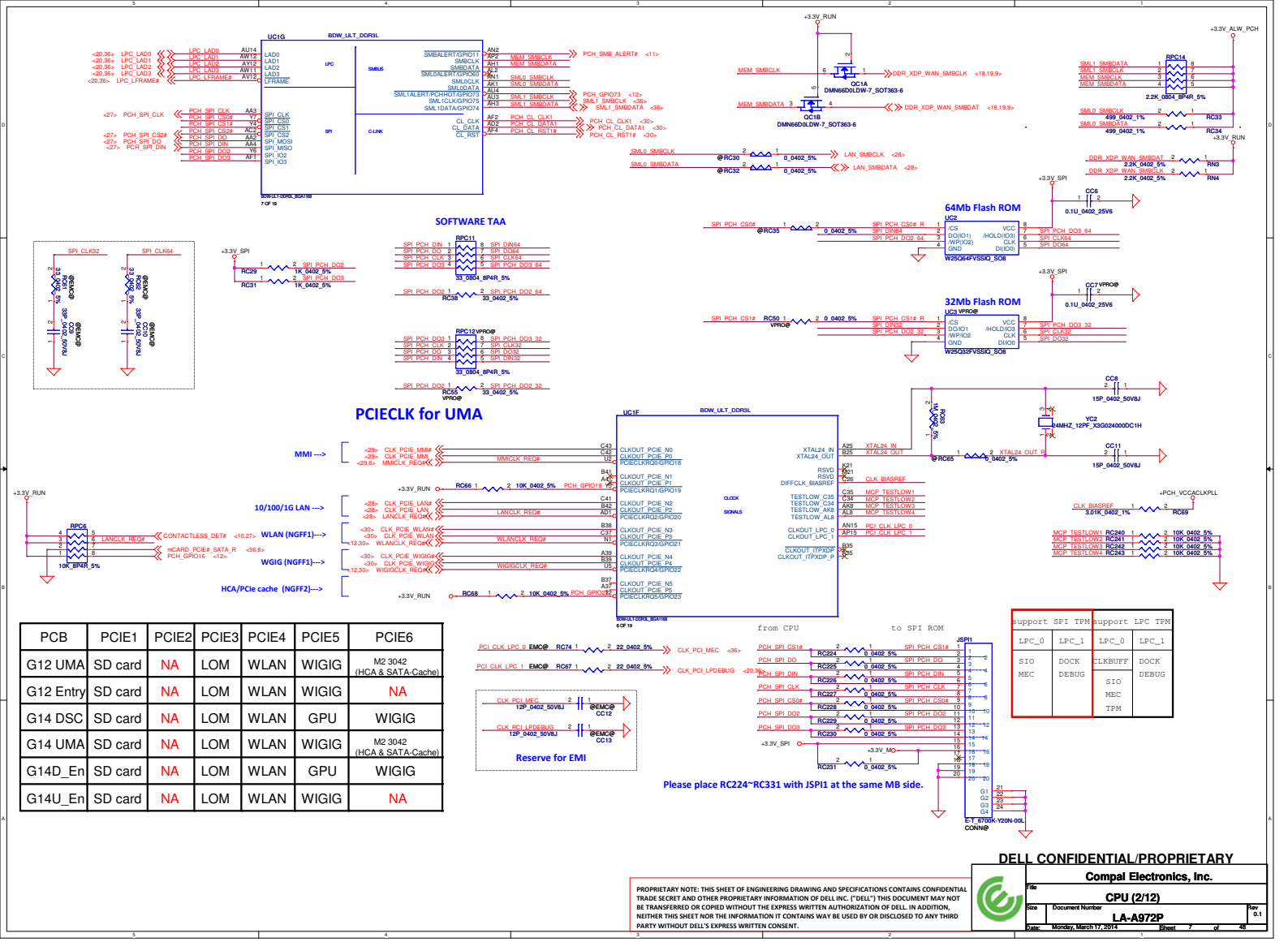

support SPI TPM		support LPC TPM	
LPC_0	LPC_1	LPC_0	LPC_1
SIO	DOCK	CLKBUFF	DOCK
MEC	DEBUG	SIO	DEBUG
		MEC	
		TPM	

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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Title: CPU (2/12)

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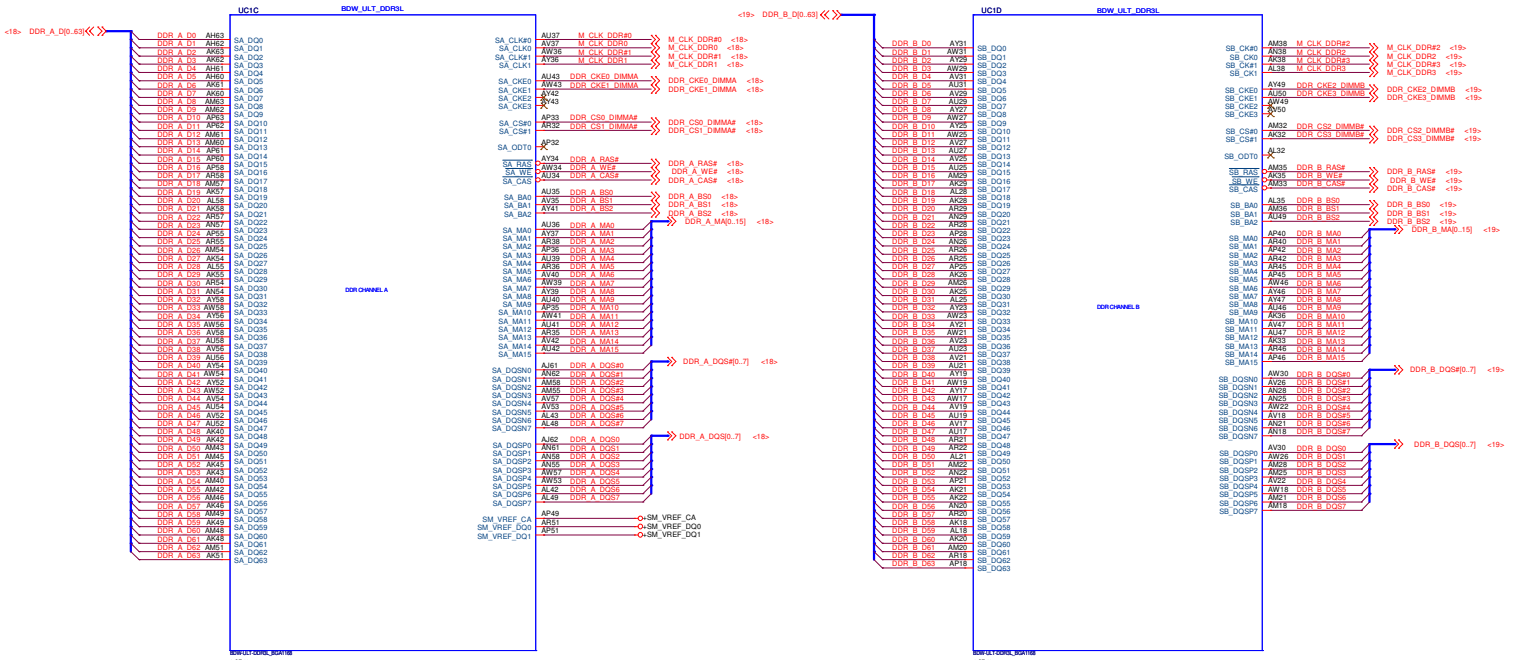

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Title	CPU (3/12)	
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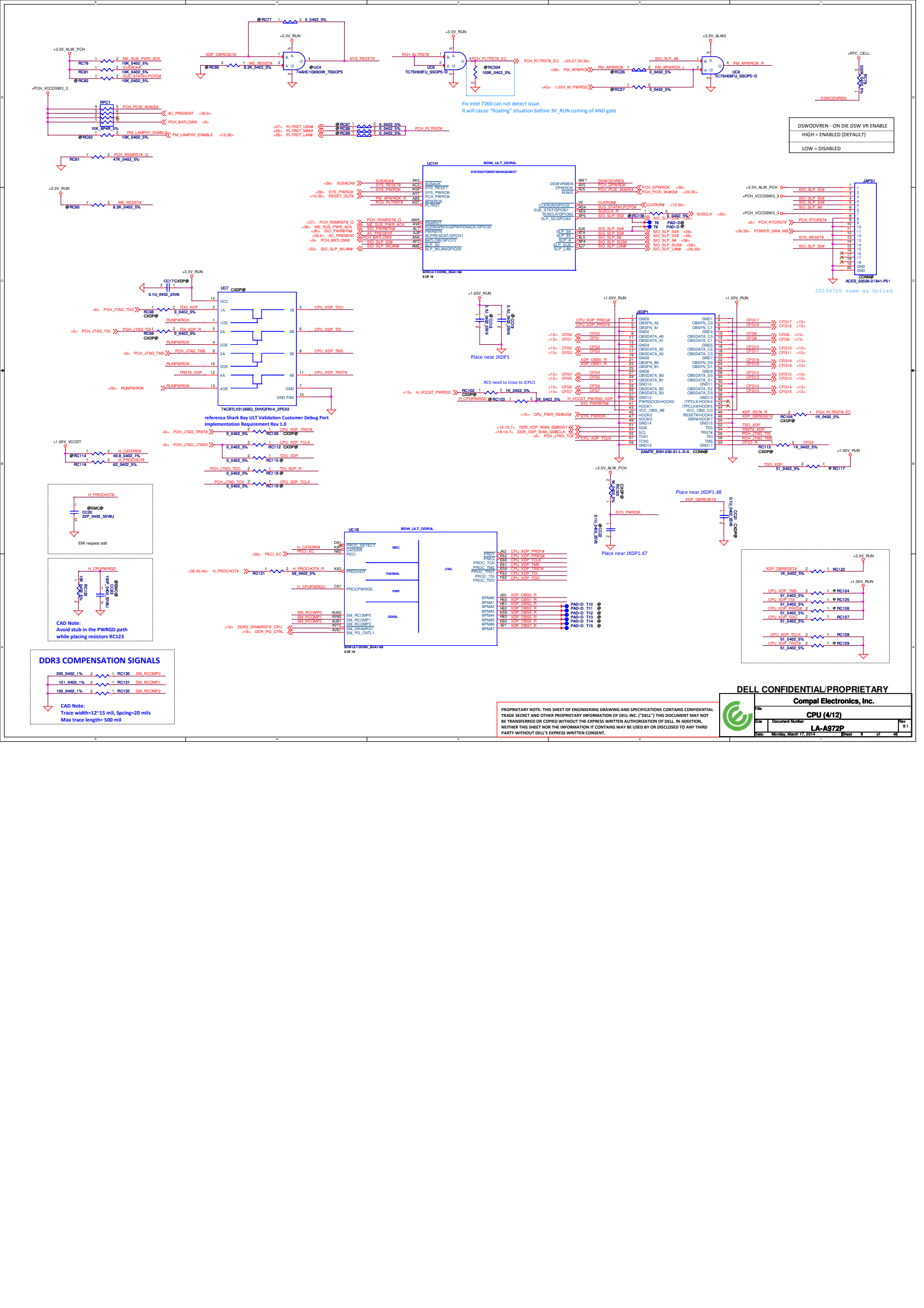
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
Fix Int 7260 can not detect issue.
It will cause "floating" situation before 3V_RUN coming of AND gate
Place near JXDP1
Place near JXDP1.48
Place near JXDP1.47
20130726 same as Goliad
reference Shark Bay ULT Validation Customer Debug Port
Implementation Requirement Rev 1.0
RCS need to close to JCPU1
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC123
DDR3 COMPENSATION SIGNALS
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil
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CPU (4/12)
LA-A972P
Monday, March 17, 2014
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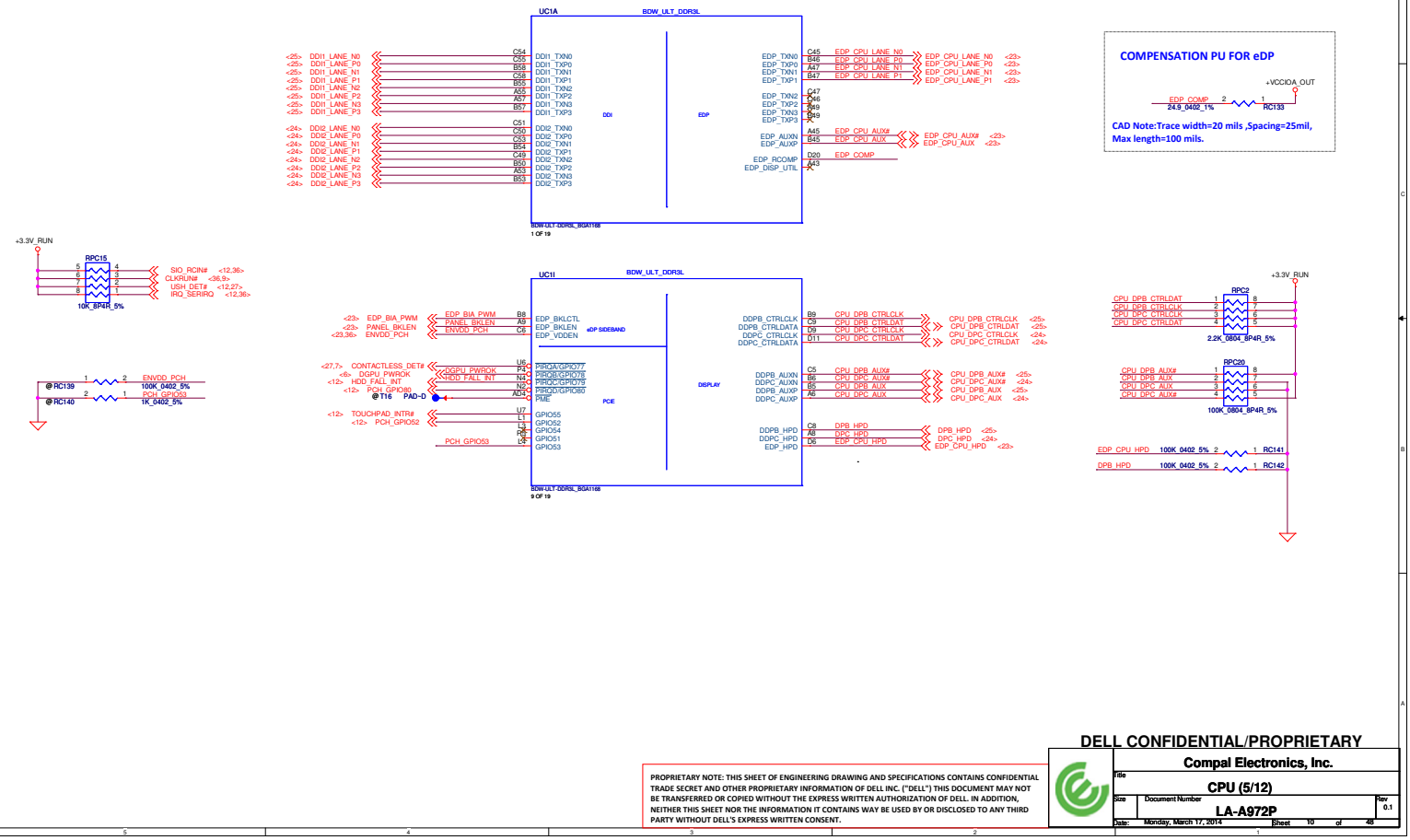

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Title: CPU (5/12)		
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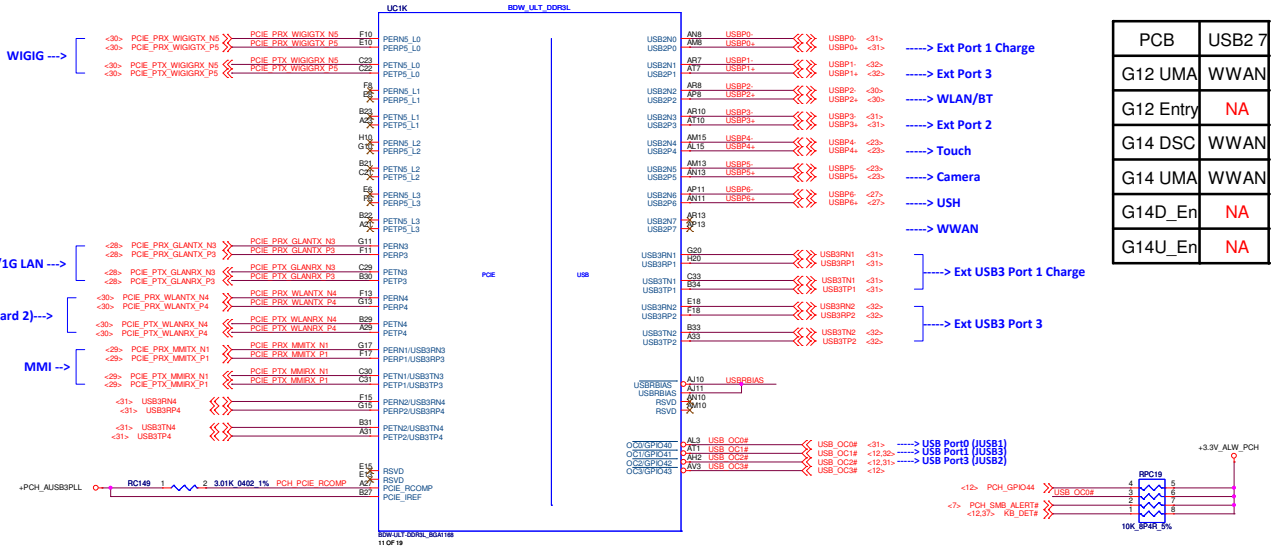
PCIE for UMA



PCB	USB2 7
G12 UMA	WWAN
G12 Entry	NA
G14 DSC	WWAN
G14 UMA	WWAN
G14D_En	NA
G14U_En	NA

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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Title: CPU (6/12)

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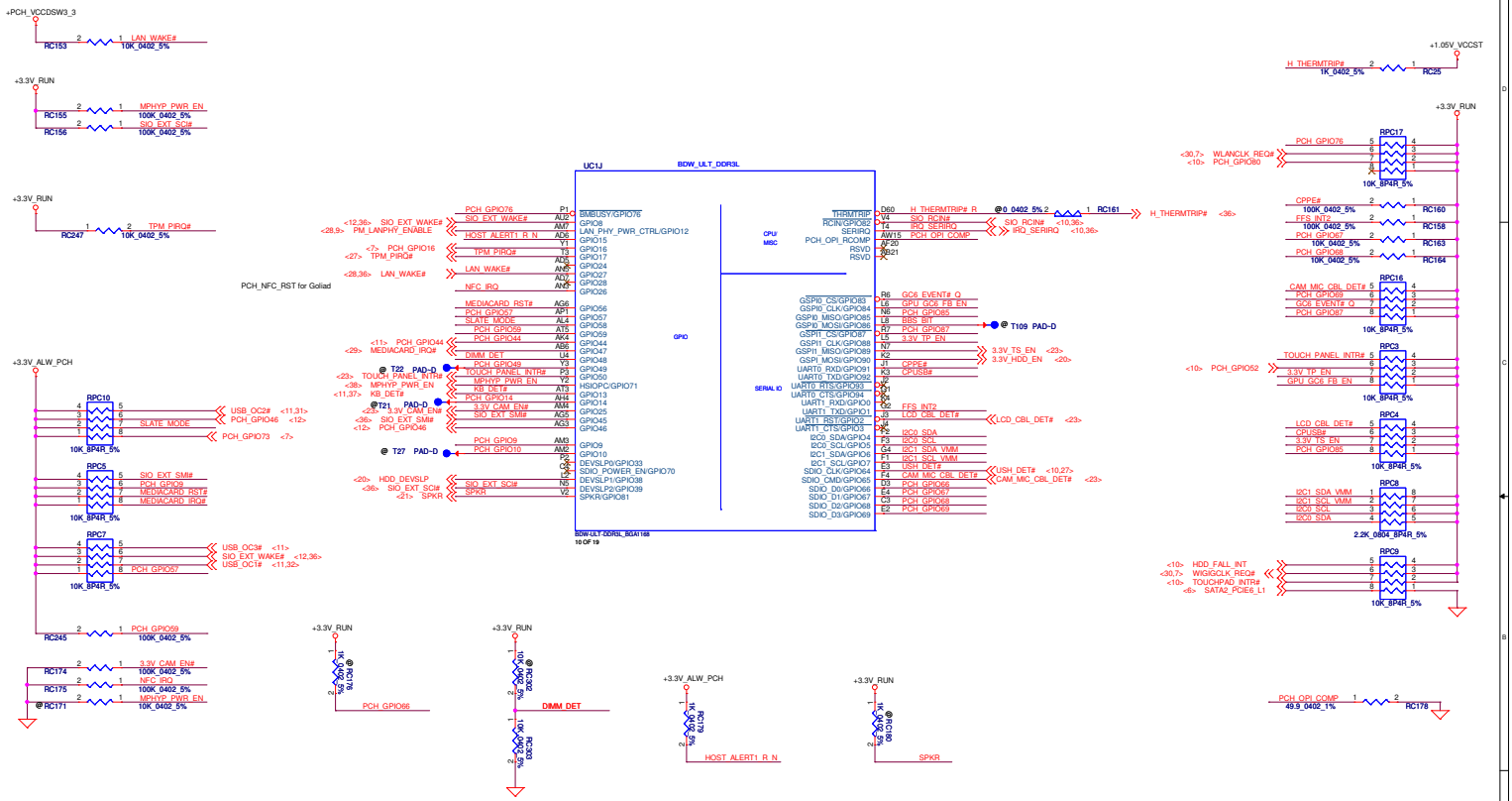

TOP-BLOCK SWAP OVERRIDE	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

No Reboot on TCO Timer expiration	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

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Title	CPU (7/12)	
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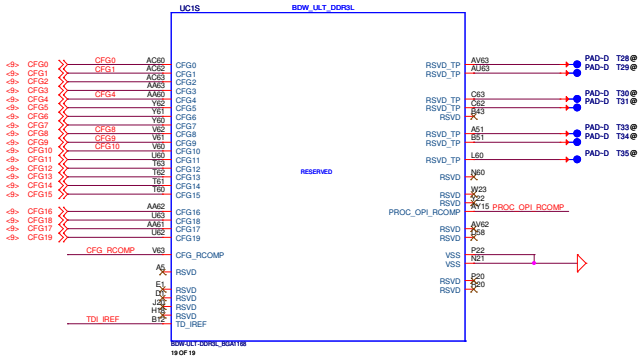
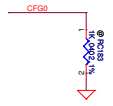
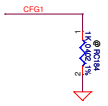
CFG STRAPS for CPU

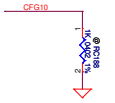


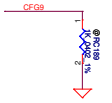


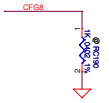
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

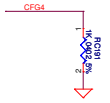


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: CPU (8/12)

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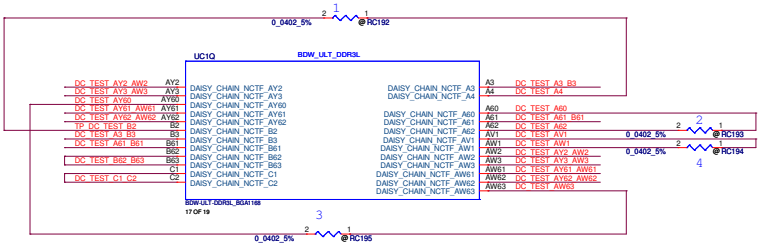


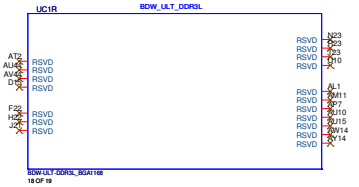
Package Daisy Chain:

1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4

2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60

3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63

4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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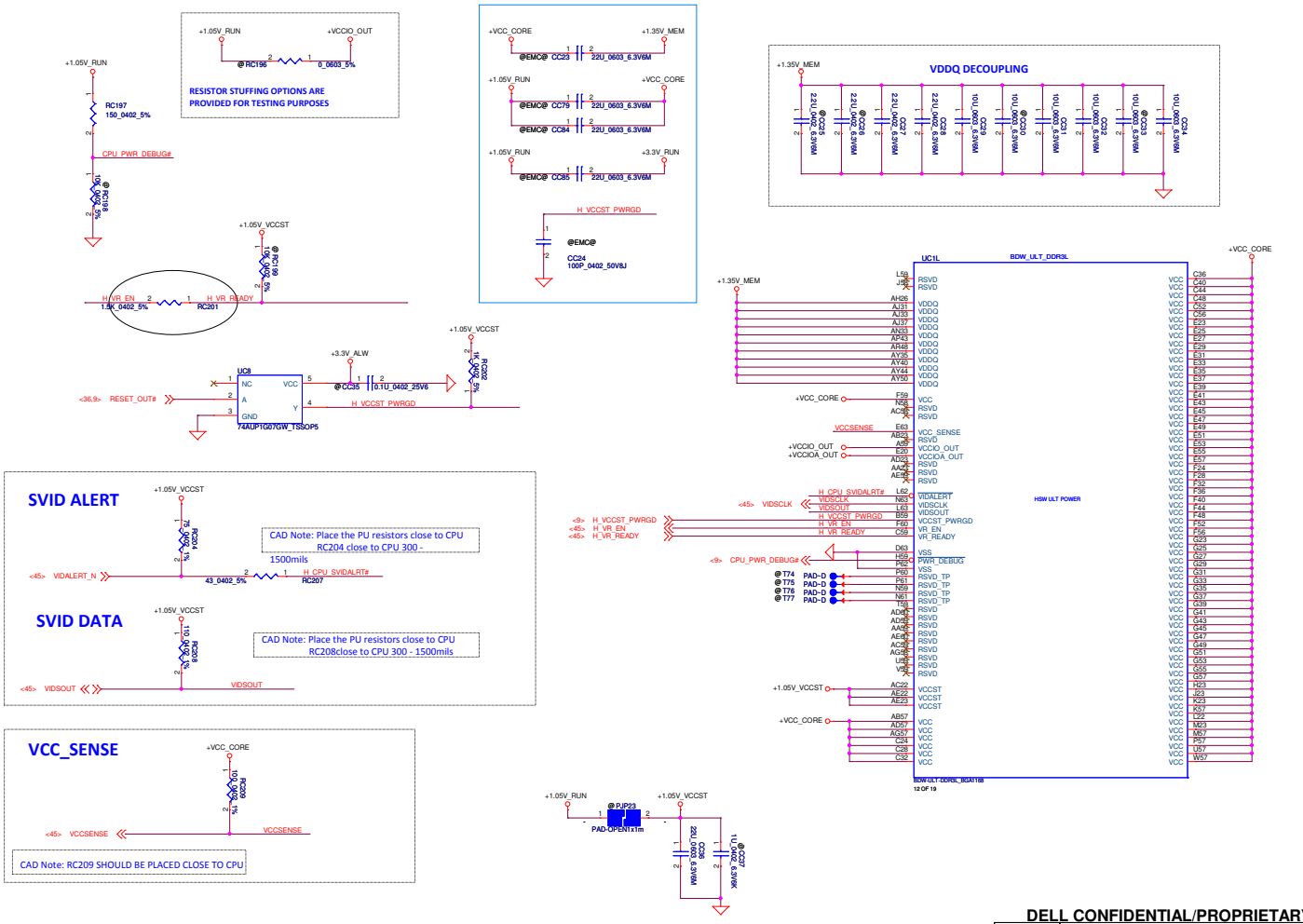
ESD Request



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Title: CPU (10/12)

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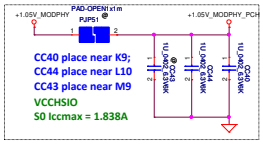

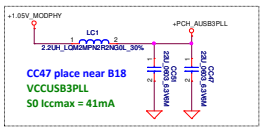

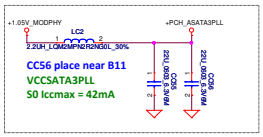

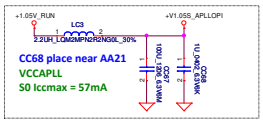

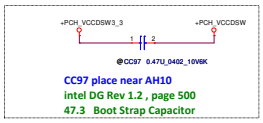

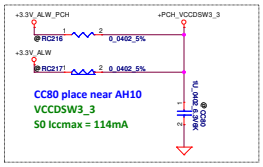

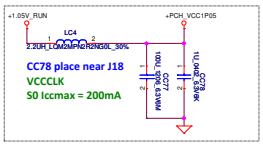

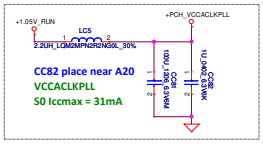

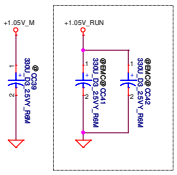

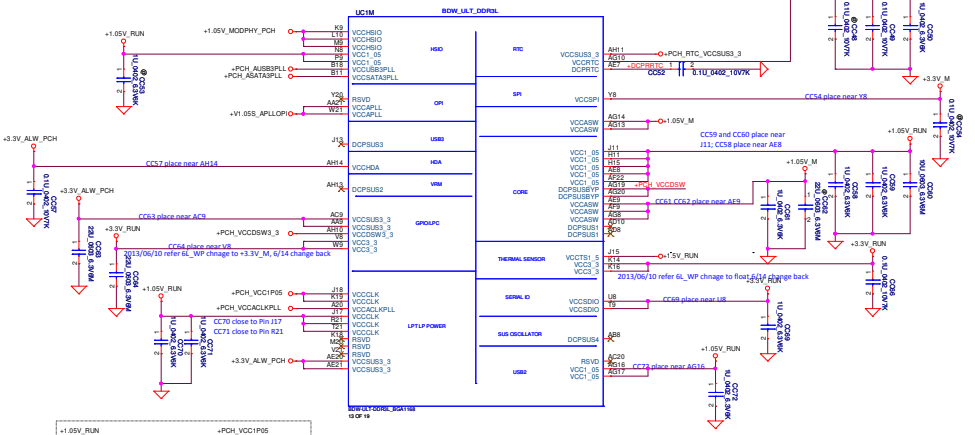

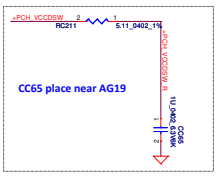

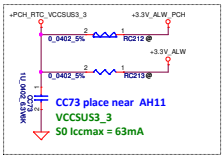

Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	< 1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DcpSus2[4]	1.05	0.025	0.001	0	0
DcpSus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Power Rail Isolation

Voltage Supply	Interface: (power rail isolation required)	PCH Pins sharing power rail
V1.05S	Core	J11, H11, H15, AE8, AF22
	OPI	AA21, W21
	HSIO	K9, L10, N8, P9, B18, B11, M9
	USB2	AG16, AG17
	CLK(PLL	A20
	CLK(A)	R21, T21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3A	GPIO	AC9, AA9, AE20, AE21
	RTC	AH11
	HDA	AH14
V3.3S	GPIO	V8, W9
	SDIO	U8, T9
	Thermal Sensor	K14, K16

Compal Electronics, Inc.

Title: CPU (11/12)

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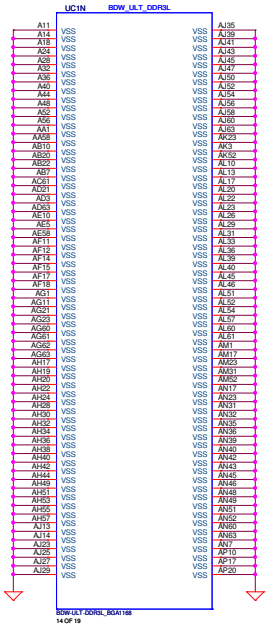

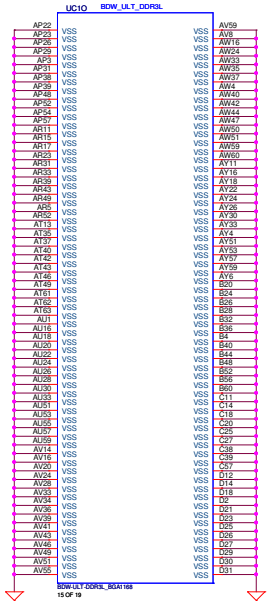

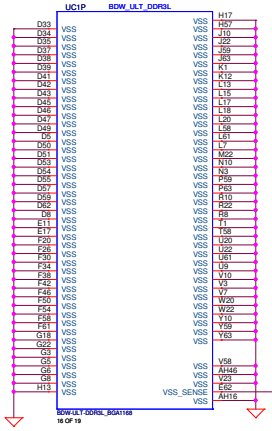

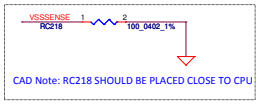

Compal Electronics, Inc.		
Title: CPU (12/12)		
Size	Document Number: LA-A972P	Rev: 0.1
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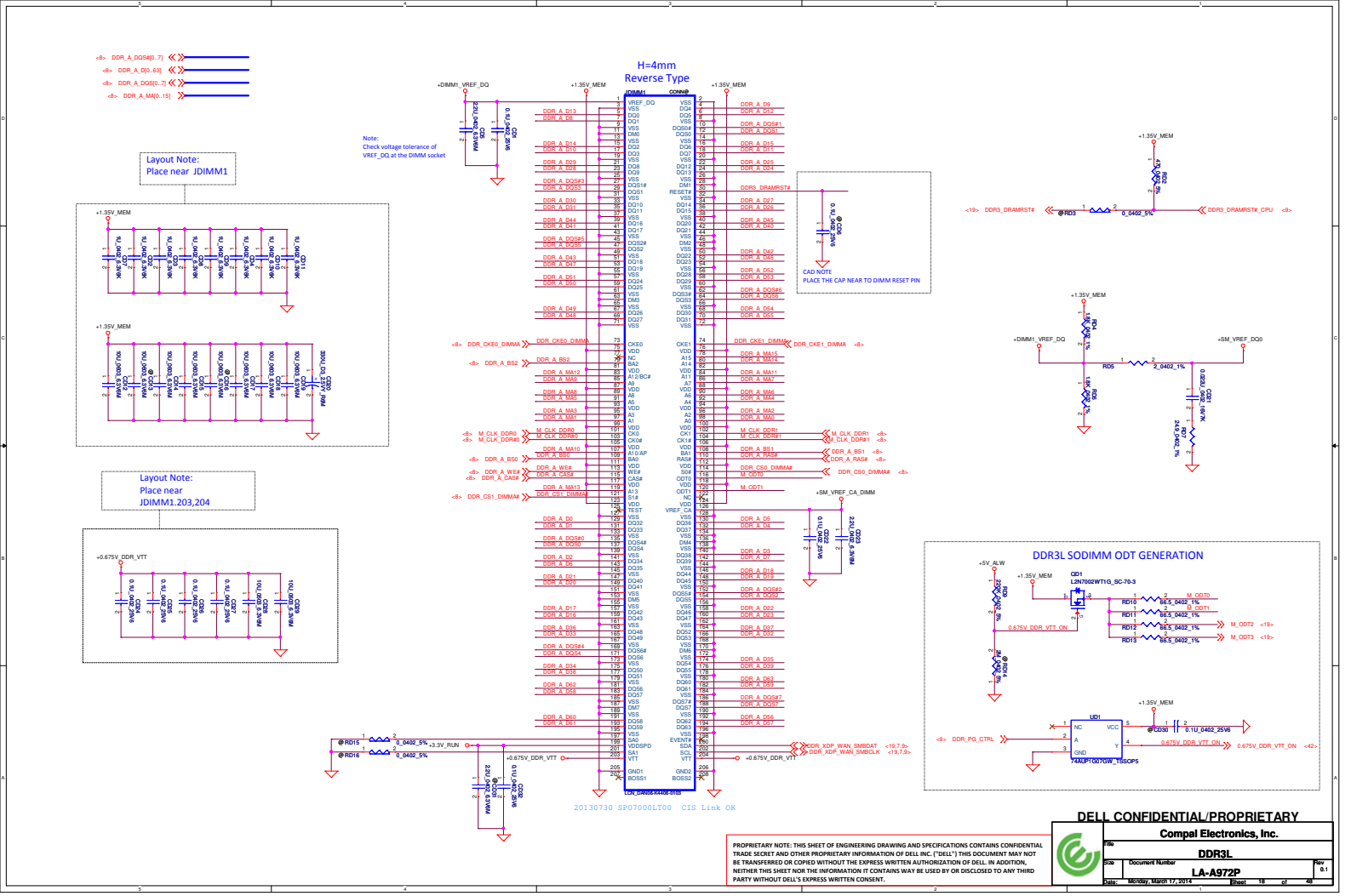

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Title: DDR3L		
Size:	Document Number: LA-A972P	Rev: 0.1
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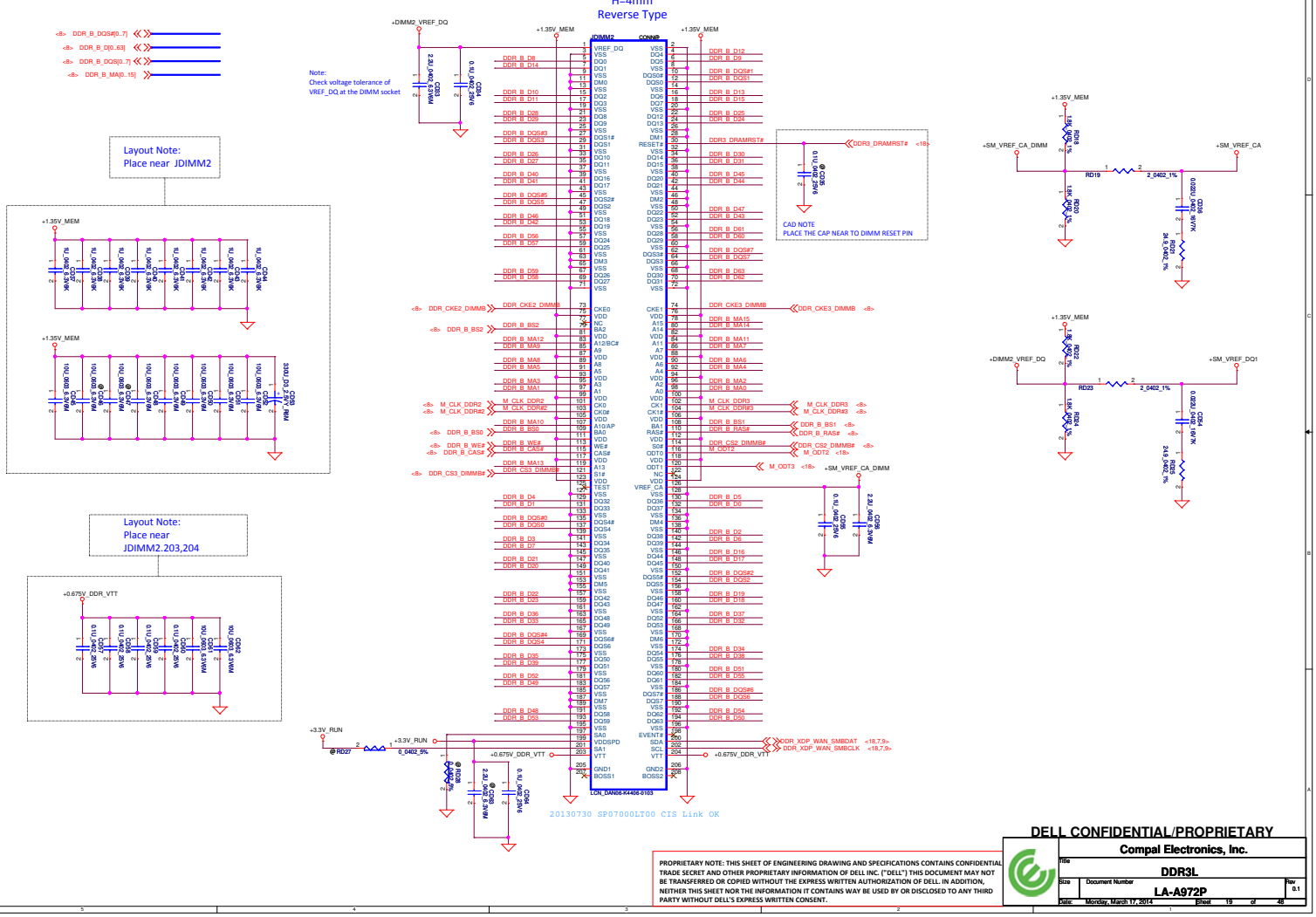

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Title: DDR3L

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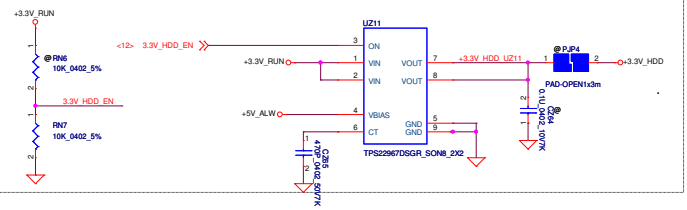
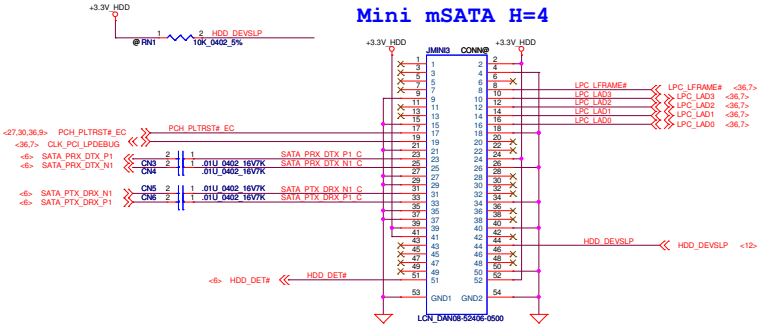
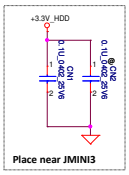
+3.3V_HDD source



Mini mSATA H=4





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Title	HDD CONN	
Size	Document Number: LA-A972P	Rev: 0.1
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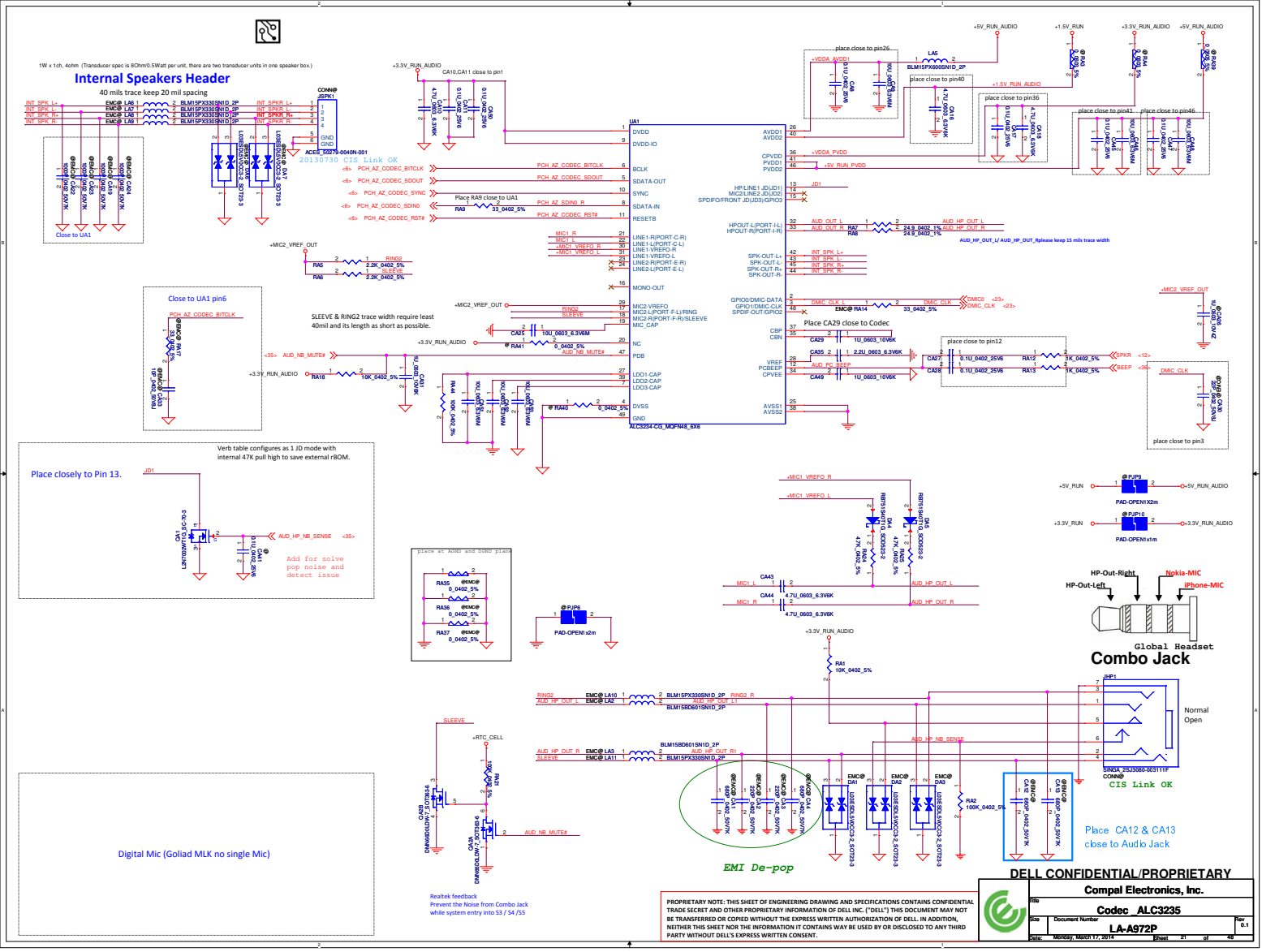

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Compal Electronics, Inc.		
Title: DP 1.2 MST HUB		
Size	Document Number: LA-A972P	Rev: 0.1
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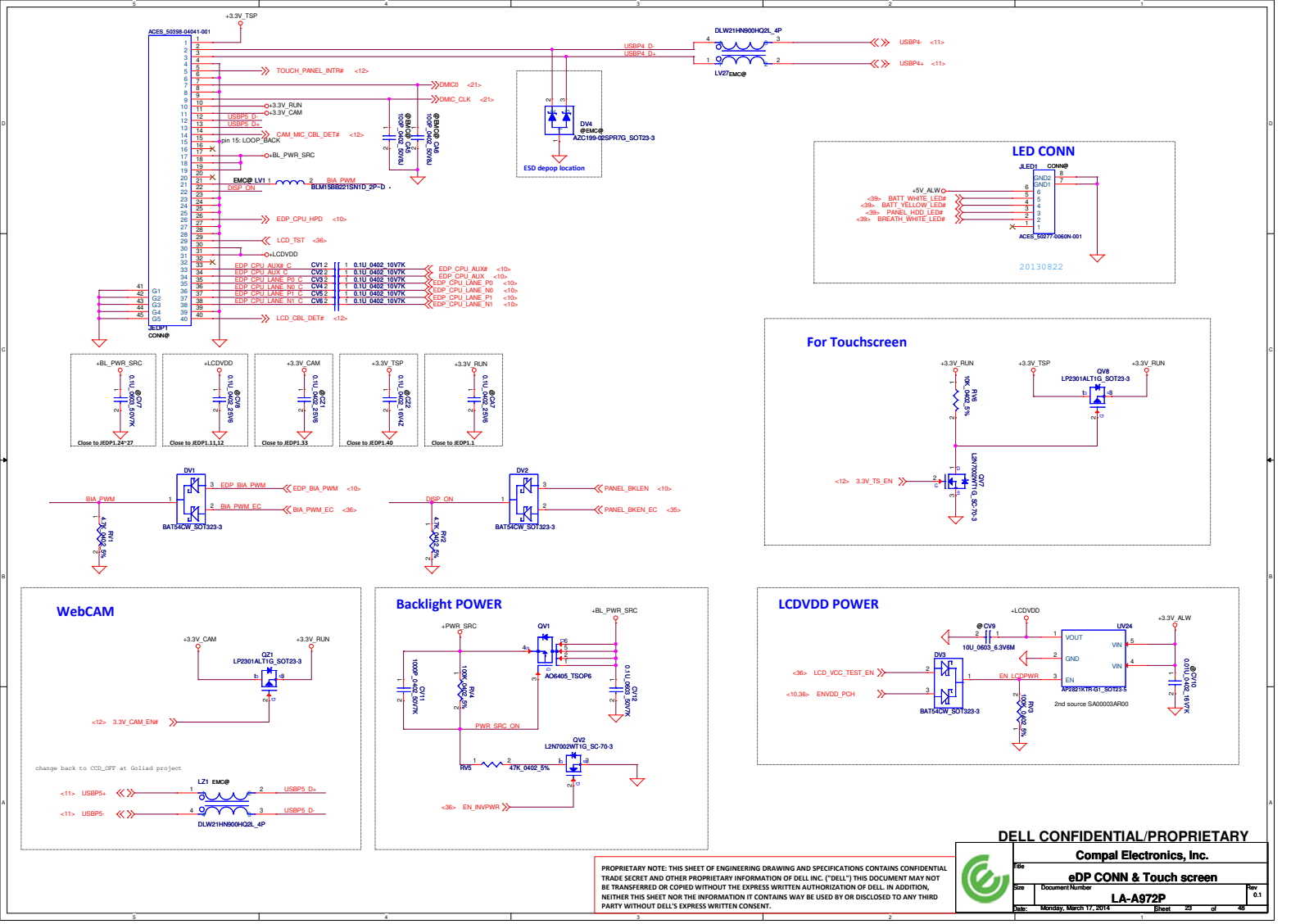

Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size: Document Number: LA-A972P

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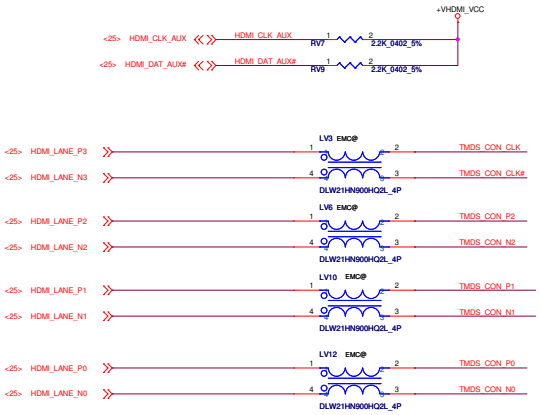
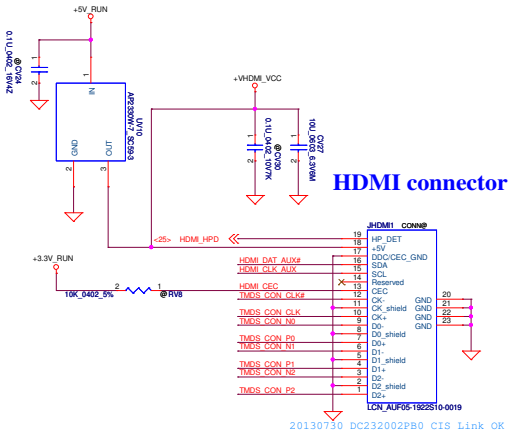
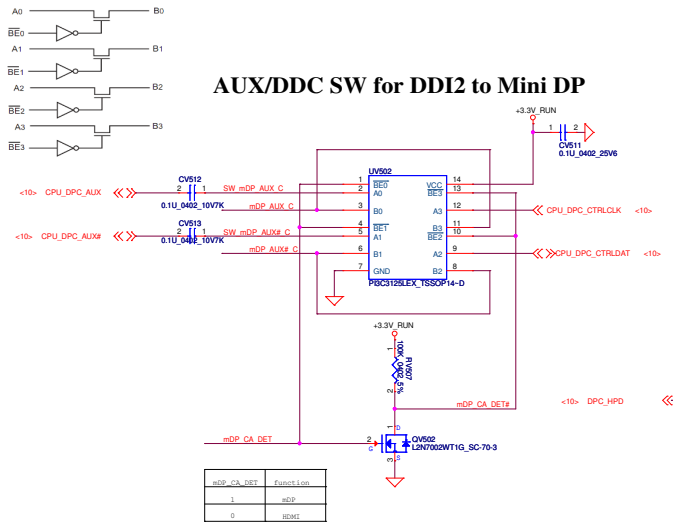




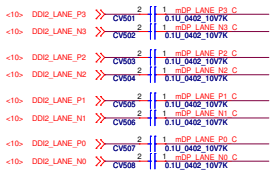
HDMI connector

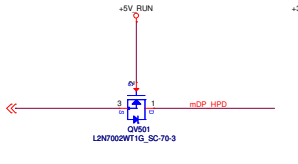
20130730 DC232002PB0 CIS Link OK

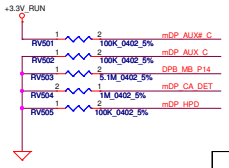
AUX/DDC SW for DDI2 to Mini DP

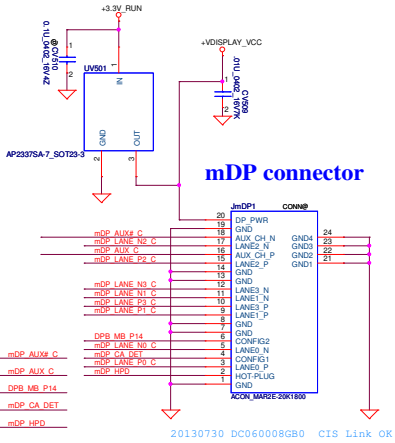


mDP_CA_DET	function
1	mDP
0	HDMI









mDP connector

20130730 DC060008GB0 CIS Link OK

Compal Electronics, Inc.

Title: HDMI CONN

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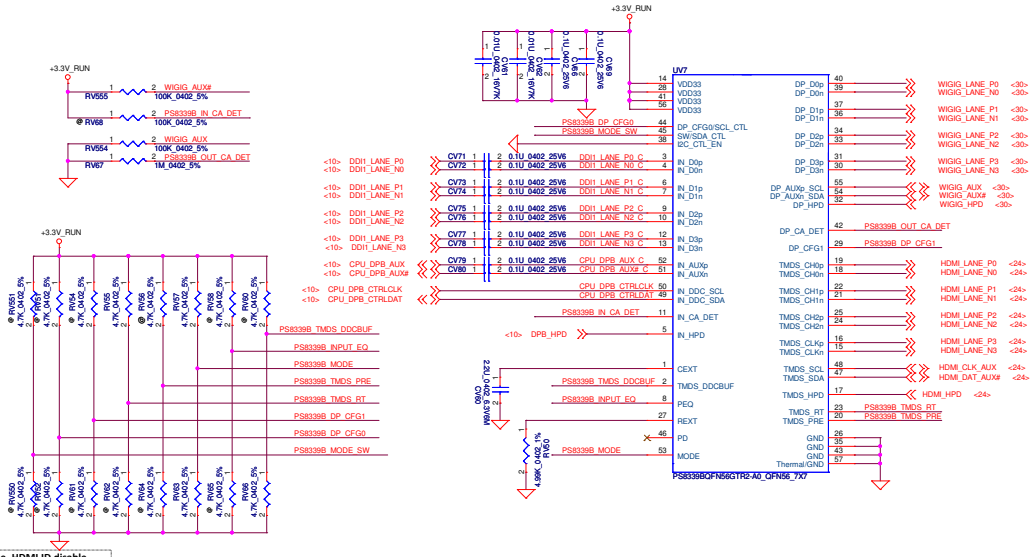
PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable

TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors

TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable

DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

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Title: DP SW

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Title: DP to VGA & VGA Conn		
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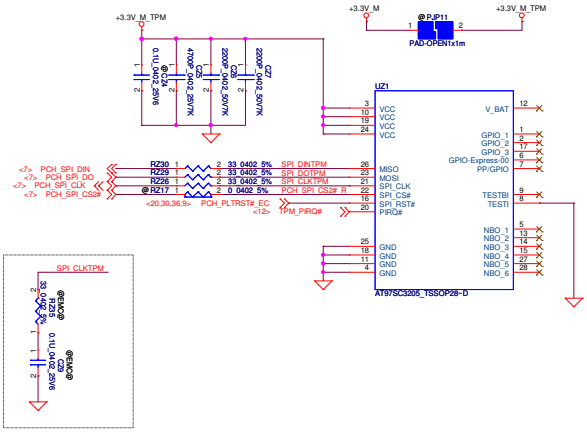

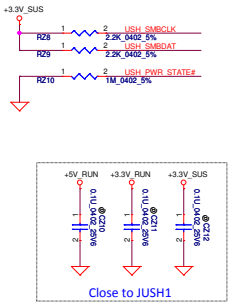

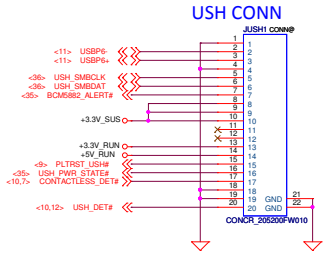

Compal Electronics, Inc.

Title: USH & TPM

Size: | Document Number: LA-A972P | Rev: 0.1

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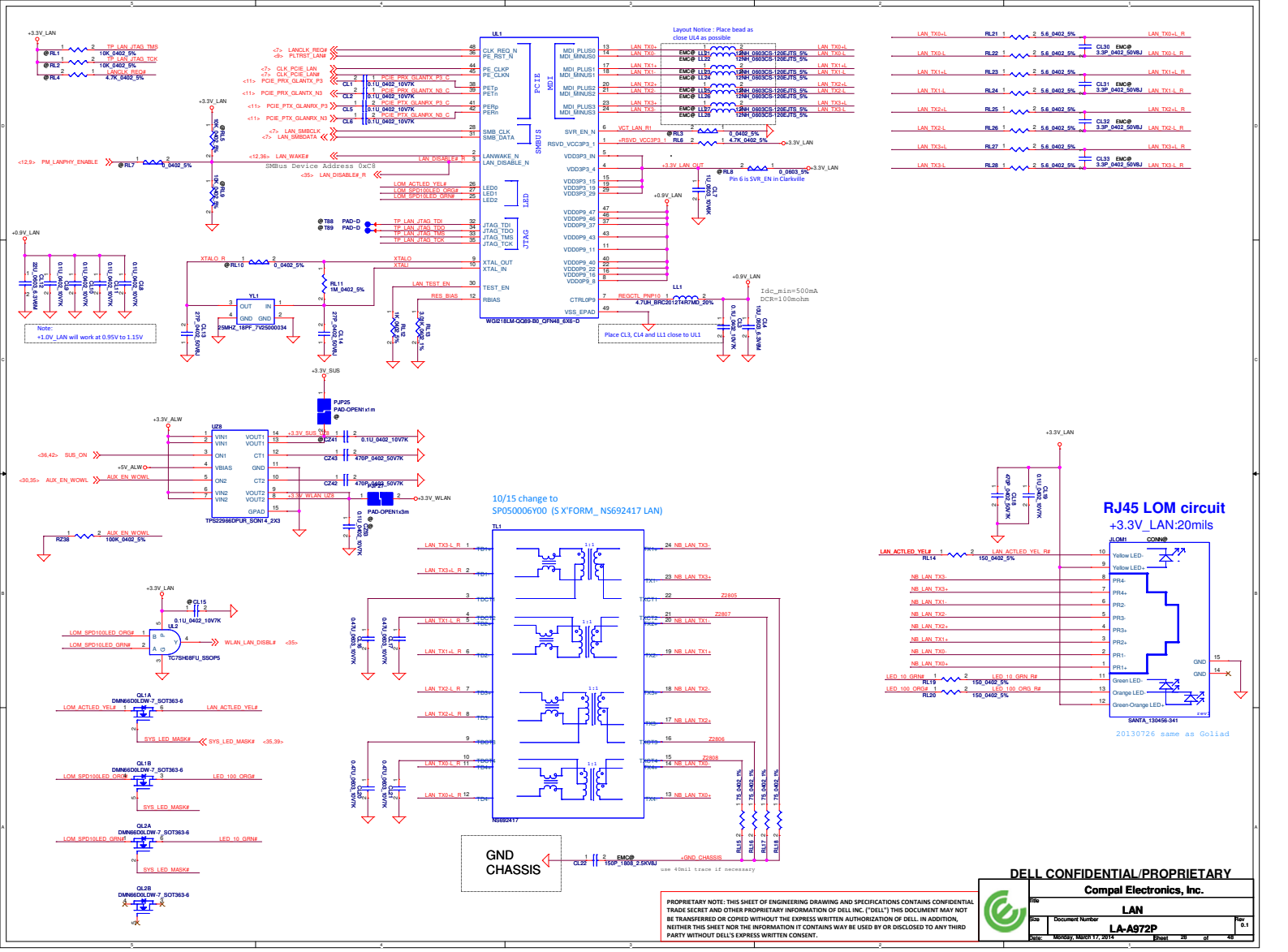

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Title: LAN			
Size	Document Number		Rev
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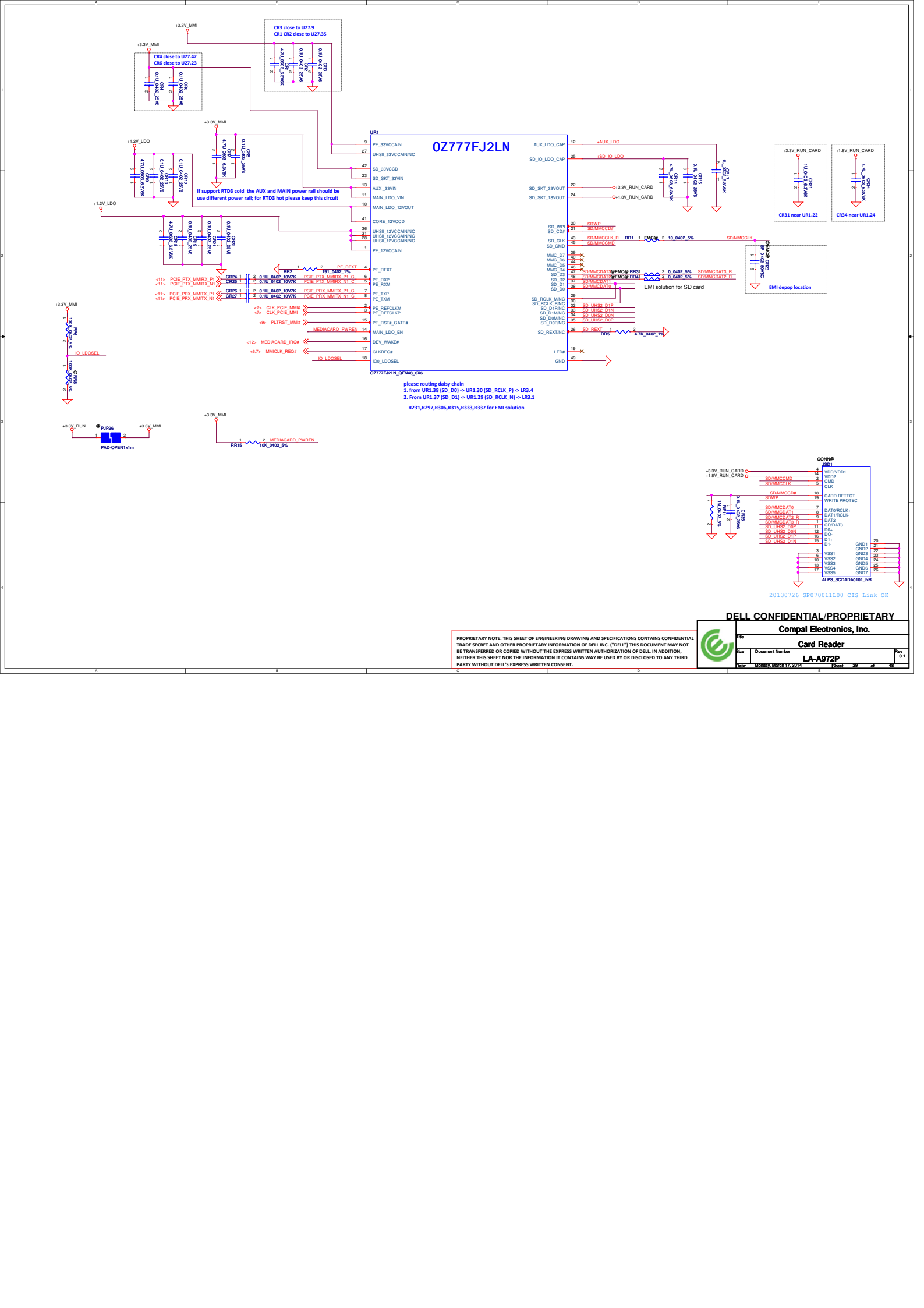

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Title	Card Reader
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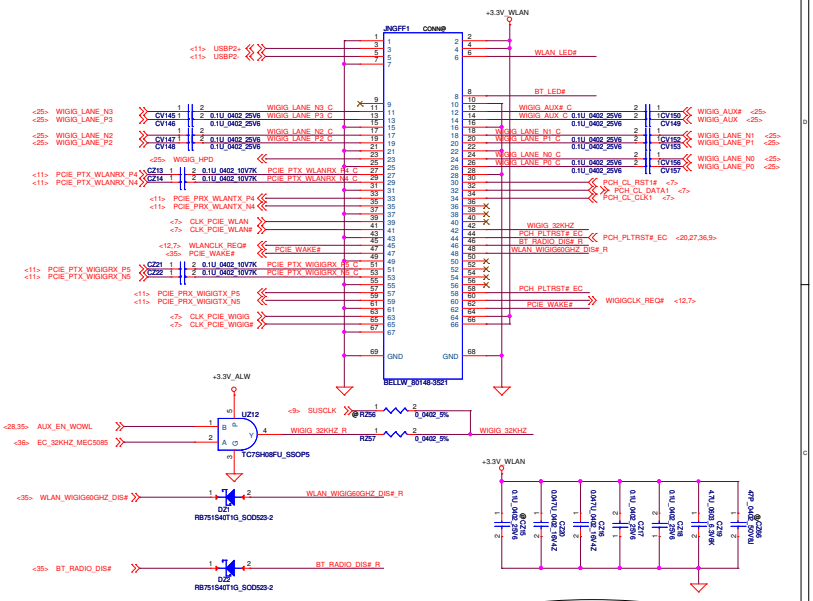
NGFF for UMA

NGFF slot A Key A

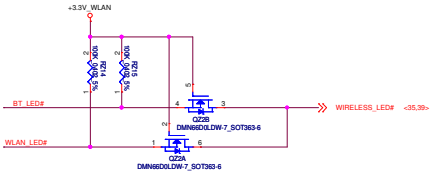


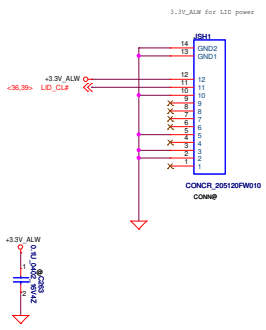
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

LED control circuit





Compal Electronics, Inc.

Title: NGFF Card

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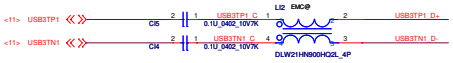
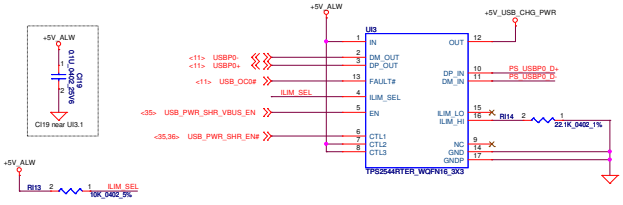
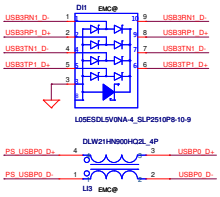
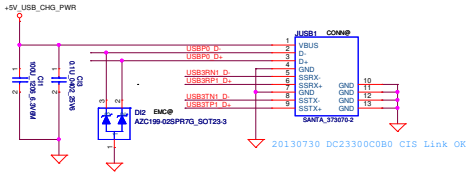
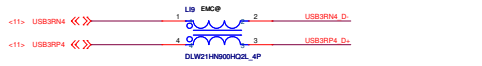


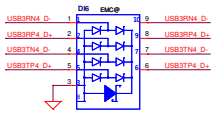


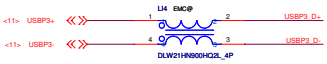


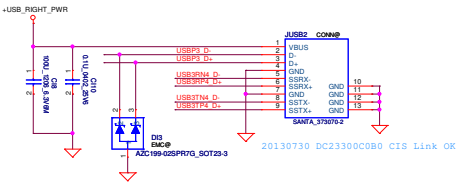


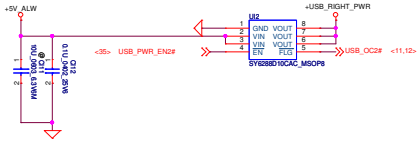
PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA











Compal Electronics, Inc.

Title: USB3.0

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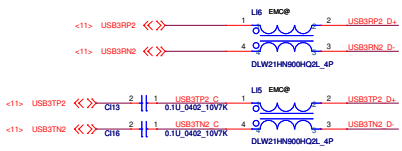

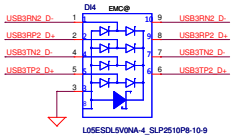

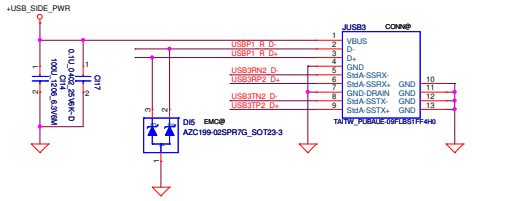

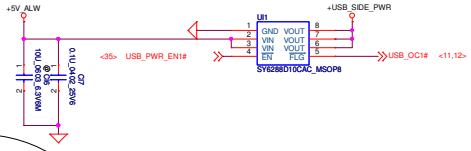

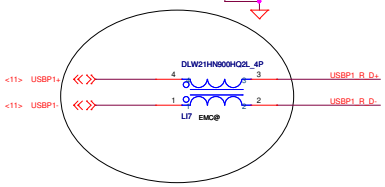

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Compal Electronics, Inc.		
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NFC on USH/B

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Compal Electronics, Inc.

Title: E-Dock

Size | Document Number: LA-A972P | Rev: 0.1

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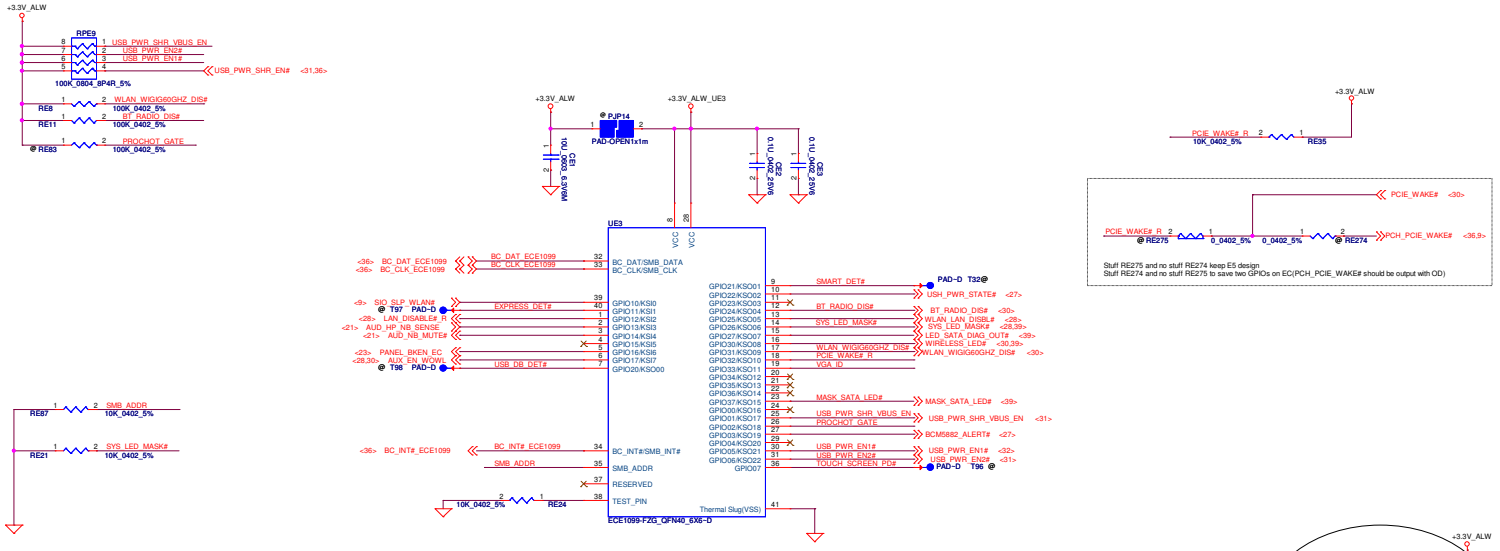
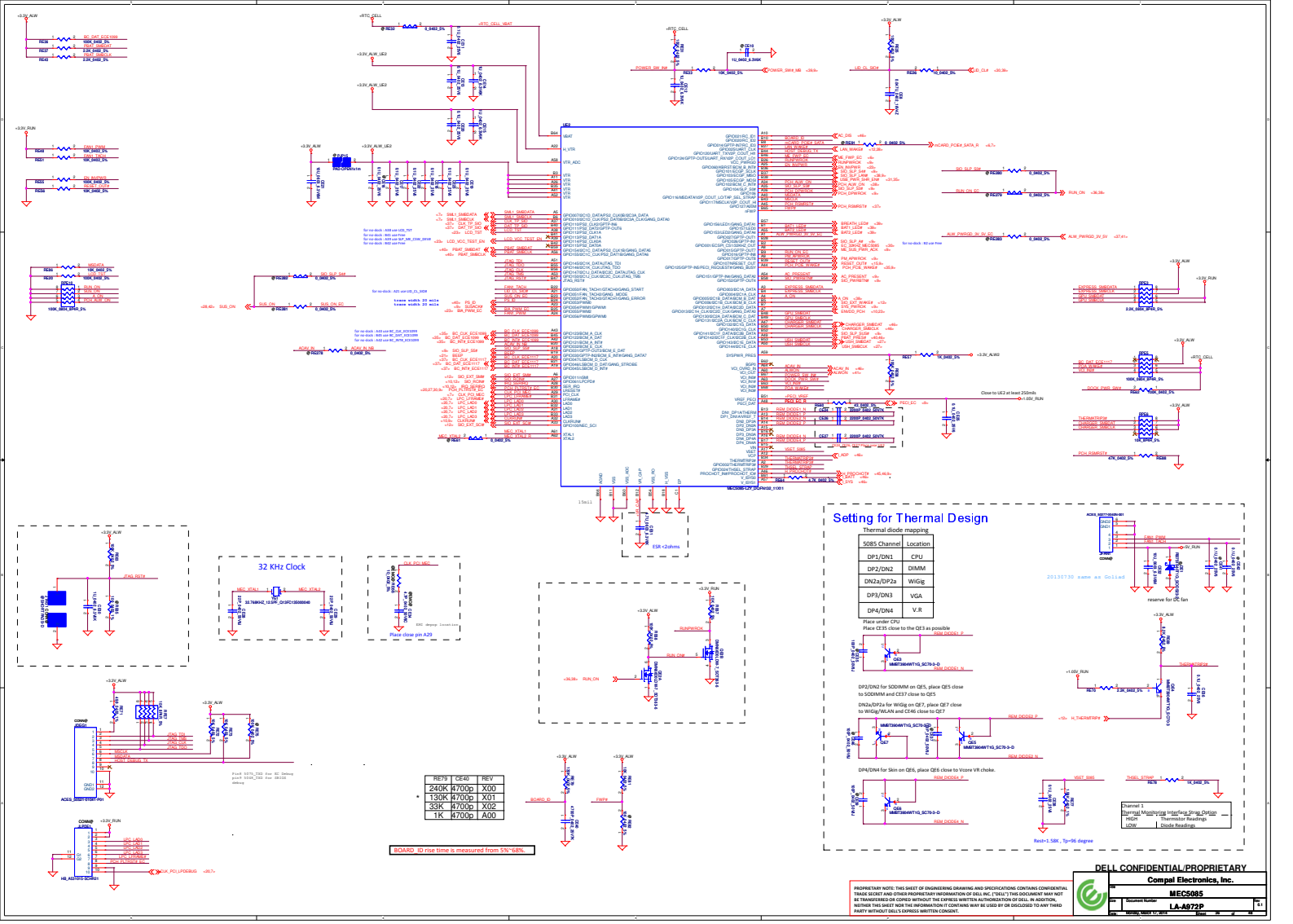


Compal Electronics, Inc.

Title: ECE5048

Size: Document Number: LA-A972P Rev: 0.1

Date: Monday, March 17, 2014 Sheet 35 of 47



Setting for Thermal Design

Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DN2a/DP2a	WiGig
DP3/DN3	VGA
DP4/DN4	V.R

Place under CPU
Place C35 close to the QE3 as possible

DP2/DN2 for SDDIMM on QE5, place QE5 close to SDDIMM and CE37 close to QE5

DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig/WLAN and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

Channel 1
Thermal Monitoring Interface Smsg Option

Thermistor Readings	
HIGH	Diode Readings
LOW	

Rest=1.58K , Tp=96 degree

32 KHz Clock

RE'9	CE46	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
1K	4700p	A00

BOARD_ID rise time is measured from 5%~68%

Compal Electronics, Inc.

Size	Document Number	Rev
	MEC5085	0.1
	LA-A972P	
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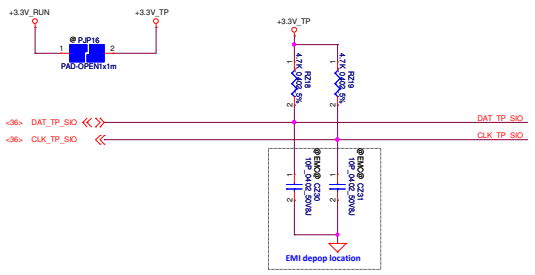
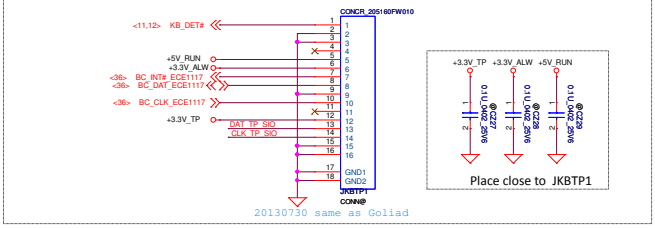
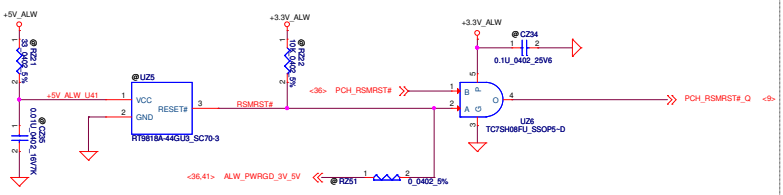
Touch Pad



Keyboard



RSMRST circuit



@eDP Cable

Part Number	Description
DC02C007P00	H-CONN SET 14A MB-EDP-LED-CAMERA

@eDP TS Cable

Part Number	Description
DC02C007Q00	H-CONN SET 14A MB-EDP-LED-CAMERA-TS

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HR3 ADDA

@USH Board FFC

Part Number	Description
NBX0001KE00	FFC 26P G P0.5 PAD=0.3 47MM MB-USH

@KBTP FFC

Part Number	Description
NBX0001KD00	FFC 16P G P0.5 PAD=0.3 82MM MB-KBTP

@NFC Board FFC

Part Number	Description
NBX0001RC00	FFC 15P F P0.5 PAD=0.3 40.5MM MB-NFC

@FP FFC

Part Number	Description
NBX0001KB00	FFC 8P F P0.5 PAD=0.3 22.5MM MB-FP

@SIM+Hall/B FFC

Part Number	Description
NBX0001CR00	FFC 12P G P0.5 PAD=0.3 73.3MM MB-SIM+HALL_B

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

Compal Electronics, Inc.

Title: Keyboard

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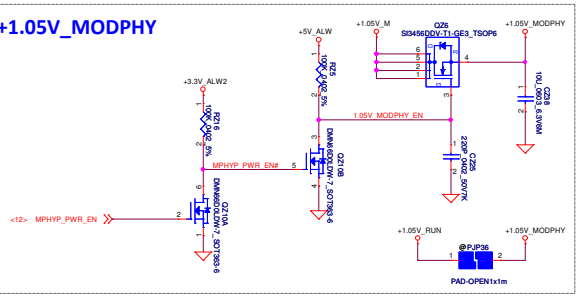
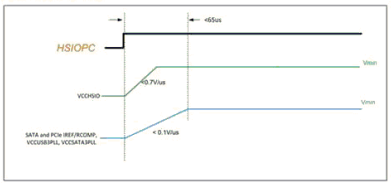
+1.05V_MODPHY

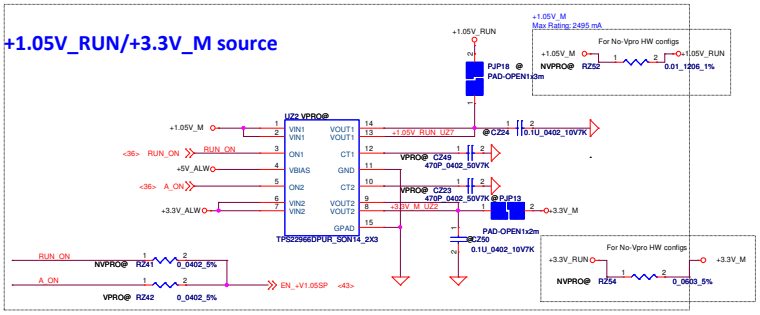


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

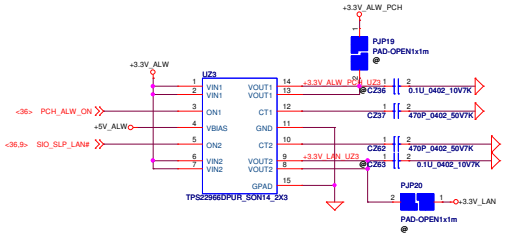
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



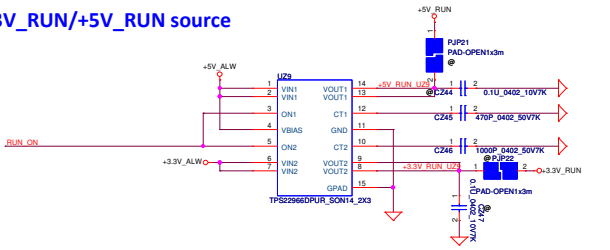
+1.05V_RUN/+3.3V_M source



+3.3V_ALW_PCH/+3.3V_LAN source

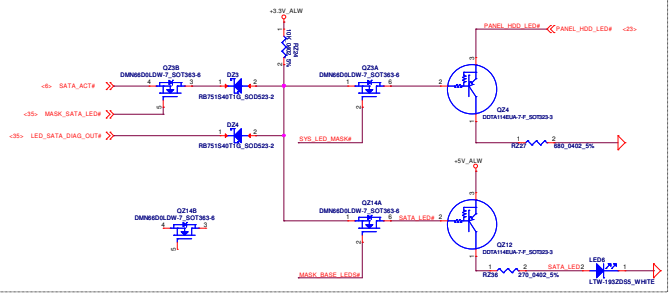


+3.3V_RUN/+5V_RUN source

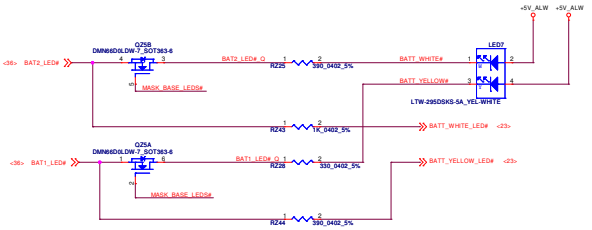


Compal Electronics, Inc.		
Title: Power control		
Size	Document Number: LA-A972P	Rev: 0.1
Date: Monday, March 17, 2014	Sheet 38 of 48	

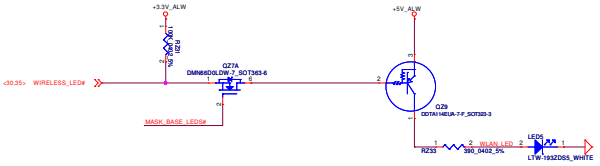
HDD LED solution for White LED



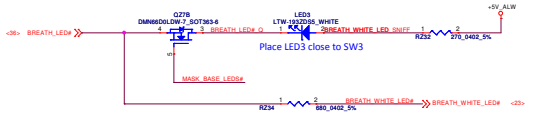
Battery LED

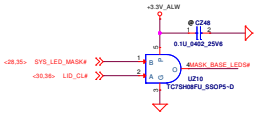


WLAN LED solution for White LED

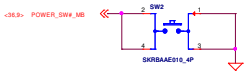


Breath LED





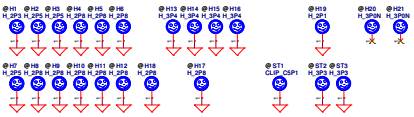
POWER & INSTANT ON SWITCH



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

FD1 FIDUCIAL MARK~D
FD2 FIDUCIAL MARK~D
FD3 FIDUCIAL MARK~D
FD4 FIDUCIAL MARK~D



Compal Electronics, Inc.

Title: PAD, LED

Size | Document Number: LA-A972P | Rev: 0.1

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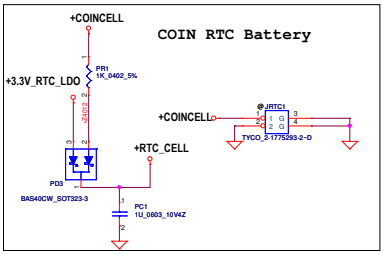

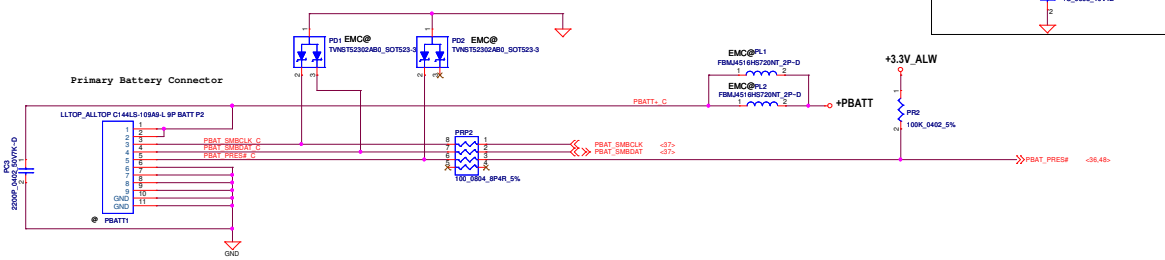

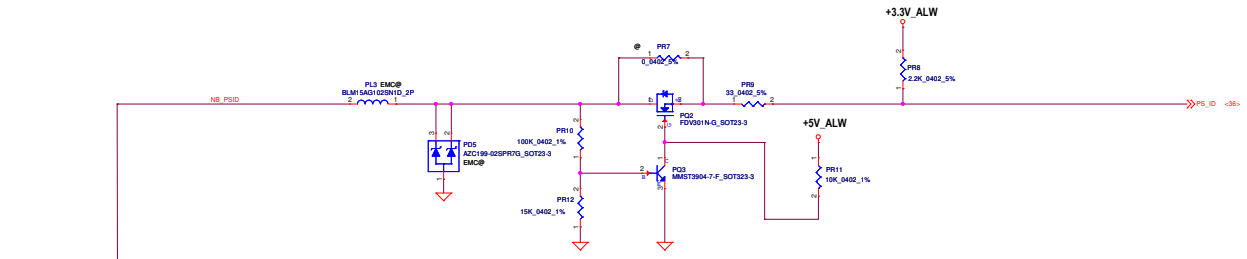

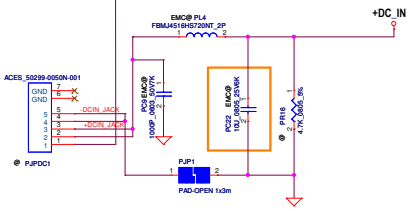

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-A902P	Rev: 0.1
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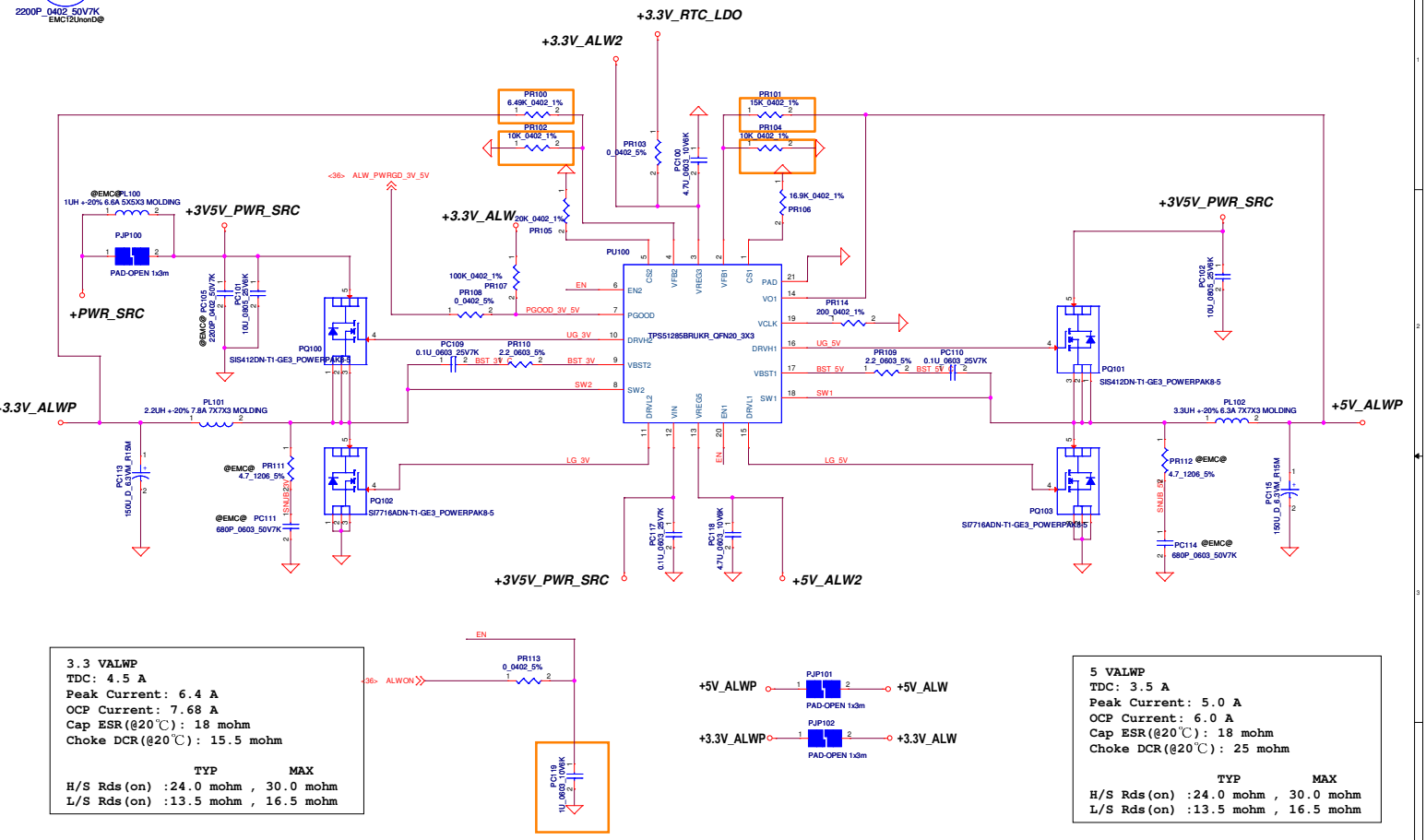


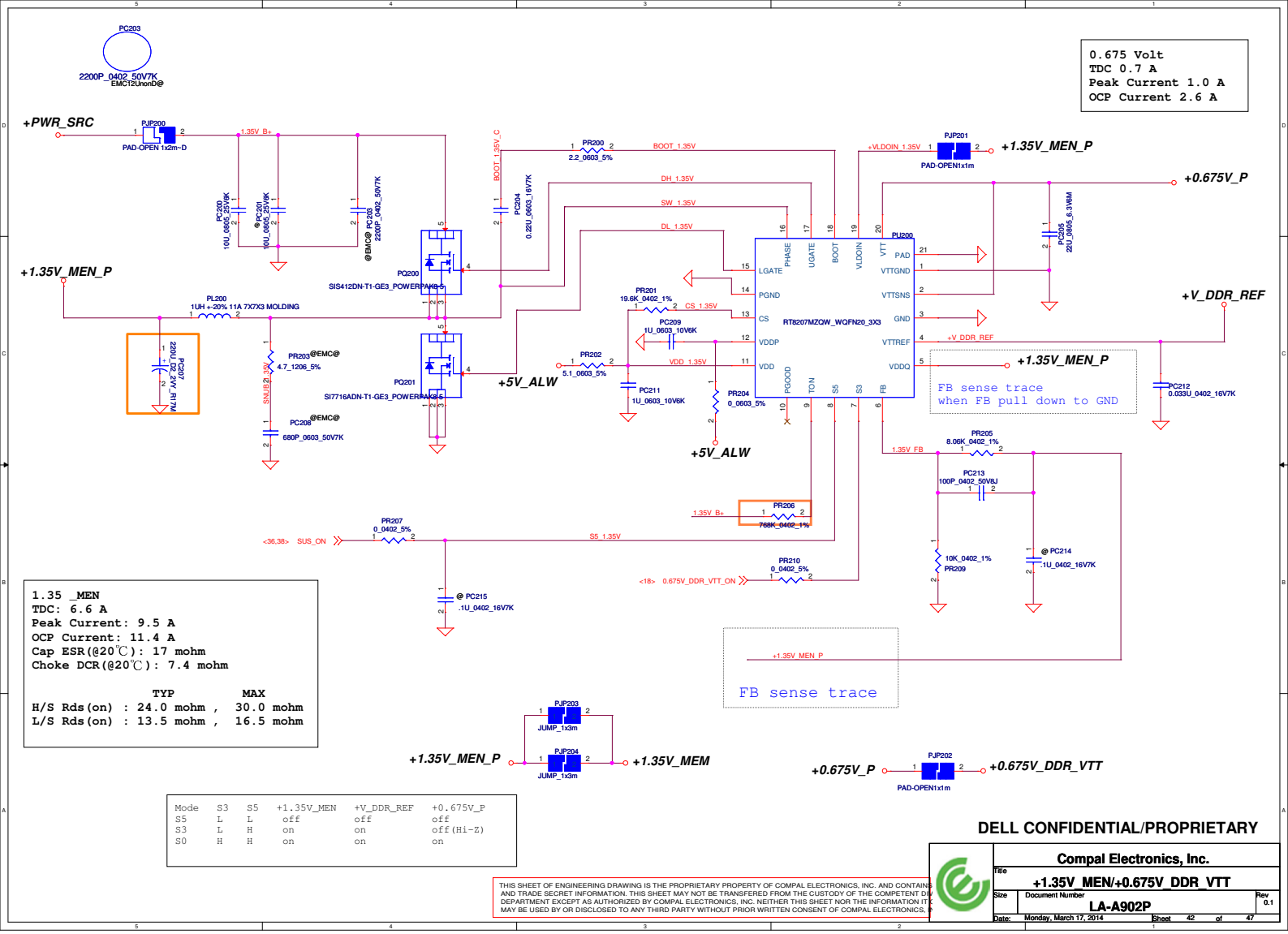
3.3 VALWP
TDC: 4.5 A
Peak Current: 6.4 A
OCP Current: 7.68 A
Cap ESR(@20℃): 18 mohm
Choke DCR(@20℃): 15.5 mohm

	TYP	MAX
H/S Rds(on)	:24.0 mohm ,	30.0 mohm
L/S Rds(on)	:13.5 mohm ,	16.5 mohm

5 VALWP
TDC: 3.5 A
Peak Current: 5.0 A
OCP Current: 6.0 A
Cap ESR(@20℃): 18 mohm
Choke DCR(@20℃): 25 mohm

	TYP	MAX
H/S Rds(on)	:24.0 mohm ,	30.0 mohm
L/S Rds(on)	:13.5 mohm ,	16.5 mohm

Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
Size	Document Number: LA-A902P
Rev	0.1
Date: Monday, March 17, 2014	Sheet 41 of 47



Compal Electronics, Inc.

Title: +1.35V_MEN/+0.675V_DDR_VTT

Size: | Document Number: LA-A902P | Rev: 0.1

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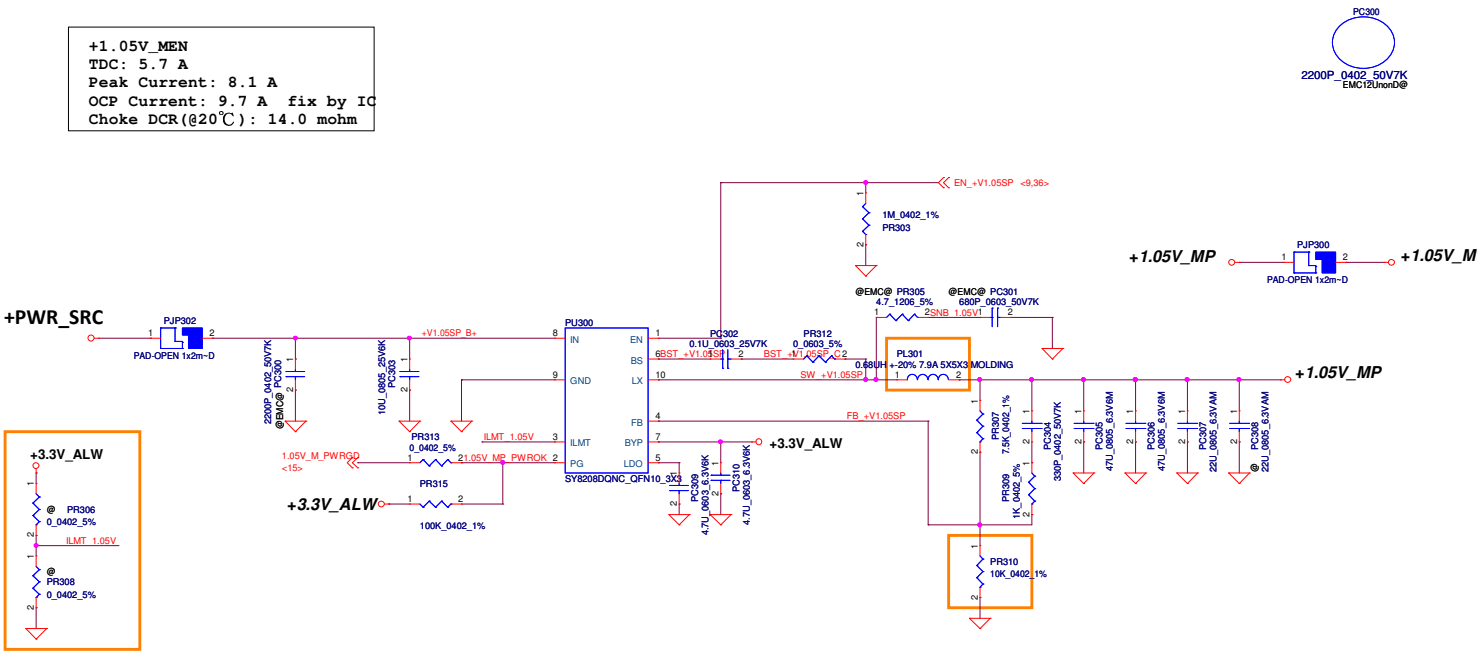
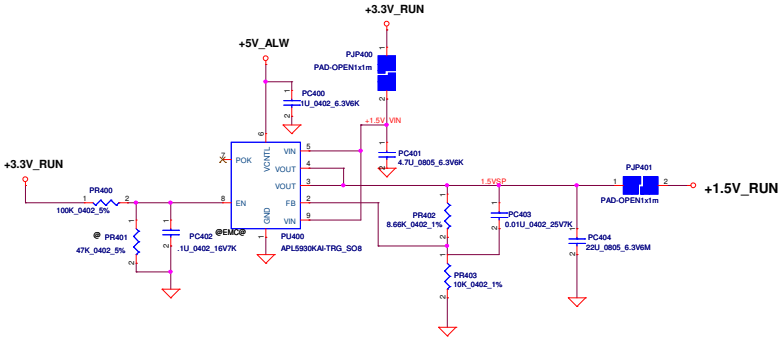
+1.05V_MEN
TDC: 5.7 A
Peak Current: 8.1 A
OCP Current: 9.7 A fix by IC
Choke DCR(@20℃): 14.0 mohm



Compal Electronics, Inc.

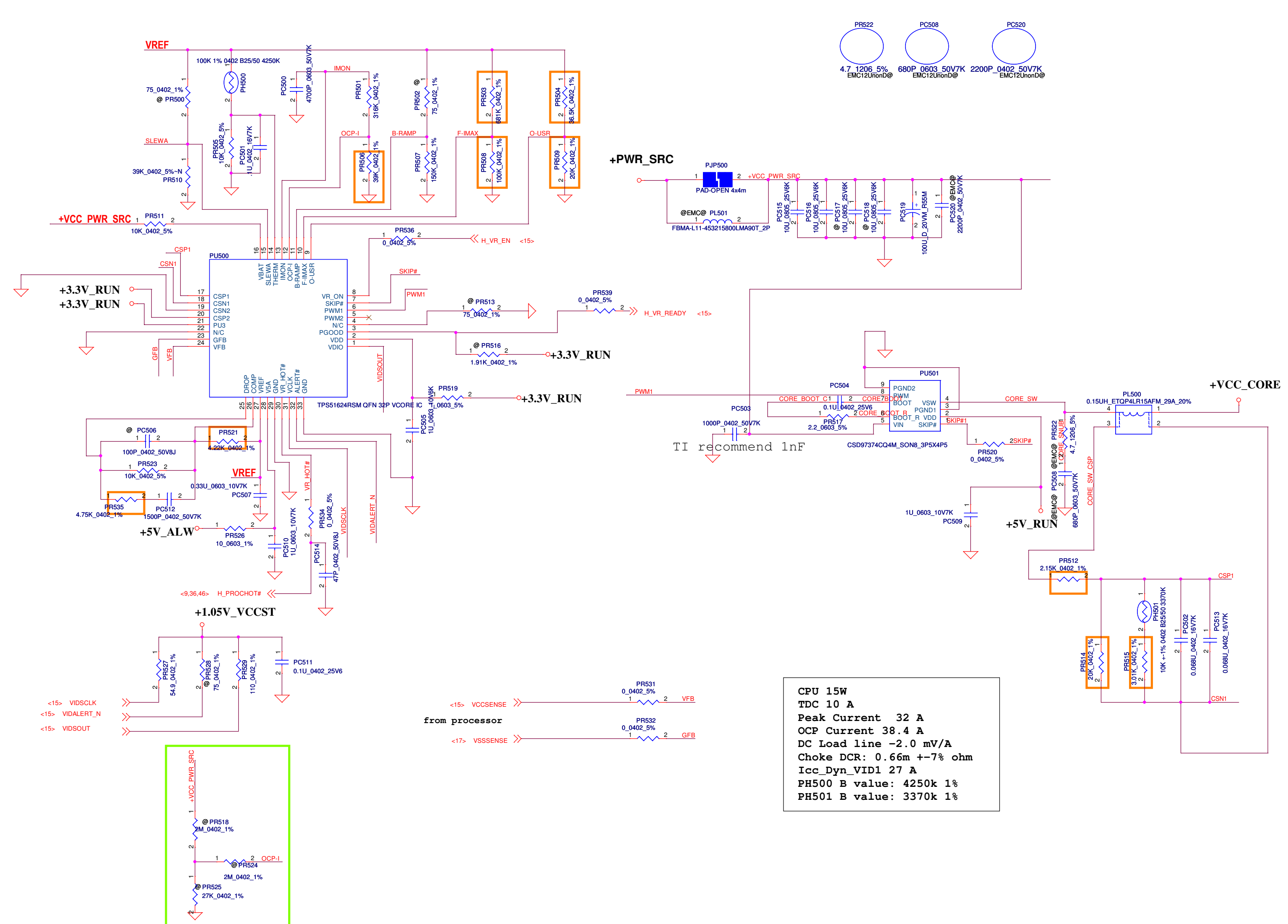
Title	+1.05V_M	
Size	Document Number: LA-A902P	Rev: 0.1
Date: Monday, March 17, 2014	Sheet 43 of 47	

+1.5V_RUN
TDC: 0.47 A
Peak Current: 0.67 A



Compal Electronics, Inc.

Title	+1.5VSP	
Size	Document Number: LA-A902P	Rev: 0.1
Date: Monday, March 17, 2014	Sheet 44 of 47	



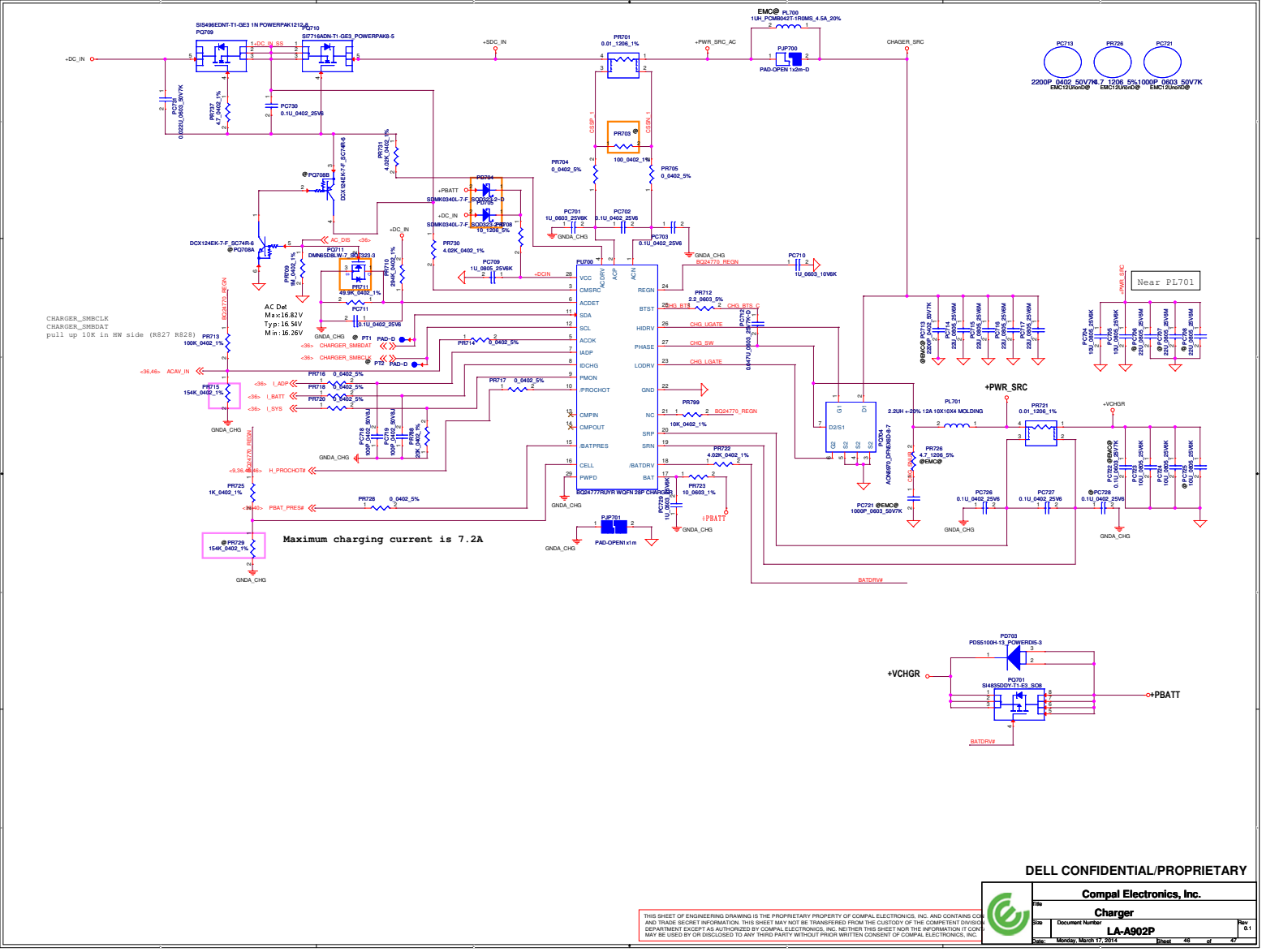
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: +VCC_CORE

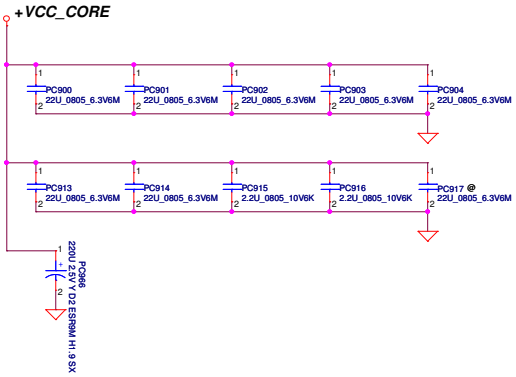
Document Number: LA-A902P — Rev 0.1

Date: Monday, March 17, 2014 — Sheet 45 of 47



DELL CONFIDENTIAL/PROPRIETARY

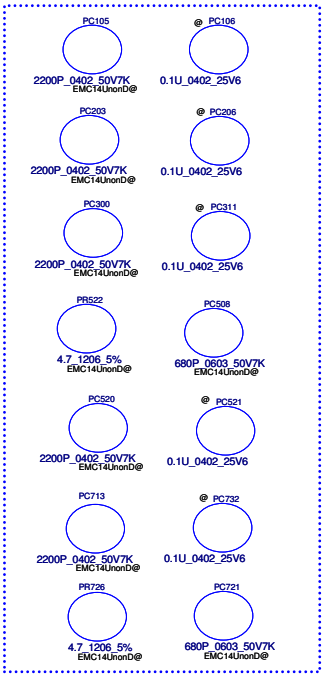
Compal Electronics, Inc.		
Title: Charger		
Size	Document Number: LA-A902P	Rev: 0.1
Date: Monday, March 17, 2014	Sheet 48 of 47	



Based on _RF Cheng. Hill

鄭智仁(11257) for PT 20131107

962



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: PROCESSOR DECOUPLING		
Size	Document Number: LA-A902P	Rev: 0.1
Date: Monday, March 17, 2014	Sheet 47 of 47	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
2	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
3	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR715, PR729 to 154k	X01
4	41,43,44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
5	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
6	ALL	ALL	10/31	Compal	RF request	Pop PR522,PC508, PR726, PC721, PC713, PL501, PC520	X01
7	46	Charger	12/05	Compal	Has the same behavior with dock circuit	Add PQ711	X01
8	46	Charger	12/05	Compal	To add 2nd source	Remove PQ702 Add PQ709, PQ710	X01
9	46	Charger	12/05	Compal	To reduce leakage current	Remove PD701 Add PD704, PD705	X01
10	46	Charger	3/03	Compal	To set OVP level	Remove PR729	X02
11	46	Charger	3/03	Compal	To set IC function	Remove PC720 Add PR788, PR799	X02
12	40	DCIN	3/03	Compal	For ME change request	Change PBATT1	X02
13	40	DCIN	3/03	Compal	For EMC change request	Add PD5 PC20 PC21 PC22 Remove PC11	X02

Compal Electronics, Inc.

Title: PWR P.I.R (1/1)

Size | Document Number: LA-A902P | Rev: 0.1

Date: Monday, March 17, 2014 | Sheet 48 of 48

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2(X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2(X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2(X01)
4	22	HW	2013/10/9	COMPAL			0.2(X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2(X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2(X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2(X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2(X01)
9	24	HW	2013/10/9	COMPAL	SATA ciruit issue	Swap mSATA P & N	0.2(X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2(X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2(X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2(X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2(X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2(X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 → RUN_ON_EC	0.2(X01)
17	12	HW	2013/10/24	COMPAL			0.2(X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2(X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2(X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 &CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2(X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2(X01)
22	30	HW	2013/10/29	COMPAL			0.2(X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2(X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2(X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDP_WAN_SMBDAT/SMBCLK	0.2(X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2(X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2(X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2(X01)
39	21	HW	2013/12/17	COMPAL			0.3(X01)
40	22	HW	2013/12/17	COMPAL			0.3(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	22	HW	2013/12/17	COMPAL			0.3(X01)
30	22	HW	2013/12/17	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2. remove QZ12,RZ48,RZ49,RZ50	0.3(X01)
31	22	HW	2013/12/17	COMPAL			0.3(X01)
32	7	HW	2013/12/27	COMPAL	Intel recommend	Change RC33, RC34 from 1k to 499 ohm	0.3(X01)