

Compal Confidential

Model Name :Q5WV1/Q5WS1

Compal Project Name :

File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document

Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH

Nvidia N13P GS/GL

2011-12-24

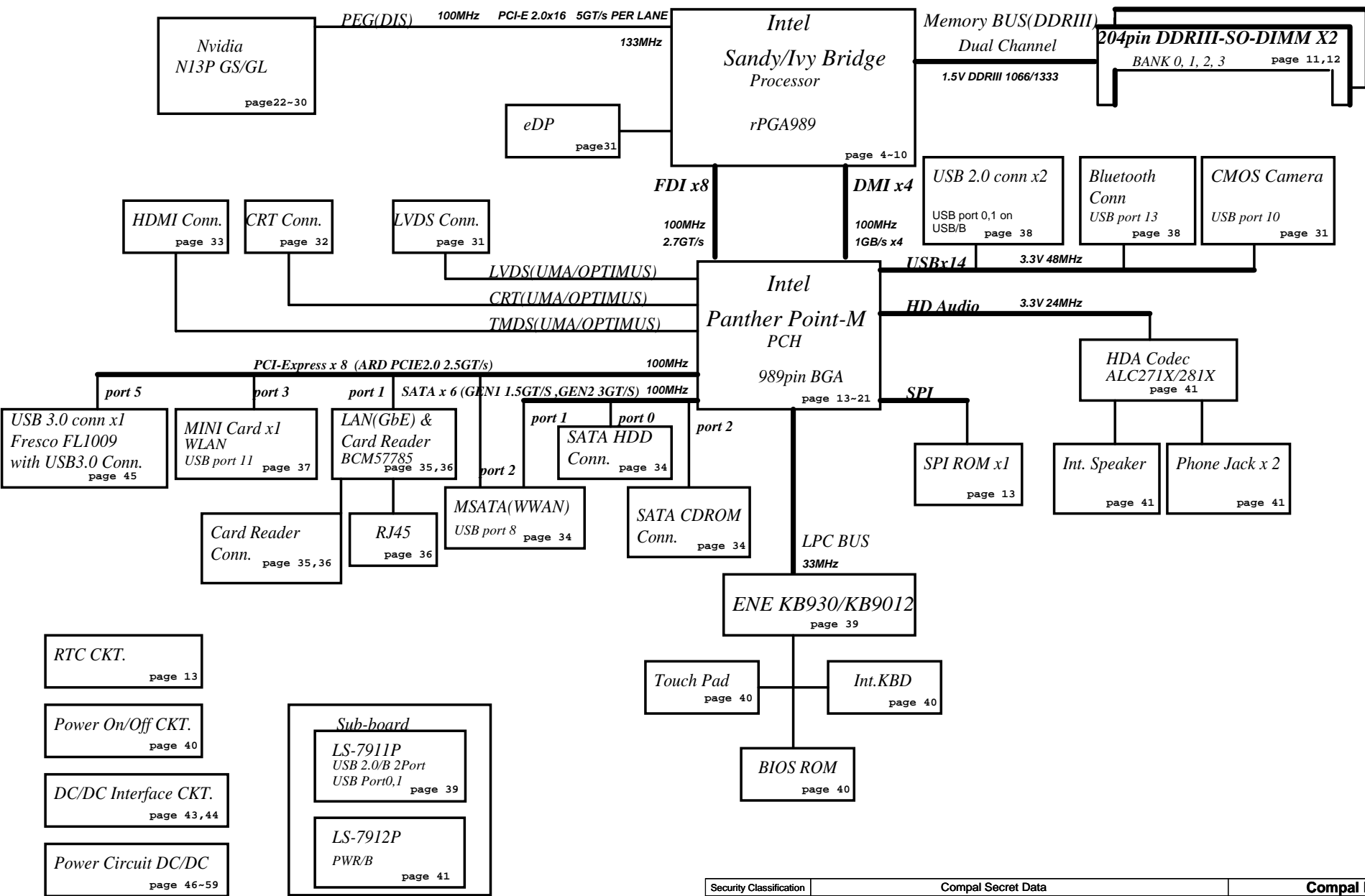
REV:0.2

Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B



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Fan Control
page 42



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BT & USB30 & USB20 Config

OPTMIUS SKU:DIS@ N13P-GL:GL@ N13P-GS:GS@ N13P-GF108_ES4:GF108@
 BT SKU:BT@
 internal USB SKU: PUSB@ DIS USB30 SKU:DUSB@
 eDP SKU: EDP@
 LVDS SKU: LVDS@
 EC 930 SKU: 930@ EC 9012 SKU: 9012@
 PCH HM65: HM65@ PCH HM76: HM76@
 Win8: WIN8@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

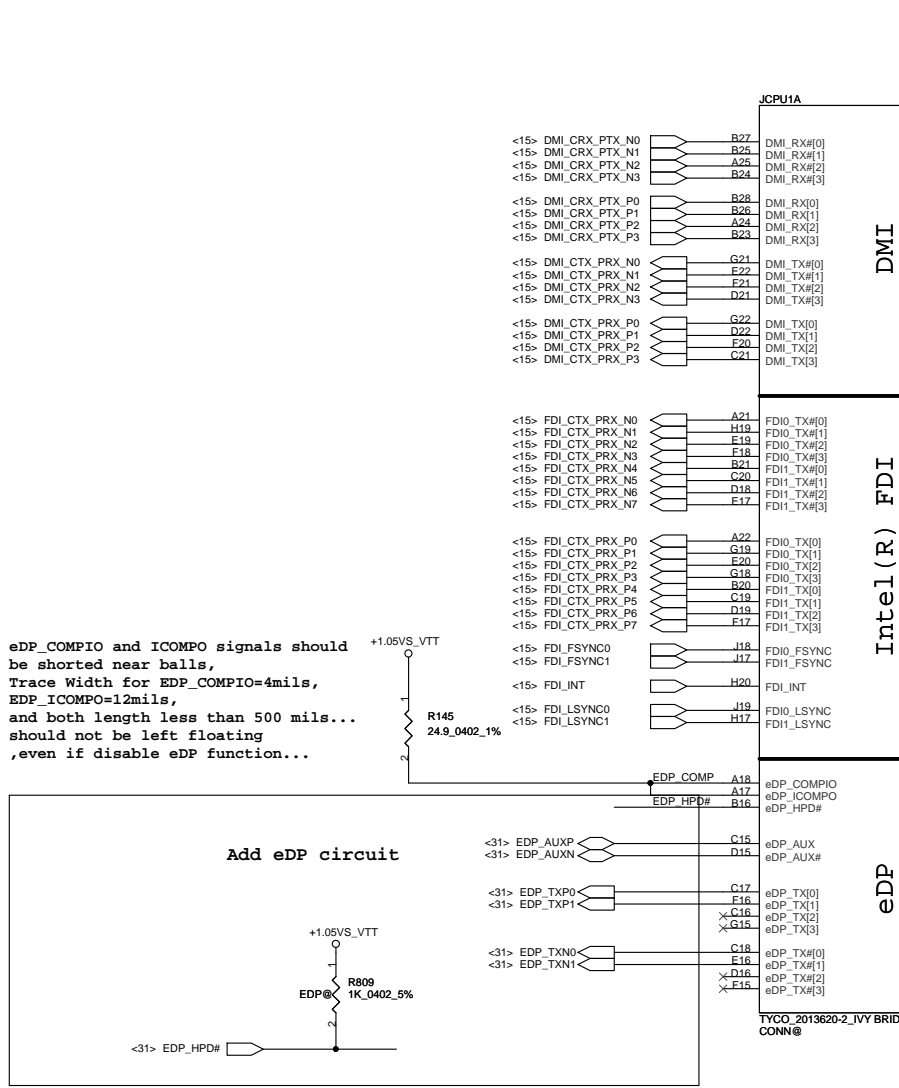
BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@

USB Port Table

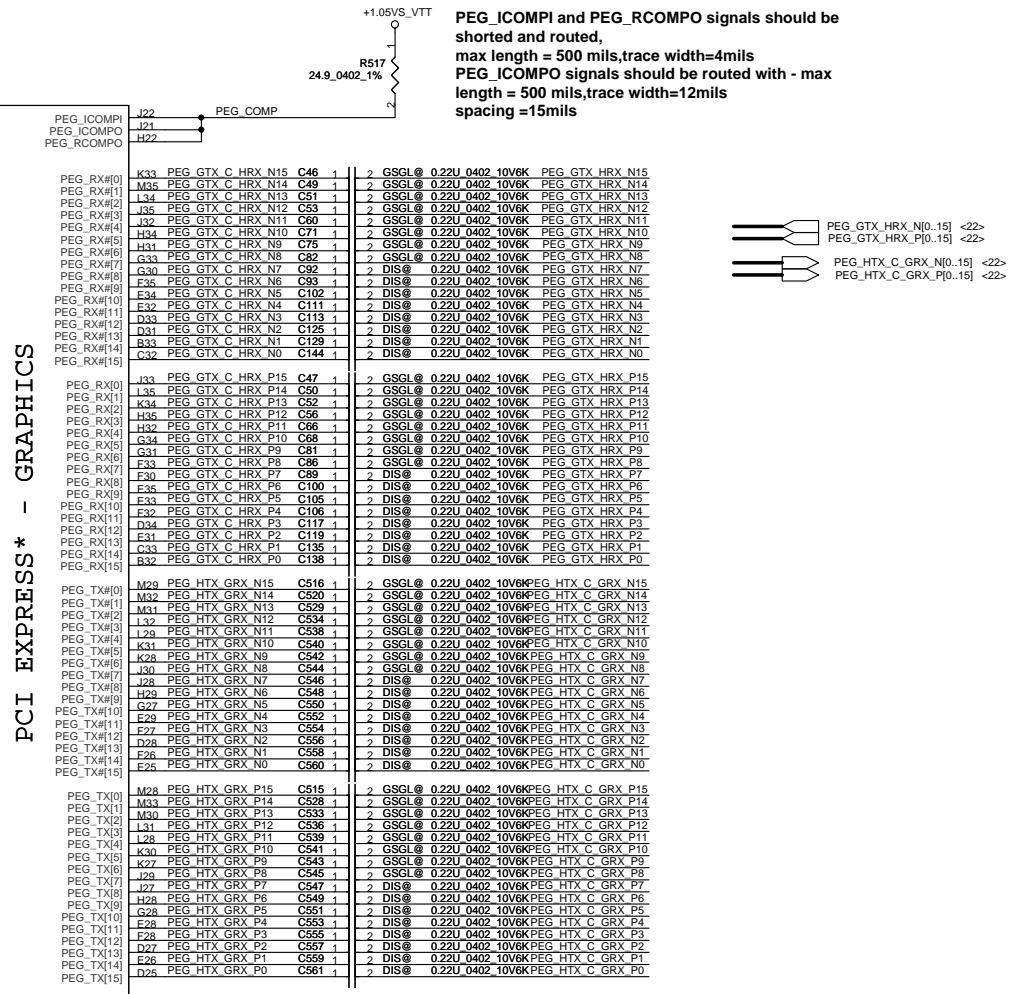
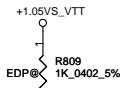
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
	UHCI1	2	USB/B (Right Side)
		3	
		4	
	UHCI2	5	
		6	
7			
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	
	UHCI5	10	Camera
		11	BlueTooth
	UHCI6	12	
		13	

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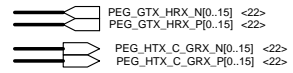


eDP_COMPIO and ICOMPO signals should be shorted near balls, Trace Width for EDP_COMPIO=4mils, EDP_ICOMPO=12mils, and both length less than 500 mils... should not be left floating ,even if disable eDP function...

Add eDP circuit



PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed, max length = 500 mils, trace width=4mils PEG_ICOMPO signals should be routed with - max length = 500 mils, trace width=12mils spacing =15mils

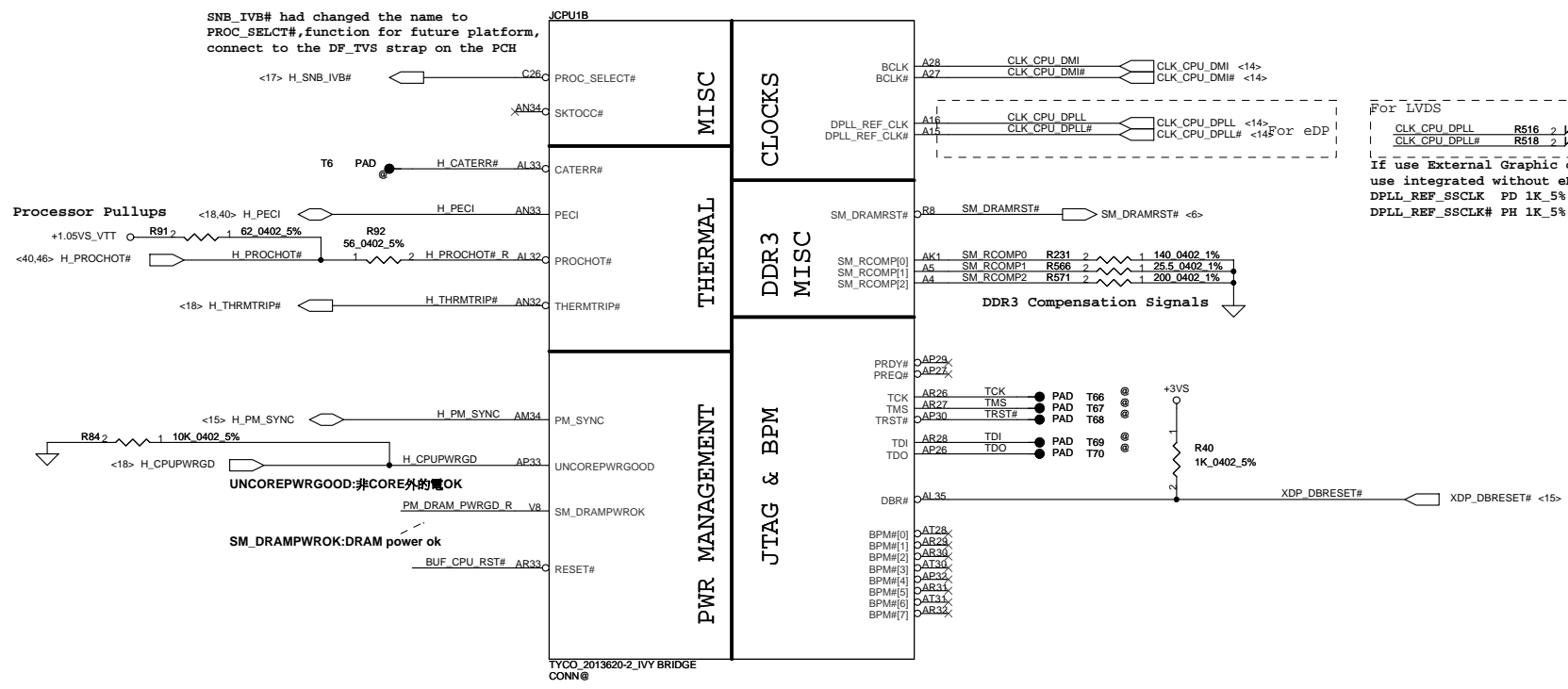


PCI EXPRESS* - GRAPHICS

eDP

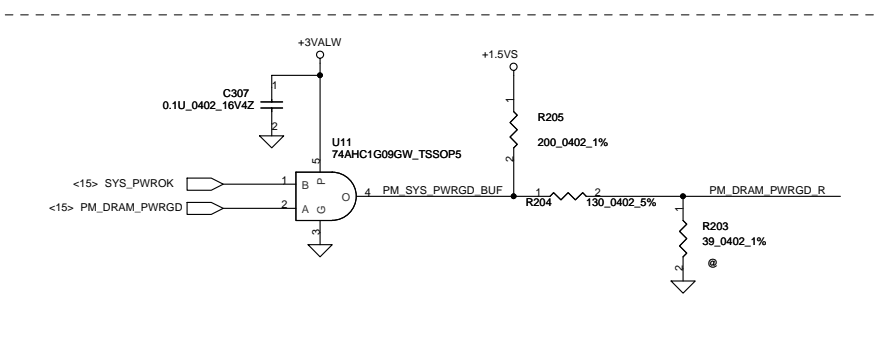
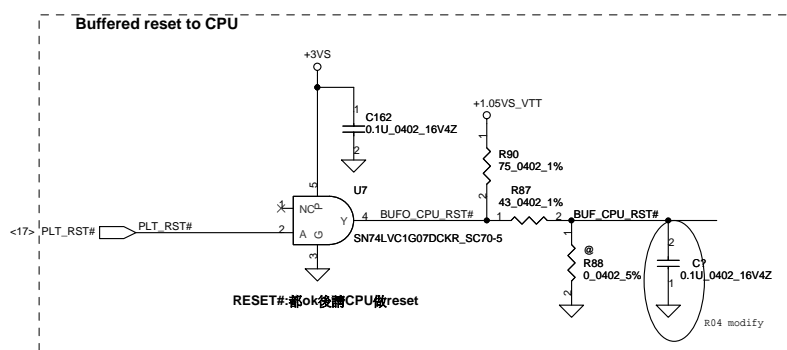
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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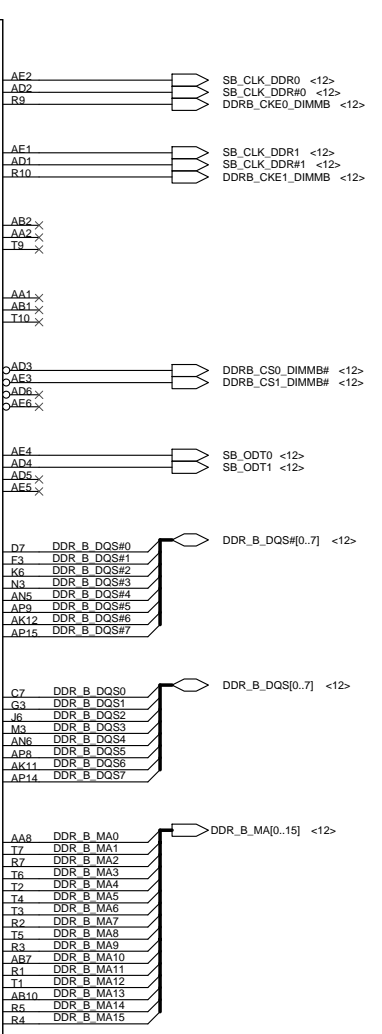
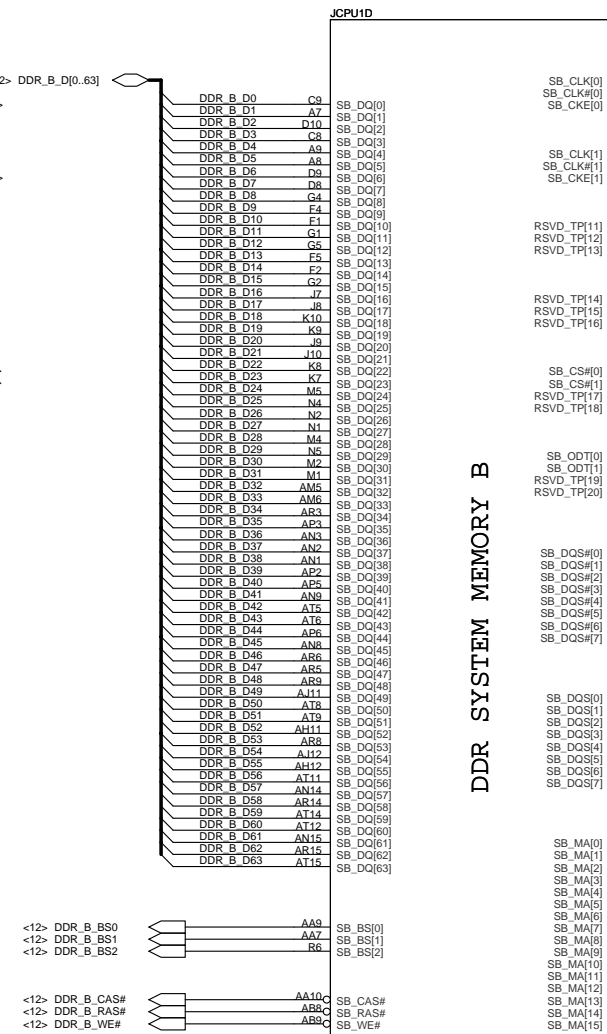
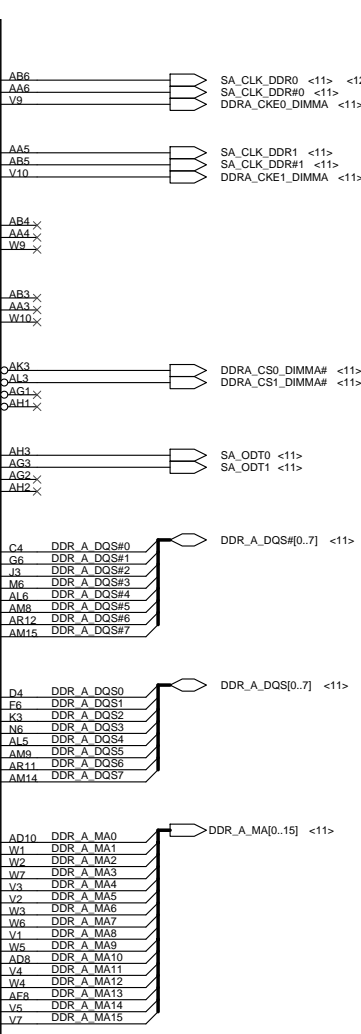
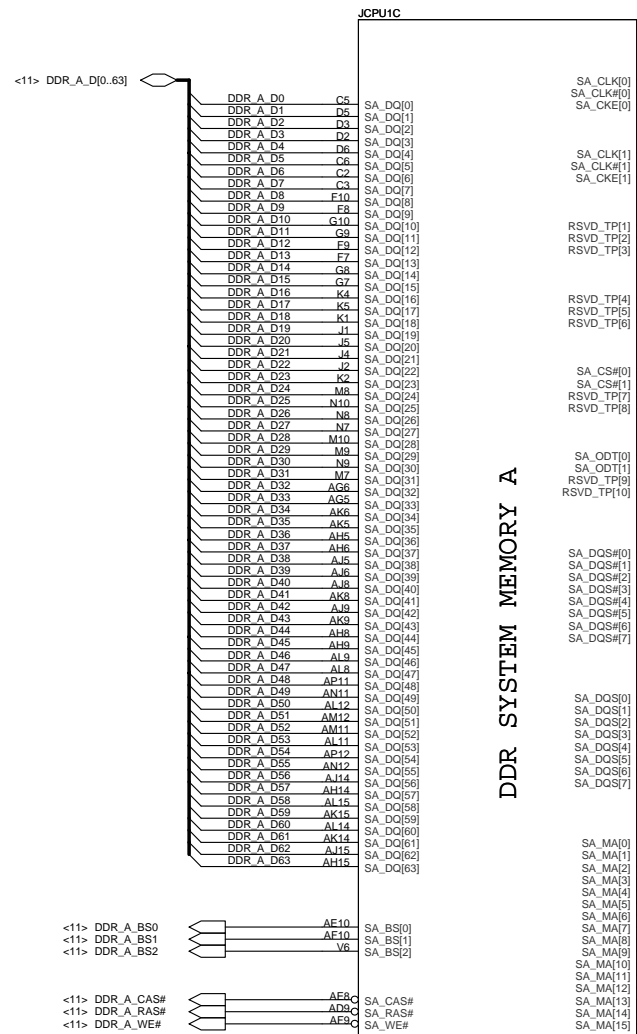


For LVDS
 CLK CPU DPLL R516 2 LVDS@ 1.1K 0.402 5%
 CLK CPU DPLL# R518 2 LVDS@ 1.1K 0.402 5%
 +1.05VS_VTT

If use External Graphic or use integrated without eDP
 DPLL_REF_SSCLK PD 1K_5% to GND
 DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT



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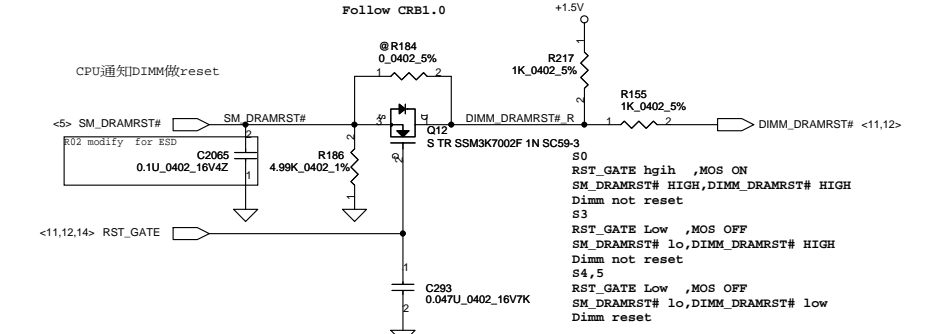


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

TYCO_2013620-2_IVY BRIDGE
CONN@

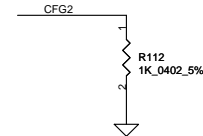
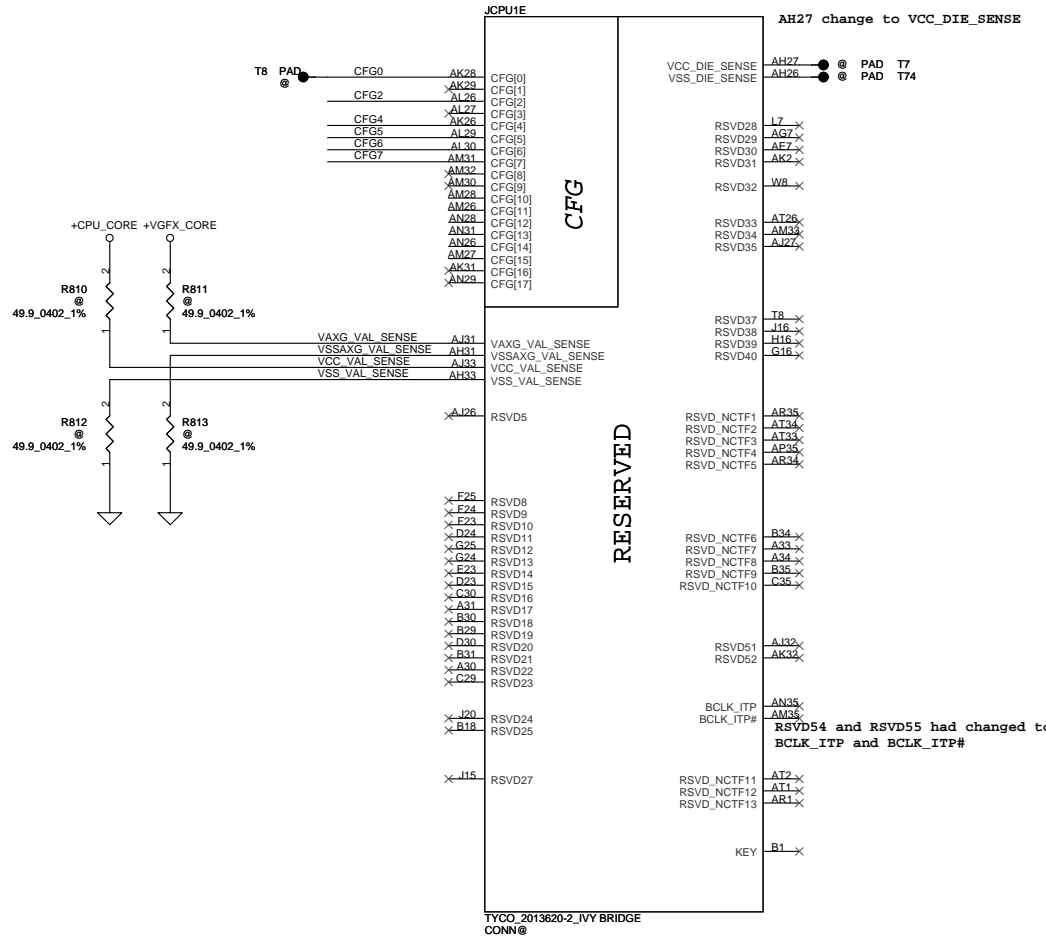
TYCO_2013620-2_IVY BRIDGE
CONN@



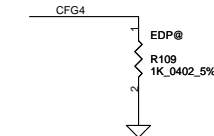
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CFG Straps for Processor

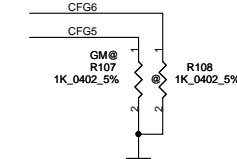
AH26	Sandy	Ivy
	GND	VSS_DIE_SENSE



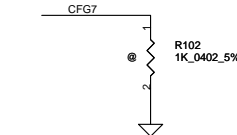
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

SV type CPU

JCPU1F

POWER

+CPU_CORE
QC 53A
DC 53A

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- P35 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC99
- P25 VCC100

PEG AND DDR

CORE SUPPLY

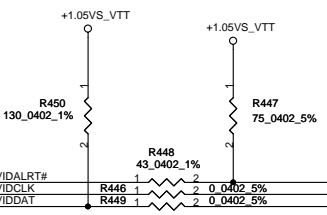
SVID

SENSE LINES

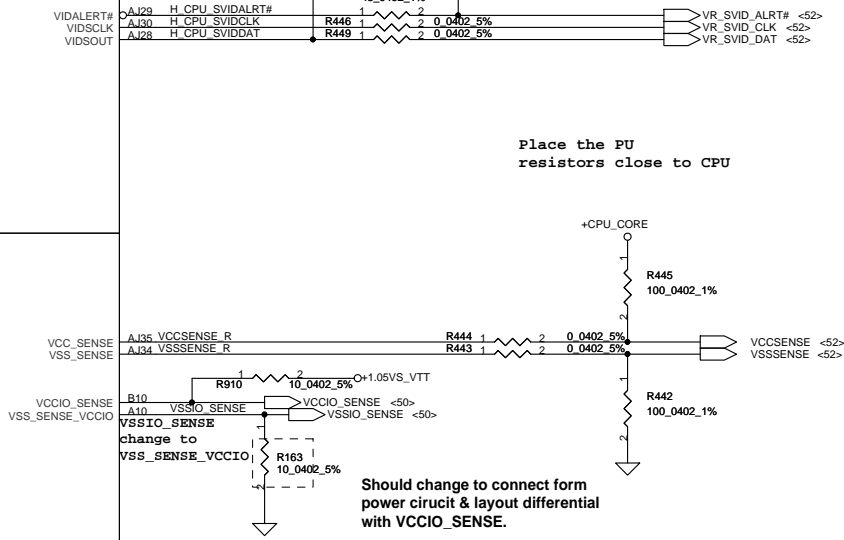
- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AC10
- VCCIO4 Y10
- VCCIO5 U10
- VCCIO6 L10
- VCCIO7 L10
- VCCIO8 J14
- VCCIO9 J13
- VCCIO10 J12
- VCCIO11 H14
- VCCIO12 H14
- VCCIO13 H12
- VCCIO14 H11
- VCCIO15 G14
- VCCIO16 G13
- VCCIO17 G12
- VCCIO18 F14
- VCCIO19 F13
- VCCIO20 F12
- VCCIO21 F11
- VCCIO22 E14
- VCCIO23 E12
- VCCIO24 E12
- VCCIO25 F11
- VCCIO26 D14
- VCCIO27 D13
- VCCIO28 D12
- VCCIO29 D11
- VCCIO30 C14
- VCCIO31 C13
- VCCIO32 C12
- VCCIO33 C11
- VCCIO34 B14
- VCCIO35 B12
- VCCIO36 A14
- VCCIO37 A13
- VCCIO38 A12
- VCCIO39 A11
- VCCIO40 J23

8.5A

+1.05VS_VTT



Place the PU resistors close to CPU

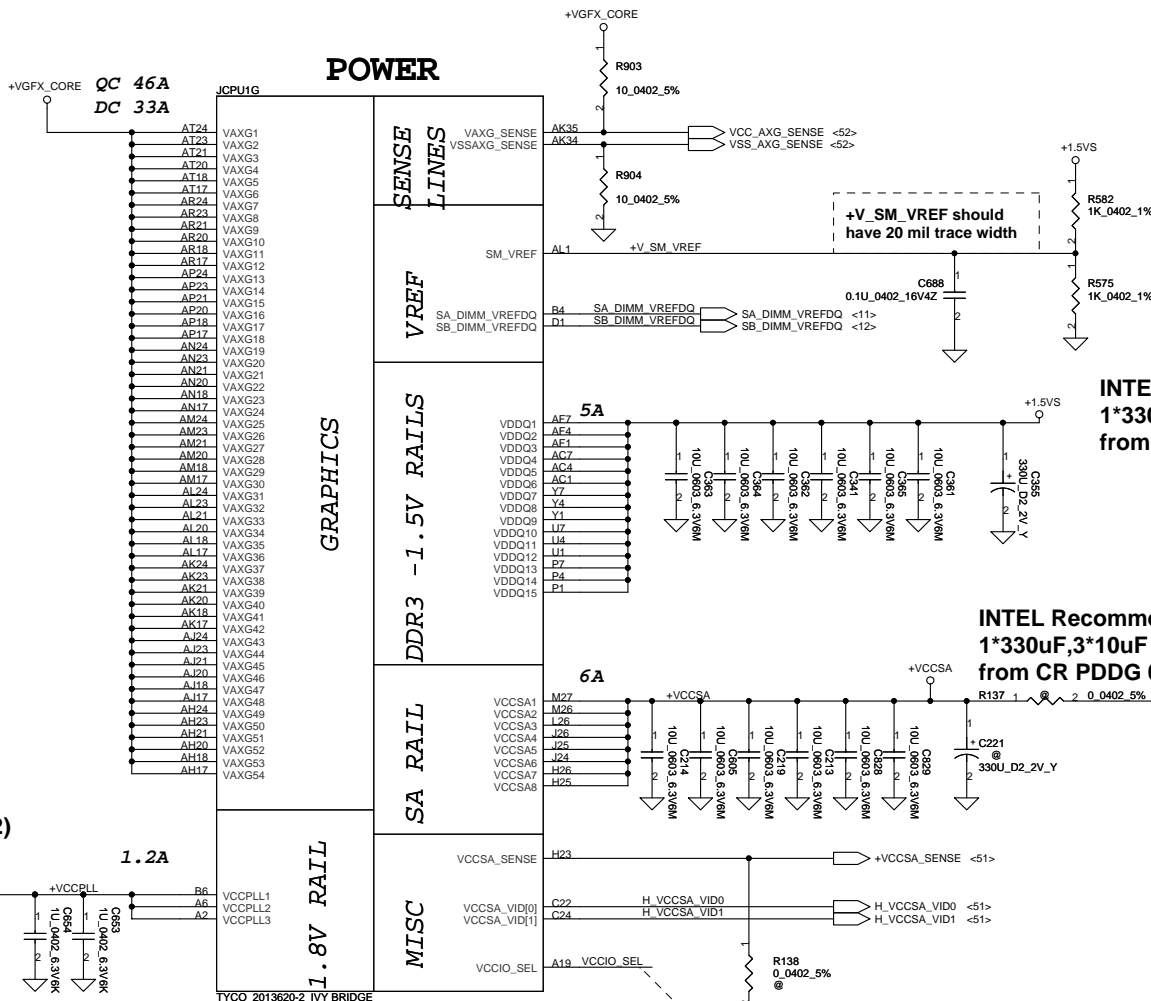


Should change to connect form power circuit & layout differential with VCCIO_SENSE.

TYCO_2013620-2_IVY BRIDGE CONN@

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INTEL Recommend
1*330uF, 1*10uF and 2*1uF(0402)
from CR PDDG 0.8

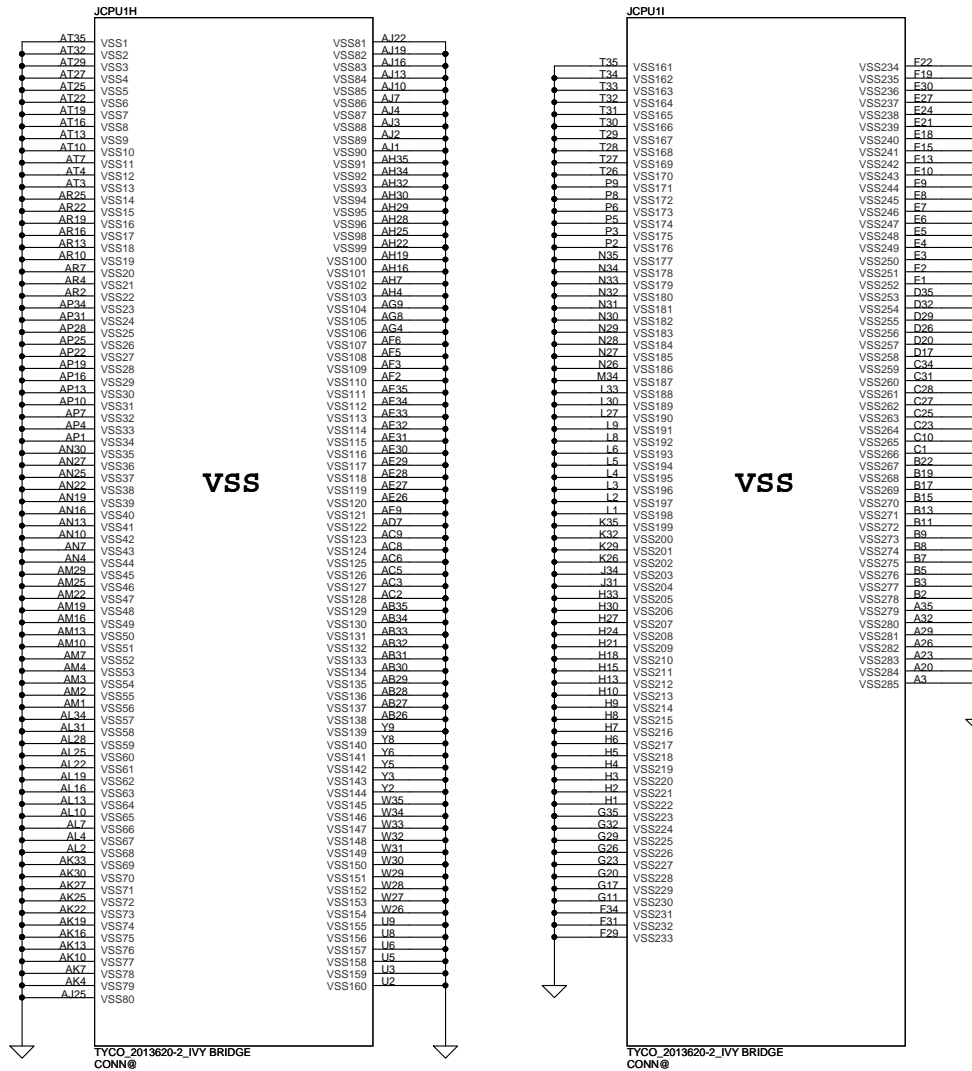
INTEL Recommend
1*330uF, 6*10uF
from CR PDDG 0.8

INTEL Recommend
1*330uF, 3*10uF
from CR PDDG 0.8

VCCSA				
VID0	VID1	Vout	Sandy	Ivy
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

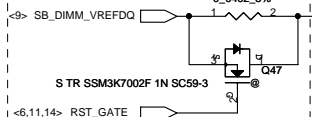
VCCIO_SEL For 2012 CPU support	
A19	* 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

RSVD26 had changed the name to VCCIO_SEL
 Need PH +3VALW 10K at +1.05VS_VTT source
 for 2012 processor +1.05V and +1.0V select

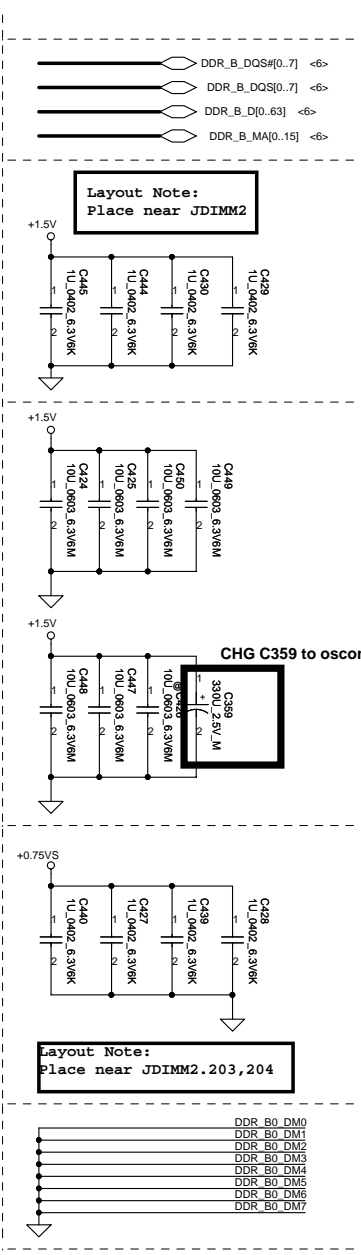
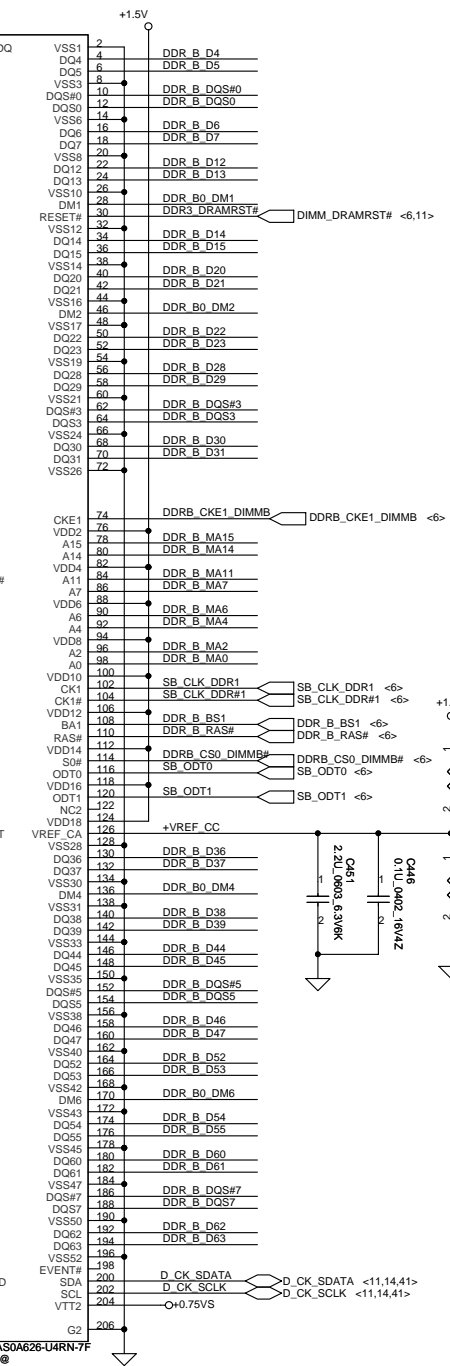
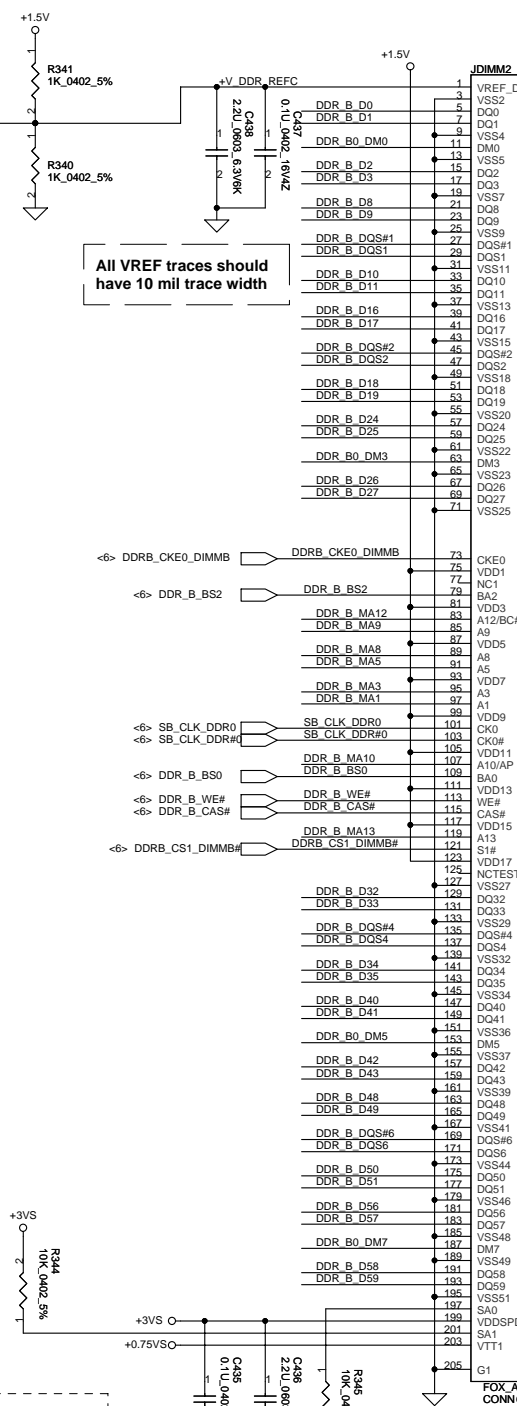


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M3 support

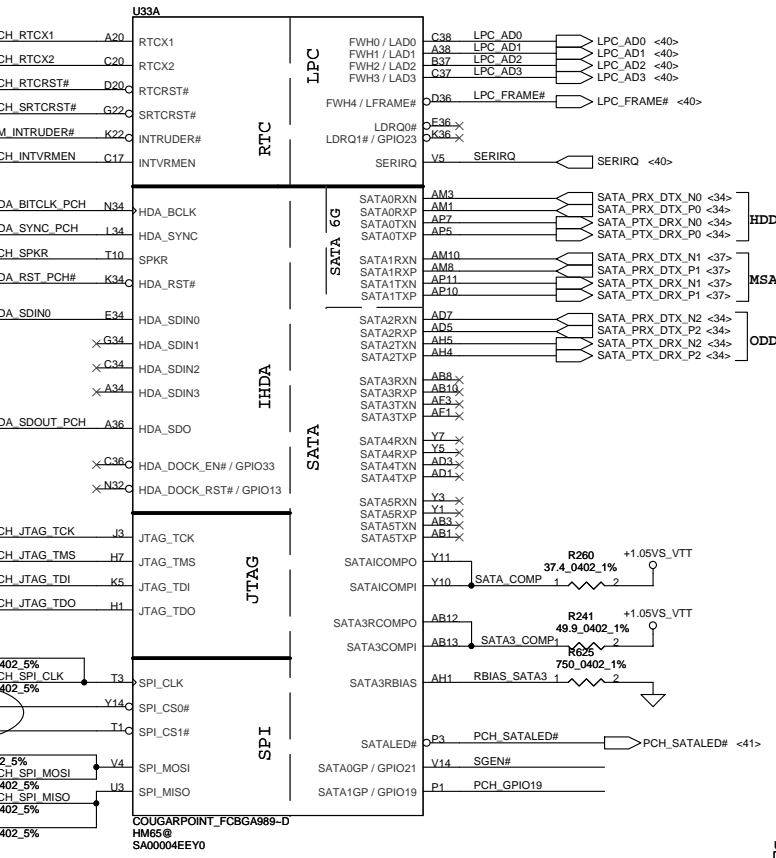
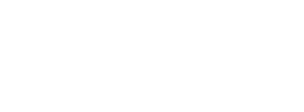
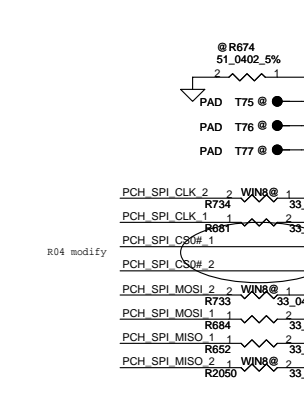
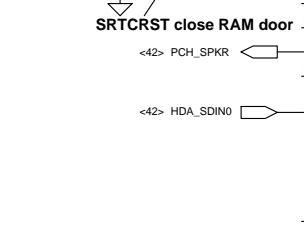
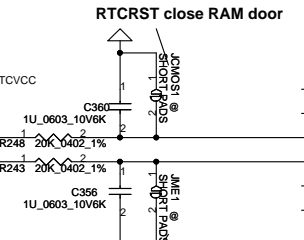
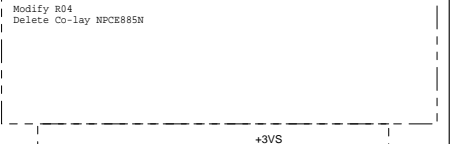
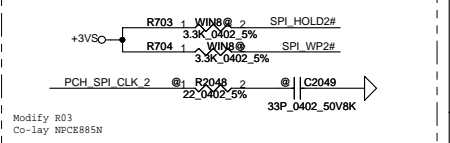
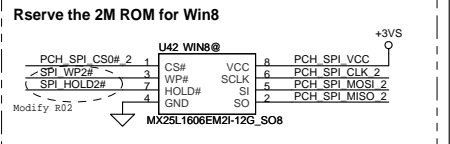
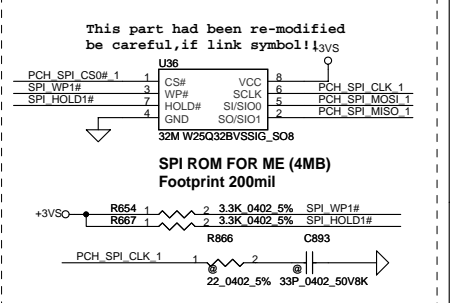
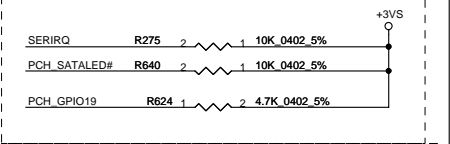
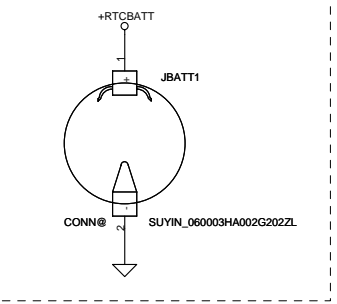
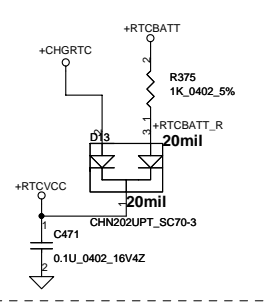
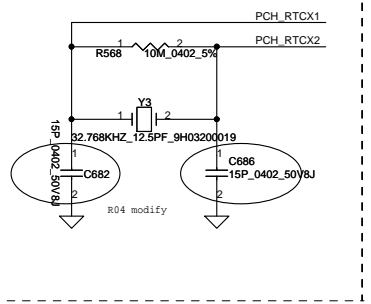
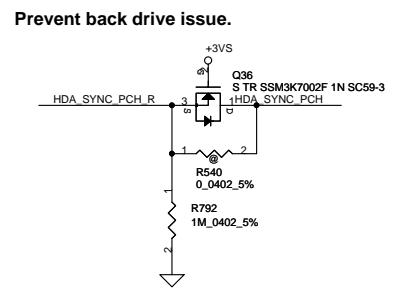
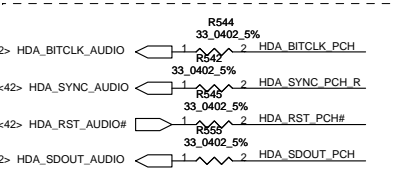
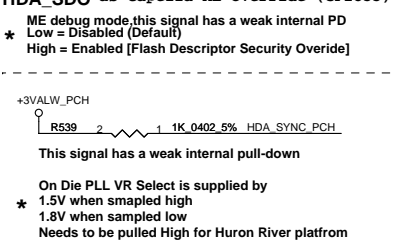
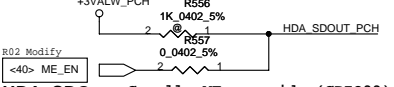
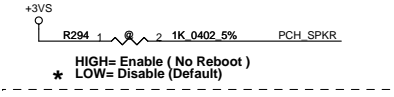
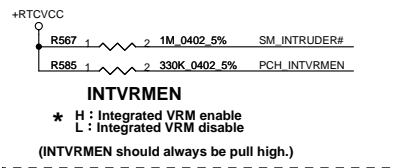


All VREF traces should have 10 mil trace width



<Address(SA1,SA0): 10>
DIMM_2 Reserve H:4mm

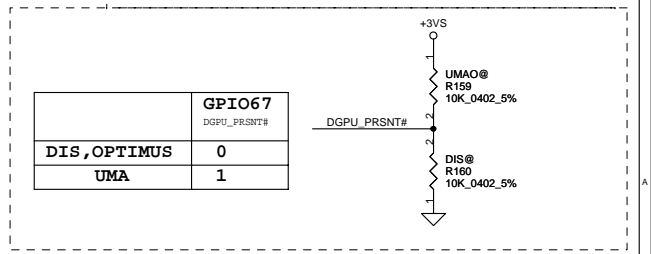
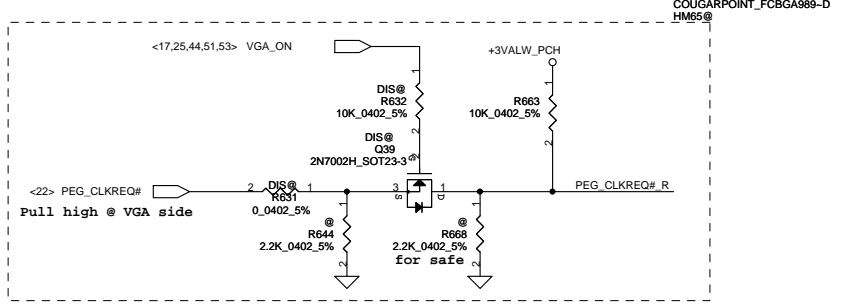
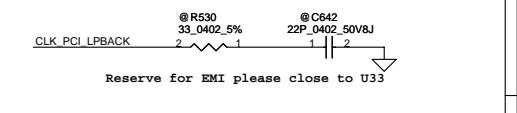
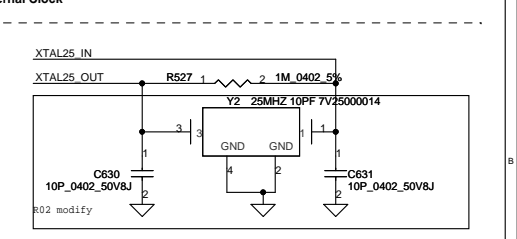
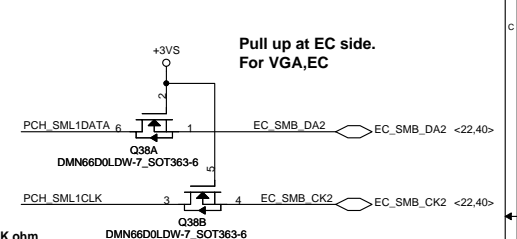
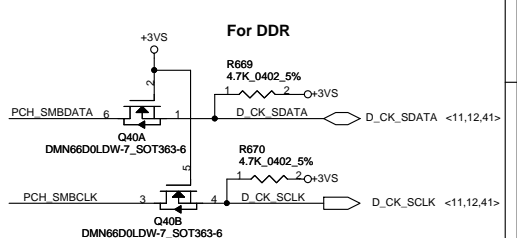
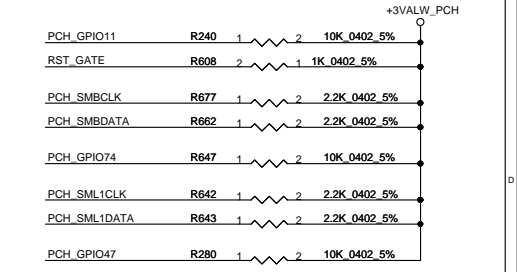
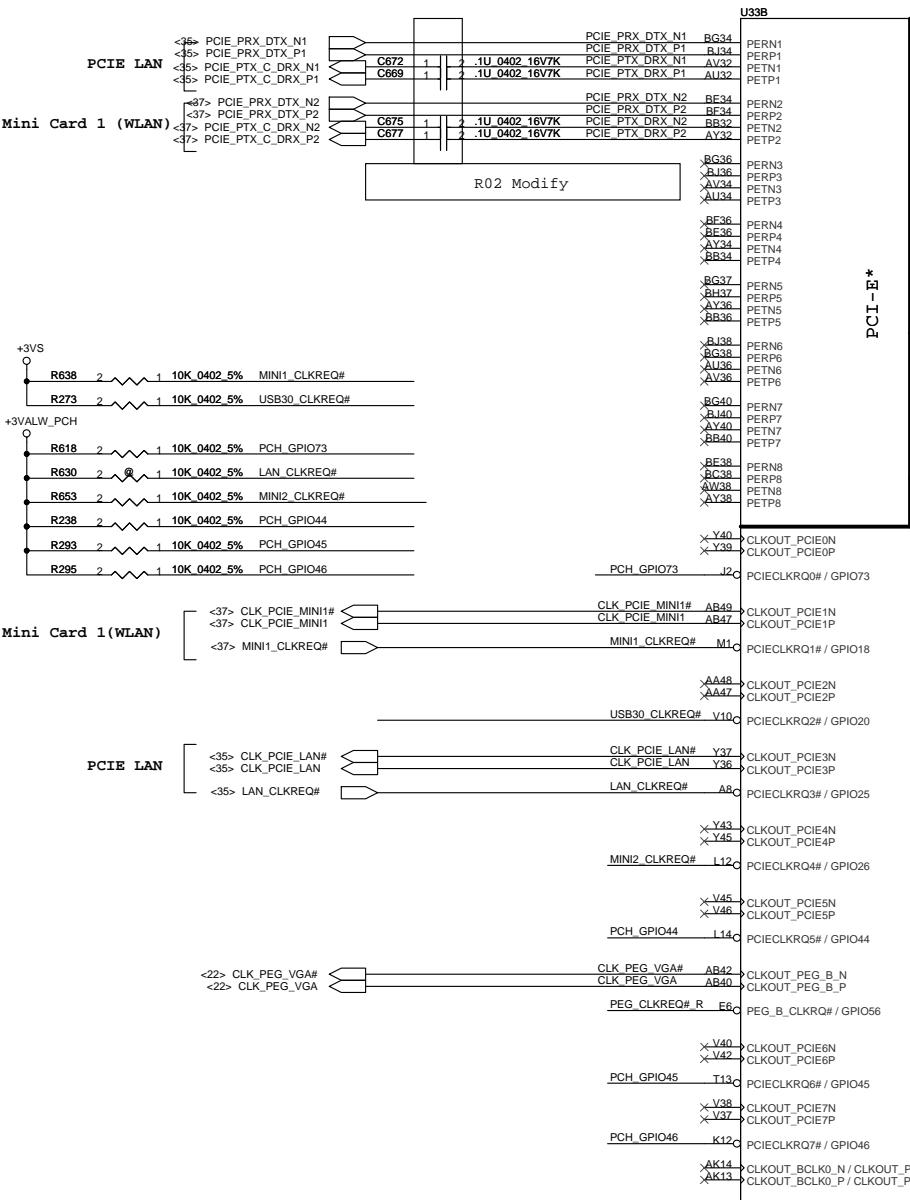
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GPIO21	
SGEN#	
Switchable GPU	0
*Non-Switchable	1

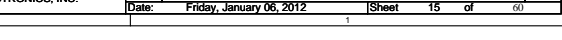
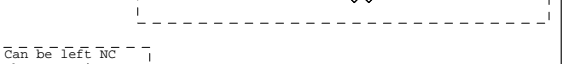
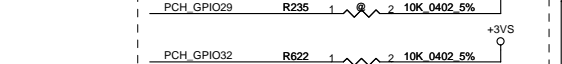
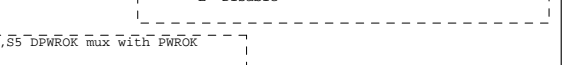
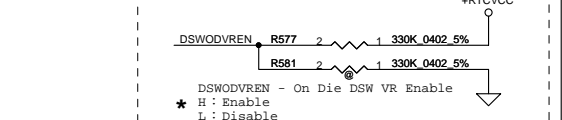
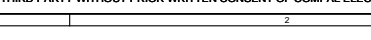
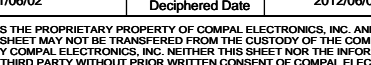
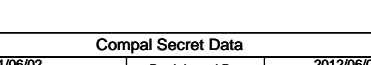
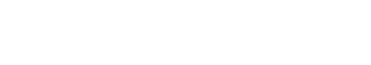
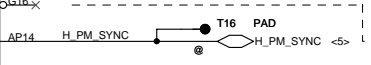
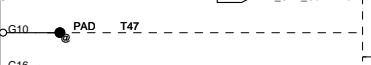
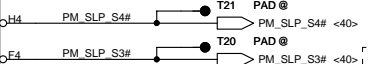
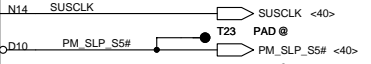
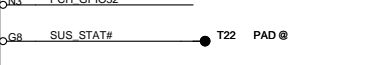
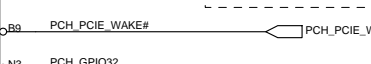
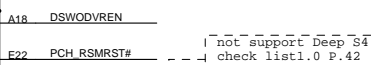
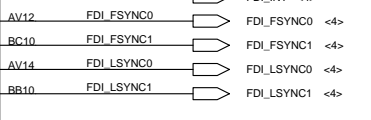
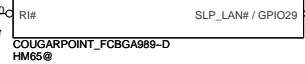
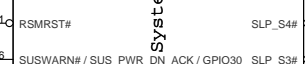
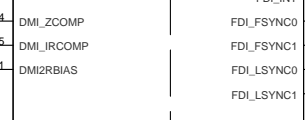
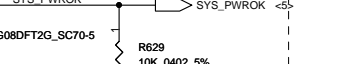
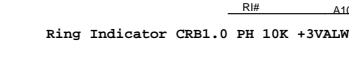
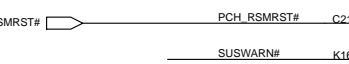
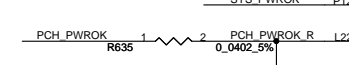
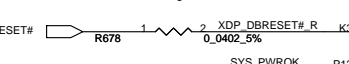
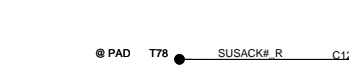
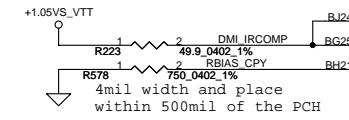
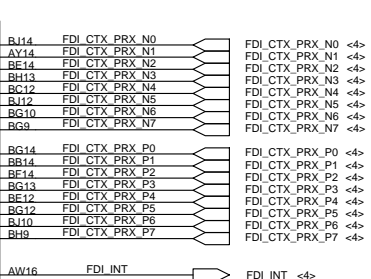
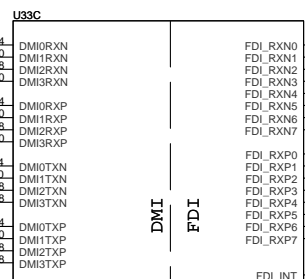
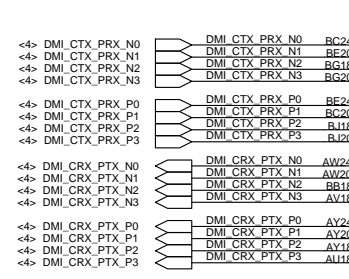
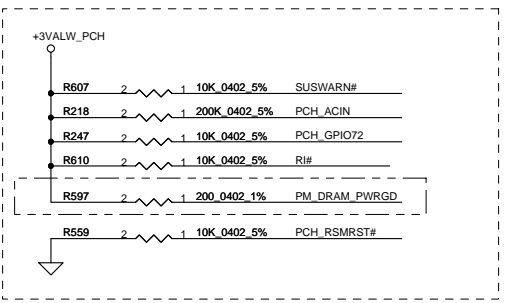
Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

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GPIO67	DGPU_PRSN#
DIS,OPTIMUS	0
UMA	1

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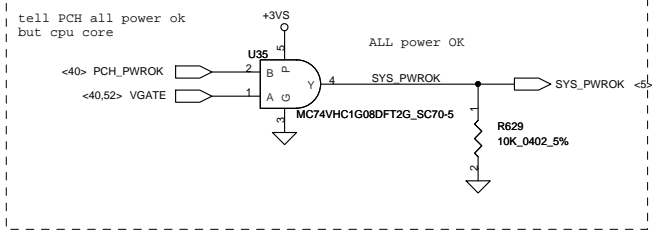


not support AMT APWROK can mux with PWROK (check list1.0 P.40)

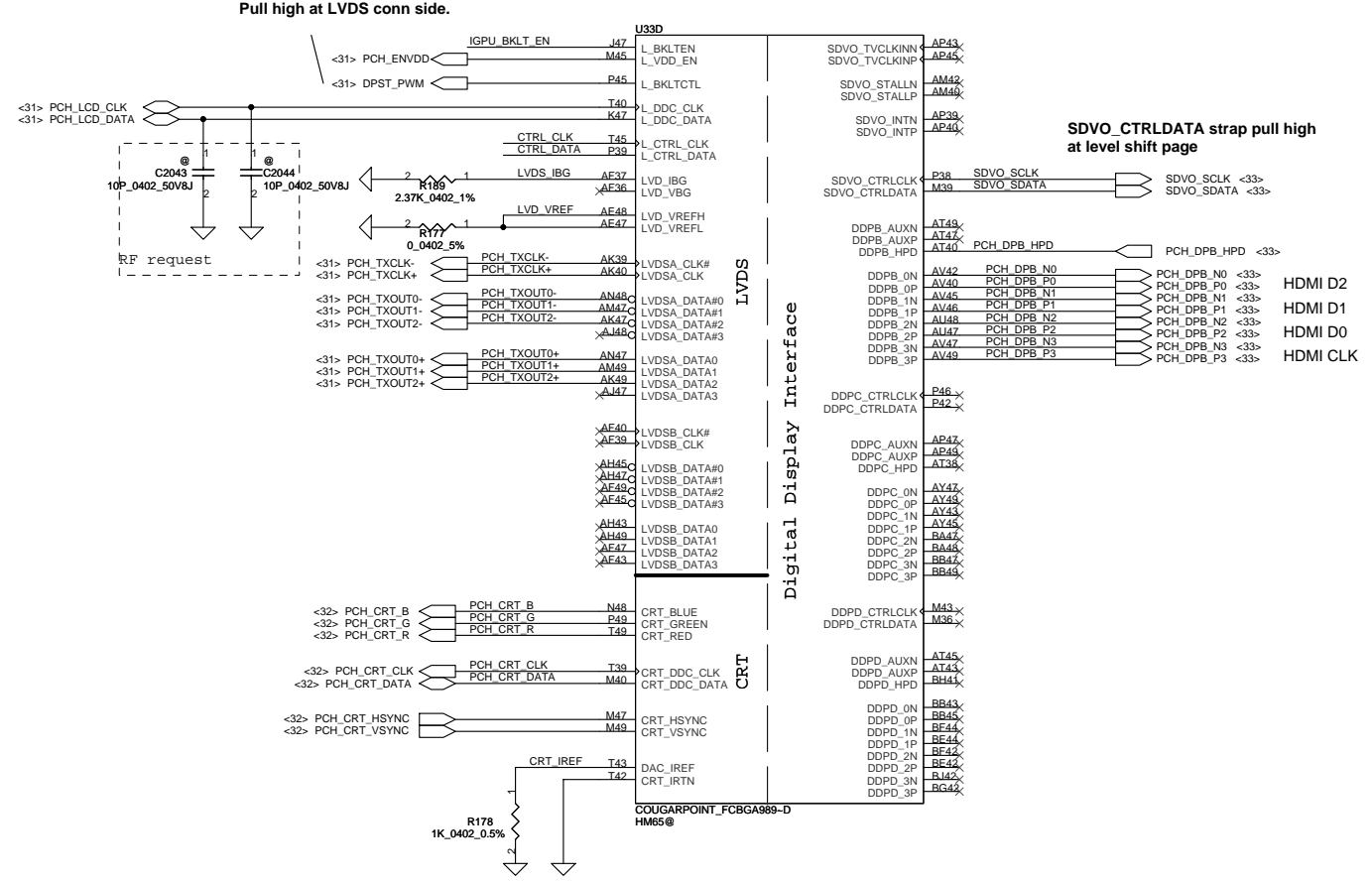
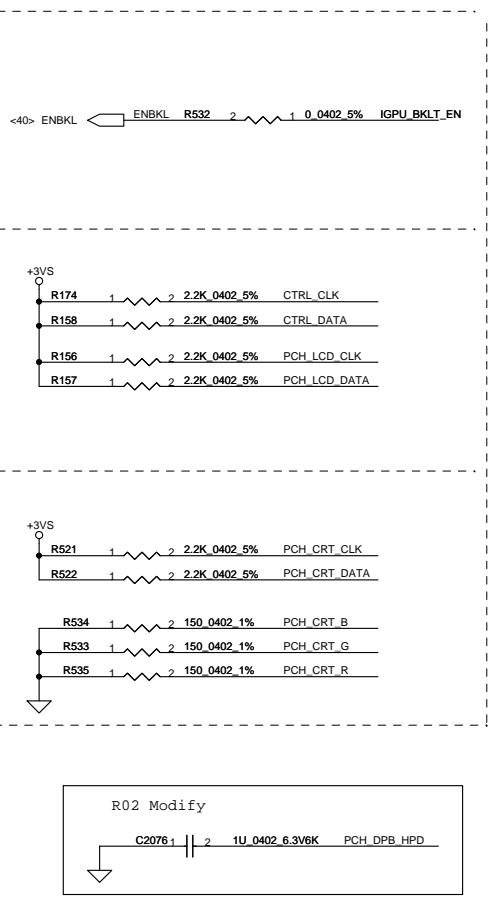
not support Deep S4,S5 DPWROK mux with PWROK check list1.0 P.42

Can be left NC when IAMT is not support on the platform

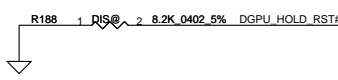
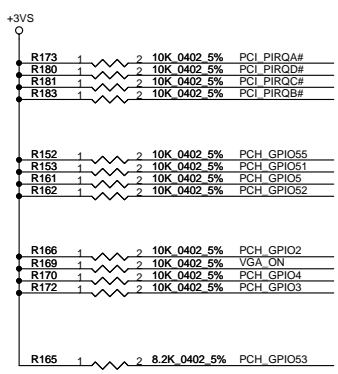
not support Deep S4,S5 can NC PCH EDS1.2 P.74



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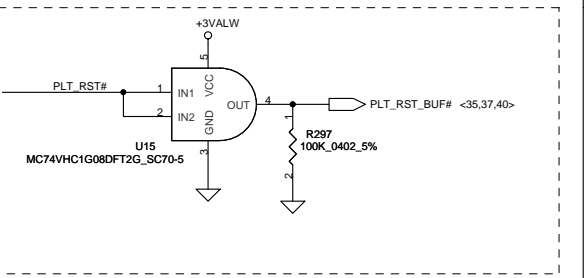
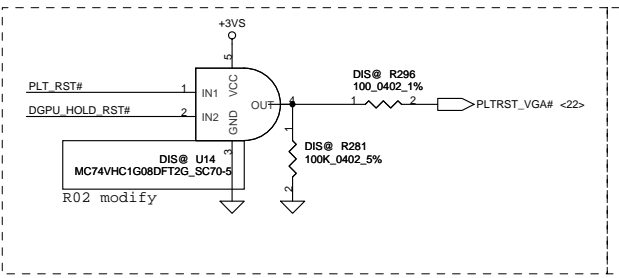
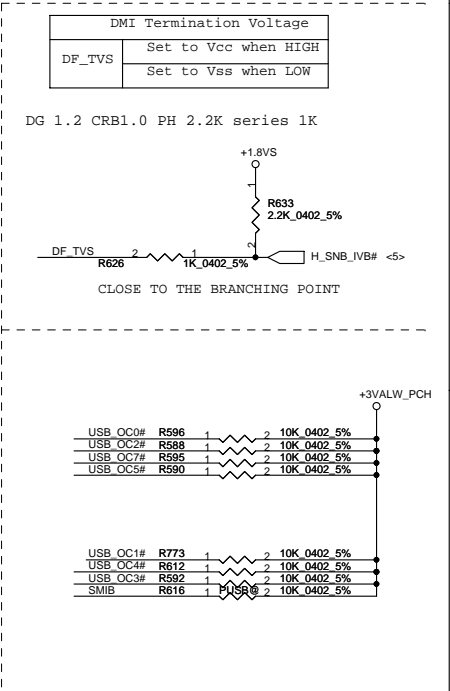
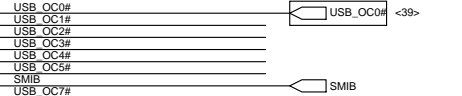
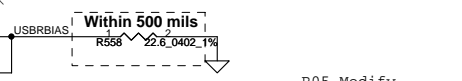
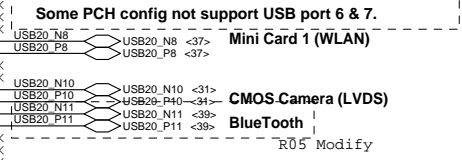
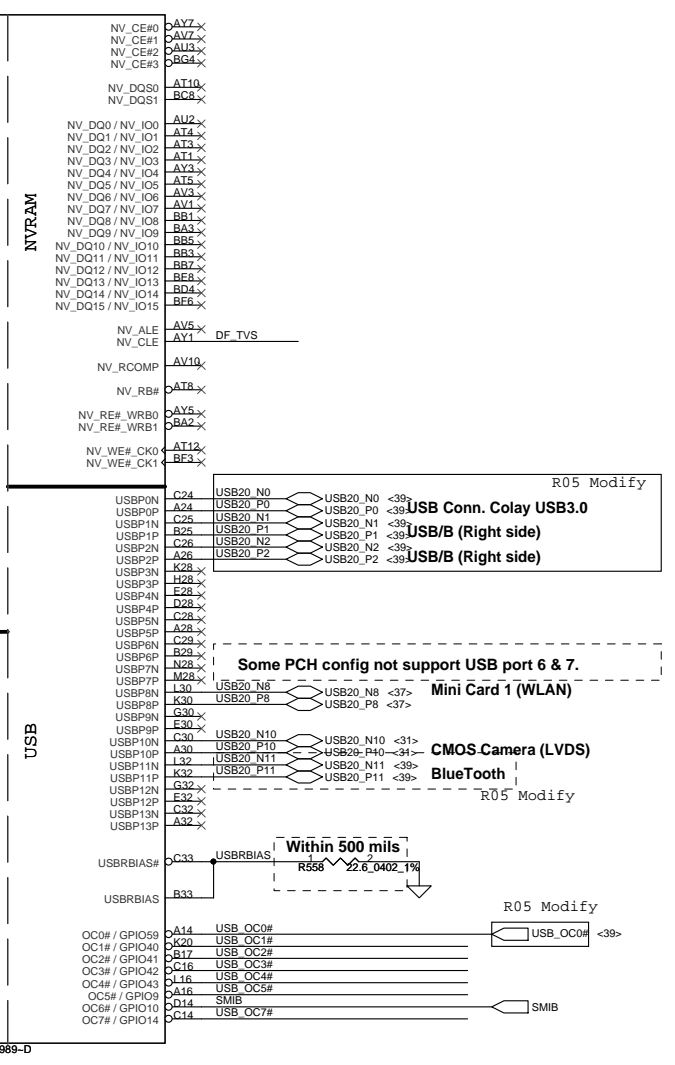
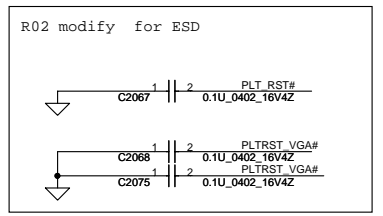
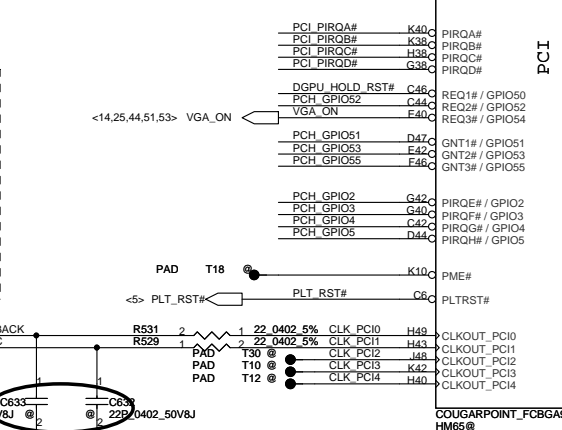
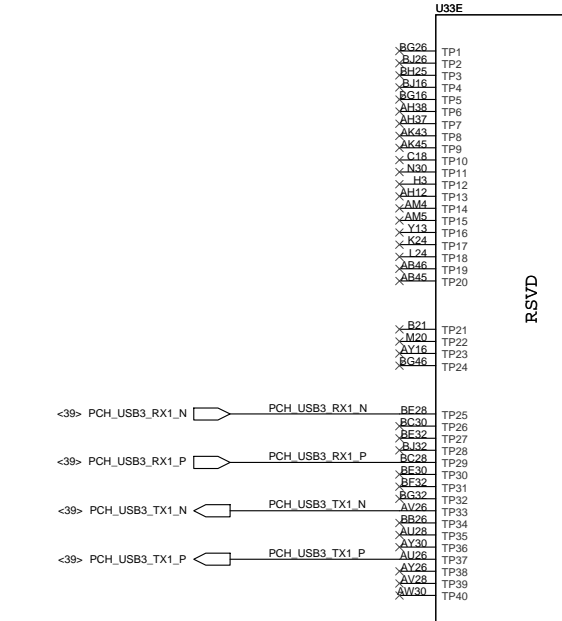
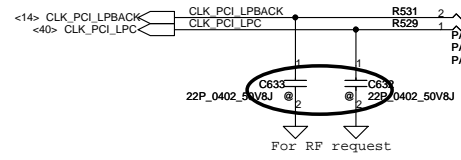


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GPIO51 Internal pull high

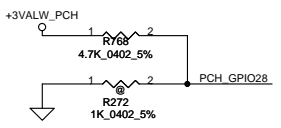
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	Bit11	Bit10	Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



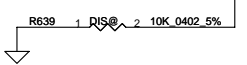
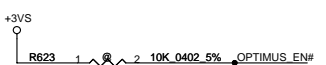
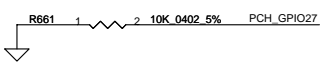
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Date:	Friday, January 06, 2012	Sheet	17	of 60

HDA_SYNC PH(PLL =+1.5VS)
 GPIO28
 On-Die PLL Voltage Regulator
 This signal has a weak internal pull up

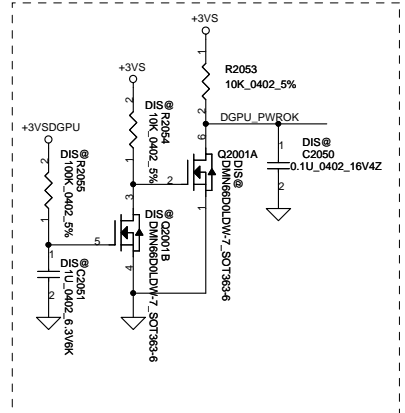
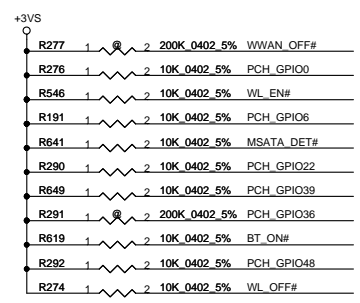
* H : On-Die voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



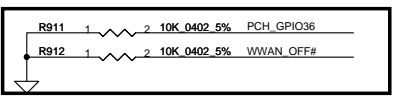
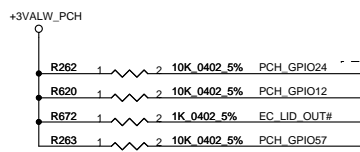
Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal
 No use PD to GND Check list1.0 P.70



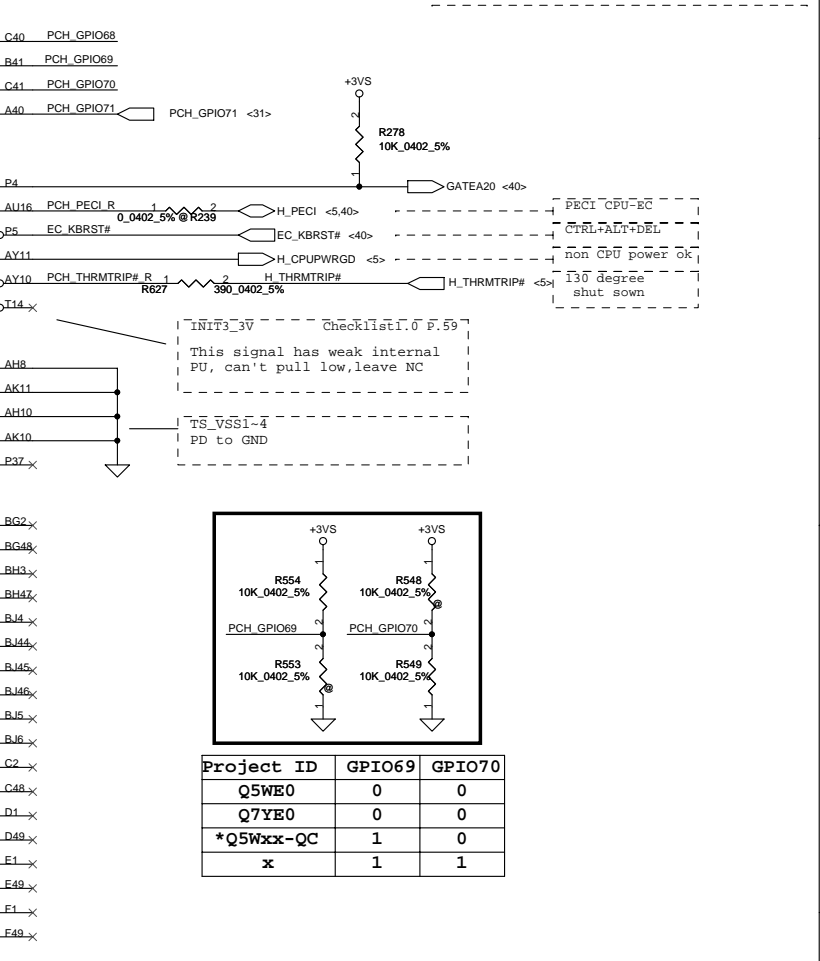
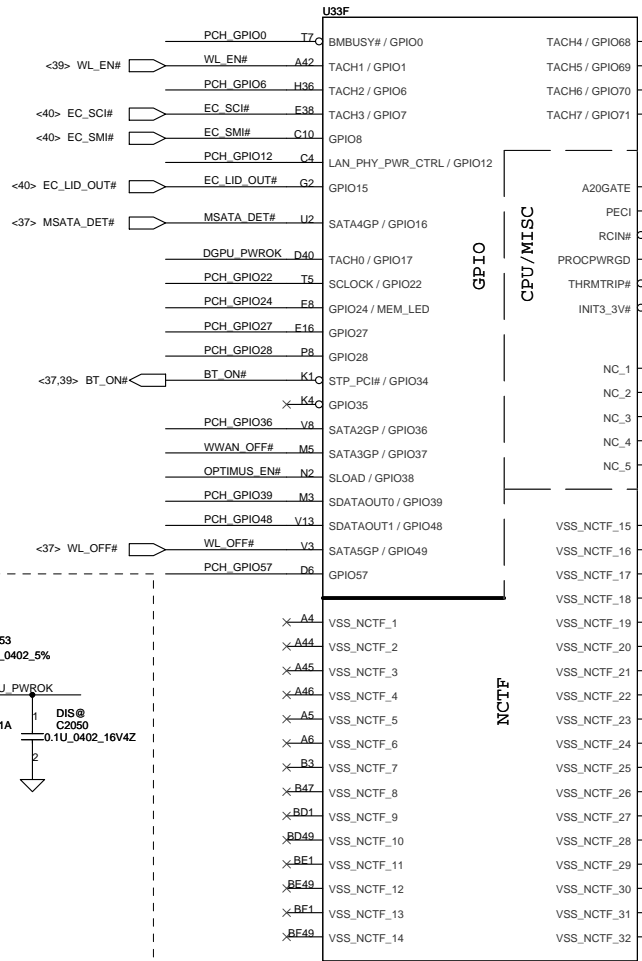
	GPIO38
	OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1



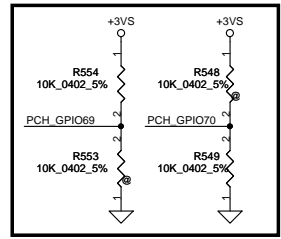
GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration register bits are not cleared by CP9h reset event.
 CRB1.0 PH10K to +3VALW



GPIO36/GPIO37 is Strap functionality that requires internal pull down to be sampled at rising PWROK. When uses as SATA2GP/SATA3GP for mechanical presence detect -use an external pull up 150K-200K ohm to Vcc3_3
 When used as GP input -ensure GPI is not driven high during strap sampling window
 When Unused as GPIO or SATA*GP -use 8.2K-10K pull-down
 check list page 47



INIT3_3V Check list 1.0 P.59
 This signal has weak internal PU, can't pull low, leave NC
 TS_VSS1-4 PD to GND



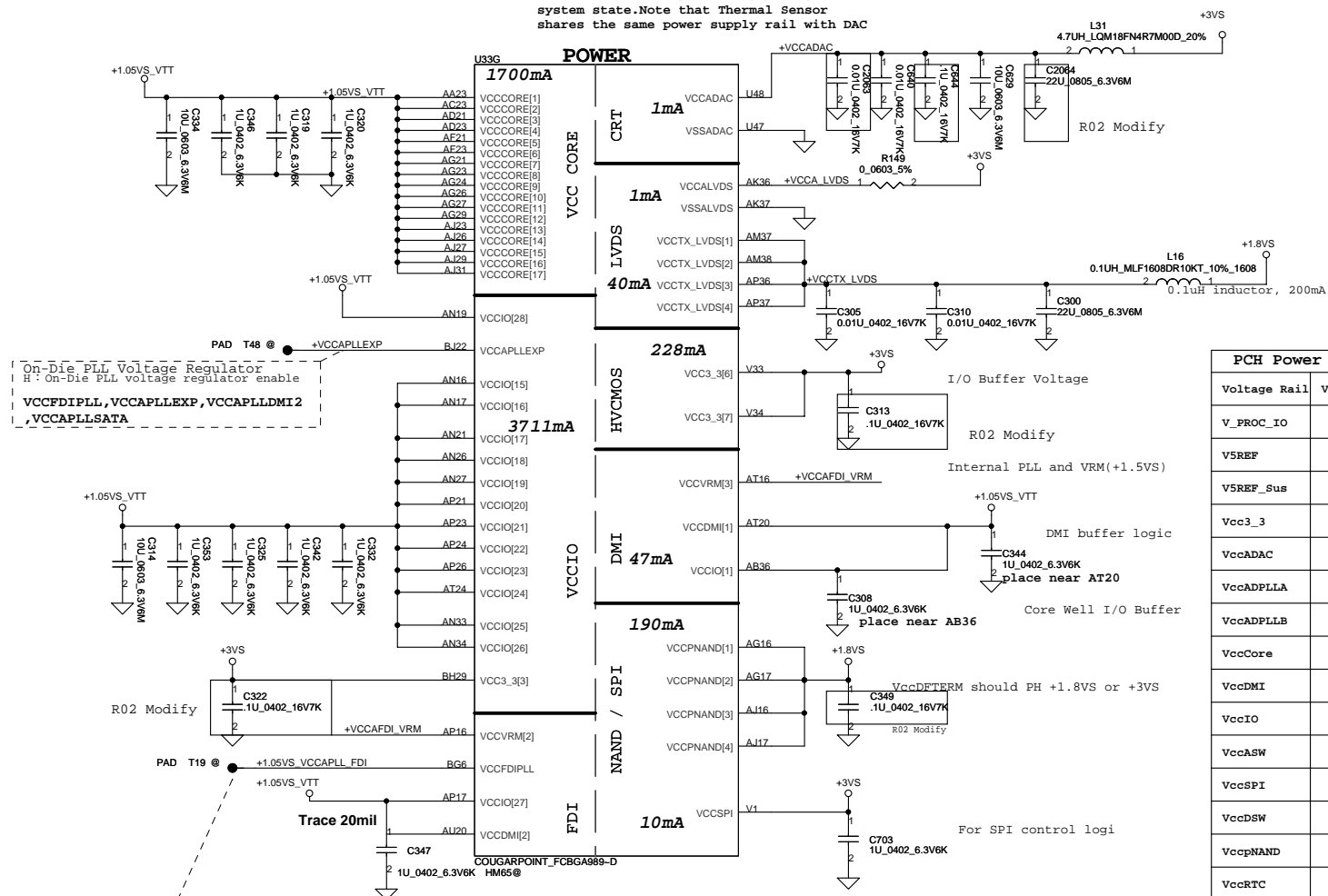
Project ID	GPIO69	GPIO70
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

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+VCCADAC should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC



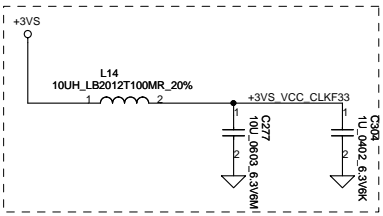
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

GPIO28
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2

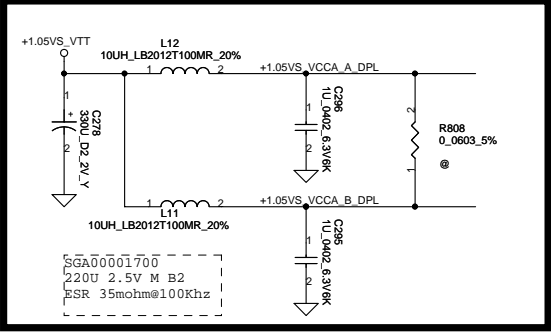
+1.5VS
R257 0.0603 5% +VCCAFDI_VRM
+VCCAFDI_VRM

VCCVRM=>1.5V FOR MOBILE
VCCVRM=>1.8V FOR DESKTOP
VCCVRM = 160mA dotal waiting for newest spec
HDA_SYNC PH(PLL =+1.5VS)

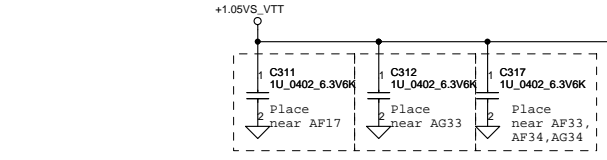
PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)



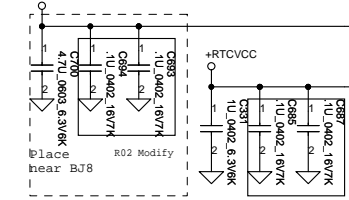
GPI028
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA



SGA0001700
220U 2.5V M B2
ESR 35mohm@100Khz

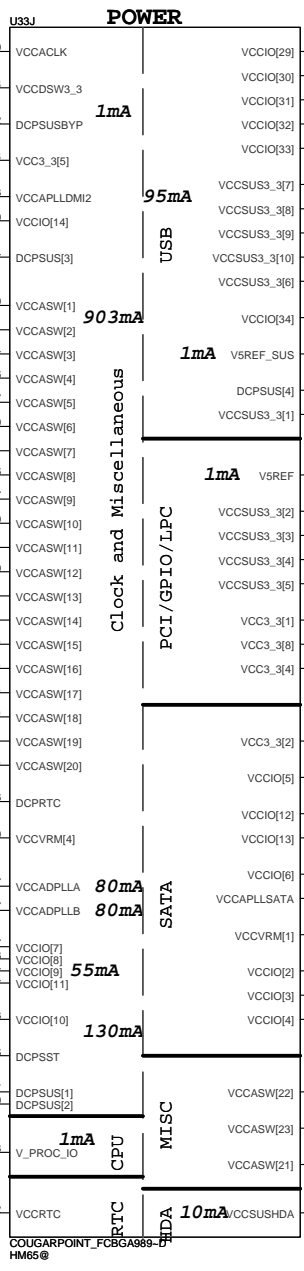
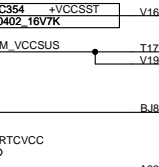
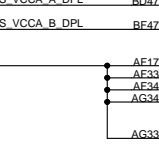
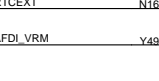
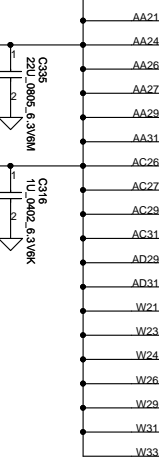
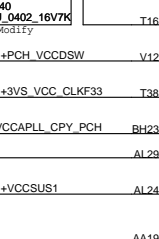


supplied by internal 1.05V VR Must NC



POWER

Have internal VRM



POWER

1mA

95mA

1mA

903mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

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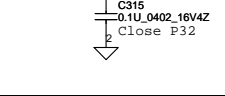
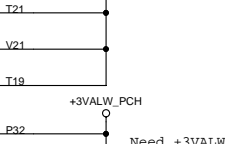
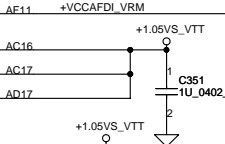
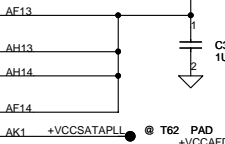
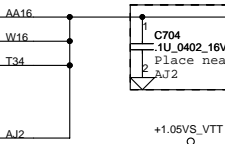
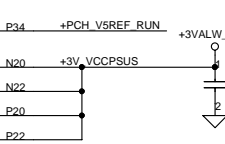
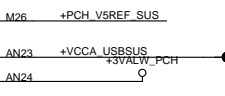
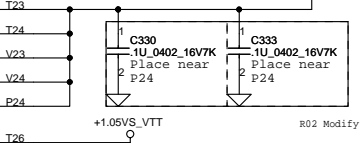
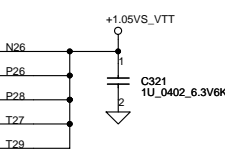
1mA

1mA

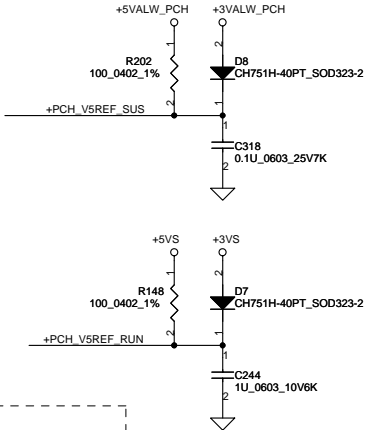
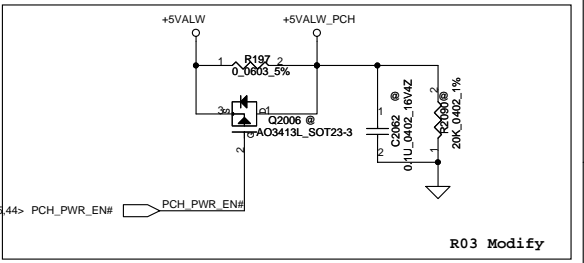
1mA

1mA

1mA

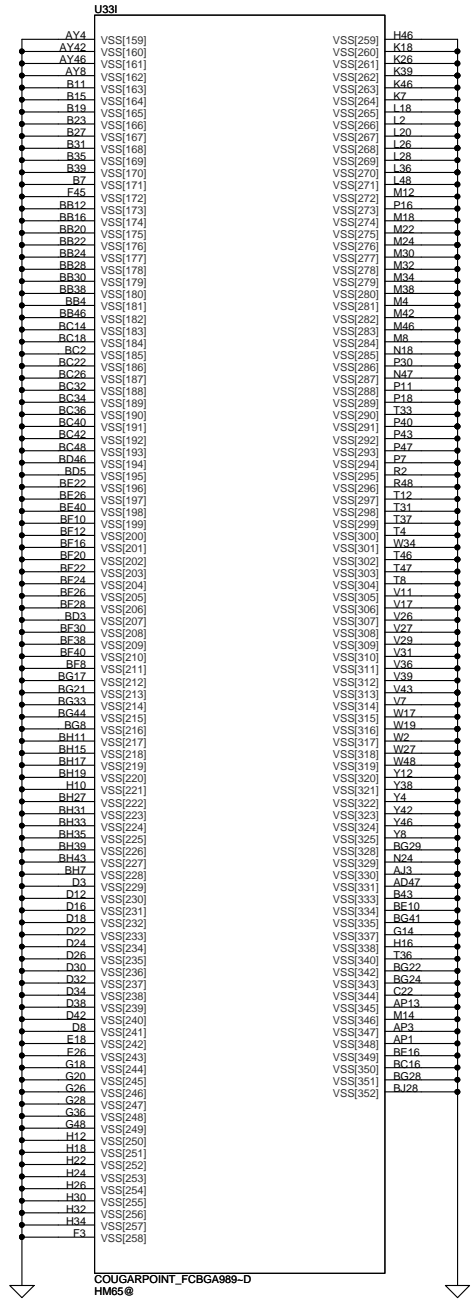
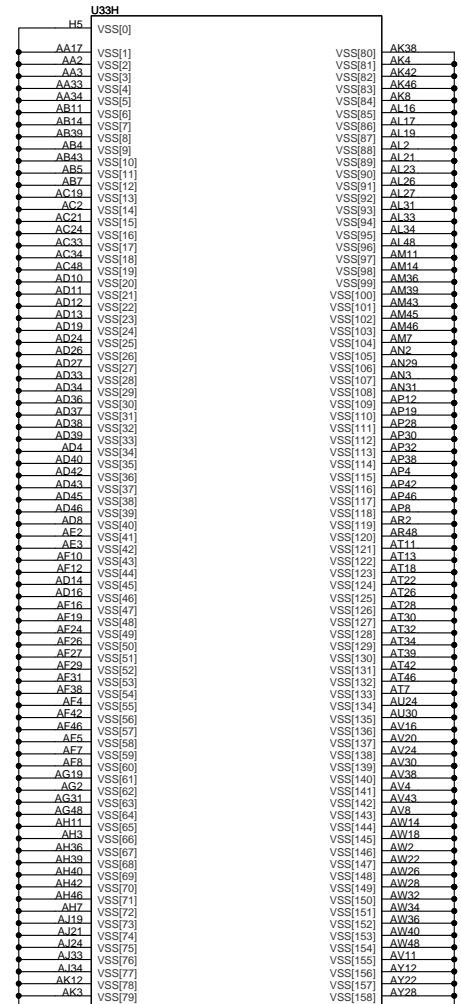


VCC3_3 = 266mA detail waiting for newest spec
VCCDMI = 42mA detail waiting for newest spec
+5VALW TO +5VALW_PCH(PCH AUX Power)

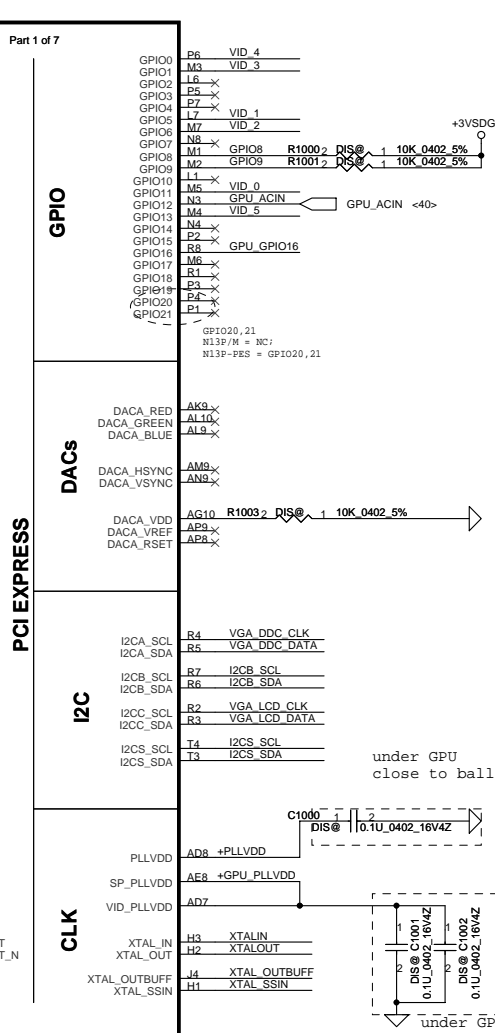
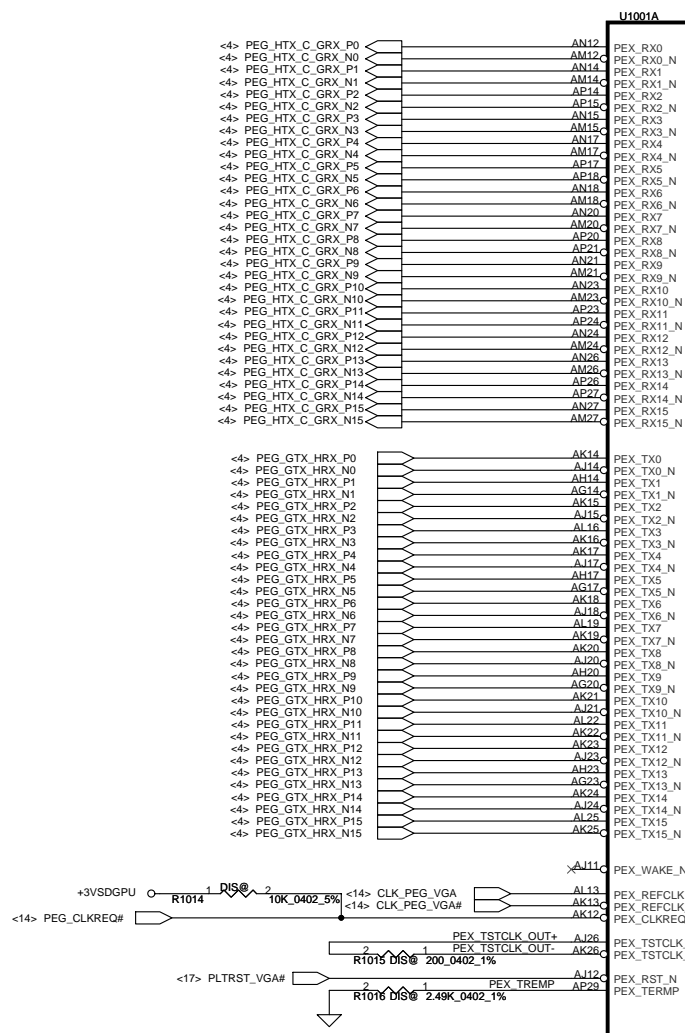


GPI028
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

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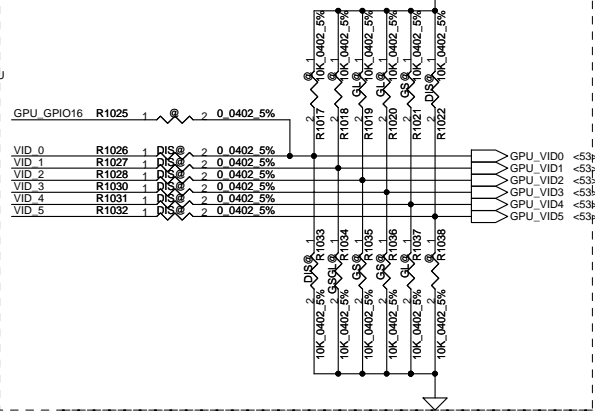


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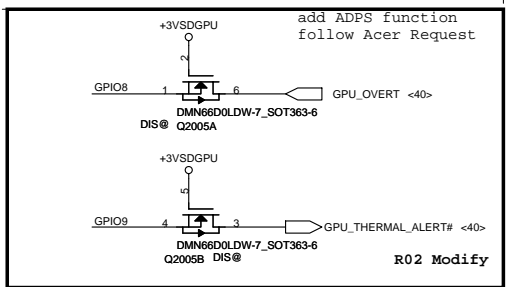


04/06 : Add 6bit VID Function.

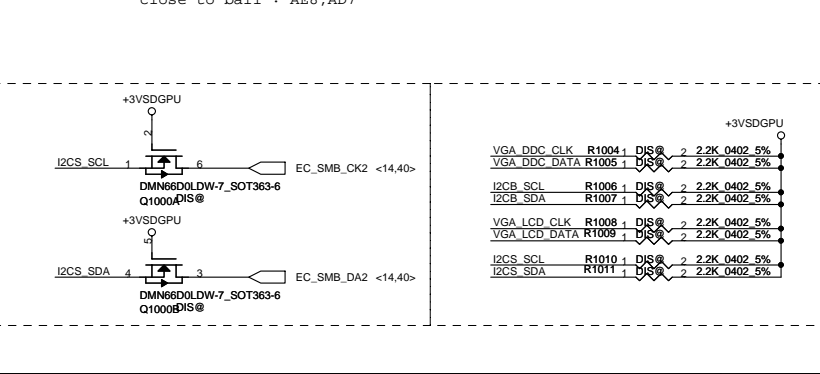
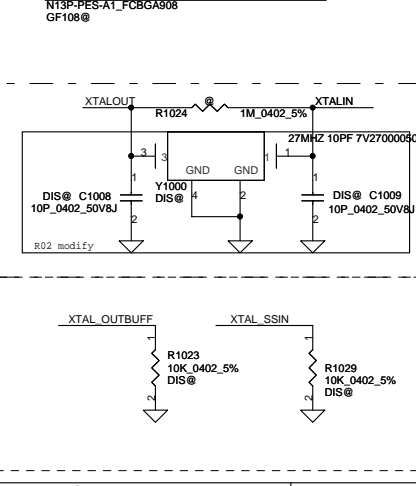
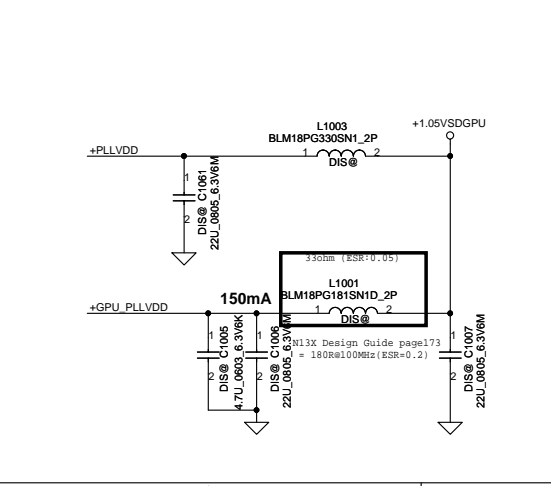
for GS4, the boot voltage is 0.975V
for GV4, the boot voltage is 0.85V



R02 Modify
EC control ACIN



GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		



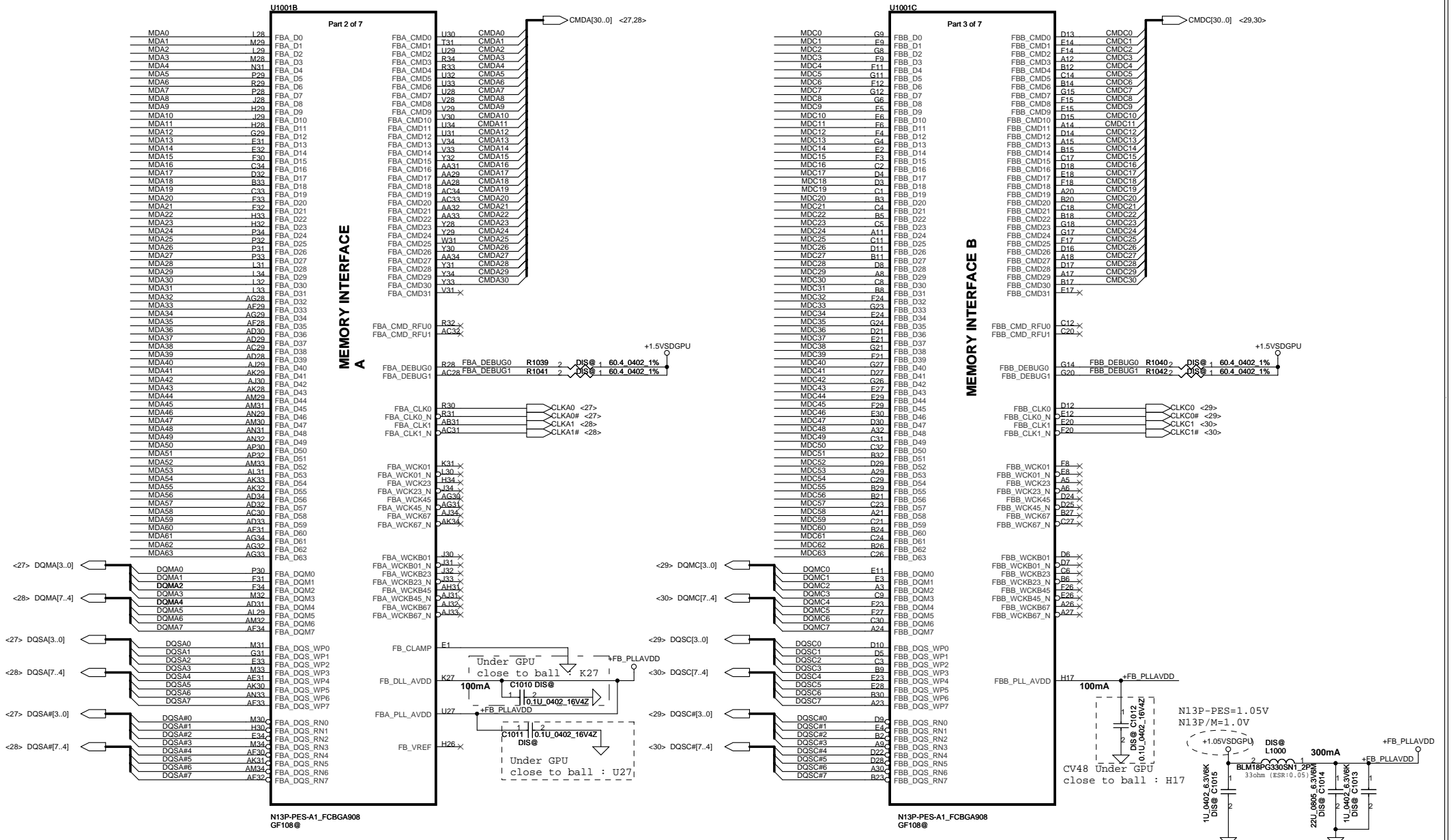
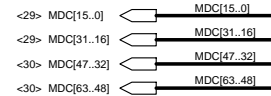
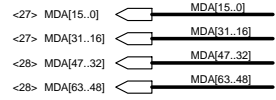
U1001
N13P-GS-A2 FCBGA 908P
GS@
SA000051880

U1001
N13P-GL-A1 FCBGA 908P
GL@
SA000051A00

U1001
N13M-GS FCBGA 908P
GM@
SA000057F20

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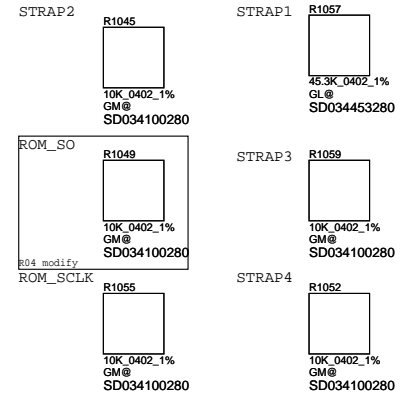
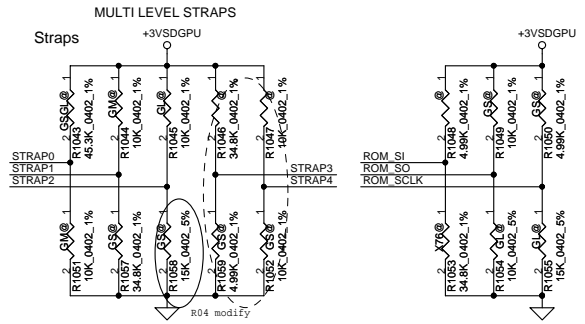
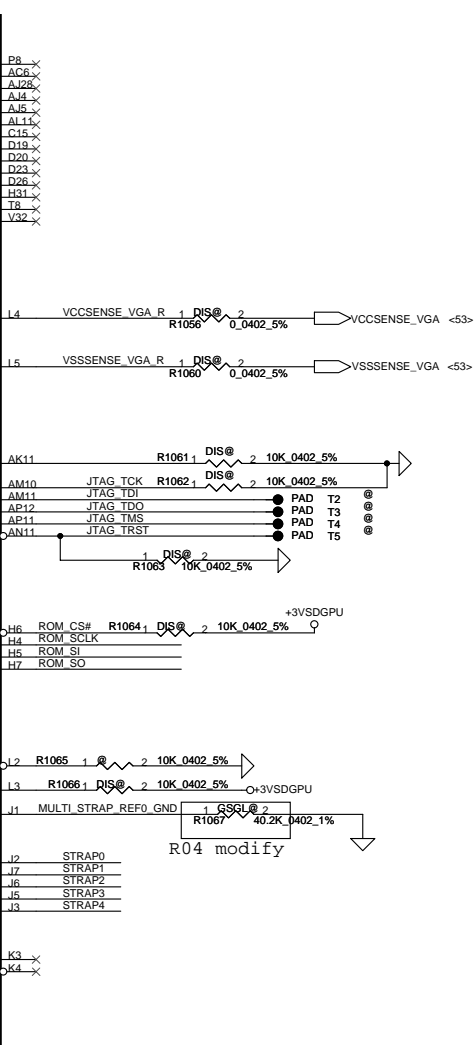
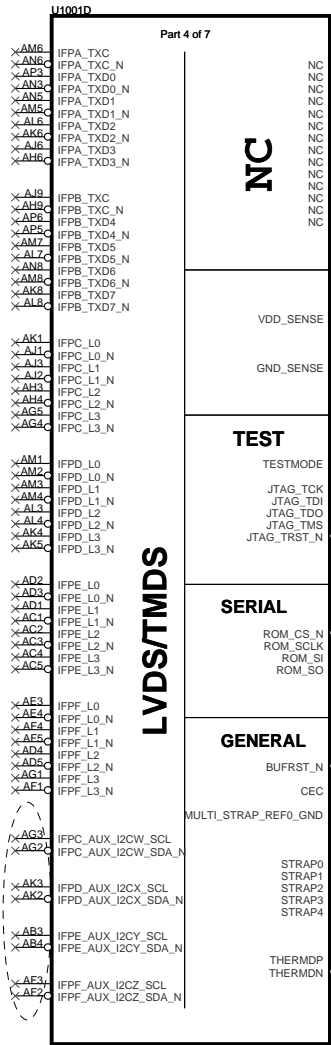
VRAM Interface



N13P-PES-A1_FCBGA908 GF108@

N13P-PES-A1_FCBGA908 GF108@

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For N13P-GS(ES) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 35K	R PD 15K	R PD 5K	R PD 10K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 35K	R PD 15K	R PD 5K	R PD 10K	R PD 15K	R PU 10K	R PU 5K

For N13P-GL(QS) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

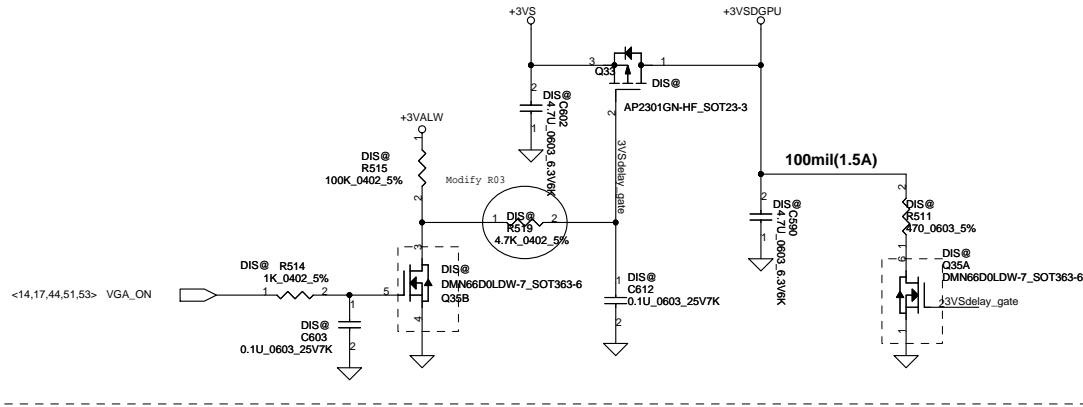
For N13M-GS(QS) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PU 10K	R PD 10K

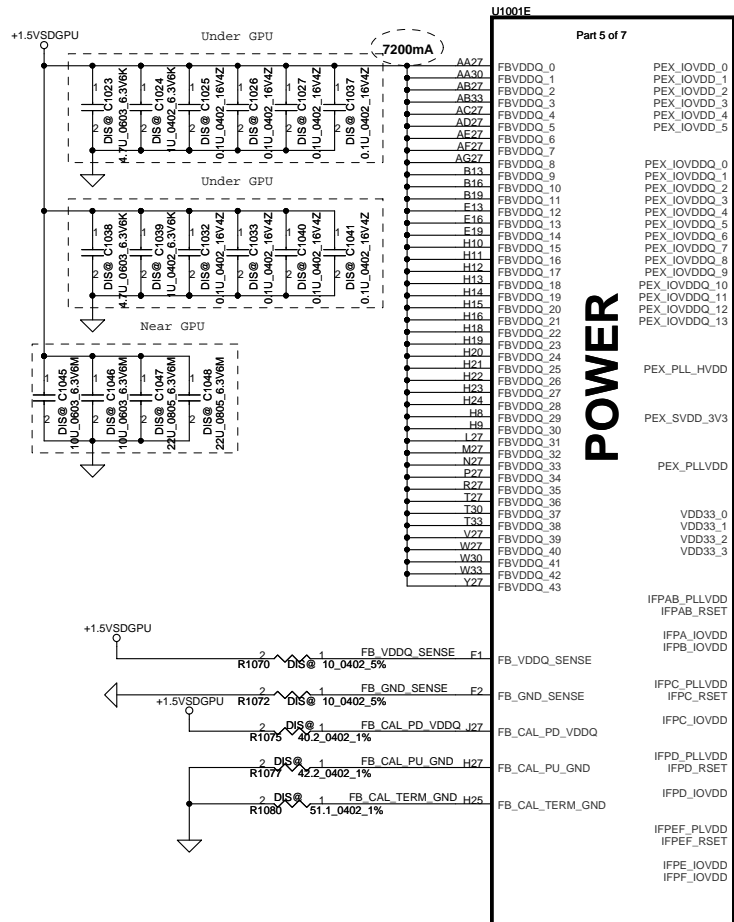
N13P-PES-A1_FCBGA908 GF108@

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				4019ID	B	
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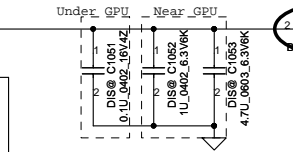
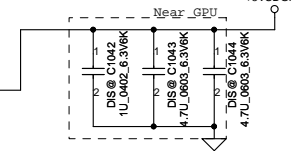
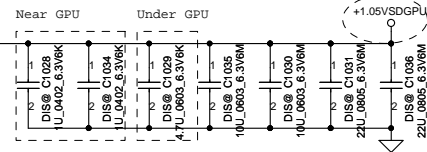
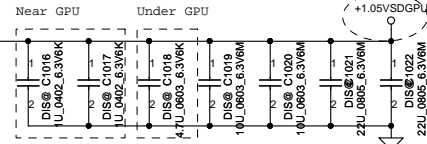
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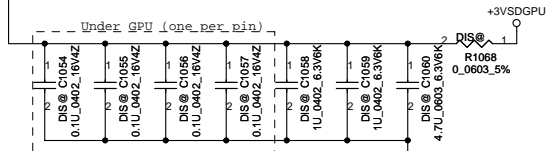
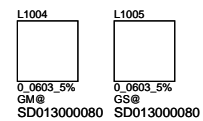
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N13P-PES-A1_FCBGA908
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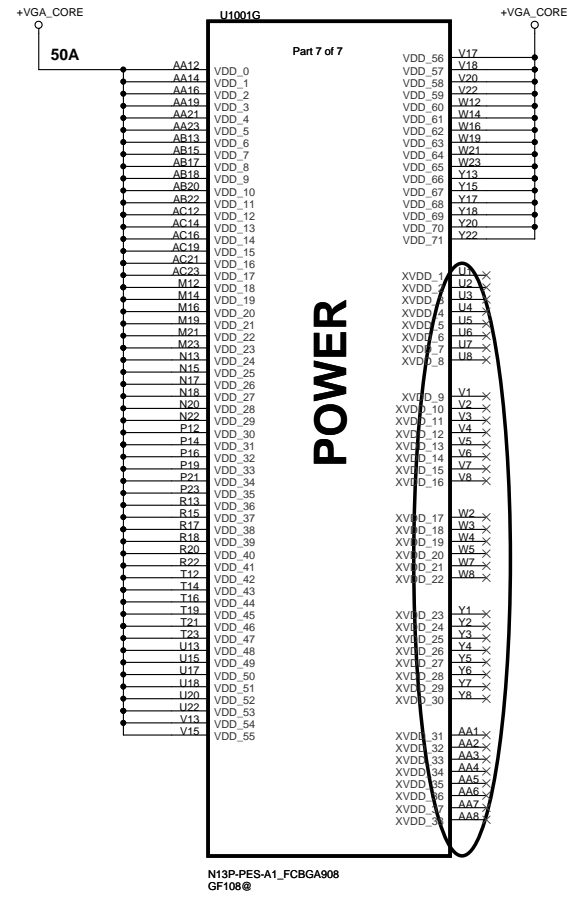
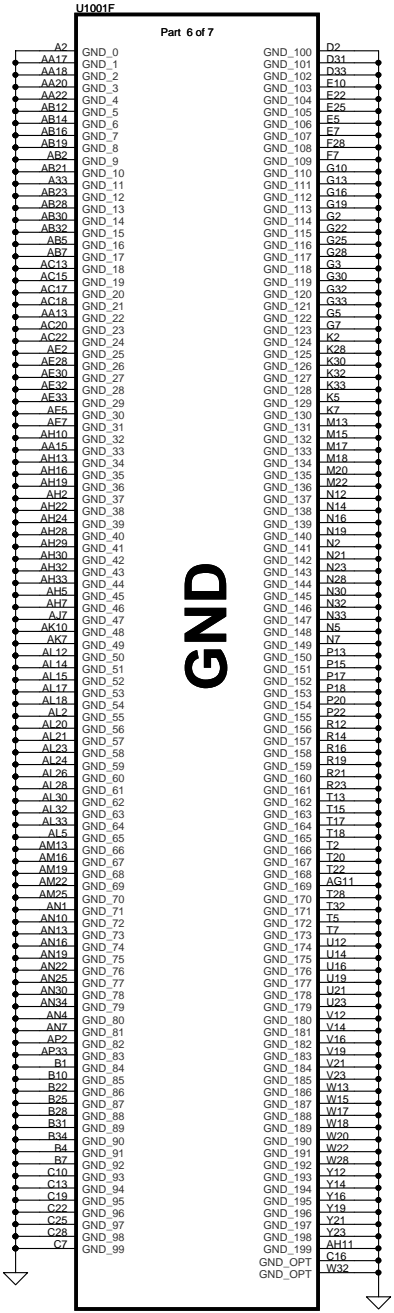


Reference Sch = 300R@100MHz
Design Guide page69 未定義



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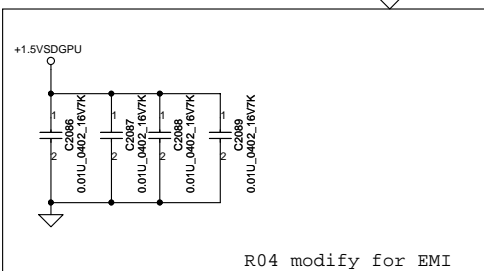
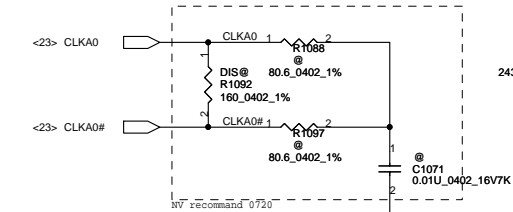
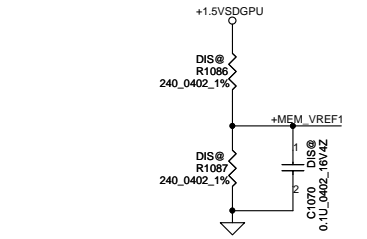
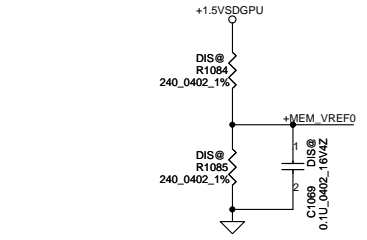
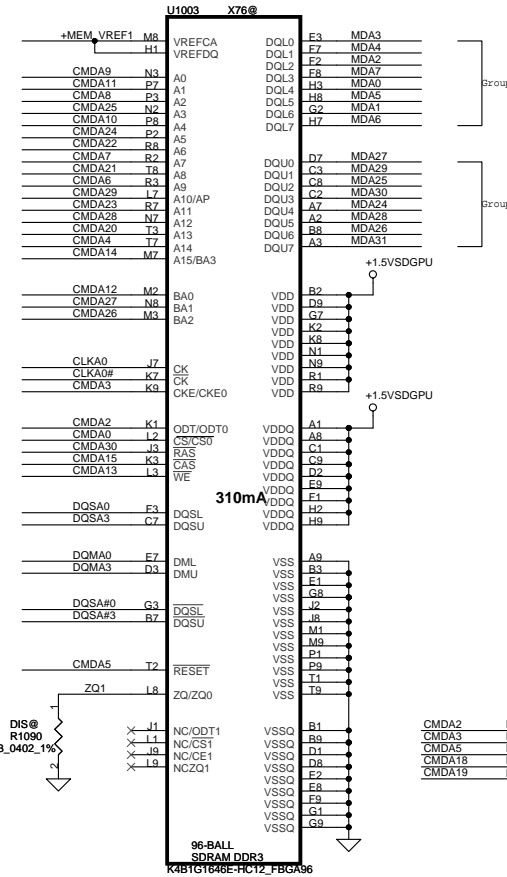
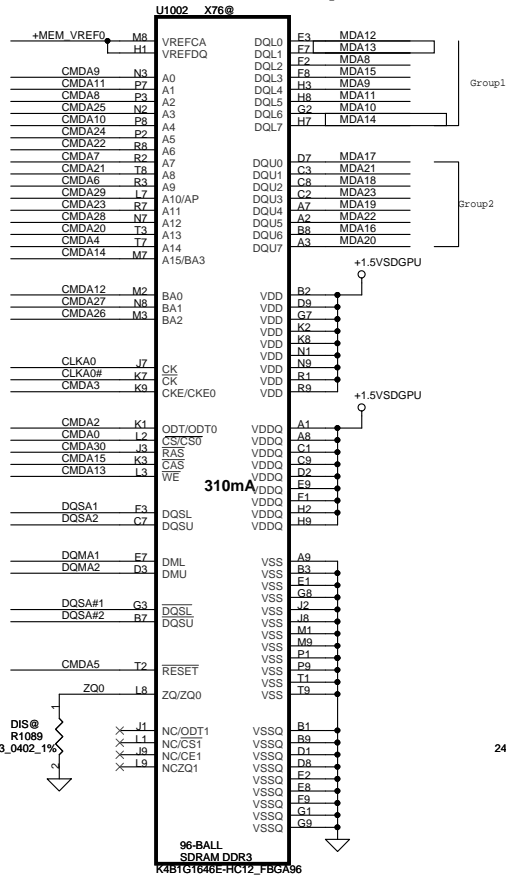
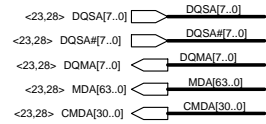
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VRAM DDR3 chips (1GB)

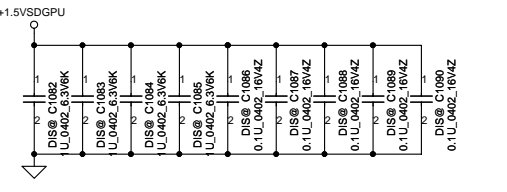
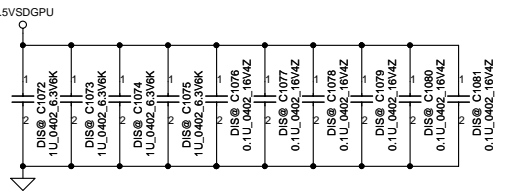
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

R02 modify
Swap MDA13 and MDA14



R04 modify for EMI



Command Bit	Default Pull-down
ODT#	10k
CKE	10k
RST	10k
CS*	No Termination

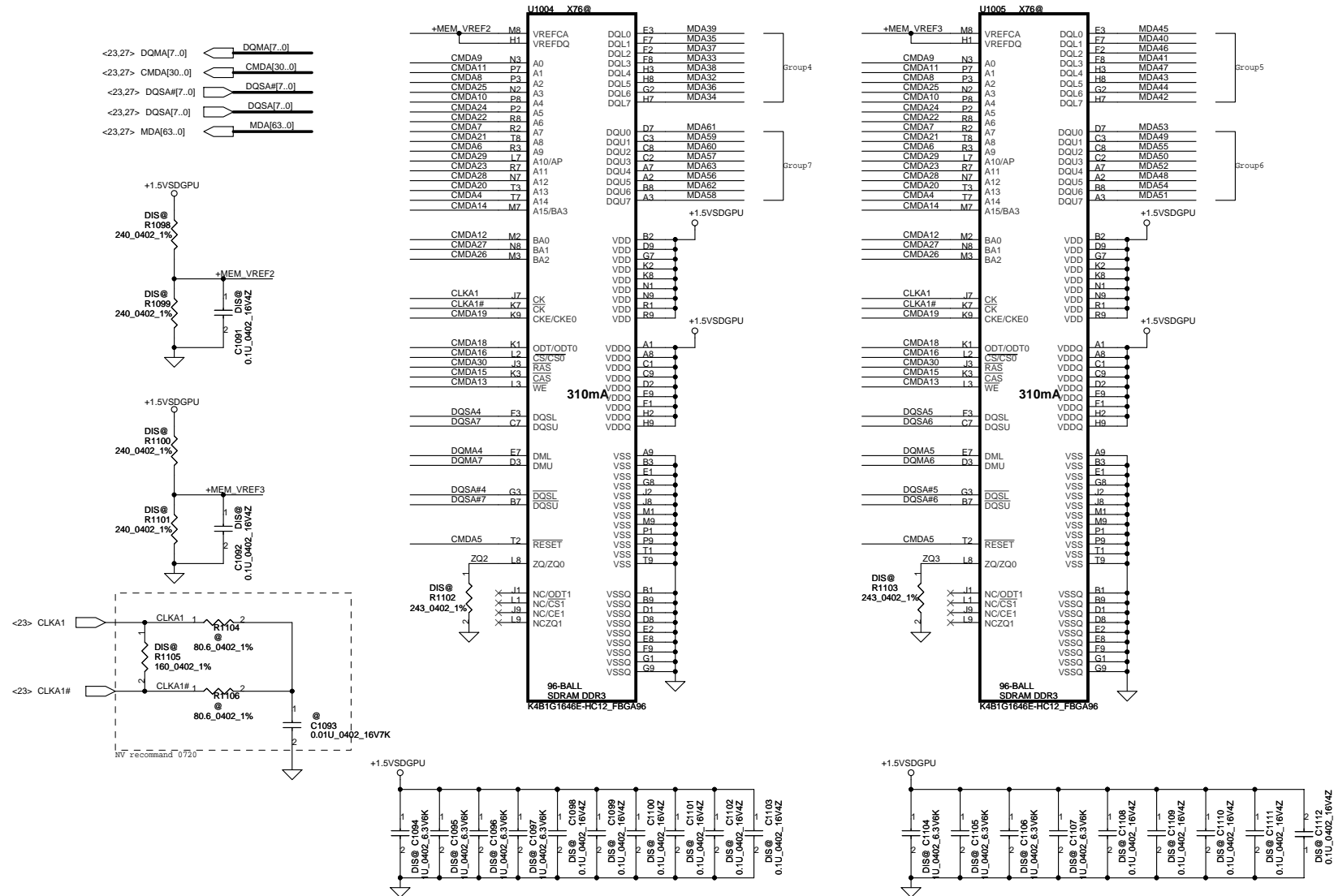
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Hynix : SA000032400 (S IC D3 64Mx16 H5TQ1G63BFR-12C FBGA 1.5V)

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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

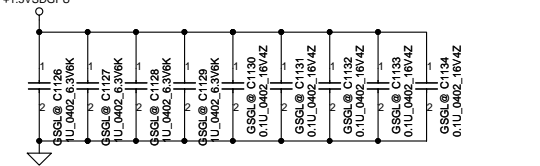
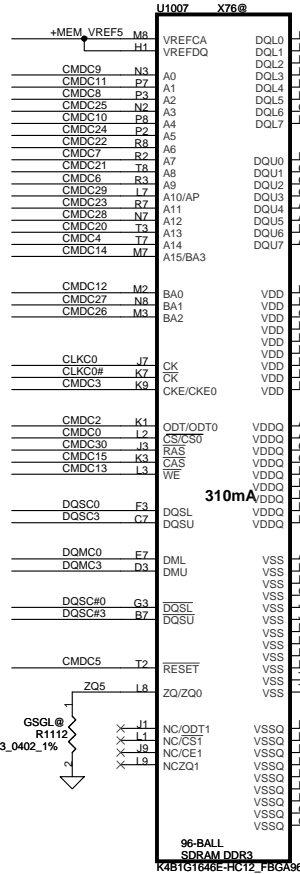
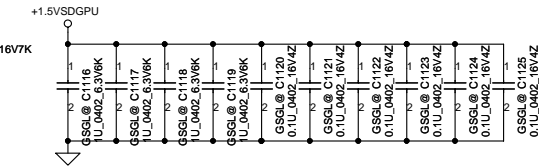
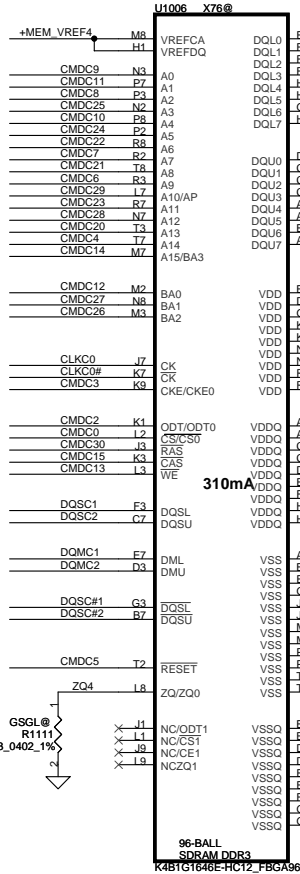
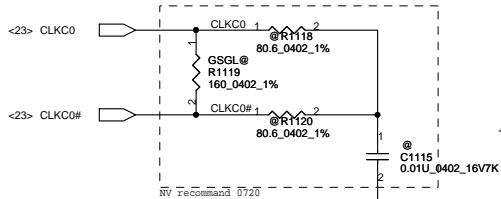
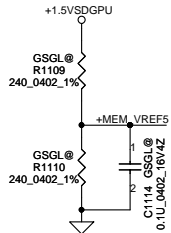
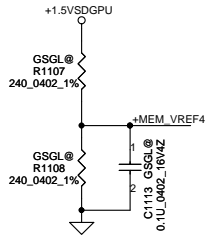
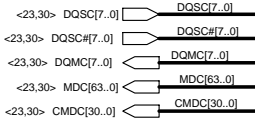
Not Available LOW HIGH

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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CAS*	No Termination
	CSD	

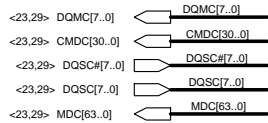
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SCHEMATIC, MB A7912	
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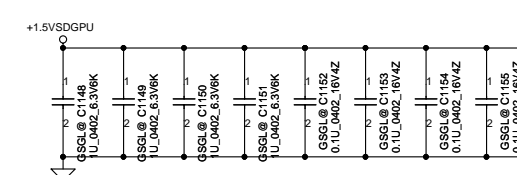
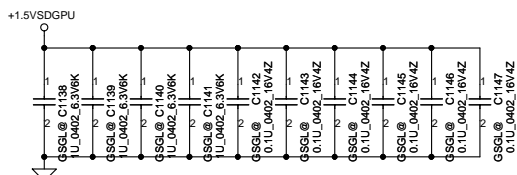
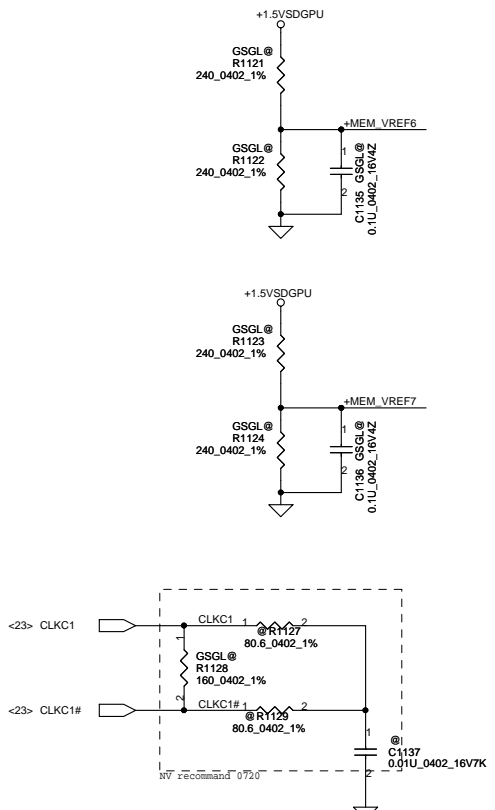
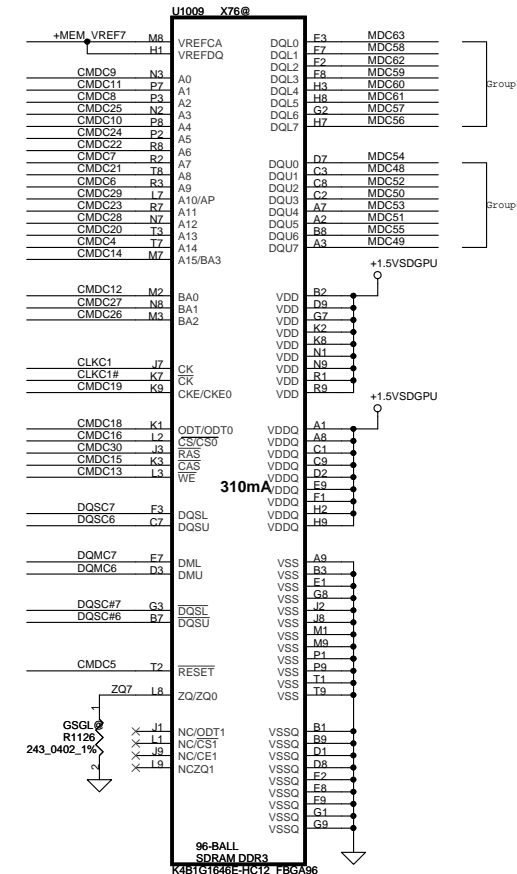
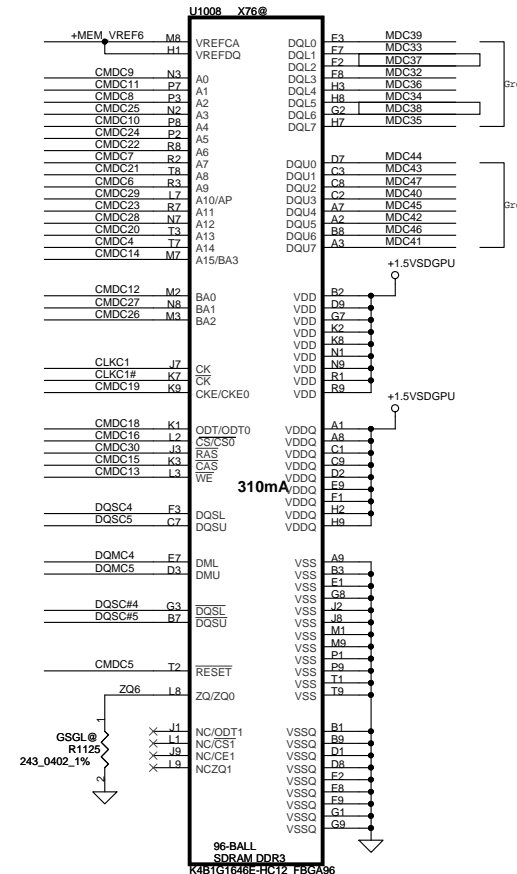
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



R02 modify
Swap MDC37 and MDC38

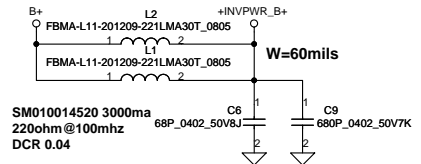
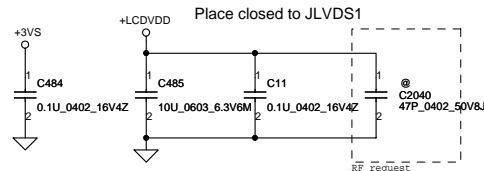
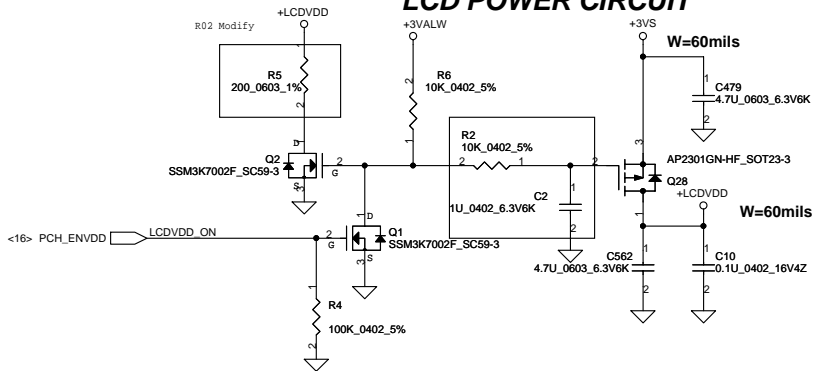


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

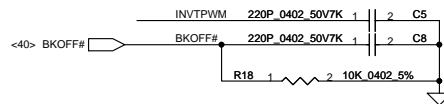
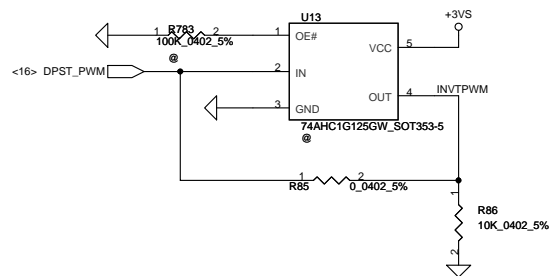
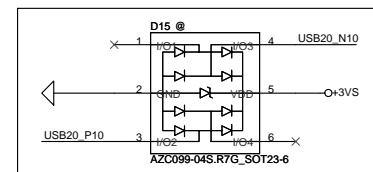
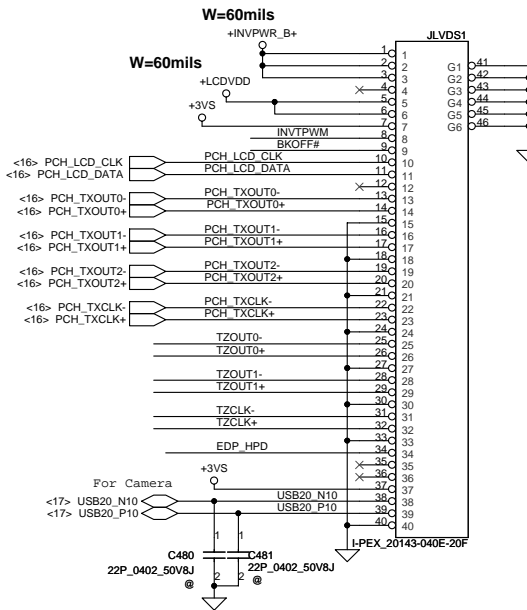
LOW HIGH

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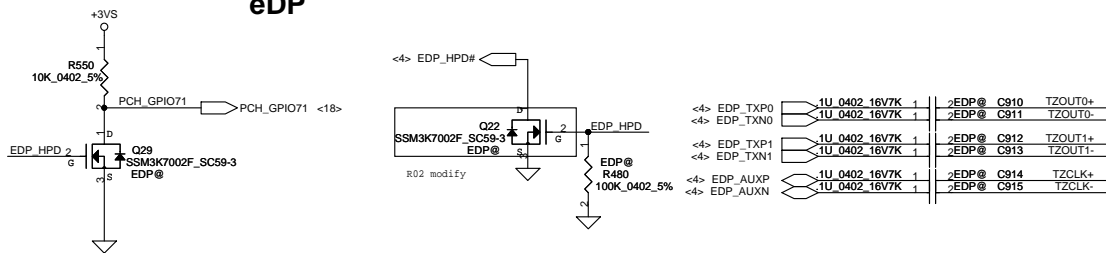
LCD POWER CIRCUIT



LCD/LED PANEL Conn.

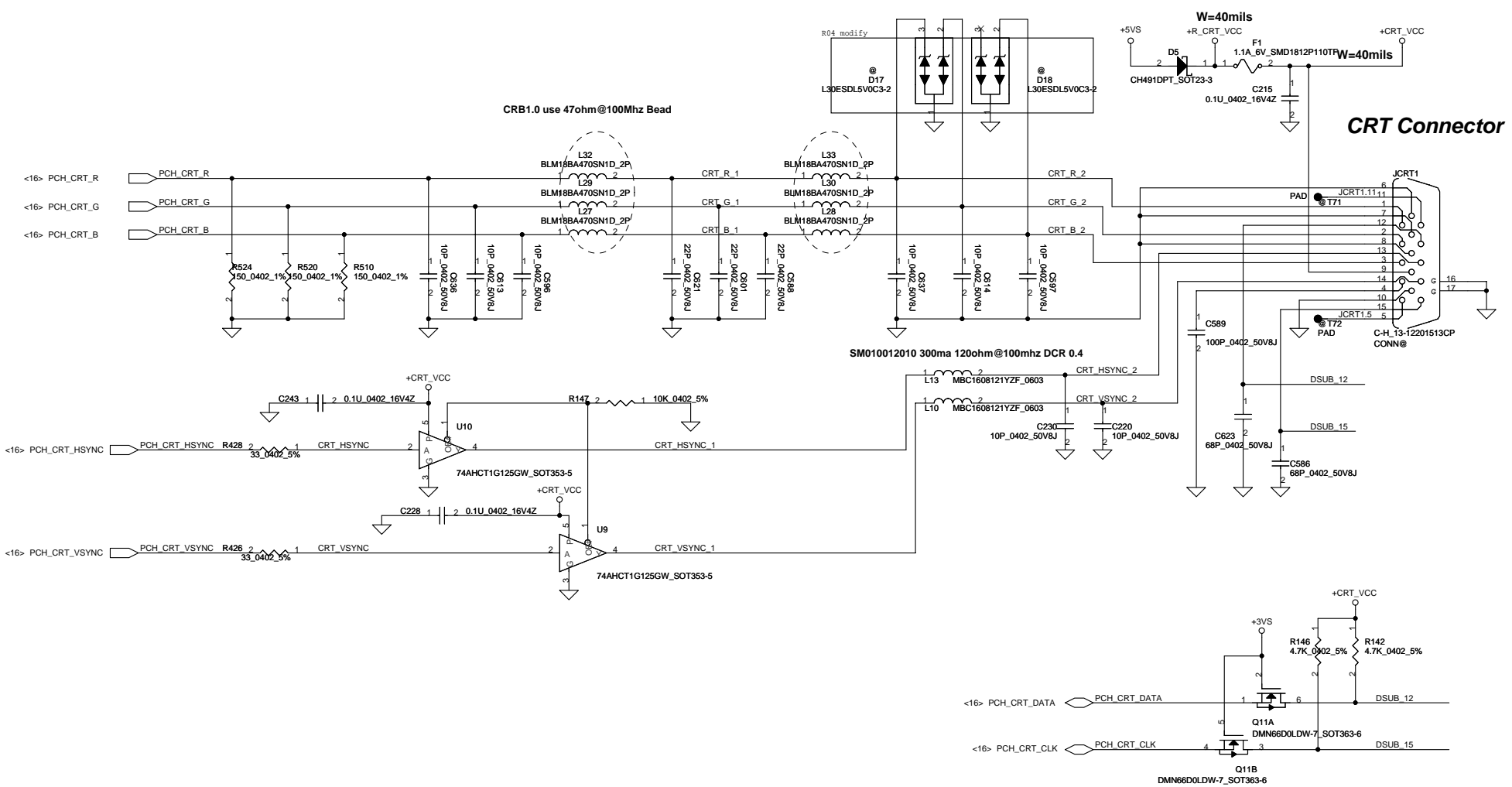


eDP

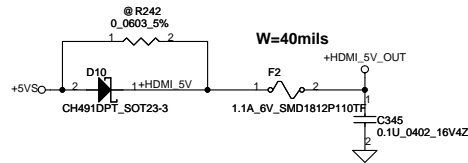


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<4> EDP_TXP1	1U 0402 16V7K	1	2	EDP@ C912	TZOUT1+
<4> EDP_TXN1	1U 0402 16V7K	1	2	EDP@ C913	TZOUT1-
<4> EDP_AUXP	1U 0402 16V7K	1	2	EDP@ C914	TZCLK+
<4> EDP_AUXN	1U 0402 16V7K	1	2	EDP@ C915	TZCLK-

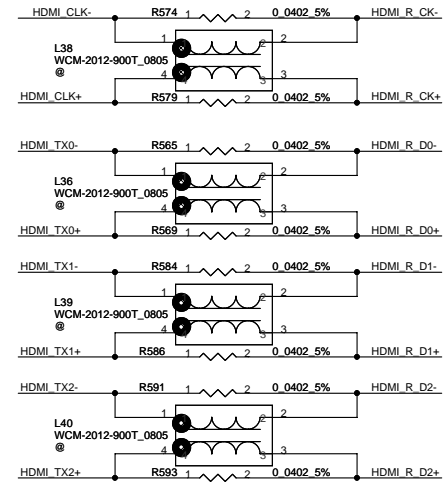
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	PCH_GPIO71
eDP	0
LVDS	1



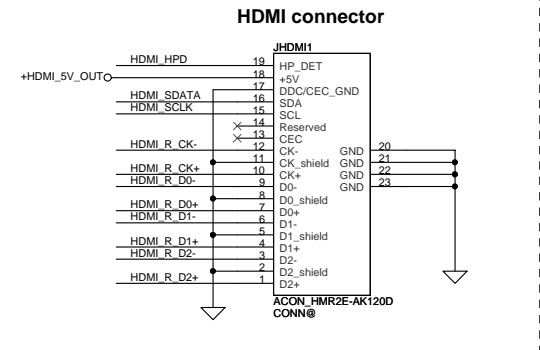
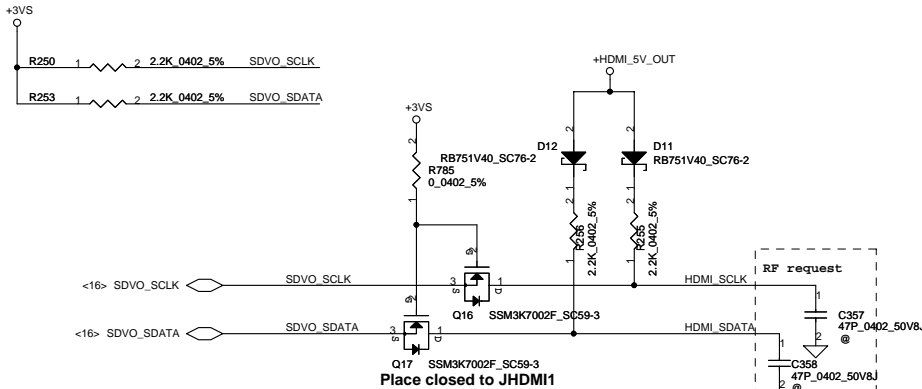
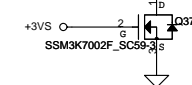
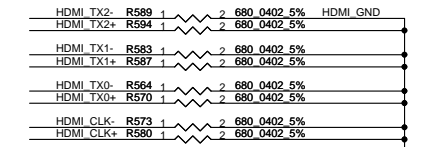
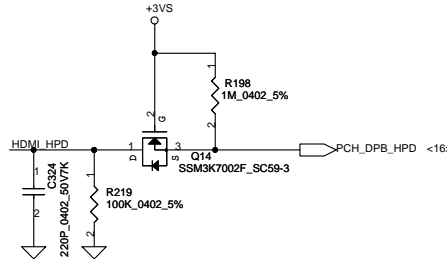
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SM070001310 400ma 90ohm@100mhz DCR 0.3



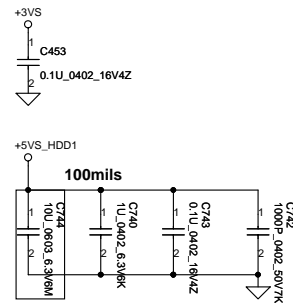
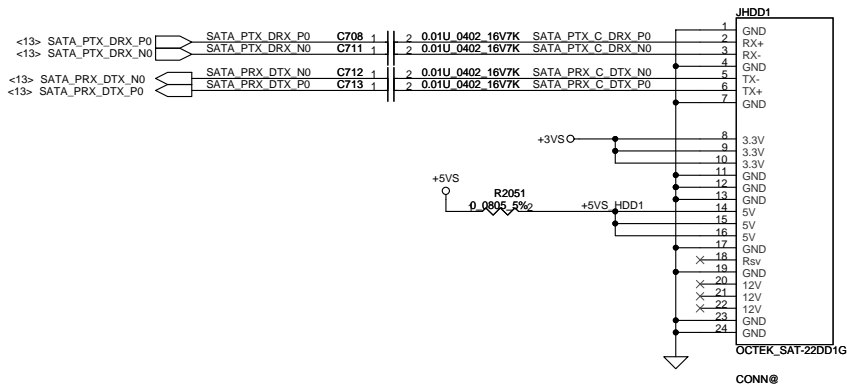
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Date:	Friday, January 06, 2012	Sheet	33	of	60

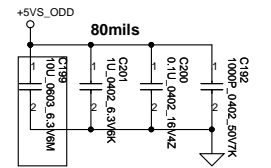
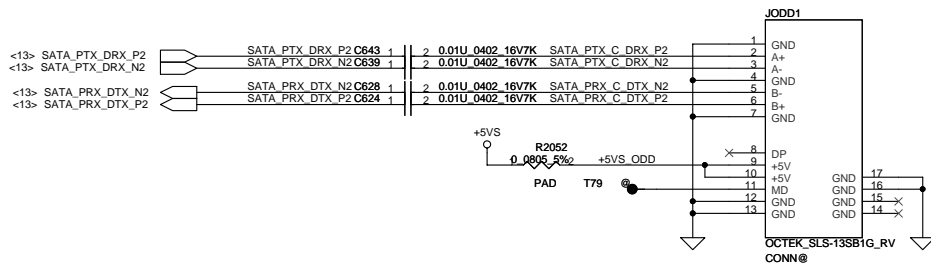
SATA HDD1 Conn.

CL 4.0 mm



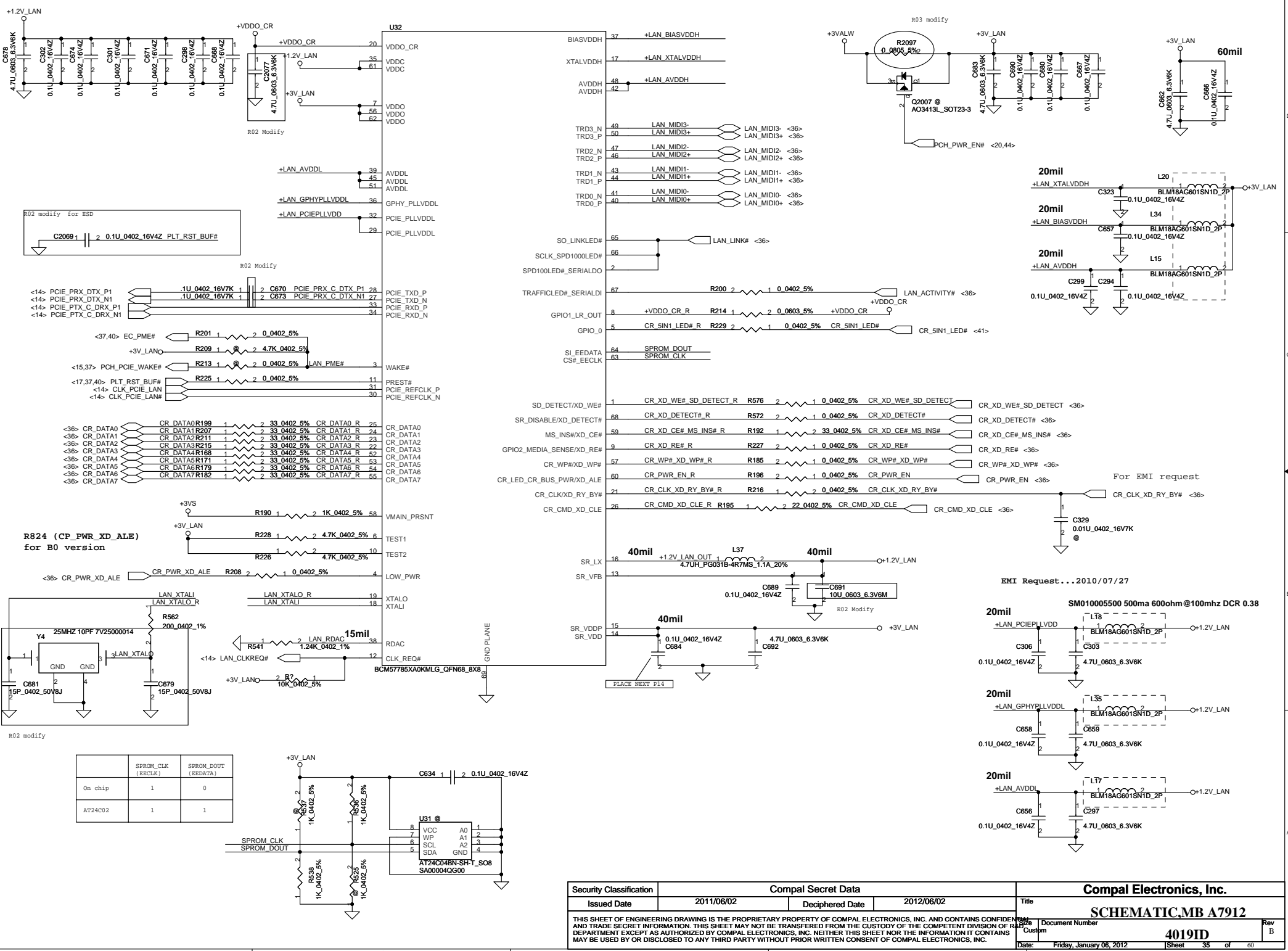
R02 Modify

SATA ODD Conn.



R02 Modify

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Issued Date	2011/06/02	Deciphered Date	2012/06/02	Title	Schematic, MB A7912	
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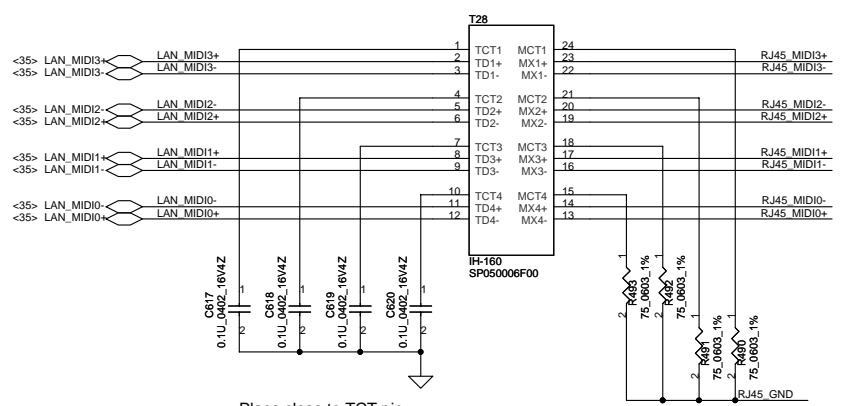
Compal Electronics, Inc.

Title **SCHEMATIC_MB A7912**

Document Number **4019ID**

Date: Friday, January 06, 2012 **Rev** B

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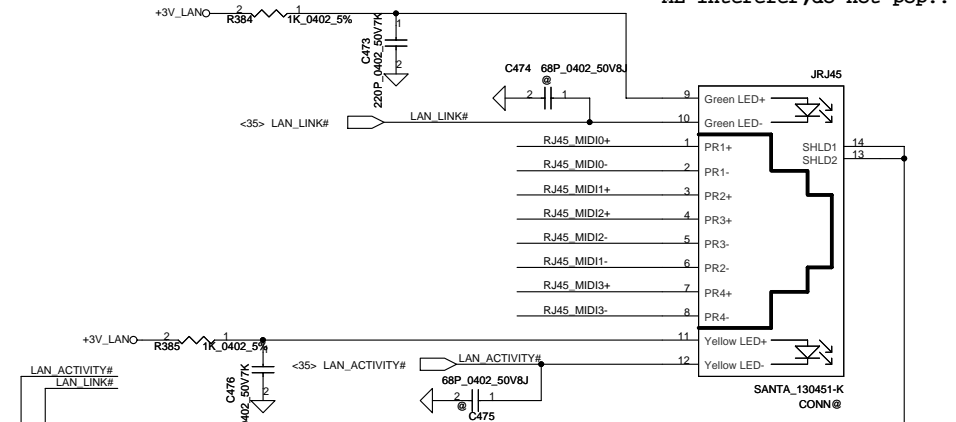


Place close to TCT pin

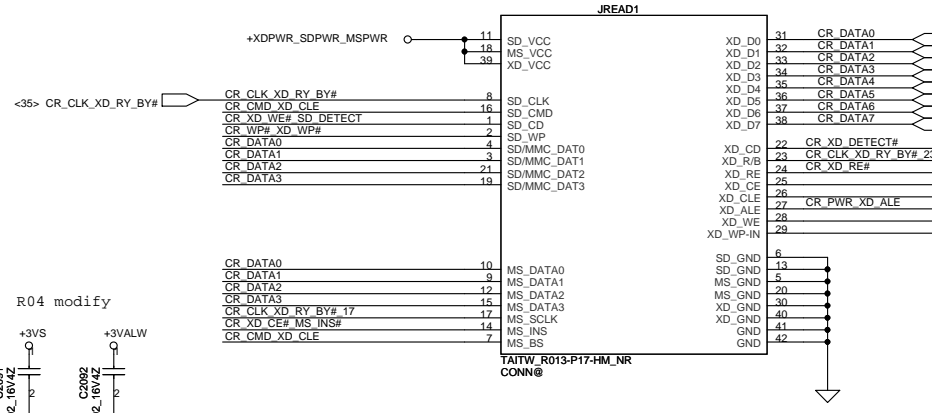
BOTH HAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_IH-160 LAN , SP050006F00

LAN Connector

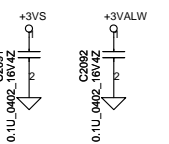
C474, C475 and D14
ME interfere, do not pop!!



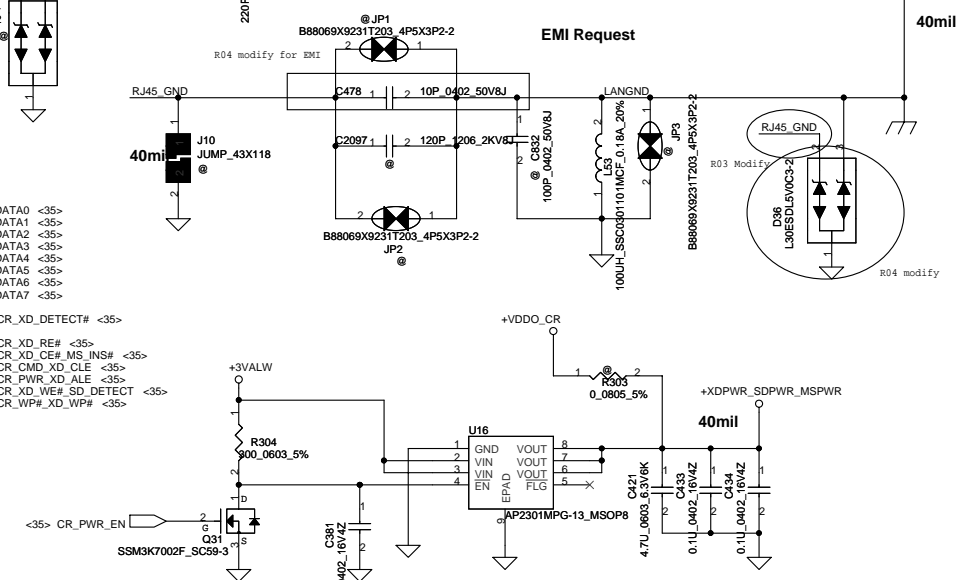
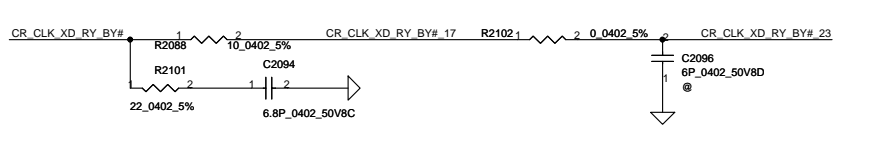
Card Reader Connector



R04 modify

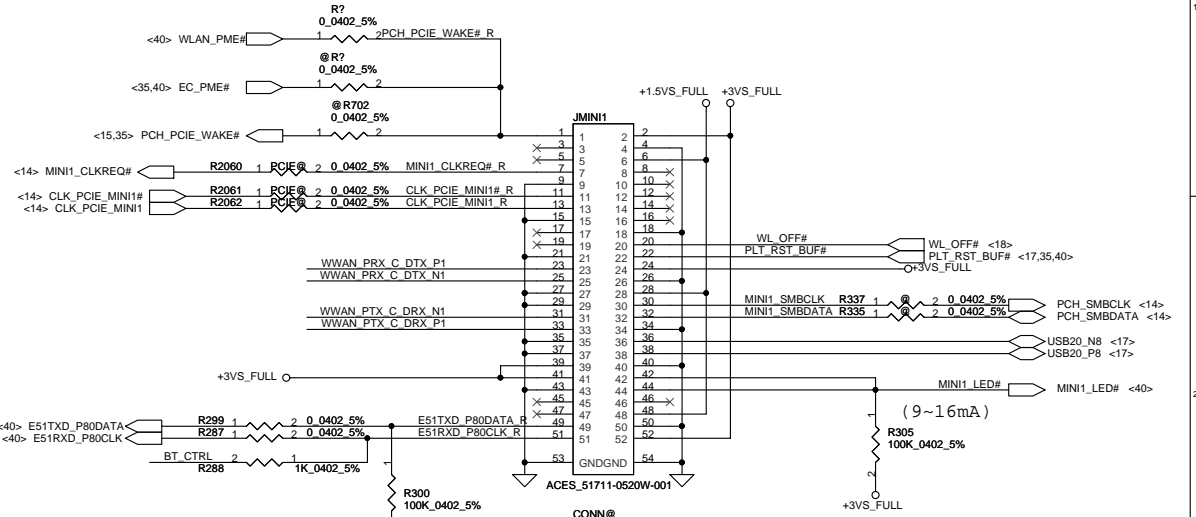
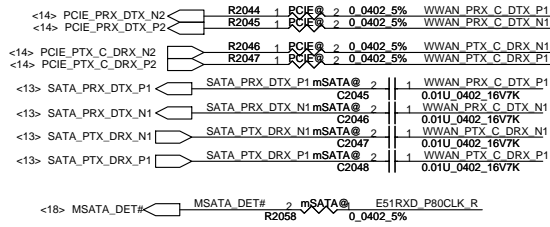
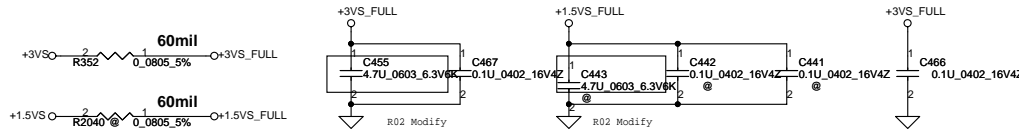


R02 modify for SD3.0 issue



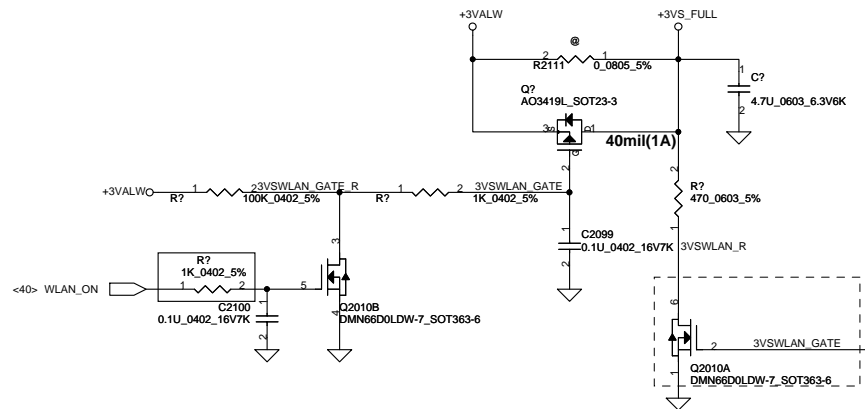
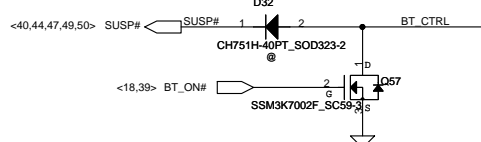
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Issued Date	2011/06/02	Deciphered Date	2012/06/02	Title
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				Rev B
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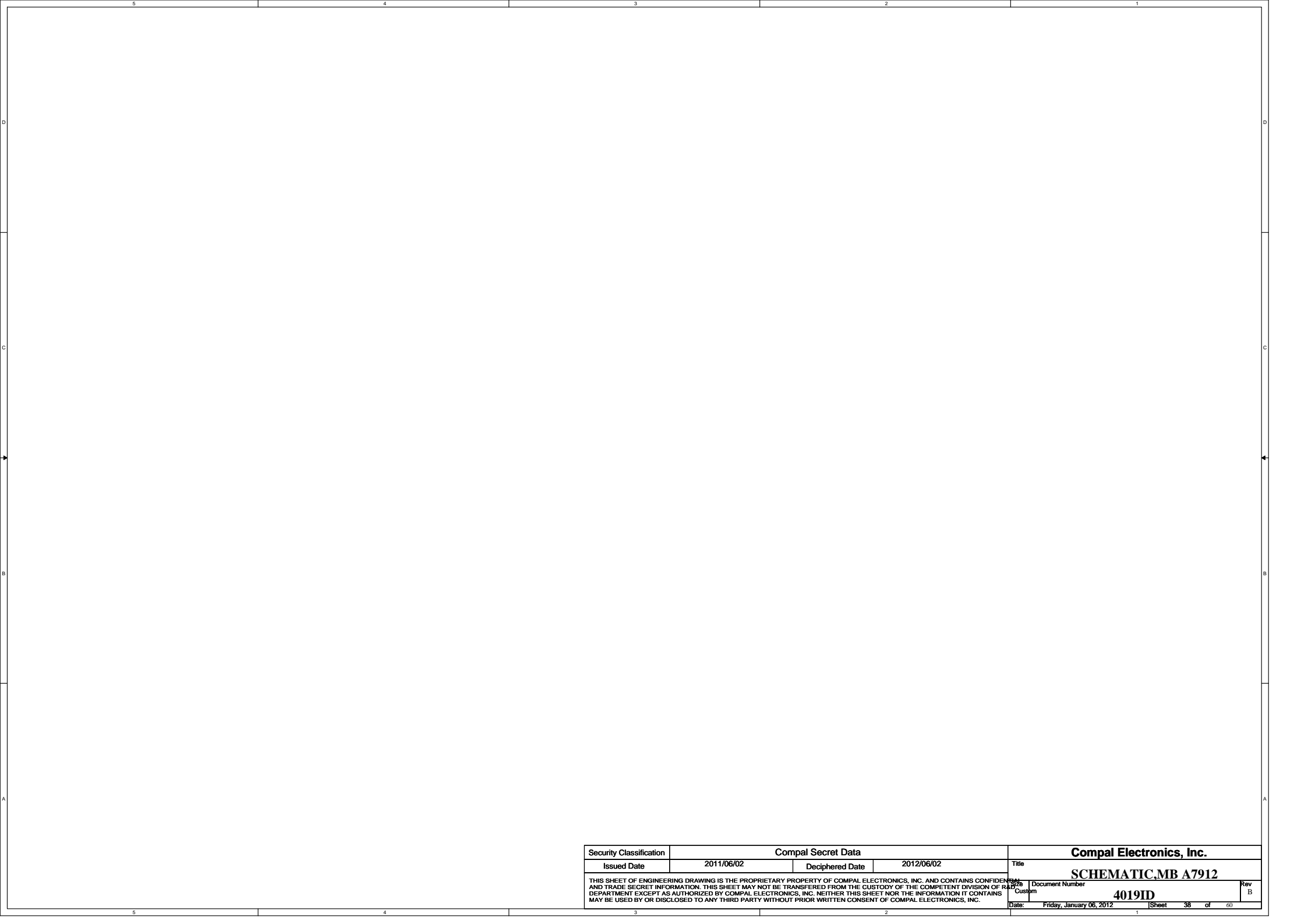
For Wireless LAN or MSATA



WLAN&BT Combo module circuits

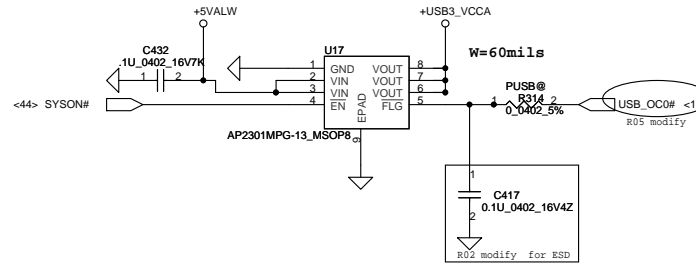
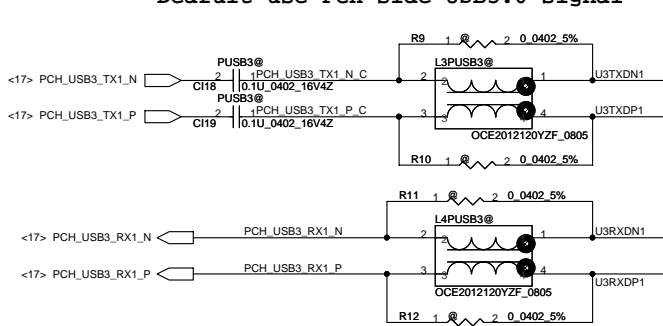
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



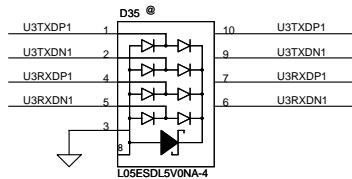


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				Custom	4019ID	B
				Date:	Friday, January 06, 2012	Sheet 38 of 61

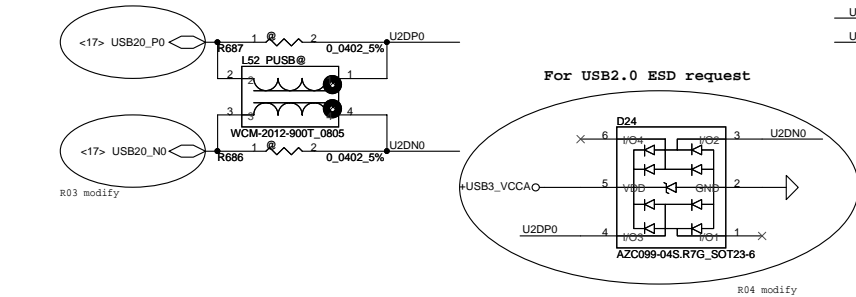
Default use PCH side USB3.0 signal



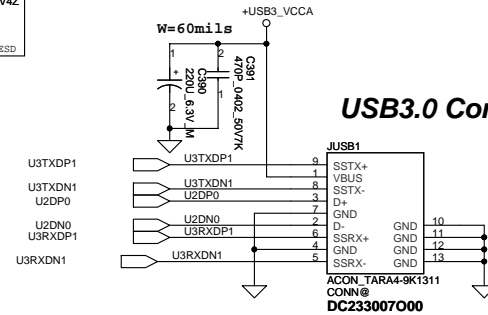
For ESD request



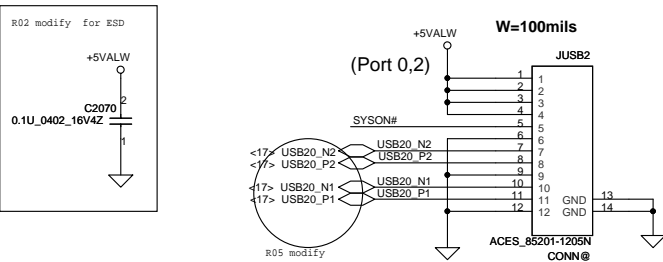
For USB2.0 ESD request



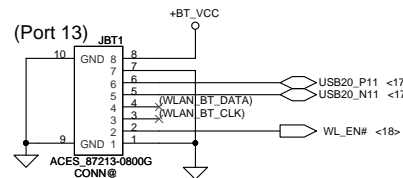
USB3.0 Conn.



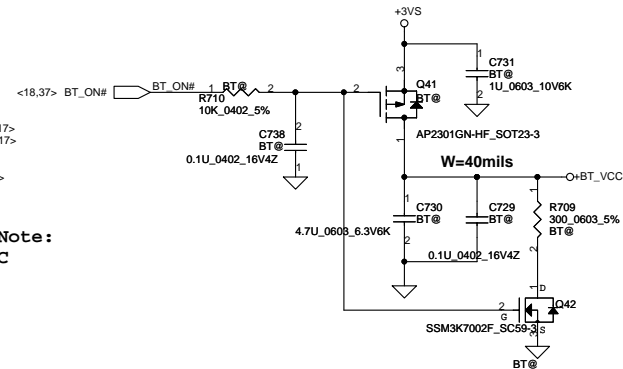
USB/B Conn.



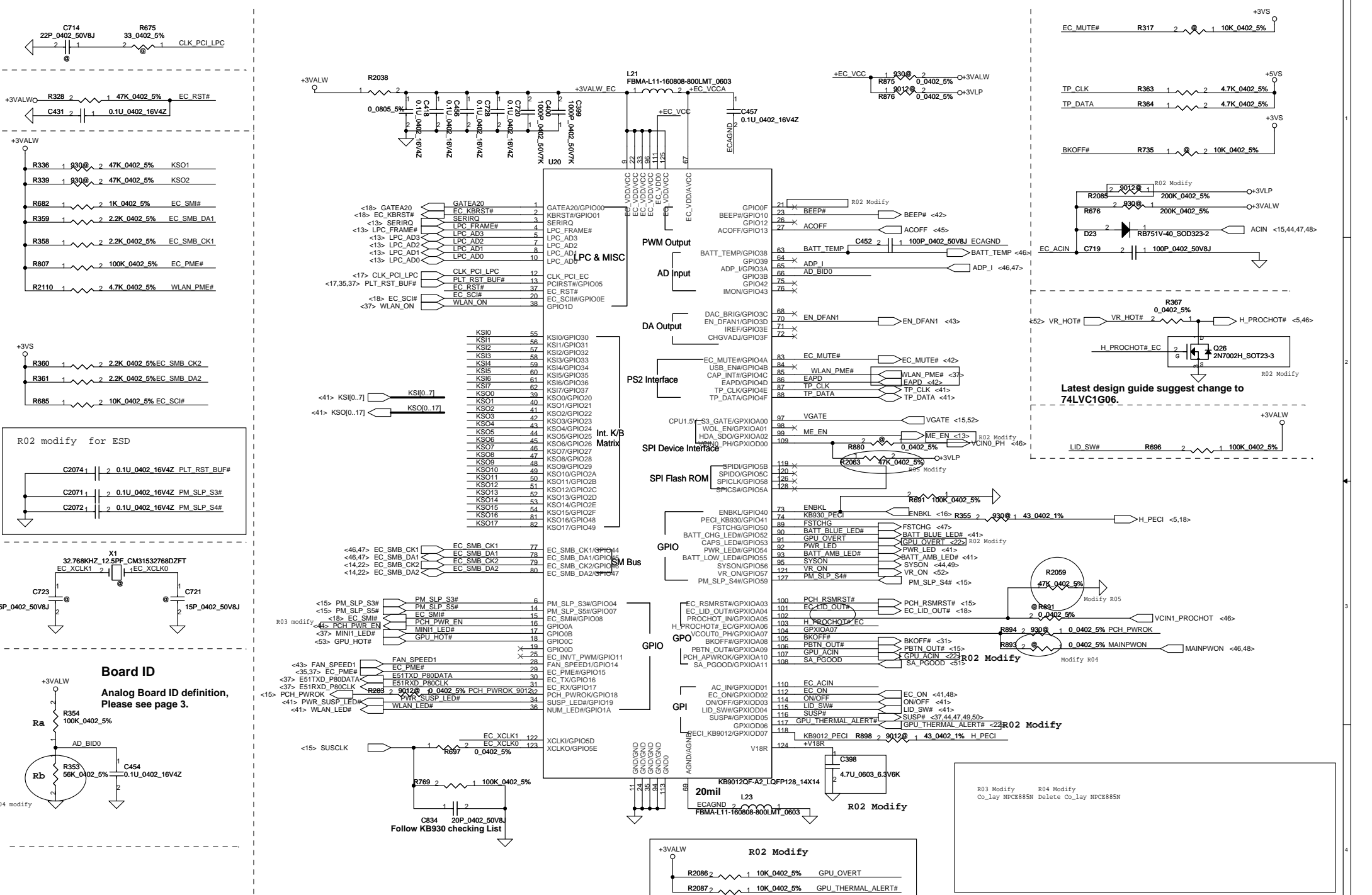
BT Conn.



BT Wire Cable Note:
Pin 3, Pin 4 NC



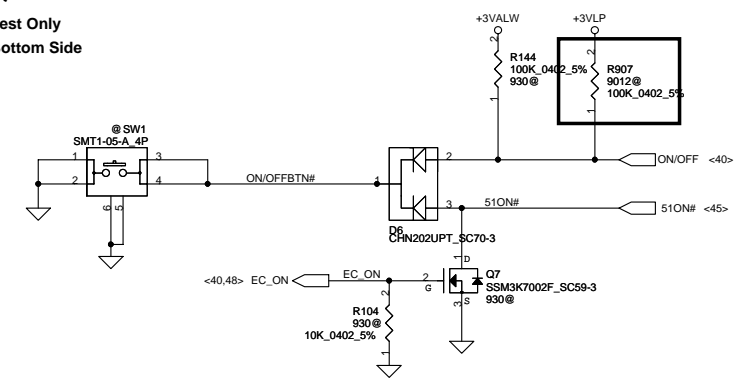
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Date: Friday, January 06, 2012						Document Number	4019ID	
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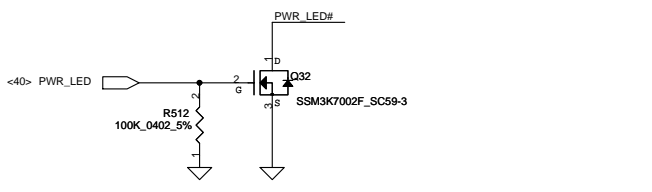
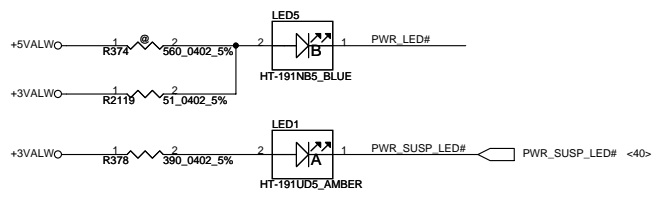
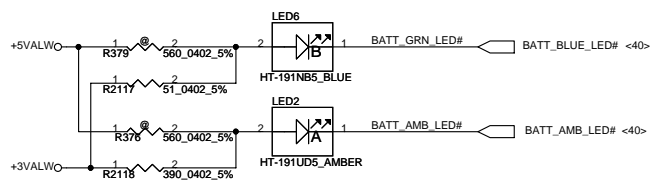
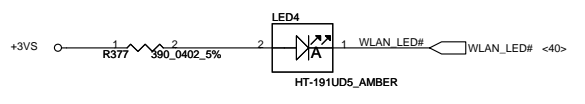
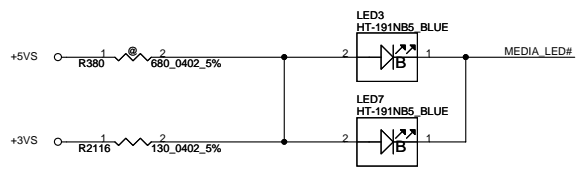
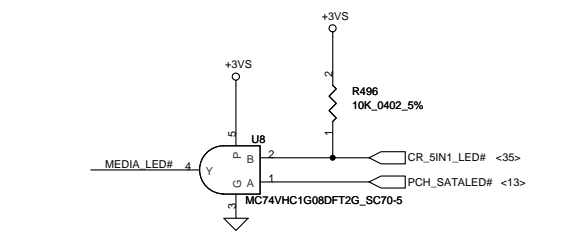
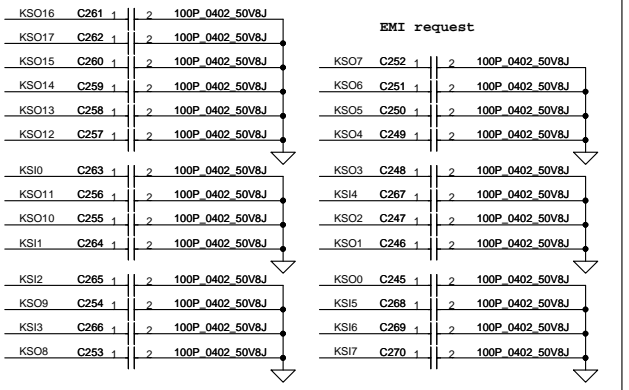
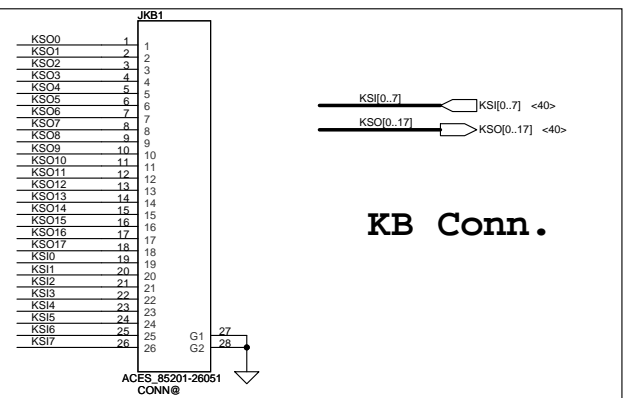
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ON/OFF BTN

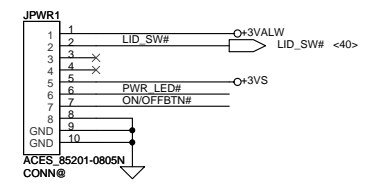
Test Only
Bottom Side



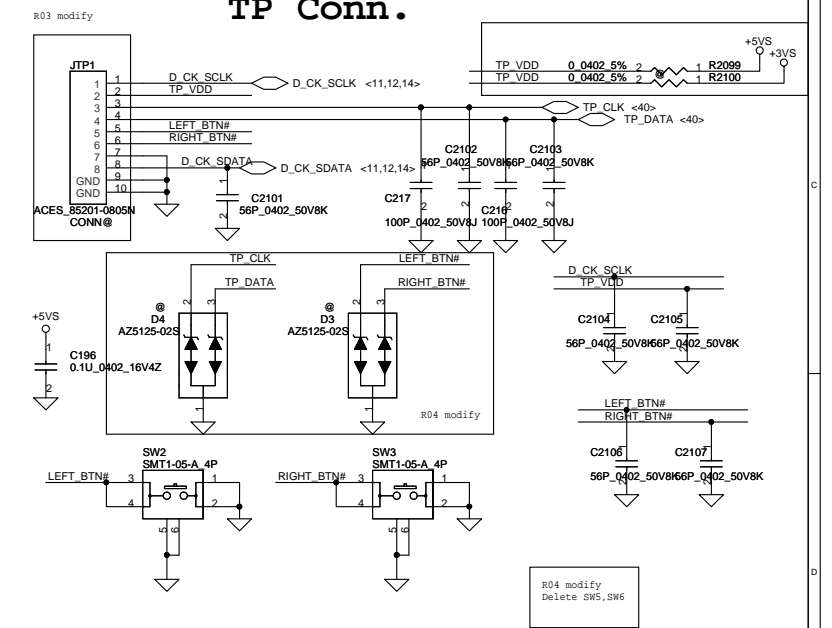
KB Conn.



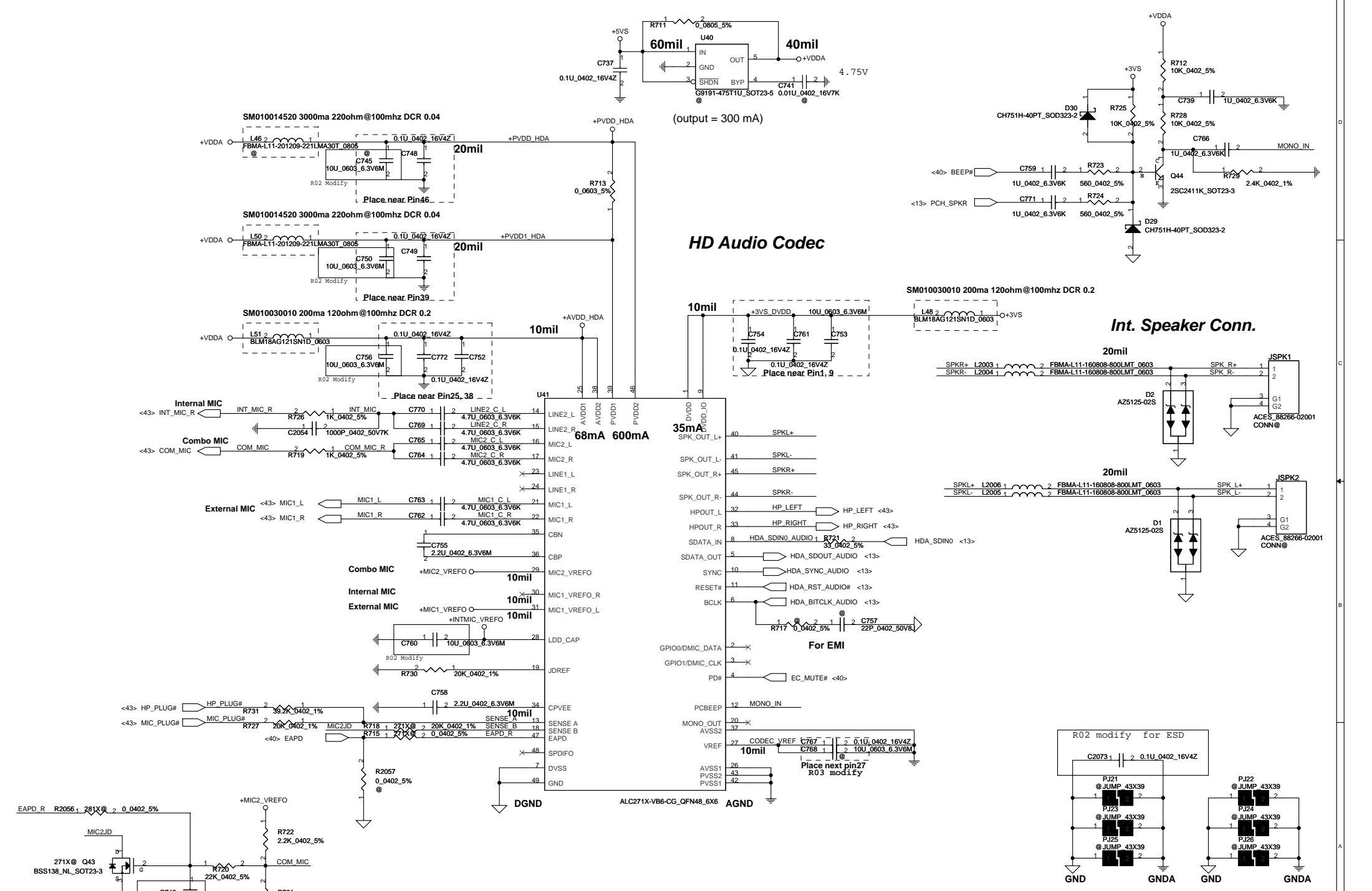
PWR/B



TP Conn.



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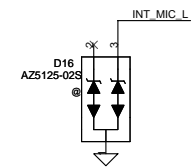
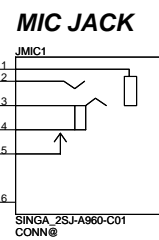
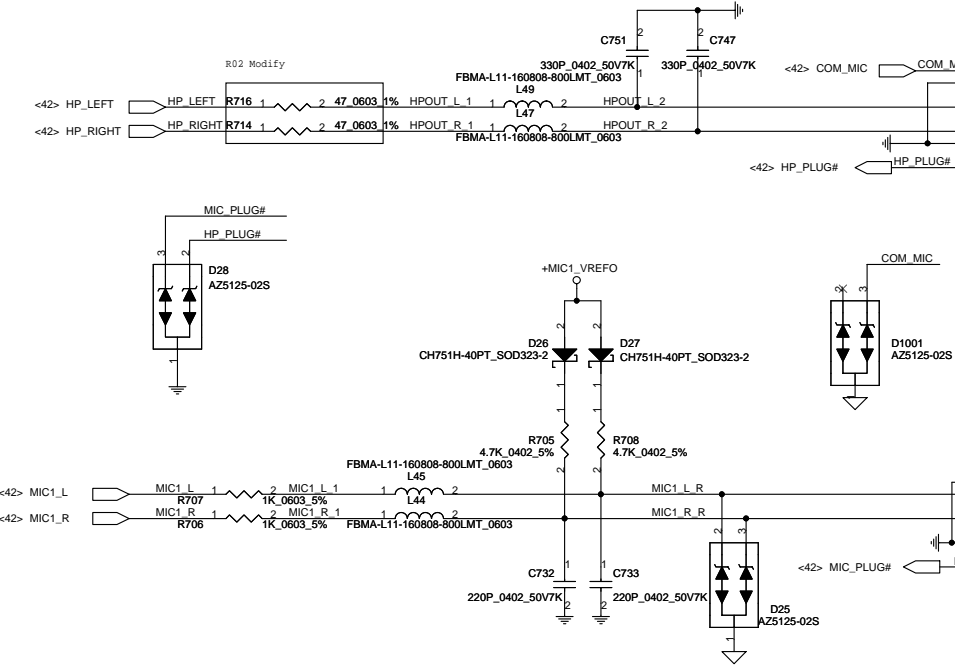
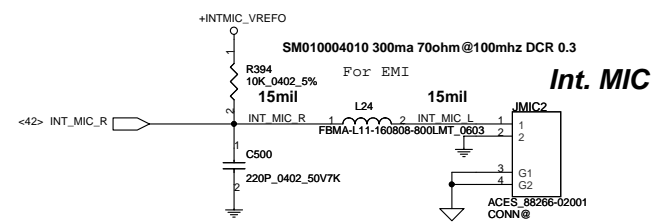
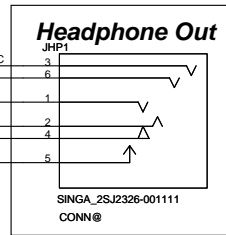


HD Audio Codec

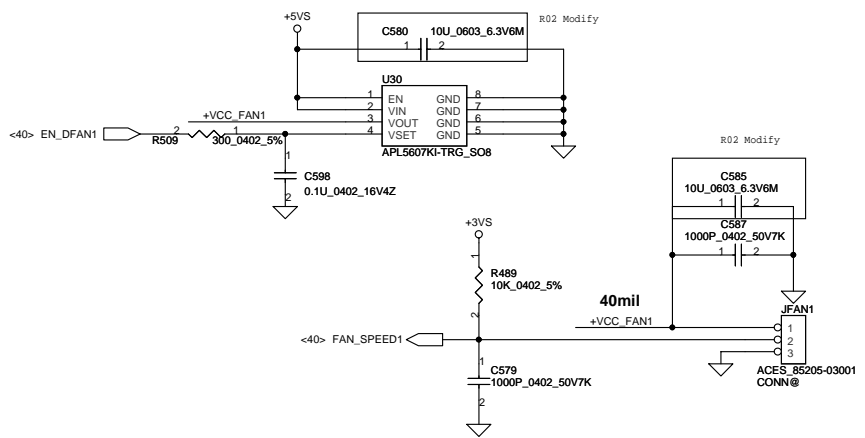
Int. Speaker Conn.

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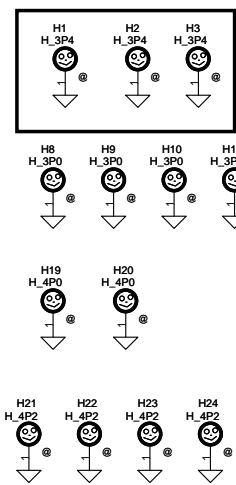
Singatron 2SJ2326
DC021007151



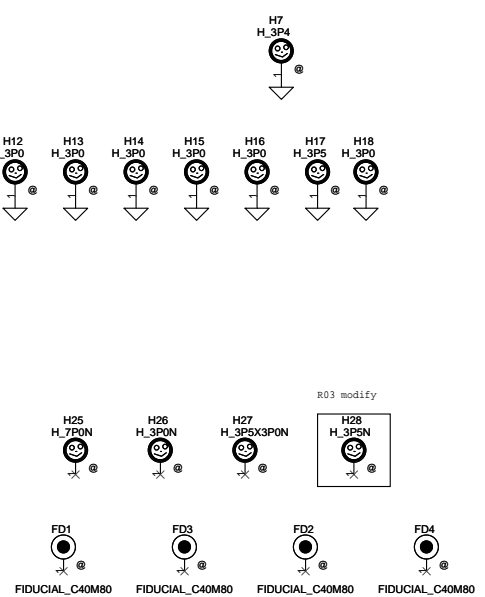
FAN1 Conn



FAN Stand-Off

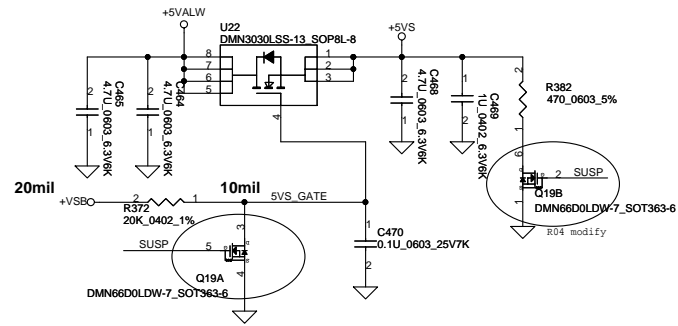


USB3 Stand-Off

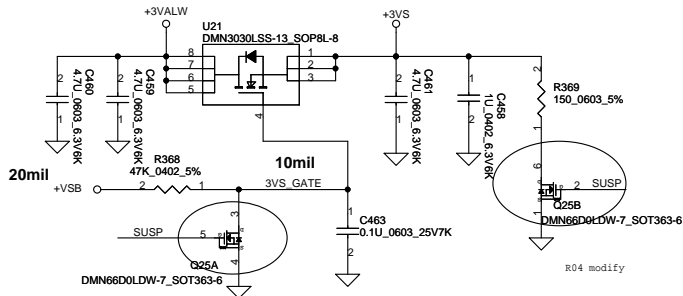


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Date:	Friday, January 06, 2012	Sheet	43 of 60	Customer Document Number 4019ID

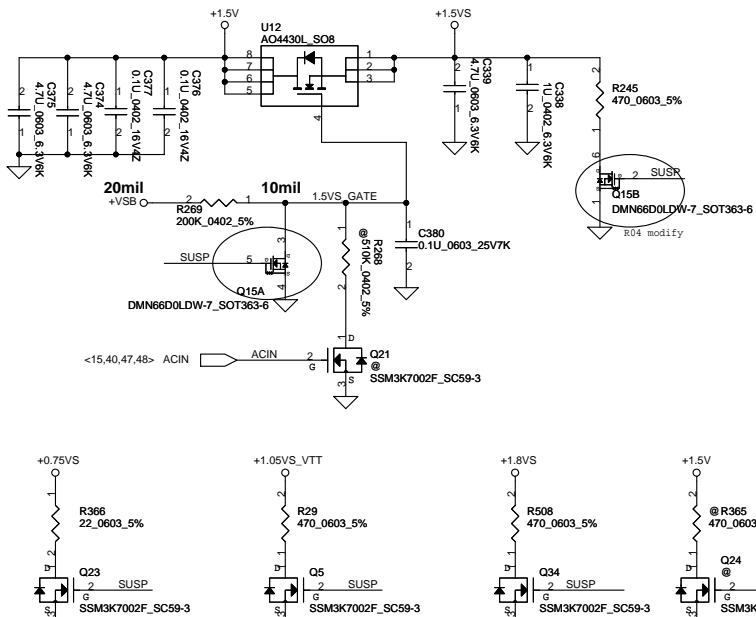
+5VALW TO +5VS



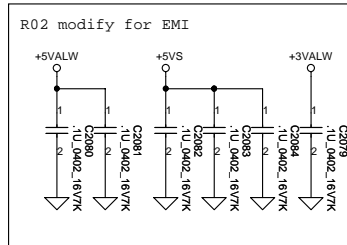
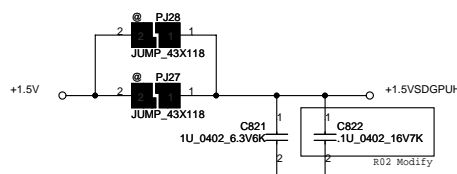
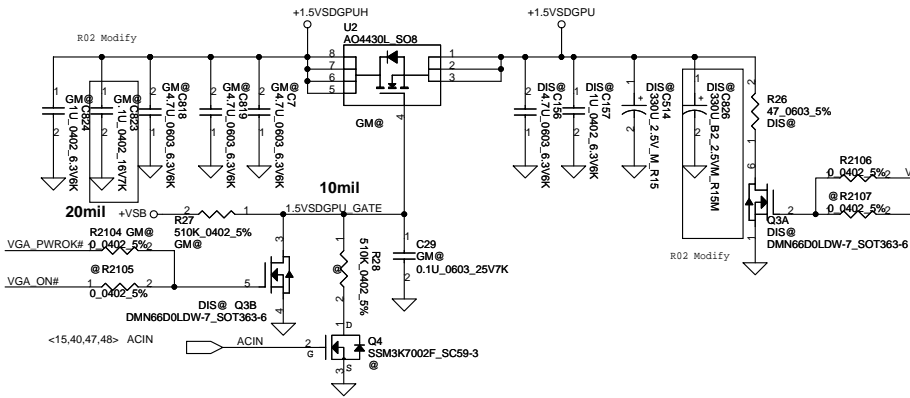
+3VALW TO +3VS



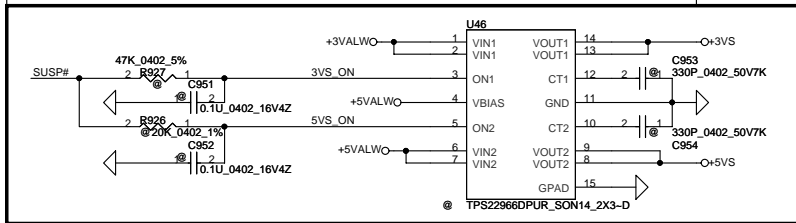
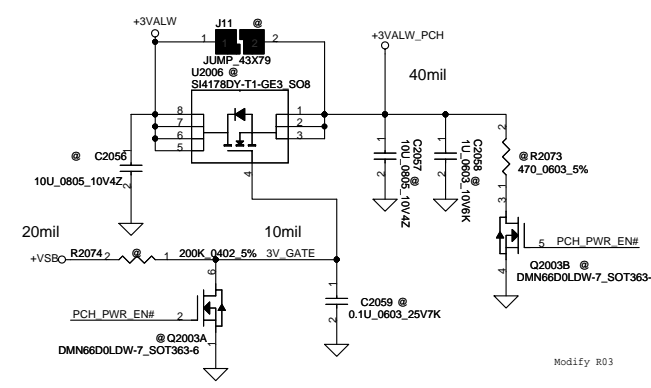
+1.5V to +1.5VS



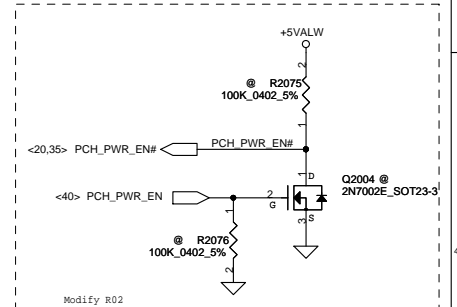
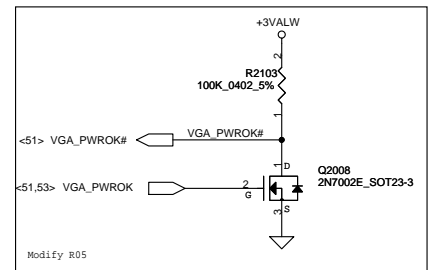
+1.5VSDGPUH to +1.5VSDGPU for GPU



+3VALW TO +3VALW(PCH AUX Power)



Use 100k to make sure the divided voltage is enough!!

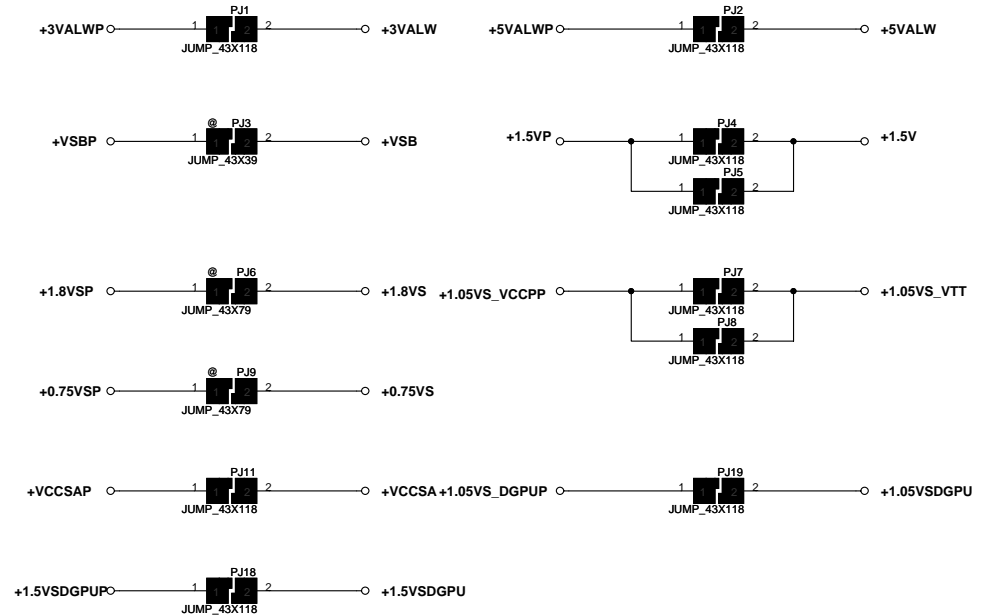
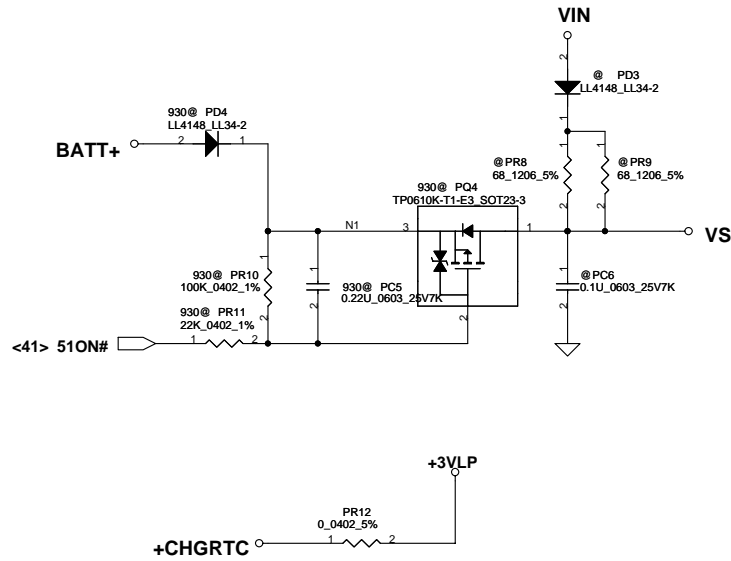
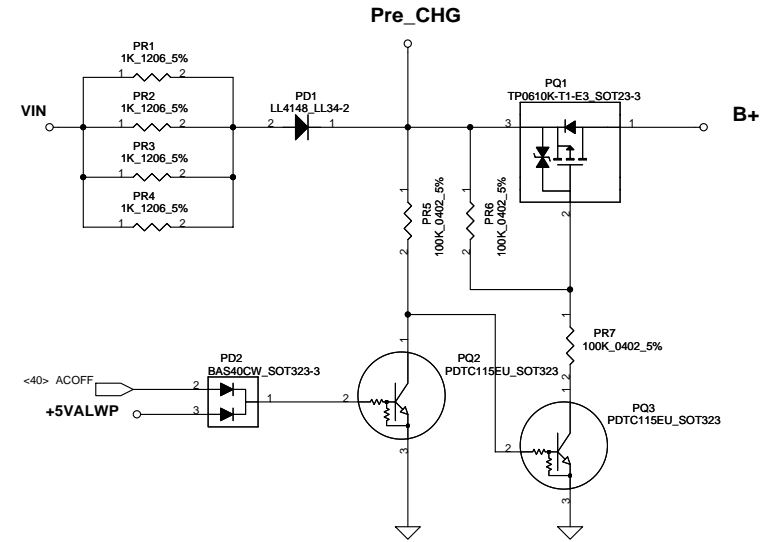
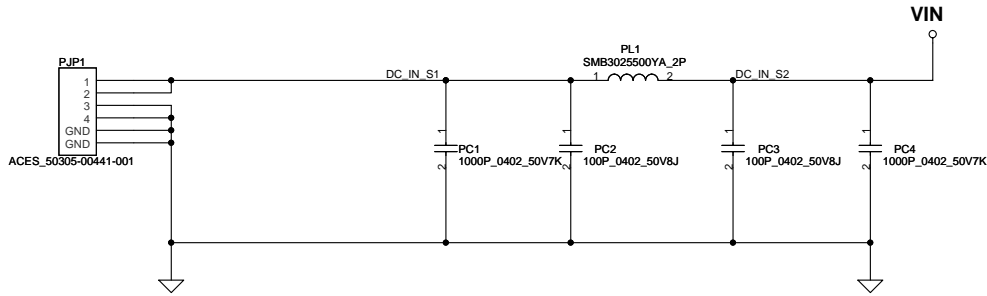


Reserved

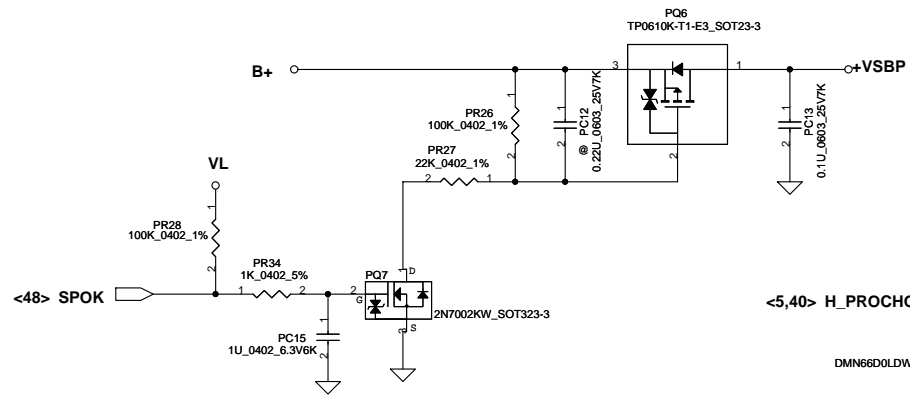
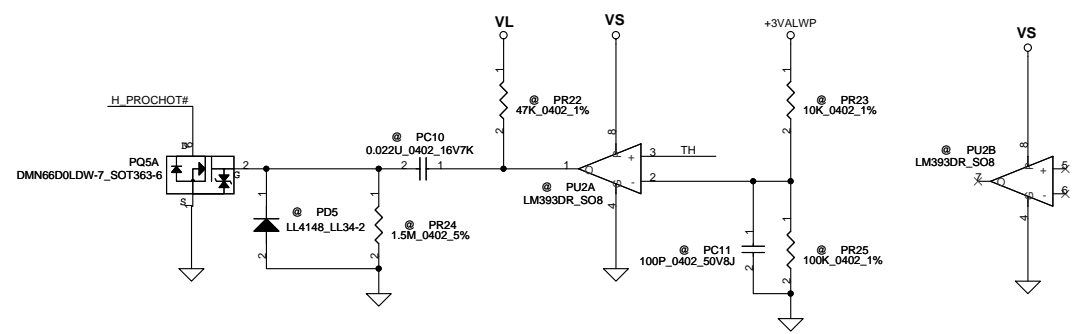
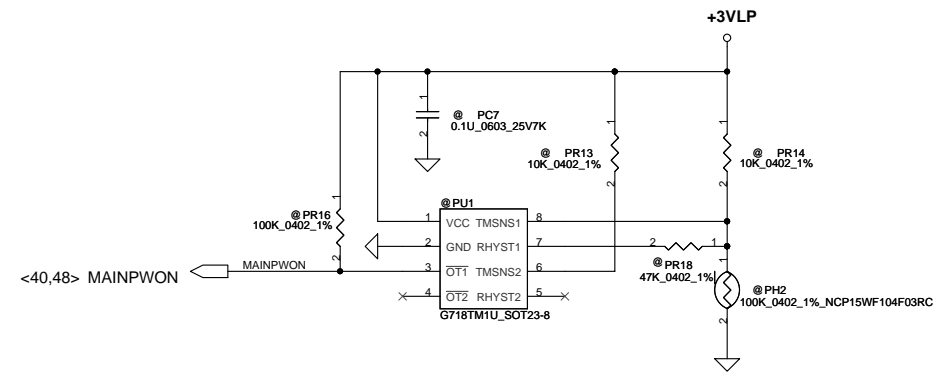
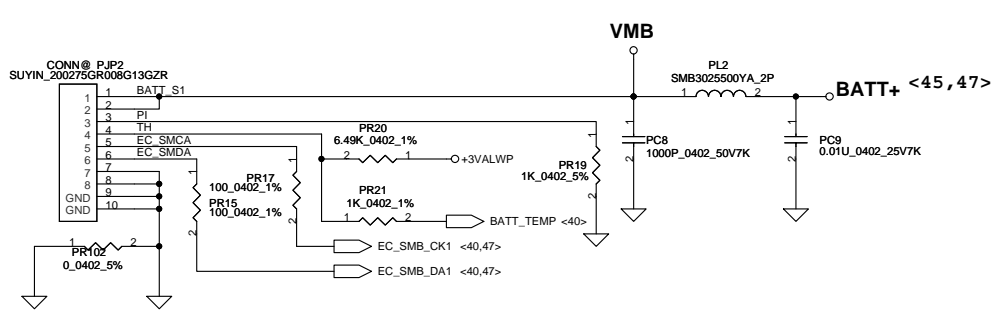
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Issued Date	2011/06/02
Deciphered Date	2012/06/02

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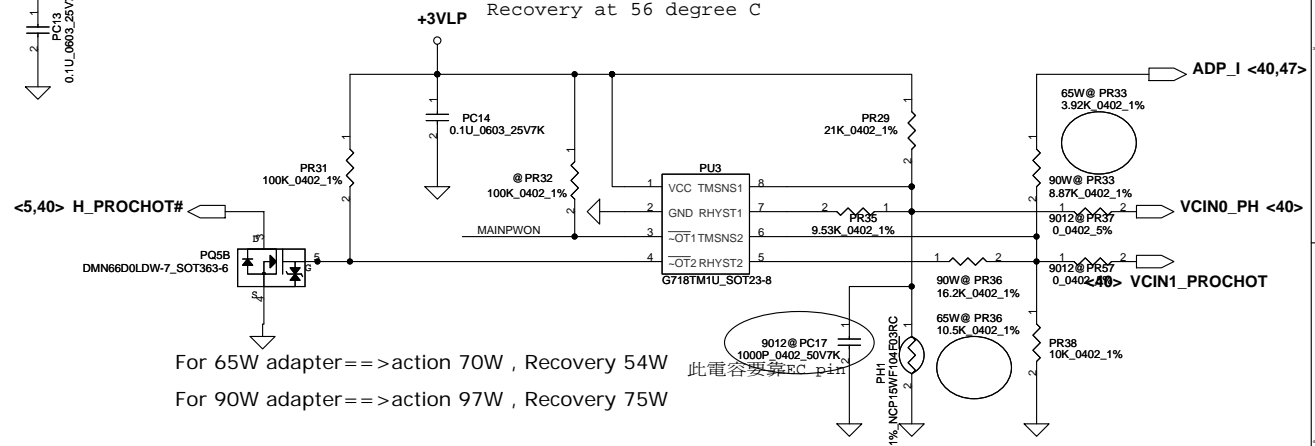
Compal Electronics, Inc.		
SCHMATIC_MB A7912		
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

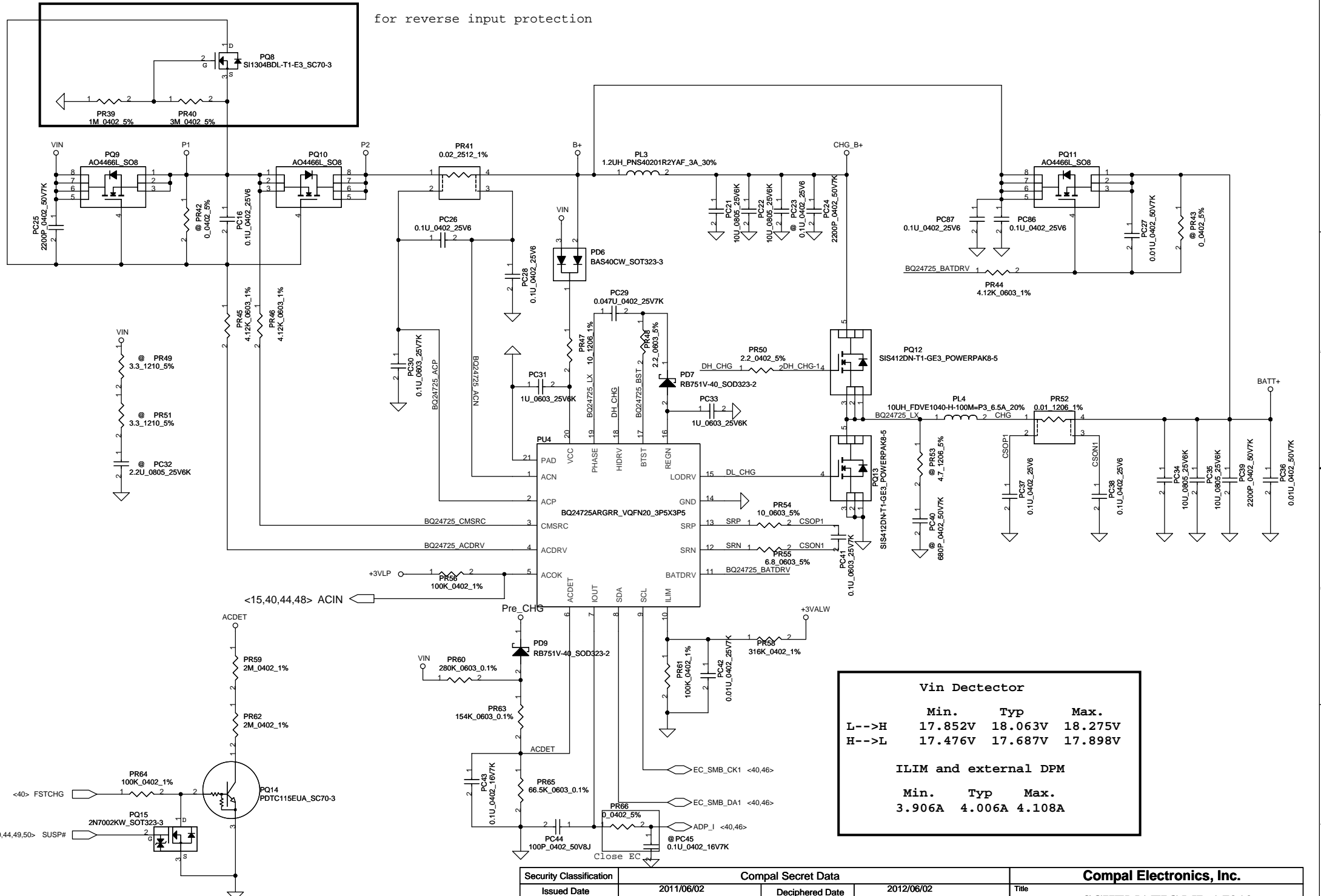


For 65W adapter ==> action 70W , Recovery 54W
 For 90W adapter ==> action 97W , Recovery 75W

此電容要算PC pin

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for reverse input protection

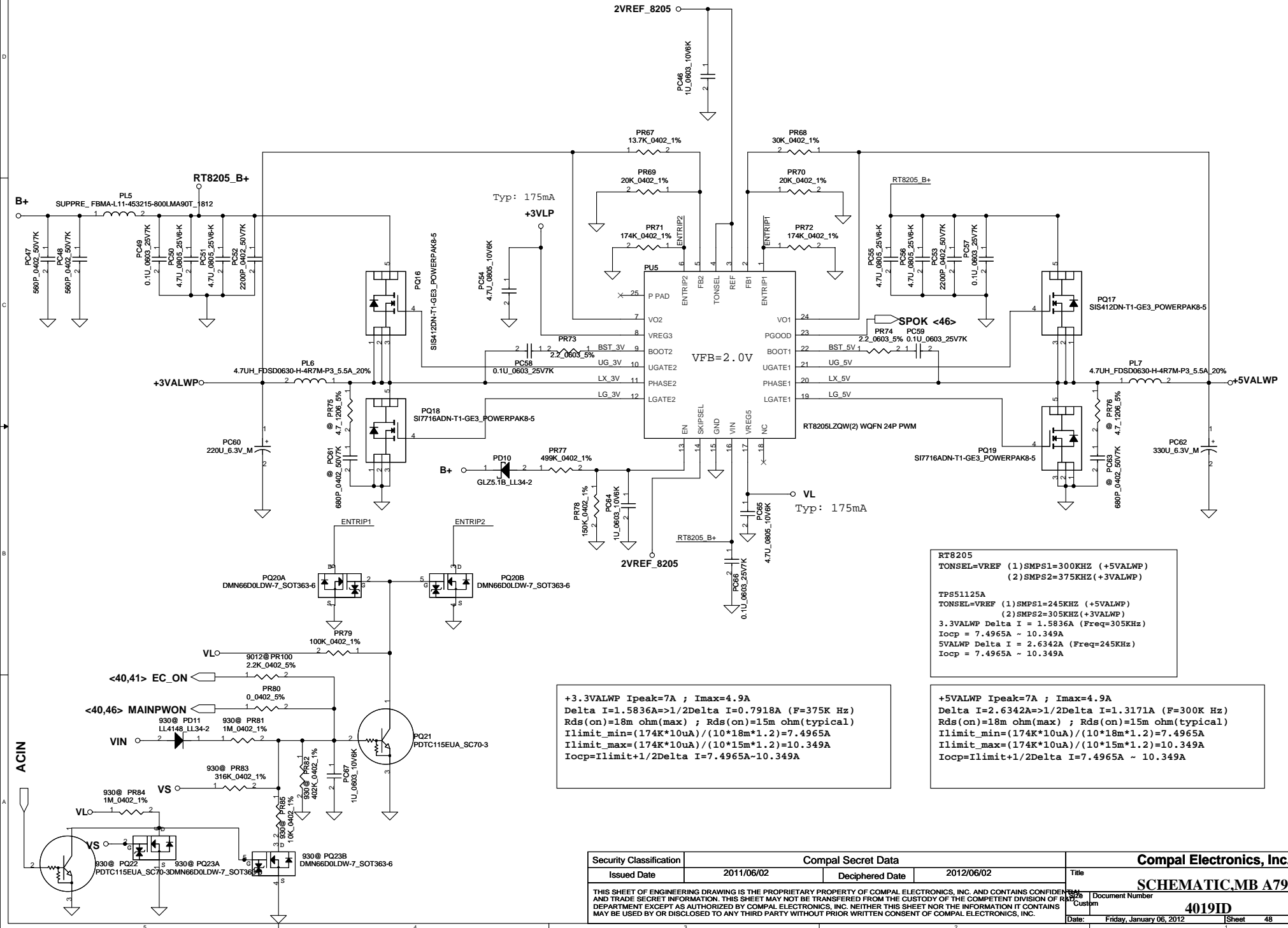


Vin Detector			
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



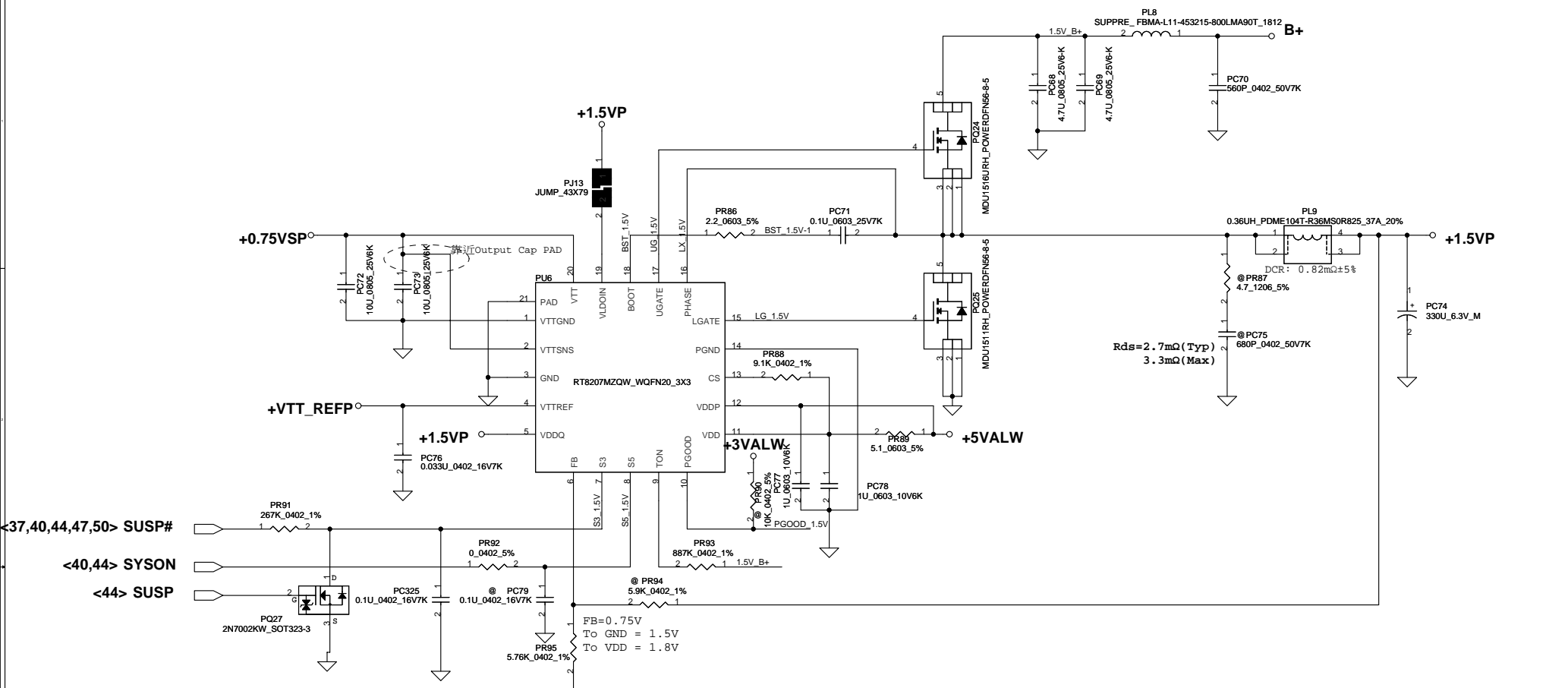
+3.3VALWP Ipeak=7A ; Imax=4.9A
 $\Delta I = 1.5836A > 1/2 \Delta I = 0.7918A$ (F=375K Hz)
 $R_{ds(on)} = 18m\ \Omega$ (max) ; $R_{ds(on)} = 15m\ \Omega$ (typical)
 $I_{limit_min} = (174K * 10\mu A) / (10 * 18m * 1.2) = 7.4965A$
 $I_{limit_max} = (174K * 10\mu A) / (10 * 15m * 1.2) = 10.349A$
 $I_{ocp} = I_{limit} + 1/2 \Delta I = 7.4965A - 10.349A$

RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

TPS51125A
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
 (2) SMPS2=305KHZ (+3VALWP)
 3.3VALWP $\Delta I = 1.5836A$ (Freq=305KHZ)
 $I_{ocp} = 7.4965A \sim 10.349A$
 5VALWP $\Delta I = 2.6342A$ (Freq=245KHZ)
 $I_{ocp} = 7.4965A \sim 10.349A$

+5VALWP Ipeak=7A ; Imax=4.9A
 $\Delta I = 2.6342A > 1/2 \Delta I = 1.3171A$ (F=300K Hz)
 $R_{ds(on)} = 18m\ \Omega$ (max) ; $R_{ds(on)} = 15m\ \Omega$ (typical)
 $I_{limit_min} = (174K * 10\mu A) / (10 * 18m * 1.2) = 7.4965A$
 $I_{limit_max} = (174K * 10\mu A) / (10 * 15m * 1.2) = 10.349A$
 $I_{ocp} = I_{limit} + 1/2 \Delta I = 7.4965A \sim 10.349A$

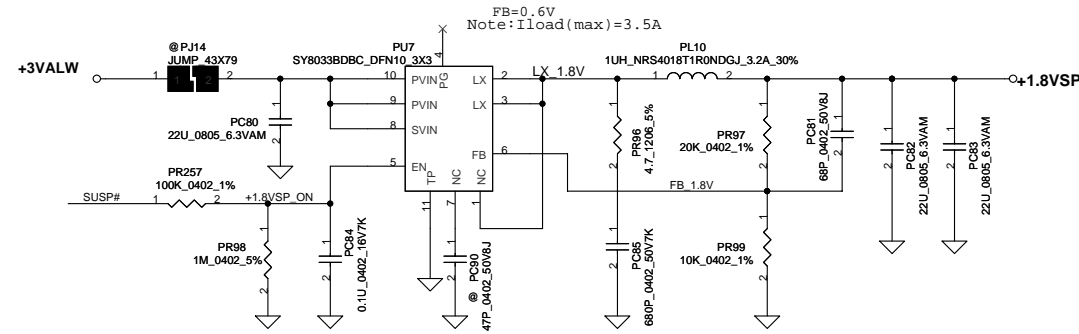
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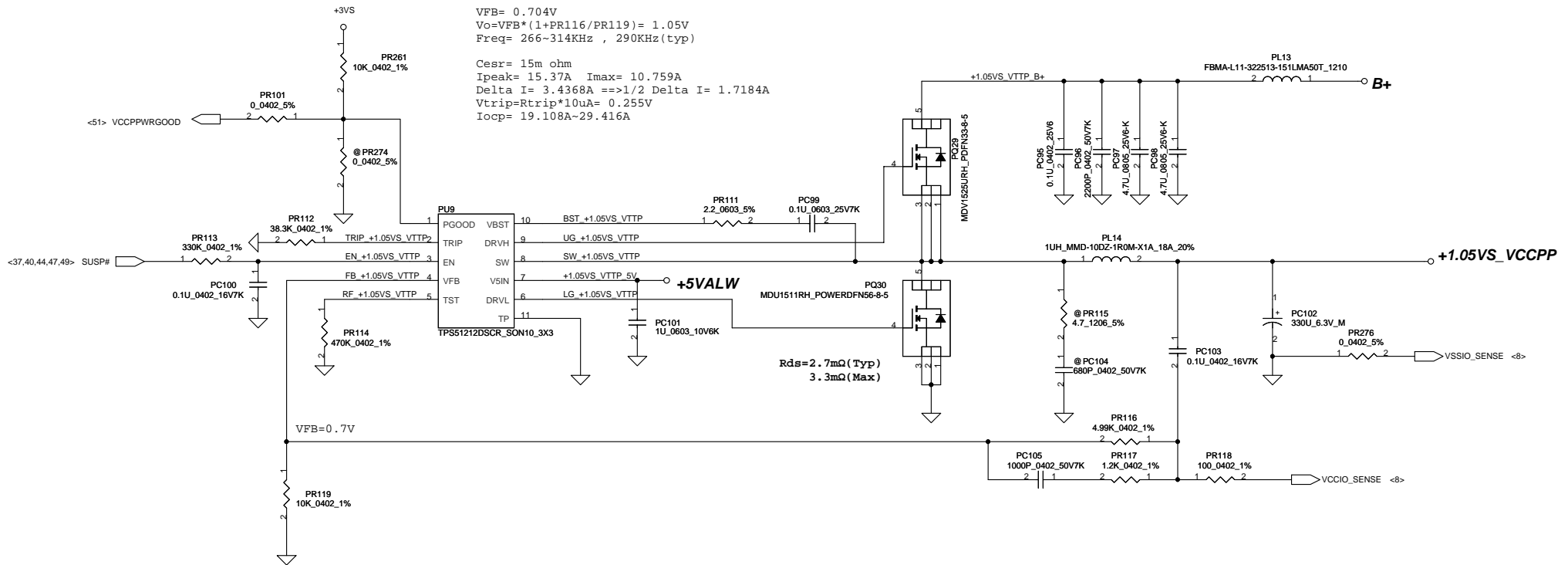
<37,40,44,47,50> SUSP#
 <40,44> SYSON
 <44> SUSP

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

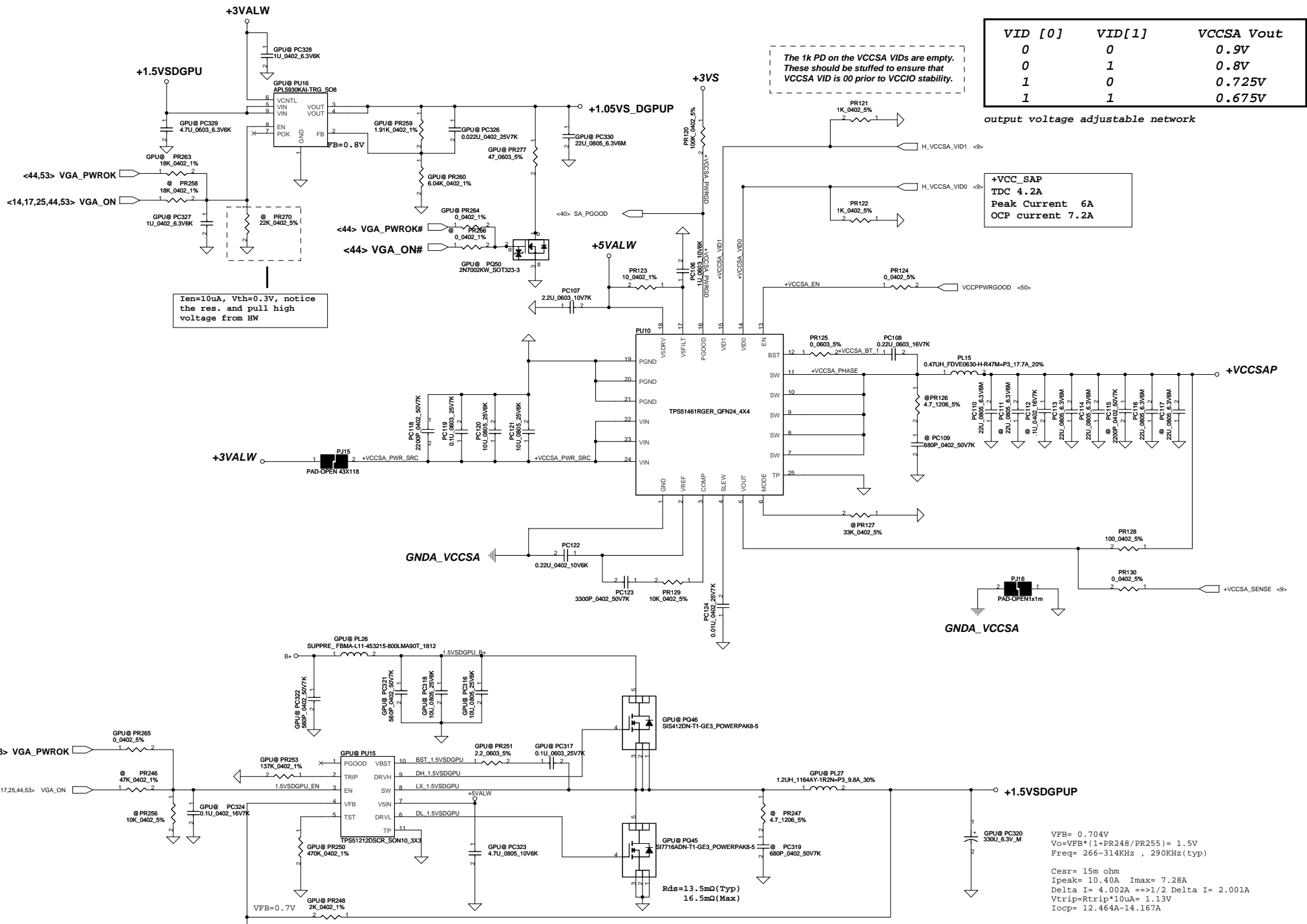
Note: S3 - sleep ; S5 - power off



Notice: Internal resistance about 500K on 2nd EN pin



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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

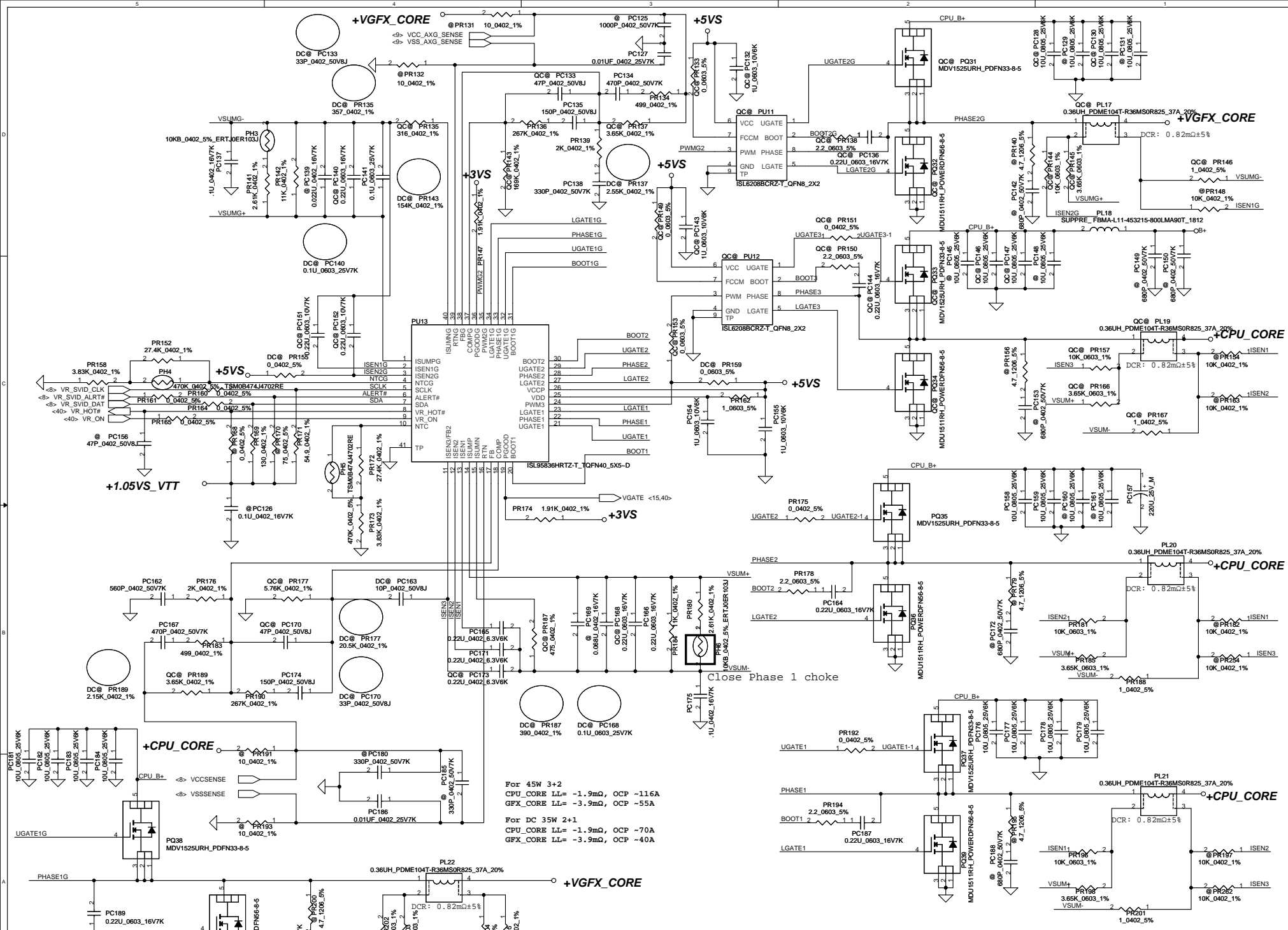
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

Ien=10uA, Vth=0.3V, notice the res. and pull high voltage from HW

VFB= 0.704V
Vo=VFB*(1+PR248/PR255) = 1.5V
Freq= 266-314KHz , 290KHz(typ)
Cesr= 15m ohm
Ipeak= 10.40A Imax= 7.28A
Delta I= 4.002A ==>1/2 Delta I= 2.001A
Vtrip=Rtrip*10uA= 1.13V
Iocp= 12.464A-14.167A

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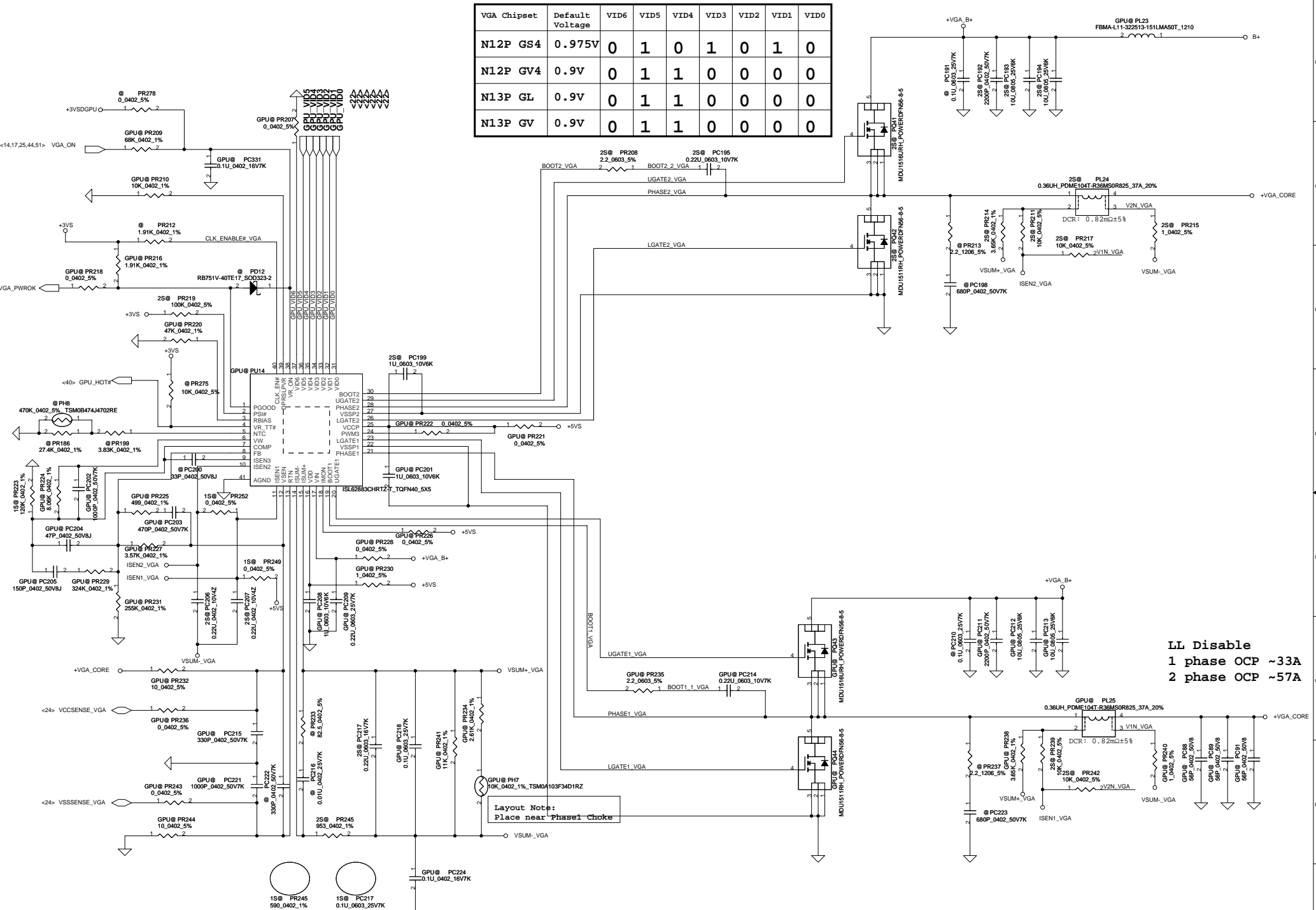


For 45W 3+2
 CPU_CORE LL = -1.9mΩ, OCP -116A
 GFX_CORE LL = -3.9mΩ, OCP -55A

For DC 35W 2+1
 CPU_CORE LL = -1.9mΩ, OCP -70A
 GFX_CORE LL = -3.9mΩ, OCP -40A

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VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0

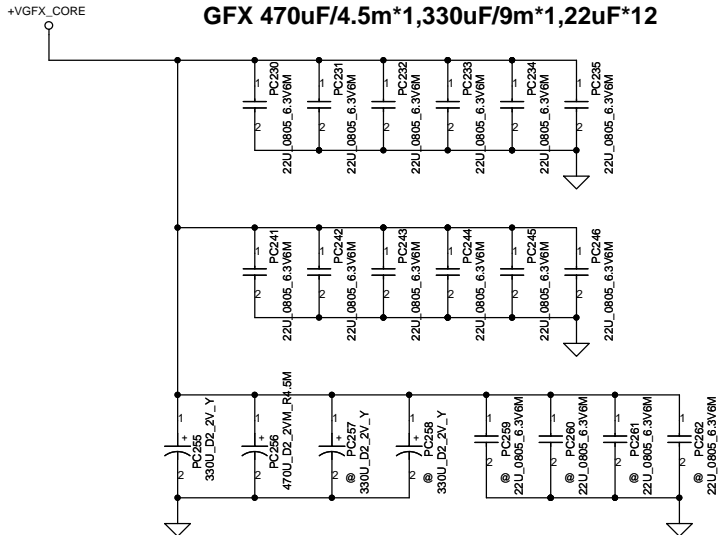


LL Disable
 1 phase OCP ~33A
 2 phase OCP ~57A

Layout Note:
 Place near Phase1 Choke

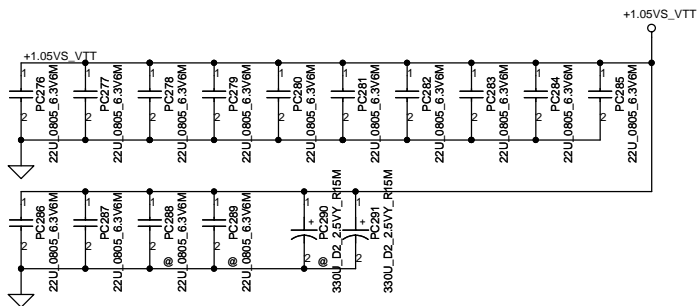
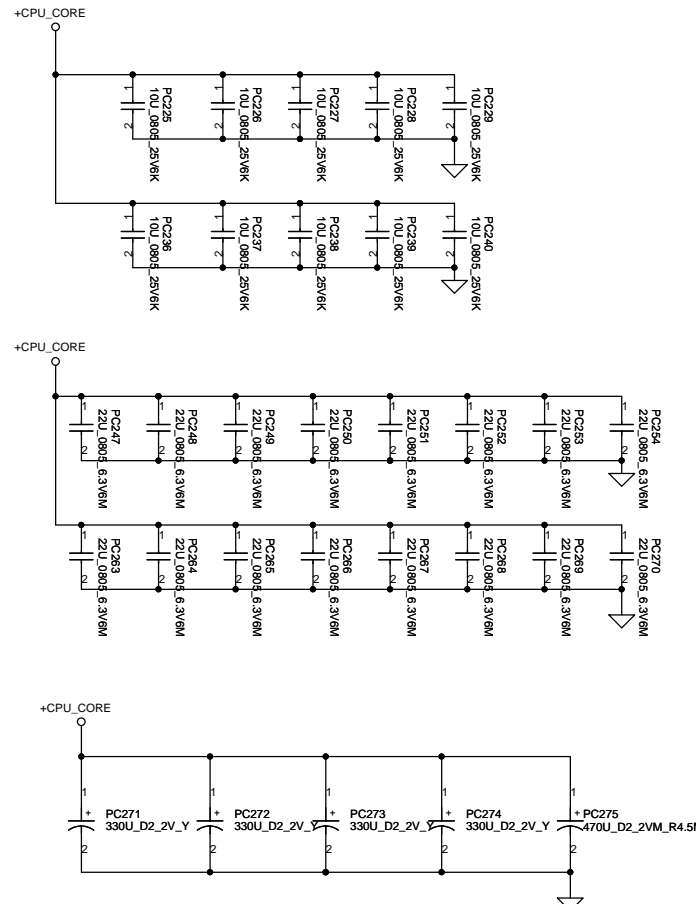
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PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12



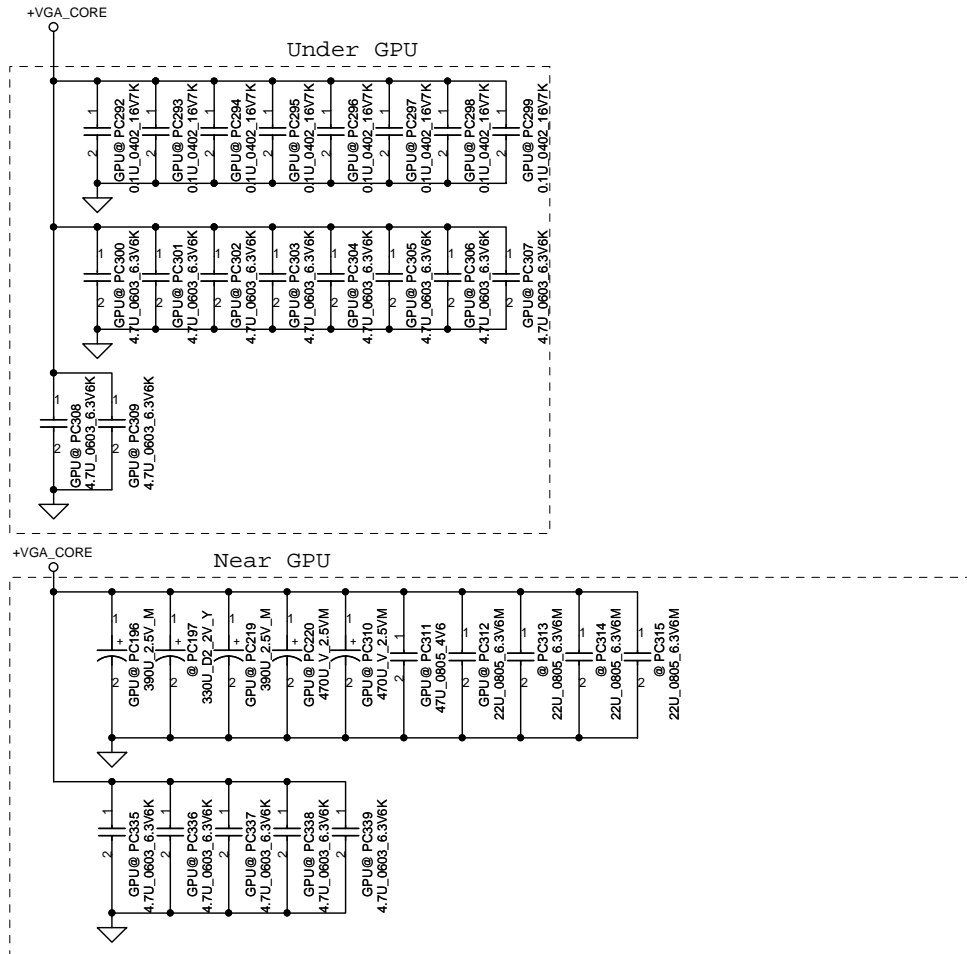
Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2		
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	DVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	DVT
8							
9							
10							
11							
12							
13							
14							
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16							
17							
18							
19							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
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11							
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1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add f11009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	Add USB chargeaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)		0.2
7	P.44		9/7	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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25	P.44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P.36		9/20	HW	For SD3.0 issue (Add R2088.R2089)		0.2
27	P.20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P.44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P.40		10/17	HW	Board ID error. Add R353.		0.3
30	P.40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P.17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P.18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P.13.40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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43	P.41		11/16	ME		Delete SW5,SW6, Pop SW2,SW3	0.4
44	P.05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P.35		11/17	HW	LAN SPROM on Chip	De-pop U31,R537 Pop R538	0.4
46	P.36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P.13		11/17	HW	RTC issue	Change C682,C686 to 15P	0.4
48	P.31,32,41		11/17	ESD		De-pop D3,D4,D17,D18,D15 Pop D24,D36	0.4
49	P.40		11/17	HW		De-pop R891,R893	0.4
50	P.24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P.13		11/21	HW		Chip Select Change R651,R2049 to 0ohm	0.4
52	P.13,40		11/21	HW		Delete NPCE885N (R2091.R2092.R2094.R2095.R2096,R698, R699,R692,C2085)	0.4
53	P.45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P.35,36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091-C2093 Change R525,R536,R537,R538 to 1k	0.4
56	P.13		11/23	HW		Delete R2093,R2049,R651(0ohm)	0.4
57	P.13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P.35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P.36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2012/06/02	Title	Schematic, MB A7912
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