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NIWE2

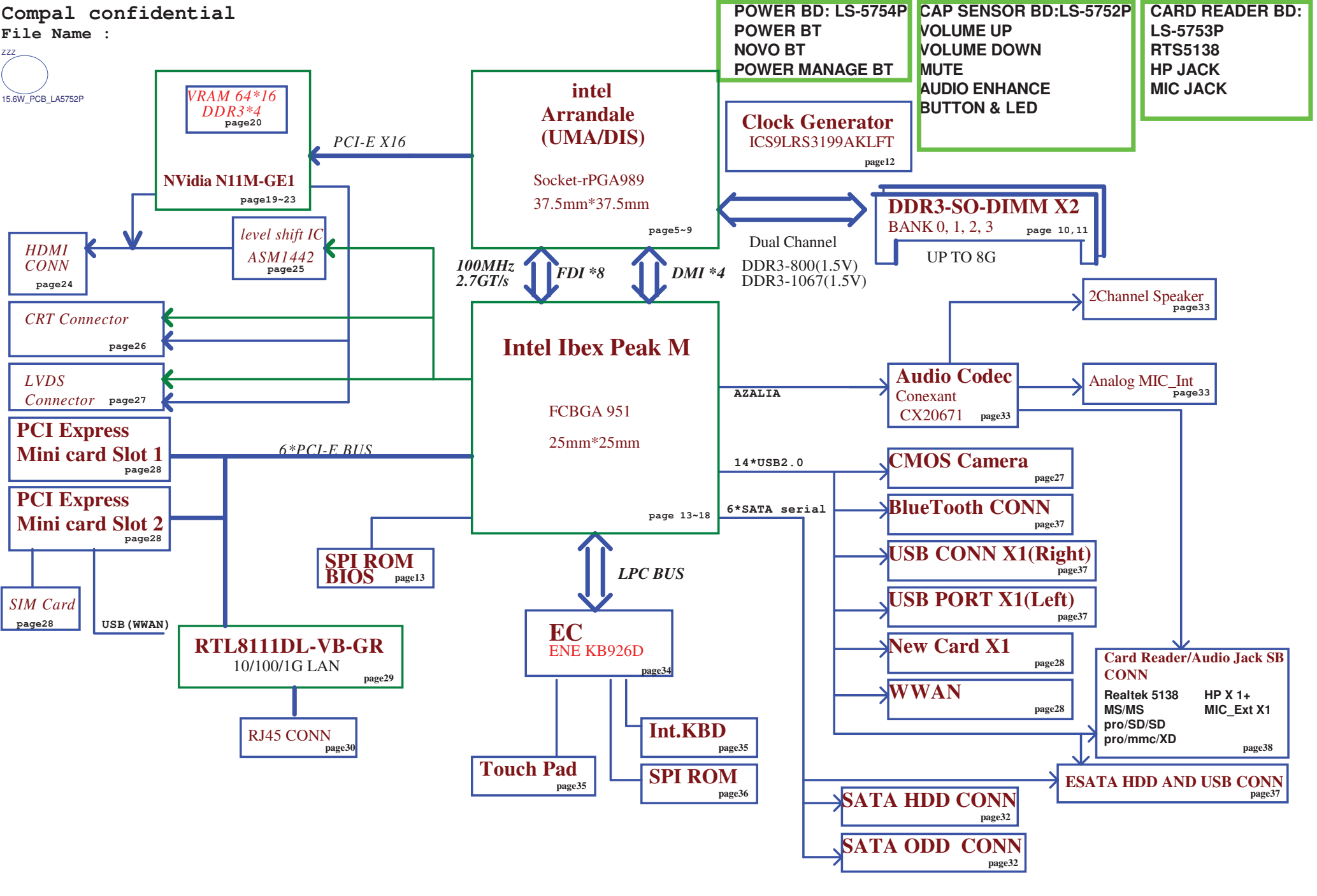
Schematics Document

Arrandale

with Intel IBEX PEAK-M core logic

REV: 0.3

Security Classification	Compal Secret Data			<i>Compal Electronics, Ltd.</i>		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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				Custom	LA-5752P	0.3
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POWER BD: LS-5754P
 POWER BT
 NOVO BT
 POWER MANAGE BT

CAP SENSOR BD:LS-5752P
 VOLUME UP
 VOLUME DOWN
 MUTE
 AUDIO ENHANCE
 BUTTON & LED

CARD READER BD: LS-5753P
 RTS5138
 HP JACK
 MIC JACK

Clock Generator
 ICS9LRS3199AKLFT
 page12

DDR3-SO-DIMM X2
 BANK 0, 1, 2, 3
 page 10, 11
 UP TO 8G

Intel Ibox Peak M
 FCBGA 951
 25mm*25mm
 page 13-18

VRAM 64*16 DDR3*4
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NVidia N11M-GE1
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HDMI CONN
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CRT Connector
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LVDS Connector
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PCI Express Mini card Slot 1
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SIM Card
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 10/100/1G LAN
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RJ45 CONN
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SPI ROM BIOS
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 ENE KB926D
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Touch Pad
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Int.KBD
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Audio Codec
 Conexant CX20671
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CMOS Camera
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BlueTooth CONN
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USB CONN X1(Right)
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USB PORT X1(Left)
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New Card X1
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WWAN
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2Channel Speaker
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Analog MIC_Int
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Card Reader/Audio Jack SB CONN
 Realtek 5138 MS/MS pro/SD/SD pro/mmc/XD
 HP X 1+ MIC_Ext X1
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ESATA HDD AND USB CONN
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SATA HDD CONN
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SATA ODD CONN
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DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
				State
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW	X	X	X	X	X	X	X	X	X	X	X
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V +3VALW
SMB_EC_DA2	+3VALW	X	X	X	X	X	X	X	X	X	X	X
SMBCLK	PCH	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	V +3VS	X
SMBDATA	+3VALW	X	X	X	X	X	X	X	X	X	X	X
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW	X	X	X	X	X	X	X	X	X	X	X
SML1CLK	PCH	X	X	V +3VALW	X	X	X	V +3VS	X	V +3VS	X	X
SML1DATA	+3VALW	X	X	X	X	X	X	X	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
10M@	FOR 10M CHIP	
11M@	FOR 11M CHIP	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
VGA@	FOR NVIDIA PART	
HYBRID@	FOR SWITCHABLE	
HU@	SWITCHABLE or UMA only	
HD@	SWITCHABLE or DIS only	

SKU

Arrandale (dGPU) DIS only	DIS@ / 100@ for EVT
Arrandale (iGPU) UMA only	UMA@ / 100@ for EVT
Arrandale (iGPU+dGPU) SWITCHABLE	VGA@+HD@+HU@+HYBRID@

PCIe PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

<http://hobi-elektronika.net>

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0, 10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

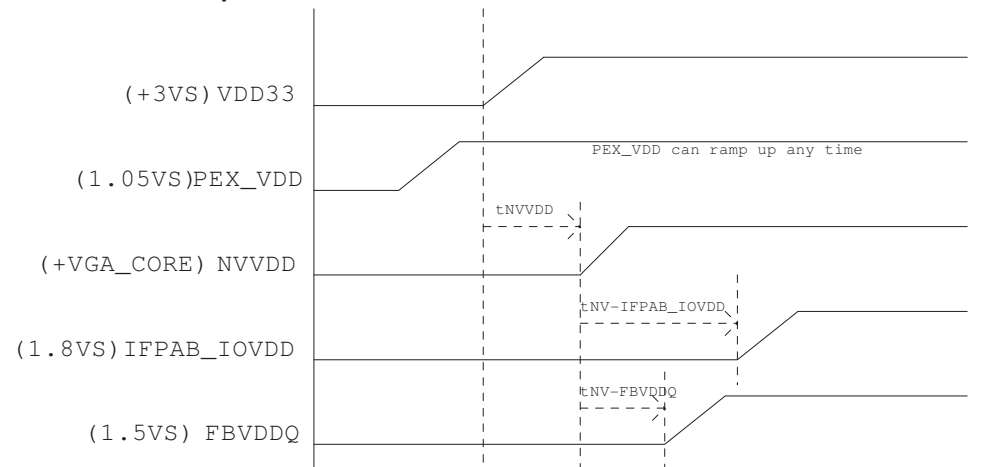
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.8V) (W)		I/O and PLLVDD (1.05V) (W)		Other (3.3V) (W)	
				(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.8V) (W)		I/O and PLLVDD (1.05V) (W)		Other (3.3V) (W)	
				(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

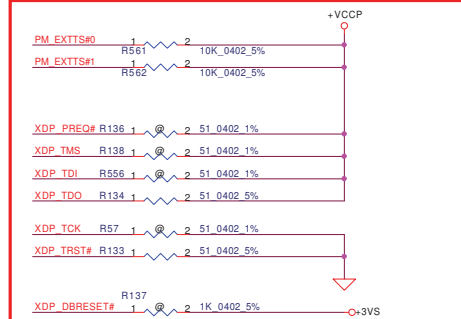
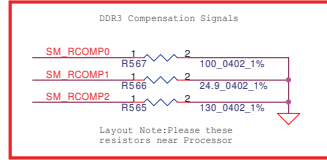
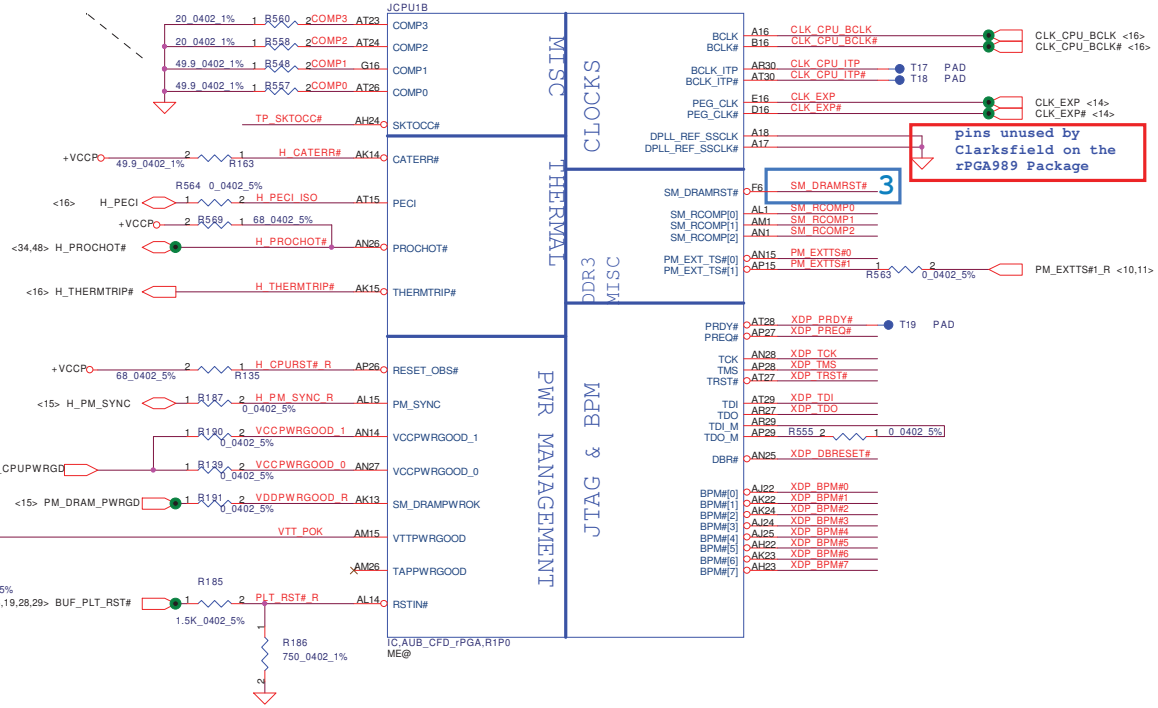
Power Sequence

The ramp time for any rail must be more than 40us

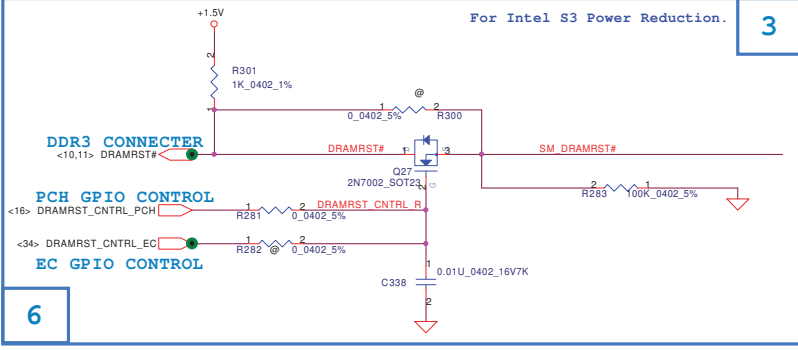
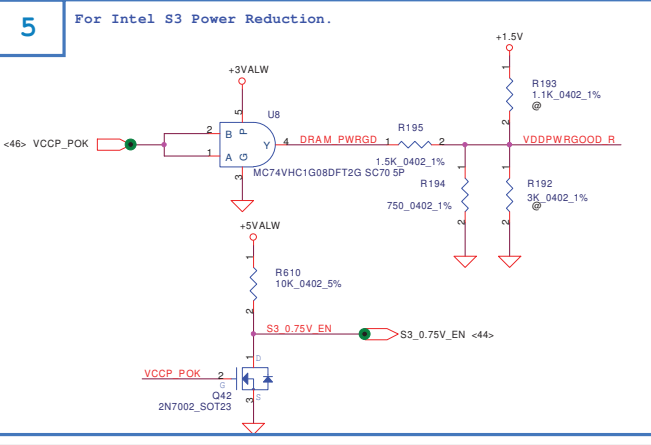
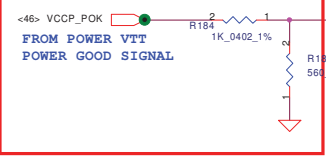


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				VGA Notes List		
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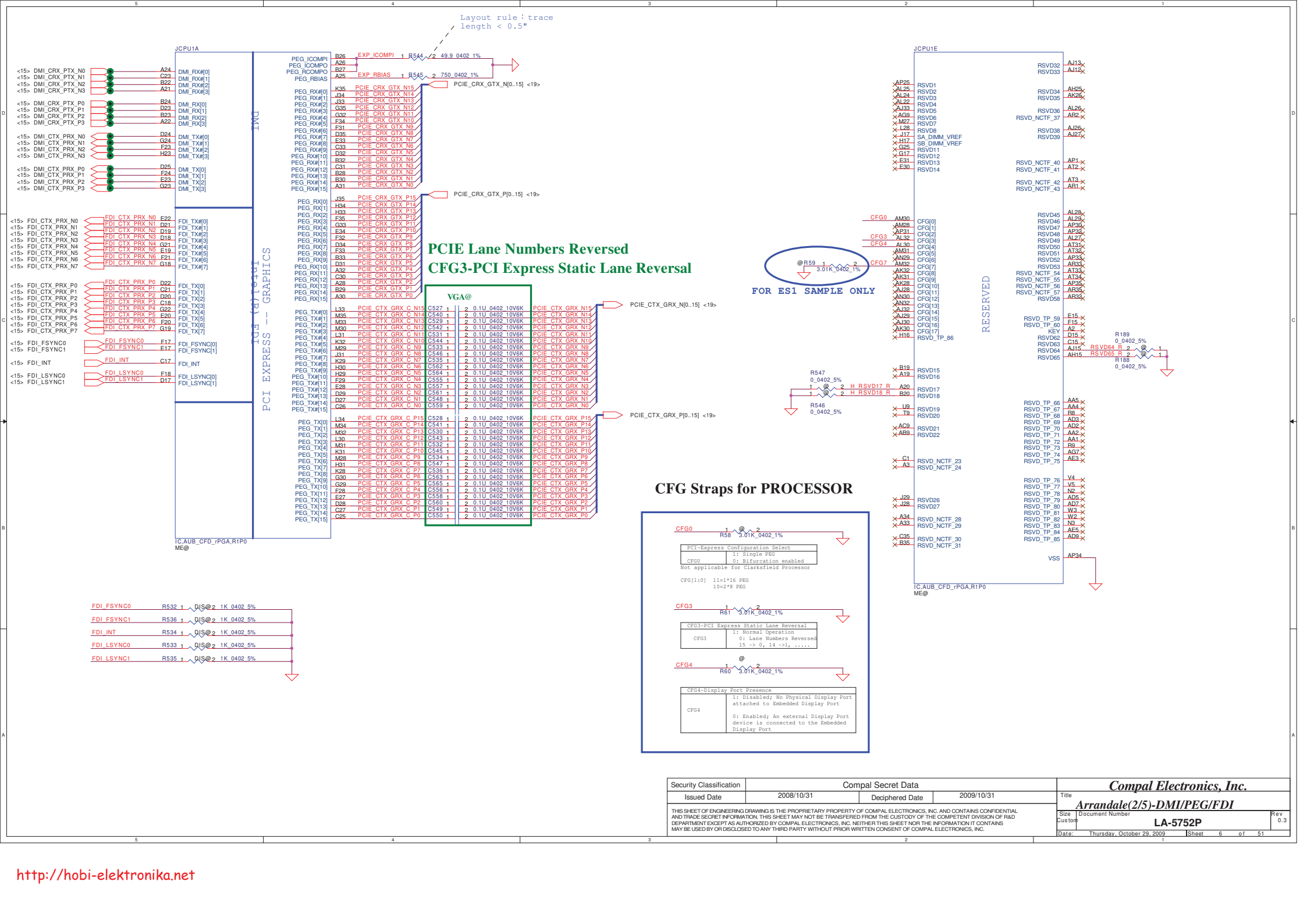
Layout rule: 10mil width trace
length < 0.5", spacing 20mil



**CHECK INTEL DOCUMENT #385422
Debug Port Design Guide Rev1.3**



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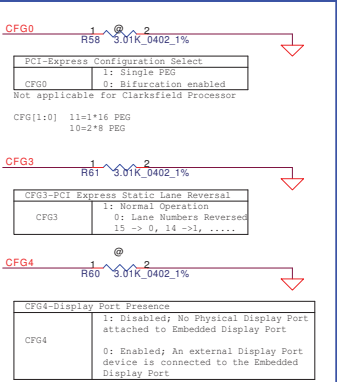
Layout rule: trace length < 0.5"

**PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal**

VGA@

FOR ES1 SAMPLE ONLY

CFG Straps for PROCESSOR



PCI EXPRESS -- GRAPHICS

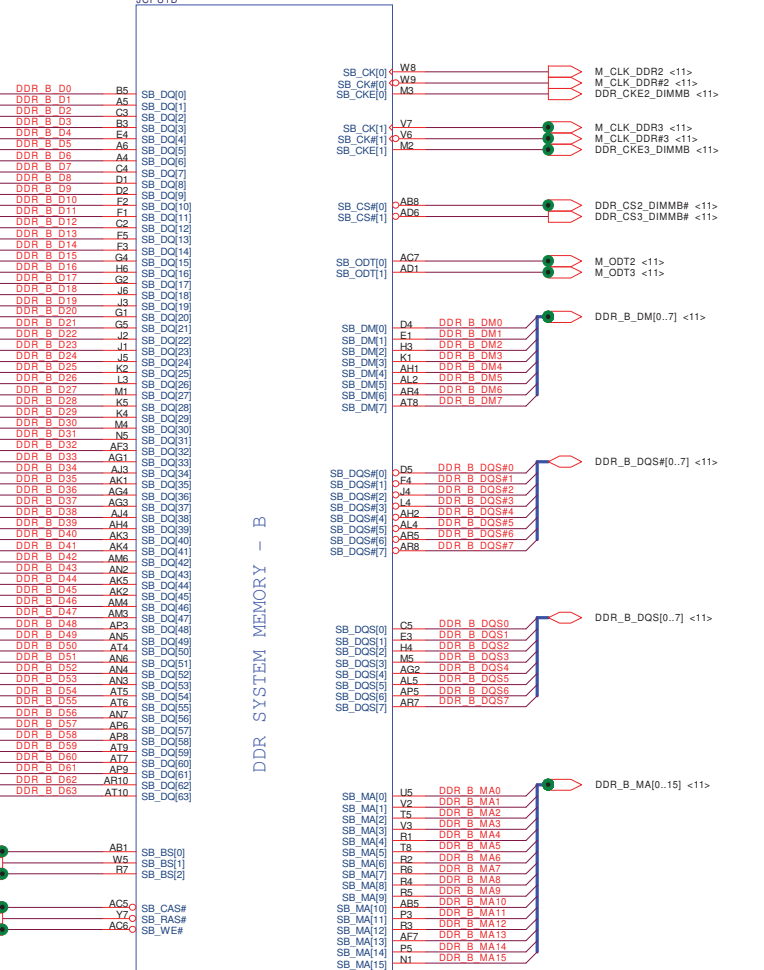
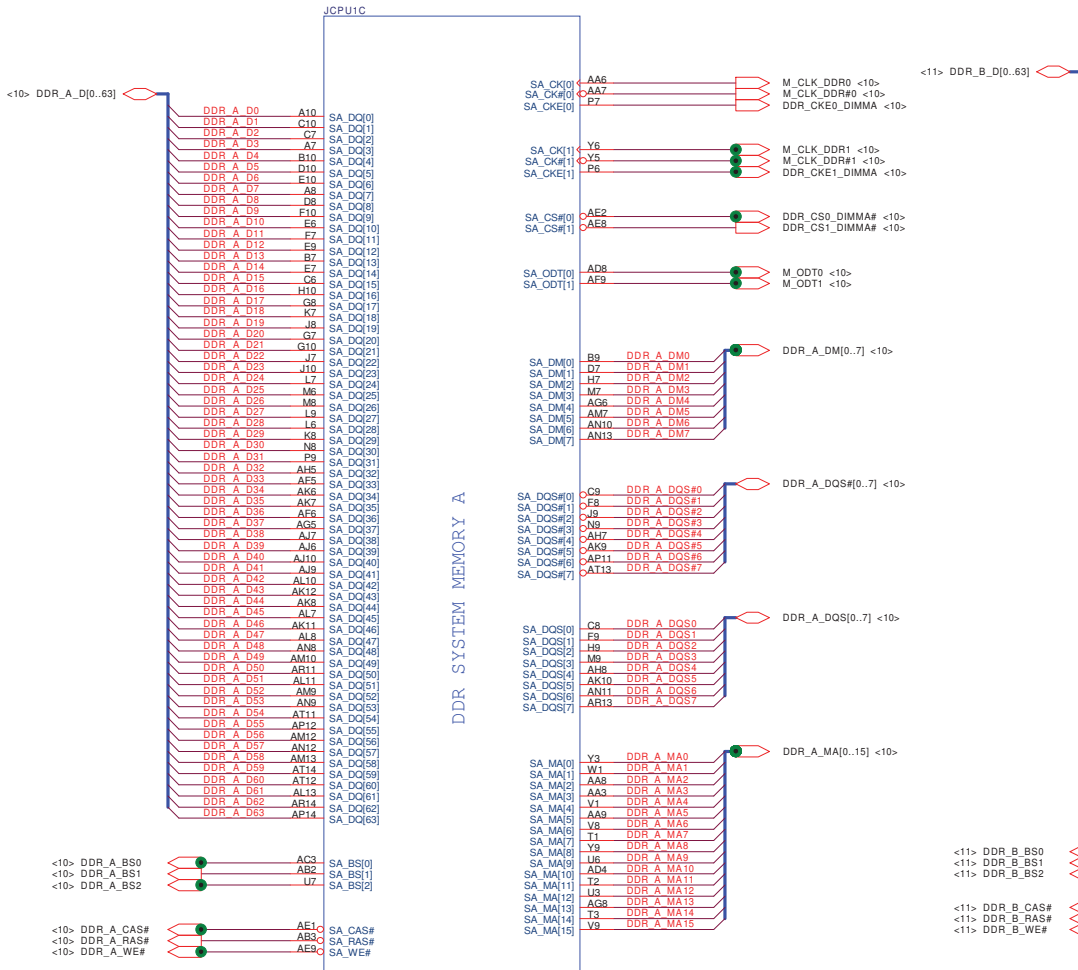
RESERVED

Signal	Value	Unit	Frequency
EXP_ICOMPI	1	R544	2 49.9 0402 1%
EXP_RBIAS	1	R545	2 750 0402 1%

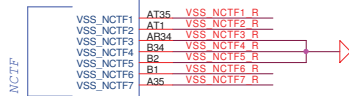
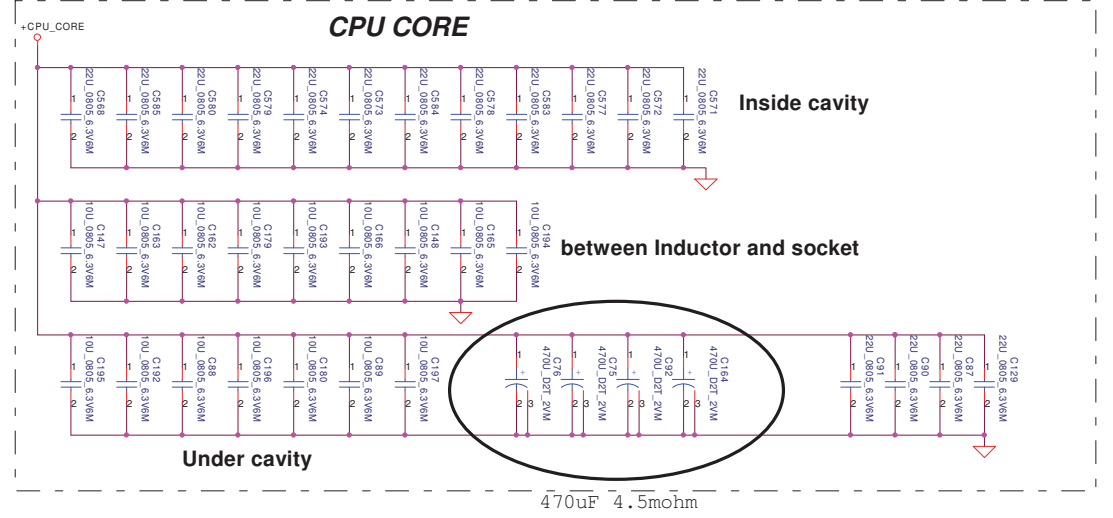
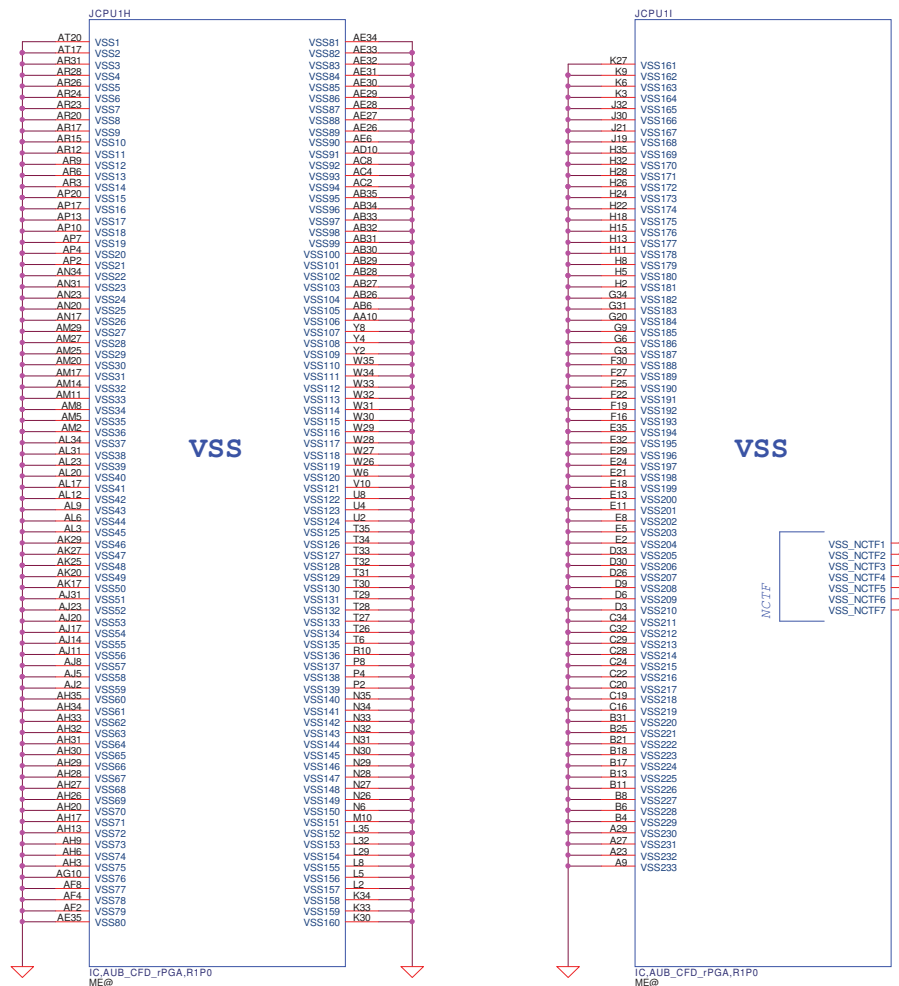
Signal	Value	Unit	Frequency
PCIE_CRX GTX N15	<19>		
PCIE_CRX GTX P15	<19>		
PCIE_CRX GTX N14	<19>		
PCIE_CRX GTX P14	<19>		
PCIE_CRX GTX N13	<19>		
PCIE_CRX GTX P13	<19>		
PCIE_CRX GTX N12	<19>		
PCIE_CRX GTX P12	<19>		
PCIE_CRX GTX N11	<19>		
PCIE_CRX GTX P11	<19>		
PCIE_CRX GTX N10	<19>		
PCIE_CRX GTX P10	<19>		
PCIE_CRX GTX N9	<19>		
PCIE_CRX GTX P9	<19>		
PCIE_CRX GTX N8	<19>		
PCIE_CRX GTX P8	<19>		
PCIE_CRX GTX N7	<19>		
PCIE_CRX GTX P7	<19>		
PCIE_CRX GTX N6	<19>		
PCIE_CRX GTX P6	<19>		
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PCIE_CRX GTX P4	<19>		
PCIE_CRX GTX N3	<19>		
PCIE_CRX GTX P3	<19>		
PCIE_CRX GTX N2	<19>		
PCIE_CRX GTX P2	<19>		
PCIE_CRX GTX N1	<19>		
PCIE_CRX GTX P1	<19>		

Signal	Value	Unit	Frequency
PCIE_CTX GRX C N15	C527	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N14	C540	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N13	C529	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N12	C542	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N11	C531	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N10	C544	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N9	C533	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N8	C546	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N7	C535	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N6	C562	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N5	C564	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N4	C555	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N3	C557	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N2	C561	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N1	C548	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C N0	C559	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P15	C528	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P14	C541	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P13	C530	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P12	C543	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P11	C532	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P10	C545	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P9	C534	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P8	C547	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P7	C536	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P6	C563	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P5	C565	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P4	C556	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P3	C558	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P2	C560	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P1	C549	1	2 0.1U 0402 10VK6
PCIE_CTX GRX C P0	C550	1	2 0.1U 0402 10VK6

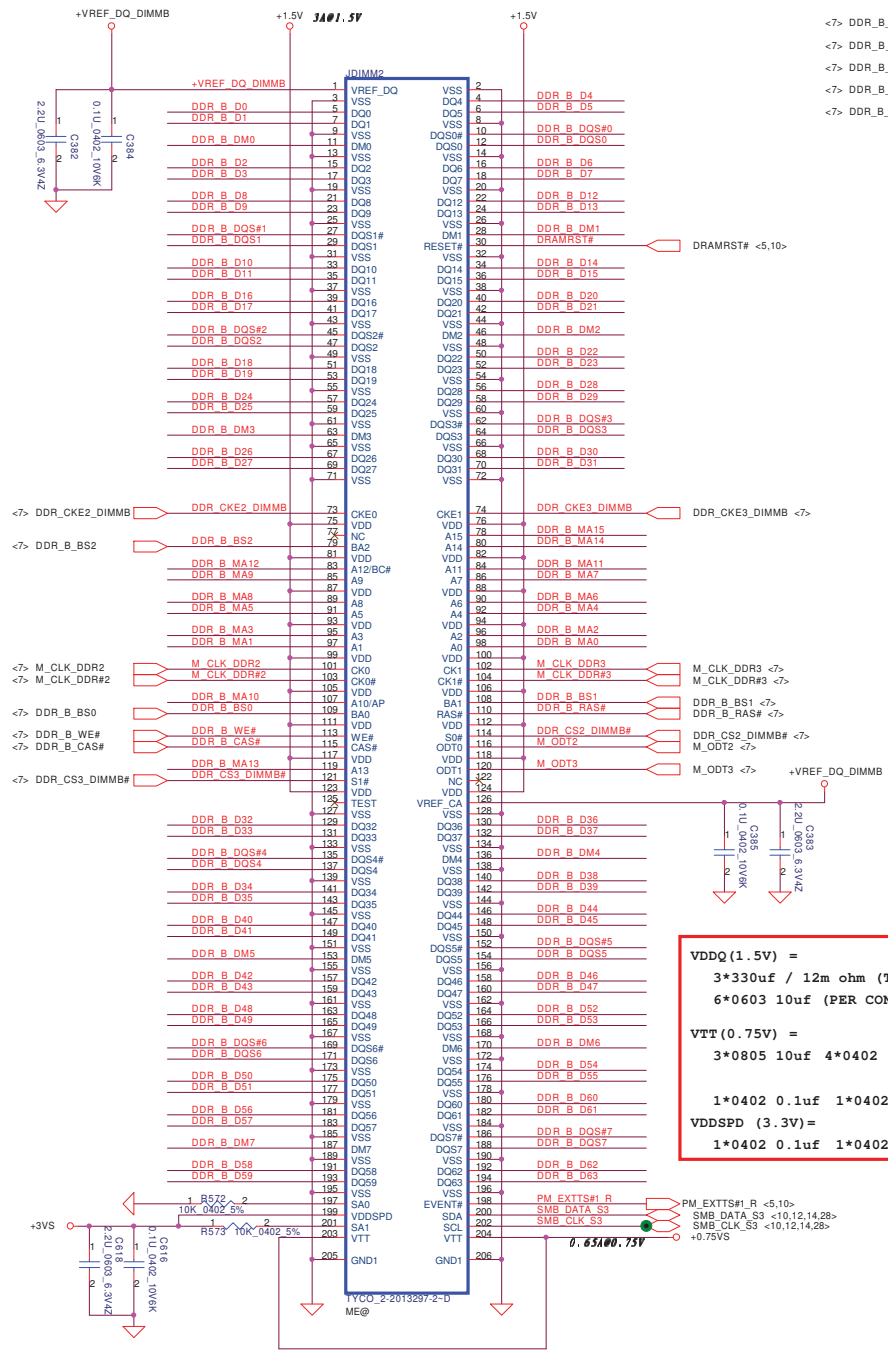
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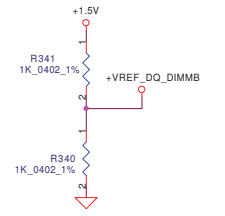
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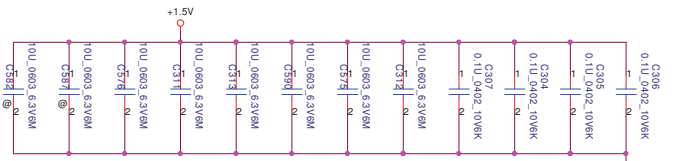


- <7> DDR_B_DQS#0[0..7]
- <7> DDR_B_D0[0..63]
- <7> DDR_B_DM0[0..7]
- <7> DDR_B_DQS#0[0..7]
- <7> DDR_B_MA[0..15]

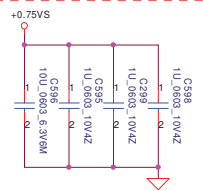


For Arranale only +VREF_DQ_DIMMB supply from an external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



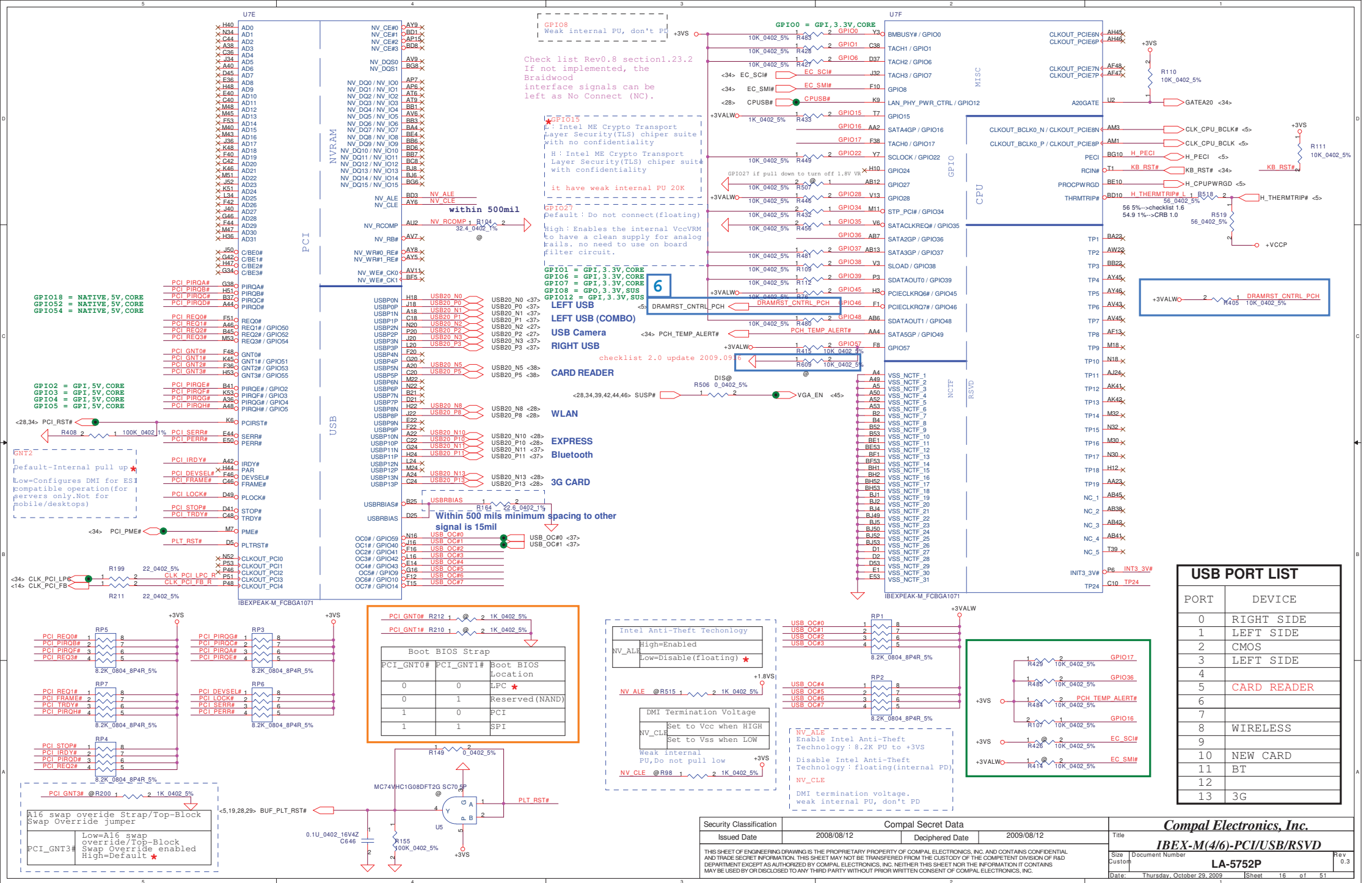
VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT (0.75V) =
3*0805 10uf 4*0402 1uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

1*0402 0.1uf 1*0402 2.2uf

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				DDR3-SODIMM SLOT2
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Check list Rev0.8 section1.23.2
If not implemented, the
Braidwood
interface signals can be
left as No Connect (NC).

Intel ME Crypto Transport
Layer Security (TLS) chipser suite
with no confidentiality
H: Intel ME Crypto Transport
Layer Security (TLS) chipser suite
with confidentiality
it have weak internal PU 20K

Default: Do not connect (floating)
High: Enables the internal VccVRM
to have a clean supply for analog
rails. no need to use on board
filter circuit.

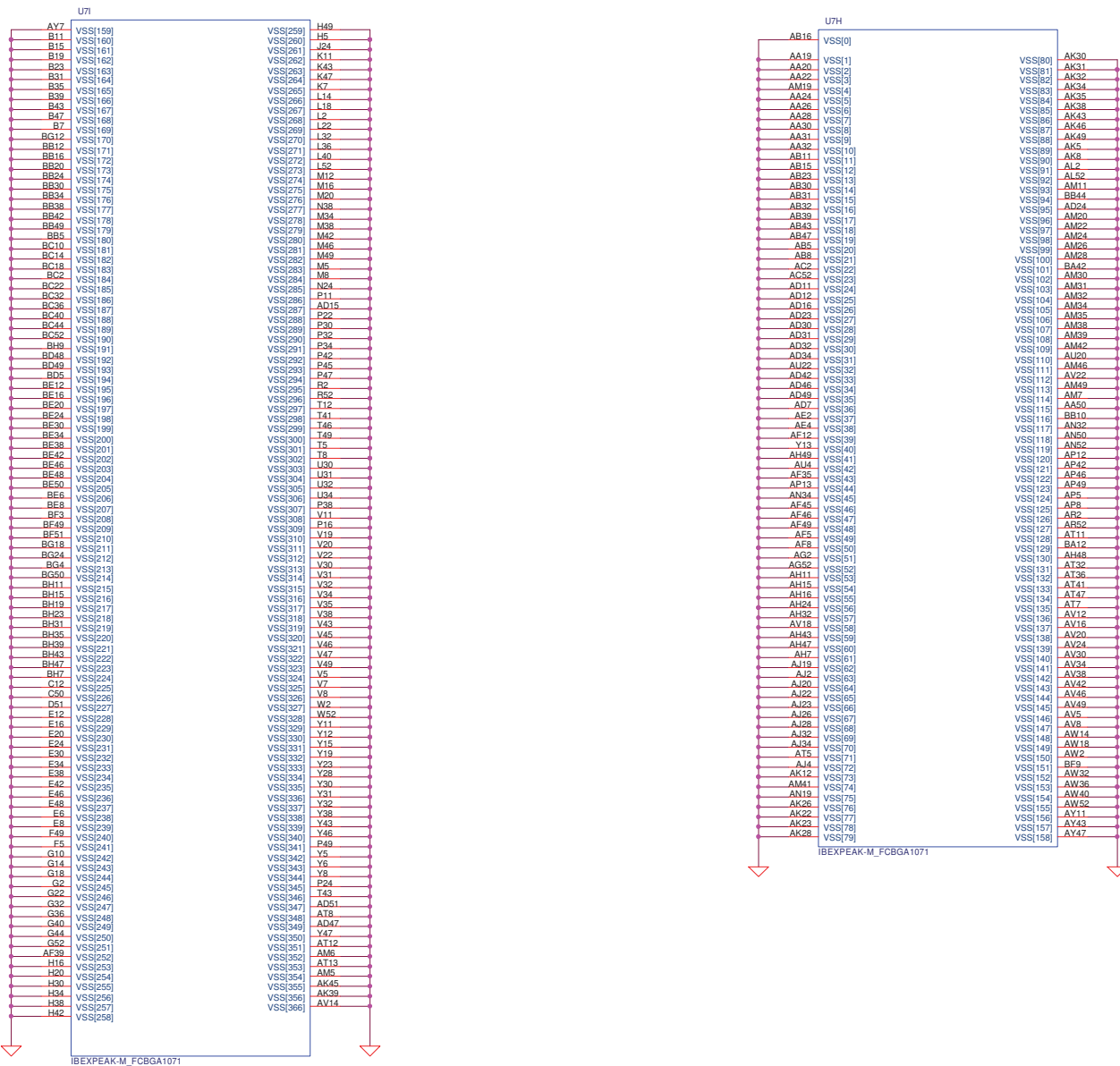
checklist 2.0 update 2009.09.6

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	
5	CARD READER
6	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

Security Classification	Compal Secret Data
Issued Date	2008/08/12
Deciphered Date	2009/08/12

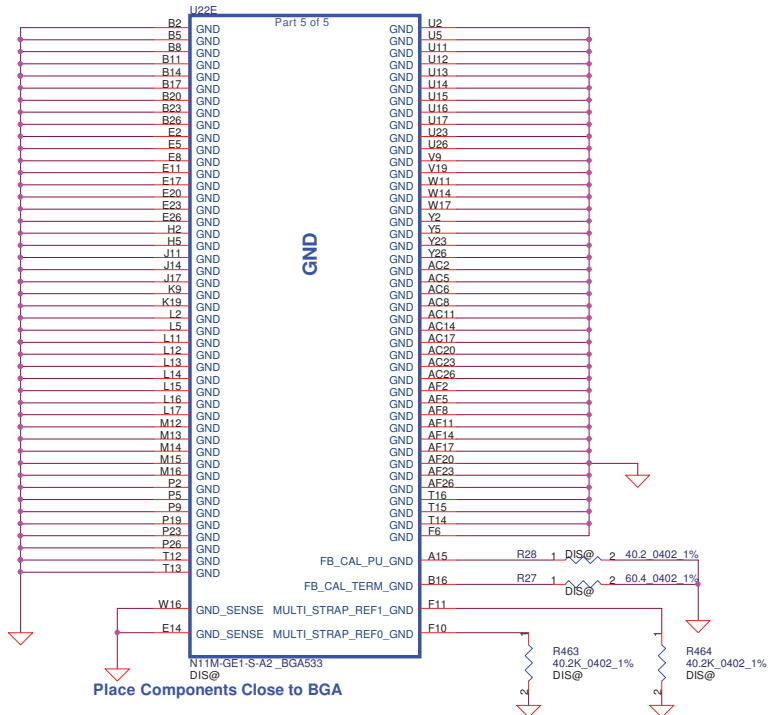
Compal Electronics, Inc.	
IBEX-M(4/6)-PCI/USB/RSVD	
Title	Document Number
Rev	LA-5752P
Date	Thursday, October 29, 2009
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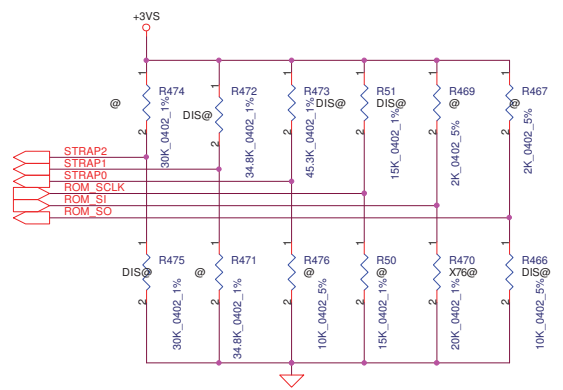
Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	Compal Electronics, Inc.
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A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



Place Components Close to BGA

<20> STRAP2
 <20> STRAP1
 <20> STRAP0
 <20> ROM_SCLK
 <20> ROM_SI
 <20> ROM_SO



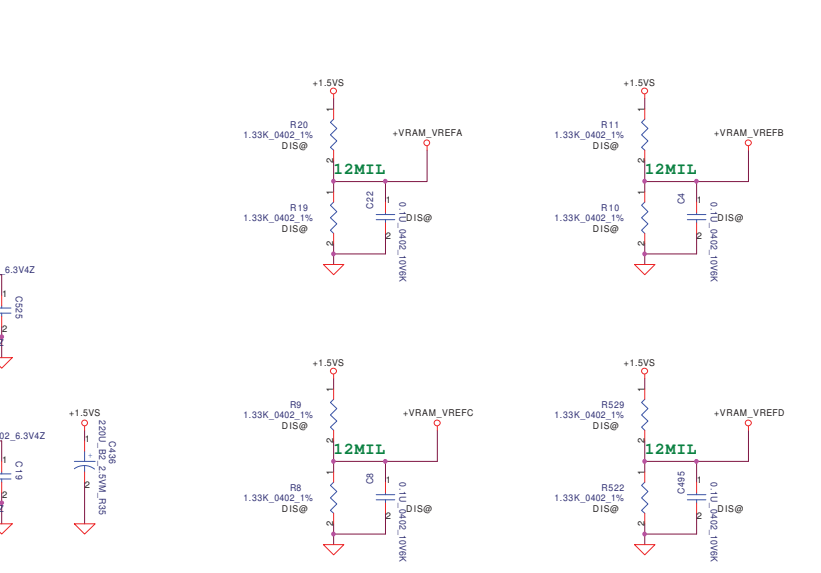
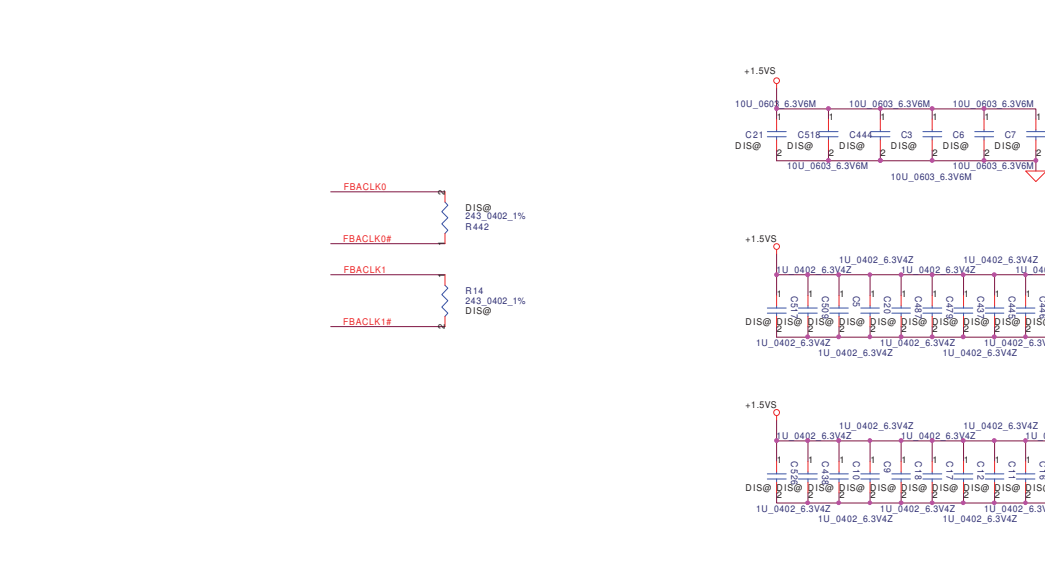
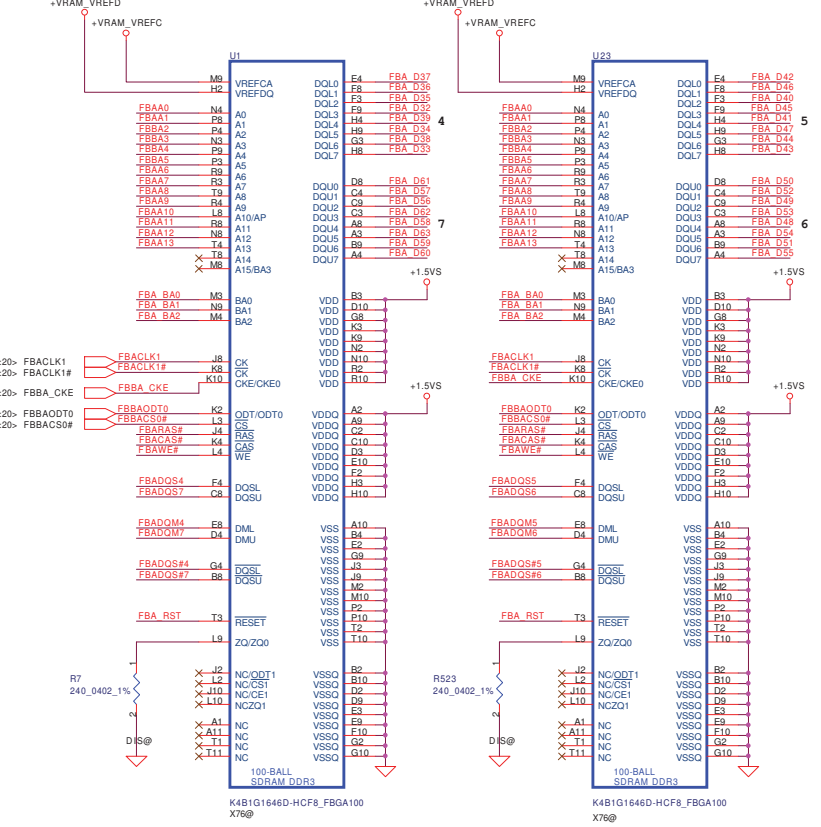
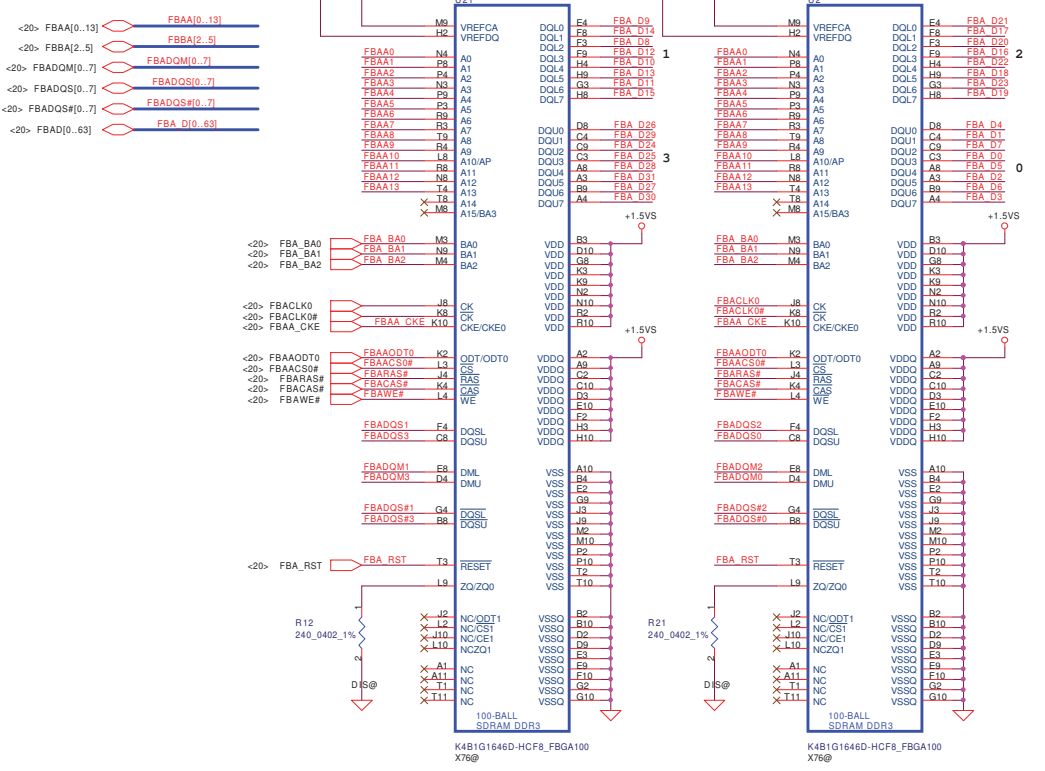
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
 (PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
	64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
Hynix 800MHz	H5TQ1G63BFR-12C						
	64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
				X76			

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

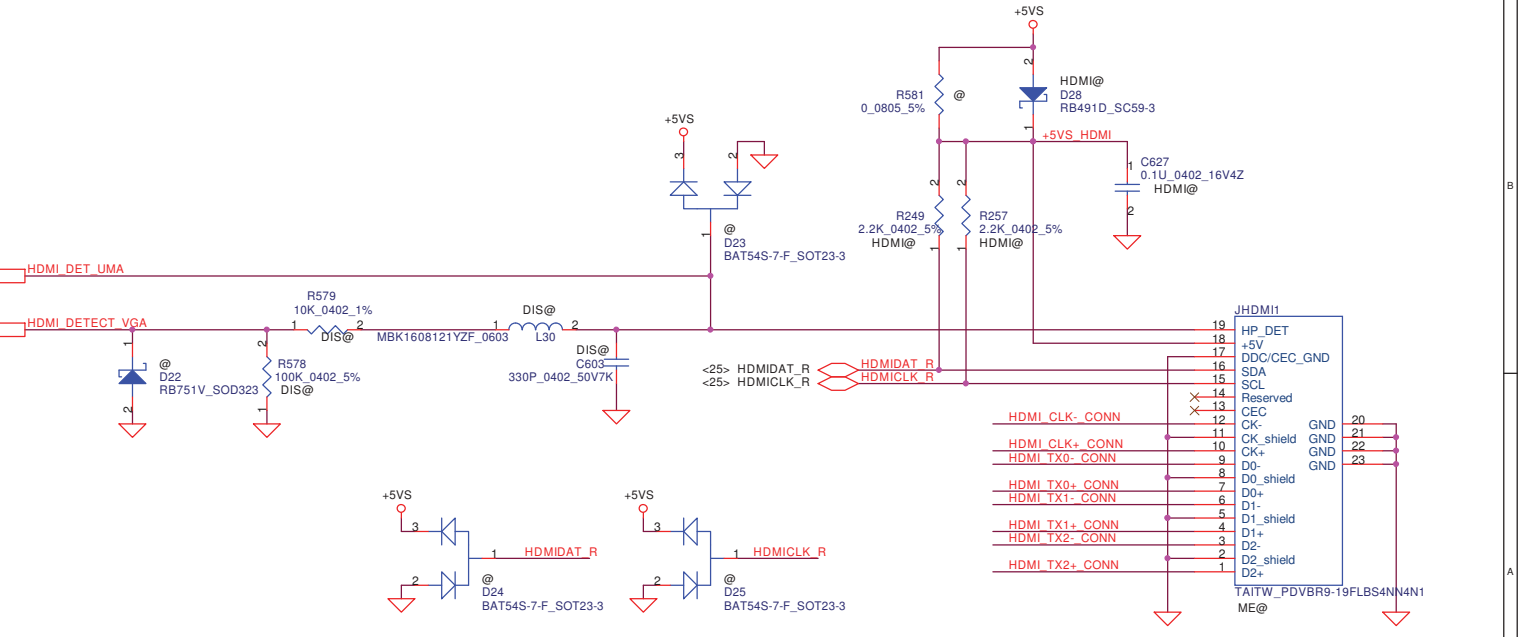
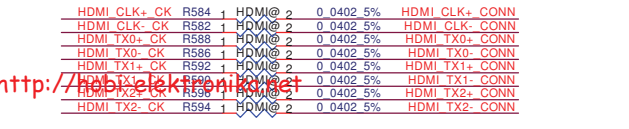
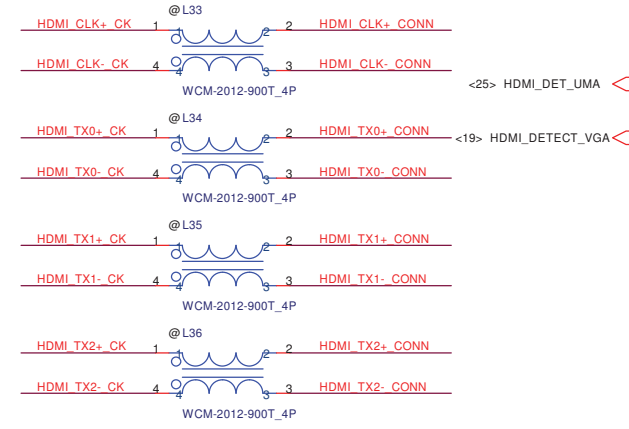
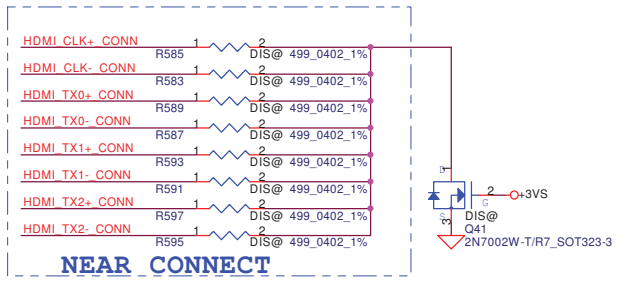
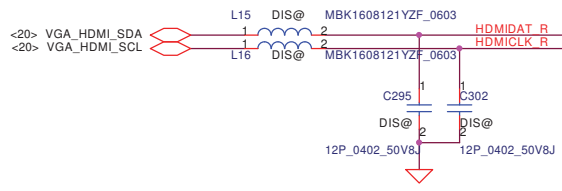
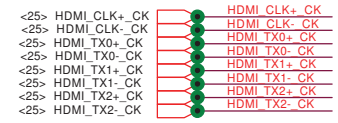
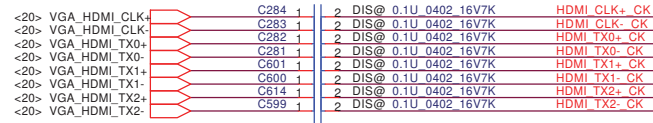
Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



<http://hobi-elektronika.net>

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Title	VRAM DDR3			
Size	Document Number	LA-5752P		Rev. 0.3
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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	
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Size	Document Number			Rev	0.3
Custom	LA-5752P				
Date: Thursday, October 29, 2009	Sheet	24	of	51	

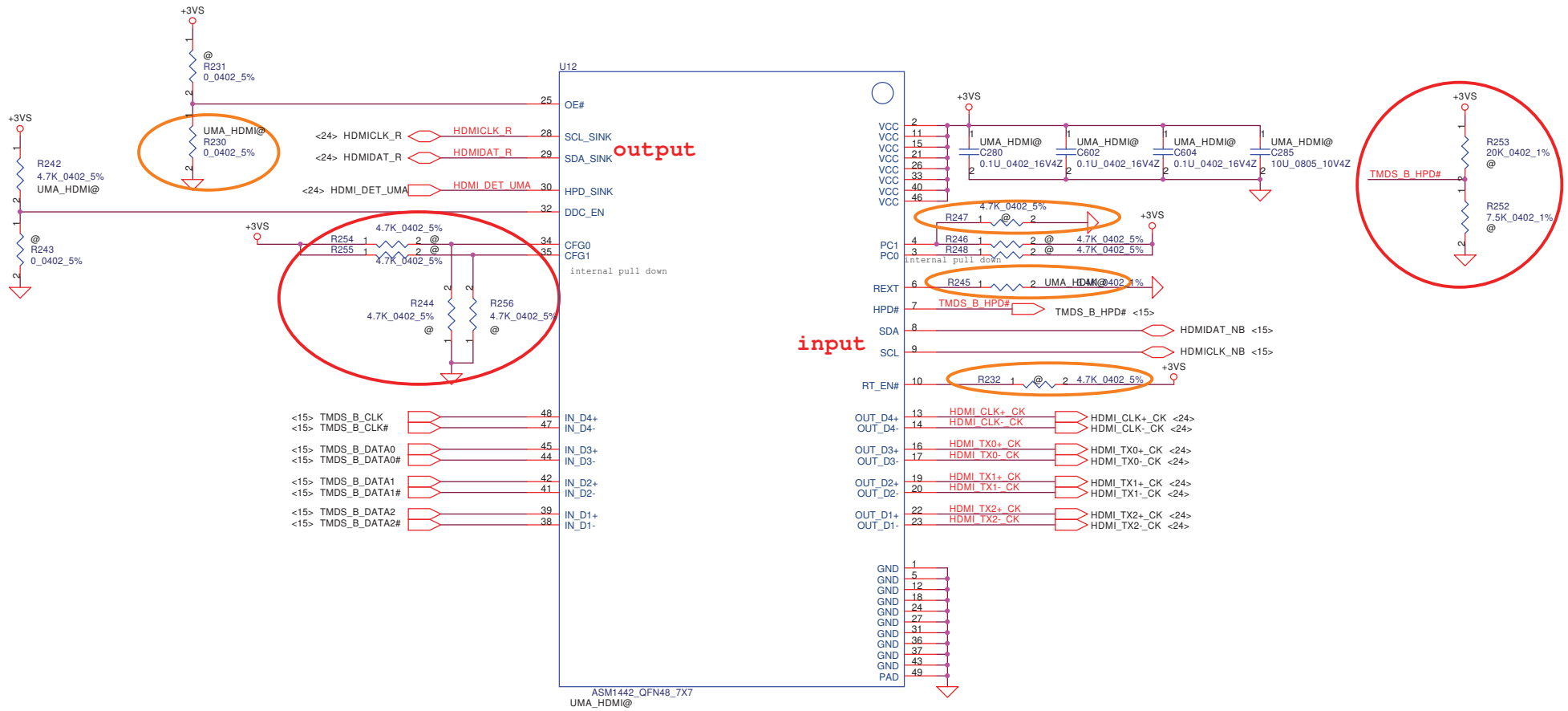
<http://www.compalelectronics.com>

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P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

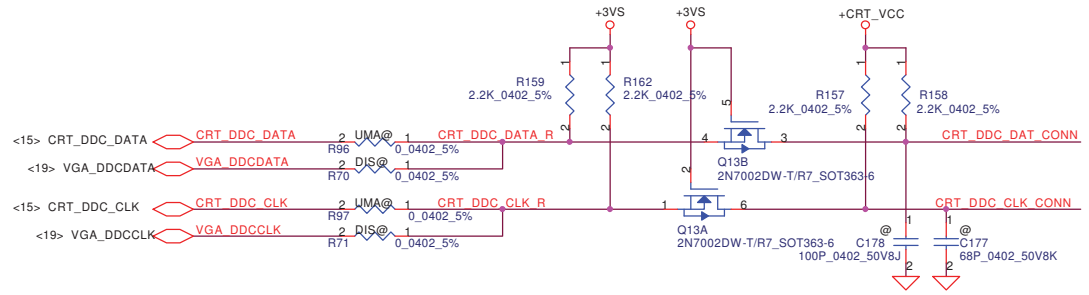
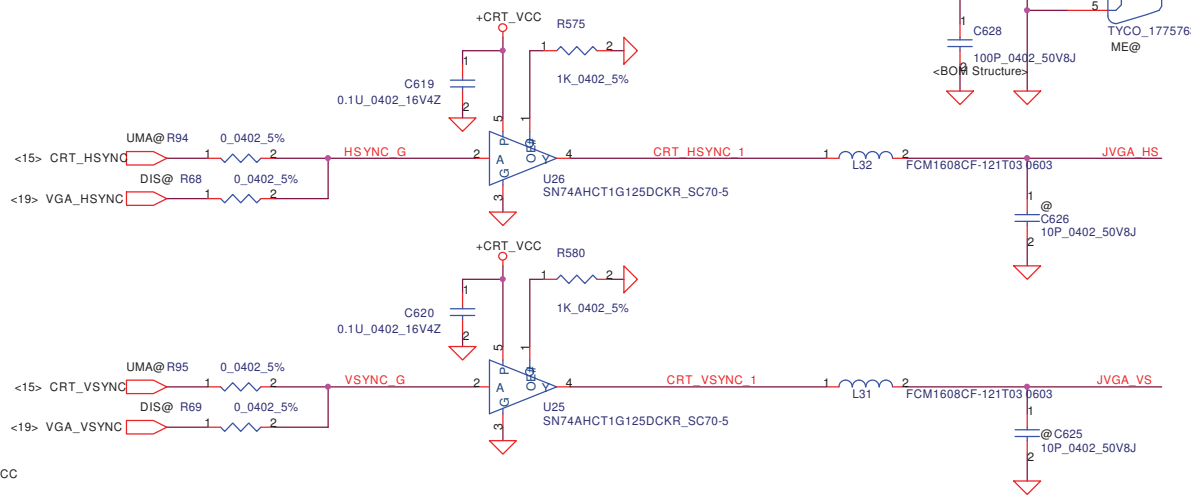
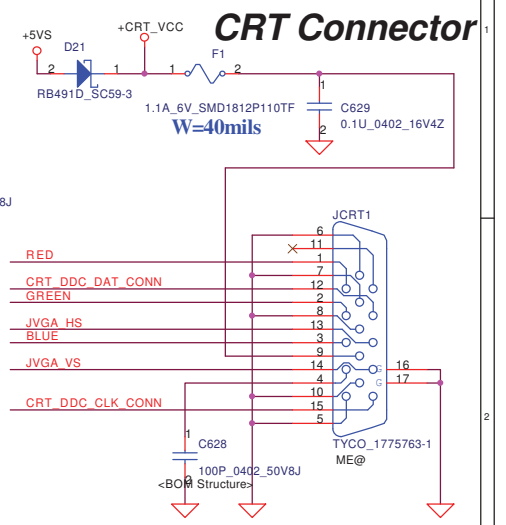
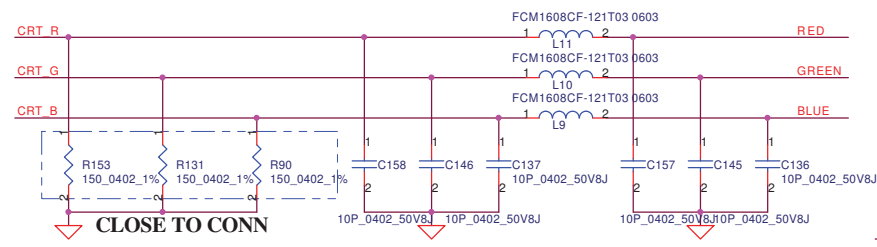
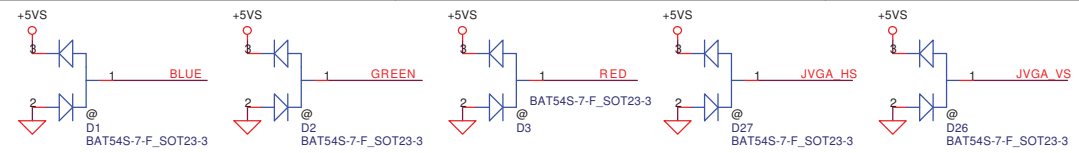
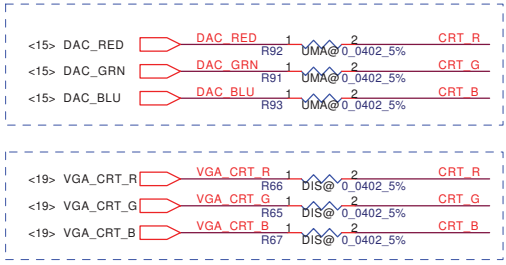
FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R483 FROM 499 TO 3.4K OHM

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm



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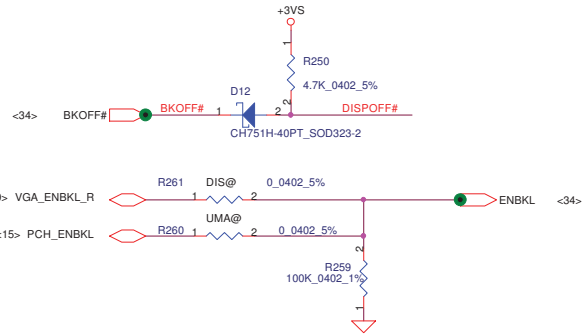
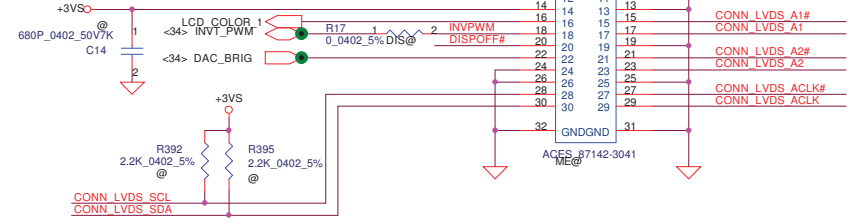
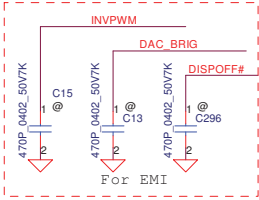
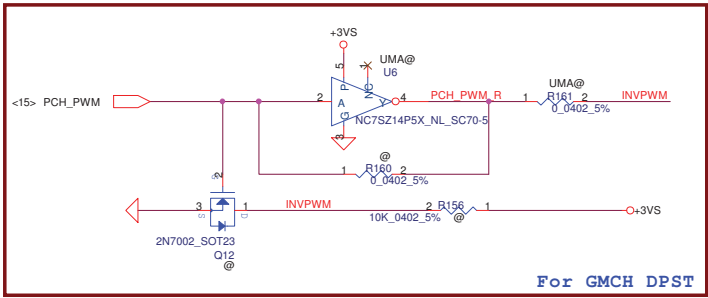
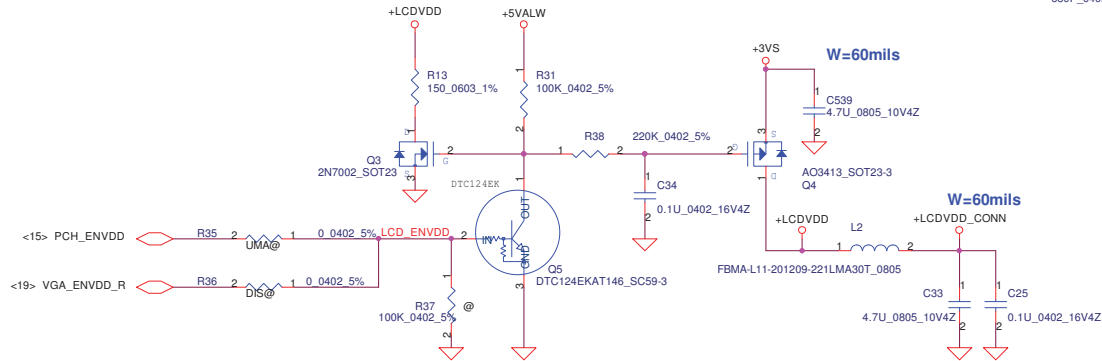
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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shifter_ASM1442
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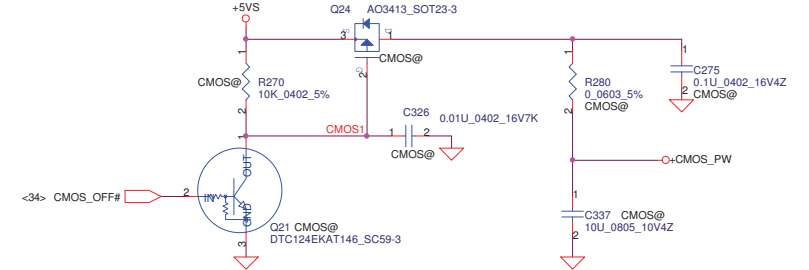
<http://hobi-elektronika.net>

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Size	Document Number	Rev		0.3	
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LCD POWER CIRCUIT



CMOS Camera



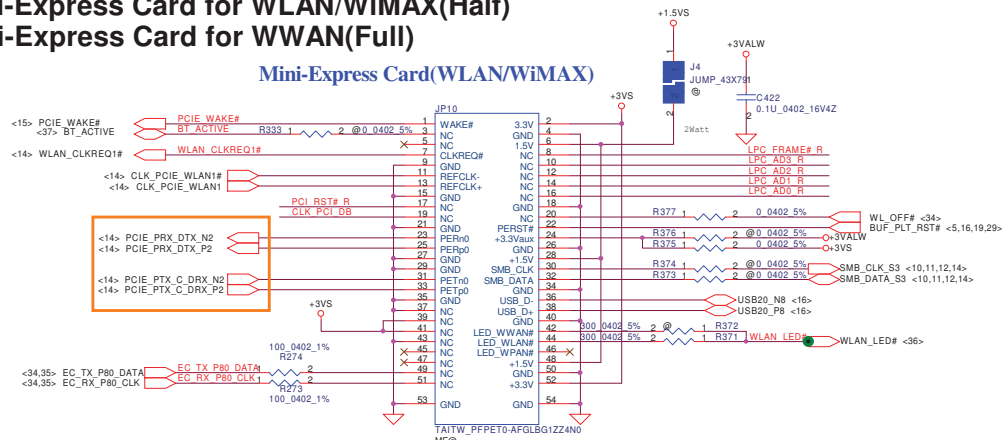
- <19> VGA_LVDS_SCL VGA_LVDS_SCL 0.0402 5% 2 DIS@ 1 R390 CONN_LVDS_SCL
- <19> VGA_LVDS_SDA VGA_LVDS_SDA 0.0402 5% 2 DIS@ 1 R391 CONN_LVDS_SDA
- <20> VGA_LVDS_A0 VGA_LVDS_A0 0.0402 5% 2 DIS@ 1 R86 CONN_LVDS_A0
- <20> VGA_LVDS_A0# VGA_LVDS_A0# 0.0402 5% 2 DIS@ 1 R85 CONN_LVDS_A0#
- <20> VGA_LVDS_A1 VGA_LVDS_A1 0.0402 5% 2 DIS@ 1 R150 CONN_LVDS_A1
- <20> VGA_LVDS_A1# VGA_LVDS_A1# 0.0402 5% 2 DIS@ 1 R128 CONN_LVDS_A1#
- <20> VGA_LVDS_A2 VGA_LVDS_A2 0.0402 5% 2 DIS@ 1 R126 CONN_LVDS_A2
- <20> VGA_LVDS_A2# VGA_LVDS_A2# 0.0402 5% 2 DIS@ 1 R127 CONN_LVDS_A2#
- <20> VGA_LVDS_ACLK VGA_LVDS_ACLK 0.0402 5% 2 DIS@ 1 R84 CONN_LVDS_ACLK
- <20> VGA_LVDS_ACLK# VGA_LVDS_ACLK# 0.0402 5% 2 DIS@ 1 R125 CONN_LVDS_ACLK#
- <15> EDID_CLK EDID_CLK 0.0402 5% 2 UMA@ 1 R393 CONN_LVDS_SCL
- <15> EDID_DATA EDID_DATA 0.0402 5% 2 UMA@ 1 R394 CONN_LVDS_SDA
- <15> LVDS_A0 LVDS_A0 0.0402 5% 2 UMA@ 1 R383 CONN_LVDS_A0
- <15> LVDS_A0# LVDS_A0# 0.0402 5% 2 UMA@ 1 R382 CONN_LVDS_A0#
- <15> LVDS_A1 LVDS_A1 0.0402 5% 2 UMA@ 1 R389 CONN_LVDS_A1
- <15> LVDS_A1# LVDS_A1# 0.0402 5% 2 UMA@ 1 R388 CONN_LVDS_A1#
- <15> LVDS_A2 LVDS_A2 0.0402 5% 2 UMA@ 1 R386 CONN_LVDS_A2
- <15> LVDS_A2# LVDS_A2# 0.0402 5% 2 UMA@ 1 R387 CONN_LVDS_A2#
- <15> LVDS_ACLK LVDS_ACLK 0.0402 5% 2 UMA@ 1 R384 CONN_LVDS_ACLK
- <15> LVDS_ACLK# LVDS_ACLK# 0.0402 5% 2 UMA@ 1 R385 CONN_LVDS_ACLK#

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<http://www.ktronika.net>

Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for WWAN(Full)

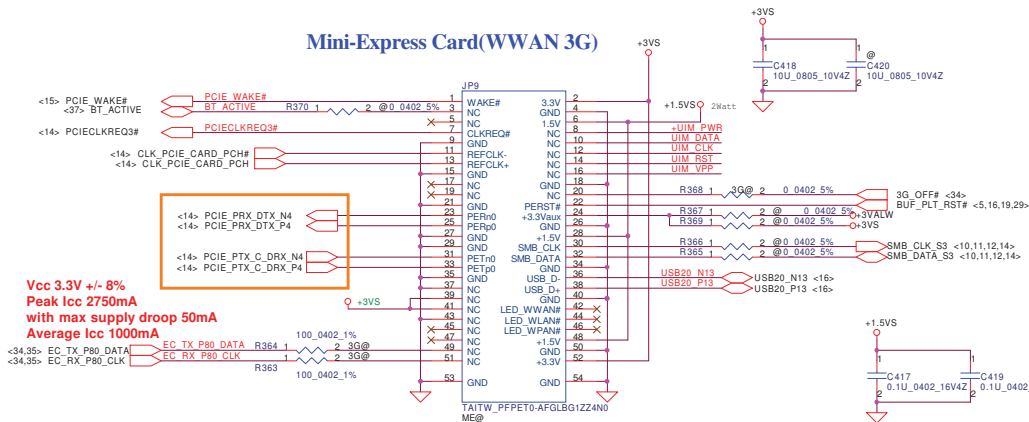
Mini-Express Card(WLAN/WiMAX)



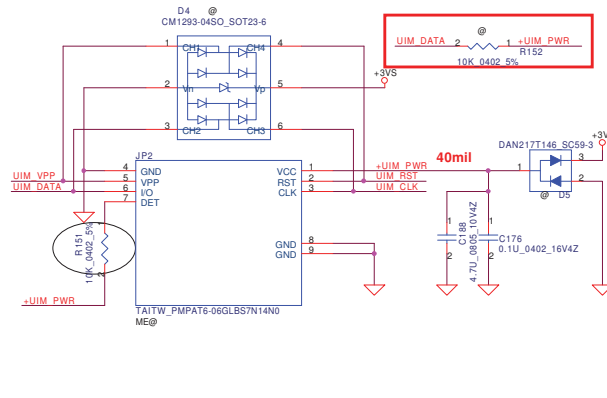
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC FRAME# R	R284	1	2	0.0402 5%	LPC FRAME#	<13,34>
LPC AD3 R	R285	1	2	0.0402 5%	LPC AD3	<13,34>
LPC AD2 R	R286	1	2	0.0402 5%	LPC AD2	<13,34>
LPC AD1 R	R287	1	2	0.0402 5%	LPC AD1	<13,34>
LPC ADD R	R288	1	2	0.0402 5%	LPC ADD	<13,34>
PCI RST# R	R290	1	2	0.0402 5%	PCI RST#	<13,34>
CLK PCI DB	R290	1	2	0.0402 5%	CLK PCI DB	<14>

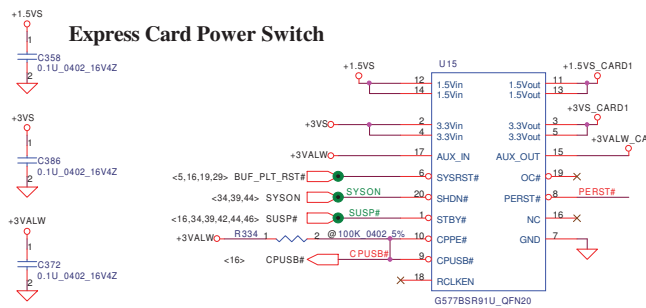
Mini-Express Card(WWAN 3G)



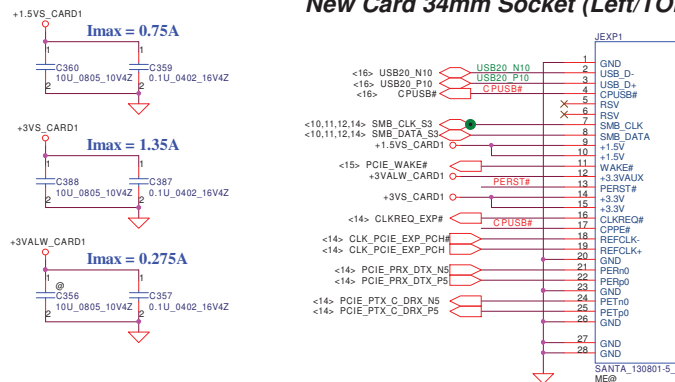
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



Express Card Power Switch

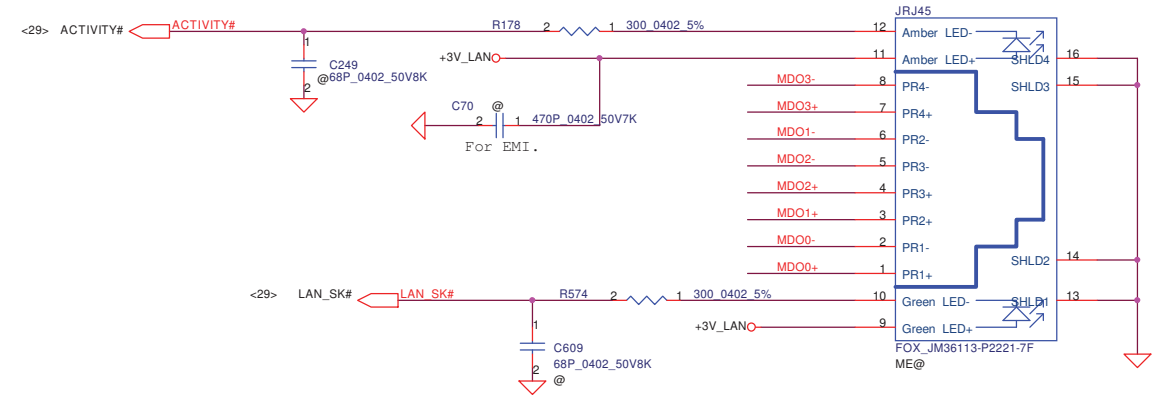
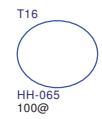
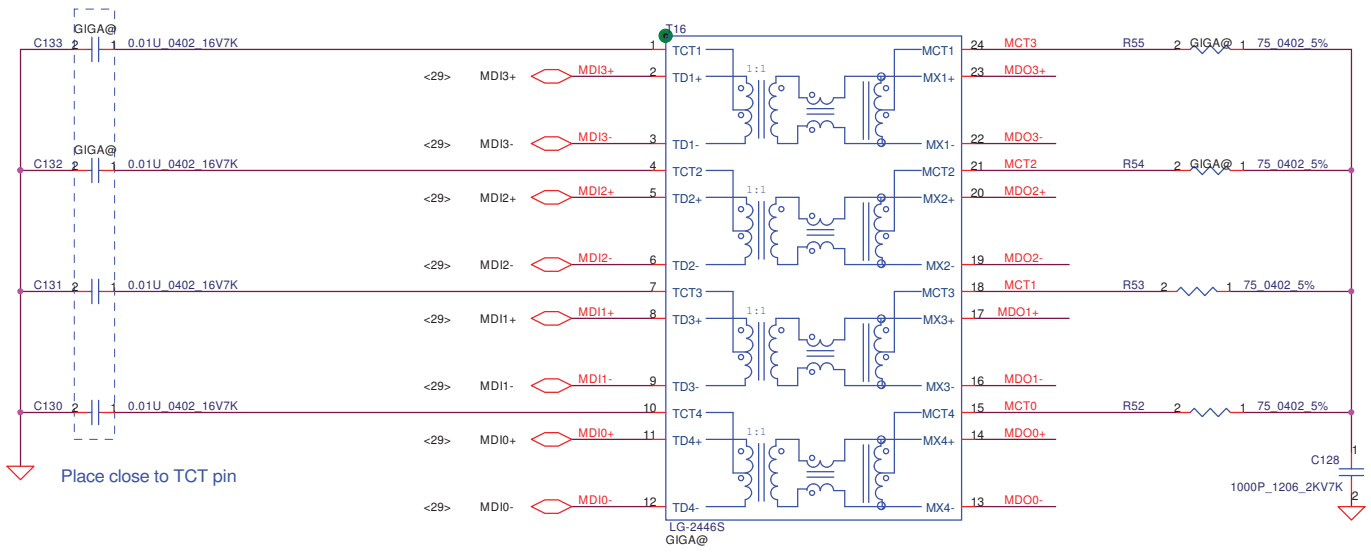


New Card 34mm Socket (Left/TOP)



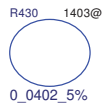
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Close to T14

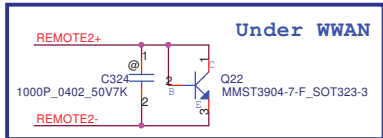
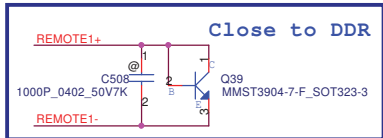
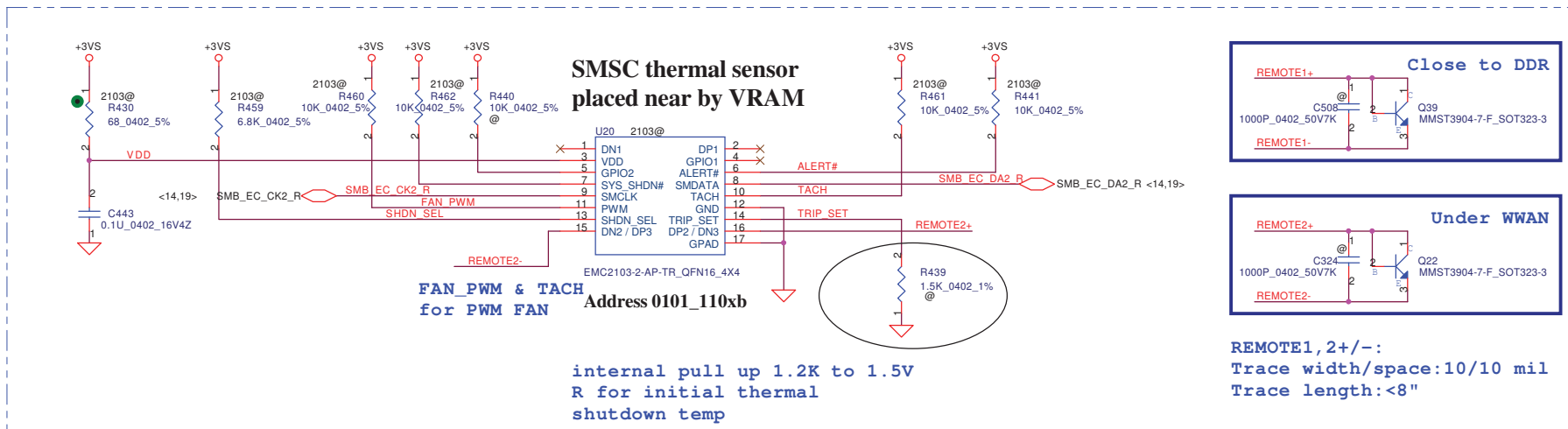


RJ45 Conn.

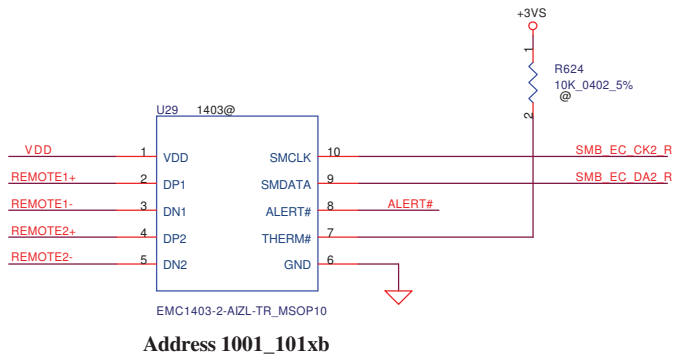
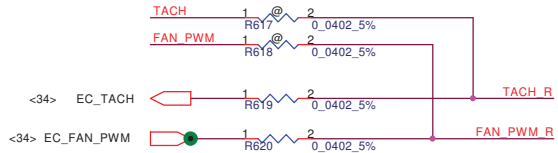
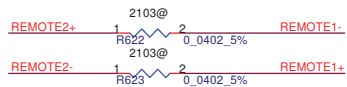
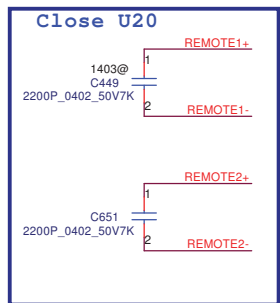
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/03/20	Deciphered Date	2010/03/20	Title	
				LAN_Transformer	
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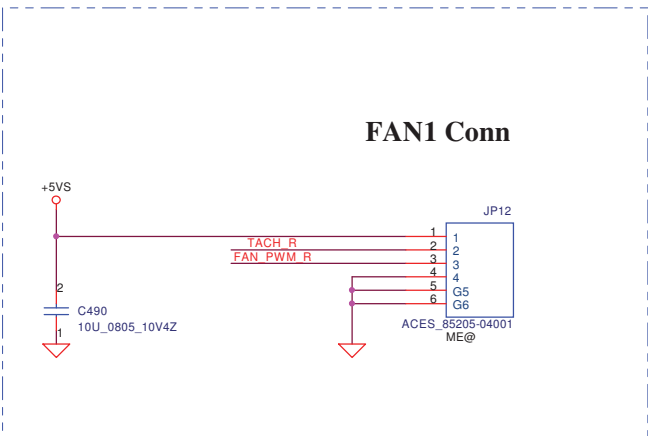
1403:
@C508/@C324=100p



REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"



Address 1001_101xb

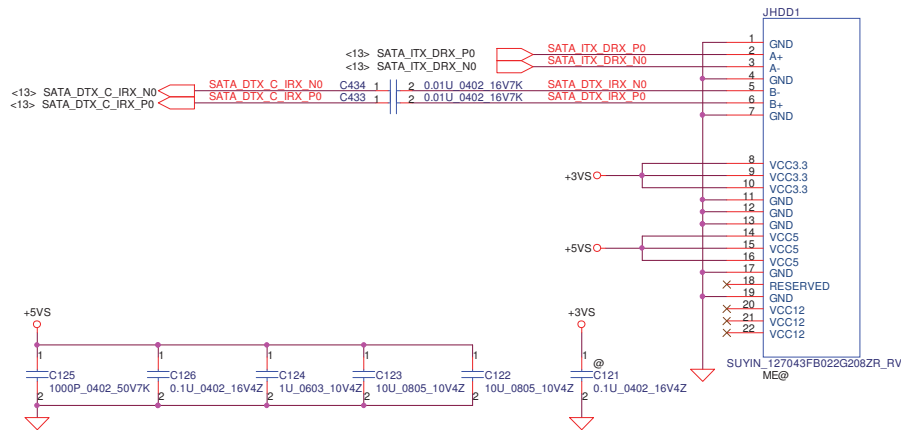


Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
105	2050ohm

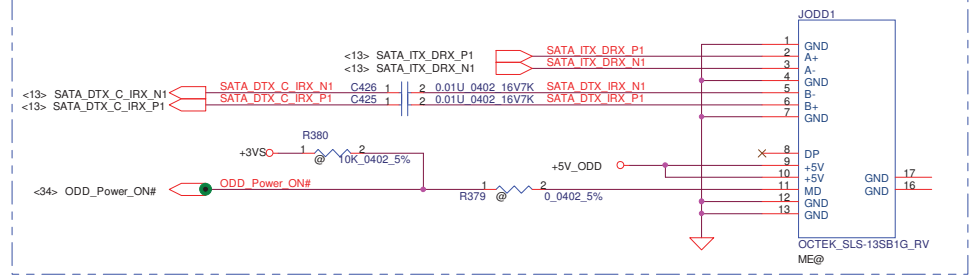
<http://hobi-electronics.net>

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	EMC2103/1403_Thermal sensor/FAN
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Date:	Thursday, October 29, 2009	Sheet	31 of 51	Rev	0.3

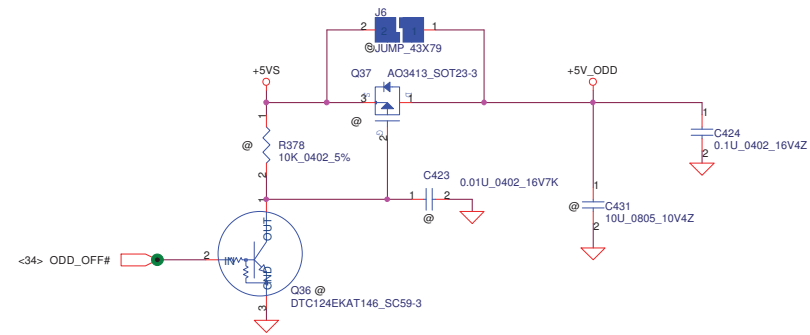
SATA HDD Conn.



SATA ODD Conn.

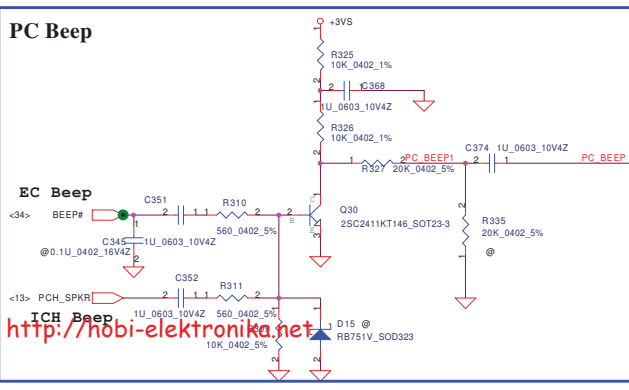
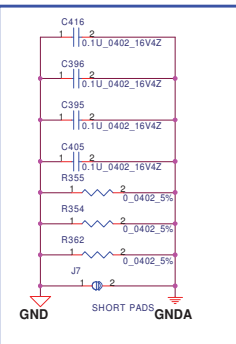
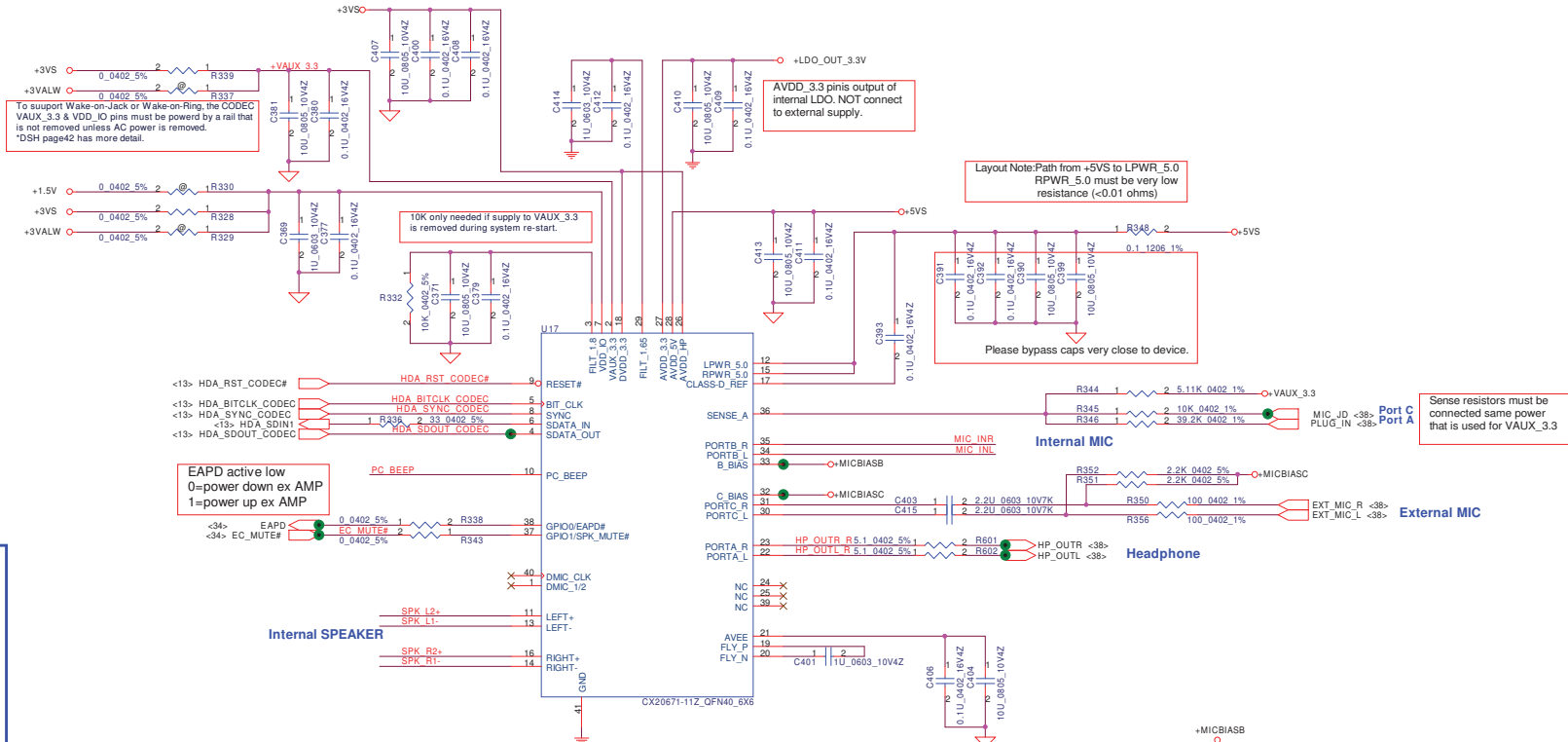
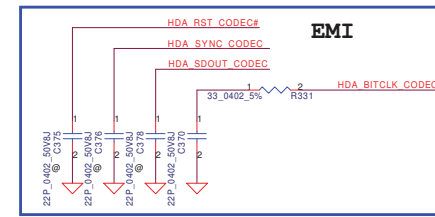


ODD Power Control

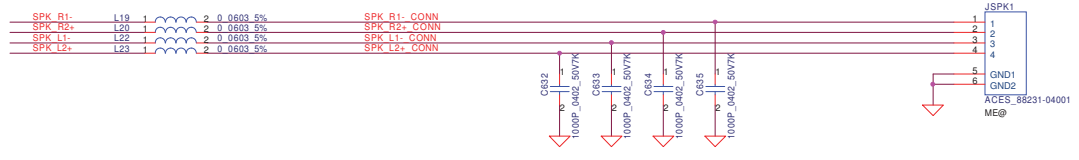


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc. HDD/ODD Connector		
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				LA-5752P Date: Thursday, October 29, 2009 Sheet 32 of 51		

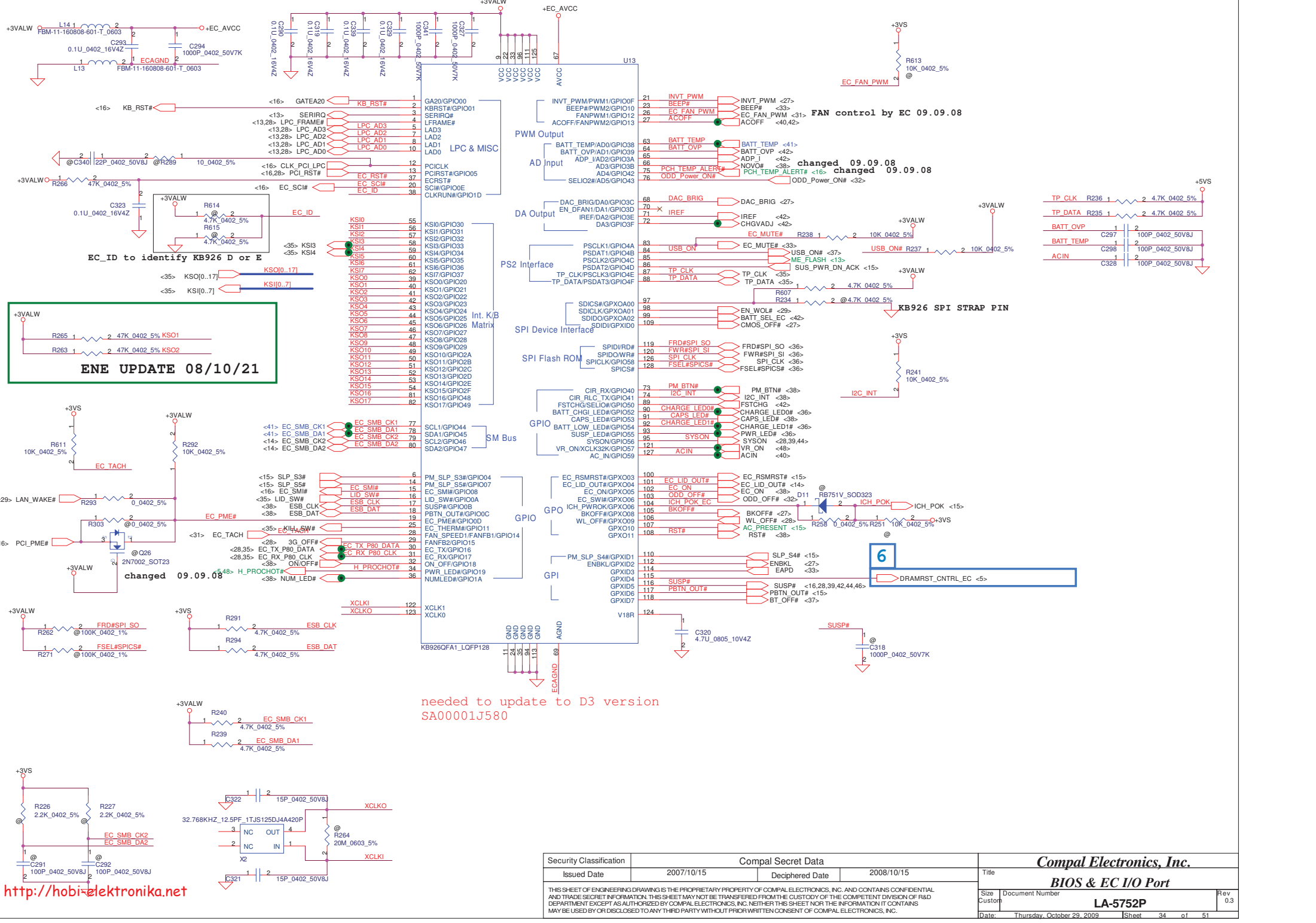
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



wide 20MIL



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title
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Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	BIOS & EC I/O Port
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Size	Document Number	Rev		0.3
Customer	LA-5752P	Date		Thursday, October 29, 2009
Date		Thursday, October 29, 2009	Sheet	34 of 51

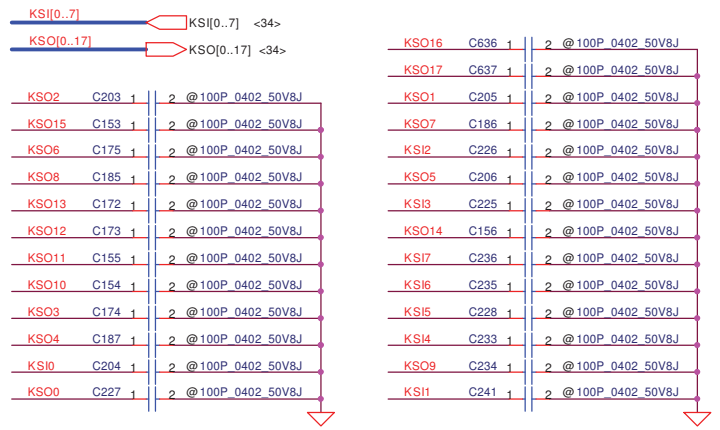
Compal Electronics, Inc.

BIOS & EC I/O Port

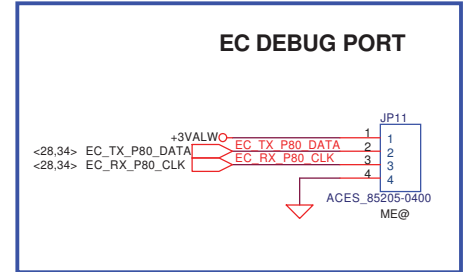
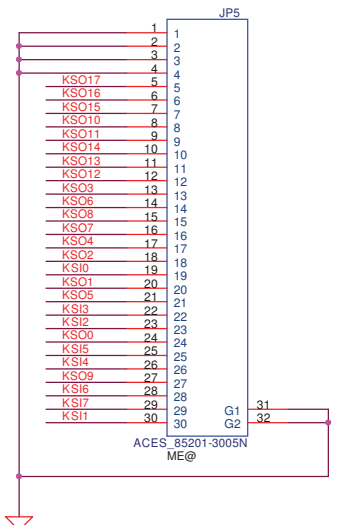
LA-5752P

Rev 0.3

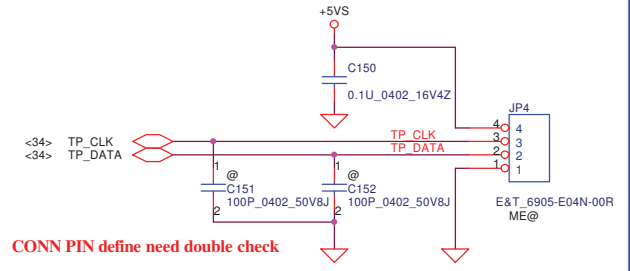
INT_KBD Conn.



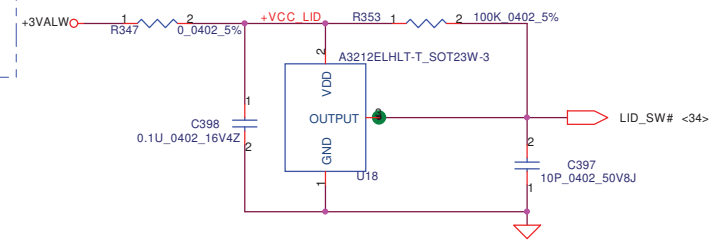
reversal of NIWE1



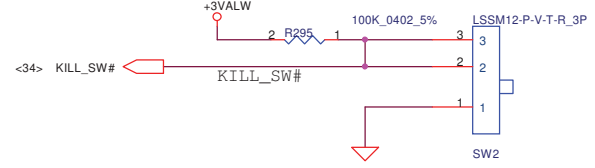
To TP/B Conn.



Lid Switch

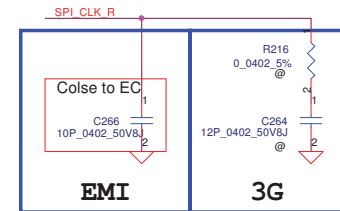
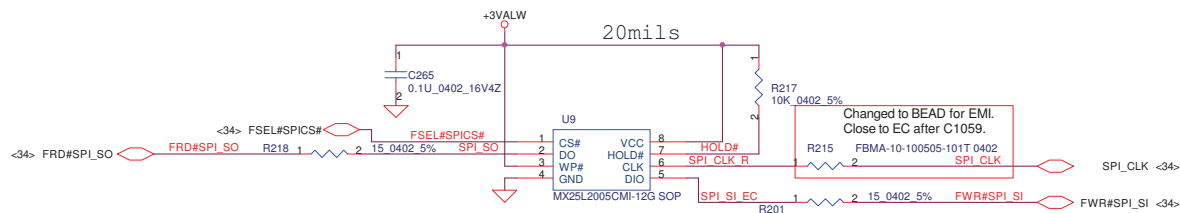


Kill Switch



Kill	
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

**FOR EC 256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00**

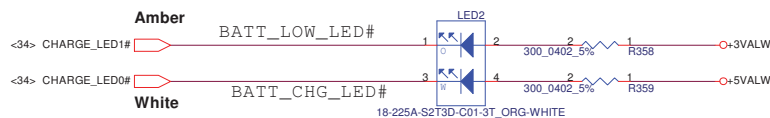


LED

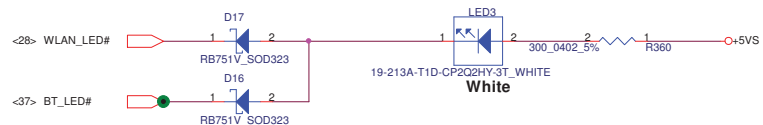
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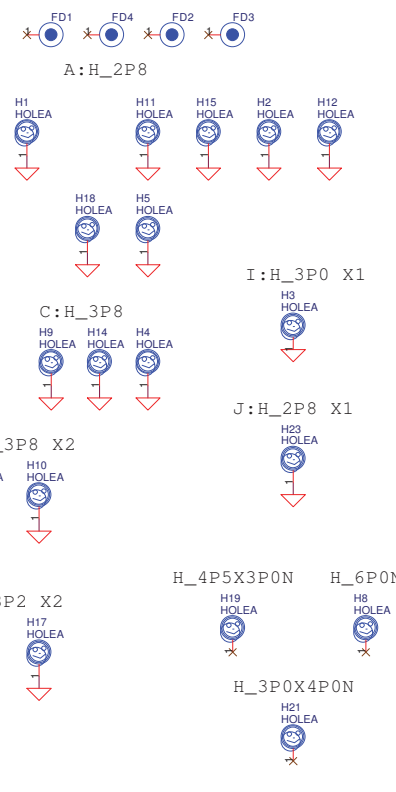
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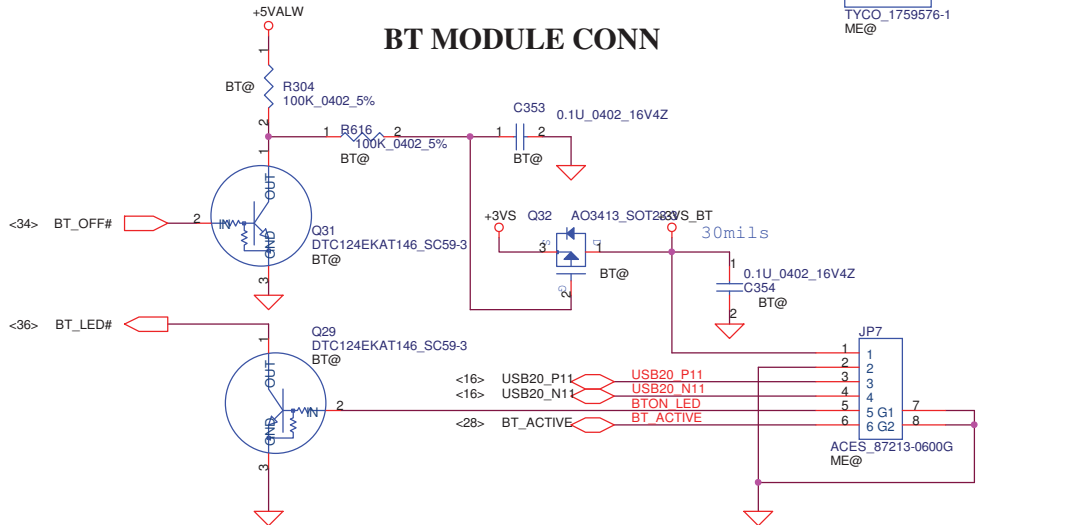
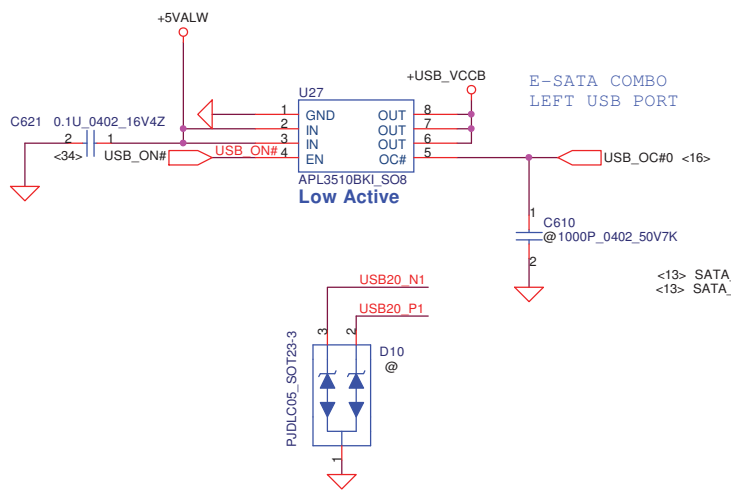
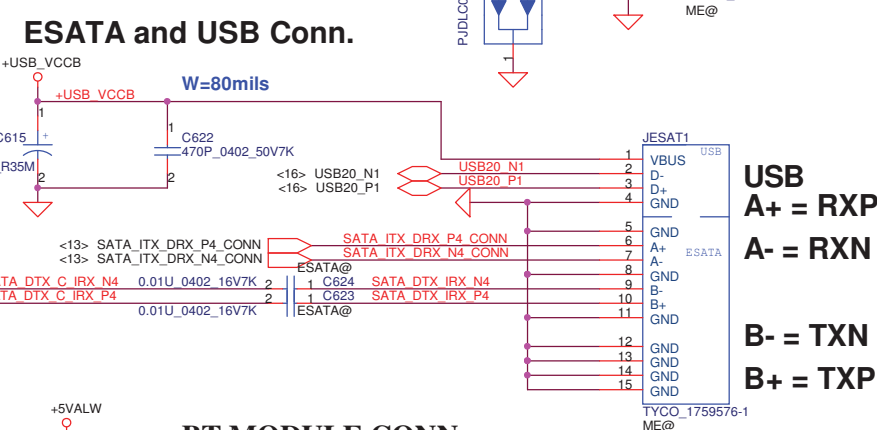
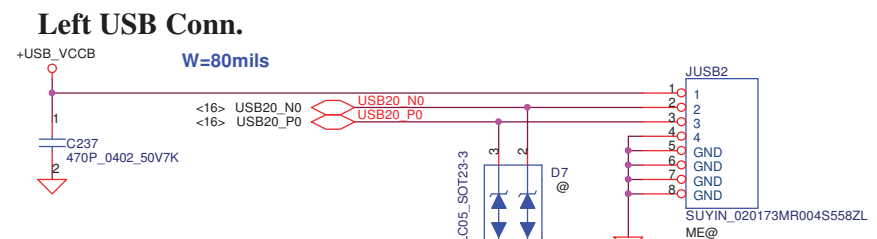
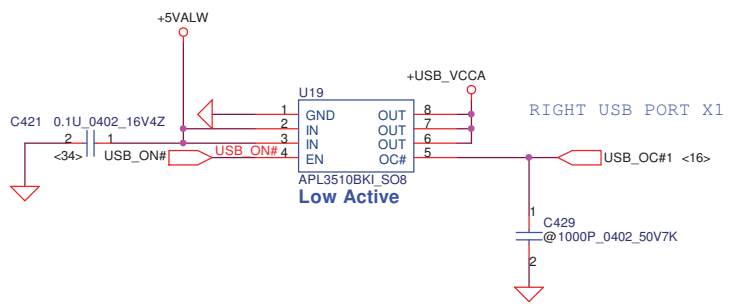
SC500005B00



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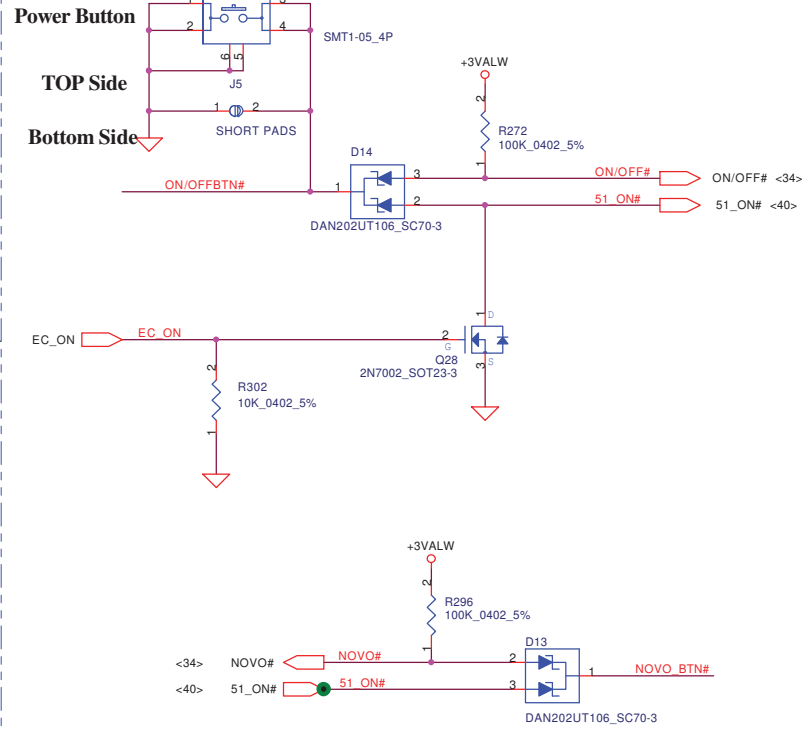


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Size B	Document Number		LA-5752P	Rev 0.3
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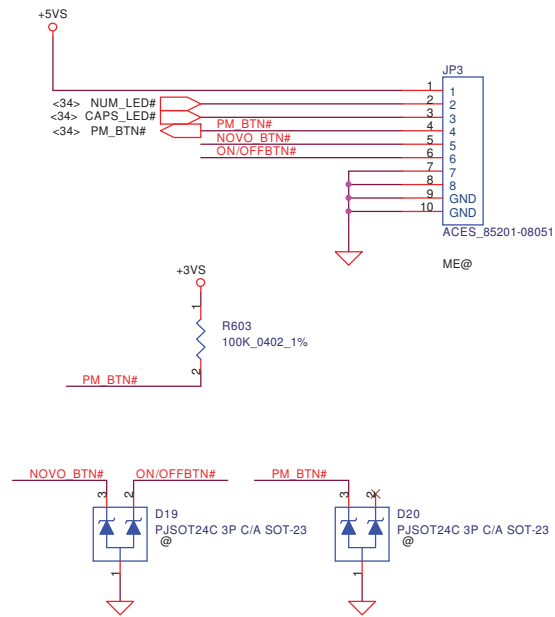


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Size	Document Number	Rev		Date	
Custom	LA-5752P	0.3		Thursday, October 29, 2009	
				Sheet 37 of 51	

ON/OFF switch

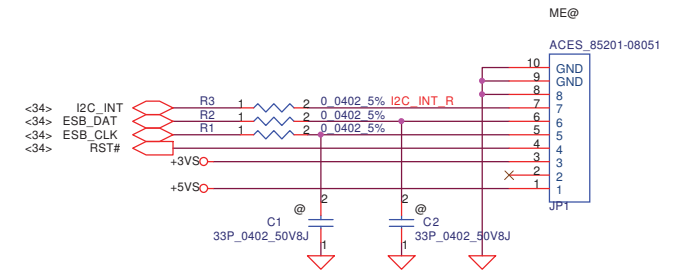


Power Bottom Board Conn. 8pin

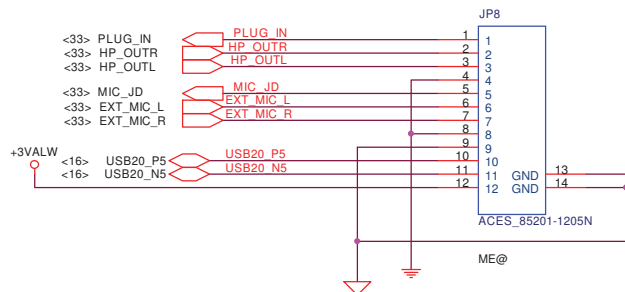


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Cap Sensor Board Conn. 6pin ENE SB3534

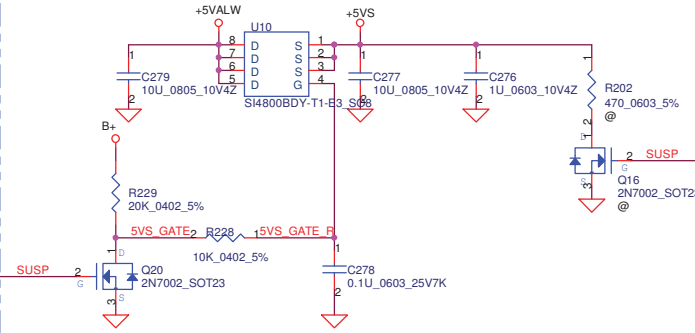


Card Reader/Audio Jack SB CONN

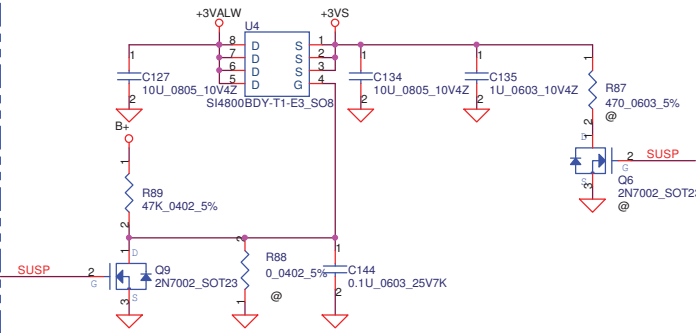


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Size	Document Number	LA-5752P		Rev
Custom				0.3
Date:	Thursday, October 29, 2009	Sheet	38 of 51	

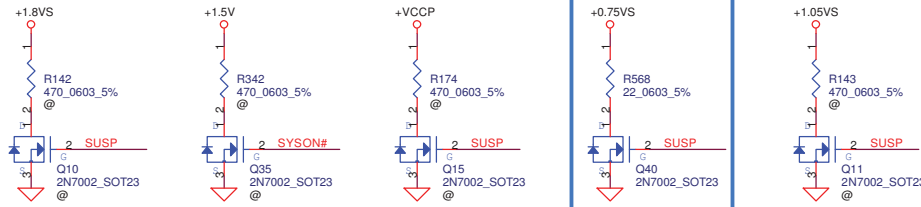
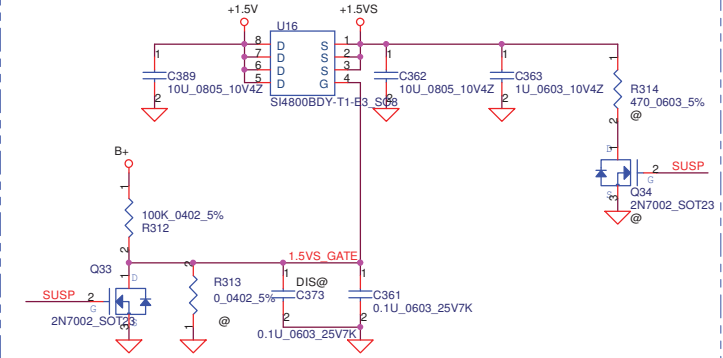
+5VALW TO +5VS



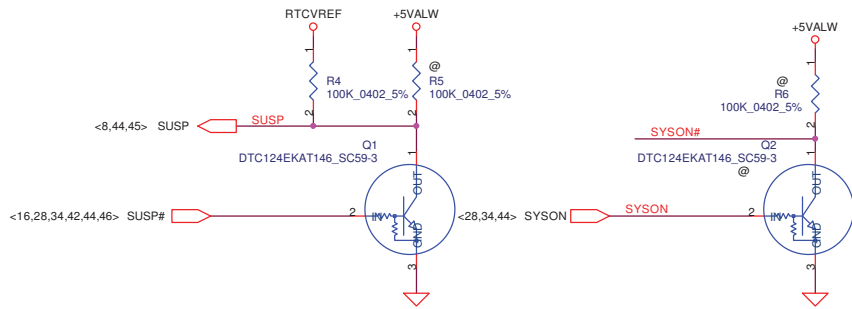
+3VALW TO +3VS



+1.5V to +1.5VS

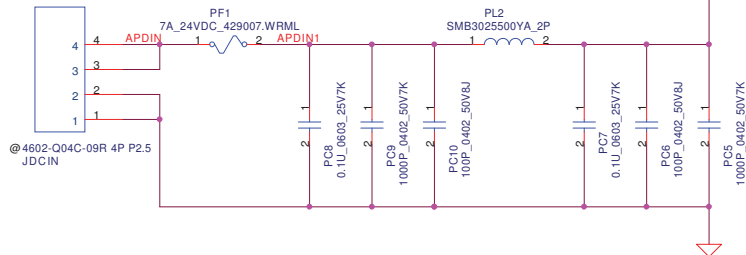


For Intel S3 Power Reduction.

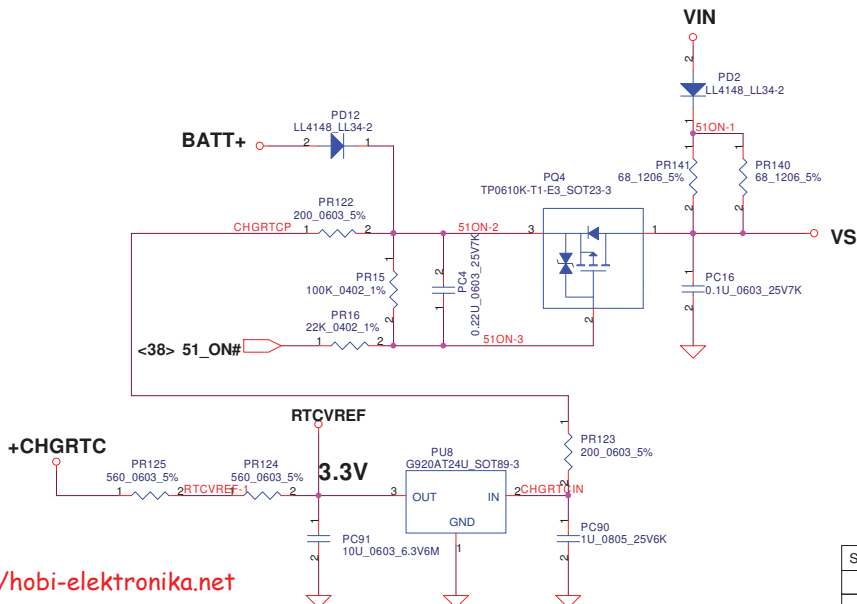
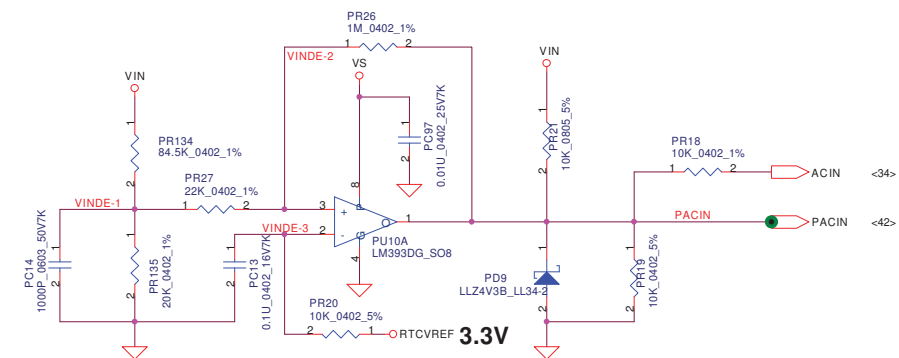


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DC030006J00



Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

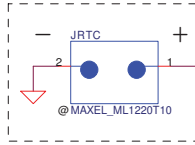
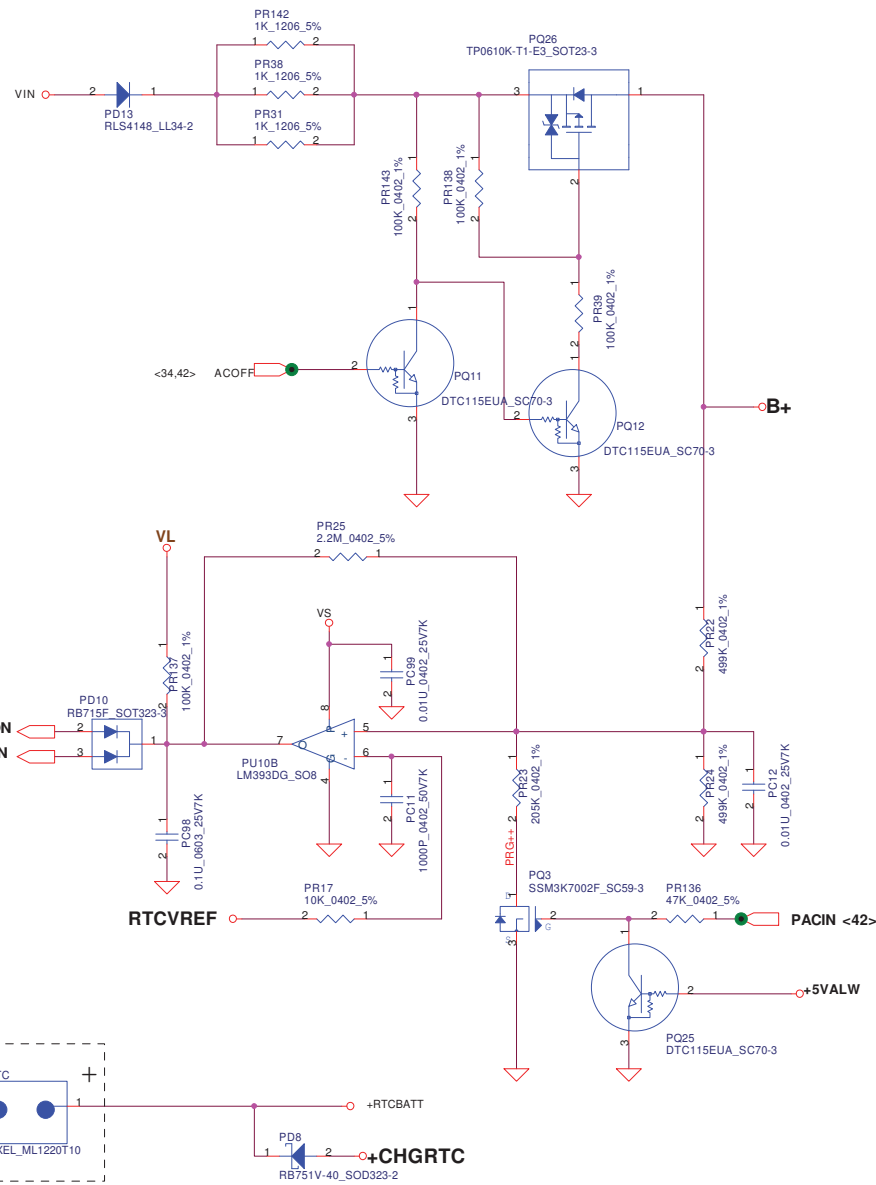


ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

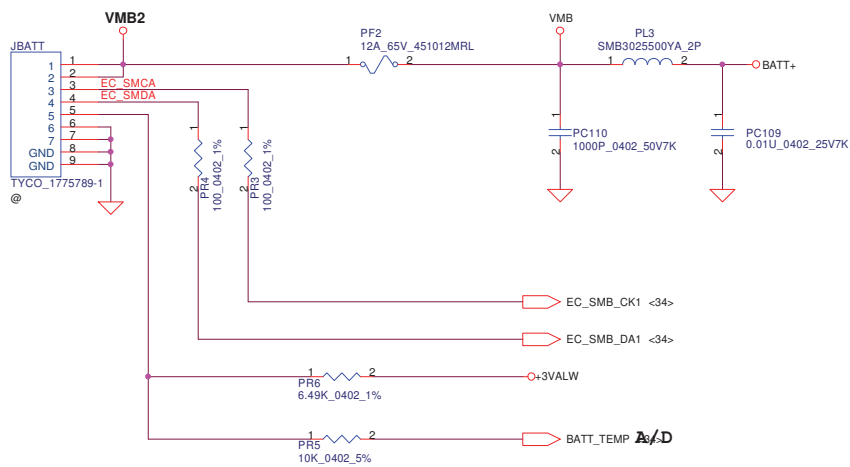
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



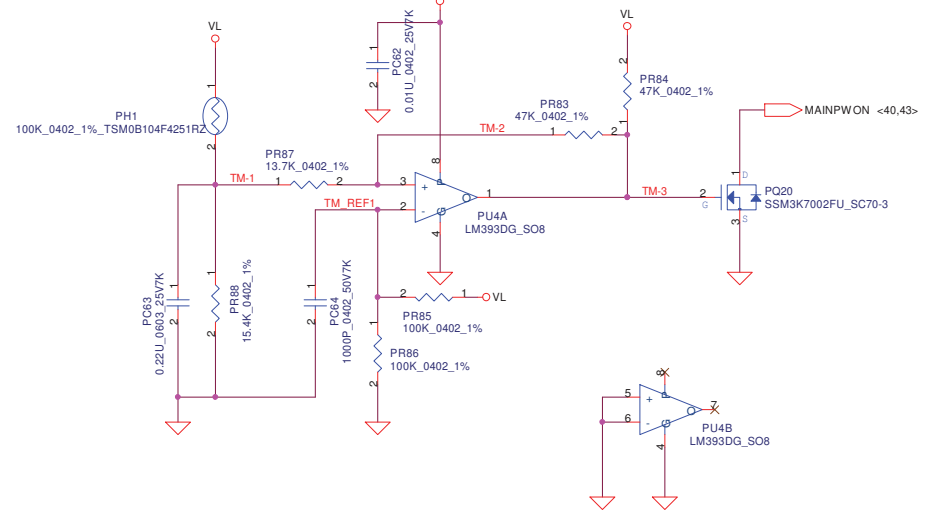
RTC Battery

<http://hobi-elektronika.net>

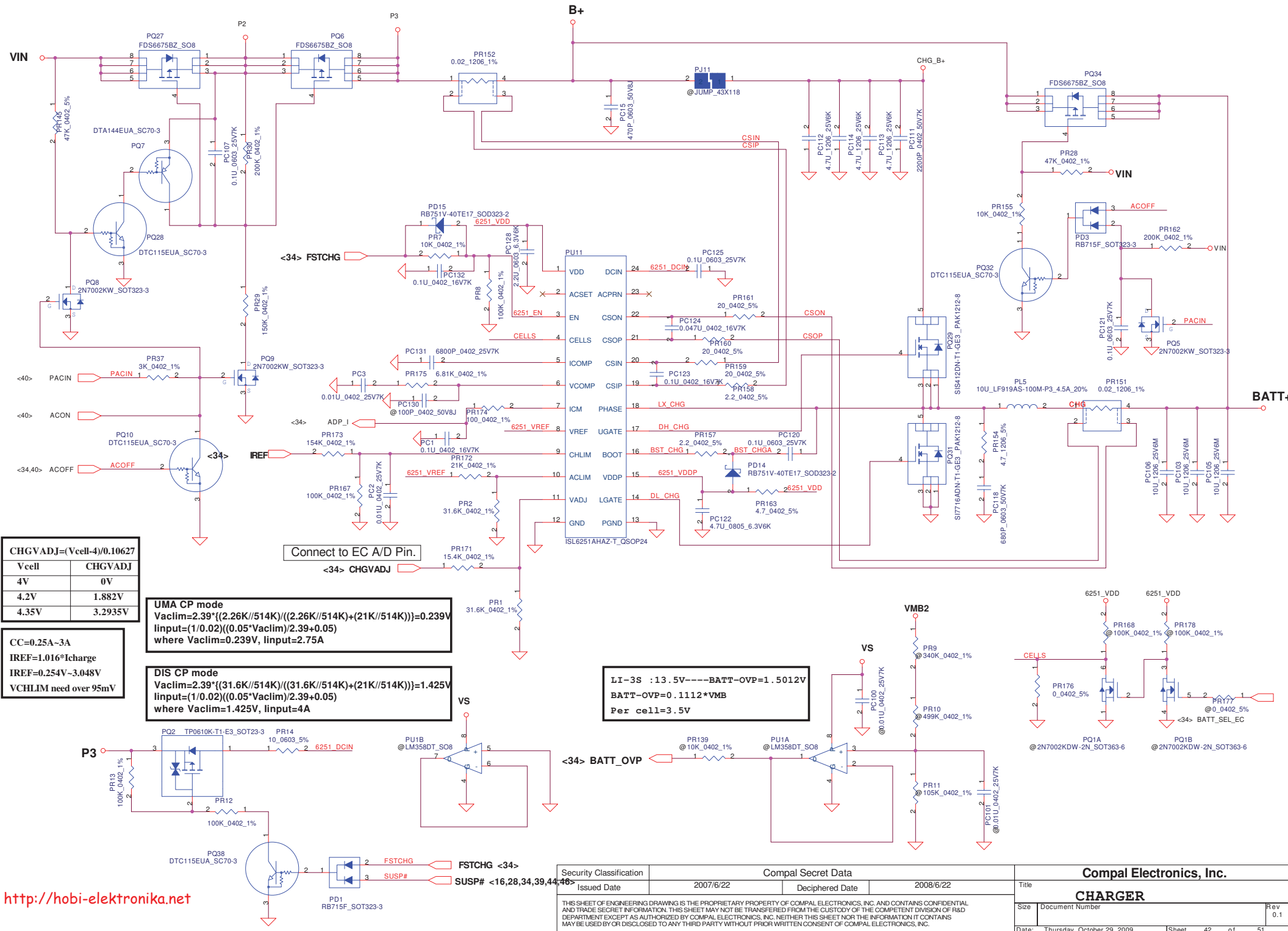
Security Classification				Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title				
				DCIN & DETECTOR				
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

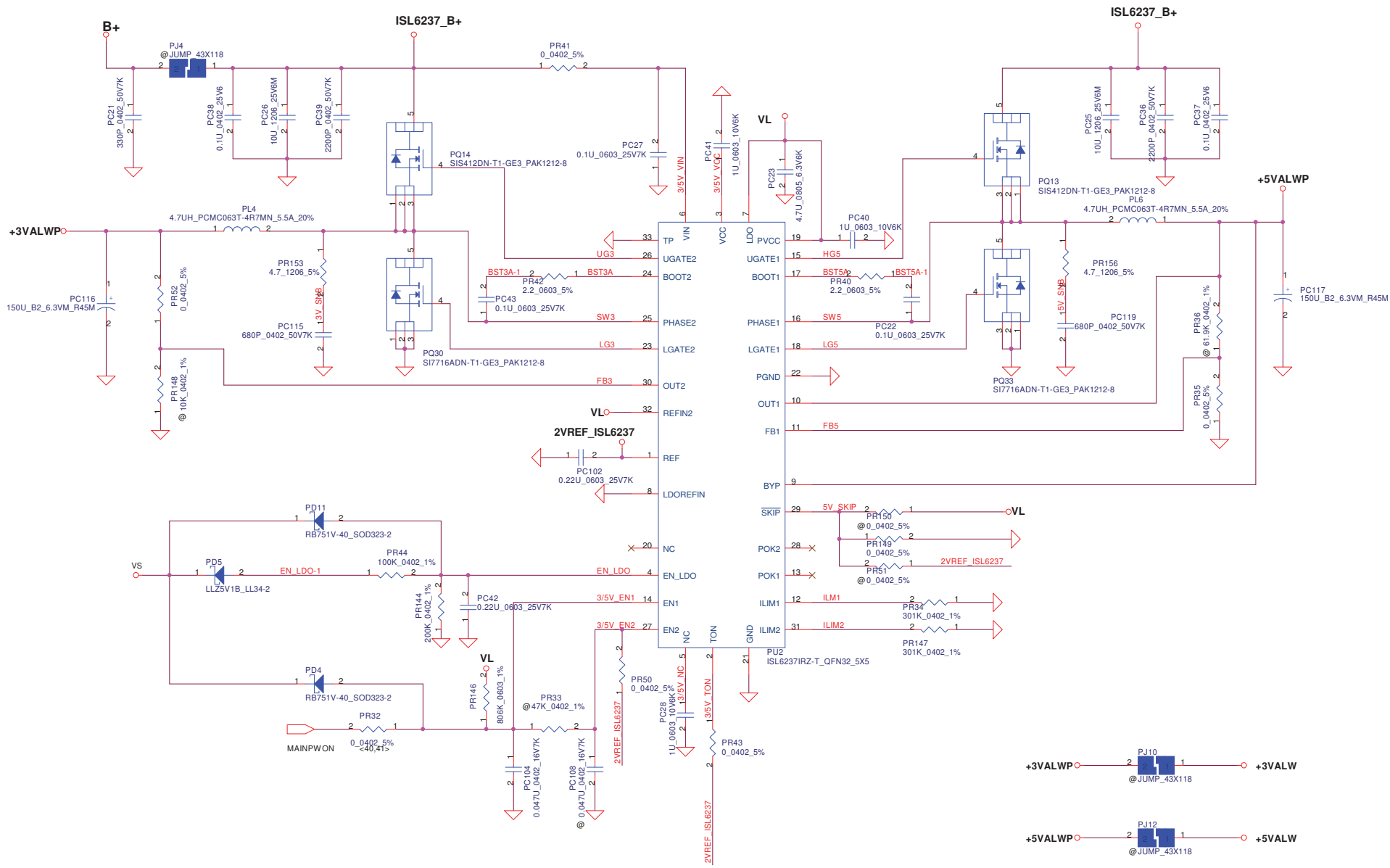
UMA CP mode
 $V_{acli} = 2.39 * ((2.26K/514K) / ((2.26K/514K) + (21K/514K))) = 0.239V$
 $I_{in} = (1/0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 0.239V$, $I_{in} = 2.75A$

DIS CP mode
 $V_{acli} = 2.39 * ((31.6K/514K) / ((31.6K/514K) + (21K/514K))) = 1.425V$
 $I_{in} = (1/0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 1.425V$, $I_{in} = 4A$

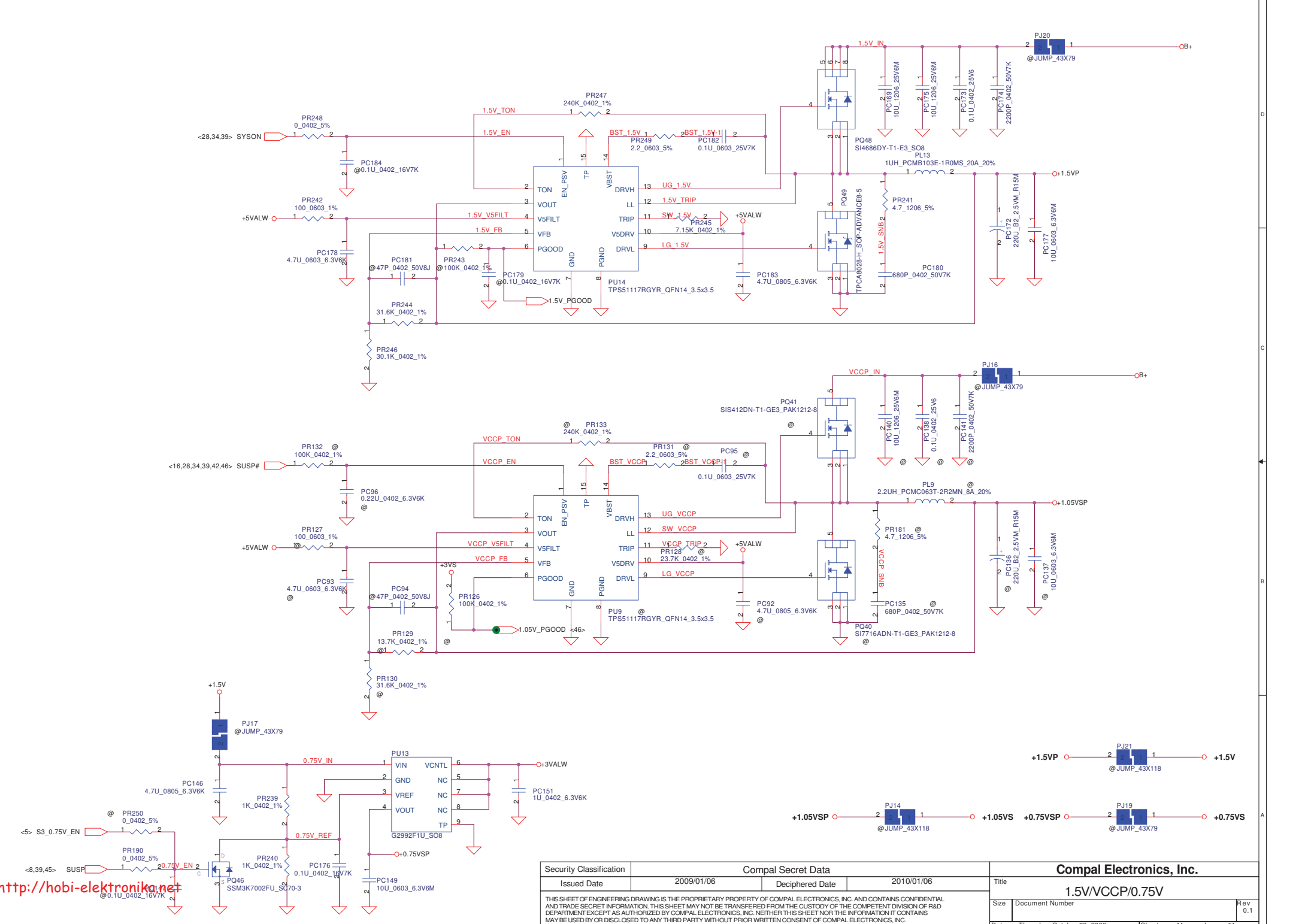
LI-3S : 13.5V --- BATT-OVP=1.5012V
BATT-OVP=0.1112 * VMB
Per cell=3.5V

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Date	Thursday, October 29, 2009	Sheet	42 of 51	Rev
				0.1

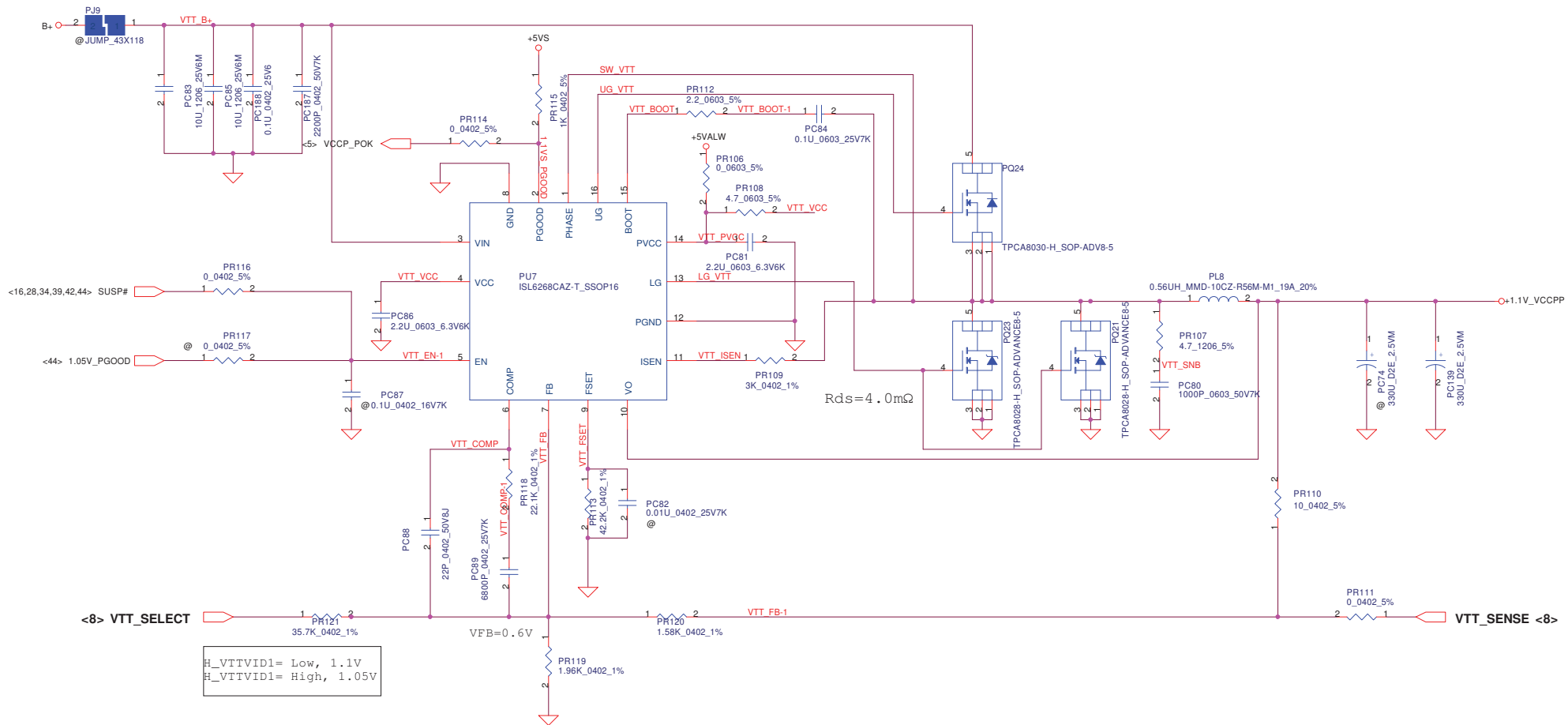


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Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title
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Size	Document Number	Sheet	43	of
Custom		Date:	Thursday, October 29, 2009	Rev
				0.1

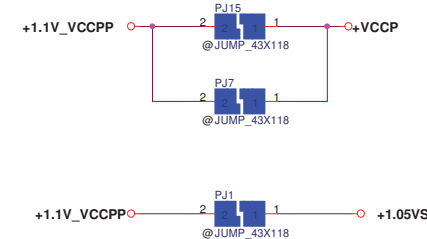


<http://hobi-elektronika.net>

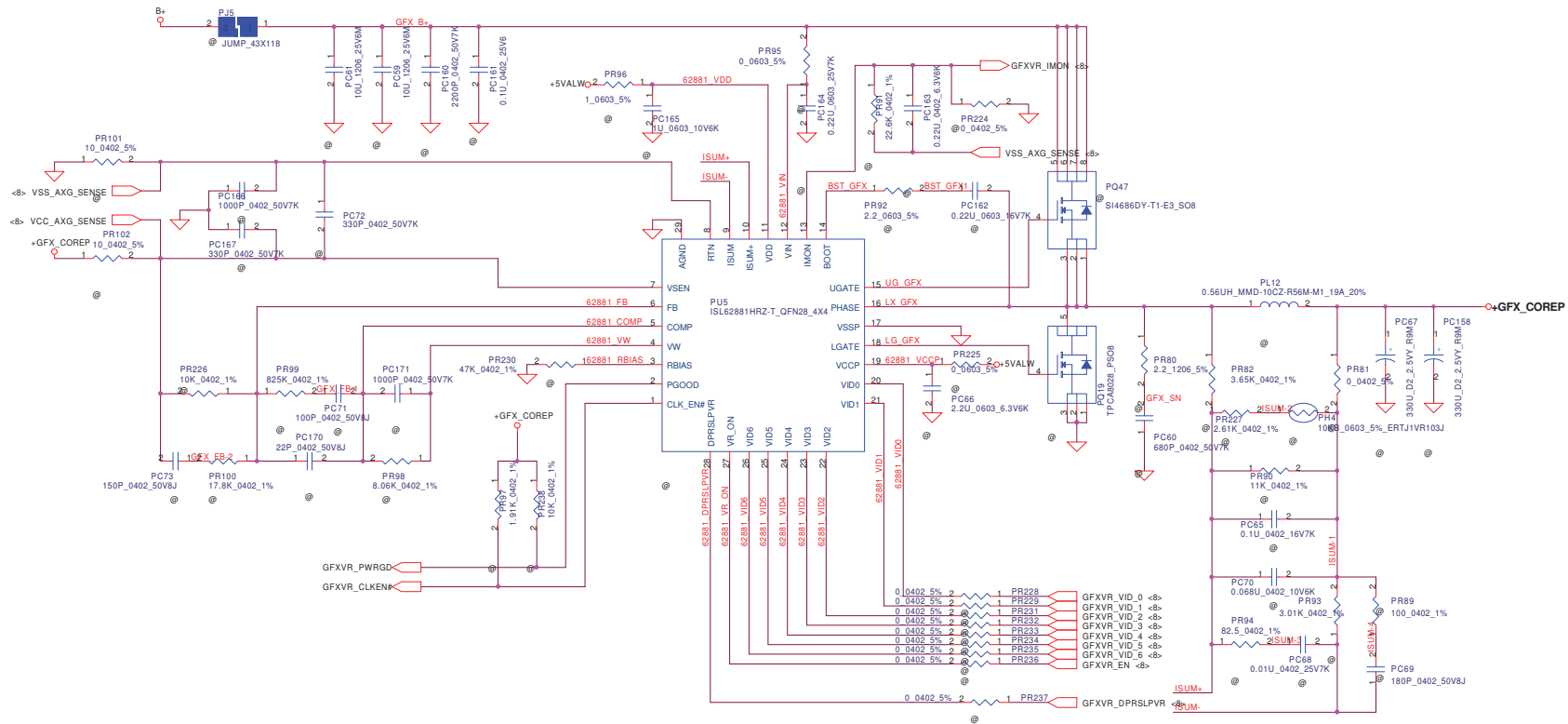
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Issued Date	2009/01/06	Deciphered Date	2010/01/06	1.5V/VCCP/0.75V	
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H_VTTVID1= Low, 1.1V
H_VTTVID1= High, 1.05V

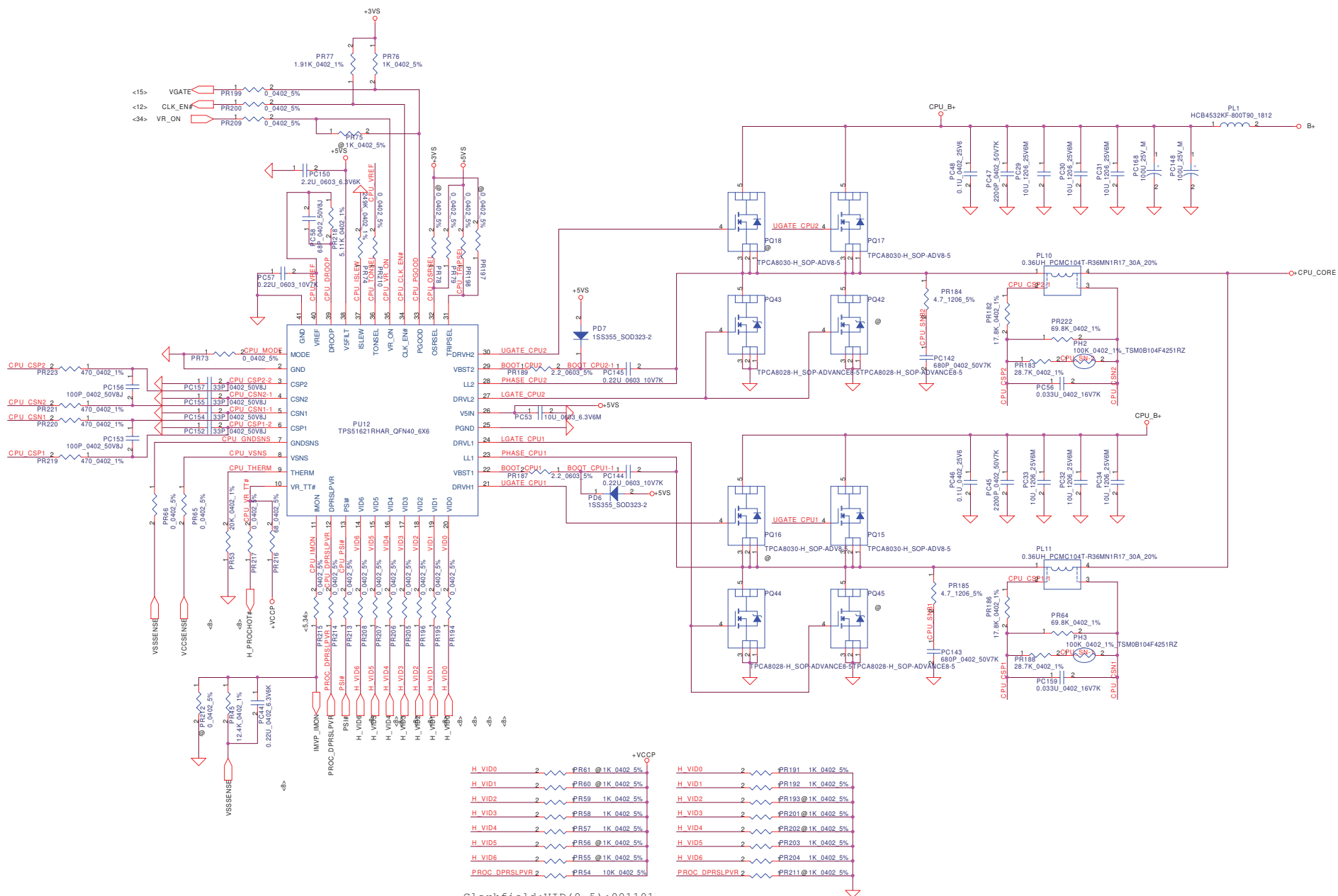


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(15A,600mils ,Via NO.= 30)

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				0.1
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Clarkfield:VID(0-5):001101
 Auburndale:VID(0-5):001110

- | | | | | | |
|---------------|---|--------------------|---------------|---|--------------------|
| H_VID0 | 2 | PR191 @1K 0.402 5% | H_VID0 | 2 | PR191 1K 0.402 5% |
| H_VID1 | 2 | PR192 @1K 0.402 5% | H_VID1 | 2 | PR192 1K 0.402 5% |
| H_VID2 | 2 | PR193 1K 0.402 5% | H_VID2 | 2 | PR193 @1K 0.402 5% |
| H_VID3 | 2 | PR194 1K 0.402 5% | H_VID3 | 2 | PR201 @1K 0.402 5% |
| H_VID4 | 2 | PR195 1K 0.402 5% | H_VID4 | 2 | PR202 @1K 0.402 5% |
| H_VID5 | 2 | PR196 @1K 0.402 5% | H_VID5 | 2 | PR203 1K 0.402 5% |
| H_VID6 | 2 | PR197 1K 0.402 5% | H_VID6 | 2 | PR204 1K 0.402 5% |
| PROC_DPRSLPVR | 2 | PR198 10K 0.402 5% | PROC_DPRSLPVR | 2 | PR211 @1K 0.402 5% |

Item	Reason for change	PG#	Modify List	Date	Phase
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B	LA-5752P	0.3
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B	LA-5751	0.3	
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