

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

www.rosefix.com

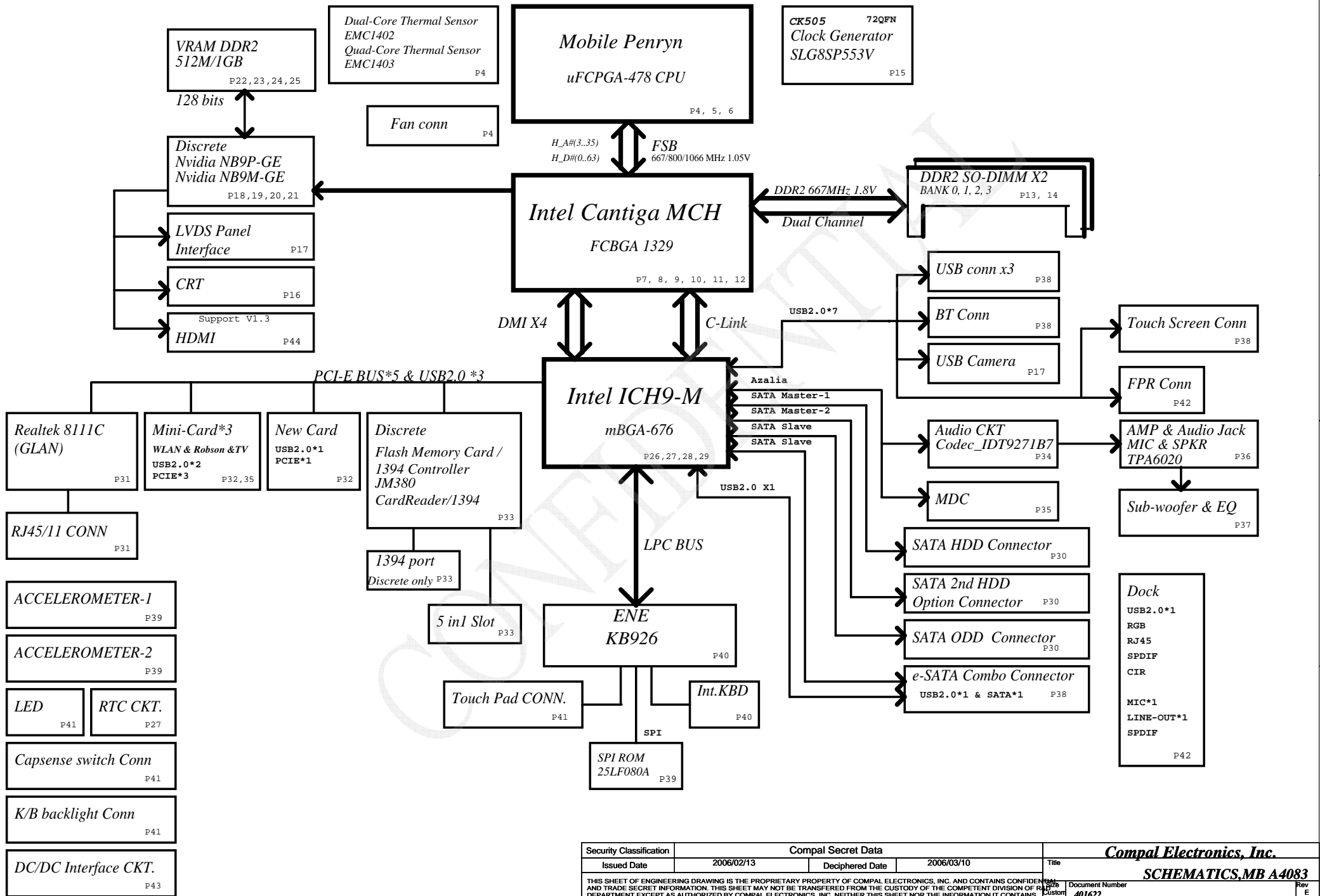
LA-4083P Vader Discrete (NB9P-GS, NB9M-GE)

2009-10-20 Rev 1.0

機 密	等級	硬體二部
	產出人員	
	產出日期	
	解密日期	

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Schematics, MB A4083			
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Montevina Consumer Discrete



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power plane	+B	+5VALW +3VALW	+1.8V	+5VS
				+3VS
State				+1.5VS
				+0.9V
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+2.5VS
				+1.8VS
				+1.2VS
				+0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_DA1										
SMB_EC_CK2	KB926	X	X	X	V	X	X	X	X	X
SMB_EC_DA2										
SMB_CK_CLK1	ICH9	X	X	X	X	V	V	V	X	X
SMB_CK_DAT1										
DDC2_CLK	NB9M	X	X	X	X	X	X	X	V	X
DDC2_DATA										



USB

assignment:
 USB-0 Right side
 USB-1 Right side
 USB-2 Left side(with ESATA)
 USB-3 Dock
 USB-4 Camera
 USB-5 WLAN
 USB-6 Bluetooth
 USB-7 Finger Printer
 USB-8 MiniCard(WWAN/TV)
 USB-9 Express
 USB-10 X
 USB-11 X

PCIe

assignment:
 PCIe-1 TV tuner/WWAN/Robeson
 PCIe-2 X
 PCIe-3 WLAN
 PCIe-4 New Card
 PCIe-5 Card
 PCIe-6 GLAN (Marvell)

Symbol Note :

 : means Digital Ground
 : means Analog Ground
 @ : means just reserve , no build
 DEBUG@ : means just reserve for debug.

EC SM Bus1 address

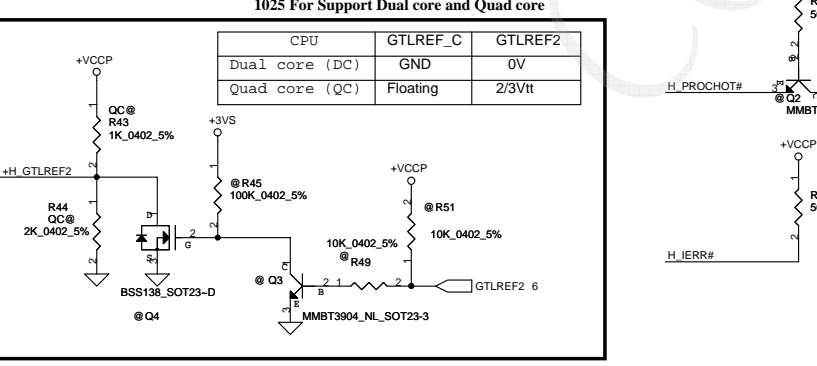
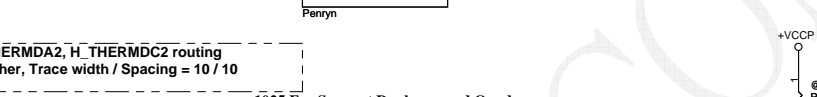
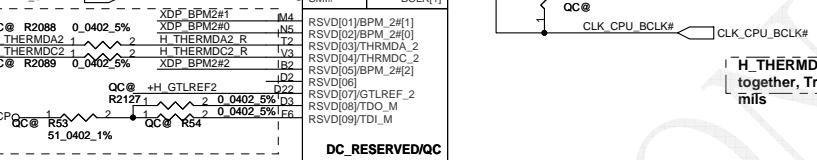
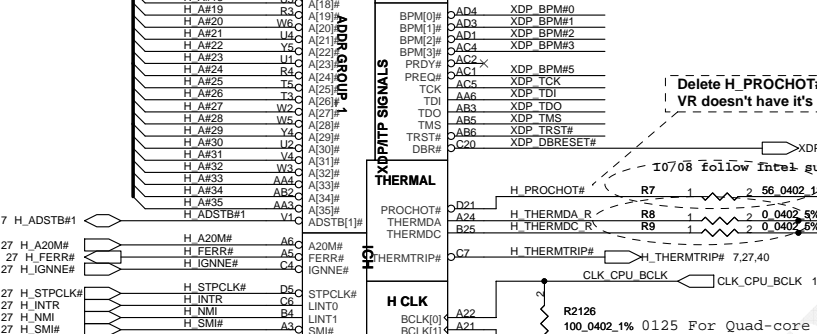
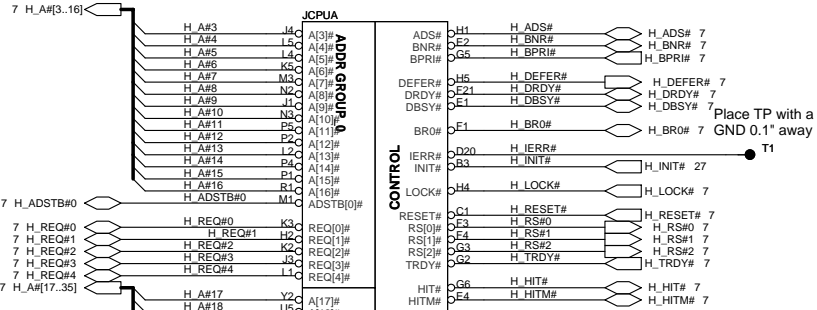
EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X	CPU EMC1402	4CH	1001 1000b
24C16	A0H	1010 000X	VGA	4DH	1001 1010b
CAP BOARD -- Cypress	38H				
CAP BOARD -- ST	b0H				
G-sensor		0011 1001(read) 0011 1010(write)			

I2C / SMBUS ADDRESSING

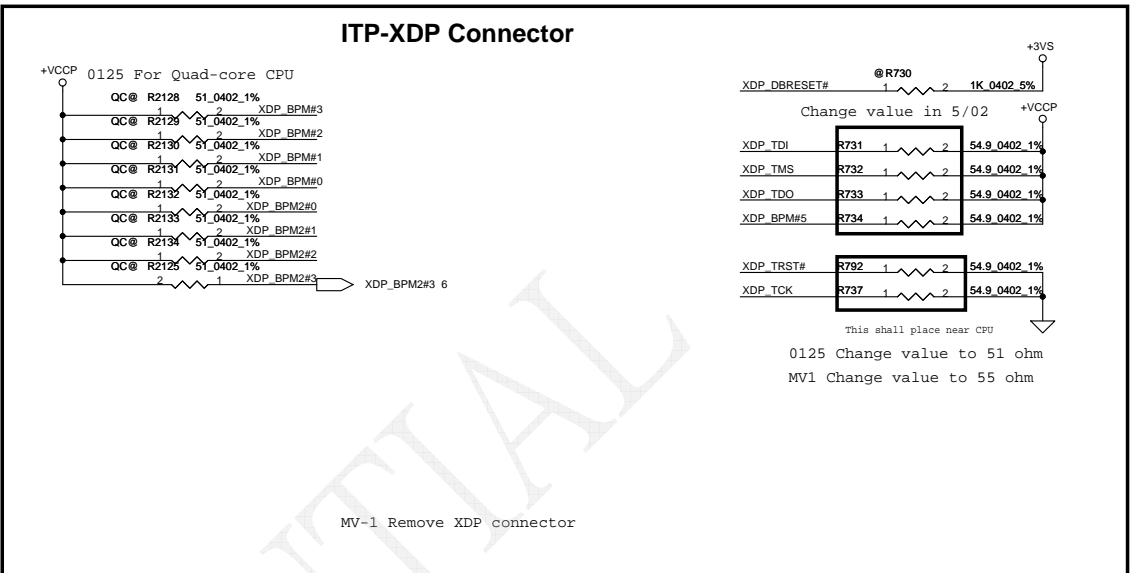
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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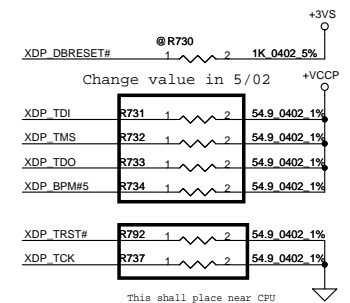


1025 For Support Dual core and Quad core

	CPU	GTLREF_C	GTLREF2
Dual core (DC)		GND	0V
Quad core (QC)		Floating	2/3Vtt



MV-1 Remove XDP connector

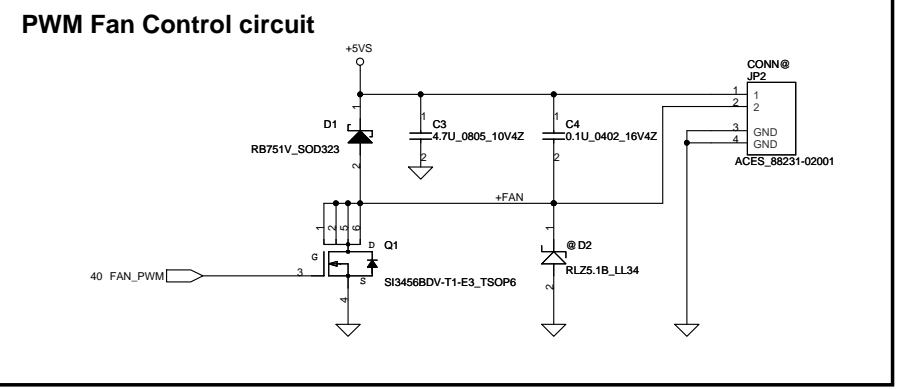
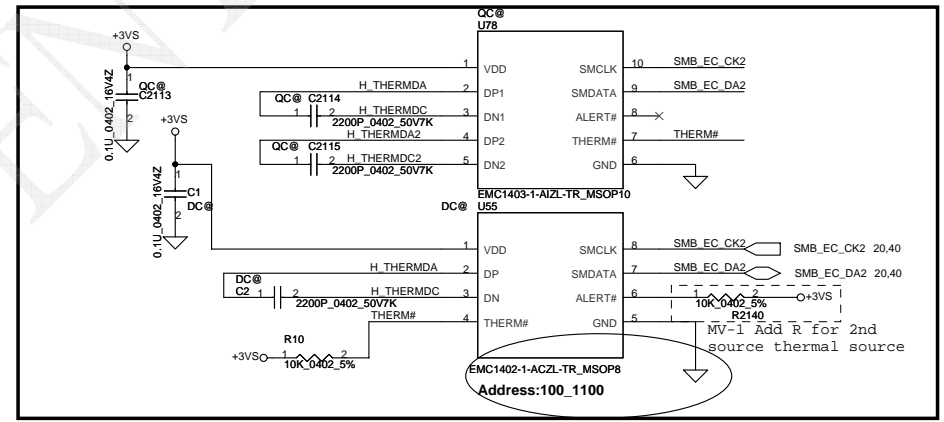


This shall place near CPU
0125 Change value to 51 ohm
MV1 Change value to 55 ohm

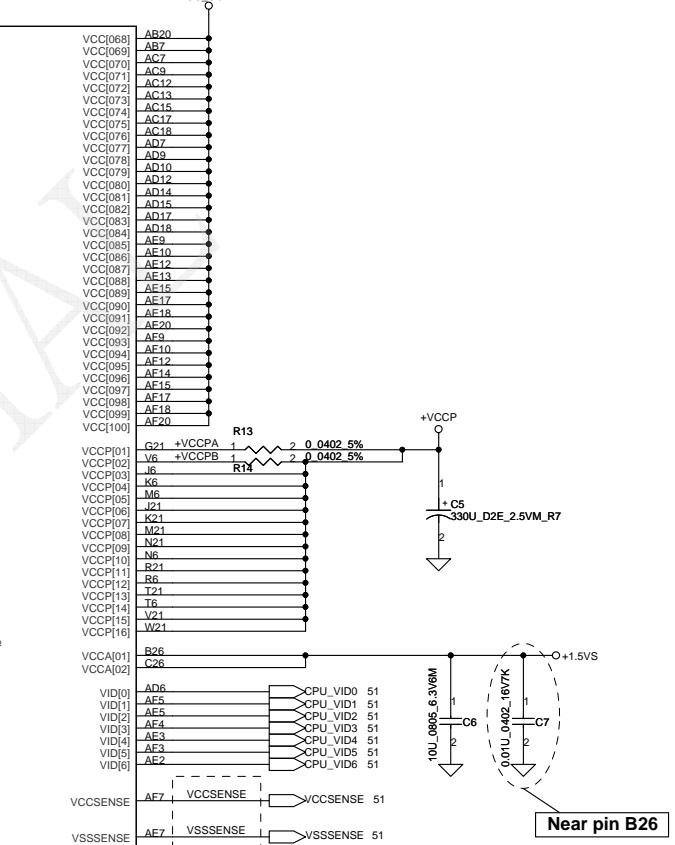
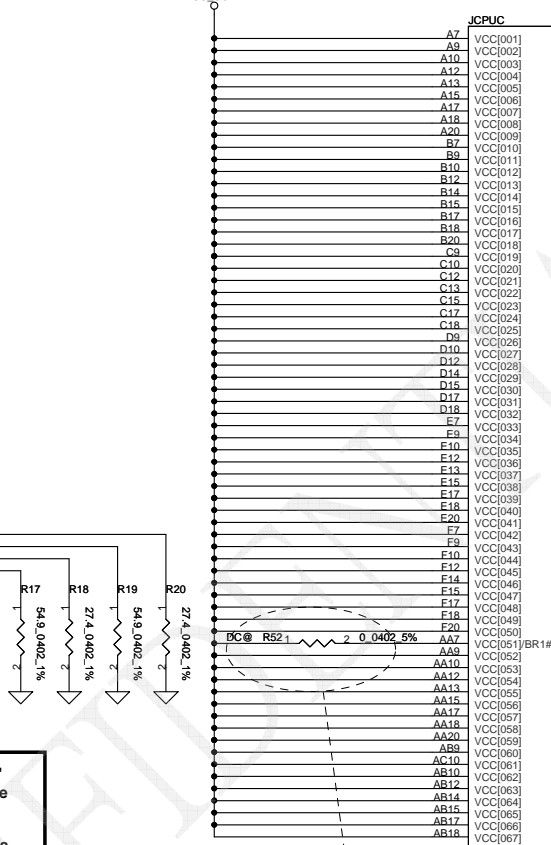
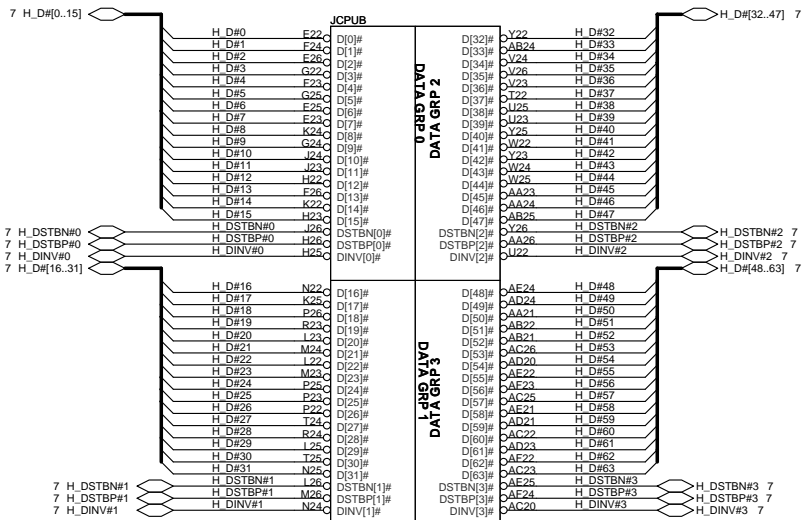
Delete H_PROCHOT# off-page due to VR doesn't have it's input pin @08/31

10708 follow Intel suggestion to change value

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mils



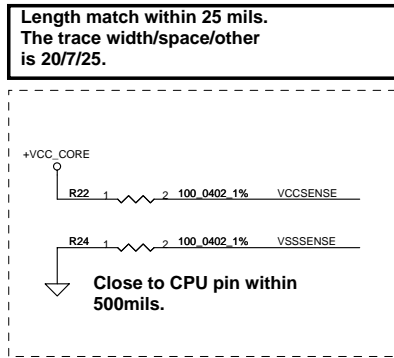
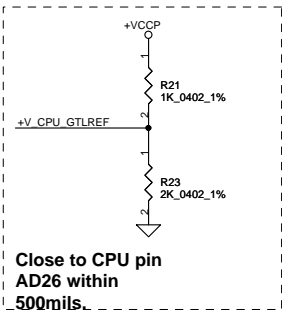
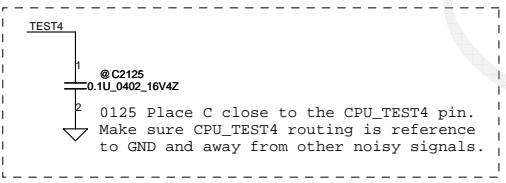
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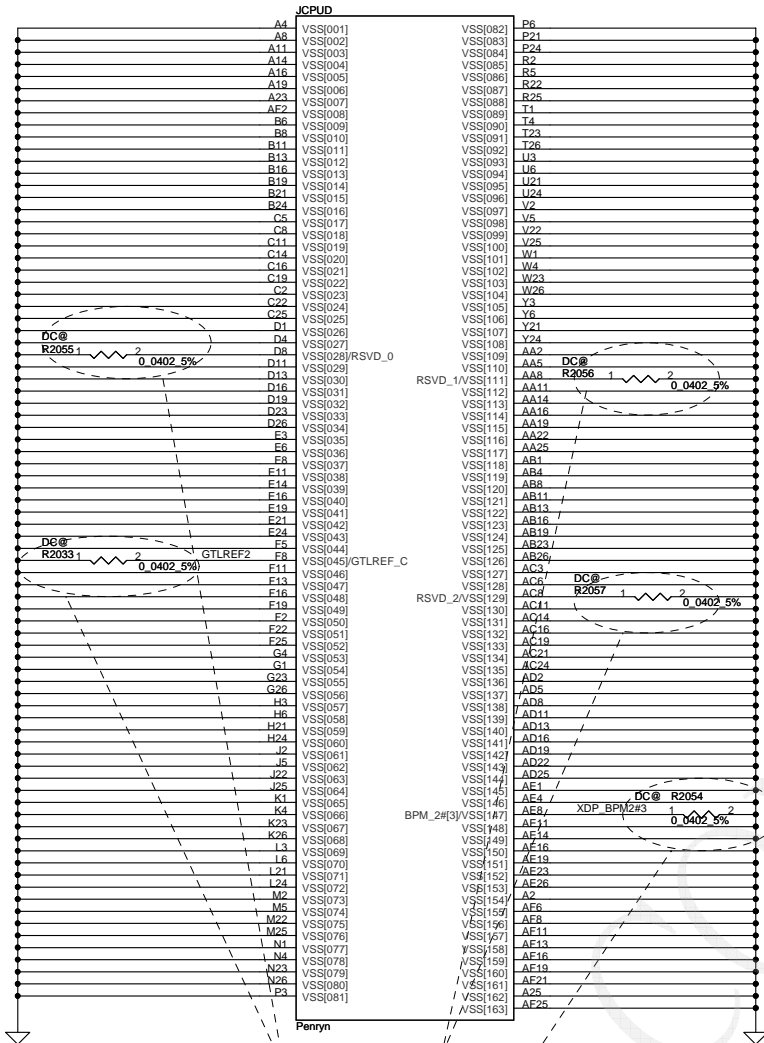


* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

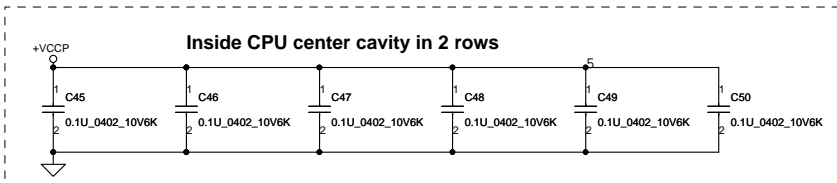
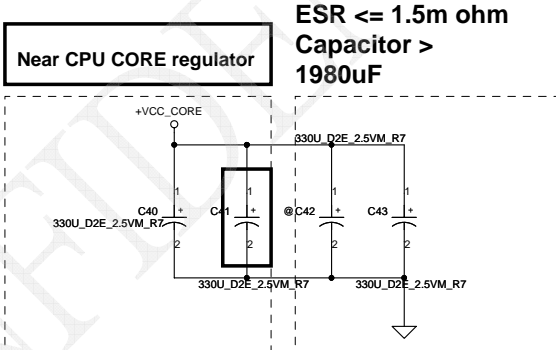
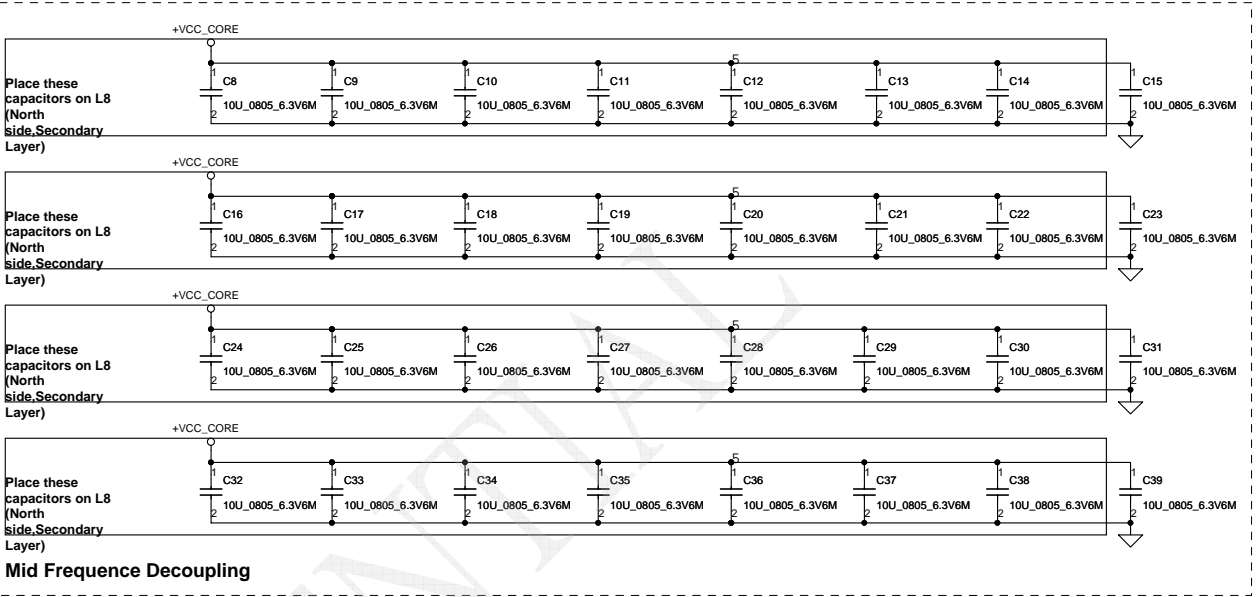
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



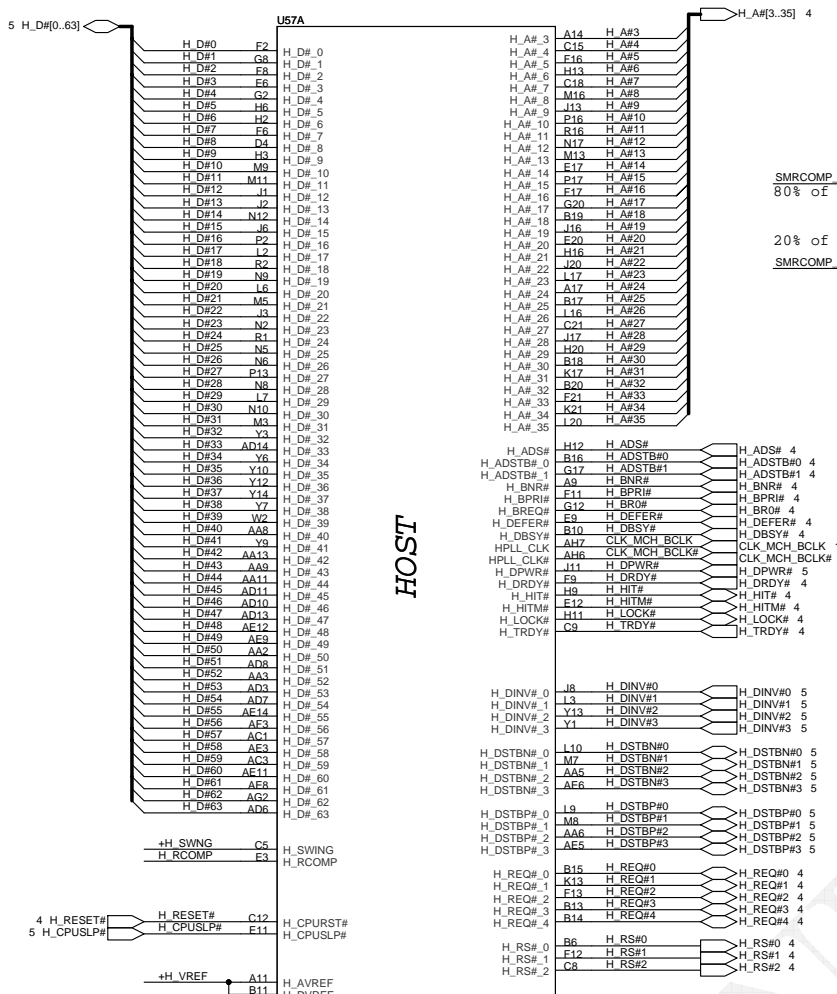


1025 For Support Dual core and Quad core

- GTLREF2 GTLREF2 4
- XDP_BPM2#3 XDP_BPM2#3 4



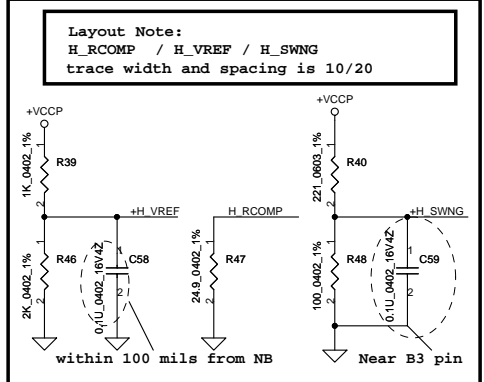
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HOST

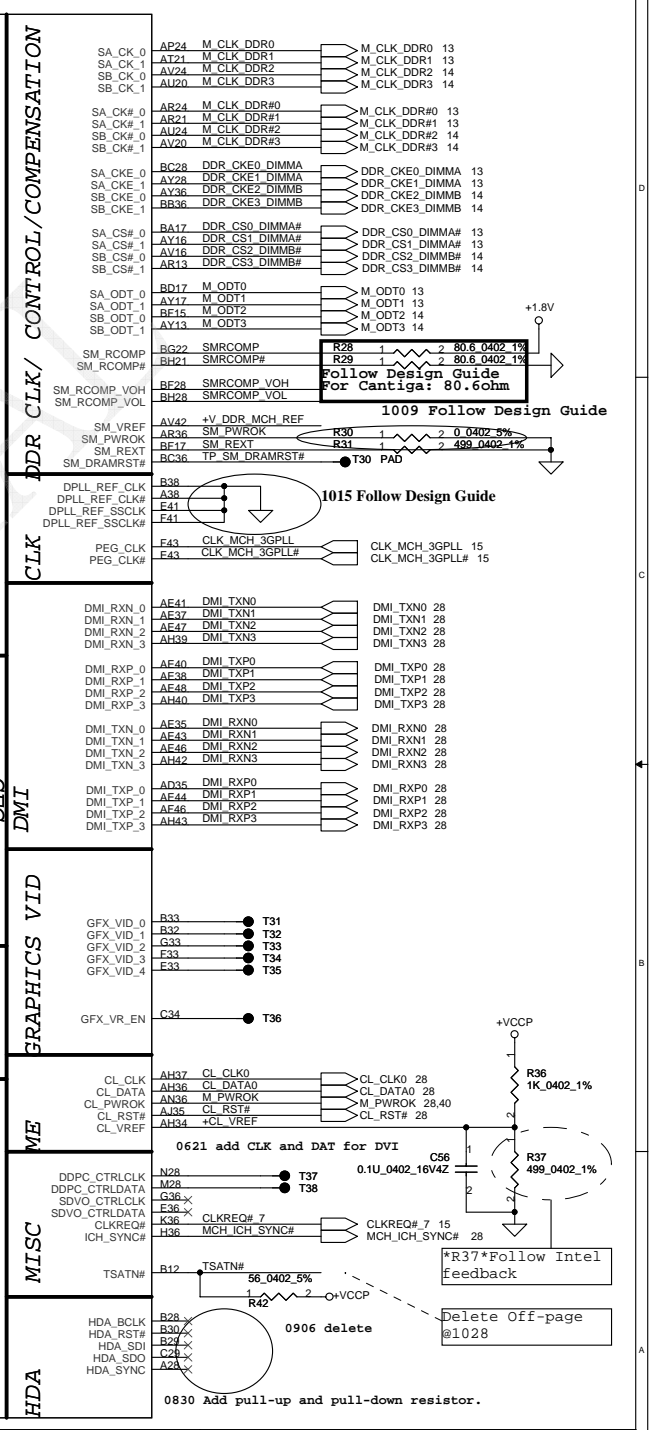
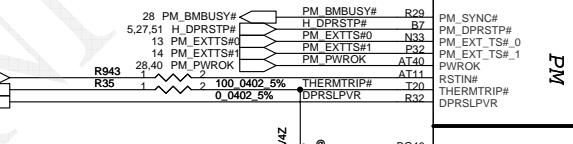
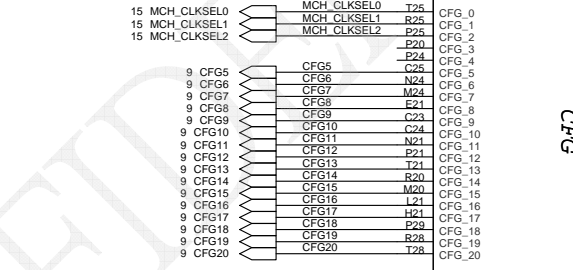
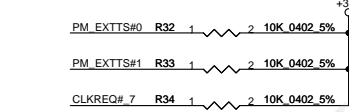
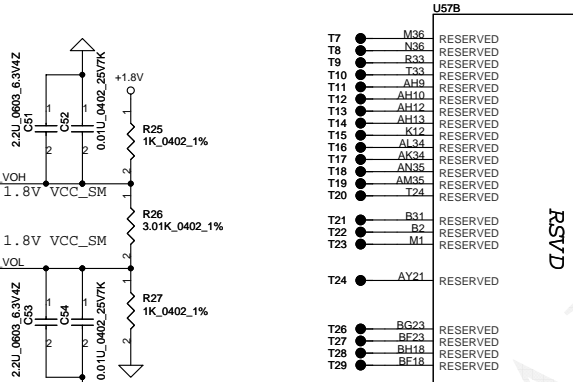
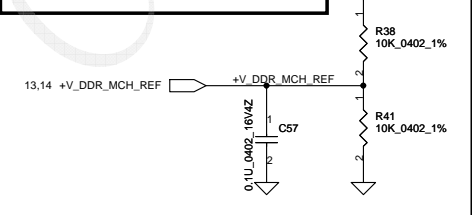
layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



Layout Note: v_DDR_MCH_REF trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC



U57B

1009 Follow Design Guide

1015 Follow Design Guide

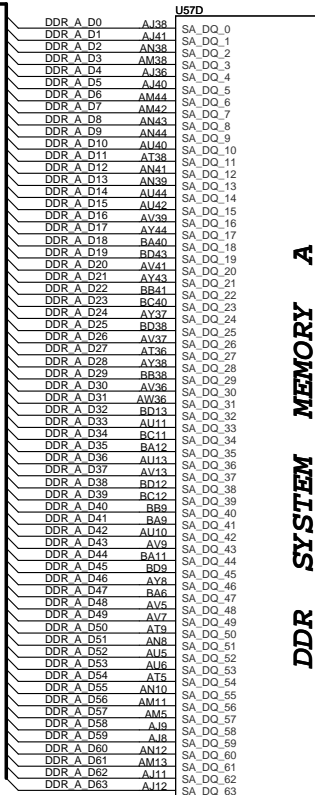
0906 delete

Delete Off-page @1028

0830 Add pull-up and pull-down resistor.

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13 DDR_A_D[0..63]

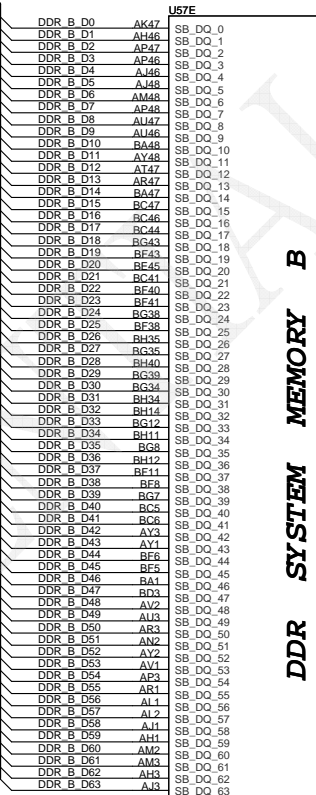


U57D

DDR SYSTEM MEMORY A

CANTIGA ES_FCBGA1329

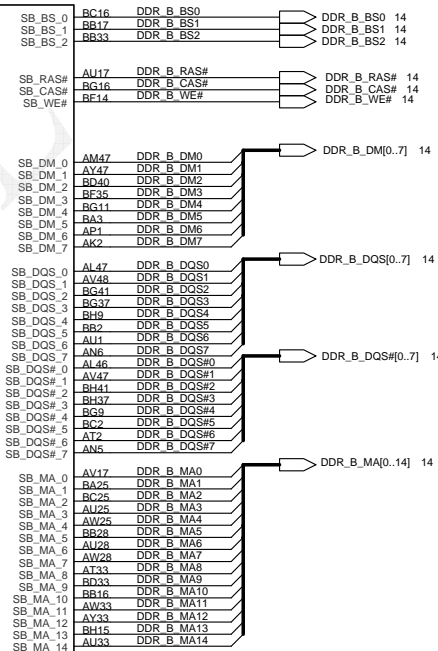
14 DDR_B_D[0..63]



U57E

DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329



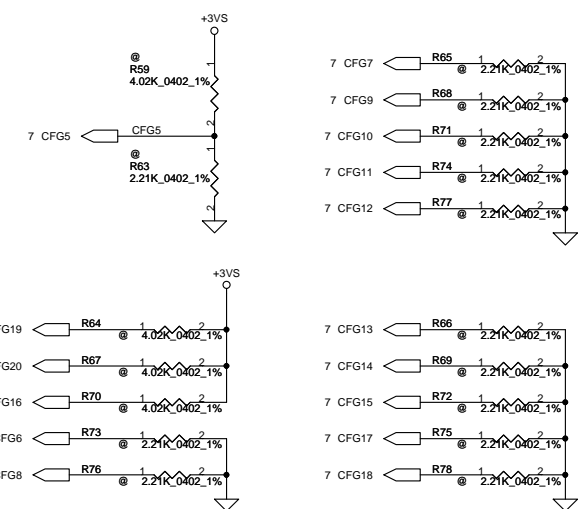
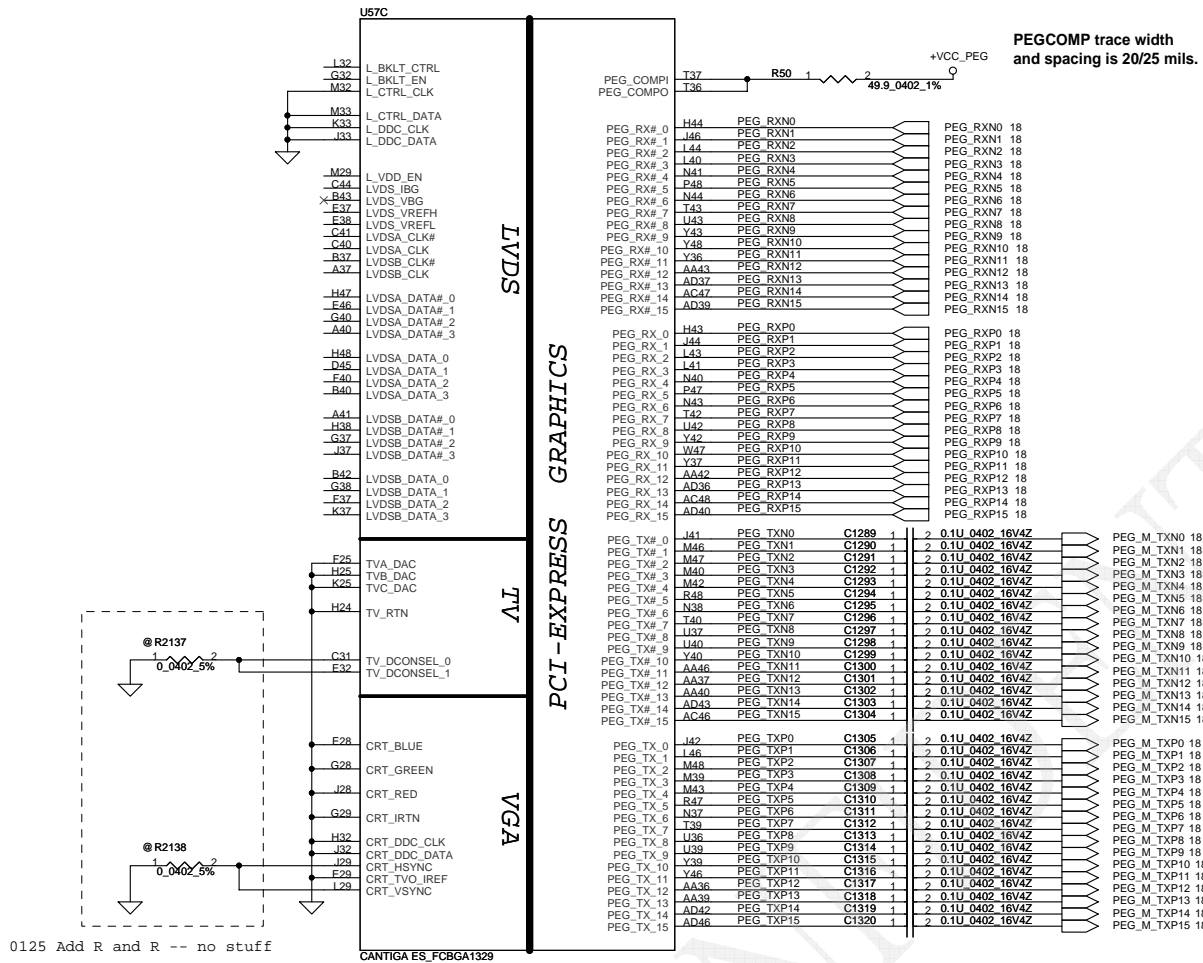
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SCHEMATICS, MB A4083

Strap Pin Table

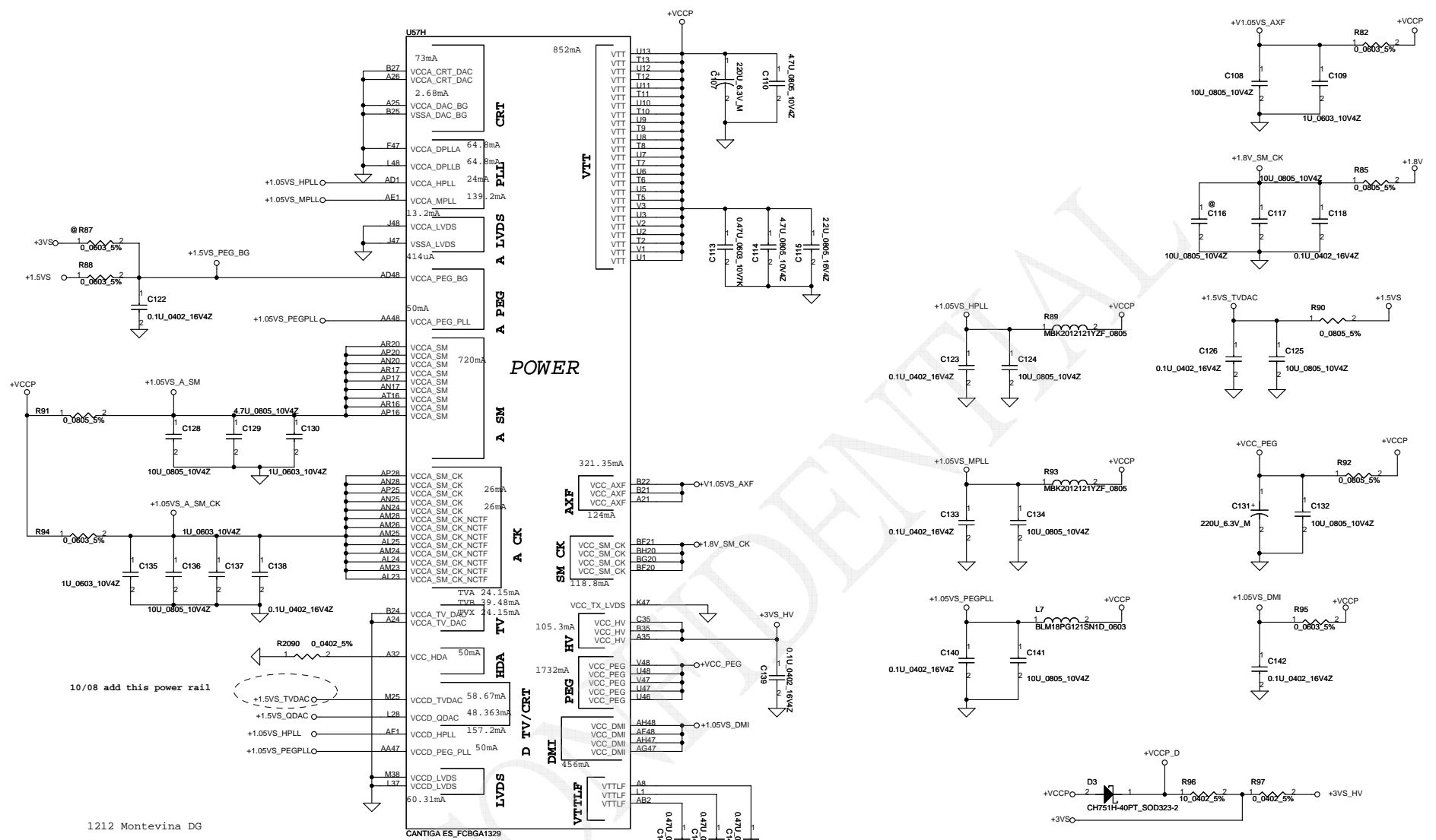
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz Selected By CPU 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

PEGCOMP trace width and spacing is 20/25 mils.



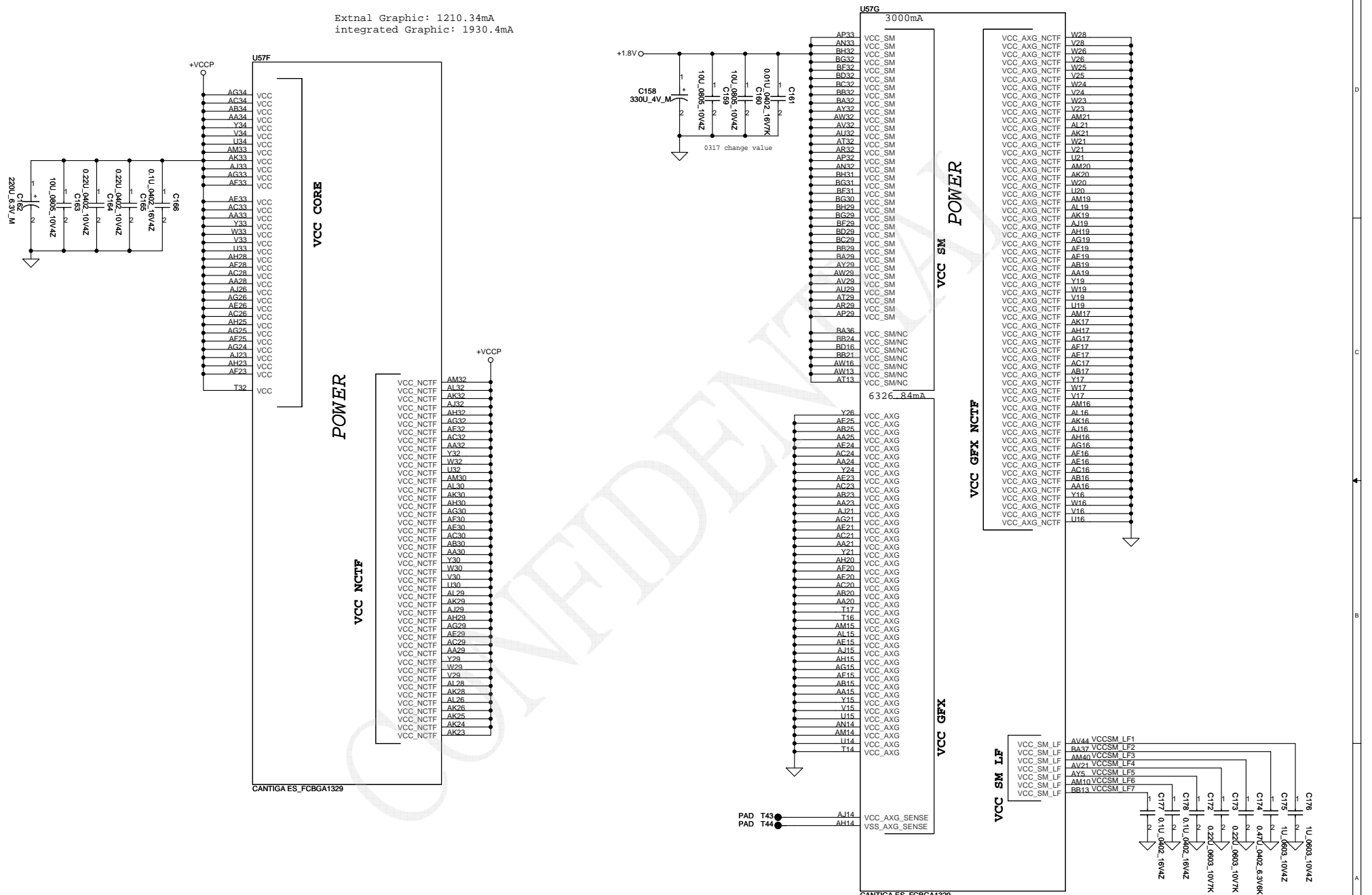
MV1 No-stuff R59,R67,R65,R77,R66

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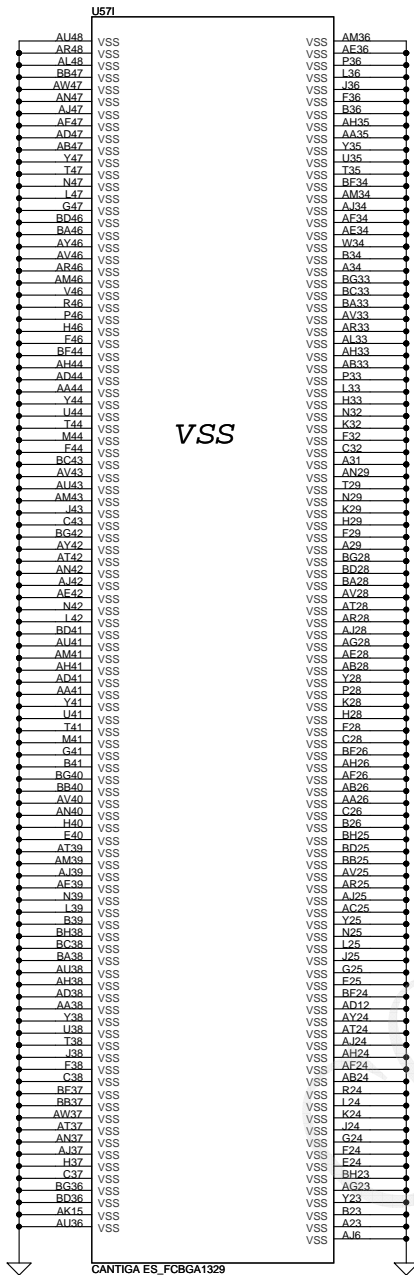


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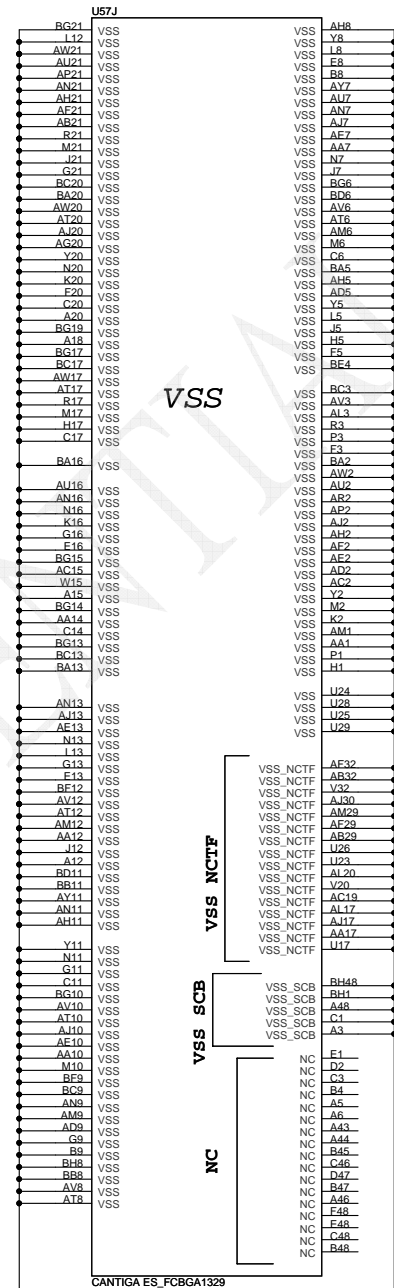
Extenal Graphic: 1210.34mA
 integrated Graphic: 1930.4mA



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CANTIGA ES_FCBGA1329



CANTIGA ES_FCBGA1329

VSS

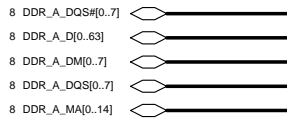
VSS

VSS NCTF

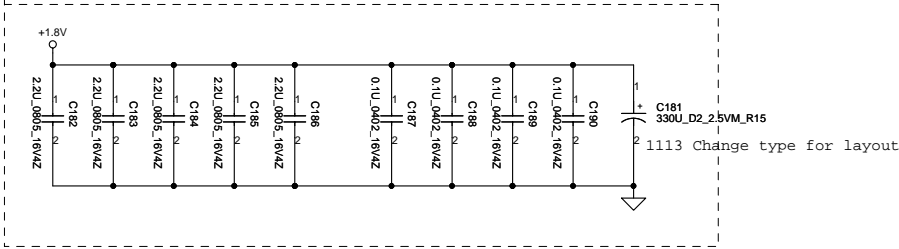
VSS SCB

NC

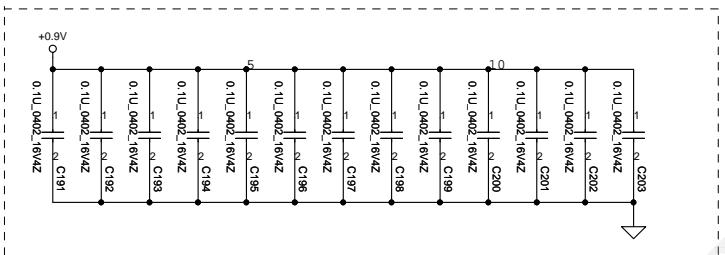
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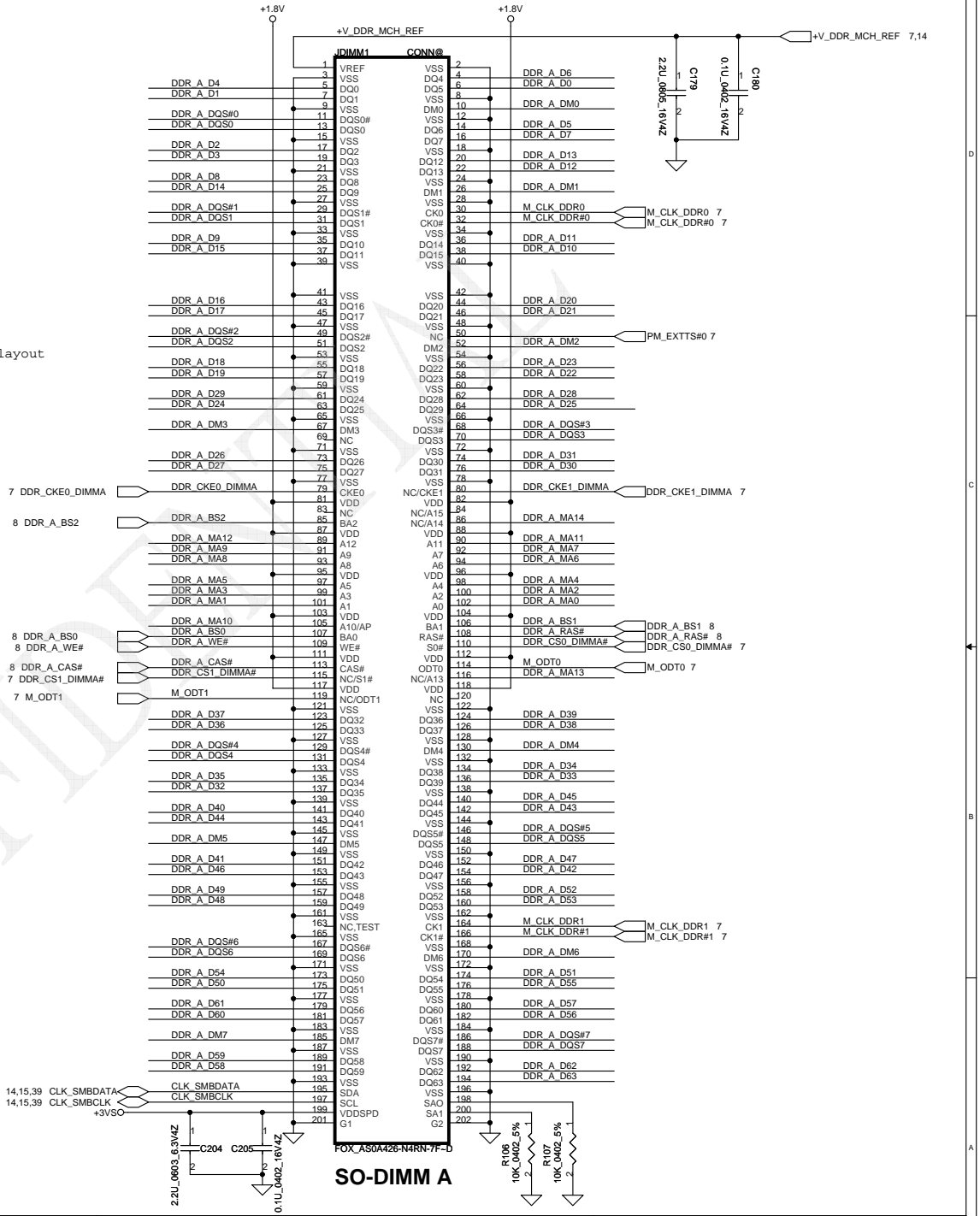
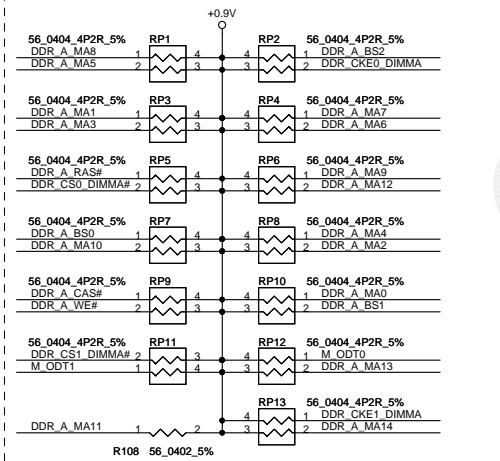
Layout Note:
Place near JP3



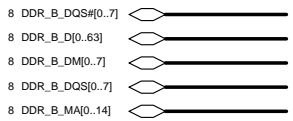
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



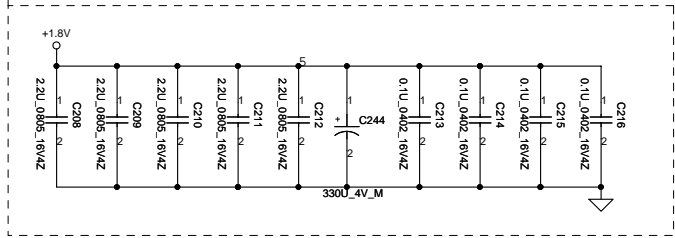
Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



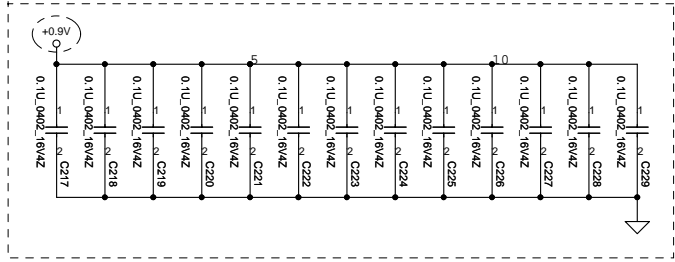
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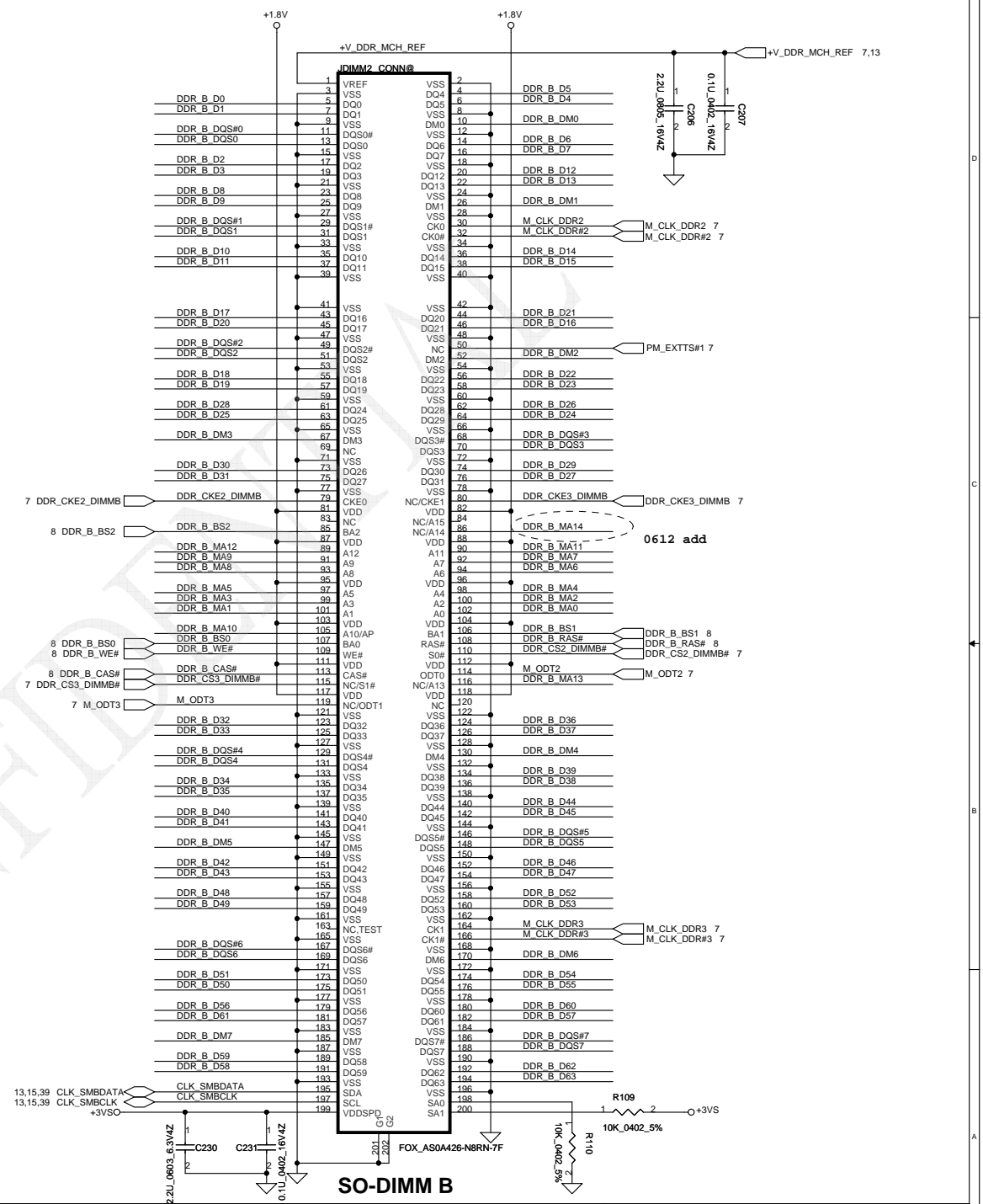
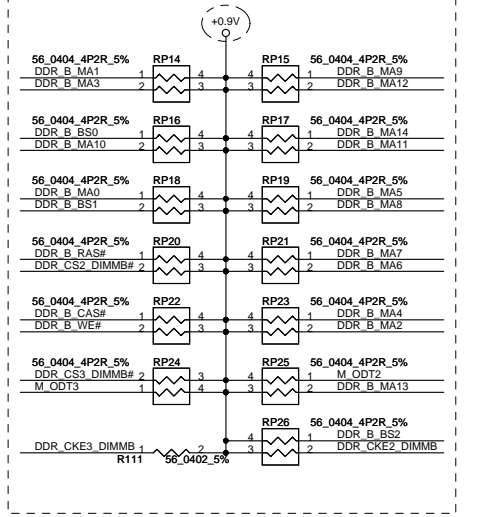
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

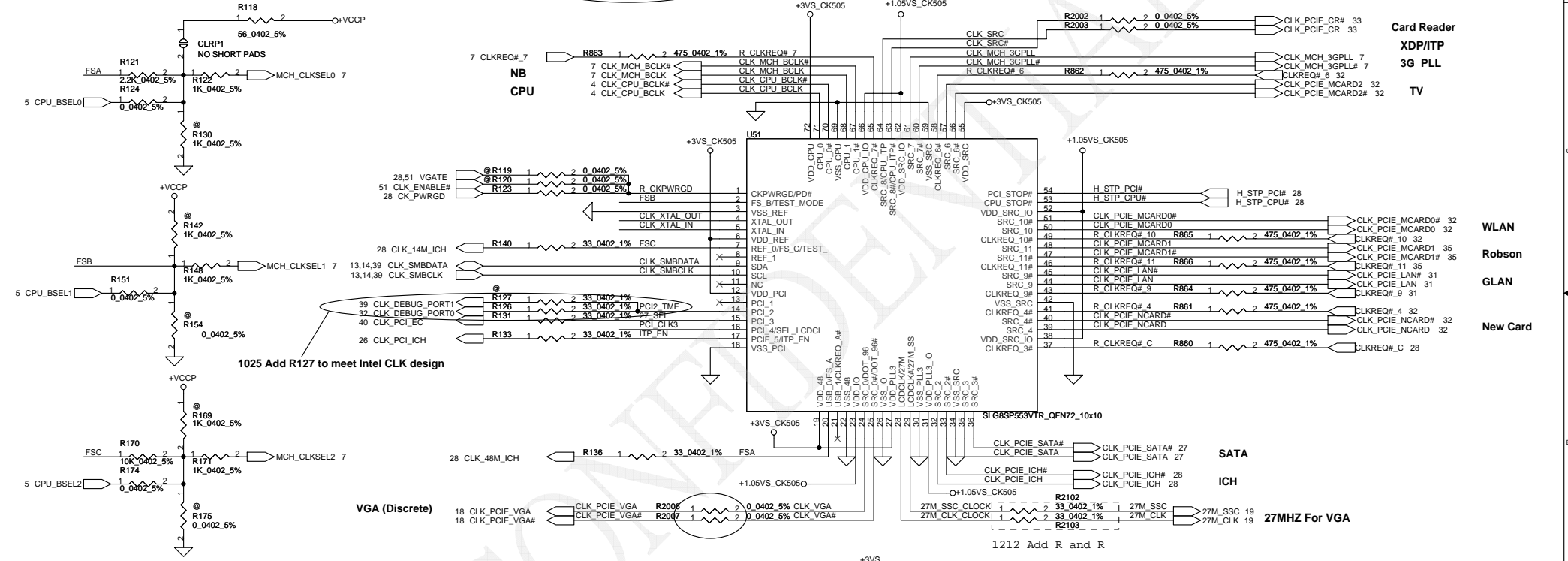
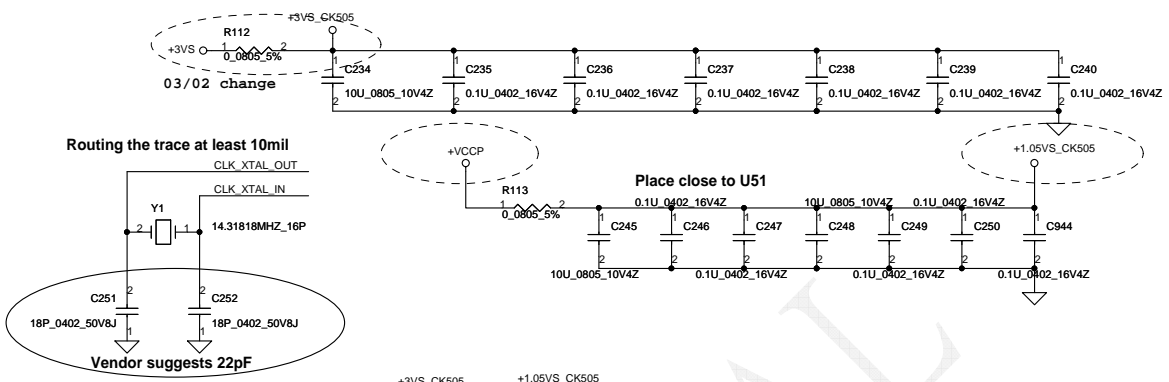


Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"

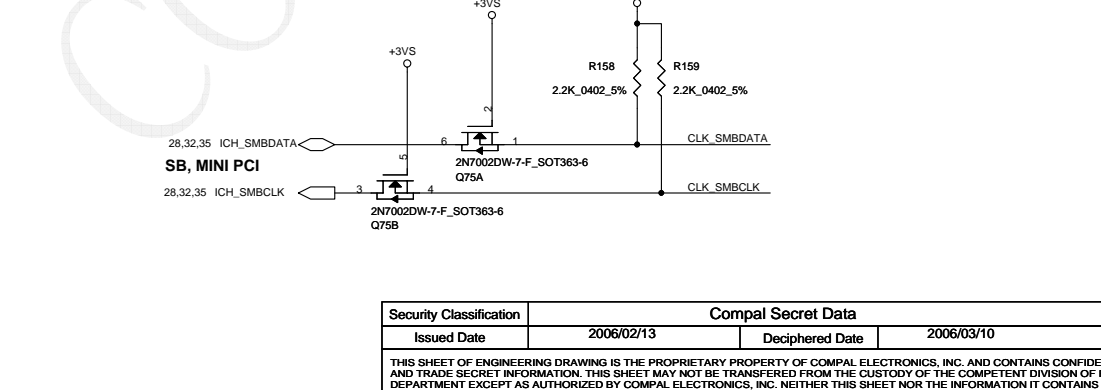


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				Date:	Thursday, October 22, 2009	Sheet	14 of 61

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						



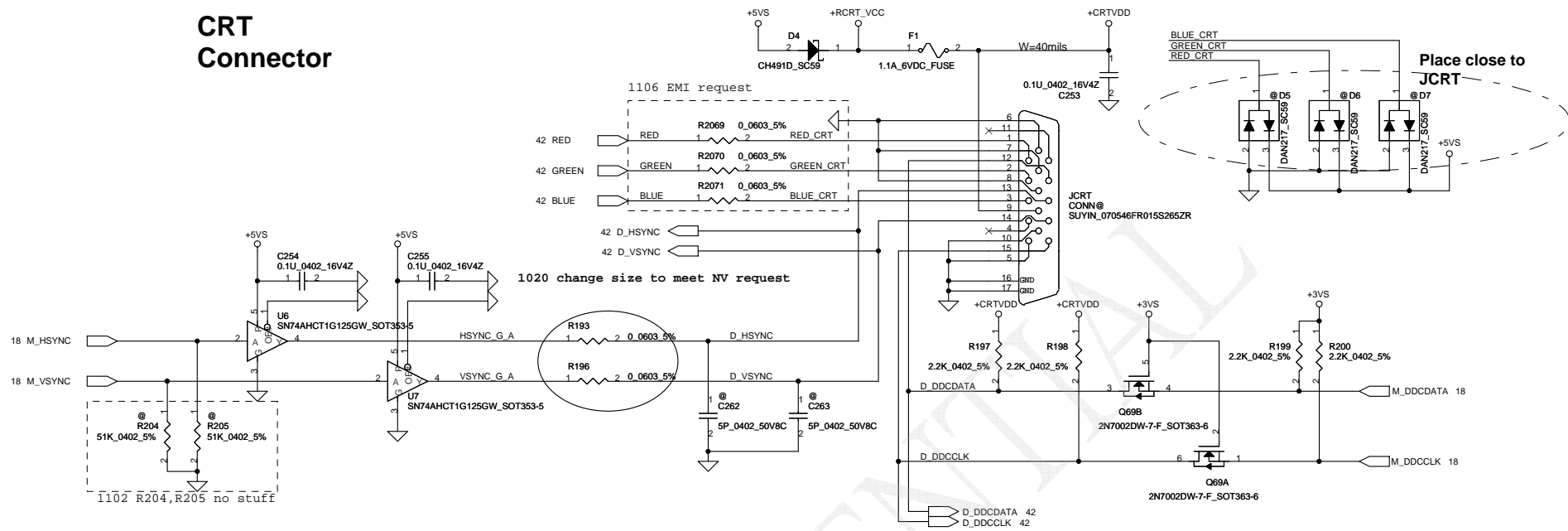
I TP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



@ C232	5P_0402_50V8C	2	1	CLK_48M_ICH
@ C233	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@ C241	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@ C242	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@ C243	4.7P_0402_50V8C	2	1	CLK_DEBUG_PORT0

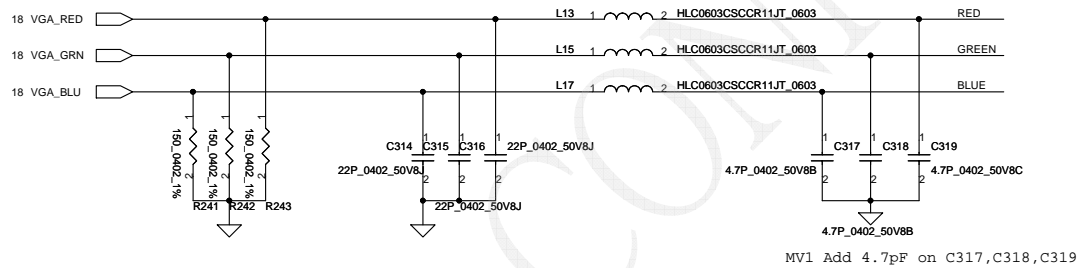
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Document Number	401622	Rev	E	Date:	Thursday, October 22, 2009
			Sheet	15	of 61

CRT Connector

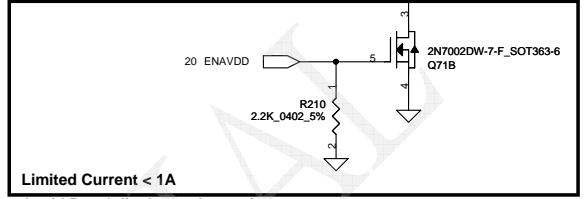
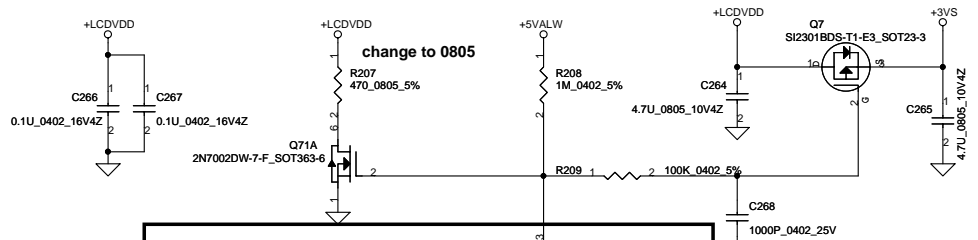
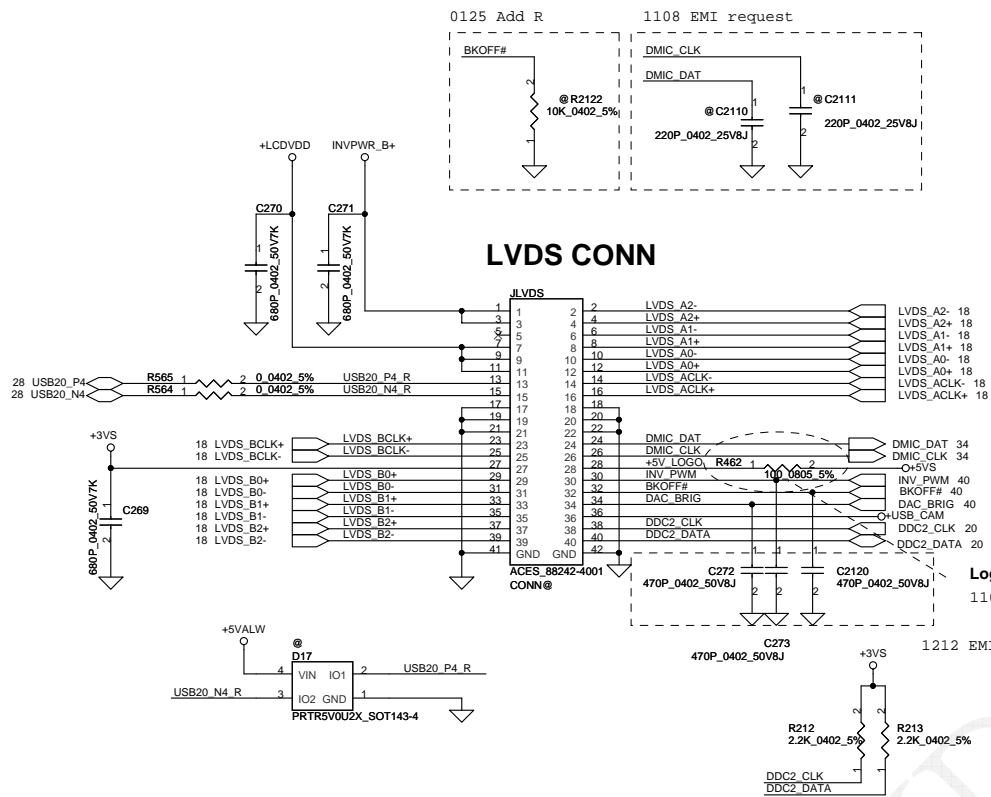


CRT Termination/EMI Filter

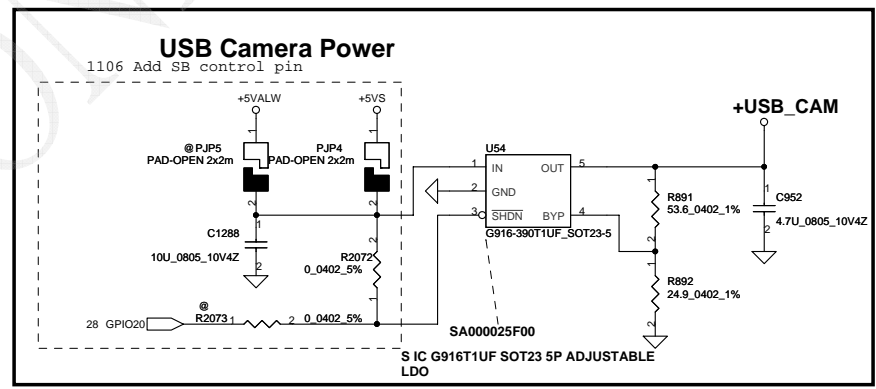
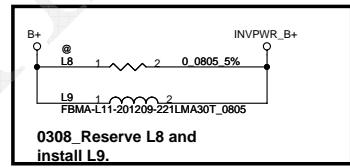
Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.



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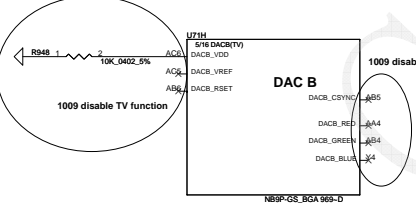
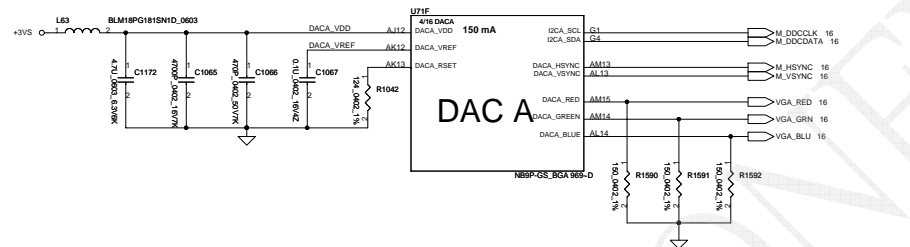
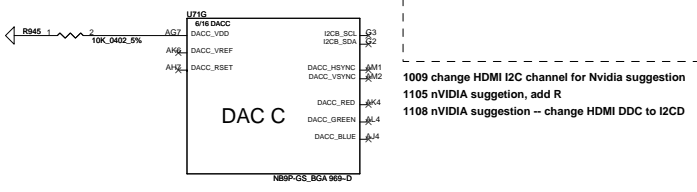
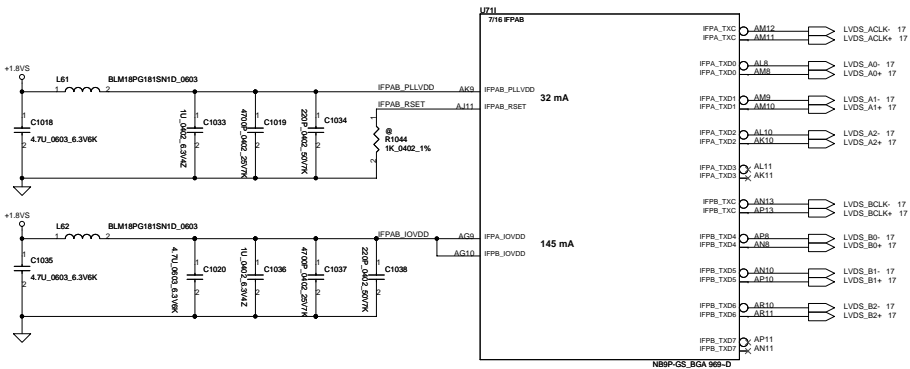


Avoid Panel display garbage after power on.

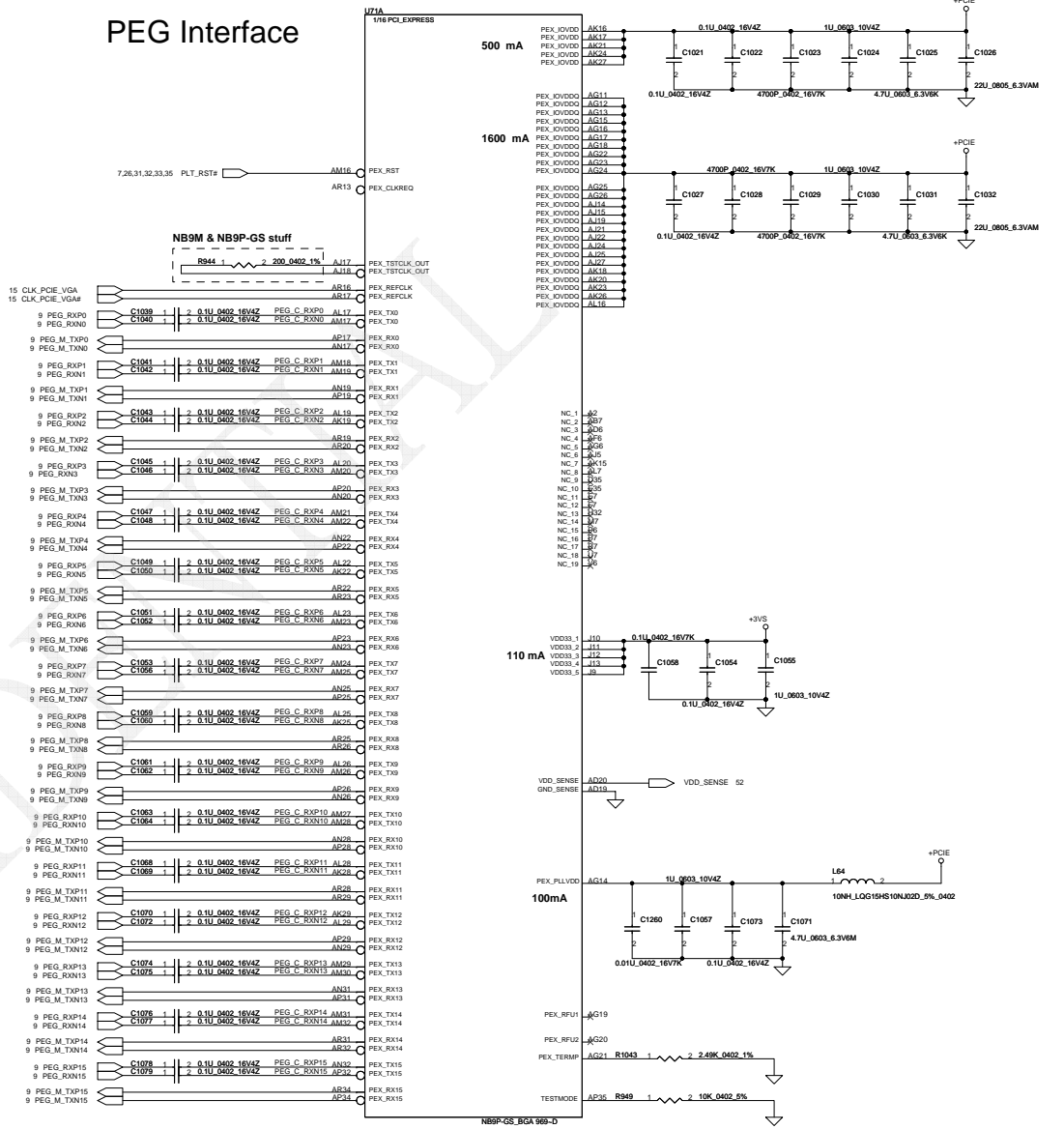


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Date:	Thursday, October 22, 2009		Sheet	17 of 61		

LVDS & DAC Interface



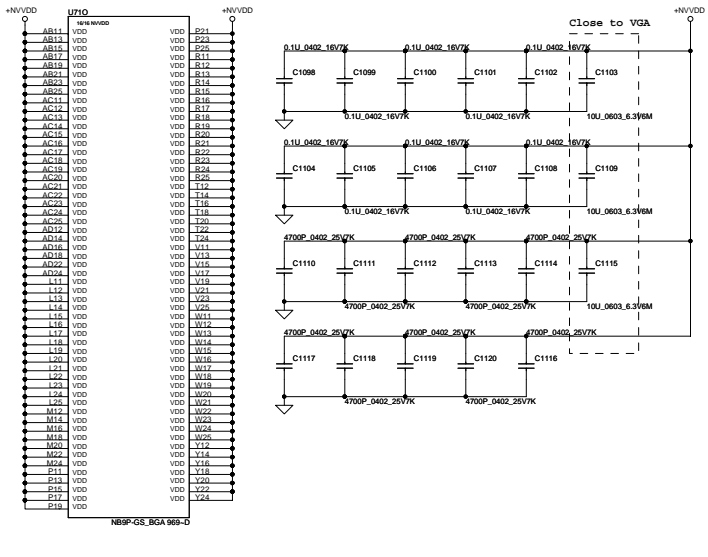
PEG Interface



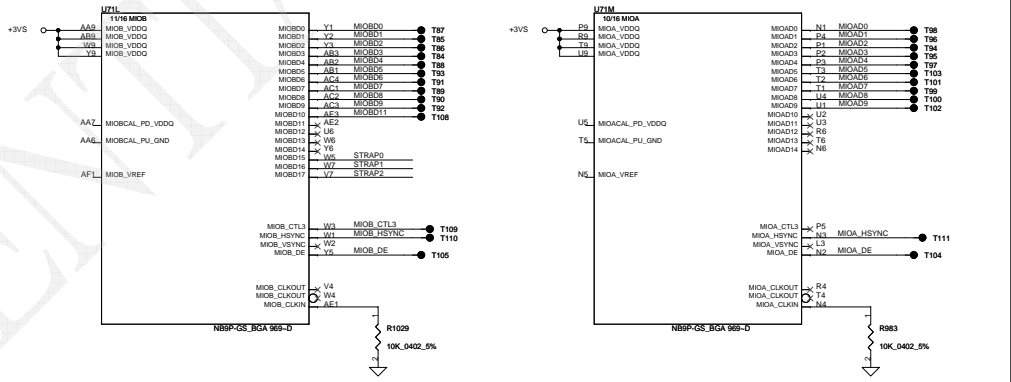
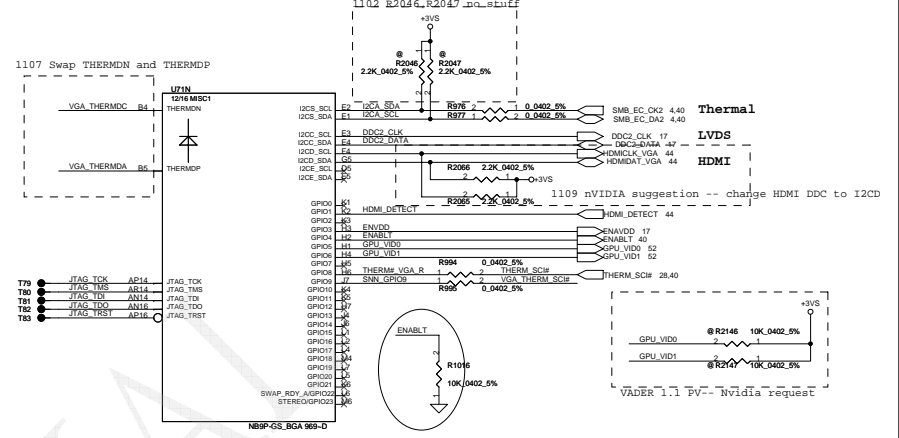
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VGA Core power

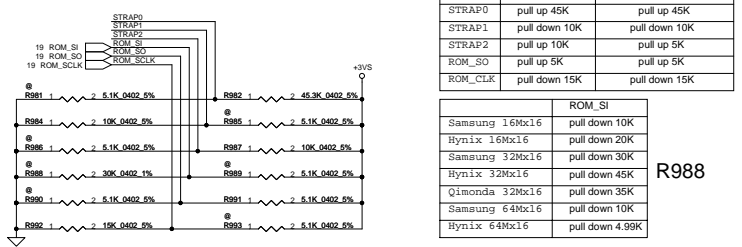


GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



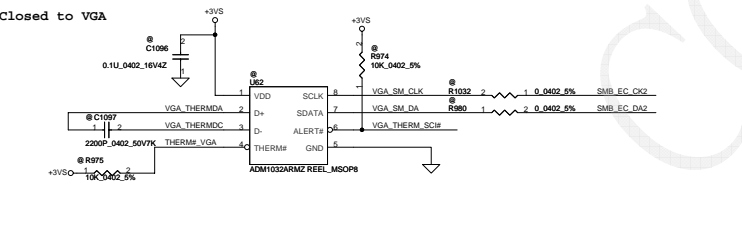
MULTI LEVEL STRAPS For NB9M-Gx (64bit)

NB9P-GS and NB9P-GE2 is as same as NB9M-GE-B



STRAP2 -- R987

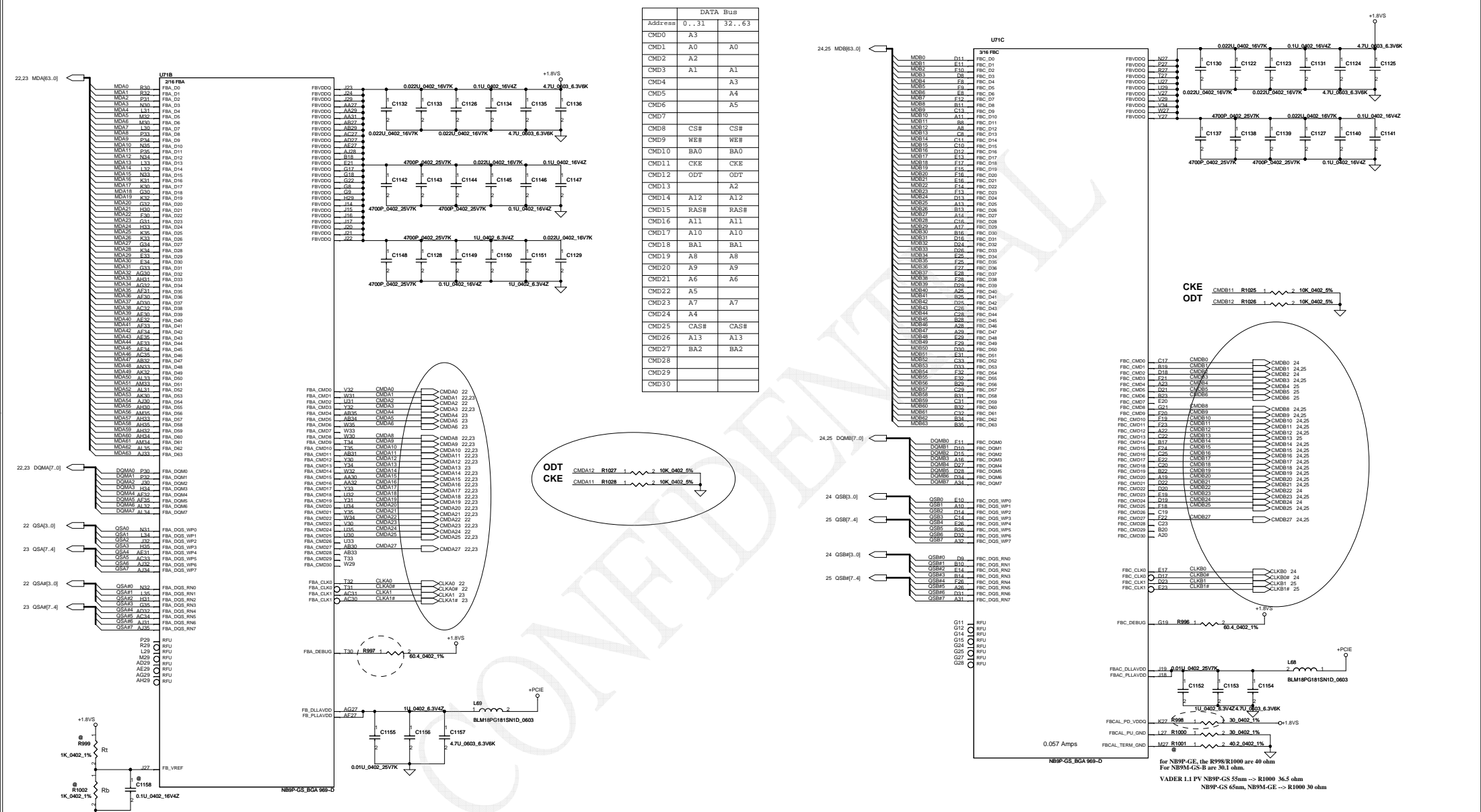
VGA Thermal Sensor ADM1032ARMZ



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Compal Electronics, Inc.
SCHMATIC, MB A4083

VRAM Interface



VREF = 0.5 * FBVDDQ
 DDR2: 1.0V = 2.0V * 1K/(1K + 1K)
 FBVREF = FBVDDQ * Rb/(Rt + Rb)

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			SCHMATIC, MB A4083

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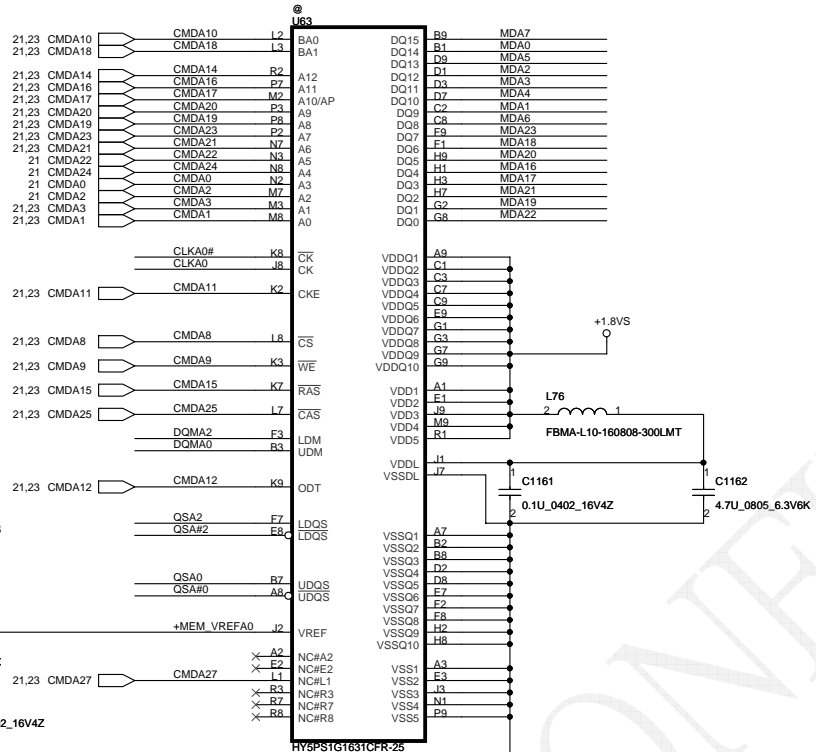
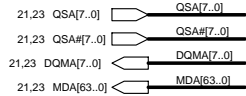
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for NB9P-GE: the R998/R1000 are 40 ohm
 For NB9M-GE-B are 30.1 ohm
 VADER I.1 PV NB9P-GS 55um -> R1000 36.5 ohm
 NB9P-GS 65um, NB9M-GE -> R1000 30 ohm

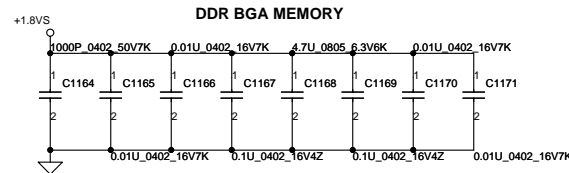
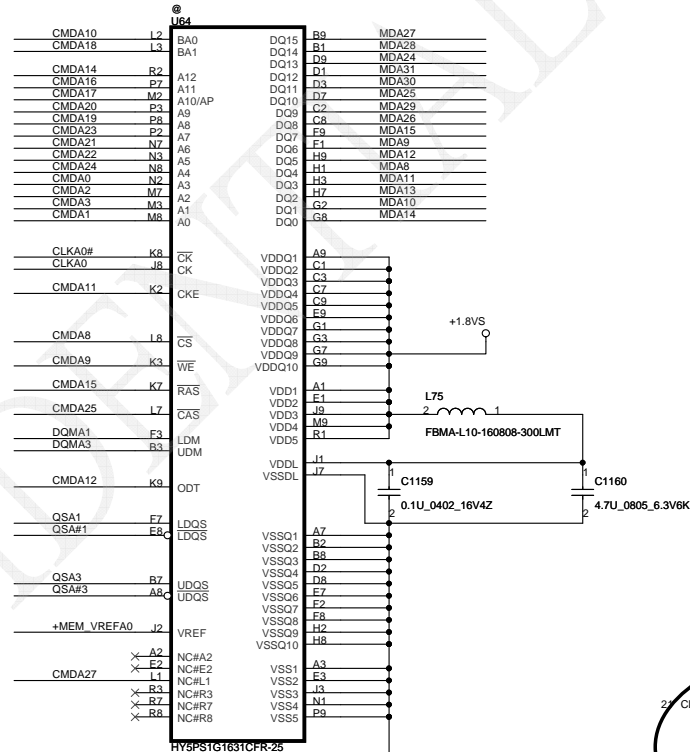
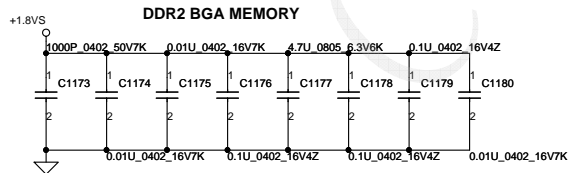
VRAM DDR2 chips (512MB & 1GB)

64Mx16 DDR2 400MHz *8==>1GB

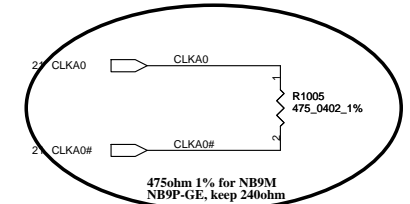
64Mx16 DDR2 400MHz *4==>512MB



Vref = 0.5 * 1.8V for NB9M, R1004=1K ohm
 Vref = 0.5 * 1.8V for NB9P-GS/GE, R1004=1K ohm



		DATA Bus	
Address	0..31	32..63	
CMD0	A3		
CMD1	A0	A0	
CMD2	A2		
CMD3	A1	A1	
CMD4		A3	
CMD5		A4	
CMD6		A5	
CMD7			
CMD8	CS#	CS#	
CMD9	WE#	WE#	
CMD10	BA0	BA0	
CMD11	CKE	CKE	
CMD12	ODT	ODT	
CMD13		A2	
CMD14	A12	A12	
CMD15	RAS#	RAS#	
CMD16	A11	A11	
CMD17	A10	A10	
CMD18	BA1	BA1	
CMD19	A8	A8	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A5		
CMD23	A7	A7	
CMD24	A4		
CMD25	CAS#	CAS#	
CMD26	A13	A13	
CMD27	BA2	BA2	
CMD28			
CMD29			
CMD30			



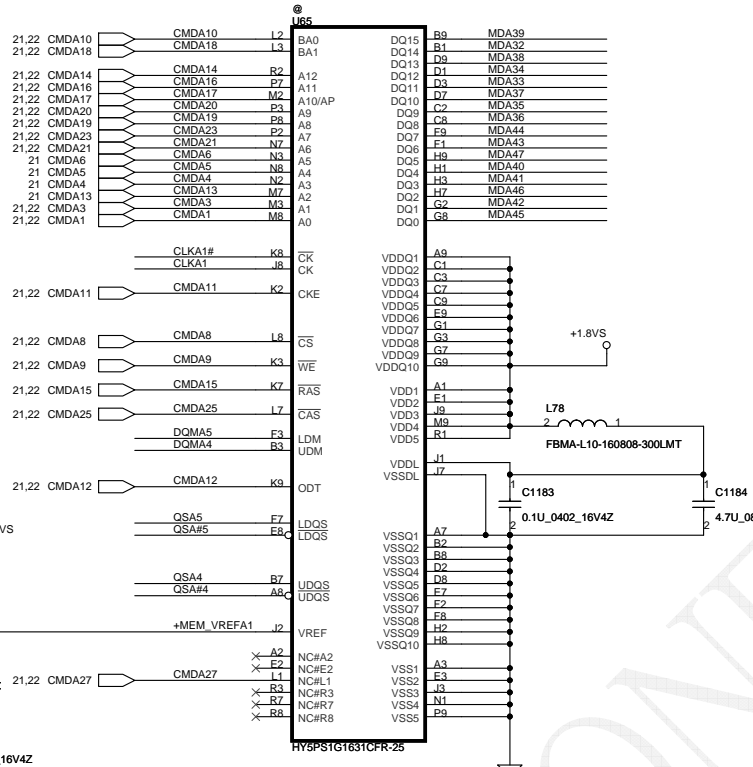
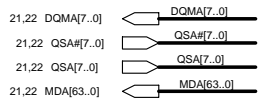
475ohm 1% for NB9M
 NB9P-GE, keep 240ohm

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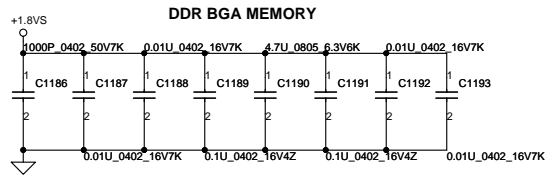
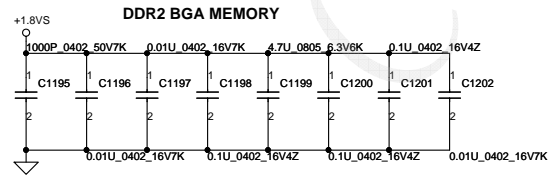
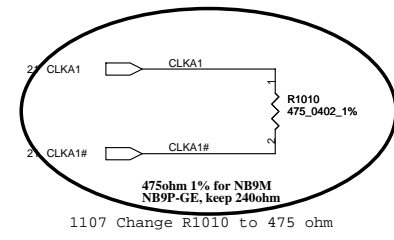
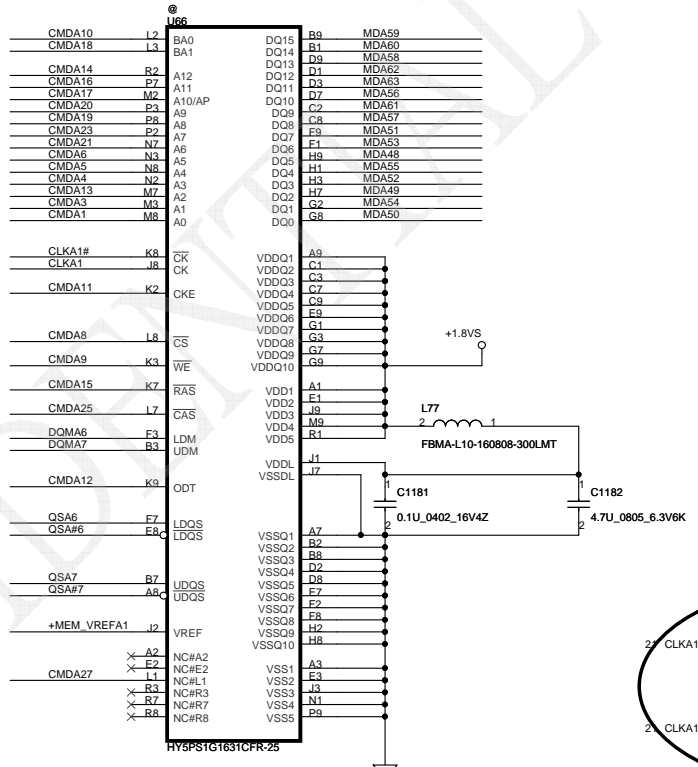
VRAM DDR2 chips (512MB & 1GB)

64Mx16 DDR2 400MHz *8==>1GB

64Mx16 DDR2 400MHz *4==>512MB



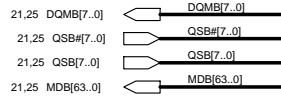
Vref= 0.5* 1.8V for NB9M, R1009=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1009=1K ohm



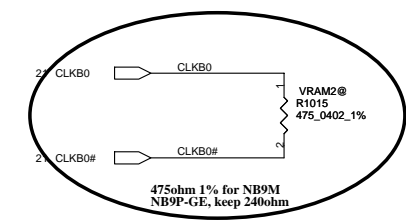
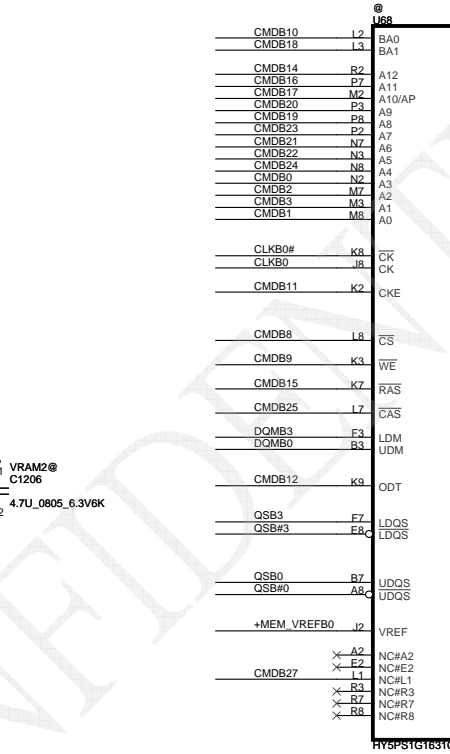
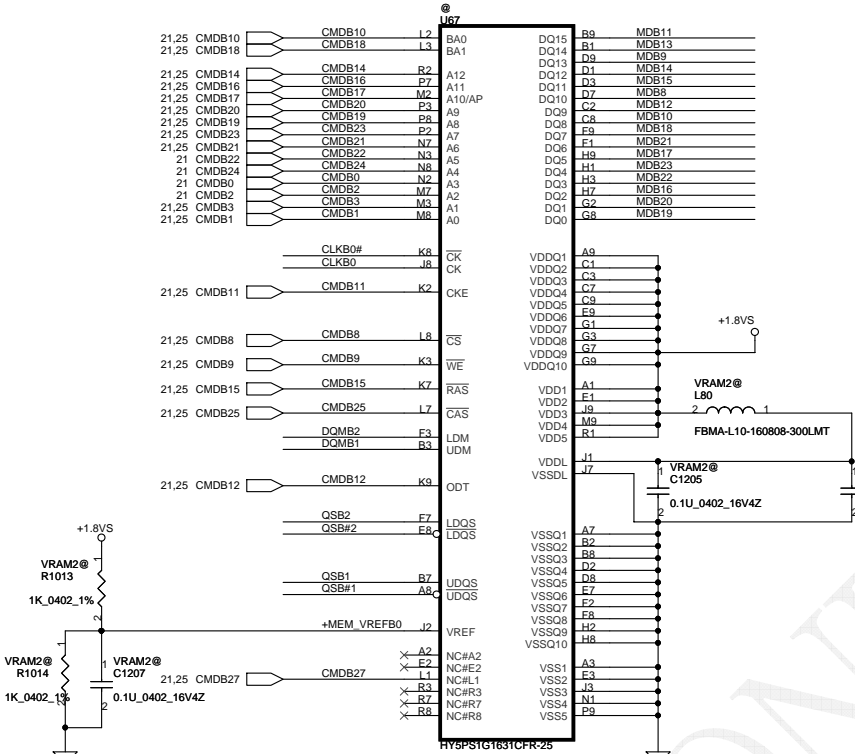
Address	DATA Bus	
	0..31	32..63
CMD0	A3	A3
CMD1	A0	A0
CMD2	A2	A2
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	A5
CMD23	A7	A7
CMD24	A4	A4
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

VRAM DDR2 chips (512MB & 1GB)

64Mx16 DDR2 400MHz *8==>1GB

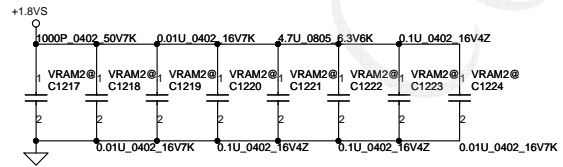


		DATA Bus	
Address	0..31	32..63	
CMD0	A3		
CMD1	A0	A0	
CMD2	A2		
CMD3	A1	A1	
CMD4		A3	
CMD5		A4	
CMD6		A5	
CMD7			
CMD8	CS#	CS#	
CMD9	WE#	WE#	
CMD10	BA0	BA0	
CMD11	CKE	CKE	
CMD12	ODT	ODT	
CMD13		A2	
CMD14	A12	A12	
CMD15	RAS#	RAS#	
CMD16	A11	A11	
CMD17	A10	A10	
CMD18	BA1	BA1	
CMD19	A8	A8	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A5	A5	
CMD23	A7	A7	
CMD24	A4	A4	
CMD25	CAS#	CAS#	
CMD26	A13	A13	
CMD27	BA2	BA2	
CMD28			
CMD29			
CMD30			

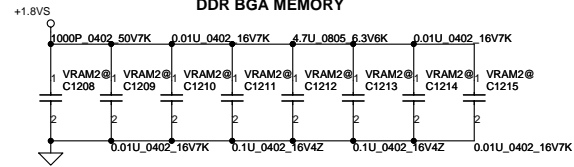


Vref= 0.5* 1.8V for NB9M, R1014=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1014=1K ohm

DDR2 BGA MEMORY



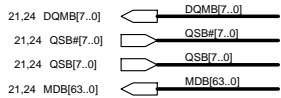
DDR2 BGA MEMORY



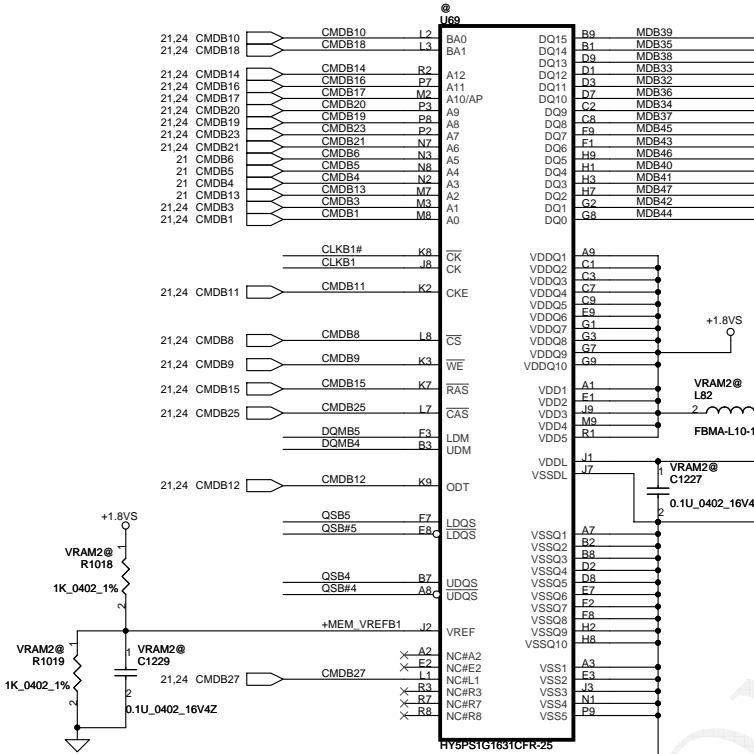
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Issued Date	2006/02/13	Deciphered Date	
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Rev	401622	Date	Thursday, October 22, 2009
Sheet	24	of	61

VRAM DDR2 chips (512MB & 1GB)

64Mx16 DDR2 400MHz *8==>1GB

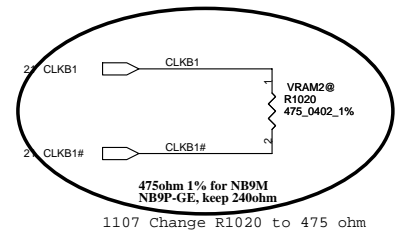
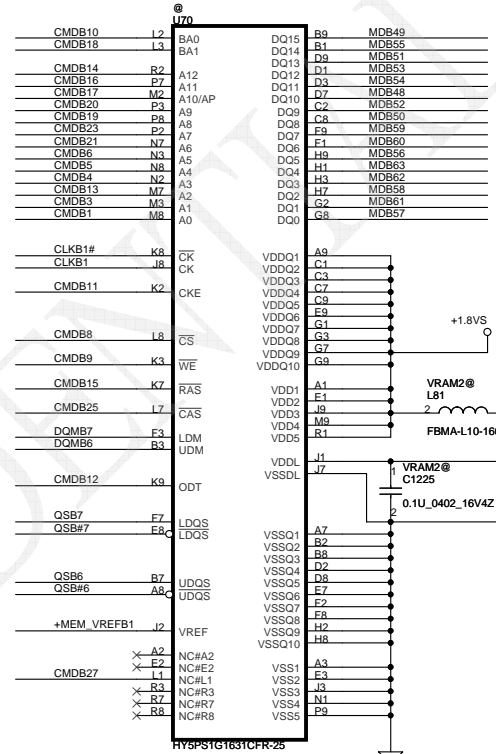
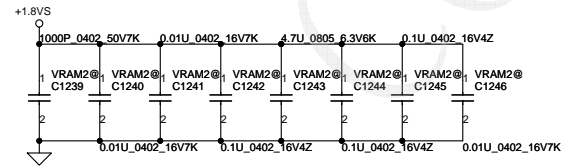


		DATA Bus	
Address	0..31	32..63	
CMD0	A3		
CMD1	A0	A0	
CMD2	A2		
CMD3	A1	A1	
CMD4		A3	
CMD5		A4	
CMD6		A5	
CMD7			
CMD8	CS#	CS#	
CMD9	WE#	WE#	
CMD10	BA0	BA0	
CMD11	CKE	CKE	
CMD12	ODT	ODT	
CMD13		A2	
CMD14	A12	A12	
CMD15	RAS#	RAS#	
CMD16	A11	A11	
CMD17	A10	A10	
CMD18	BA1	BA1	
CMD19	A8	A8	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A5		
CMD23	A7	A7	
CMD24	A4		
CMD25	CAS#	CAS#	
CMD26	A13	A13	
CMD27	BA2	BA2	
CMD28			
CMD29			
CMD30			

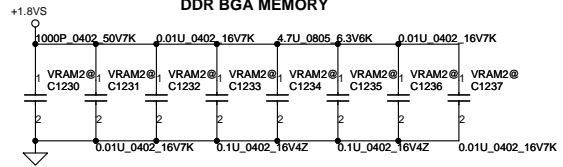


Vref= 0.5* 1.8V for NB9M, R1019=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1019=1K ohm

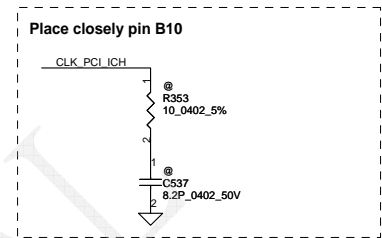
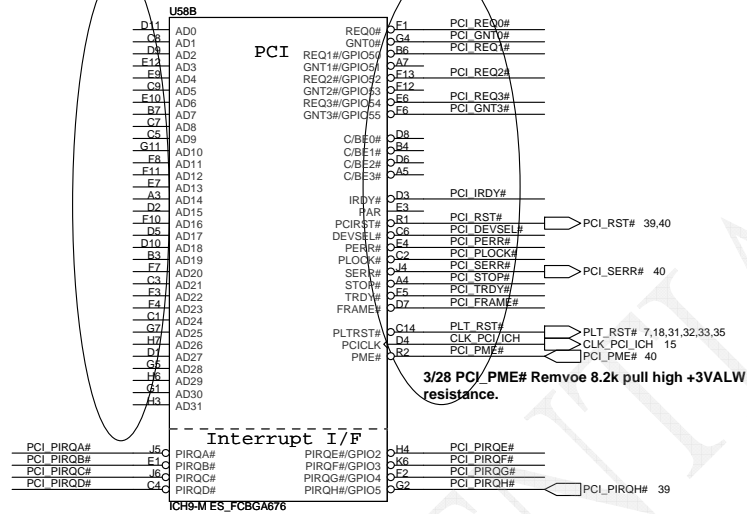
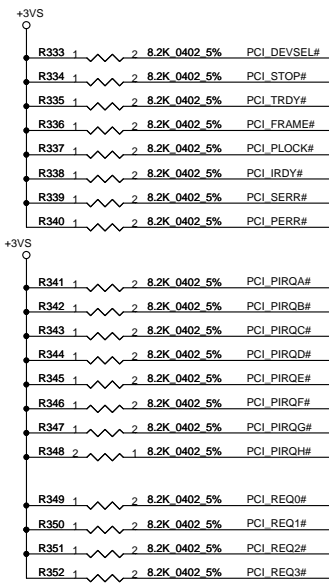
DDR2 BGA MEMORY



DDR BGA MEMORY



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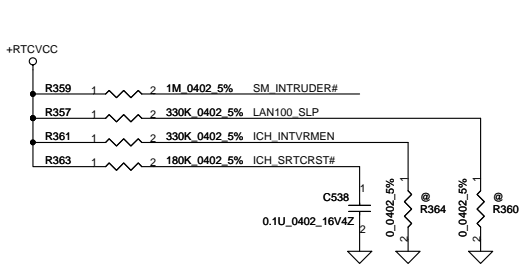
Interrupt I/F

A16 swap override Strap

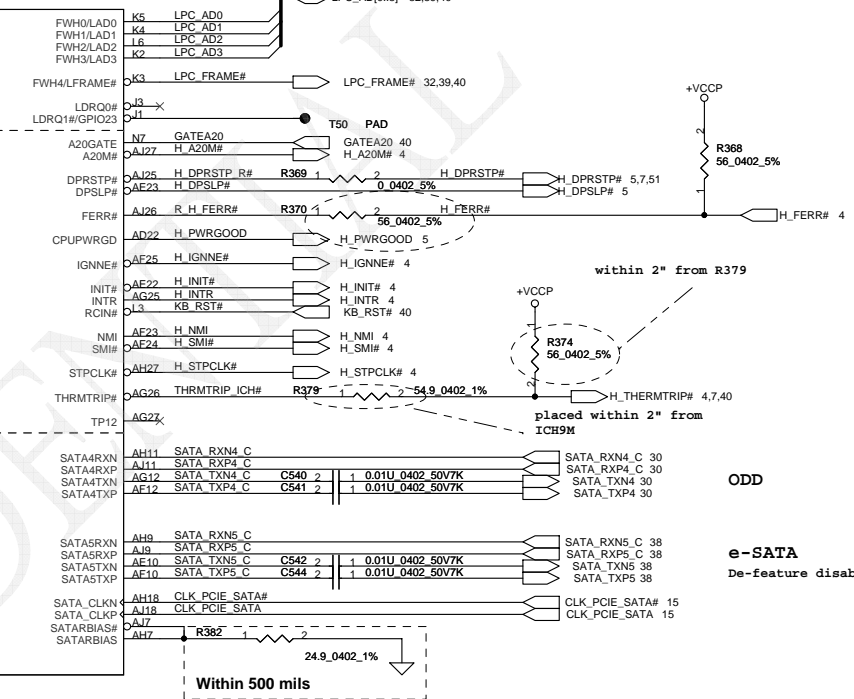
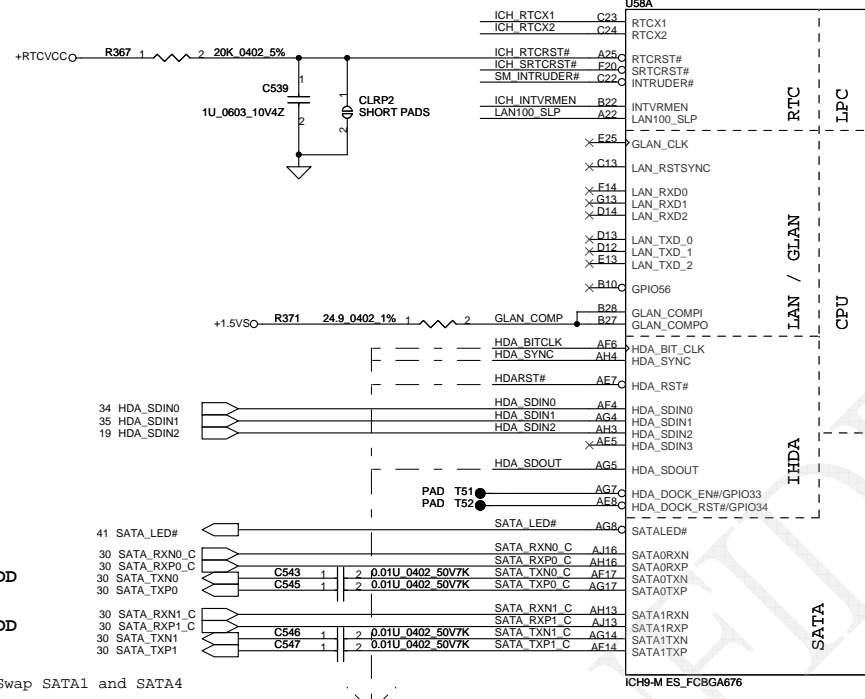
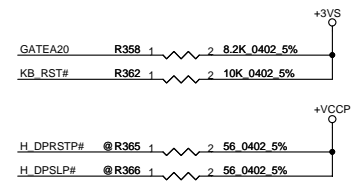
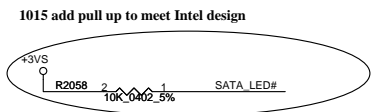
PCI_GNT3#	Low= A16 swap override Enable High= Default*
------------------	---

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

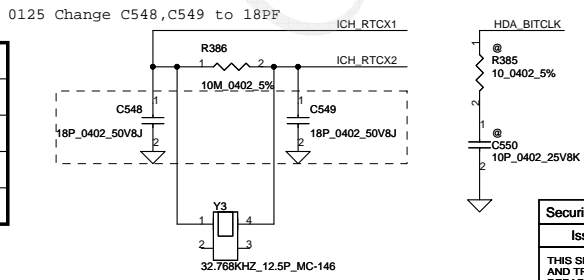
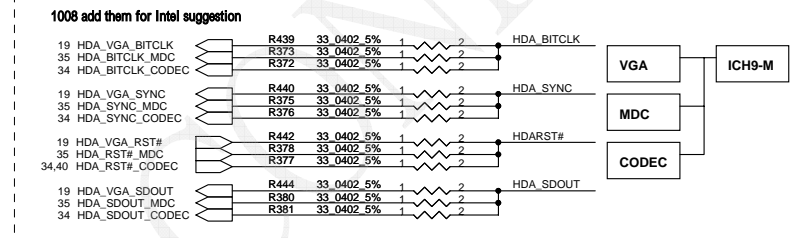
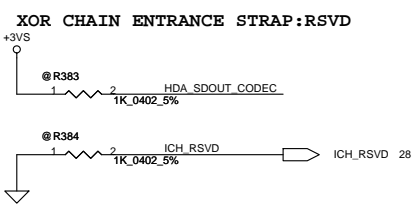


ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

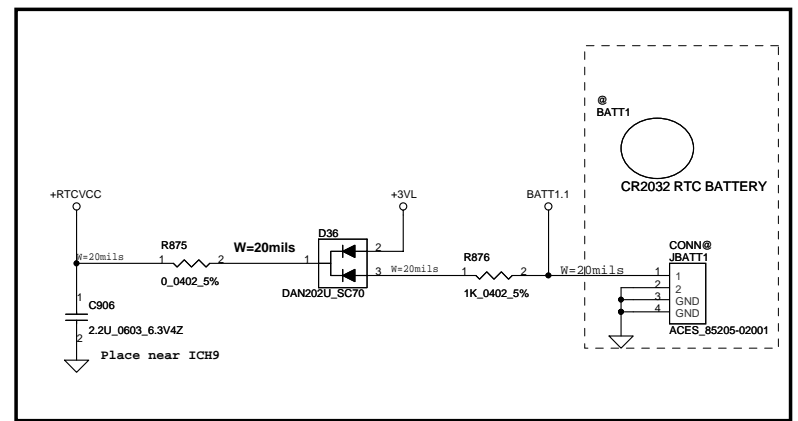


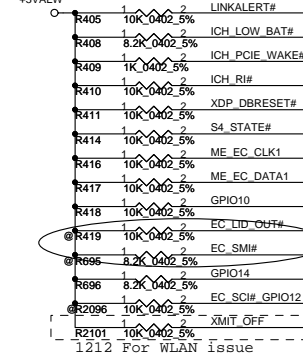
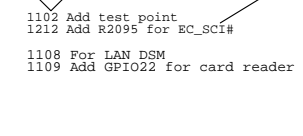
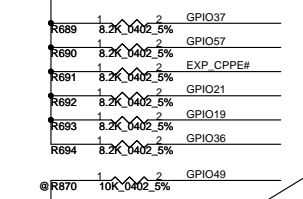
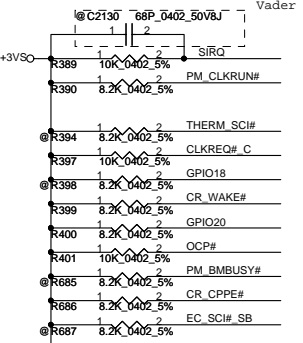
P- HDD
S- HDD
1212 Swap SATA1 and SATA4

ODD
e-SATA
De-feature disable



ICH_RSVD	HDA_SDOUT_CODECC	
0	0	
0	1	
1	0	
1	1	





0718 INSTALL R179

low ---> default
High ---> No boot

WLAN

Robson

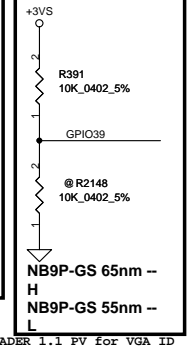
TV Tuner

GLAN

1394_CR1

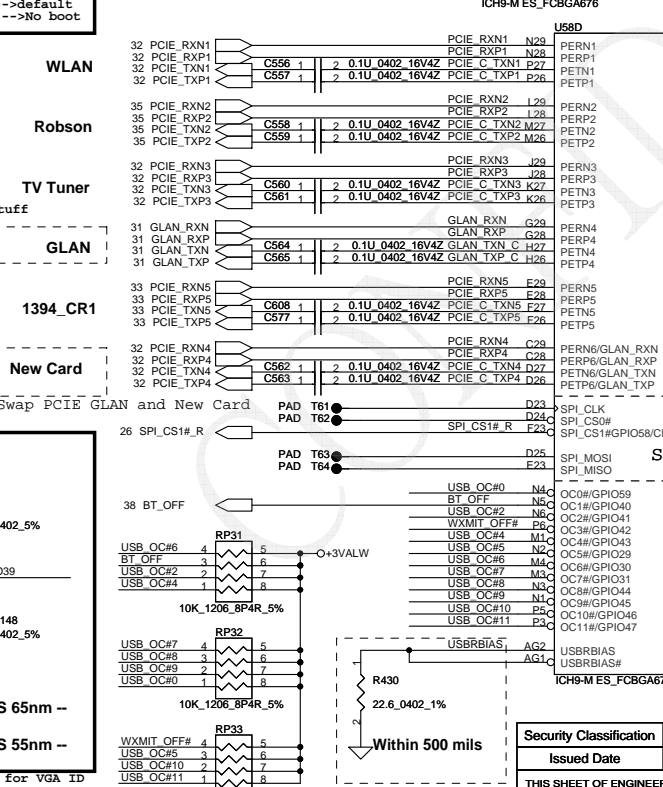
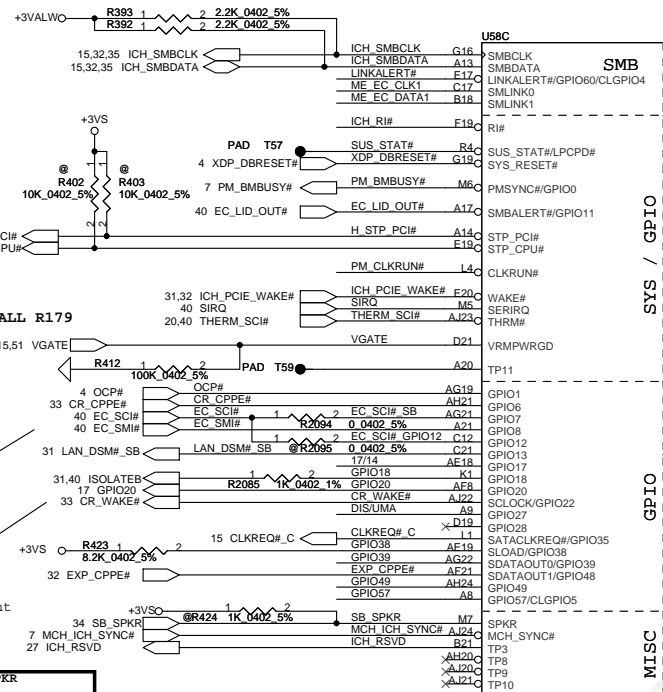
New Card

1212 Swap PCIe GLAN and New Card

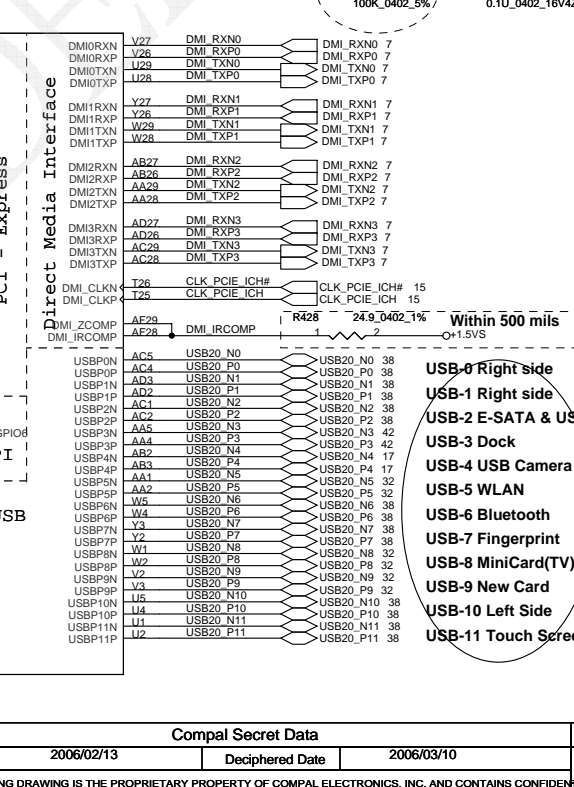
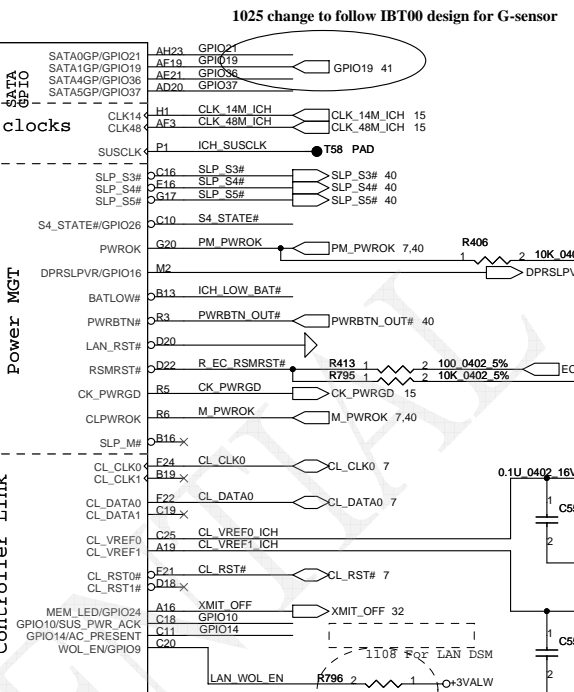


1008 add board ID detection

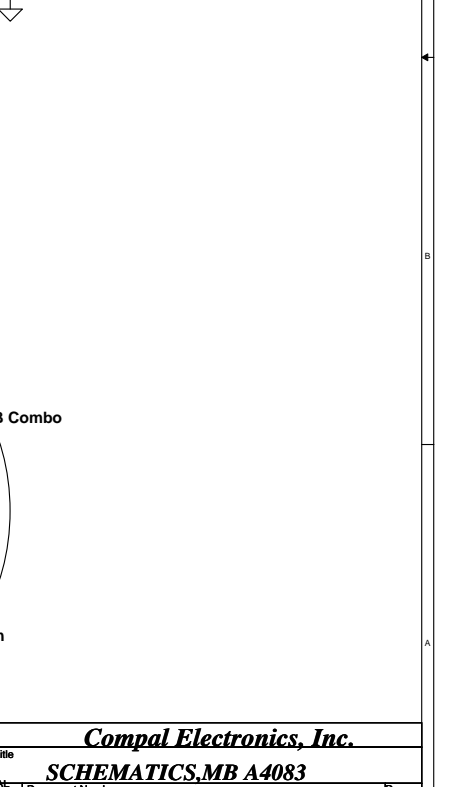
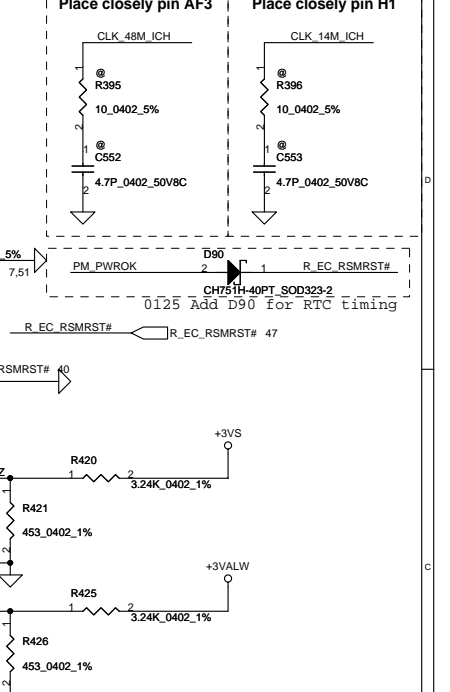
VADER 1.1 PV for VGA ID



10K_1206_8P4R_5%



10K_1206_8P4R_5%

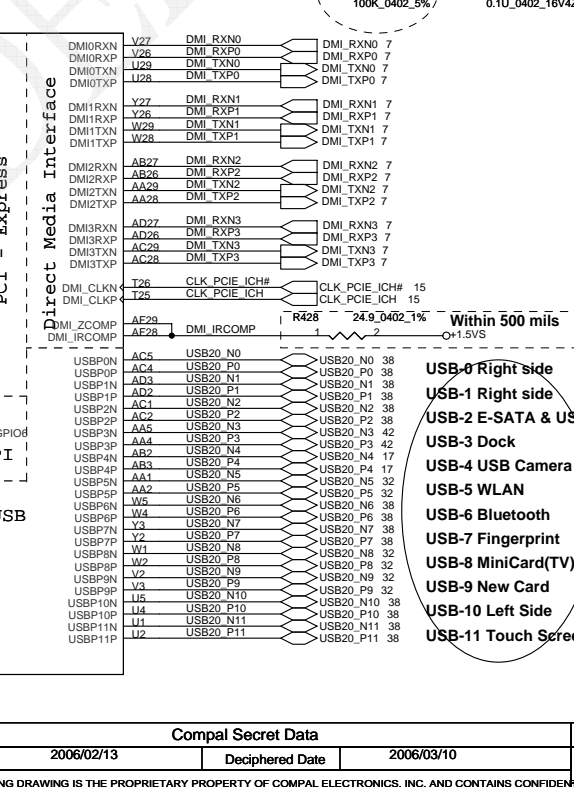
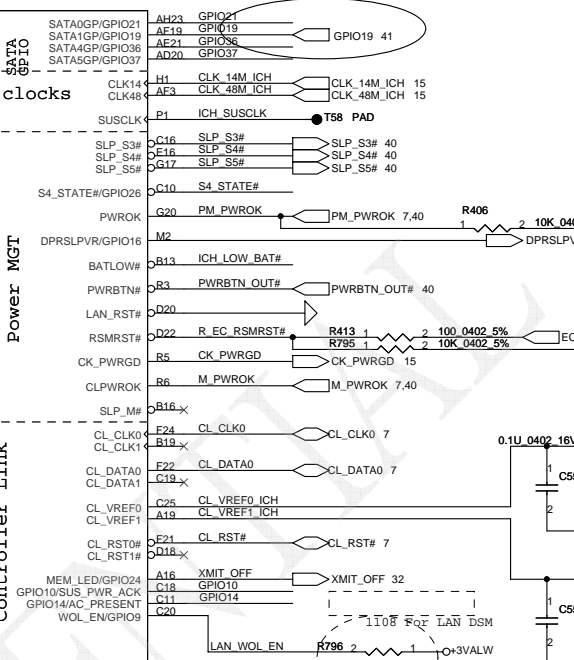


10K_1206_8P4R_5%

1025 change to follow IBT00 design for G-sensor

Place closely pin AF3

Place closely pin H1



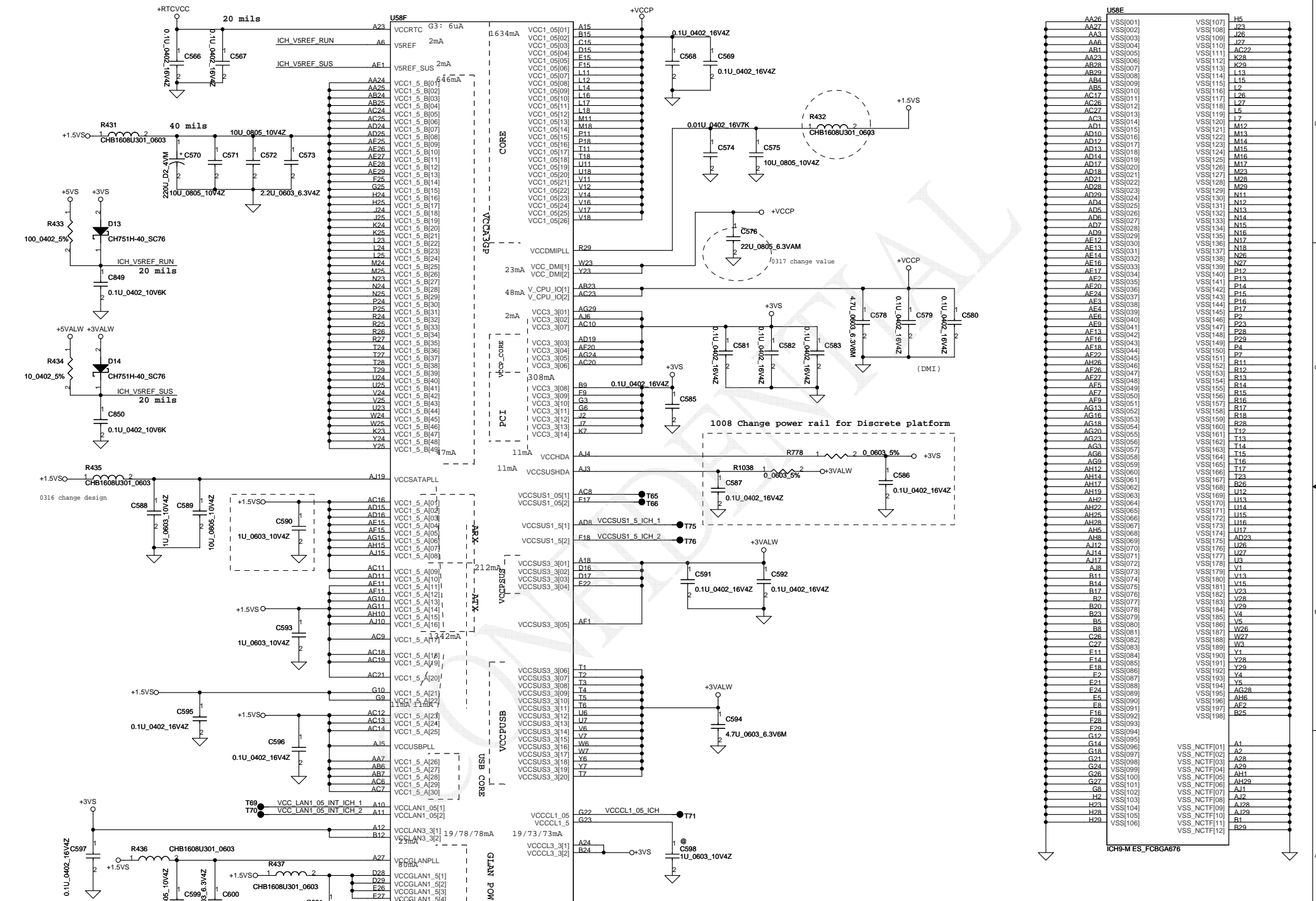
10K_1206_8P4R_5%

Security Classification	Compal Secret Data	
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		2006/03/10

- USB-0 Right side
- USB-1 Right side
- USB-2 E-SATA & USB Combo
- USB-3 Dock
- USB-4 USB Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Fingerprint
- USB-8 MiniCard(TV)
- USB-9 New Card
- USB-10 Left Side
- USB-11 Touch Screen

Compal Electronics, Inc.	
Document Number	SCHEMATICS.MB A4083
Rev	E

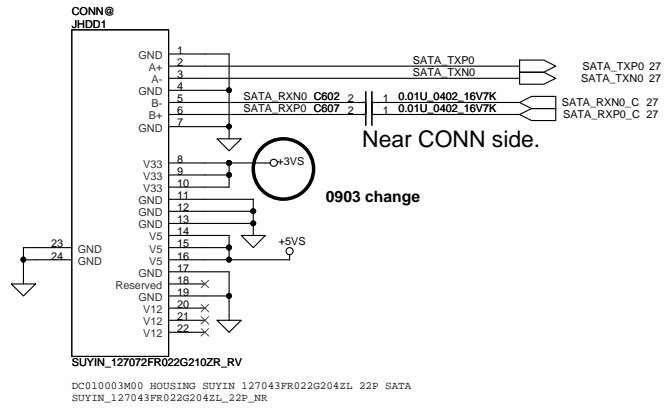
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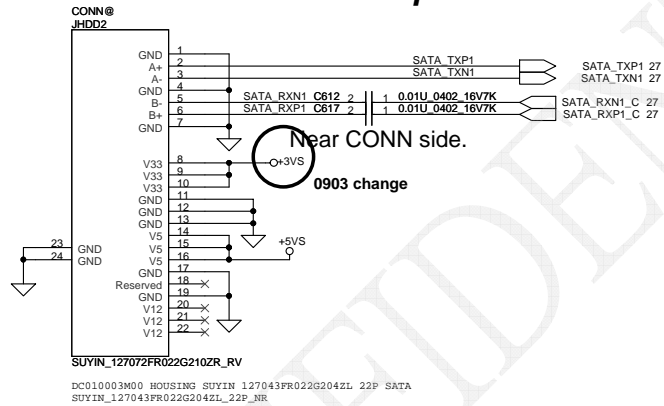
U58F	VSS[001]	VSS[107]	H5
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	L2
AA3	VSS[003]	VSS[109]	J26
AA6	VSS[004]	VSS[110]	J27
AA6	VSS[005]	VSS[111]	AC22
AA23	VSS[006]	VSS[112]	K28
AB23	VSS[007]	VSS[113]	K29
AB23	VSS[008]	VSS[114]	L13
AB6	VSS[009]	VSS[115]	L15
AB6	VSS[010]	VSS[116]	L2
AC17	VSS[011]	VSS[117]	L26
AC28	VSS[012]	VSS[118]	L27
AC3	VSS[013]	VSS[119]	L7
AD1	VSS[014]	VSS[120]	M12
AD10	VSS[015]	VSS[121]	M17
AD10	VSS[016]	VSS[122]	M13
AD13	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD22	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	M29
AD29	VSS[024]	VSS[130]	N11
AD4	VSS[025]	VSS[131]	N12
AD6	VSS[026]	VSS[132]	N13
AD6	VSS[027]	VSS[133]	N14
AD7	VSS[028]	VSS[134]	N15
AD9	VSS[029]	VSS[135]	N16
AE1	VSS[030]	VSS[136]	N17
AE13	VSS[031]	VSS[137]	N18
AE14	VSS[032]	VSS[138]	N26
AE16	VSS[033]	VSS[139]	N27
AE2	VSS[034]	VSS[140]	P13
AE24	VSS[035]	VSS[141]	P14
AE24	VSS[036]	VSS[142]	P15
AE3	VSS[037]	VSS[143]	P17
AE4	VSS[038]	VSS[144]	P2
AE6	VSS[039]	VSS[145]	P2
AE9	VSS[040]	VSS[146]	P28
AE9	VSS[041]	VSS[147]	P28
AE18	VSS[042]	VSS[148]	P29
AE18	VSS[043]	VSS[149]	P4
AE22	VSS[044]	VSS[150]	P8
AE22	VSS[045]	VSS[151]	P7
AH26	VSS[046]	VSS[152]	R11
AH27	VSS[047]	VSS[153]	R12
AF2	VSS[048]	VSS[154]	R13
AF5	VSS[049]	VSS[155]	R14
AF7	VSS[050]	VSS[156]	R15
AG3	VSS[051]	VSS[157]	R16
AG13	VSS[052]	VSS[158]	R17
AG16	VSS[053]	VSS[159]	R18
AG18	VSS[054]	VSS[160]	R28
AG23	VSS[055]	VSS[161]	T13
AG3	VSS[056]	VSS[162]	T14
AG6	VSS[057]	VSS[163]	T15
AH12	VSS[058]	VSS[164]	T16
AH12	VSS[059]	VSS[165]	T17
AH14	VSS[060]	VSS[166]	T23
AH17	VSS[061]	VSS[167]	T26
AH22	VSS[062]	VSS[168]	T26
AH22	VSS[063]	VSS[169]	U12
AH22	VSS[064]	VSS[170]	U14
AH22	VSS[065]	VSS[171]	U14
AH25	VSS[066]	VSS[172]	U15
AH28	VSS[067]	VSS[173]	U16
AH8	VSS[068]	VSS[174]	AD23
AH11	VSS[069]	VSS[175]	U17
AH12	VSS[070]	VSS[176]	U26
AH14	VSS[071]	VSS[177]	U27
AH17	VSS[072]	VSS[178]	U3
B11	VSS[073]	VSS[179]	V13
B14	VSS[074]	VSS[180]	V13
B17	VSS[075]	VSS[181]	V23
B2	VSS[076]	VSS[182]	V28
B20	VSS[077]	VSS[183]	V28
B23	VSS[078]	VSS[184]	V29
B8	VSS[079]	VSS[185]	V4
C26	VSS[080]	VSS[186]	W26
C27	VSS[081]	VSS[187]	W27
E11	VSS[082]	VSS[188]	W3
E14	VSS[083]	VSS[189]	Y1
E18	VSS[084]	VSS[190]	Y28
E2	VSS[085]	VSS[191]	Y29
E21	VSS[086]	VSS[192]	Y4
E21	VSS[087]	VSS[193]	Y4
E24	VSS[088]	VSS[194]	Y5
E5	VSS[089]	VSS[195]	AG28
F18	VSS[090]	VSS[196]	AH6
F20	VSS[091]	VSS[197]	AF2
F28	VSS[092]	VSS[198]	B25
G12	VSS[093]		
G14	VSS[094]	VSS_NCTF[01]	A1
G17	VSS[095]	VSS_NCTF[02]	A2
G21	VSS[096]	VSS_NCTF[03]	A28
G24	VSS[097]	VSS_NCTF[04]	A29
G26	VSS[098]	VSS_NCTF[05]	AH1
G27	VSS[099]	VSS_NCTF[06]	AH28
G8	VSS[100]	VSS_NCTF[07]	AJ1
H2	VSS[101]	VSS_NCTF[08]	AJ2
H23	VSS[102]	VSS_NCTF[09]	AJ28
H28	VSS[103]	VSS_NCTF[10]	BL
H28	VSS[104]	VSS_NCTF[11]	B29
H28	VSS[105]	VSS_NCTF[12]	
H29	VSS[106]		

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Drawn	Customer	401622	Date	Thursday, October 22, 2009
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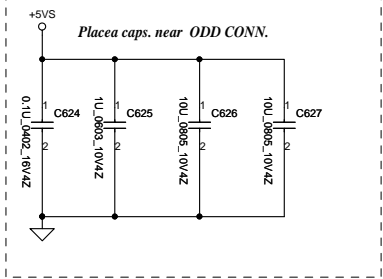
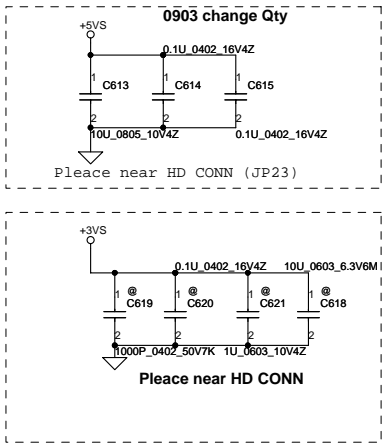
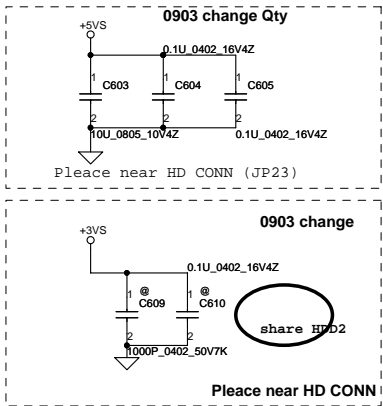
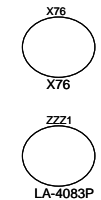
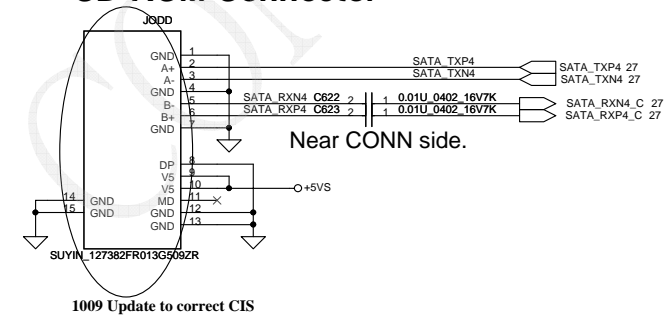
HDD Connector



2nd HDD Connector-option



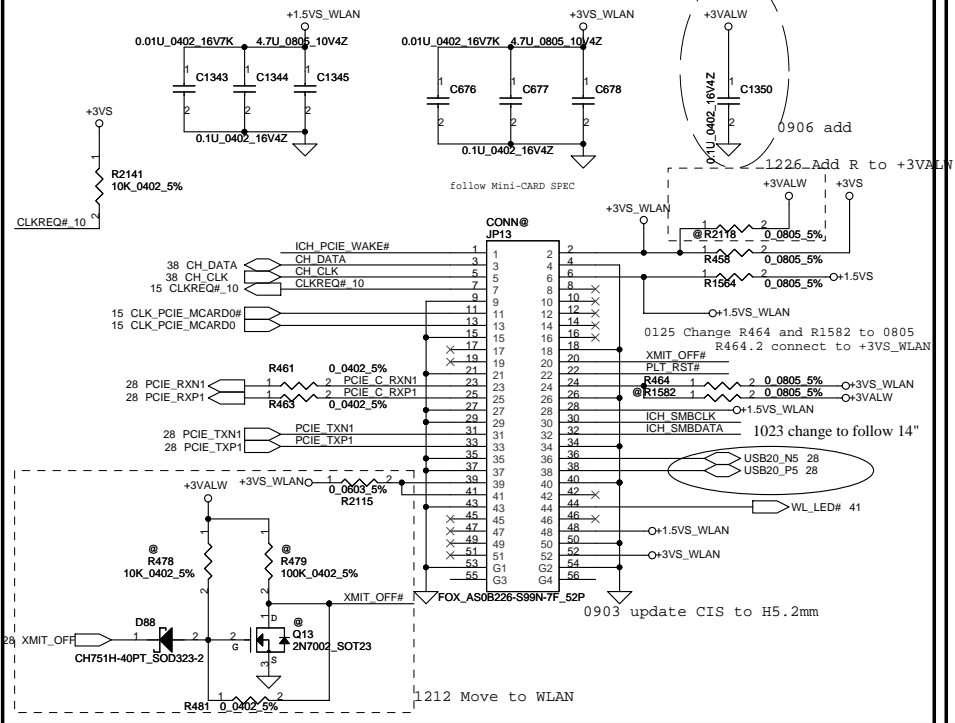
CD-ROM Connector



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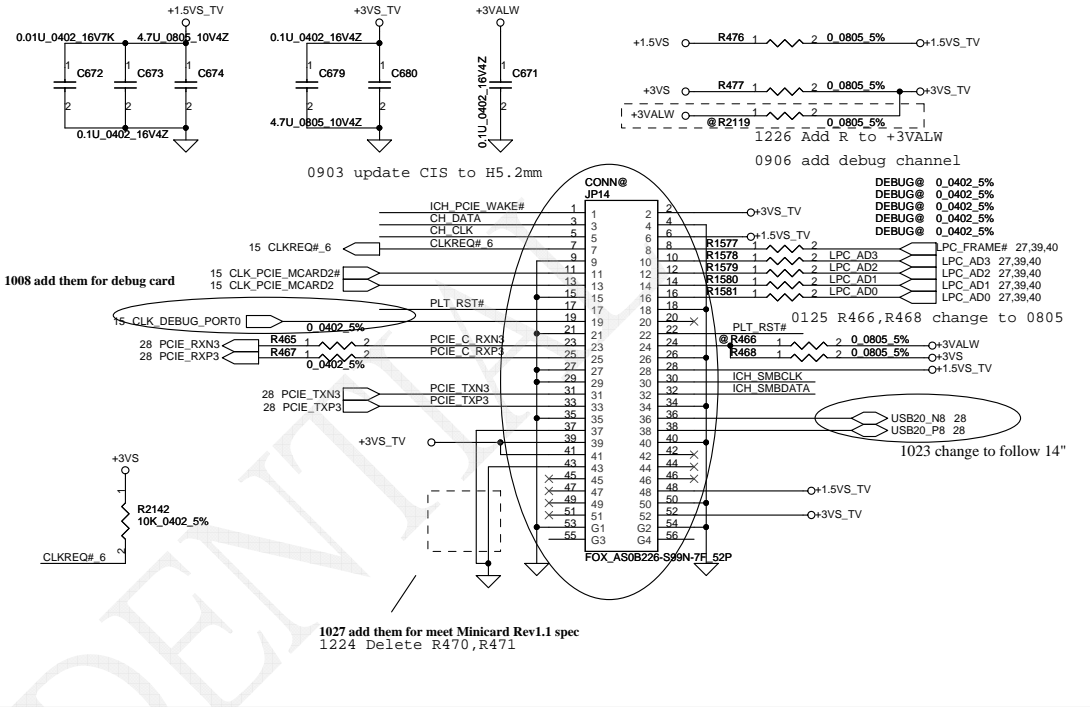
Mini Card 0--WLAN

1022 change to follow HP design

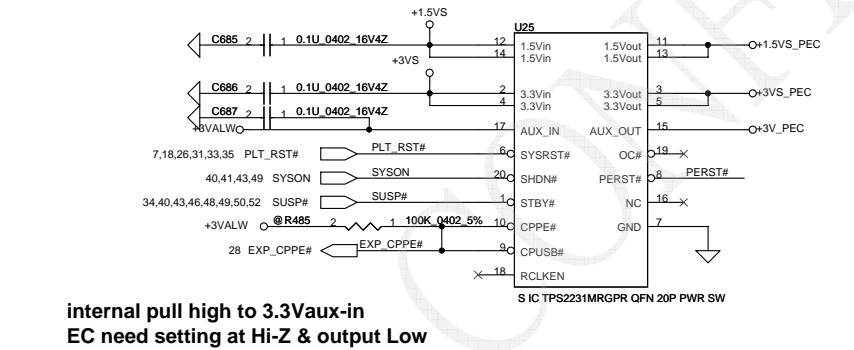


Mini Card 2---TV tuner

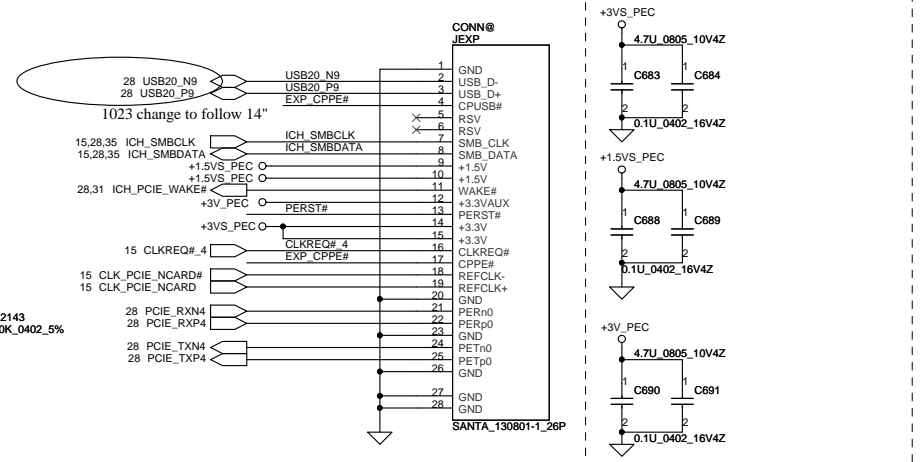
1022 change to follow HP design



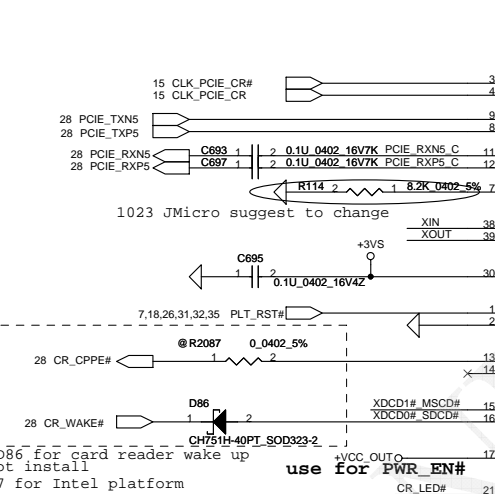
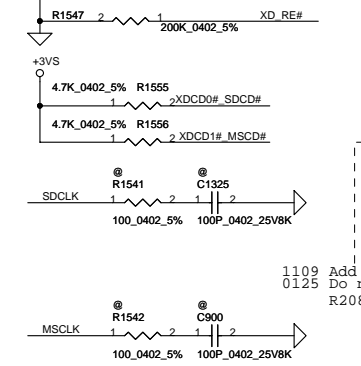
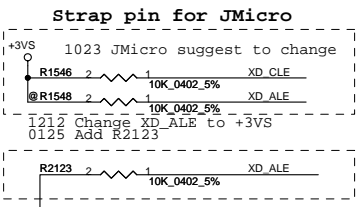
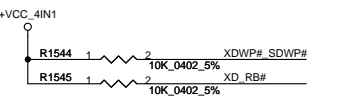
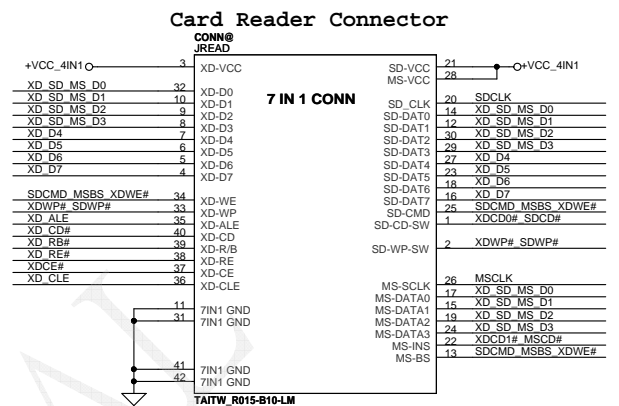
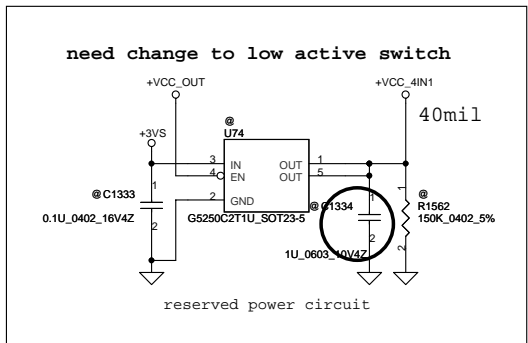
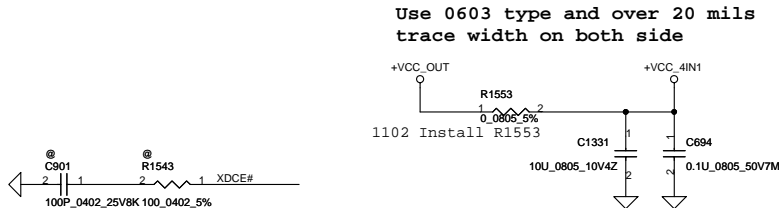
New Card



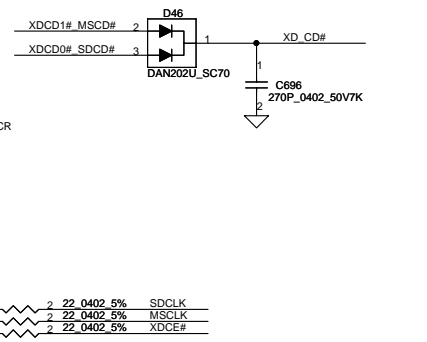
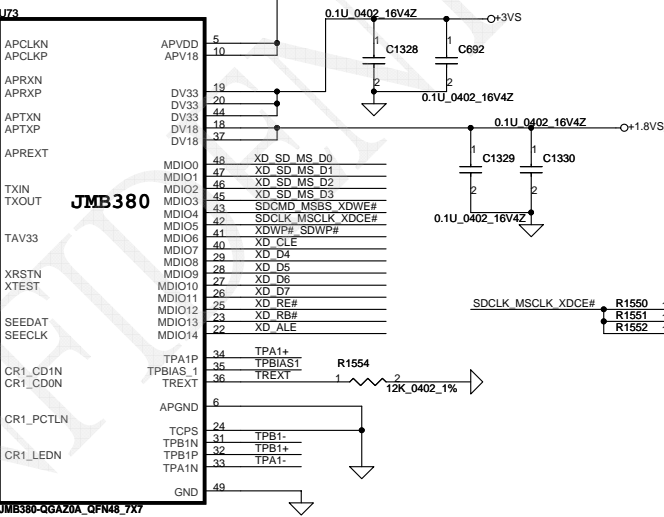
Near to Express Card slot.



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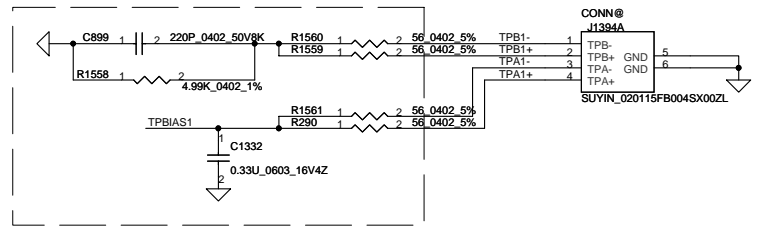
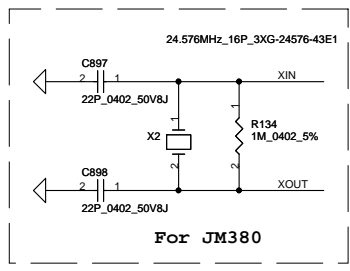
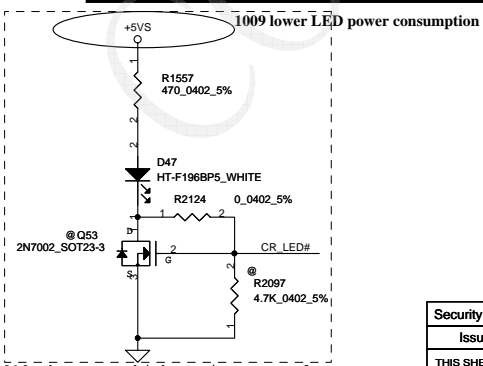


Power Circuit



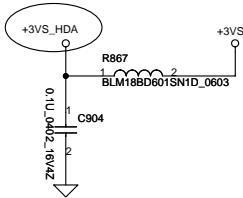
1109 Add D86 for card reader wake up
0125 Do not install R2087 for Intel platform

White LED: VF=3V, IF = 5mA, Res = 56ohm

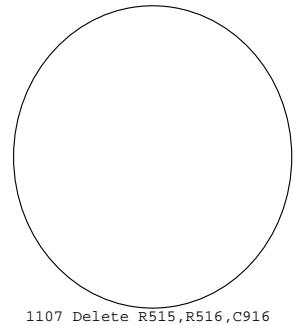
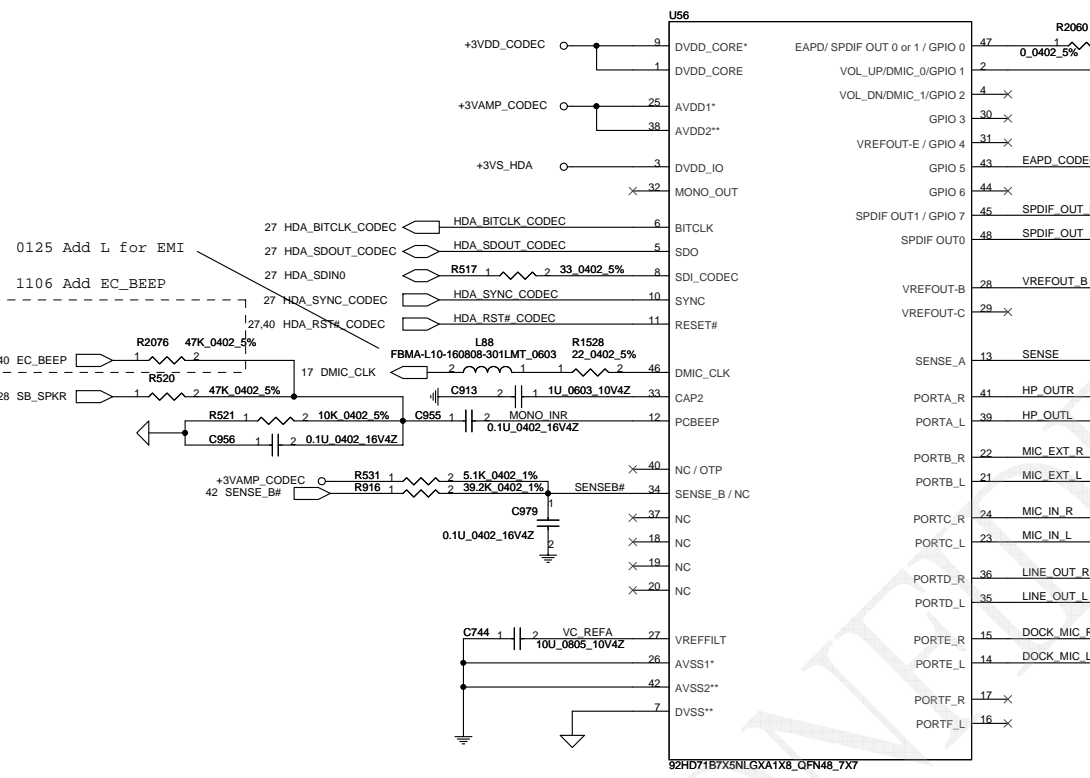
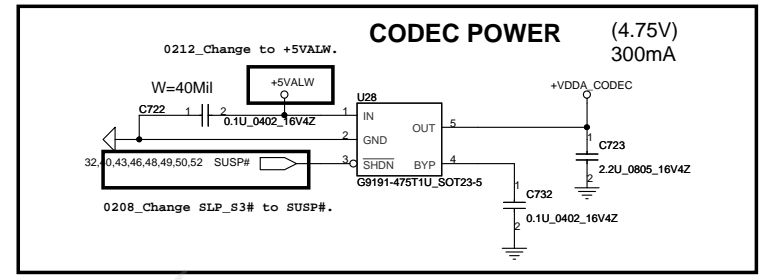
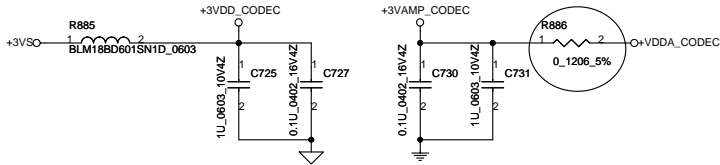


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1008 Change to +3V

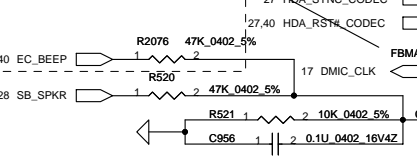


1019 Change Size to 1206 for IDT request



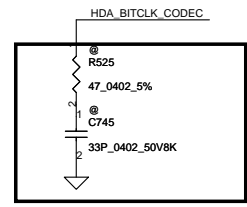
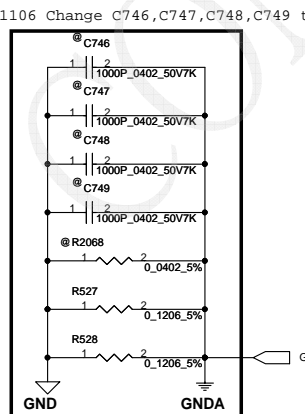
0125 Add L for EMI

1106 Add EC_BEEP



1106 Change C746, C747, C748, C749 to 1000PF

SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



1023 change detection circuit to solve Speaker can not work.

Jack MIC

Internal MIC

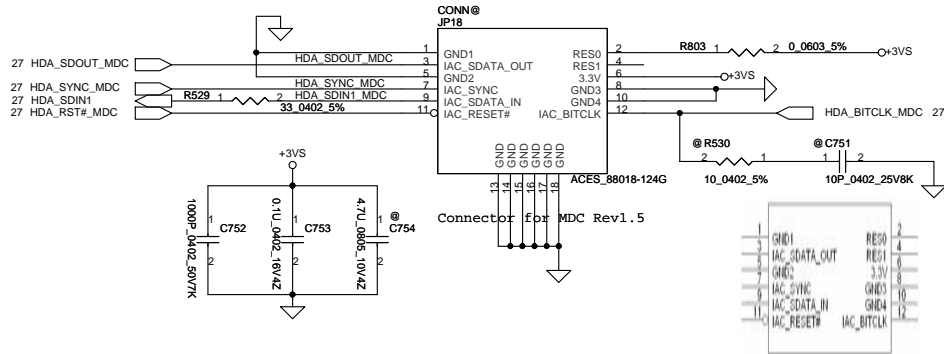
Internal SPKR.

DOCK MIC

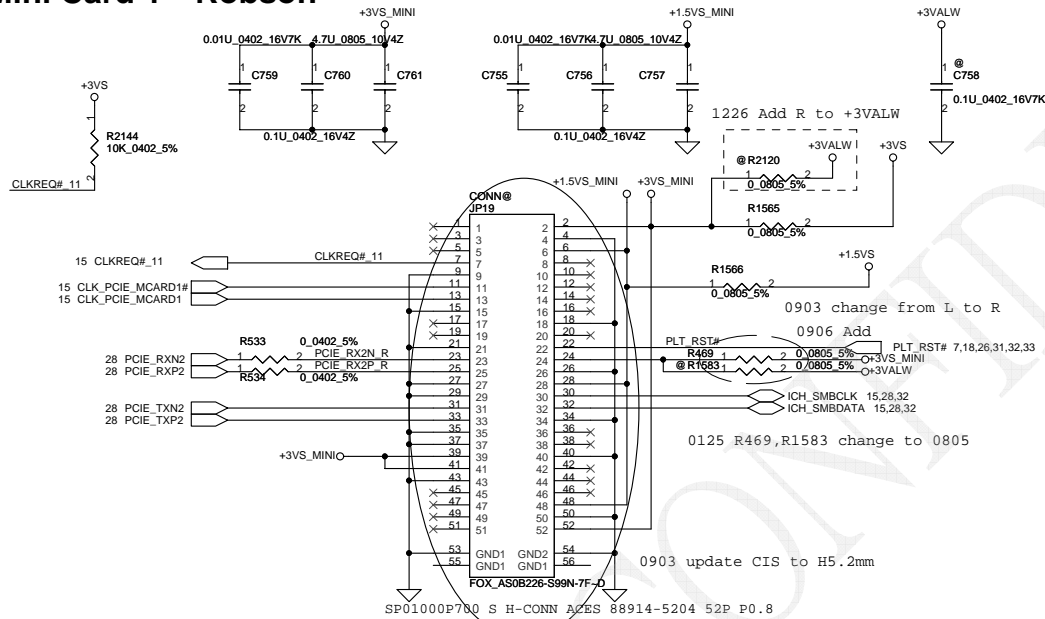
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MDC 1.5 Conn.

Change type 4/25

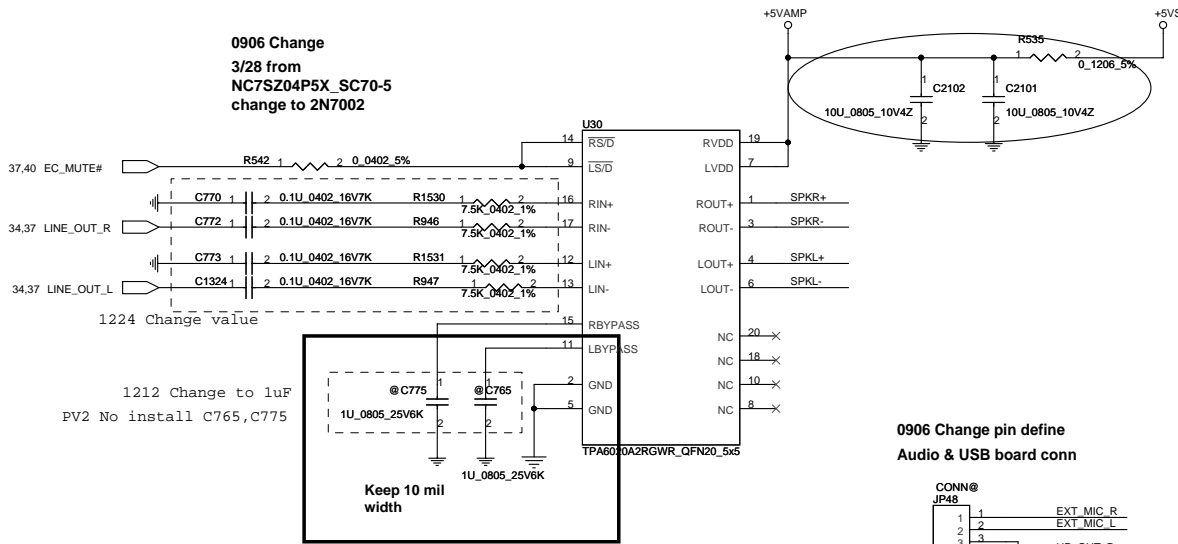


Mini Card 1---Robson

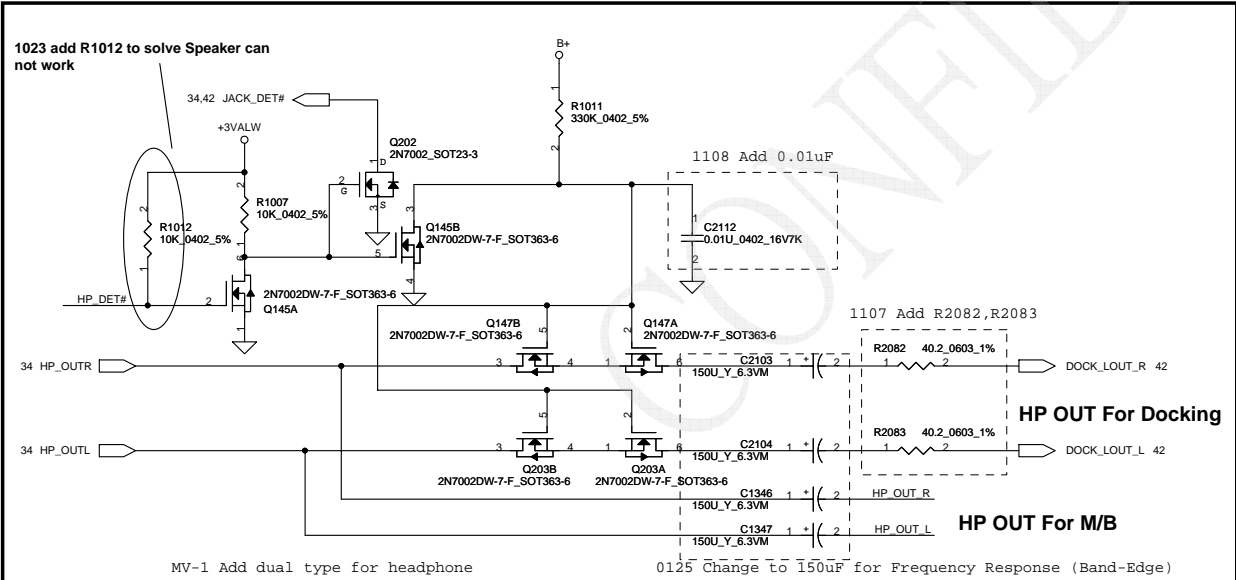
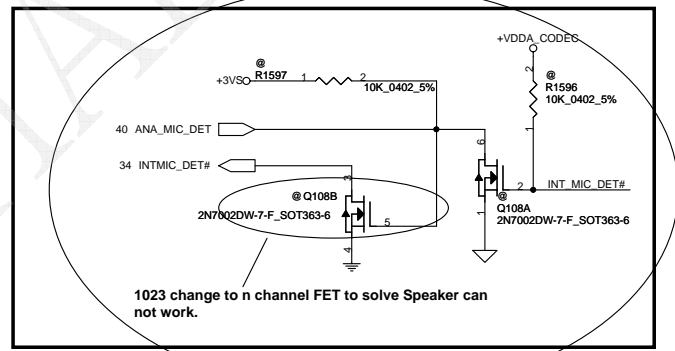
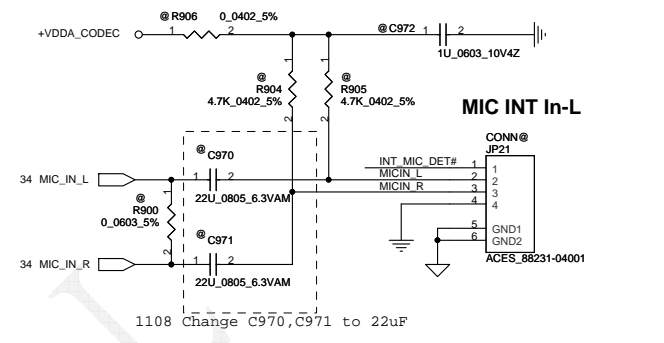
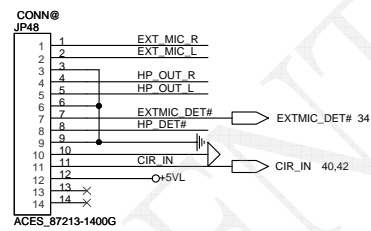


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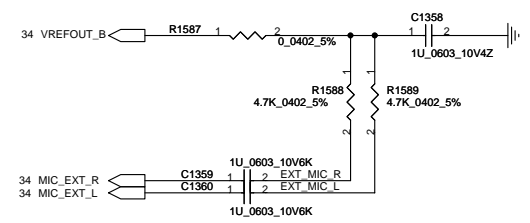
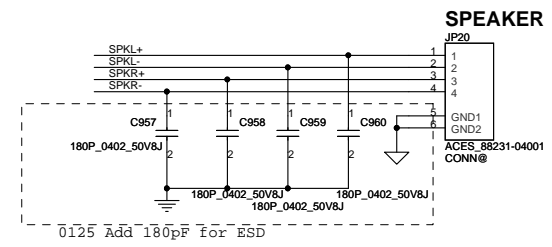
0906 Change
3/28 from
NC7SZ04P5X_SC70-5
change to 2N7002



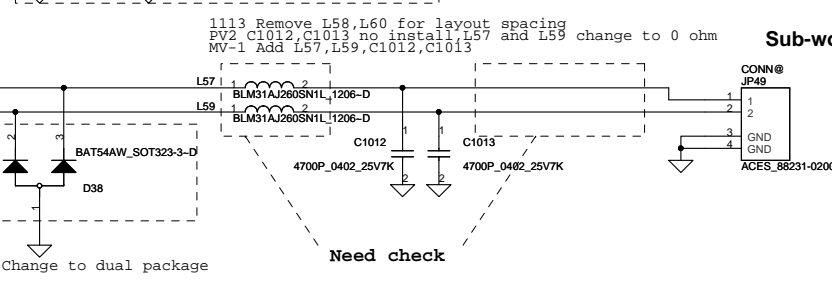
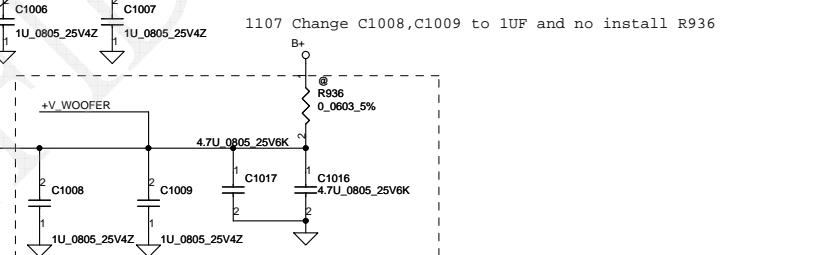
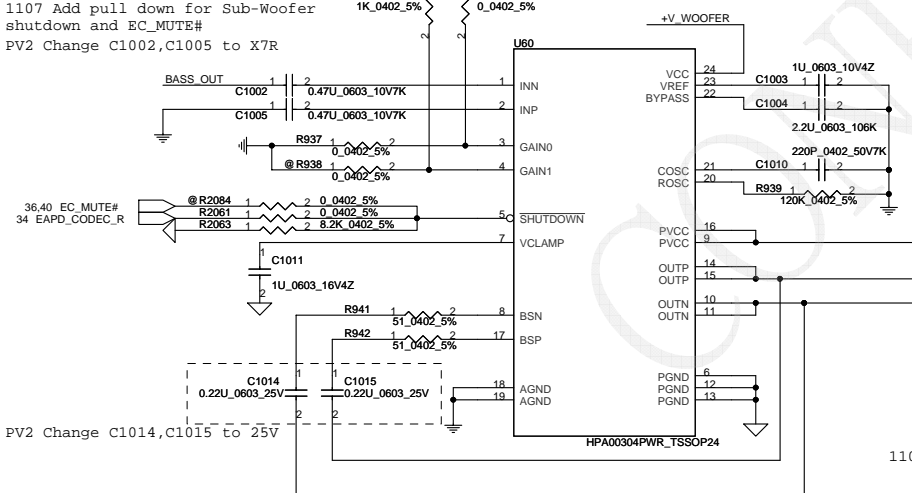
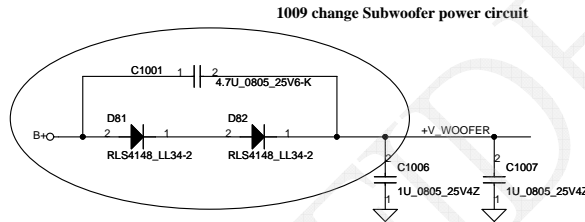
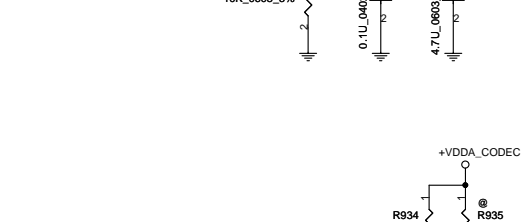
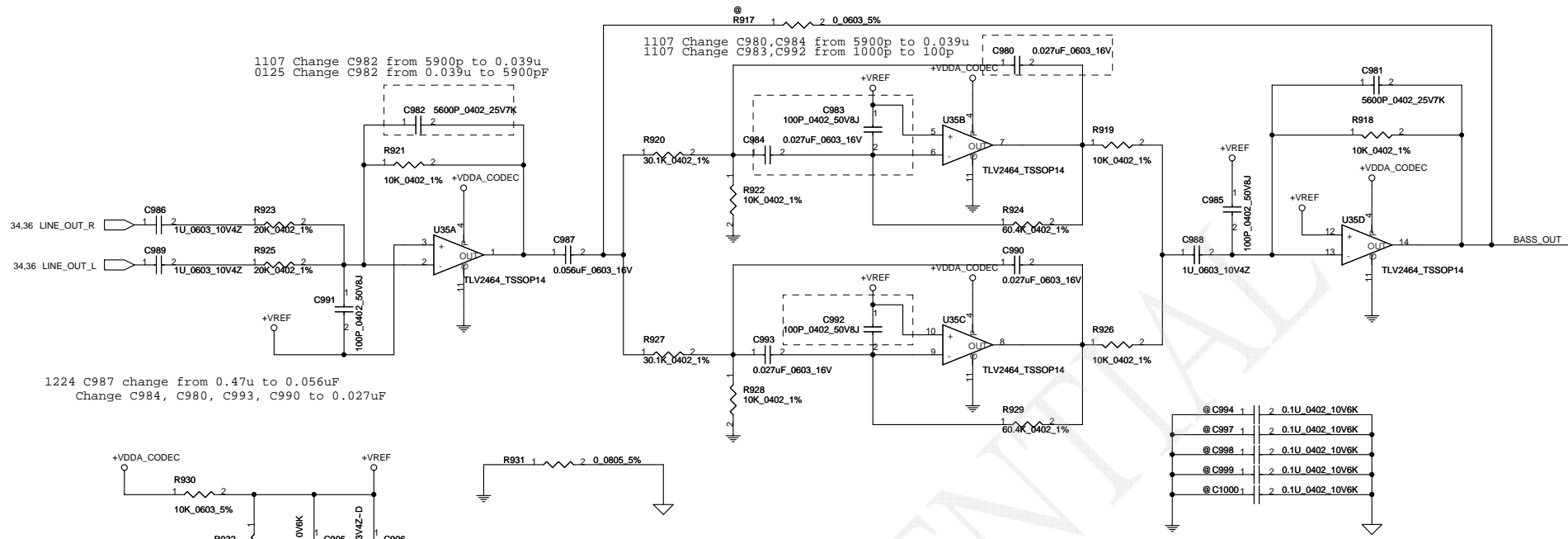
0906 Change pin define
Audio & USB board conn



SP02000D000 S W-CONN ACES 85204-04001 4P P1.25

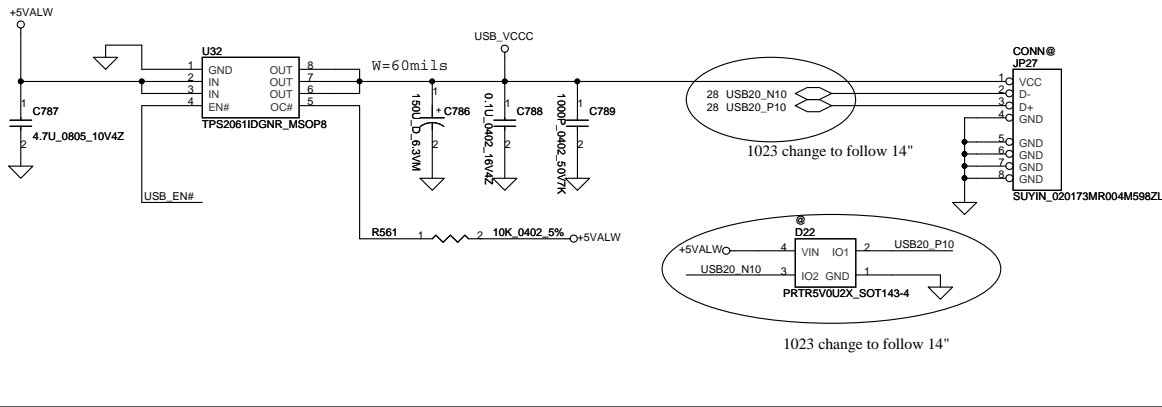


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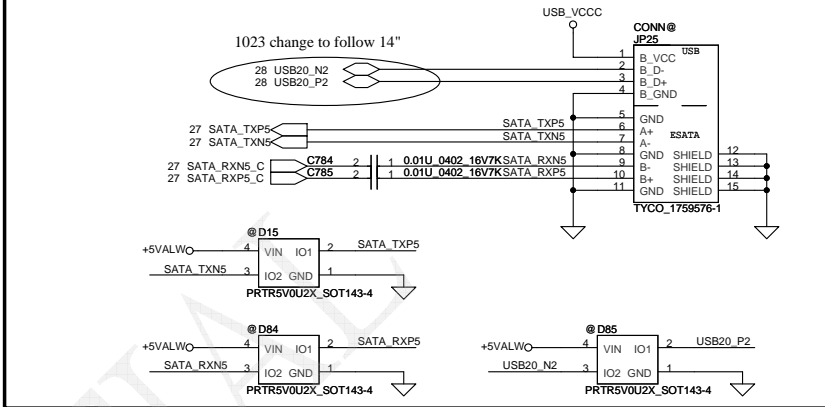


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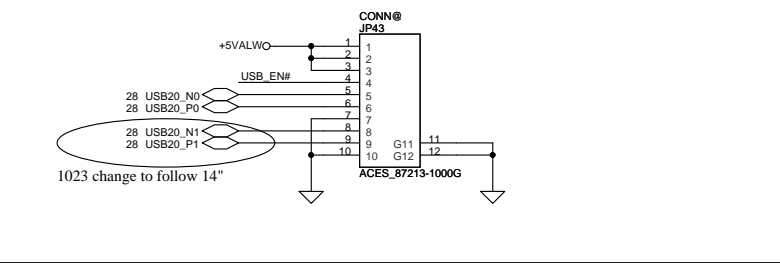
Left side USB Connector



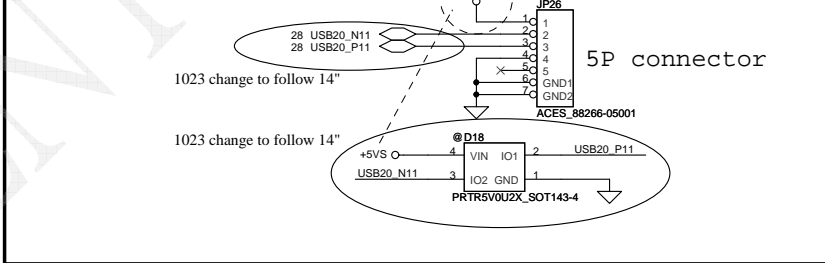
Left side ESATA/USB combination Connector



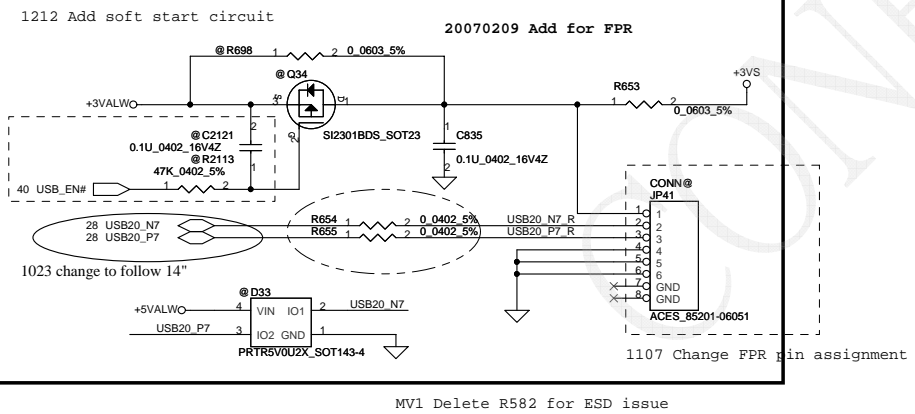
USB cable connector for Right side



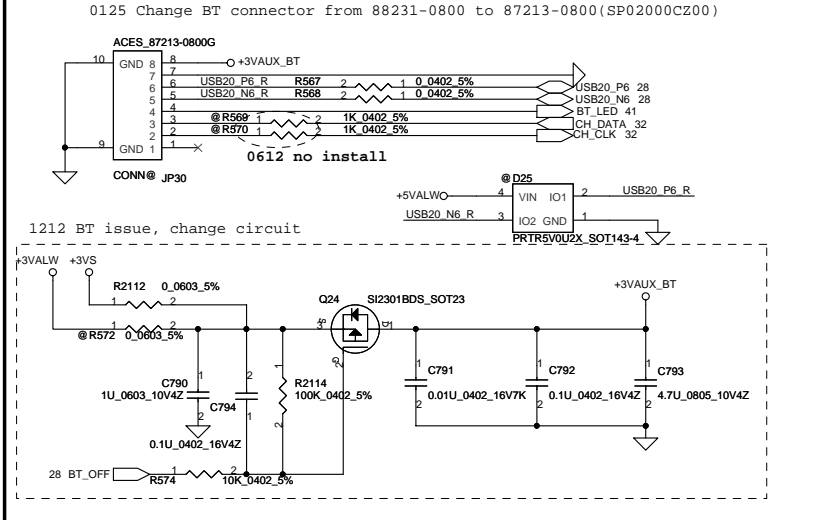
Touch screen connector



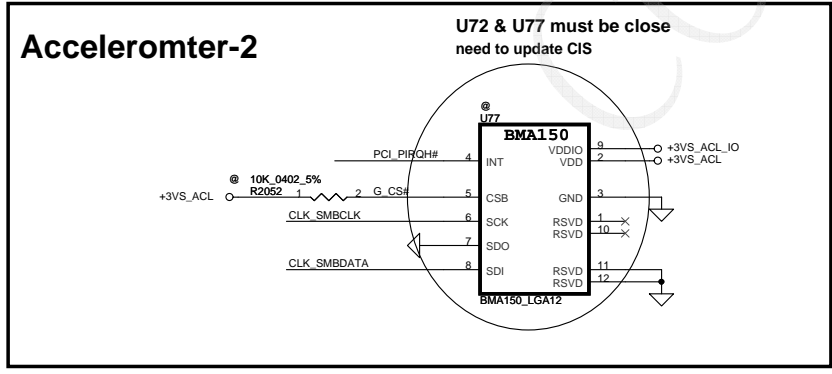
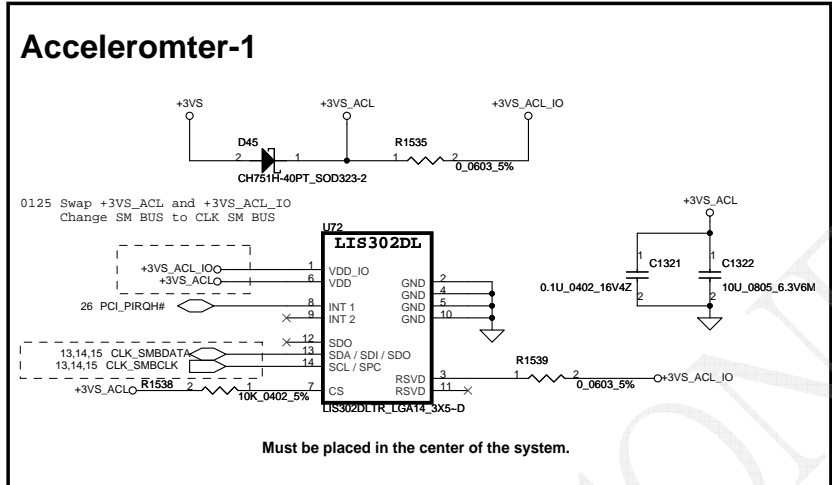
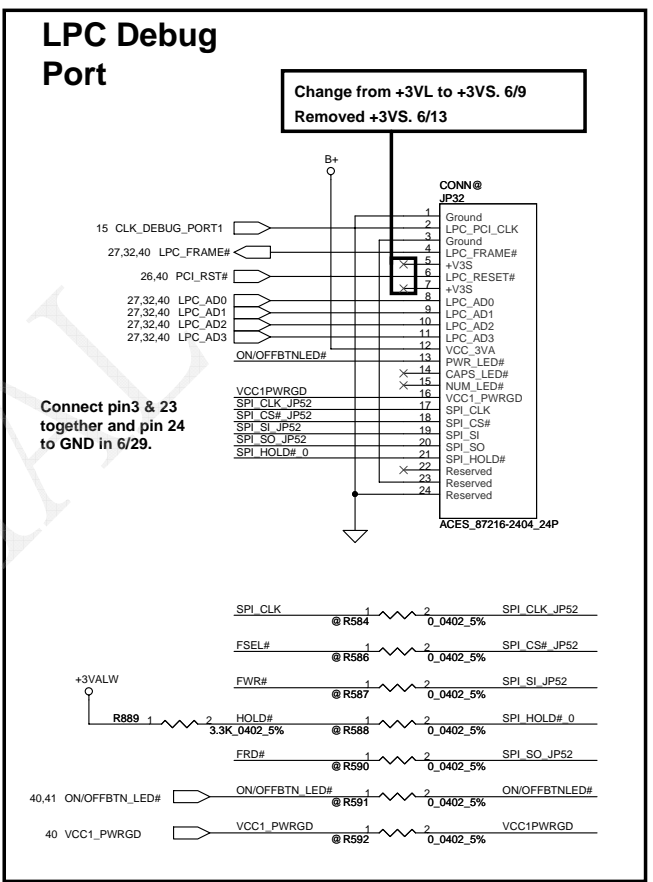
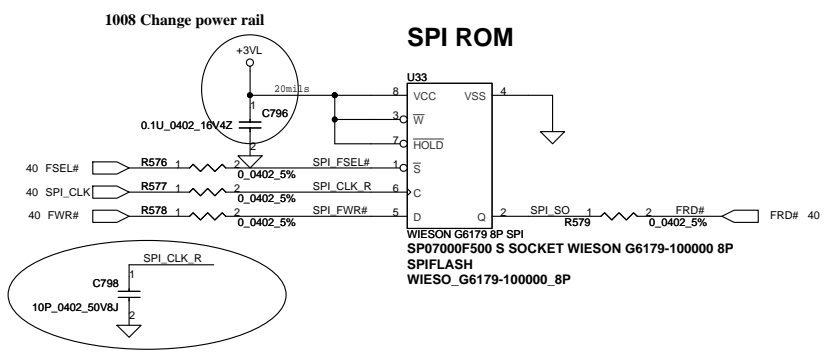
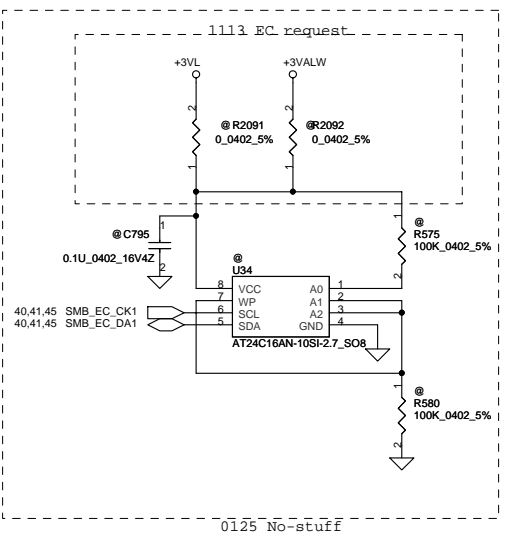
Finger printer



BT Connector

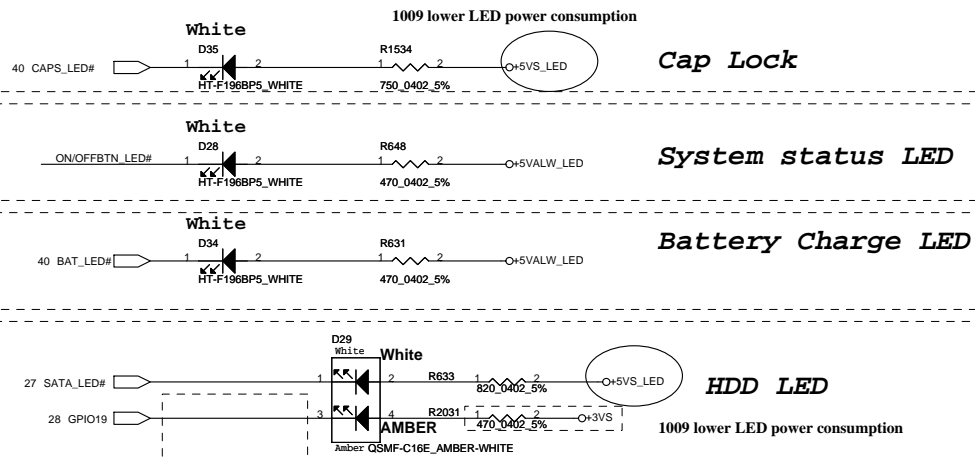


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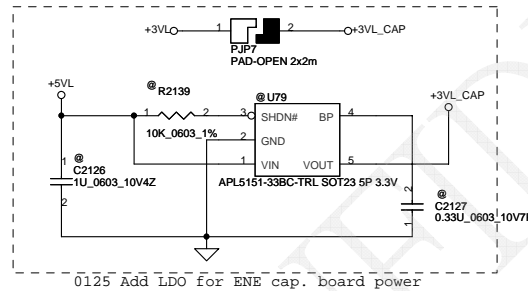
LED



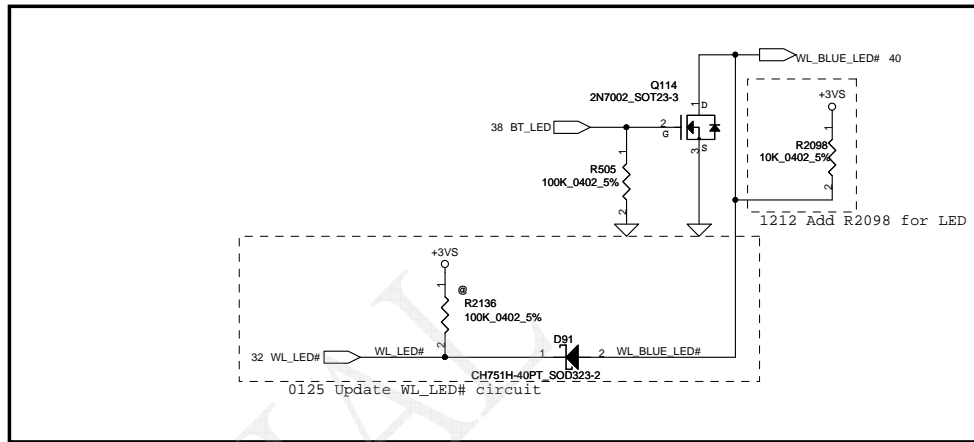
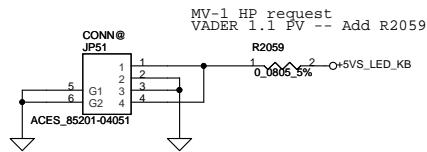
1025 change to follow BT00 design
 1102 Change GSENSOR LED control pin from SB to KBC
 1106 Delete R668, control by SB

for debug only

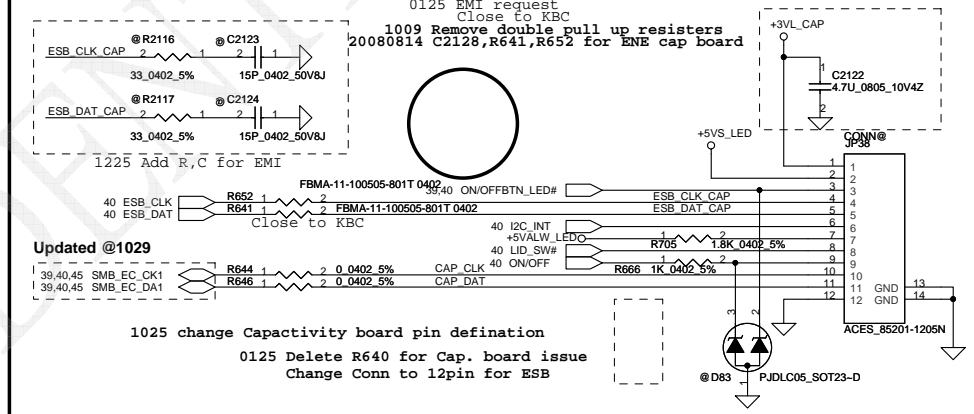
1212 Delete SW5, SW6



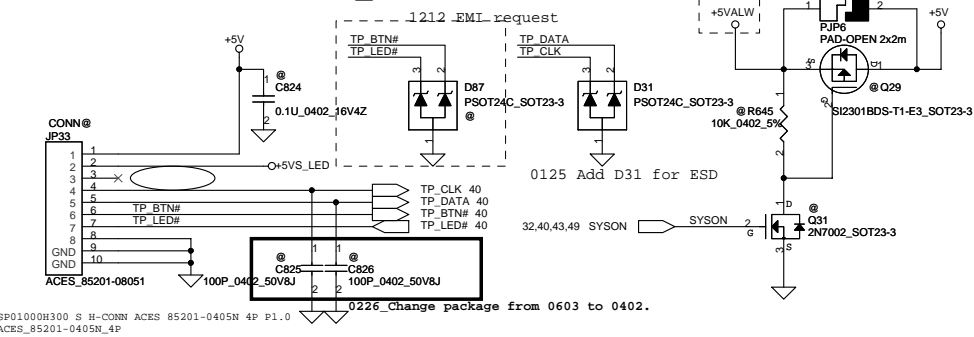
K/B backlight



SWITCH BOARD.

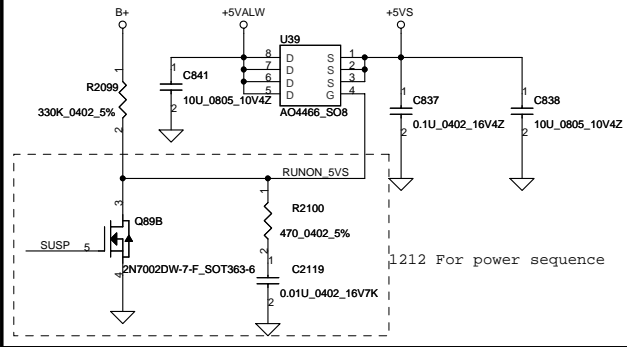


T/P Board (Include T/P_ON/OFF)

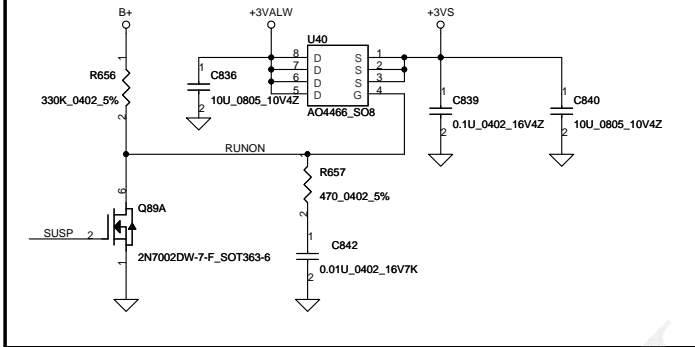


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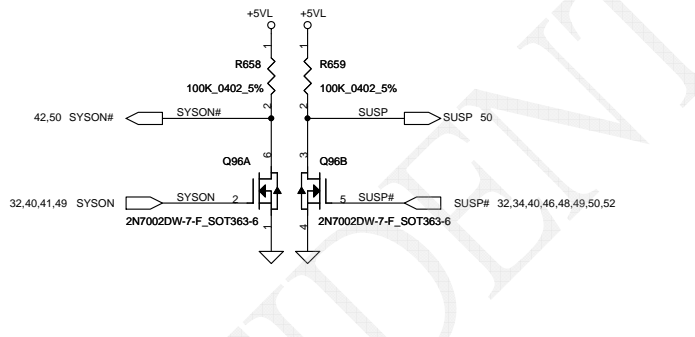
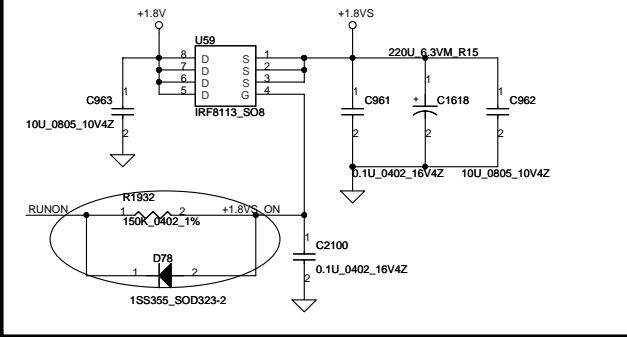
+5VALW to +5VS Transfer



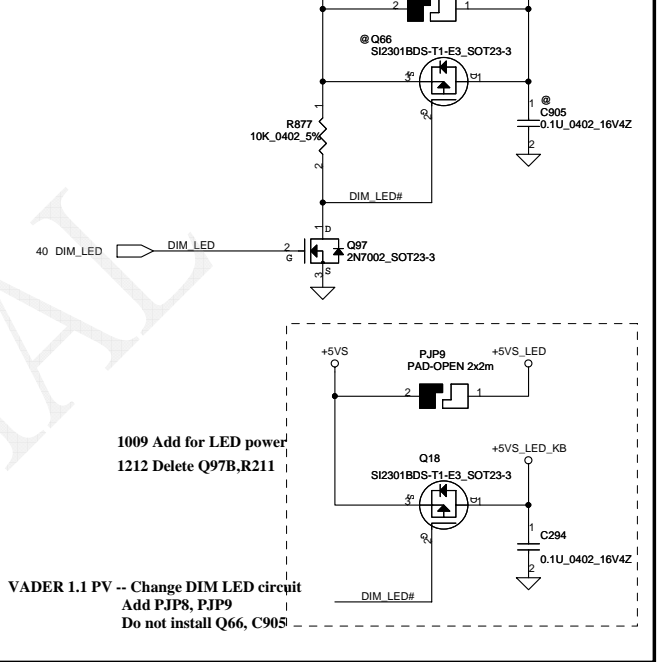
+3VALW to +3VS Transfer



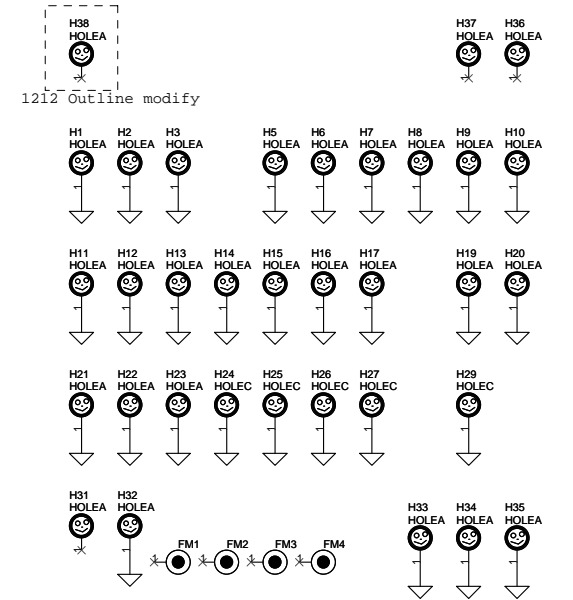
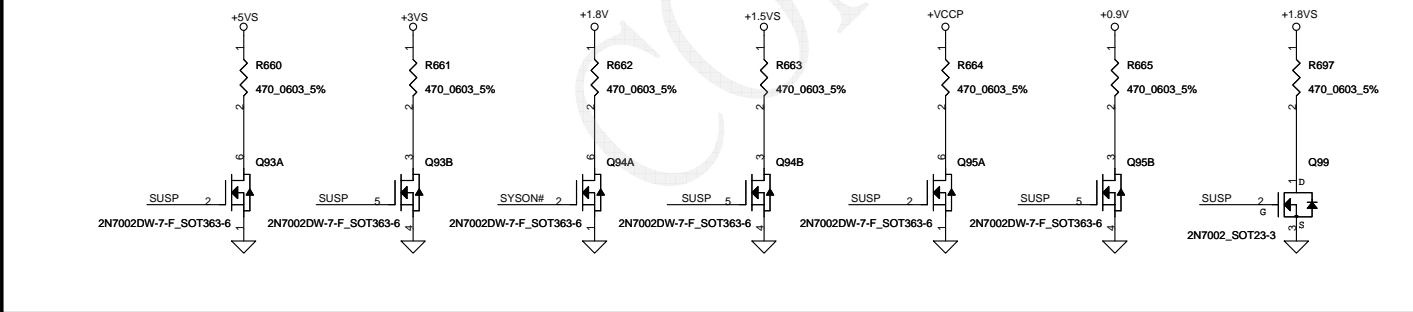
+1.8V to +1.8VS Transfer



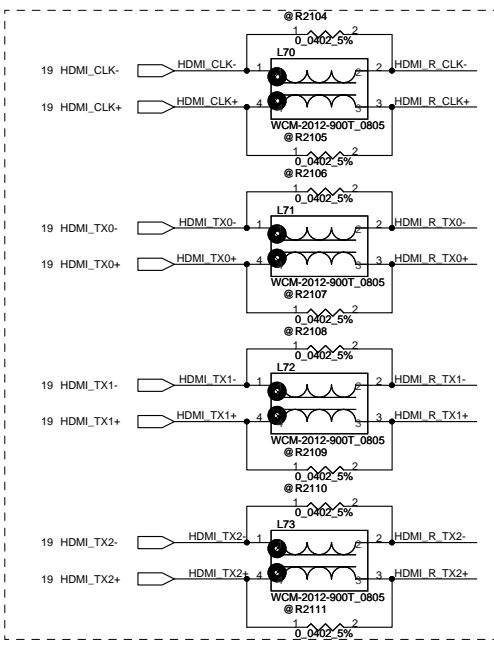
DIMM LED



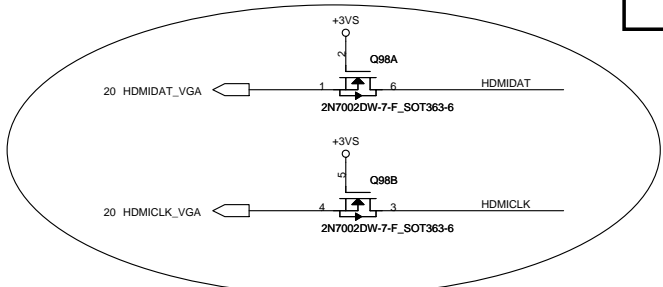
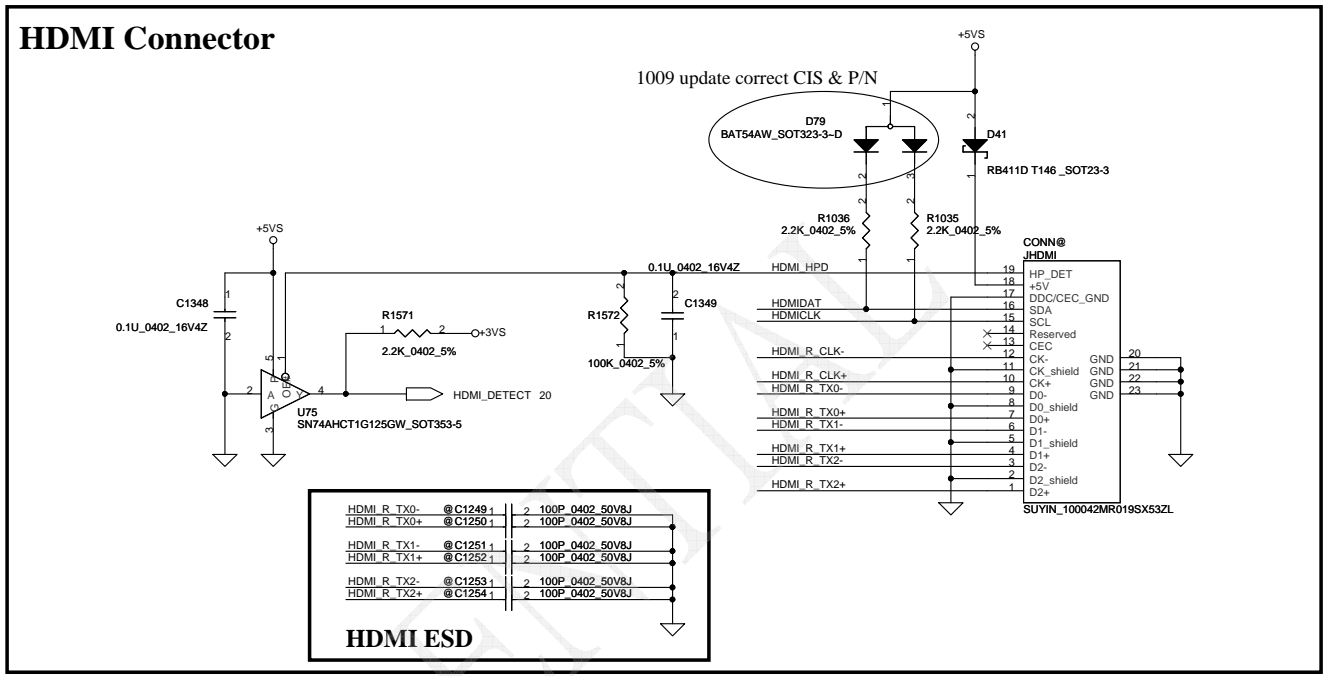
Discharge circuit



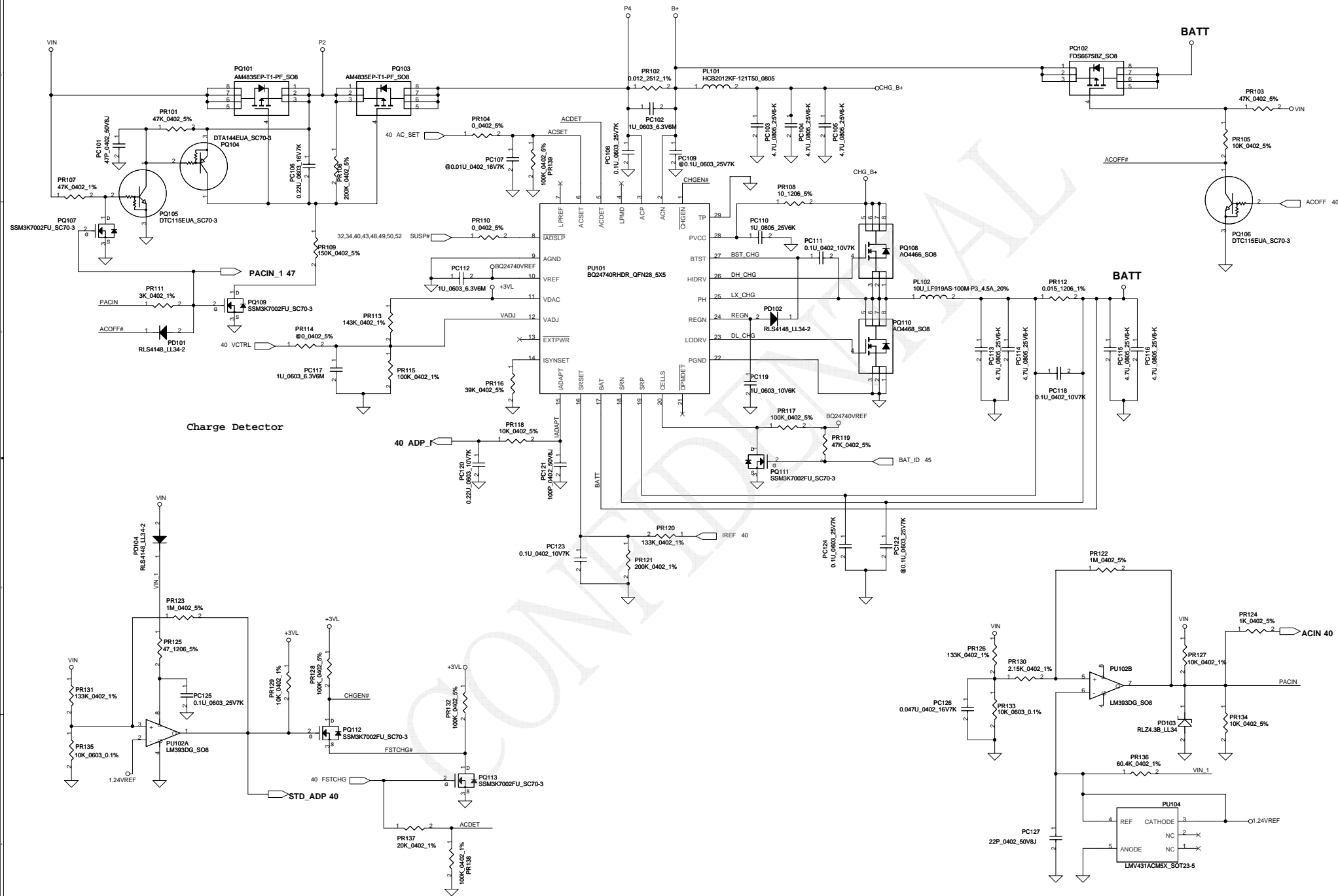
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1212 Add 0 ohm

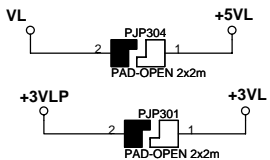
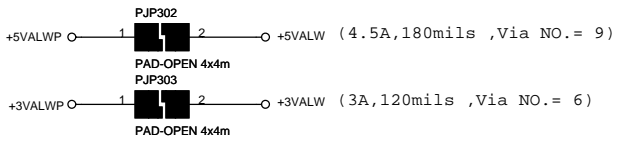
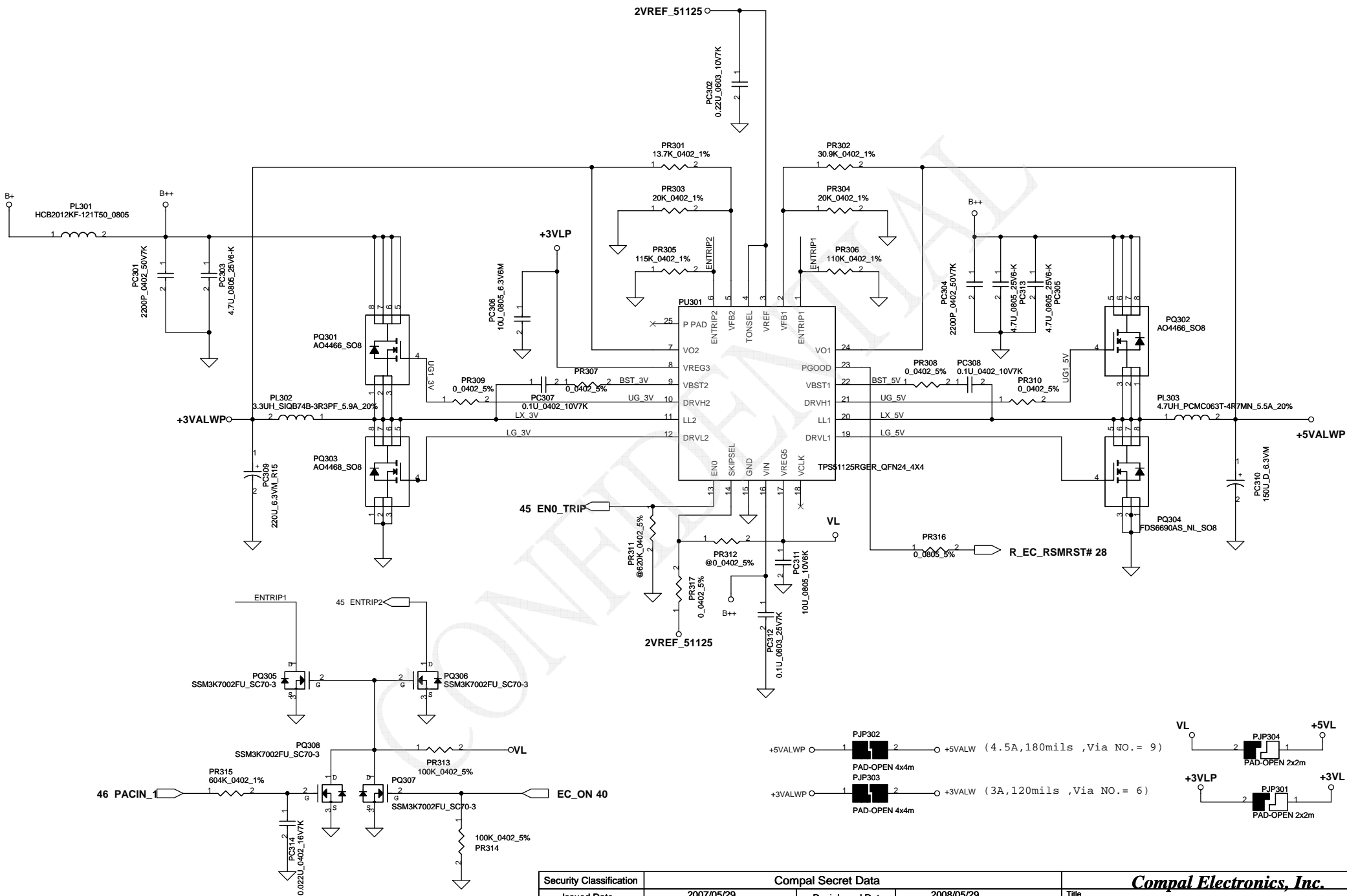


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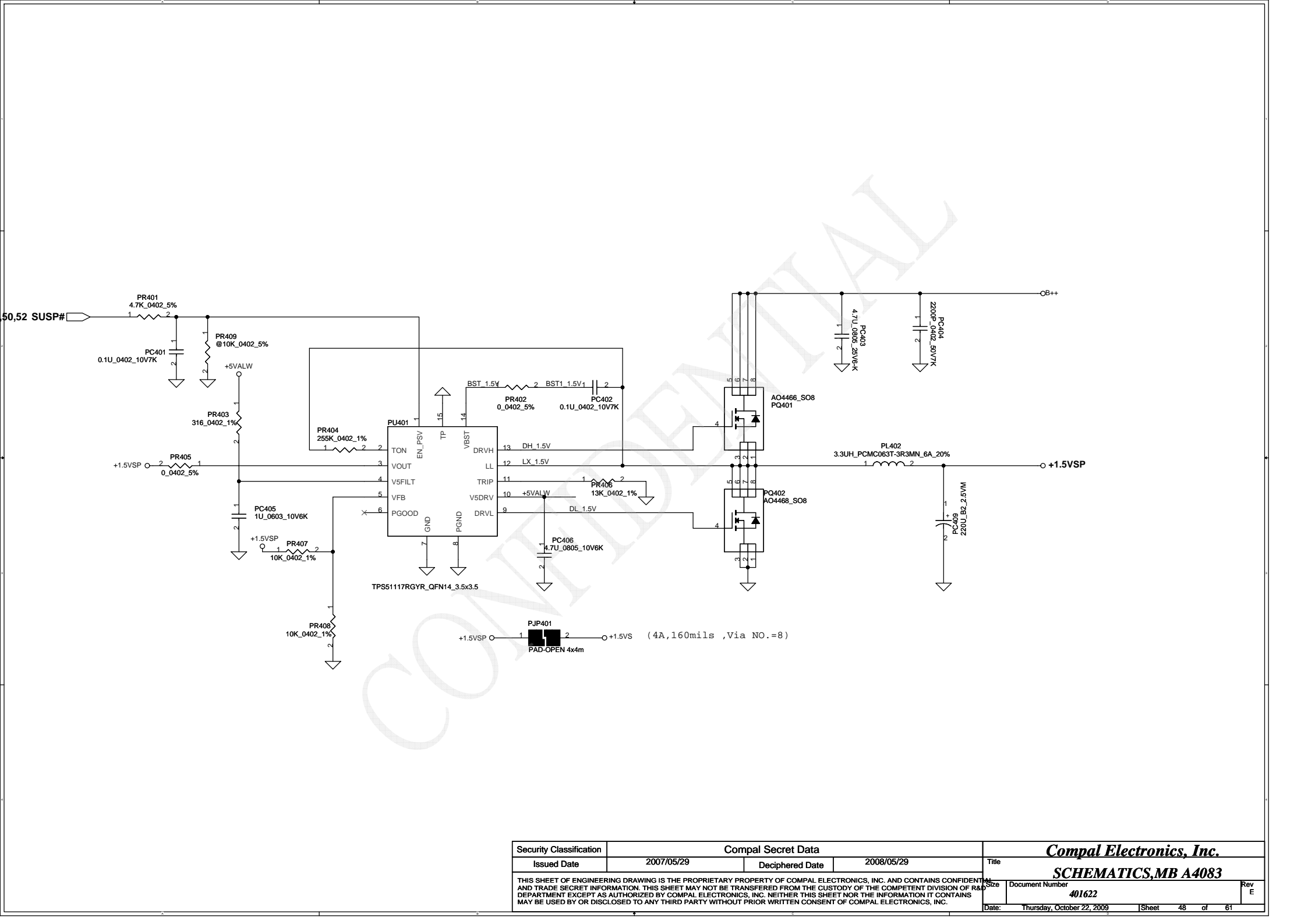


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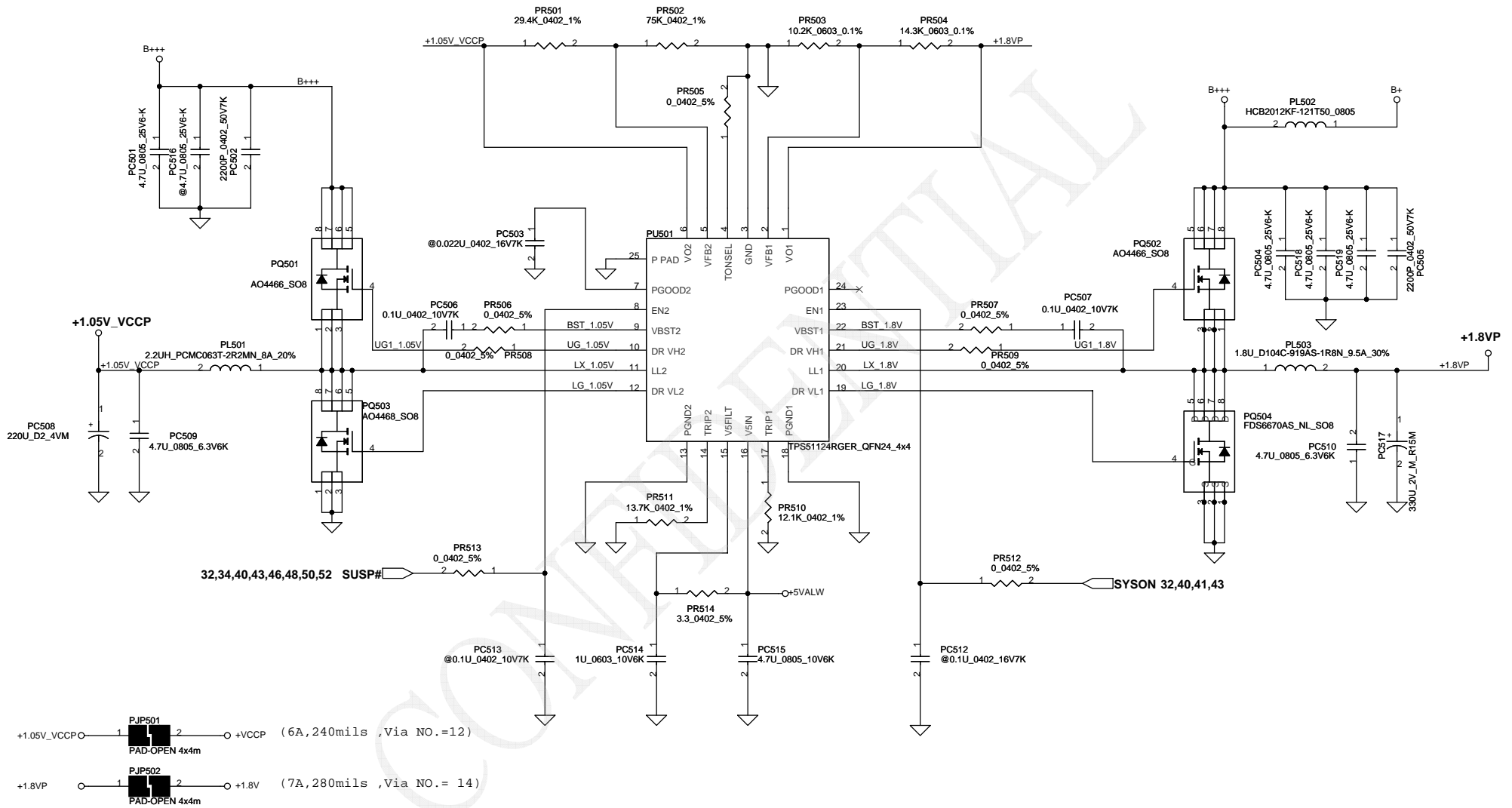
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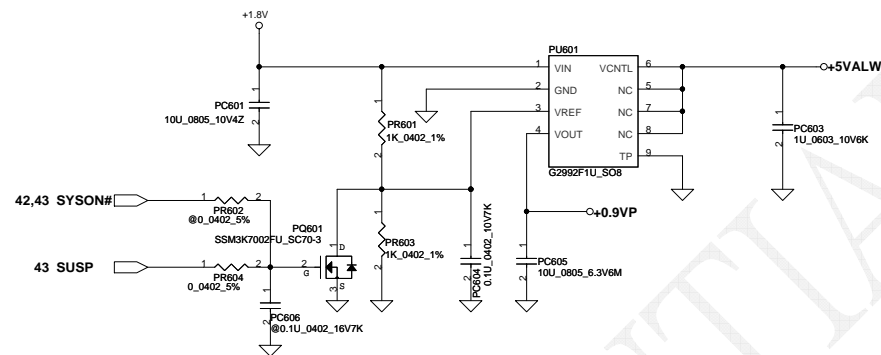
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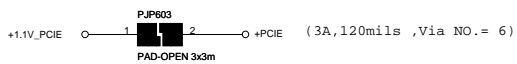
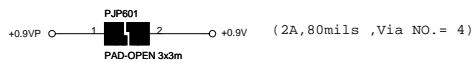


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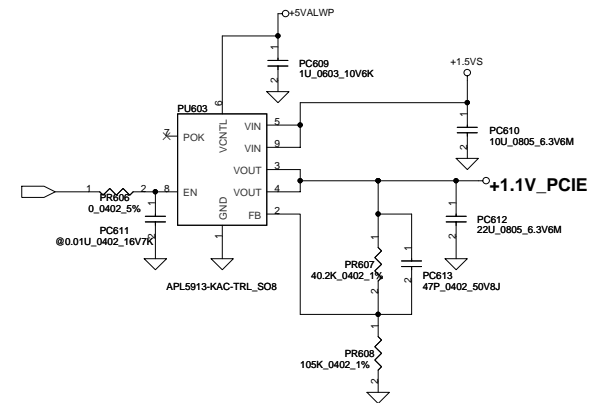


42,43 SYSON#

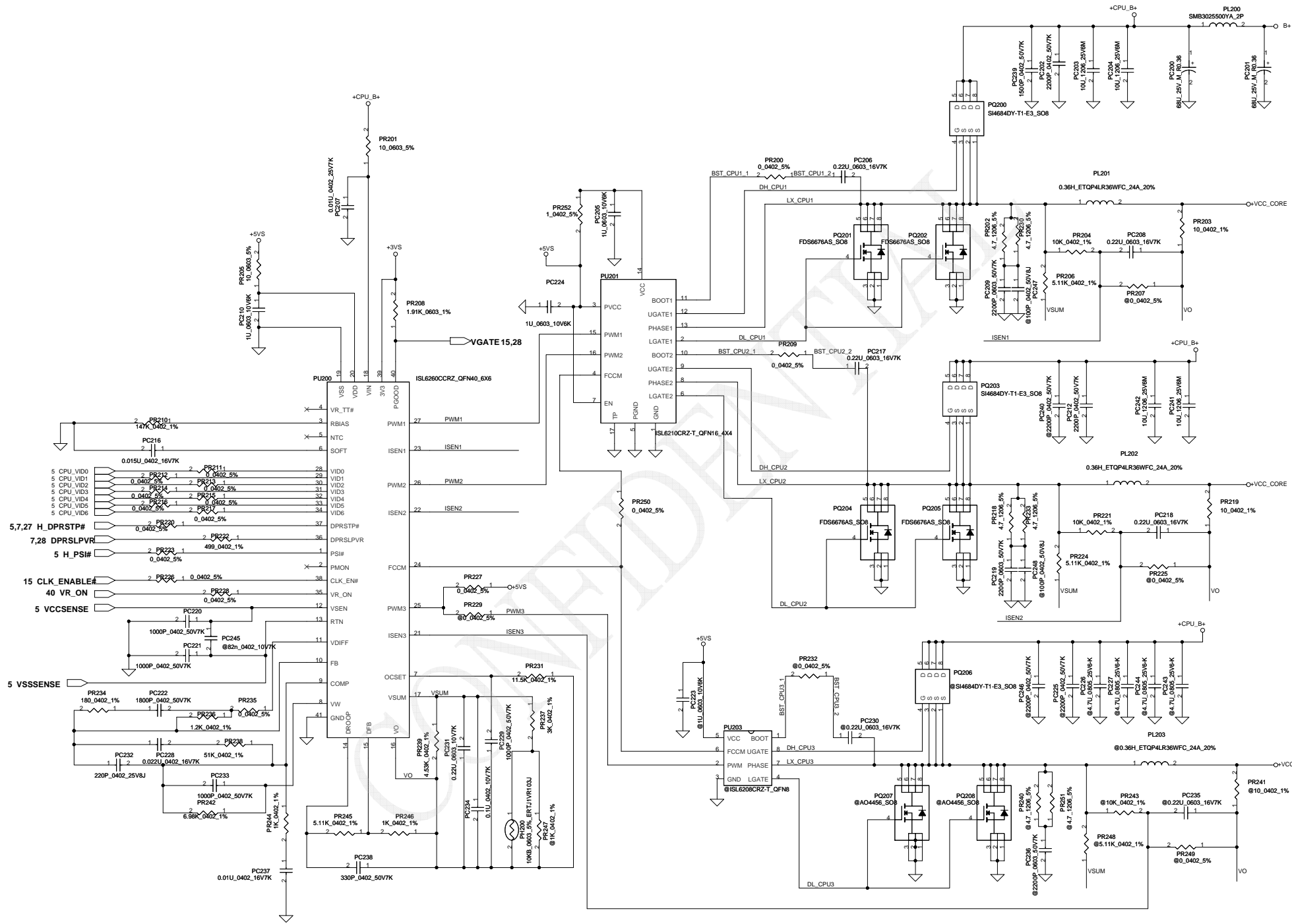
43 SUSP



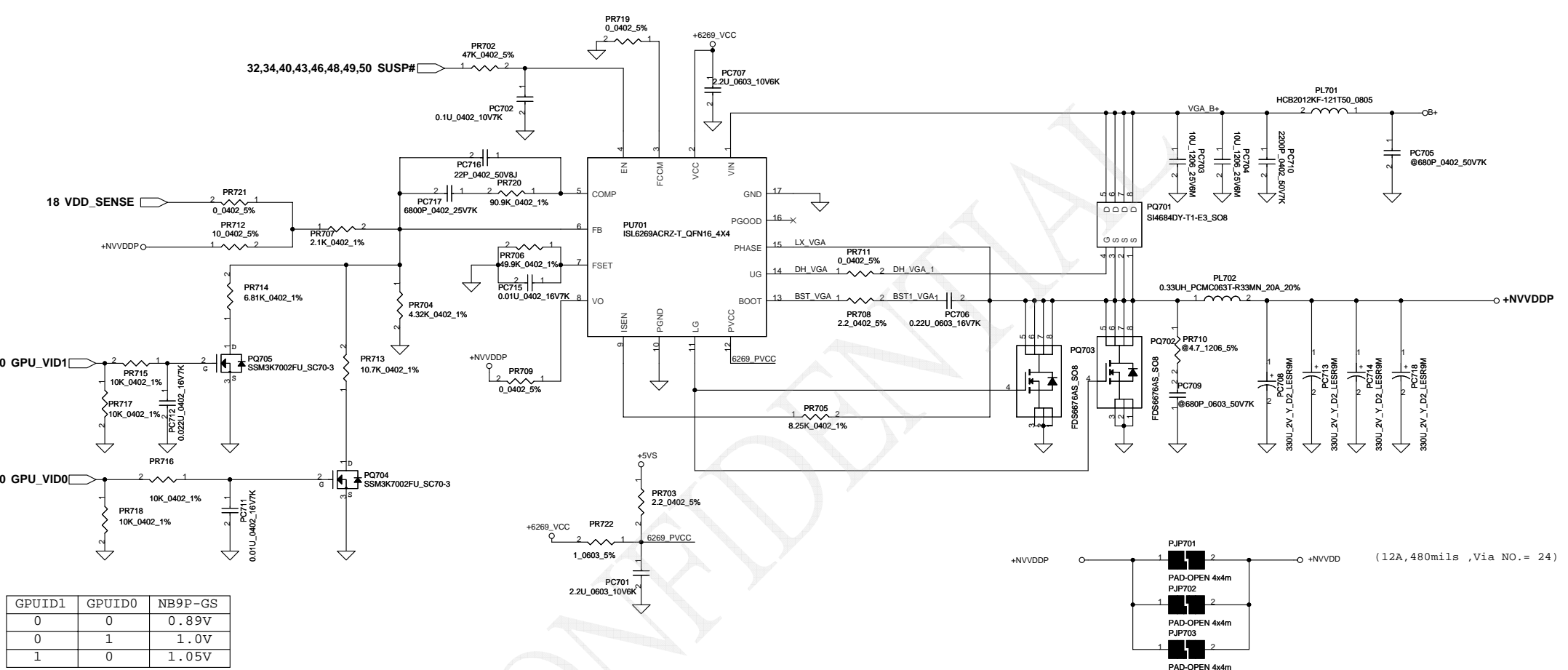
32,34,40,43,46,48,49,52 SUSP#



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GPUID1	GPUID0	NB9P-GS
0	0	0.89V
0	1	1.0V
1	0	1.05V

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as luf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.	
<2007.10.08>	1	Fix Audio disappear	follow Intel SB design suggestion to separate HDA Bus	27	Add R439, R440, R442, R444	0.2
	2		Add to determine board type and project	28	Add R777, R776, R774, R775	0.2
			Meet EC request	28	non-stuff R419, R695	
	3	Fix Audio disappear	follow Intel SB design suggestion	29	Change power rail from +1.5v to +3v	0.2
	4		meet SW debug request	32	Add Debug CLK and PLT_RST#	0.2
	5	Fix Audio disappear	follow Intel HDA bus design for Discrete platform	34	Change codec power rail from +1.5v to +3v	0.2
	6	Fix can not power on issue	Meet EC and SPI access sequence	39	change SPI power rail from+3v to +3VL	0.2
<2007.10.09>	7		Follow Intel design guide	7	Change R30 value	0.2
	1	Fix HDMI can not detect	follow Nvidia design request	18	change HDMI I2C channel to I2C B channel	0.2
	2		Meet HP request to remove TV	18	Remove TV all components at VGA side	0.2
	3		update ODD footprint	30	update JODD footprint	0.2
	4	Fix ODD wrong pins	lower system power consumption	33	change Card Reader LED power rail	0.2
	5		Meet Sub-woofer pwoer request	37	change D81, D82	0.2
	6	Solve EC always damage	Solve EC always damage	40	change D53 direction	0.2
	7		Double pull up and pwoer rail is different	41	Remove pull up resistors	0.2
	8		lower system power consumption	41	change Cap-lock, HDD LED power rail	0.2
	9		Meet HP request to remove TV	42	Remove TV all components at Dock side	0.2
	10		lower system power consumption and meet LED status	43	Add +5VS_LED (Inculde DIM function)	0.2
<2007.10.19>	11		solve HDMI pull up	44	update D79 footprint	0.2
	1		Meet ME limit area at KBC	27	Change Y4 material	0.2
	2		Follow IDT suggestion	35	change R886 to 1206	0.2
<2007.10.20>	3		Follow Nvidia suggestion	25	Change R193, R196 size to 0603	0.2
	1		follow correct power rail	38	change Touch screen power rail	0.2
	2		Meet HP request	39	Change ST G-sensor P/N & package	0.2
<2007.10.22>	3		Meet HP request for WLAN &TV slot swap	32	Swapped WLAN and TV all support components	0.2
	1		Change LAN chip to meet Energy star spec	31	change LAN brand to Realtek	0.2
	2					

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.	
<2007.10.23>	1	Fix USB loading of SB	follow 14" Blade USB channel design	28	Chnage all USB channel	0.2
				17	Change USB channel of Camera	
				32	Change USB channel of WLAN & TV Tuner & New card	
				38	Change USB channel of Left side, Right side, E-SATA	
				38	Change USB channel of Touch screen, Finger print	
			42	Change USB channel of Dock		
	2		Follow JMicro CardReader Vendor Suggestion	33	Change R114 & R1546 value	0.2
	3		Solve Speak no sound issue	36	add pullup at HP_DET#	0.2
				36	Change Q203 to N-channel FET	
				34	Change R524 pin2 connect to JACK_DET#	
<2007.10.25>	1		Meet HP request for QC and DC co-lay	4	add GTLREF and XDP circuits	0.2
				5		
				6		
	2		Meet Intel request for CLK request	15	Add R127 to meet Intel CLK design	0.2
3		Solve G-sensor LED control	28, 41	change G-sensor LED control to GPIO19 of SB	0.2	
4		Follow Capactivity board design	41	change Pin7 & 7 NET	0.2	
<2007.10.31>	1			34	Use Audio Codec GPIO5 to shutdown Sub-woofer	
	2			40	Connect HDA_RST#_CODEC to EC	
	3			34	Separate SPDIF out to VGA and Docking	
<2007.11.02>	1		Common design	16	R204,R205 no stuff	0.3
	2		Change +5VS_LOGO resistor size to 0805	17	R642 size to 0805	0.3
	3		Double pull up	20	R2046,R2047 no stuff	0.3
	4		For card reader power	33	install R1553	0.3
	5		For KBC C0 version	40	R616 no stuff	0.3
	6		Add pull down resistor for SUSP# and SYSON	40	Change R615 to 8.2k and add R2062	0.3
	7		Change HAD_RST#_CODEC from KBC pin 36 to pin 38	40		0.3
	8		Change GSENSOR LED control pin from SB to KBC	41	Install R668, no install R667	0.3
	9		Add pull down for sub-woofer power-down	37	Add R2063	0.3

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.11.04>		Move resistor from LS4086P to MB	41	Add R2064	0.3
		Change to dual type for layout space	16	Change Q69,Q70 to dual type	0.3
		Only use LIS302DLTR	39	U77, R2025 no install	0.3
		Change CIR_IN power rail	40	Connect R642.1 to +5VL	0.3
<2007.11.05>		nVIDIA suggestion for NB9M-GS/GE	22	R1005 change to 475 ohm	0.3
		nVIDIA suggestion -- add Pull up 2.2K on HDMIDAT_VGA and HDMICLK_VGA to +3VS. at VGA side	18	Add R2065,R2066	0.3
<2007.11.06>	EMI request	CRT add resistor for EMI	16	Add R2069,R2070,R2071	0.3
		HP suggestion	34	Change C746,C747,C748,C749 to 1000PF	0.3
		USB camere power and add GPO pin for shutdown	17	Add PJP5,R2072,R2073	0.3
		LAN DSM support	31	1. USB camera -- SB GPIO20 2. ISOLATE - SB GPIO18 3. LAN OGPIO - SB GPIO14	0.3
		EC_BEEP	34	Add R2076	0.3
		G-sensor LED control by SB	41	Delete R668	0.3
<2007.11.07>		Modify FPR connector pin assignment	38	Modify JP41 pin assignment	0.3
		Modify Audio	34 36 37 42	1. Add C2108,C2109,R2080,R2081 2. Add R2082,R2083 3. Change C1008,C1009 to 1uF 4. Delete C976,C977 5. Delete R515,R516,C916 6. Change C982,C980,C984 from 5900p to 0.039u 7. Change C983,C992 from 1000p to 100p 8. Add EC_MUTE# to sub-woofer shutdown pin and R2084	0.3
		nVIDIA suggestion	20	1. Delete strap pin 2. Change R1020, R1015, R1010 to 475 ohm 3. Swap THERMDN and THERMDP	0.3
<2007.11.08>		EMI request	17	Add C2100,C2111	0.3
		Audio	36 37	Change C970,C971 to 22uF, add C2112, change D38 to dual type	0.3
<2007.11.09>		nVIDIA suggestion	19 20	Change HDMI DDC to I2CD R387,R388,R415,R422,R427 -- install Change R415 to 10 ohm and no install Delete R99, Change +IFPC_PLLVDD to +PCIE	0.3
		JMicron suggestion	33	Do not install R2030 Add D86 for card reader wake up Add SB GPIO22 for wake up event	0.3
<2007.11.12>		HP request	4	Add EMC1403 for Qaud core	0.3

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<2007.12.12>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		MV DG for VDDC_QDAC	10	Chagne VCCD_QDAC to +1.5VS	0.4
2		WLAN issue	32	Change XMIT_OFF#,WL_LED# and component to WLAN connector	0.4
3		PCIE issue	28	Swap GLAN and NewCard PCIE port	0.4
4		Modify CardReader LED	33	Use 2N7002 to control LED	0.4
5		KBC	40	Change SMB_EC_DA1,SMB_EC_CK1 power rail from +5VL to +3VL Add C2118 for KBC pin124 Chagne EC_THERM power rail to +3VS	0.4
6		WL_BLUE_LED# issue	41	Add R2089 pull up for WL_BLUE_LED#	0.4
7		Power sequence	43	Add R2099,R2100,C2119 and Q89 change to dual type	0.4
8		DIM_LED	43	Delete Q97B,R211	0.4
9		EC_PME#	40	Change EC_PME# power rail to +3VALW	0.4
10		WLAN issue	28	Add R2101	0.4
11		Change TP power rail	41	Change TP power rail to +5VALW	0.4
12		G-sensor	41	G-sensor -- R2031 change to 470 ohm and pull up to +3VS	0.4
13		For Dock present	42	R1570 change to 22 ohm,R61 change to 2K ohm	0.4
14		Clock generator	15	Add series R2102,R2103 for 27M_SSC and 27M_CLK	0.4
15		HDCP ROM	19	R951 pull up,R959 no install	0.4
16		EMI request	17	C272,C273,C2120 -- 470pF C828,C798 -- 10pF C2111 -- 220pF Add D87	0.4
17		Modify BT/FPR circuit	38		0.4
<2007.12.24> 1		HP request	36 37	Change value	0.4
<2007.12.25> 1		For ENE cap board EMI issue	40	Add R and C	0.4
<2007.12.26> 1		For Mini PCI	32 35	Add R2118,R2119,R2120	0.4

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<2008.01.25>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		G-sensor power rail G-sensor SM BUS	39	Swap +3VS_ACL and +3VS_ACL_IO Change G-sensor SM BUS to CLK SM BUS -- +3VS power rail	0.5
2		KBC PIN97 -- AC in LED issue For DOCK_SLP_BTN# For Mute_LED	40	KBC pin 97 connect to power Change R543 to 33 ohm Add R2121 33 ohm	0.5
3		Cap. board INT issue	41	Delete R640 for Cap. board issue	0.5
4		Current issue	32 32 35	Change R464 and R1582 to 0805 R466,R468 change to 0805 R469,R1583 change to 0805	0.5
5		KBC EEPROM issue	39	Do not install KBC EE prom	0.5
6		Frequency Response (Band-Edge)	36	Change C2103,C2104,C1346,C1347 to 150uF	0.5
7		D3E function	33	Do not install R2087 for Intel platform	0.5
8		Change BT connector(JP30)	38	Change BT connector from 88231-0800 to 87213-0800(SPO2000CZ00)	0.5
9		Audio circuit	37	Change C982 from 0.039u to 5900pF	0.5
10		BKOFF# issue	39	Add R2122 on BKOFF# and no-stuff	0.5
11		TP LED	41	Add PJP6 and no-install Q29,Q31,R645	0.5
12		RTC timing	27	Change C548,C549 to 18PF	0.5
13		Change LED control signal	33	Add R2123 and R2124 No-install R1548,C53,R2097	0.5
14		Quad Core CPU	4,6	R2125,R2126,R2127,C2125,R2128-R2134	0.5
15		ESD	36 41 38	Add D31 for TP --- OK Change D33 to PRTR5V0U2X_SOT143-4 and install -- Check P/N Add C957,C958,C959,C960 -- 180pF	0.5
16		PM_PWROK timing	28	Add D90 and R2135 for PM_PWROK timing	0.5
17		ENE cap. board	41	Change JP38 to 12pin Change R641,R652 to 800 ohm bead	0.5
18		Reduce 0 ohm		Delete R622, R404, R407, R429, R438, R667, R970	0.5
19		change WLAN LED circuit	41	Need to change R2098 value, Add D91, R2136	0.5
20		ESB LDO CIRCUIT	41	Add U79,R2139,C2126,C2127,PJP7 for ENE cap. board power	0.5
1		nVIDIA suggestion	19	Change R951 and R953 to 2.2K ohm	0.6

<2008.03.16>

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Docking headphone issue	36	Change Q147 to dual tpye and add Q203	1.0
2		For 2nd source thermal sensor	4	Add resistor R2140on pin6	1.0
3		EMI request	16	Add 4.7pF for C317,C318,C319	1.0
4		LED brightness	41	R705 : from 150ohm to 1.8K ohm R1534 : from 470ohm to 750ohm D29 : from SC500005400 to SC500006R00	1.0
5		HP request	41	Remove R2059 for KB backlight	1.0
6		Clock generator -- CLKREQ#		Add R2141-R2145 for CLKREQ#	1.0
7		ESD issue	38	Delete R582	1.0
8		Cap board auto trigger issue	40	R618.1 connect to +3VL	1.0
9		Intel Check list	9	No-stuff R59,R67,R65,R77,R66	1.0
10		Remove C2129 for ENE cap. board	40	Remove C2129	1.0

<2008.06.13>

1		HP request -- change VRAM to 64Mx16	21	Add CMDA27 and CMDB27	0.1
2		For VGA thermal issue	20	Add pull up resistor(R2146,R2147 no stuff) on GPU_VID0,1	0.1
3		backlight control circuit	41	Add R2059 for keyboard backlight	0.1
4		SB GPIO39 for VGA 65nm and 55nm	28	Add pull down resistor R2148 NB9P-GS 65nm --> H NB9P-GS 55nm --> L NB9P-GE --> H	0.1
5		Remove dim LED function	41	1. Do not install Q66,C905 and add jumper PJP8 for +5VALW_LED 2. Add jumper PJP9 for +5VS_LED 3. +5VS_LED_KB for keyboard backlight	0.1

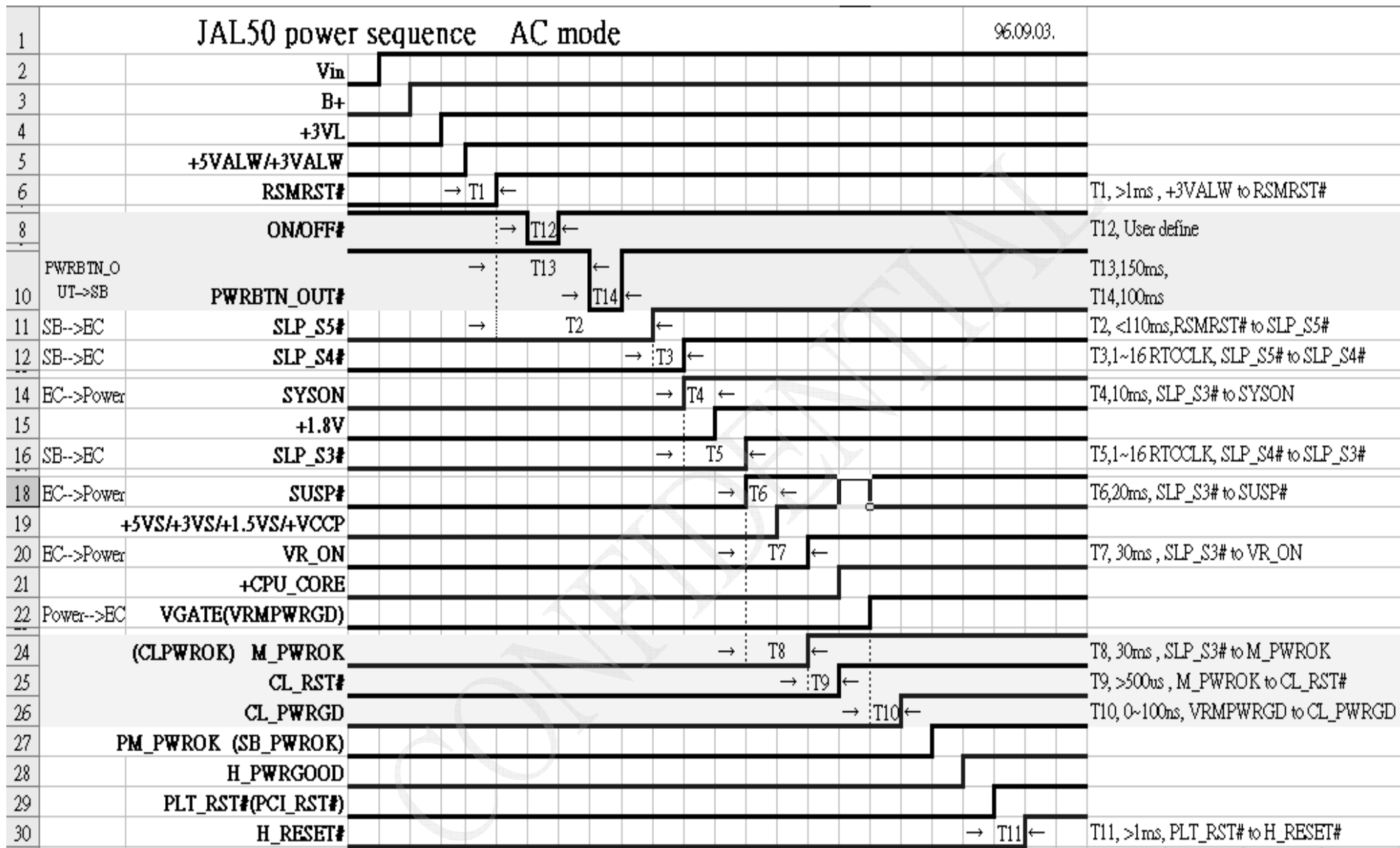
<2008.08.01>

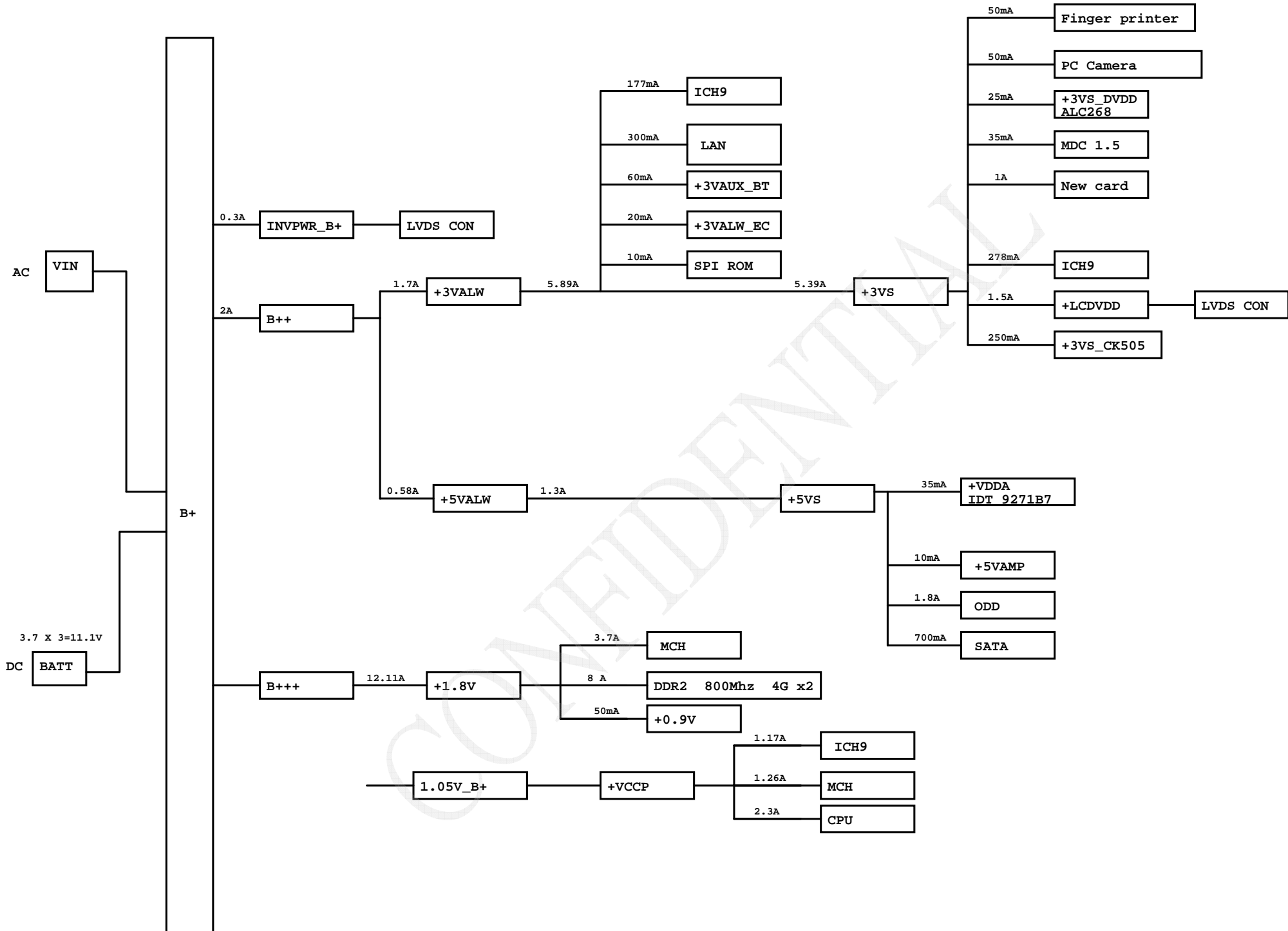
1		Debug 2F issue	28	Add C2130 to solve this issue	0.2
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<2009.03.06>

1		Can not charge issue when dock on Saturn	42	remove R804, change Q14 P/N to SB00000DT00	1.0
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