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HSF Property: ROHS or Halogen-Free(5L3?)

DB BUILD QUANTITY LIST :

1310A2493104 10 PCS CR-SG + H-VRAM + GIGA LAN
 1310A2493105 72 PCS CR-SG + S-VRAM + 10/100 LAN
 1310A2493106 55 PCS CR-UMA + GIGA LAN
 1310A2493201 137 PCS POWER /B
 1310A2493601 137 PCS PICK BTN /B
 1310A2493701 137 PCS USB /B

For DB build
SOUTH BRIDGE
HM75 QPEG Q0
BD82PPSM
 P/N : 6019B0919101

MOTHER BOARD PCB
 P/N : 6050A2493101

POWER BOARD PCB
 P/N : 6050A2493201

USB BOARD PCB
 P/N : 6050A2493601

TOUCHPAD BOARD PCB
 P/N : 6050A2493701

HARVEY 14

CR / HR UMA / DIS

2011.09.27

HARVEY 14 ID LIST
 HURON RIVER UMA : 0X1854
 HURON RIVER DIS : 0X1855
 CHIEF RIVER UMA : 0X1856
 CHIEF RIVER DIS : 0X1857
 SUB SYSTEM ID :
 HP : 0X103C

BASE SCHEMATIC :
 CR-SG + SAMSUNG VRAM + 10/100 LAN + 90W ADAPTER + SUPPORT 27MHZ GREEN CLK + USB2.0 CONN

PAD402 不開銅板 RTC Rest
 PAD4500 不開銅板 SM_Vrer
 PAD2 開
 PAD4 開
 PAD400 開
 PAD4700 開
 PAD500 開
 PAD508 開
 PAD6015 開
 PAD6100 開
 PAD6103 開
 PAD6105 開
 PAD6110 開
 PAD6150 開
 PAD6200 開
 PAD6210 開
 PAD6220 開
 PAD6300 開
 PAD6301 開
 PAD6310 開
 PAD6510 開
 PAD6500 開
 PAD6610 開
 PAD6710 開
 PAD6750 開
 PAD6900 開
 PAD9000 開
 PAD9001 開
 PAD9200 開

GPU VRAM TYPE:

U5 , U6 , U7 , U8

SAMSUNG 1GB C-DIE
 PN : 6019B0818601

R2 : NA
 R3 : NA
 R33 : NA
 R61 : NA

HYNIX 1GB D-DIE
 PN : 6019B0938301

R2 : MOUNT OR : 60130B0000ZT
 R3 : NA
 R33 : NA
 R61 : NA

SAMSUNG 512KB

R2 : NA
 R3 : MOUNT
 R33 : NA
 R61 : NA

HYNIX 512MB

R2 : MOUNT
 R3 : MOUNT
 R33 : NA
 R61 : NA

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DIS GREEN CLK SUPPORT 27MHZ

U9 SLG3NB300V P/N : 6019B0941101
 C188 MOUNT 0.1UF : 6010A0036403
 R126 MOUNT 10R : 60130B10000X
 D4400 NA P/N : 6011A0026803

UMA GREEN CLK

U9 SLG3NB250V 6019B0934701
 C188 NA
 R126 NA
 D4400 NA

DIS ADAPTER 90W

R802 MOUNT 100K : 60130B1040ZT
 R769 NA

UMA ADAPTER 65W

R802 NA
 R769 MOUNT 100K : 60130B1040ZT

USB 3.0 CONN

CN518 6012B0370301
 C2405 MOUNT 0.1UF : 6010A0036403
 C2406 MOUNT 0.1UF : 6010A0036403
 D2400 NA >> ESD
 L470 MOUNT P/N : 6014B0177901
 L471 MOUNT P/N : 6014B0177901

USB 2.0 CONN

CN518 6012B0370102
 C2405 NA
 C2406 NA
 D2400 NA >> ESD
 L470 NA
 L471 NA

BOARD ID	CR-UMA HR-UMA INTEL	CR-SG HR-SG SEYMOUR	CR-SG HR-SG THAMES
ID0-HI R960	0	1	0
ID1-HI R905	0	0	1
ID2-HI R902	0	0	0
ID3-HI R967	0	0	0
ID4-HI R899	0	0	0
ID5-HI R914	1	1	1
ID0-LO R961	1	0	1
ID1-LO R903	1	1	0
ID2-LO R904	1	1	1
ID3-LO R968	1	1	1
ID4-LO R900	1	1	1
ID5-LO R920	0	0	0

ID0 = GPIO40 RXXX = 10K : 60130B1030ZT
 ID1 = GPIO41 0 : RXXX NA 1 : RXXX MOUNT

BOARD_ID5 ONLY FOR WEBCAN USE
 FOR HD WEB CAM BOARD_ID5 PULL P3V3A
 FOR VGA WEB CAM BOARD_ID5 PULL GND

M/B ID	DB	SI	PV	MV
R844	MOUNT	NA	MOUNT	NA
R824	MOUNT	MOUNT	NA	NA
R845	NA	MOUNT	NA	MOUNT
R828	NA	NA	MOUNT	MOUNT

RXXX = 10K : 60130B1030ZT NOV JAN MAR

RTL8161FH = 6019B0928101(10/100/1000)
 RTL8165EH = 6019B0928301(10/100)

RTL8165EH(10/100) LDO MODE

R408 : MOUNT ----> CHOOSE LDO MODE OR : 60130B0000ZT
 R407 : NA ----> CHOOSE SWITCHING MODE

R413 : NA
 C404 : NA
 C405 : NA
 C406 : NA
 C409 : NA
 C411 : NA
 C415 : NA
 C417 : NA
 C420 : NA
 L400 : NA
 U470 : NA

U502 : MOUNT 6016B0008101
 U400 : MOUNT 6019B0928301 (10/100 LAN)

RTL8161FH(GIGA-LAN) SWITCHING MODE

R408 : NA ----> CHOOSE LDO MODE
 R407 : MOUNT ----> CHOOSE SWITCHING MODE OR : 60130B1030ZT
 R413 : MOUNT OR_0603 : 60130B000000Z
 C404 : MOUNT 4.7UF : 6010B0009904

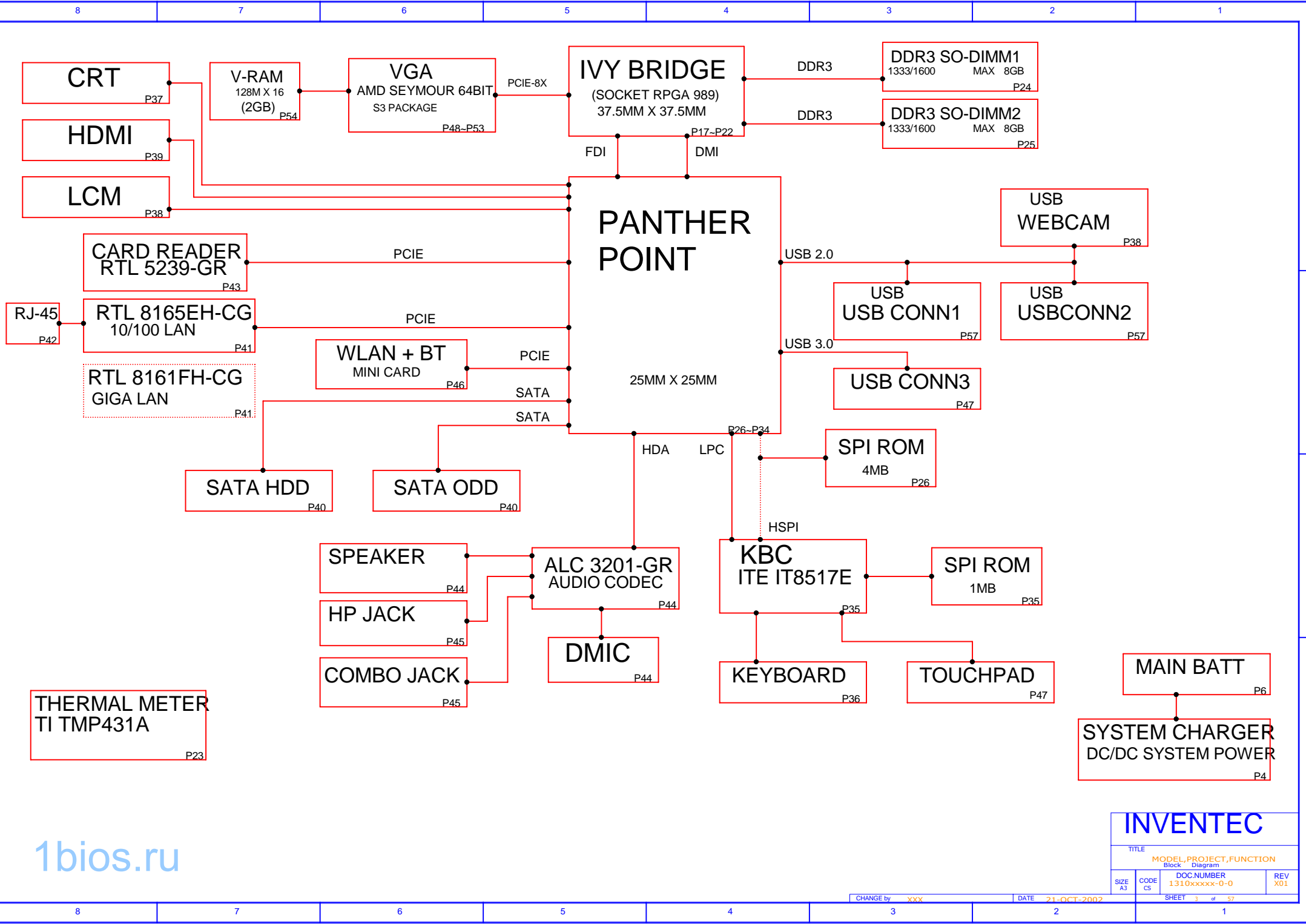
C405 : MOUNT 0.1UF : 6010A0036403
 C406 : MOUNT 0.1UF : 6010A0036403
 C409 : MOUNT 0.1UF : 6010A0036403
 C411 : MOUNT 0.1UF : 6010A0036403
 C415 : MOUNT 0.1UF : 6010A0036403
 C417 : MOUNT 4.7UF : 6010B0009904
 C420 : MOUNT 0.1UF : 6010A0036403
 L400 : MOUNT P/N : 6014B0200401
 U470 : MOUNT 6016B0010401
 U502 : NA
 U400 : MOUNT 6019B0928101 (GIGALAN)

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN CHECK					TITLE MODEL_PROJECT_FUNCTION HARVEY 14			
RESPONSIBLE					SIZE	CODE	DOCNUMBER	REV
FILE NAME:					IS	1310xxxx-9-0		X01
P/N	6019B0928101				SHEET			of 57

DATE	CHANGE NO.	REV
2010.02.20		X01

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06	Battery Connector	31	PCH-6	56	DGPU POWER
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09	P1V05S	34	PCH-9		
10	P1V8S	35	EC ITE8517E		
11	PVSA	36	KB & LED		
12	PVCORE-1	37	CRT		
13	PVCORE-2	38	LCD & WEBCAN		
14	PORT & EMI PART	39	HDMI		
15	P3V3S, P5V0S	40	SATA HDD& ODD		
16	GREEN CLK	41	LAN		
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18	CPU-2	43	CARD READER		
19	CPU-3	44	AUDIO CODEC		
20	CPU-4	45	HP & MIC JACK		
21	CPU-5	46	WLAN		
22	CPU-6	47	USB 3.0 CONN		
23	Thermal & Fan	48	SEYMOUR PCI-E INTERFACE		
24	DDR3-1	49	SEYMOUR CRT CLK THERMAL		
25	DDR3-2	50	SEYMOUR THERMAL SENSOR		

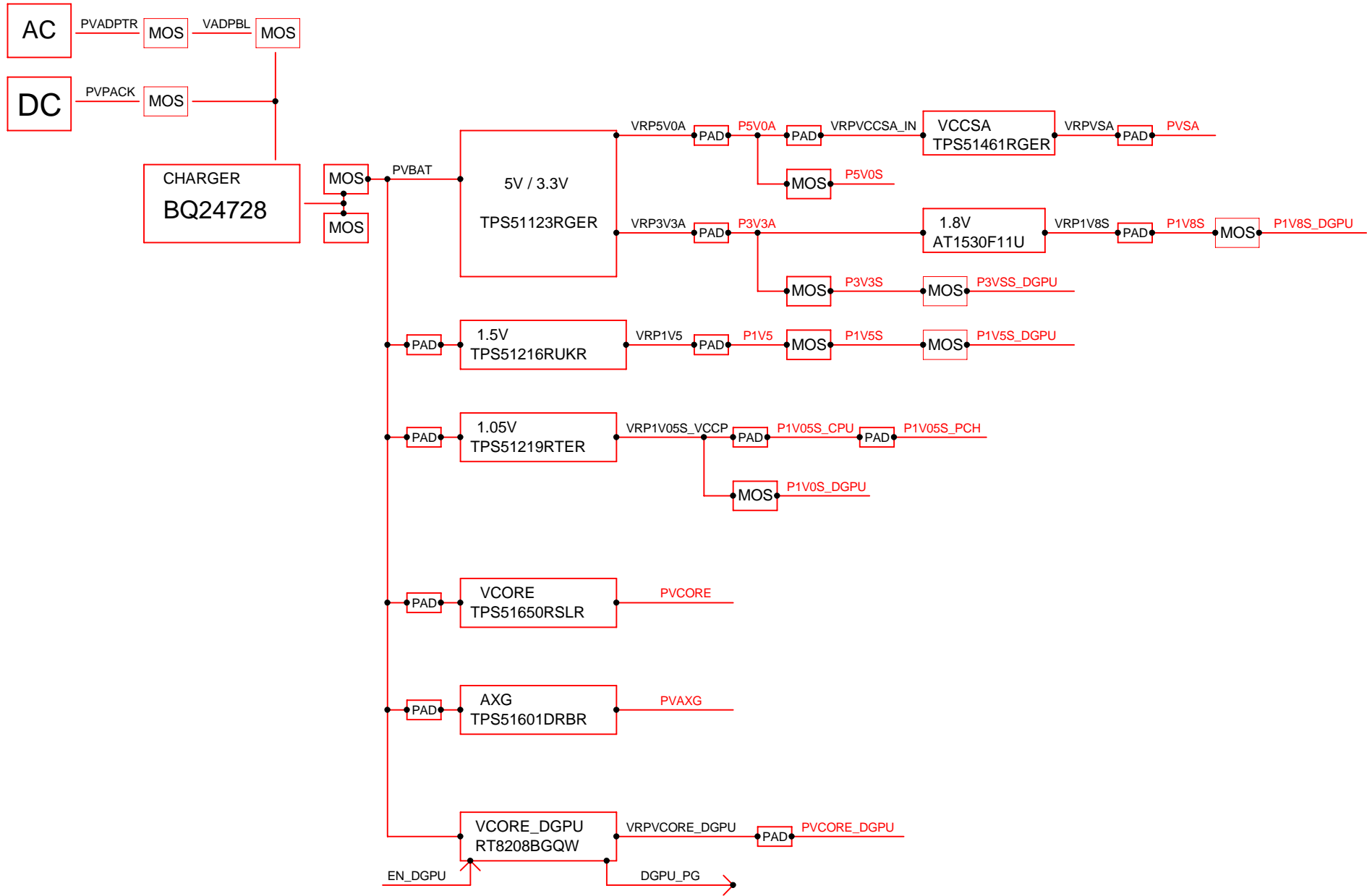


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INVENTEC			
TITLE Block Diagram			
MODEL, PROJECT, FUNCTION			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 3 of 57

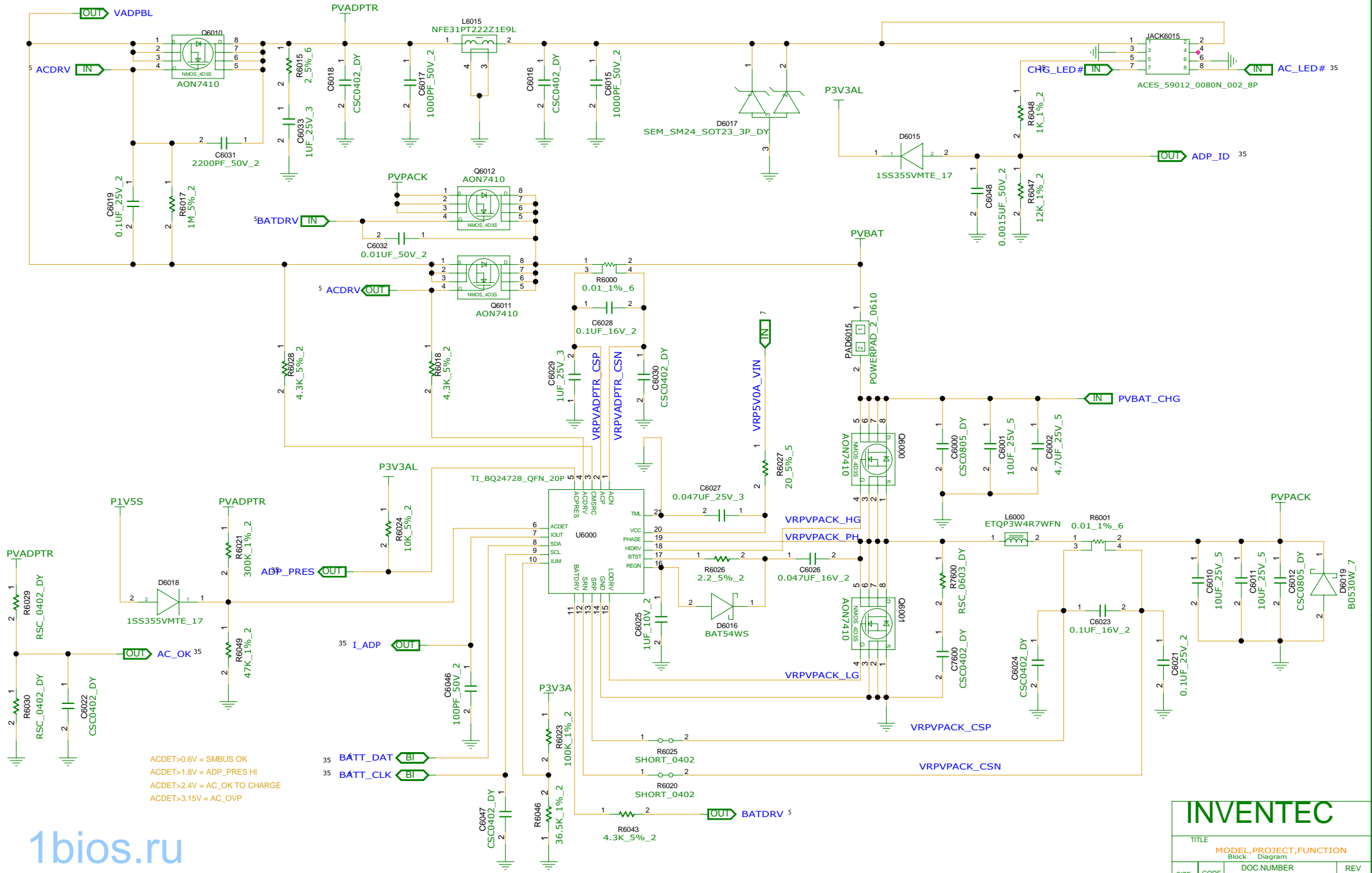
8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1



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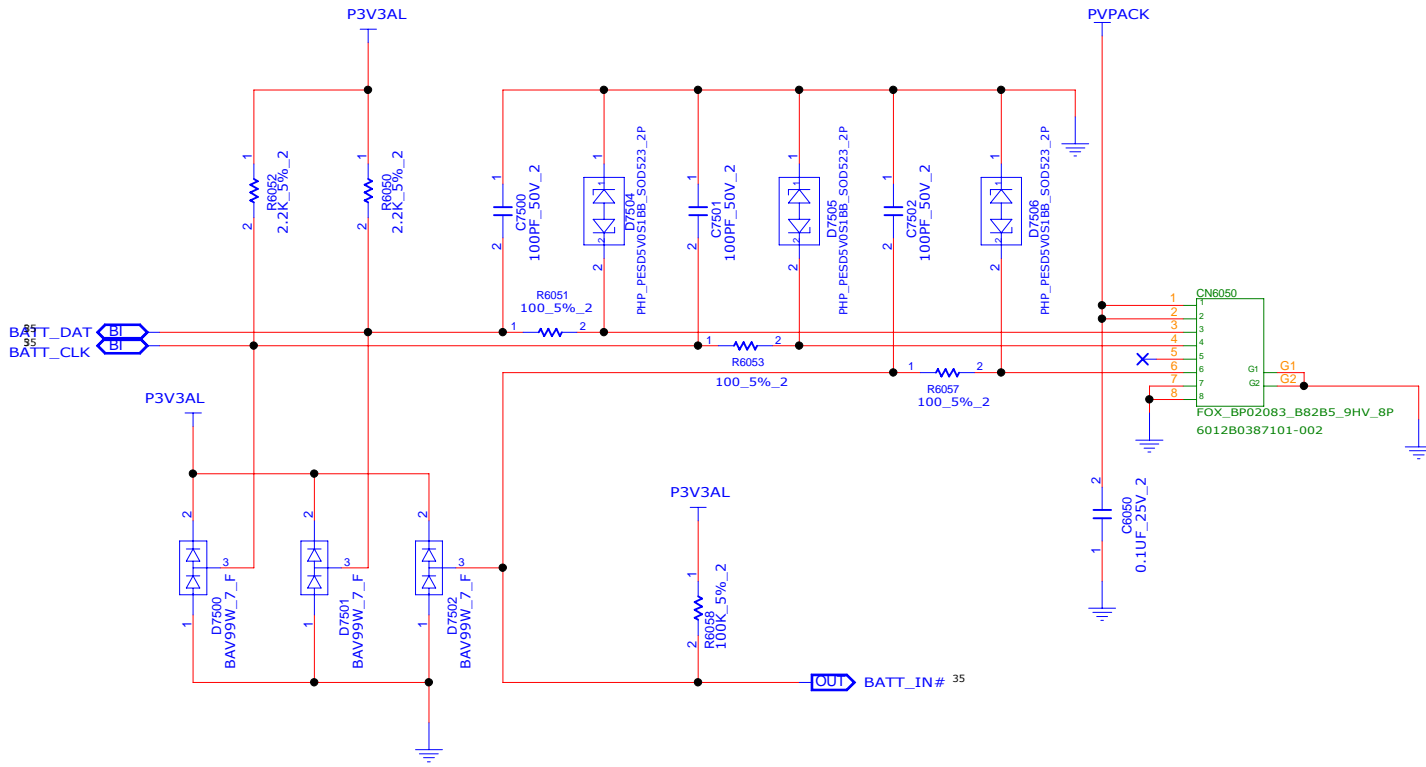
INVENTEC			
TITLE MODEL PROJECT FUNCTION POWER PROCEDURE			
DOC NUMBER 1310xxxxx-0-0		REV X01	
SIZE A3	CODE CS	SHEET 4 of 57	



ACDET>0.6V = SMBUS OK
 ACDET>1.8V = ADP_PRES HI
 ACDET>2.4V = AC_OK TO CHARGE
 ACDET>3.15V = AC_OVP

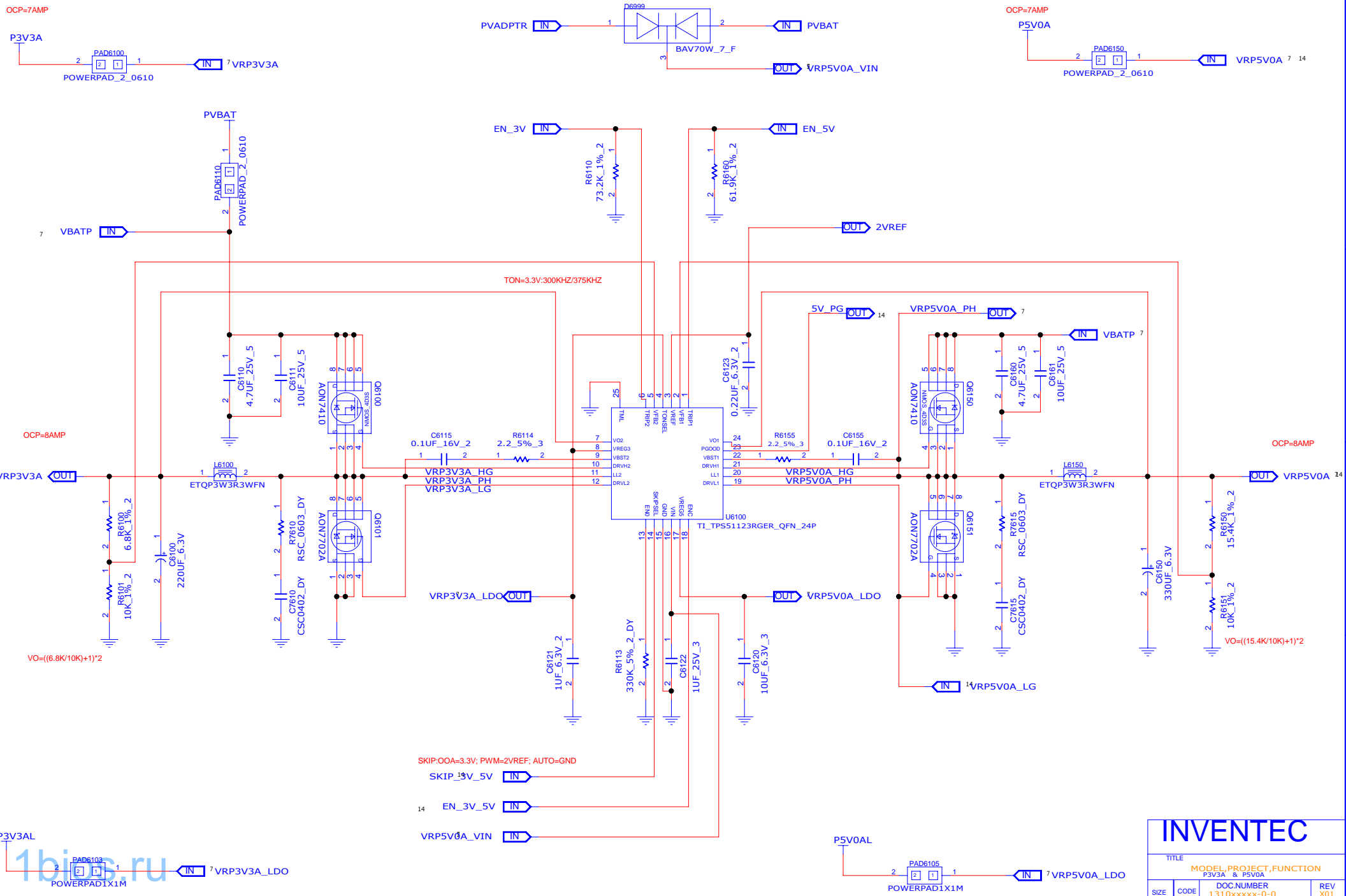
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INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	
A3	CS	1310xxxxx-0-0	
			REV
			X01
CHANGE by			DATE
XXX			21-OCT-2002
SHEET			of
5			57



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION SELECTOR			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 6 of 57			



INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
P3V3A & P5V0A			
SIZE		REV	
A3	CODE	CS	X01
CHANGE by		DATE	
XXX		21-OCT-2002	
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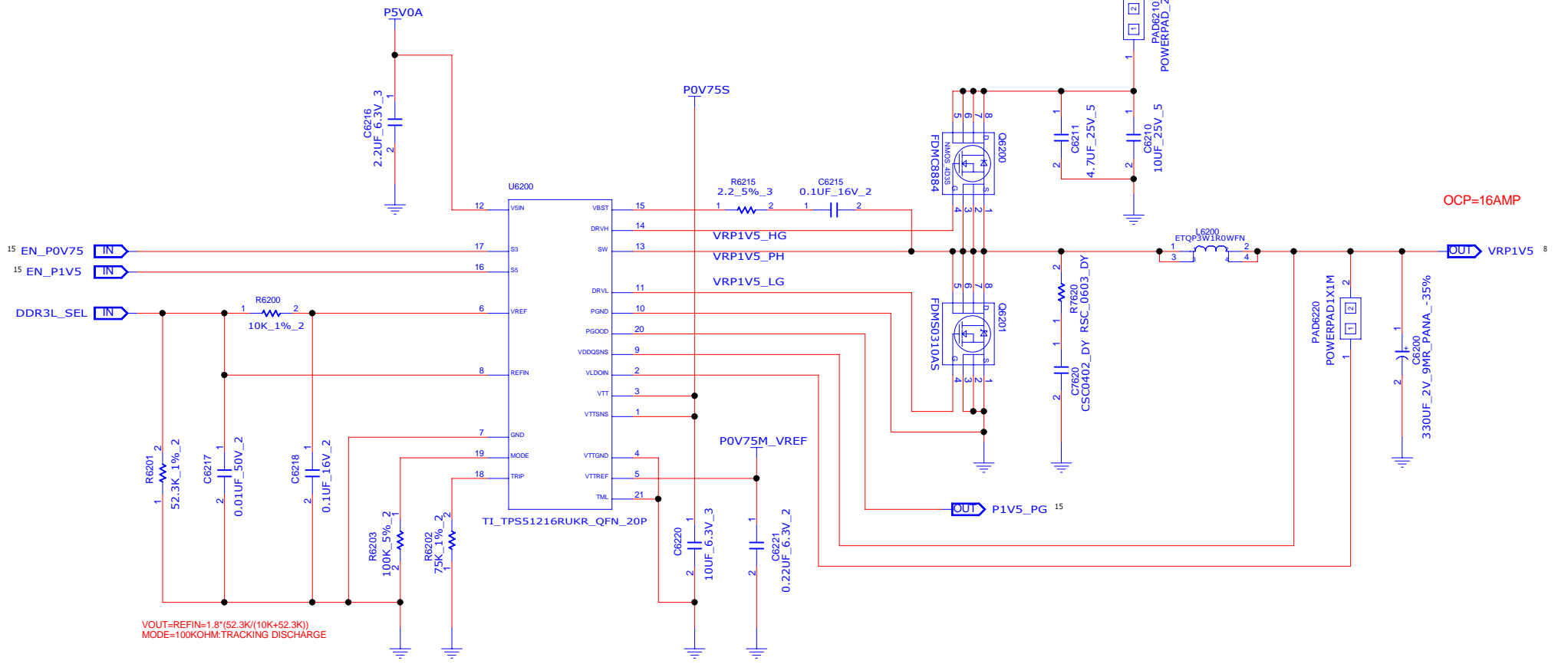


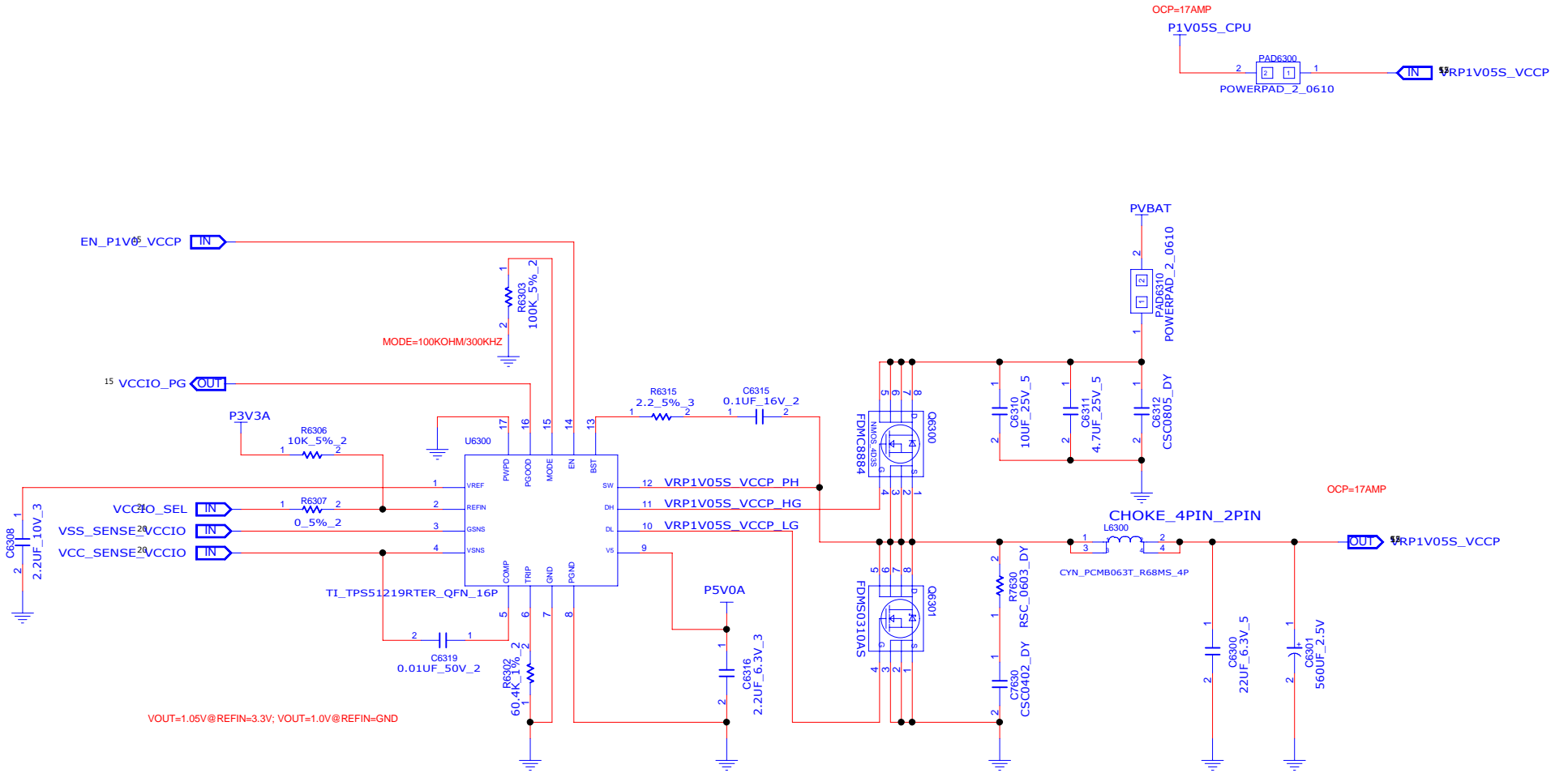
Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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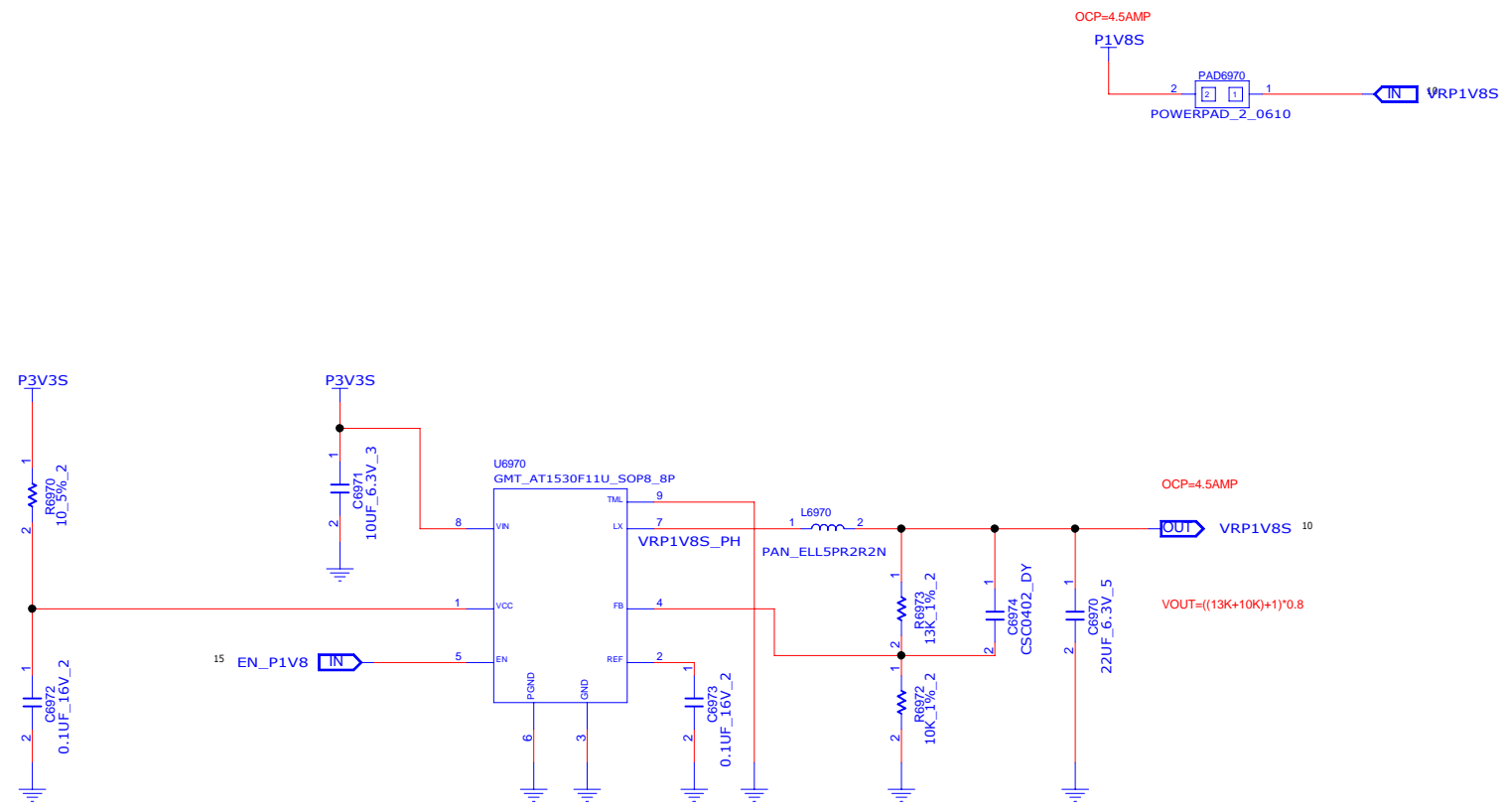
INVENTEC

TITLE P1V5		
MODEL,PROJECT,FUNCTION		
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0
		REV X01



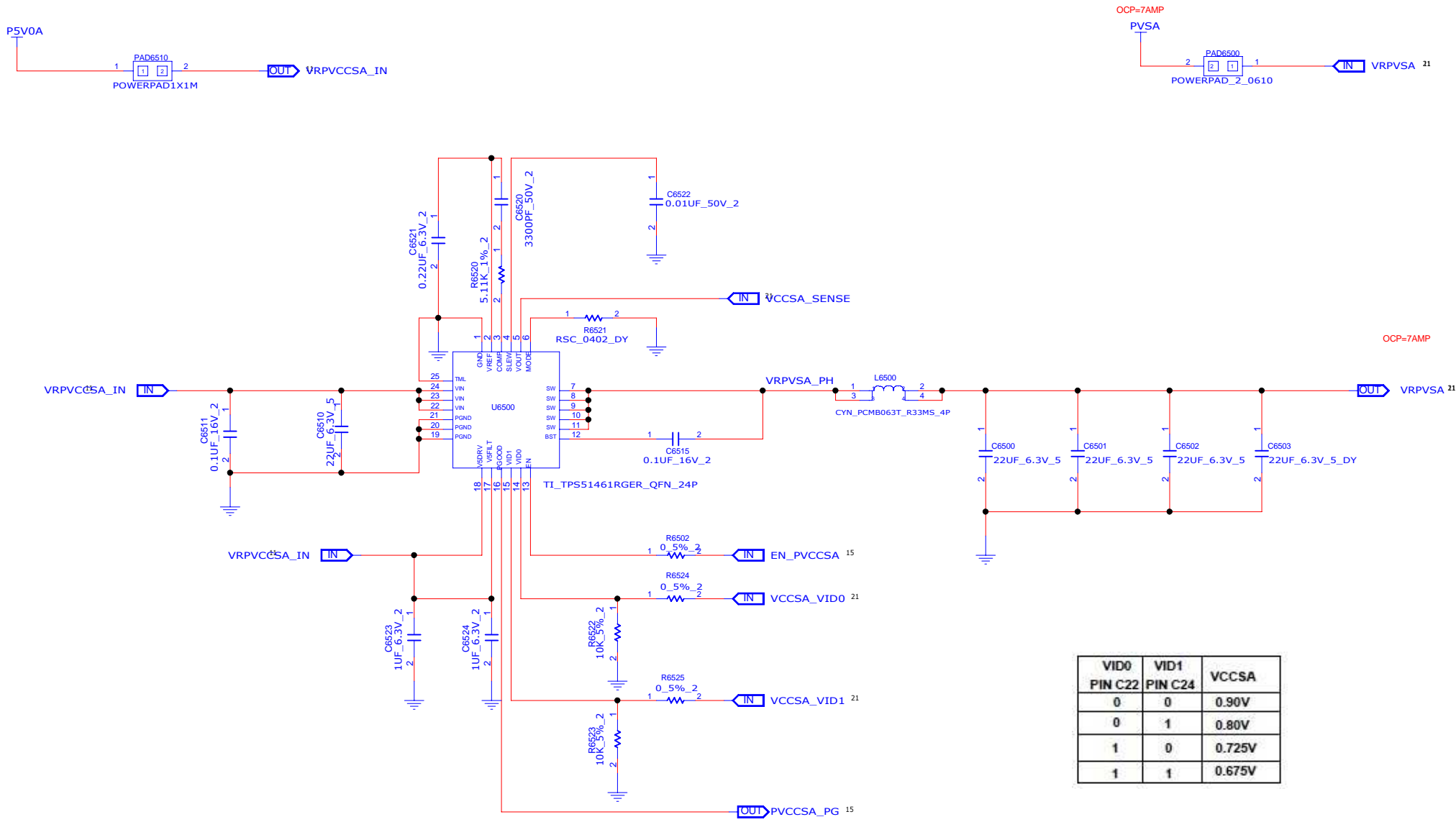
INVENTEC

TITLE			
MODEL_PROJECT,FUNCTION			
P1V05S_CPU			
SIZE		DOC NUMBER	
A3	CS	1310xxxxx-0-0	
REV			X01



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INVENTEC			
TITLE MODEL PROJECT,FUNCTION P1V8S			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 10 of 57



VID0 PIN C22	VID1 PIN C24	VCCSA
0	0	0.90V
0	1	0.80V
1	0	0.725V
1	1	0.675V

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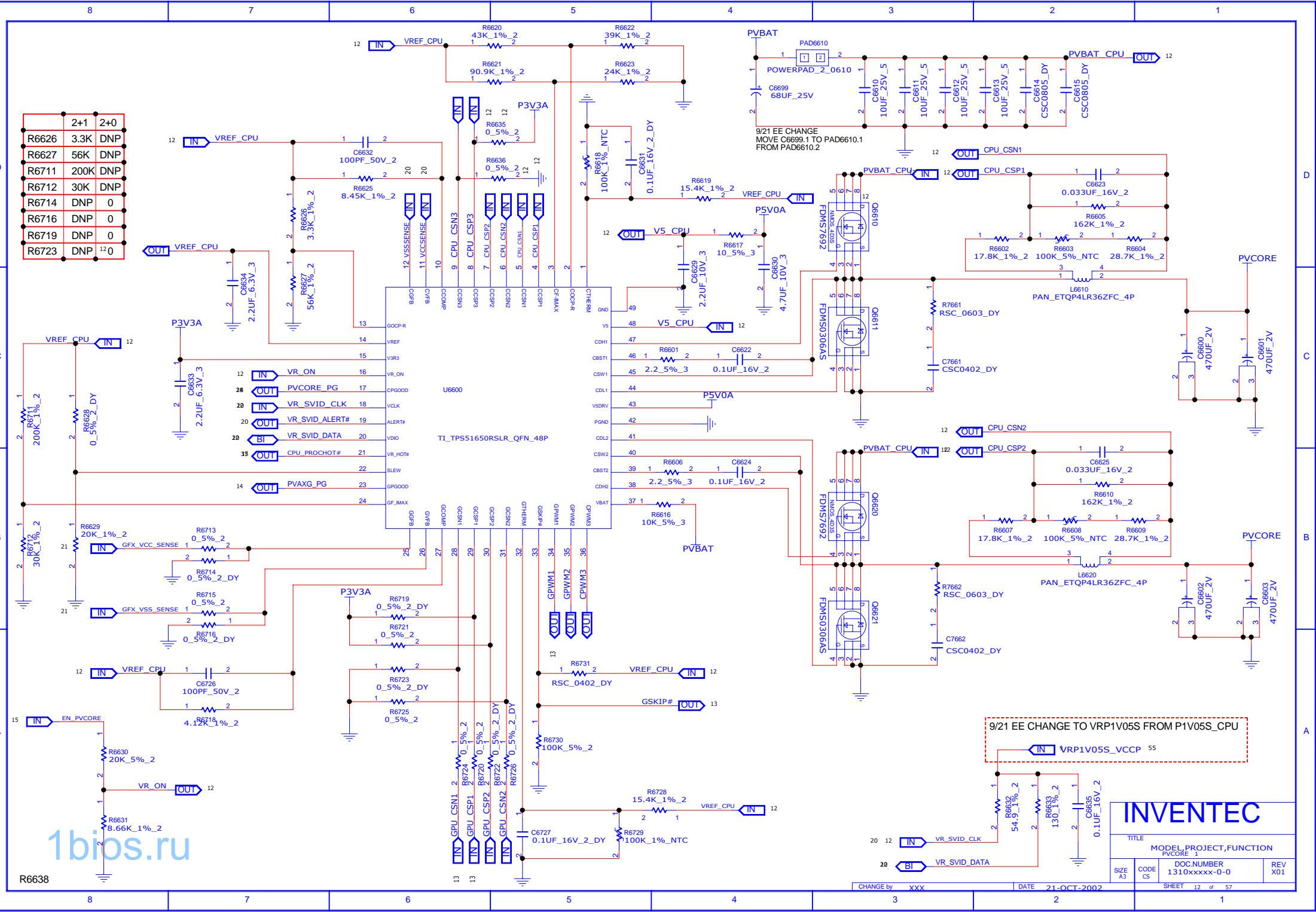
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
PVSA

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 11 of 57

	2+1	2+0
R6626	3.3K	DNP
R6627	56K	DNP
R6711	200K	DNP
R6712	30K	DNP
R6714	DNP	0
R6716	DNP	0
R6719	DNP	0
R6723	DNP	120

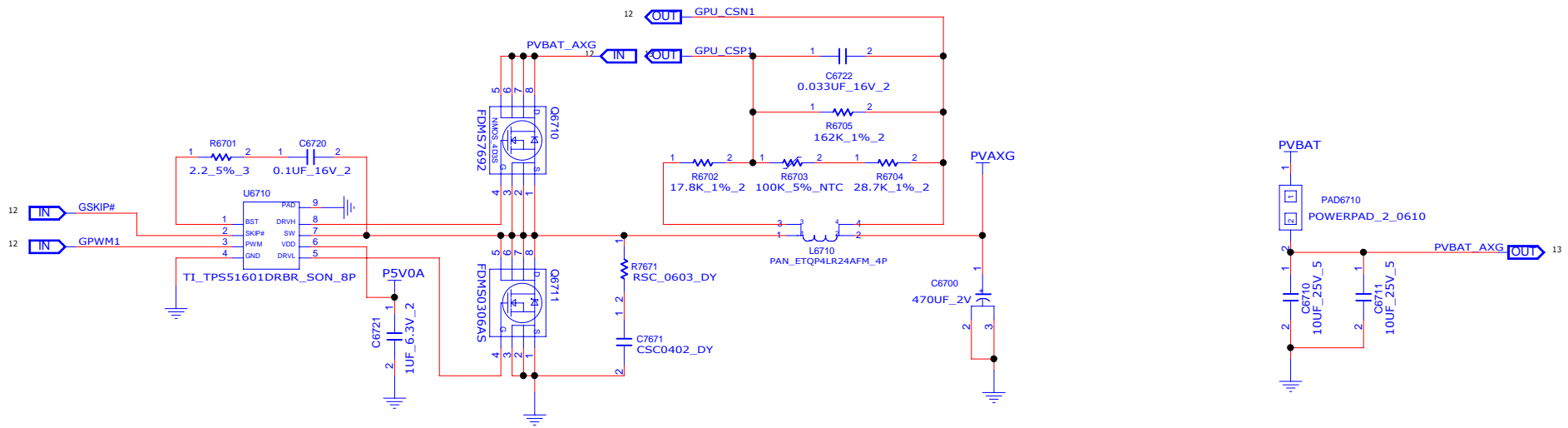


9/21 EE CHANGE TO VRP1V05S FROM P1V05S_CPU

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION			
PVCORE_1			
SIZE A3		CODE CS	REV X01
DOC NUMBER 1310xxxxx-0-0		REV X01	
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 12		of 57	

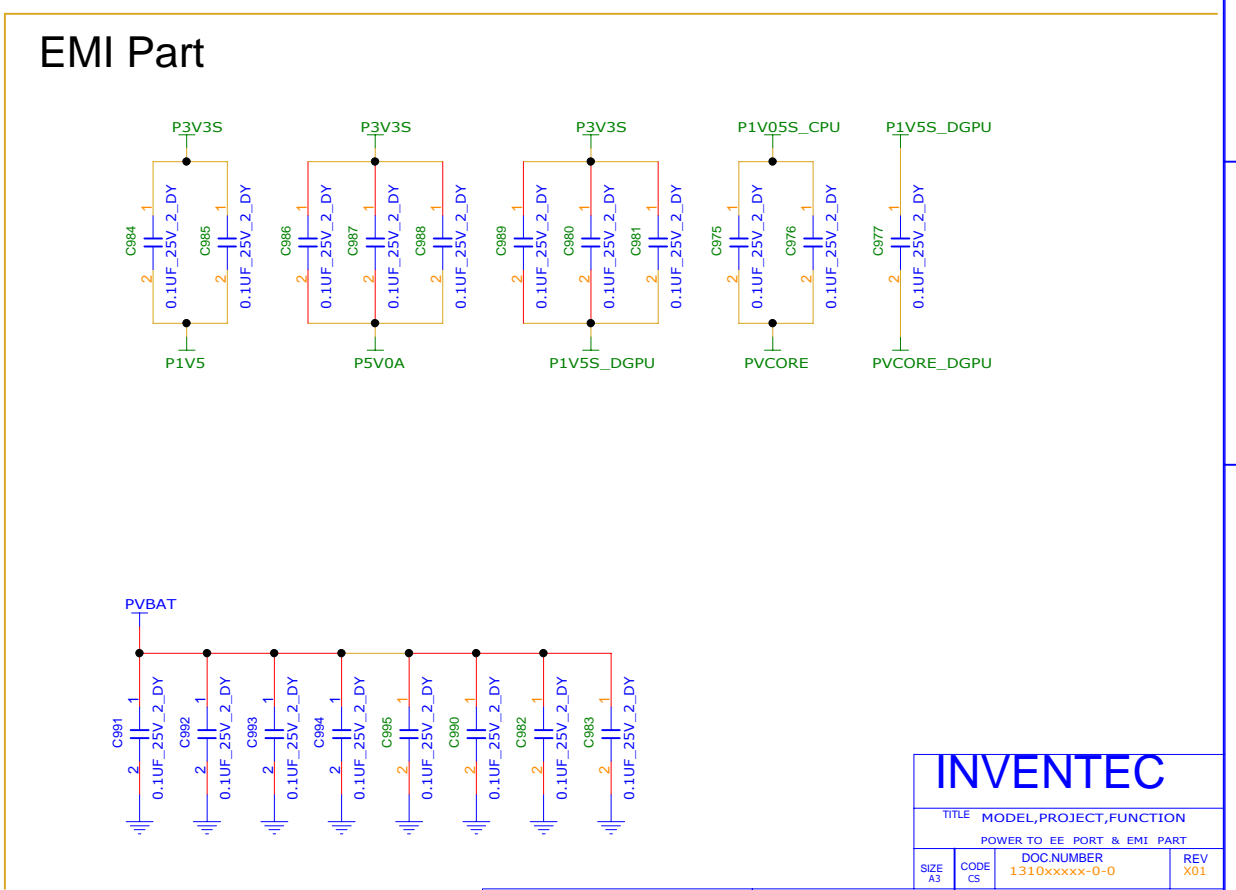
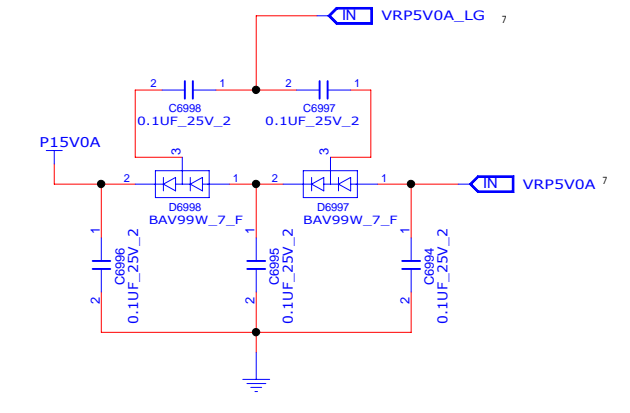
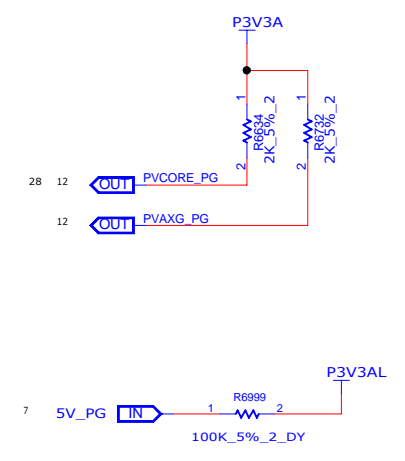
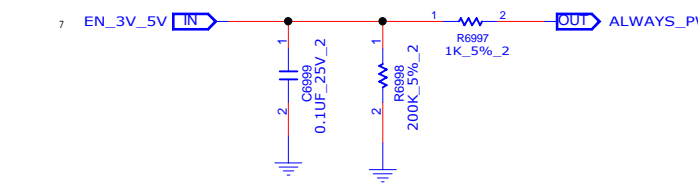
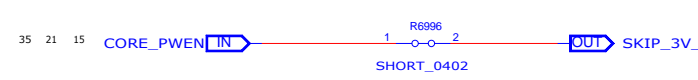
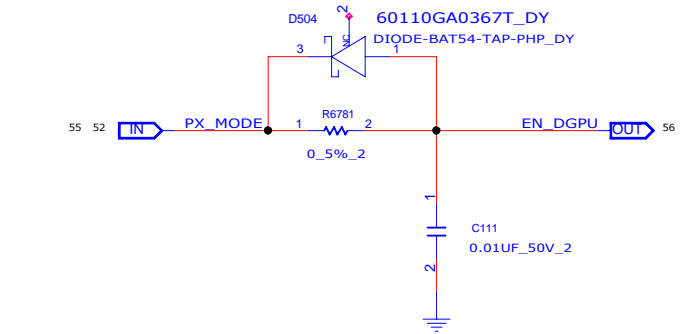
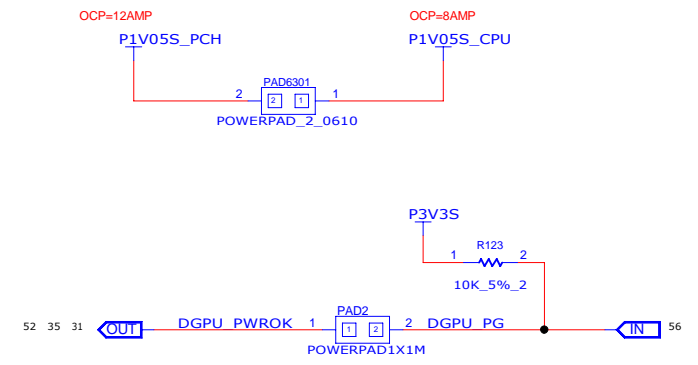
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R6638



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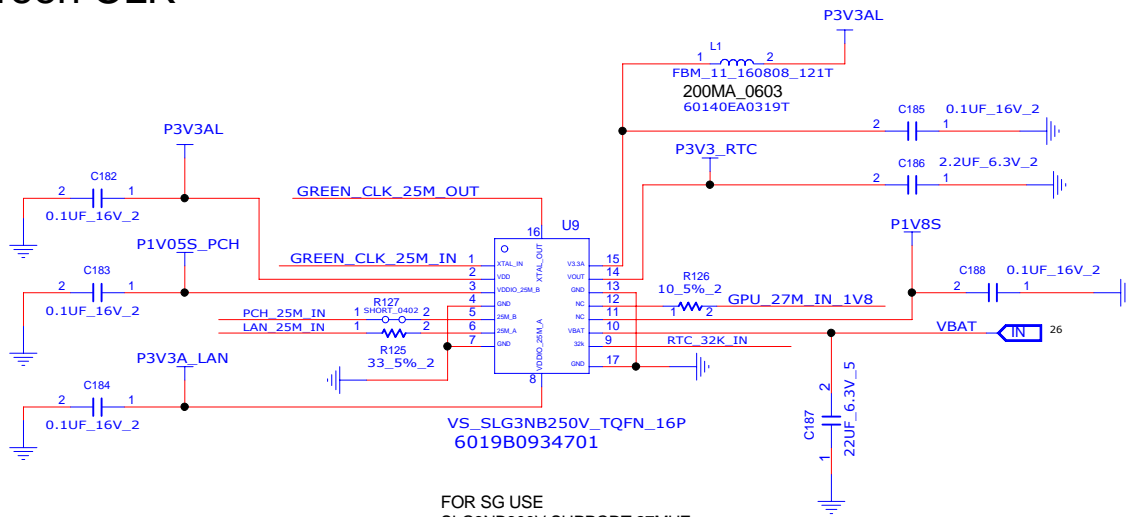
INVENTEC			
TITLE MODEL,PROJECT,FUNCTION PVCORE_2			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 13 of 57



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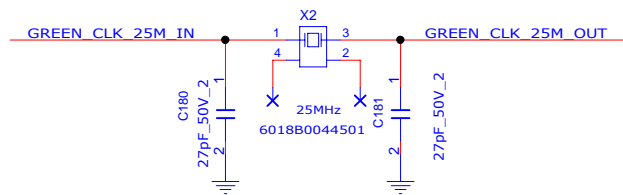
INVENTEC			
TITLE MODEL,PROJECT,FUNCTION			
POWER TO EE PORT & EMI PART			
DOC NUMBER		REV	
1310xxxxx-0-0		X01	
SIZE A3	CODE CS	SHEET 14 of 57	

Green CLK



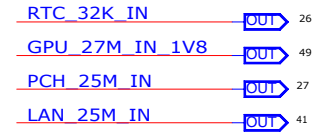
FOR SG USE
 SLG3NB300V SUPPORT 27MHZ
 P/N : 6019B0941101

FOR UMA USE
 SLG3NB250V
 P/N : 6019B0934701



FOR UMA
 U9 : 6019B0934701
 R126 : NA
 C188 : NA

FOR SG
 U9 : SLG3NB300V P/N APPLY
 R126 : MOUNT
 C188 : MOUNT



TYPICAL RTC_32K_IN TRACE <= 6
 MAX. LENGTH <= 24

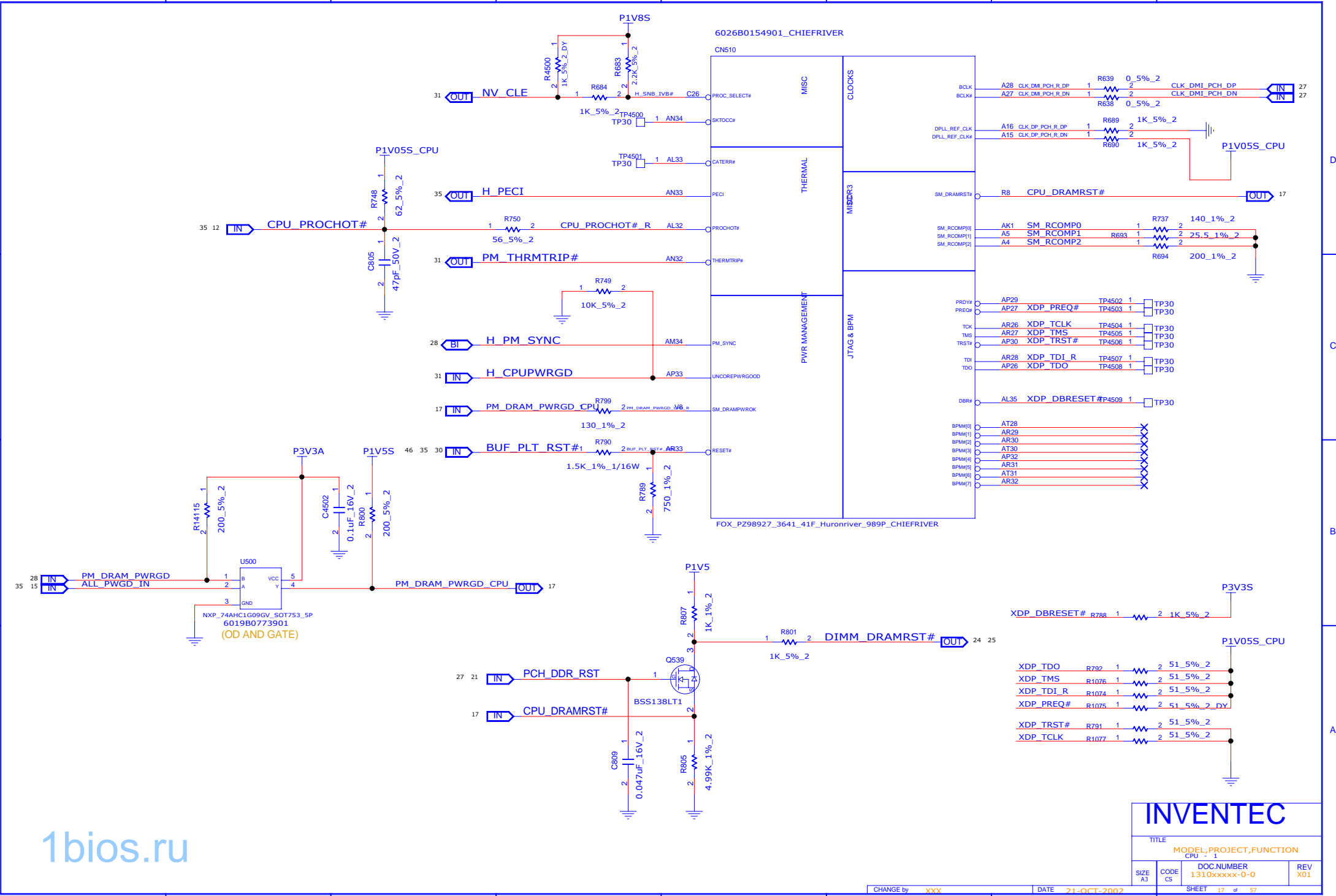
TYPICAL GPU_27M_IN TRACE <= 8
 MAX. LENGTH <= 12

TYPICAL LAN_25M_IN TRACE <= 8
 MAX. LENGTH <= 12

TYPICAL LAN_25M_IN TRACE <= 8
 MAX. LENGTH <= 12

IF USE U9 (SLG3NB250V)

MOUNT	OPEN (PAGE26)	OPEN (PAGE41)
X2	D4400	X400
R1	X501	C402
L1	R958	C403
C180	C874	
C181	C875	
C182		
C183	OPEN (PAGE27)	OPEN (PAGE49)
C184	X503	X1
C185	R1041	R29
C186	C962	C35
C187	C965	C36
R906 (PAGE26)		
R912 (PAGE27)		
R414 (PAGE41)		
R120 (PAGE49)		



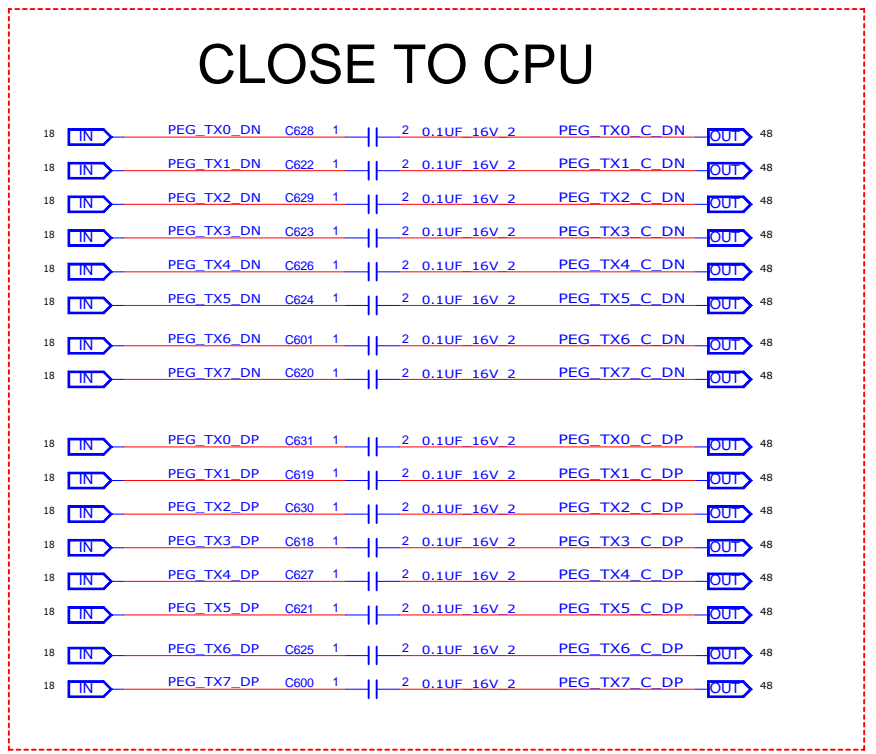
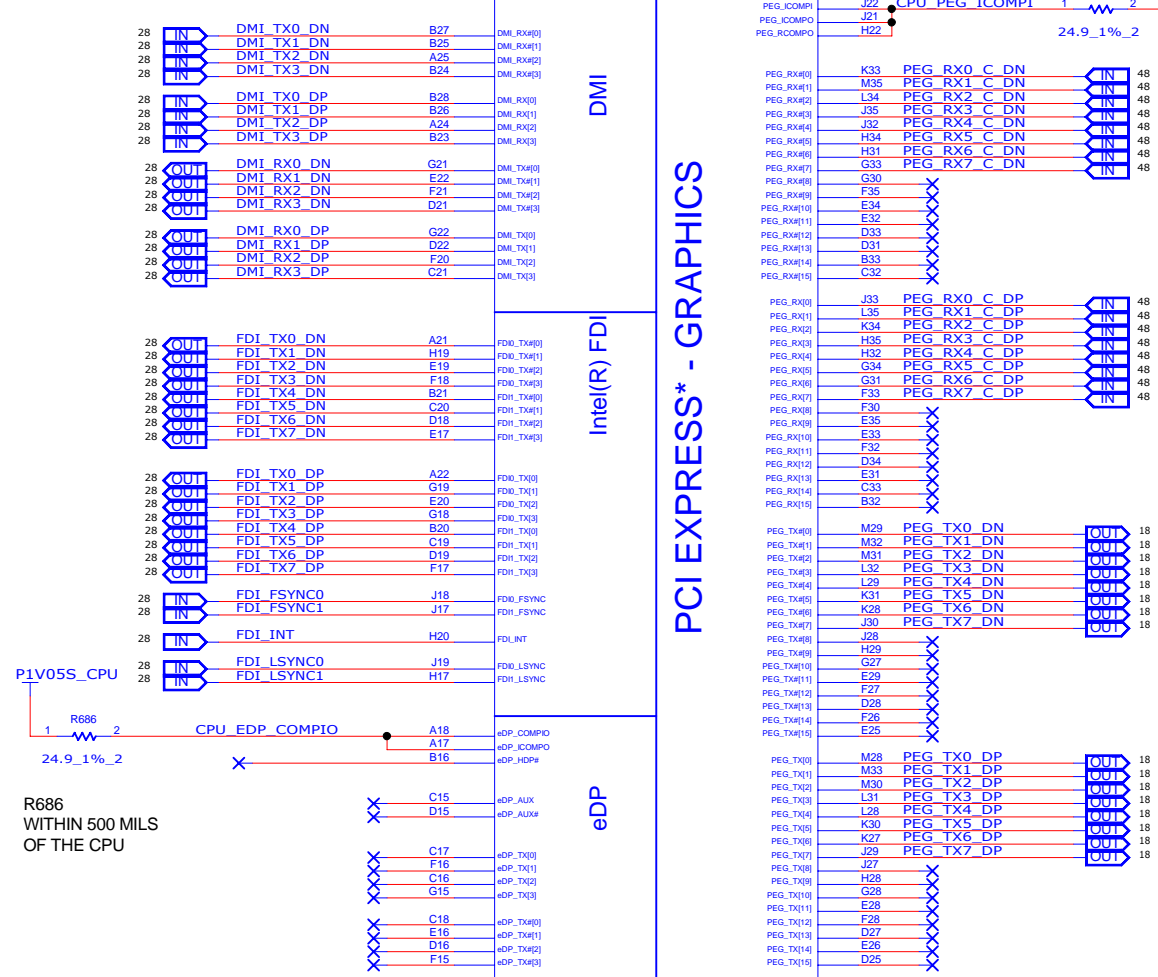
R736
WITHIN 500 MILS
OF THE CPU

P1V05S_CPU

J22 CPU_PEG_ICOMPI 1 R736 2
H22 24.9_1%_2

CN510 6026B0154901_CHIEFRIVER

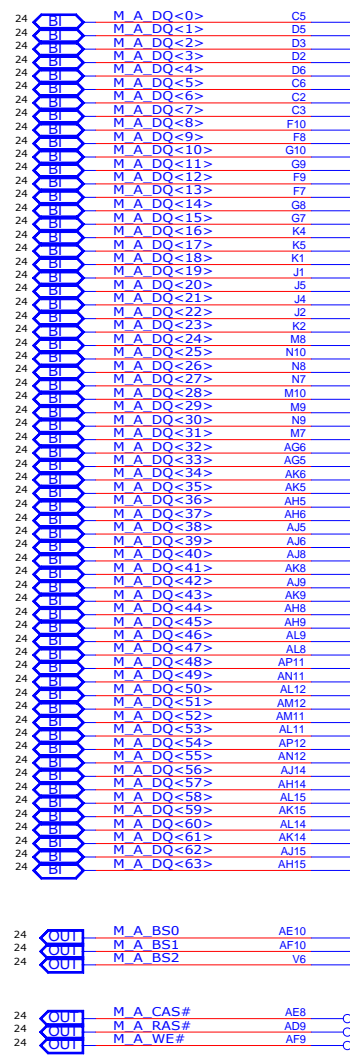
FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER



CN510

6026B0154901_CHIEFRIVER

DDR SYSTEM MEMORY A

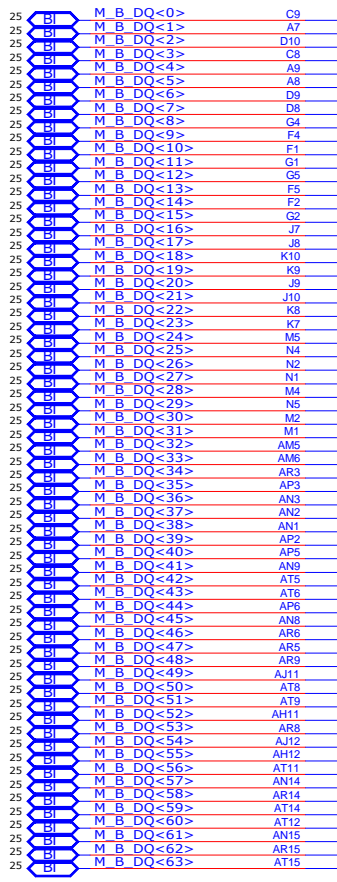


FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

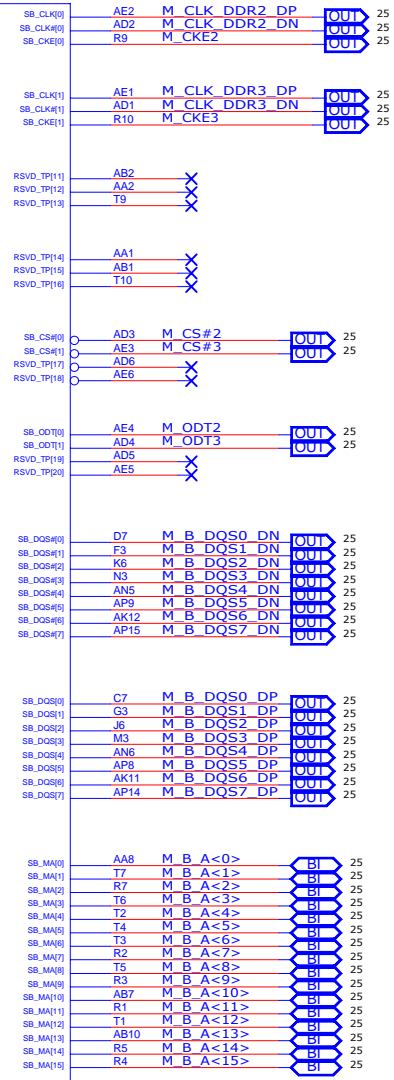
CN510

6026B0154901_CHIEFRIVER

DDR SYSTEM MEMORY B



FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER



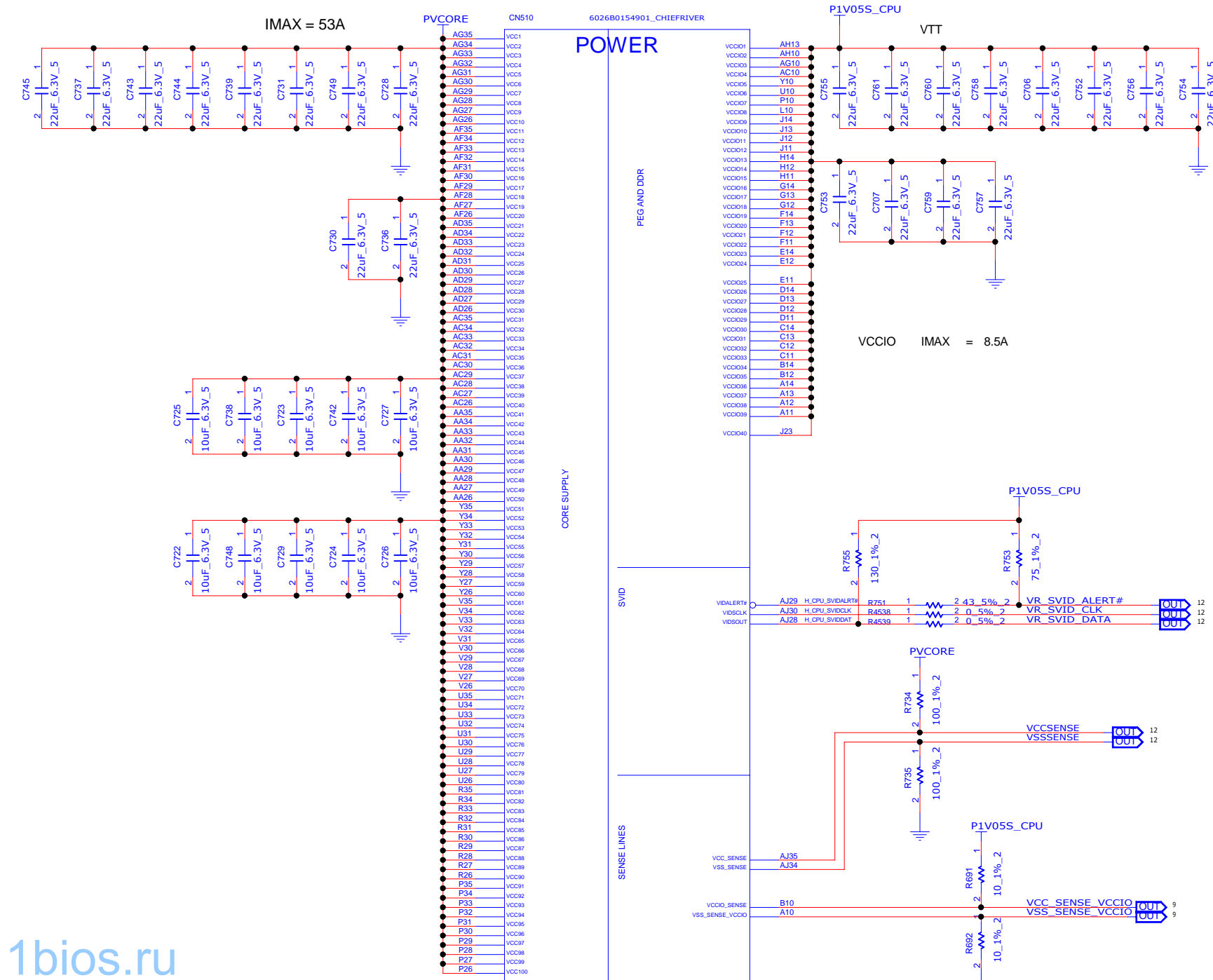
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
CPU 3

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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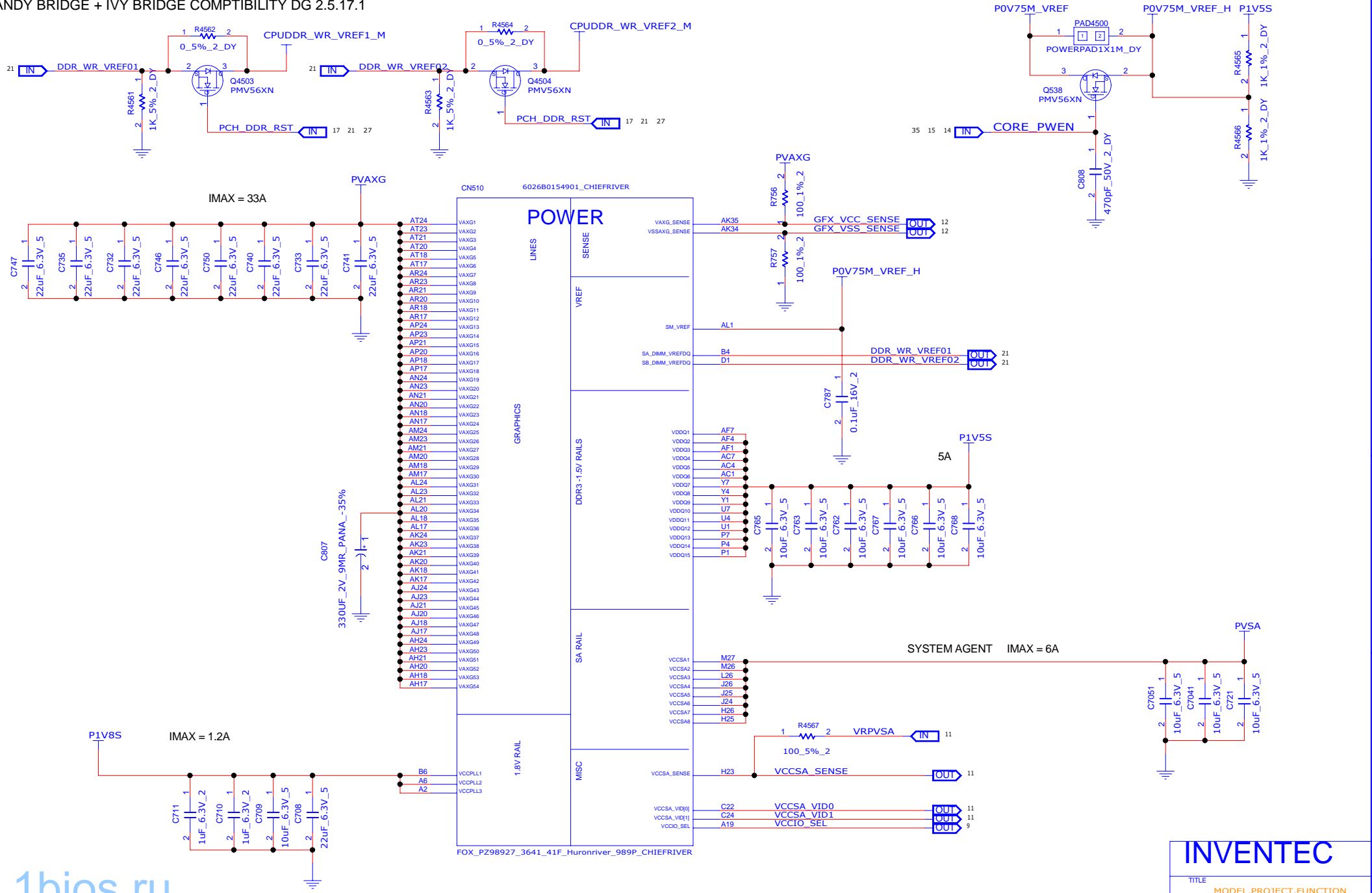
POWER



FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

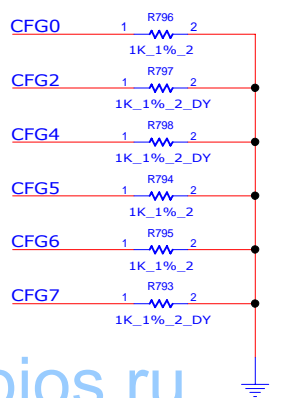
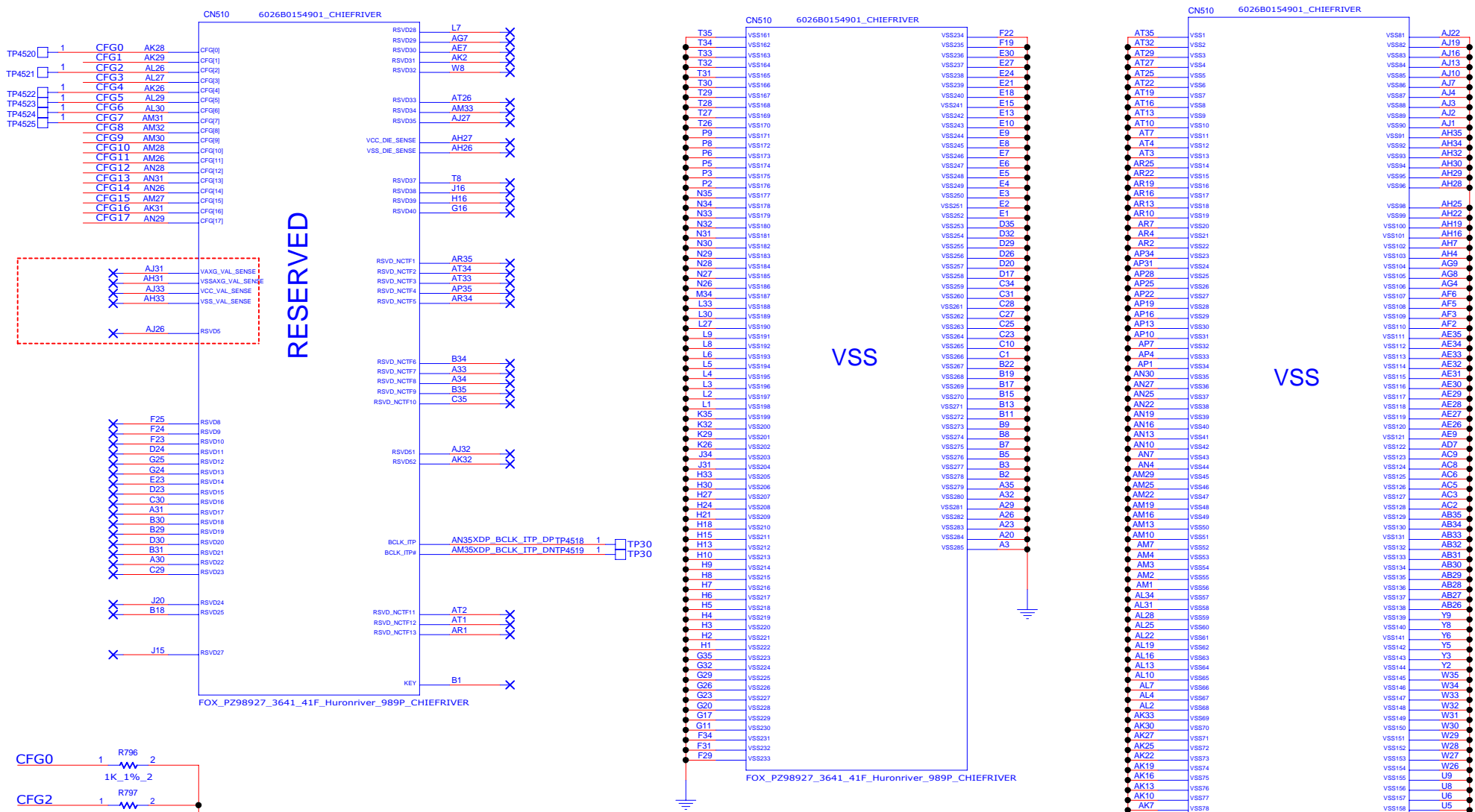
INVENTEC			
TITLE MODEL,PROJECT,FUNCTION CPU - 4			
SIZE A3		CODE CS	REV X01
DOC NUMBER 1310xxxxx-0-0		REV X01	
CHANGE by XXX		DATE 21-OCT-2002	SHEET 20 of 57

SANDY BRIDGE + IVY BRIDGE COMPTIBILITY DG 2.5.17.1



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INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
CPU			
SIZE A3		DOC NUMBER	
CODE CS		1310xxxxx-0-0	
REV X01		DATE	
CHANGE by		21-OCT-2002	
SHEET		21 of 57	



CFG[2] : PCI Express* Static x16 Lane Numbering Reversal.
 1 = Normal operation
 0 = Lane numbers reversed

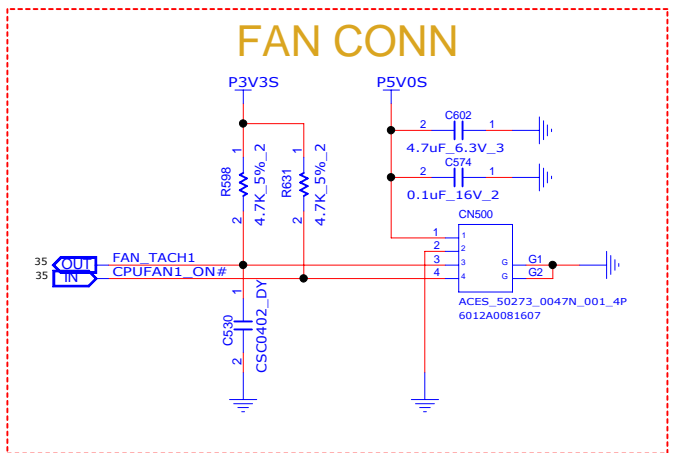
CFG[4] : eDP enable
 1 = Disabled
 0 = Enabled

CFG[6:5] : PCI Express Bifurcation:
 00 = 1 x8, 2 x4 PCI Express
 01 = reserved
 10 = 2 x8 PCI Express
 11 = 1 x16 PCI Express

CFG[7] : PEG DEFER TRAINING
 1: (Default) PEG Train immediately following RESETB deassertion
 0: PEG Wait for BIOS for training

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INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 22 of 57



7.2.5 Register : Local Diode Temperature Alert Temperature

Location : Read = Address 05h Write = Address 0Bh
 Type : Read/Write

Power on default value : Hardware strapping.

BIT	7	6	5	4	3	2	1	0
NAME	LDT Alert Temperature							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	Hardware strapping							

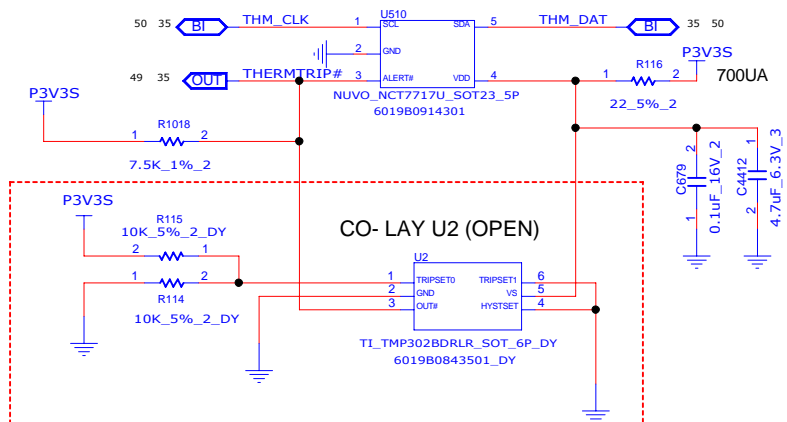
6.6 ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR	TEMPERATURE (°C)
2KΩ	75
7.5KΩ	90
10.5KΩ	100
14KΩ	105
18.7KΩ	110

THERMAL SENSOR(LOCAL)

NCT7717U I2C / SMBus address is 1001000xb (x is R/W bit).



TMP302 Available Versions⁽¹⁾

DEVICE	SELECTABLE TRIP POINTS (°C)
TMP302A	50, 55, 60, 65
TMP302B	70, 75, 80, 85
TMP302C	90, 95, 100, 105
TMP302D	110, 115, 120, 125

(1) For other available trip points, please contact a TI representative.

Table 1. Trip Point vs TRIP_{SET1} and TRIP_{SET0}

TRIP _{SET1}	TRIP _{SET0}	TMP302A	TMP302B	TMP302C	TMP302D
GND	GND	+50°C	+70°C	+90°C	+110°C
GND	V _S	+55°C	+75°C	+95°C	+115°C
V _S	GND	+60°C	+80°C	+100°C	+120°C
V _S	V _S	+65°C	+85°C	+105°C	+125°C

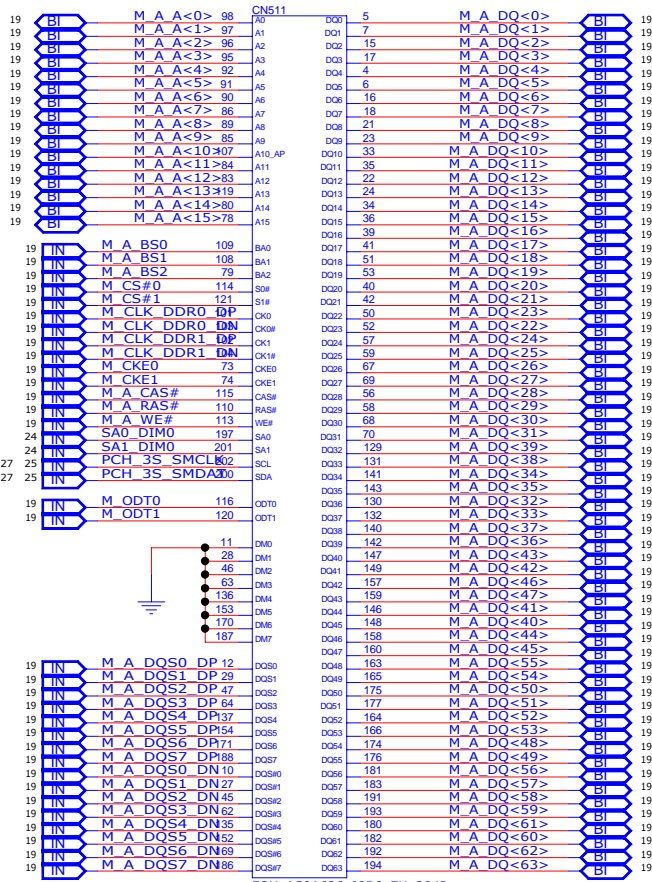
Table 2. HYST_{SET} Window

HYST _{SET}	THRESHOLD HYSTERESIS
GND	+5°C
V _S	+10°C

INVENTEC

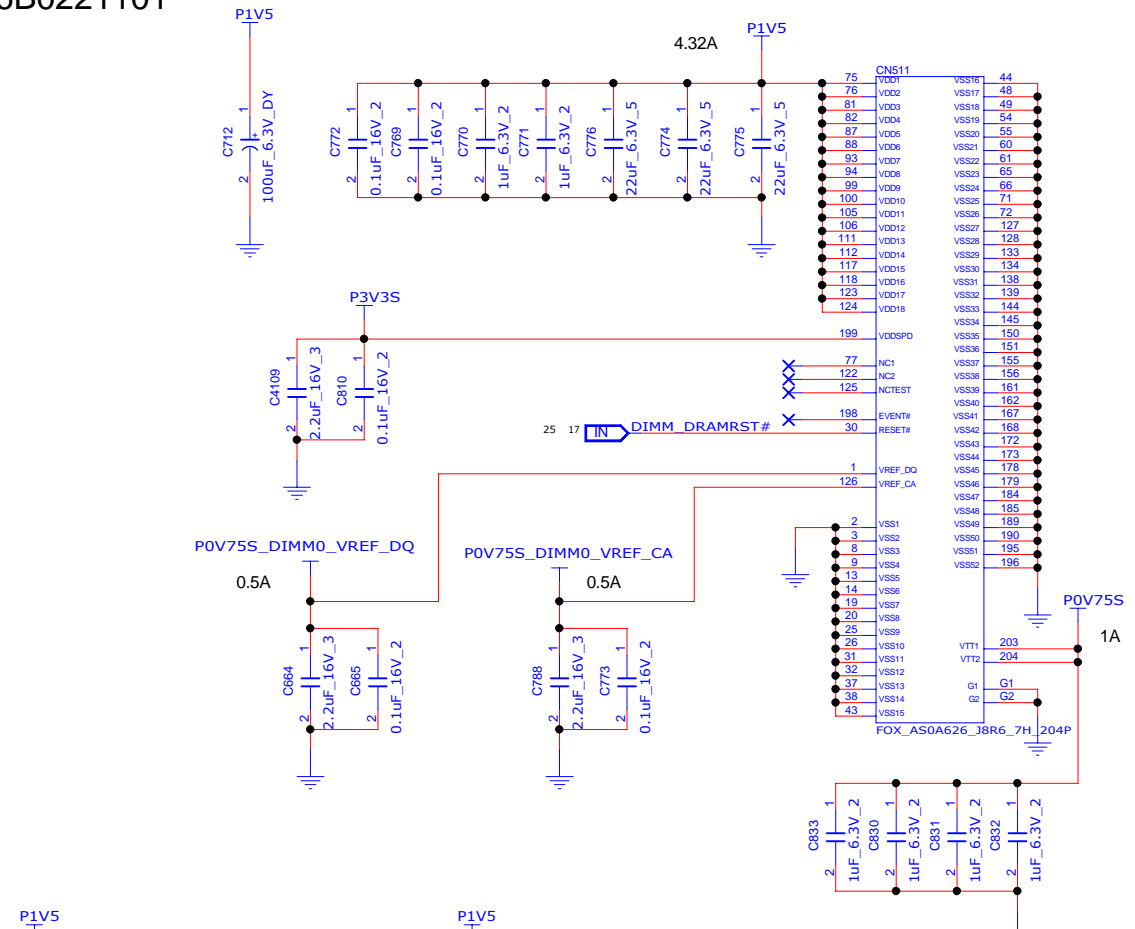
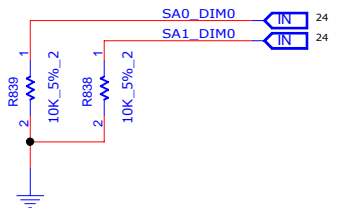
TITLE			
MODEL,PROJECT,FUNCTION			
THERMAL & FAN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 23 of 57			

DDR3 (8mm) P/N : 6026B0221101



FOX_AS0A626_J8R6_7H_204P

Note :
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

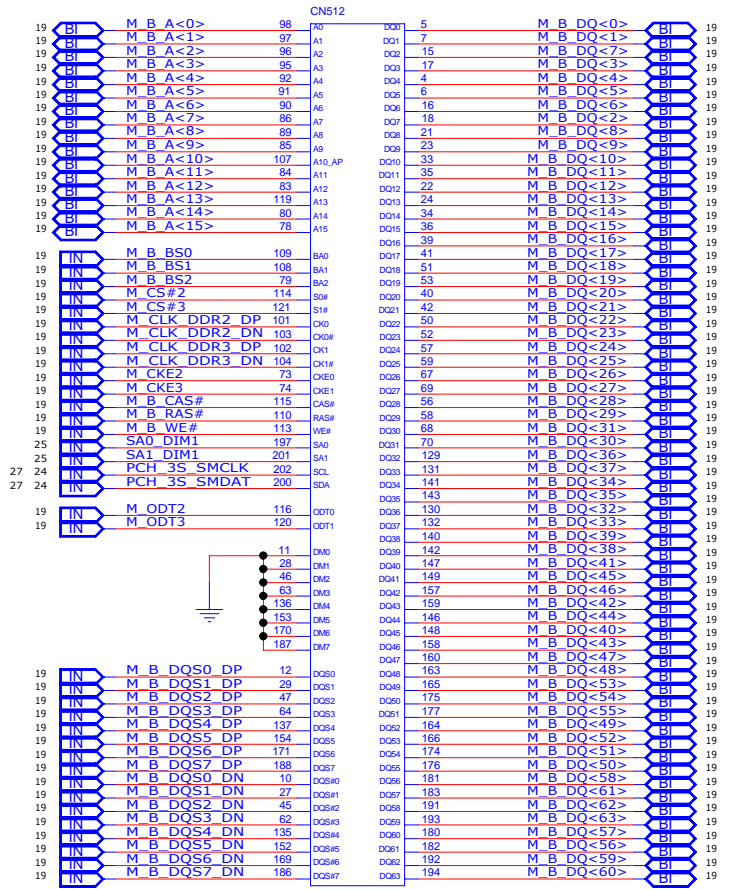


SANDY BRIDGE + IVY BRIDGE DG4.14

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
DDR3_1			
SIZE	CODE	DOCNUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXX			
DATE 21-OCT-2002			
SHEET 24 of 57			

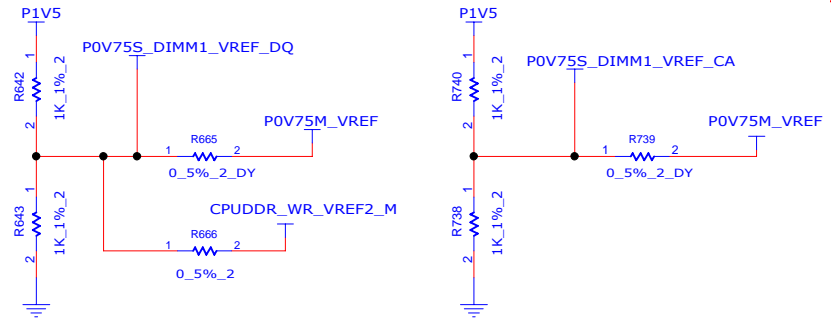
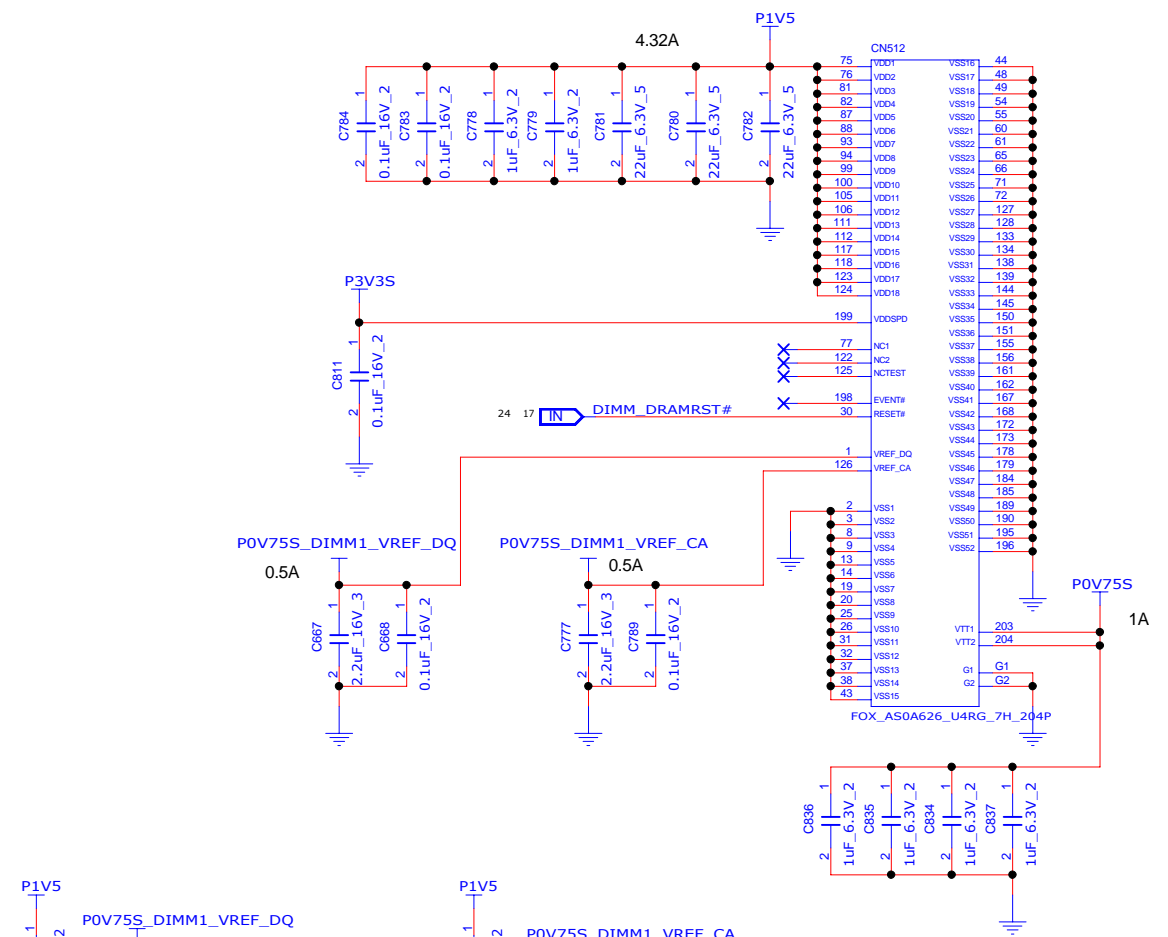
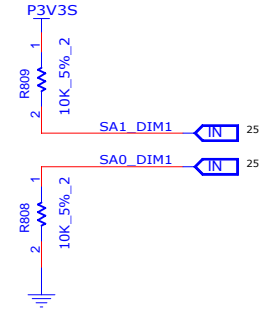
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DDR3 (4mm) P/N : 6026B0221601

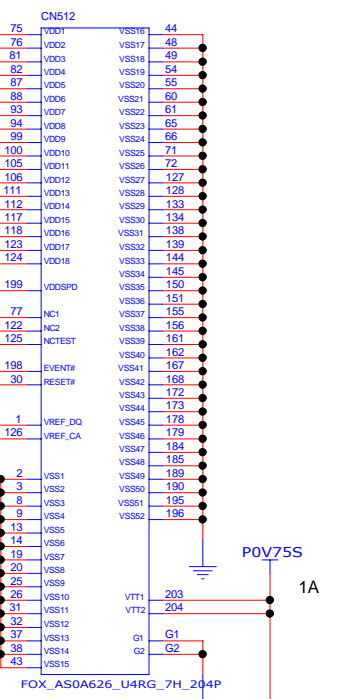


FOX_AS0A626_U4RG_7H_204P

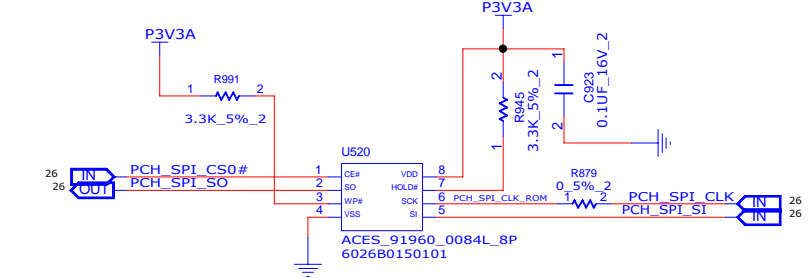
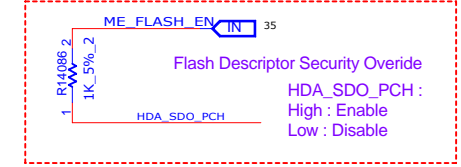
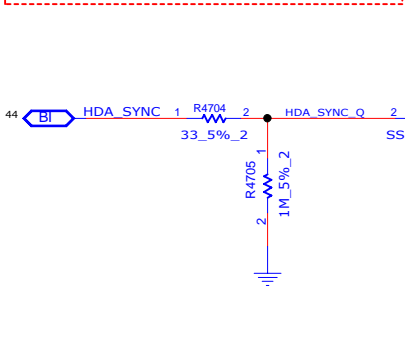
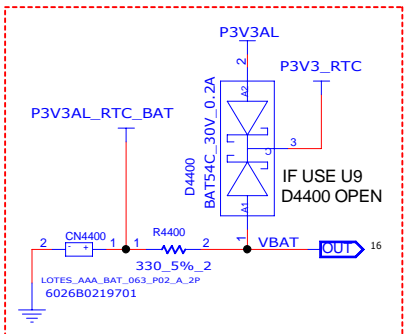
Note :
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34



SANDY BRIDGE + IVY BRIDGE DG4.14

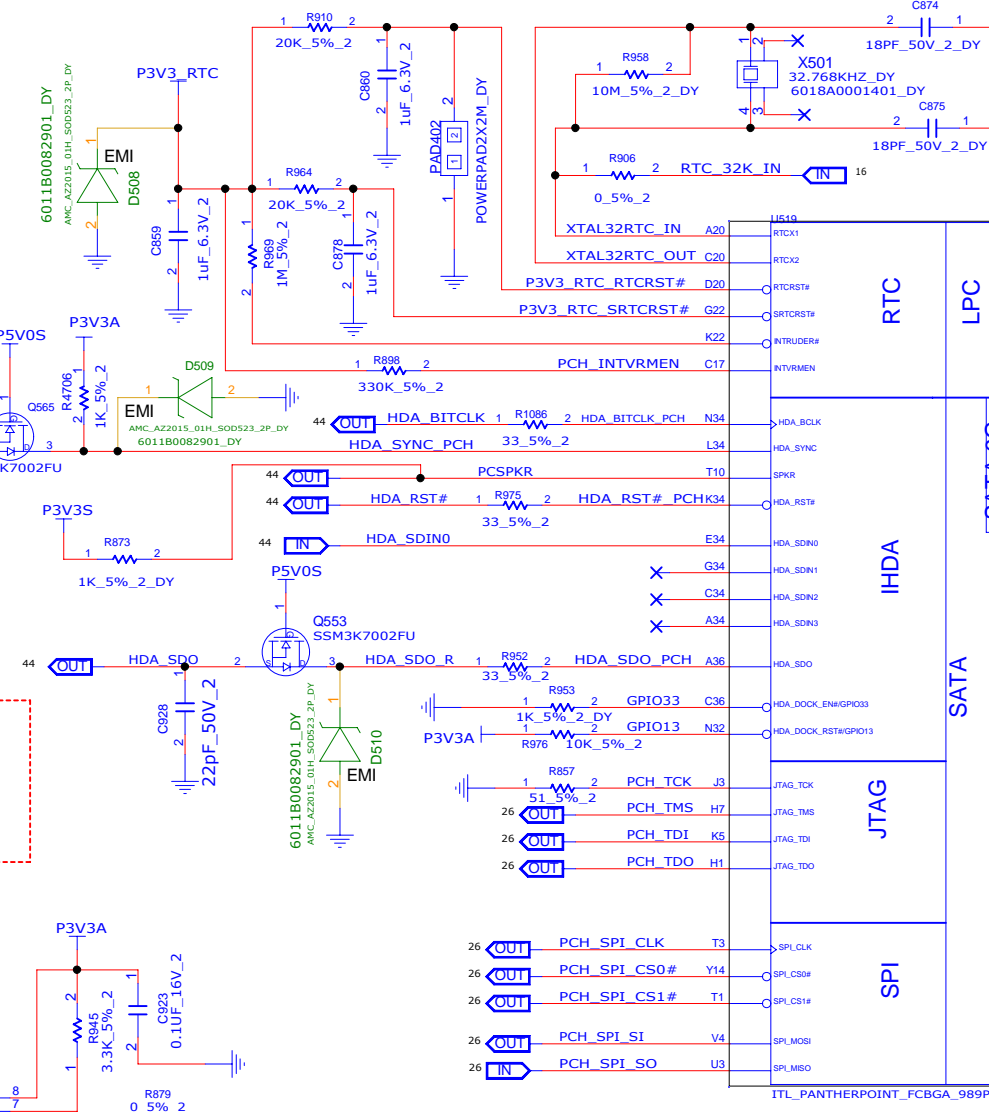


INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
DDR3			
SIZE	CODE	DOCNUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXX			
DATE 21-OCT-2002			
SHEET 25 of 57			



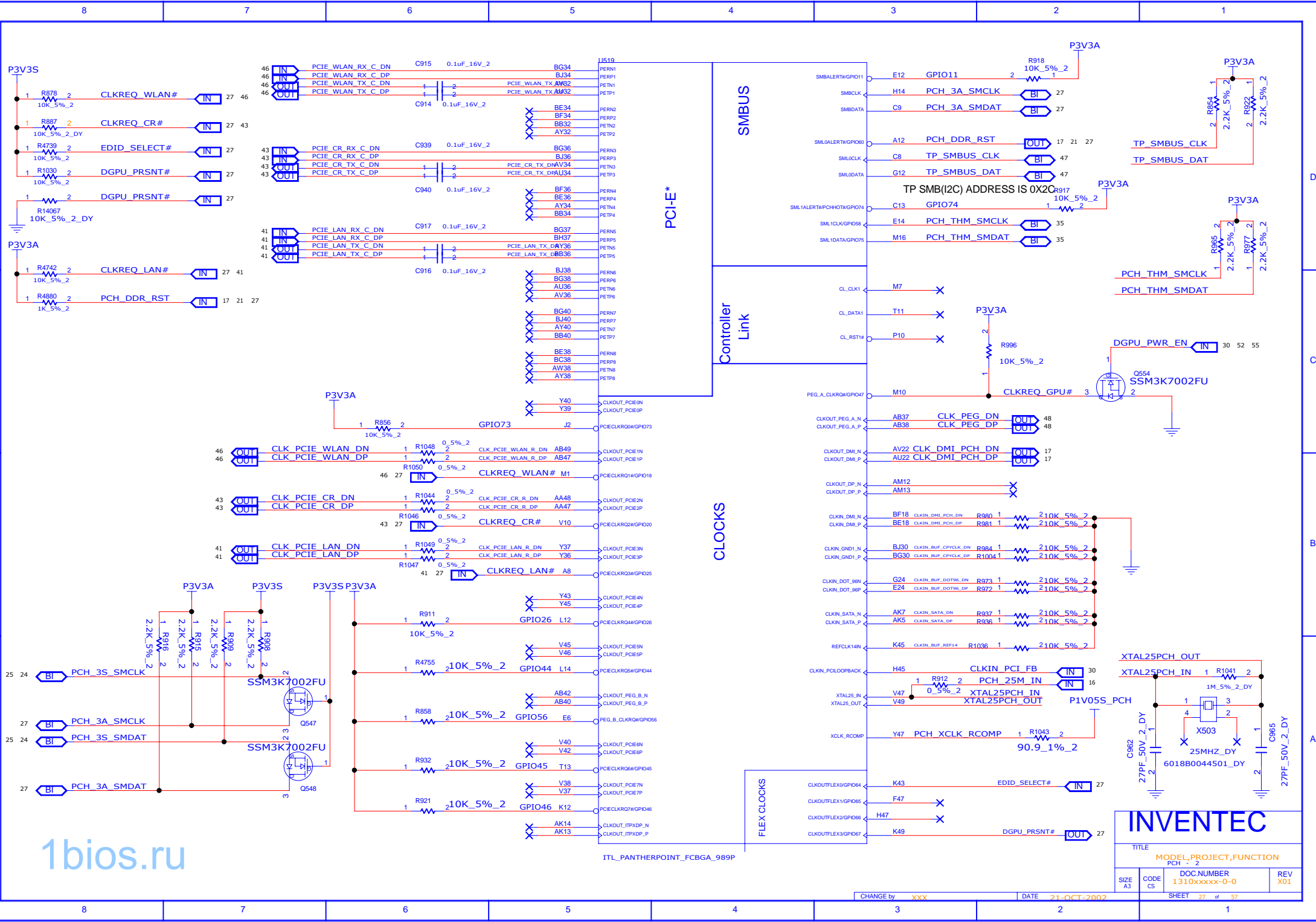
BIOS ROM 4MB (BIOS & EC ROM VENDOR MUST SAME)
 MXIC_MX25L3206EM2I-12G P/N : 6019B0794701
 WINBOND_W25Q32BVSSIG P/N : 6019B0704901

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For DB build
 HM75 QPEG Q0
 BD82PPSM
 P/N : 6019B0919101

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION			
PCH 1			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 26 of 57



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INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
PCH - 2			
SIZE A3	CODE CS	DOCNUMBER 1310xxxxx-0-0	REV X01

D

D

C

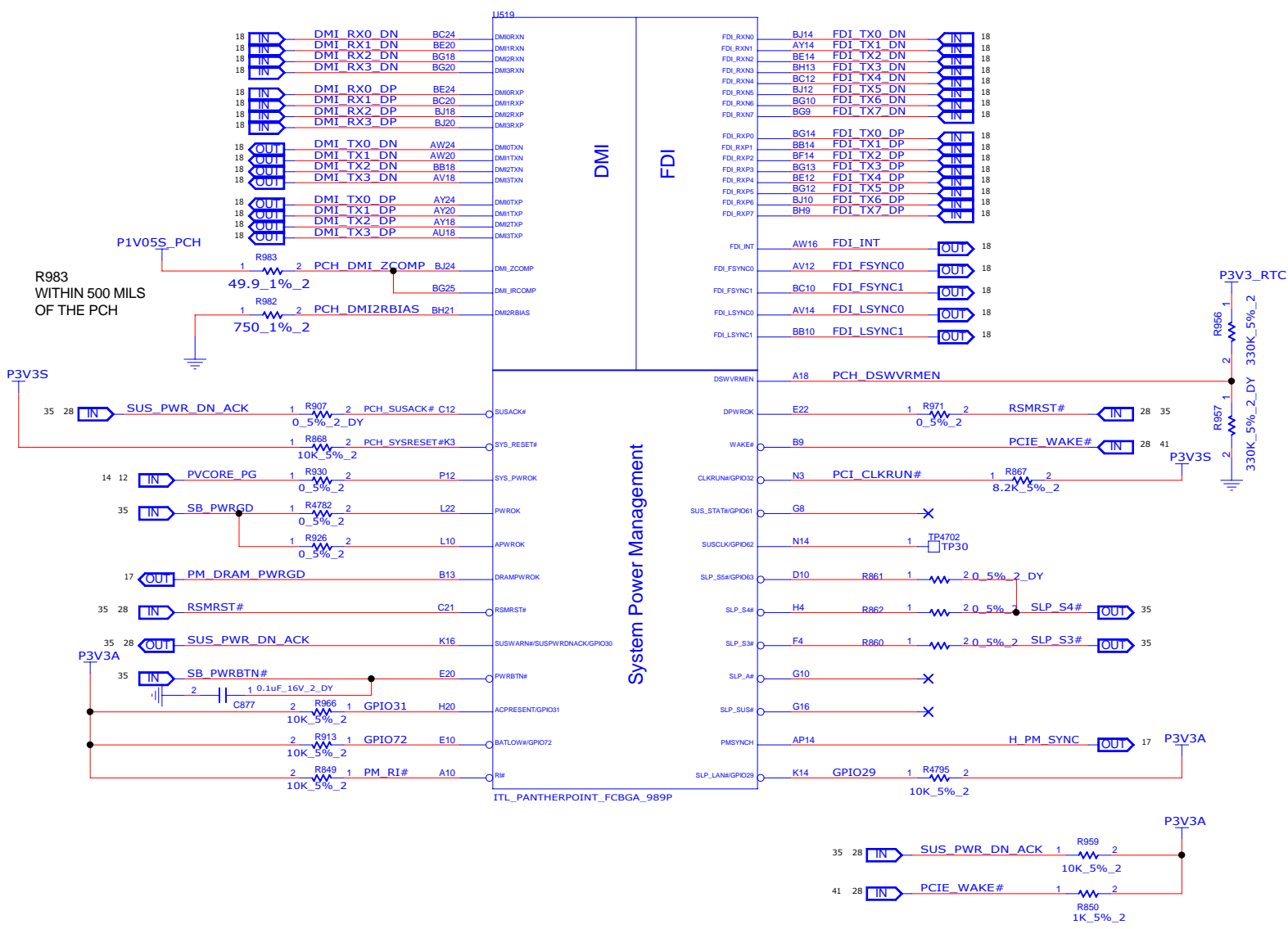
C

B

B

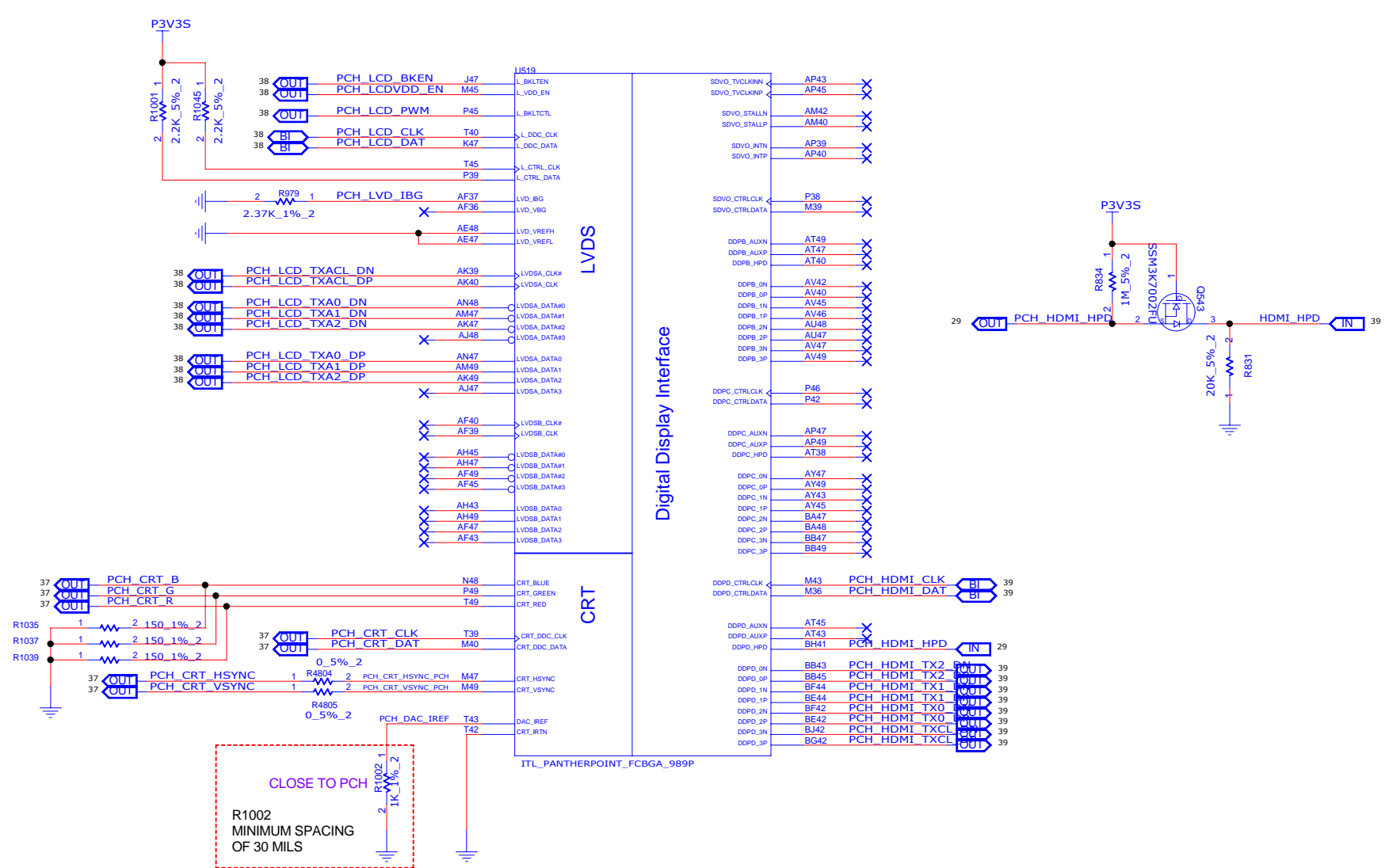
A

A



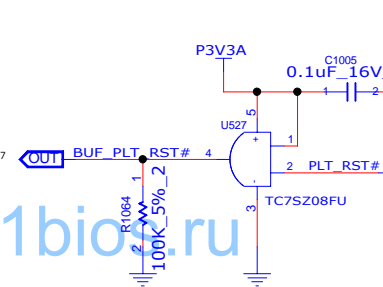
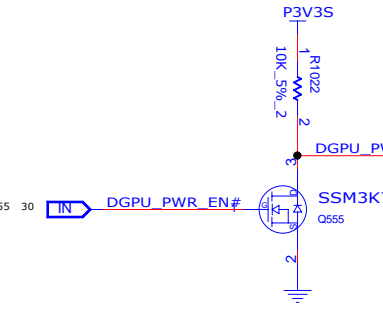
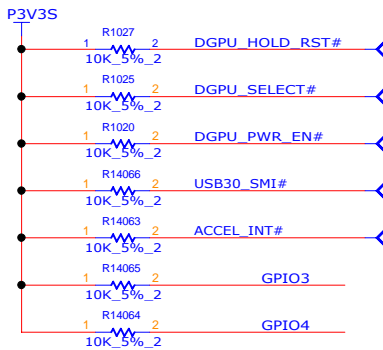
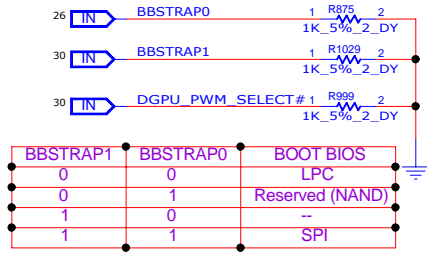
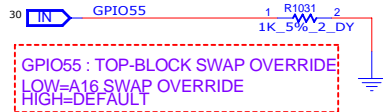
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INVENTEC			
TITLE MODEL,PROJECT,FUNCTION PCH - 3			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 28 of 57

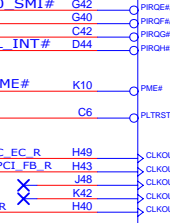
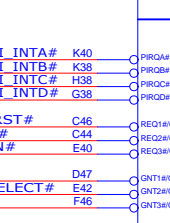
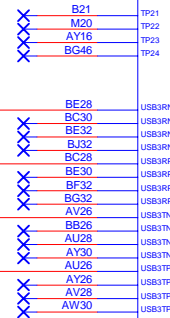
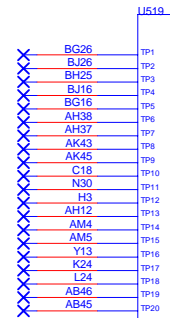


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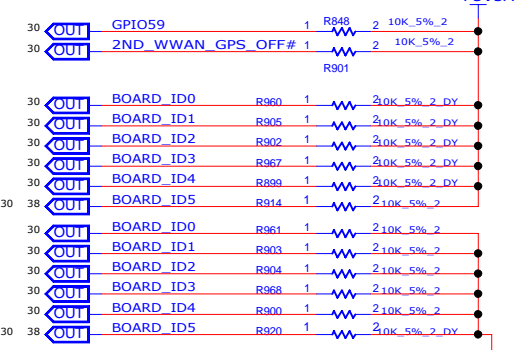
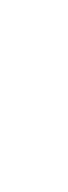
INVENTEC			
TITLE MODEL,PROJECT,FUNCTION PCH - 4			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 29 of 57



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ITL_PANTHERPOINT_FCBGA_989P



BOARD_ID5 ONLY FOR WEBCAM USE
FOR HD WEB CAM BOARD_ID5 PULL P3V3A
FOR VGA WEB CAM BOARD_ID5 PULL GND

	ID5	ID4	ID3	ID2	ID1	ID0
UMA-INTEL	1	0	0	0	0	0
SG-SEYMOUR	1	0	0	0	0	1
SG-THAMES	1	0	0	0	1	0

USB3.0
USB2.0 DB (DeBug Port)

WEBCAM

WLAN COMBO
USB2.0 DB (DeBug Port)

R951
WITHIN 500 MILS
OF THE PCH

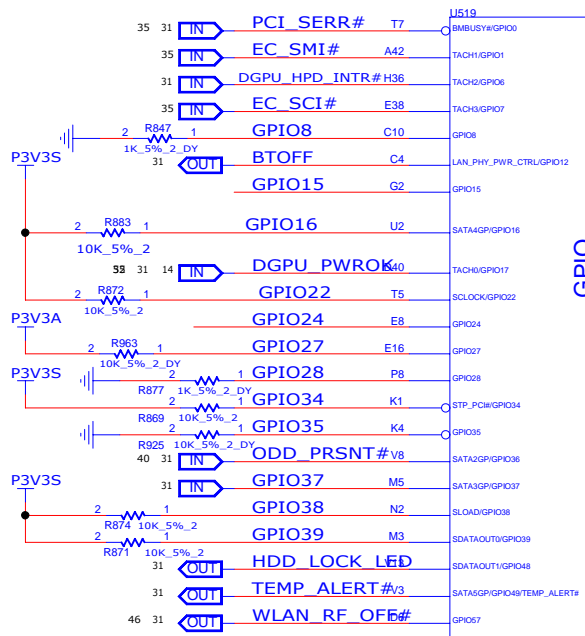
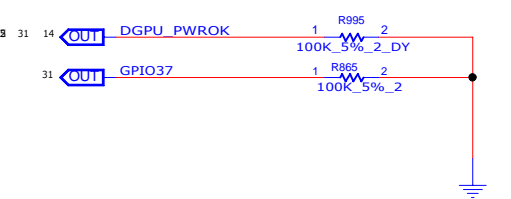
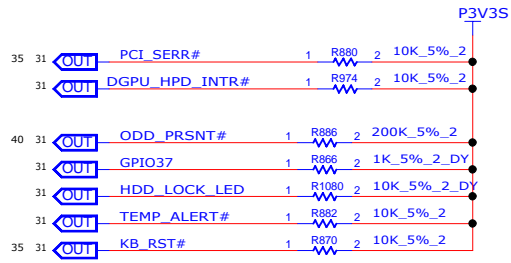
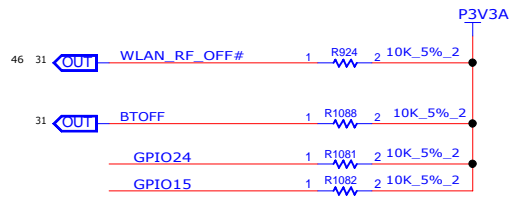


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
PCH - 5

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 30 of 57

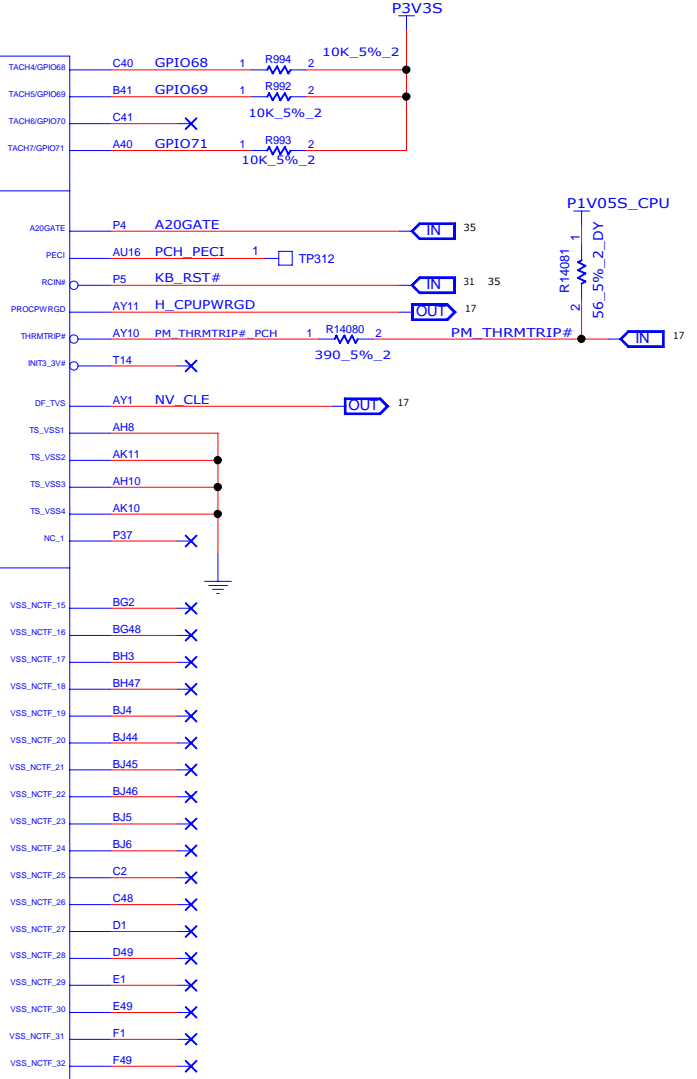


GPIO

- X A4 VSS_NCTF_1
- X A44 VSS_NCTF_2
- X A45 VSS_NCTF_3
- X A46 VSS_NCTF_4
- X A5 VSS_NCTF_5
- X A6 VSS_NCTF_6
- X B3 VSS_NCTF_7
- X B47 VSS_NCTF_8
- X BD1 VSS_NCTF_9
- X BD49 VSS_NCTF_10
- X BE1 VSS_NCTF_11
- X BE49 VSS_NCTF_12
- X BF1 VSS_NCTF_13
- X BF49 VSS_NCTF_14

NCTF

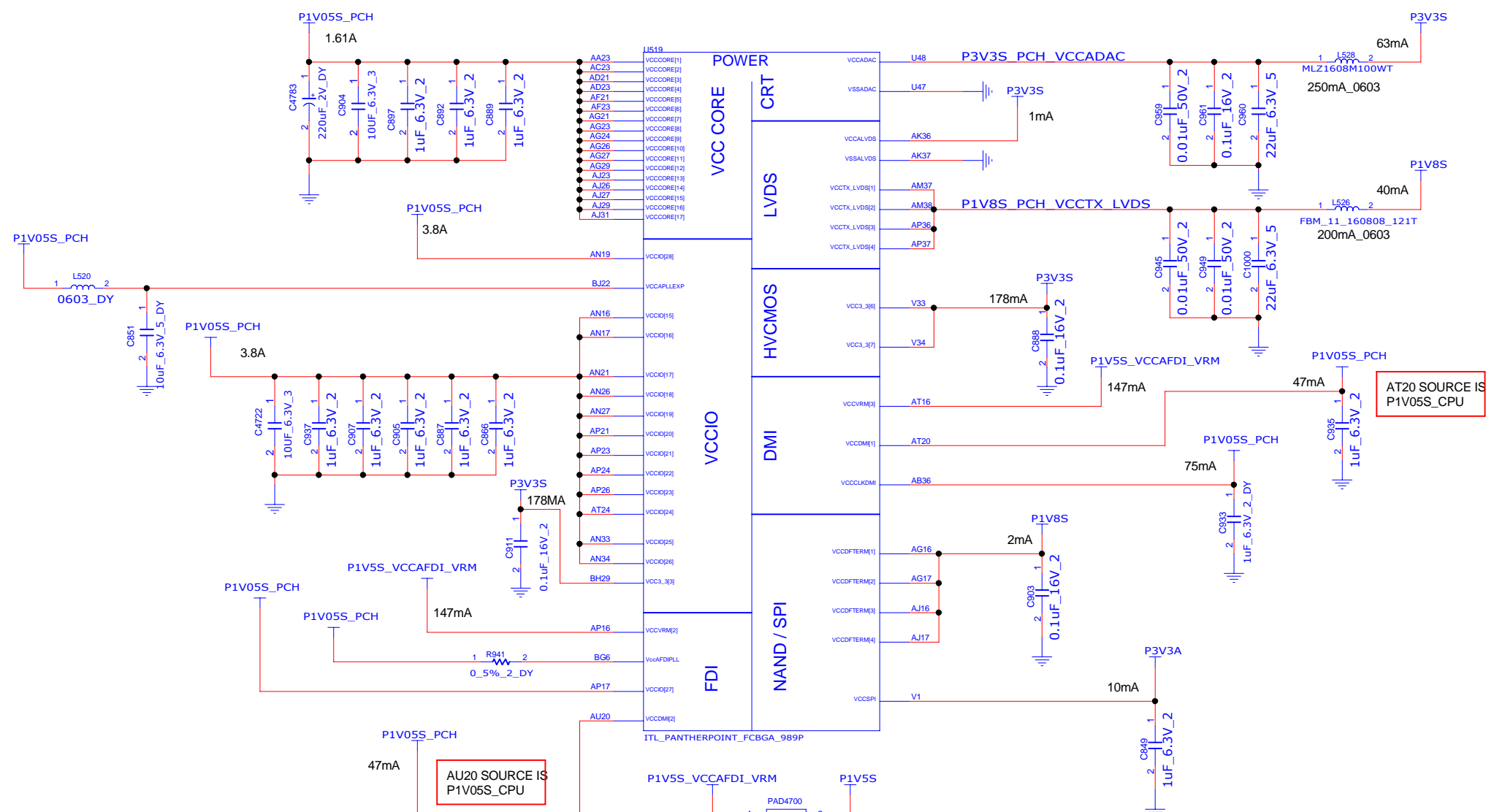
CPU/MISC



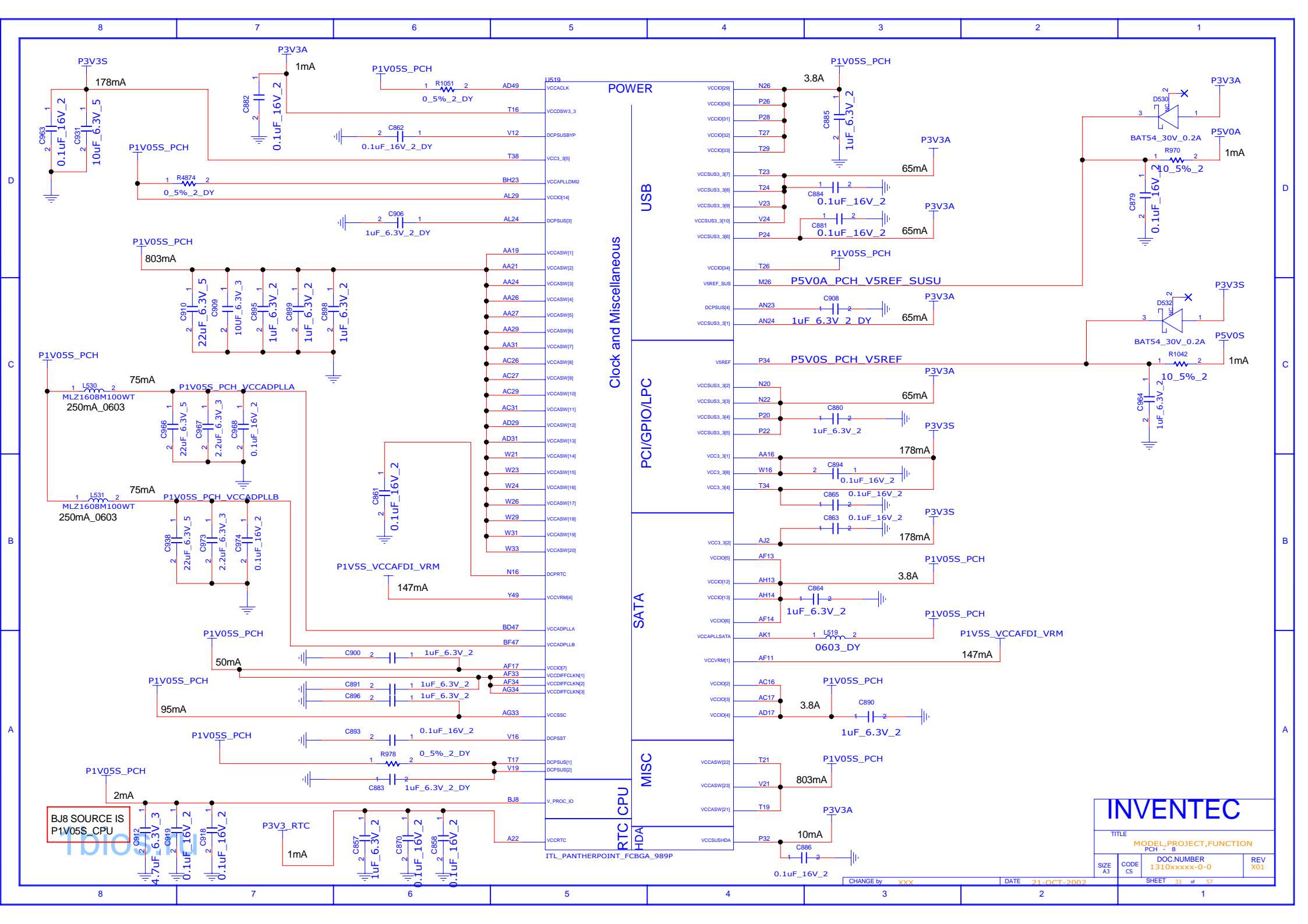
ITL_PANTHERPOINT_FCBGA_989P

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INVENTEC			
TITLE MODEL,PROJECT,FUNCTION PCH - G			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 31 of 57



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION			
PCH - 7			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 32 of 57



BJ8 SOURCE IS P1V05S_CPU

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION PCH_8			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 33 of 57

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

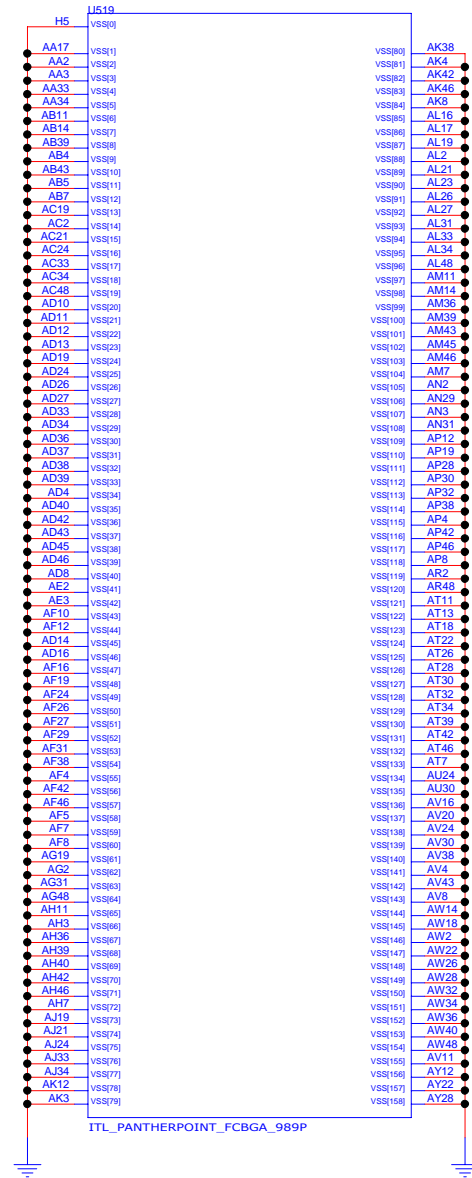
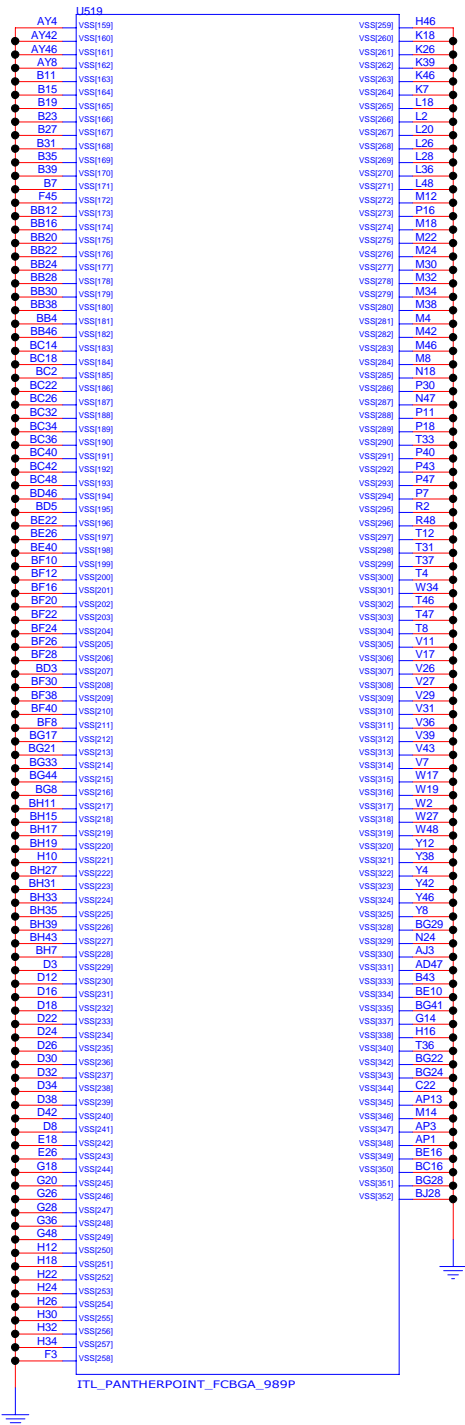
SATA

MISC

RTC CPU

HDA

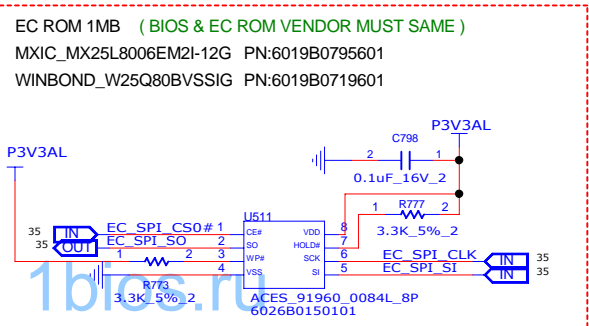
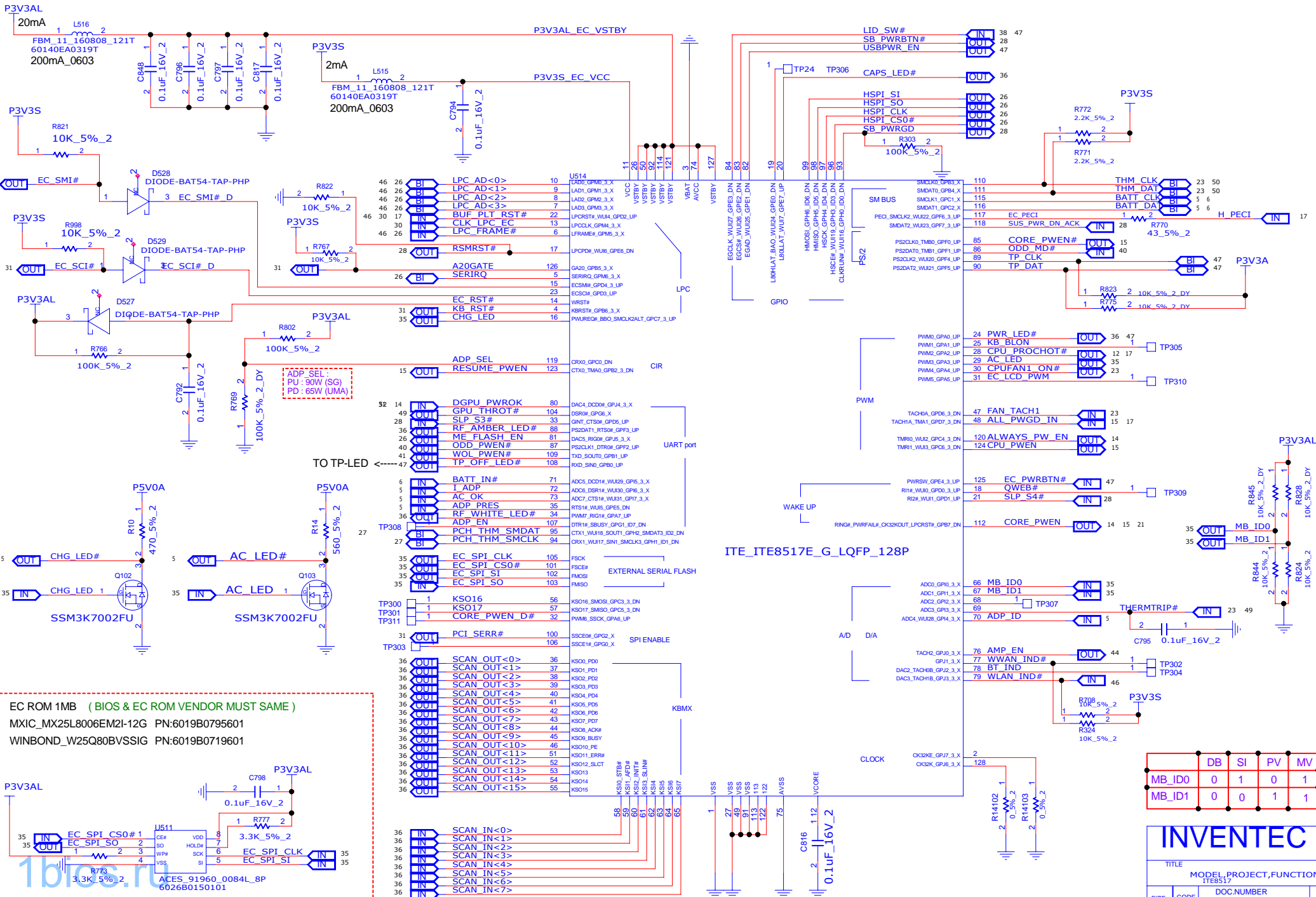
- J519 VCCADCLK
- VCCD[3:3]
- VCCD[3:0]
- VCCD[3:2]
- VCCD[3:1]
- VCCD[3:0]
- VCCSUS3_3[7]
- VCCSUS3_3[8]
- VCCSUS3_3[9]
- VCCSUS3_3[10]
- VCCSUS3_3[6]
- VCCD[3:4]
- V5REF_SUSU
- DCPSUS[4]
- VCCSUS3_3[11]
- V5REF
- VCCSUS3_3[2]
- VCCSUS3_3[3]
- VCCSUS3_3[4]
- VCCSUS3_3[5]
- VCC3_3[1]
- VCC3_3[8]
- VCC3_3[4]
- VCC3_3[2]
- VCCD[3:0]
- VCCD[1:2]
- VCCD[1:3]
- VCCD[1:0]
- VCCAPLSATA
- VCCVRM[1]
- VCCD[0:7]
- VCCDFFCLKN[1]
- VCCDFFCLKN[2]
- VCCDFFCLKN[3]
- VCCSSC
- DCPSST
- DCPSUS[1]
- DCPSUS[2]
- V_PROG_IO
- VCCRTC
- ITL_PANTHERPOINT_FCBGA_989P
- AA19 VCCASW[1]
- AA21 VCCASW[2]
- AA24 VCCASW[3]
- AA26 VCCASW[4]
- AA27 VCCASW[5]
- AA29 VCCASW[6]
- AA31 VCCASW[7]
- AC26 VCCASW[8]
- AC27 VCCASW[9]
- AC29 VCCASW[10]
- AC31 VCCASW[11]
- AD29 VCCASW[12]
- AD31 VCCASW[13]
- W21 VCCASW[14]
- W23 VCCASW[15]
- W24 VCCASW[16]
- W26 VCCASW[17]
- W29 VCCASW[18]
- W31 VCCASW[19]
- W33 VCCASW[20]
- N16 DQPRTC
- Y49 VCCVRM[4]
- BD47 VCCADPLLA
- BF47 VCCADPLB
- AF17 VCCD[0:7]
- AF33 VCCDFFCLKN[1]
- AF34 VCCDFFCLKN[2]
- AG34 VCCDFFCLKN[3]
- AG33 VCCSSC
- V16 DCPSST
- T17 DCPSUS[1]
- V19 DCPSUS[2]
- BJ8 V_PROG_IO
- A22 VCCRTC



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INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
PCH 9			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX			
DATE		21-OCT-2002	
SHEET 34 of 57			



ADP_SEL:
 PU : 90W (SG)
 PD : 65W (UMA)

ITE_ITE8517E_G_LQFP_128P

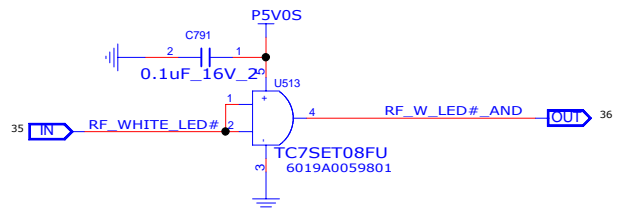
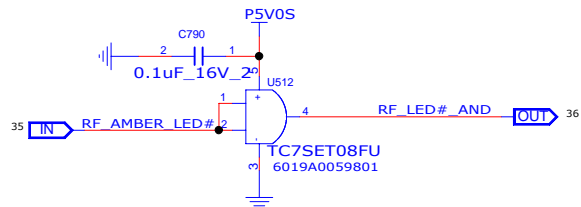
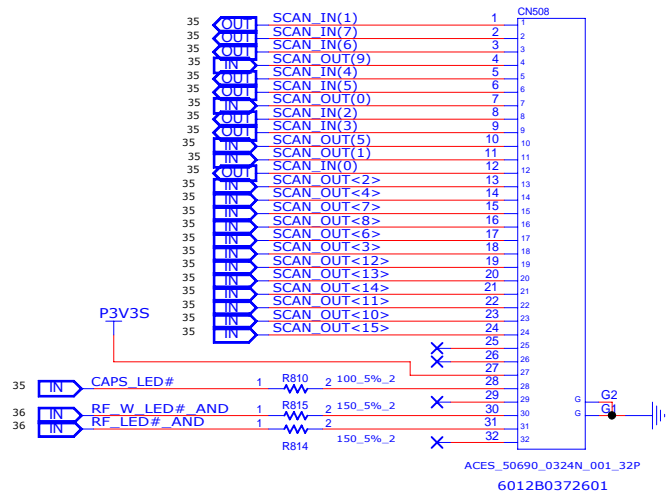
46	26	BI	LPC AD<0>	10	LD0D_GPM0_3_X	11	VCC	26	50	11	VCC	26	50
46	26	BI	LPC AD<1>	9	LAD1_GPM1_3_X	12	VSTBY	92	26	12	VSTBY	92	26
46	26	BI	LPC AD<2>	8	LAD2_GPM2_3_X	13	VSTBY	91	26	13	VSTBY	91	26
46	26	BI	LPC AD<3>	7	LAD3_GPM3_3_X	14	VSTBY	114	26	14	VSTBY	114	26
46	26	BI	BUF_PLT_RST#	22	LPCDST0_WU01_GPD3_UP	15	VSTBY	114	26	15	VSTBY	114	26
46	26	BI	CLK_LPC_EC	13	LPCDCK_GPM4_3_X	16	VSTBY	121	26	16	VSTBY	121	26
46	26	BI	LPC_FRAME#	6	LPCFRAME_GPM5_3_X	17	VSTBY	121	26	17	VSTBY	121	26
28	OUT	BI	RSMRST#	17	LPCDPO_WU01_GPE6_DN	18	VBAT	3	74	18	VBAT	3	74
26	BI	BI	A20GATE	126	GA01_GPB5_3_X	19	AVCC	127	26	19	AVCC	127	26
31	OUT	BI	SERIRQ	5	SERIRQ_GPM6_3_X	20	VSTBY	127	26	20	VSTBY	127	26
35	OUT	BI	KB_RST#	15	ECSMH_GPD4_3_UP	21	VSTBY	127	26	21	VSTBY	127	26
35	OUT	BI	KB_RST#	23	ECSMH_GPD3_UP	22	VSTBY	127	26	22	VSTBY	127	26
35	OUT	BI	CHG_LED	16	PWUREQ_W_B00_SMCCLKALT_GPC7_3_UP	23	VSTBY	127	26	23	VSTBY	127	26
31	OUT	BI	ADP_SEL	119	CRX0_GPC0_DN	24	VSTBY	127	26	24	VSTBY	127	26
31	OUT	BI	RESUME_PWEN	123	CTX0_TMA0_GPB2_3_DN	25	VSTBY	127	26	25	VSTBY	127	26
52	14	IN	DGPU PWROK	80	DAC4_DCD0H_GPH4_3_X	26	VSTBY	127	26	26	VSTBY	127	26
49	IN	IN	GPU THROT#	104	DSR0H_GPG6_X	27	VSTBY	127	26	27	VSTBY	127	26
28	IN	IN	SLP_S3#	33	GINT_CTS0H_GPD6_UP	28	VSTBY	127	26	28	VSTBY	127	26
36	IN	IN	RF_AMBER_LED#	88	PS2DAT1_RTS0H_GPP3_UP	29	VSTBY	127	26	29	VSTBY	127	26
26	IN	IN	ME_FLASH_EN	81	DACS_RIG0H_GPB_3_X	30	VSTBY	127	26	30	VSTBY	127	26
40	IN	IN	ODD_PWEN#	87	PS2CK1_DTR0H_GPP2_UP	31	VSTBY	127	26	31	VSTBY	127	26
41	IN	IN	WOL_PWEN#	109	TXD_SOUT0_GPB1_UP	32	VSTBY	127	26	32	VSTBY	127	26
47	IN	IN	TP_OFF_LED#	108	RXD_SIND_GPB0_UP	33	VSTBY	127	26	33	VSTBY	127	26
6	IN	IN	BATT_IN#	71	ADCS_DCD1H_WU29_GPB_3_X	34	VSTBY	127	26	34	VSTBY	127	26
5	IN	IN	AC ADP	72	ADCS_DSR1H_WU30_GPB_3_X	35	VSTBY	127	26	35	VSTBY	127	26
5	IN	IN	AC OK	73	ADCT_CTS1H_WU31_GPP_3_X	36	VSTBY	127	26	36	VSTBY	127	26
5	IN	IN	ADP PRES	35	RTS1H_WU15_GPE6_DN	37	VSTBY	127	26	37	VSTBY	127	26
36	IN	IN	RF_WHITE_LED#	34	PWM7_RIG1H_GPA7_UP	38	VSTBY	127	26	38	VSTBY	127	26
36	IN	IN	ADP_EN	107	DTR1H_SBUSY_GPG1_ID7_DN	39	VSTBY	127	26	39	VSTBY	127	26
27	BI	BI	PCH_THM_SMDAT	95	CTX1_WU18_SOUT1_GPH2_SMDAT3_ID2_DN	40	VSTBY	127	26	40	VSTBY	127	26
27	BI	BI	PCH_THM_SMCCLK	94	CRX1_WU17_SIN1_SMCCLK_GPH1_ID1_DN	41	VSTBY	127	26	41	VSTBY	127	26
35	OUT	BI	EC SPI CLK	105	FSCK	42	VSTBY	127	26	42	VSTBY	127	26
35	OUT	BI	EC SPI CS0#	101	FSCE#	43	VSTBY	127	26	43	VSTBY	127	26
35	OUT	BI	EC SPI SI	102	FMOSI	44	VSTBY	127	26	44	VSTBY	127	26
35	OUT	BI	EC SPI SO	103	FMISO	45	VSTBY	127	26	45	VSTBY	127	26
TP300	1	IN	KSO16	56	KS016_SMO3H_GPC3_3_DN	46	VSTBY	127	26	46	VSTBY	127	26
TP301	1	IN	KSO17	57	KS017_SMO3H_GPC3_3_DN	47	VSTBY	127	26	47	VSTBY	127	26
TP311	1	IN	CORE_PWEN_D#	32	PWM6_S5CK_GPA6_UP	48	VSTBY	127	26	48	VSTBY	127	26
TP303	1	OUT	PCI_SERR#	100	SSCED0H_GPC2_X	49	VSTBY	127	26	49	VSTBY	127	26
36	OUT	BI	SCAN_OUT<0>	36	SSCE1H_GPC0_X	50	VSTBY	127	26	50	VSTBY	127	26
36	OUT	BI	SCAN_OUT<1>	37	KS01_P03	51	VSTBY	127	26	51	VSTBY	127	26
36	OUT	BI	SCAN_OUT<2>	38	KS02_P01	52	VSTBY	127	26	52	VSTBY	127	26
36	OUT	BI	SCAN_OUT<3>	39	KS02_P02	53	VSTBY	127	26	53	VSTBY	127	26
36	OUT	BI	SCAN_OUT<4>	40	KS03_P03	54	VSTBY	127	26	54	VSTBY	127	26
36	OUT	BI	SCAN_OUT<5>	41	KS03_P04	55	VSTBY	127	26	55	VSTBY	127	26
36	OUT	BI	SCAN_OUT<6>	42	KS04_P05	56	VSTBY	127	26	56	VSTBY	127	26
36	OUT	BI	SCAN_OUT<7>	43	KS04_P06	57	VSTBY	127	26	57	VSTBY	127	26
36	OUT	BI	SCAN_OUT<8>	44	KS05_P07	58	VSTBY	127	26	58	VSTBY	127	26
36	OUT	BI	SCAN_OUT<9>	45	KS05_ADP6	59	VSTBY	127	26	59	VSTBY	127	26
36	OUT	BI	SCAN_OUT<10>	46	KS06_BUSY	60	VSTBY	127	26	60	VSTBY	127	26
36	OUT	BI	SCAN_OUT<11>	51	KS010_PE	61	VSTBY	127	26	61	VSTBY	127	26
36	OUT	BI	SCAN_OUT<12>	52	KS011_ERRR	62	VSTBY	127	26	62	VSTBY	127	26
36	OUT	BI	SCAN_OUT<13>	53	KS012_SLCT	63	VSTBY	127	26	63	VSTBY	127	26
36	OUT	BI	SCAN_OUT<14>	54	KS013	64	VSTBY	127	26	64	VSTBY	127	26
36	OUT	BI	SCAN_OUT<15>	55	KS014	65	VSTBY	127	26	65	VSTBY	127	26
36	OUT	BI	SCAN_IN<0>	56	KS015	66	VSTBY	127	26	66	VSTBY	127	26
36	OUT	BI	SCAN_IN<1>	57	KS016	67	VSTBY	127	26	67	VSTBY	127	26
36	OUT	BI	SCAN_IN<2>	58	KS017	68	VSTBY	127	26	68	VSTBY	127	26
36	OUT	BI	SCAN_IN<3>	59	KS018	69	VSTBY	127	26	69	VSTBY	127	26
36	OUT	BI	SCAN_IN<4>	60	KS019	70	VSTBY	127	26	70	VSTBY	127	26
36	OUT	BI	SCAN_IN<5>	61	KS020	71	VSTBY	127	26	71	VSTBY	127	26
36	OUT	BI	SCAN_IN<6>	62	KS021	72	VSTBY	127	26	72	VSTBY	127	26
36	OUT	BI	SCAN_IN<7>	63	KS022	73	VSTBY	127	26	73	VSTBY	127	26
36	OUT	BI	SCAN_IN<8>	64	KS023	74	VSTBY	127	26	74	VSTBY	127	26
36	OUT	BI	SCAN_IN<9>	65	KS024	75	VSTBY	127	26	75	VSTBY	127	26

	DB	SI	PV	MV
MB_ID0	0	1	0	1
MB_ID1	0	0	1	1

INVENTEC

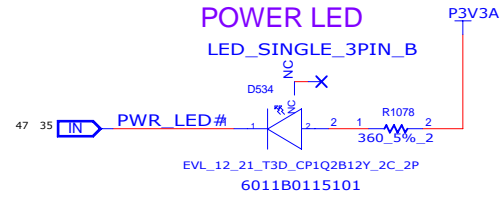
TITLE		MODEL,PROJECT,FUNCTION	
ITE8517		1310xxxxx-0-0	
SIZE A3	CODE CS	DOC NUMBER	REV X01
		1310xxxxx-0-0	

KeyBoard CONN(30 pin)

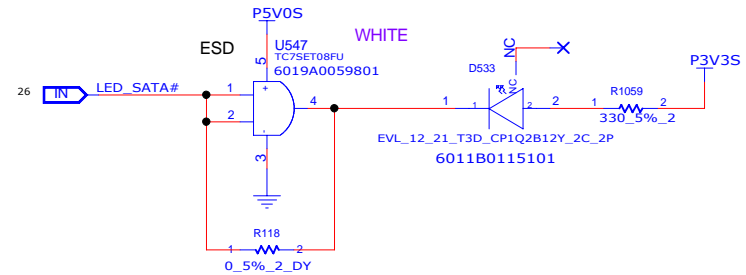


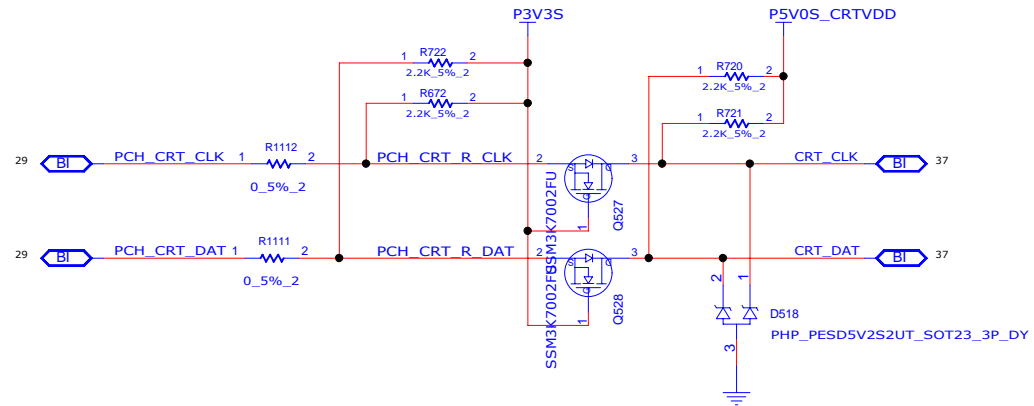
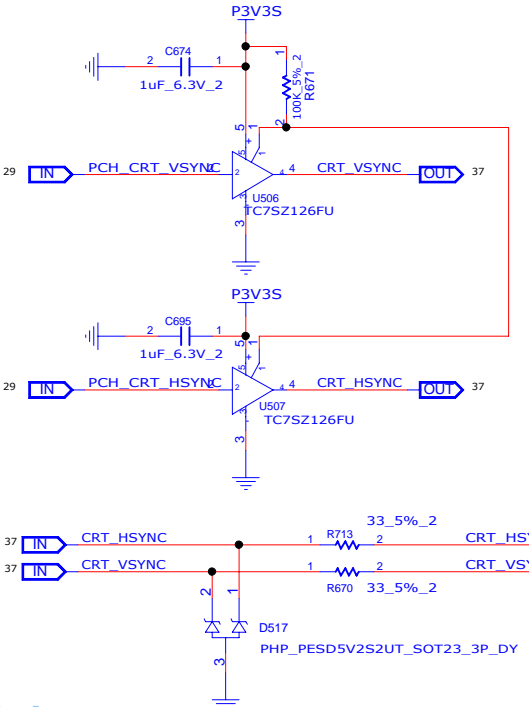
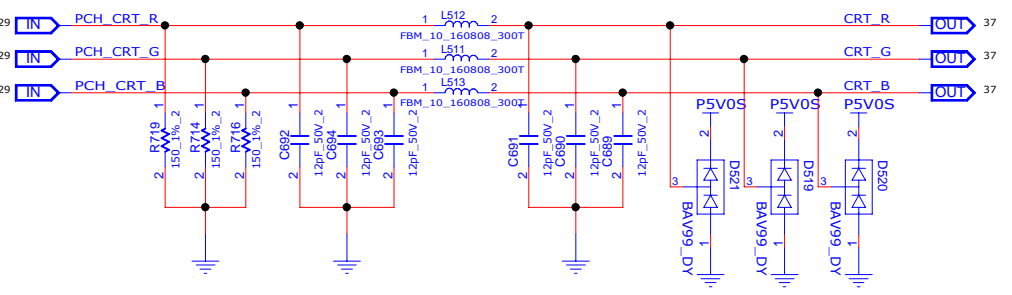
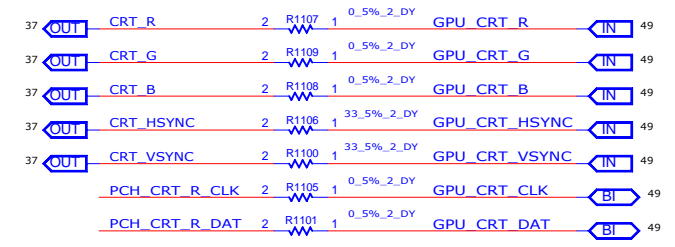
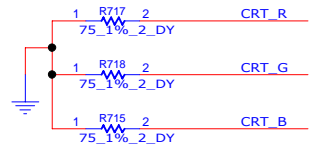
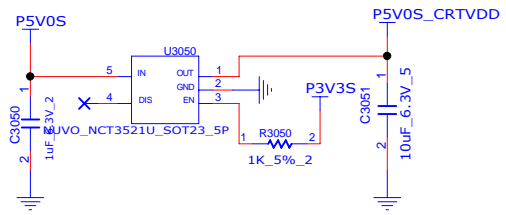
POWER LED

LED_SINGLE_3PIN_B

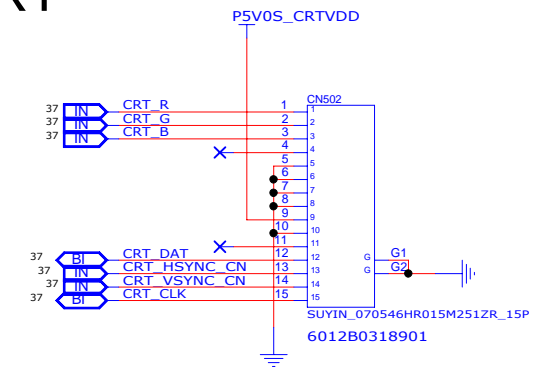


SATA LED & HDD HALTED LED





CRT

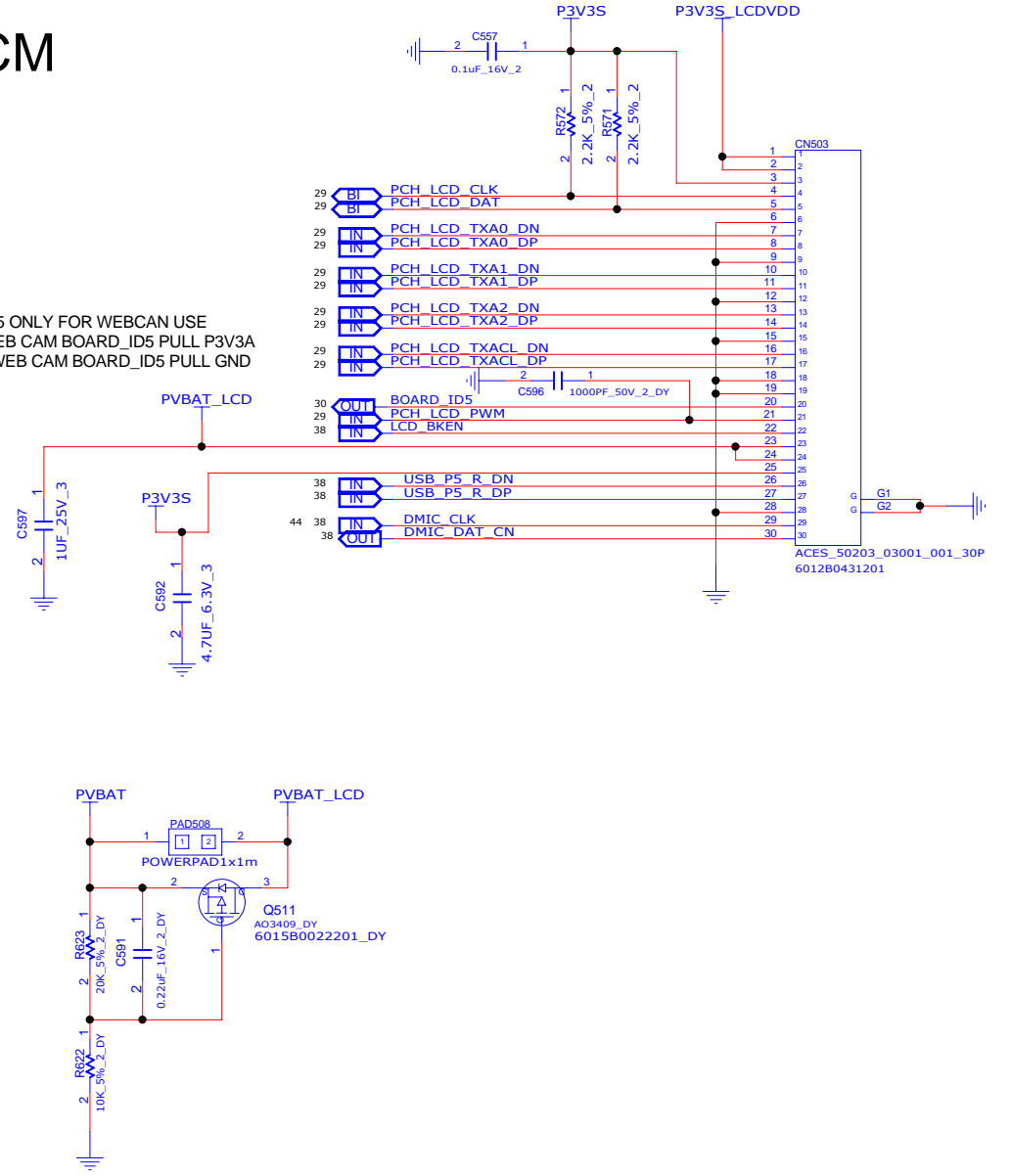
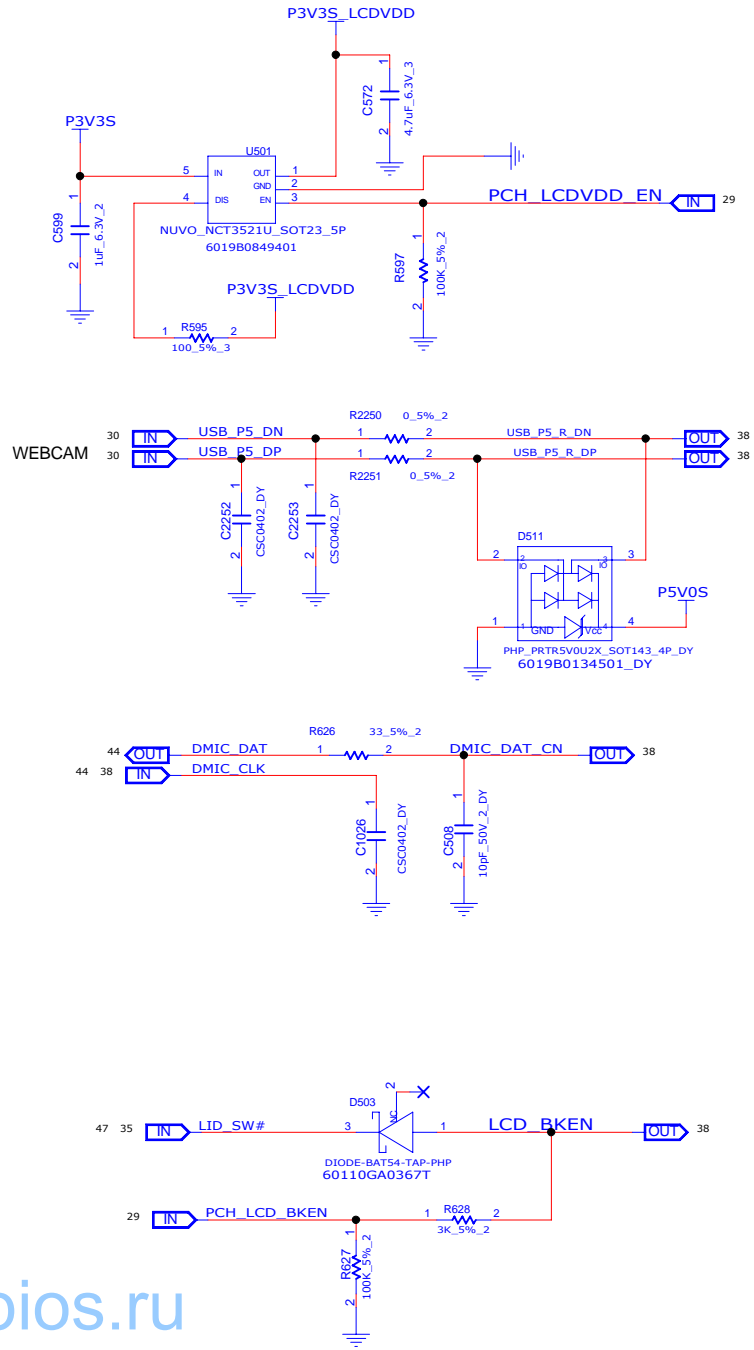


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INVENTEC			
TITLE MODEL,PROJECT,FUNCTION			
SIZE A3		CODE CS	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 37 of 57

LCM

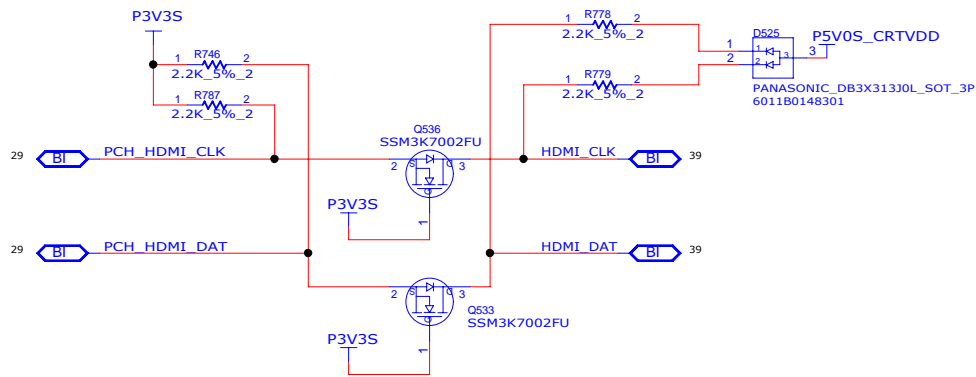
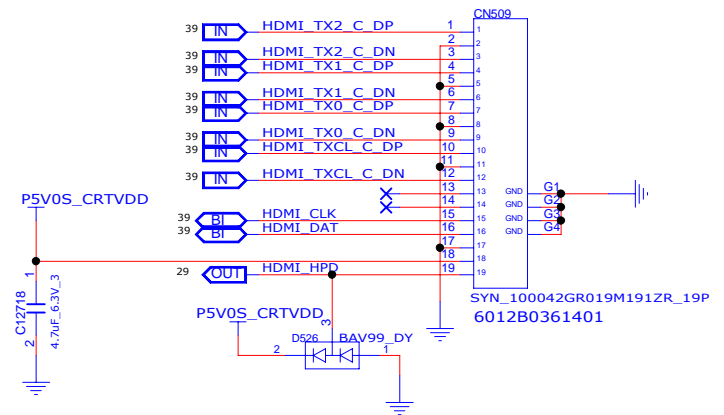
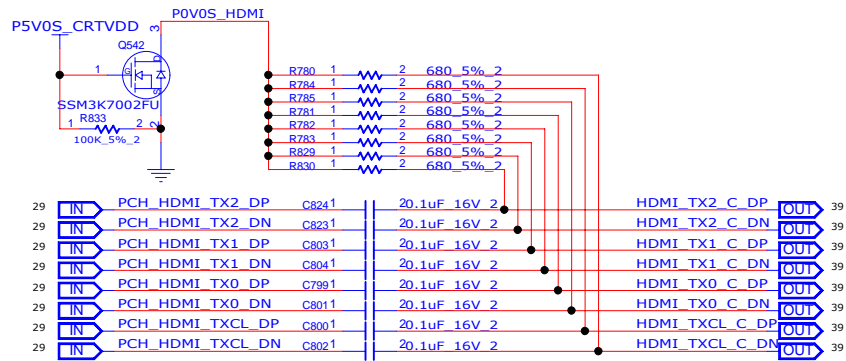
BOARD_ID5 ONLY FOR WEBCAM USE
 FOR HD WEB CAM BOARD_ID5 PULL P3V3VA
 FOR VGA WEB CAM BOARD_ID5 PULL GND



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INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
SIZE A3		CODE CS	
DOC NUMBER		REV	
1310xxxxx-0-0		X01	
SHEET 38 of 57			

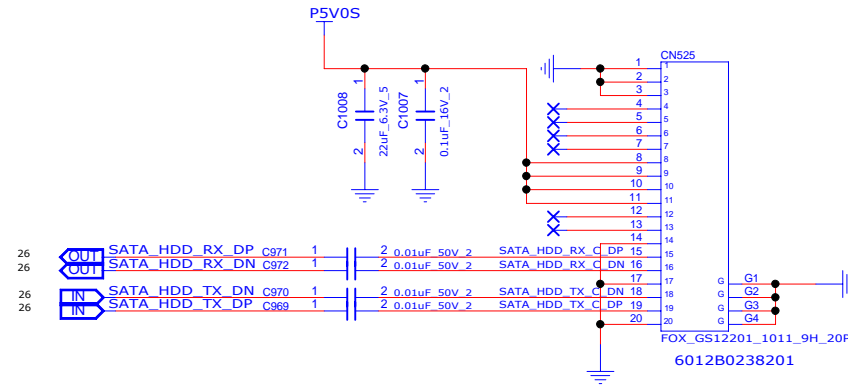
HDMI



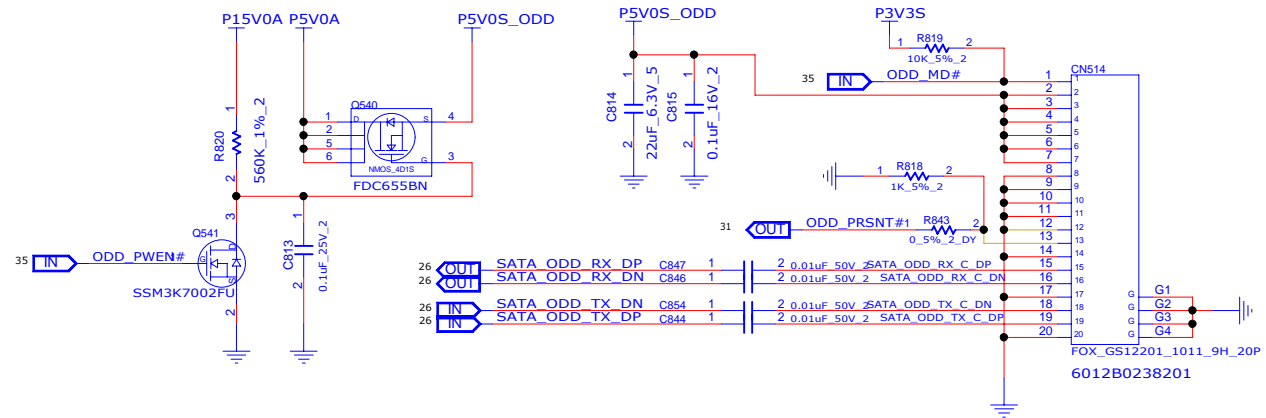
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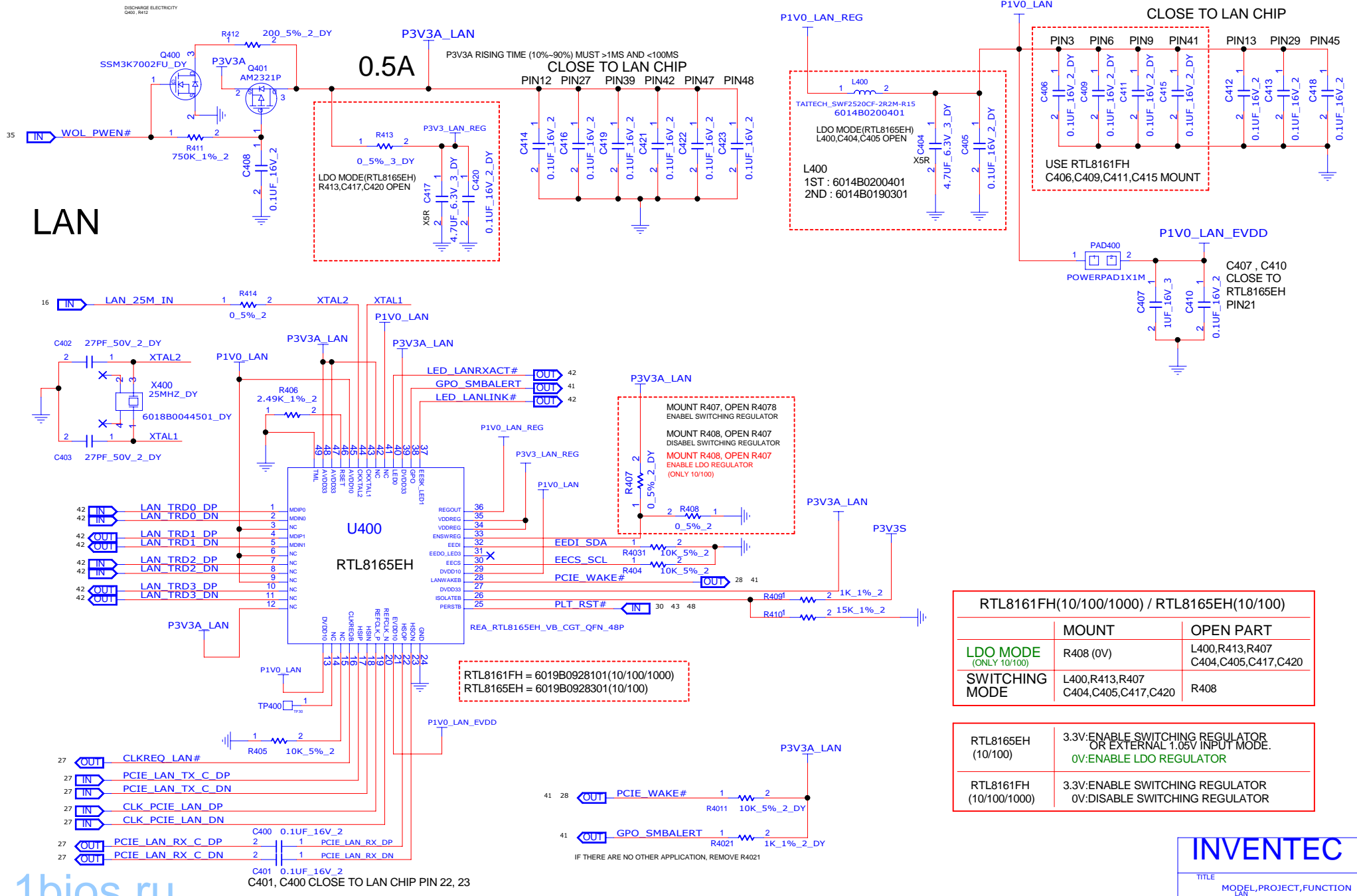
INVENTEC			
TITLE MODEL, PROJECT, FUNCTION HDMI_CONN			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 39 of 57

SATA HDD CABLE CONN on MB



SATA ODD CABLE CONN on MB





LAN

RTL8161FH(10/100/1000) / RTL8165EH(10/100)

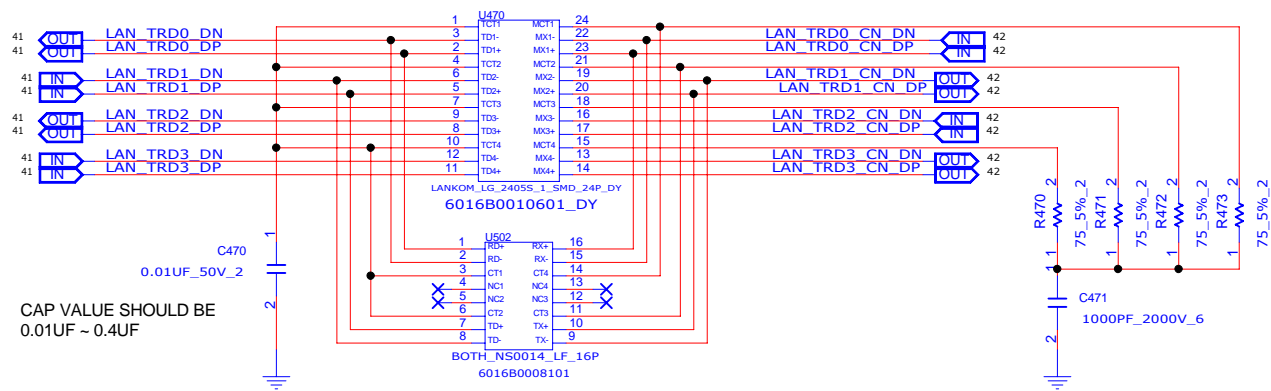
	MOUNT	OPEN PART
LDO MODE (ONLY 10/100)	R408 (0V)	L400,R413,R407 C404,C405,C417,C420
SWITCHING MODE	L400,R413,R407 C404,C405,C417,C420	R408

RTL8165EH (10/100)	3.3V:ENABLE SWITCHING REGULATOR OR EXTERNAL 1.05V INPUT MODE. 0V:ENABLE LDO REGULATOR
RTL8161FH (10/100/1000)	3.3V:ENABLE SWITCHING REGULATOR 0V:DISABLE SWITCHING REGULATOR

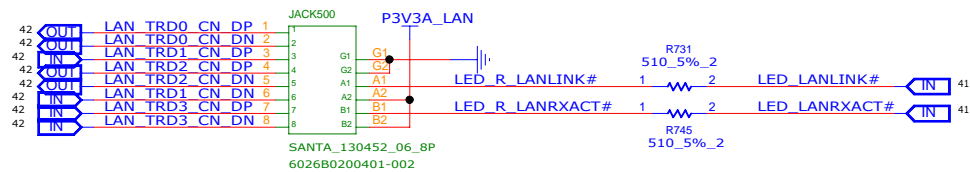
RTL8161FH = 6019B0928101(10/100/1000)
 RTL8165EH = 6019B0928301(10/100)

TRANSFORMER

U470 FOR GIGALAN
U502 FOR 10/100 LAN

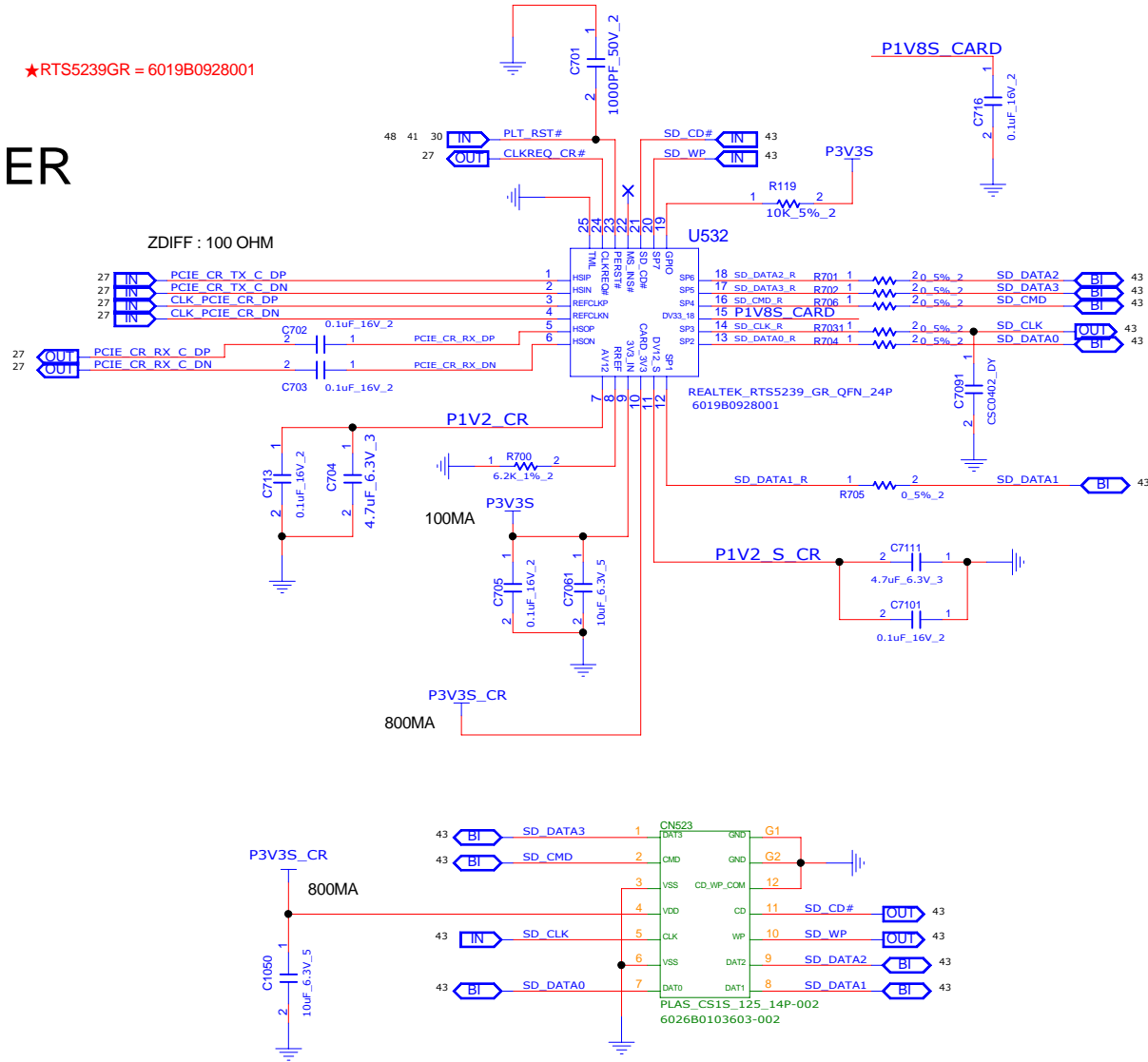


CAP VALUE SHOULD BE
0.01UF - 0.4UF



CARE READER

★RTS5239GR = 6019B0928001

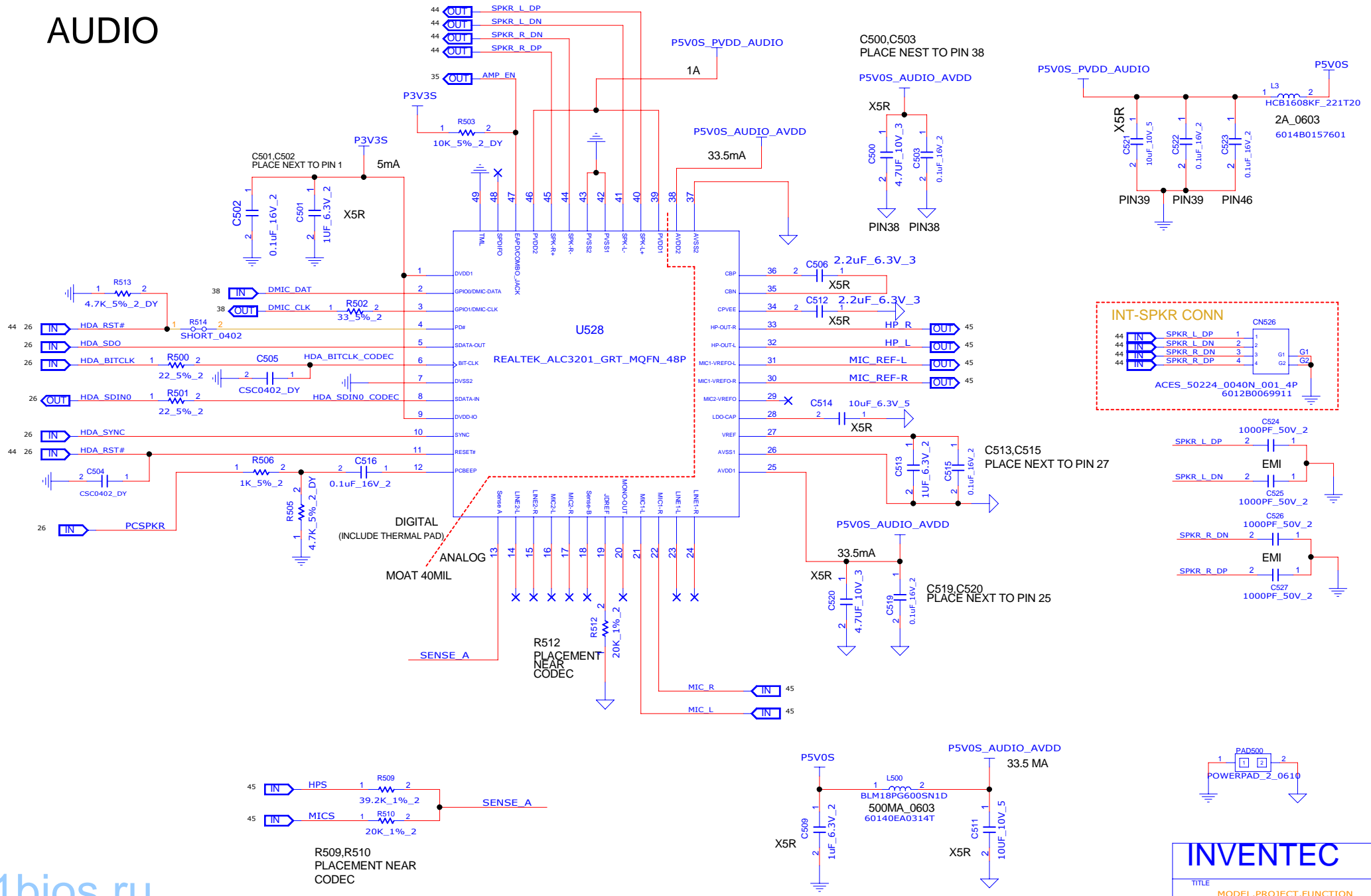


1 ■ On chip 800ma MOSFET for direct power control of all types memory cards

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
CARD READER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 43 of 57			

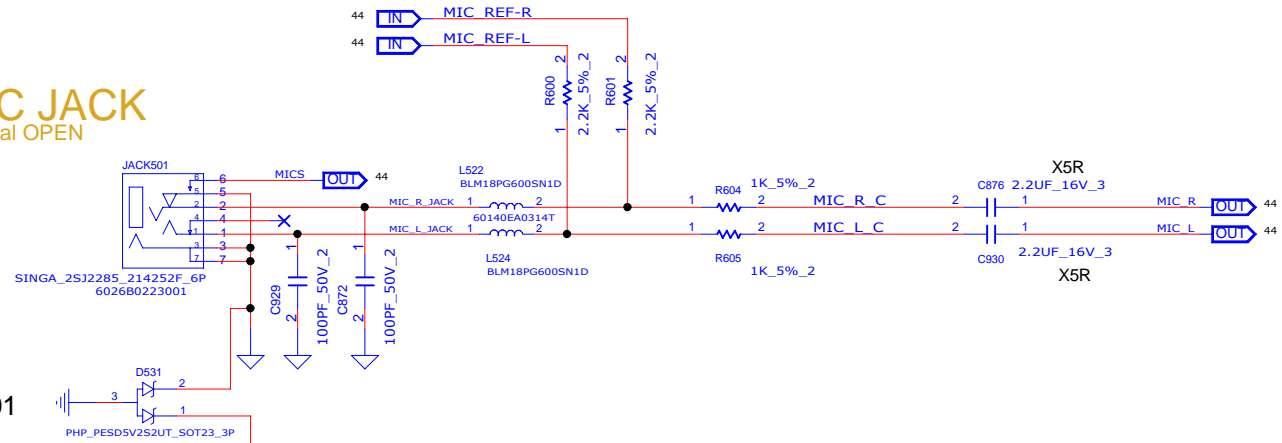
AUDIO



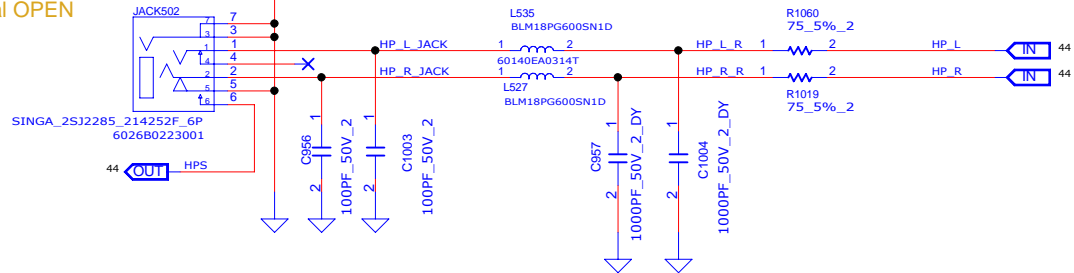
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INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
DOC NUMBER			
SIZE A3	CODE CS	1310xxxxx-0-0	REV X01
SHEET 44 of 57			

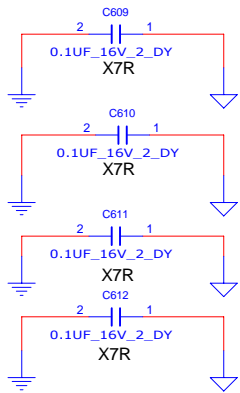
MIC JACK Normal OPEN



HP JACK Normal OPEN



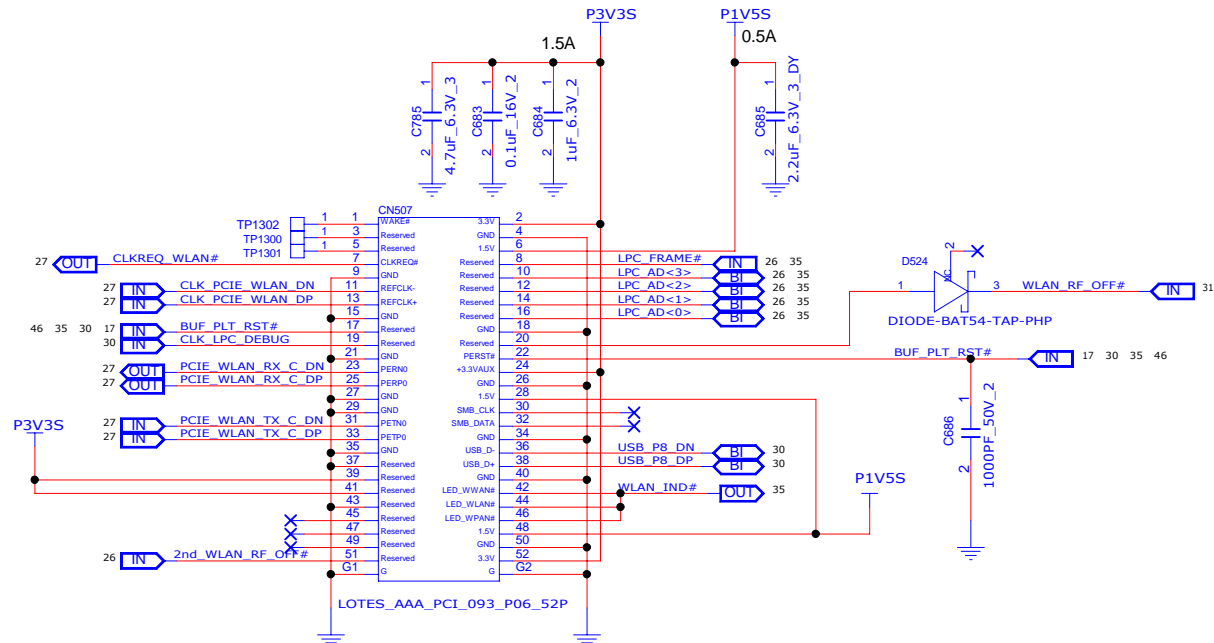
JACK CHANGE TO 6026B0223001



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INVENTEC			
TITLE MODEL,PROJECT,FUNCTION HP JACK & MIC JACK			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 45 of 57

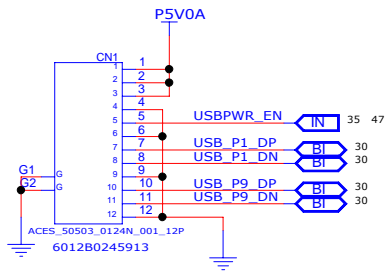
WLAN CONN (MINICARD)



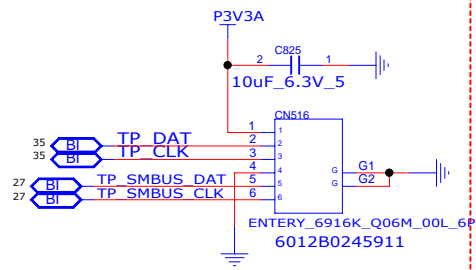
SI build change to 6026B0221502

MARILYN	RIPPLE3
ATHEROS	FOXCONN
AR5B125	RALINK RT5390
VENDOR ID : 0X168C	0X1814
DEVICE ID : 0X0032	0X539A
(SSID) SUBSYSTEM ID : 0X1838	0X1839
SUBSYSTEM VENDOR ID : 0X103C	0X103C
HP P/N : 670036-001	670285-001

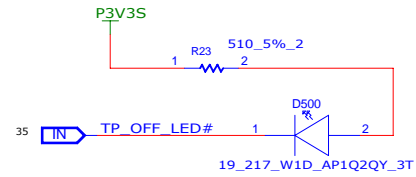
USB 2.0 BOARD Cable CONN on MB



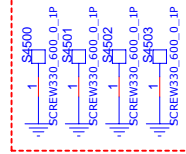
TouchPad Module CONN



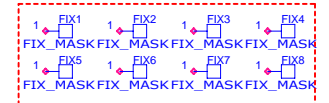
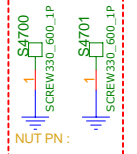
TOUCHPAD LED ON MB



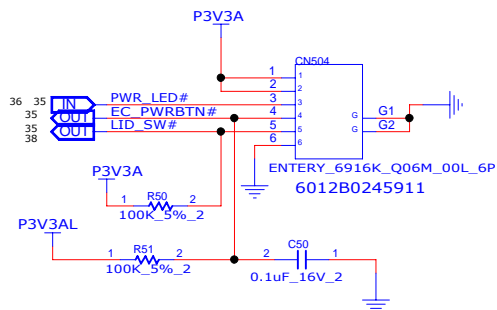
for CPU



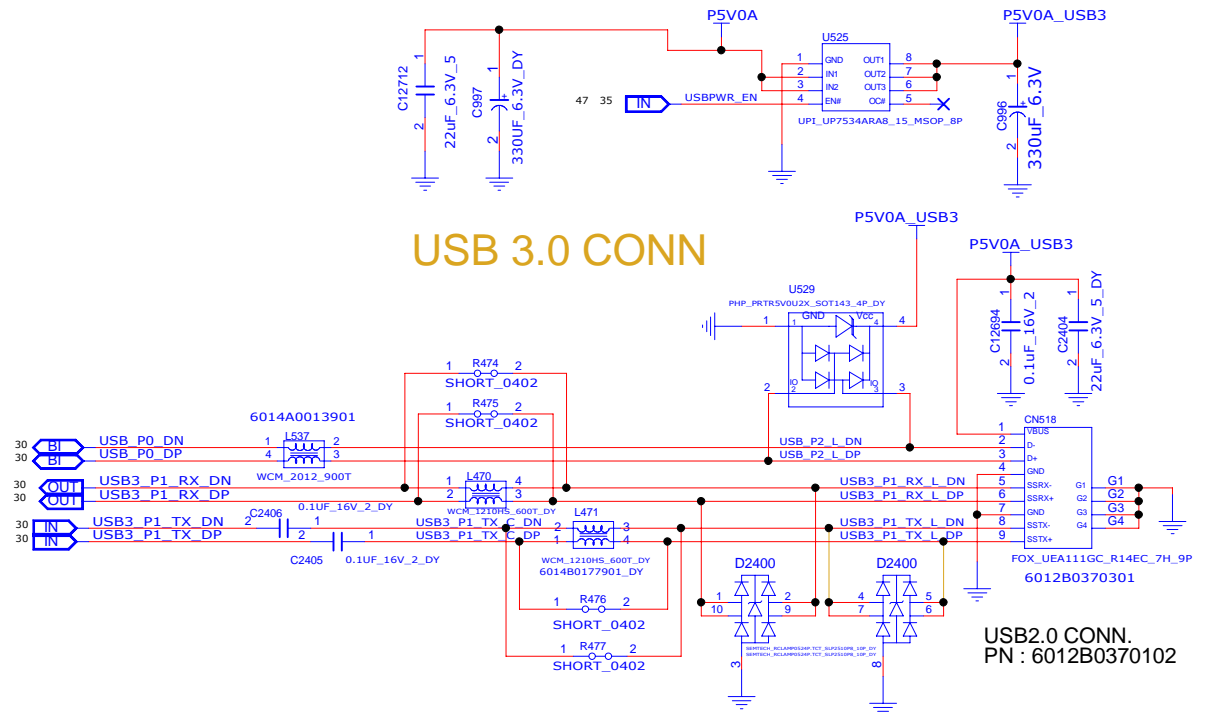
for GPU



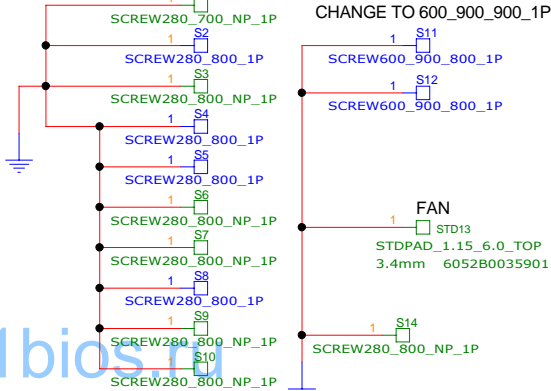
POWER BUTTON CONN ON MB



USB 3.0 CONN

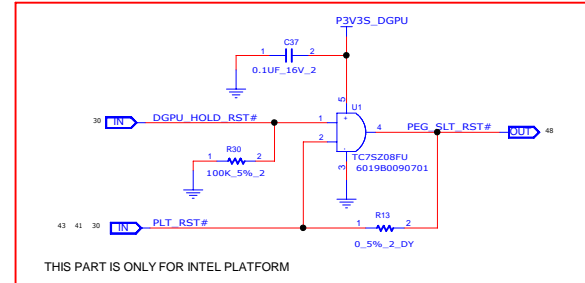
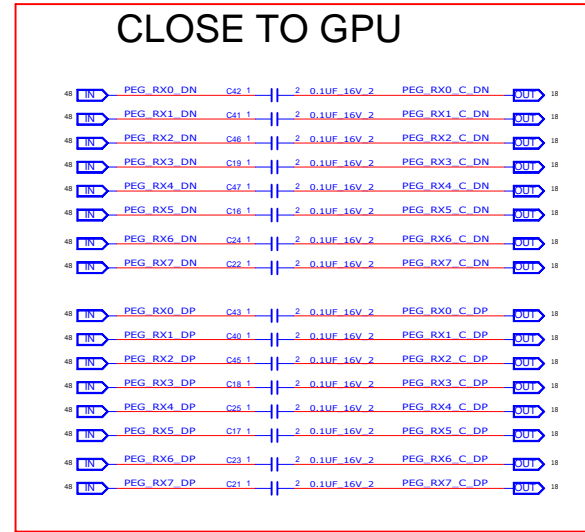
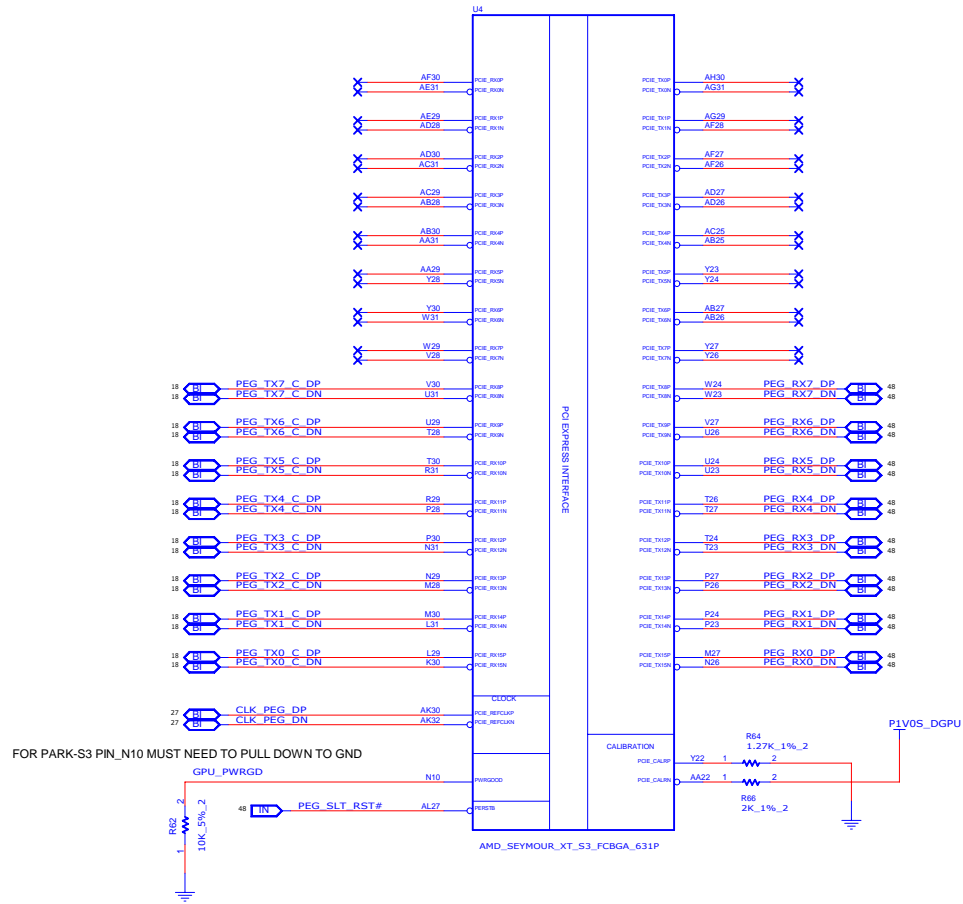


FOR M/B



INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
USB 3.0 CONN & M/B TO D/B CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01



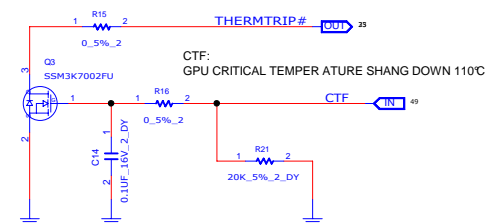
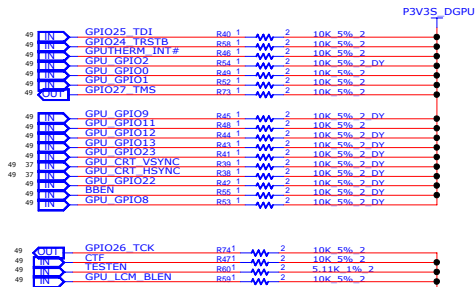
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	2Gb * 4 = 1GB
0	0	0	0	SAMSUNG C-DIE K4W2G1646C-HC11
0	0	0	1	HYNIX D-DIE H5TQ2G63DFR-11C
0	0	1	0	MICRON MT41J128M16HA-107G-D
0	0	1	1	

128M * 16 * 4
128M * 16 * 4
128M * 16 * 4
PN : 6019B0818601
PN : 6019B0938301
P/N : APPLY

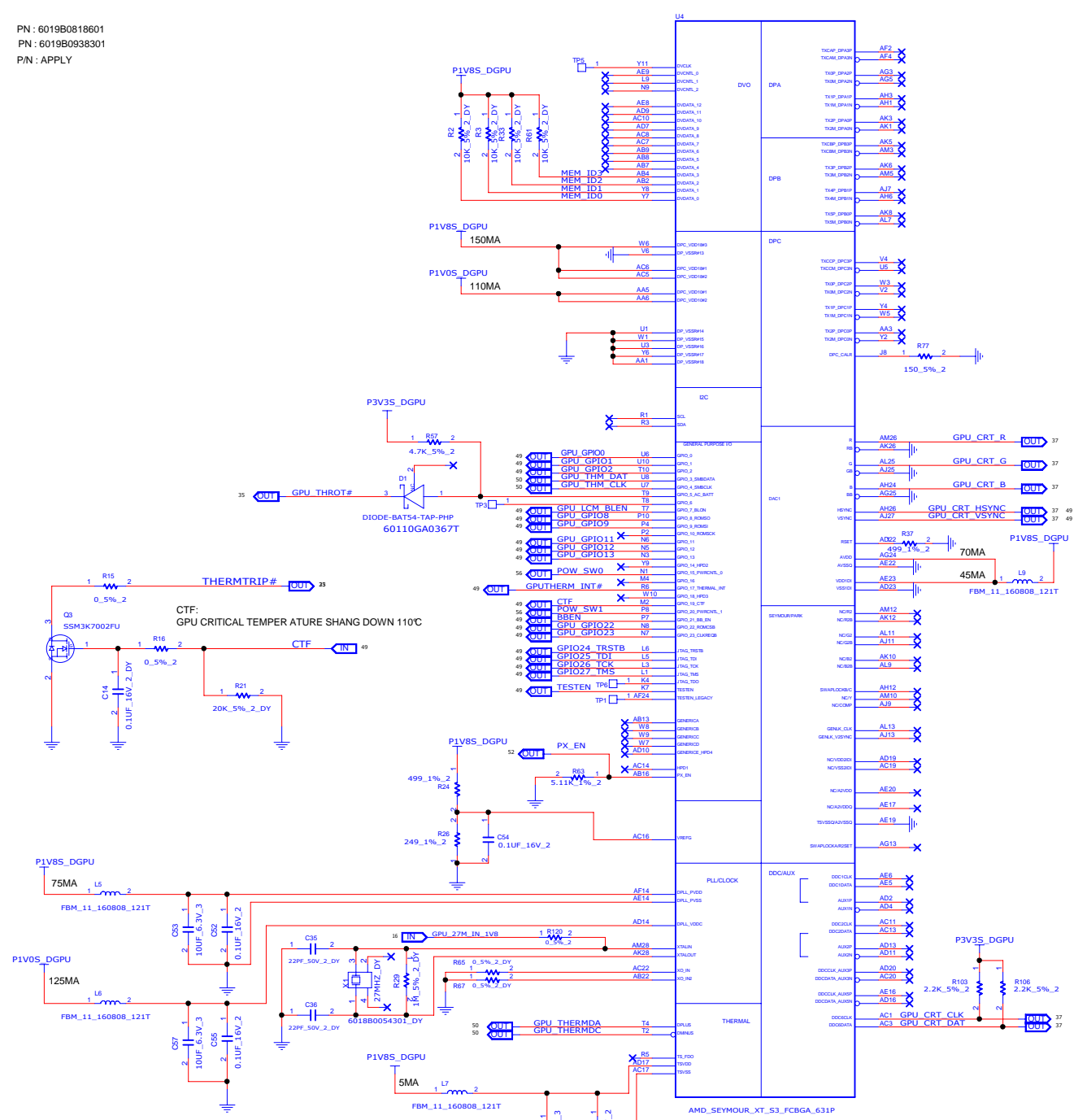
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTING
TX_PWRS_ENB	GPIO0	PCI FULL TX OUTPUT SWING
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS ENABLED
BIF_GEN2_EN_A	GPIO2	PCI GEN2 ENABLED
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MIXED OUT
BIF_VGA_DIS	GPIO7_BLON	CONTROL BACKLIGHT ON/OFF
ROMIDCFG(2.0)	GPIO9	VGA ENABLED
	GPIO[11:13]	MEMORY APERTURE SIZE SELECT

IF GPIO_22_EN=0, THEN GPIO[11:13] DEFINES THE PRIMARY MEMORY APERTURE SIZE

GPIO_13	GPIO_12	GPIO_11	MEMORY APERTURE SIZE
0	0	1	512/256 MB (DEFAULT)
1	1	0	RESERVED



POW_SW1	POW_SW0	+VDDC_GPU
0	0	1.1V
0	1	1V
1	0	0.95V
1	1	0.9V

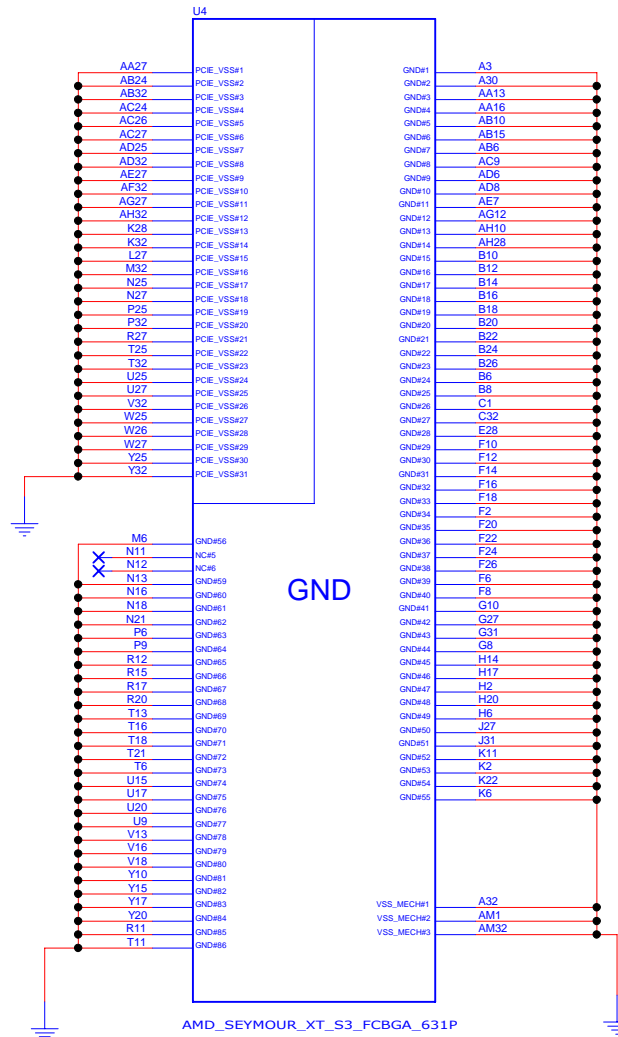
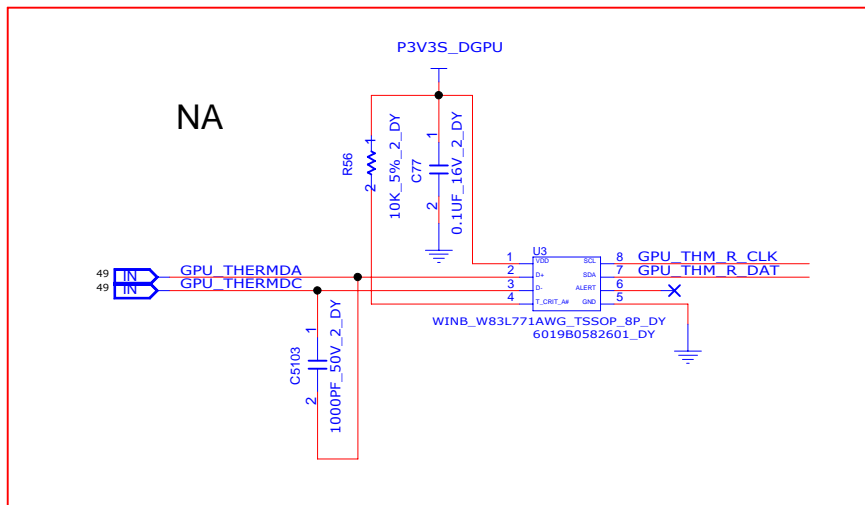
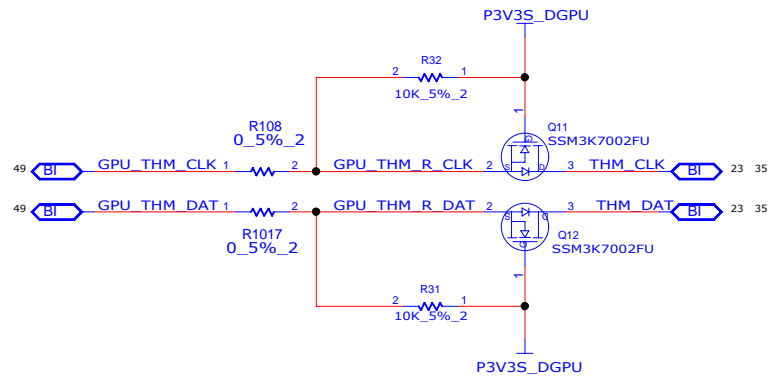


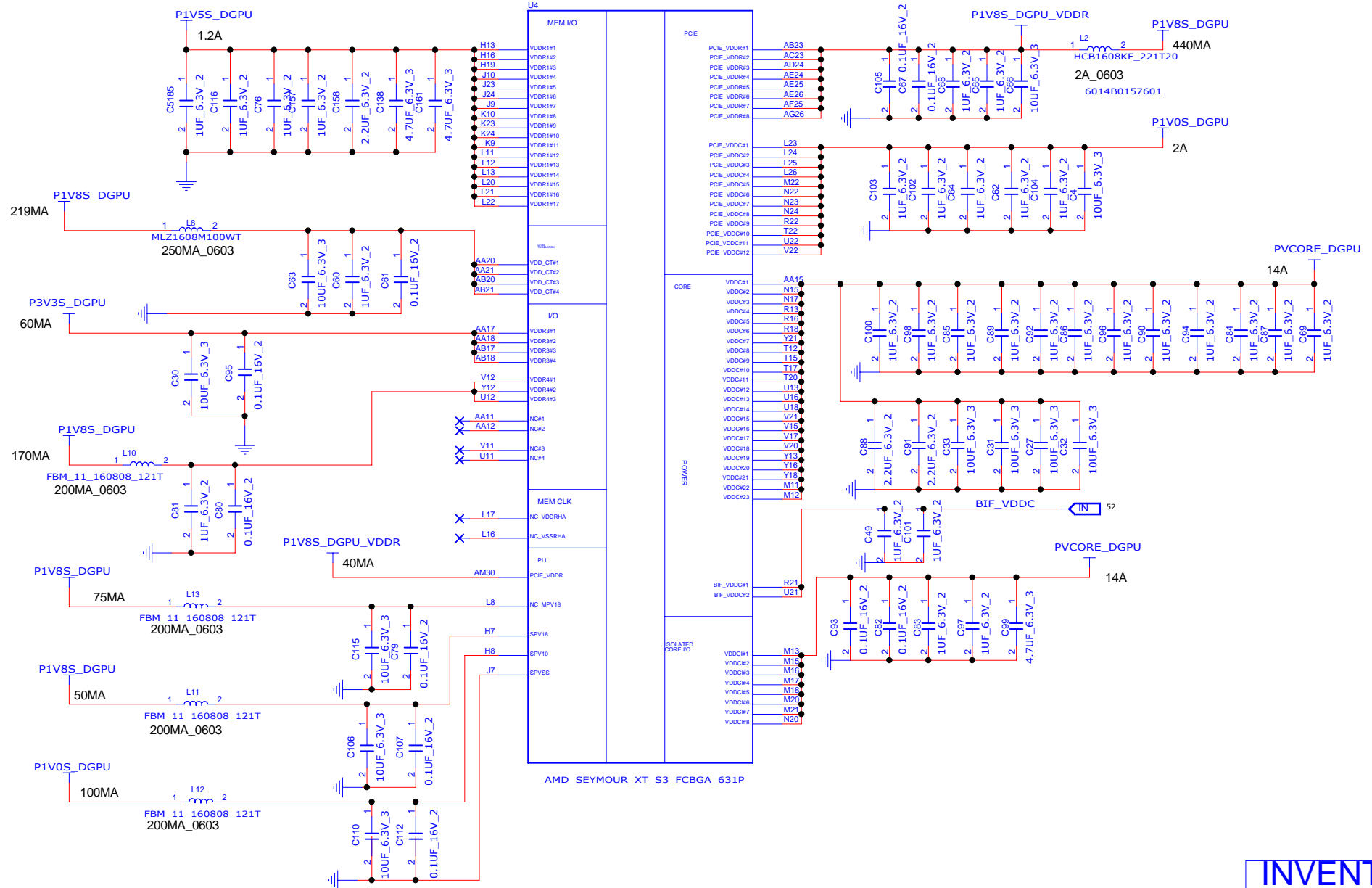
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SEYMOUR XT-S3

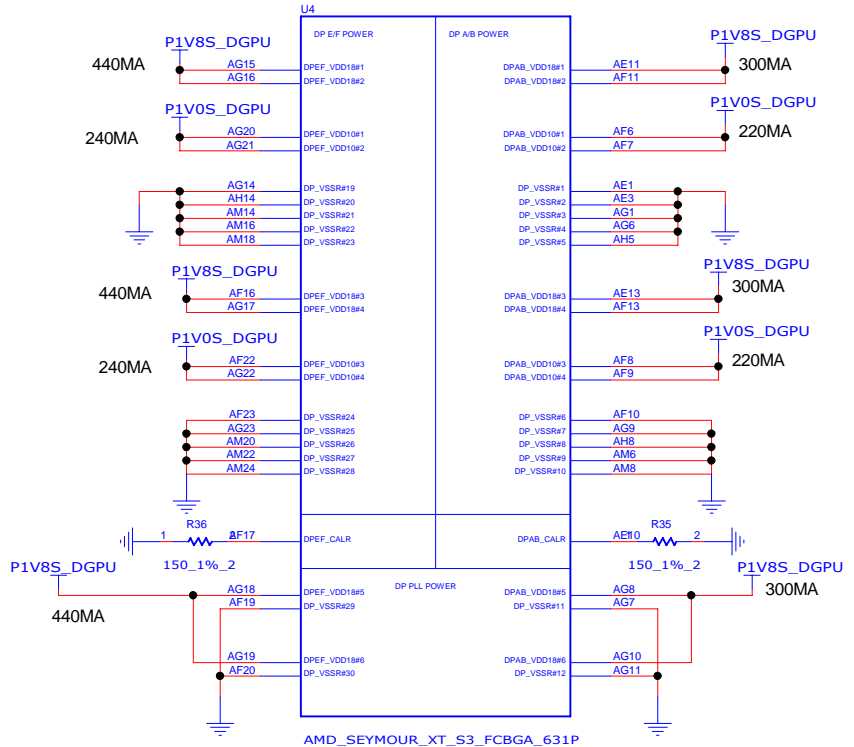
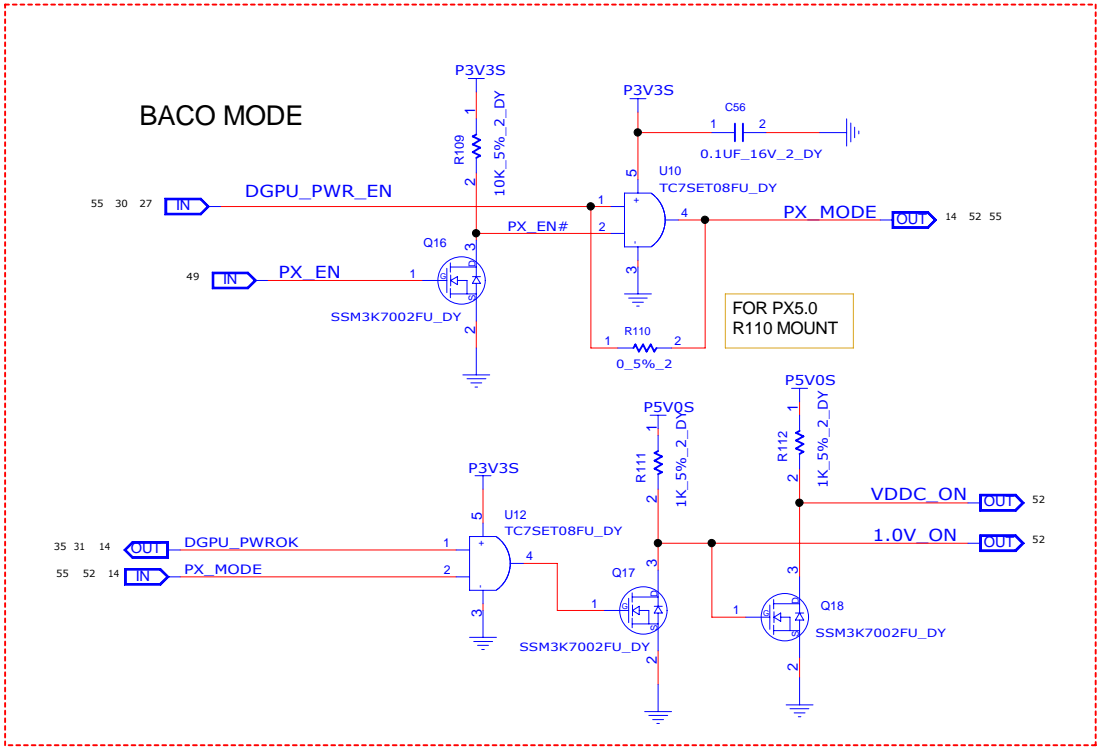
SIZE	CODE	DOC NUMBER	REV
E	13	13110XXXX-0-0	X01

SHEET 49 of 57

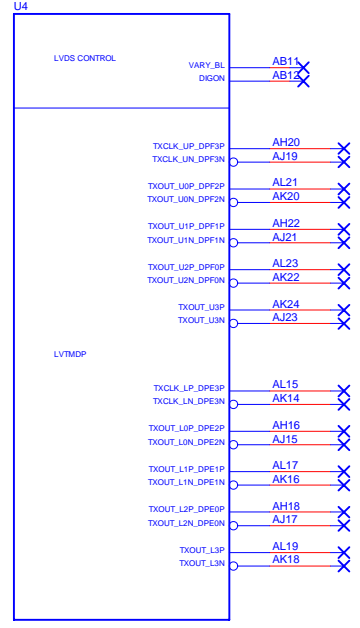
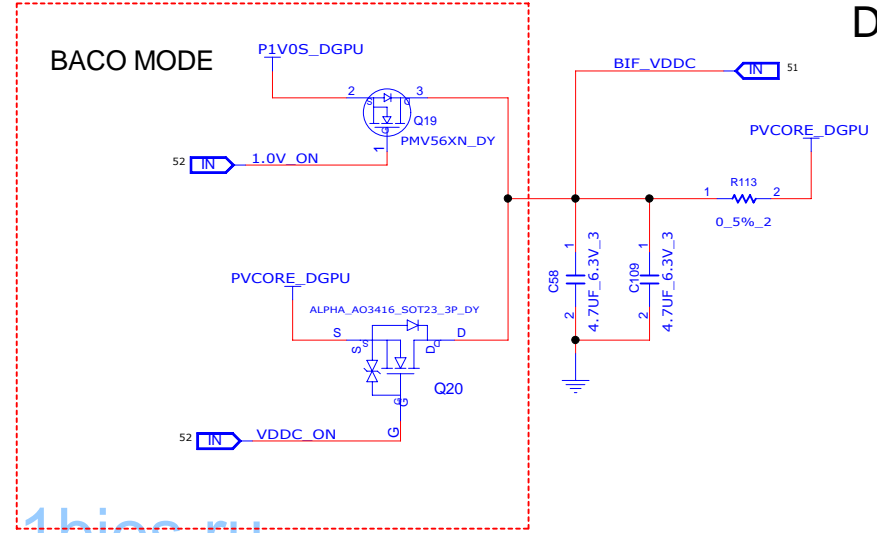




INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
SEYMOUR_XT_S3			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX			
DATE 21-OCT-2002			
SHEET 51 of 57			

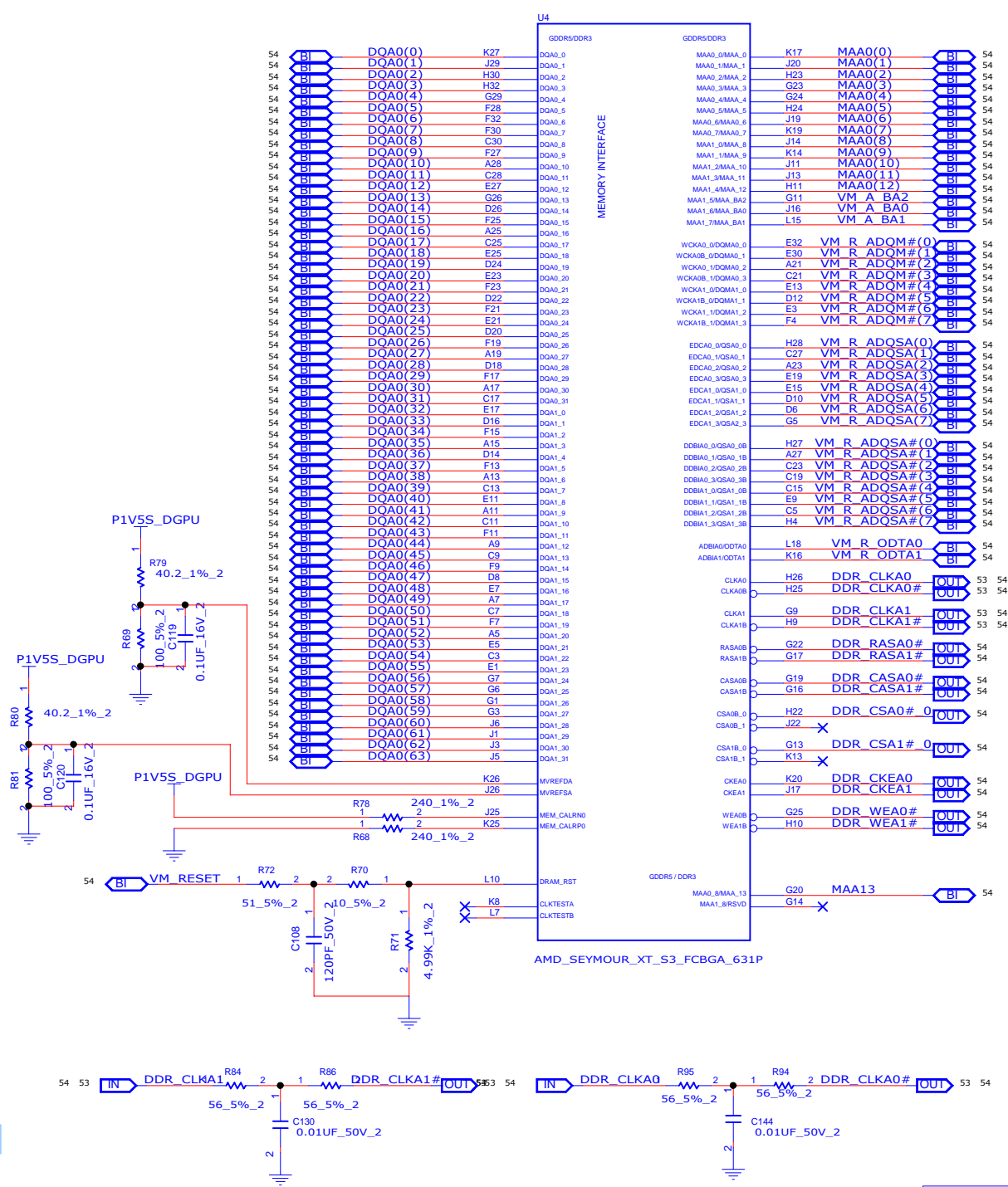


DEFULT IS PX5.0



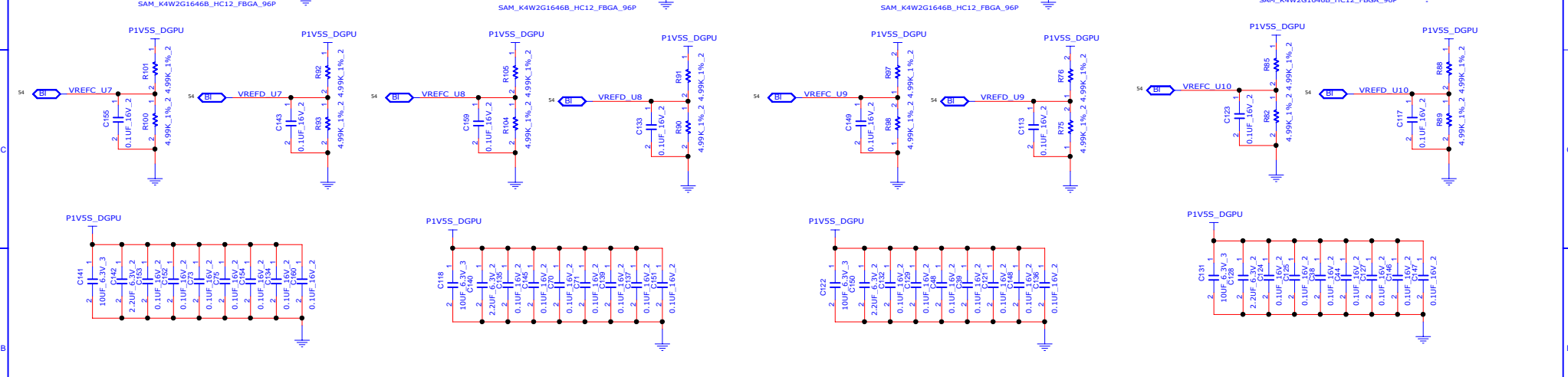
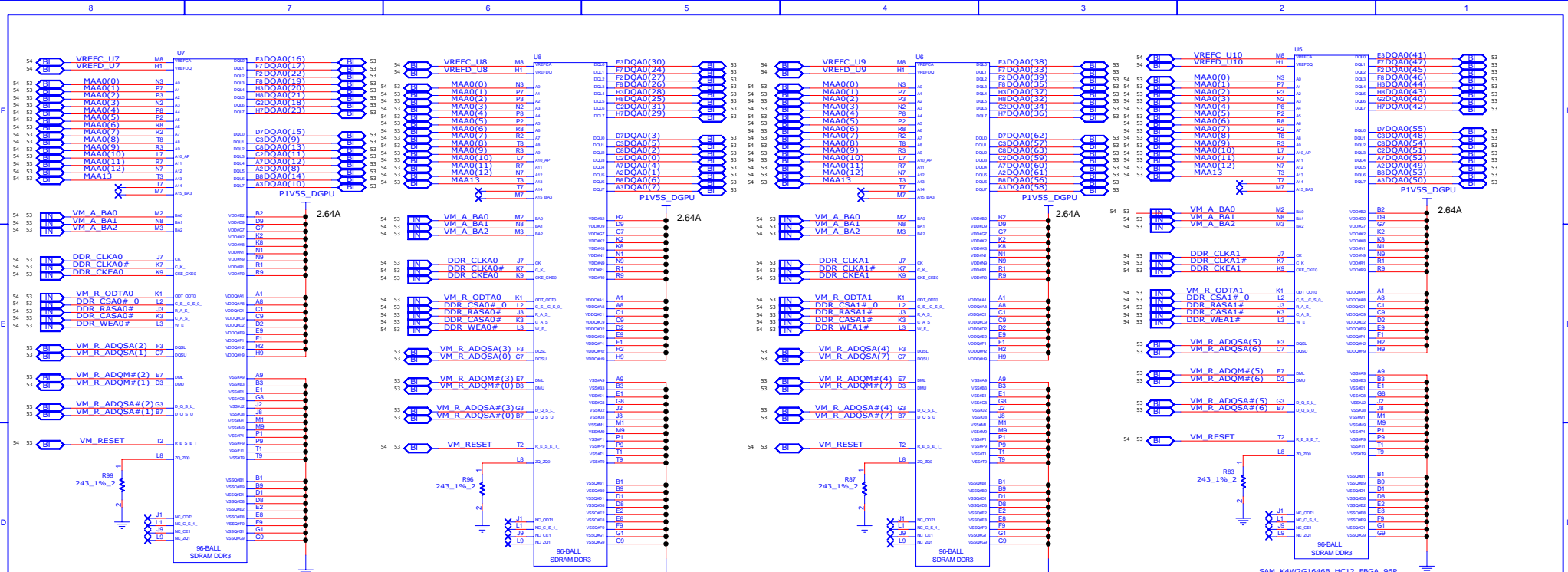
INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION SEYMOUR_XT_S3			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 52 of 57

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INVENTEC			
TITLE MODEL PROJECT FUNCTION SEYMOUR XT_S3			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX			
DATE 21-OCT-2002			
SHEET 53 of 57			



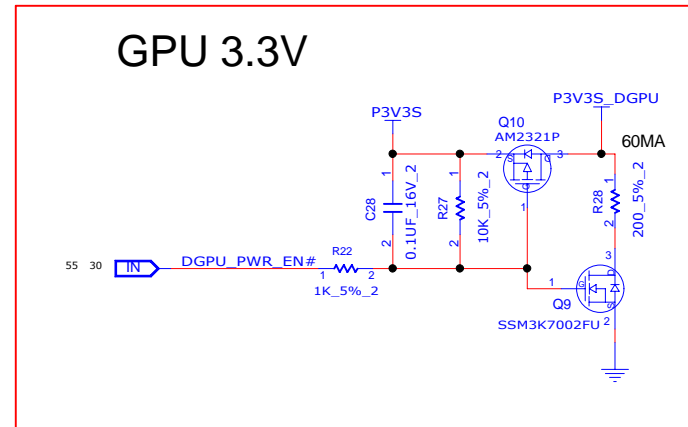
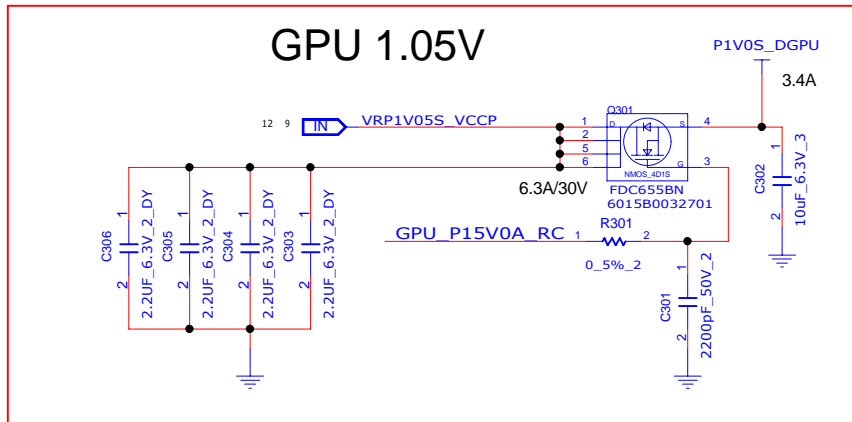
HYNIX 1GB D-DIE PN : 6019B0938301
 SAMSUNG 1GB C-DIE PN : 6019B0818601

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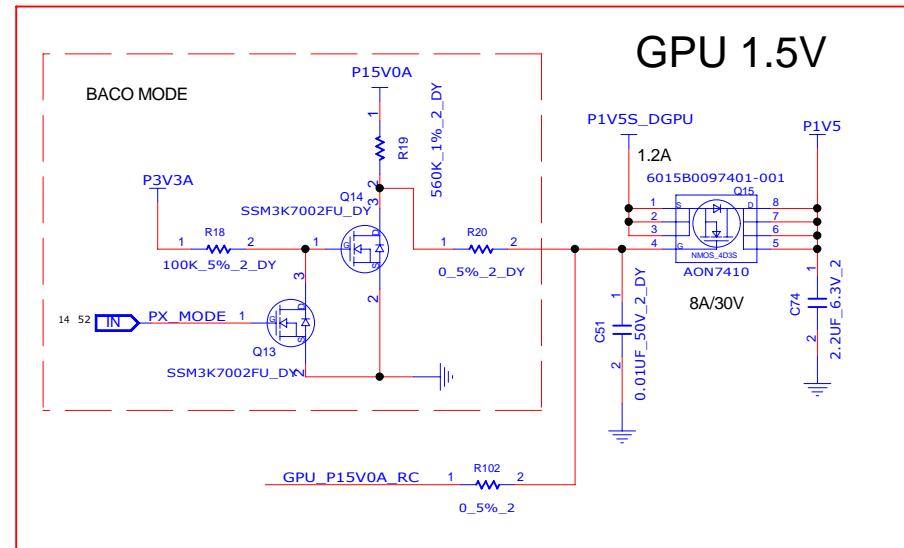
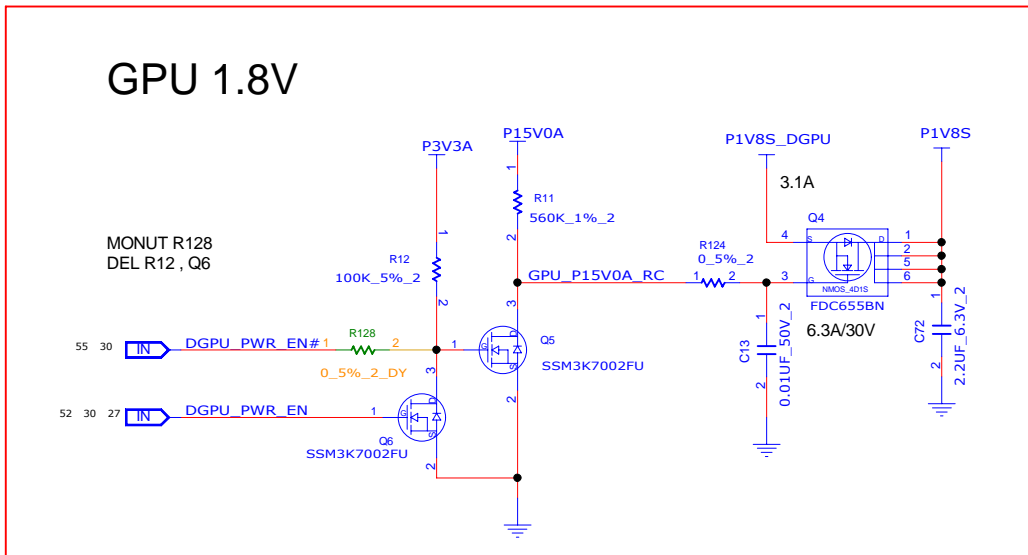
INVENTEC

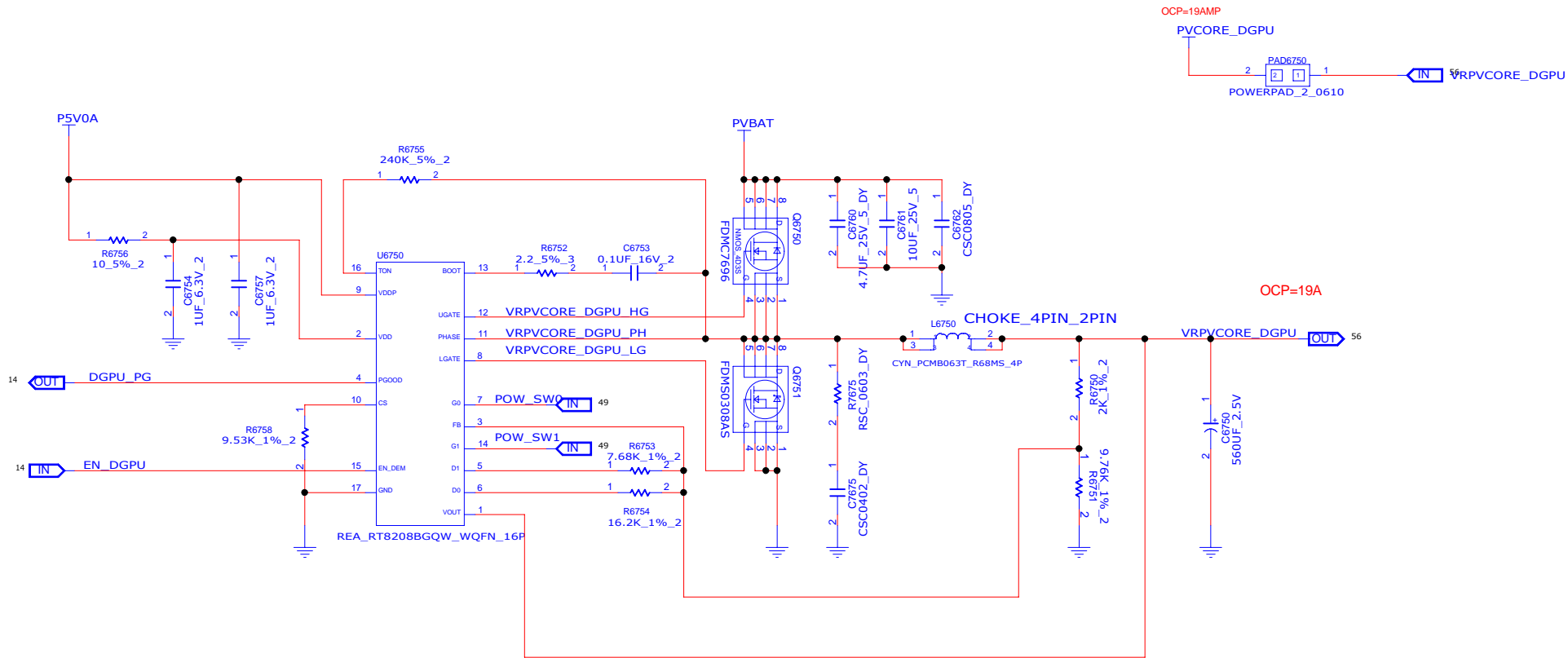
FILE	MODEL,PROJECT,FUNCTION	DOCNUMBER	REV
SIZE	CODE	1310XXXXX-0-0	X01
SHEET 54		of 57	

CHANGE BY: xxx DATE: 21-OCT-2002



DEFULT IS PX5.0



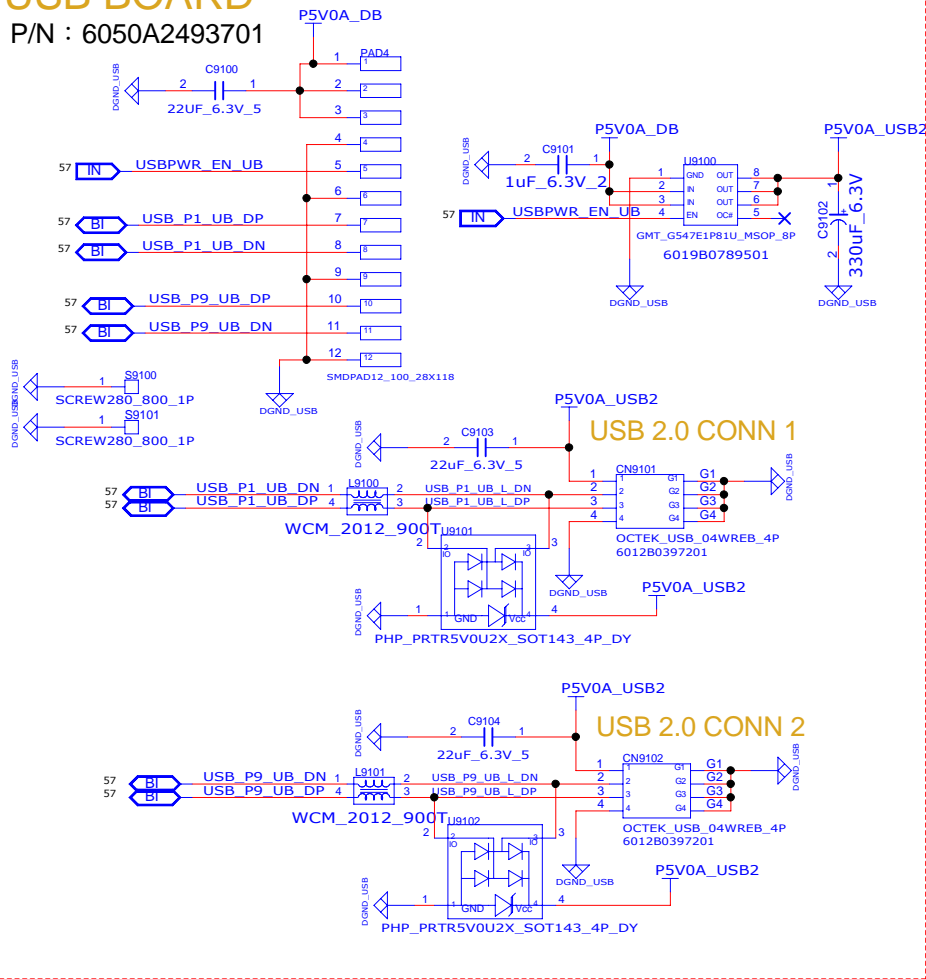


P.S. R6750(R1)R6751(R2)R6753(R3)R6754(R4)

RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

USB BOARD

P/N : 6050A2493701



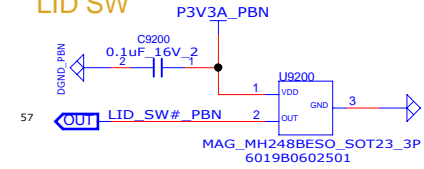
for Dauther Board

1 FIX9100 1 FIX9101 1 FIX9102 1 FIX9103
 1 FIX_MASK 1 FIX_MASK 1 FIX_MASK 1 FIX_MASK
 1 FIX9200 1 FIX9201 1 FIX9202 1 FIX9203
 1 FIX_MASK 1 FIX_MASK 1 FIX_MASK 1 FIX_MASK

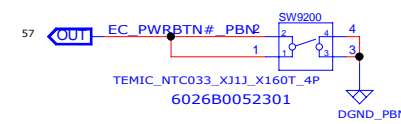
POWER BUTTON BOARD

P/N : 6050A2493201

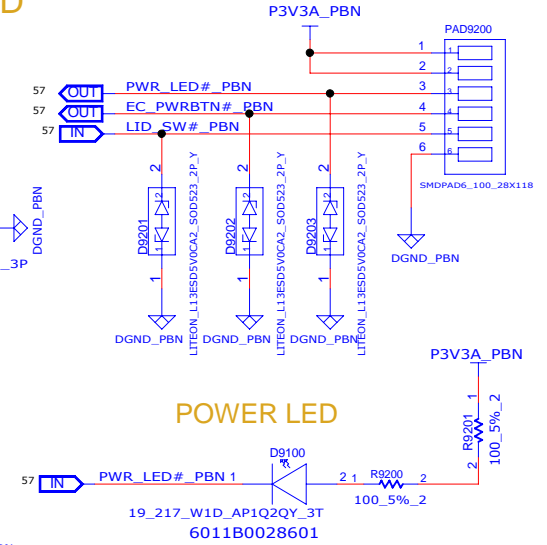
LID SW



POWER BUTTON

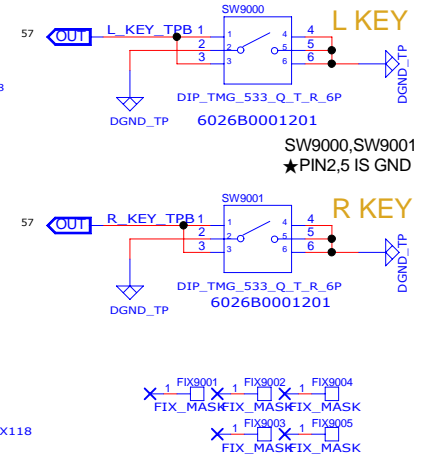
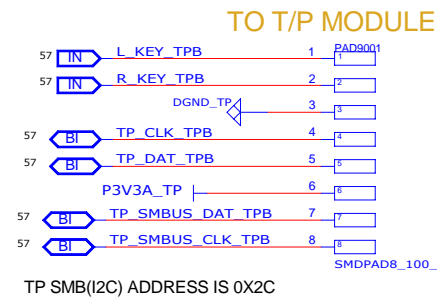
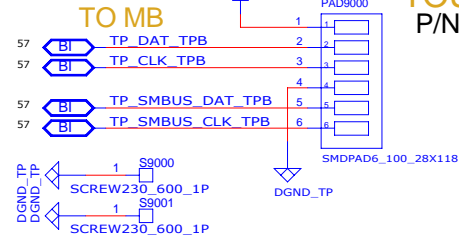


POWER LED



TOUCHPAD R / L BOARD

P/N : 6050A2493601



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
USB, POWER BUTTON DB			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXX			DATE 21-OCT-2002
SHEET 57 of 57			