SYSTEM PAGE REF.

K42Jv SCHEMATIC Revision 2.0

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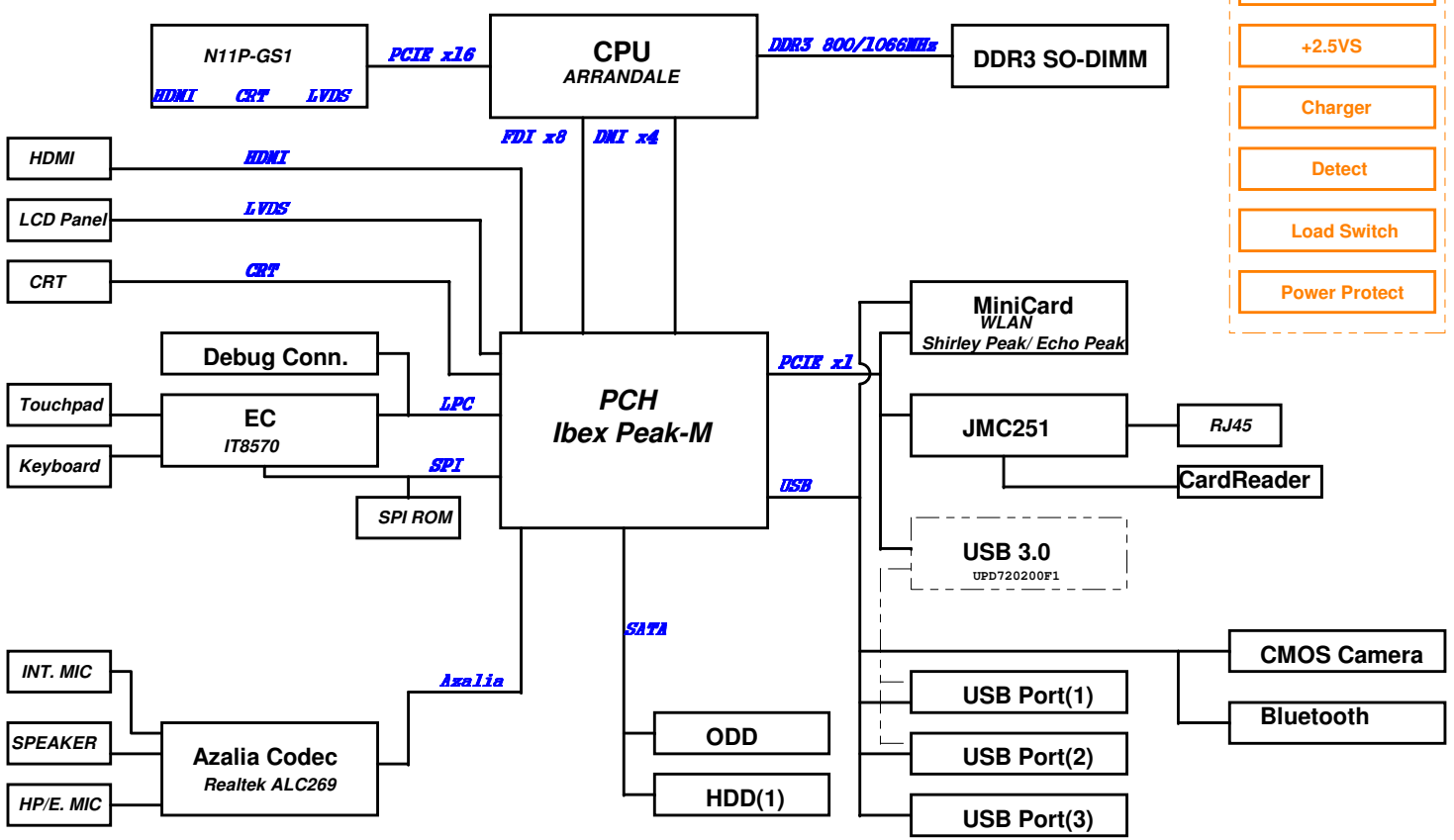
BLOCK DIAGRAM



Power
- VCORE
- System
- 1.5VS & 1.05VS
- DDR & VTT
- +2.5VS
- Charger
- Detect
- Load Switch
- Power Protect

Clock Generator
ICS9LVS3162

VID controller | Discharge Circuit | DC & BATT. Conn.

PWM Fan | Reset Circuit | Skew Holes

ASUSTeK COMPUTER INC. NB4

Title : Block Diagram
Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.1

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PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	-	INT TBD	+3VS
GPIO 07	GPI	USB30_SMIB	EXT PU	+3VS
GPIO 08	GPI	EC_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	OC5#	EXT PU	+3VSUS
GPIO 10	Native	OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EC_SCI#	EXT PU	+3VSUS
GPIO 12	Native	-	EXT PU	+3VSUS
GPIO 13	GPO	-		+3VSUS
GPIO 14	Native	OC7#	EXT PU	+3VSUS
GPIO 15	GPO	-	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWRGD_PCH	EXT PD	+3VS
GPIO 18	Native	CLK_REQ1#	EXT PU	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2_WLAN#_R	EXT PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_BT_LED	EXT PD	+3VS
GPIO 23	Native	LPC_DRQ#1		+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLK_REQ3#	EXT PU	+3VSUS
GPIO 26	Native	CLK_REQ4#(USB 3.0)	EXT PU	+3VSUS
GPIO 27	Native	PCH_VRM_EN	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON	-	+3VSUS
GPIO 29	GPO		-	+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	PCH_SPI_OV_RW	INT WEAK PU	+3VS
GPIO 34	Native	STP_PCI#	EXT PU	+3VS
GPIO 35	Native	SATACLKREQ#	EXT PD	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PD	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC2#	EXT PU	+3VSUS
GPIO 41	Native	OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	PECLK_REQ#	EXT PU	+3VSUS
GPIO 48	GPO	-	EXT PU	+3VS
GPIO 49	GPO	PCH_TEMP_EN	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#	EXT PU	+5VS
GPIO 53	GPO	PCI_GNT2#	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	Native	CLKREQ2_GLAN#_R	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC01#	EXT PU	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	EDID_SELECT#	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	PM_BATLOW#	EXT PU (Not used)	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC IT8570

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	KB_RST#
GPB7	O	PM_RSMRST#
GPC0	O	CLK_UC
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7		-
GPD0		-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EC_SCI#
GPD4	O	EC_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	I	HDMI_HPD
GPE0		-
GPE1		-
GPE2		-
GPE3		-
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0		-
GPF1	O	VSUS_ON
GPF2	O	VTT_DRAM_PWR_SEL1
GPF3	O	VTT_DRAM_PWR_SEL2
GPF4	IO	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	VGA_DEEPIDLE (TBD)
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5		-
GPH6	O	CAP_LED#
GPI0	I	GPU_ALERT#
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ENABLE
GPI5	I	CPU_VCORE_I_SEN
GPI6	I	DGPU_VCORE_I_SEN
GPI7		-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	V_DA_EC/VCORE_SEL1
GPJ5	O	VCORE_SEL2

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LVS3162)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A4)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
VGA Thermal IC(G781-1)	1001101x (9A)	

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	
USB 4	
USB 5	
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	

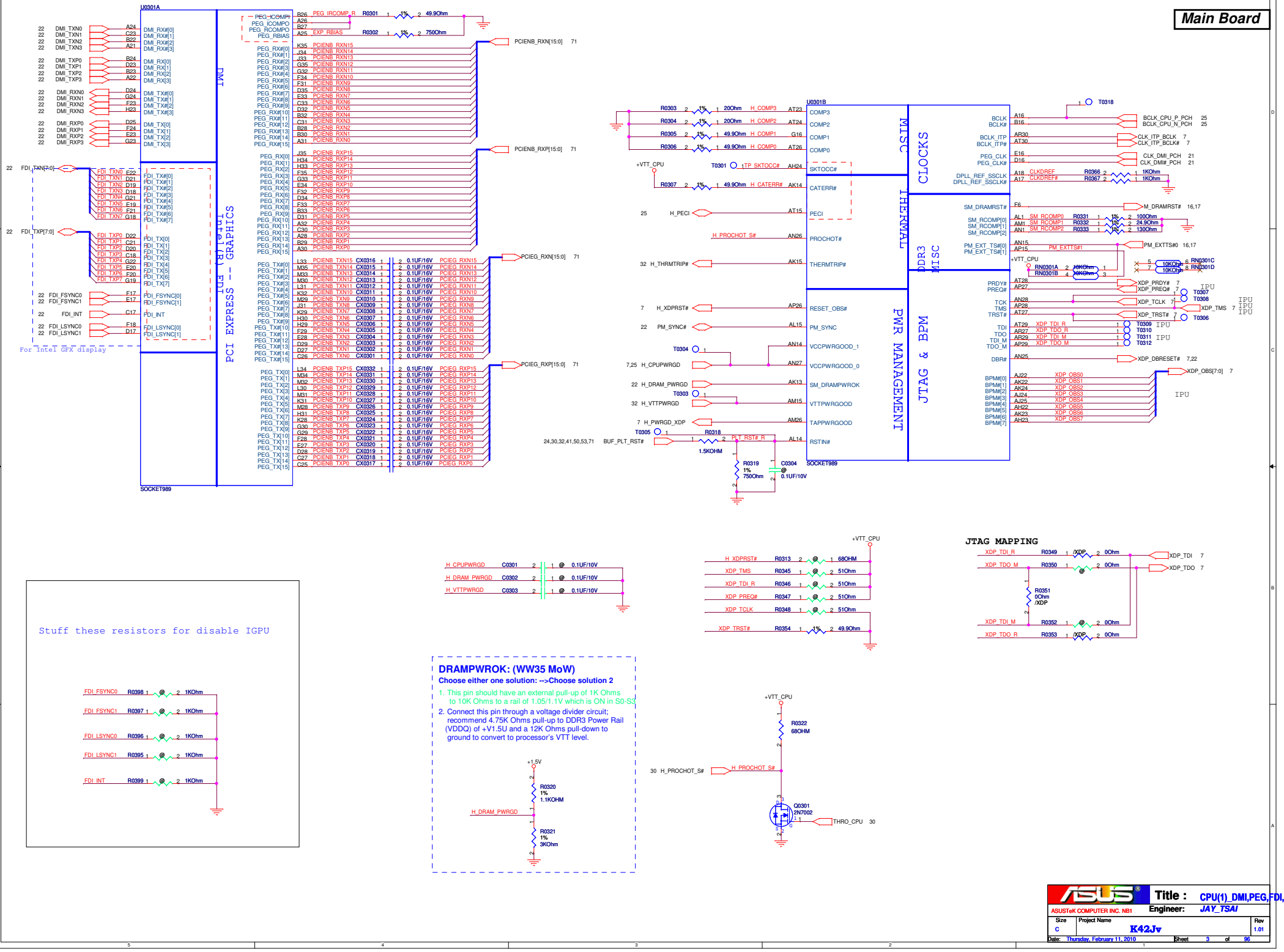
ASUSTeK COMPUTER INC. NB4

Title : System Setting

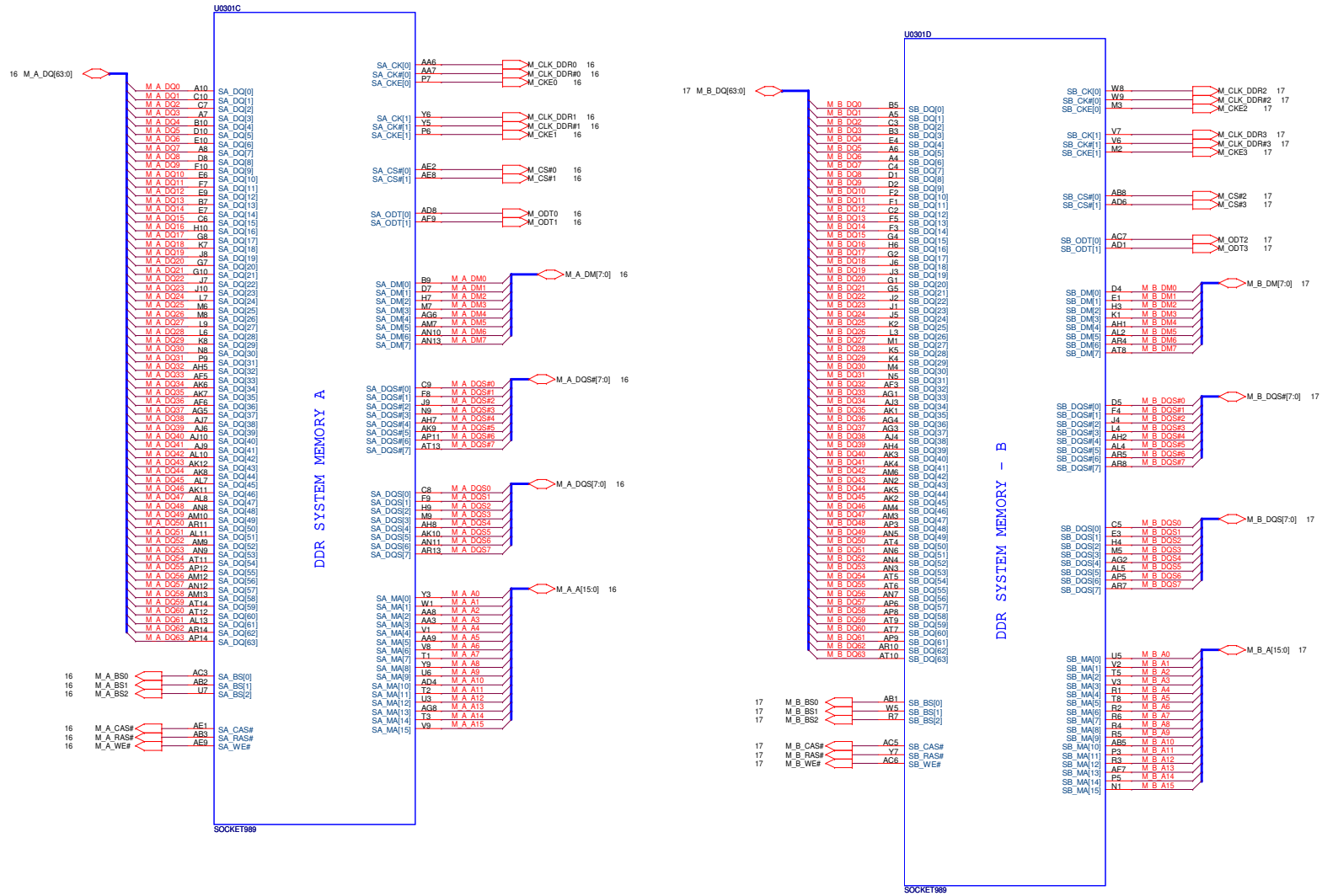
Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 2 of 96



ASUSTeK COMPUTER INC. NB1	Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC	
	Engineer:	JAY_TSAI	
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 3 of 96		



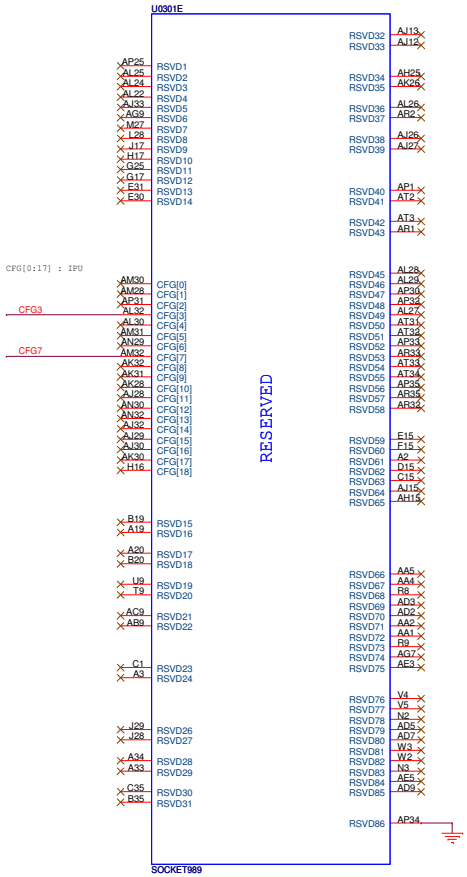
ASUSTeK COMPUTER INC. NB1

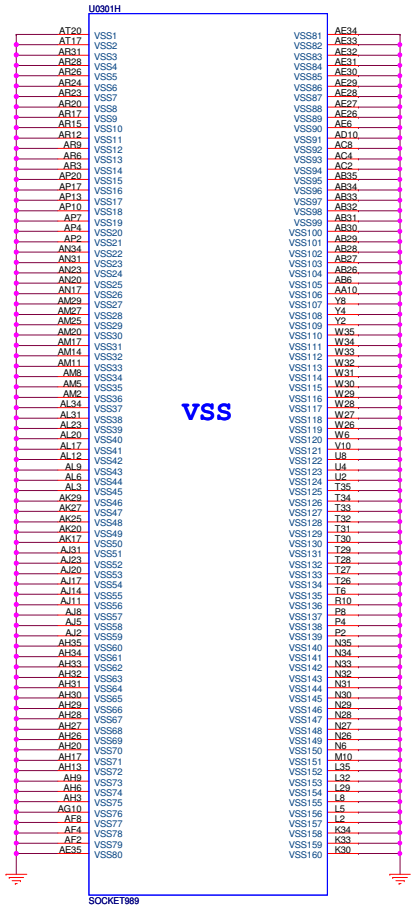
Title : CPU(2)_DDR3

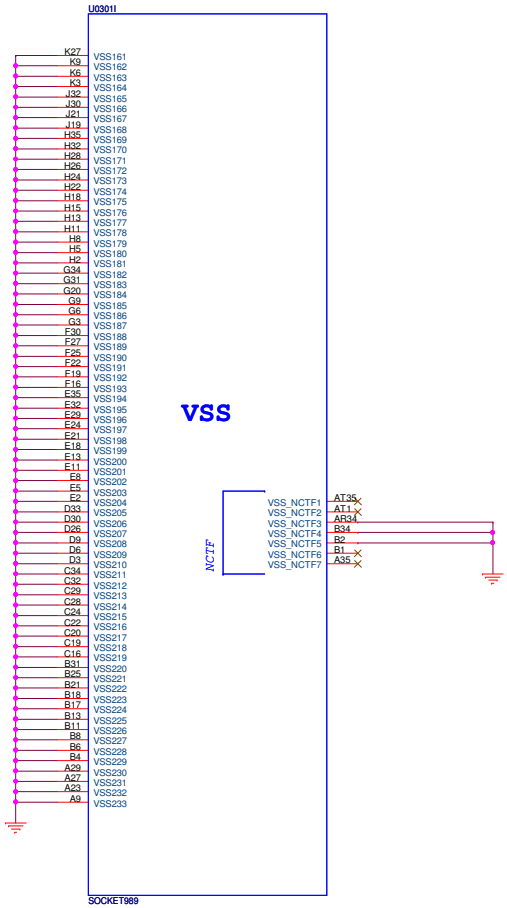
Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 4 of 96







CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

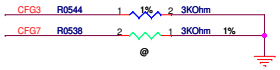
CFG[3]: PCIE Static Numbering Lane Reversal.(Arrandale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.
CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.
CFG[17:5] - Reserved configuration pins.
Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifucation:
- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.
CFG[3] – Reserved (Used by Arrandale Pporcessors for PCI Express* Static Lane Numbering Reversal)
CFG[11:4] - Reserved configuration pins.
CFG[12] - N/A on Clarksfield processors.
CFG[17:13] - Reserved configuration pins.
Note: Hardware straps are sampled after RSTIN# de-assertion.

ASUSTeK COMPUTER INC. NB1

Title : CPU(3)_CFG,RSVD,GND

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

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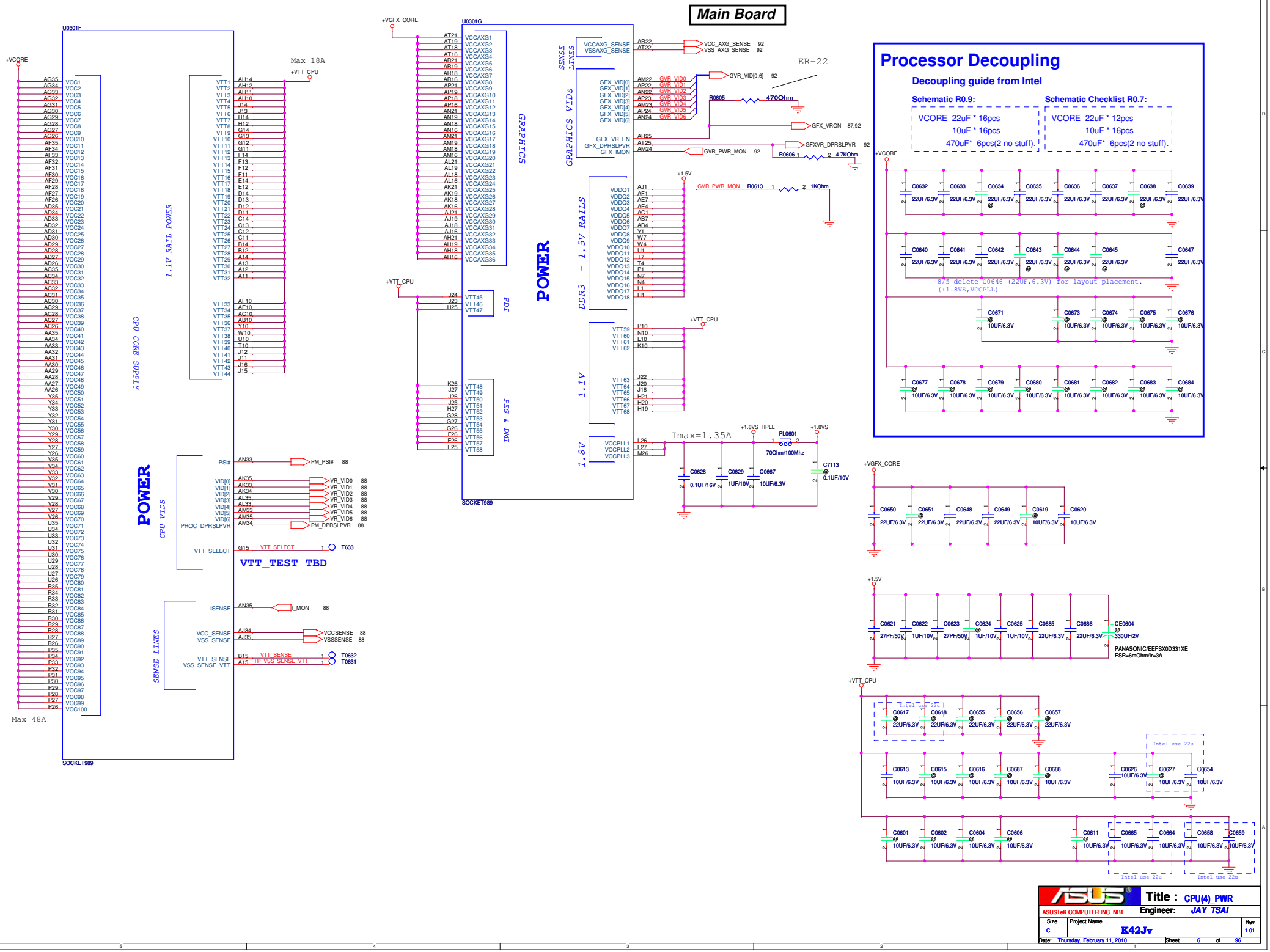
Main Board



Processor Decoupling

Decoupling guide from Intel

Schematic R0.9:	Schematic Checklist R0.7:
VCORE 22uF * 16pcs	VCORE 22uF * 12pcs
10uF * 16pcs	10uF * 16pcs
470uF* 6pcs(2 no stuff).	470uF* 6pcs(2 no stuff).

8/5 delete C0646 (22UF,6.3V) for layout placement.
(+1.8VS,VCCPLL)

ER-22

Title :	CPU(4)_PWR
Engineer:	JAY_TSAI
Company	ASUSTeK COMPUTER INC. NB1
Size	C
Project Name	K42Jv
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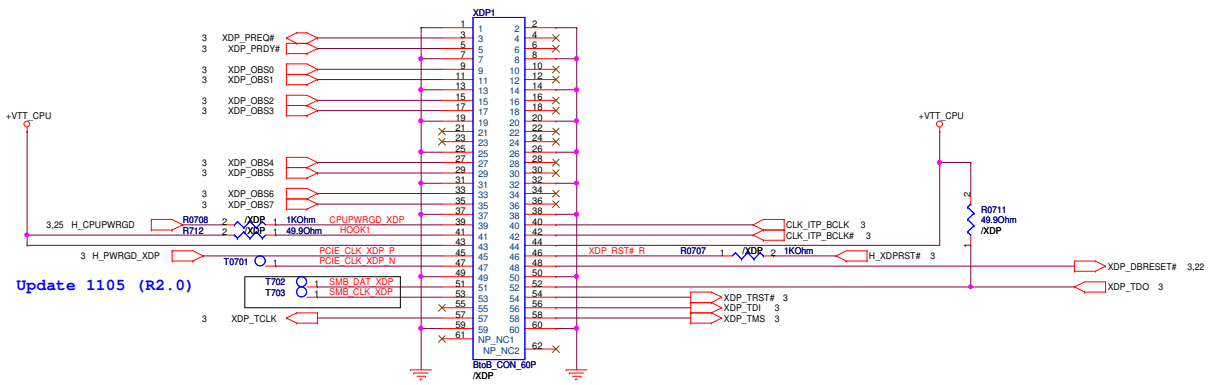
CPU XDP connector



Update 1105 (R2.0)

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 7 of 96		

Title :	NB_****
ASUSTeK COMPUTER INC. NB1	Engineer:
Size: Custom	Project Name: K42Jv
Rev: 1.01	
Date: Thursday, February 11, 2010	Sheet 8 of 96

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 9 of 96		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 10 of 96		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 11 of 96		

Main Board

ASUSTeK COMPUTER INC. NB1

Title : NB_****

Engineer:

Size	Project Name	Rev
Custom	K42Jv	1.01

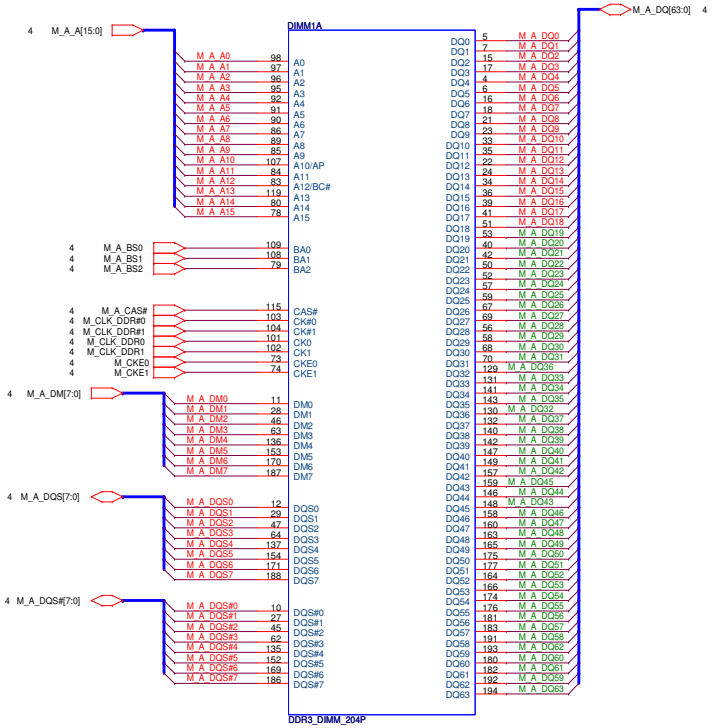
Date: Thursday, February 11, 2010 Sheet 12 of 96

Main Board

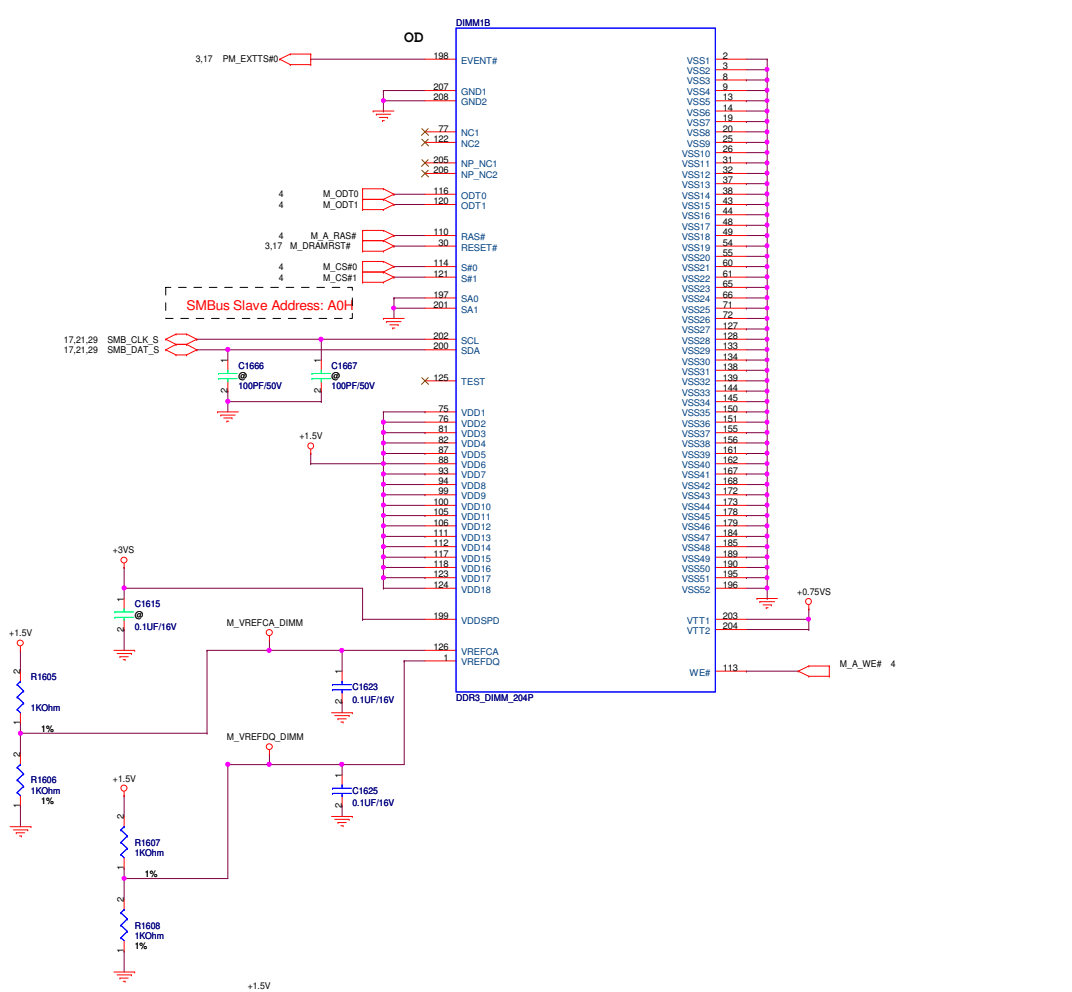
ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 13 of 96		

ASUSTeK COMPUTER INC. NB6	Title :
	Engineer:
Size: A	Project Name: K42Jv
	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 14 of 96

ASUSTeK COMPUTER INC. NB6	Title :
	Engineer:
Size: A	Project Name: K42Jv
	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 15 of 96

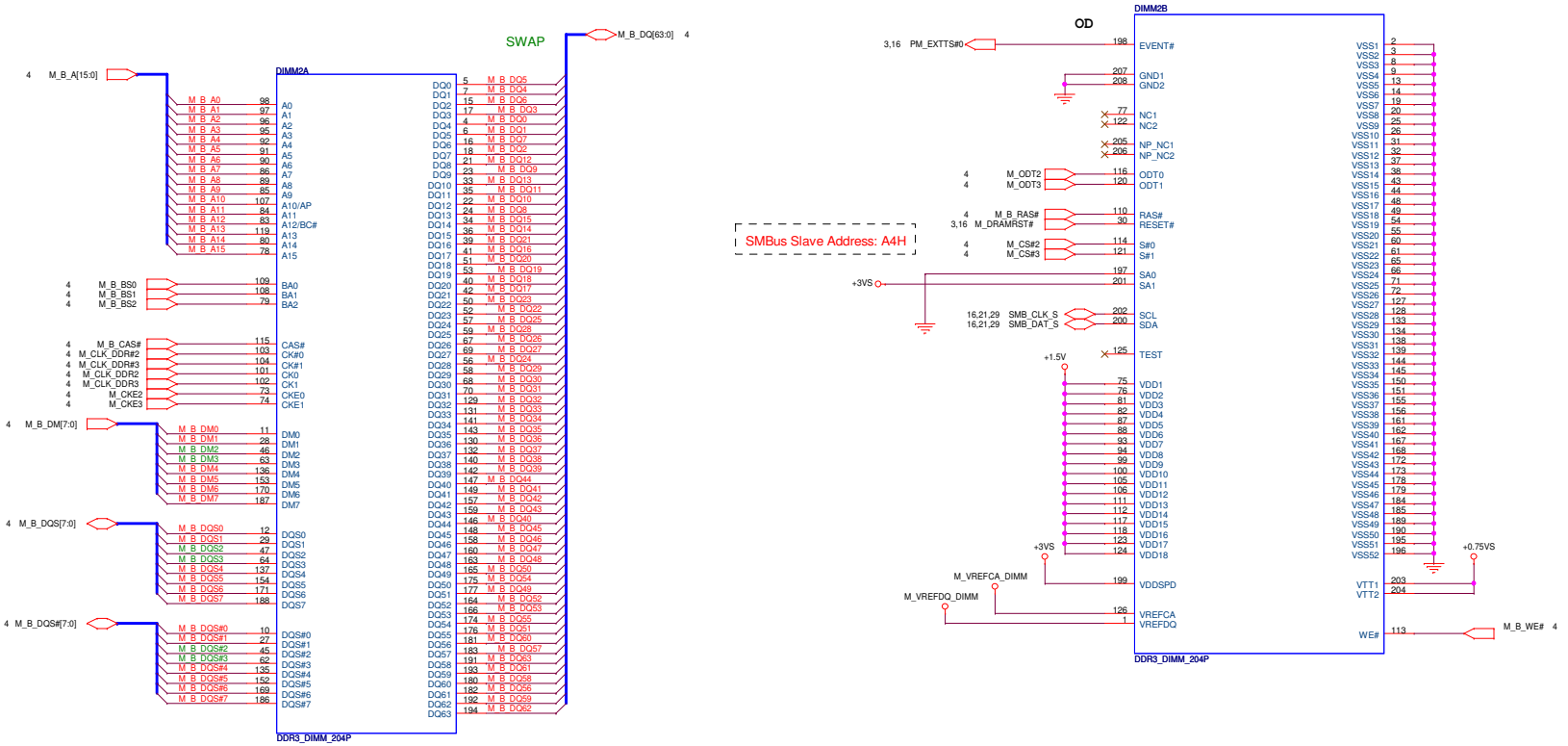


REV 9.2mm



Layout Note: Place these caps near SO DIMMS

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_0		
	Engineer: JAY_TSAI		
Size C	Project Name K42Jv		Rev 1.01
Date: Thursday, February 11, 2010	Sheet 16	of	96



STD 5.2mm

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1		
	Engineer: JAY_TSAI		
Size C	Project Name K42Jv		Rev 1.01
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Title DDR3 CA_DQ VOLTAGE

ASUSTeK COMPUTER INC. NB6

Engineer: JAY_TSAI

Size	Project Name	Rev
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Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. **NOTE:** This signal should not be pulled low.
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts.If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination**: 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDATA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDATA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination**: 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high

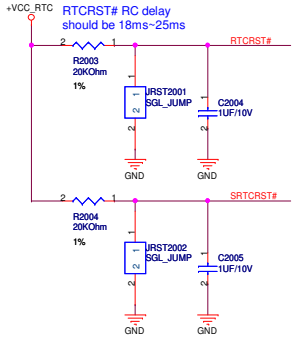
Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN#/GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. **NOTE:** Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. **NOTE:** This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. **NOTE:** A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

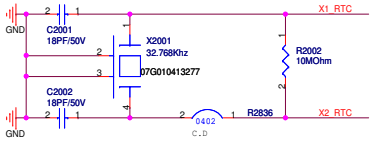
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

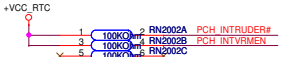


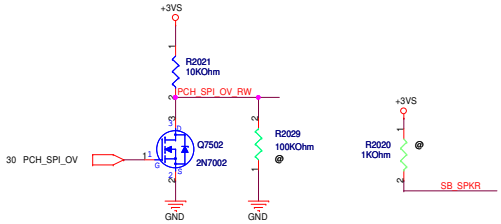
DG2.0 P297
RTCRST# and SRTCRST# can not be shorted together

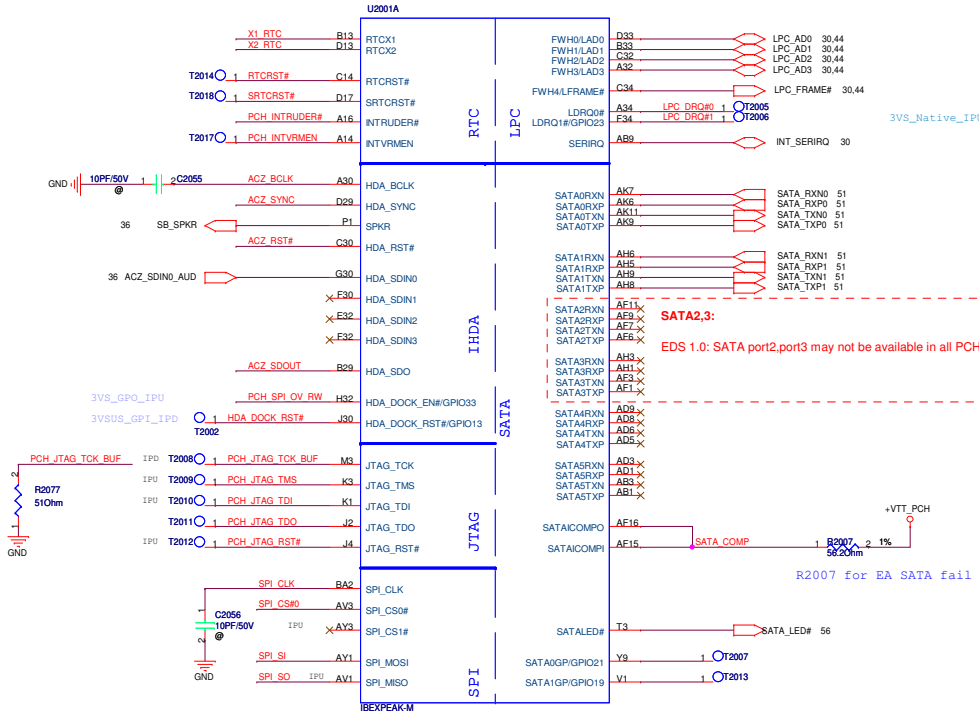
Strap information:

	H	L
ACZ_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_SI: iTPM strap. (IPD)	Enable	Disable
PCH_INTVRMEN Integrated 1.05 V VRM Enable /Disable	Enable	Disable

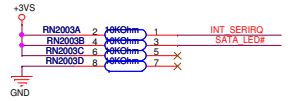




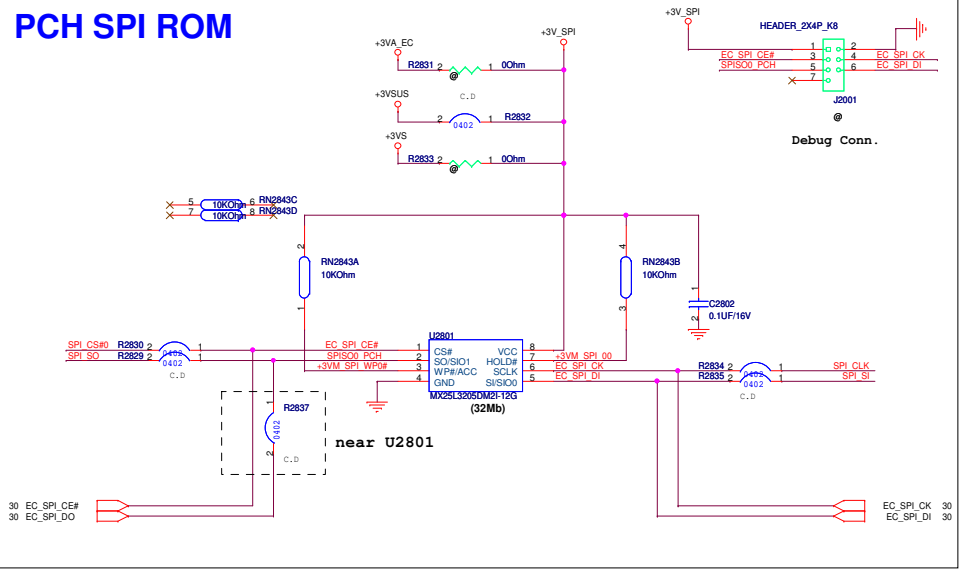




R2007 for EA SATA fail

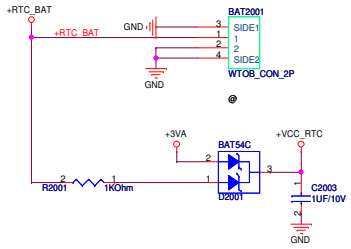


PCH SPI ROM



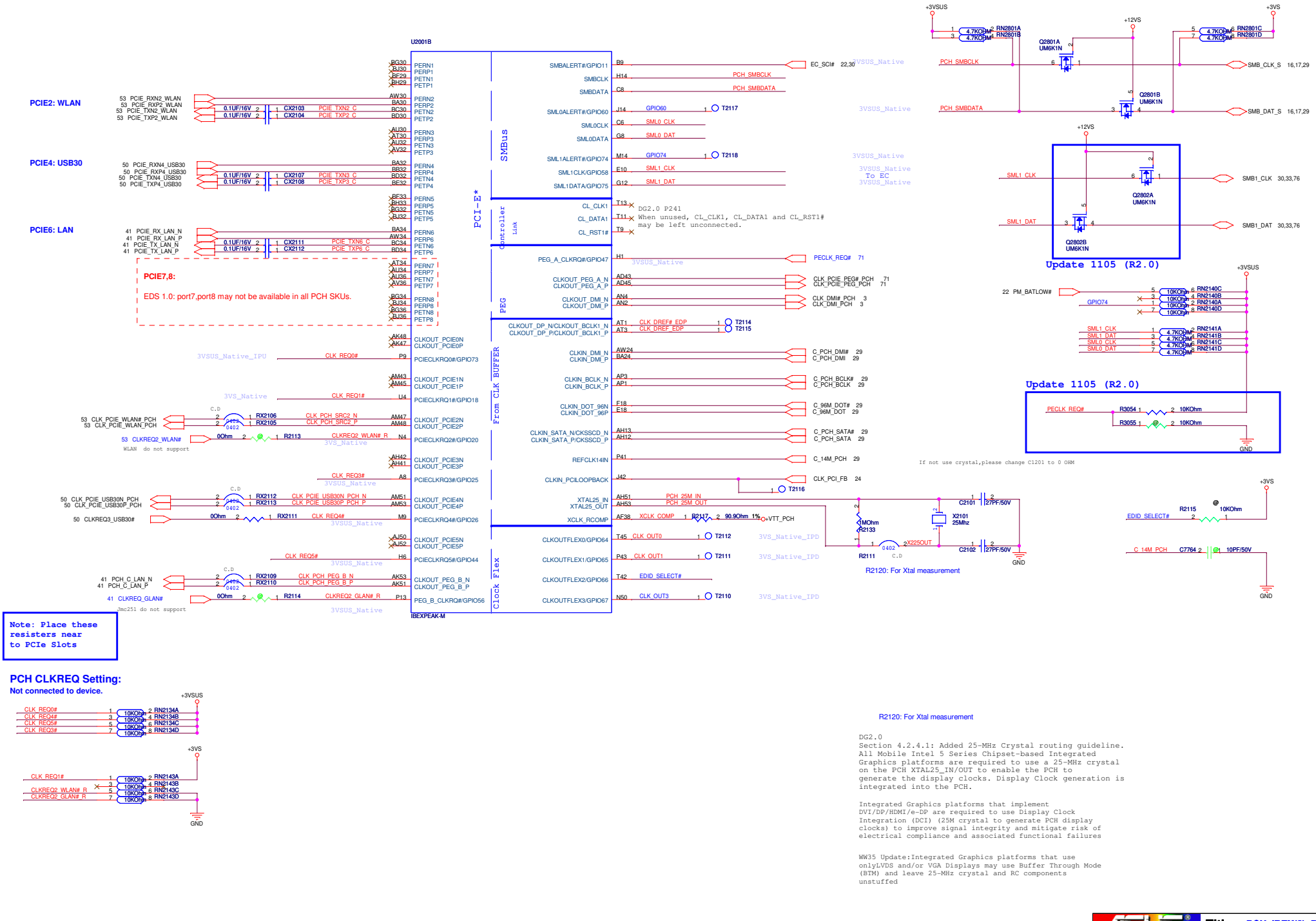
RTC battery

PR-07

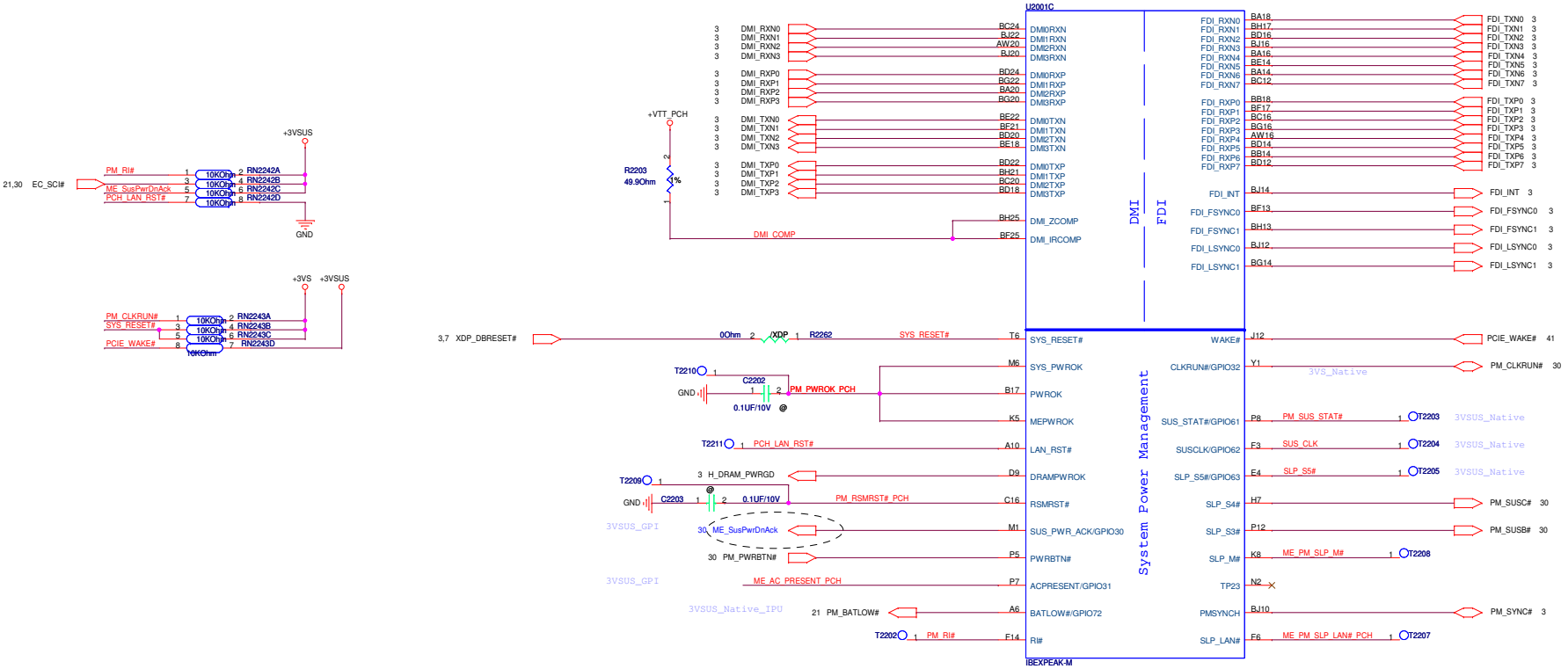


0122 Add BAT2001 for RTC BATT

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(1)SATA,IHDA,RTC,LPC	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 20 of 96	


U2001B
IBEXPEAK-M
PCIE2: WLAN
PCIE4: USB30
PCIE6: LAN
PCIE7,8:
EDS 1.0: port7,port8 may not be available in all PCH SKUs.
PCI-E*
SMBus
Controller Link
PEG
From Clk BUFFER
Clock Flex
Note: Place these resisters near to PCIe Slots
PCH CLKREQ Setting:
Not connected to device.
DG2.0 P241
When unused, CL_CLK1, CL_DATA1 and CL_RST1# may be left unconnected.
Update 1105 (R2.0)
Update 1105 (R2.0)
If not use crystal,please change C1201 to 0 OHM
R2120: For Xtal measurement
R2120: For Xtal measurement
DG2.0
Section 4.2.4.1: Added 25-MHz Crystal routing guideline.
All Mobile Intel 5 Series Chipset-based Integrated Graphics platforms are required to use a 25-MHz crystal on the PCH XTAL25_IN/OUT to enable the PCH to generate the display clocks. Display Clock generation is integrated into the PCH.
Integrated Graphics platforms that implement DVI/DP/HDMI/e-DP are required to use Display Clock Integration (DCI) (25M crystal to generate PCH display clocks) to improve signal integrity and mitigate risk of electrical compliance and associated functional failures
WW35 Update:Integrated Graphics platforms that use onlyLVDS and/or VGA Displays may use Buffer Through Mode (BTM) and leave 25-MHz crystal and RC components unstuffed
Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG
ASUSTeK COMPUTER INC. NB6
Engineer: JAY_TSAI
Size C
Project Name K42Jv
Rev 1.01
Date: Thursday, February 11, 2010
Sheet 21 of 96

pre-ES1 not support
Reversal Feature



R1.1,item L15

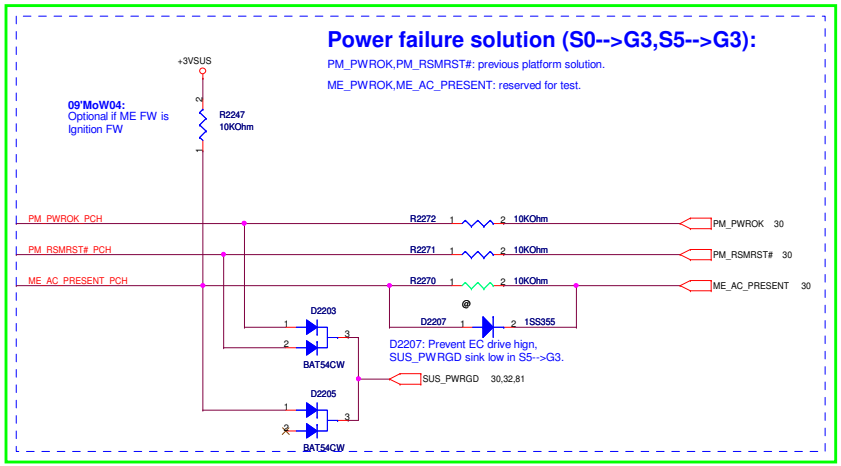


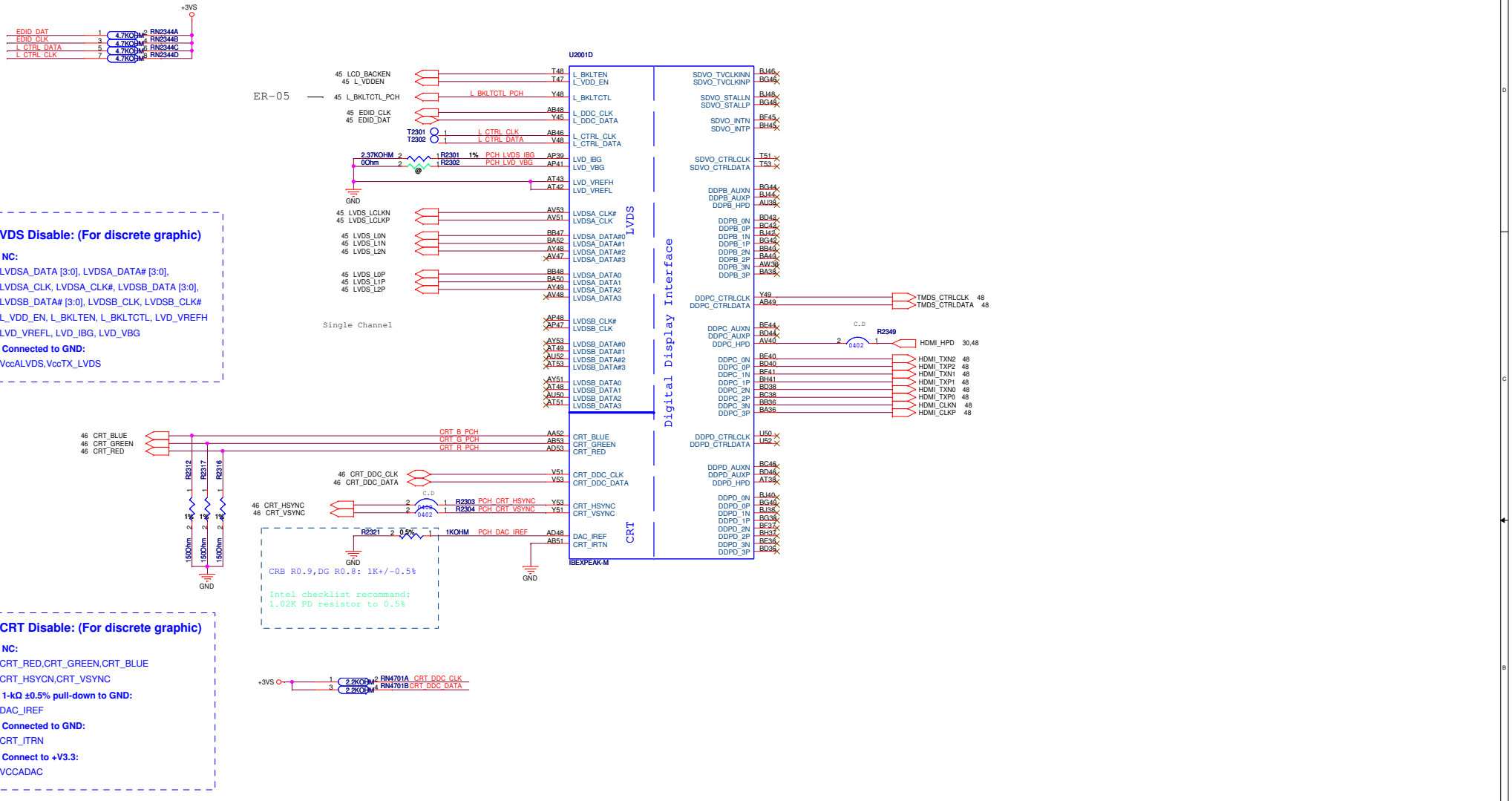
Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required **Note:** Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) **Note:** If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required **Note:** If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(3)_FDI,DMI,SYS PWR		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 22 of 96		



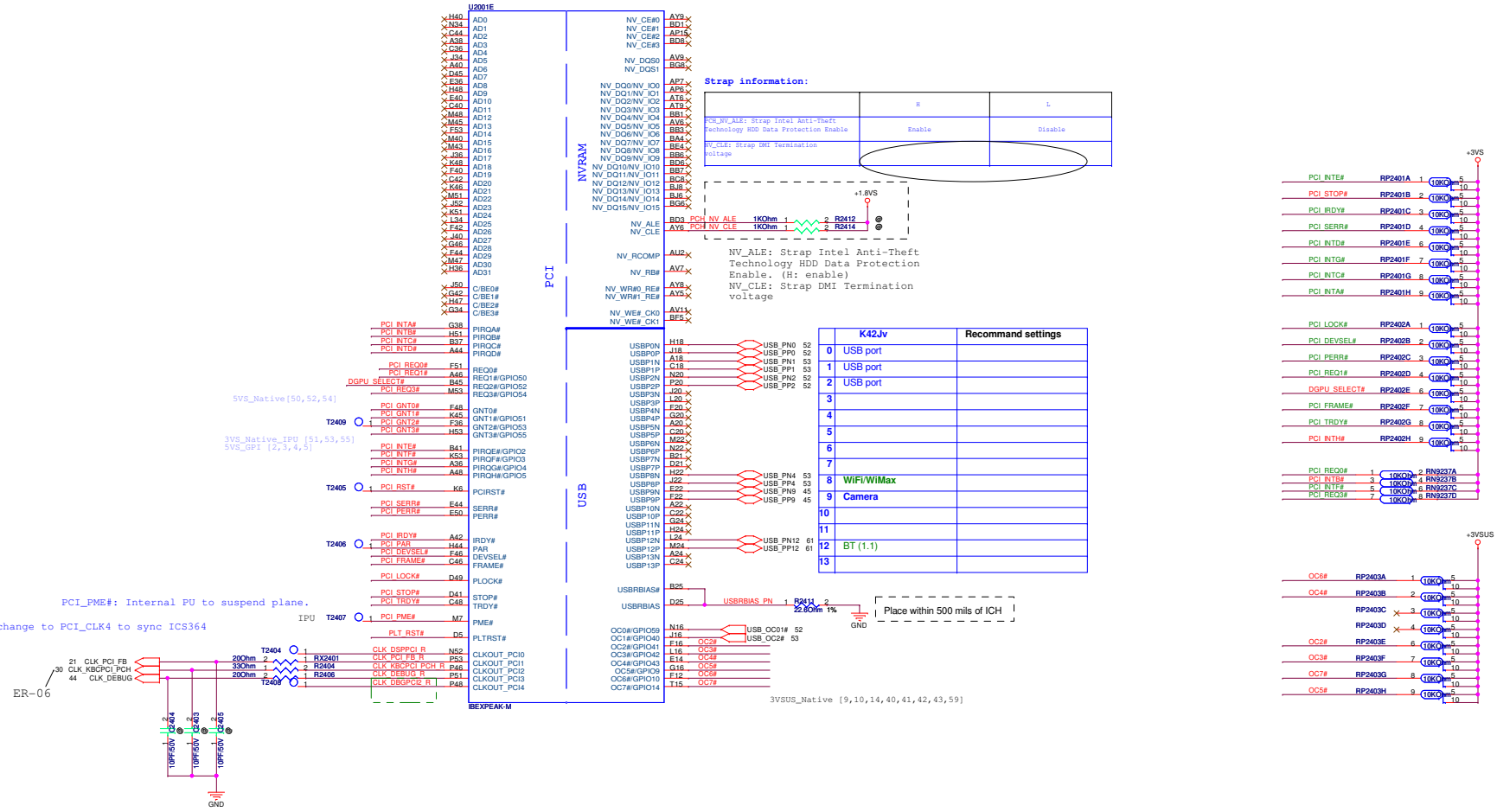
LVDS Disable: (For discrete graphic)

1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

CRT Disable: (For discrete graphic)

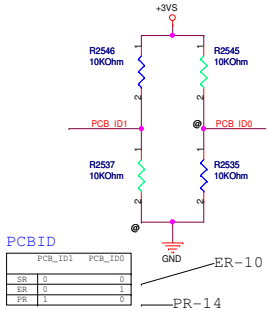
1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(4)_DP,LVDS,CRT	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 23 of 96	



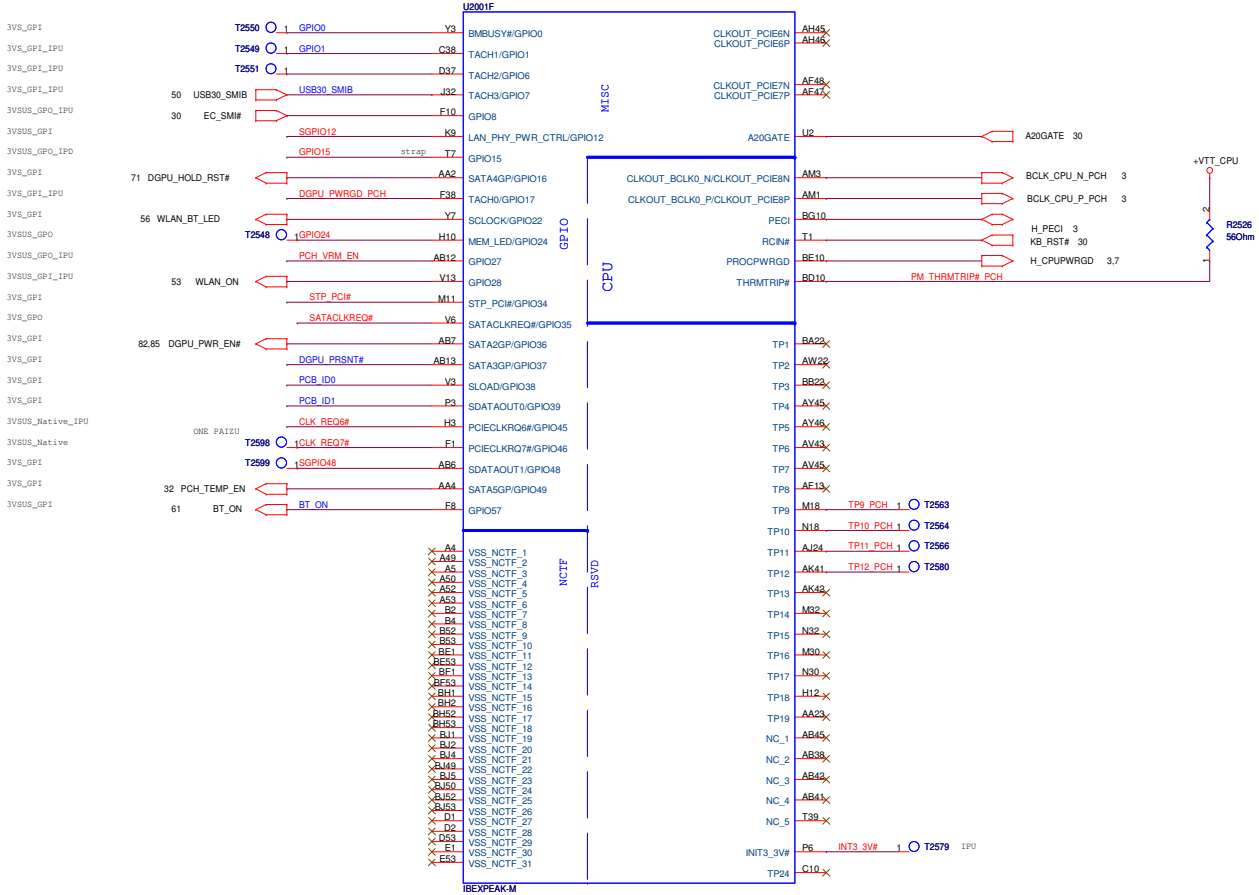
Title : PCH_IBEX(5)_PCI,NVRAM,U		
ASUSTeK COMPUTER INC. NB6	Engineer: JAY_TSAI	
Size: A2	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 24 of 98	

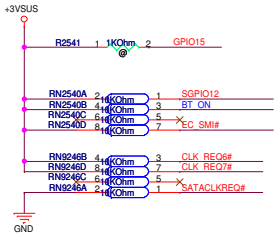
POWER按照提供的default值調節電壓

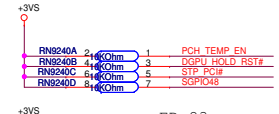


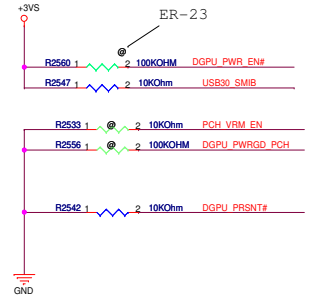
All GPIOs are reset to the default state by CF9h reset except GPIO24.

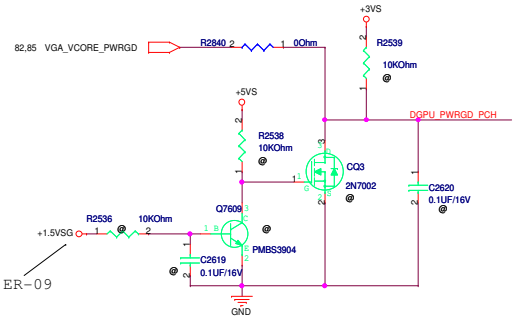
GPIO 27:Enable VCCVRM
Low=disable.
Default internal pull up.



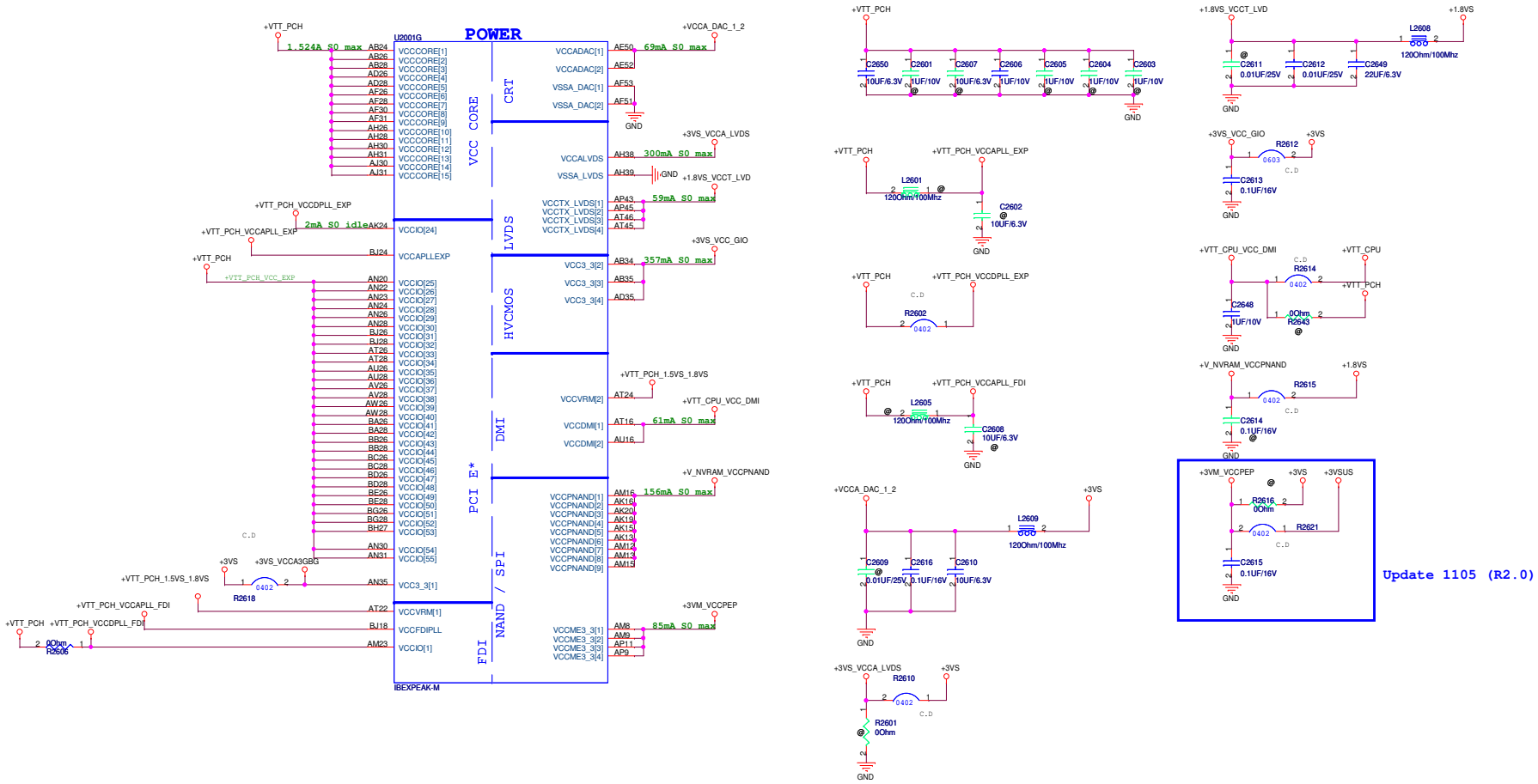




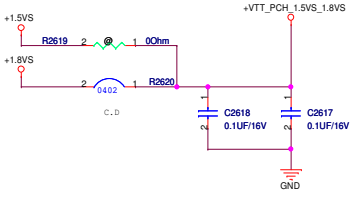




ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(6)CPU,GPIO,MISC		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 25 of 96		



Update 1105 (R2.0)

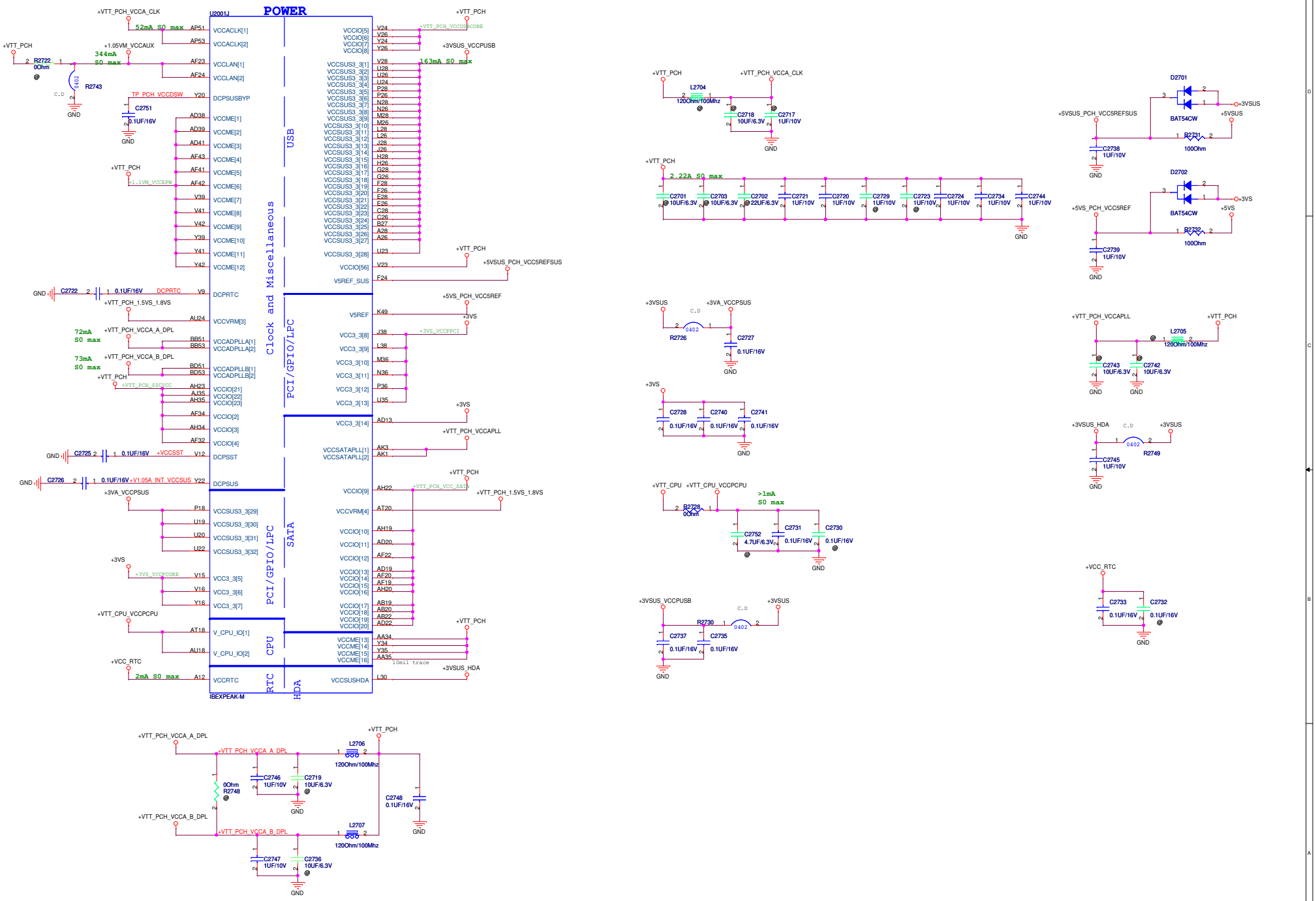


HDA_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)
Low: 1.8V
High: 1.5V

GPIO27 NC:enable internal regulator for:

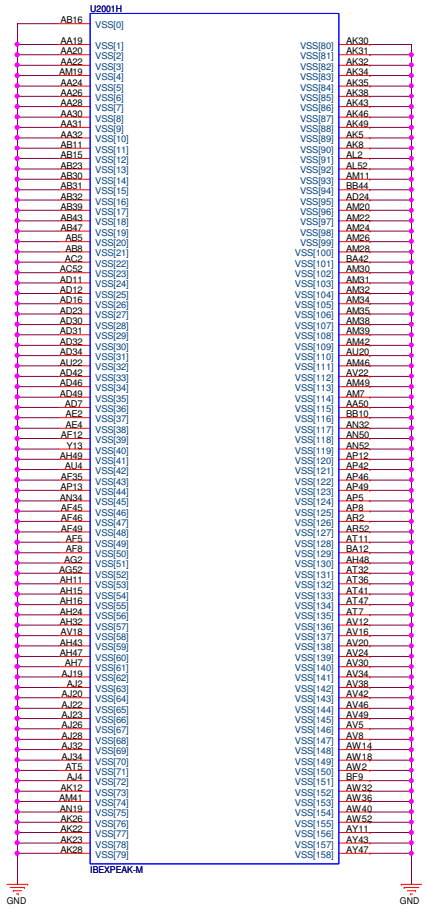
VccAClk	VccapllEXP
VccFDIPLL	VccSATAPLL

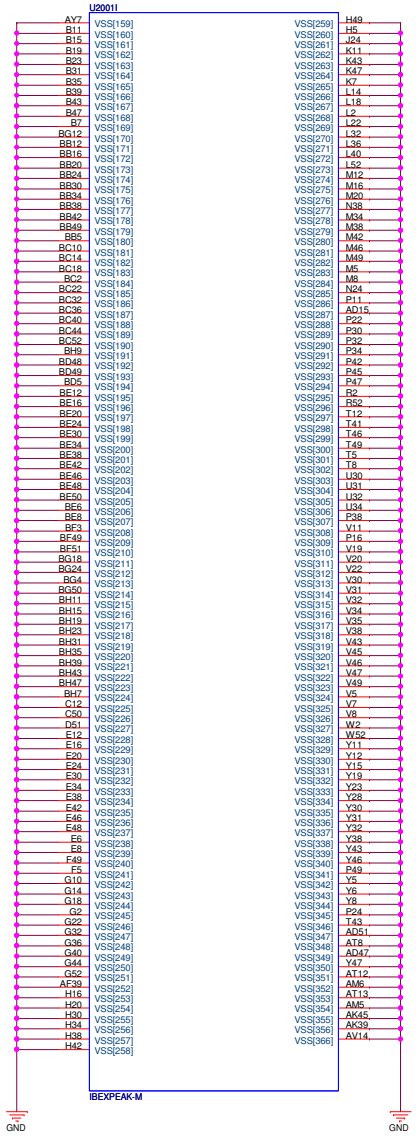
ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(7)_POWER,GND		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 26 of 96		



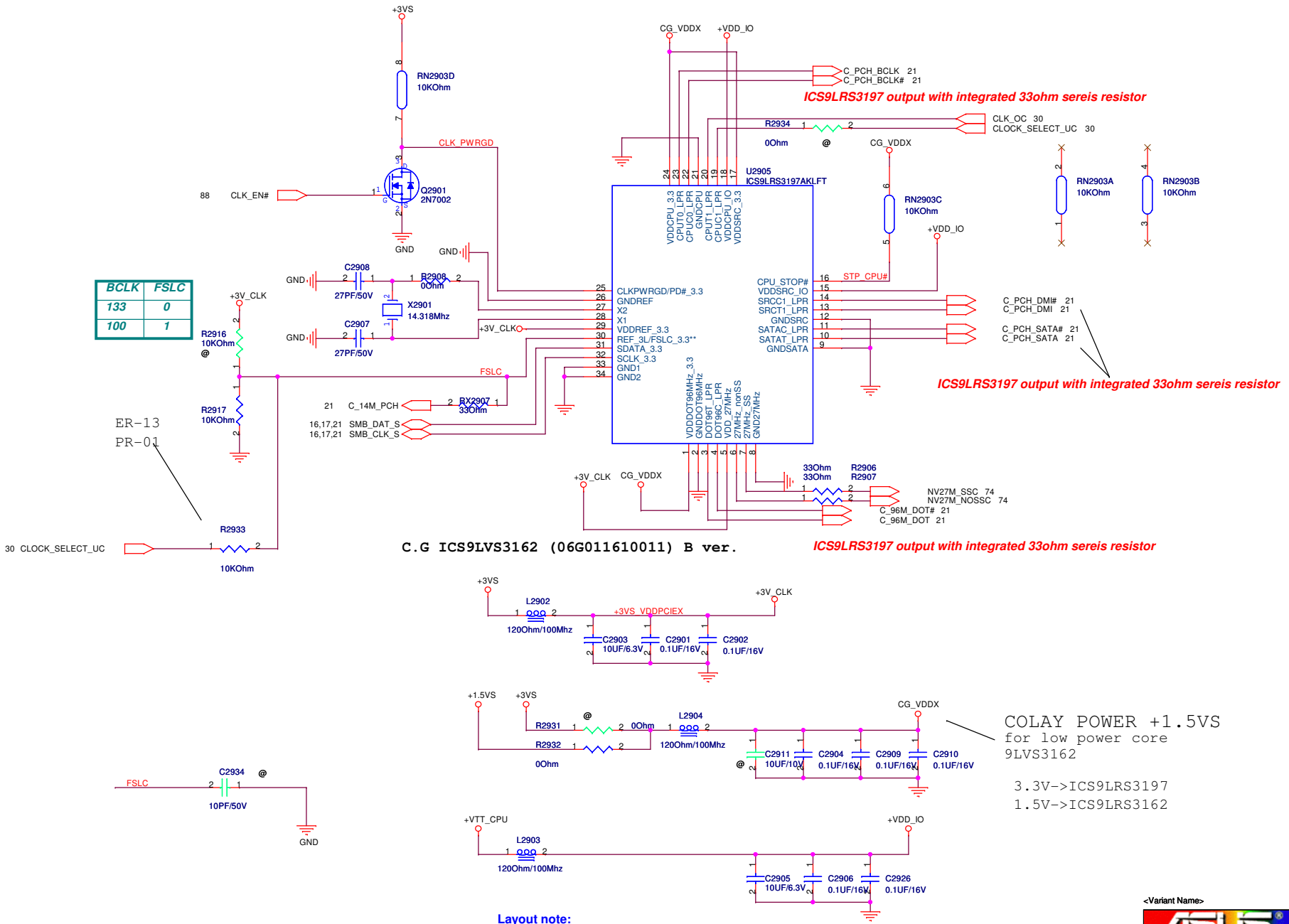
ASUSTeK COMPUTER INC. NB6	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 27 of 96	

Title :PCH_IBEX(8)_POWER,GND



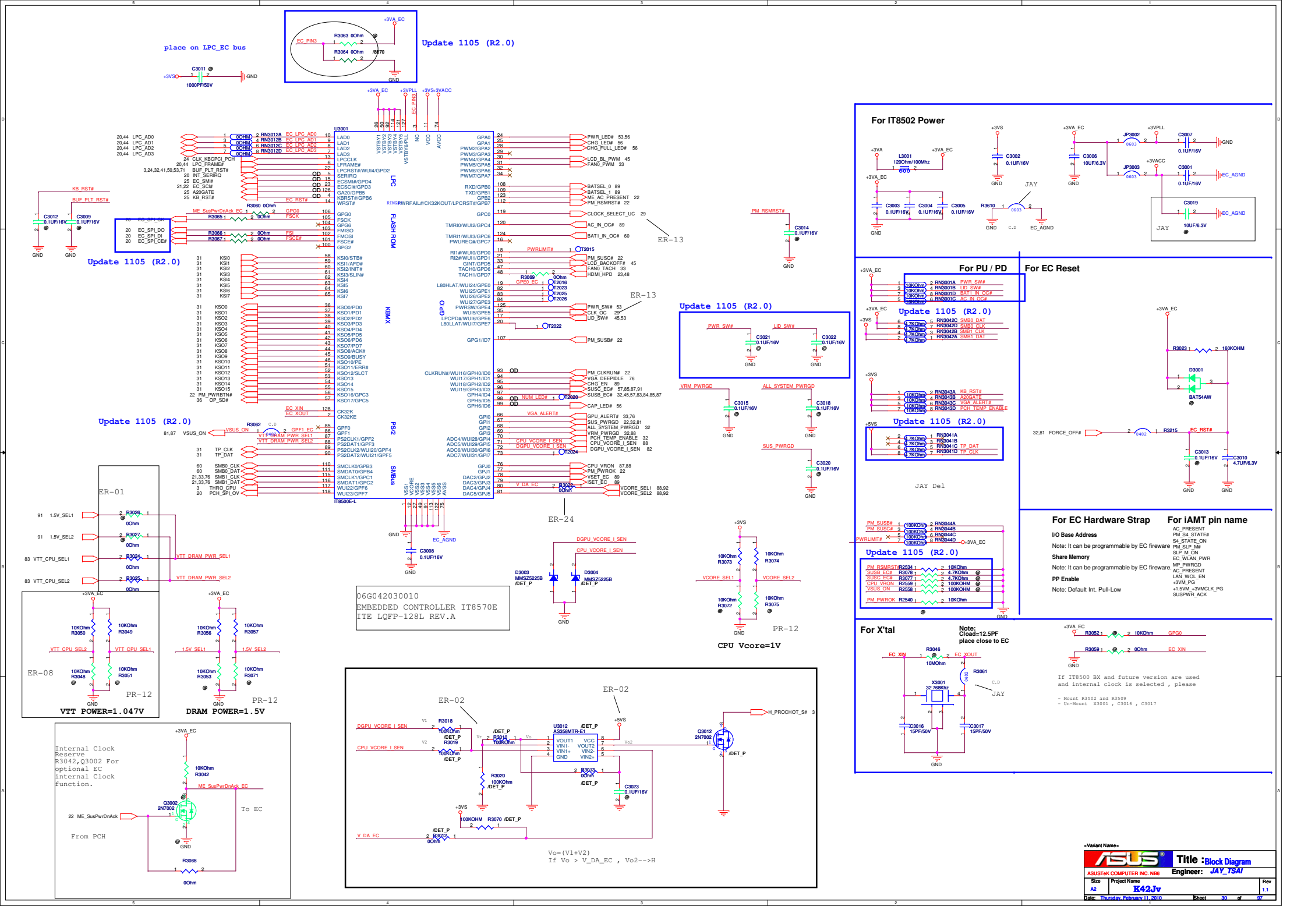


ASUSTeK COMPUTER INC. NB6	Title :PCH GND	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 28 of 96	



<Variant Name>

Title :	ICS9LRS3197
ASUSTek Computer INC.	Engineer: JAY_TSAI
Size: A3	Project Name: K42Jv
Rev: 1.0G	
Date: Thursday, February 11, 2010	Sheet 29 of 96


place on LPC_EC bus
Update 1105 (R2.0)
U3001
IT8500E-L
LPC
FLASH ROM
KBMX
GPIO
PS2
SMBus
ER-01
ER-02
ER-08
ER-12
ER-13
ER-24
VTT POWER=1.047V
DRAM POWER=1.5V
CPU Vcore=1V
06G042030010
EMBEDDED CONTROLLER IT8570E
ITE LQFP-128L REV.A
Internal Clock
Reserve
R3042,Q3002 For
optional EC
internal Clock
function.
To EC
From PCH
Vo=(V1+V2)
If Vo > V_DA_EC , Vo2-->H
For IT8502 Power
For PU / PD
For EC Reset
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
For X'tal
Note:
Cload=12.5PF
place close to EC
JAY Del
If IT8500 BX and future version are used
and internal clock is selected , please
- Mount R3502 and R3509
- Un-Mount X3001 , C3016 , C3017
<Variant Name>
Title : Block Diagram
ASUSTeK COMPUTER INC. NB6
Engineer: JAY_TSAI
Size A2
Project Name K42Jv
Rev 1.1
Date: Thursday, February 11, 2010
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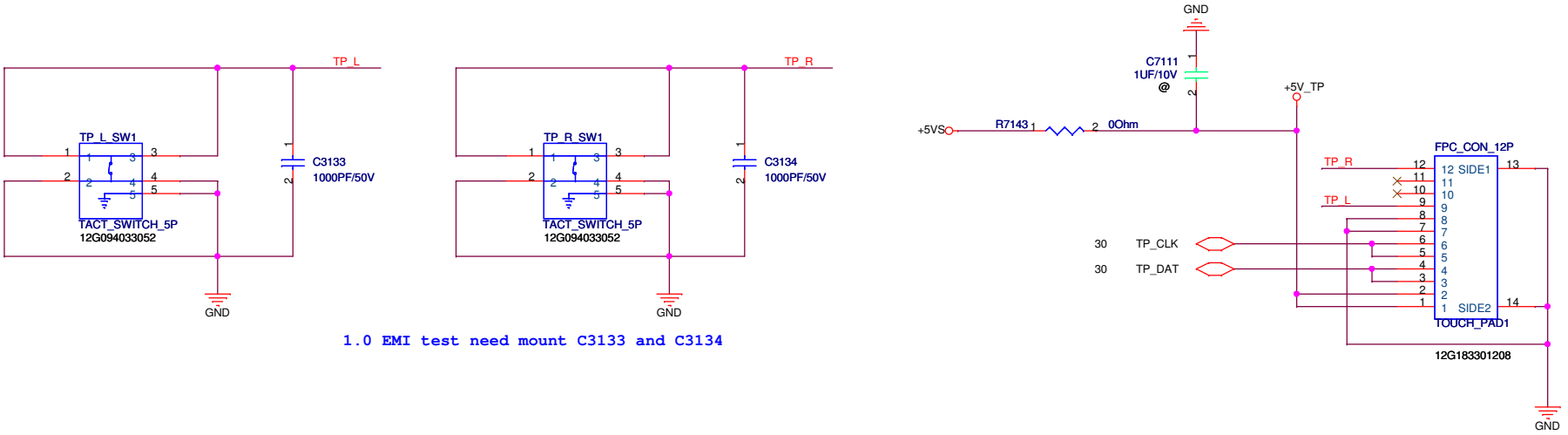
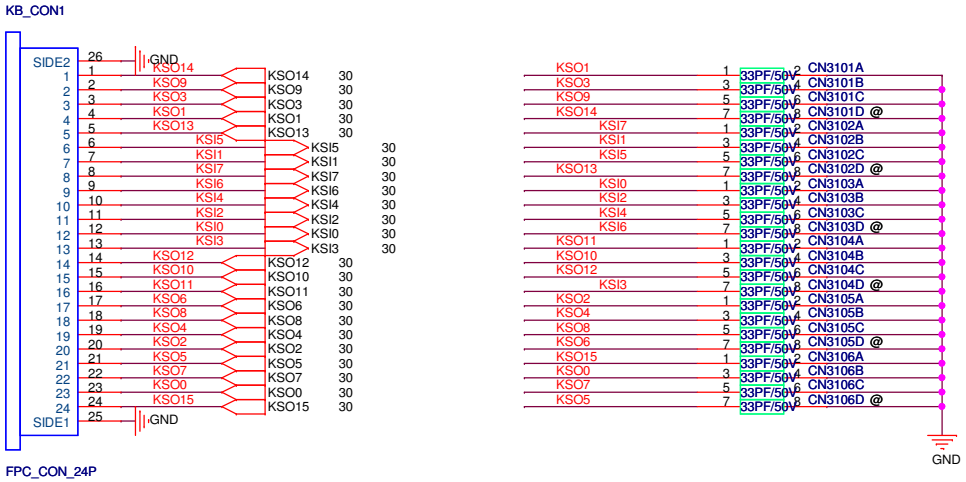
TouchPad



1.0 EMI test need mount C3133 and C3134

Keyboard Connector

EMI Request



<Variant Name>

Title : Block Diagram

ASUSTeK COMPUTER INC. NB6

Engineer: JAY_TSAI

Size	Project Name	Rev
Custom	K42Jv	1.1

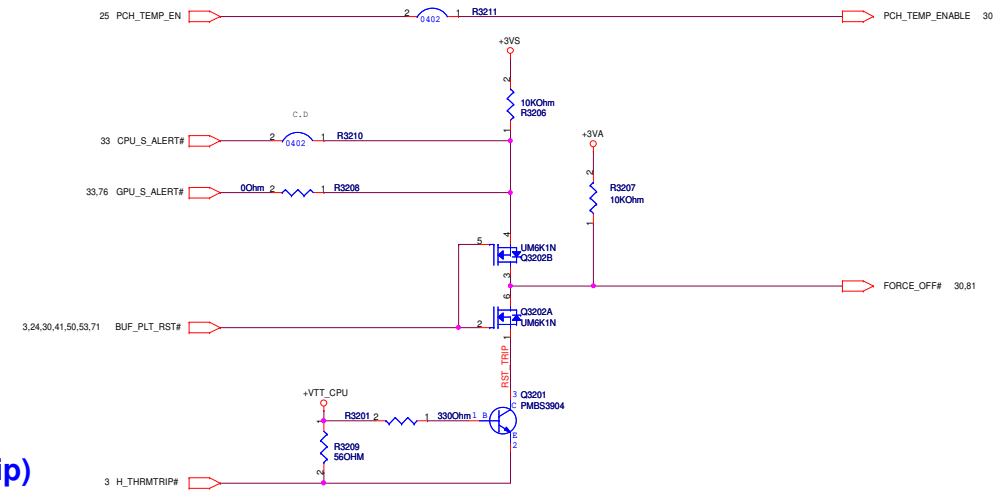
Date: Thursday, February 11, 2010 Sheet 31 of 97

Thermal Policy

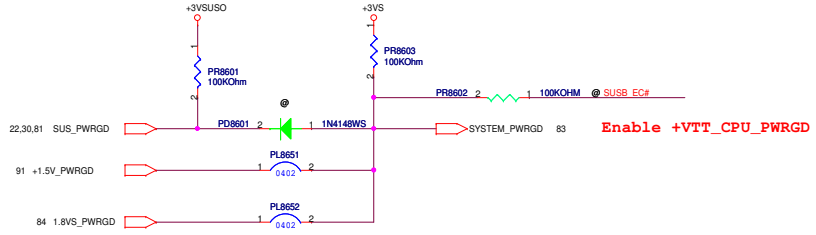
Input 1(sensor)

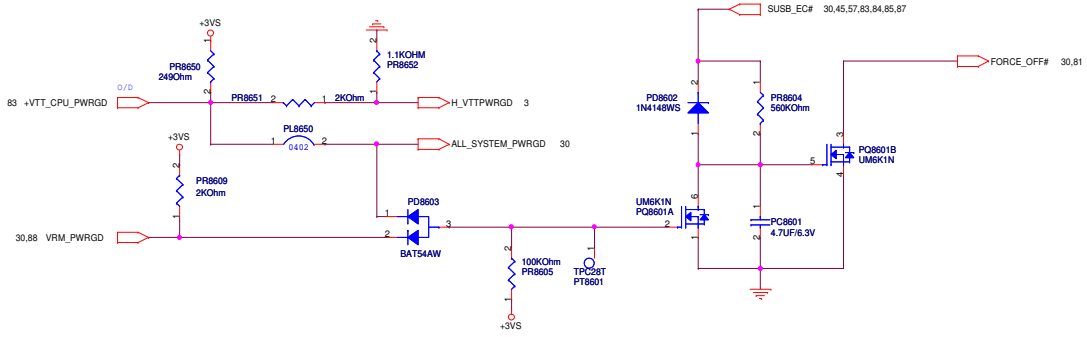
Input 2(thermtrip)

Output (shut down)



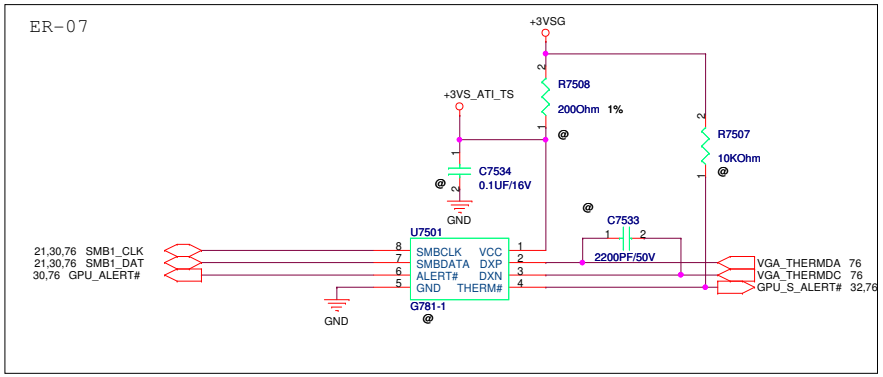
POWER GOOD DETECTER





ASUSTeK COMPUTER INC. NB4	Title : Forceoff#_PWRGD_Thermal	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 32 of 96	

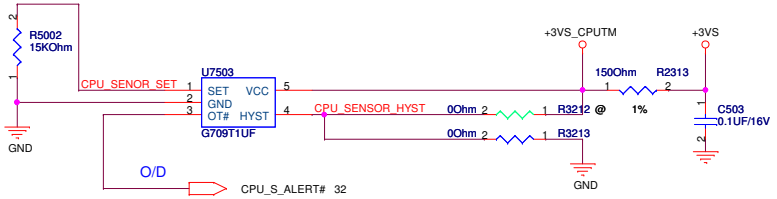
GPU Thermal Sensor



CPU Thermal Sensor

Update 1108 (R2.0)

R5002 for thermal 96C

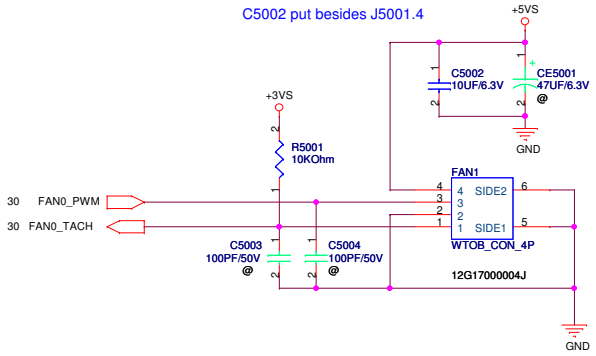


HYST=VCC : 10 degree
HYST=GND : 10 degree C

U7503 under CPU socket

PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.



ASUSTeK COMPUTER INC

Title : FAN_Thermal

Engineer: JAY_TSAI

Size	Project Name	Rev
Custom	K42Jv	108

Date: Thursday, February 11, 2010 Sheet 33 of 96

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	K42Jv	108

Date: Thursday, February 11, 2010 Sheet 34 of 96

Main Board

ASUSTeK COMPUTER INC. NB4	Title : ****	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 35 of 96	

ANALOG MOAT

Update 11.08 (R2.0)

+3VS 50mA
C3639 0.1UF/16V
C3635 0.1UF/16V
GND
Close to pin1,9

+5VS
0Ohm R7977 /ALC269_VB
PU9021 UP7714BMA5-00 /ALC269_VA
EN NC/SS/FB GND VIN VOUT
P_5VASET
PC9027 10UF/16V /ALC269_VA
PC9022 /ALC269_VA 1000PF/50V
PR9020 1% 49.9KOHM /ALC269_VA
PR9021 10.2KOHM 1% /ALC269_VA
PC9028 1UF/16V /ALC269_VA
+5VS_AUDIO PT9021 TPC26T
PC9023 10UF/6.3V /ALC269_VA
PC9024 0.1UF/16V
PC9026 0.1UF/16V
GND_AUDIO
Place next to pin 38,25
Vout=0.8*(1+(49.9K/10.2K))

+5VS L3621 70Ohm/100Mhz +5VS_AMP
C3620 10UF/6.3V @
C3623 10UF/6.3V
C3622 1UF/10V
C3621 0.1UF/16V
GND
Place next to pin 39,46

U3621B
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9
50 51 52 53 54 55 56 57 58
ALC269Q-VA6-GR
GND

For EMI
JP3004 JP3005 JP3006 JP3007 0603
GND GND_AUDIO
CHANGE 0 OHM

PR-04
+3VS +5VS
R3623 @ 100KOhm
R3622 10KOhm /ALC269_VB
ER-11
D3702 BAT54AW
Q3605 2N7002
ACZ_RST#_AUD AMP_PD#_Q OP_SD#
AMP_PD#
ACZ_BCLK_AUD C3636 10PF/50V @
20 ACZ_SDOUT_AUD 20 ACZ_BCLK_AUD 20 ACZ_SDIN0_AUD 20 ACZ_SYNC_AUD 20 ACZ_RST#_AUD
R3621 33Ohm ACZ_SDIN
PC_BEEP
ER-15 PR-03
R3631 0402 SENSE_A
37 A_JD_MIC1
MIC2_INT_L MIC2_INT_R

37 H_SPKL+ H_SPKL- H_SPKR- H_SPKR+
EAPD +5VS_AMP +5VS_AUDIO GND GND_AUDIO

U3621A
GND SPDIFO PVDD2 SPK_OUT_R+ SPK_OUT_R- PVSS1 SPK_OUT_L- SPK_OUT_L+ AVDD2 AVSS2
DVDD GPIO0/DMIC_DATA GPIO1/DMIC_CLK PD# SDATA_OUT BCLK DVSS SDATA_IN DVDD_IO SYNC RESET# PCBEEP
CBP CBN CPVEE HPOUT_R HPOUT_L CPVREF MIC1_VREFO_R MIC2_VREFO MIC1_VREFO_L VREF AVSS1 AVDD1
A_CBP C3628 2.2UF/10V
A_CBN
A_CPVEE C3629 2.2UF/10V
A_CPVREF_VBMICREF
VB_LDO_CAP VREF_CODEC VB_LDO_CAP
C3631 C3650 2.2UF/10V 0.1UF/16V
MIC1_VREFOUT_R 37
MIC2_VREFOUT 37
SPKREA LINE2_R LINE2_L MIC2_L MIC2_R SPKREB JDREF MONO_OUT MIC1_R MIC1_L LINE1_L LINE1_R
ALC269Q-VA6-GR
PR-02

R3624 20KOhm 1%
A_JDREF
AC_MIC_HP_R AC_MIC_HP_L

Update 11.08 (R2.0)
A_CPVREF_VBMICREF 0Ohm R7979 /ALC269_VA GND_AUDIO
0Ohm R7980 /ALC269_VB
VB_LDO_CAP 0Ohm R7978 /ALC269_VA MIC1_VREFOUT_L 37
10UF/6.3V C3624 /ALC269_VB GND_AUDIO
PIN28 ,PIN31 MODIDY

MIC2_VREFOUT AC53 100PF/50V @ GND_AUDIO

PR-13
269_VB2 : 02G611005010
269_VB5 : 02G611005015

PC BEEP

20 SB_SPKR R3643 4.7KOhm SB_SPKR PC_BEEP_C C3646 0.1UF/16V PC_BEEP
R3642 4.7KOhm GND

INTERNAL MIC

MIC2_INT_R C3641 1UF/10V MIC_IN_AC 37
MIC2_INT_L C3642 1UF/10V
AC45 0.1UF/16V @ GND_AUDIO

MIC1_INT_R C3644 1UF/10V EX_MIC_IN_AC 37
MIC1_INT_L C3643 1UF/10V
AC46 0.1UF/16V @ GND_AUDIO
EXT. MIC

PR-06

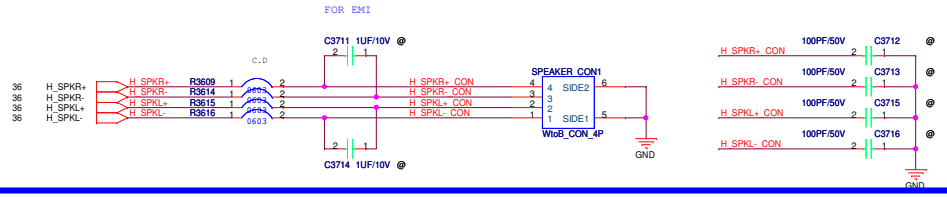
MUTE
+3VSUS +12V
R3625 10KOhm
R3627 2.2MOhm
R3626 10KOhm MUTE_POP#
Q3608A UM6K1N Q3608B UM6K1N
C3647 0.1UF/16V
EAPD OP_SD# D3703 BAT54AW
ACZ_RST#_AUD R3644 100KOhm
GND

Option 1
Q3606A UM6K1N Q3607A UM6K1N
AC_MIC_HP_R AC_MIC_HP_R_Q
MUTE_POP#
AC_MIC_HP_L AC_MIC_HP_L_Q
Q3606B UM6K1N Q3607B UM6K1N
C3637 100UF/6.3V A_MIC_HP_R 37
C3638 100UF/6.3V A_MIC_HP_L 37

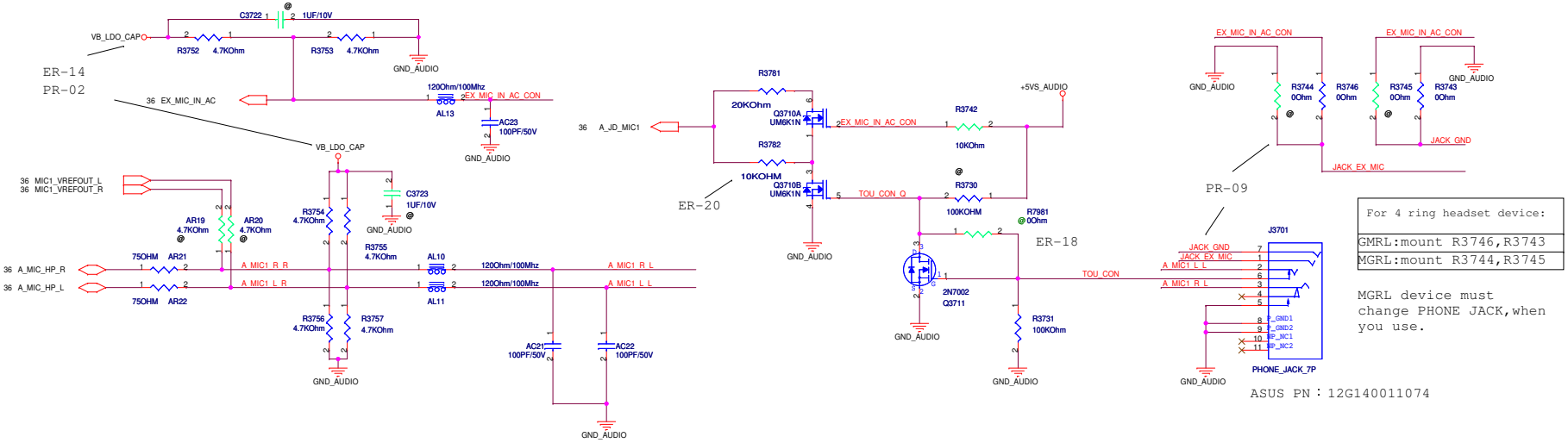
bypass Q3606,3607
AC_MIC_HP_R 0Ohm R3628 @ AC_MIC_HP_R_Q
AC_MIC_HP_L 0Ohm R3629 @ AC_MIC_HP_L_Q
Option 2

<Variant Name>
ASUSTeK COMPUTER INC. NB2
Title : CODEC ALC 269
Engineer: JAY_TSAI
Size C | Project Name K42Jv | Rev 1.01
Date: Thursday, February 11, 2010 | Sheet 36 of 96

SPEAKER



HP and MIC

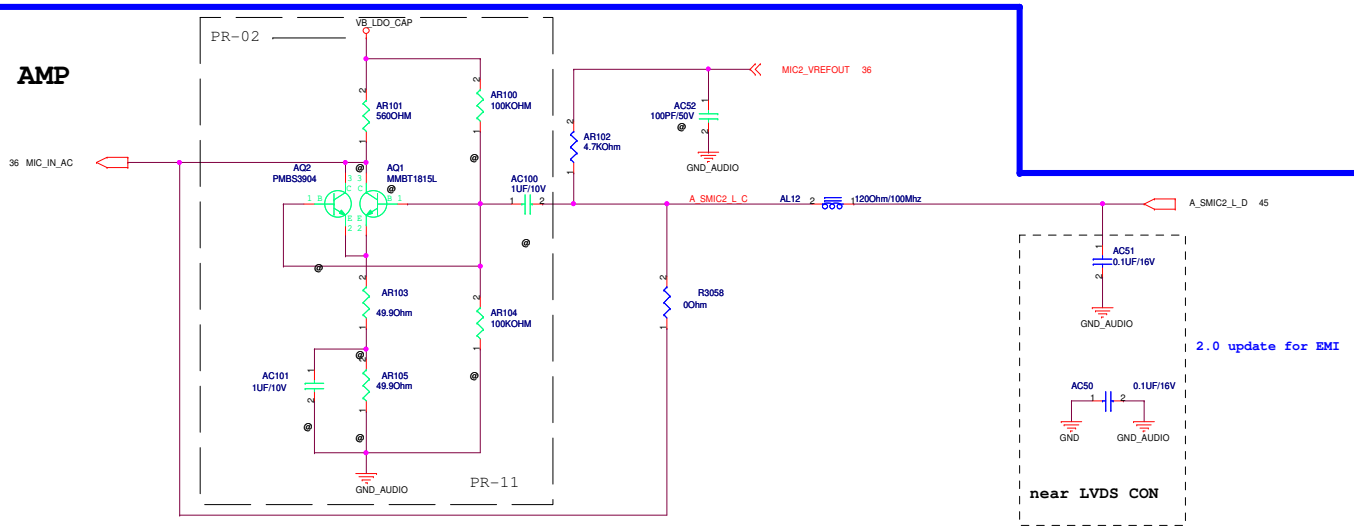


For 4 ring headset device:
GMRL:mount R3746,R3743
MGRL:mount R3744,R3745

MGRL device must change PHONE JACK,when you use.

ASUS PN：12G140011074

Internal MIC and AMP



ASUS	Title : AUDIO AMP	
ASUSTeK COMPUTER INC. NB2	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 37 of 96	

Main Board

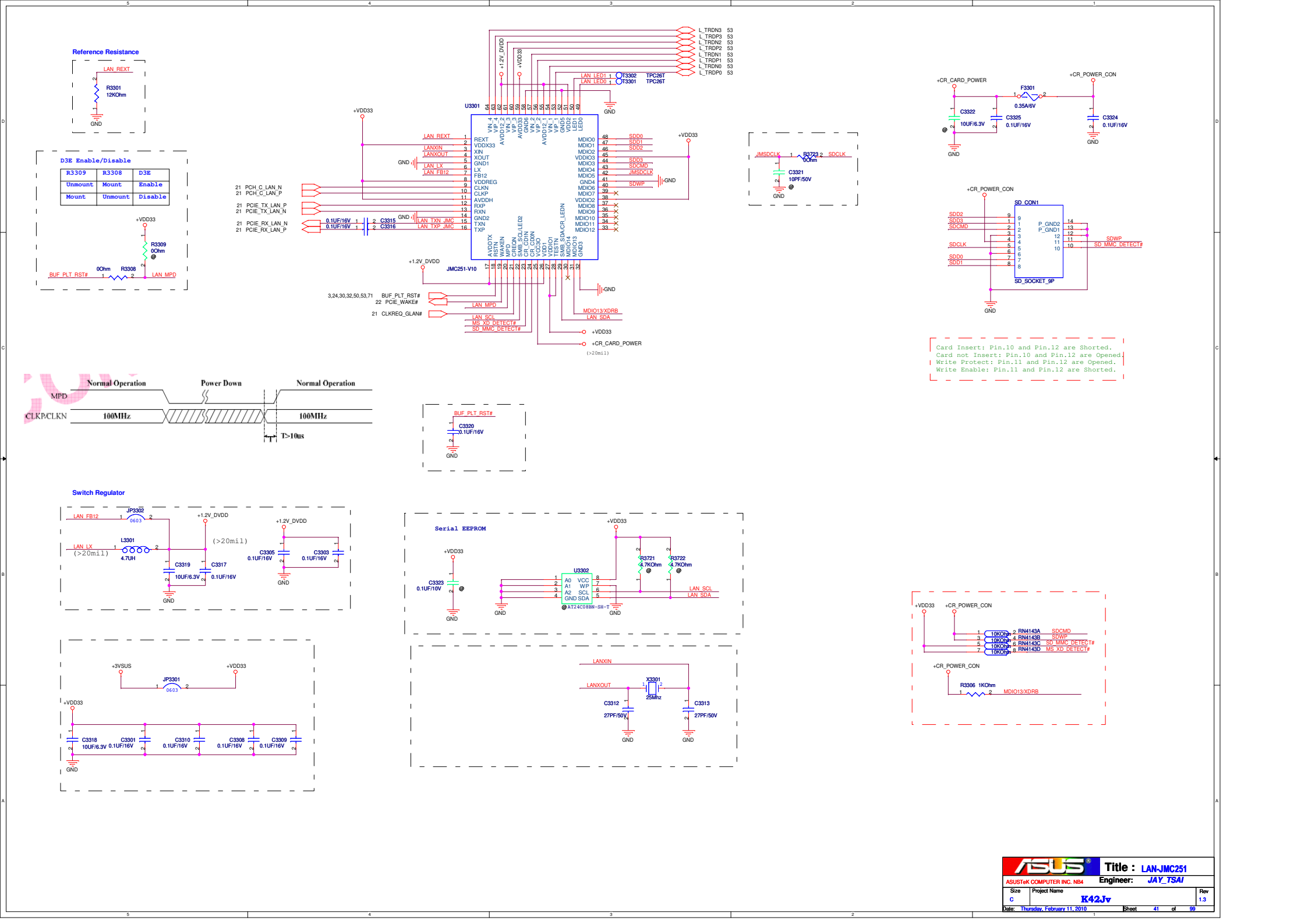
ASUSTeK COMPUTER INC. NB4	Title :	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 38 of 96	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : AUD_****		
	Engineer: JAY_TSAI		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 39 of 96		

<Variant Name>

ASUSTek Computer Inc.	Title : ***	
	Engineer: JAY_TSAI	
Size: A3	Project Name: K42Jv	Rev: 1.0G
Date: Thursday, February 11, 2010	Sheet 40 of 96	

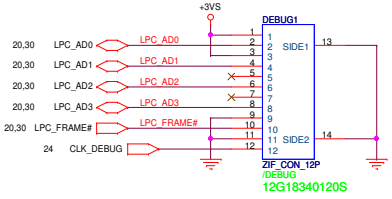


ASUSTeK COMPUTER INC. NB4	Title : LAN-JMC251	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.3
Date: Thursday, February 11, 2010	Sheet 41 of 99	

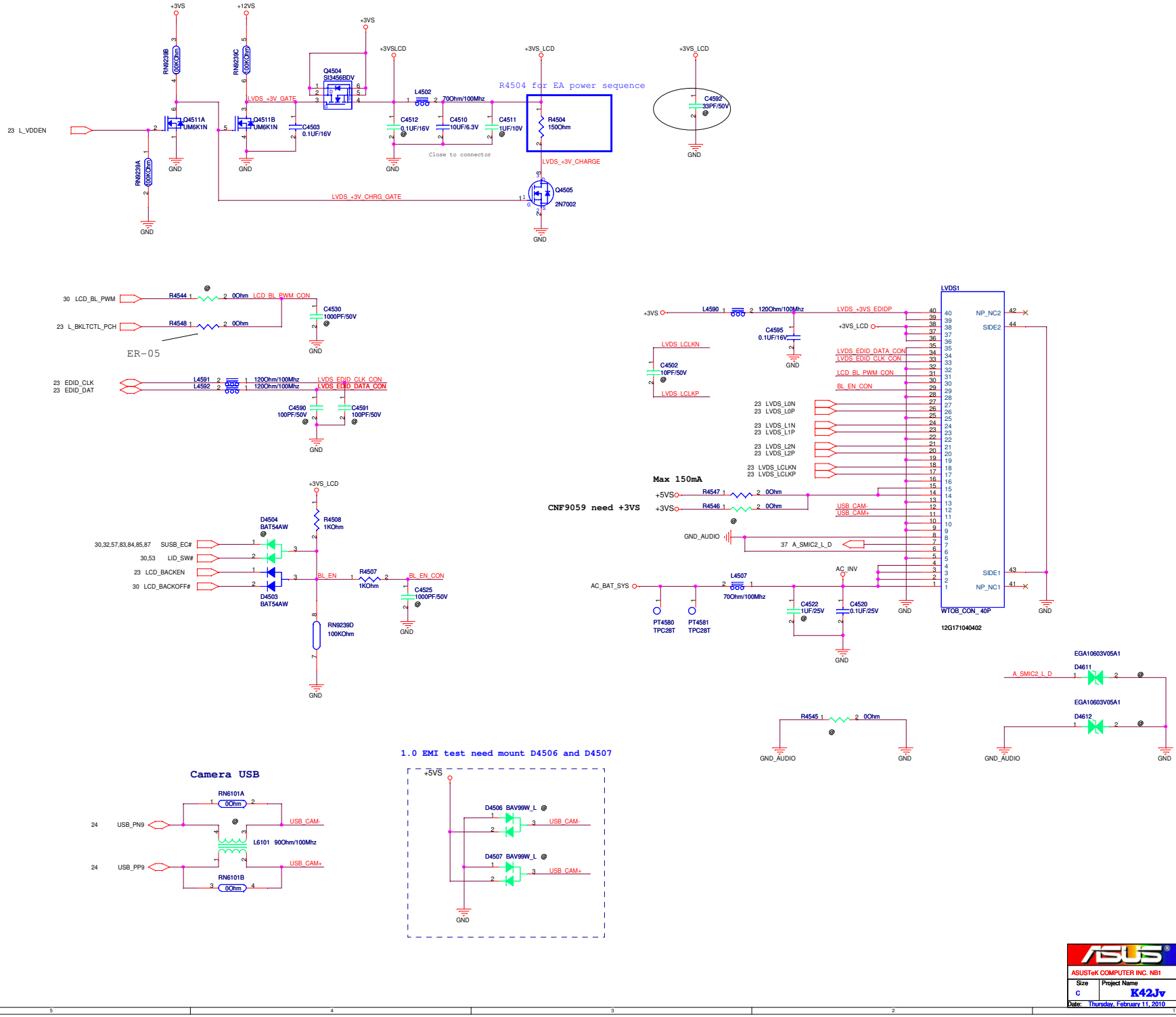
Title :	***
ASUSTeK COMPUTER INC. NB4	Engineer: JAY_TSAI
Size: Custom	Project Name: K42Jv
Rev: 1.3	
Date: Thursday, February 11, 2010	Sheet 42 of 99

ASUSTeK COMPUTER INC. NB4	Title : ***		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 43 of 96		

LPC Debug Port

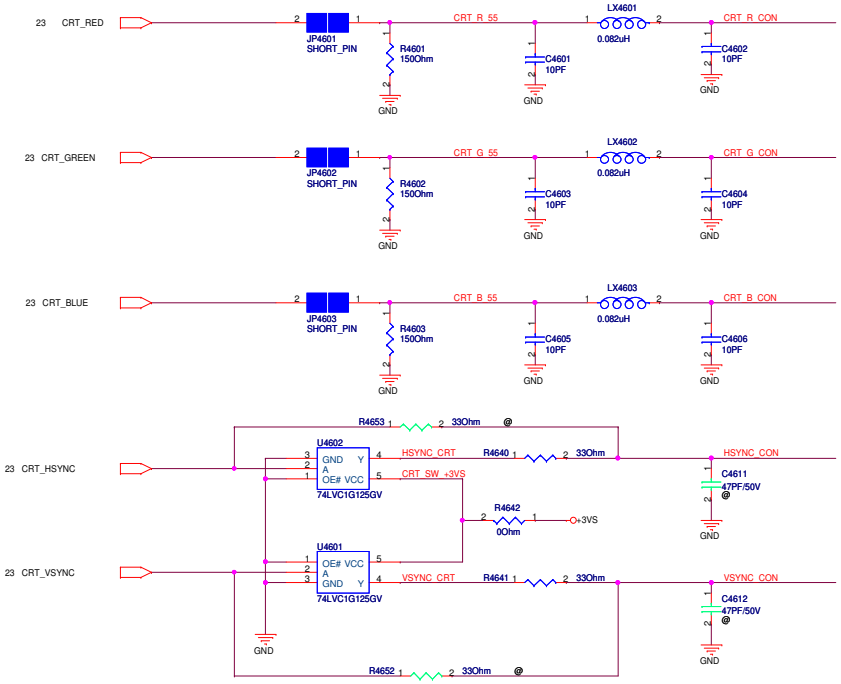


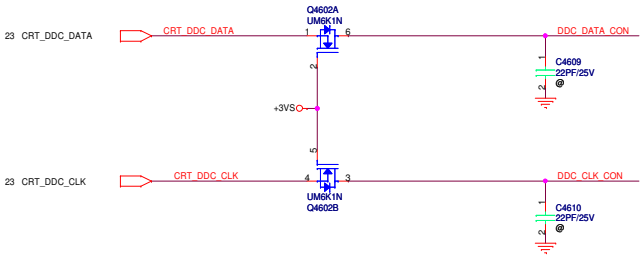
ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 44 of 96	

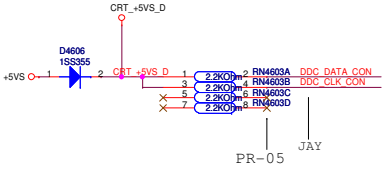


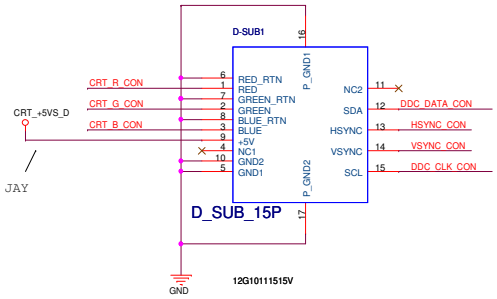
ASUSTeK COMPUTER INC. NB1	Title: LVDS & Inverter CON	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.00
Date: Thursday, February 11, 2010	Sheet 45 of 94	

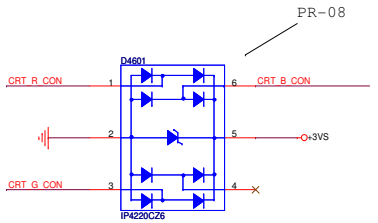
Main Board

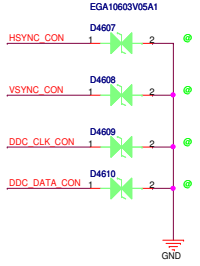






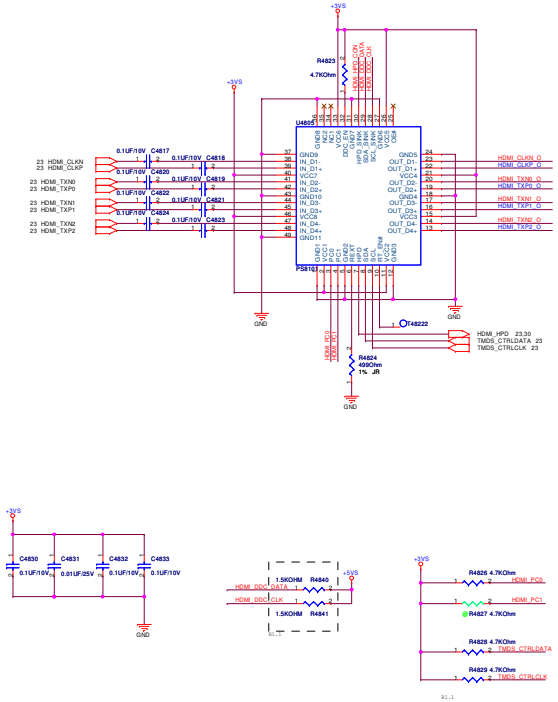


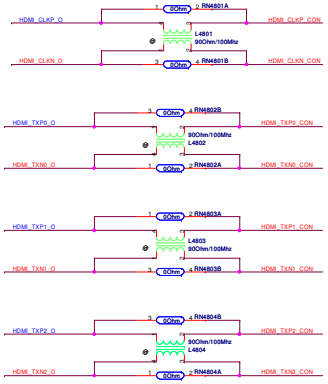


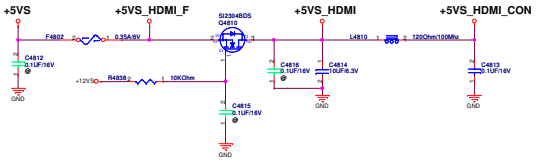


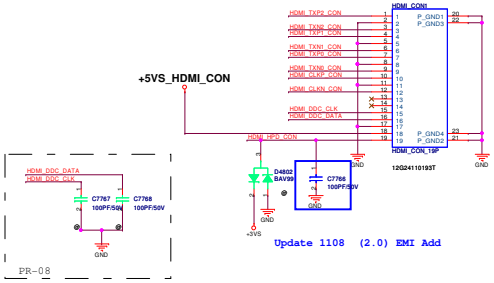
ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 46 of 96	

ASUSTeK COMPUTER INC. NB4	Title : ***		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 47 of 96		









Update 1108 (2.0) EMI Add

ASUSTeK COMPUTER INC. NB4	Title : TV_HDMI		
	Engineer: JAY_TSAI		
Size: D	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 48 of 96		

Main Board

Title : TV_****

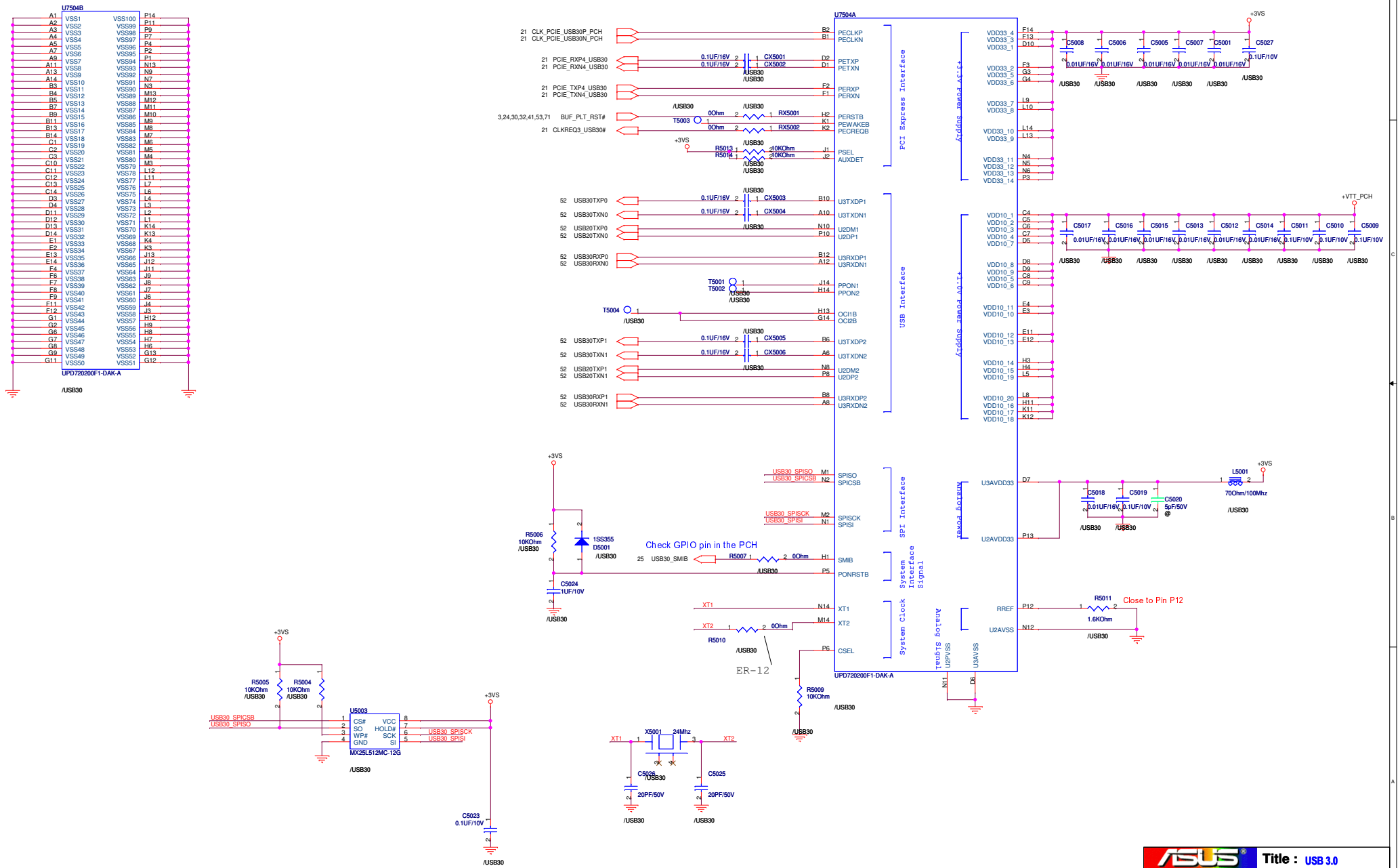
ASUSTeK COMPUTER INC. NB4

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

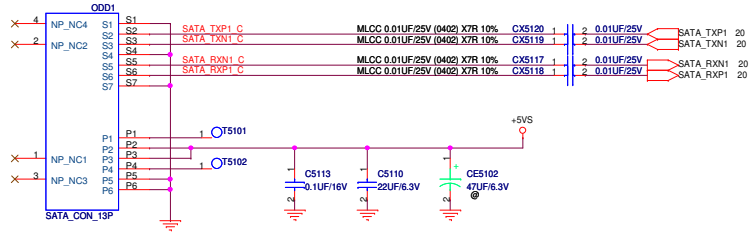
Date: Thursday, February 11, 2010 Sheet 49 of 96

Main Board

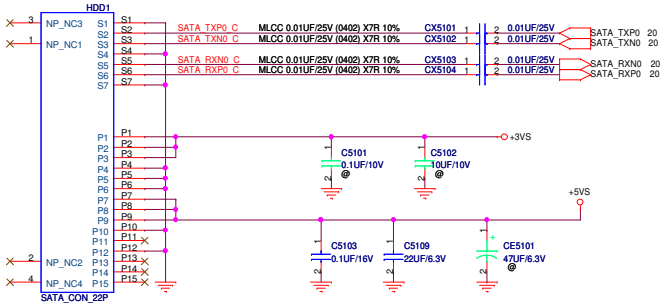


ASUSTeK COMPUTER INC. NB4	Title : USB 3.0		
	Engineer: Frank_Ma		
Size: C	Project Name: K42JV		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 50 of 96		

ODD



HDD (1st)



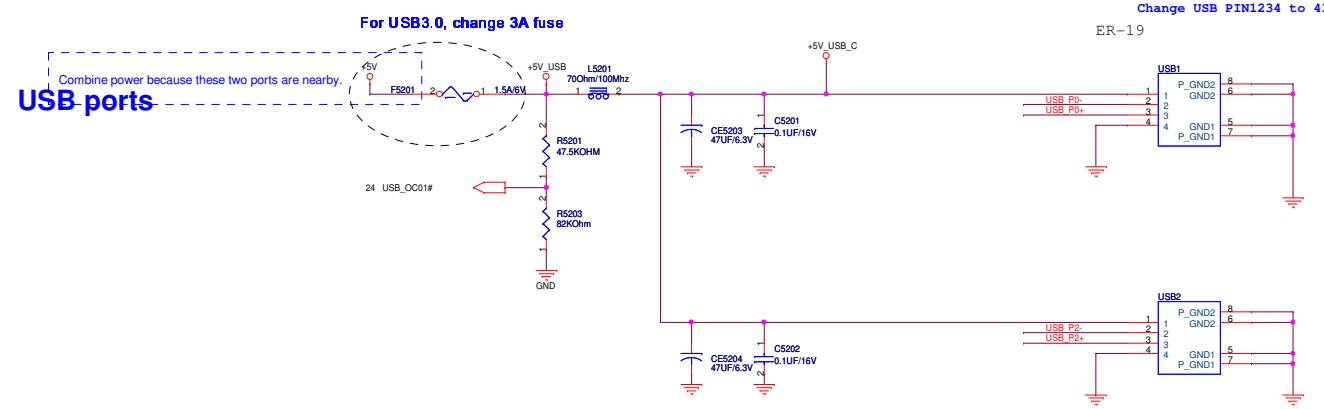
ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 51 of 96	

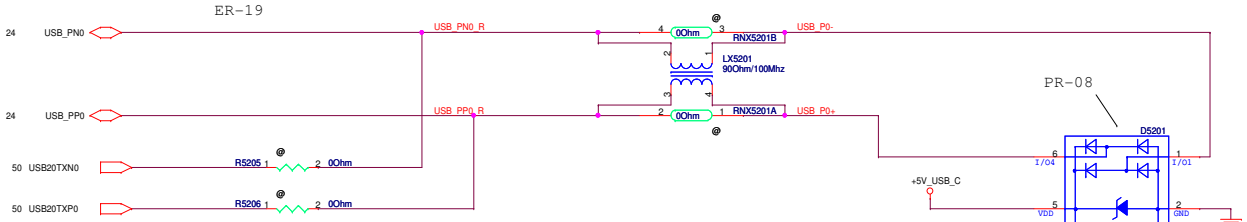
USB2.0 CON PN:12G131030042
Change USB PIN1234 to 4321

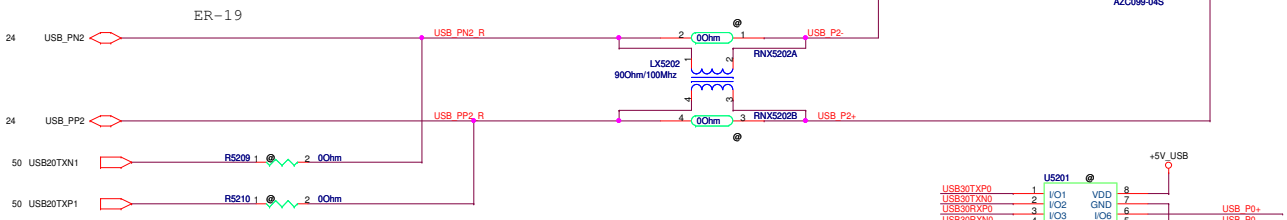
For USB3.0, change 3A fuse

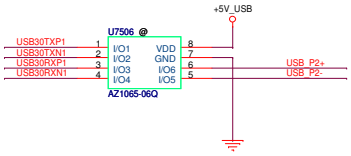
Combine power because these two ports are nearby.

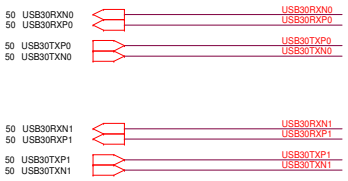
USB ports





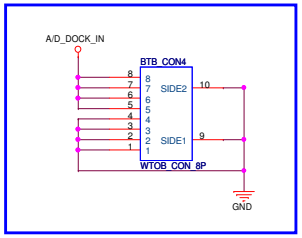




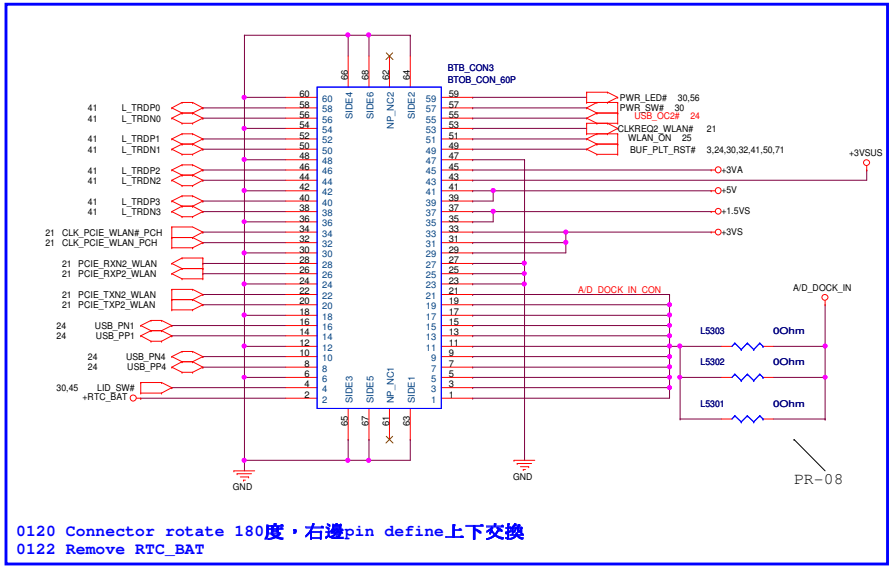


ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *2	
	Engineer: Frank_Ma	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 52 of 96	

0125 Add 8 pin WtoB connector



PR-07



0120 Connector rotate 180度，右邊pin define上下交換
0122 Remove RTC_BAT

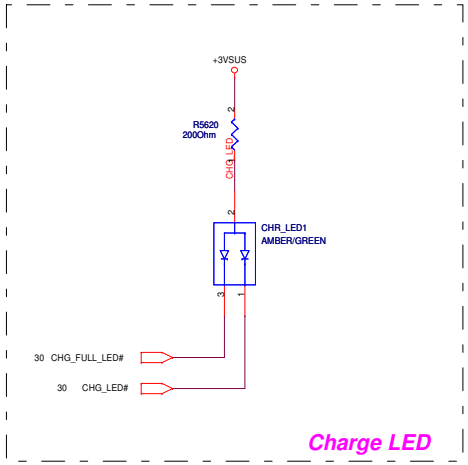
ASUSTeK COMPUTER INC. NB6	Title : B TO B	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 53 of 96	

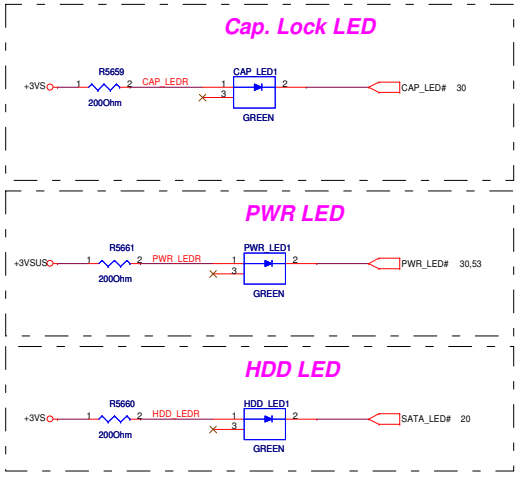
Main Board

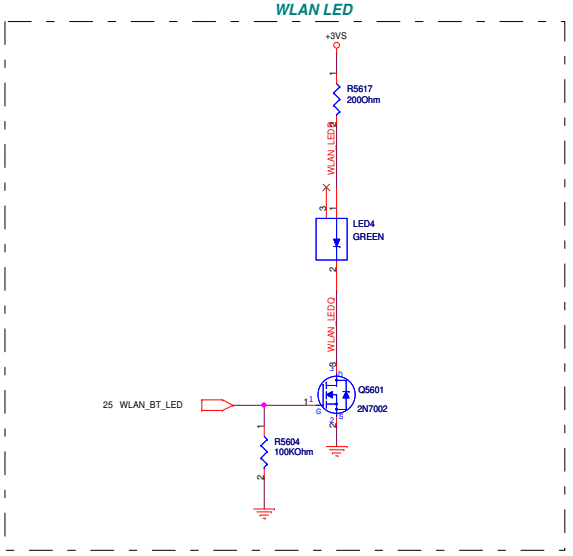
ASUSTeK COMPUTER INC. NB4	Title : BAR_****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 54 of 96		

Main Board

ASUSTeK COMPUTER INC. NB4	Title : SIO_****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 55 of 96		





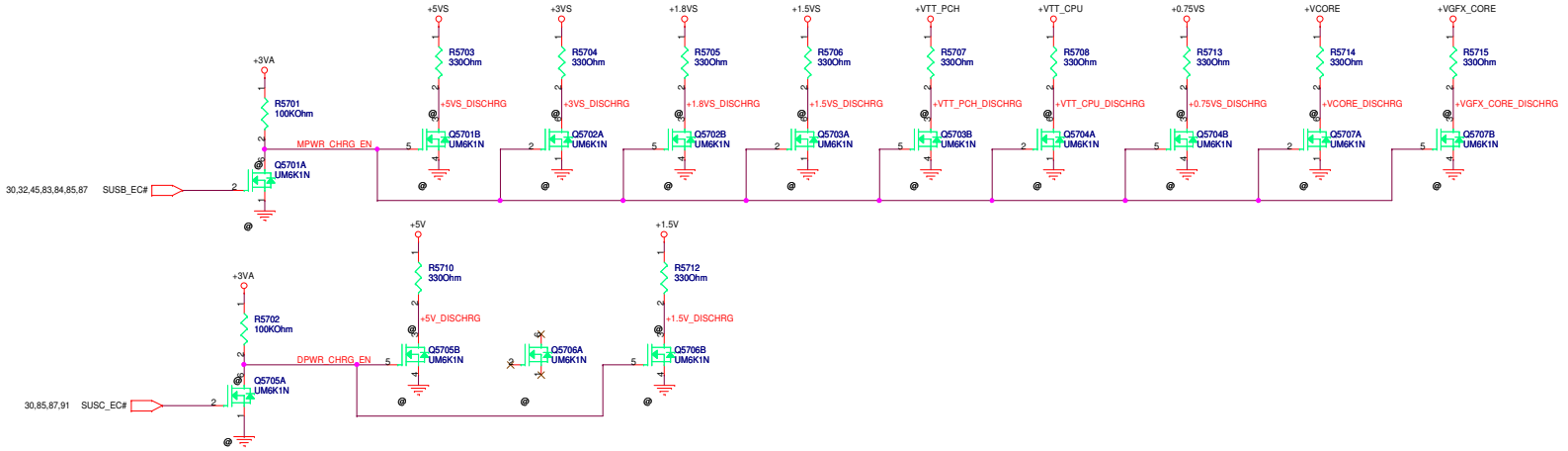


Change LED part number

ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 56 of 96	

Main Board

Remove +2.5Vs is for ATI GFX



ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 57 of 96	

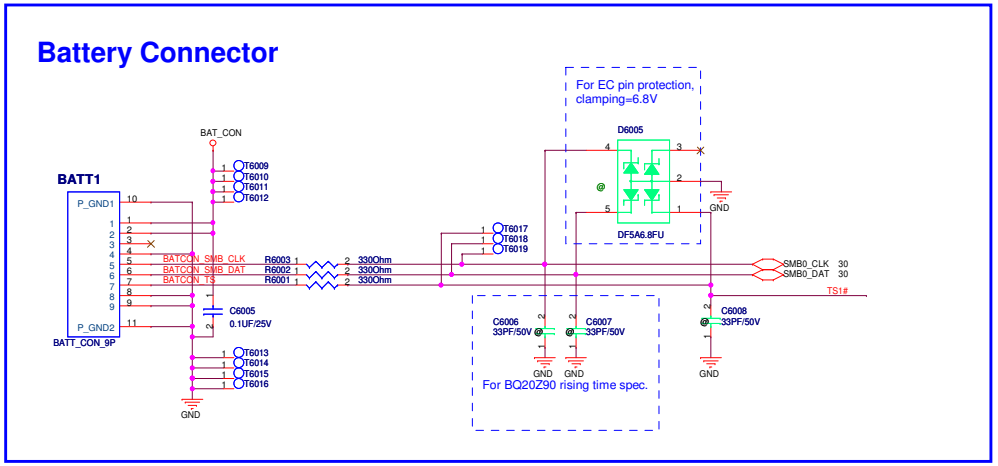
Main Board

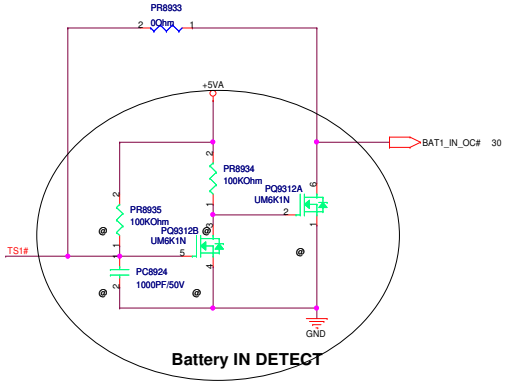
ASUSTeK COMPUTER INC. NB4	Title : PCI_****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 58 of 96		

Main Board

ASUSTeK COMPUTER INC. NB4	Title : DJ_****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 59 of 96		

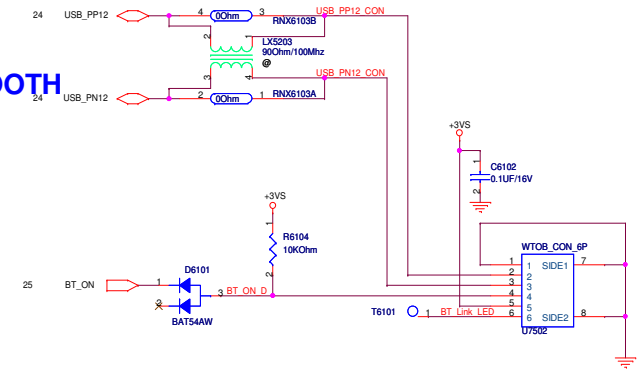
Battery Connector





ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 60 of 96	

BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 61 of 96		

Main Board

Title : TPM_****

ASUSTeK COMPUTER INC. NB4

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 62 of 96

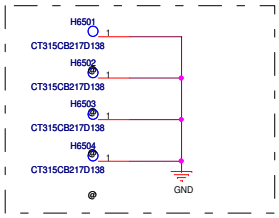
Main Board

ASUSTeK COMPUTER INC. NB4	Title : ***		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 63 of 96		

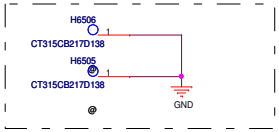
ASUSTeK COMPUTER INC. NB4	Title : ***		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 64 of 96		

Main Board

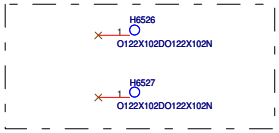
For CPU



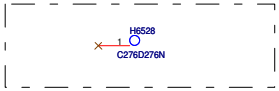
For GPU

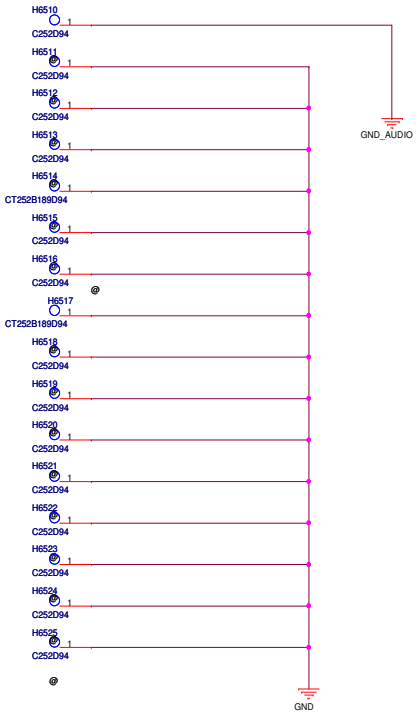


For 橢圓定位孔

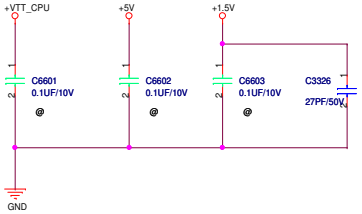


HHD 呼吸孔





ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 65 of 96	



ASUSTeK COMPUTER INC. NB4	Title : EMI	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 66 of 96	

Title :***

ASUSTeK COMPUTER INC. NB4

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 67 of 96

Title : OTH_LCM

ASUSTeK COMPUTER INC. NB4

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 68 of 96

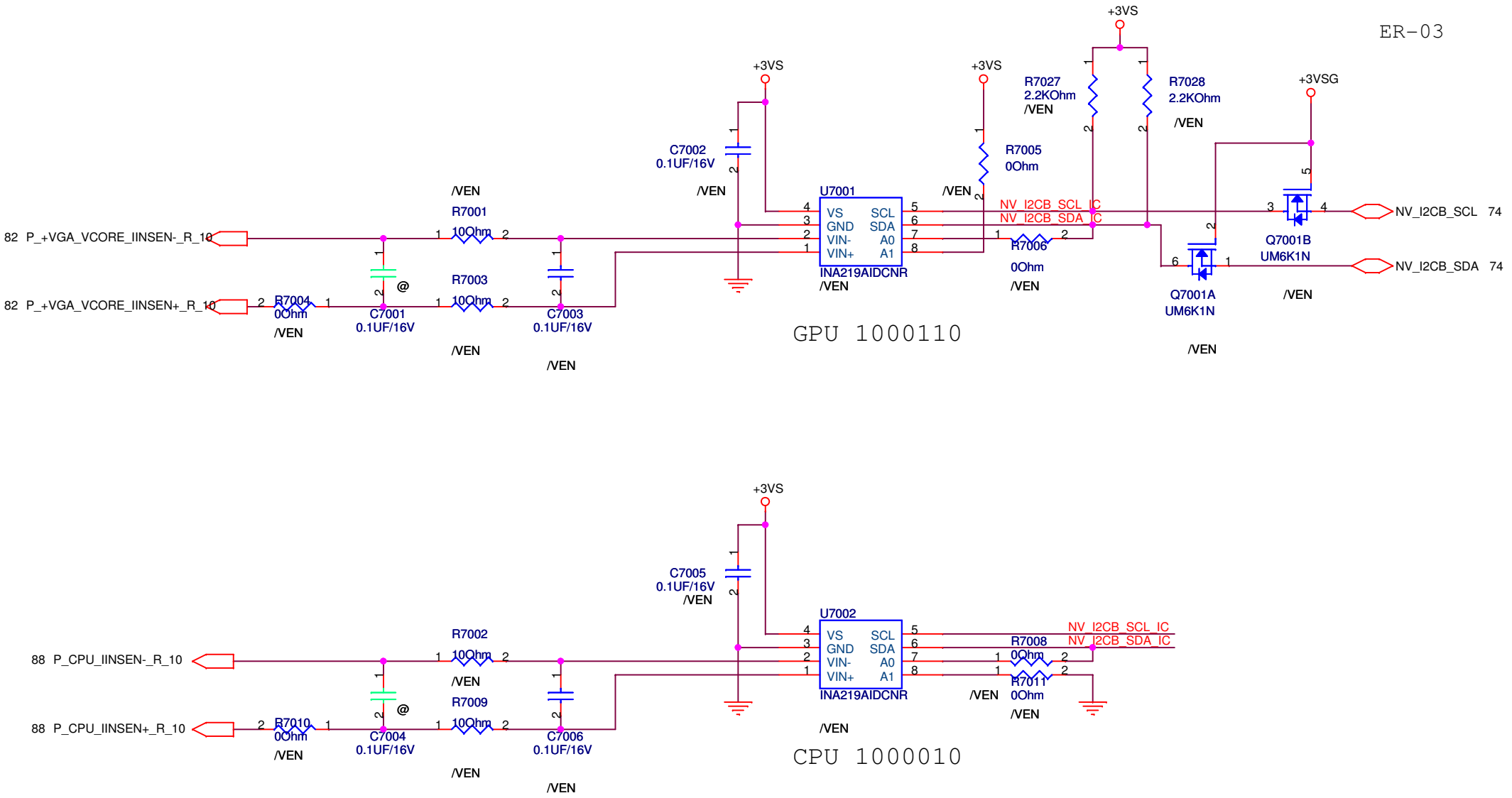
Title : OTH_GAME-LED*****

ASUSTeK COMPUTER INC. NB4

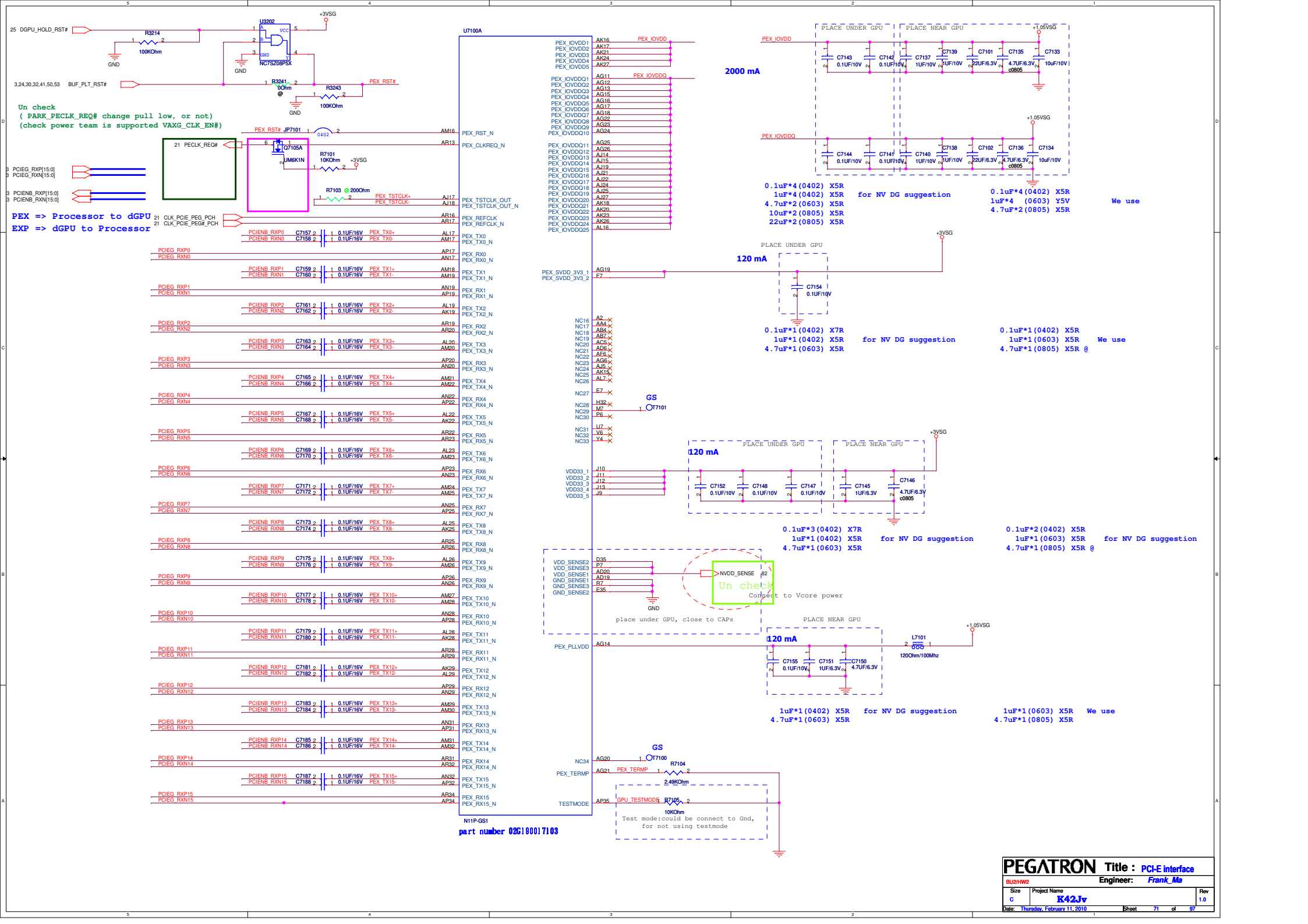
Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 69 of 96



ASUSTeK COMPUTER INC. NB4	Title : VENTURA	
	Engineer: JAY_TSAI	
Size: A4	Project Name: K42JV	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 70 of 96	


25 DGPU_HOLD_RST#
R3214
100KOhm
U3202
NC7SZ08P5X
+3VSG
GND
3,24,30,32,41,50,53 BUF_PLT_RST#
R3241
0Ohm
@
R3243
100KOhm
PEX_RST#
Un check
(PARK_PECLK_REQ# change pull low, or not)
(check power team is supported VAXG_CLK_EN#)
PEX_RST# JP7101
0402
21 PECLK_REQ#
Q7105A
UM6K1N
R7101
10KOhm
R7103 @ 200Ohm
PEX_TSTCLK+
PEX_TSTCLK-
3 PCIEG_RXP[15:0]
3 PCIEG_RXN[15:0]
3 PCIENB_RXP[15:0]
3 PCIENB_RXN[15:0]
PEX => Processor to dGPU
EXP => dGPU to Processor
21 CLK_PCIE_PEG_PCH
21 CLK_PCIE_PEG#_PCH
U7100A
PEX_RST_N
PEX_CLKREQ_N
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
PEX_REFCLK
PEX_REFCLK_N
PEX_IOVDD
PEX_IOVDDQ
2000 mA
PLACE UNDER GPU
PLACE NEAR GPU
C7143 0.1UF/10V
C7142 0.1UF/10V
C7137 1UF/10V
C7139 1UF/10V
C7101 22UF/6.3V
C7135 4.7UF/6.3V c0805
C7133 10uF/10V
C7144 0.1UF/10V
C7141 0.1UF/10V
C7140 1UF/10V
C7138 1UF/10V
C7102 22UF/6.3V
C7136 4.7UF/6.3V c0805
C7134 10uF/10V
0.1uF*4(0402) X5R
1uF*4(0402) X5R for NV DG suggestion
4.7uF*2(0603) X5R
10uF*2(0805) X5R
22uF*2(0805) X5R
0.1uF*4(0402) X5R
1uF*4 (0603) Y5V We use
4.7uF*2(0805) X5R
PEX_SVDD_3V3_1
PEX_SVDD_3V3_2
120 mA
C7154 0.1UF/10V
0.1uF*1(0402) X7R
1uF*1(0402) X5R for NV DG suggestion
4.7uF*1(0603) X5R
0.1uF*1(0402) X5R
1uF*1(0603) X5R We use
4.7uF*1(0805) X5R @
GS
T7101
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
C7152 0.1UF/10V
C7148 0.1UF/10V
C7147 0.1UF/10V
C7145 1UF/6.3V
C7146 4.7UF/6.3V c0805
0.1uF*3(0402) X7R
1uF*1(0402) X5R for NV DG suggestion
4.7uF*1(0603) X5R
0.1uF*2(0402) X5R
1uF*1(0603) X5R for NV DG suggestion
4.7uF*1(0805) X5R @
VDD_SENSE2
VDD_SENSE3
VDD_SENSE1
GND_SENSE1
GND_SENSE3
GND_SENSE2
NVDD_SENSE
82
Un check
Connect to Vcore power
place under GPU, close to CAPs
PEX_PLLVDD
120 mA
L7101
120Ohm/100Mhz
C7155 0.1UF/10V
C7151 1UF/6.3V
C7150 4.7UF/6.3V
1uF*1(0402) X5R for NV DG suggestion
4.7uF*1(0603) X5R
1uF*1(0603) X5R We use
4.7uF*1(0805) X5R
GS
T7100
PEX_TERMP
R7104
2.49KOhm
GPU_TESTMODE
R7105
10KOhm
Test mode:could be connect to Gnd,
for not using testmode
N11P-GS1
part number 02G100017103
PEGATRON
Title : PCI-E interface
Engineer: Frank_Ma
BU2/HW2
Size C
Project Name K42Jv
Rev 1.0
Date: Thursday, February 11, 2010
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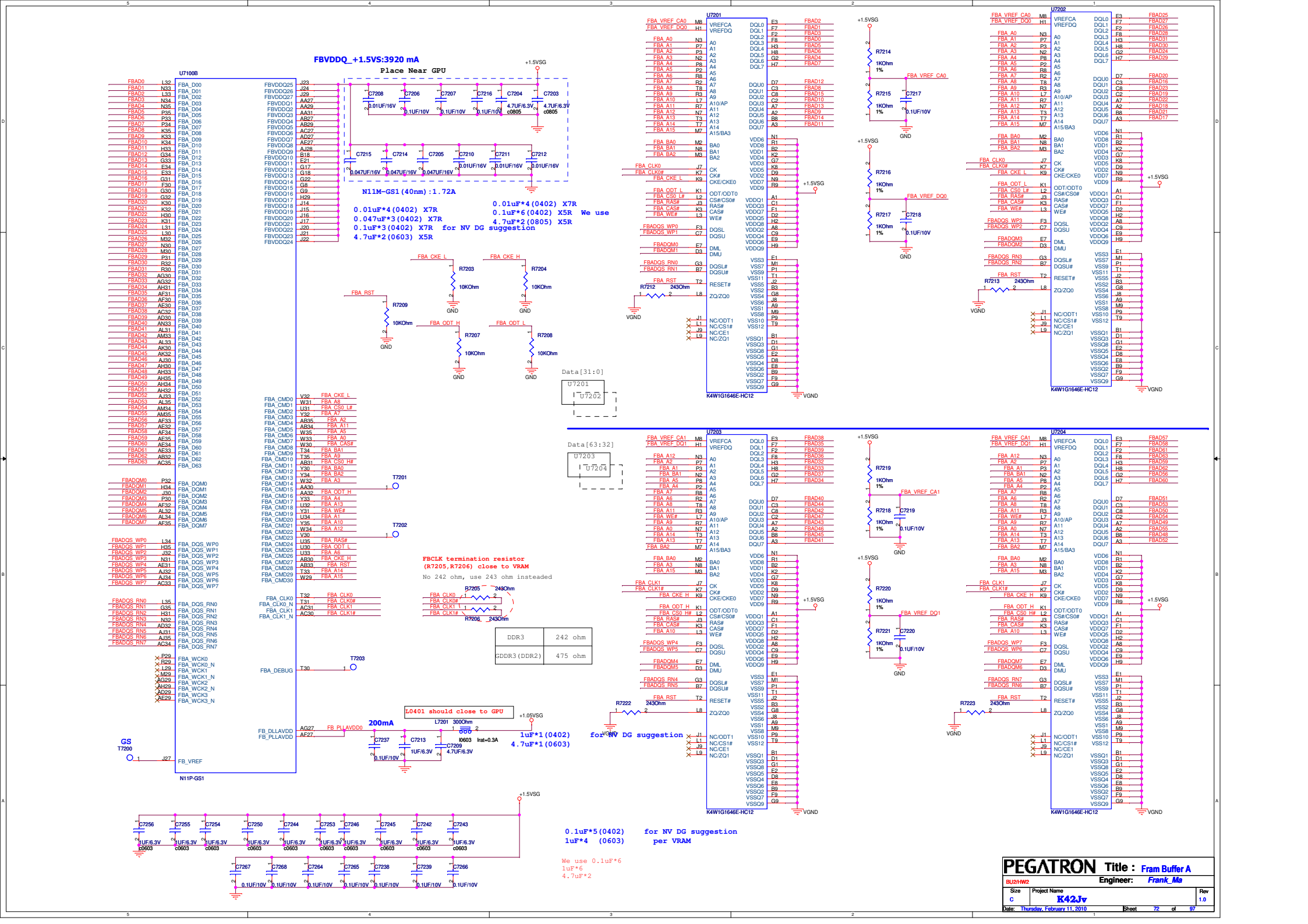
FBVDDQ_+1.5VS:3920 mA
Place Near GPU
N11M-GS1(40nm):1.72A
0.01uF*4(0402) X7R
0.047uF*3(0402) X7R
0.1uF*3(0402) X7R for NV DG suggestion
4.7uF*2(0603) X5R
0.01uF*4(0402) X7R
0.1uF*6(0402) X5R We use
4.7uF*2(0805) X5R
U7100B
N11P-GS1
U7201
U7202
U7203
U7204
K4W1G1646E-HC12
Data[31:0]
Data[63:32]
FBCLK termination resistor
(R7205,R7206) close to VRAM
No 242 ohm, use 243 ohm insteaded
DDR3 242 ohm
GDDR3(DDR2) 475 ohm
L0401 should close to GPU
200mA
1uF*1(0402)
4.7uF*1(0603)
for NV DG suggestion
0.1uF*5(0402)
1uF*4 (0603)
for NV DG suggestion
per VRAM
We use 0.1uF*6
1uF*6
4.7uF*2
GS
T7200
PEGATRON
Title : Fram Buffer A
Engineer: Frank_Ma
BU2/HW2
Size C
Project Name K42Jv
Rev 1.0
Date: Thursday, February 11, 2010
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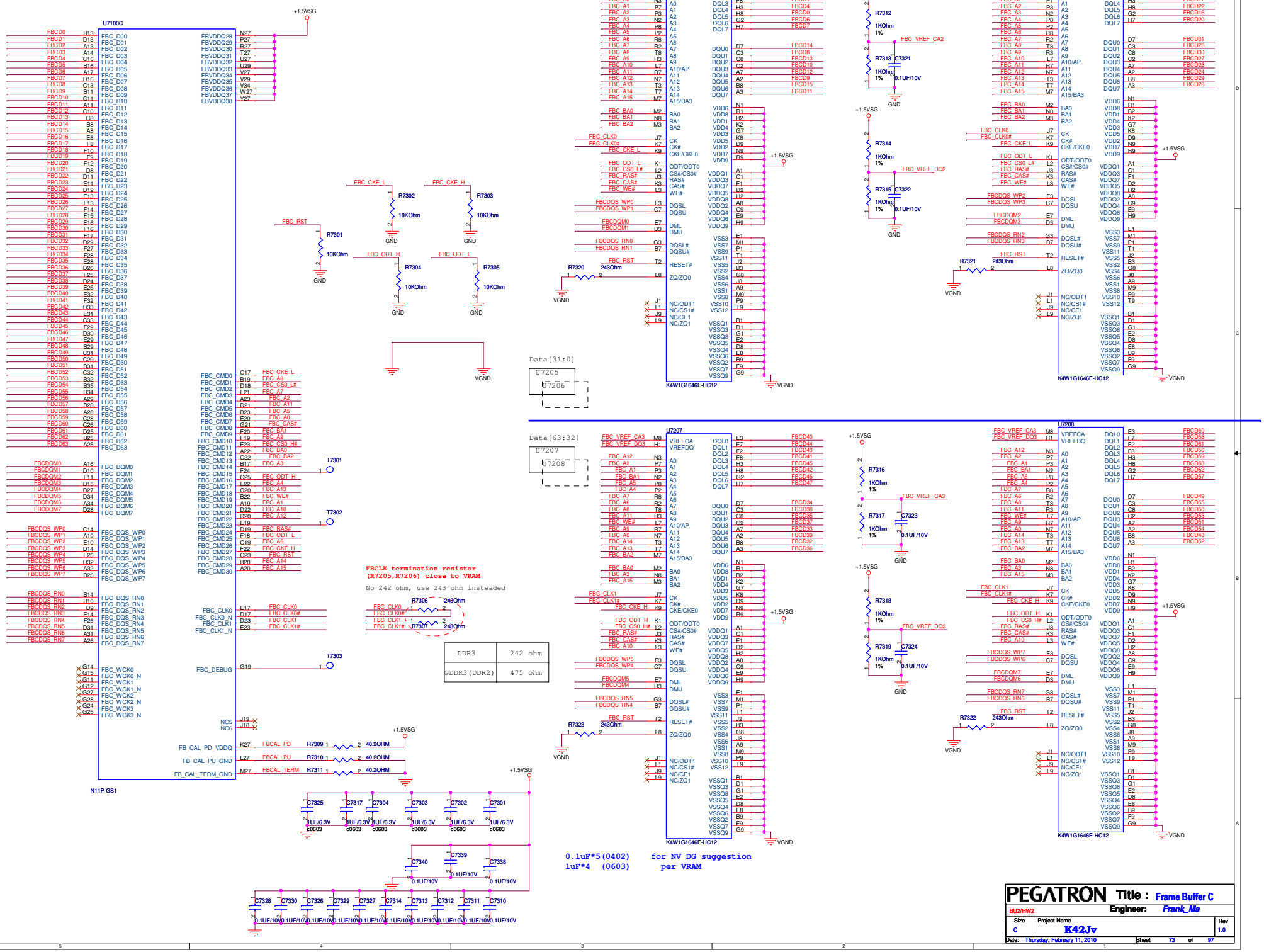
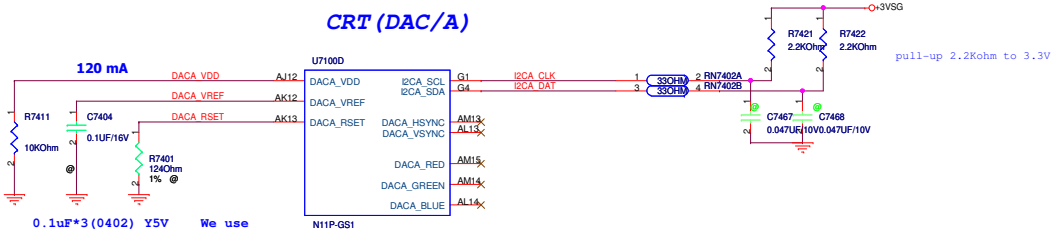


PEGATRON	Title : Frame Buffer C
BU2/HW2	Engineer: Frank_Ma
Size: C	Project Name: K42Jv
Rev: 1.0	
Date: Thursday, February 11, 2010	Sheet 73 of 97

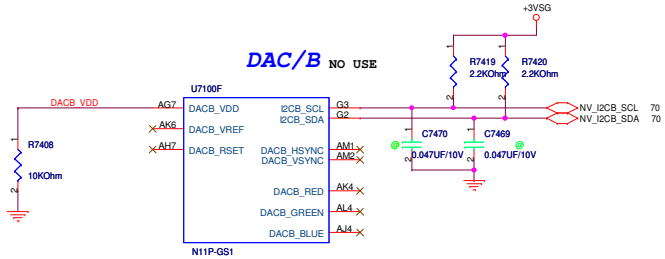
CRT (DAC/A)

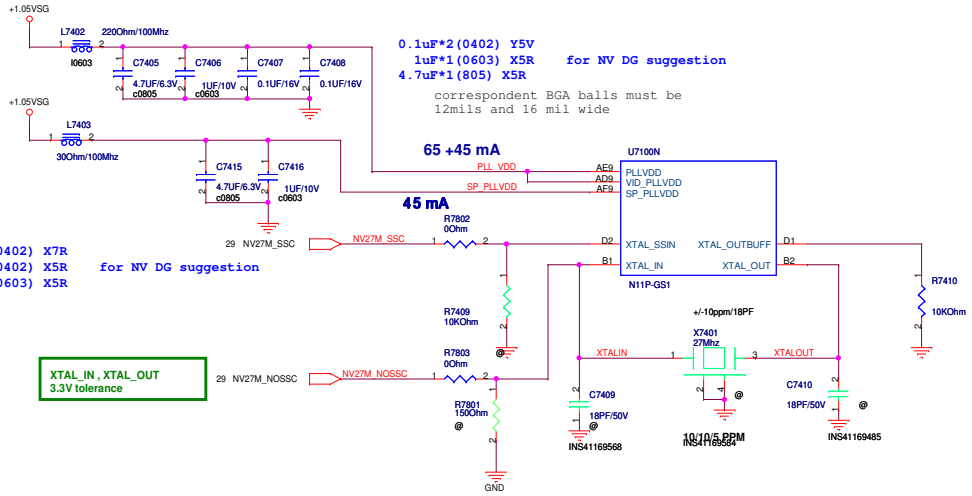


470pF*1(0402) X7R
4700pF*1(0402) X7R
100nF*3(0402) X7R for NV DG suggestion
1uF*1(0402) X5R
4.7uF*1(0603) X5R

0.1uF*3(0402) Y5V We use
4.7uF*1(0805) X5R

DAC/B NO USE





0.1uF*2(0402) X7R
1uF*2(0402) X5R for NV DG suggestion
4.7uF*2(0603) X5R

Option /SSC and /XTAL unmount

Ask to FAE if necessary or not

PEGATRON	Title : DACs, CLK GEN	
BU2/HW2	Engineer: Frank_Ma	
Size: C	Project Name: K42Jv	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 74 of 97	

GPU	IFP A	IFP B	IFP C	IFP D
GB1-128	LVDS (Single Link)	LVDS (Dual Link)	HDMI	DisplayPort (unused)

LVDS (IFPAB)

U7100G

220 mA

R7501 1KOhm
R7525 10KOhm
AK9 IFPAB_PLLVDD
AJ11 IFPAB_RSET

220 mA

R7524 10KOhm
AG9 IFPA_IOVDD
AG10 IFPB_IOVDD

IFPA_TXD0_N AL8
IFPA_TXD0 AM8
IFPA_TXD1_N AM9
IFPA_TXD1 AM10
IFPA_TXD2_N AL10
IFPA_TXD2 AK10
IFPA_TXD3_N AL11
IFPA_TXD3 AK11
IFPA_TXC_N AM12
IFPA_TXC AM11
IFPB_TXD4_N AP8
IFPB_TXD4 AN8
IFPB_TXD5_N AN10
IFPB_TXD5 AP10
IFPB_TXD6_N AR10
IFPB_TXD6 AR11
IFPB_TXD7_N AP11
IFPB_TXD7 AN11
IFPB_TXC_N AN13
IFPB_TXC AP13
GPIO0 K1 T7525

N11P-GS1

0.1uF*2(0402) for NV DG suggestion
1uF*1(0402)
4.7uF*1(0603)

Follow K42Jr and NV pull up 4.7k ohm to 3.3 (please chenk page 49)

HDMI (IFPC)

U7100H

285 mA

R7522 10KOhm
R7502 1KOhm

220 mA

R7523 10KOhm
AJ9 IFPC_PLLVDD
AK7 IFPC_RSET
AJ8 IFPC_IOVDD

IFPC_AUX_I2CW_SDA_N AN3 IFPC_AUX#
IFPC_AUX_I2CW_SCL AP2 IFPC_AUX
IFPC_L3_N AR2
IFPC_L3 AP1
IFPC_L2_N AM4
IFPC_L2 AM3
IFPC_L1_N AM5
IFPC_L1 AL5
IFPC_L0_N AM6
IFPC_L0 AM7
GPIO1 K2 T7526

+3VSG
R7520 2.2KOhm
R7521 2.2KOhm
Reserved for pull-up 2.2Kohm to 3.3V
ER-17
C7567 0.047UF/10V
C7568 0.047UF/10V

N11P-GS1

0.1uF*2(0402) for NV DG suggestion
1uF*1(0402)
4.7uF*1(0603)

DP (IFPD)

U7100E

R7518 10KOhm
GND
AC6 IFPD_PLLVDD
AB6 IFPD_RSET
AK8 IFPD_IOVDD
R7519 10KOhm
GND

IFPD_AUX_I2CX_SDA_N AN4
IFPD_AUX_I2CX_SCL AP4
IFPD_L3_N AR4
IFPD_L3 AR5
IFPD_L2_N AP5
IFPD_L2 AN5
IFPD_L1_N AN7
IFPD_L1 AP7
IFPD_L0_N AR7
IFPD_L0 AR8
GPIO19 L7

N11P-GS1

IFPEF is unused

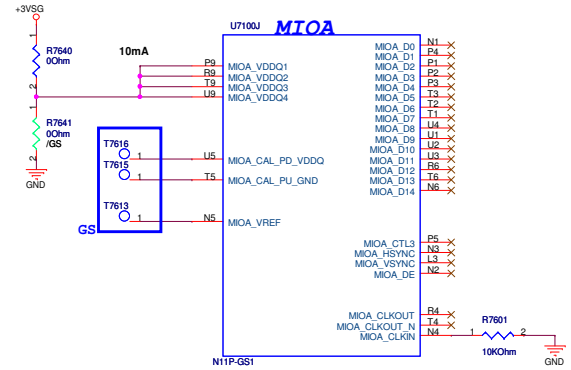
U7100I

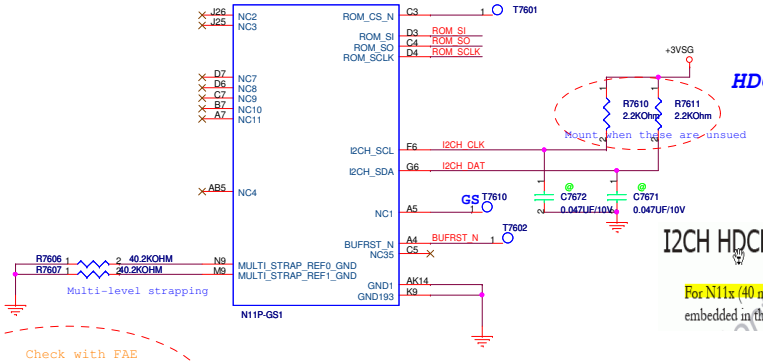
R7504 10KOhm
GND
AJ6 IFPEF_PLLVDD
AL1 IFPEF_RSET
R7505 10KOhm
GND
AE7 IFPE_IOVDD
AD7 IFPF_IOVDD

IFPE_AUX_I2CY_SDA_N AD4
IFPE_AUX_I2CY_SCL AE4
IFPE_L3_N AE5
IFPE_L3 AE6
IFPE_L2_N AF5
IFPE_L2 AF4
IFPE_L1_N AG4
IFPE_L1 AH4
IFPE_L0_N AH5
IFPE_L0 AH6
GPIO15 L1
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_AUX_I2CZ_SCL AF3
IFPF_L3_N AH3
IFPF_L3 AH2
IFPF_L2_N AH1
IFPF_L2 AJ1
IFPF_L1_N AJ2
IFPF_L1 AJ3
IFPF_L0_N AL3
IFPF_L0 AL2
GPIO21 K6

N11P-GS1

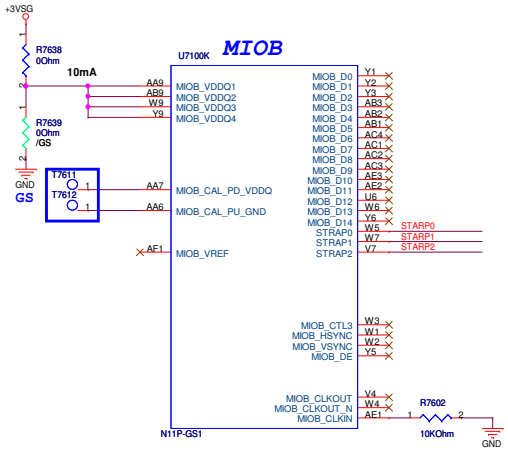
PEGATRON Title : LVDS/HDMI/DP
Engineer: Frank_Ma
BU2/HW2
Size C | Project Name K42Jv | Rev 1.0
Date: Thursday, February 11, 2010 | Sheet 75 of 97





I2CH HDCP Interface

For N11x (40 nm), an external HDCP ROM is not required. HDCP functionality is embedded in the GPU. External connections are not required to support HDCP.



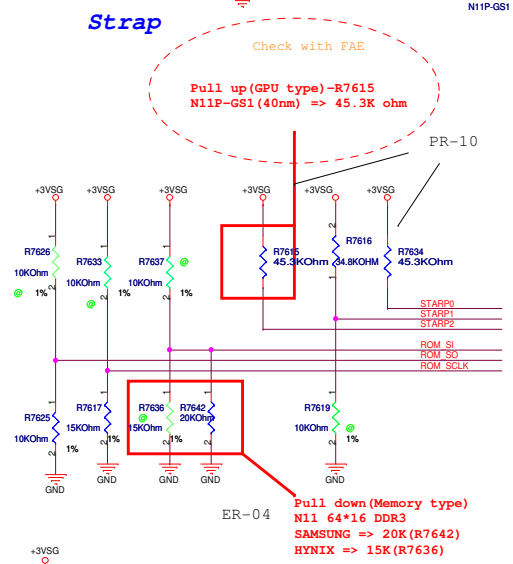
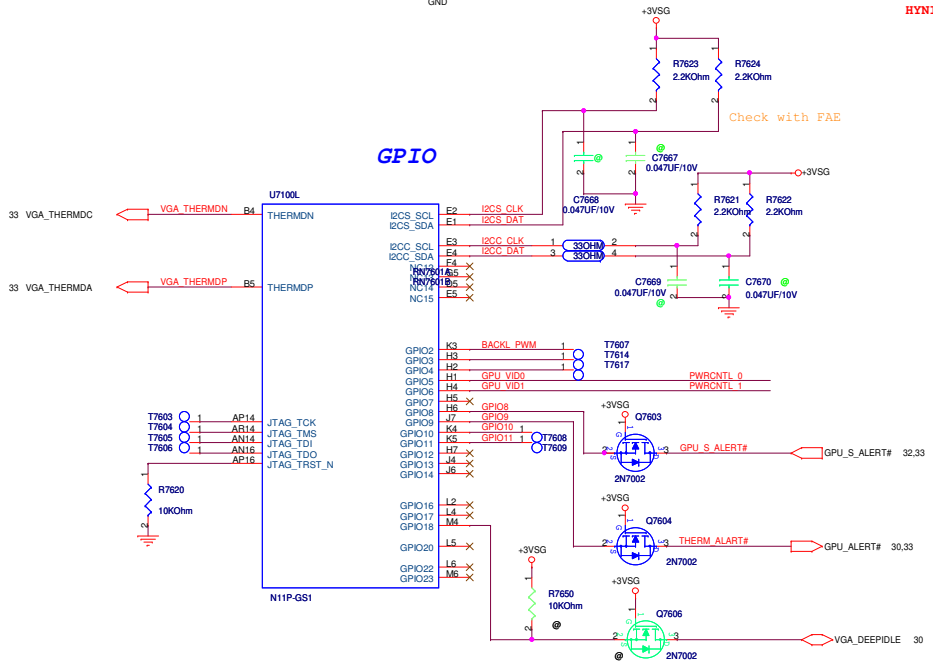
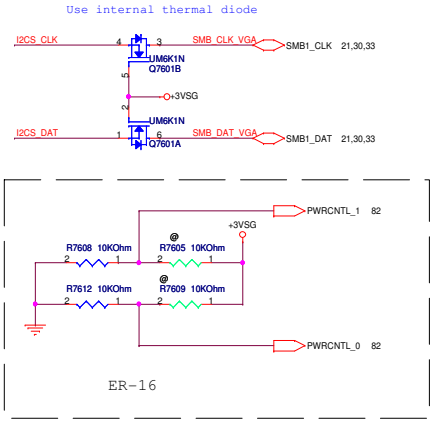


Table 13-5. Multilevel Strapping Options

Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]





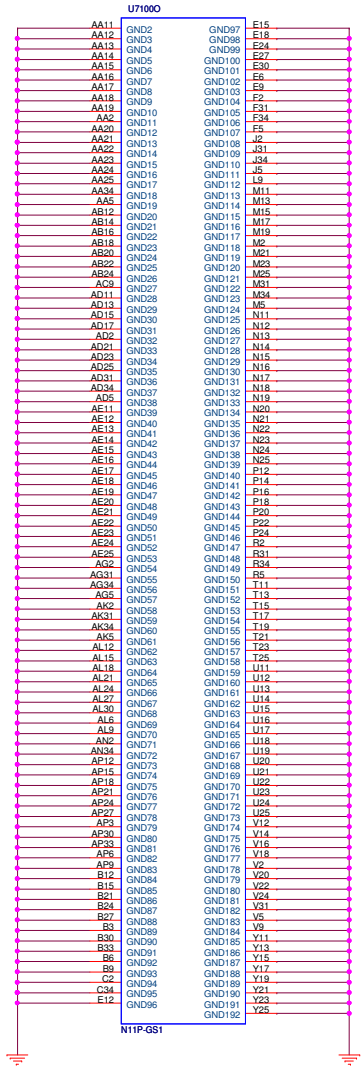
I2C ASSIGNMENTS

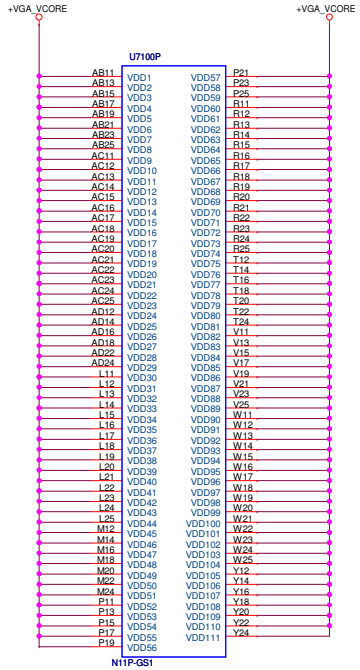
I2CA: CRT --3V
I2CB: N/A
I2CC: LVDS(EDID)
I2CS: Slave for GPU internal thermal
I2CH: HDCP
IFPC_AUX_I2CW: HDMI --3 V
IFPD_AUX_I2CX: DP --3 V
IFPE_AUX_I2CY: N/A
IFPF_AUX_I2CZ: N/A

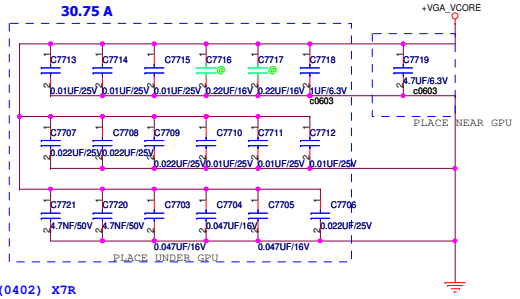
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	n/a	n/a	p.75
1	IN	-	IFPC HPD-C (HDMI) p.75
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	-	NVVDD VID 0
6	OUT	-	NVVDD VID 1
7	OUT	-	NVVDD VID 2
8	I/O	LOW	OVERT
9	I/O	LOW	THERMAL ALERT
10	OUT		Memory VREF switch
11	I/O	LOW	SLI raster sync
12	IN	-	AC DETECT
13	OUT	-	MEM_VID
14	OUT	-	PWR_CRT1
15	IN	-	IFPE HPD-E
16	OUT	-	FAN_PWM
17	IN	-	Reserved
18	IN	-	Reserved
19	IN	-	IFPD HPD-D (DP) P.75
20	IN	-	Reserved
21	IN	-	IFPF HPD-F
22	IN	-	SLI swap ready signal
23	I/O		

PEGATRON Title : Strap, GPIO
BU2/HW2 Engineer: Frank_Ma
Size C | Project Name K42Jv | Rev 1.0
Date: Thursday, February 11, 2010 | Sheet 76 of 97







4700pF*2 (0402) X7R
0.01uF*6 (0402) X7R
0.022uF*4 (0402) X7R
0.047uF*3 (0402) X7R
0.22uF*2 (0603) X7R
1uF*1 (0603) X5R
4.7uF*1 (0603) X5R

for NV DG suggestion

0.1uF*15 (0402) X5R
0.22uF*2 (0603) X7R @
1uF*1 (0603) X5R
4.7uF*1 (0603) X5R

We use

PEGATRON Title : PWR&GND
BU2/HW2 Engineer: Frank_Ma
Size C | Project Name K42Jv | Rev 1.0
Date: Thursday, February 11, 2010 | Sheet 77 of 97

ER Modify list:

ER-01 : For VTT Power adjustable and DRAM power fix

ER-02 : Exchange PIN 2 and PIN 3 connection and Power rail chagne from +3VS to +5VS.

ER-03 : Add /Ven lable for Ventura option.

ER-04 : According GPU strap define setting to P.D.

ER-05 : LCD backlight control change to accord DESIGN IP.

ER-06 : Change R2404 to 33OHM for EA measurement.

ER-07 : Unmount External thermal sensor change to use DGPU internal thermal sensor.

ER-08 : According for VTT power default setting.

ER-09 : To change from +1.8VSG to +1.5VSG.

ER-10 : PCB ID change from SR to ER setting.

ER-11 : ALC269 ver B. must add 10K P.U for PD# pin.

ER-12 : Modify Crystal Rd location and add /USB30 lable.

ER-13 : For Smart33 Down freq. and reserve over clock design.
R2933 mount 4.7K 0603 at ER stage.

ER-14 : Modify power rail to +5VS_AUDIO.

ER-15 : R3631 change from 10K to 0R.

ER-16 : Setting DGPU Vcore default power to 0.8V.

ER-17 : Unmount R7520,R7521 from vendor suggestion.

ER-18 : Reserve vendor solution add 0R for bypass other circuit.

ER-19 : Change USB port to 2.0 connector and design only for USB 2.0.

ER-20 : For line-in channel ,HP jack sensor must change to 10K.

ER-22 : To resolve "3622146 A Voltage Spike on Graphics Core Rail (Vaxg) to 1.5V seen during system shutdown"change from 4.7K to 470 OHM.

ER-23 : Follow Design IP,change to P.D.

ER-24 : Change mount for smart 33 control Vcore power.

For cost down and short jump ,Please search "C.D"

PR Modify list:

PR-01 : Change R2933 to 10K 0402.

PR-02 : Mic bias voltage change from +5VS_AUDIO to CODEC's PIN28(integreated regulator).To avoid MIC noise by drity power.

PR-03 : Change R3631 from 0R to short jump.

PR-04 : Add level shift circuit.

PR-05 : Del RN9250.

PR-06 : Add for pop and click sounds.

PR-07 : Change for B to B re-design.(copy from K42JC schematic)

PR-08 : EMI/ESD request.

PR-09 : Add MGRL of headset device design.

PR-10 : According to vendor suggestion.(45K change to 45.3K)

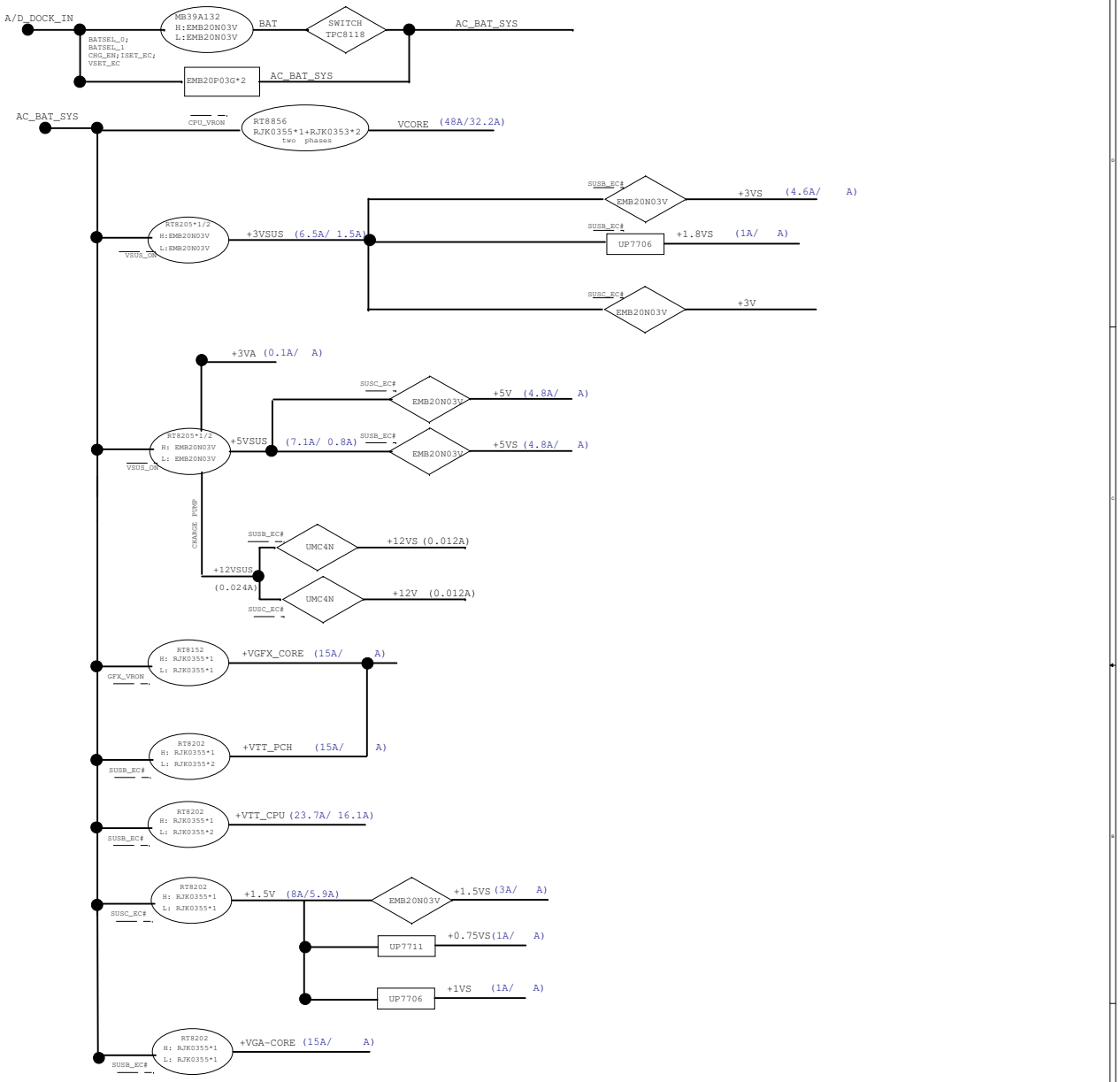
PR-11 : Bypass INT. MIC amplifier.

PR-12 : VTT,+1.5V,VCORE power set to default normal power rails.

PR-13 : Codec IC(ALC269) change from VB2 to VB5.

PR-14 : PCB ID change from ER to PR setting.

ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: Frank_Ma	
Size: C	Project Name: K42Jv	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 79 of 99	



<Variant Name>

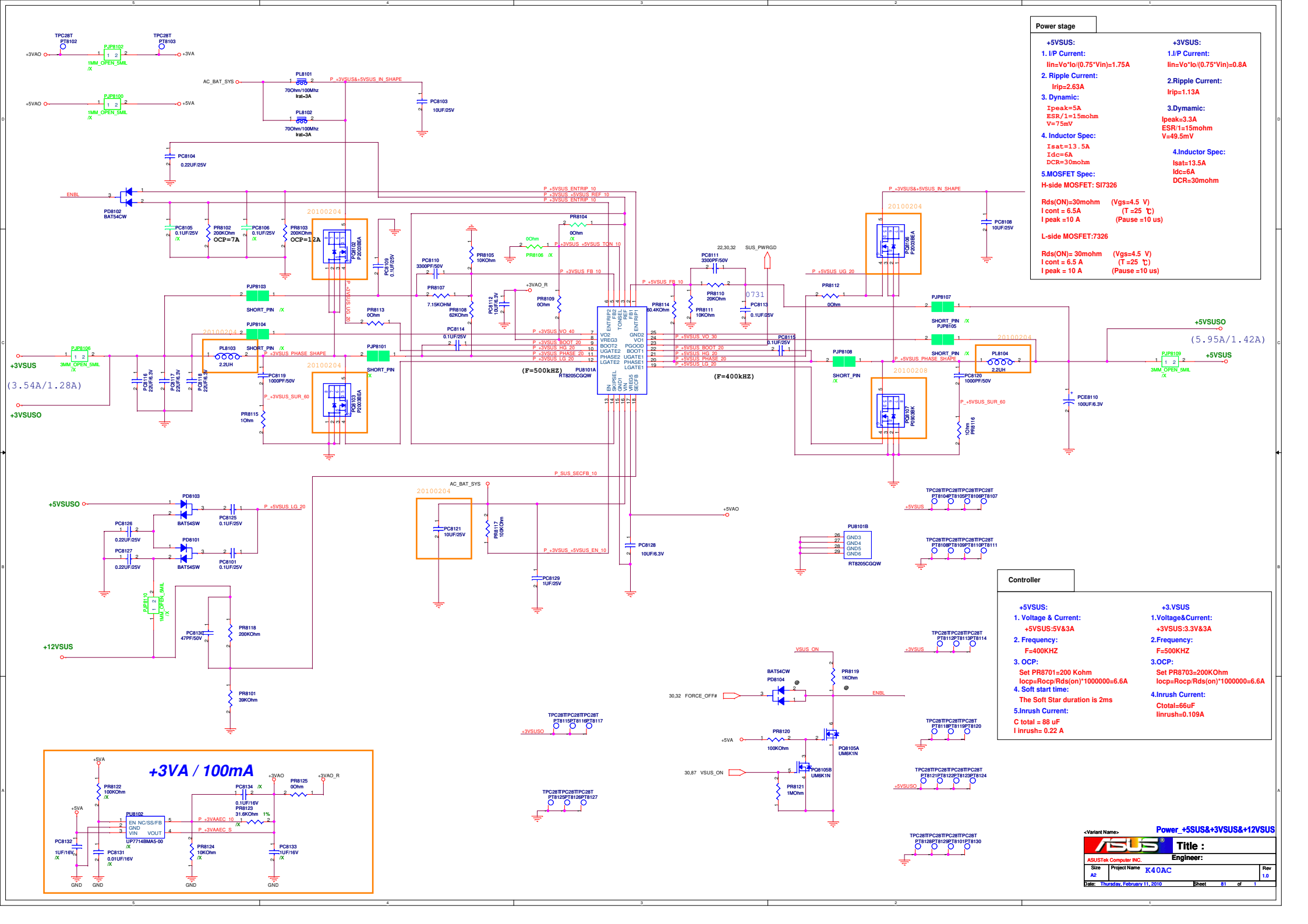
ASUSTek Computer INC.

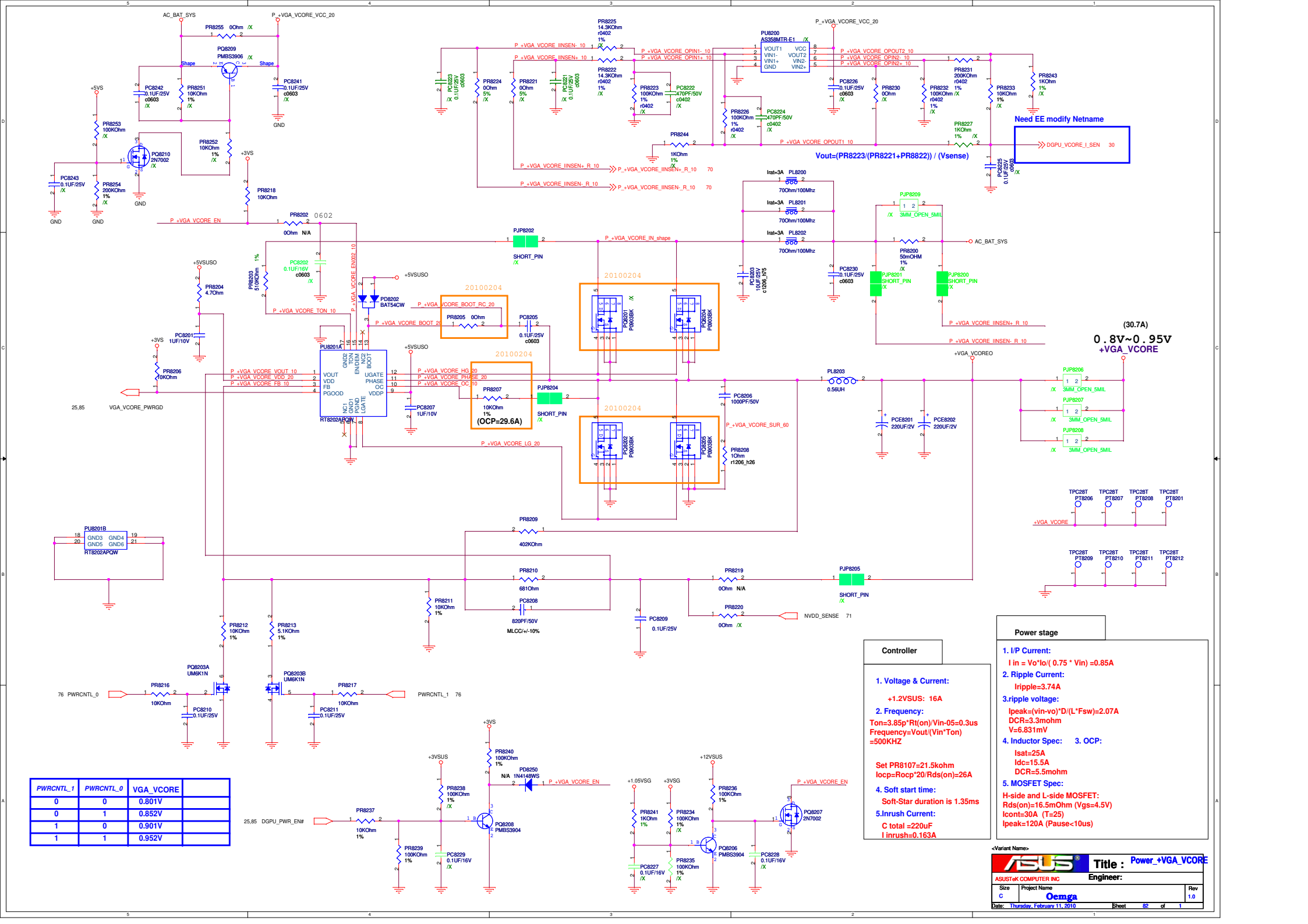
Title : Power_Flow

Engineer: ZHI-KUN_LIU

Size	Project Name	Rev
Custom	K80A	1.0

Date: Thursday, February 11, 2010 Sheet 80 of 79


Power stage
+5VSUS:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=1.75A
2. Ripple Current:
Irip=2.63A
3. Dynamic:
Ipeak=5A
ESR/1=15mohm
V=75mV
4. Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
5.MOSFET Spec:
H-side MOSFET: SI7326
Rds(ON)=30mohm (Vgs=4.5 V)
I cont = 6.5A (T =25 ℃)
I peak =10 A (Pause =10 us)
L-side MOSFET:7326
Rds(ON)= 30mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25 ℃)
I peak = 10 A (Pause =10 us)
+3VSUS:
1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=0.8A
2.Ripple Current:
Irip=1.13A
3.Dymamic:
Ipeak=3.3A
ESR/1=15mohm
V=49.5mV
4.Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
Controller
+5VSUS:
1. Voltage & Current:
+5VSUS:5V&3A
2. Frequency:
F=400KHZ
3. OCP:
Set PR8701=200 Kohm
Iocp=Rocp/Rds(on)*1000000=6.6A
4. Soft start time:
The Soft Star duration is 2ms
5.Inrush Current:
C total = 88 uF
I inrush= 0.22 A
+3.VSUS
1.Voltage&Current:
+3VSUS:3.3V&3A
2.Frequency:
F=500KHZ
3.OCP:
Set PR8703=200KOhm
Iocp=Rocp/Rds(on)*1000000=6.6A
4.Inrush Current:
Ctotal=66uF
Iinrush=0.109A
+3VA / 100mA
+3VSUS
(3.54A/1.28A)
+5VSUSO
(5.95A/1.42A)
+12VSUS
(F=500kHz)
(F=400kHz)
OCP=7A
OCP=12A
PU8101A RT8205CGQW
PU8101B RT8205CGQW
PU8102 UP7714BMA5-00
PQ8105A UM6K1N
PQ8105B UM6K1N
<Variant Name>
Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTek Computer INC.
Engineer:
Size A2
Project Name K40AC
Rev 1.0
Date: Thursday, February 11, 2010
Sheet 81 of 1



PWRCNTL_1	PWRCNTL_0	VGA_VCORE	
0	0	0.801V	
0	1	0.852V	
1	0	0.901V	
1	1	0.952V	

Controller

1. Voltage & Current:

   +1.2VSUS: 16A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

Set PR8107=21.5kohm
Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5. Inrush Current:

   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:

   Iripple=3.74A

3. ripple voltage:

   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV

4. Inductor Spec: 3. OCP:

   Isat=25A
   Idc=15.5A
   DCR=5.5mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

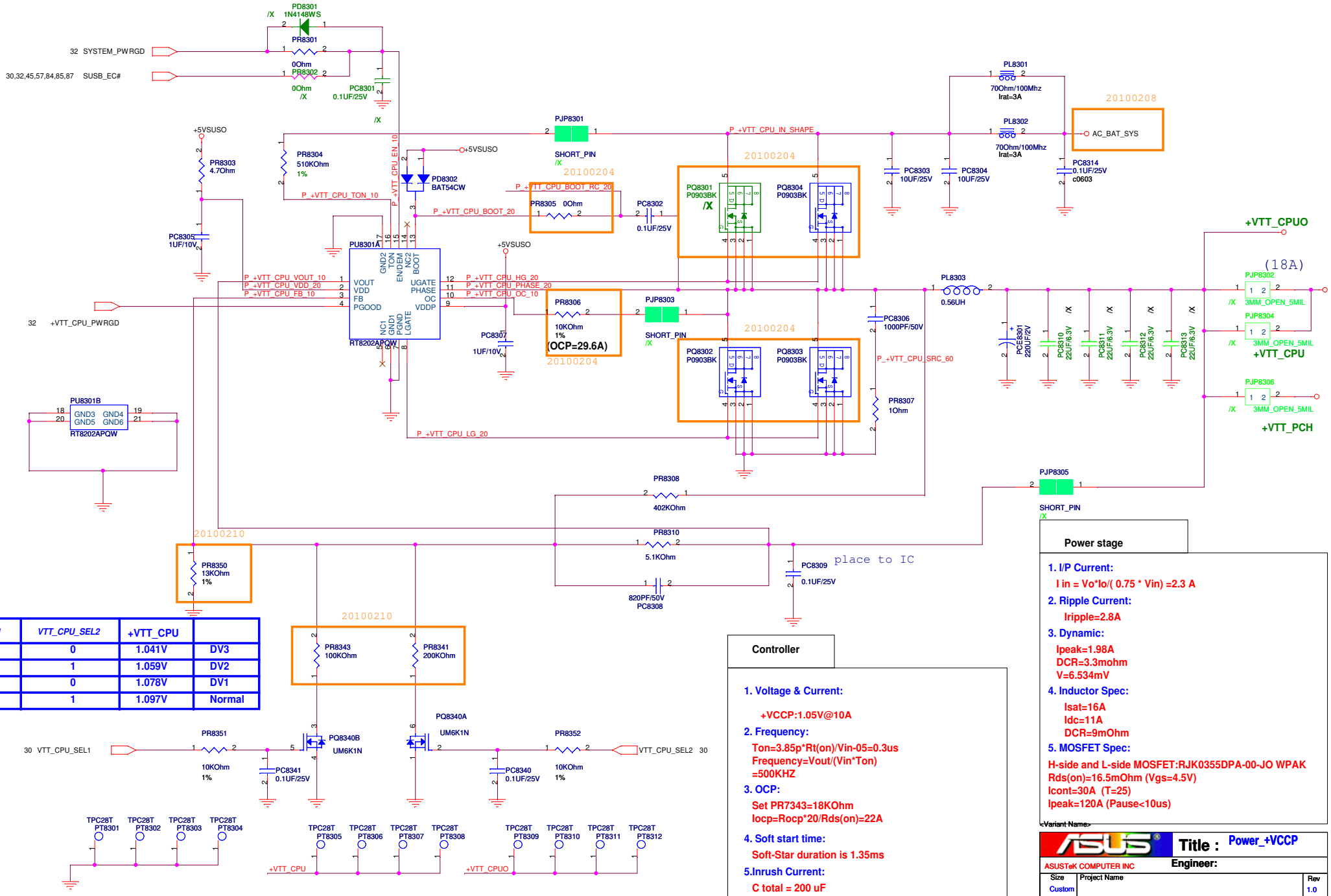
ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Thursday, February 11, 2010 Sheet 82 of 1



VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	1.041V	DV3
0	1	1.059V	DV2
1	0	1.078V	DV1
1	1	1.097V	Normal

Controller

1. Voltage & Current:
   +VCCP:1.05V@10A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR7343=18KOhm
   Iocp=Rocp*20/Rds(on)=22A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total = 200 uF
   I inrush= 0.16 A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.3 A
2. Ripple Current:
   Iripple=2.8A
3. Dynamic:
   Ipeak=1.98A
   DCR=3.3mohm
   V=6.534mV
4. Inductor Spec:
   Isat=16A
   Idc=11A
   DCR=9mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

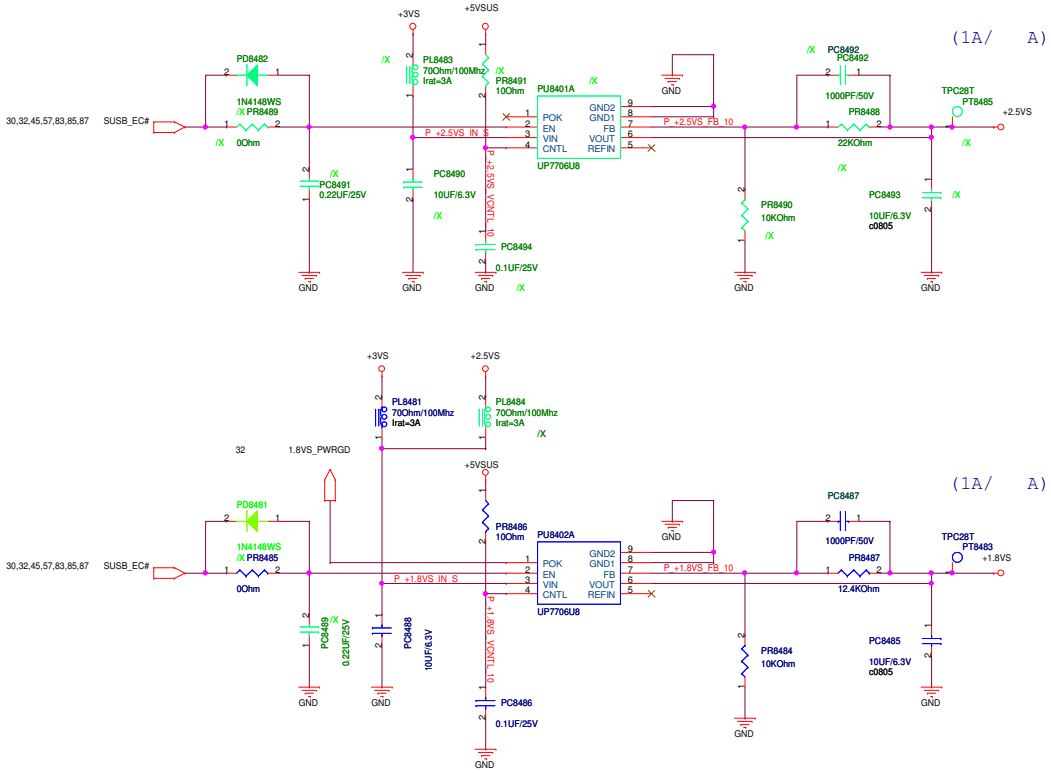
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, February 11, 2010 Sheet 83 of 1



Controller

1. Voltage & Current:

   +1.8V:+1.8V&12A

2. Frequency:

   Ton=3.85p*Rt(on)*Vo/Vin-05
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   Set PR7343=18kohm
   Iocp=Rocp*20/Rds(on)
   =20*21.5/16.5=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5.Inrush Current:

   C total =100uF
   I
   inrush=0.133A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.8 * Vin) =0.947A

2. Ripple Current:

   Iripple=2.342A

3. Ripple Voltage:

   Ipeak=(vin-vo)*D/(L*Fsw)=3.25A
   DCR=3.3mohm
   V=10.75mV

4. Inductor Spec:

   Isat=36A
   Idc=18A
   DCR=3.3mohm

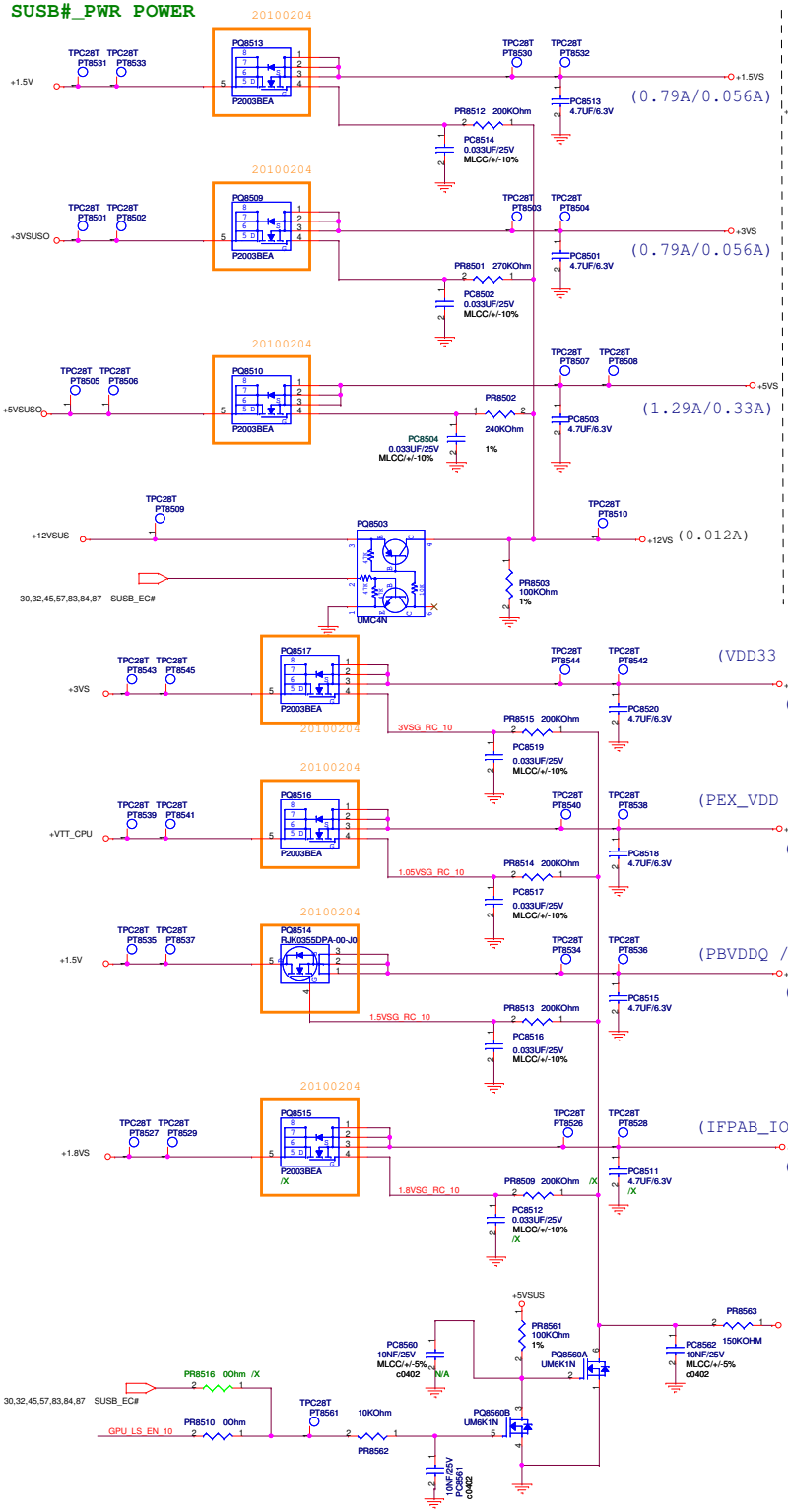
5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

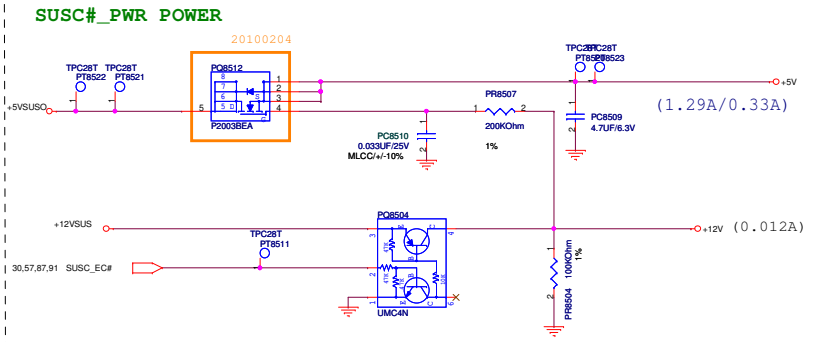
<Variant Name>

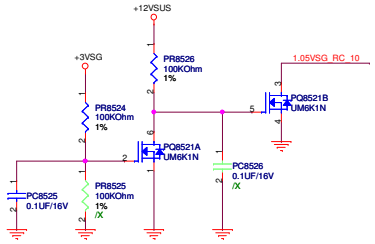
ASUSTeK COMPUTER INC	Title : Power_+1.8V&+0.9V	
	Engineer:	
Size: C	Project Name	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 84 of 1	

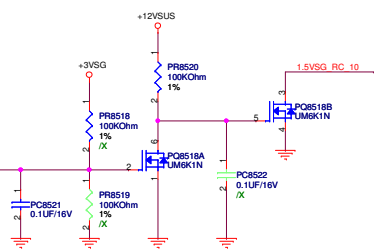
SUSB#_PWR POWER

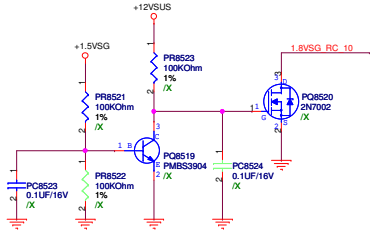


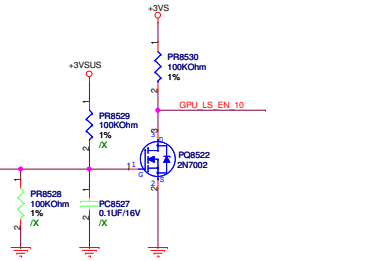
SUSC#_PWR POWER







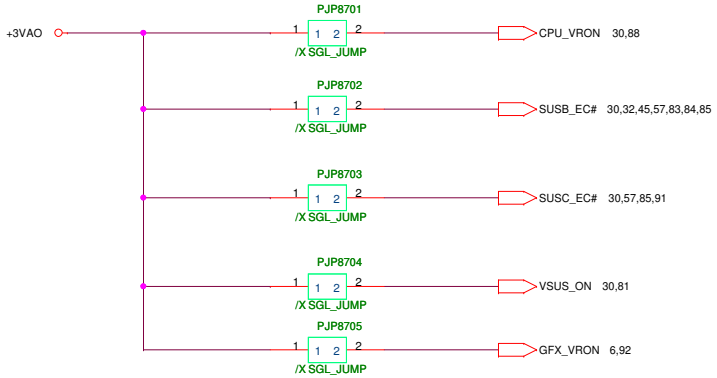




<Variant Name>
Title : Power_Load_Switch
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name
Rev: 1.0
Date: Thursday, February 11, 2010
Sheet 85 of 1

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_good_detecter	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 86 of 1	



<Variant Name>

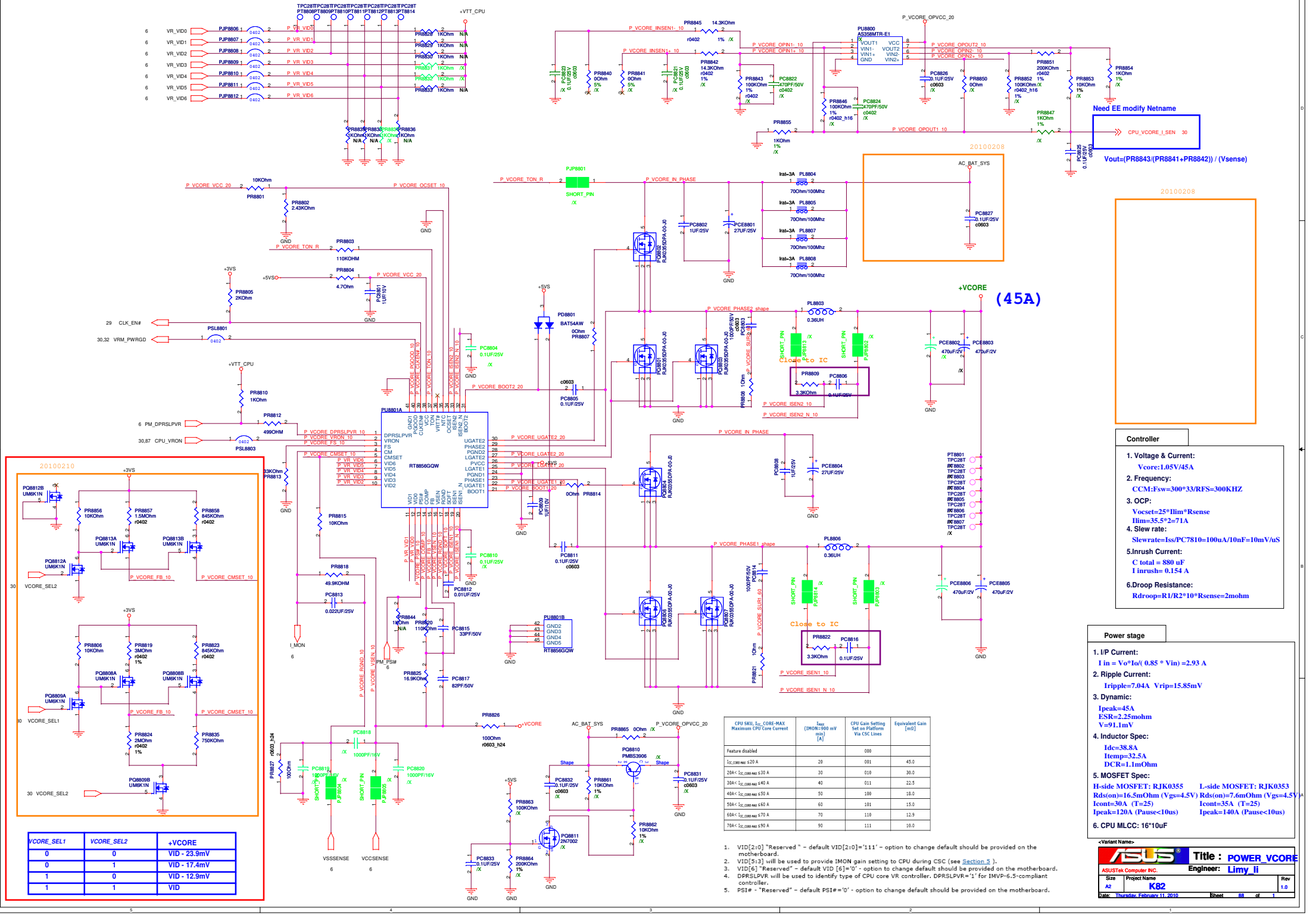
ASUSTeK COMPUTER INC

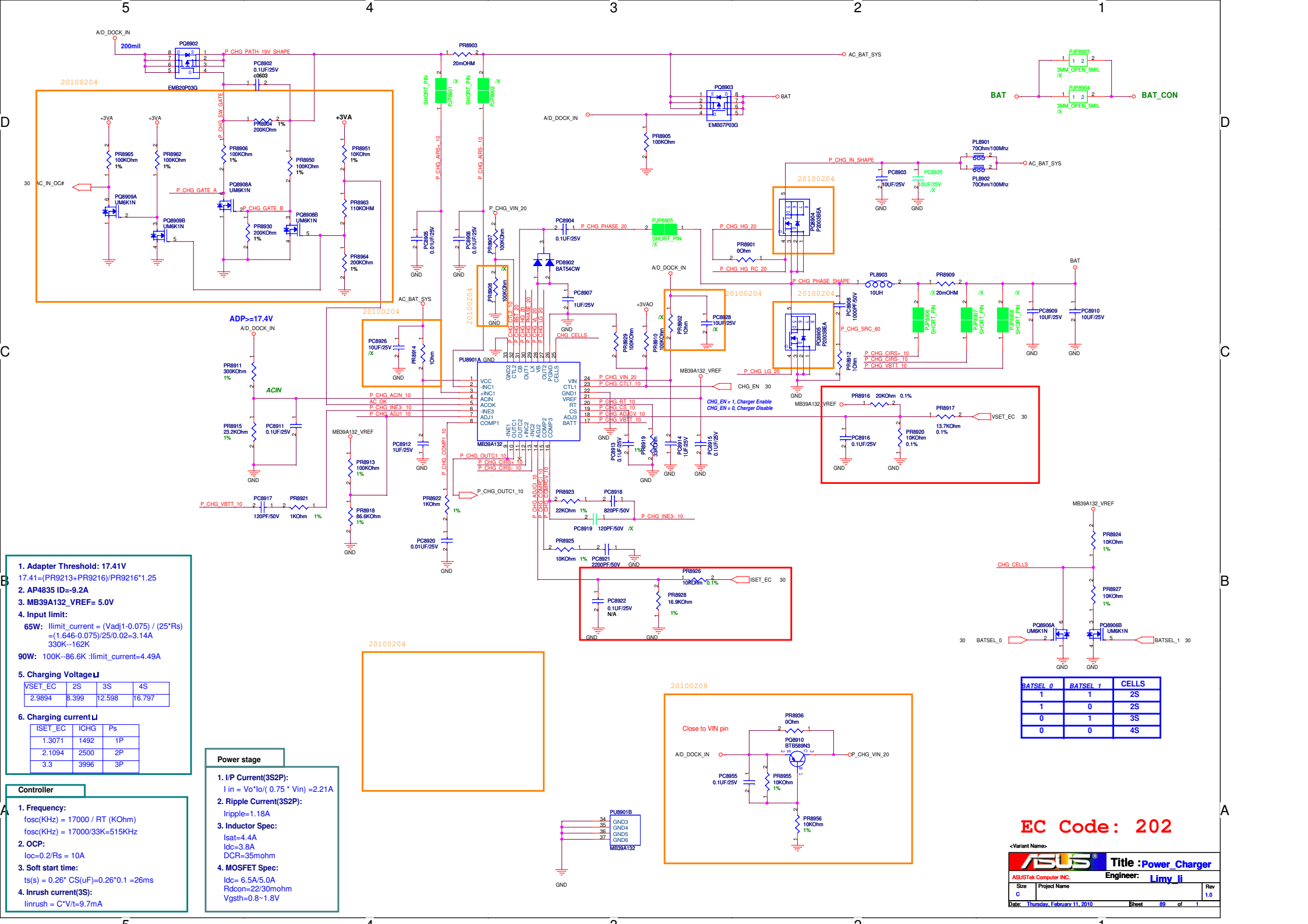
Title : Power_for_test

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, February 11, 2010 Sheet 87 of 1


+VTT_CPU
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
P_VR_VID0
P_VR_VID1
P_VR_VID2
P_VR_VID3
P_VR_VID4
P_VR_VID5
P_VR_VID6
P_VCORE_OPVCC_20
P_VCORE_OPOUT2_10
P_VCORE_OPIN2-_10
P_VCORE_OPIN2+_10
P_VCORE_OPOUT1_10
P_VCORE_IINSEN1-_10
P_VCORE_IINSEN1+_10
P_VCORE_OPIN1-_10
P_VCORE_OPIN1+_10
Need EE modify Netname
CPU_VCORE_I_SEN 30
Vout=(PR8843/(PR8841+PR8842)) / (Vsense)
20100208
AC_BAT_SYS
P_VCORE_VCC_20
P_VCORE_OCSET_10
P_VCORE_TON_R
P_VCORE_IN_PHASE
+5VSO
+3VS
CLK_EN#
VRM_PWRGD
PM_DPRSLPVR
CPU_VRON
P_VCORE_DPRSLPVR_10
P_VCORE_VRON_10
P_VCORE_FS_10
P_VCORE_CMSET_10
P_VCORE_BOOT2_20
P_VCORE_UGATE2_20
P_VCORE_LGATE2_20
P_VCORE_BOOT1_20
P_VCORE_UGATE1_20
P_VCORE_LGATE1_20
P_VCORE_PHASE2_shape
P_VCORE_PHASE1_shape
P_VCORE_ISEN2_10
P_VCORE_ISEN2_N_10
P_VCORE_ISEN1_10
P_VCORE_ISEN1_N_10
Close to IC
+VCORE
(45A)
RT8856GQW
PU8801A
PU8801B
RT8856GQW
I_MON
PM_PSI#
VCORE_SEL2
VCORE_SEL1
VSSSENSE
VCCSENSE
Controller
1. Voltage & Current:
Vcore:1.05V/45A
2. Frequency:
CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
Vocset=25*Ilim*Rsense
Ilim=35.5*2=71A
4. Slew rate:
Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5.Inrush Current:
C total = 880 uF
I inrush= 0.154 A
6.Droop Resistance:
Rdroop=R1/R2*10*Rsense=2mohm
Power stage
1. I/P Current:
I in = Vo*Io/(0.85 * Vin) =2.93 A
2. Ripple Current:
Iripple=7.04A Vrip=15.85mV
3. Dynamic:
Ipeak=45A
ESR=2.25mohm
V=91.1mV
4. Inductor Spec:
Idc=38.8A
Itemp=32.5A
DCR=1.1mOhm
5. MOSFET Spec:
H-side MOSFET: RJK0355 L-side MOSFET: RJK0353
Rds(on)=16.5mOhm (Vgs=4.5V) Rds(on)=7.6mOhm (Vgs=4.5V)
Icont=30A (T=25) Icont=35A (T=25)
Ipeak=120A (Pause<10us) Ipeak=140A (Pause<10us)
6. CPU MLCC: 16*10uF
VCORE_SEL1 | VCORE_SEL2 | +VCORE
0 | 0 | VID - 23.9mV
0 | 1 | VID - 17.4mV
1 | 0 | VID - 12.9mV
1 | 1 | VID
CPU SKU, Icc_CORE-MAX Maximum CPU Core Current | Imax (IMON=900 mV min) [A] | CPU Gain Setting Set on Platform Via CSC Lines | Equivalent Gain [mΩ]
Feature disabled | | 000 |
Icc_CORE-MAX ≤20 A | 20 | 001 | 45.0
20A< Icc_CORE-MAX ≤30 A | 30 | 010 | 30.0
30A< Icc_CORE-MAX ≤40 A | 40 | 011 | 22.5
40A< Icc_CORE-MAX ≤50 A | 50 | 100 | 18.0
50A< Icc_CORE-MAX ≤60 A | 60 | 101 | 15.0
60A< Icc_CORE-MAX ≤70 A | 70 | 110 | 12.9
70A< Icc_CORE-MAX ≤90 A | 90 | 111 | 10.0
1. VID[2:0] "Reserved " – default VID[2:0]='111' – option to change default should be provided on the motherboard.
2. VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
3. VID[6] "Reserved" – default VID [6]='0' - option to change default should be provided on the motherboard.
4. DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR='1' for IMVP-6.5-compliant controller.
5. PSI# - "Reserved" – default PSI#='0' - option to change default should be provided on the motherboard.
<Variant Name>
Title : POWER_VCORE
ASUSTek Computer INC.
Engineer: Limy_li
Size A2
Project Name K82
Rev 1.0
Date: Thursday, February 11, 2010
Sheet 88 of 1



1. Adapter Threshold: 17.41V

17.41=(PR9213+PR9216)/PR9216*1.25

2. AP4835 ID=-9.2A

3. MB39A132_VREF= 5.0V

4. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25/0.02=3.14A
330K--162K

90W: 100K--86.6K :Ilimit_current=4.49A

5. Charging Voltage

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

6. Charging current

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:

fosc(KHz) = 17000 / RT (KOhm)

fosc(KHz) = 17000/33K=515KHz

2. OCP:

Ioc=0.2/Rs = 10A

3. Soft start time:

ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms

4. Inrush current(3S):

Iinrush = C*V/t=9.7mA

Power stage

1. I/P Current(3S2P):

I in = Vo*Io/(0.75 * Vin) =2.21A

2. Ripple Current(3S2P):

Iripple=1.18A

3. Inductor Spec:

Isat=4.4A
Idc=3.8A
DCR=35mohm

4. MOSFET Spec:

Idc= 6.5A/5.0A
Rdcon=22/30mohm
Vgsth=0.8~1.8V

BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

EC Code: 202

<Variant Name>

ASUSTek Computer INC.

Title : Power_Charger

Engineer: Limy_li

Size	Project Name	Rev
C		1.0

Date: Thursday, February 11, 2010 Sheet 89 of 1

<Variant Name>

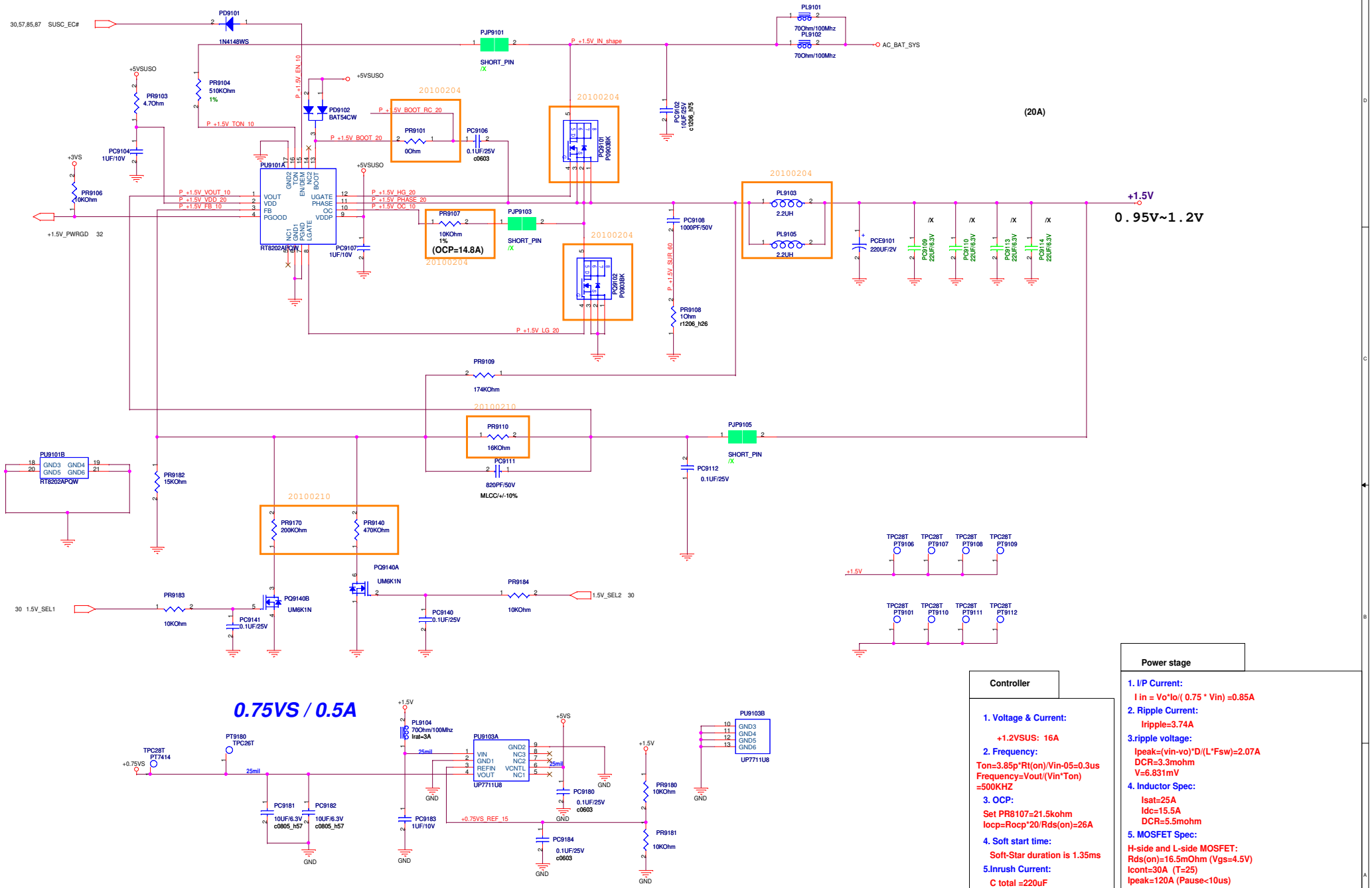
Title : Power_Charger

ASUSTek Computer INC.

Engineer: Limy_li

Size	Project Name	Rev
A3	F83T	2.1G

Date: Thursday, February 11, 2010 Sheet 90 of 1



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.483V	DV3
0	1	1.506V	DV2
1	0	1.538V	DV1
1	1	1.561V	Normal

Controller

1. Voltage & Current:

   +1.2VSUS: 16A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:

Set PR8107=21.5kohm
Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:

Soft-Star duration is 1.35ms

5.Inrush Current:

C total =220uF
I inrush=0.163A

Power stage

1. I/P Current:

I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:

Iripple=3.74A

3.ripple voltage:

Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
DCR=3.3mohm
V=6.831mV

4. Inductor Spec:

Isat=25A
Idc=15.5A
DCR=5.5mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

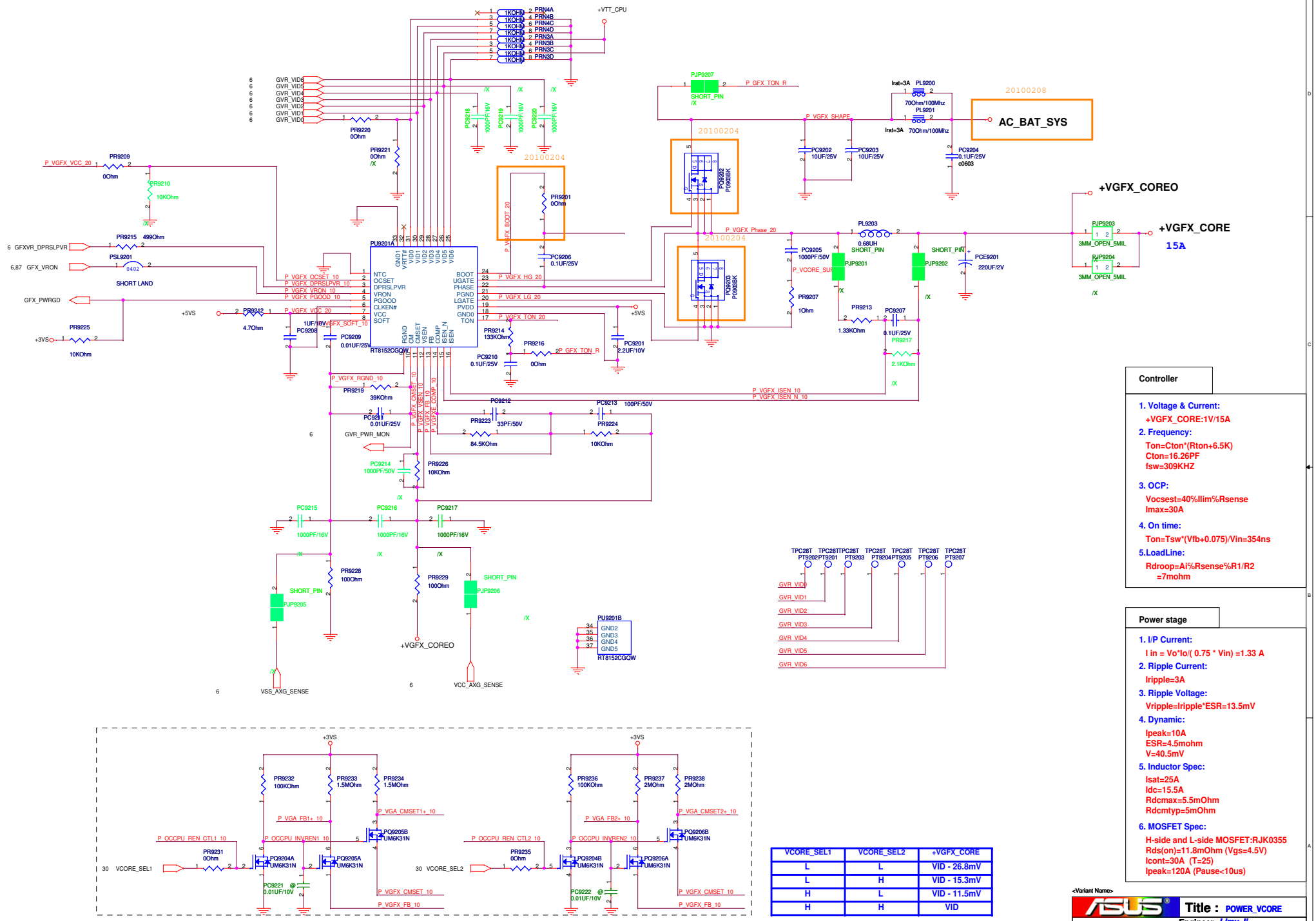
ASUSTeK COMPUTER INC

Title : +1.5V

Engineer:

Size	Project Name	Rev
C	K80A	1.0

Date: Thursday, February 11, 2010 Sheet 91 of 91



Controller

1. Voltage & Current:
   +VGFX_CORE:1V/15A
2. Frequency:
   Ton=Cton*(Rton+6.5K)
   Cton=16.26PF
   fsw=309KHZ
3. OCP:
   Vocsest=40%Ilim%Rsense
   Imax=30A
4. On time:
   Ton=Tsw*(Vfb+0.075)/Vin=354ns
5. LoadLine:
   Rdroop=Ai%Rsense%R1/R2
   =7mohm

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=10A
   ESR=4.5mohm
   V=40.5mV
5. Inductor Spec:
   Isat=25A
   Idc=15.5A
   Rdcmax=5.5mOhm
   Rdcmtyp=5mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

VCORE_SEL1	VCORE_SEL2	+VGFX_CORE
L	L	VID - 26.8mV
L	H	VID - 15.3mV
H	L	VID - 11.5mV
H	H	VID

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
C	UX21	1.0

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<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_+VCCP	
	Engineer:	
Size: C	Project Name	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 93 of 1	

<Variant Name>

Title : Power_+VCCP

ASUSTeK COMPUTER INC

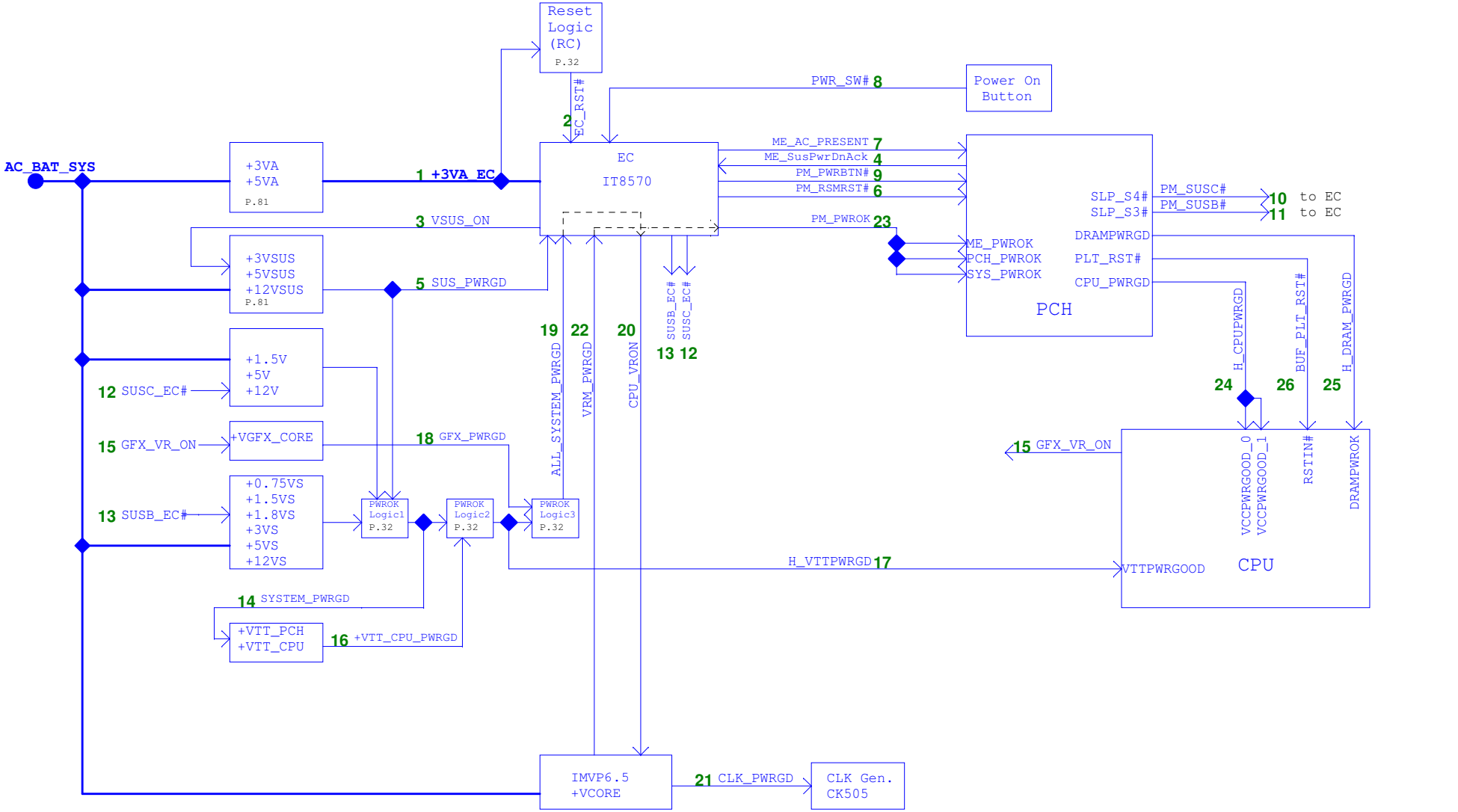
Engineer:

Size	Project Name	Rev
A3		1.0

Date: Thursday, February 11, 2010 Sheet 94 of 1

AC-IN Mode

k42Jv Power On Sequence Diagram Rev. 0.31



Power On Sequence

1 → 26

ASUSTeK COMPUTER INC

Title : POWER SEQUENCE

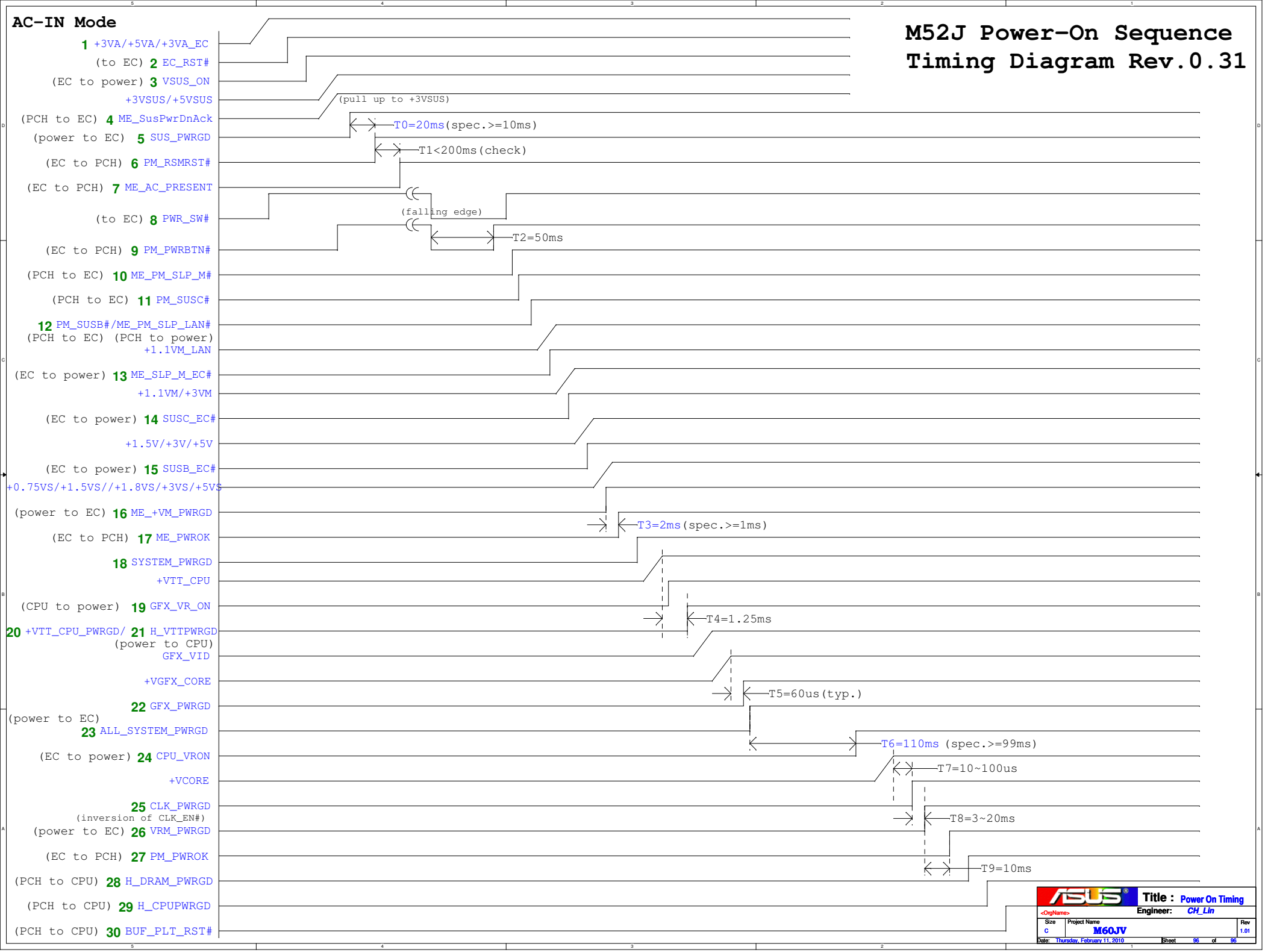
Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 95 of 96

M52J Power-On Sequence Timing Diagram Rev.0.31

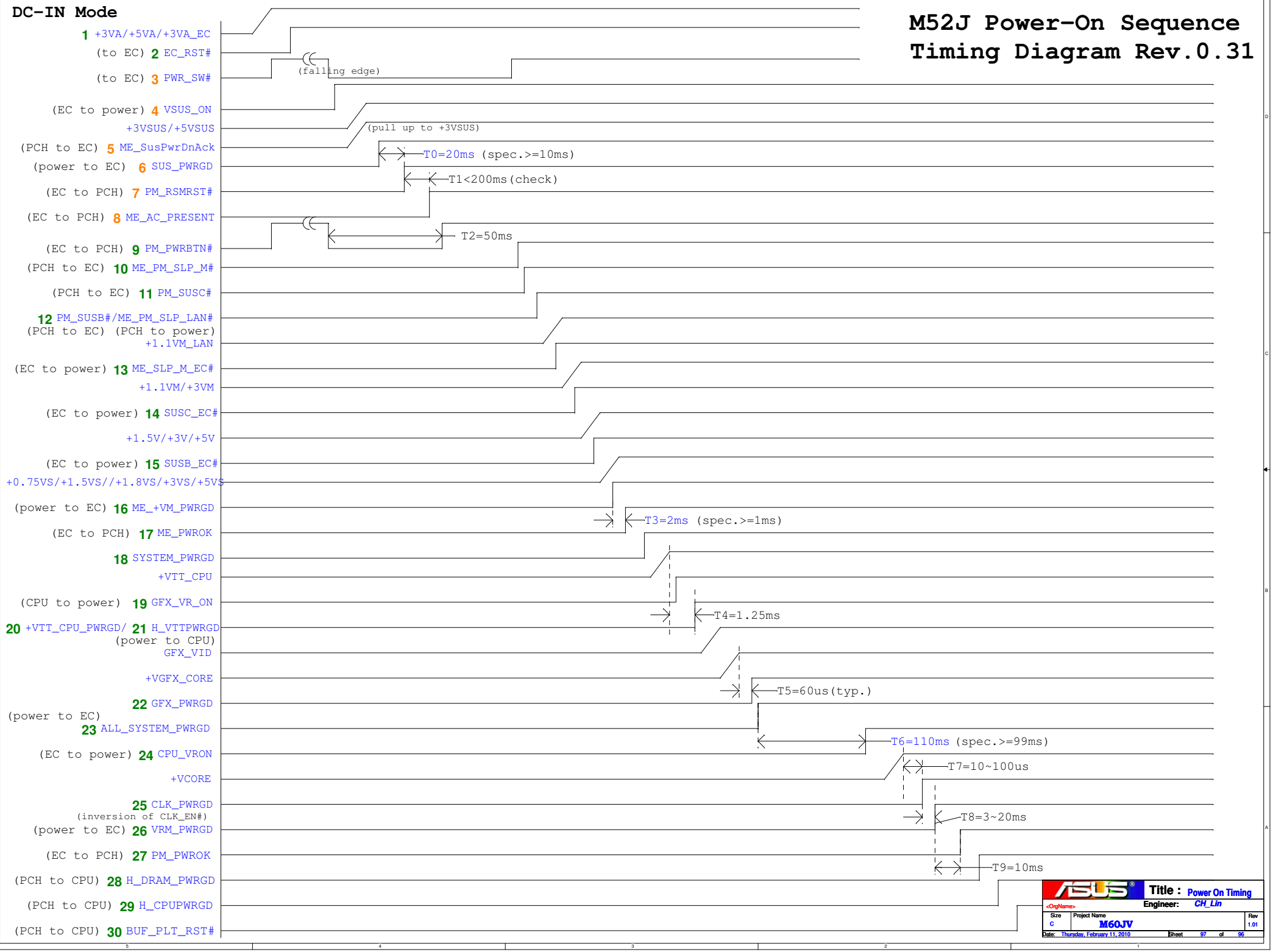
AC-IN Mode



Title : Power On Timing		
<OrgName>	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 96 of 96	

M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode



Title :	Power On Timing
<OrgName>	Engineer: CH_Lin
Size: C	Project Name: M60JV
Rev: 1.01	
Date: Thursday, February 11, 2010	Sheet 97 of 96