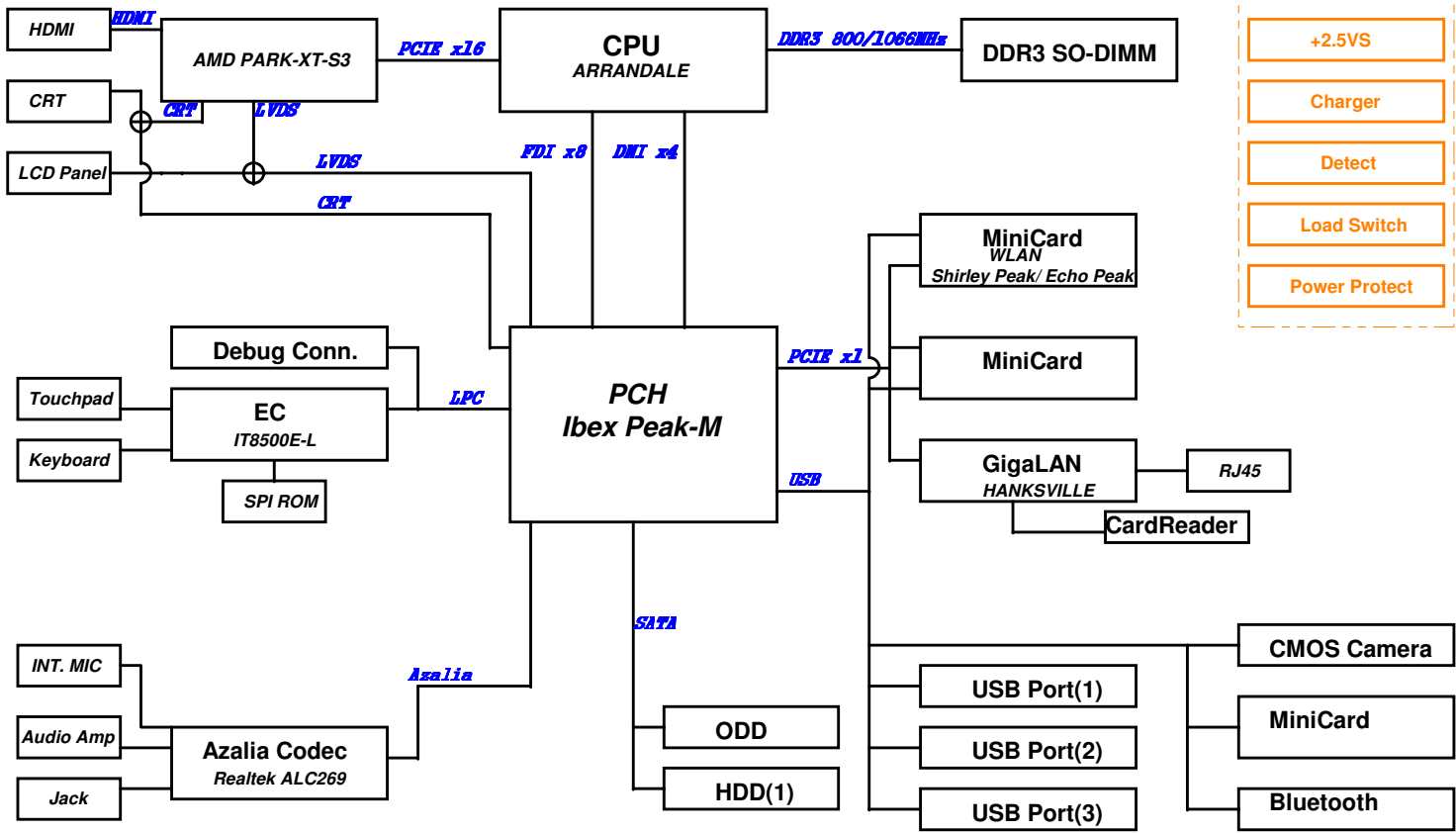


K42Jr SCHEMATIC Revision 2.0

Power

- VCORE
- System
- 1.5VS & 1.05VS
- DDR & VTT
- +2.5VS
- Charger
- Detect
- Load Switch
- Power Protect

BLOCK DIAGRAM



Clock Generator
ICS ICS9LPR427

VID controller

Discharge Circuit

DC & BATT. Conn.

PWM Fan

Reset Circuit

Skew Holes

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6	CPU(4)_PWR
7	CPU(5)_XDP
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82	PW_I/O_VTT_CPU&+1.1VM
83	PW_I/O_DDR & VTT& +1.8VS
84	PW_I/O_3VM & ME_+VM_PWEGD
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91	PW_LOAD SWITCH
92	PW_PROTECT
93	PW_SIGNAL
94	PW_FLOWCHART

**PCH_IBEX
GPIO**

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAYPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	-	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSN#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	-	-	+3VS
GPIO 49	GPO	GPU_RST#	-	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	-	-	+5VS
GPIO 53	GPO	-	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	GPO	-	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU (DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	-	-	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

**EC
IT8512**

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	CHG_LED#
GPA2	-	-
GPA3	-	-
GPA4	0	LCD_BL_PWM
GPA5	0	FAN0_PWM
GPA6	-	-
GPA7	-	-
GPB0	0	SUSC_EC#
GPB1	0	SUSB_EC#
GPB2	-	-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RC_IN#
GPB7	0	PM_RSMRST#
GPC0	-	-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	-	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	-	-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	-	-
GPE0	0	VSUS_ON
GPE1	0	EGAD (IT8301 Address/Data connect)
GPE2	0	EGCS (IT8301 Cycle Start connect)
GPE3	0	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPFO	-	-
GPF1	-	-
GPF2	I	EXP_GATE#
GPF3	-	-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	0	THRO_CPU
GPF7	-	-
GPFO	-	-
GPB1	I	PM_SUSB#
GPB2	-	-
GPB6	-	-
GPH0	IO	PM_CLKRUN#
GPH1	-	-
GPH2	0	GFX_VR_ON
GPH3	0	BAT_LEARN
GPH4	-	-
GPH5	0	NUM_LED#
GPH6	0	CAP_LED#
GPI0	-	-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6	-	-
GPI7	-	-
GPJ0	0	CPU_VRON
GPJ1	0	PM_PWROK
GPJ2	0	VSET_EC
GPJ3	0	ISET_EC
GPJ4	0	TP_LED
GPJ5	-	-

**EC
IT8301**

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2	-	-
GPIO3	-	-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	O	ME_PWROK
GPIO13	-	-
GPIO14	O	ME_SLP_M_EC#
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
GPIO31	-	-
GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO35	-	-
GPIO36	-	-
GPIO37	-	-

SM_BUS ADDRESS :

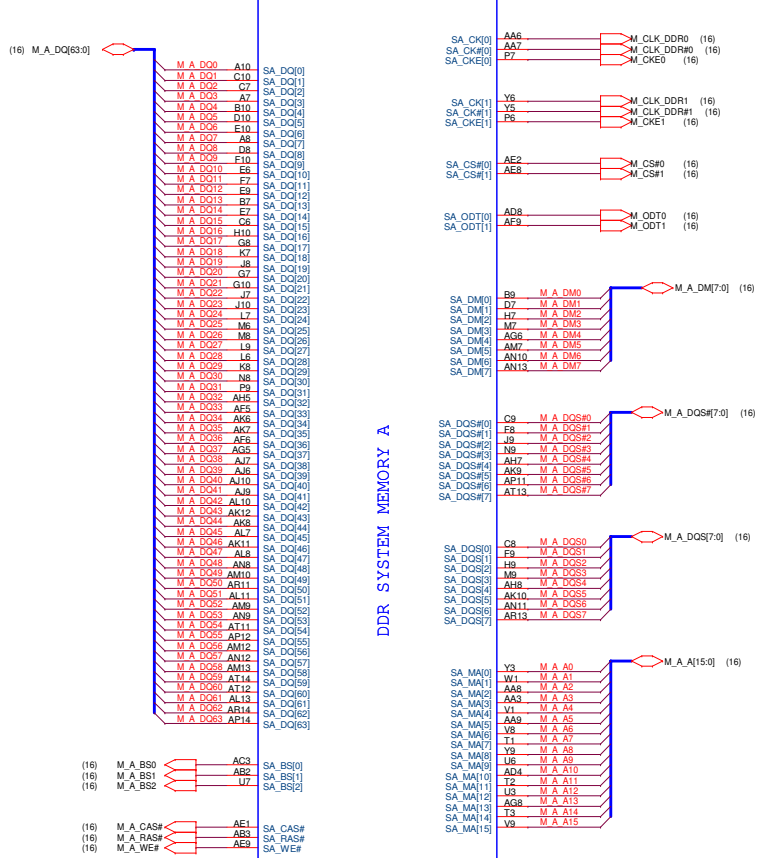
PCH Master	
SM-Bus Device	SM-Bus Address
Clock Generator(IC59LPR362)	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
VID Controller(ASM8272)	0011011x (36)
WiFi/WiMax	N/A
EC Master (SMB1)	
SM-Bus Device	SM-Bus Address
CPU Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	-
PCIE 5	ESATA (for pre-E51)
PCIE 6	GLAN
PCIE 7	-
PCIE 8	-

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	NewCard
USB 6	Minicard TV Tuner
USB 7	-
USB 8	-
USB 9	WLAN
USB 10	-
USB 11	-
USB 12	Bluetooth
USB 13	Finger Printer

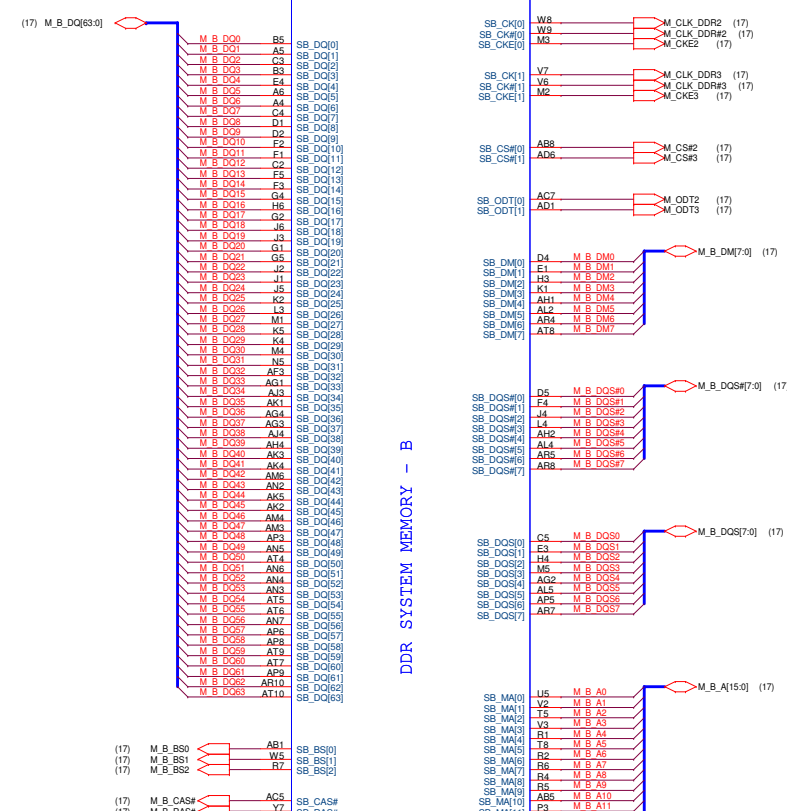
SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

U3001C

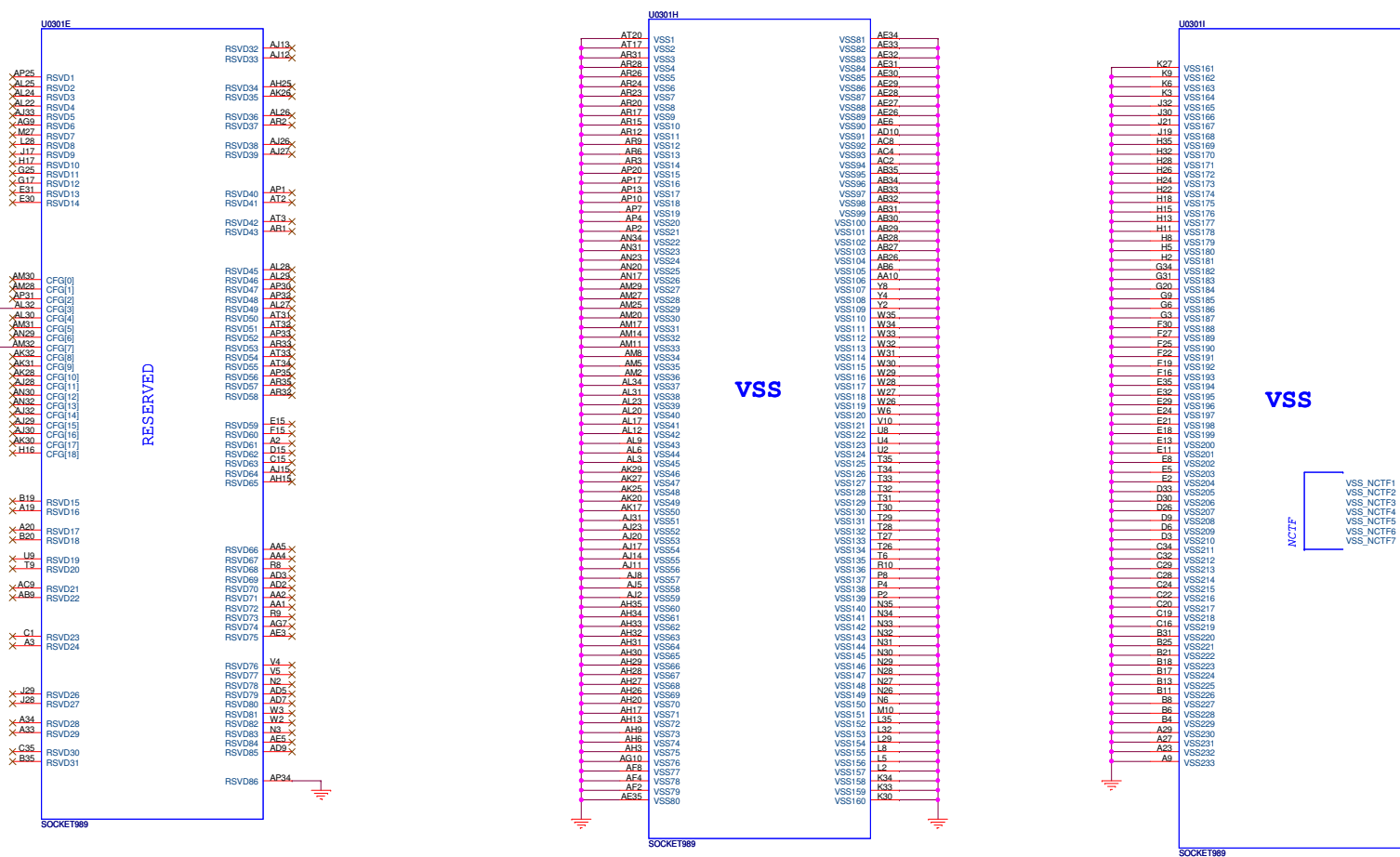


SOCKET989

U3001D



SOCKET989



CFG strapping information:

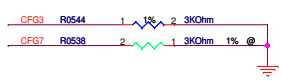
CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
 - 11 = 1 x 16 PEG (Default)
 - 10 = 2 x 8 PEG

CFG[3]: PCIe Static Numbering Lane Reversal.(Arrandale Only)
 - 1: Normal Operation (Default)
 - 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale Only)
 - 1: Disabled - No Physical Display Port attached to Embedded DisplayPort
 - 0: Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 I/O specifications.(Clarksfield Only)
 - 0: Enabled - Connected to GND with 3.0k Ohm/5% resistor for a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact Arrandale functionality.
 - 1: Disabled - Not connected to GND with 3.0k Ohm/5% resistor for a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.
 Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



CFG strapping information:

For Arrandale

CFG[2:0]: Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.

CFG[3] - PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.

- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.

CFG[17:5] - Reserved configuration pins.

Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifurcation:

- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pins.

CFG[3] - Reserved (Used by Arrandale Pprocessors for PCI Express* Static Lane Numbering Reversal)

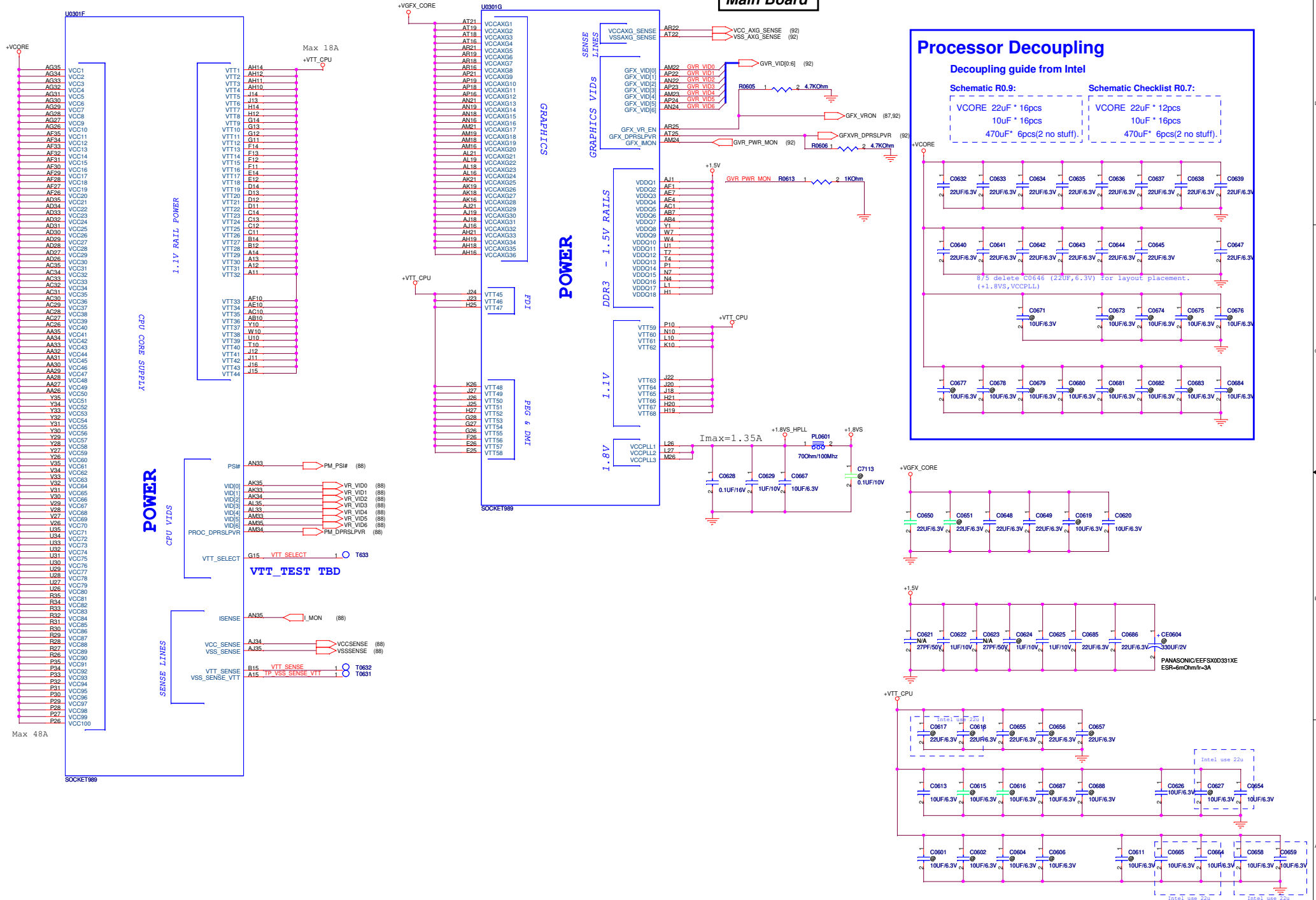
CFG[11:4] - Reserved configuration pins.

CFG[12] - N/A on Clarksfield processors.

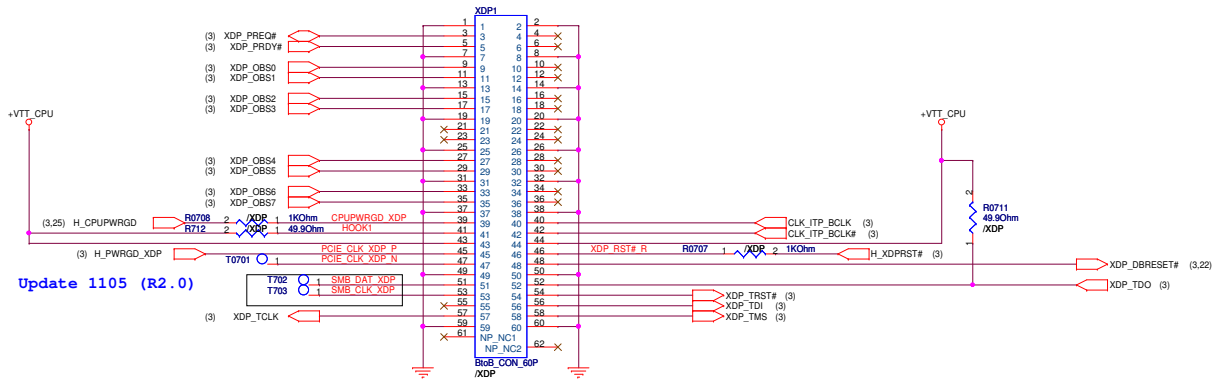
CFG[17:13] - Reserved configuration pins.

Note: Hardware straps are sampled after RSTIN# de-assertion.

Main Board



CPU XDP connector



Update 1105 (R2.0)

5

4

3

2

1

D

D

C


C

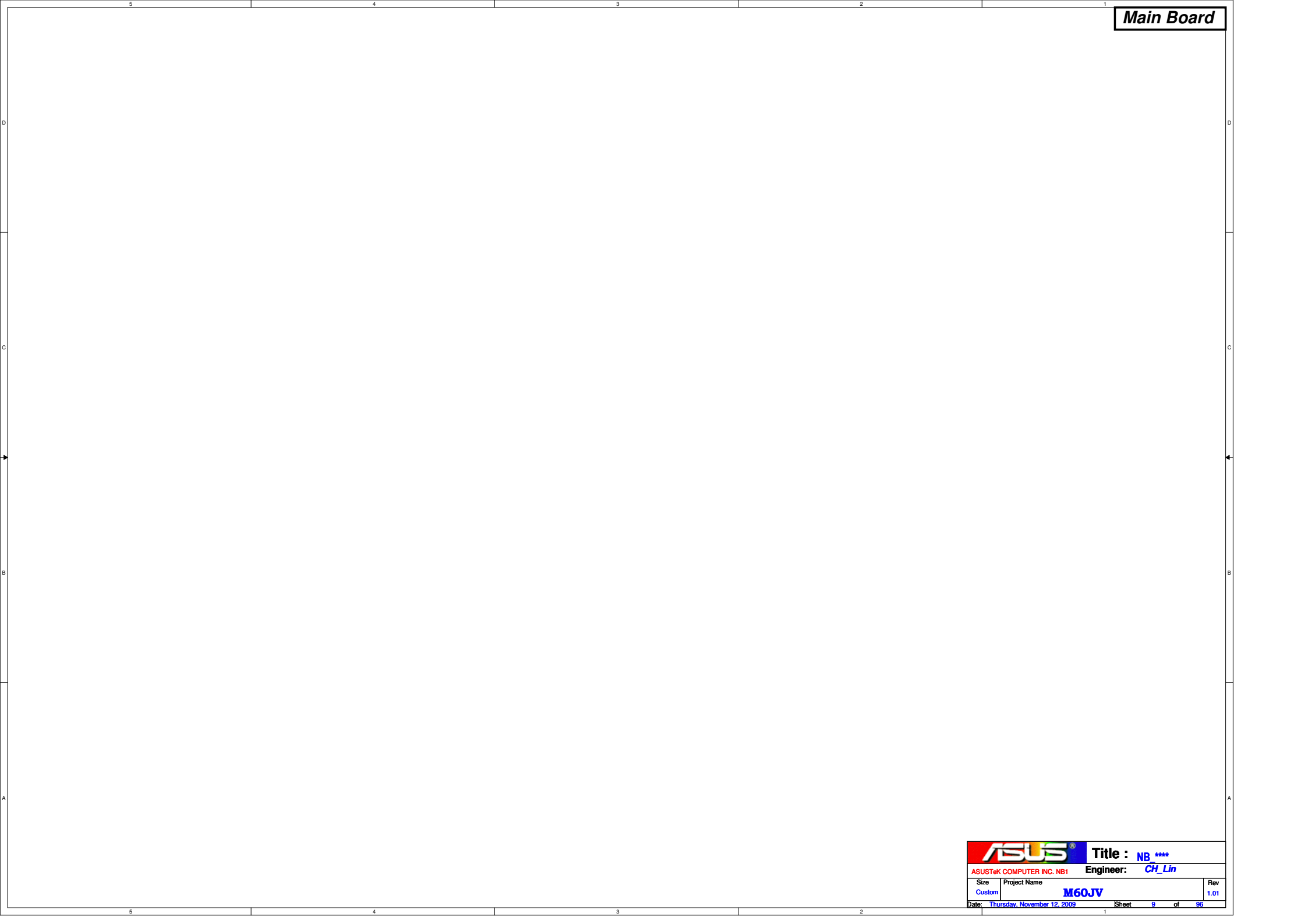
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B

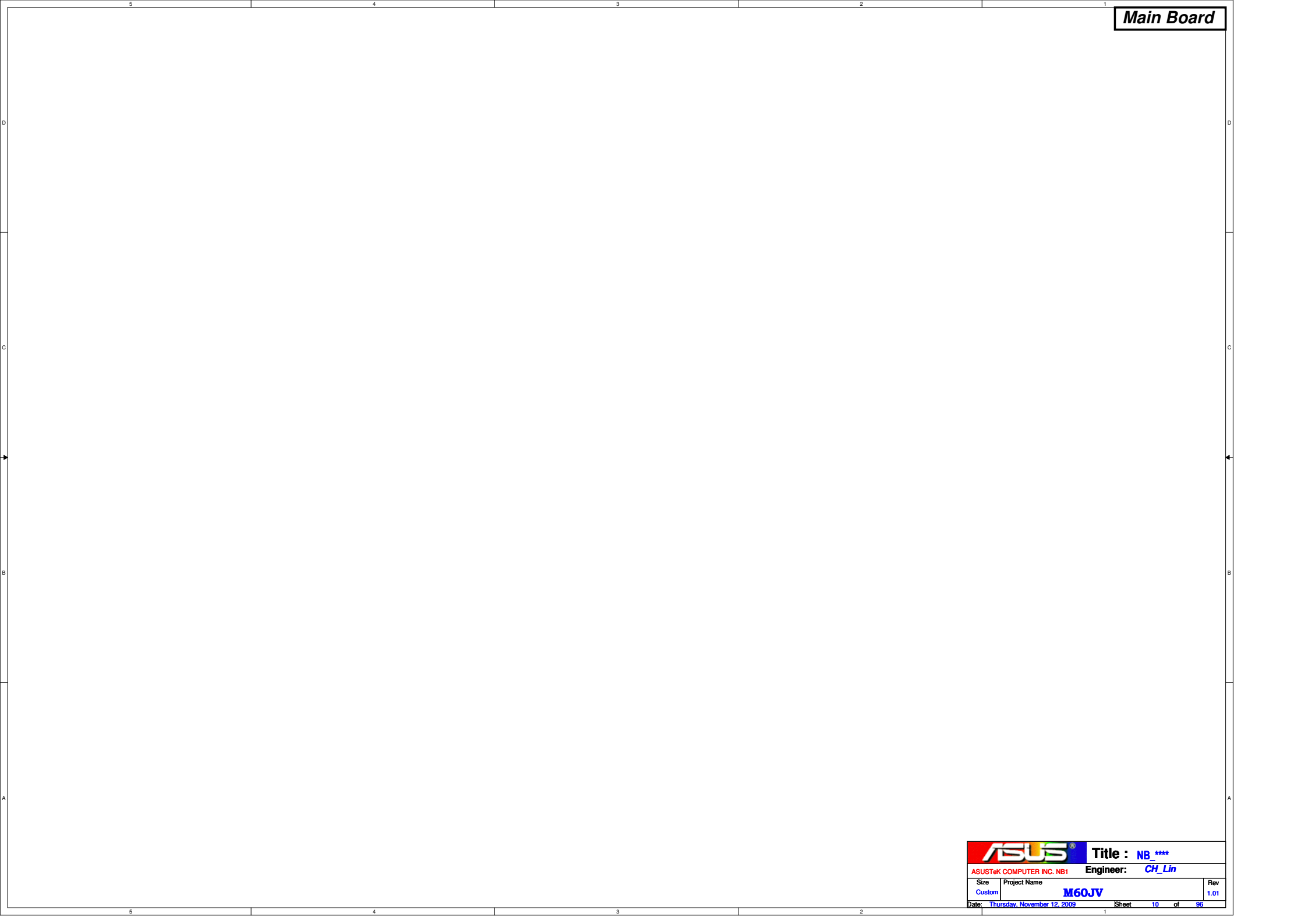
A


A

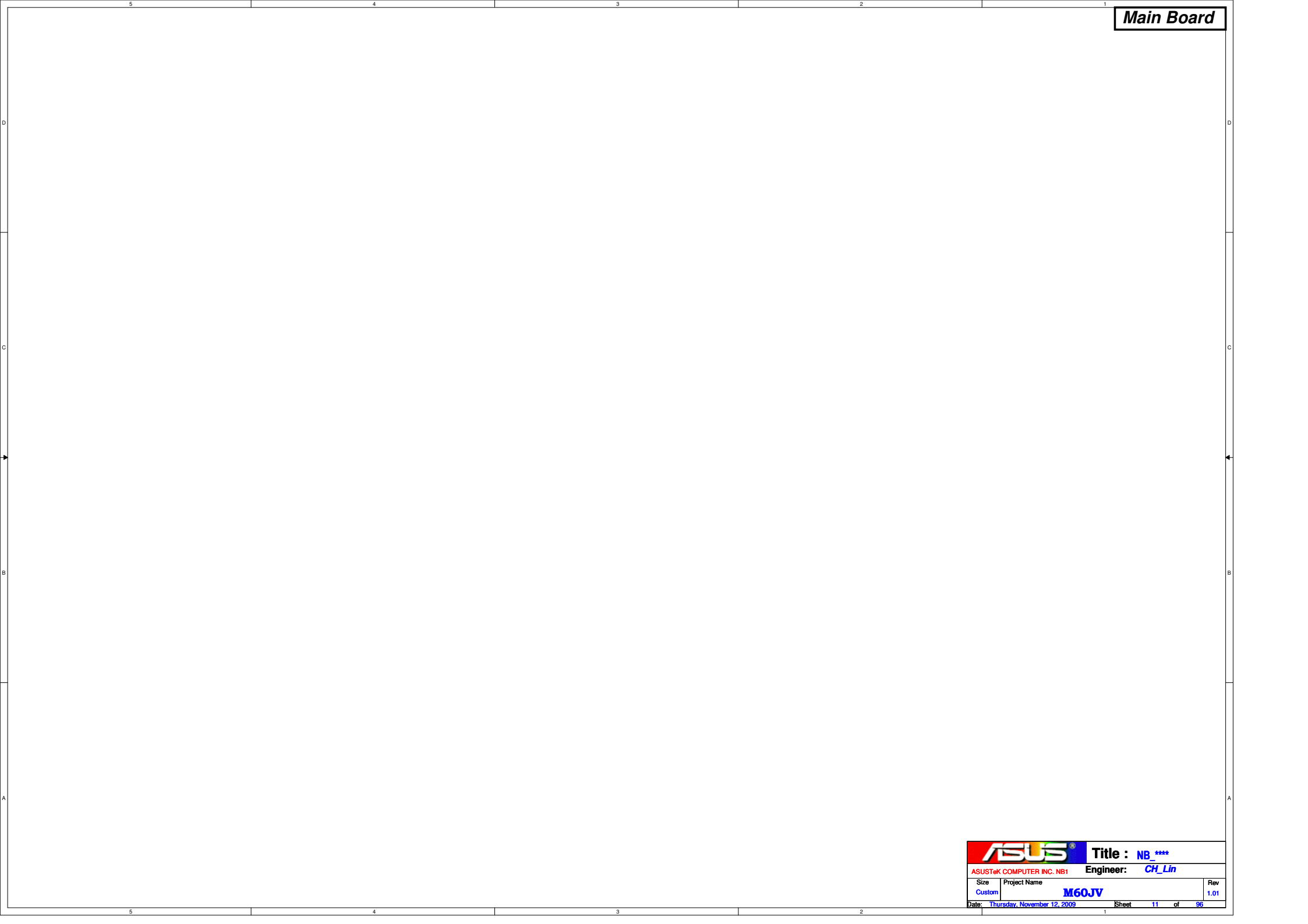
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ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	8 of 96




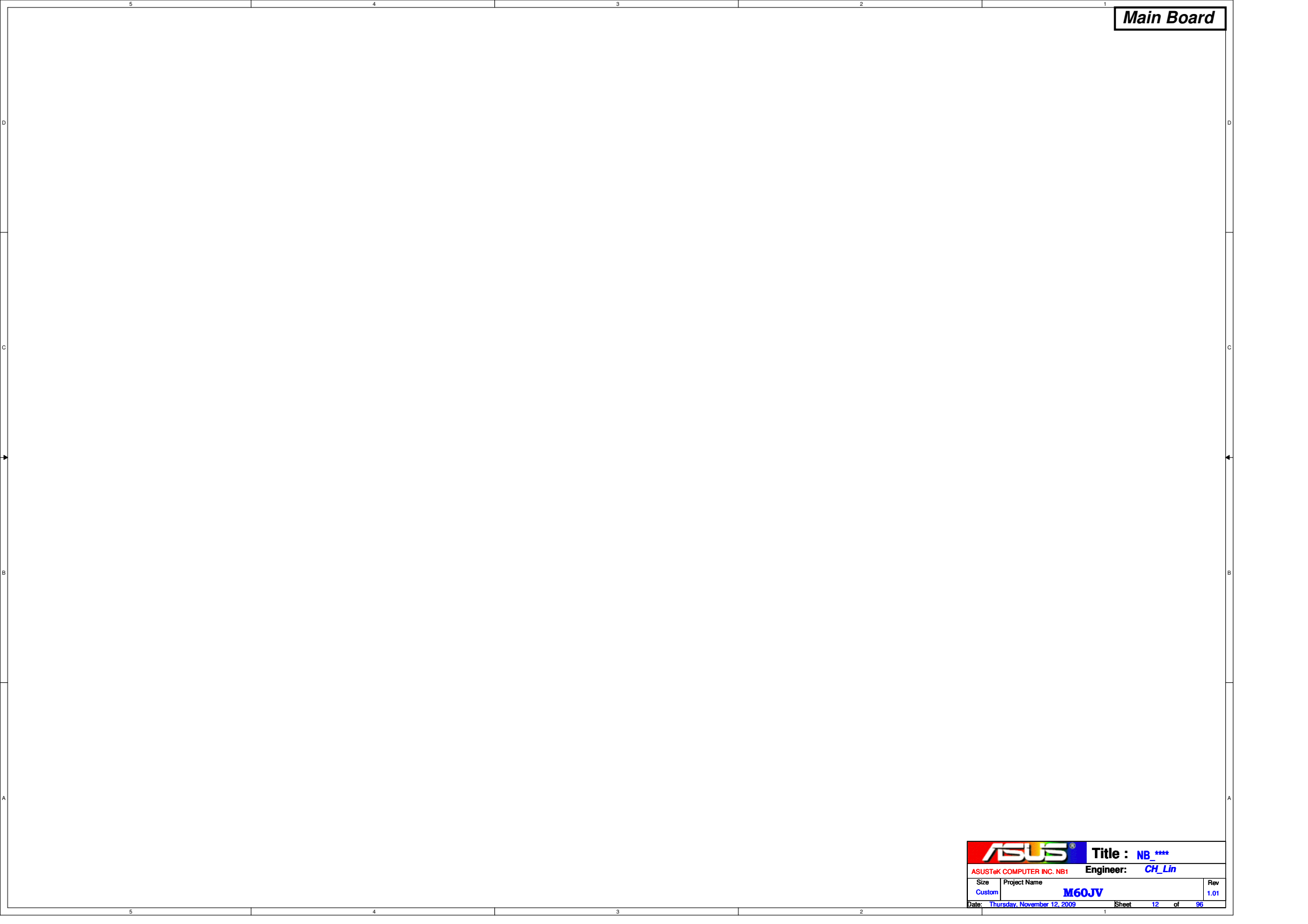
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ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	9 of 96




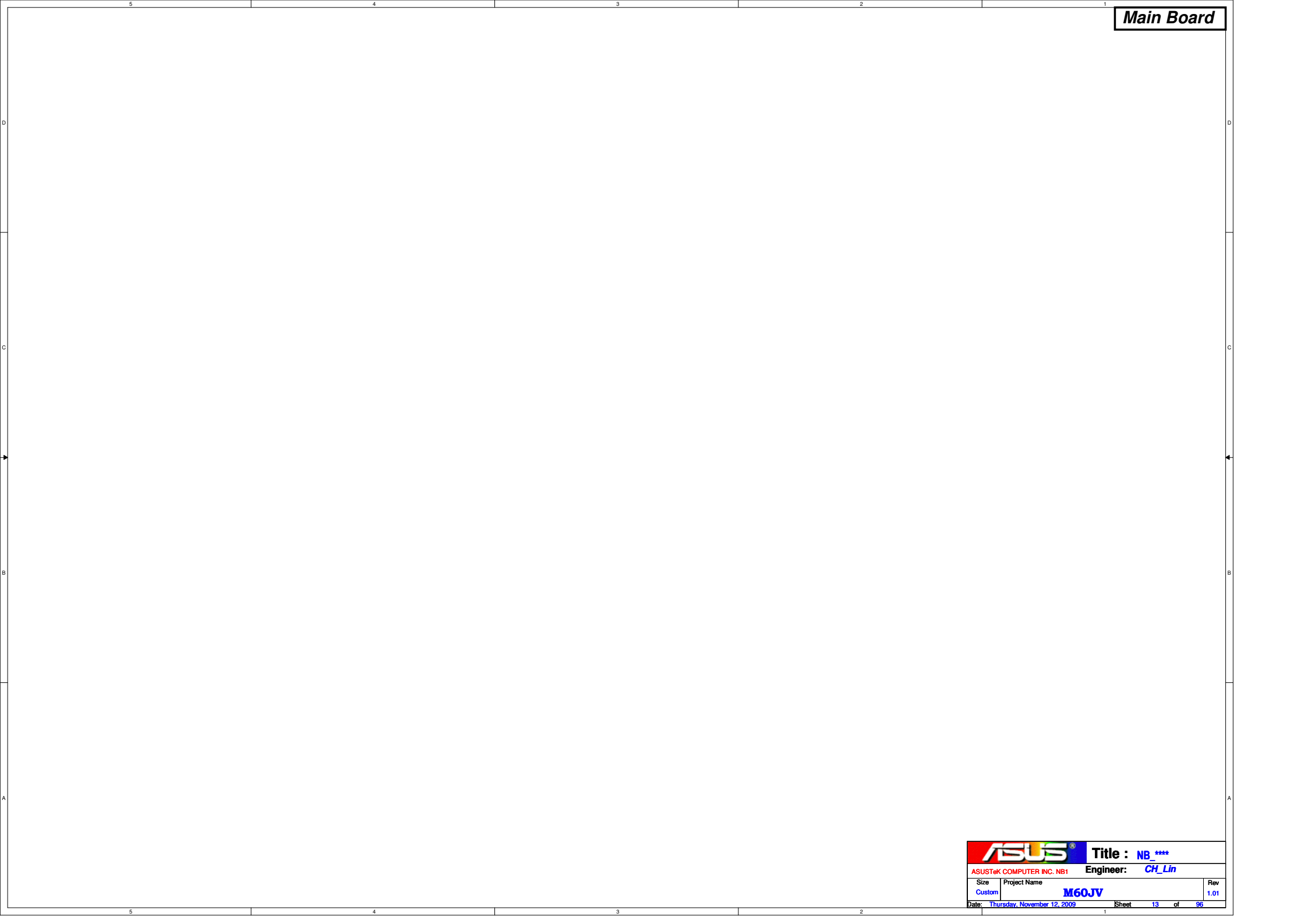
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ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	10 of 96




		Title : NB ****	
ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	11 of 96



		Title : NB ****	
ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	12 of 96



		Title : NB ****	
ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	13 of 96

5

4

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1

D

D

C


C

B

B

A

A

		Title :
ASUSTeK COMPUTER INC. NB6		Engineer: <i>CH_Lin</i>
Size	Project Name	Rev
A	M60JV	1.01
Date: <i>Thursday, November 12, 2009</i>		Sheet <i>14</i> of <i>96</i>

5

4

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2

1

5

4

3

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1

D

D

C

C

B

B

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A



Title :

ASUSTeK COMPUTER INC. NB6

Engineer: CH_Lin

Size	Project Name	Rev
A	M60JV	1.01

Date: Thursday, November 12, 2009 Sheet 15 of 96

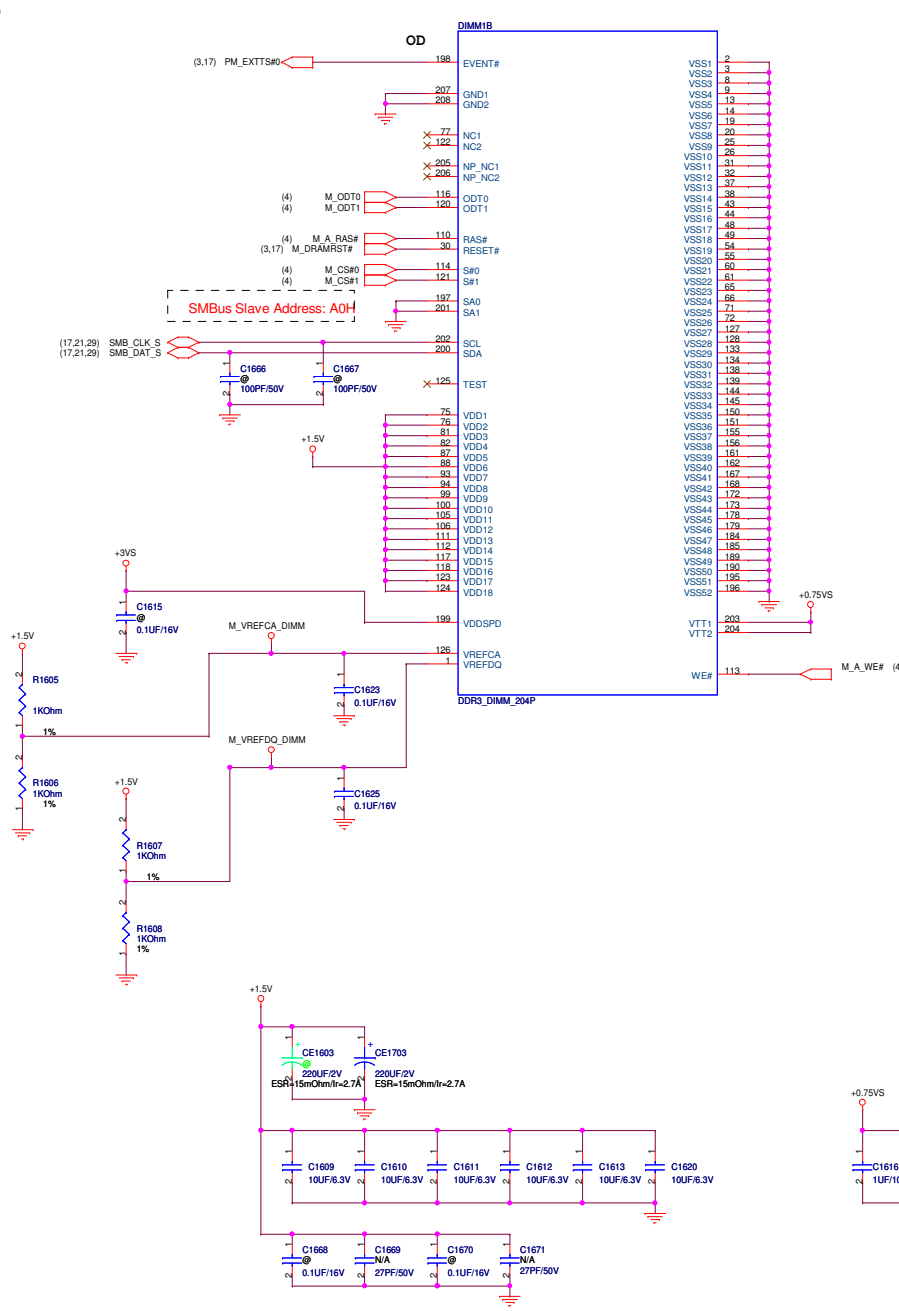
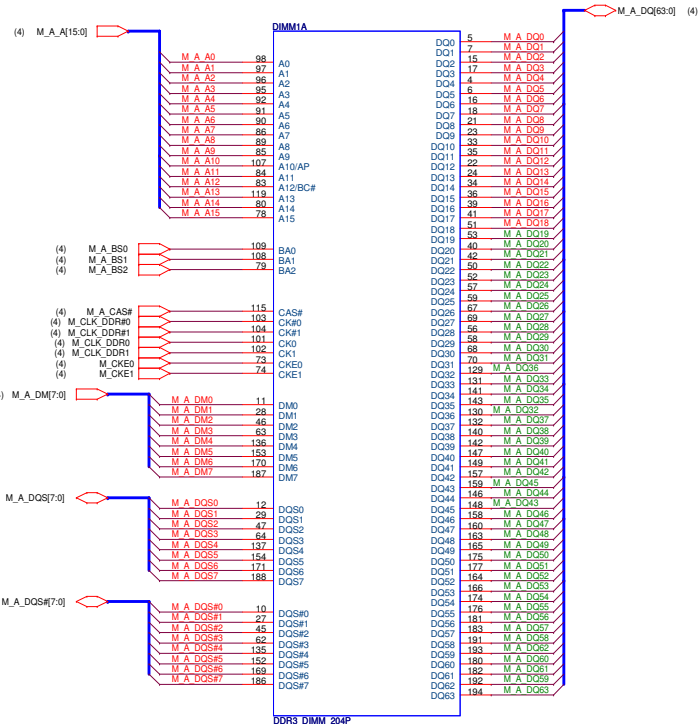
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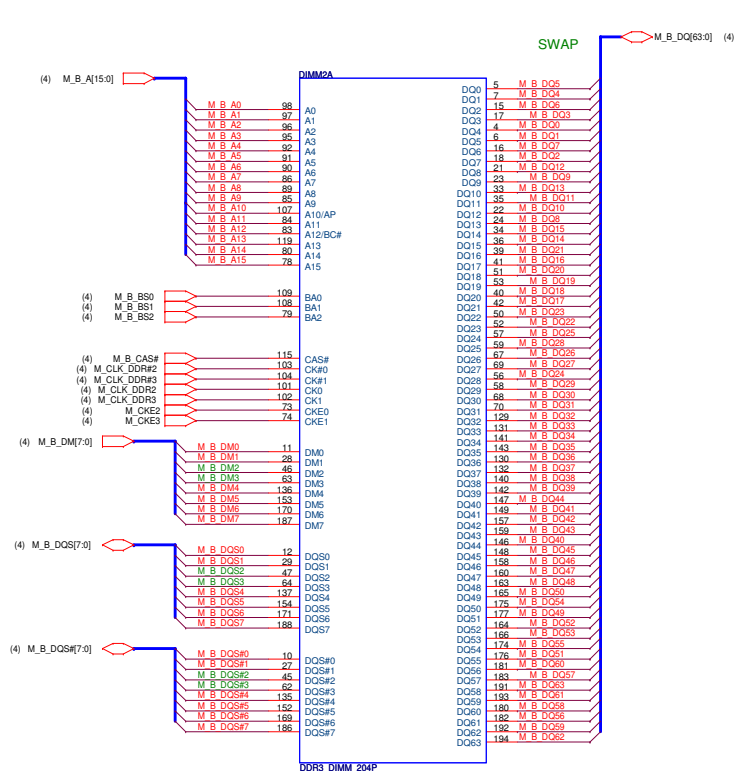
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3

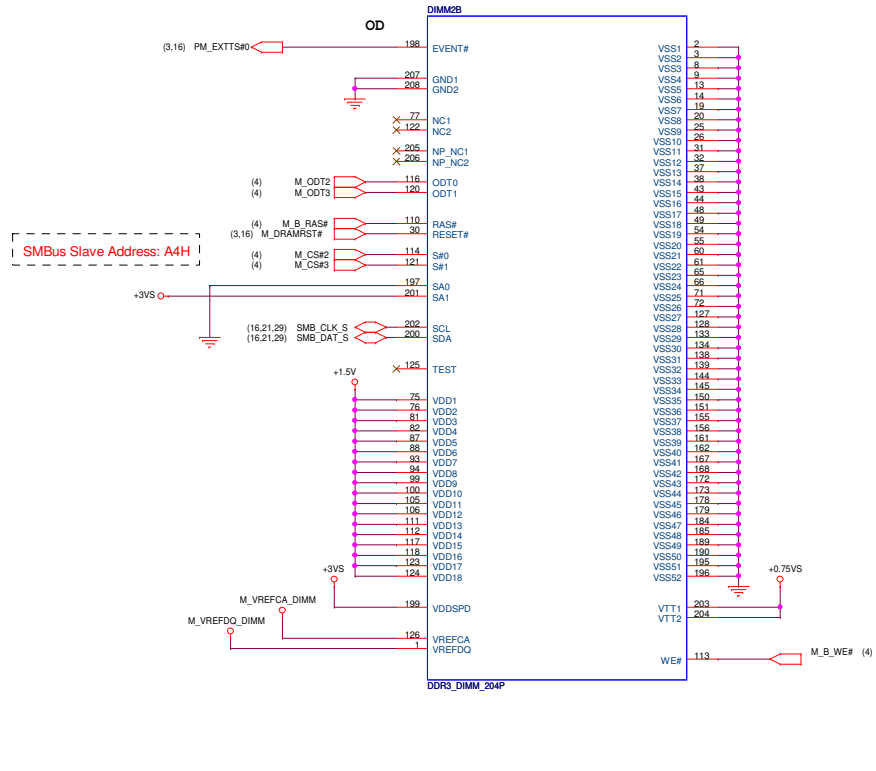
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STD 5.2mm



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C

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A


		Title DDR3 CA_DQ VOLTAGE	
ASUSTeK COMPUTER INC. N66		Engineer: CH_Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	18 of 95

Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO_REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. NOTE: This signal should not be pulled low.
GNT[3]#/GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. If the signal is sampled low, this indicates that the system is strapped to the "Topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high.

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment															
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <table border="1"> <thead> <tr> <th>Bit11</th> <th>Bit 10</th> <th>Boot BIOS Destination</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	PCI																
1	1	SPI																
0	0	LPC																

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDA TA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDA TA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDA TA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

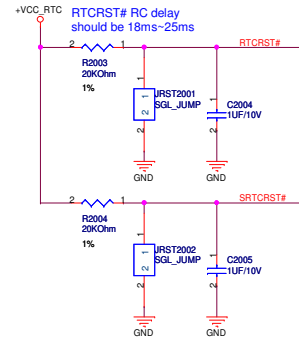
Signal	Usage	When Sampled	Comment															
GNT[0]#	Boot BIOS Strap bit [0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <table border="1"> <thead> <tr> <th>Bit11</th> <th>Bit 10</th> <th>Boot BIOS Destination</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	PCI																
1	1	SPI																
0	0	LPC																
GNT2# / GPIO53	ESI Security (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.															
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. NOTE: This signal should not be pulled high.															

Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN#/GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/debug environments ONLY. NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SP1_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. NOTE: This signal should not be pulled high.
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. NOTE: This signal should not be pulled low.
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. NOTE: A strong pull up may be needed for GPIO functionality.
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS clear function

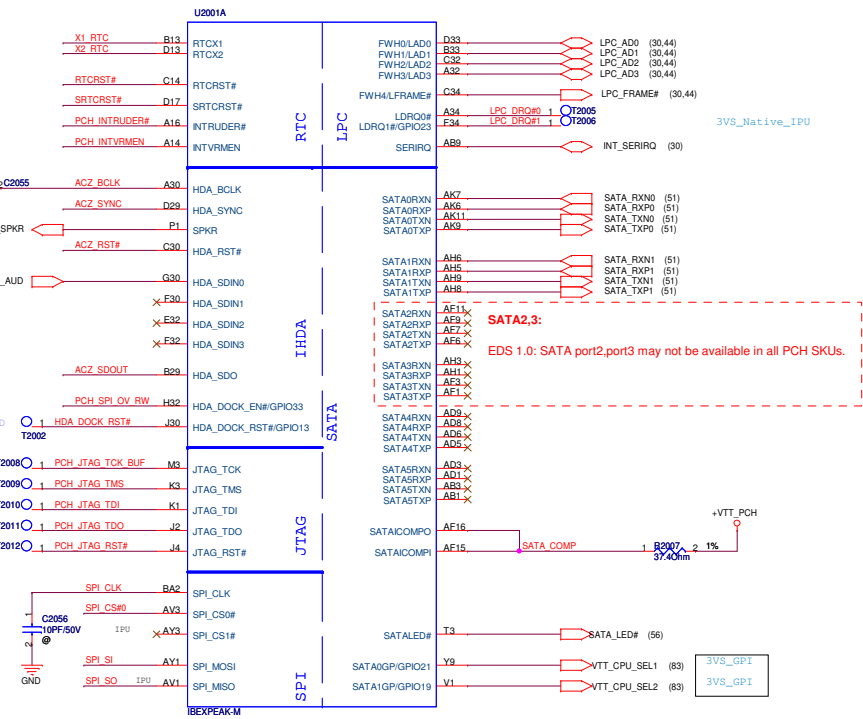
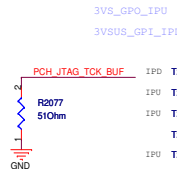
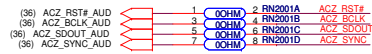
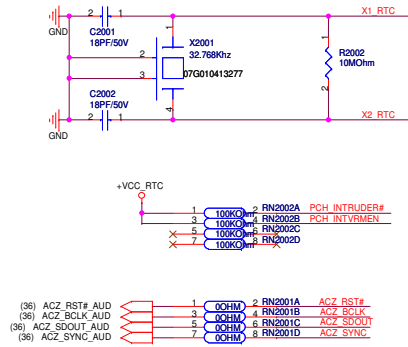
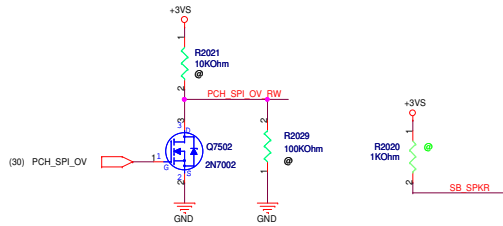
CMOS Settings		JNST2001		TPM Settings		JRST2002	
Clear CMOS	Shunt	Clear ME RTC Registers	Shunt	Clear ME RTC Registers	Shunt	Clear ME RTC Registers	Shunt
Keep CMOS	Open (Default)	Keep ME RTC Registers	Open (Default)	Keep ME RTC Registers	Open (Default)	Keep ME RTC Registers	Open (Default)



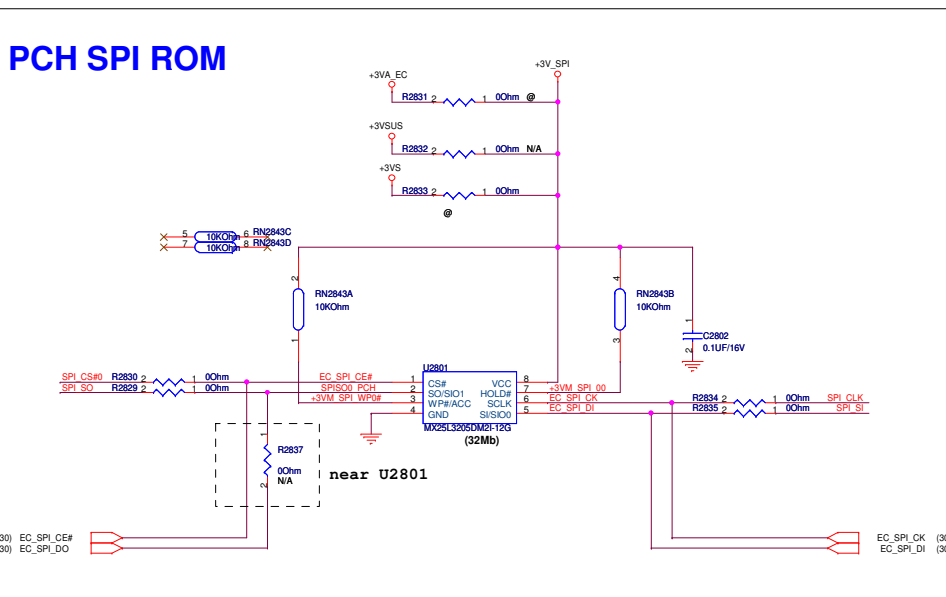
DG2_0 P297
RTCRST# and SRTCST# can not be shorted together

Strap information:

	B	L
ACZ_SYNC: Select VCCVRR 1.5V or 1.8V (IPU)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_SI: IIPM strap. (IPD)	Enable	Disable
PCH_INTVRMEN: Integrated 1.05 V VRR Enable /Disable	Enable	Disable



SATA2,3:
 EDS 1.0: SATA port2,port3 may not be available in all PCH SKUs.



Update 1105 (R2.0)

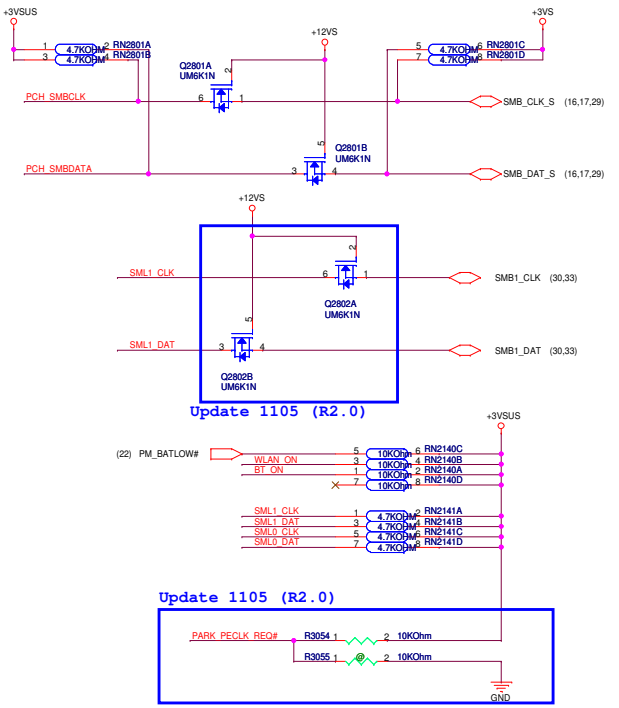
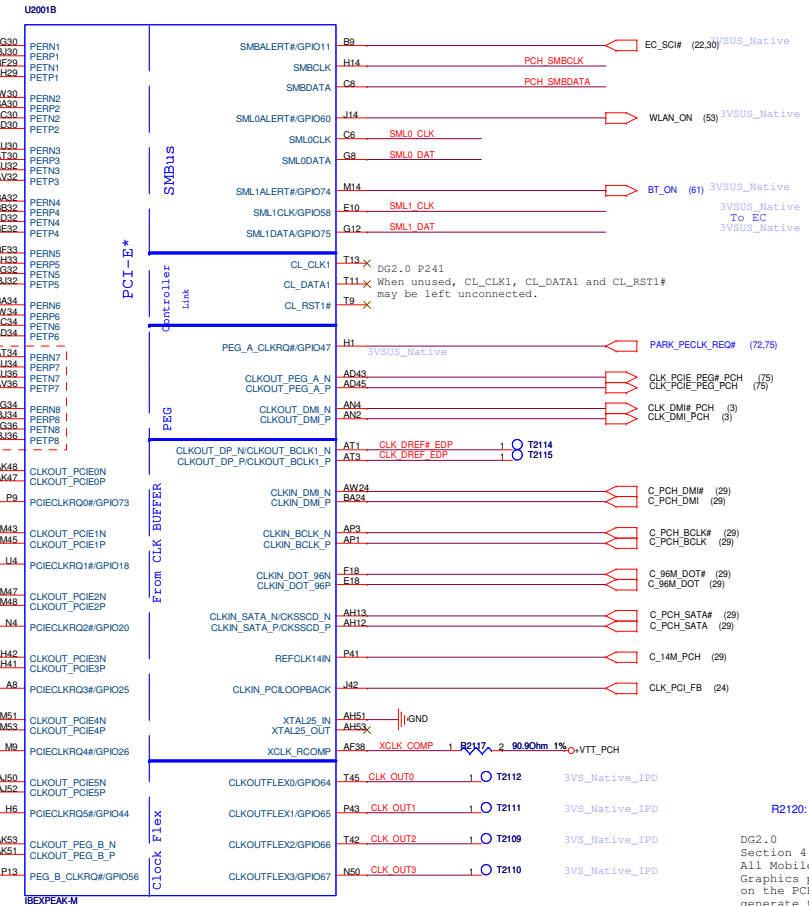
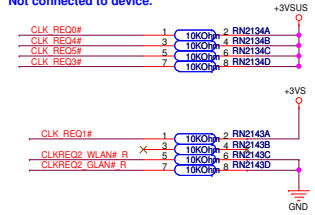
PCIE2: WLAN
 (S3) PCIE_RX2_WLAN
 (S3) PCIE_RXP2_WLAN
 (S3) PCIE_TX2_WLAN
 (S3) PCIE_TXP2_WLAN

PCIE5: LAN
 (41) PCIE_RX_LAN_N
 (41) PCIE_RX_LAN_P
 (41) PCIE_TX_LAN_N
 (41) PCIE_TX_LAN_P

PCIE7,8:
 EDS 1.0: port7,port8 may not be available in all PCH SKUs.

Note: Place these resistors near to PCIe Slots

PCH CLKREQ Setting:
 Not connected to device.



If not use crystal, please change C1201 to 0 Ohm

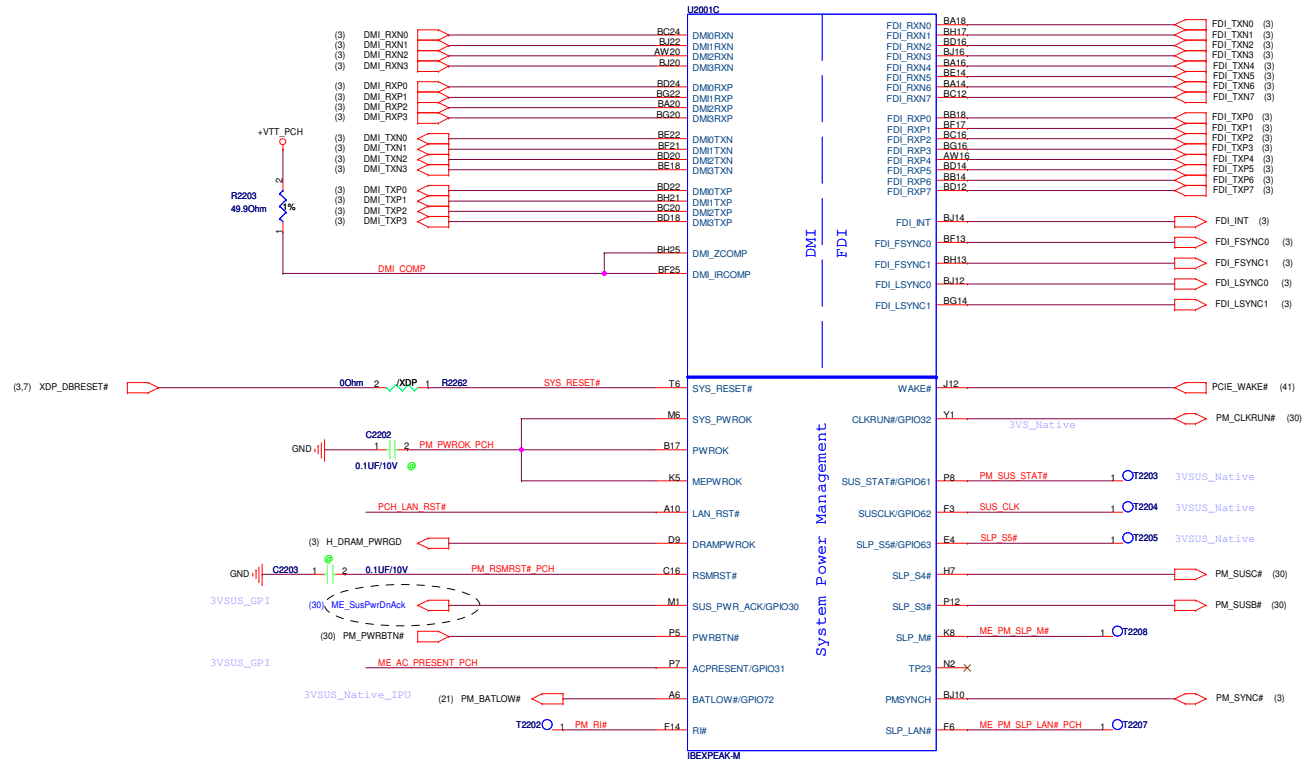
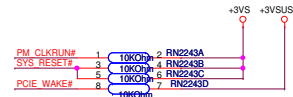
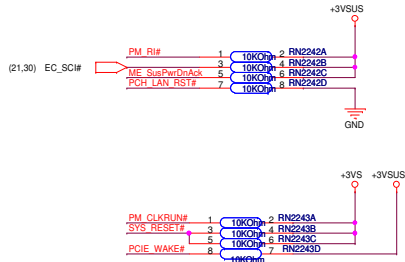
R2120: For Xtal measurement

DG2.0
 Section 4.2.4.1: Added 25-MHz Crystal routing guideline. All Mobile Intel S Series Chipset-based Integrated Graphics platforms are required to use a 25-MHz crystal on the PCH XTAL25_IN/OUT to enable the PCH to generate the display clocks. Display Clock generation is integrated into the PCH.

Integrated Graphics platforms that implement DVI/DP/HDMI/e-DP are required to use Display Clock Integration (DCI) (25M crystal to generate PCI display clocks) to improve signal integrity and mitigate risk of electrical compliance and associated functional failures

WW35 Update: Integrated Graphics platforms that use onlyLVDS and/or VGA Displays may use Buffer Through Mode (BTM) and leave 25-MHz crystal and RC components unstaffed

pre-ES1 not support
Reversal Feature



R1.1,item L15

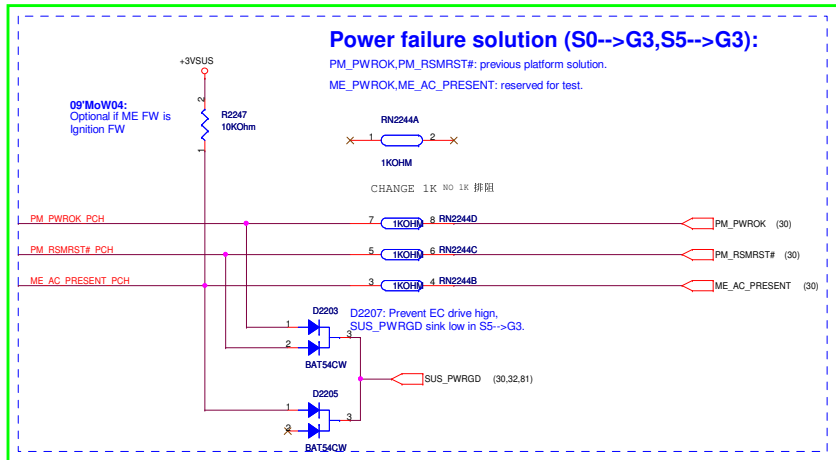
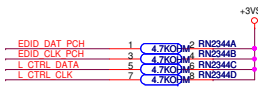


Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required Note: Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required Note: If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

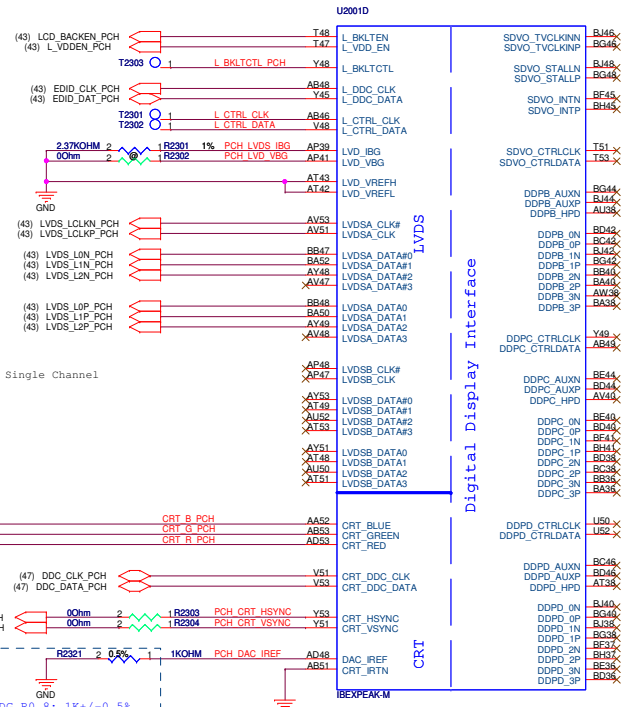
ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.



LVDS Disable: (For discrete graphic)

1. NC:
 LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
 LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
 LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
 L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
 LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:
 VccALVDS, VccTX_LVDS



CRB R0.9, DG R0.8: 1K+/-0.5%

Intel checklist recommend:
 1.02K PD resistor to 0.5%

CRT Disable: (For discrete graphic)

1. NC:
 CRT_RED, CRT_GREEN, CRT_BLUE
 CRT_HSYNC, CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:
 DAC_IREF

3. Connected to GND:
 CRT_ITRN

4. Connect to +V3.3:
 VCCADAC

U2001E

- X_H40 AD0
- X_N44 AD1
- X_C44 AD2
- X_A38 AD3
- X_C36 AD5
- X_J34 AD4
- X_A45 AD5
- X_A45 AD6
- X_A45 AD7
- X_E36 AD8
- X_H48 AD9
- X_E40 AD10
- X_C40 AD10
- X_M48 AD11
- X_M48 AD12
- X_M45 AD13
- X_M45 AD14
- X_M40 AD15
- X_M45 AD16
- X_J36 AD17
- X_K48 AD18
- X_K48 AD19
- X_K46 AD20
- X_M51 AD21
- X_J42 AD22
- X_A42 AD23
- X_A42 AD24
- X_L44 AD25
- X_F42 AD26
- X_J40 AD28
- X_A46 AD29
- X_F44 AD29
- X_M47 AD30
- X_M36 AD31
- X_J30 C:BE0#
- X_G42 C:BE1#
- X_H47 C:BE2#
- X_G34 C:BE3#

NVRAM

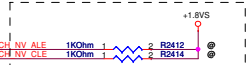
PCI

USB

- NV_CE#0 AV3
- NV_CE#1 B11
- NV_CE#2 A15
- NV_CE#3 BDB
- NV_DQS0 AV3
- NV_DQS1 BDB
- NV_DQ0NV_I00 AP7
- NV_DQ1NV_I01 AT6
- NV_DQ2NV_I02 AT6
- NV_DQ3NV_I03 BBT
- NV_DQ4NV_I04 BBT
- NV_DQ5NV_I05 AV3
- NV_DQ6NV_I06 BBS
- NV_DQ7NV_I07 B44
- NV_DQ8NV_I08 BBE
- NV_DQ9NV_I09 BBE
- NV_DQ10NV_I10 BBE
- NV_DQ11NV_I11 BBE
- NV_DQ12NV_I12 BCB
- NV_DQ13NV_I13 BCB
- NV_DQ14NV_I14 B46
- NV_DQ15NV_I15 BDB
- NV_ALE NV_ALE
- NV_CLE NV_CLE
- NV_RCOMP AV2
- NV_RB# AV7
- NV_WR#_RE# AV8
- NV_WR#_RF# AV8
- NV_WE#_CK0 AV11
- NV_WE#_CK1 BE8

Strap information:

	H	L
PCIAV_ALE# Strap Intel Anti-Theft Technology HDD Data Protection Enable	Enable	Disable
PCIALE# Strap DMI Termination Voltage		



NV_ALE: Strap Intel Anti-Theft Technology HDD Data Protection Enable. (H: enable)
 NV_CLE: Strap DMI Termination voltage

K82JR	Recommend settings
0 USB PN0	
1 USB port	
2 USB port	
3	
4 WiFi/WiMax	
5	
6	
7	
8	
9 Camera	
10	
11	
12 BT (1.1)	
13	

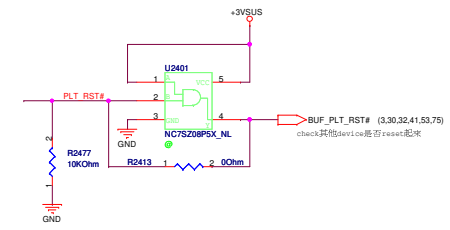
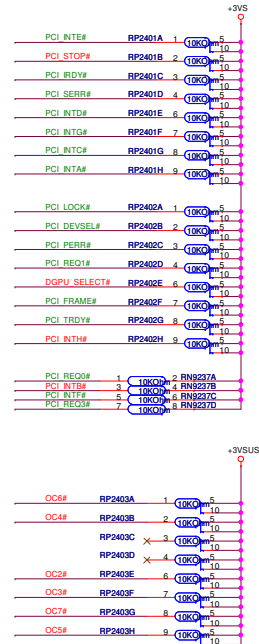
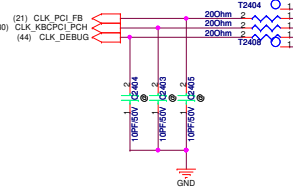
DGPU_SELECT#:
 0=GPU, 1=GPU

(43,47) DGPU_SELECT#
 3VS_Native [50,52,54]

3VS_Native_IPU [51,53,55]
 3VS_GPI [2,3,4,5]

PCI_PME#: Internal PU to suspend plane.
 change to PCI_CLK4 to sync ICS364

IPU T2407 1 PCI_PME# M7



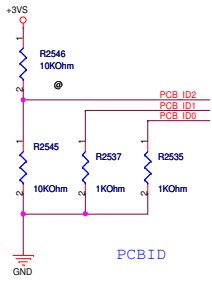
GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap		
PCI_GNT0#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

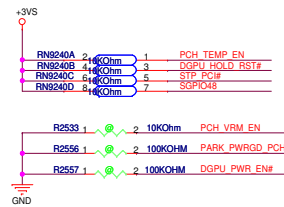
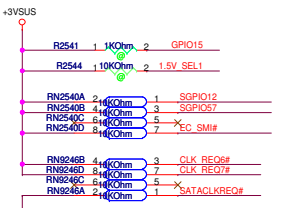
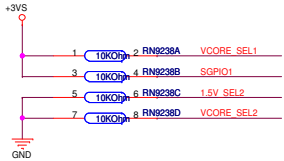
Sampled on rising edge of PWROK

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override	
High=Default	



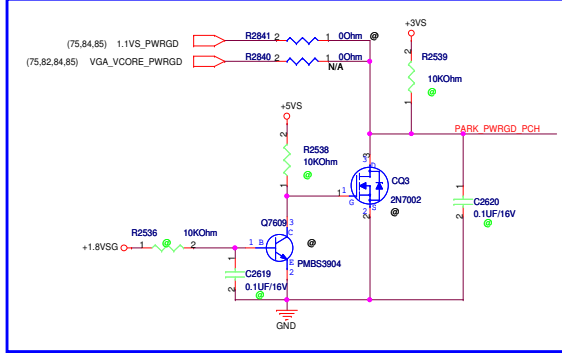
All GPIOs are reset to the default state by CP9h reset except GPIO24.
 GPIO 27: Enable VCCVRM_Low=disable. Default internal pull up.

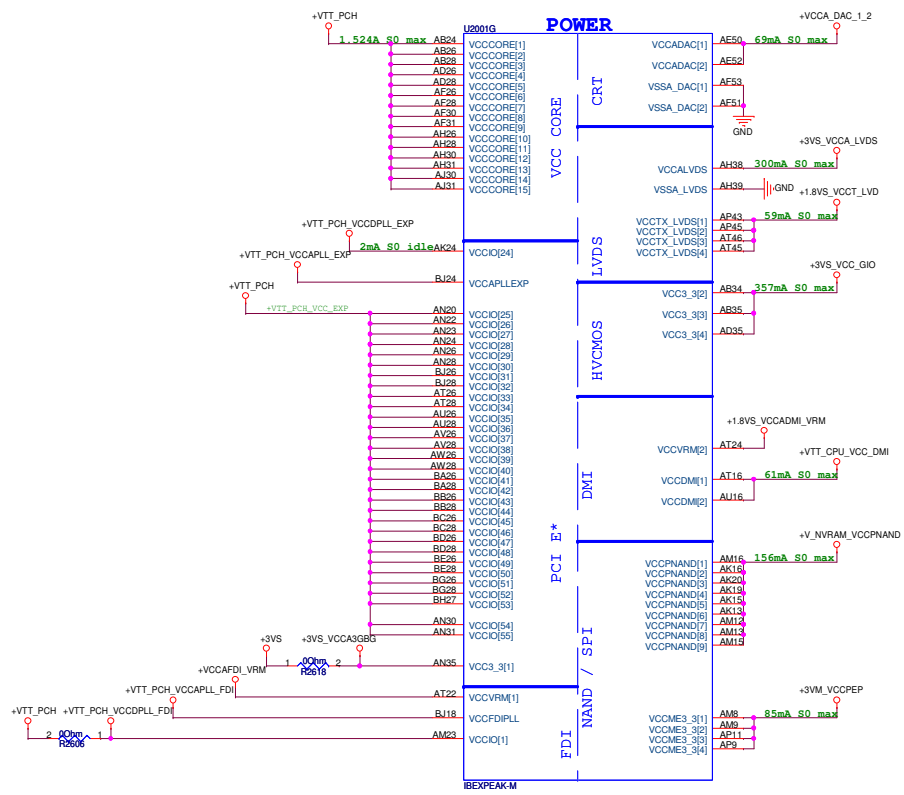


POWER按照提供的default值調節電壓

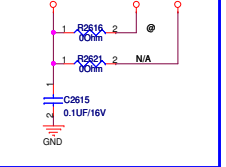
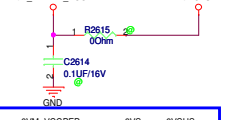
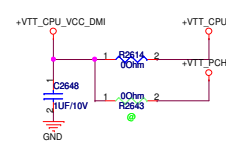
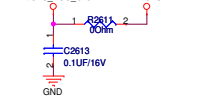
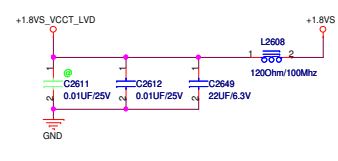
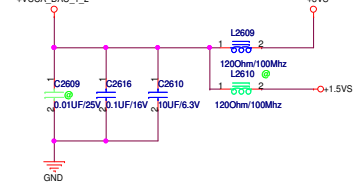
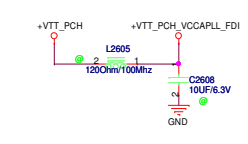
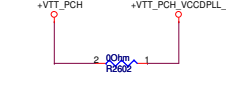
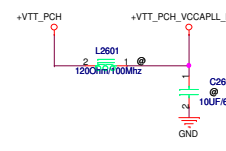
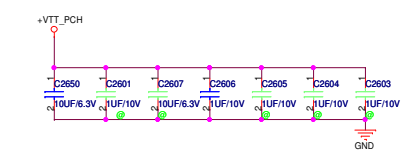
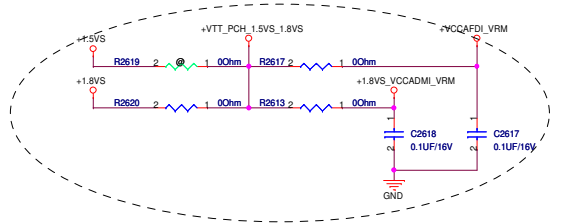


Update 1109, R2.0

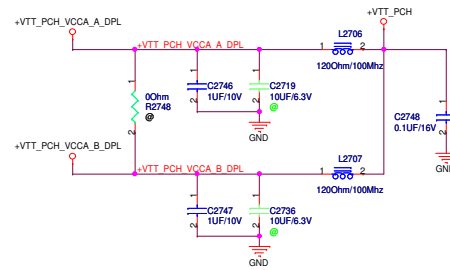
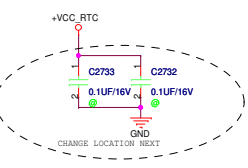
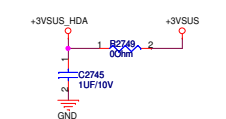
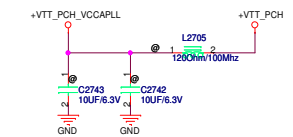
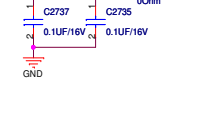
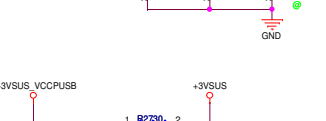
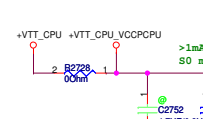
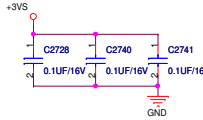
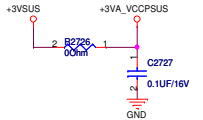
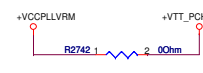
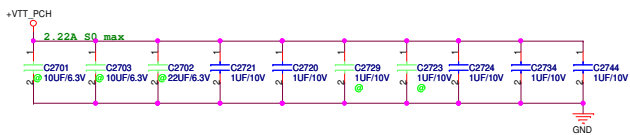
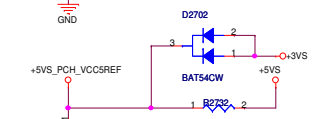
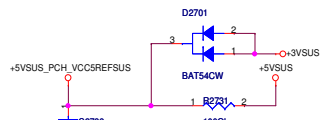
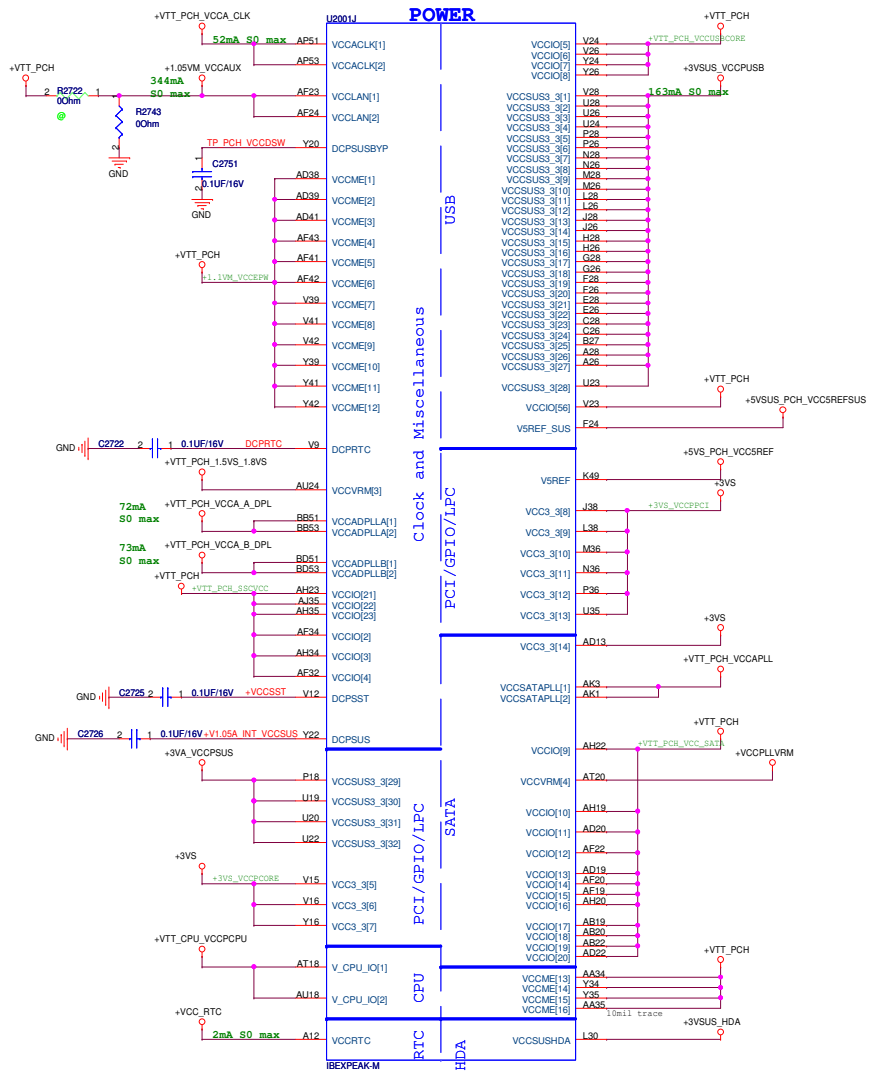


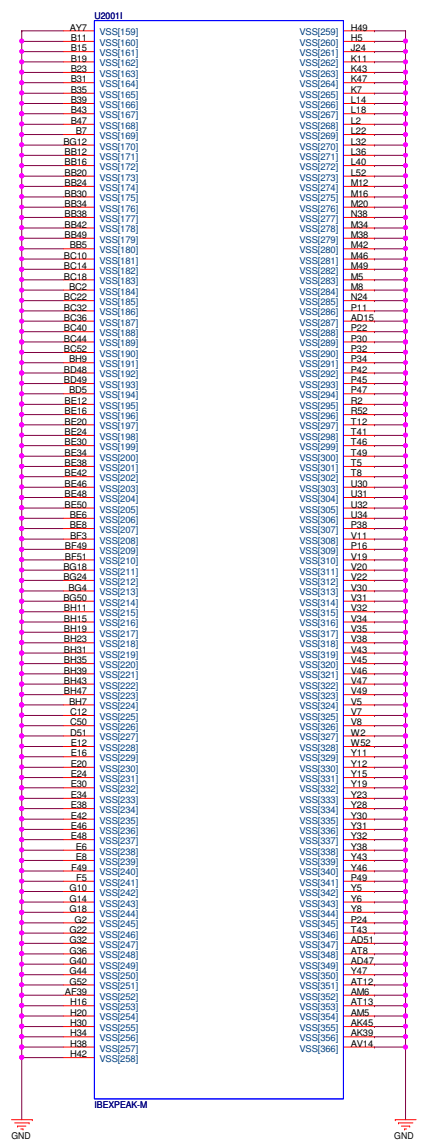
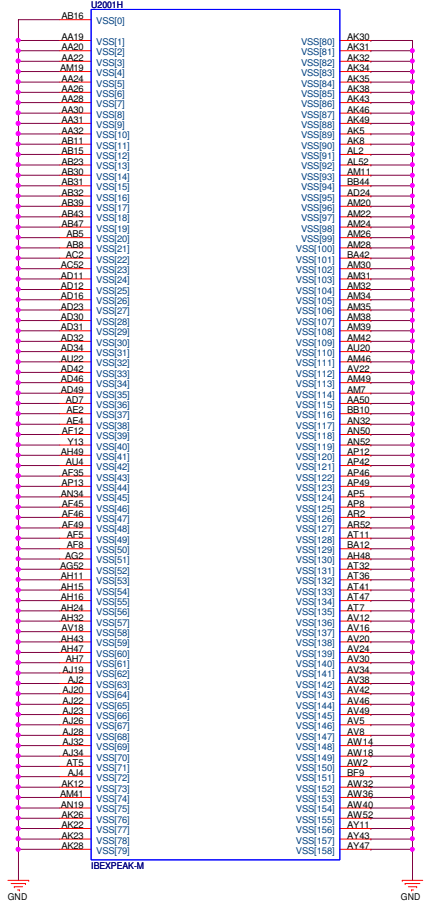


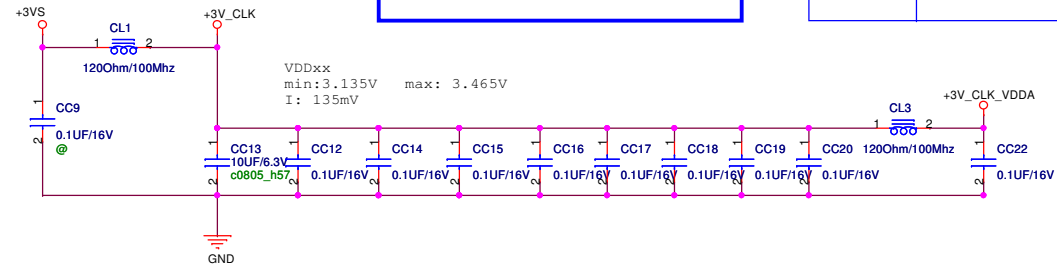
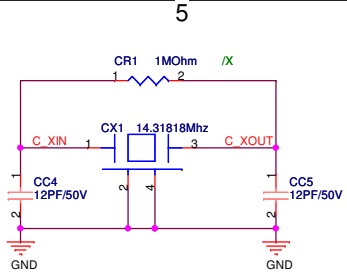
HDA_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)
 Low: 1.8V
 High: 1.5V



Update 1105 (R2.0)



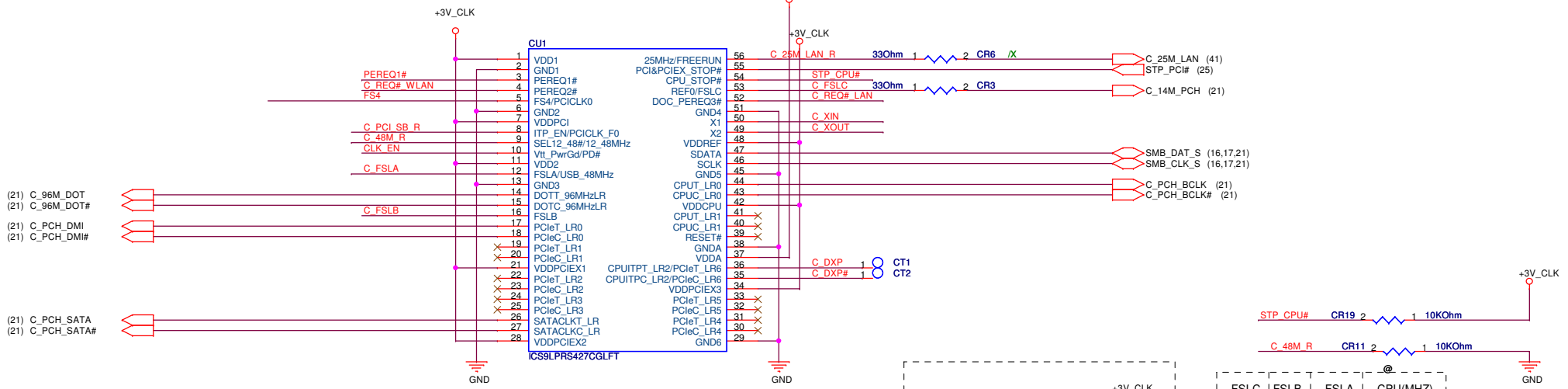




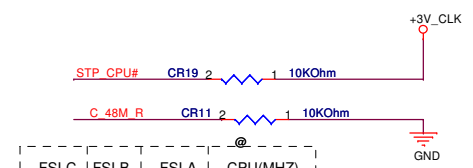
1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

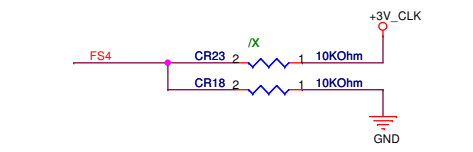
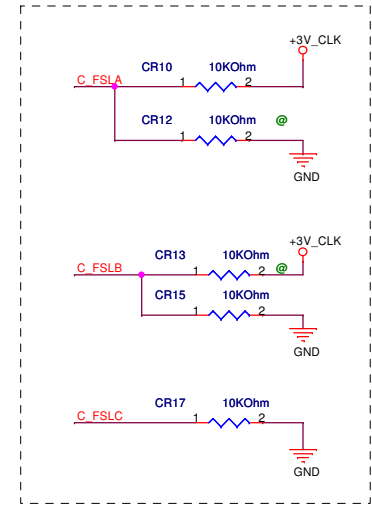
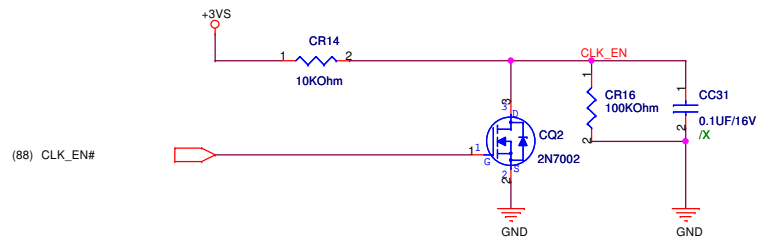
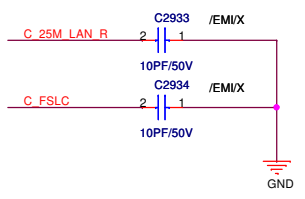
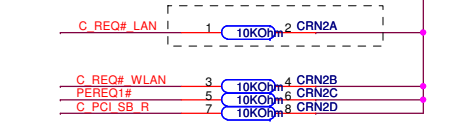
FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)



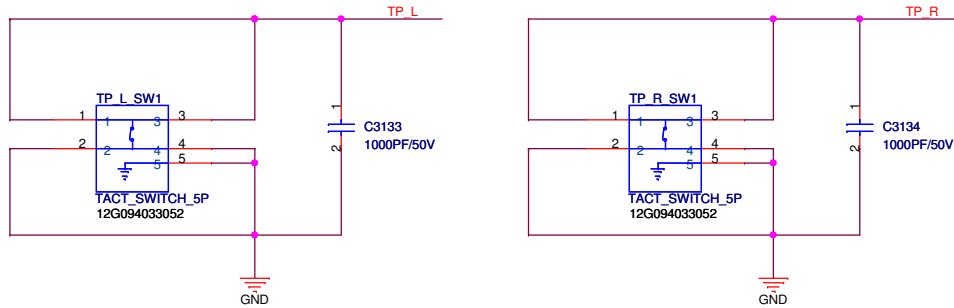
- (21) C_96M_DOT
- (21) C_96M_DOT#
- (21) C_PCH_DMI
- (21) C_PCH_DMI#
- (21) C_PCH_SATA
- (21) C_PCH_SATA#



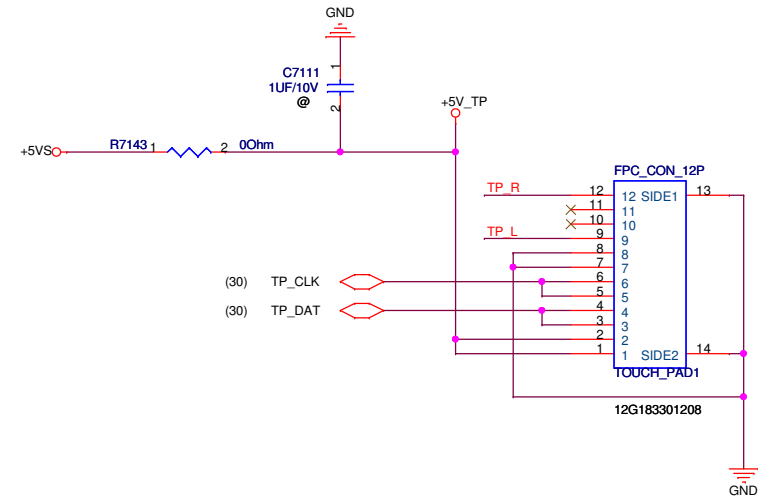
FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133
0	1	0	200



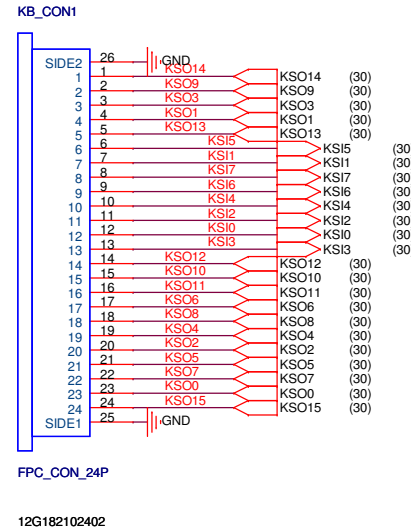
TouchPad



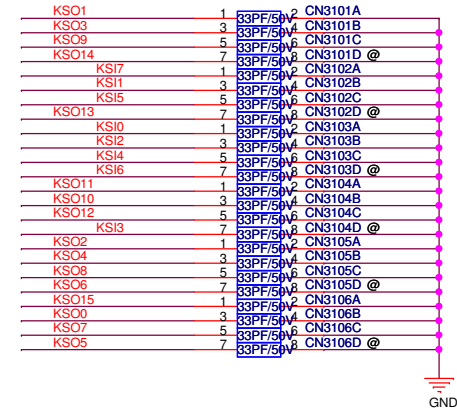
1.0 EMI test need mount C3133 and C3134



Keyboard Connector



EMI Request

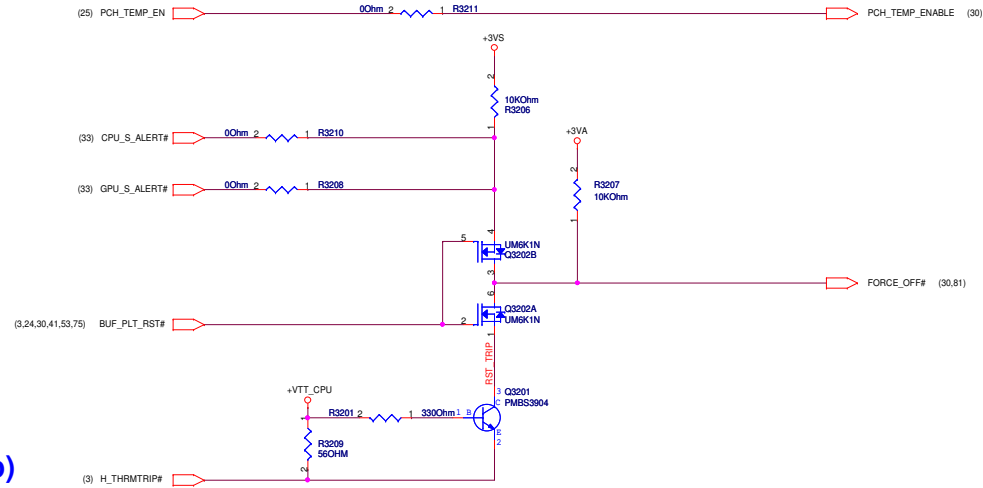


<Variant Name>

Thermal Policy

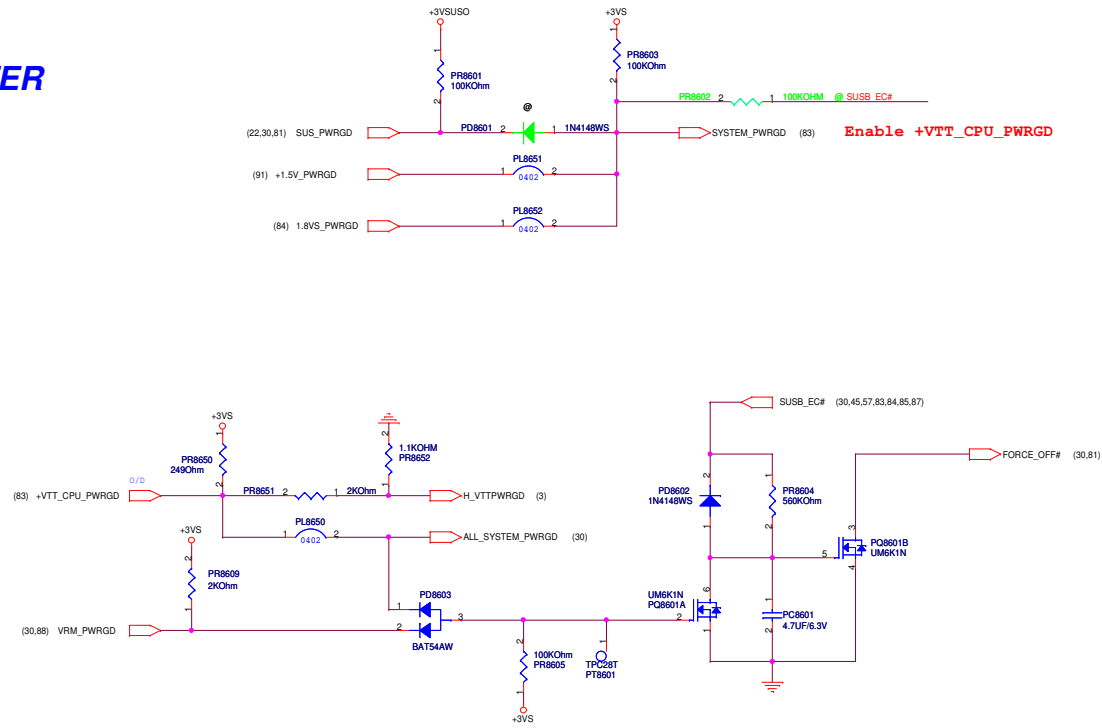
Input 1(sensor)

Input 2(thermtrip)

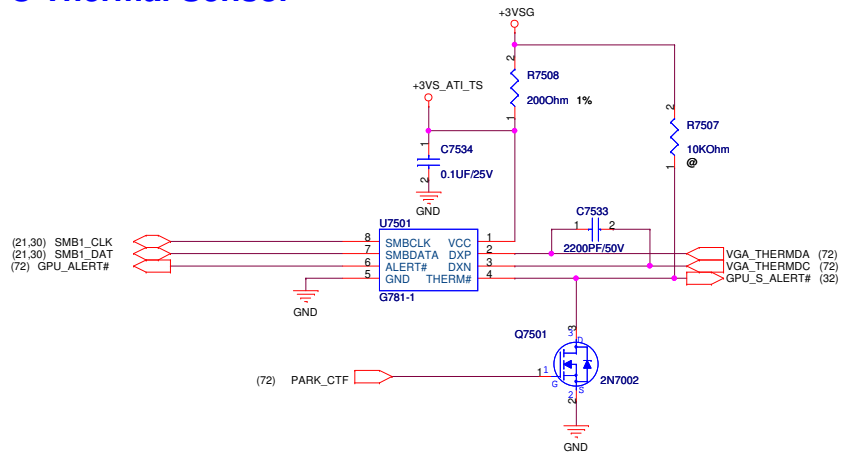


Output (shut down)

POWER GOOD DETECTER

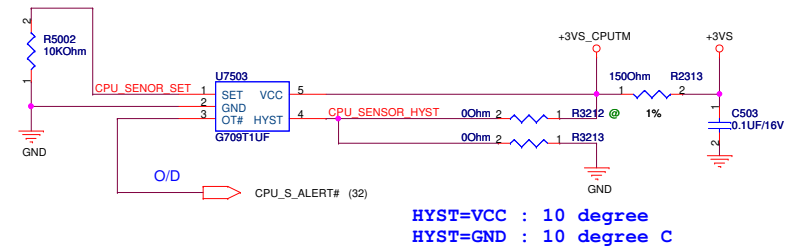


GPU Thermal Sensor



CPU Thermal Sensor

Update 1108 (R2.0)

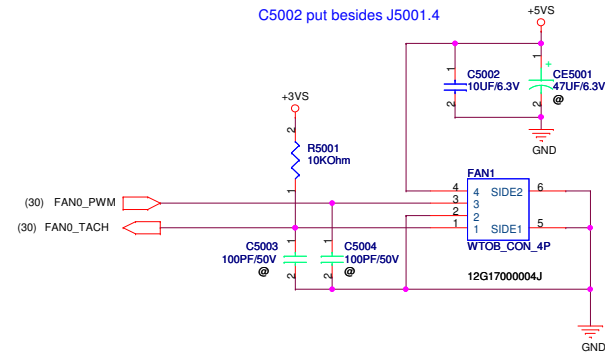


HYST=VCC : 10 degree
HYST=GND : 10 degree C

U7503 under CPU socket

PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.



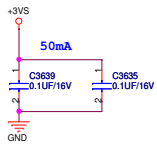
ASUS		Title : AR8131	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	LAN Design IP	108	
Date: Thursday, November 12, 2009		Sheet 33 of 96	

移至 USB BOARD

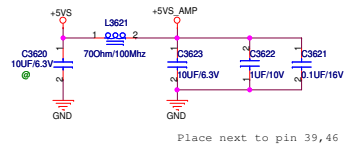
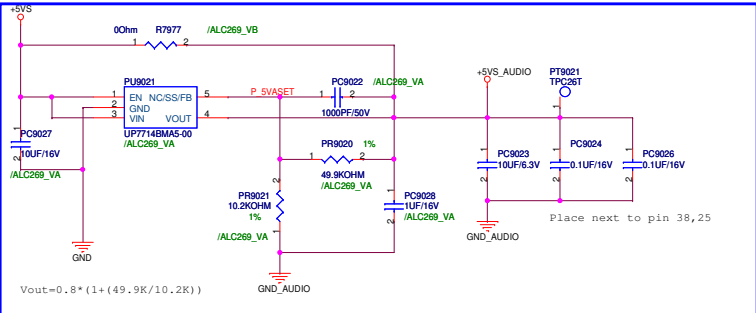
<Variant Name>

		Title : 8131
ASUSTeK COMPUTER INC		Engineer:
Size Custom	Project Name LAN Design IP	Rev 108
Date: Thursday, November 12, 2009		Sheet 34 of 96

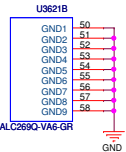
Update 11.08 (R2.0)



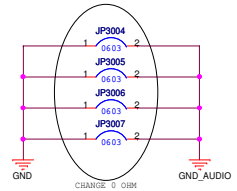
Close to pin1,9



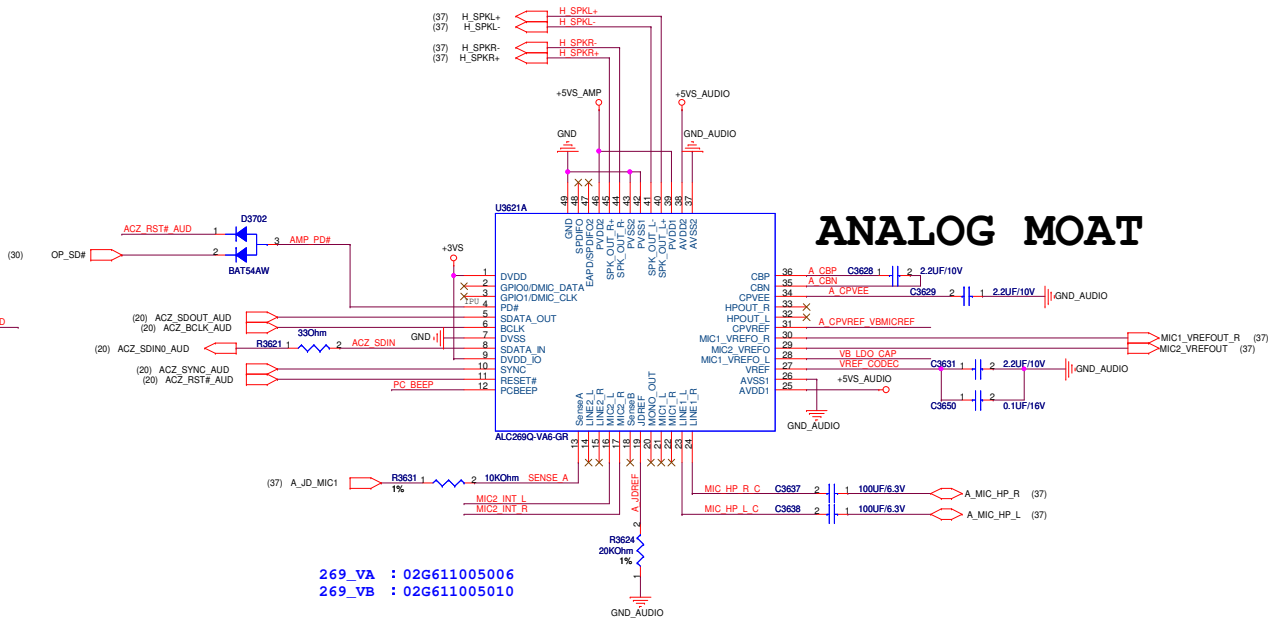
Place next to pin 39,46



For EMI

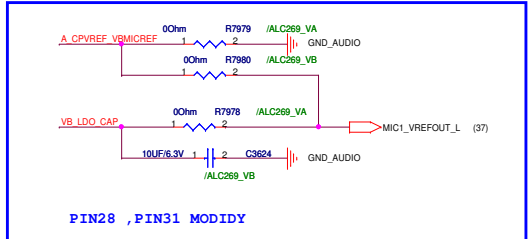


ANALOG MOAT

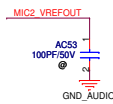


269_VA : 02G611005006
269_VB : 02G611005010

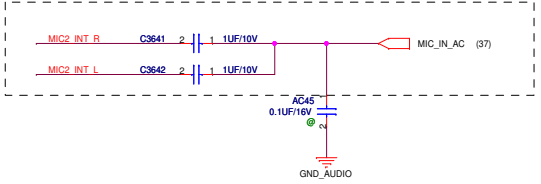
Update 11.08 (R2.0)



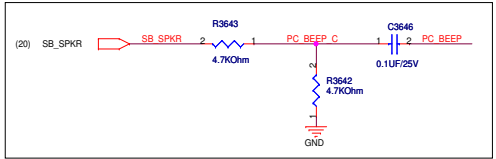
PIN28 , PIN31 MODIFY



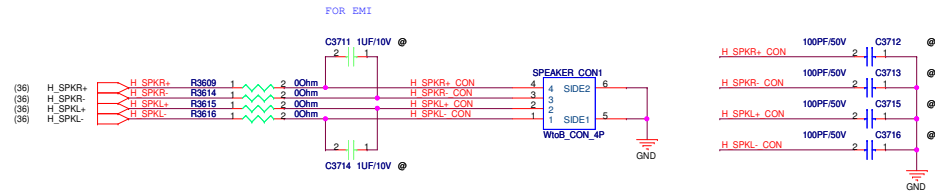
INTERNAL MIC



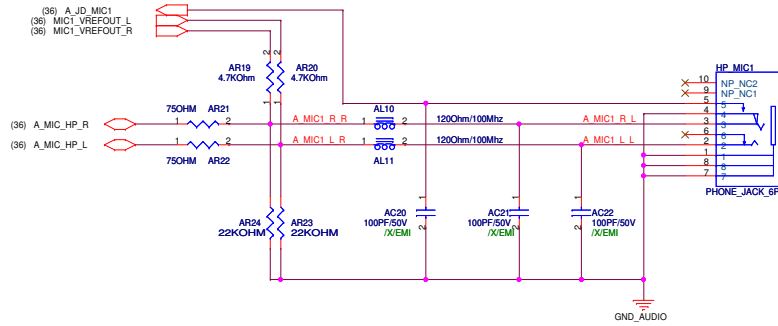
PC BEEP



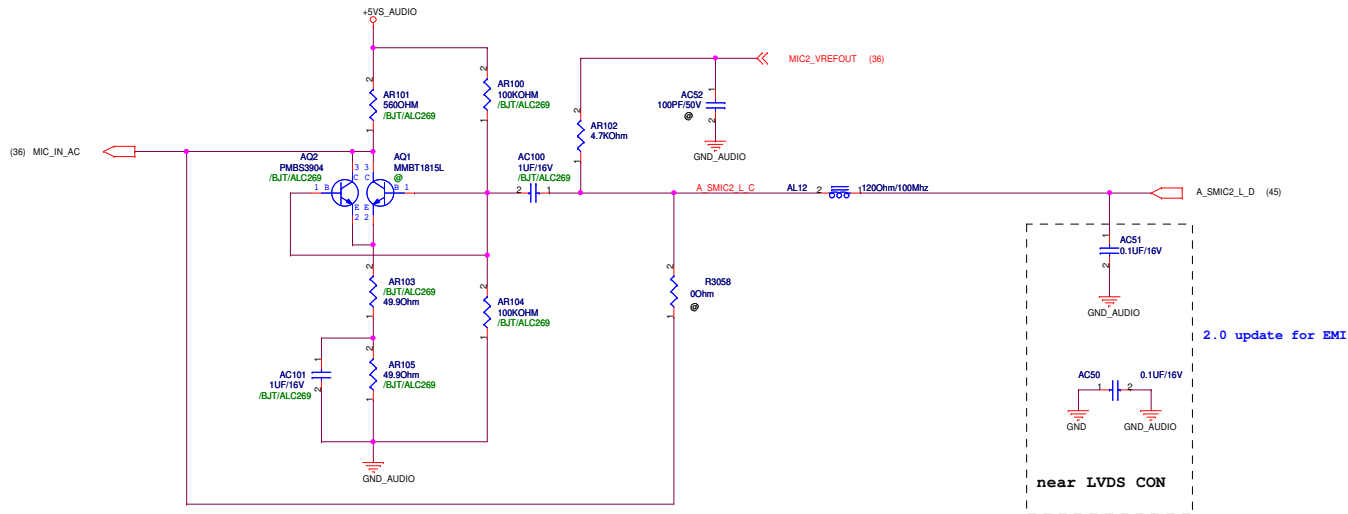
SPEAKER




HP and MIC

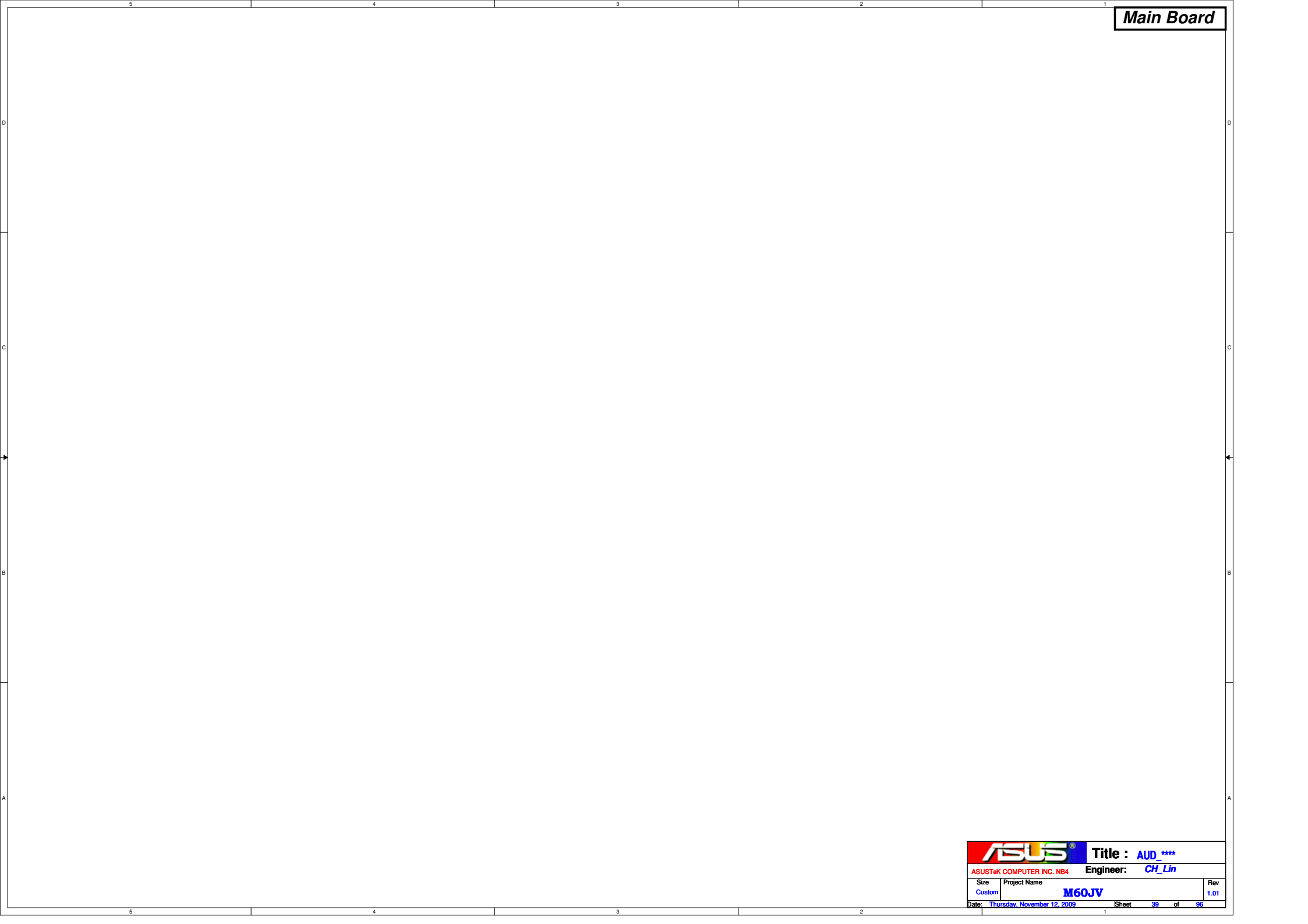



Internal MIC and AMP



Main Board

		Title : AUD_FM2010	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>CH_Lin</i>	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: <i>Thursday, November 12, 2009</i>		Sheet	38 of 95



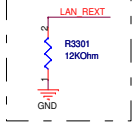
		Title : AUD ****	
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	39 of 96

Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.

<Variant Name>

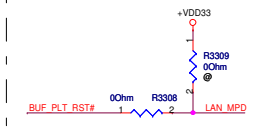
		Title : AU6433D53-GLF	
ASUSTek Computer Inc.		Engineer: Fehling_Wang	
Size	Project Name		Rev
A3	1008P Card Reader		1.0G
Date: Thursday, November 12, 2009		Sheet	40 of 96

Reference Resistance

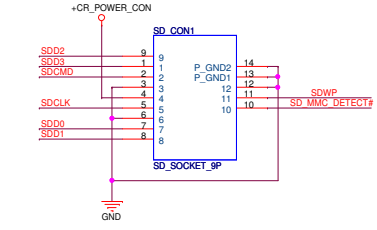
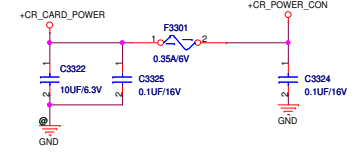
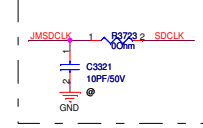
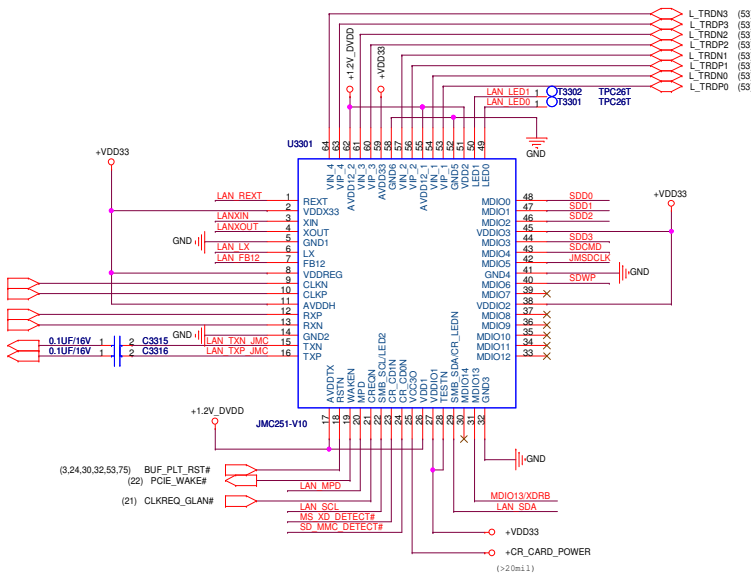


D3E Enable/Disable

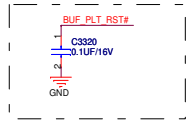
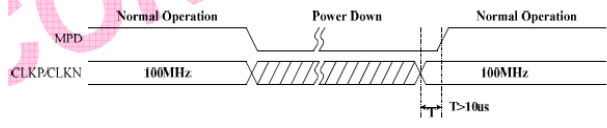
R3309	R3308	D3E
Unmount	Mount	Enable
Mount	Unmount	Disable



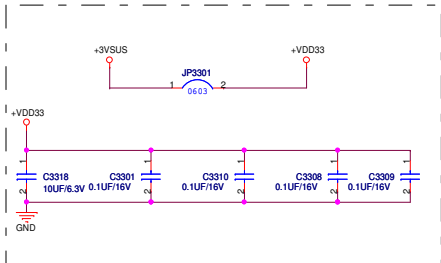
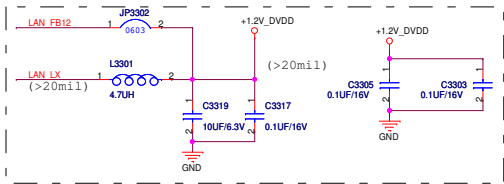
- (21) PCH_C_LAN_N
- (21) PCH_C_LAN_P
- (21) POE_TX_LAN_P
- (21) POE_TX_LAN_N
- (21) POE_RX_LAN_N
- (21) POE_RX_LAN_P



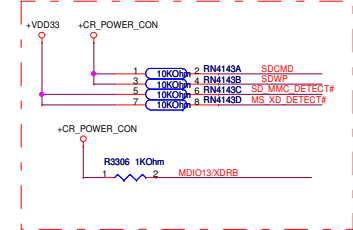
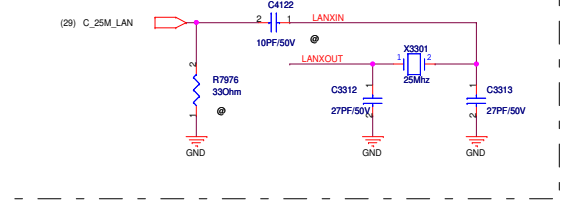
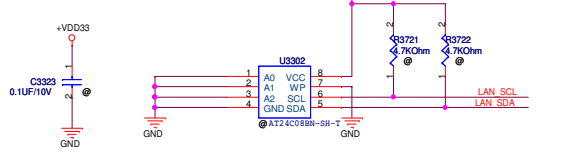
Card Insert: Pin.10 and Pin.12 are Shorted.
 Card not Insert: Pin.10 and Pin.12 are Opened.
 Write Protect: Pin.11 and Pin.12 are Opened.
 Write Enable: Pin.11 and Pin.12 are Shorted.



Switch Regulator



Serial EEPROM



5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : LAN RJ45	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name		Rev
Custom	M52J		1.3
Date: Thursday, November 12, 2009		Sheet	42 of 99

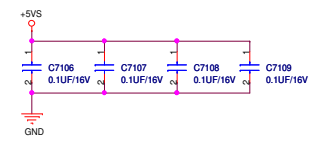
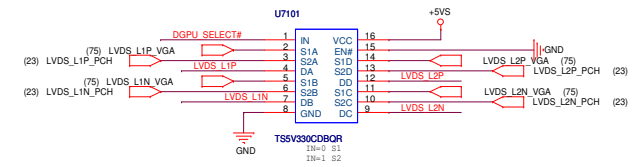
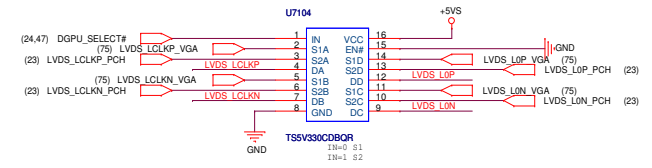
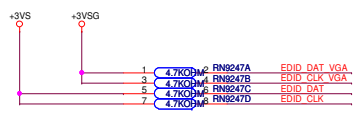
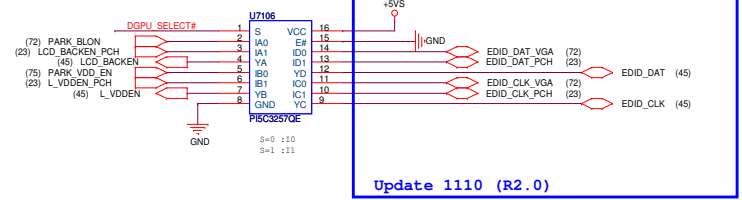
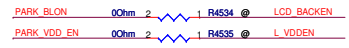
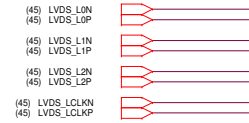
5

4

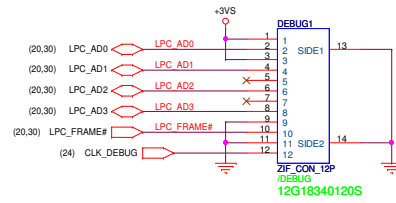
3

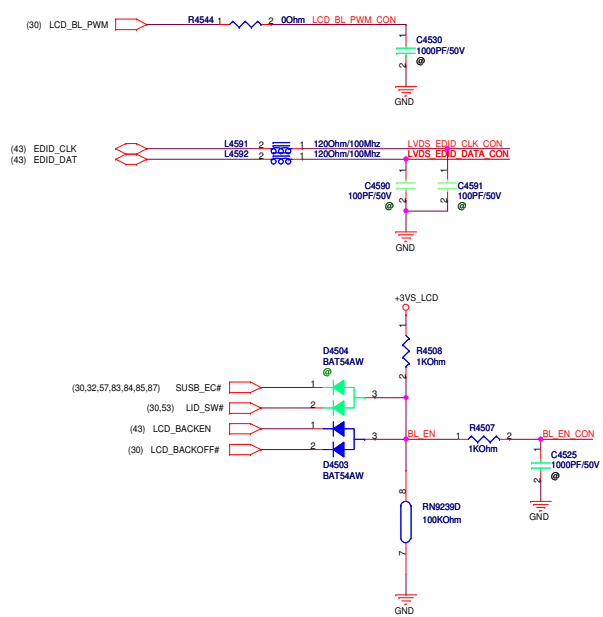
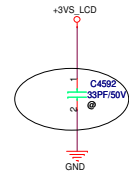
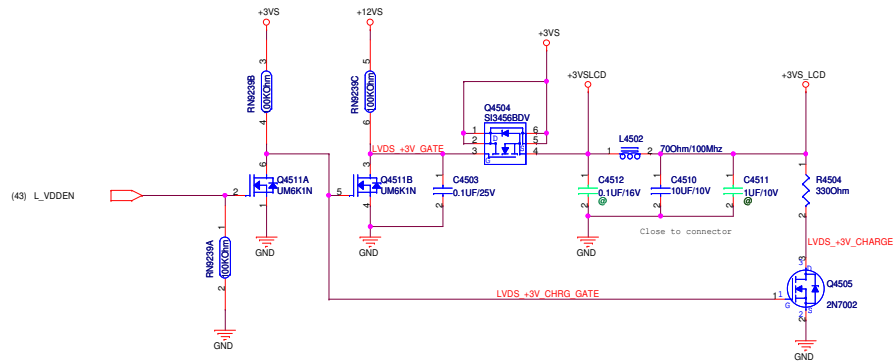
2

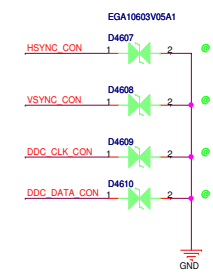
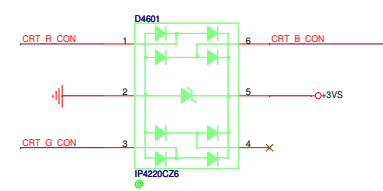
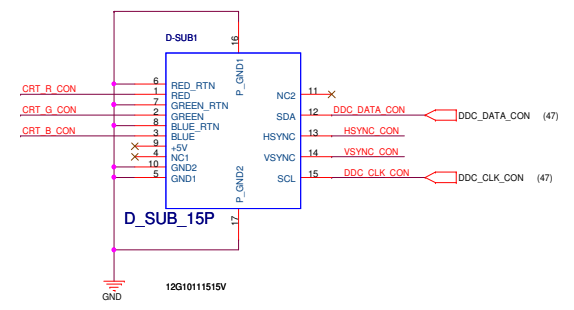
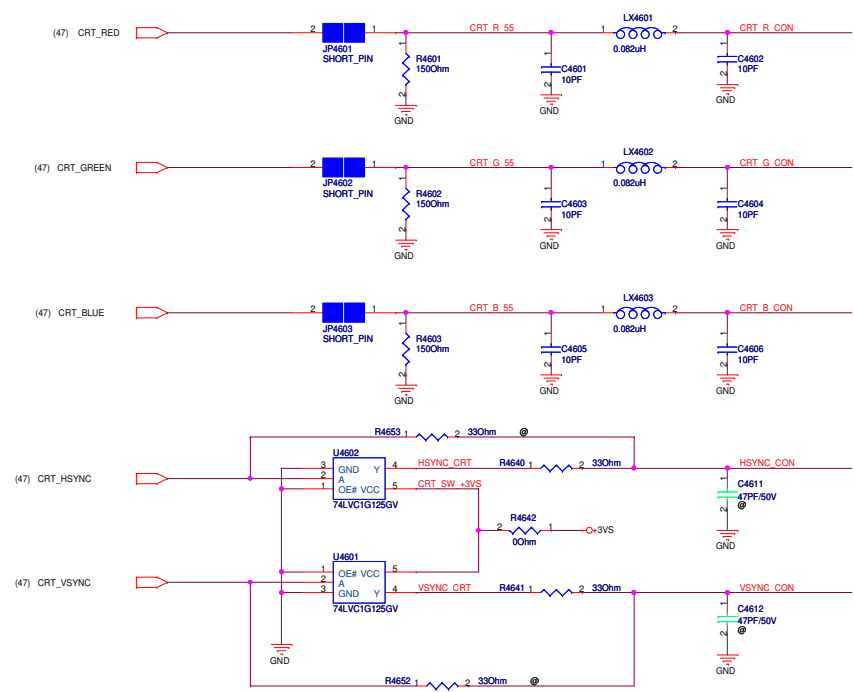
1

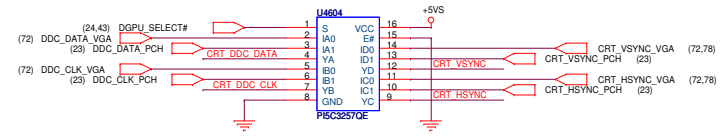
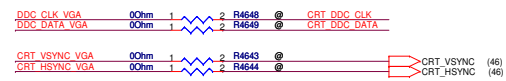
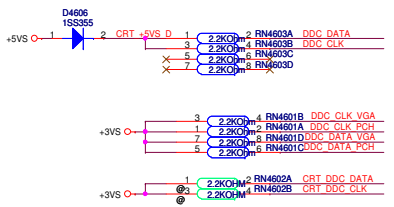
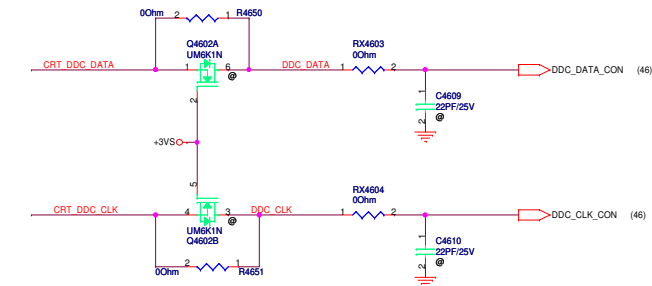


LPC Debug Port



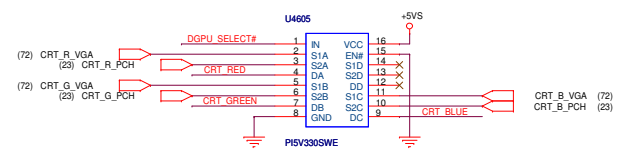
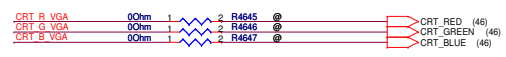






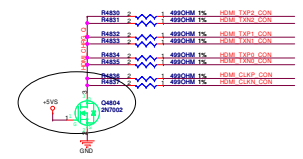
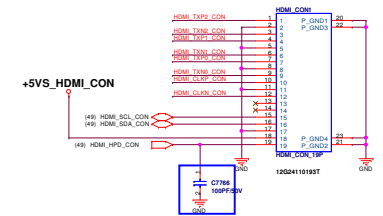
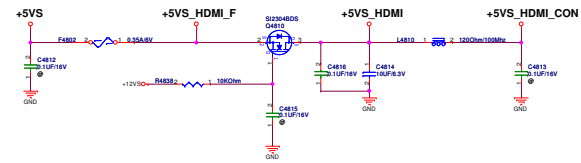
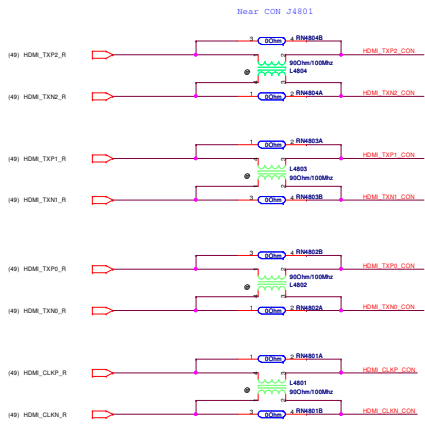
change pin define
A0 TO A1

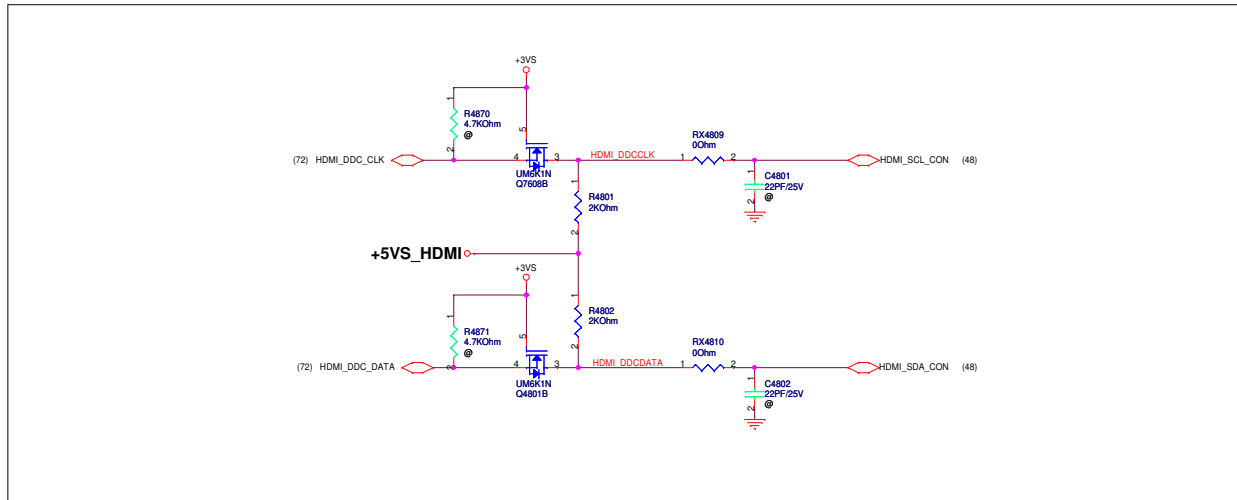
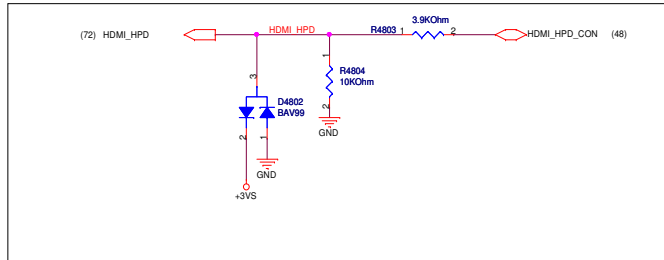
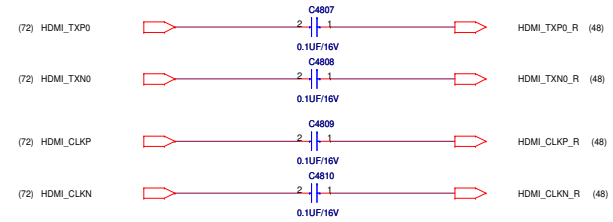
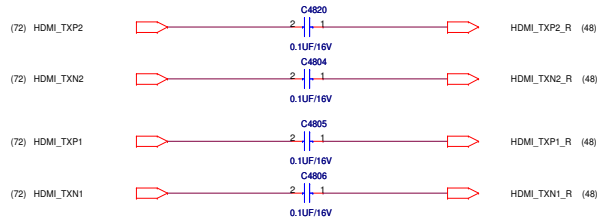
S=0 for VGA output
S=1 for PCH output




PI5V330SWE bandwidth=570MHz
PCH analog RAMDAC=350MHz.
(2048x1536 with 32bit color at 75Hz)

S=0 for VGA output
S=1 for PCH output

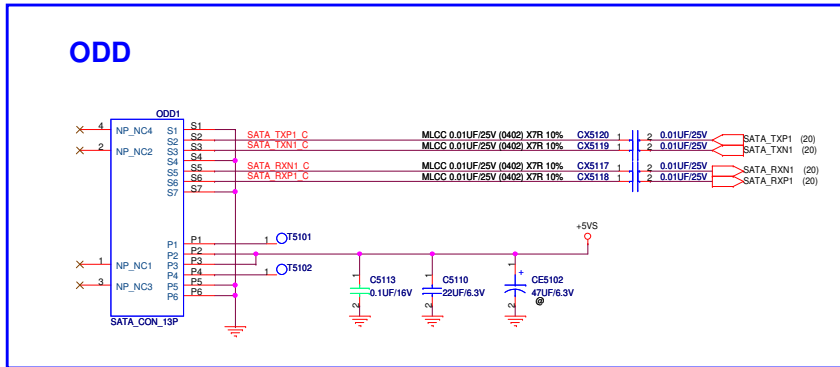




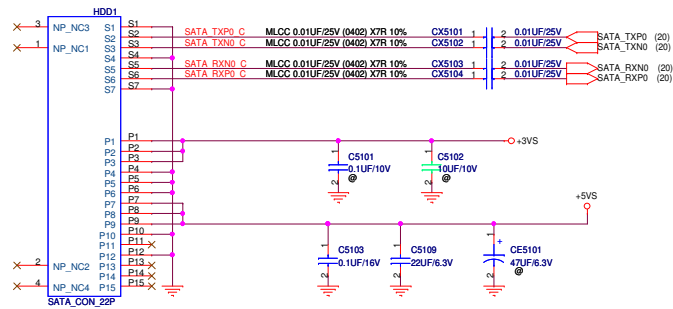
Main Board

		Title : FAN_Fan & Sensor
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin
Size	Project Name	Rev
C	M60JV	1.01
Date: Thursday, November 12, 2009		Sheet 50 of 95

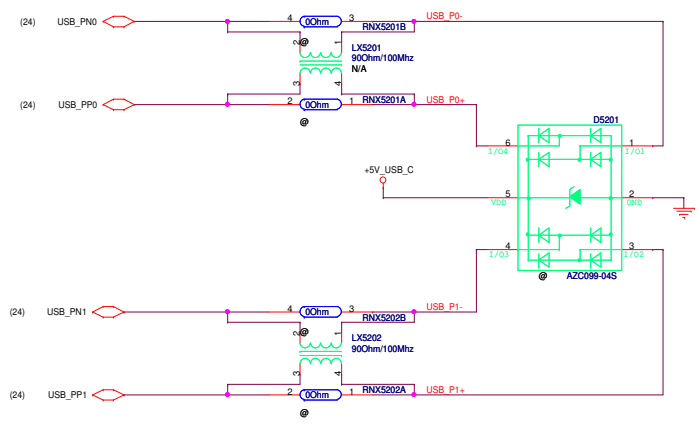
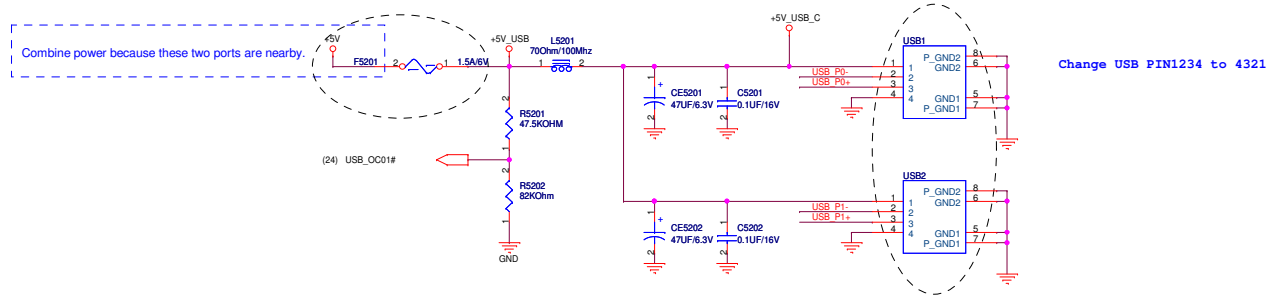
ODD

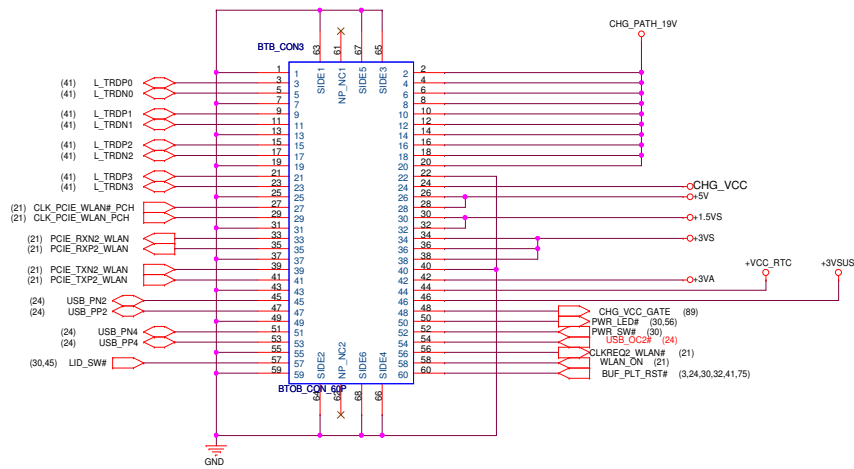


HDD (1st)



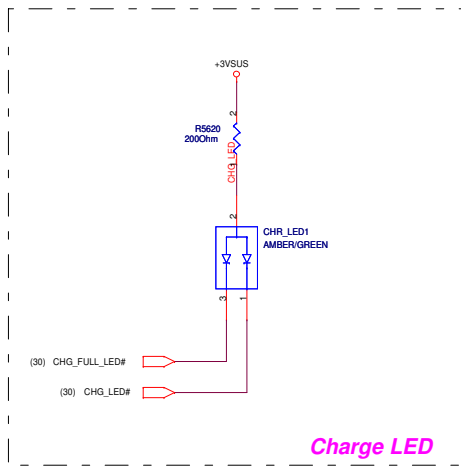
USB ports



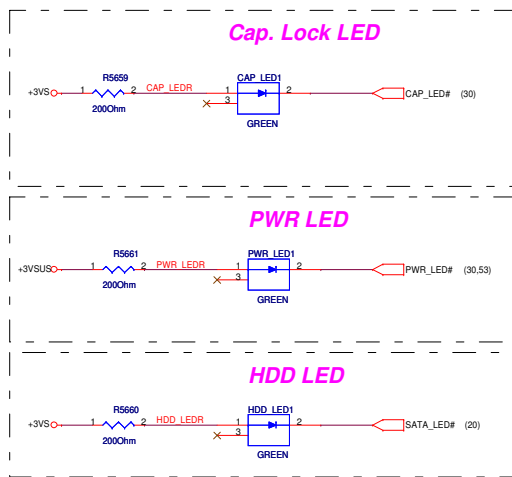


Main Board

		Title : S10 ****
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin
Size C	Project Name M60JV	Rev 1.01
Date: Thursday, November 12, 2009		Sheet 55 of 96



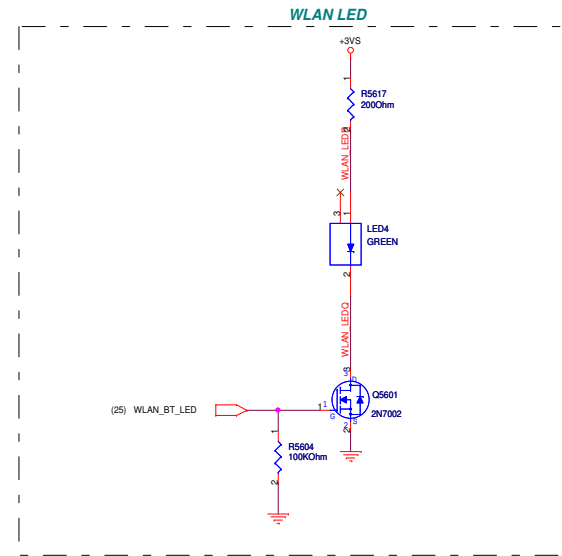
Charge LED



Cap. Lock LED

PWR LED

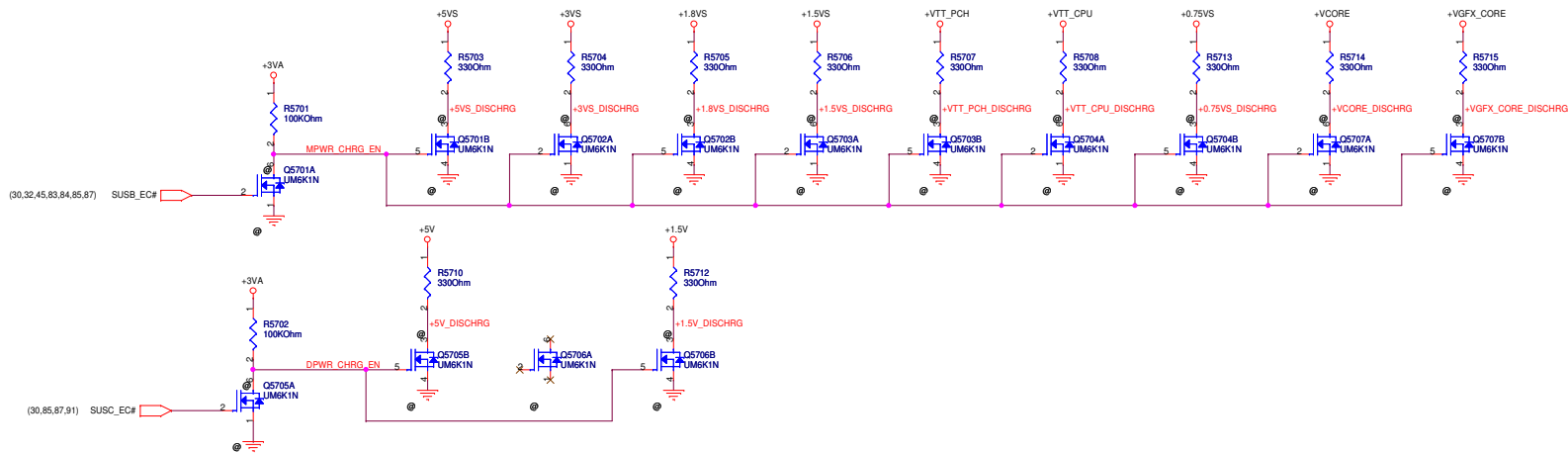
HDD LED




WLAN LED

Change LED part number

Remove +2.5Vs is for ATI GFX

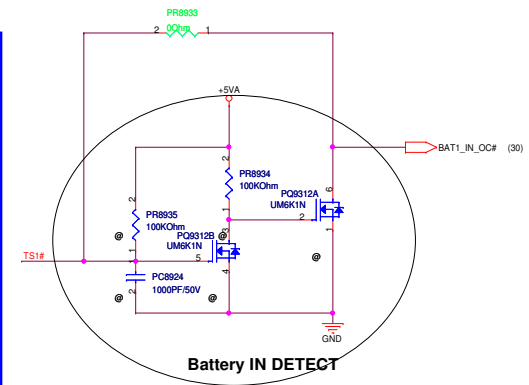
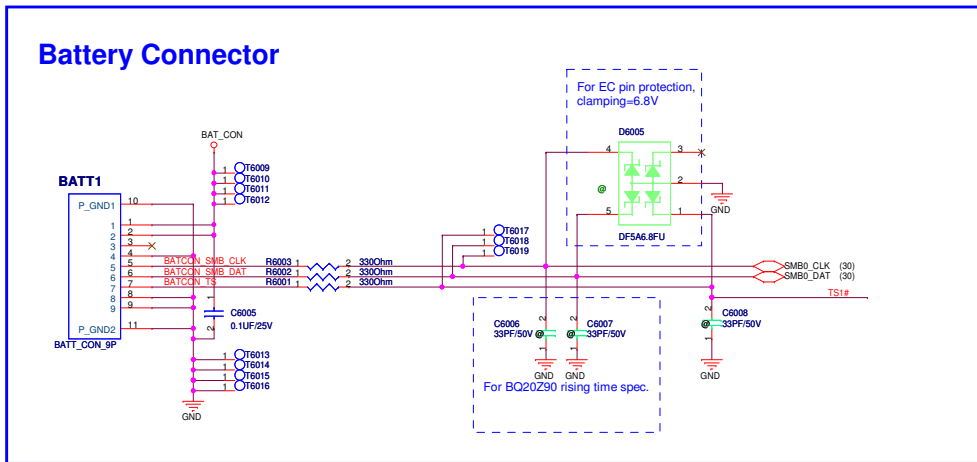


Main Board

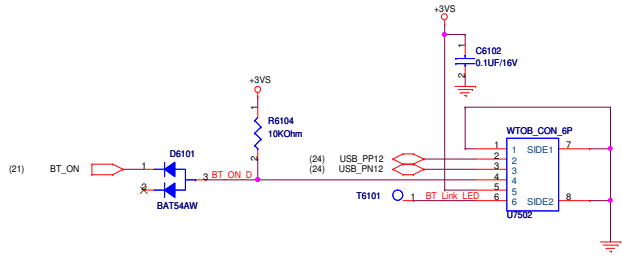
		Title : PCI ****	
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	56 of 95

Main Board


		Title : DJ ****	
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	59 of 95




BLUETOOTH



Main Board

		Title : TPM_****	
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	62 of 95

Main Board

		Title : FP_FP Conn	
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	63 of 95

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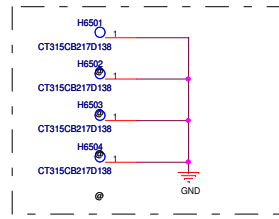
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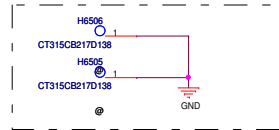
		Title : TUN_TV Tuner	
ASUSTeK COMPUTER INC. NB4		Engineer: CH_Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	64 of 95

Main Board

For CPU



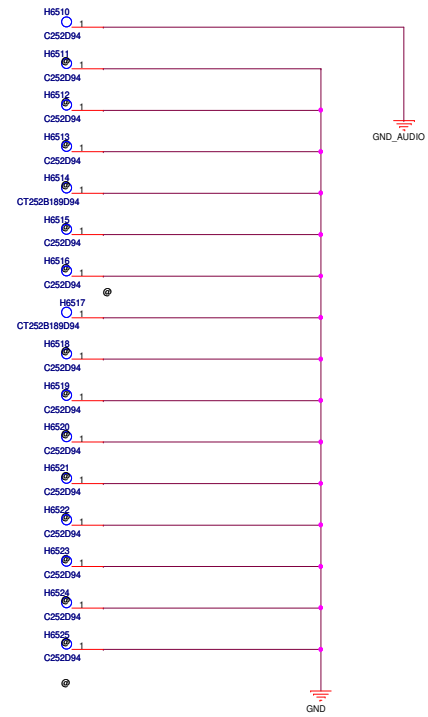
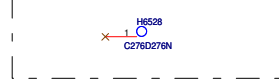
For GPU

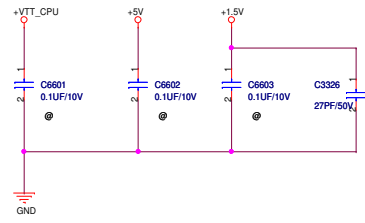


For 橢圓定位孔



HHD 呼吸孔





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		Title :PCH_XDP, ONFI	
ASUSTeK COMPUTER INC. NB4		Engineer Lin	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	67 of 96

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		Title : OTH_LCM	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>CH_Lin</i>	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: <i>Thursday, November 12, 2009</i>		Sheet	68 of 96

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		Title :OTH_GAME-LED*****	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>CH_Lin</i>	
Size	Project Name	Rev	
C	M60JV	1.01	
Date: <i>Thursday, November 12, 2009</i>		Sheet	69 of 96

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		Title :	
ASUSTeK COMPUTER INC. NB4		Engineer:	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	70 of 96

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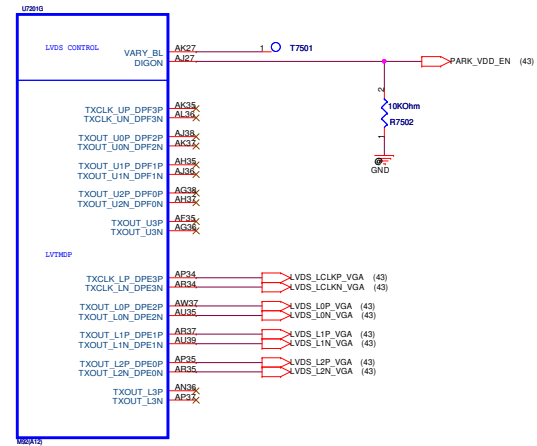
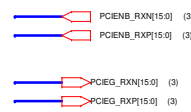
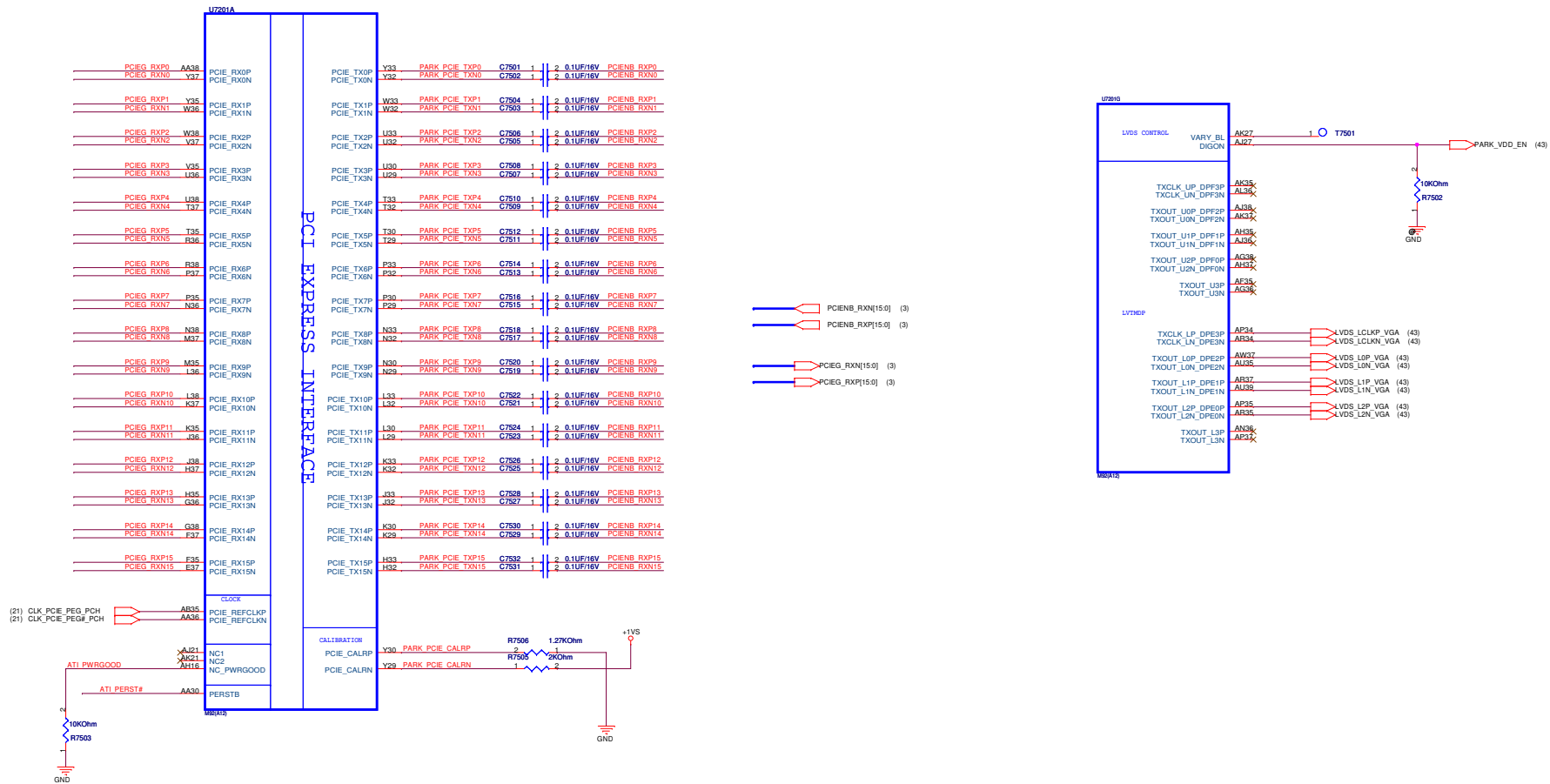
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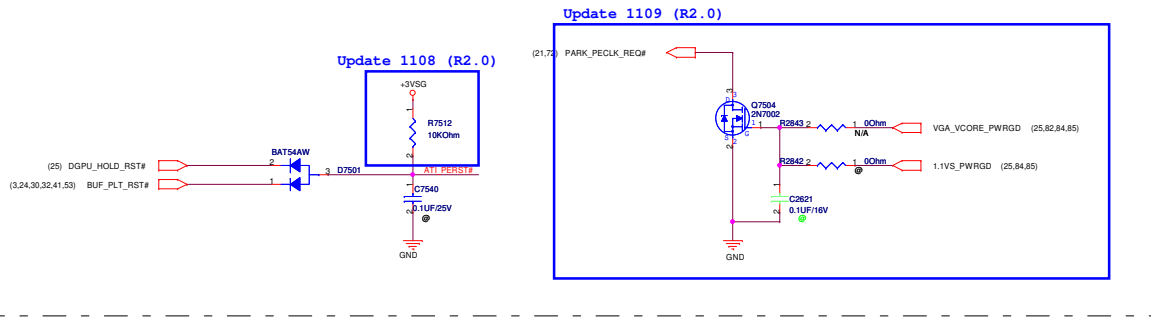
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		Title :	
ASUSTEK COMPUTER INC. NB4		Engineer:	
Size	Project Name	Rev	
C	M60JV	1.01	
Date:	Thursday, November 12, 2009	Sheet	71 of 96

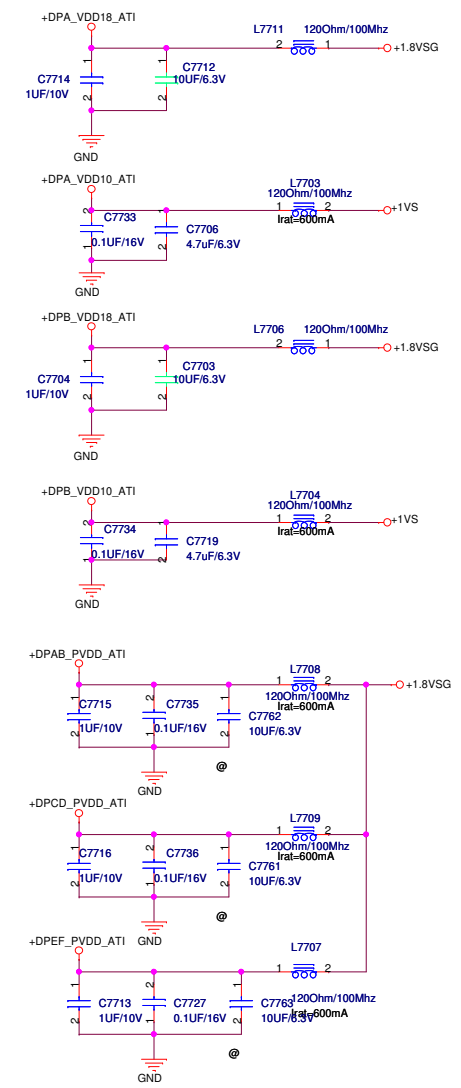
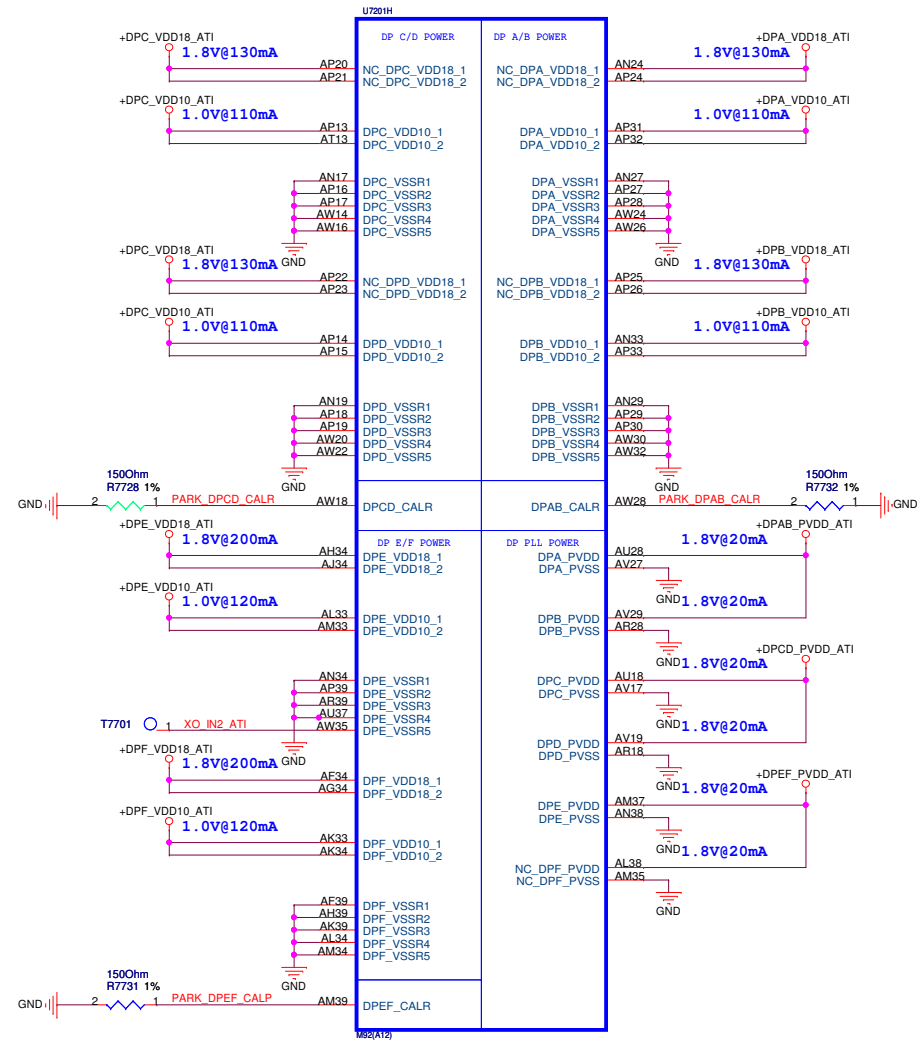
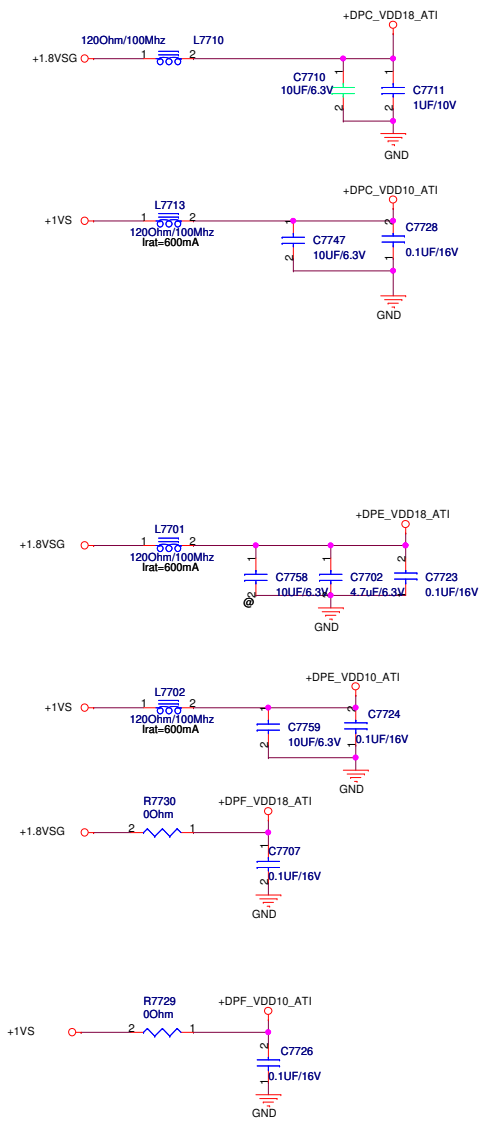
PCI EXPRESS

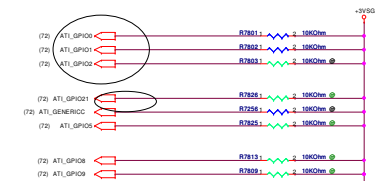


For switchable graphic

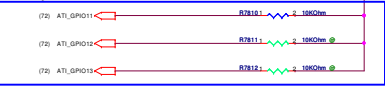


DPE: LVDS
 DPB: HDMI
 DAC1: CRT

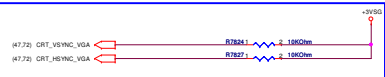




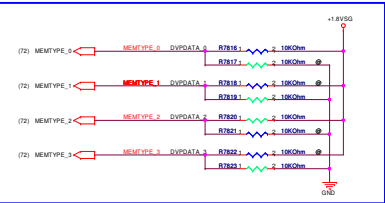
Memory Size:



Audio function:



Memory Type:



Dual Rank DDR3 1GB need AMD check pull low or high for following DDR3 VRAM
 03G15163820 DDR3 64M*16-1.2 FBGA-96 SAMSUNG/K4W1G1646E-HC12
 03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G638FR-12C

Memory ID Board Straps

Vendor	DVFDATA3.2.1.0	ID	DDR Memory Type	Channel Size
Inflieon (Gimonda)	0000	0	32M*16 (D54M)	2-AB channel
	0001	1	32M*16 (D13M)	2-AB channel
	0010	2	40M*16 (D13M)	2-AB channel
Samsung	0100	0	40M*16 (D13M)	2-AB channel
	0110	1	40M*16 (D13M)	2-AB channel
	0111	2	40M*16 (D13M)	2-AB channel
Hynix	1000	0	32M*16 (D13M)	2-AB channel
	1001	0	32M*16 (D13M)	2-AB channel
	1010	10	40M*16 (D13M)	2-AB channel
Eplida	1100	11	720	2-AB channel
	1101	12	720	2-AB channel
	1110	14	64M*16 (H)	2-AB channel

Memory ID Board Straps

Vendor	DVFDATA3.2.1.0	ID	DDR Memory Type	Channel Size
Gimonda	0000	0	32M*16 (D54M)	B channel
	0001	1	32M*16 (D13M)	B channel
	0010	2	40M*16 (D13M)	B channel
Samsung	0100	0	40M*16 (D13M)	B channel
	0110	1	40M*16 (D13M)	B channel
	0111	2	40M*16 (D13M)	B channel
Hynix	1000	0	32M*16 (D13M)	B channel
	1001	0	32M*16 (D13M)	B channel
	1010	10	40M*16 (D13M)	B channel
Eplida	1100	11	720	B channel
	1101	12	720	B channel
	1110	14	64M*16 (H)	B channel

03G42 only support B channel

TX_PWRB_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.) 1: Full Tx output swing.	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements) Otherwise: 1: Must be pulled to 3.3 V at reset using ~3-K (5%) resistor
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled. Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.) 1: Tx de-emphasis enabled.	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements) Otherwise: 1: Must be pulled to 3.3 V at reset using ~3-K (5%) resistor (e.g. MCM and add-in boards)
BIF_GEN2_EN_A	GPIO_2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on. Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CDB (compliance base board).	0 (Internal pull-down)	0 5.0 GT/s capability will be controlled by software.
VGA_DIS	GPIO_9_ROMSI	VGA Disable determines whether or not the card will be recognized as the system's VOA controller (via the SUBCLASS field in the PCI configuration space): 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VOA controller	0 (Internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO_13 GPIO_12 GPIO_11	(a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. See "ROM Configurations" on page 3-33. (b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. See "Primary Memory Aperture size requested at PCI Configuration" on page 3-33	0 (Internal pull-down)	Design dependent. See description for more information.

BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device Note that when an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low)	0 (Internal pull-down)	Design dependent. See description for more information.
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00 - No audio function. 01 - Audio for DisplayPort only. 10 - Audio for DisplayPort and HDMI if dongle is detected. 11 - Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	0 (Internal pull-down)	Design dependent. See description for more information.
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it should try to sense whether or not a VIP device is connected on the VIP Host interface. 0 - Driver would ignore the value sampled on VHAD_0 during reset 1 - Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (0 = 0 indicates yes, 1 indicates no). According to the VIP 1.1 standard, VHAD_0 is tied high, and VIP slave devices are required to drive this signal low during reset. This scheme allows for a VIP device to be connected to the graphics adapter via a daughter card. Note: If the strap is needed, it must be placed between the ball and the VSYNC output buffer. This output buffer prevents monitors from affecting the value at reset.	0 (Internal pull-down)	Design dependent. See description for more information.

RESERVED CONFIGURATION STRAPS
 Allow for pullup pads for these straps and if these GPIOs are used, they must not conflict during reset

RESERVED	HSYNC	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (Internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
----------	-------	--	---------------------------	---

Pull up pads are not required for these straps but if these GPIOs are used, they must not conflict during reset.

RESERVED	GPIO_8_ROMSO GPIO_21_BB_EN	Internal use only. THESE PADS HAVE INTERNAL PULL-DOWNS AND MUST BE 0 V AT RESET. These pads may be left unconnected, however, if they are connected to additional logic on the board, the logic must not allow these signals to be driven or pulled to any value except GND at reset.	0 (Internal pull-down)	No PAD required. Ensure that no logic conflicts with these signals during Reset.
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64 MB	010
32 MB	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

POWERPLAY Interface

Pin Name	Type	P/D/P/U	Description
GPIO_5_AC_BATT	I/O	PC-reset	GPIO_5_AC_BATT is an optional input which allows the system to request a fast power reduction by setting GPIO_5_AC_BATT to low (0V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods only in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCTL_0 GPIO_16_SSN GPIO_20_PWRCTL_1	I/O 3.3 V VDDR3	PC-reset	Voltage control signals for the core VDDC and VDDCI. At Reset, these signals will be inputs with weak internal pull-down resistors. VBIOS can define all voltage control signals to be either 3.3V or open drain outputs (all signals must be the same type). The output state (high/low) of these signals is programmable for each PlayPlay state. (Optional) Voltage control signal for memory voltage regulator. Note that this signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_21_BB_EN	I/O		

CONFIGURATION STRAPS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	Pin	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0 - DO NOT INSTALL RESISTOR 1 - INSTALL IN RESISTOR X - DESIGN DEPENDENT N - NOT APPLICABLE
TX_PWRB_ENB	GPIO0	PCI FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS ENABLED	X
RESERVED	GPIO8	RESERVED	0
RESERVED	GPIO9	RESERVED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMDFQ2:0	GPIO[3:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	HSYNC	RESERVED	0
RSVD	GENERICC	RESERVED	0
AUD[1]	AUD[1]	SEE DATABOOK FOR DETAIL	X
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	X

AMD RESERVED CONFIGURATION STRAPS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC	GENERICC	GPIO2	GPIO1
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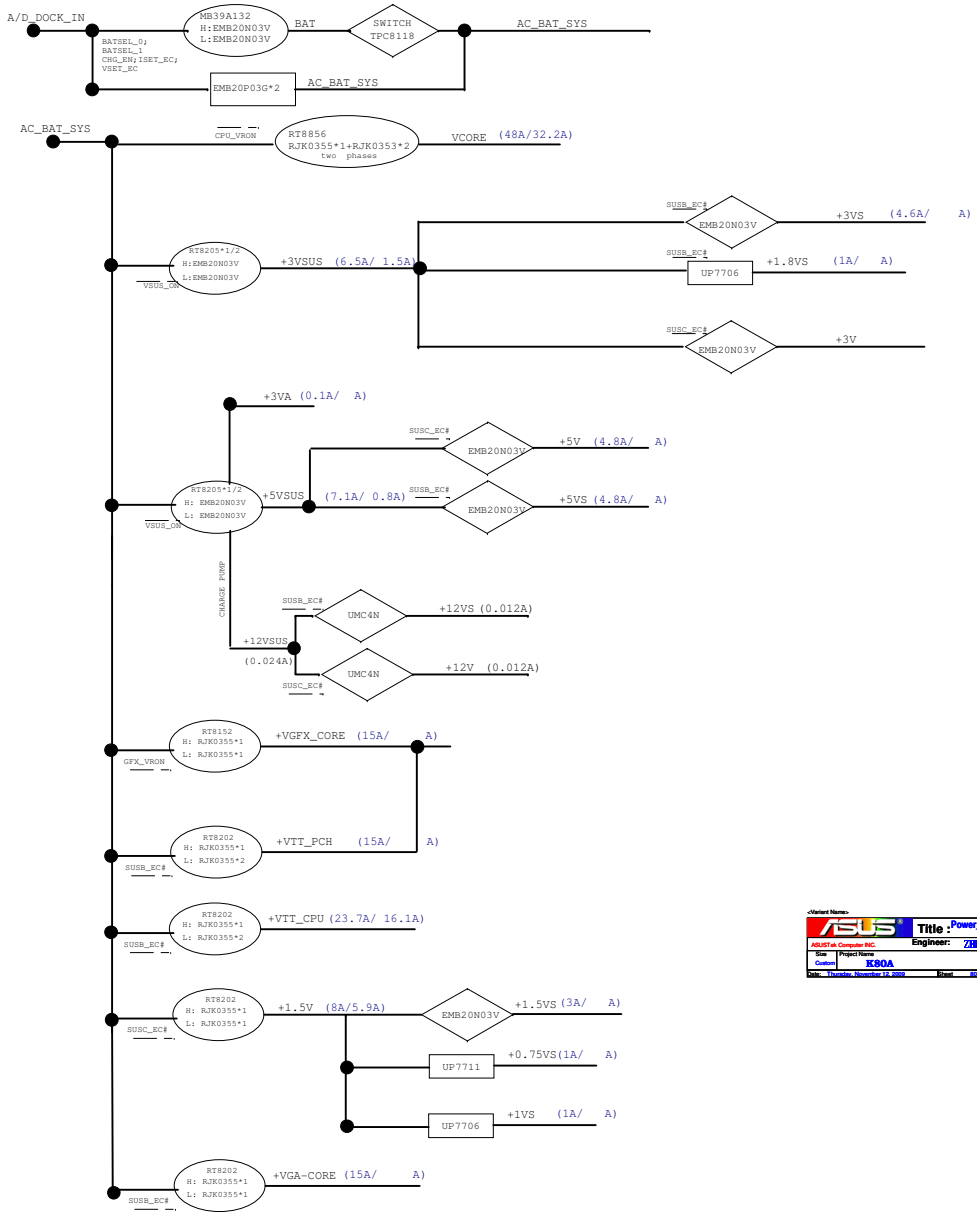
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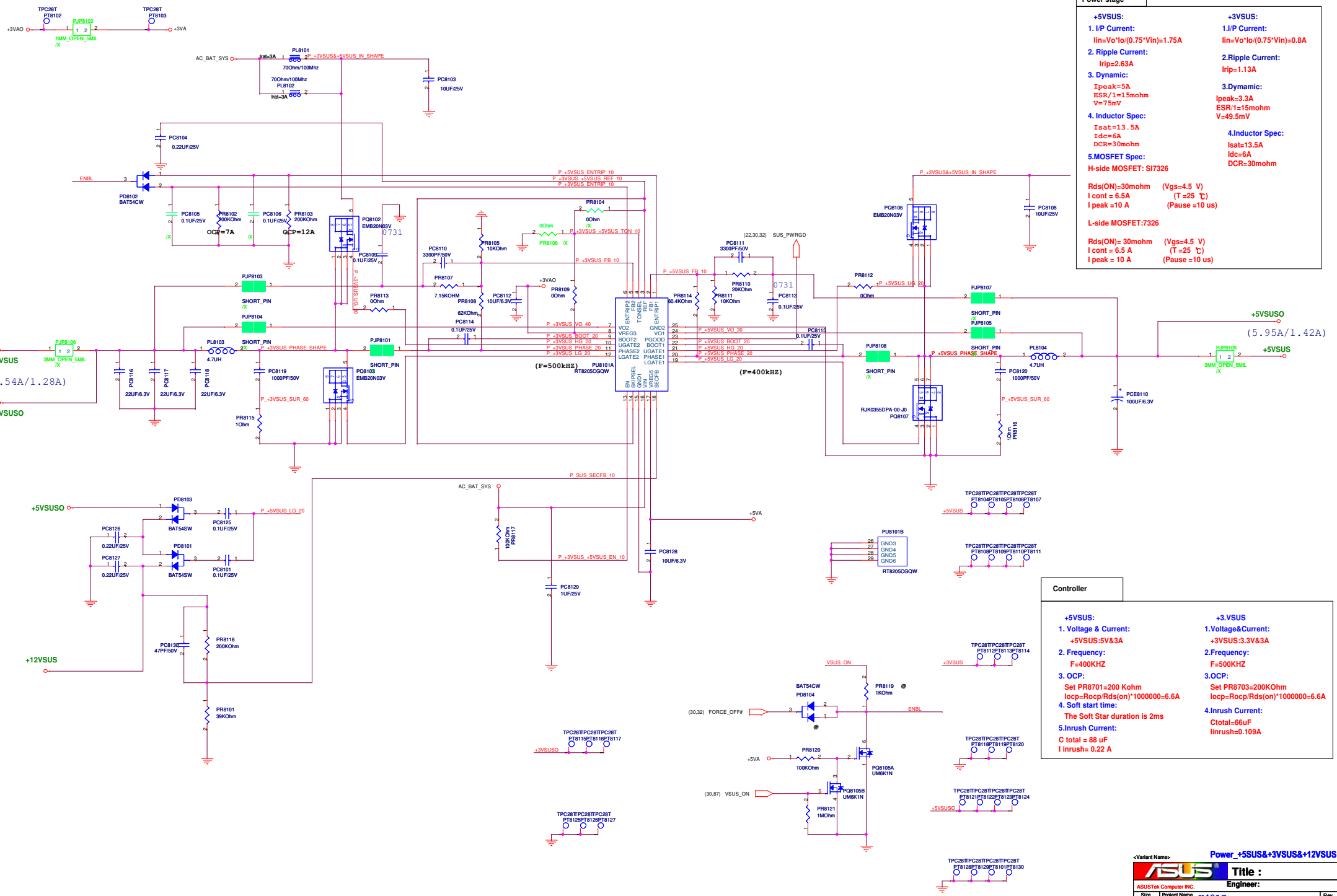
A

A

		Title : VGA_M96_STRAP	
ASUSTeK COMPUTER INC. NB4		Engineer: Leon	
Size	Project Name	Rev	
A3	K52Jr	1.0	
Date: Thursday, November 12, 2009		Sheet	79 of 99

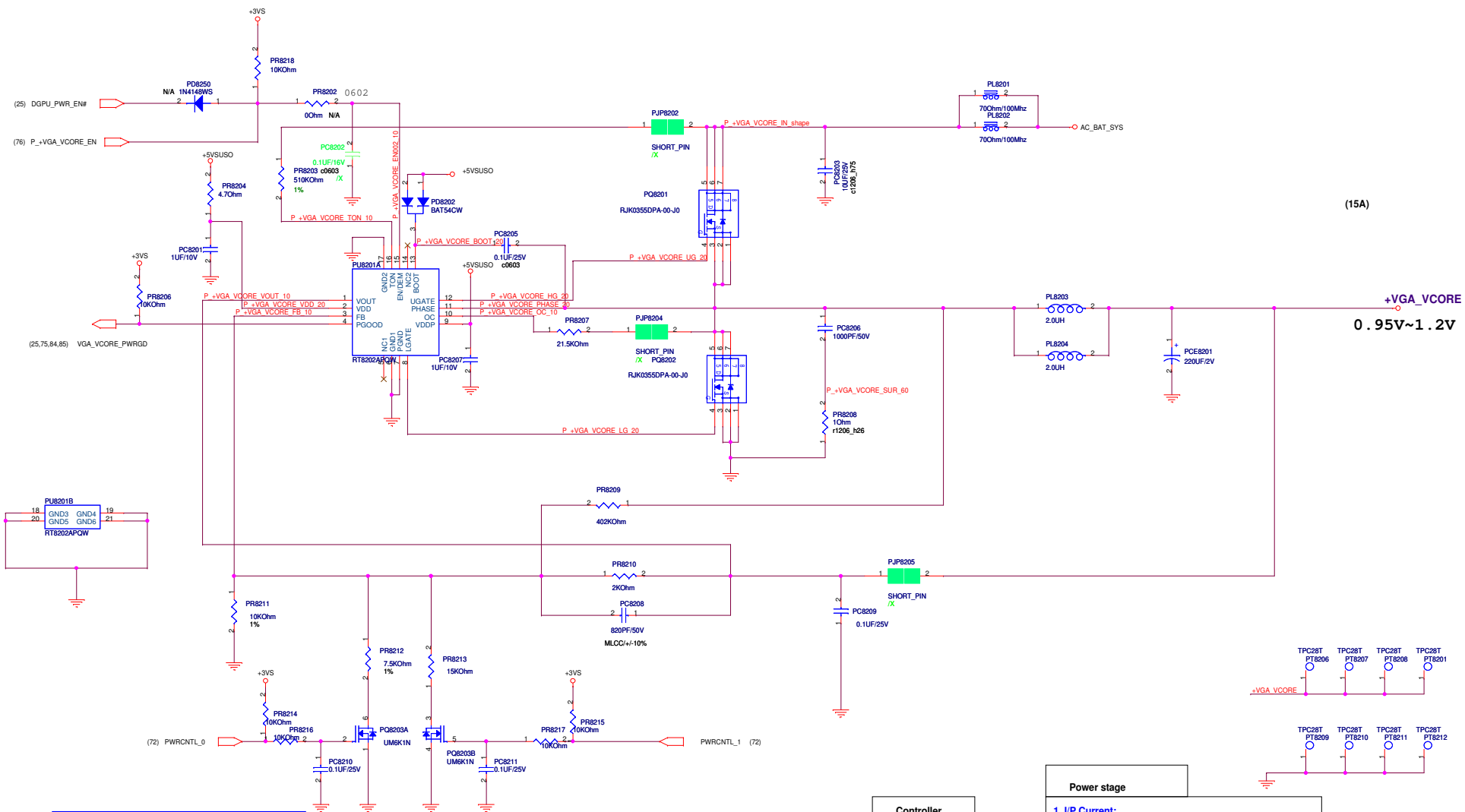


ASUS Title: Power Flow
 Project Name: Z98-K10M-L1U
 Engineer: Z98-K10M-L1U
 Date: 2014/08/04
 Version: 1.000



Power stage	
+5VSUS:	+3VSUS:
1. I/P Current: $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 1.75A$	1. I/P Current: $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 0.8A$
2. Ripple Current: $I_{rip} = 2.63A$	2. Ripple Current: $I_{rip} = 1.13A$
3. Dynamic: $I_{peak} = 5A$ $ESR / 1 = 1.5mohm$ $V = 75mV$	3. Dynamic: $I_{peak} = 3.3A$ $ESR / 1 = 15mohm$ $V = 49.5mV$
4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$	4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$
5. MOSFET Spec: H-side MOSFET: SI7326 L-side MOSFET: 7326	
$R_{ds(ON)} = 30mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 10A$ (Pause = 10us)	
$R_{ds(ON)} = 30mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 10A$ (Pause = 10us)	

Controller	
+5VSUS:	+3VSUS
1. Voltage & Current: +5VSUS: 5V & 3A	1. Voltage & Current: +3VSUS: 3.3V & 3A
2. Frequency: $F = 400KHZ$	2. Frequency: $F = 500KHZ$
3. OCP: Set PR8701 = 200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} * 1000000 = 6.6A$	3. OCP: Set PR8703 = 200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} * 1000000 = 6.6A$
4. Soft start time: The Soft Star duration is 2ms	4. Inrush Current: $C_{total} = 66uF$ $I_{inrush} = 0.109A$
5. Inrush Current: $C_{total} = 88uF$ $I_{inrush} = 0.22A$	



(15A)

+VGA_VCORE
0.95V~1.2V

PWRMNTL_0	PWRMNTL_1	VGA_VCORE	
0	0	0.9	-5%
0	1	1.0	Normal
1	0	1.1	+5%
1	1	1.2	+10%

Controller

1. Voltage & Current:
+1.2VSUS: 16A

2. Frequency:
Ton=3.85p*RT(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ

Set PR8107=21.5kohm
loop=Rocp*20/Rds(on)=26A

4. Soft start time:
Soft-Star duration is 1.35ms

5. Inrush Current:
C total =220uF
I inrush=0.163A

Power stage

1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:
Iripple=3.74A

3.ripple voltage:
Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
DCR=3.3mohm
V=6.831mV

4. Inductor Spec: 3. OCP:
Isat=25A
Idc=15.5A
DCR=5.5mohm

5. MOSFET Spec:
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

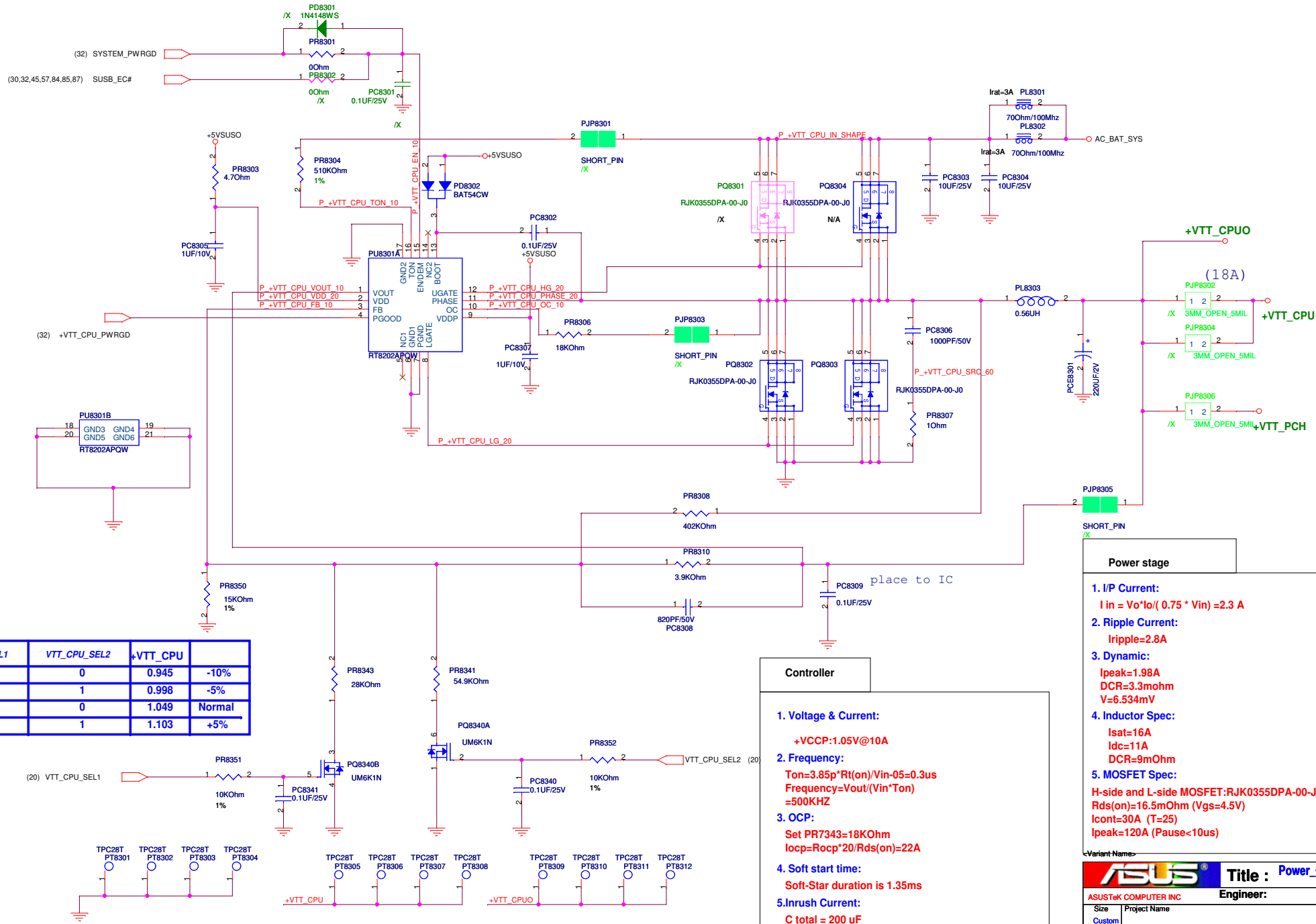
<Variant Name>

ASUS Title: Power_+VGA_VCORE

ASUSTek COMPUTER INC Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Thursday, November 12, 2009 Sheet 82 of 1



VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

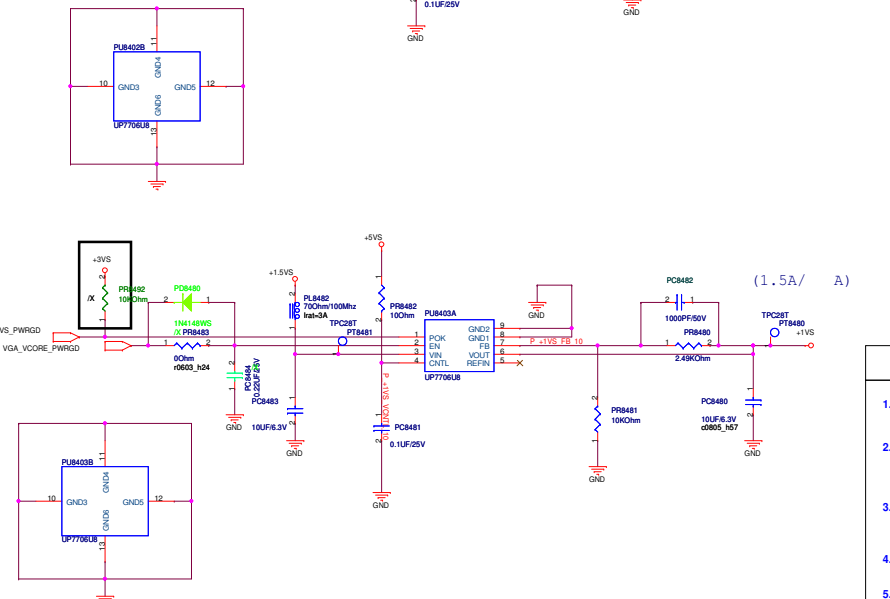
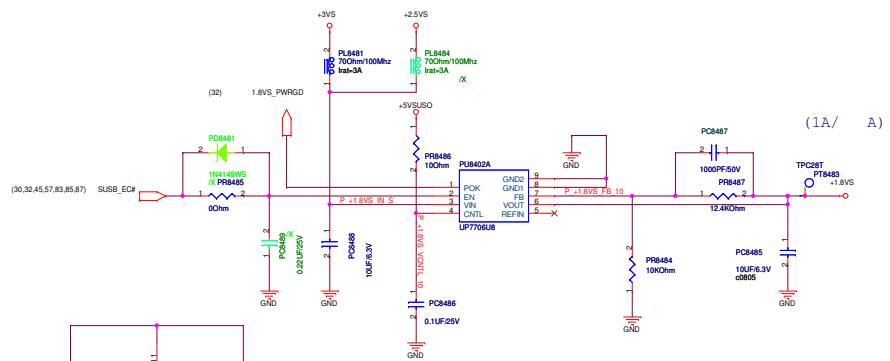
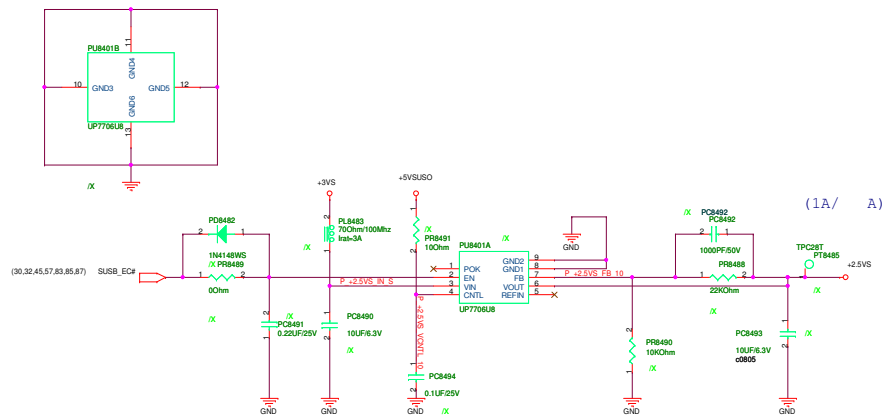
Controller

- Voltage & Current:**
+VCCP: 1.05V@10A
- Frequency:**
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ
- OCP:**
Set PR7343=18KOhm
Iocp=Rocp*20/Rds(on)=22A
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush Current:**
C total = 200 uF
I inrush= 0.16 A

Power stage

- I/P Current:**
I in = Vo*Io/(0.75 * Vin) =2.3 A
- Ripple Current:**
Iripple=2.8A
- Dynamic:**
Ipeak=1.98A
DCR=3.3mohm
V=6.534mV
- Inductor Spec:**
Isat=16A
Idc=11A
DCR=9mOhm
- MOSFET Spec:**
H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

ASUS
Title : Power_+VCCP
 ASUSTeK COMPUTER INC
 Engineer:
 Size Project Name Rev 1.0
 Custom
 Date: Thursday, November 12, 2009 Sheet 83 of 1



Controller

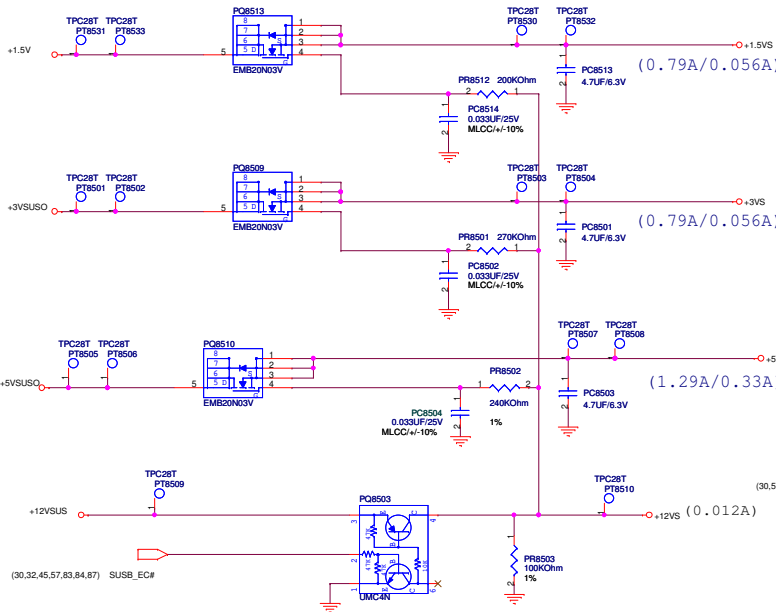
- Voltage & Current:**
+1.8V/+1.8V&12A
- Frequency:**
 $T_{on} = 3.85p \cdot R_{t(on)} \cdot V_o / V_{in} - 05$
Frequency = $V_{out} / (V_{in} \cdot T_{on})$
= 500KHZ
- OCP:**
Set PR7343=18kohm
 $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)}$
= 20 * 1.5 / 16.5 = 26A
- Soft start time:**
Soft-Start duration is 1.35ms
- Inrush Current:**
C total = 100uF
inrush = 0.133A

Power stage

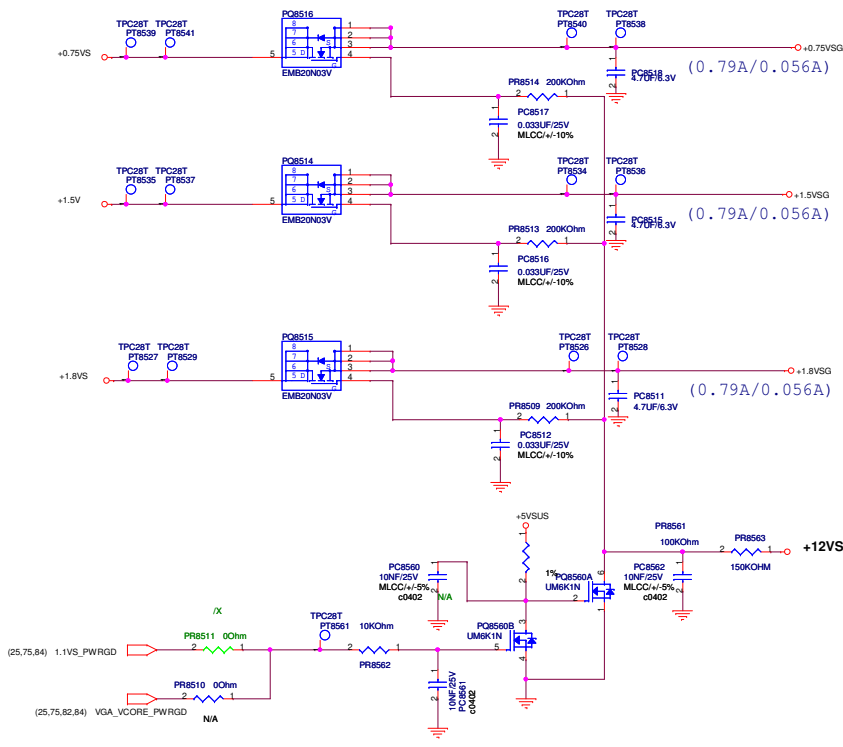
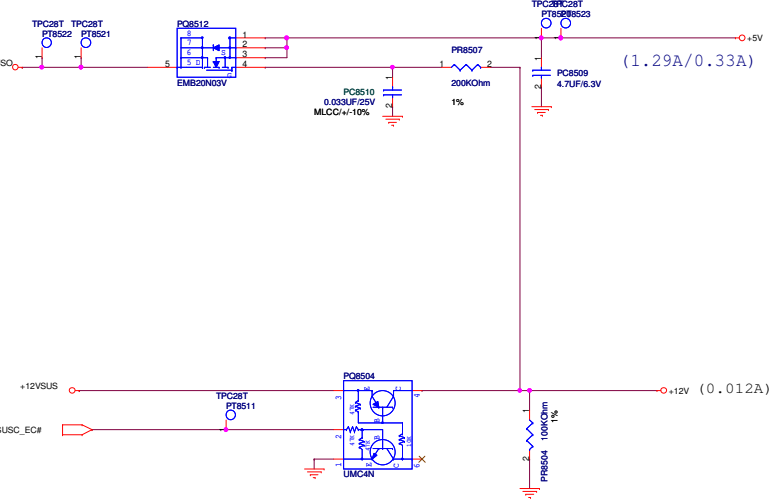
- I/P Current:**
 $I_{in} = V_o / I_o (0.8 \cdot V_{in}) = 0.947A$
- Ripple Current:**
Irripple = 2.342A
- Ripple Voltage:**
 $I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 3.25A$
DCR = 3.3mohm
 $V = 10.75mV$
- Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
DCR = 3.3mohm
- MOSFET Spec:**
H-side and L-side MOSFET:
 $R_{ds(on)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25$)
 $I_{peak} = 120A$ (Pause < 10us)

ASUS
ASUSTek COMPUTER INC
Title: Power +1.8V&+0.9V
Engineer:
Size: Custom
Date: Thursday, November 18, 2009
Sheet: 84 of 1
Rev: 1.0

SUSB#_PWR POWER



SUSC#_PWR POWER



5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title: Power_good_detector	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Thursday, November 12, 2009		Sheet	86 of 1

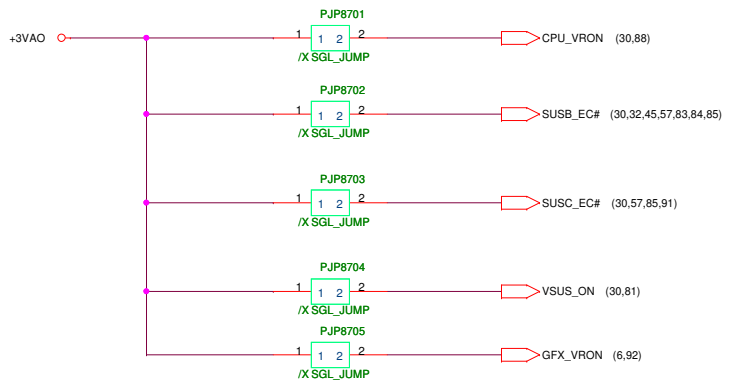
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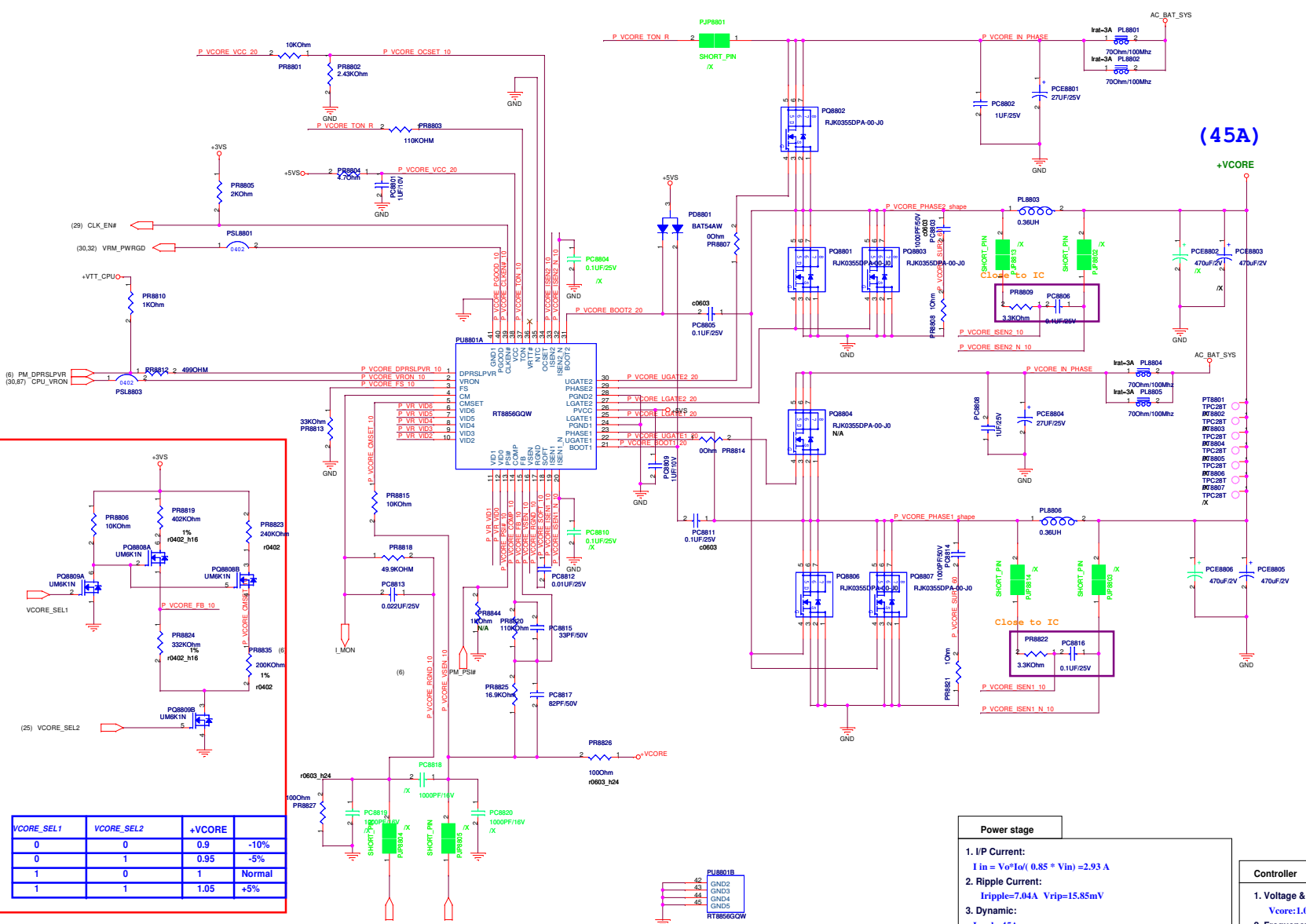
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3

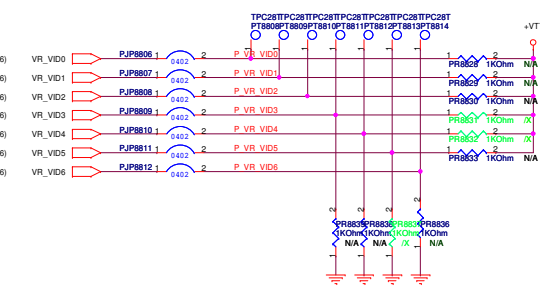
2

1





VCORE_SEL1	VCORE_SEL2	+VCORE	
0	0	0.9	-10%
0	1	0.95	-5%
1	0	1	Normal
1	1	1.05	+5%



CPU SKU	Ic_CORE-MAX Maximum CPU Core Current	Icp (IMON=300 mV min) [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled			000	
59A^C I _{CP,Core} max 520 A	30	010	011	45.0
29A^C I _{CP,Core} max 520 A	30	010	010	30.0
30A^C I _{CP,Core} max 540 A	40	011	011	22.5
40A^C I _{CP,Core} max 550 A	50	100	100	18.0
50A^C I _{CP,Core} max 560 A	60	101	101	15.0
60A^C I _{CP,Core} max 570 A	70	110	110	12.9
70A^C I _{CP,Core} max 590 A	90	111	111	10.0

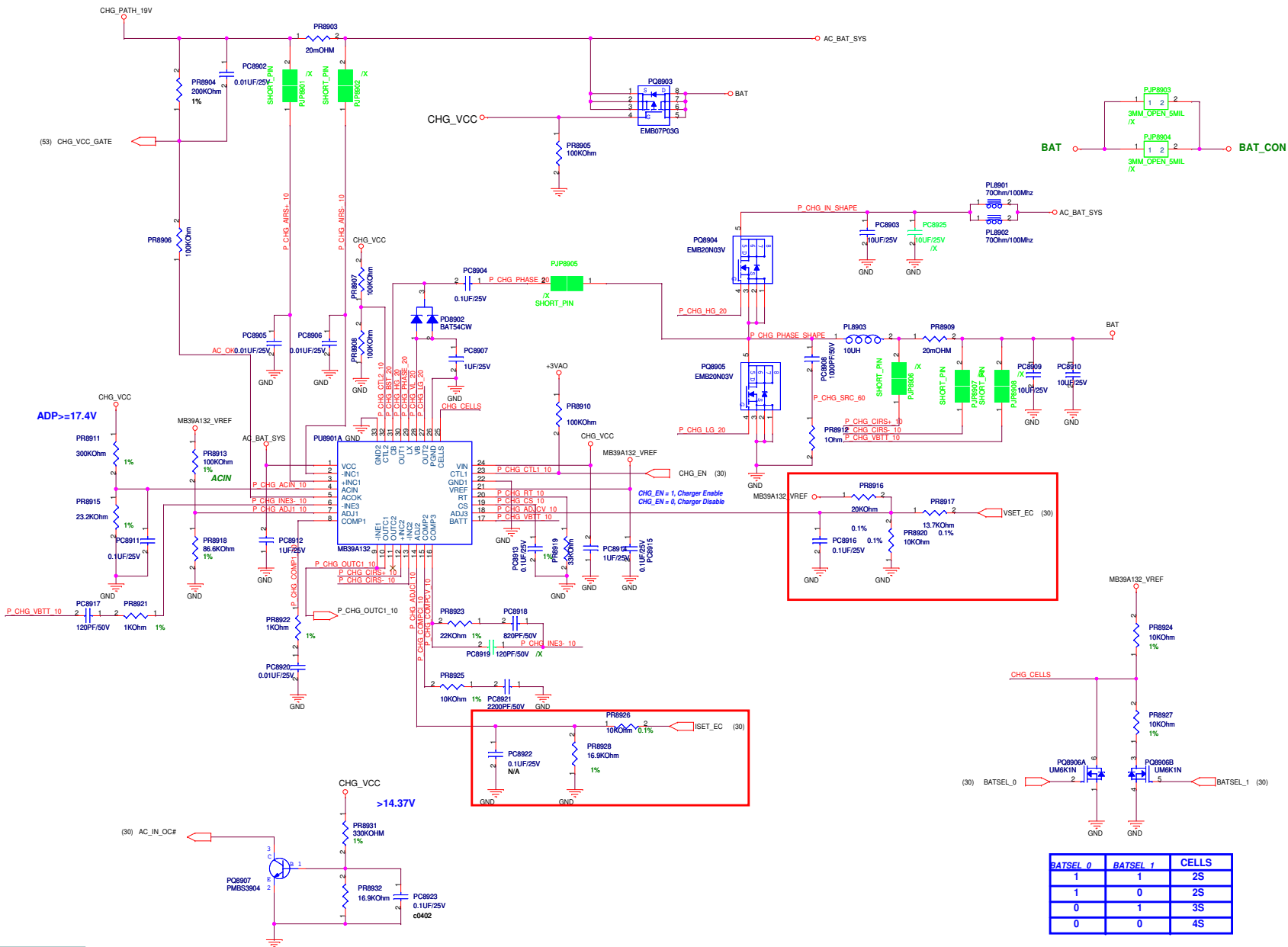
- VID[2:0] "Reserved" - default VID[2:0]='111' - option to change default should be provided on the motherboard.
- VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
- VID[6] "Reserved" - default VID [6]='0' - option to change default should be provided on the motherboard.
- DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR='1' for IMVP-6.5-compliant controller.
- PSI# - "Reserved" - default PSI#='0' - option to change default should be provided on the motherboard.

Power stage

- I/P Current:**
 $I_{in} = V_o^2 / (0.85 * V_{in}) = 2.93 A$
- Ripple Current:**
 $I_{ripple} = 7.04A$ $V_{rip} = 15.85mV$
- Dynamic:**
 $I_{peak} = 45A$
 $ESR = 2.25mohm$
 $V = 91.1mV$
- Inductor Spec:**
 $I_{dc} = 38.8A$
 $I_{temp} = 32.5A$
 $DCR = 1.1m\Omega$
- MOSFET Spec:**
 H-side MOSFET: RJK0355 L-side MOSFET: RJK0353
 $R_{ds(on)} = 16.5m\Omega$ (V_{gs}=4.5V) $R_{ds(on)} = 7.6m\Omega$ (V_{gs}=4.5V)
 $I_{cont} = 30A$ (T=25) $I_{cont} = 35A$ (T=25)
 $I_{peak} = 120A$ (Pause<100s) $I_{peak} = 140A$ (Pause<100s)
- CPU MLCC: 16*10uF**

Controller

- Voltage & Current:**
 $V_{core} = 1.05V/45A$
- Frequency:**
 $CCM: F_{sw} = 300 * 33 / R_{FS} = 300KHZ$
- OCP:**
 $V_{ocet} = 25 * I_{lim} * R_{sense}$
 $I_{lim} = 35.5 * 2 = 71A$
- Slew rate:**
 $Slewrate = I_{ss} / PC7810 = 100uA / 10nF = 10mV/uS$
- Inrush Current:**
 $C_{total} = 880 nF$
 $I_{inrush} = 0.154 A$
- Droop Resistance:**
 $R_{droop} = R1 / R2 * 10 * R_{sense} = 2mohm$



- 1. Adapter Threshold: 17.41V**
 $17.41 = (PR9213 + PR9216) / PR9216 * 1.25$
- 2. AP4835 ID=9.2A**
- 3. MB39A132_VREF= 5.0V**
- 4. Input limit:**
 $65W: I_{limit_current} = (V_{adj} - 0.075) / (25 * R_s) = (1.646 - 0.075) / 25 * 0.02 = 3.14A$
 $330K - 162K$
 $90W: 100K - 86.6K : I_{limit_current} = 4.49A$
- 5. Charging Voltage LI**

VSET_EC	2S	3S	4S
2.9894	3.399	12.598	16.797

- 6. Charging current LI**

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Power stage

- 1. I/P Current(3S2P):**
 $I_{in} = V_o * I_o / (0.75 * V_{in}) = 2.21A$
- 2. Ripple Current(3S2P):**
 $r_{ripple} = 1.18A$
- 3. Inductor Spec:**
 $I_{sat} = 4.4A$
 $I_{dc} = 3.8A$
 $DCR = 35m\Omega$
- 4. MOSFET Spec:**
 $I_{dc} = 6.5A / 5.0A$
 $R_{dcon} = 22 / 30m\Omega$
 $V_{gsth} = 0.8 - 1.8V$

Controller

- 1. Frequency:**
 $f_{osc}(KHz) = 17000 / RT (K\Omega)$
 $f_{osc}(KHz) = 17000 / 33K = 515KHz$
- 2. OCP:**
 $I_{oc} = 0.2 / R_s = 10A$
- 3. Soft start time:**
 $t_s(s) = 0.26 * CS(uF) = 0.26 * 0.1 = 26ms$
- 4. Inrush current(3S):**
 $I_{inrush} = C * V / t = 9.7mA$

EC Code: 202

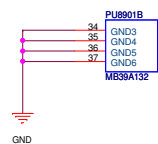
<Variant Name>

ASUS Title: **Power Charger**

ASUSTek Computer INC. Engineer: **Limy Ji**

Size	Project Name	Rev
C		1.0


Date: Thursday, November 12, 2009 Sheet 89 of 1

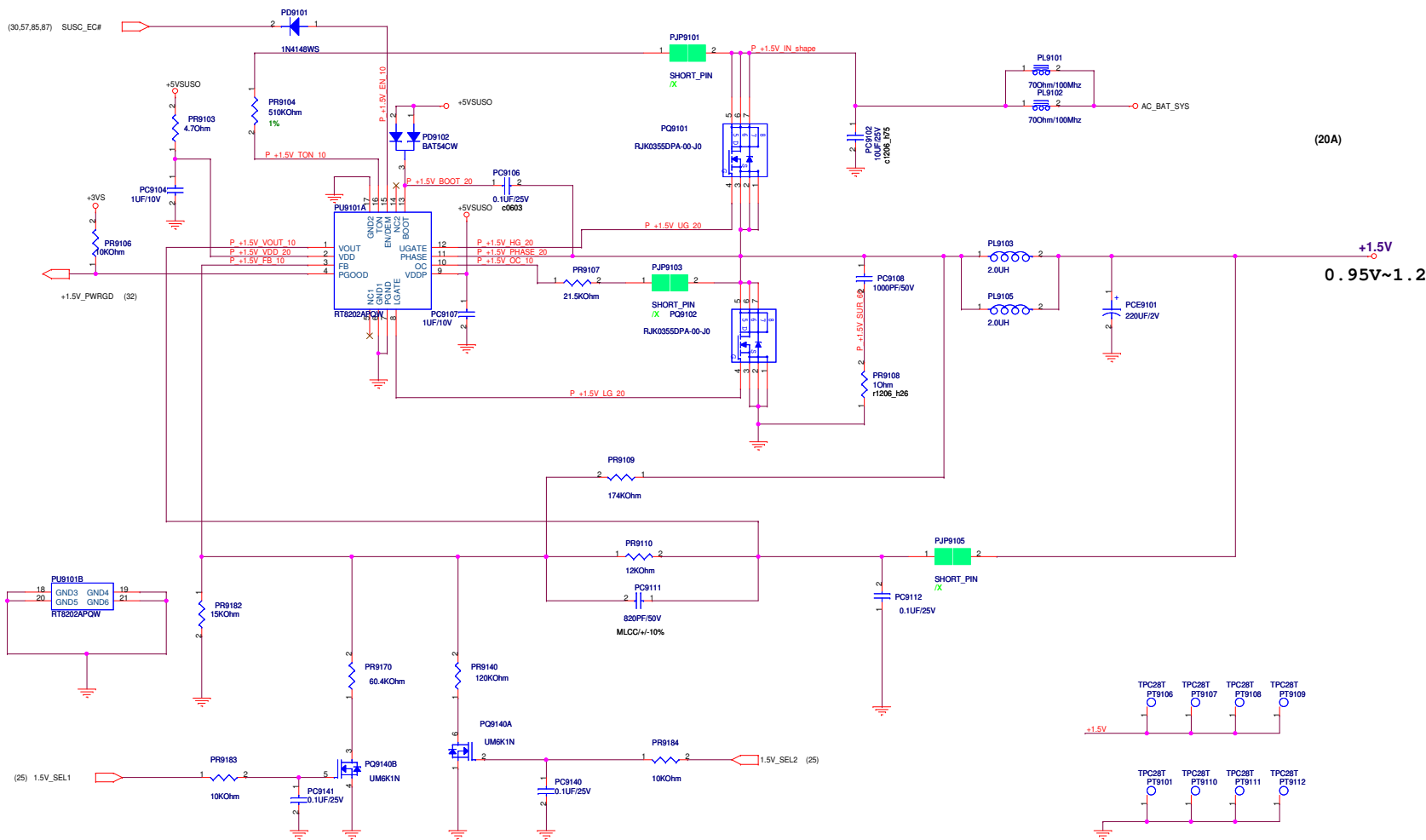


BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

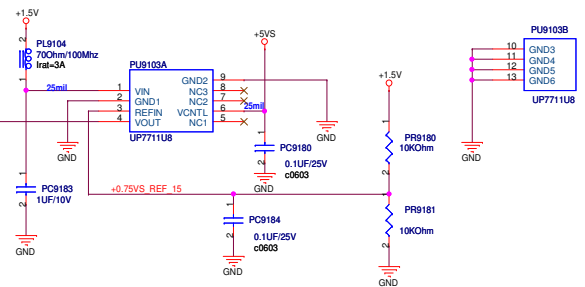


<Variant Name>

		Title : Power_Charger	
ASUSTek Computer INC.		Engineer: <i>Limy_H</i>	
Size	Project Name	Rev	
A3	F83T	2.1G	
Date: Thursday, November 12, 2009		Sheet	90 of 1



0.75VS / 0.5A



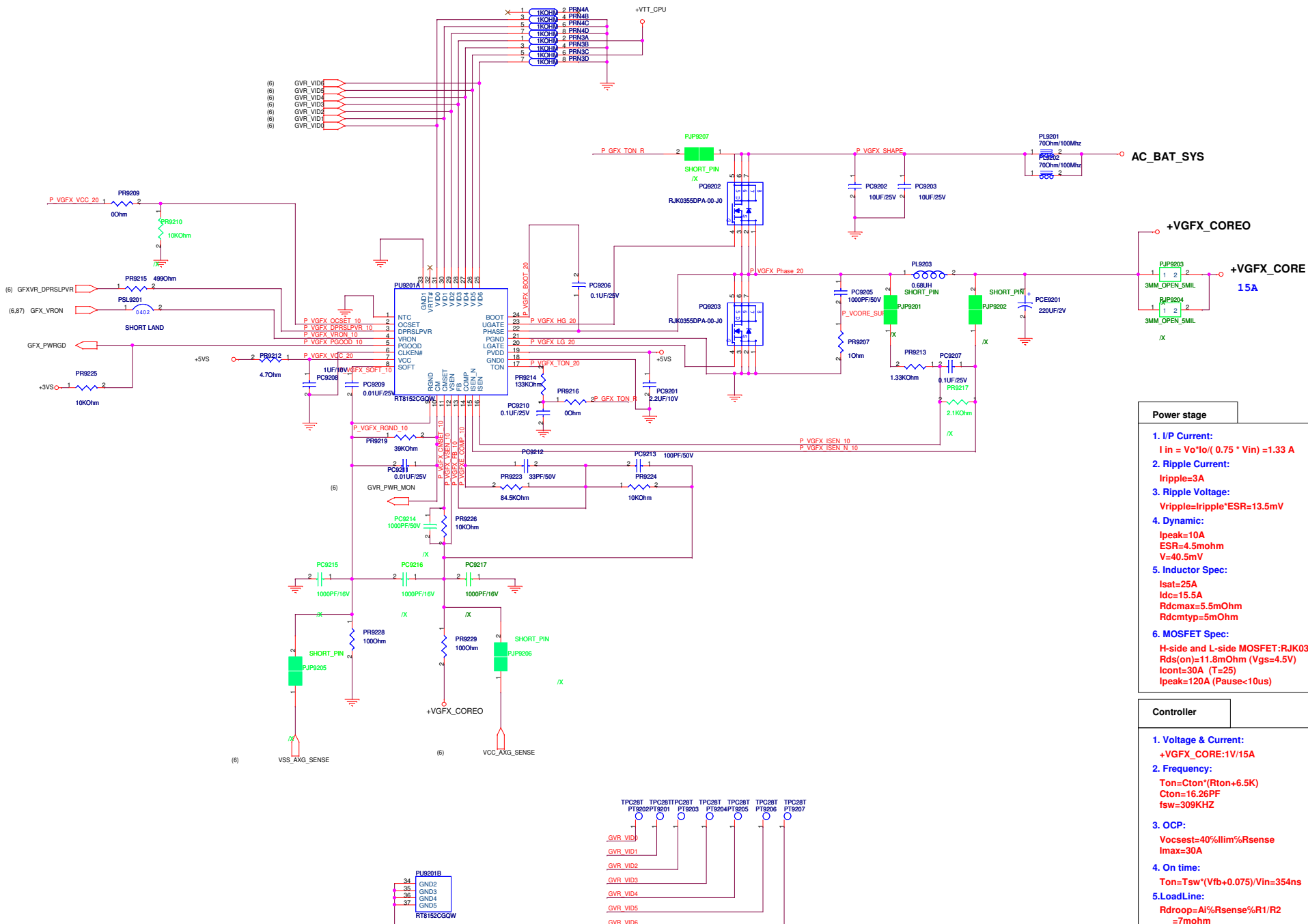
1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

Controller

- Voltage & Current:**
+1.2VSUS: 16A
- Frequency:**
Ton=3.85p*RI(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ
- OCp:**
Set PR8107=21.5kohm
Iocp=Rocp*20/Rds(on)=26A
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush Current:**
C total =220uF
I inrush=0.163A

Power stage

- I/P Current:**
I in = Vo*Io/(0.75 * Vin) =0.85A
- Ripple Current:**
Iripple=3.74A
- ripple voltage:**
Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
DCR=3.3mohm
V=6.831mV
- Inductor Spec:**
Isat=25A
I dc=15.5A
DCR=5.5mohm
- MOSFET Spec:**
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)



- Power stage**
- I/P Current:**
 $I_{in} = V_o/I_o(0.75 * V_{in}) = 1.33 A$
 - Ripple Current:**
 $I_{ripple} = 3A$
 - Ripple Voltage:**
 $V_{ripple} = I_{ripple} * ESR = 13.5mV$
 - Dynamic:**
 $I_{peak} = 10A$
 $ESR = 4.5mohm$
 $V = 40.5mV$
 - Inductor Spec:**
 $I_{sat} = 25A$
 $I_{dc} = 15.5A$
 $R_{dcmax} = 5.5mOhm$
 $R_{dcmtyp} = 5mOhm$
 - MOSFET Spec:**
 H-side and L-side MOSFET: RJK0355
 $R_{ds(on)} = 11.8mOhm (V_{gs} = 4.5V)$
 $I_{cont} = 30A (T = 25)$
 $I_{peak} = 120A (Pause < 10us)$

- Controller**
- Voltage & Current:**
 $+VGFX_CORE: 1V/15A$
 - Frequency:**
 $T_{on} = C_{ton} * (R_{ton} + 6.5K)$
 $C_{ton} = 16.26PF$
 $f_{sw} = 309KHZ$
 - OCP:**
 $V_{ocset} = 40% I_{lim} * R_{sense}$
 $I_{max} = 30A$
 - On time:**
 $T_{on} = T_{sw} * (V_{fb} + 0.075) / V_{in} = 354ns$
 - Load Line:**
 $R_{droop} = A_i * R_{sense} * R1/R2$
 $= 7mohm$

5

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2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : Power_+VCCP	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
C		1.0	
Date: Thursday, November 12, 2009		Sheet	98 of 1

5

4

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2

1

5

4

3

2

1

D

D

C

C


B

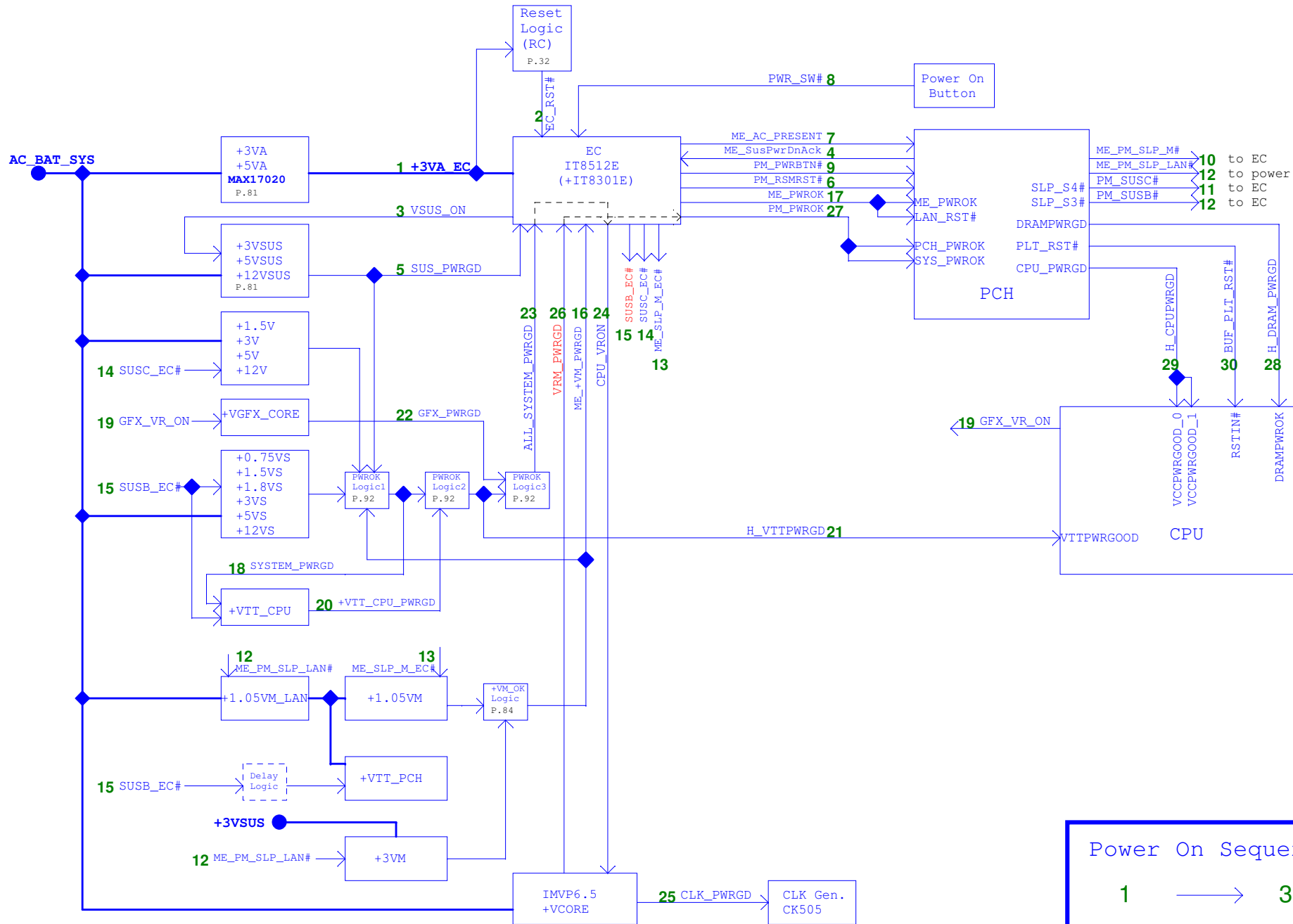
B

A

A

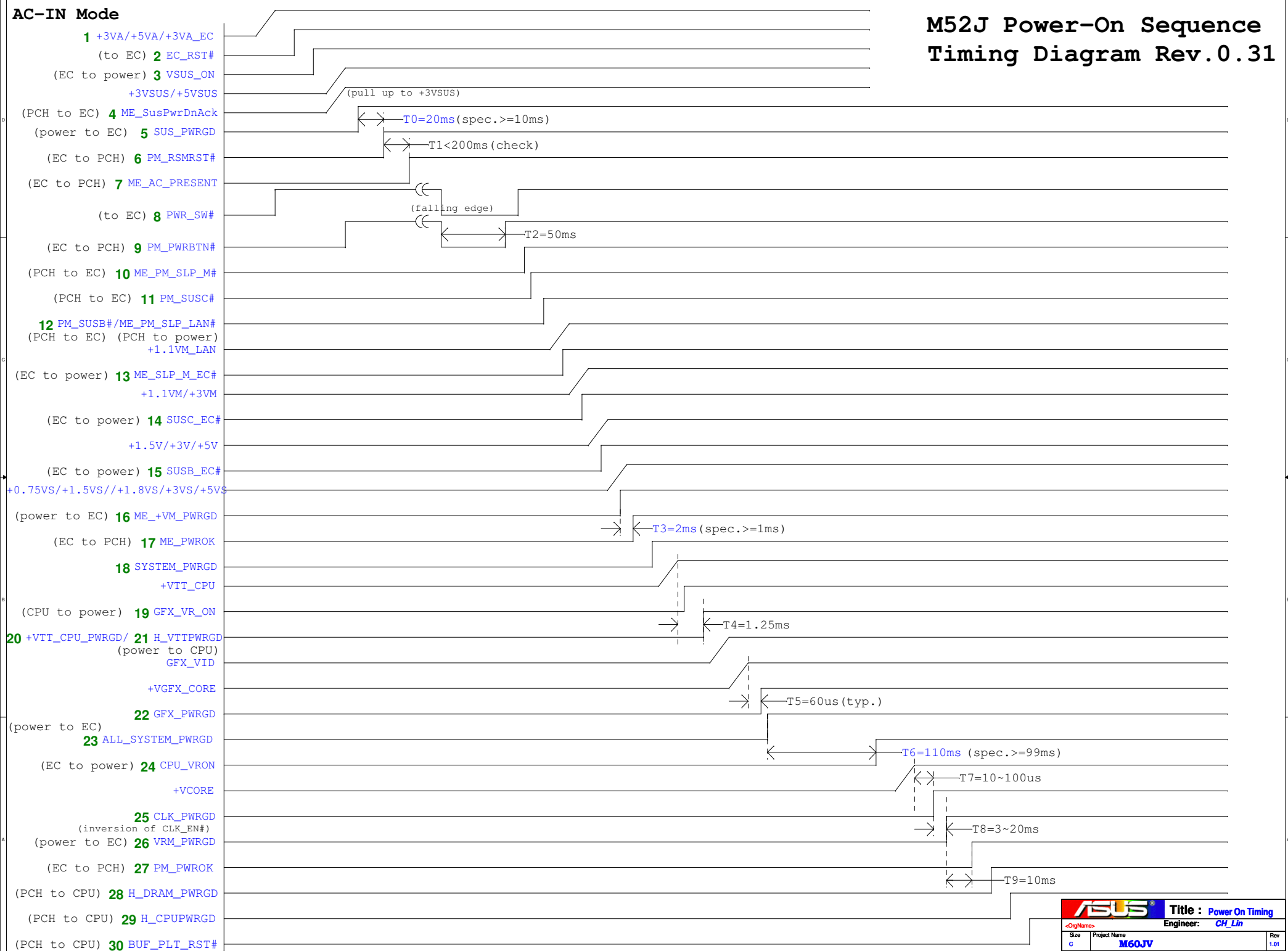
<Variant Name>

		Title : Power_+VCCP	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A3		1.0	
Date: Thursday, November 12, 2009		Sheet	94 of 1



Power On Sequence
1 → 30

M52J Power-On Sequence Timing Diagram Rev.0.31



M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode

