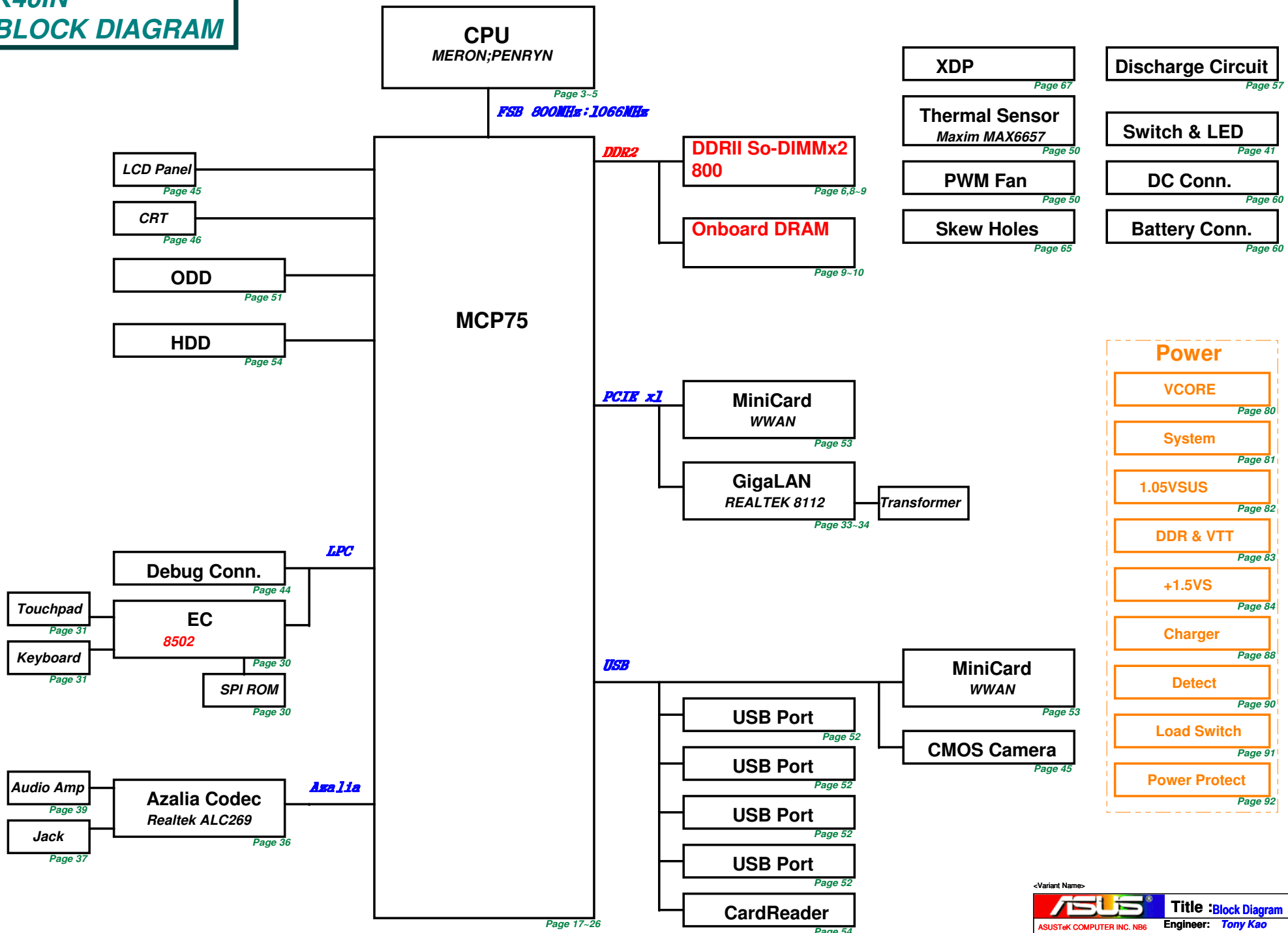
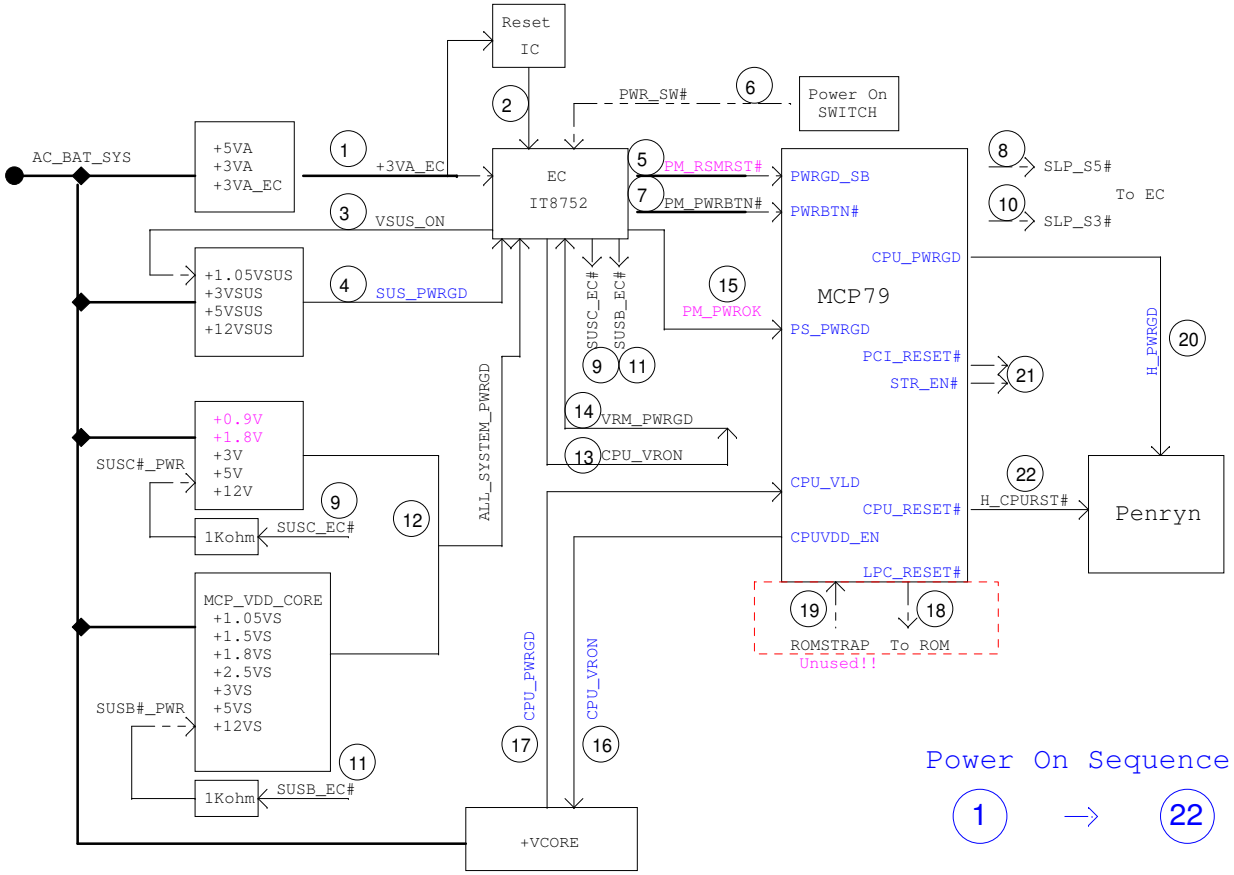
K40IN BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC. NB6	Title : Block Diagram	
	Engineer: Tony Kao	
Size: Custom	Project Name: G71G	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 1 of 91	



<Variant Name>

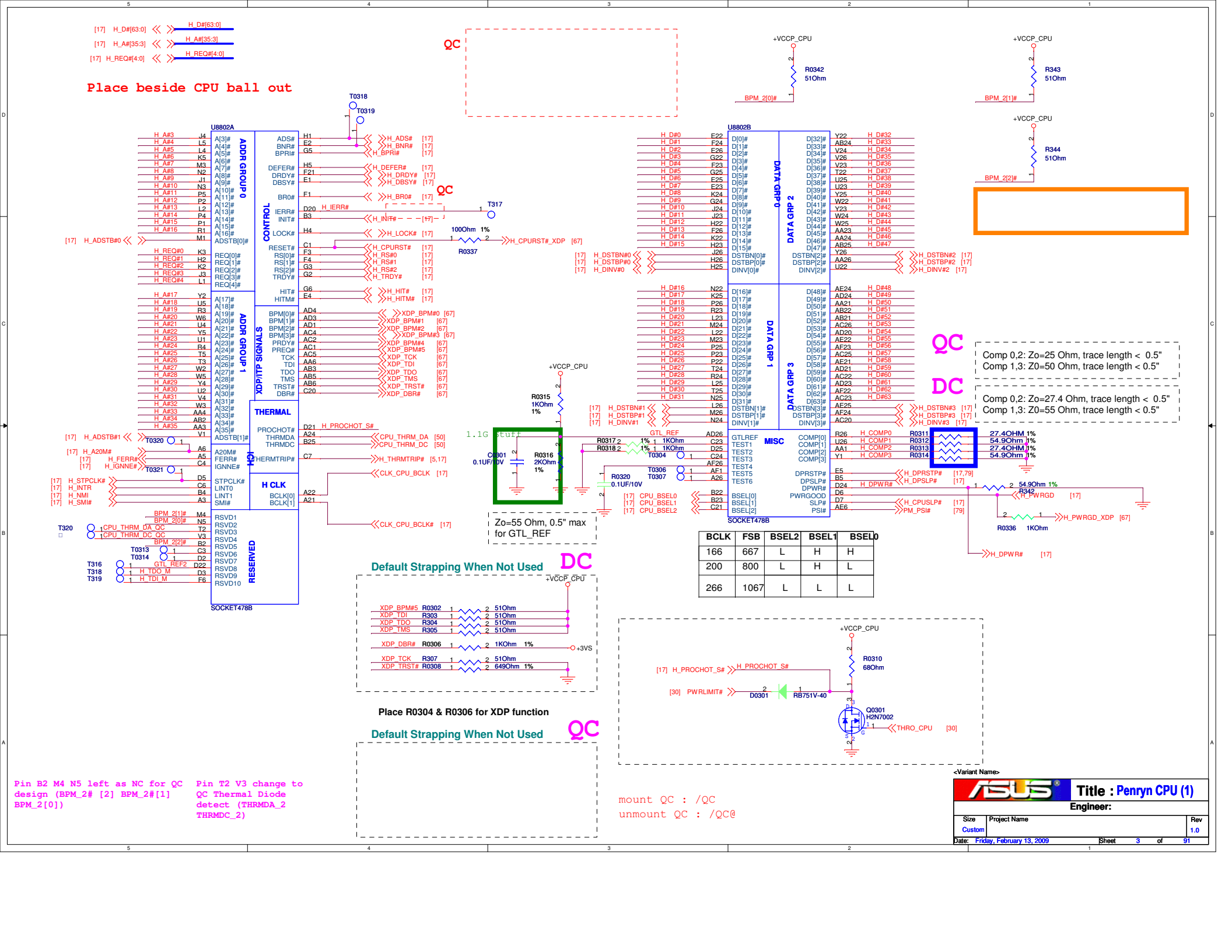
ASUSTeK COMPUTER INC. NB6

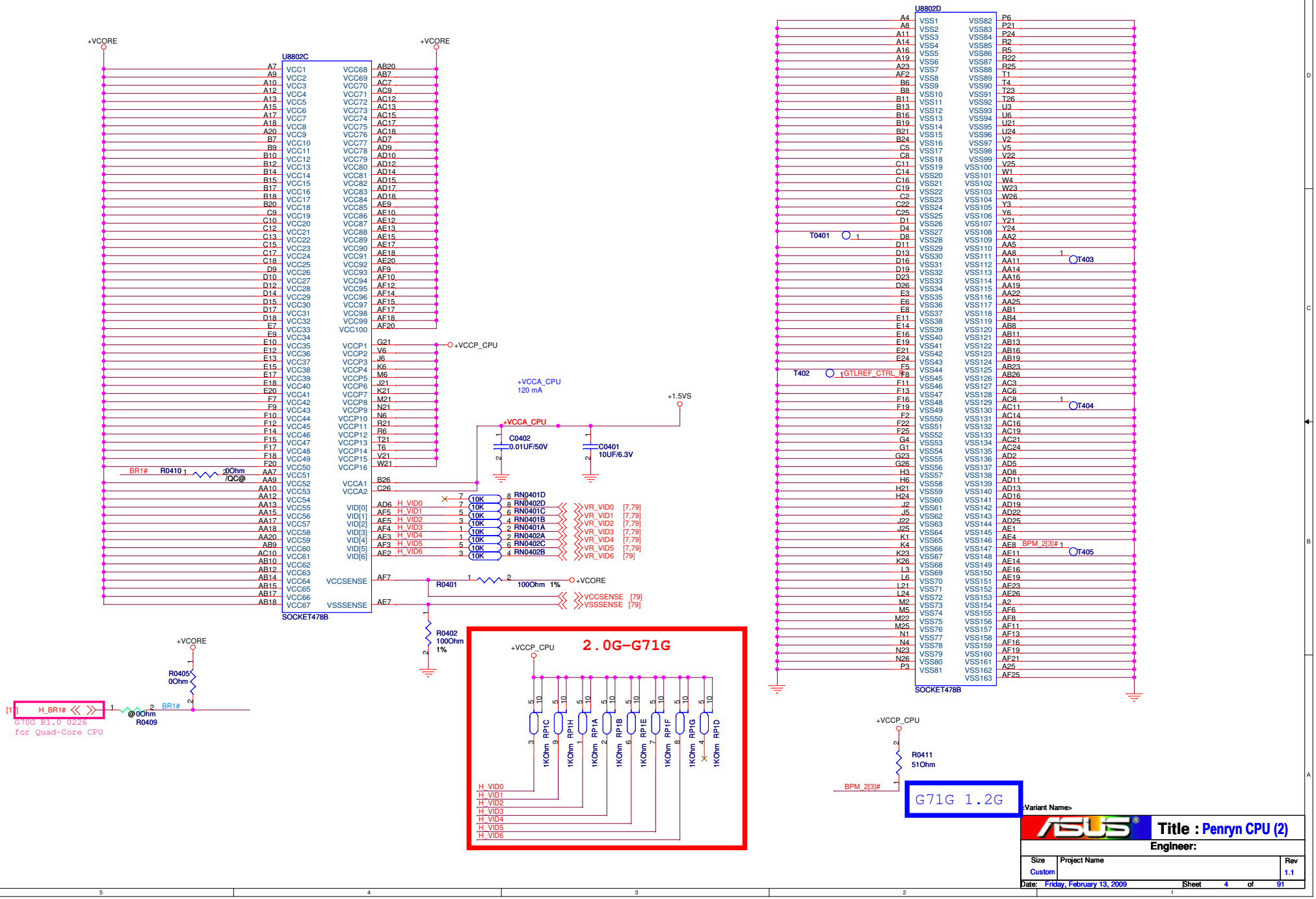
Title : Schematic Information

Engineer: Keirui Shen

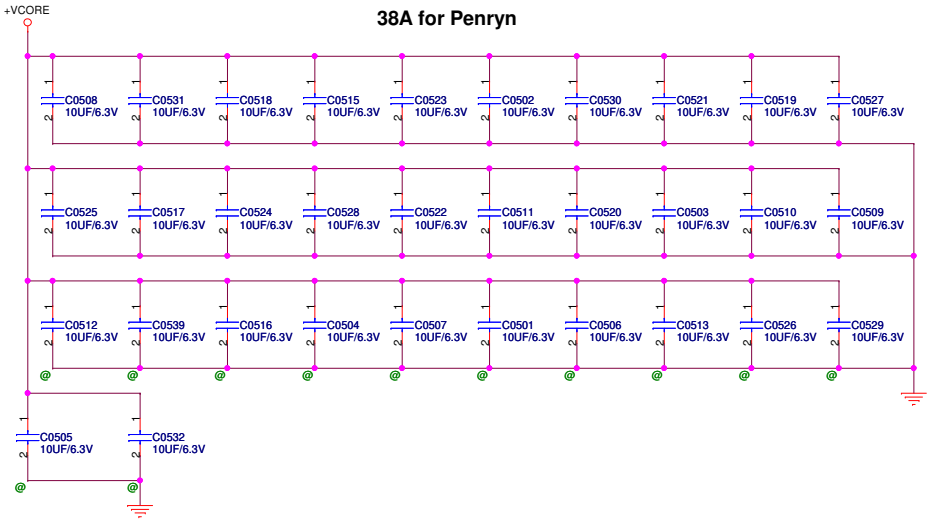
Size	Project Name	Rev
A2	G71G	1.0

Date: Friday, February 13, 2009 Sheet 2 of 91

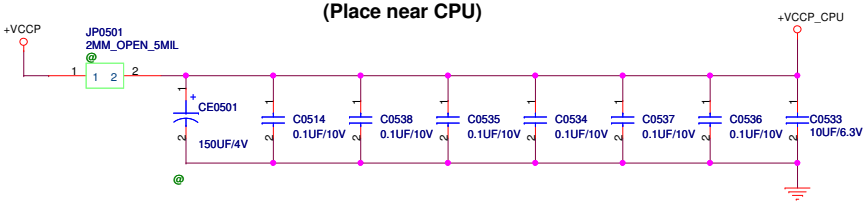

Place beside CPU ball out
QC
DC
U8802A
U8802B
SOCKET478B
ADDR GROUP 0
ADDR GROUP 1
XDP/ITP SIGNALS
CONTROL
THERMAL
H CLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Comp 0,2: Zo=25 Ohm, trace length < 0.5"
Comp 1,3: Z0=50 Ohm, trace length < 0.5"
Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"
Zo=55 Ohm, 0.5" max for GTL_REF
Default Strapping When Not Used
Place R0304 & R0306 for XDP function
Pin B2 M4 N5 left as NC for QC design (BPM_2# [2] BPM_2#[1] BPM_2[0])
Pin T2 V3 change to QC Thermal Diode detect (THRMDA_2 THRMDC_2)
mount QC : /QC
unmount QC : /QC@
BCLK FSB BSEL2 BSEL1 BSEL0
166 667 L H H
200 800 L H L
266 1067 L L L
<Variant Name>
Title : Penryn CPU (1)
Engineer:
Size Custom
Project Name
Rev 1.0
Date: Friday, February 13, 2009
Sheet 3 of 91


U8802C
SOCKET478B
+VCORE
+VCCP_CPU
+VCCA_CPU
120 mA
+1.5VS
C0402
0.01UF/50V
C0401
10UF/6.3V
R0410
0Ohm
/QC@
BR1#
R0401
100Ohm 1%
R0402
100Ohm
1%
R0405
0Ohm
R0409
@0Ohm
H_BR1#
G70G R1.0 0226
for Quad-Core CPU
RN0401D
RN0402D
RN0401C
RN0401B
RN0401A
RN0402A
RN0402C
RN0402B
10K
VR_VID0 [7,79]
VR_VID1 [7,79]
VR_VID2 [7,79]
VR_VID3 [7,79]
VR_VID4 [7,79]
VR_VID5 [7,79]
VR_VID6 [79]
VCCSENSE [79]
VSSSENSE [79]
2.0G-G71G
RP1C
RP1H
RP1A
RP1B
RP1E
RP1F
RP1G
RP1D
1KOhm
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
U8802D
SOCKET478B
T0401
T402
GTLREF_CTRL
T403
T404
T405
BPM_2[3]#
R0411
51Ohm
G71G 1.2G
<Variant Name>
Title : Penryn CPU (2)
Engineer:
Size
Custom
Project Name
Rev
1.1
Date: Friday, February 13, 2009
Sheet 4 of 91

38A for Penryn



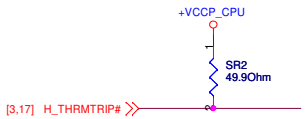
+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?



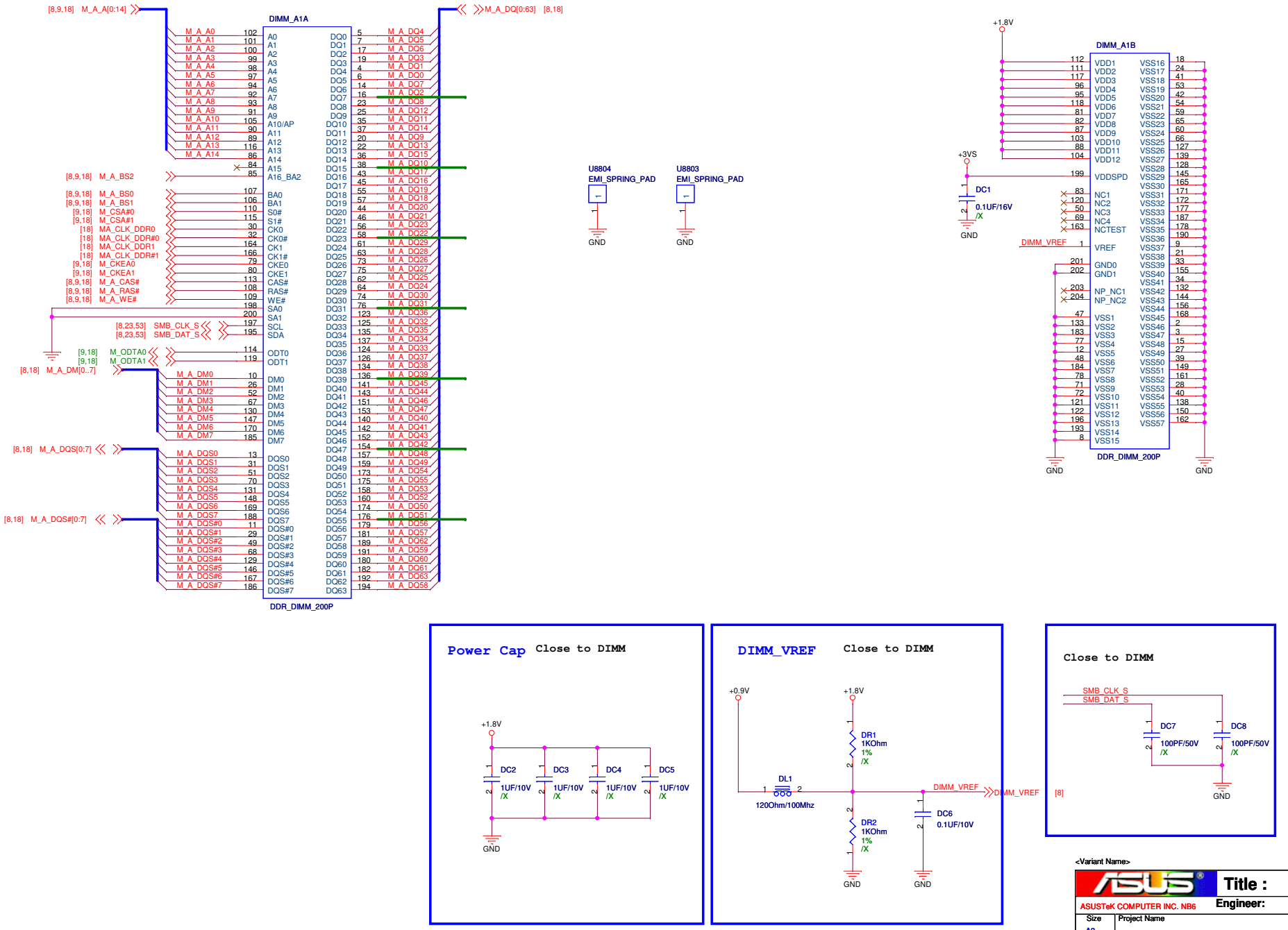
<Variant Name>

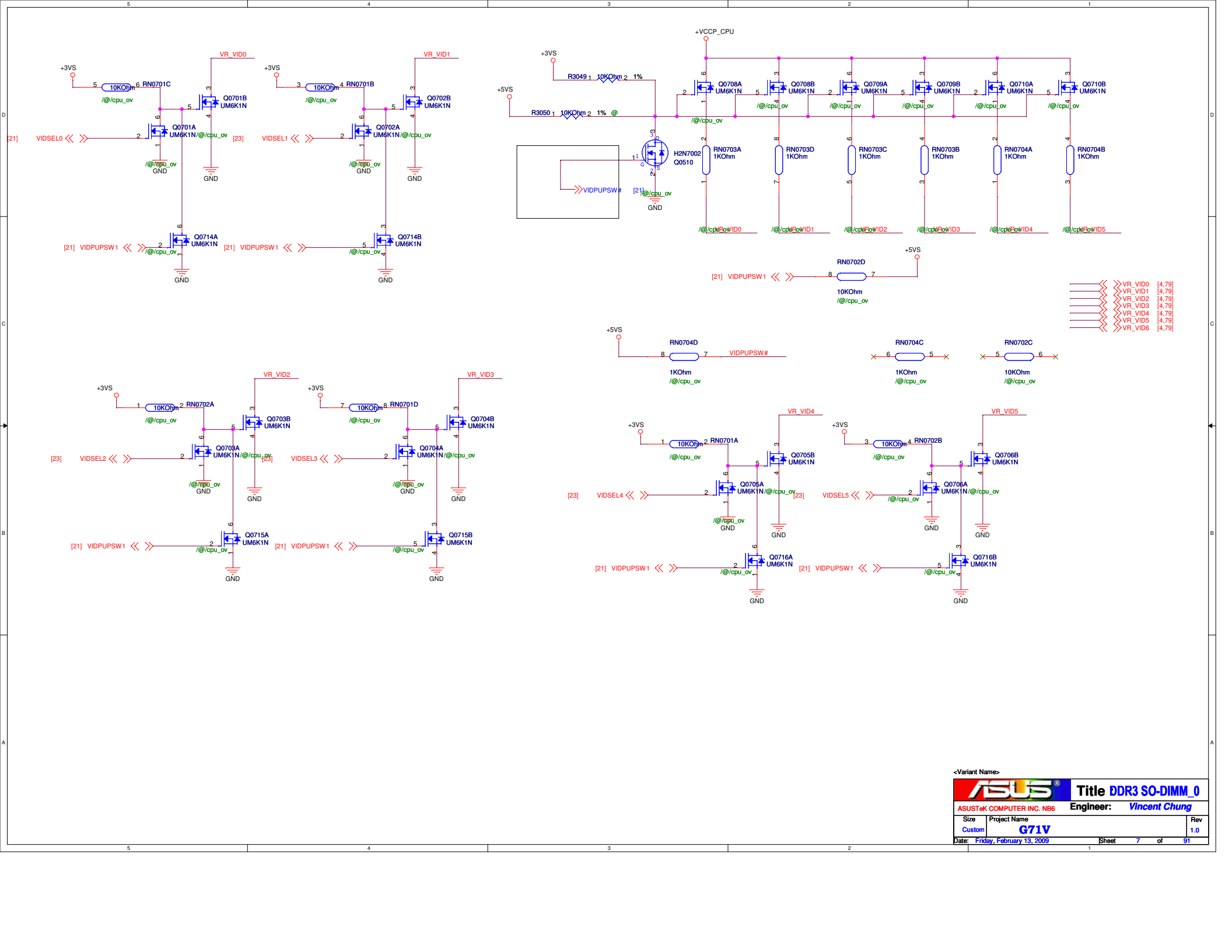
Title : CPU CAPS

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 5 of 91


DIMM_A1A
[8,9,18] M_A_A[0:14]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2
[8,9,18] M_A_BS2
[8,9,18] M_A_BS0
[8,9,18] M_A_BS1
[9,18] M_CSA#0
[9,18] M_CSA#1
[18] MA_CLK_DDR0
[18] MA_CLK_DDR#0
[18] MA_CLK_DDR1
[18] MA_CLK_DDR#1
[9,18] M_CKEA0
[9,18] M_CKEA1
[8,9,18] M_A_CAS#
[8,9,18] M_A_RAS#
[8,9,18] M_A_WE#
BA0 BA1 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#
SA0 SA1
[8,23,53] SMB_CLK_S
[8,23,53] SMB_DAT_S
SCL SDA
[9,18] M_ODTA0
[9,18] M_ODTA1
ODT0 ODT1
[8,18] M_A_DM[0..7]
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
[8,18] M_A_DQS[0:7]
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
[8,18] M_A_DQS#[0:7]
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ3 M_A_DQ1 M_A_DQ0 M_A_DQ7 M_A_DQ2 M_A_DQ8 M_A_DQ12 M_A_DQ11 M_A_DQ14 M_A_DQ9 M_A_DQ13 M_A_DQ15 M_A_DQ10 M_A_DQ17 M_A_DQ16 M_A_DQ19 M_A_DQ18 M_A_DQ20 M_A_DQ21 M_A_DQ23 M_A_DQ22 M_A_DQ29 M_A_DQ28 M_A_DQ26 M_A_DQ27 M_A_DQ25 M_A_DQ24 M_A_DQ30 M_A_DQ31 M_A_DQ36 M_A_DQ32 M_A_DQ35 M_A_DQ34 M_A_DQ33 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ45 M_A_DQ44 M_A_DQ46 M_A_DQ47 M_A_DQ40 M_A_DQ41 M_A_DQ43 M_A_DQ42 M_A_DQ48 M_A_DQ49 M_A_DQ54 M_A_DQ55 M_A_DQ53 M_A_DQ52 M_A_DQ50 M_A_DQ51 M_A_DQ56 M_A_DQ57 M_A_DQ62 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ63 M_A_DQ58
M_A_DQ[0:63] [8,18]
DDR_DIMM_200P
U8804 EMI_SPRING_PAD
U8803 EMI_SPRING_PAD
GND
DIMM_A1B
+1.8V
+3VS
DC1 0.1UF/16V /X
DIMM_VREF
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDDSPD
NC1 NC2 NC3 NC4 NCTEST VREF
GND0 GND1 NP_NC1 NP_NC2
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15
VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57
DDR_DIMM_200P
Power Cap Close to DIMM
+1.8V
DC2 1UF/10V /X
DC3 1UF/10V /X
DC4 1UF/10V /X
DC5 1UF/10V /X
GND
DIMM_VREF Close to DIMM
+0.9V
+1.8V
DR1 1KOhm 1% /X
DL1 120Ohm/100Mhz
DR2 1KOhm 1% /X
DC6 0.1UF/10V
DIMM_VREF
DIMM_VREF
Close to DIMM
SMB_CLK_S
SMB_DAT_S
DC7 100PF/50V /X
DC8 100PF/50V /X
[8]
GND
<Variant Name>
Title :
ASUSTeK COMPUTER INC. NB6
Engineer:
Size A3
Project Name
Rev 1.0
Date: Friday, February 13, 2009
Sheet 6 of 91



<variant_name>

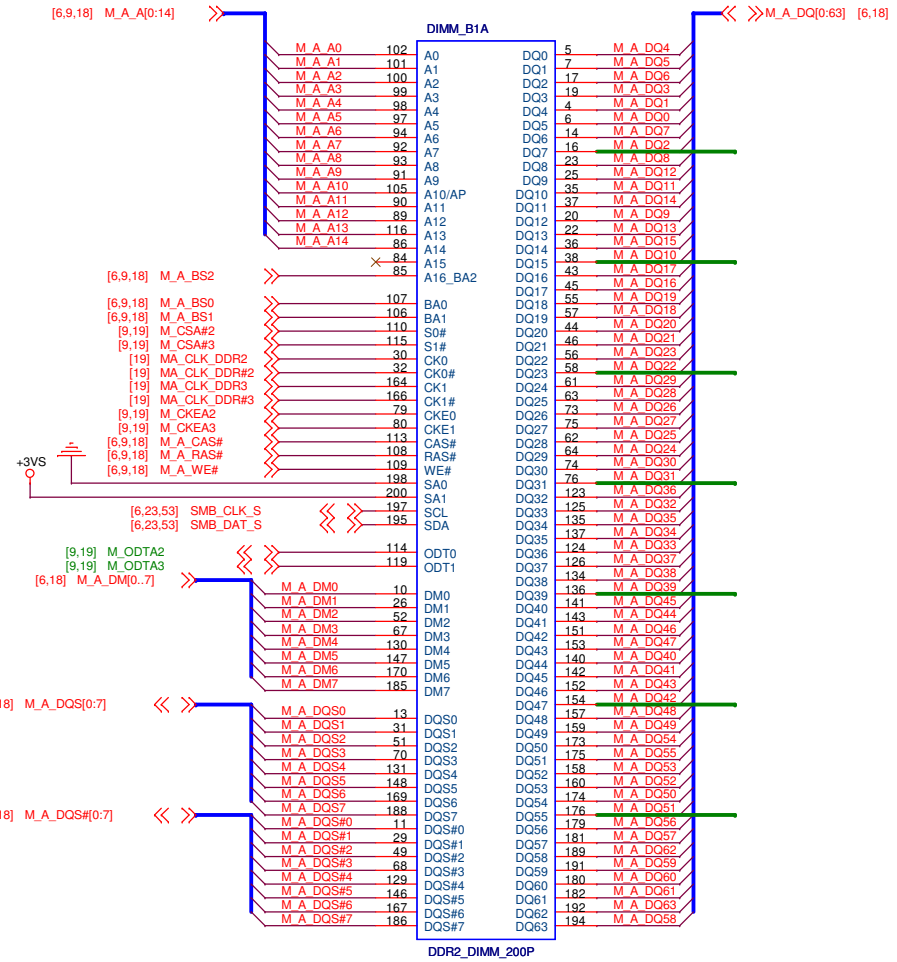
ASUSTeK COMPUTER INC. NB6

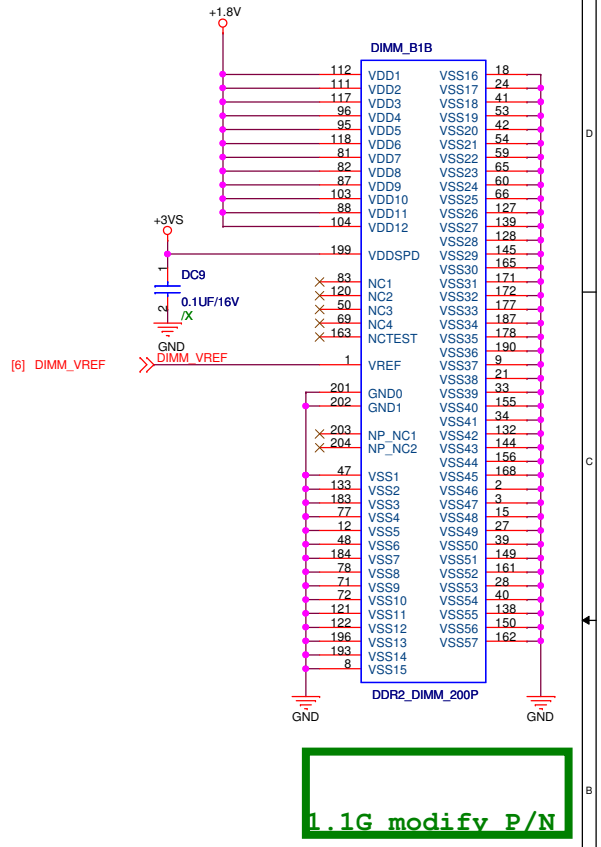
Title DDR3 SO-DIMM_0

Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 7 of 91





<Variant Name>

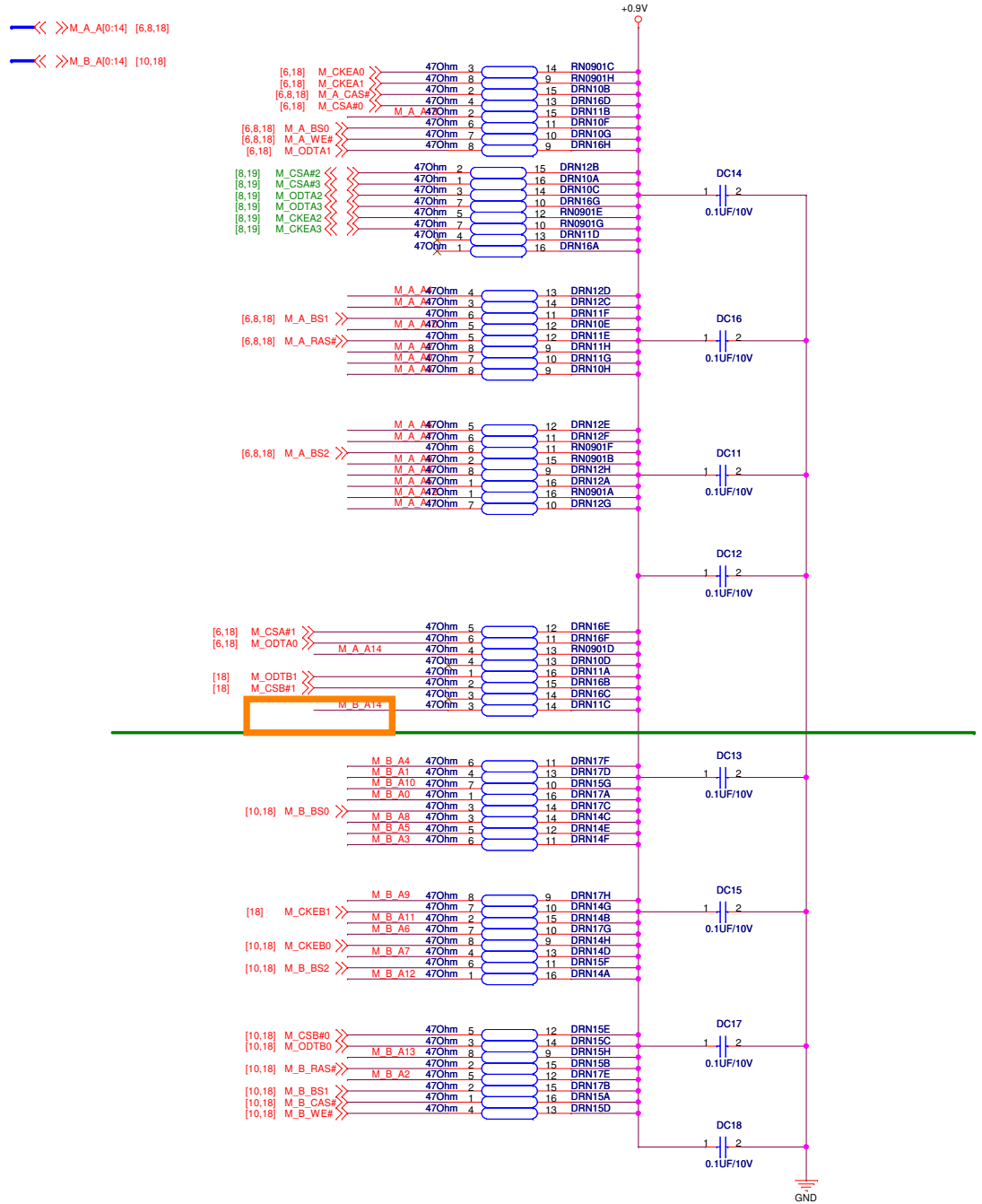
ASUSTeK COMPUTER INC. NB6

Title: DDR3 SO-DIMM_1

Engineer: Vincent Chung

Size	Project Name	Rev
B	G71V	1.0

Date: Friday, February 13, 2009 Sheet 8 of 91



<Variant Name>

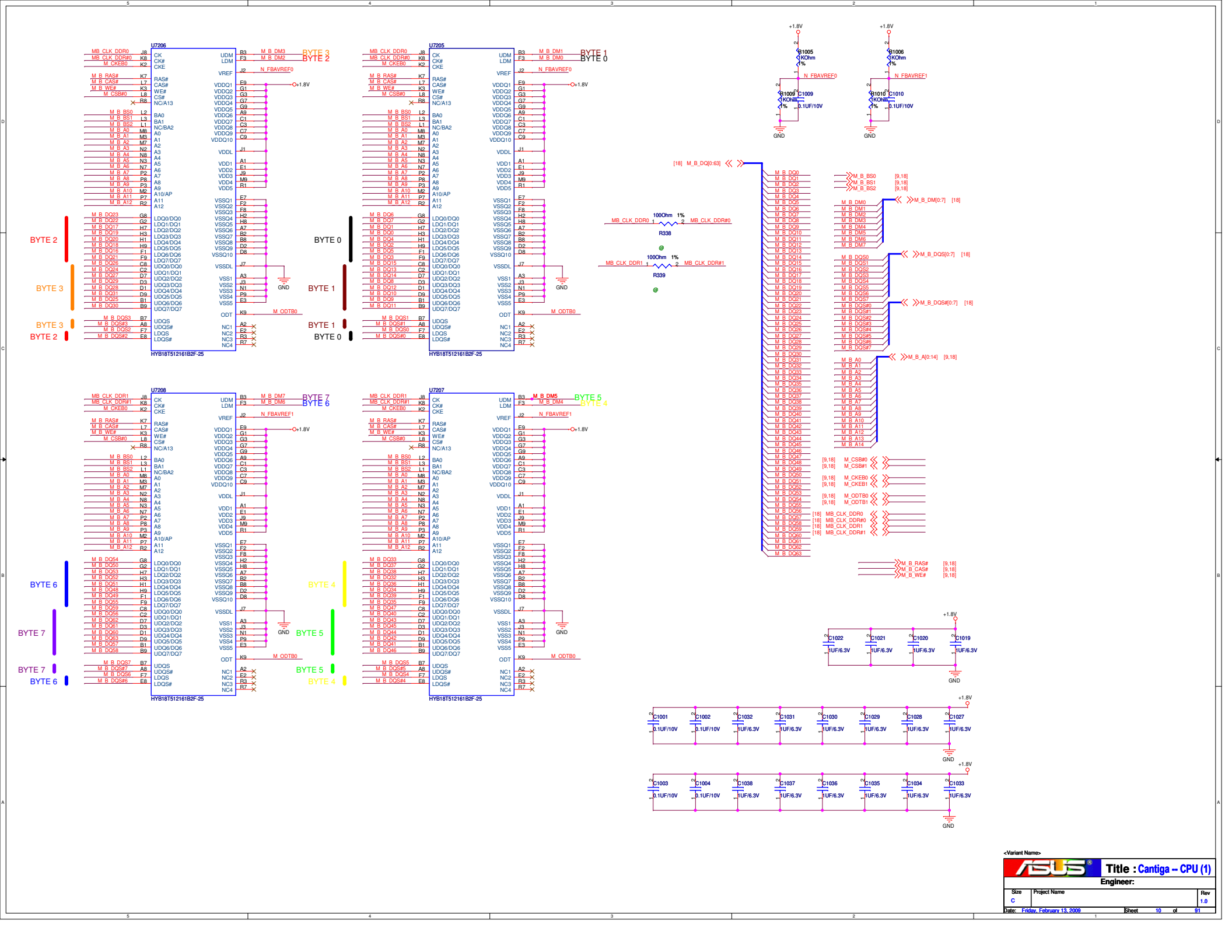
ASUSTeK COMPUTER INC. NB6

Title DDR3 termination

Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Monday, February 16, 2009 Sheet 9 of 91



<Variant Name>

Title : Cantiga – CPU (1)

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 10 of 91

<Variant Name>

Title : Cantiga-DDR3/PEG(2)

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 11 of 91

<Variant Name>

Title : Cantiga-DDR3 bus (3

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 12 of 91

<Variant Name>

Title : Cantiga--POWER (4)

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 13 of 91

<Variant Name>

Title : Cantiga-POWER(5)

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 14 of 91

<Variant Name>

Title : Cantiga-GND

Engineer:

Size	Project Name	Rev
B		1.0

Date: Friday, February 13, 2009 Sheet 15 of 91

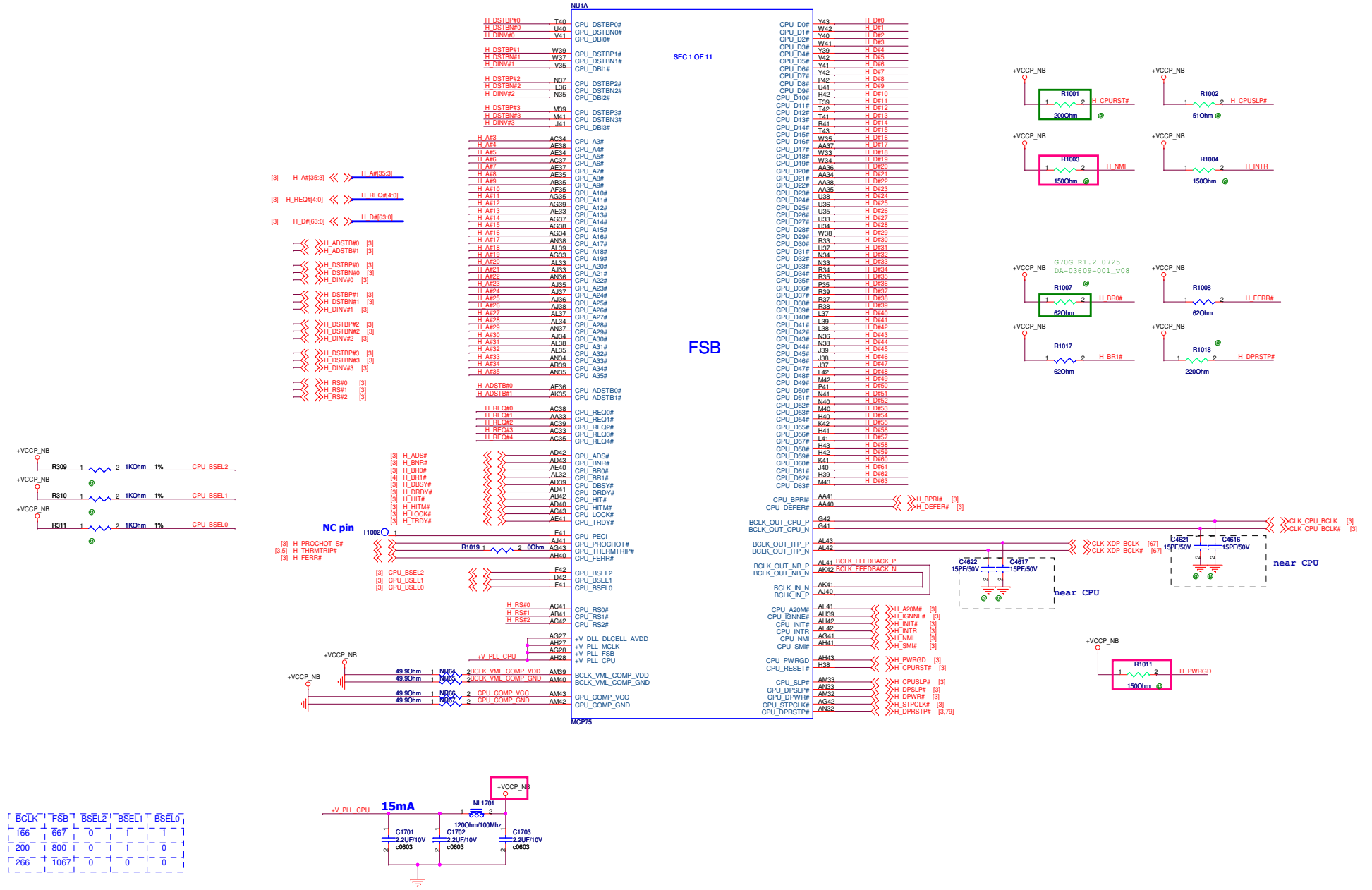
<Variant Name>

Title :

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 16 of 91


NU1A
FSB
SEC 1 OF 11
MCP75
NC pin
G70G R1.2 0725
DA-03609-001_v08
near CPU
near CPU
15mA
BCLK FSB BSEL2 BSEL1 BSEL0
166 667 0 1 1
200 800 0 1 0
266 1067 0 0 0
<Variant Name>
Title :
Engineer:
Size C
Project Name
Rev 1.0
Date: Friday, February 13, 2009
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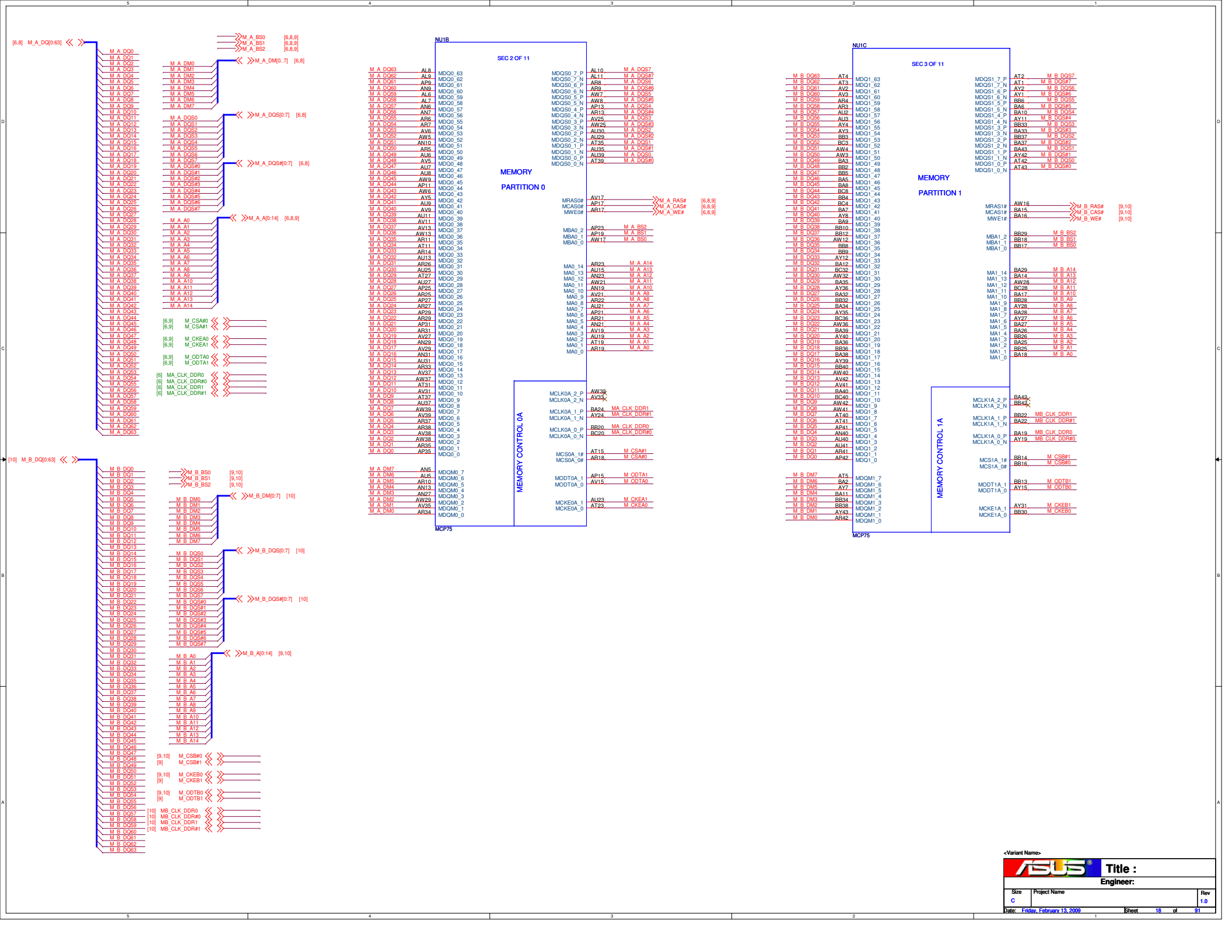


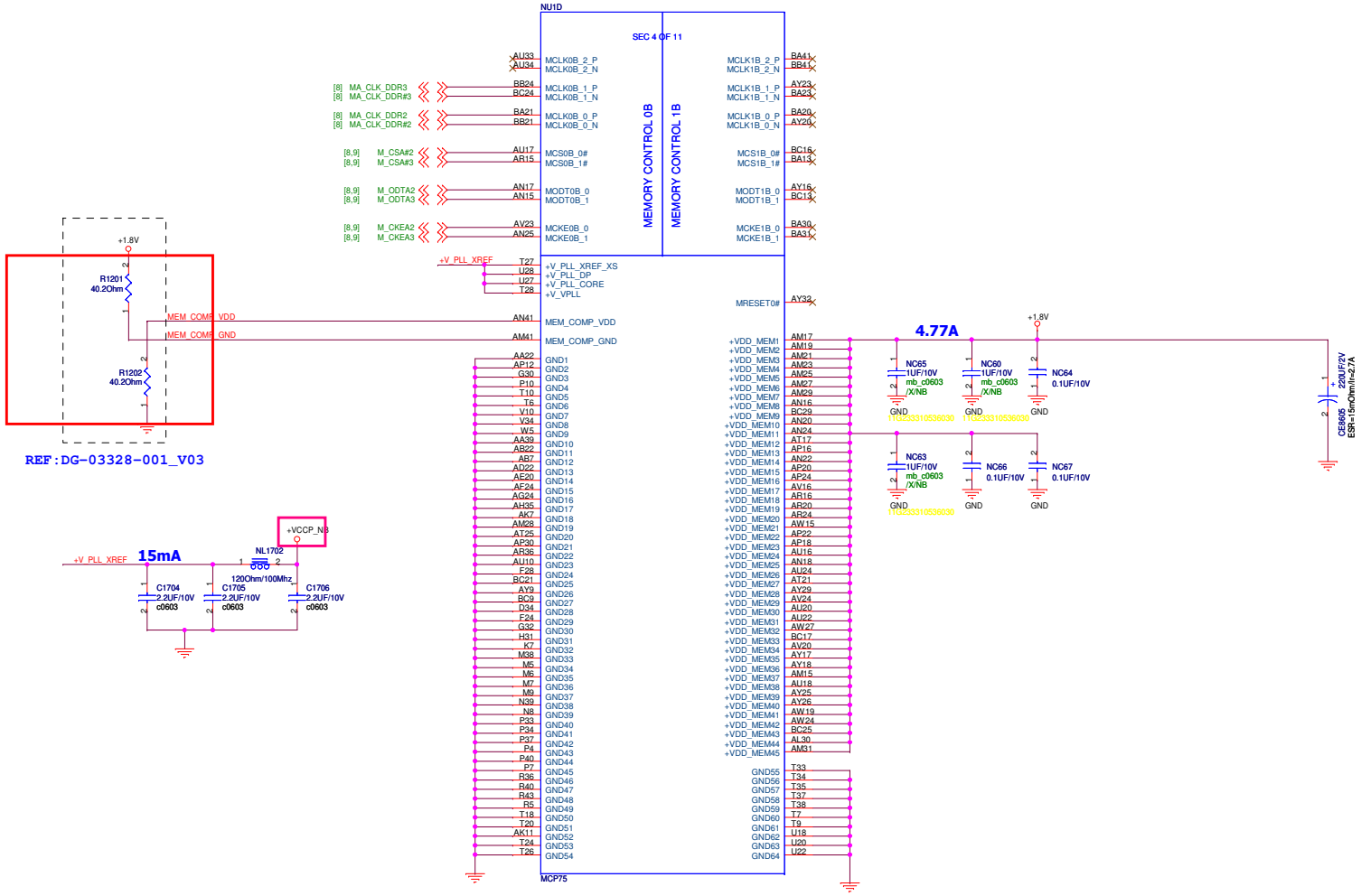
<variant_name>

Title :

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 18 of 91



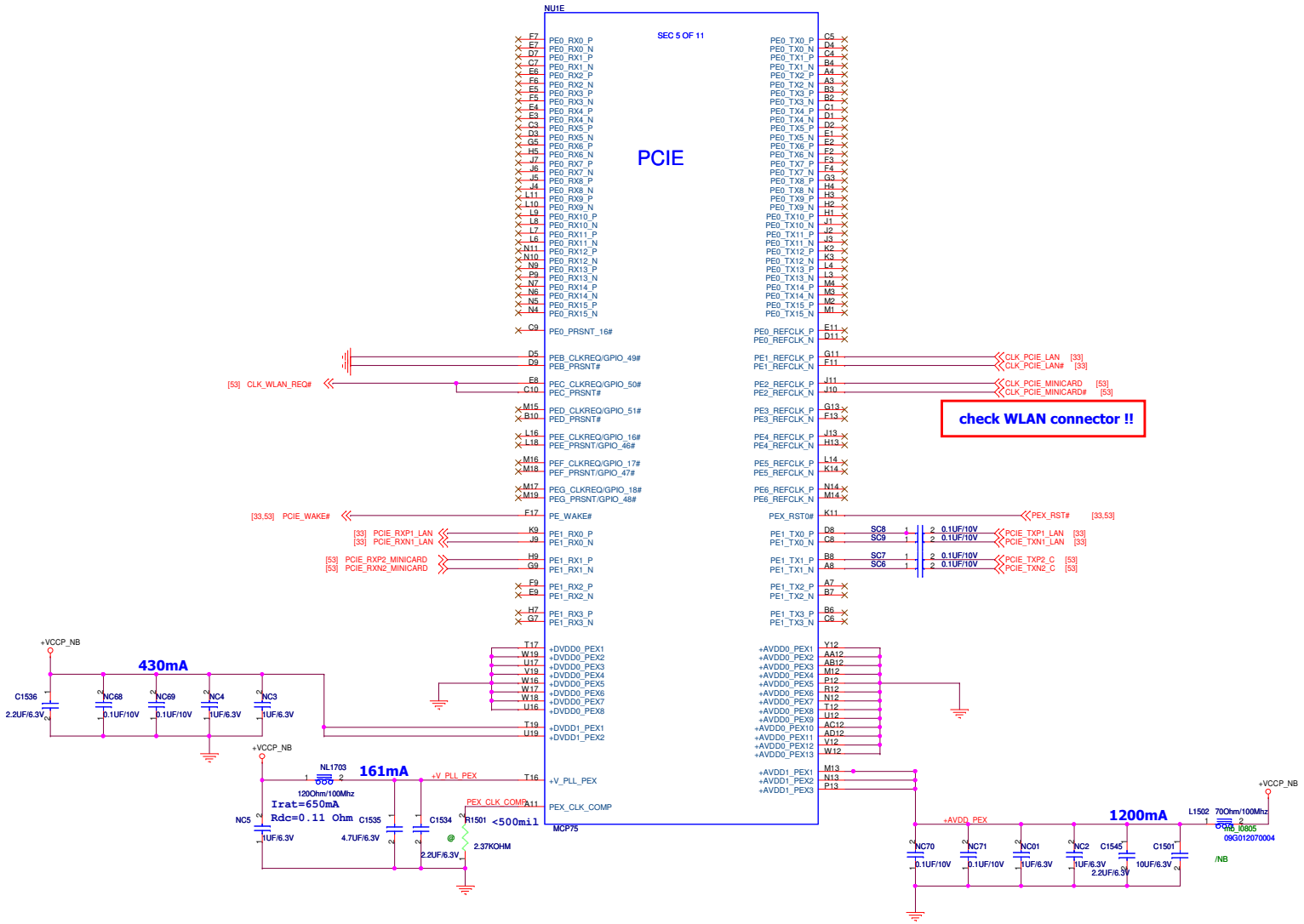
<Variant Name>

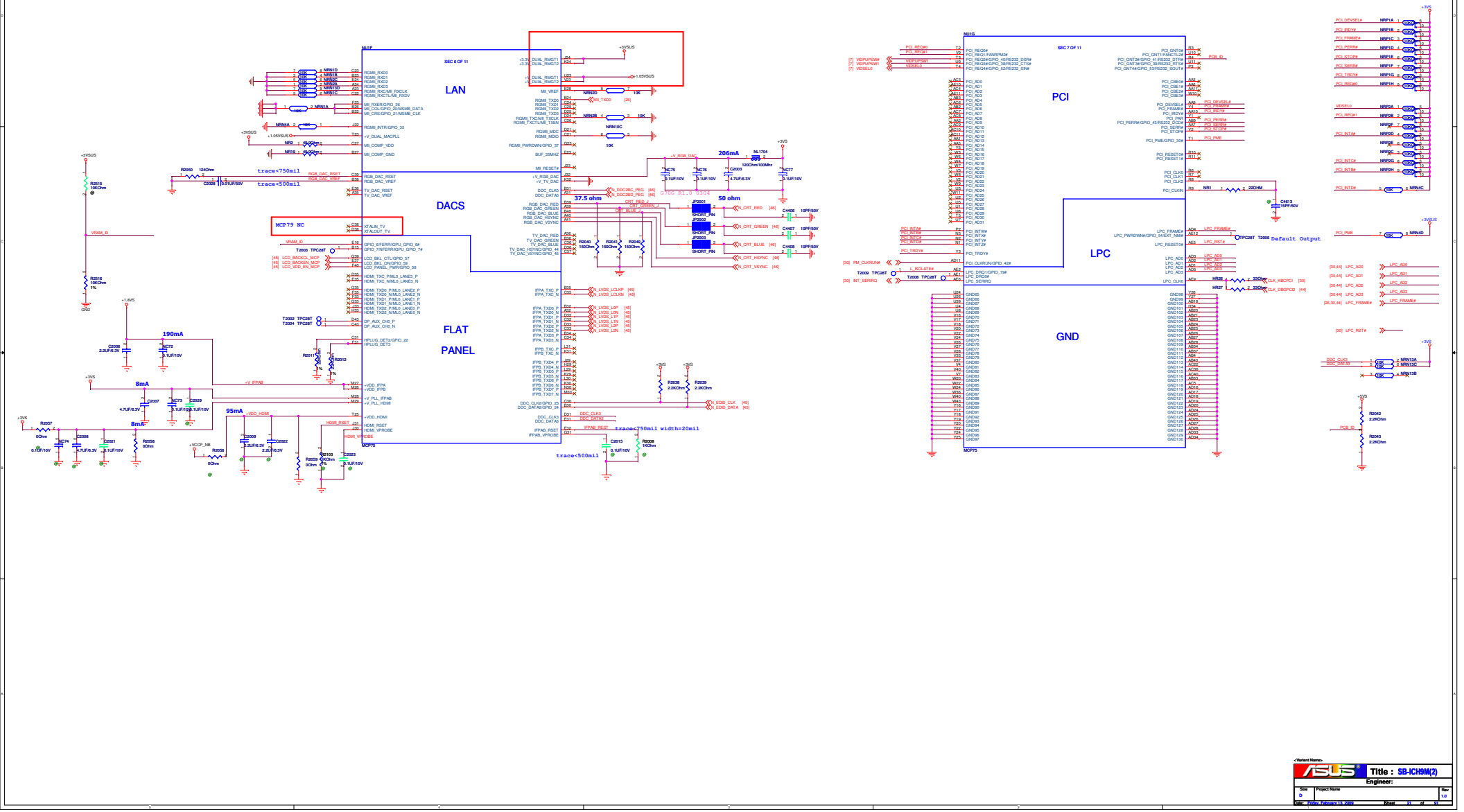
Title :

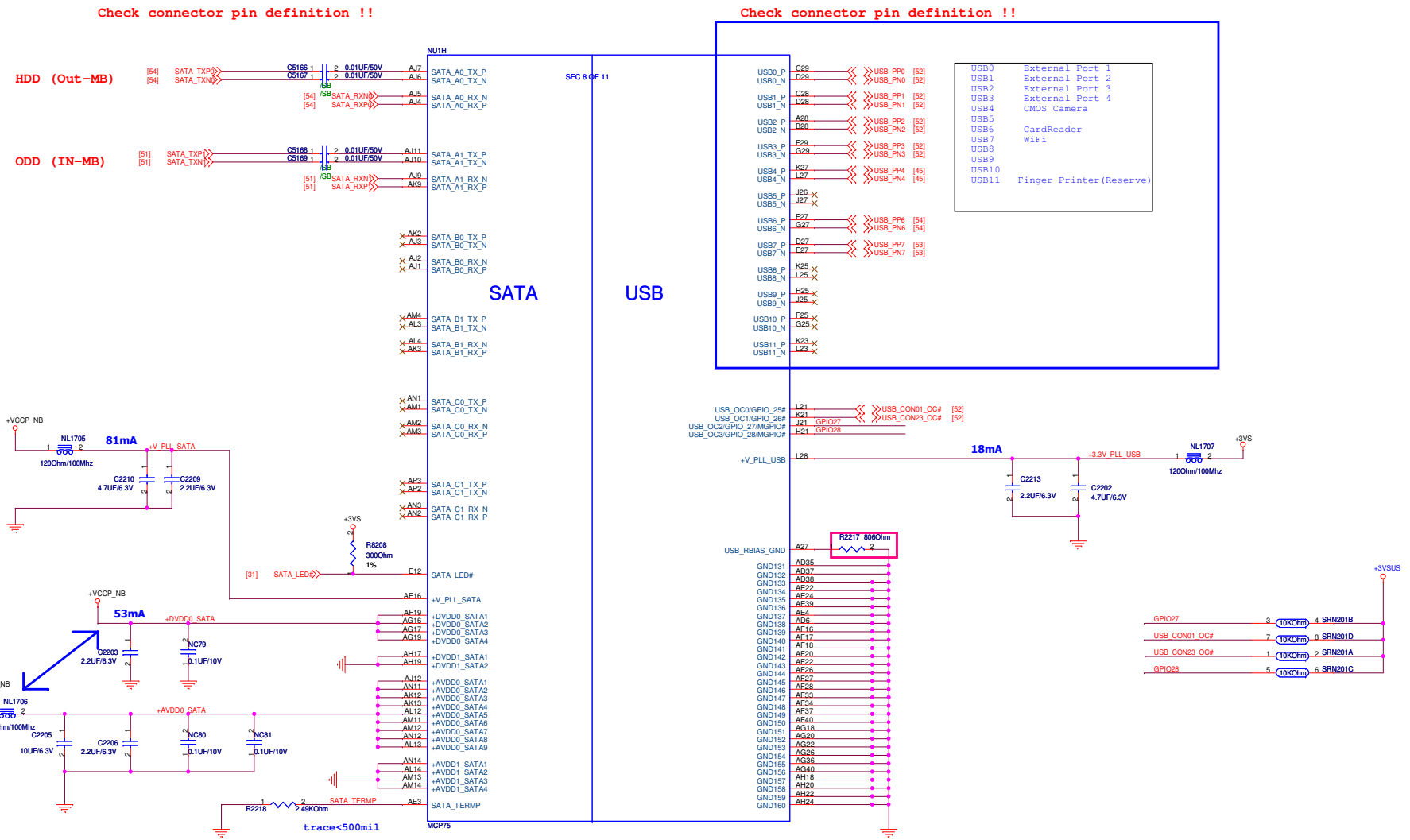
Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 19 of 91


NU1E
SEC 5 OF 11
PCIE
MCP75
check WLAN connector !!
430mA
161mA
1200mA
Irat=650mA
Rdc=0.11 Ohm
120Ohm/100Mhz
2.37KOHM
<500mil
09G012070004
/NB


LAN
DACS
FLAT
PANEL
PCI
LPC
GND
SEC 6 OF 11
SEC 7 OF 11
NU1F
NU1G
MCP79 NC
190mA
8mA
95mA
206mA
37.5 ohm
50 ohm
trace<750mil
trace<500mil
trace<750mil width=20mil
Default Output
SB-ICH9M(2)



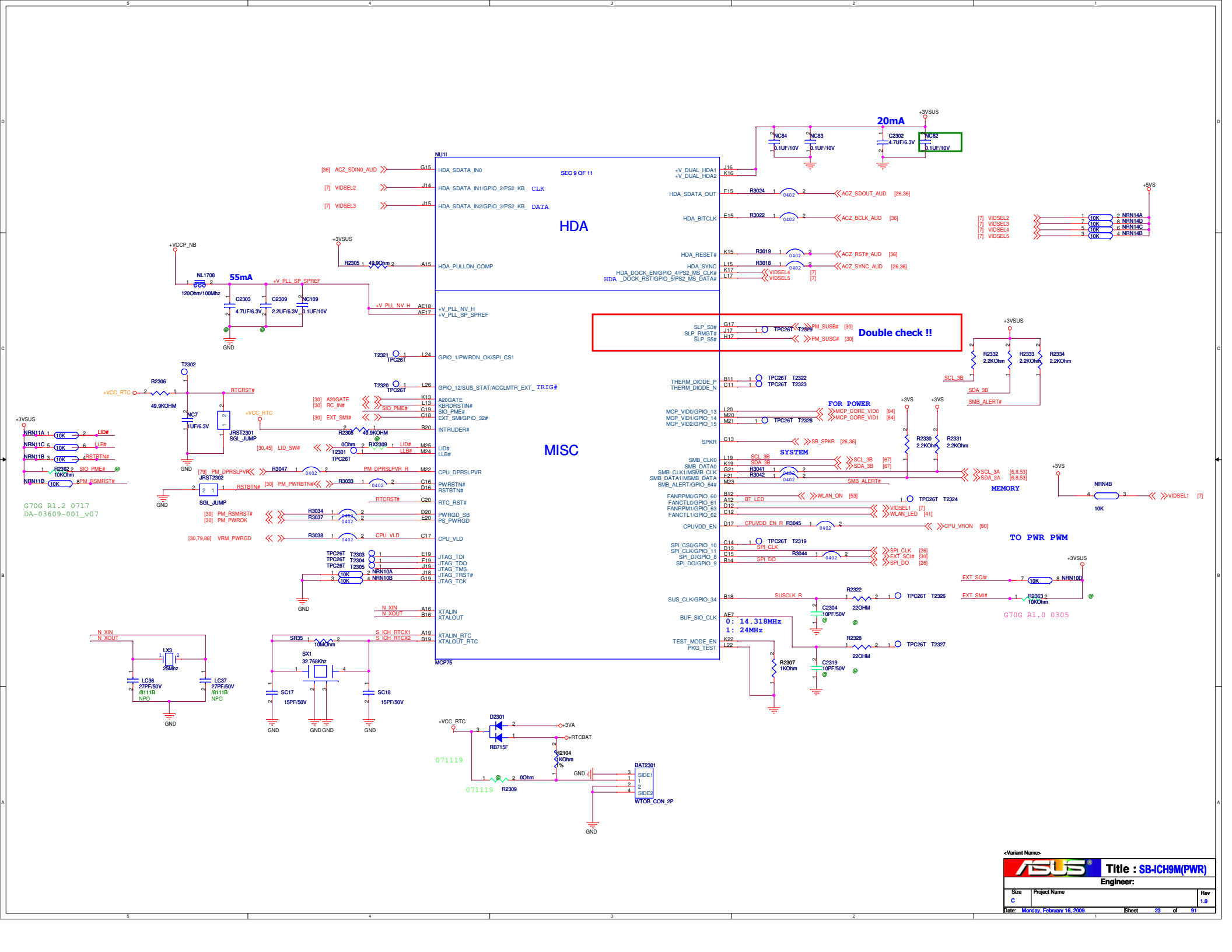
<Variant Name>

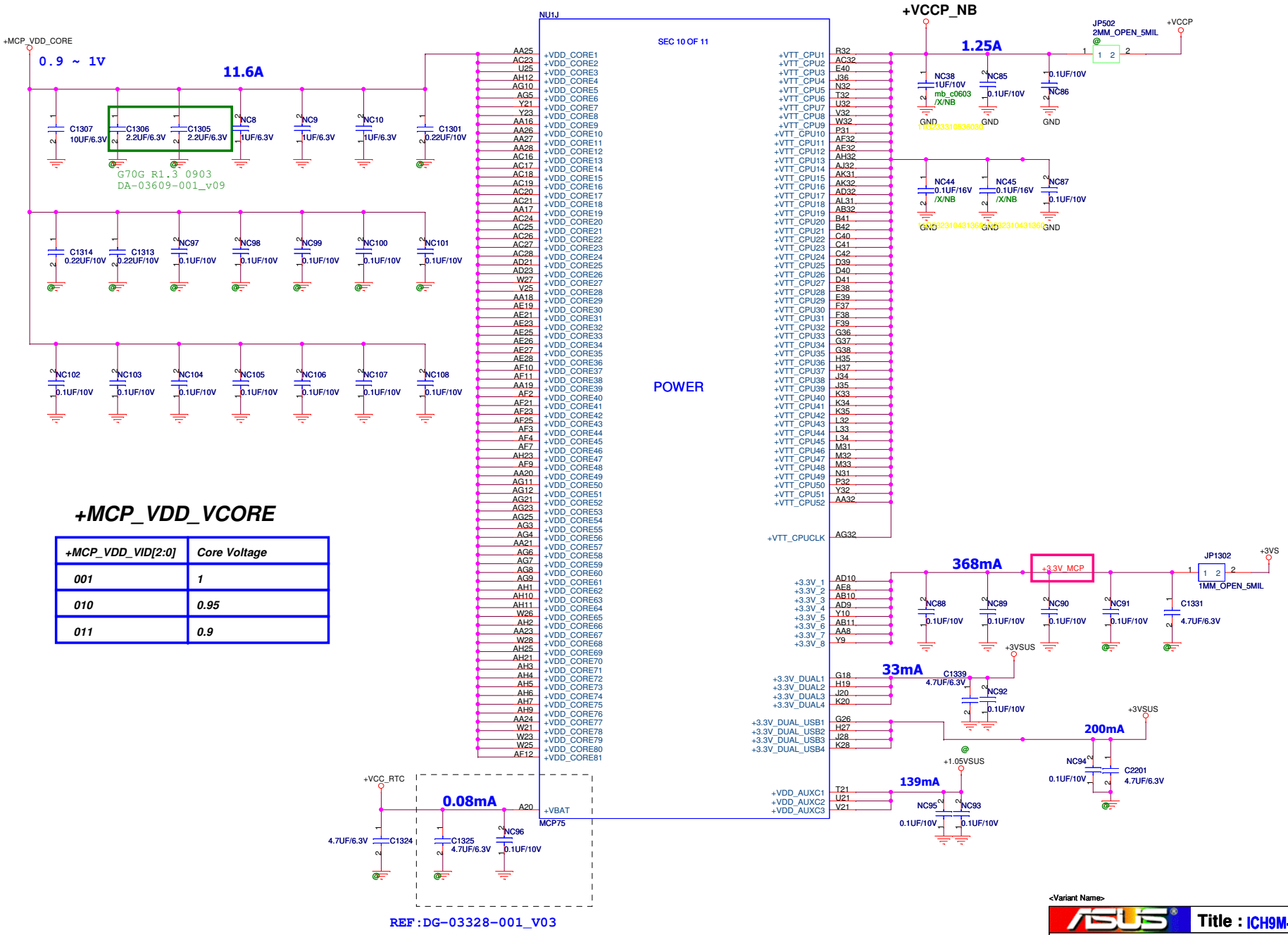
Title : SB-ICH9M(3)

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 22 of 91


NU11
HDA
SEC 9 OF 11
MISC
MCP75
HDA_SDATA_IN0
HDA_SDATA_IN1/GPIO_2/PS2_KB_ CLK
HDA_SDATA_IN2/GPIO_3/PS2_KB_ DATA
HDA_PULLDN_COMP
+V_PLL_NV_H
+V_PLL_SP_SPREF
GPIO_1/PWRDN_OK/SPI_CS1
GPIO_12/SUS_STAT/ACCLMTR_EXT_ TRIG#
A20GATE
KBRDRSTIN#
SIO_PME#
EXT_SMI/GPIO_32#
INTRUDER#
LID#
LLB#
CPU_DPRSLPVR
PWRBTN#
RSTBTN#
RTC_RST#
PWRGD_SB
PS_PWRGD
CPU_VLD
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST#
JTAG_TCK
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
+V_DUAL_HDA1
+V_DUAL_HDA2
HDA_SDATA_OUT
HDA_BITCLK
HDA_RESET#
HDA_SYNC
HDA_DOCK_EN/GPIO_4/PS2_MS_CLK#
HDA _DOCK_RST/GPIO_5/PS2_MS_DATA#
SLP_S3#
SLP_RMGT#
SLP_S5#
THERM_DIODE_P
THERM_DIODE_N
MCP_VID0/GPIO_13
MCP_VID1/GPIO_14
MCP_VID2/GPIO_15
SPKR
SMB_CLK0
SMB_DATA0
SMB_CLK1/MSMB_CLK
SMB_DATA1/MSMB_DATA
SMB_ALERT/GPIO_64#
FANRPM0/GPIO_60
FANCTL0/GPIO_61
FANRPM1/GPIO_63
FANCTL1/GPIO_62
CPUVDD_EN
SPI_CS0/GPIO_10
SPI_CLK/GPIO_11
SPI_DI/GPIO_8
SPI_DO/GPIO_9
SUS_CLK/GPIO_34
BUF_SIO_CLK
TEST_MODE_EN
PKG_TEST
20mA
55mA
Double check !!
FOR POWER
SYSTEM
MEMORY
TO PWR PWM
0: 14.318MHz
1: 24MHz
G70G R1.2 0717
DA-03609-001_v07
G70G R1.0 0305
071119
071119
+3VSUS
+VCCP_NB
+VCC_RTC
+3VS
+5VS
+3VA
+RTCBAT
GND
RTCRST#
SIO_PME#
LID#
RSTBTN#
PM_RSMRST#
PM_PWROK
VRM_PWRGD
CPU_VLD
PM_DPRSLPVR
PM_PWRBTN#
N_XIN
N_XOUT
S_ICH_RTCX1
S_ICH_RTCX2
SUSCLK_R
SMB_ALERT#
SCL_3B
SDA_3B
WLAN_ON
BT_LED
SPI_CLK
SPI_DO
CPUVDD_EN_R
CPU_VRON
EXT_SCI#
EXT_SMI#
VIDSEL1
VIDSEL2
VIDSEL3
VIDSEL4
VIDSEL5
ACZ_SDOUT_AUD
ACZ_BCLK_AUD
ACZ_RST#_AUD
ACZ_SYNC_AUD
SB_SPKR
MCP_CORE_VID0
MCP_CORE_VID1
WTOB_CON_2P
RB715F
BAT2301
NL1708
LX3
25Mhz
SX1
32.768Khz
JRST2301
SGL_JUMP
JRST2302
SGL_JUMP
NRN11A
NRN11C
NRN11B
NRN11D
NRN4B
NRN10A
NRN10B
NRN10D
NRN14A
NRN14D
NRN14C
NRN14B
TPC26T
T2321
T2320
T2322
T2323
T2328
T2329
T2324
T2326
T2327
T2319
T2303
T2304
T2305
T2301
R2306
R2308
R2309
R2104
R2305
R3024
R3022
R3019
R3018
R3041
R3042
R3045
R3044
R2322
R2328
R2307
R2330
R2331
R2332
R2333
R2334
R3047
R3033
R3034
R3037
R3038
R2362
R2363
C2303
C2309
NC109
NC84
NC83
C2302
NC82
C2304
C2319
NC7
LC36
LC37
SC17
SC18
SR35
D2301
Title : SB-ICH9M(PWR)
Engineer:
Size C
Project Name
Rev 1.0
Date: Monday, February 16, 2009
Sheet 23 of 91
<Variant Name>



+MCP_VDD_VCORE

+MCP_VDD_VID[2:0]	Core Voltage
001	1
010	0.95
011	0.9

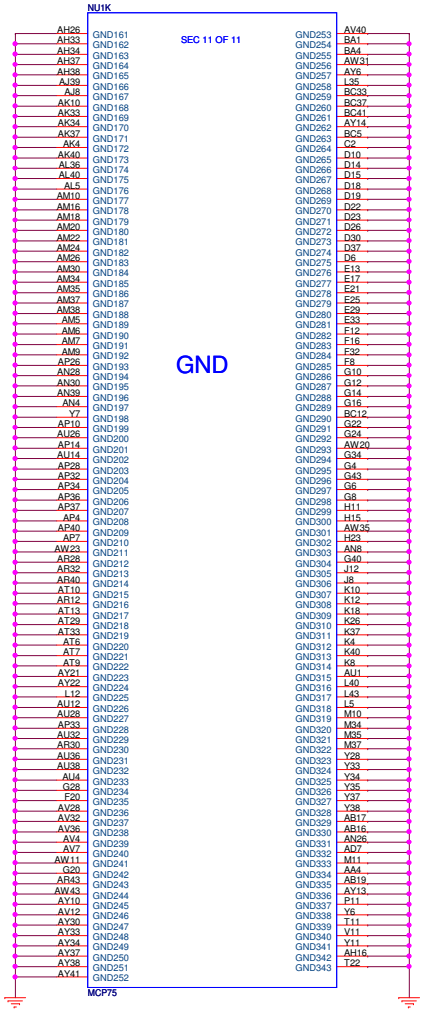
<variant_name>

Title : ICH9M-Other

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 24 of 91



<Variant Name>

Title : SPI ROM

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 25 of 91

[6,8,23,53] SCL_3A

SMB_CLK_S [6,8,23,53]

[6,8,23,53] SDA_3A

SMB_DAT_S [6,8,23,53]

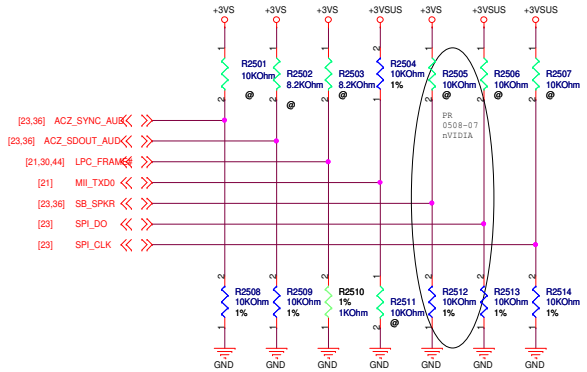
Onboard DRAM ID

GPIO_6	GPIO_11	Vendor
0	0	Qimonda HYB18T512161B2F-25
0	1	Samsung K4N51163QZ-HC25
1	0	Hynix HY5PS121621CFP-25

HDA_SYNC STRAP (BUF_SIO_CLK)	
0	14.318MHz (default)
1	24MHz

RGMII_TXD0	
0	MII
1	RGMII

SPKR	
0	User mode boot Init table
1	Safe mode boot Init table



Base on EC

HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz

<Variant Name>

Title :

Engineer:

Size	Project Name	Rev
C		1.0

Date: Monday, February 16, 2009 Sheet 26 of 91

<Variant Name>

Title :

ASUSTeK COMPUTER INC. NB6

Engineer: Vincent Chung

Size	Project Name	Rev
C	G71V	1.0

Date: Friday, February 13, 2009 Sheet 27 of 91

<Variant Name>

Title : Main Clock-1

ASUSTek Computer Inc.

Engineer: Tyson Lin

Size	Project Name	Rev
Custom	C90P	1.0G

Date: Friday, February 13, 2009 Sheet 28 of 91

<Variant Name>

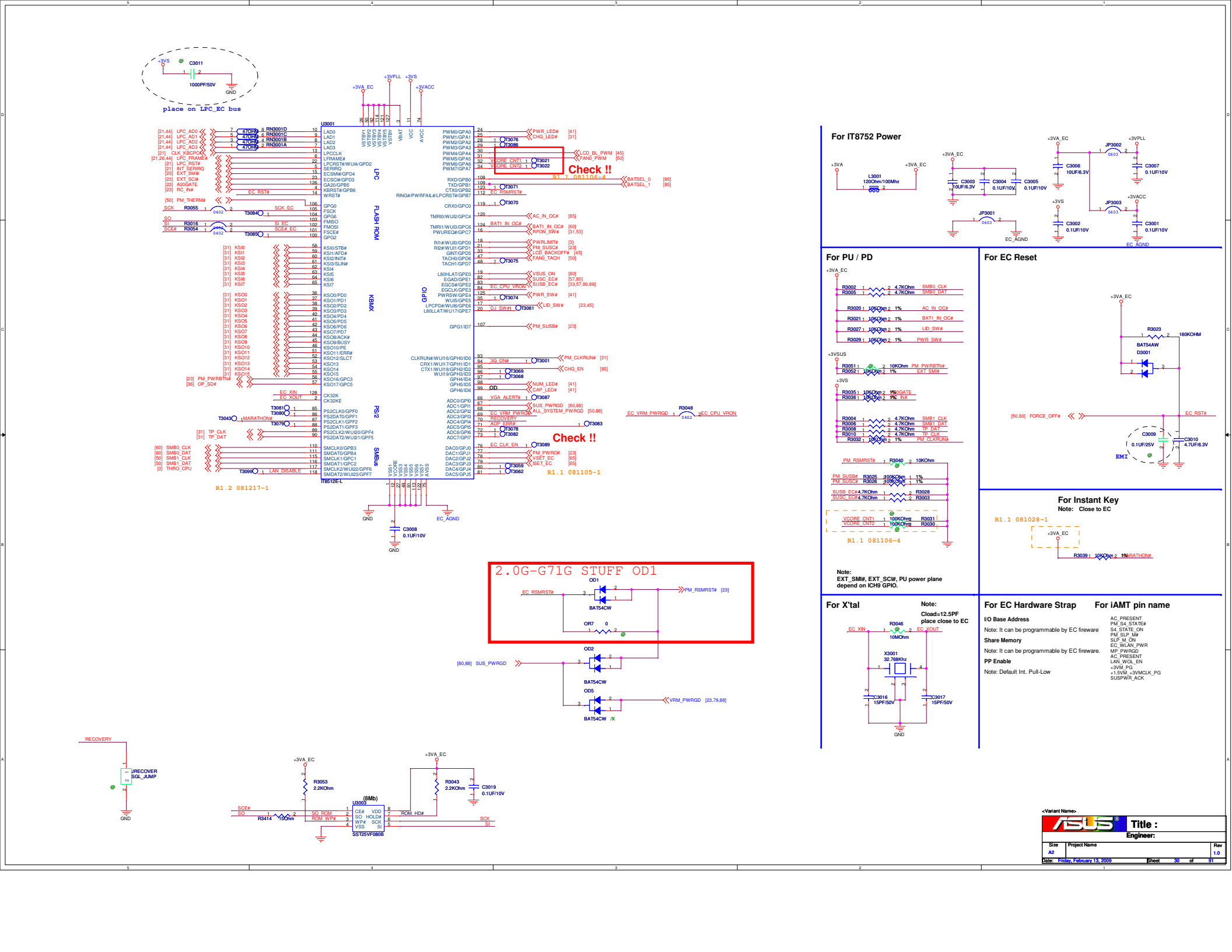
ASUSTek Computer Inc.

Title : Main Clock-2

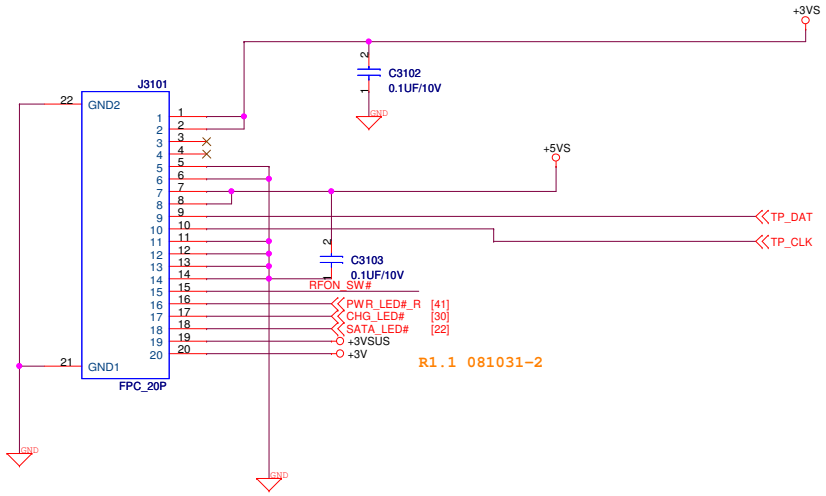
Engineer: Tony Kao

Size	Project Name	Rev
A2	C90P	1.0G

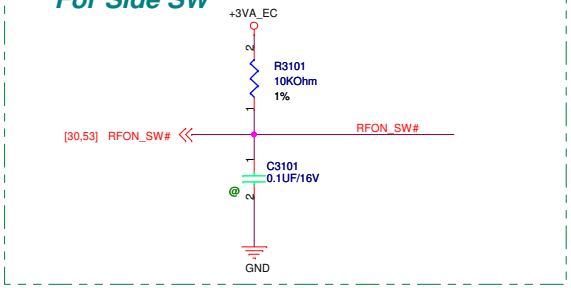
Date: Friday, February 13, 2009 Sheet 29 of 91


place on LPC_EC bus
C3011
1000PF/50V
GND
U3001
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
R1.2 081217-1
R1.1 081106-4
R1.1 081105-1
Check !!
Check !!
2.0G-G71G STUFF OD1
OD1
BAT54CW
OR7 0
OD2
BAT54CW
OD5
BAT54CW
For IT8752 Power
L3001 120Ohm/100Mhz
C3003 10UF/6.3V
C3004 0.1UF/10V
C3005 0.1UF/10V
JP3001
C3006 10UF/6.3V
C3007 0.1UF/10V
C3002 0.1UF/10V
C3001 0.1UF/10V
JP3002
JP3003
EC_AGND
For PU / PD
For EC Reset
R3023 160KOHM
BAT54AW
D3001
C3009 0.1UF/25V
C3010 4.7UF/6.3V
EM1
For Instant Key
Note: Close to EC
R1.1 081028-1
For X'tal
Note:
Cload=12.5PF
place close to EC
X3001 32.768Khz
C3016 15PF/50V
C3017 15PF/50V
R3046 10MOhm
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH9 GPIO.
RECOVERY
JRECOVER
SGL_JUMP
R3053 2.2KOhm
R3043 2.2KOhm
C3019 0.1UF/10V
U3003 (8Mb)
SST25VF080B
R3414 10Ohm
<Variant Name>
Title :
Engineer:
Size A2
Project Name
Rev 1.0
Date: Friday, February 13, 2009
Sheet 30 of 91

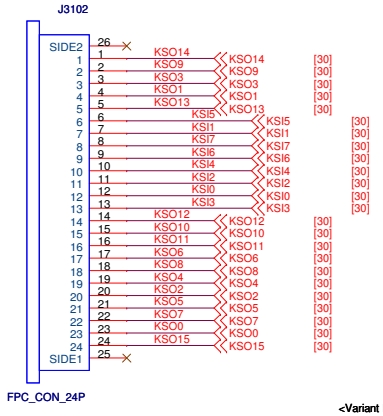
TouchPad & FingerPrint

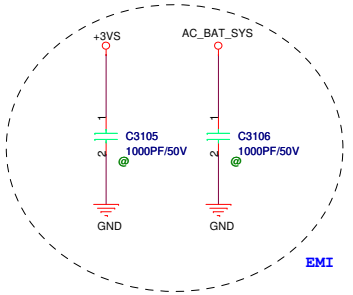


For Side SW



Keyboard Connector





For Thermal Control Method

Remove redundant components

<Variant Name>

Title : EC_IT8511 (2/2)

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 31 of 91

Main Board

<Variant Name>

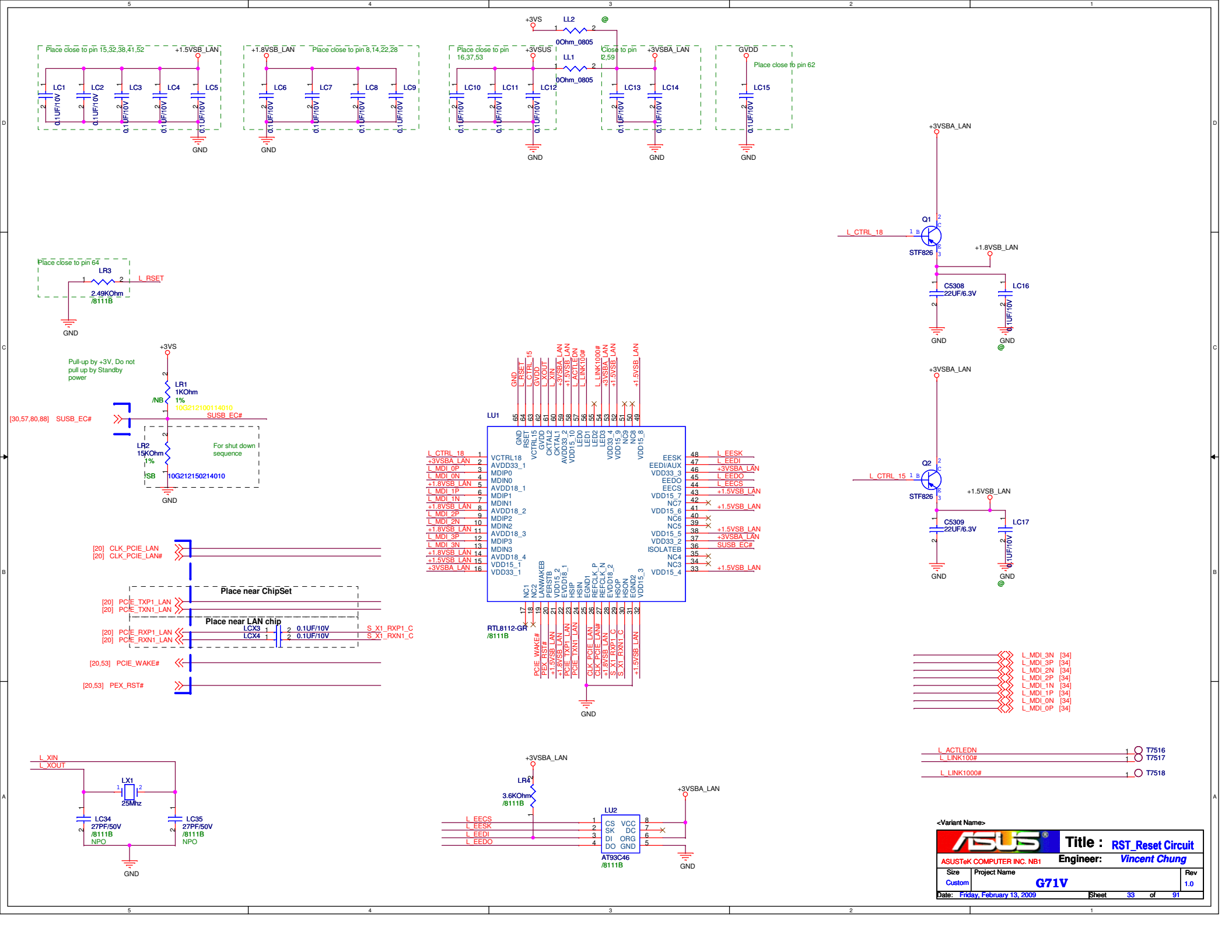
Title : RST_Reset Circuit

ASUSTeK COMPUTER INC. NB1

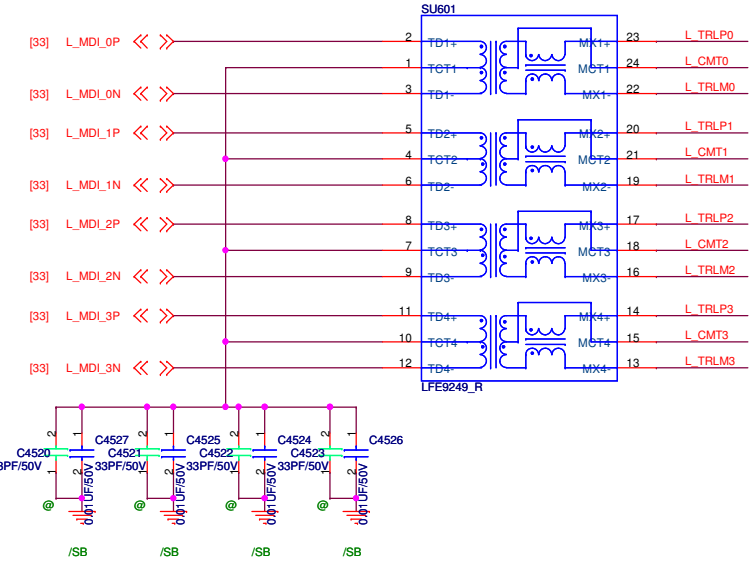
Engineer: Vincent Chung

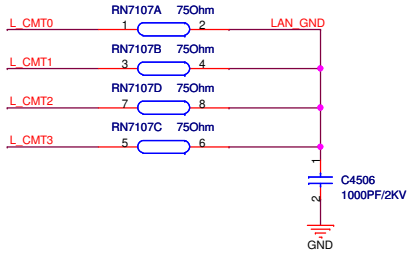
Size	Project Name	Rev
Custom	G71V	1.0

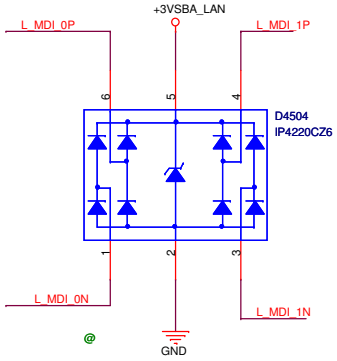
Date: Friday, February 13, 2009 Sheet 32 of 91

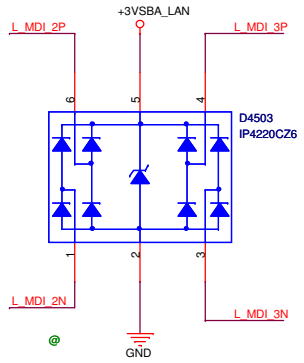

Place close to pin 15,32,38,41,52
+1.5VSB_LAN
LC1 LC2 LC3 LC4 LC5
0.1UF/10V
GND
+1.8VSB_LAN
Place close to pin 8,14,22,28
LC6 LC7 LC8 LC9
+3VS
LL2
0Ohm_0805
Place close to pin 16,37,53
+3VSUS
LL1
0Ohm_0805
Close to pin 2,59
+3VSBA_LAN
LC10 LC11 LC12 LC13 LC14
GVDD
Place close to pin 62
LC15
Place close to pin 64
LR3
2.49KOhm /8111B
L_RSET
Pull-up by +3V, Do not pull up by Standby power
LR1
1KOhm 1%
/NB
10G212100114010
SUSB_EC#
[30,57,80,88] SUSB_EC#
LR2
15KOhm 1%
/SB
10G212150214010
For shut down sequence
LU1
RTL8112-GR /8111B
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
MDIP2
MDIN2
AVDD18_3
MDIP3
MDIN3
AVDD18_4
VDD15_1
VDD33_1
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
VDD15_7
NC7
VDD15_6
NC6
NC5
VDD15_5
VDD33_2
ISOLATEB
NC4
NC3
VDD15_4
L_CTRL_18
+3VSBA_LAN
L_MDI_0P
L_MDI_0N
+1.8VSB_LAN
L_MDI_1P
L_MDI_1N
+1.8VSB_LAN
L_MDI_2P
L_MDI_2N
+1.8VSB_LAN
L_MDI_3P
L_MDI_3N
+1.8VSB_LAN
+1.5VSB_LAN
+3VSBA_LAN
L_EESK
L_EEDI
+3VSBA_LAN
L_EEDO
L_EECS
+1.5VSB_LAN
+1.5VSB_LAN
+1.5VSB_LAN
+3VSBA_LAN
SUSB_EC#
+1.5VSB_LAN
[20] CLK_PCIE_LAN
[20] CLK_PCIE_LAN#
Place near ChipSet
[20] PCIE_TXP1_LAN
[20] PCIE_TXN1_LAN
Place near LAN chip
LCX3 LCX4 0.1UF/10V
[20] PCIE_RXP1_LAN
[20] PCIE_RXN1_LAN
S_X1_RXP1_C
S_X1_RXN1_C
[20,53] PCIE_WAKE#
[20,53] PEX_RST#
L_XIN
L_XOUT
LX1
25Mhz
LC34 LC35
27PF/50V /8111B NPO
LR4
3.6KOhm /8111B
LU2
AT93C46 /8111B
CS VCC
SK DC
DI ORG
DO GND
L_EECS
L_EESK
L_EEDI
L_EEDO
Q1
STF826
L_CTRL_18
C5308 22UF/6.3V
LC16
Q2
L_CTRL_15
C5309 22UF/6.3V
LC17
L_MDI_3N [34]
L_MDI_3P [34]
L_MDI_2N [34]
L_MDI_2P [34]
L_MDI_1N [34]
L_MDI_1P [34]
L_MDI_0N [34]
L_MDI_0P [34]
L_ACTLEDN
L_LINK100#
L_LINK1000#
T7516
T7517
T7518
<Variant Name>
Title : RST_Reset Circuit
ASUSTeK COMPUTER INC. NB1
Engineer: Vincent Chung
Size Custom
Project Name G71V
Rev 1.0
Date: Friday, February 13, 2009
Sheet 33 of 91

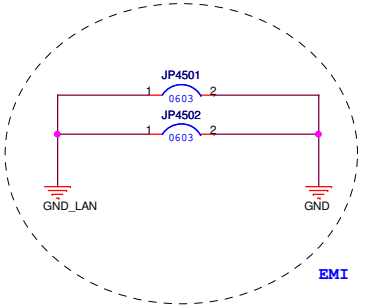
LAN CONN.

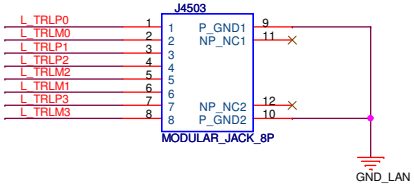












<Variant Name>

ASUSTeK COMPUTER INC	Title : IO Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 34 of 91	

<Variant Name>

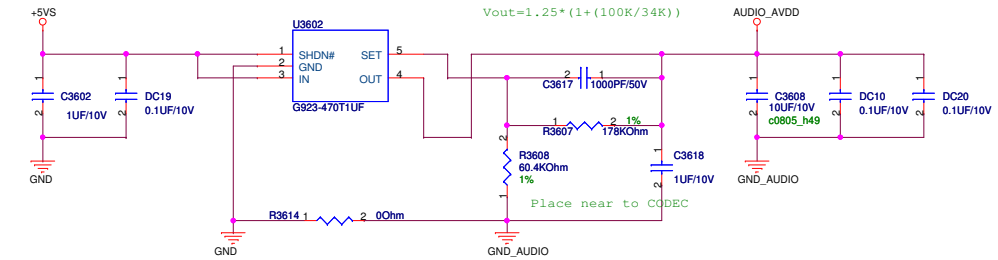
Title : MDC

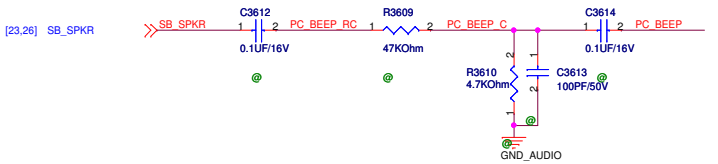
ASUSTeK COMPUTER INC

Engineer: Vincent Chung

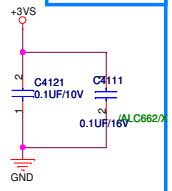
Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 35 of 91

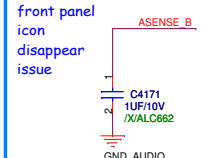




DVDD



Reserved
front panel
icon
disappear
issue



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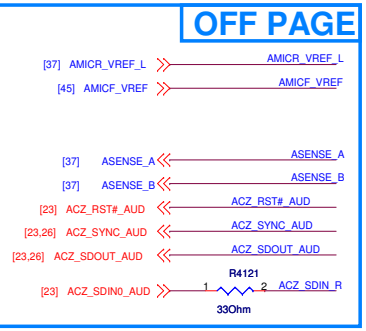
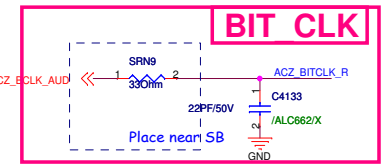
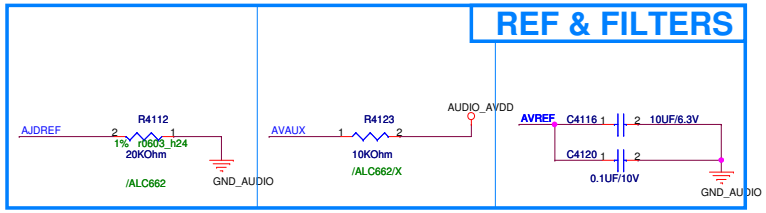


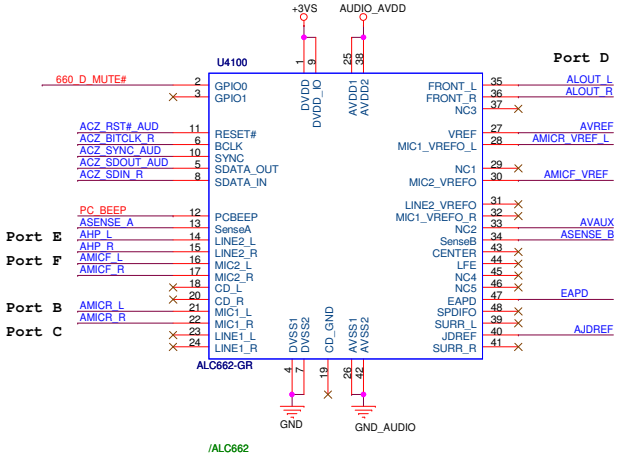
BIT_CLK



REF & FILTERS

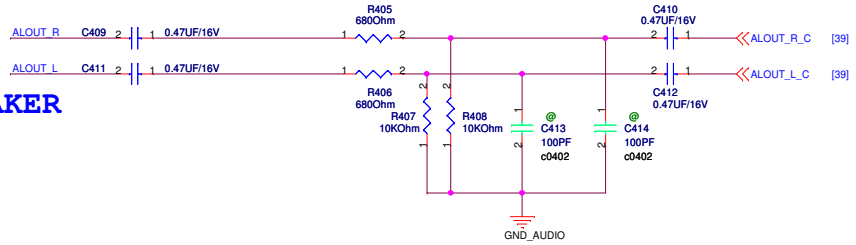


CODEC ALC662



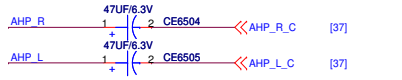
SPEAKER

Port D



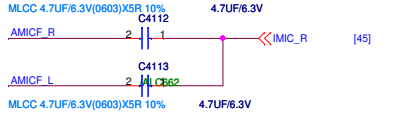
HP CONN

Port E



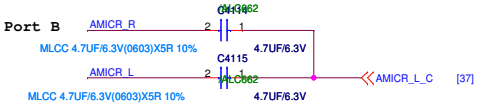
Internal Mic

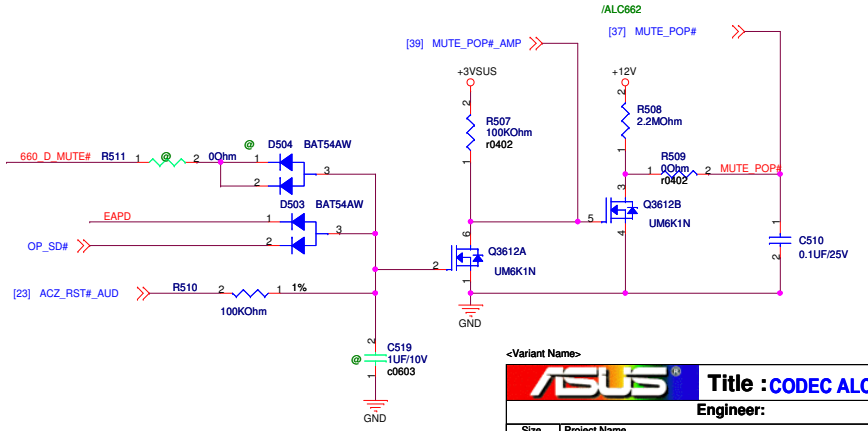
Port F



External Mic

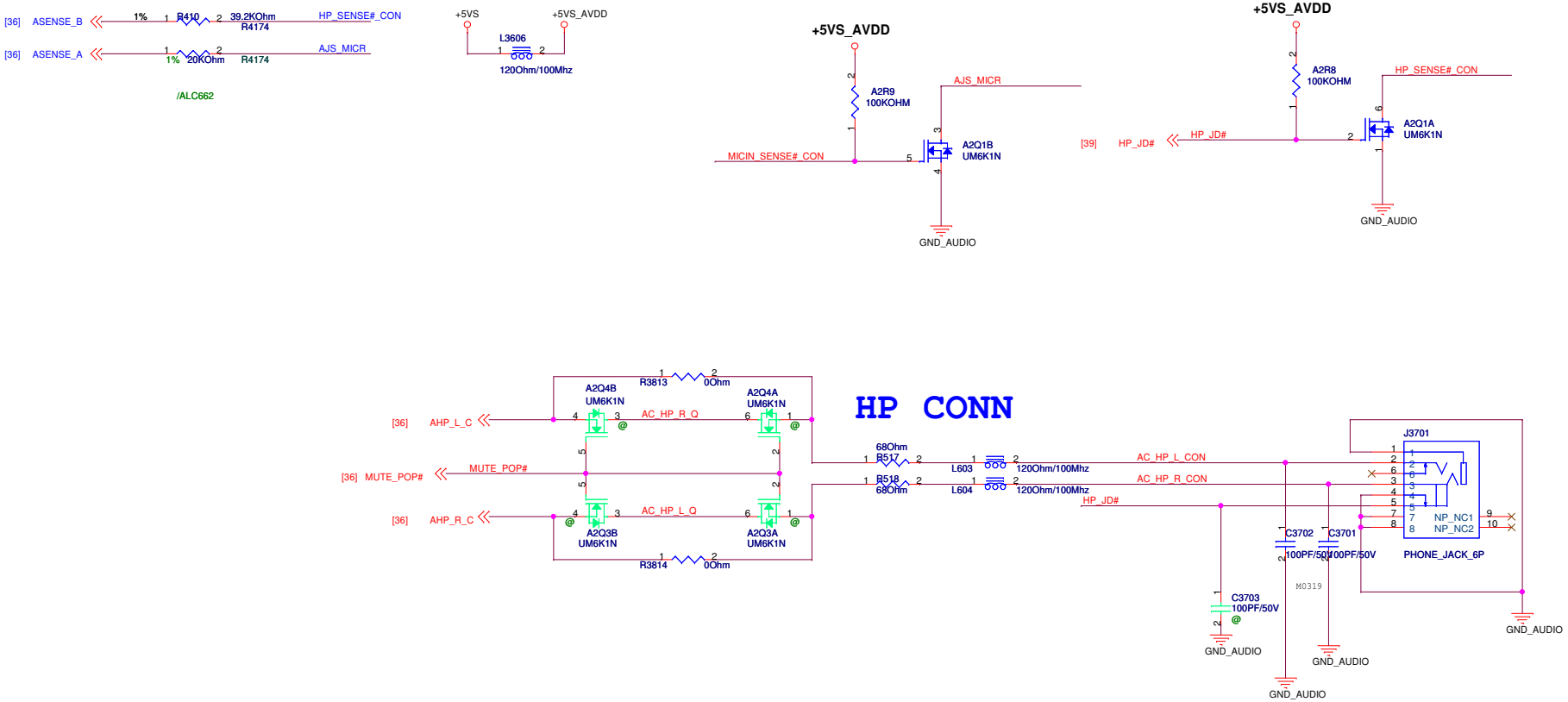
Port B





<Variant Name>

ASUS	Title : CODEC ALC662	
	Engineer:	
Size: Custom	Project Name	Rev: 1.1
Date: Friday, February 13, 2009	Sheet 36 of 91	



<Variant Name>

Title : AUD_Amp & Jack

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 37 of 91

<Variant Name>

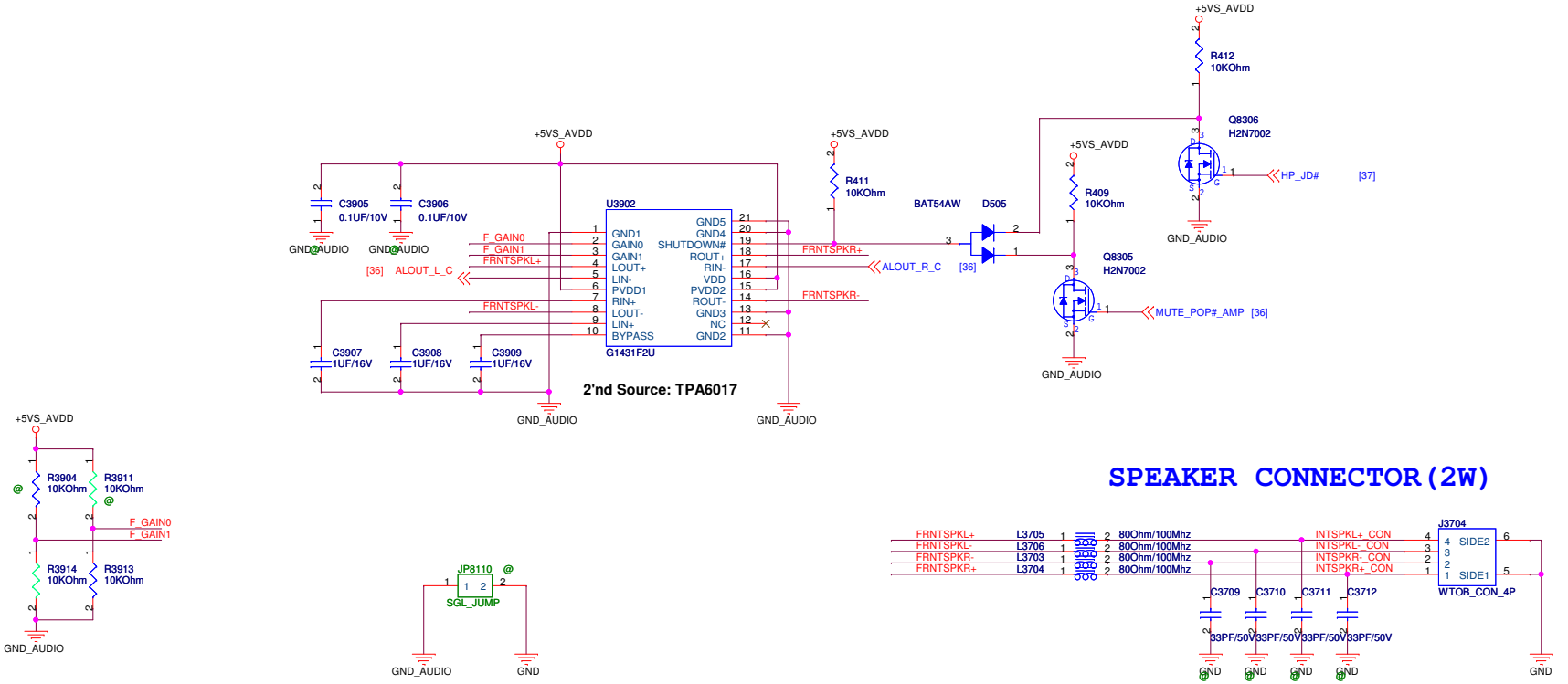
Title : AUD_FM2010

ASUSTeK COMPUTER INC. NB1

Engineer: John Hung

Size	Project Name	Rev
Custom	N2Sv	1.0

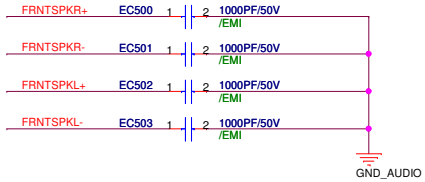
Date: Friday, February 13, 2009 Sheet 38 of 91



SPEAKER CONNECTOR(2W)

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

2.0G-G71G-EMI



<Variant Name>

Title : AUD_Woofer & Front

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 39 of 91

<Variant Name>

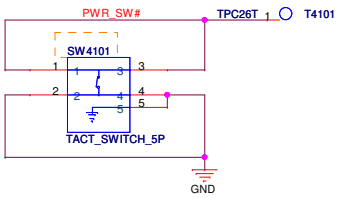
Title : CB_R5C833

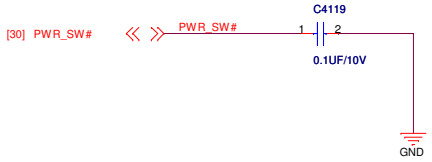
Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 40 of 91

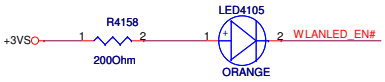
SWITCH BUTTON



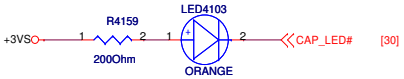


LED

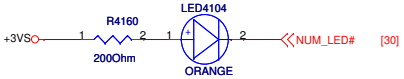
For WireLess LED

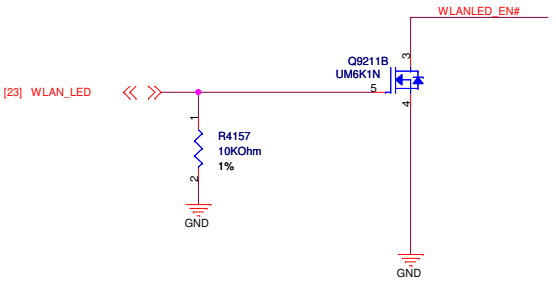


for Cap. Lock

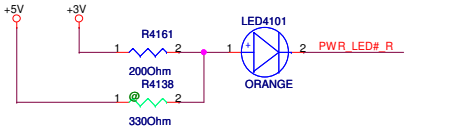


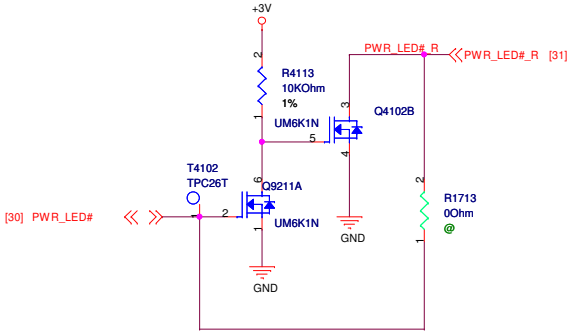
for Num Lock

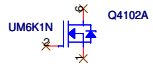




For POWER LED







<variant_name>

ASUSTeK COMPUTER INC. NB1	Title : CB_R5C833	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 41 of 91	

<Variant Name>

Title : CB_4in1 CardReader

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 42 of 91

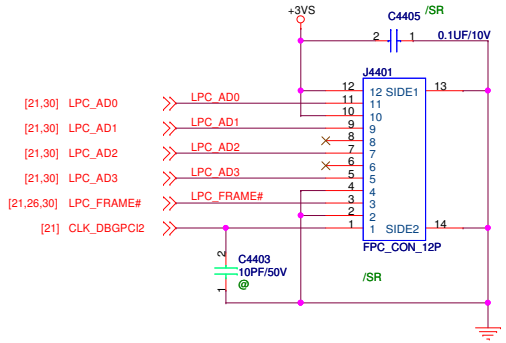
<Variant Name>

Title : NEW CARD

Engineer:

Size	Project Name	Rev
Custom		1.1

Date: Friday, February 13, 2009 Sheet 43 of 91



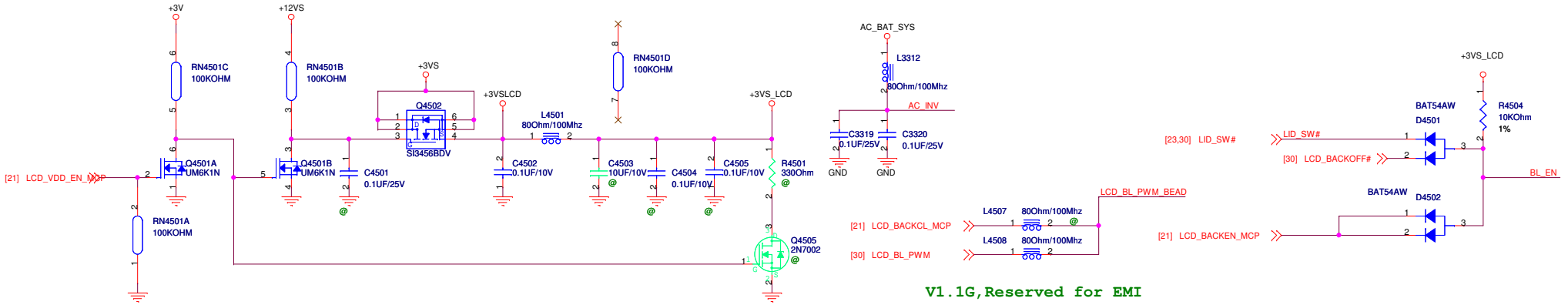
<Variant Name>

Title : DEBUG

Engineer:

Size	Project Name	Rev
Custom		1.0

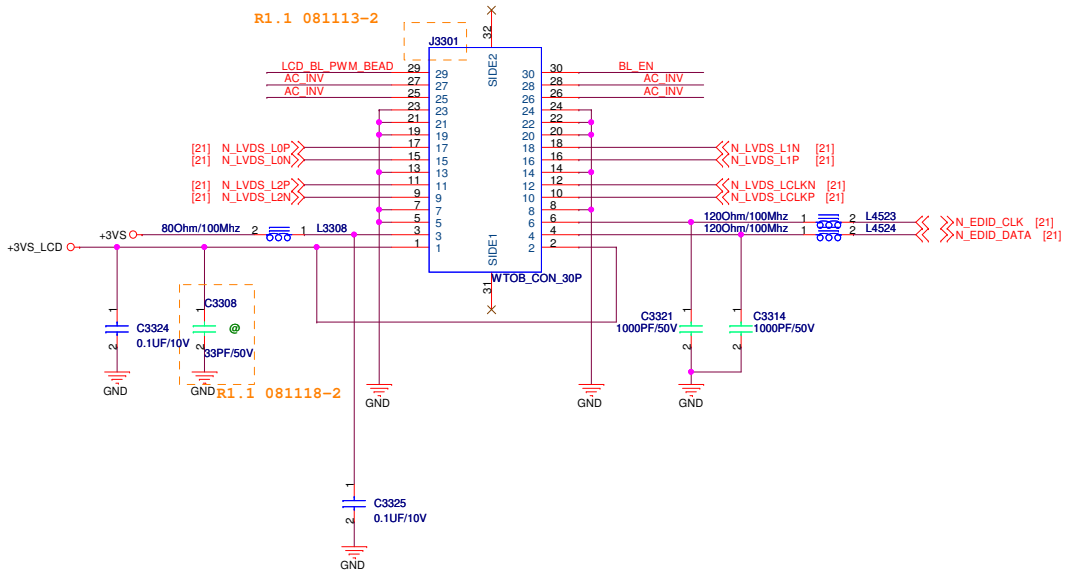
Date: Friday, February 13, 2009 Sheet 44 of 91



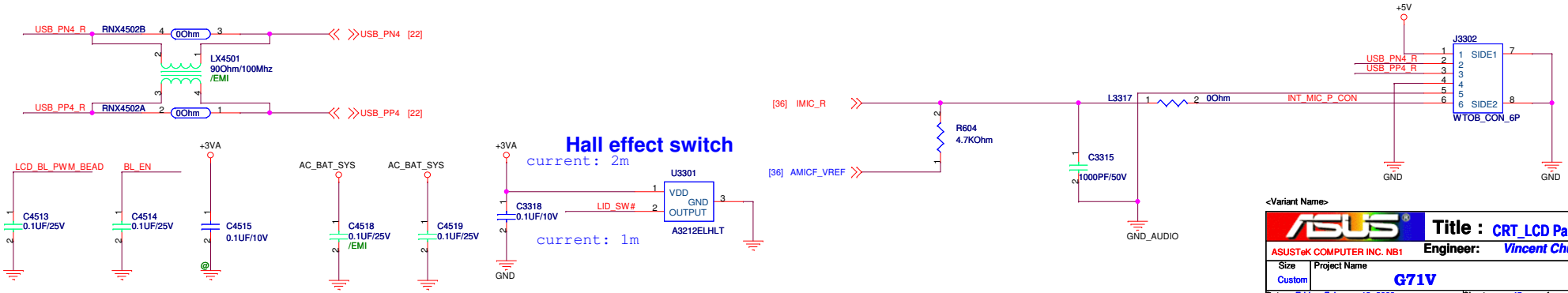
V1.1G,Reserved for EMI

LED PANEL LVDS Interface

R1.1 081113-2
R1.2 081202-1



CAMERA & MIC



Hall effect switch

<Variant Name>

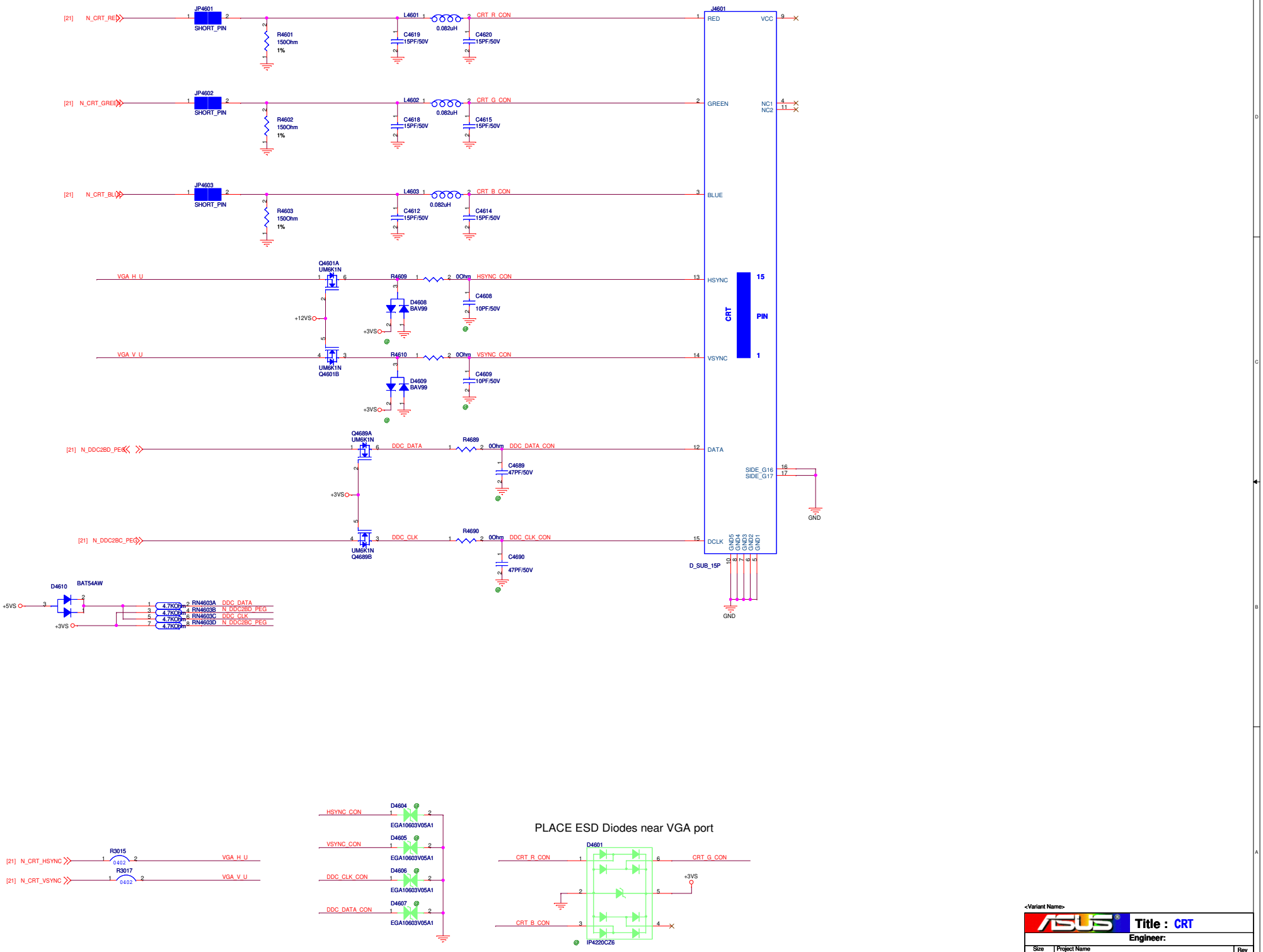
ASUSTeK COMPUTER INC. NB1

Title : CRT_LCD Panel

Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 45 of 91



<Variant Name>

Title : CRT

Engineer:

Size	Project Name	Rev
C		1.1

Date: Friday, February 13, 2009 Sheet 46 of 91

<Variant Name>

Title : TPM

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 47 of 91

<Variant Name>

Title LVDS & Inverter CON

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 48 of 91

<Variant Name>

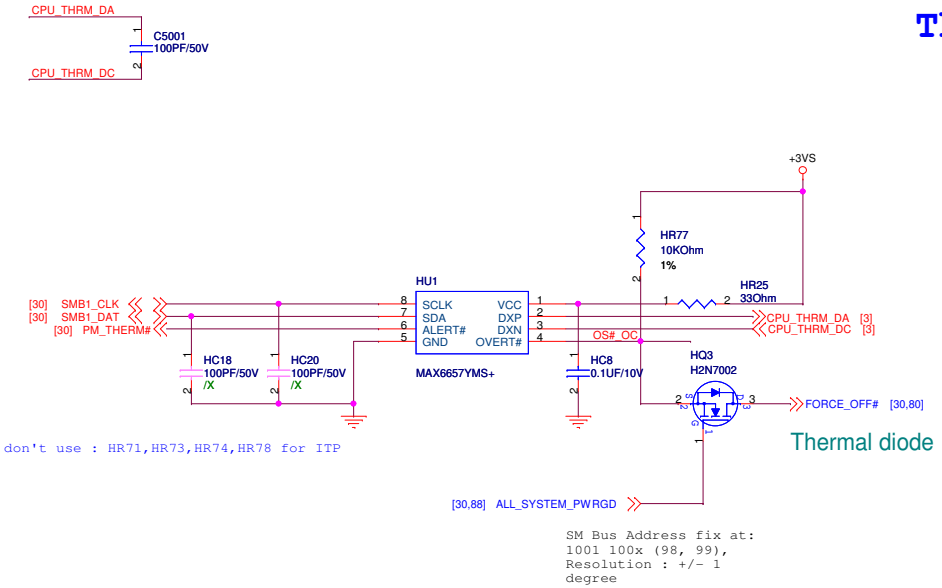
Title :

Engineer:

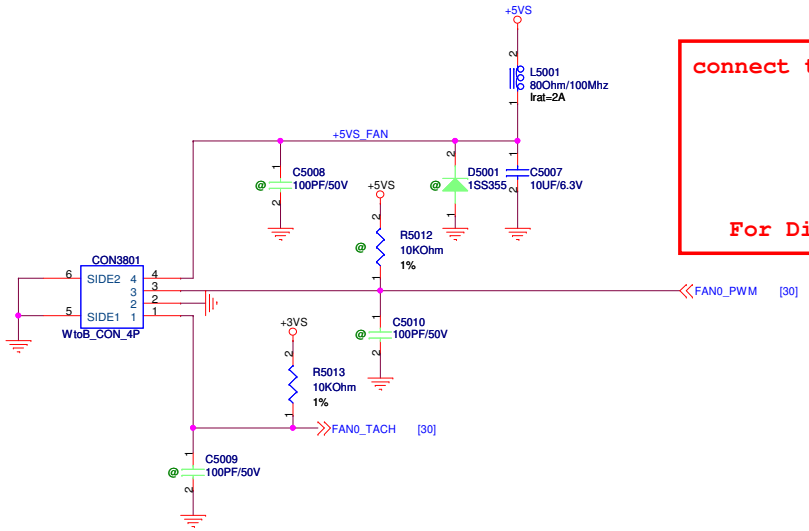
Size	Project Name	Rev
A		1.0

Date: Friday, February 13, 2009 Sheet 49 of 91

Thermal Sensor



DC FAN Control



connect to EC, trigger EC reset

For Discrete VGA

<Variant Name>

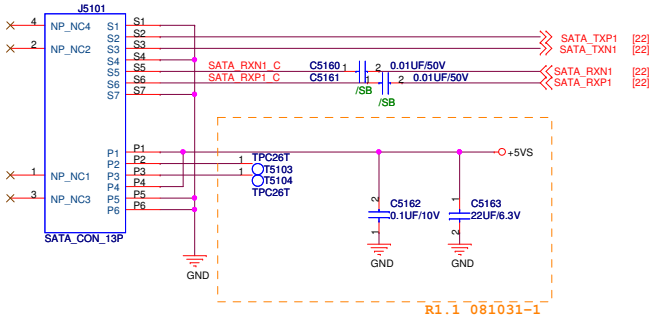
Title : Thermal & Fan

Engineer:

Size	Project Name	Rev
Custom		1.1

Date: Friday, February 13, 2009 Sheet 50 of 91

ODD



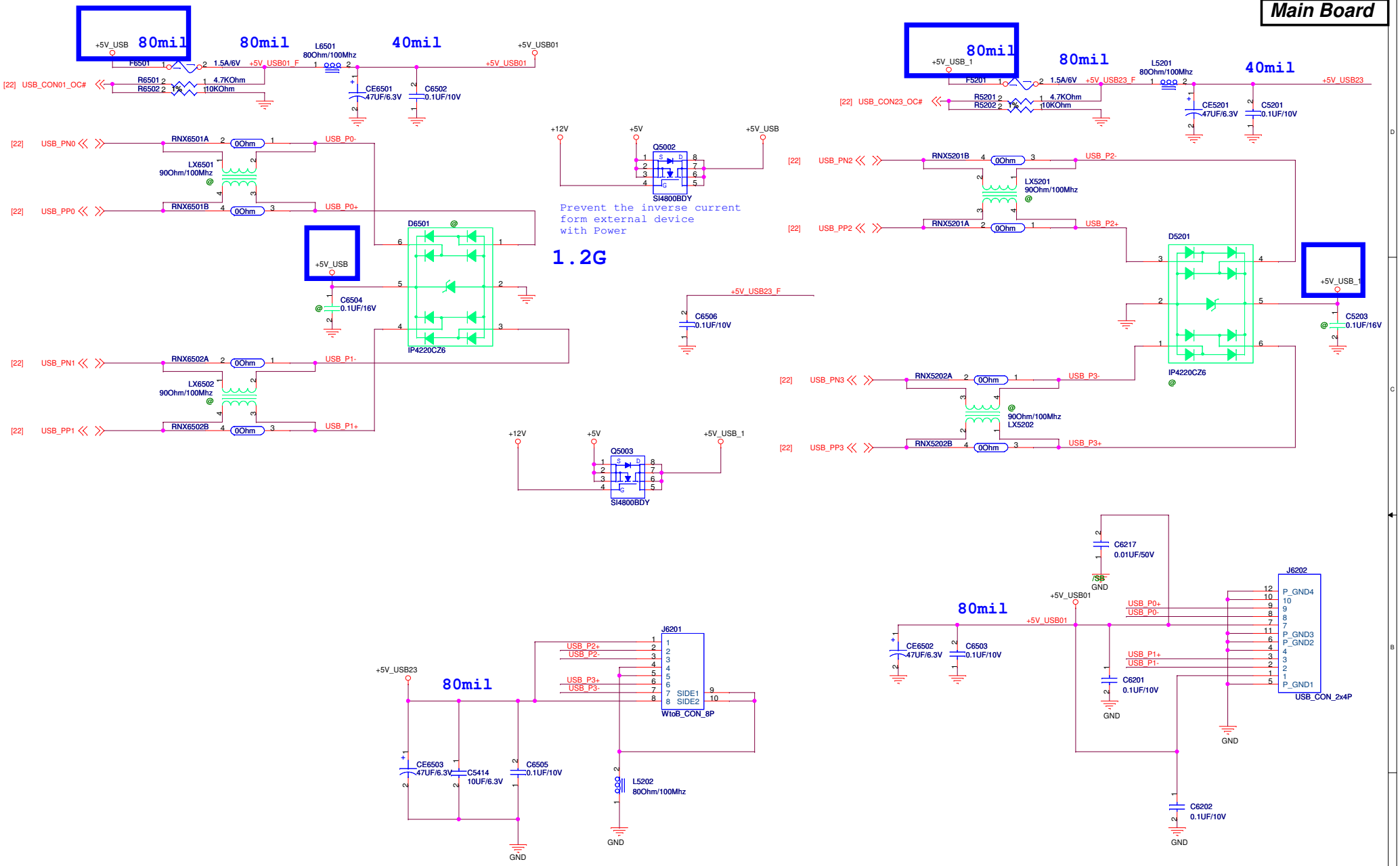
<Variant Name>

Title Sata HDD & Swap Bay

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 51 of 91



<Variant Name>

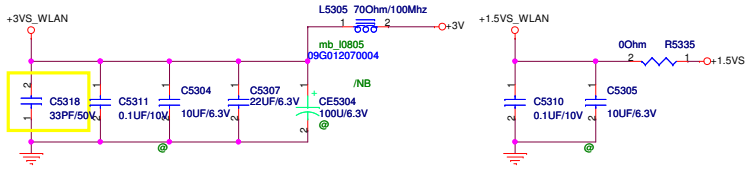
ASUSTeK COMPUTER INC. NB1

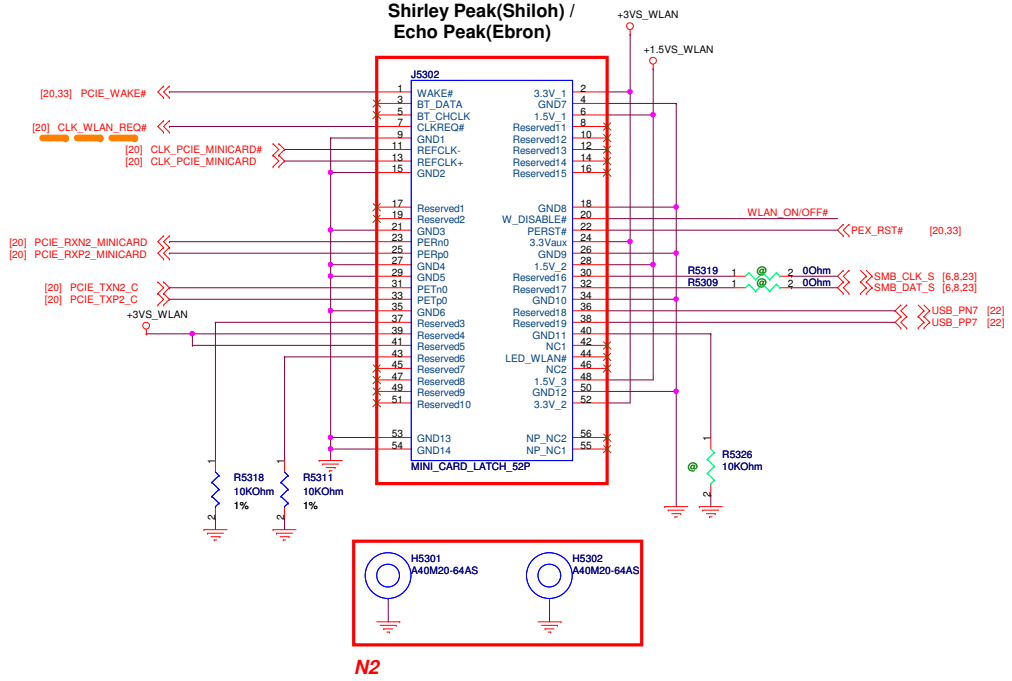
Title : USB_USB Ports

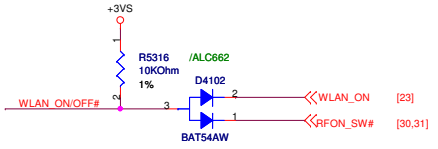
Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 52 of 91







<Variant Name>

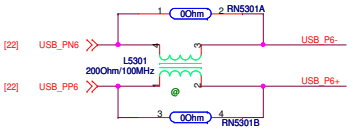
Title :Minicard card & Nut

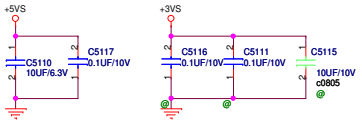
Engineer:

Size	Project Name	Rev
Custom		1.0

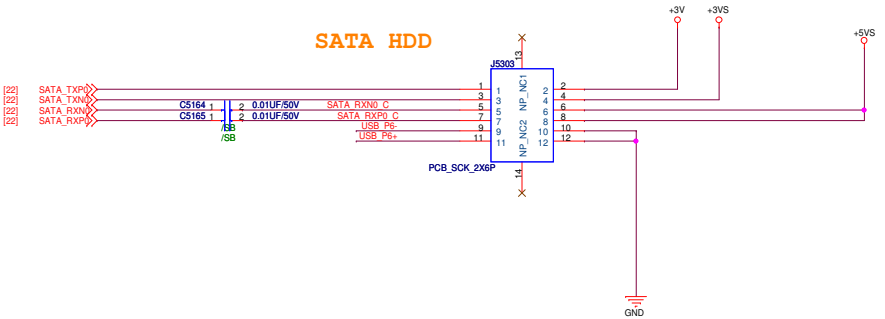
Date: Friday, February 13, 2009 Sheet 53 of 91

USB Cardreader





SATA HDD



<Variant Name>

I2C GPIO Controller

Title :

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 54 of 91

<Variant Name>

Title :

Engineer:

Size	Project Name	Rev
A		1.0

Date: Friday, February 13, 2009 Sheet 55 of 91

<Variant Name>

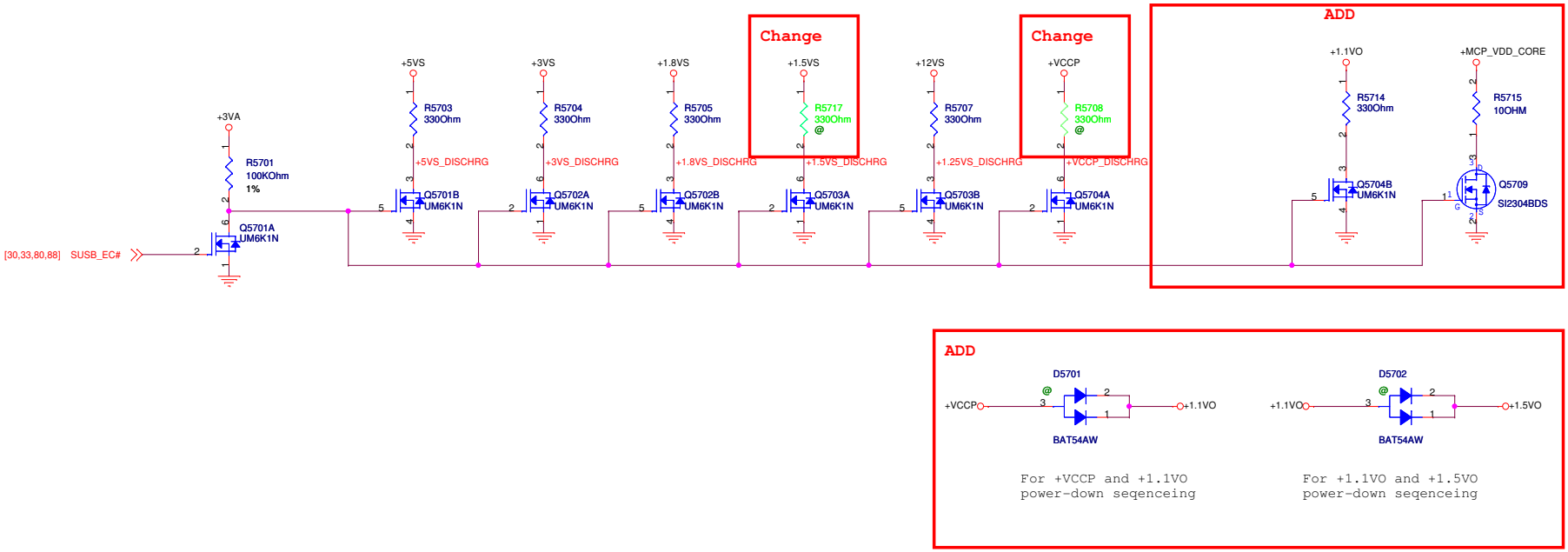
Title : LED_Indicator

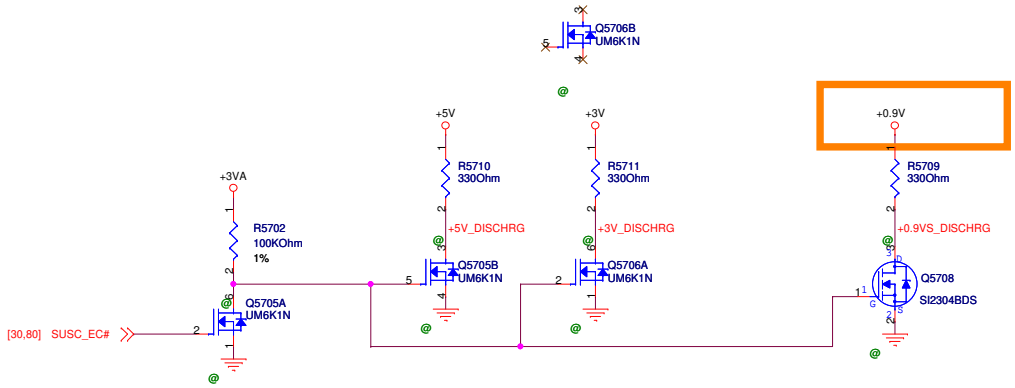
ASUSTeK COMPUTER INC. NB1

Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 56 of 91





<Variant Name>

Title : DSG_Discharge

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
Custom	G71G	1.0

Date: Friday, February 13, 2009 Sheet 57 of 91

<Variant Name>

Title :

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 58 of 91

<Variant Name>

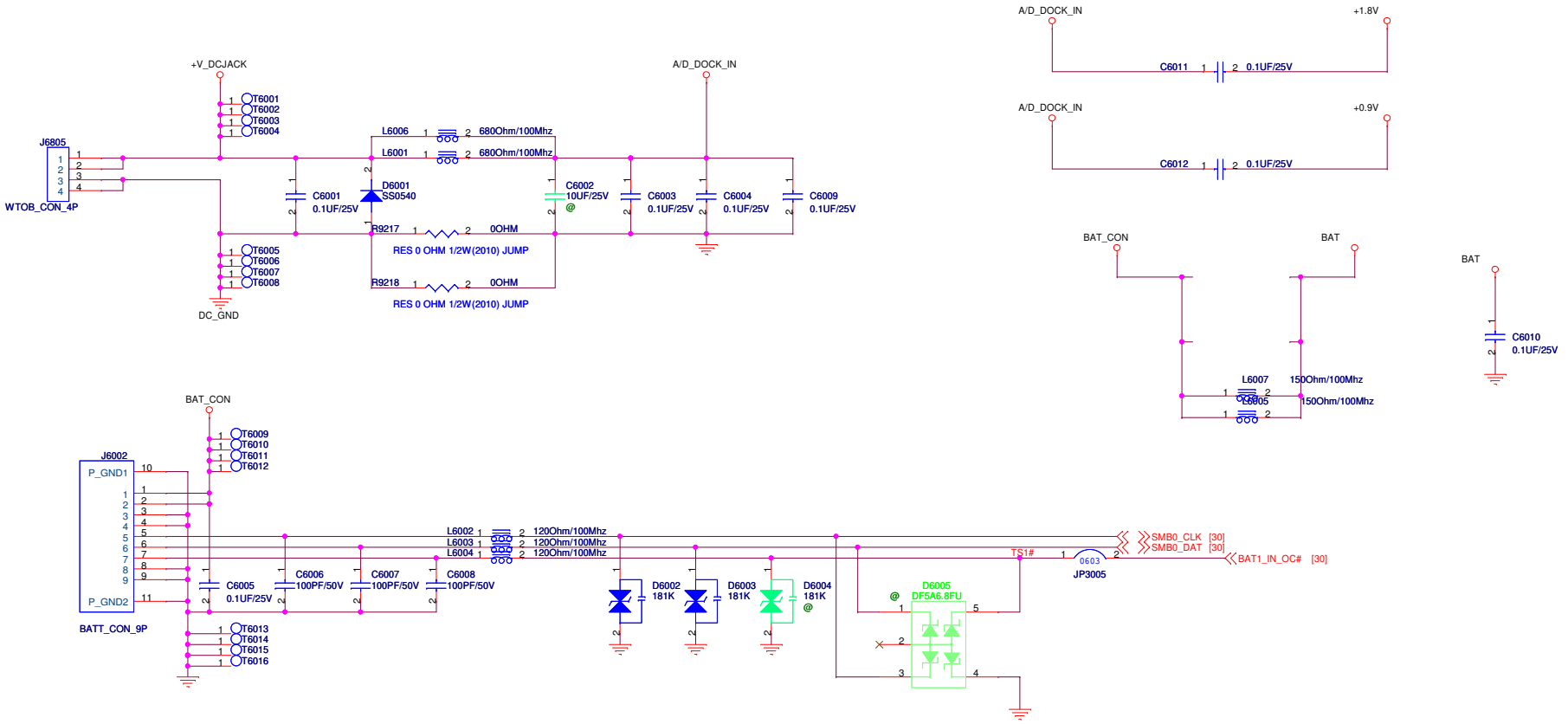
Title :

ASUSTeK COMPUTER INC. NB6

Engineer:

Size	Project Name	Rev
A		1.0

Date: Friday, February 13, 2009 Sheet 59 of 91



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT Conn.	
	Engineer: Vincent Chung	
Size: Custom	Project Name: G71V	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 60 of 91	

Main Board

<Variant Name>

Title : BT_Bluetooth

ASUSTeK COMPUTER INC. NB1

Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 61 of 91

Main Board

<Variant Name>

Title :

ASUSTeK COMPUTER INC. NB1

Engineer: John Hung

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 62 of 91

<Variant Name>

Title : FP_Fingerprint Conn.

ASUSTeK COMPUTER INC. NB1

Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 63 of 91

<Variant Name>

Title : TUN_TV Tuner

ASUSTeK COMPUTER INC. NB1

Engineer: John Hung

Size	Project Name	Rev
Custom	N2Sv	1.0

Date: Friday, February 13, 2009 Sheet 64 of 91

Hole-A

H7401
C71D71N

Hole-B

H7402
HOLE_NPTH

H7403
HOLE_NPTH

H7404
HOLE_NPTH

Hole-C

H7405
O83X71DO83X71N

Hole-D

H7409
CT276CB197ID138

H7410
CT276CB197ID138

H7411
CT276CB197ID138

H7412
CT276CB197ID138

GND

Hole-E

H7414
CT256B315D91N

H7406
CT256B315D91N

GND

H7407
CT256RB276X287D91N

H7408
CT256RB276X287D91N

GND

H7416
CT256B315D91N

GND_AUDIO

Hole-F

H7417
CT256B220D91N

H7420
CT256B220D91N

GND

H7418
CRT266X256D91N

GND

H7419
RT335X305D91N

GND

H7421
CT256B220D91N

H7422
CT256B220D91N

H7413
CT256B220D91N

H7415
CT256B220D91N

GND

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : ME_Conn & Screw Holes	
	Engineer: Vincent Chung	
Size: Custom	Project Name: G71V	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 65 of 91	

<Variant Name>

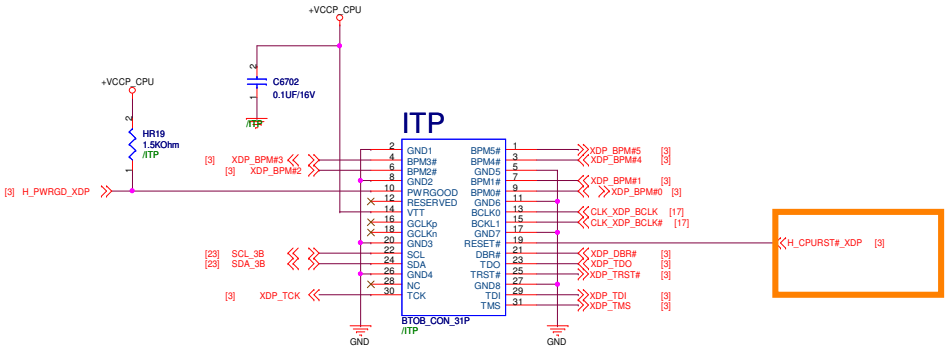
Title : E-SATA

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 66 of 91

Place Beside CPU



RSD, NB should be push-pull output

IN CPU page

<Variant Name>

Title :

Engineer:

Size	Project Name	Rev
C		1.0

Date: Friday, February 13, 2009 Sheet 67 of 91

<Variant Name>

Title :

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 68 of 91

ASUSTeK COMPUTER INC	Title : N10M-GE1_PCIE	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10JG	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 69 of 91	

ASUSTeK COMPUTER INC	Title : N10M-GE1_FB		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10JG		Rev: 1.0
Date: Friday, February 13, 2009	Sheet 70 of 91		

ASUSTeK COMPUTER INC	Title : N10M-GE1_VRAM	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10JG	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 71 of 91	

Title :	N10M-GE1_DISPLAY
ASUSTeK COMPUTER INC	Engineer: ENGINEER
Size: Custom	Project Name: N10JG
Rev: 1.0	
Date: Friday, February 13, 2009	Sheet 72 of 91

Title : N10M-GE1_XTAL

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10JG	1.0

Date: Friday, February 13, 2009 Sheet 73 of 91

ASUSTeK COMPUTER INC	Title : N10M-GE1_ROM		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10JG		Rev: 1.0
Date: Friday, February 13, 2009	Sheet 74 of 91		

Fingerprint Board

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : LED & Touchpad	
	Engineer: Vincent_Chung	
Size: Custom	Project Name: G71V	Rev: 1.1
Date: Friday, February 13, 2009	Sheet 75 of 91	

Fingerprint Board

<Variant Name>

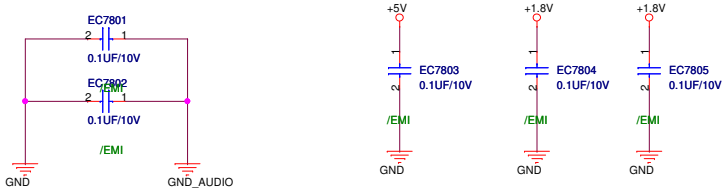
Title : Fingerprint & Touchpad

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
Custom	M70Sv	1.1

Date: Friday, February 13, 2009 Sheet 76 of 91



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : Fingerprint & Touchpad	
	Engineer: Wenchi_Shen	
Size: Custom	Project Name: M70Sv	Rev: 1.1
Date: Friday, February 13, 2009	Sheet 77 of 91	

History

1.0G:@ 1.1G power modify : $ 1.2G: %
1.1G EE modify :

20080520 1.2G

Page 52 1. ADD USB+5V gate Q5002

Page 56 2. ADD R5626,R5609

Page 4 3. DEL R0412

Page 54 4. ADD C5402,C5403 5p for SMBus in GPIO controller ; GPRN10 change to 10K ohm

Page 84 5. Controlle +5V with SUSC#_PWR

Page 82 6. Change +VCCP to 1.2V default for CPU O.C. ability improve

20080701 2.0G

Page 56 1. TP-LED v.s. TP-disable LED reverse
Page 45 2. Inverter CN pin 19 reserve 0 phm to GND ,never stuff for single-lamp inverter
Page 46 3. Battery in P/H change to +3VA
Page 80 4. CPU load-line modify to 2.1 mini-ohm (R8036 由 10.5K改成 9.31K 1%)

<Variant Name>

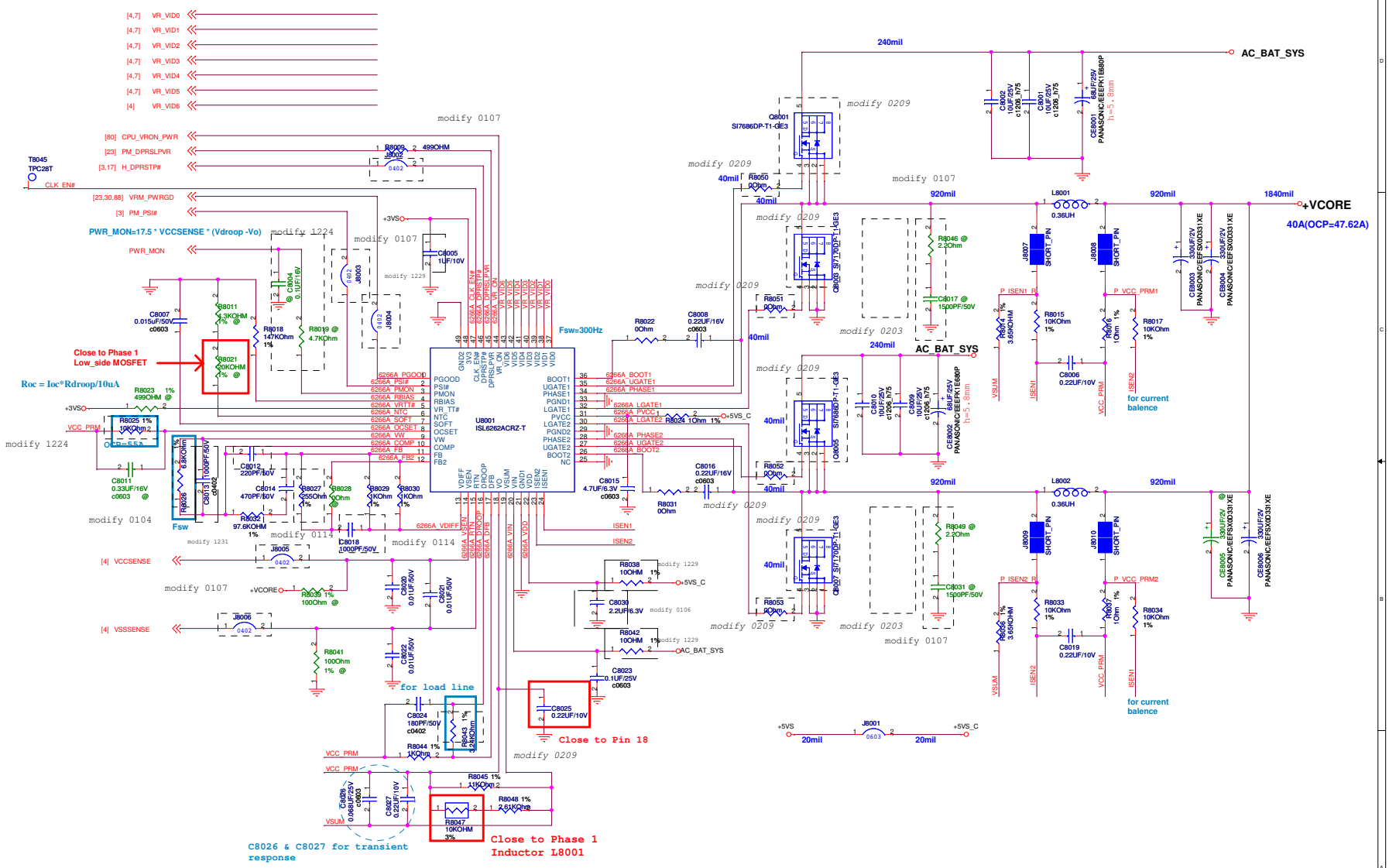
ASUSTeK COMPUTER INC

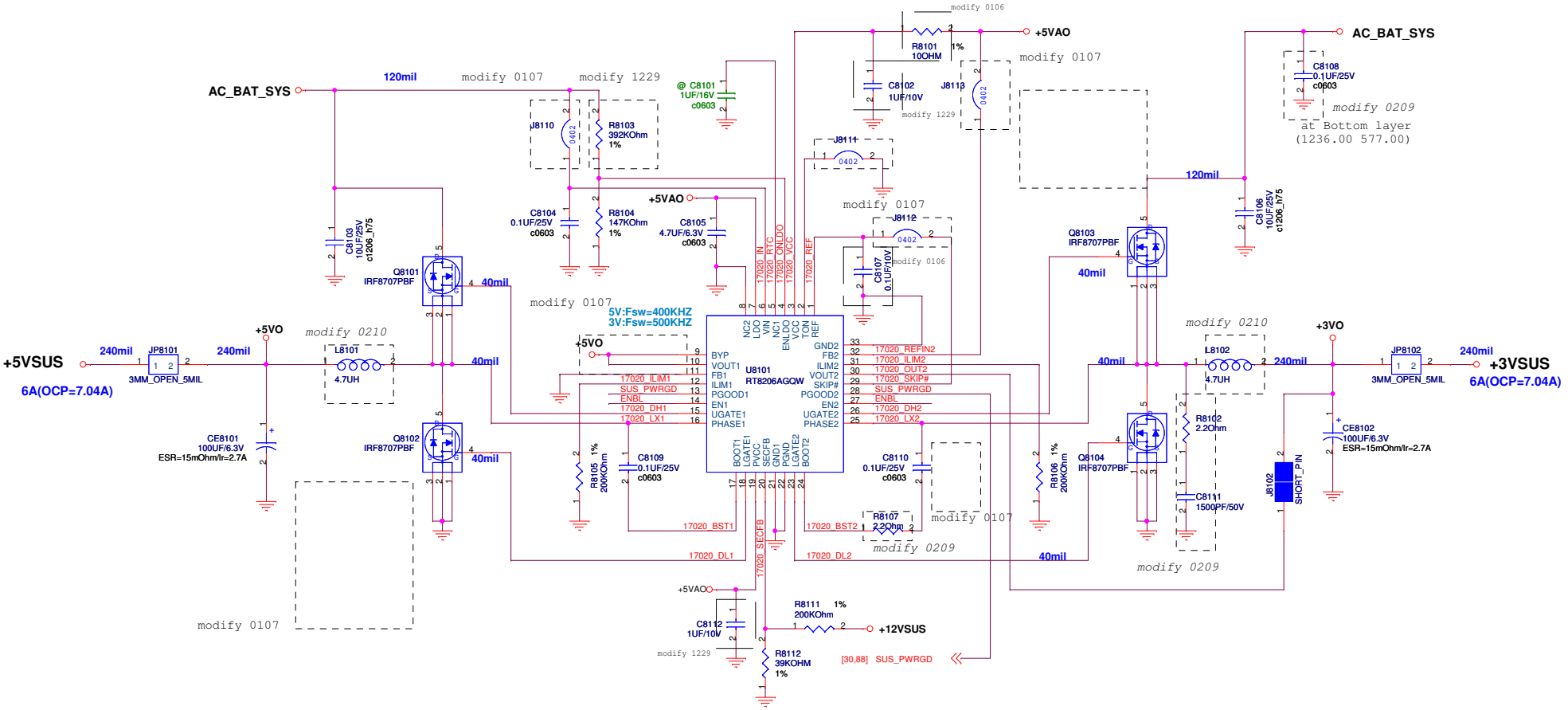
Title : History

Engineer:

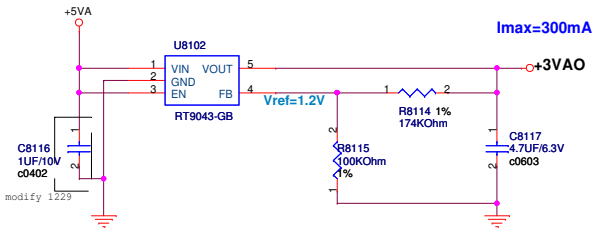
Size	Project Name	Rev
Custom		1.0

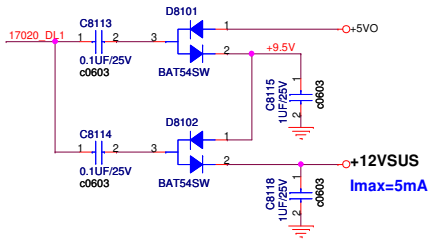
Date: Friday, February 13, 2009 Sheet 78 of 91

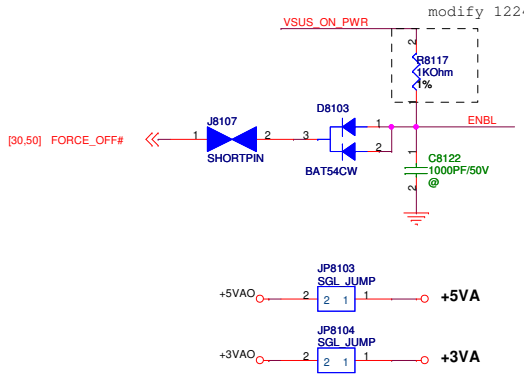

[4,7] VR_VID0
[4,7] VR_VID1
[4,7] VR_VID2
[4,7] VR_VID3
[4,7] VR_VID4
[4,7] VR_VID5
[4] VR_VID6
[80] CPU_VRON_PWR
[23] PM_DPRSLPVR
[3,17] H_DPRSTP#
T8045
TPC28T
CLK_EN#
[23,30,88] VRM_PWRGD
[3] PM_PSI#
PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
PWR_MON
Close to Phase 1
Low_side MOSFET
Roc = Ioc*Rdroop/10uA
Fsw
Fsw=300Hz
U8001
ISL6262ACRZ-T
[4] VCCSENSE
[4] VSSSENSE
for load line
Close to Pin 18
Close to Phase 1
Inductor L8001
C8026 & C8027 for transient
response
Total count: 72 pcs
AC_BAT_SYS
+VCORE
40A(OCP=47.62A)
for current
balence
HS MOS Second source IRF8714
LS MOS Second source IRF8736
Title : +VCORE
ASUSTeK COMPUTER INC. NB1
Engineer: Eason
K50I
Date: Friday, February 13, 2009
Sheet 79 of 91



+3VAO

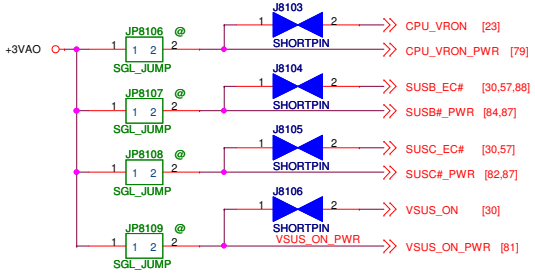






Total count: 42 pcs

FOR POWER TEST



<Variant Name>

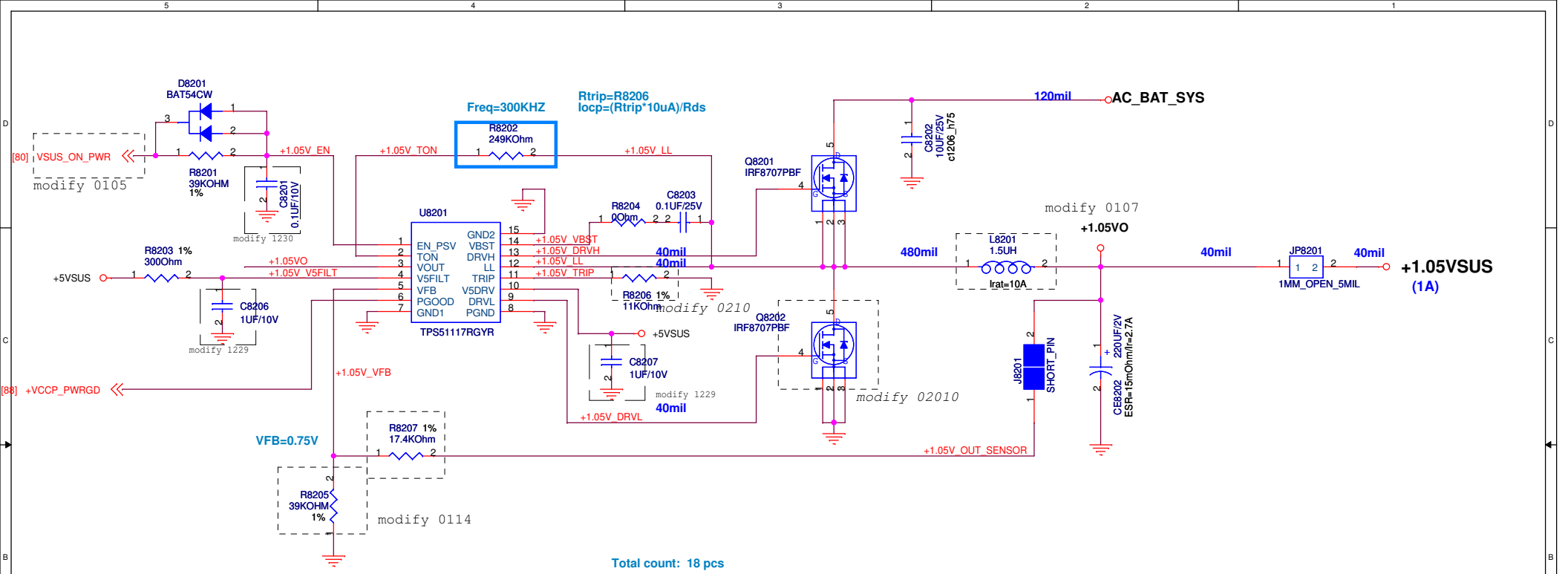
ASUSTeK COMPUTER INC. NB

Title : POWER_SYSTEM

Engineer: Eason

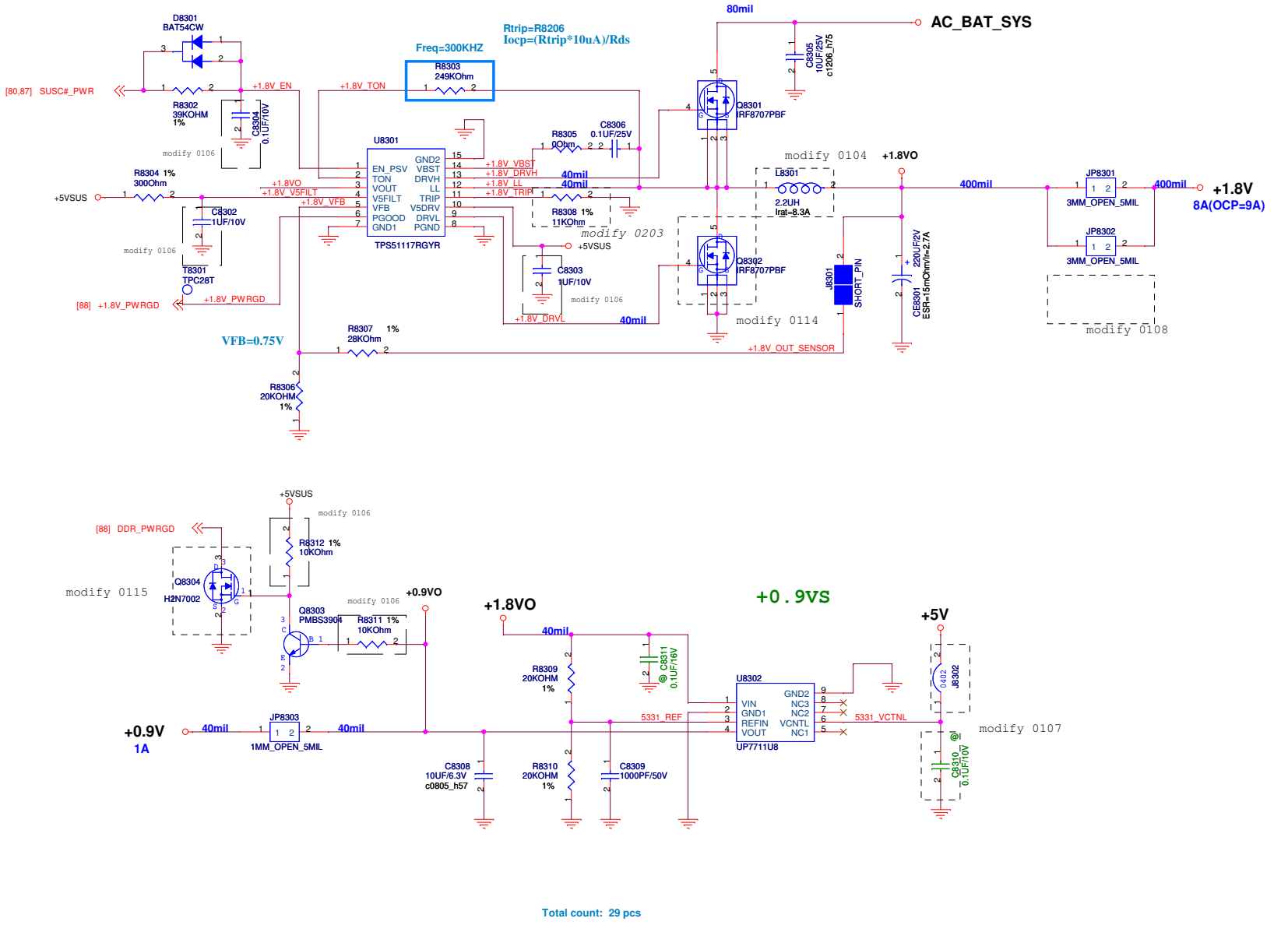
Size	Project Name	Rev
Custom	K50I	1.0

Date: Friday, February 13, 2009 Sheet 80 of 91



<Variant Name>

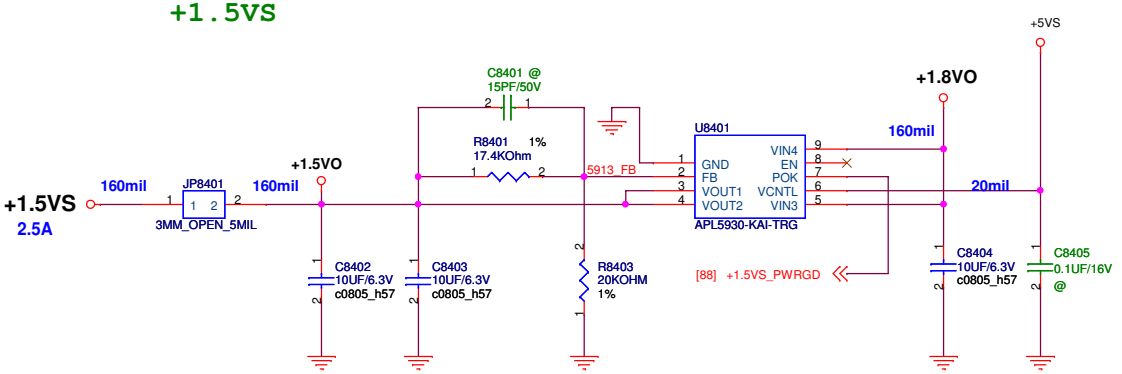
ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_+VCCP	
	Engineer: Eason	
Size: Custom	Project Name: K50I	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 81 of 91	



Total count: 29 pcs

ASUSTeK COMPUTER INC. NB3	Title : DDR	
	Engineer: EASON	
Size: Custom	Project Name: K50IA	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 82 of 91	

+1.5VS



Total count: 6 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : INS29491694

Engineer: Eason

Size	Project Name	Rev
B	K50I	1.0

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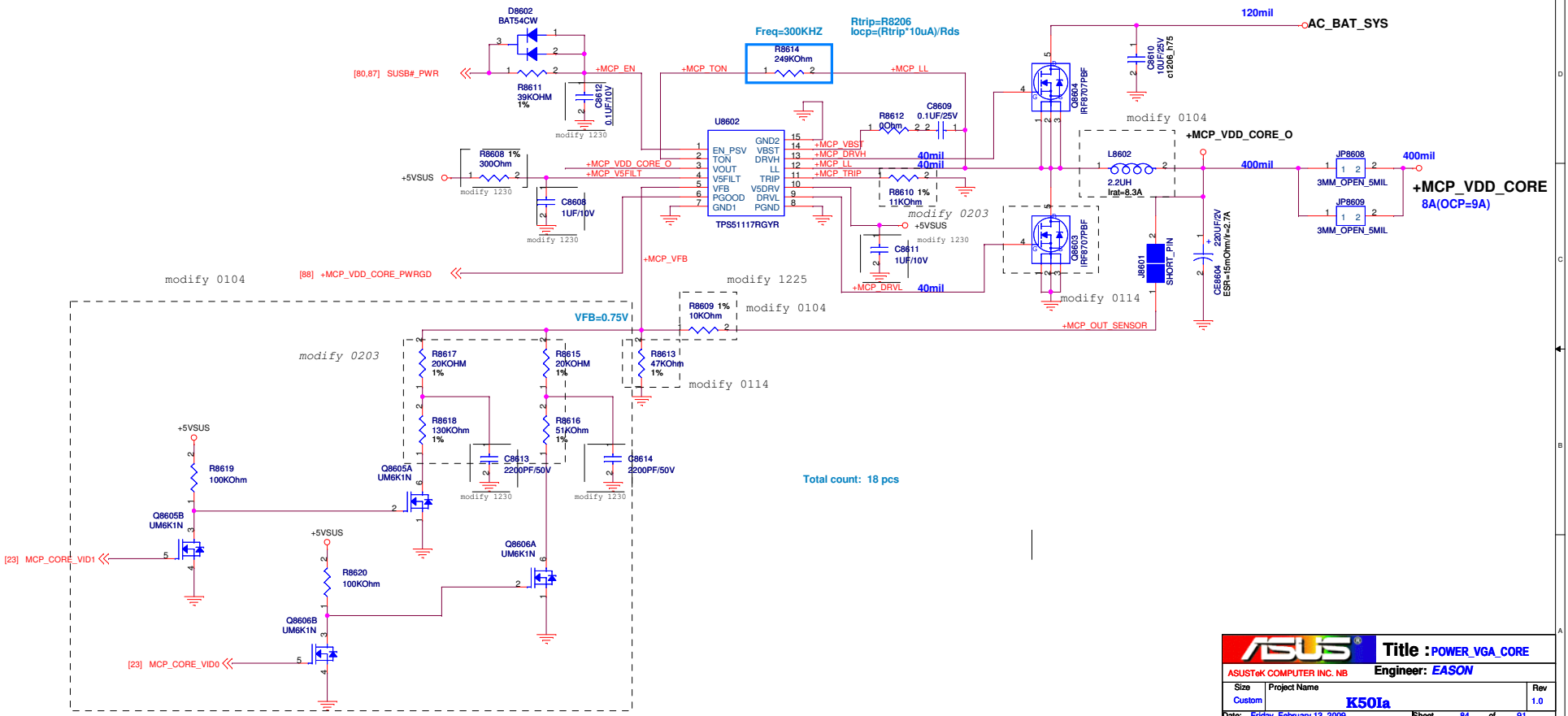

ASUSTeK COMPUTER INC. NB	Title : POWER_VGA_CORE	
	Engineer: EASON	
Size: Custom	Project Name: K50Ia	Rev: 1.0
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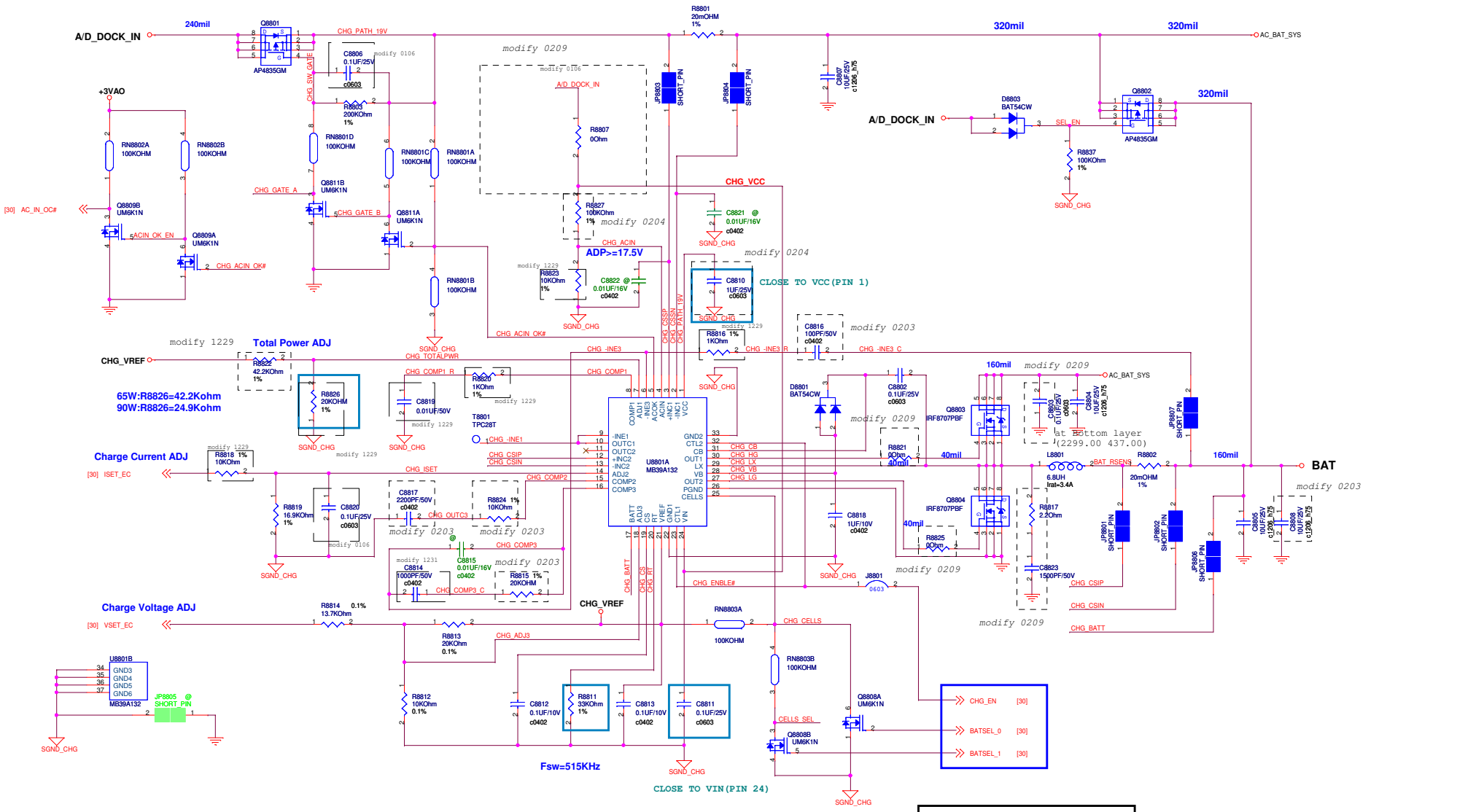

Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
H	L	2 CELLS
L	H	3 CELLS
L	L	4 CELLS

TOTAL COUNT:56 PCS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

<Variant Name>

Title : POWER_CHARGER_202

ASUSTeK COMPUTER INC. NB

Engineer: Eason

Size	Project Name	Rev
C	K50I	1.0

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BATTERY IN DETECT

<Variant Name>

Title :POWER_DETECT

ASUSTeK COMPUTER INC. NB

Engineer: Eason

Size	Project Name	Rev
Custom	K50I	1.0

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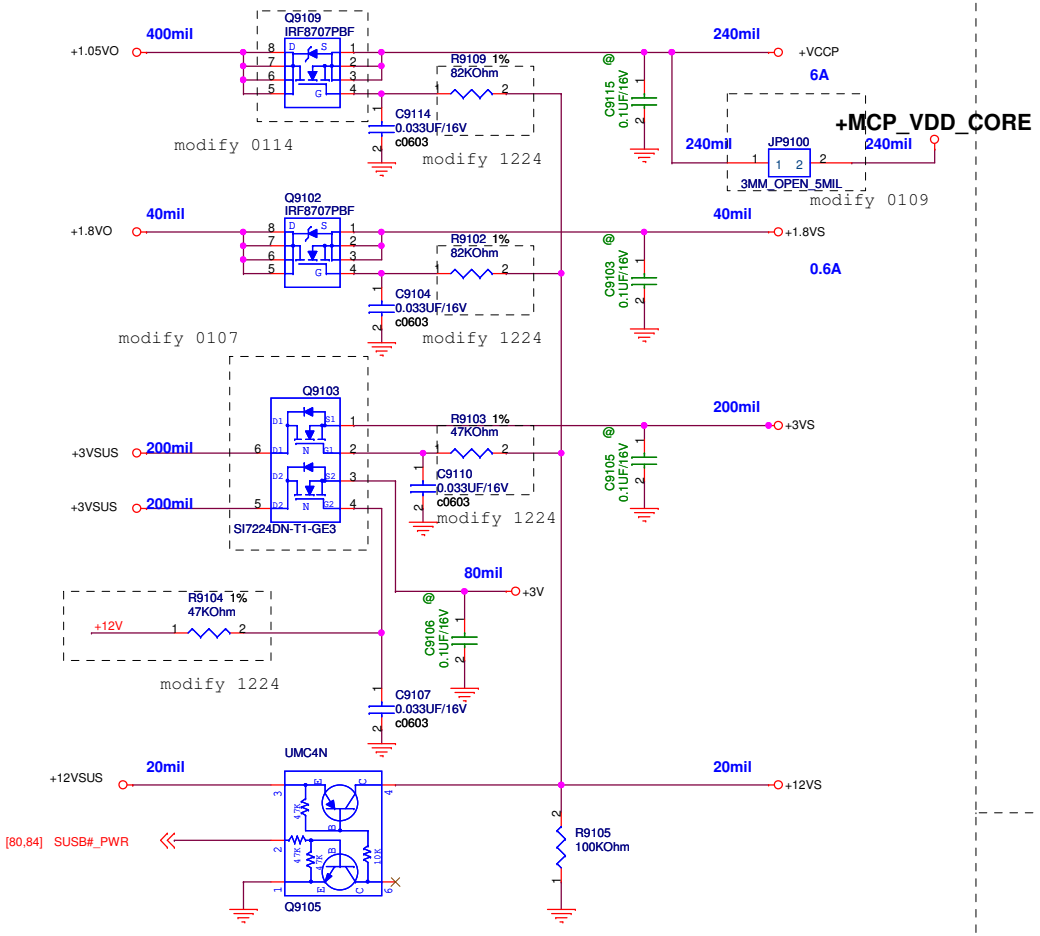
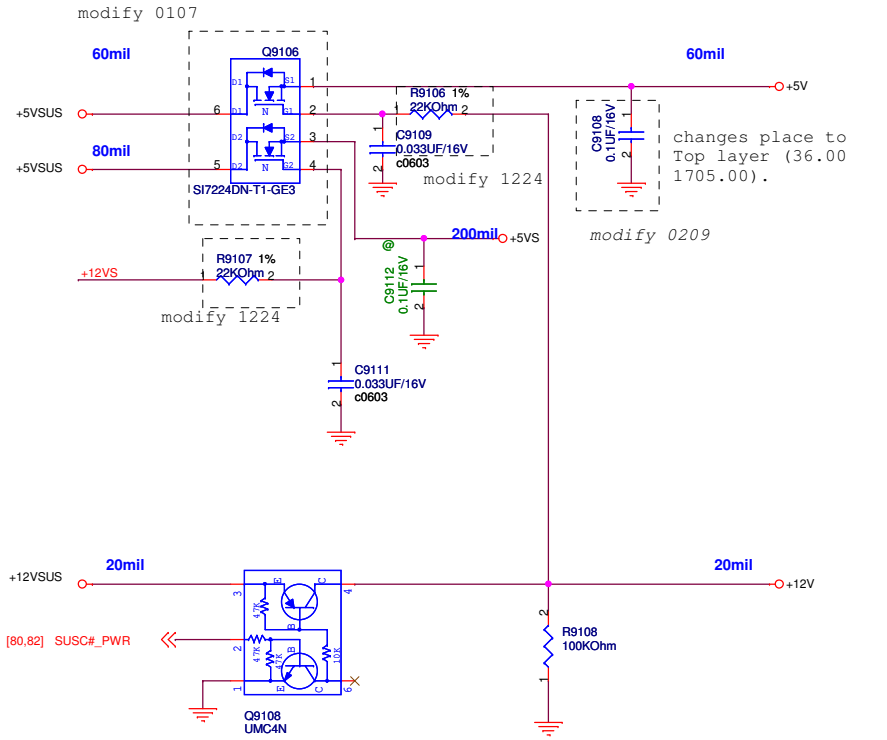
SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER



<Variant Name>

Title : POWER_LOAD SWITCH

ASUSTeK COMPUTER INC. NB

Engineer: Eason

Size	Project Name	Rev
B	K50I	1.0

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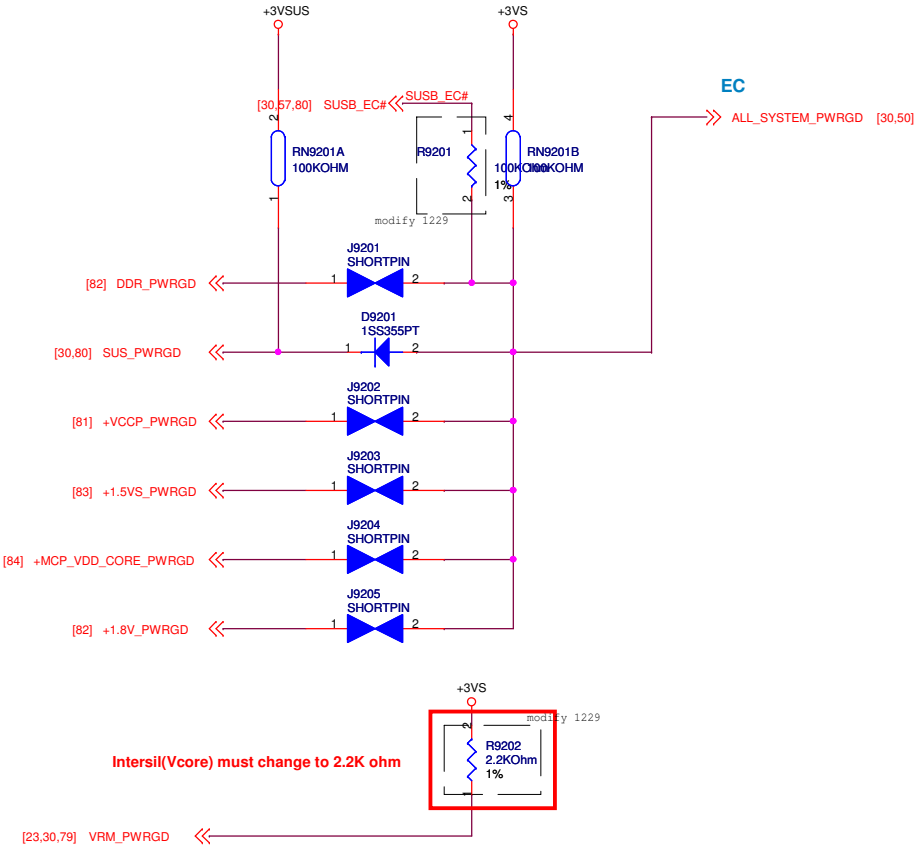
POWER GOOD DETECTER



Total count: 8 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Eason	
Size: B	Project Name: K50I	Rev: 1.0
Date: Friday, February 13, 2009	Sheet 88 of 91	

AC_BAT_SYS	AC_BAT_SYS	[31,45,79,80,81,82,84,85]
BAT	BAT	[60,85]
BAT_CON	BAT_CON	[60]
+3VAO	+3VAO	[80,85]
+5VA	+5VA	[80]
+3VA	+3VA	[23,30,45,57,80]
+5VAO	+5VAO	[80]
+5VO	+5VO	[80]
+5VSUS	+5VSUS	[80,81,82,84,87]
+5V	+5V	[41,45,52,57,82,87]
+5VS	+5VS	[7,31,36,37,39,46,50,51,54,57,79,83,87]
+3VO	+3VO	[80]
+3VSUS	+3VSUS	[21,22,23,24,26,30,31,33,36,80,87,88]
+3V	+3V	[31,41,45,53,54,57,87]
+3VS	+3VS	[3,6,7,8,21,22,23,24,26,30,31,33,36,41,44,45,46,50,53,54,57,79,87,88]
+12VSUS	+12VSUS	[80,87]
+12V	+12V	[36,52,87]
+12VS	+12VS	[45,46,57,87]
+1.8VO	+1.8VO	[82,83,87]
+1.8V	+1.8V	[6,8,10,19,82]
+1.8VS	+1.8VS	[21,57,87]
+0.9V	+0.9V	[6,9,57,82]
+0.9VO	+0.9VO	[82]
+1.05VO	+1.05VO	[81,87]
+VCCP	+VCCP	[5,24,57,87]
+1.5VO	+1.5VO	[57,83]
+1.5VS	+1.5VS	[4,53,57,83]
+VCORE	+VCORE	[4,5,79]
A/D_DOCK_IN	A/D_DOCK_IN	[60,85]

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Eason

Size	Project Name	Rev
Custom	K50I	1.0

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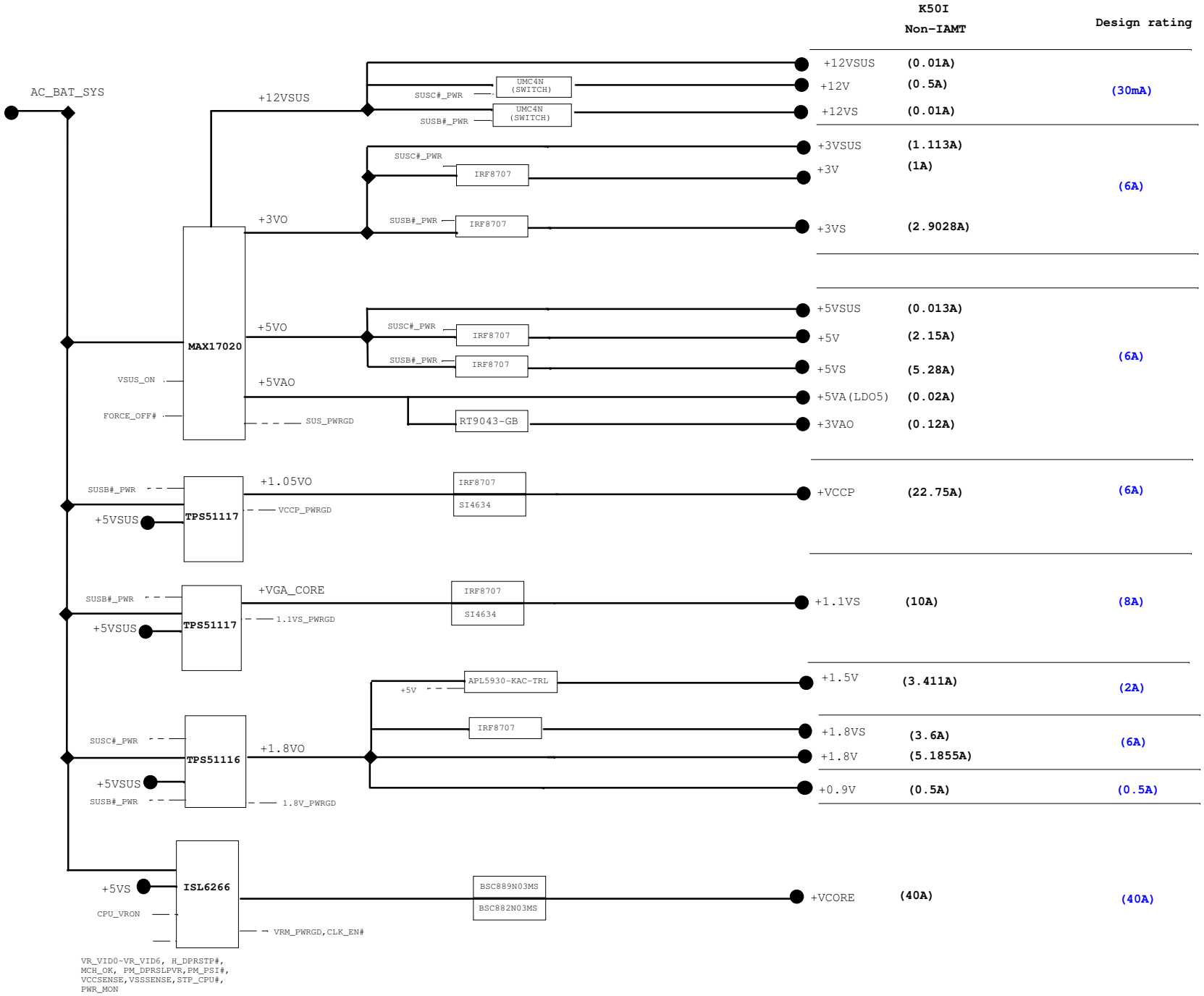

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Eason

Size	Project Name	Rev
Custom	K50I	1.0

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<variant_name>
Title : POWER_N/A

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom	G71G	1.0

Date: Friday, February 13, 2009 Sheet 91 of 91
</variant_name>