CHELSEA DJ2 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M

2010-04-13

REV : X01

```
    DY : Nopop Component
  HDMI : Pop for HDMI function
  GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN
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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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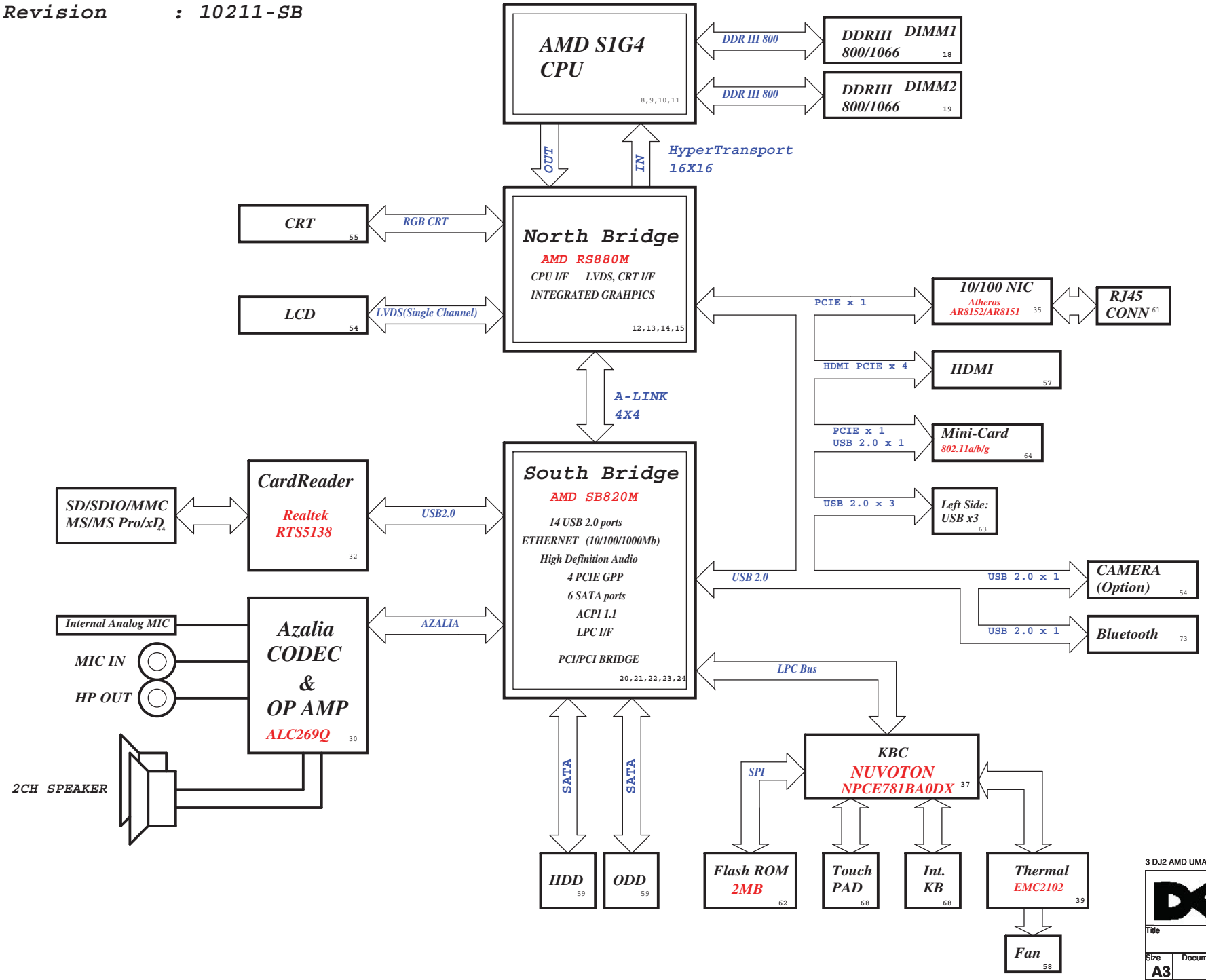
Title	Cover Page	
Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 1 of 90	

Project code : 91.4EM01.001
PCB P/N : 48.4EM18.0SA
Revision : 10211-SB

Chelsea DJ2 AMD UMA Block Diagram



CHARGER BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

SYSTEM DC/DC RT8205BGQW-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC RT8209EGQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN

CPU CORE ISL6265AHRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

DDR III SUS&VTT TPS51116RGER 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

SYSTEM DC/DC APL5930KAI 52	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC Swithes/RT9013 42,53	
INPUTS	OUTPUTS
+3.3V_ALW	+3.3V_RUN
+5V_ALW	+5V_RUN
+1.5V_SUS	+1.5V_RUN
+3.3V_RUN	+2.5V_RUN

SYSTEM DC/DC TPS51125RGER 48,51	
INPUTS	OUTPUTS
+3.3V_ALW +1.5V_SUS	+1.1V_ALW +CPU_VDDR

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Title: Block Diagram

Size	Document Number	Rev
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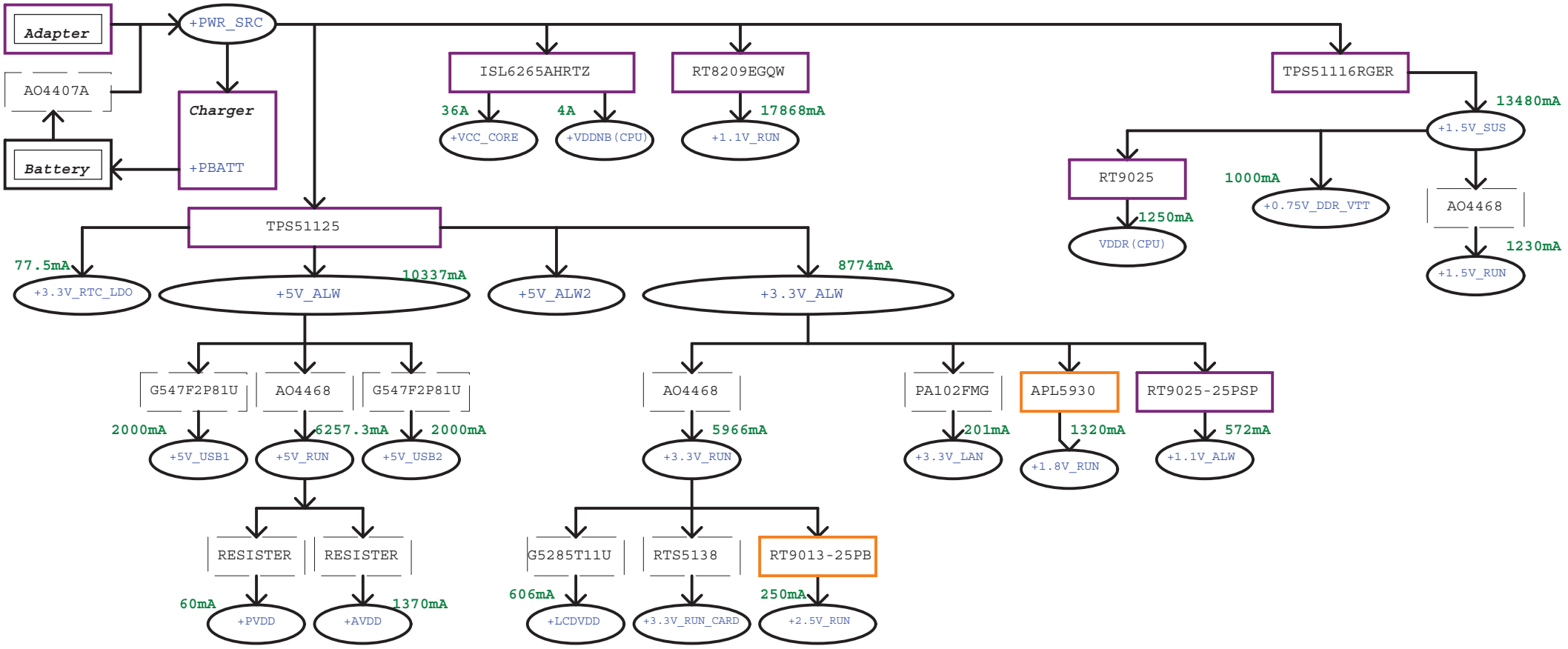
Power Block Diagram

Power Shape

Regulator | LDO | Switch



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Title: Power Block Diagram		
Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
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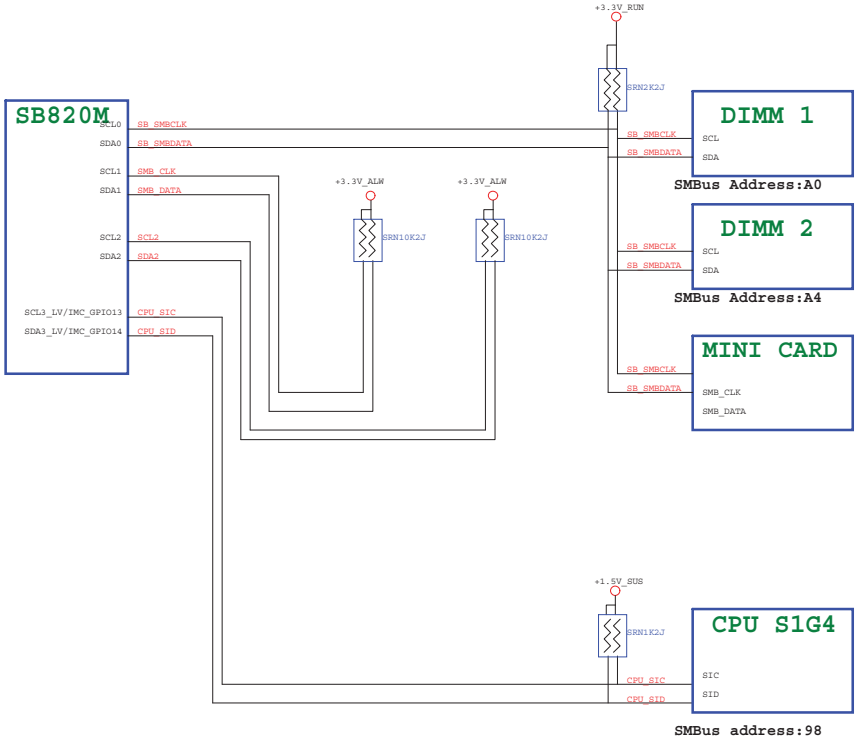
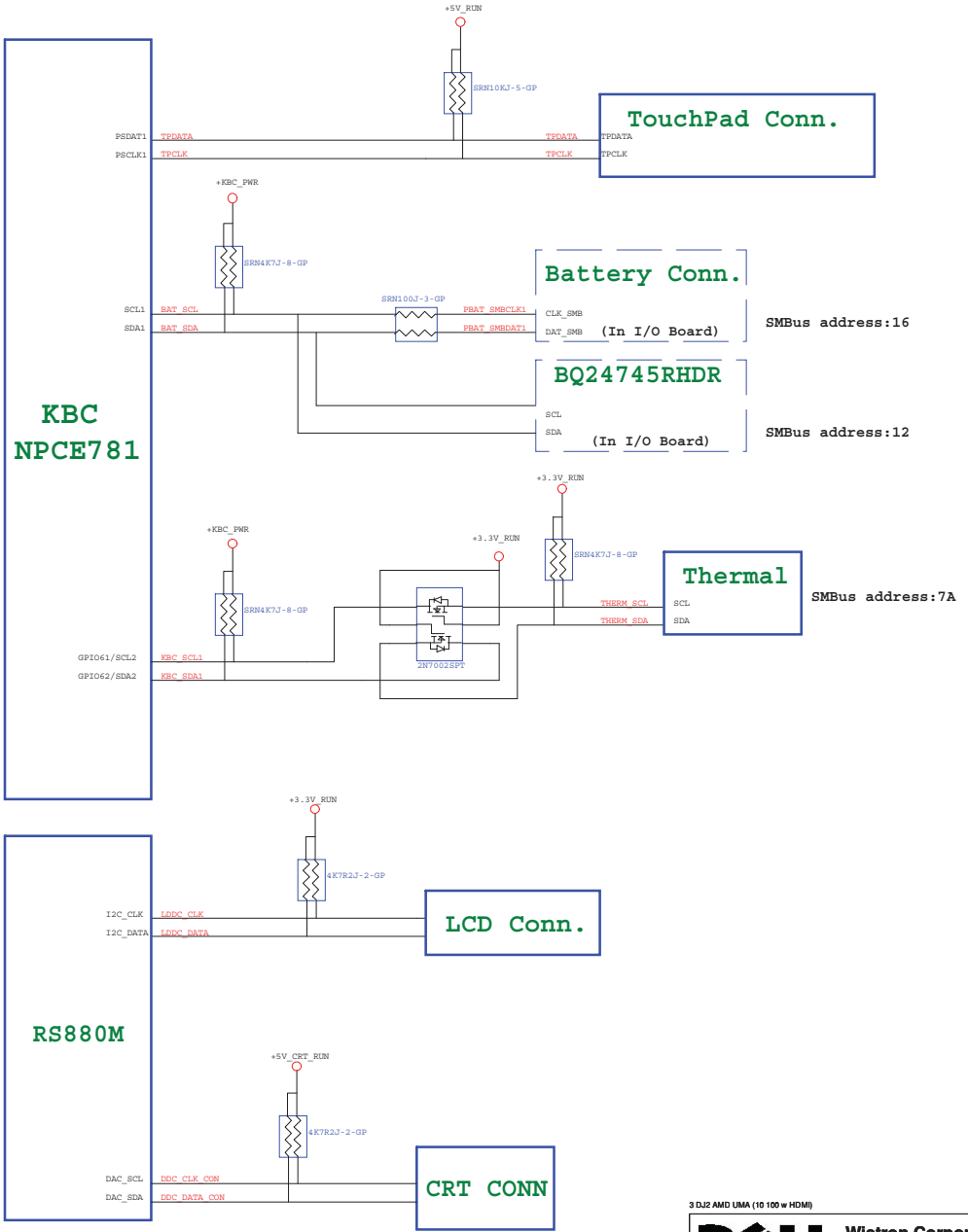
SB820M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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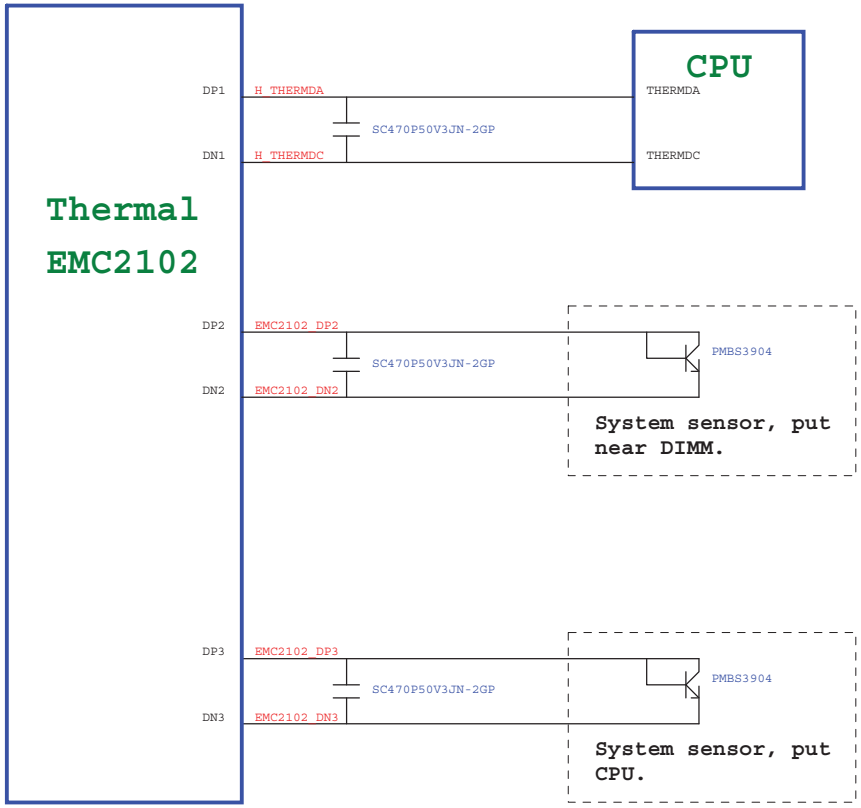
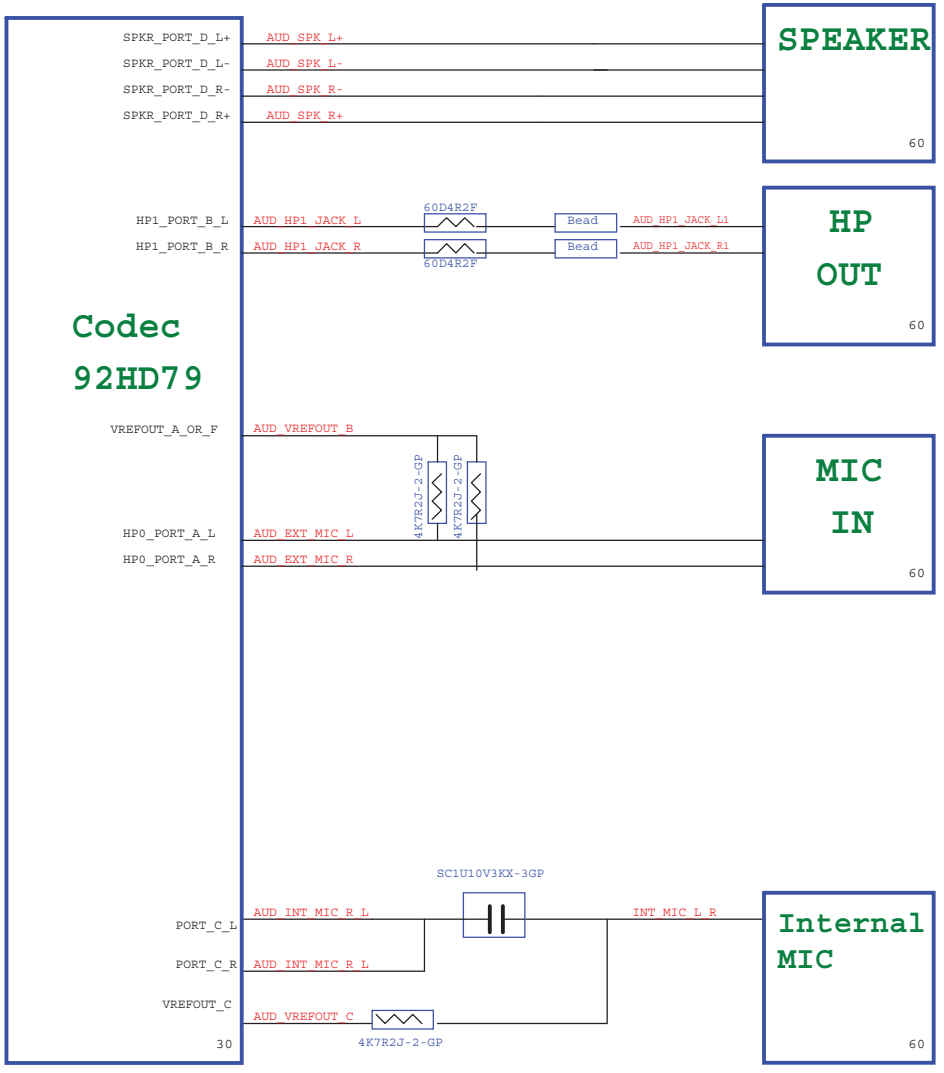
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub * 0V / 3.3V / LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. * 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode

NB880M Strapping

Capture from 46113 rs880m ds nda 1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available * 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	Reserve
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	Reserve

PCIE Routing

LANE0	MiniCard WLAN
LANE1	LAN

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Title: Table of Content

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(Blanking)

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Title: Clock Generator ICS9LPRS480

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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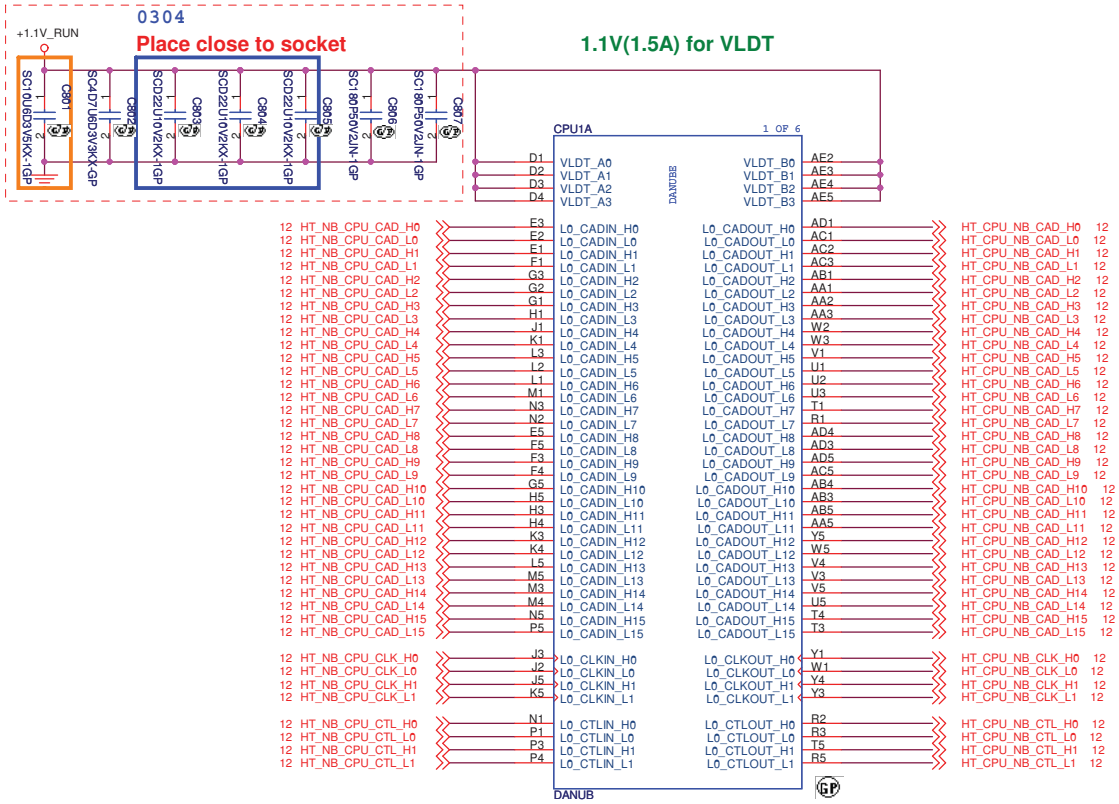
SSID = CPU



SKT-BGA638H176

1'nd 62.10055.111

2'nd 62.10055.181

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Title: CPU_HT_LINK I/F_(1/4)

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SSID = CPU

4.7UF*4
0.22UF*4
1000PF*4
180PF*4

Place near to CPU

+CPU_VDDR

C901 SC4D7U6D3V0KX-GP
C902 SC4D7U6D3V0KX-GP
C903 SC4D7U6D3V0KX-GP
C904 SC4D7U6D3V0KX-GP
C913 SC4D7U6D3V0KX-GP
C907 SCD22U10V2KX-1GP
C914 DY Do Not Stuff
C905 DY Do Not Stuff
C906 SCD22U10V2KX-1GP
C907 SC1KP50V3KX-GP
C915 SC1KP50V3KX-GP
C908 SC1KP50V3KX-GP
C909 SC1KP50V3KX-GP
C910 SC180P50V2JN-1GP
C911 SC180P50V2JN-1GP
C916 DY Do Not Stuff
C912 DY Do Not Stuff

0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V---DDR1333 (1.75A)

+CPU_VDDR

CPU1B 2 OF 6 DANUBB

VDDR: D10, C10, B10, AD10, W10, AC10, AB10, AA10, A10
MEMZP AE10
MEMZN AE10
VDDR_SENSE Y10 TP_CPU_VDDR_SENSE
MEMVREF W17
MA_RESET# H16 18 DDR3_A_DRAMRST#
MB_RESET# B18 DDR3_B_DRAMRST#

+0.75V_SUS_CPU_M_VREF
TP901

+1.5V_SUS
R901 39D2R2F-L-GP MEMZP
R903 39D2R2F-L-GP MEMZN
C917 SC10U6D3V5KX-1GP

+1.5V_SUS
C918 SCD1U10V2KX-5GP
R902 1KR3F-GP
+V_DDR_REF
R904 DY Do Not Stuff
C919 SC1KP50V3KX-GP
C920 SCD1U10V2KX-5GP
R905 1KR3F-GP

CLOSE TO CPU

MA0_ODT0 T19 18 MEM_MA0_ODT0
MA0_ODT1 V22 18 MEM_MA0_ODT1
MA1_ODT0 U21
MA1_ODT1 V19
MB0_ODT0 W26 MEM_MB0_ODT0 19
MB0_ODT1 W23 MEM_MB0_ODT1 19
MB1_ODT0 Y26

MA0_CS#0 T20 18 MEM_MA0_CS#0
MA0_CS#1 U19 18 MEM_MA0_CS#1
MA1_CS#0 U20
MA1_CS#1 V20
MB0_CS#0 V26 MEM_MB0_CS#0 19
MB0_CS#1 W25 MEM_MB0_CS#1 19
MB1_CS#0 U22

MA_CKE0 J22 18 MEM_MA_CKE0
MA_CKE1 J20 18 MEM_MA_CKE1
MB_CKE0 J25 MEM_MB_CKE0 19
MB_CKE1 H26 MEM_MB_CKE1 19

MA_CLK_H5 N19 18 MEM_MA_CLK0_P
MA_CLK_L5 N20 18 MEM_MA_CLK0_N
MA_CLK_H1 E16
MA_CLK_L1 F16
MA_CLK_H7 Y16
MA_CLK_L7 AA16
MA_CLK_H4 P19 18 MEM_MA_CLK1_P
MA_CLK_L4 P20 18 MEM_MA_CLK1_N
MB_CLK_H5 P22 MEM_MB_CLK0_P 19
MB_CLK_L5 R22 MEM_MB_CLK0_N 19
MB_CLK_H1 A17
MB_CLK_L1 A18
MB_CLK_H7 AF18
MB_CLK_L7 AF17
MB_CLK_H4 R26 MEM_MB_CLK1_P 19
MB_CLK_L4 R25 MEM_MB_CLK1_N 19

18 MEM_MA_ADD[0..15]
MA_ADD0 N21 MEM_MA_ADD0
MA_ADD1 M20 MEM_MA_ADD1
MA_ADD2 N22 MEM_MA_ADD2
MA_ADD3 M19 MEM_MA_ADD3
MA_ADD4 M22 MEM_MA_ADD4
MA_ADD5 L20 MEM_MA_ADD5
MA_ADD6 M24 MEM_MA_ADD6
MA_ADD7 L21 MEM_MA_ADD7
MA_ADD8 L19 MEM_MA_ADD8
MA_ADD9 K22 MEM_MA_ADD9
MA_ADD10 R21 MEM_MA_ADD10
MA_ADD11 L22 MEM_MA_ADD11
MA_ADD12 K20 MEM_MA_ADD12
MA_ADD13 V24 MEM_MA_ADD13
MA_ADD14 K24 MEM_MA_ADD14
MA_ADD15 K19 MEM_MA_ADD15
MB_ADD0 P24 MEM_MB_ADD0
MB_ADD1 N24 MEM_MB_ADD1
MB_ADD2 P26 MEM_MB_ADD2
MB_ADD3 N23 MEM_MB_ADD3
MB_ADD4 N26 MEM_MB_ADD4
MB_ADD5 L23 MEM_MB_ADD5
MB_ADD6 N25 MEM_MB_ADD6
MB_ADD7 L24 MEM_MB_ADD7
MB_ADD8 M26 MEM_MB_ADD8
MB_ADD9 K26 MEM_MB_ADD9
MB_ADD10 T26 MEM_MB_ADD10
MB_ADD11 L26 MEM_MB_ADD11
MB_ADD12 L25 MEM_MB_ADD12
MB_ADD13 W24 MEM_MB_ADD13
MB_ADD14 J23 MEM_MB_ADD14
MB_ADD15 J24 MEM_MB_ADD15
MEM_MB_ADD[0..15] 19

MA_BANK0 R20 18 MEM_MA_BANK0
MA_BANK1 R23 18 MEM_MA_BANK1
MA_BANK2 J21 18 MEM_MA_BANK2
MB_BANK0 R24 MEM_MB_BANK0 19
MB_BANK1 U26 MEM_MB_BANK1 19
MB_BANK2 J26 MEM_MB_BANK2 19

MA_RAS# R19 18 MEM_MA_RAS#
MA_CAS# T22 18 MEM_MA_CAS#
MA_WE# T24 18 MEM_MA_WE#
MB_RAS# U25 MEM_MB_RAS# 19
MB_CAS# U24 MEM_MB_CAS# 19
MB_WE# U23 MEM_MB_WE# 19

DANUB

18 M_A_DQ[63..0]

CPU1C 3 OF 6 DANUBB

M_A_DQ0	G12	MA_DATA0	MB_DATA0	C11	M_B_DQ0
M_A_DQ1	F12	MA_DATA1	MB_DATA1	A11	M_B_DQ1
M_A_DQ2	H14	MA_DATA2	MB_DATA2	A14	M_B_DQ2
M_A_DQ3	G14	MA_DATA3	MB_DATA3	B14	M_B_DQ3
M_A_DQ4	H11	MA_DATA4	MB_DATA4	G11	M_B_DQ4
M_A_DQ5	H12	MA_DATA5	MB_DATA5	E11	M_B_DQ5
M_A_DQ6	C13	MA_DATA6	MB_DATA6	D12	M_B_DQ6
M_A_DQ7	E13	MA_DATA7	MB_DATA7	A13	M_B_DQ7
M_A_DQ8	H15	MA_DATA8	MB_DATA8	A15	M_B_DQ8
M_A_DQ9	E15	MA_DATA9	MB_DATA9	A16	M_B_DQ9
M_A_DQ10	E17	MA_DATA10	MB_DATA10	A19	M_B_DQ10
M_A_DQ11	H17	MA_DATA11	MB_DATA11	A20	M_B_DQ11
M_A_DQ12	E14	MA_DATA12	MB_DATA12	C14	M_B_DQ12
M_A_DQ13	F14	MA_DATA13	MB_DATA13	D14	M_B_DQ13
M_A_DQ14	C17	MA_DATA14	MB_DATA14	C18	M_B_DQ14
M_A_DQ15	G17	MA_DATA15	MB_DATA15	D18	M_B_DQ15
M_A_DQ16	G18	MA_DATA16	MB_DATA16	D20	M_B_DQ16
M_A_DQ17	C19	MA_DATA17	MB_DATA17	A21	M_B_DQ17
M_A_DQ18	D22	MA_DATA18	MB_DATA18	D24	M_B_DQ18
M_A_DQ19	E20	MA_DATA19	MB_DATA19	C25	M_B_DQ19
M_A_DQ20	E18	MA_DATA20	MB_DATA20	B20	M_B_DQ20
M_A_DQ21	F18	MA_DATA21	MB_DATA21	C20	M_B_DQ21
M_A_DQ22	B22	MA_DATA22	MB_DATA22	B24	M_B_DQ22
M_A_DQ23	C23	MA_DATA23	MB_DATA23	C24	M_B_DQ23
M_A_DQ24	F20	MA_DATA24	MB_DATA24	E23	M_B_DQ24
M_A_DQ25	F22	MA_DATA25	MB_DATA25	E24	M_B_DQ25
M_A_DQ26	H24	MA_DATA26	MB_DATA26	G25	M_B_DQ26
M_A_DQ27	J19	MA_DATA27	MB_DATA27	G26	M_B_DQ27
M_A_DQ28	E21	MA_DATA28	MB_DATA28	C26	M_B_DQ28
M_A_DQ29	F22	MA_DATA29	MB_DATA29	D26	M_B_DQ29
M_A_DQ30	H20	MA_DATA30	MB_DATA30	G23	M_B_DQ30
M_A_DQ31	H22	MA_DATA31	MB_DATA31	G24	M_B_DQ31
M_A_DQ32	Y24	MA_DATA32	MB_DATA32	AA24	M_B_DQ32
M_A_DQ33	AB24	MA_DATA33	MB_DATA33	AA23	M_B_DQ33
M_A_DQ34	AB22	MA_DATA34	MB_DATA34	AD24	M_B_DQ34
M_A_DQ35	AA21	MA_DATA35	MB_DATA35	AE24	M_B_DQ35
M_A_DQ36	W22	MA_DATA36	MB_DATA36	AA26	M_B_DQ36
M_A_DQ37	W21	MA_DATA37	MB_DATA37	AA25	M_B_DQ37
M_A_DQ38	Y22	MA_DATA38	MB_DATA38	AD26	M_B_DQ38
M_A_DQ39	AA22	MA_DATA39	MB_DATA39	AE25	M_B_DQ39
M_A_DQ40	Y20	MA_DATA40	MB_DATA40	AC22	M_B_DQ40
M_A_DQ41	AA20	MA_DATA41	MB_DATA41	AD22	M_B_DQ41
M_A_DQ42	AA18	MA_DATA42	MB_DATA42	AE20	M_B_DQ42
M_A_DQ43	AB18	MA_DATA43	MB_DATA43	AF20	M_B_DQ43
M_A_DQ44	AB21	MA_DATA44	MB_DATA44	AF24	M_B_DQ44
M_A_DQ45	AD21	MA_DATA45	MB_DATA45	AF23	M_B_DQ45
M_A_DQ46	AD19	MA_DATA46	MB_DATA46	AC20	M_B_DQ46
M_A_DQ47	Y18	MA_DATA47	MB_DATA47	AD20	M_B_DQ47
M_A_DQ48	AD17	MA_DATA48	MB_DATA48	AD18	M_B_DQ48
M_A_DQ49	W16	MA_DATA49	MB_DATA49	AE18	M_B_DQ49
M_A_DQ50	W14	MA_DATA50	MB_DATA50	AC14	M_B_DQ50
M_A_DQ51	Y14	MA_DATA51	MB_DATA51	AD14	M_B_DQ51
M_A_DQ52	Y17	MA_DATA52	MB_DATA52	AF19	M_B_DQ52
M_A_DQ53	AB17	MA_DATA53	MB_DATA53	AC18	M_B_DQ53
M_A_DQ54	AB15	MA_DATA54	MB_DATA54	AF16	M_B_DQ54
M_A_DQ55	AD15	MA_DATA55	MB_DATA55	AF15	M_B_DQ55
M_A_DQ56	AB13	MA_DATA56	MB_DATA56	AE13	M_B_DQ56
M_A_DQ57	AD13	MA_DATA57	MB_DATA57	AC12	M_B_DQ57
M_A_DQ58	Y12	MA_DATA58	MB_DATA58	AB11	M_B_DQ58
M_A_DQ59	W11	MA_DATA59	MB_DATA59	Y11	M_B_DQ59
M_A_DQ60	AB14	MA_DATA60	MB_DATA60	AE14	M_B_DQ60
M_A_DQ61	AA14	MA_DATA61	MB_DATA61	AF14	M_B_DQ61
M_A_DQ62	AB12	MA_DATA62	MB_DATA62	AE11	M_B_DQ62
M_A_DQ63	AA12	MA_DATA63	MB_DATA63	AD11	M_B_DQ63

18 M_A_DQ[63..0] 19

18 M_A_DM[7..0]

M_A_DM0	E12	MA_DM0	MB_DM0	A12	M_B_DM0
M_A_DM1	C15	MA_DM1	MB_DM1	B16	M_B_DM1
M_A_DM2	E19	MA_DM2	MB_DM2	A22	M_B_DM2
M_A_DM3	F24	MA_DM3	MB_DM3	E25	M_B_DM3
M_A_DM4	AC24	MA_DM4	MB_DM4	AB26	M_B_DM4
M_A_DM5	Y19	MA_DM5	MB_DM5	AE22	M_B_DM5
M_A_DM6	AB16	MA_DM6	MB_DM6	AC16	M_B_DM6
M_A_DM7	Y13	MA_DM7	MB_DM7	AD12	M_B_DM7

M_B_DM[7..0] 19

18 M_A_DQS0	G13	MA_DQS_H0	MB_DQS_H0	C12	M_B_DQS0 19
18 M_A_DQS#0	H13	MA_DQS_L0	MB_DQS_L0	B12	M_B_DQS#0 19
18 M_A_DQS1	G16	MA_DQS_H1	MB_DQS_H1	D16	M_B_DQS1 19
18 M_A_DQS#1	G15	MA_DQS_L1	MB_DQS_L1	C16	M_B_DQS#1 19
18 M_A_DQS2	C22	MA_DQS_H2	MB_DQS_H2	A24	M_B_DQS2 19
18 M_A_DQS#2	C21	MA_DQS_L2	MB_DQS_L2	A23	M_B_DQS#2 19
18 M_A_DQS3	G22	MA_DQS_H3	MB_DQS_H3	F26	M_B_DQS3 19
18 M_A_DQS#3	G21	MA_DQS_L3	MB_DQS_L3	E26	M_B_DQS#3 19
18 M_A_DQS4	AD23	MA_DQS_H4	MB_DQS_H4	AC25	M_B_DQS4 19
18 M_A_DQS#4	AC23	MA_DQS_L4	MB_DQS_L4	AC26	M_B_DQS#4 19
18 M_A_DQS5	AB19	MA_DQS_H5	MB_DQS_H5	AF21	M_B_DQS5 19
18 M_A_DQS#5	AB20	MA_DQS_L5	MB_DQS_L5	AF22	M_B_DQS#5 19
18 M_A_DQS6	Y15	MA_DQS_H6	MB_DQS_H6	AE16	M_B_DQS6 19
18 M_A_DQS#6	W15	MA_DQS_L6	MB_DQS_L6	AD16	M_B_DQS#6 19
18 M_A_DQS7	W12	MA_DQS_H7	MB_DQS_H7	AF12	M_B_DQS7 19
18 M_A_DQS#7	W13	MA_DQS_L7	MB_DQS_L7	AE12	M_B_DQS#7 19

DANUB

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR(2/4)
Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01
Date: Tuesday, April 13, 2010 | Sheet 9 of 90

SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

+2.5V_RUN
+2.5V_RUN_VDDA
L1001
PBY160808T-330Y-N-GP
SC180P50V2JN-1GP
SC4D7U6D3V3KX-GP
SC22U10V2KX-1GP
SC330P50V2KX-1GP
C1001
C1002
C1003
C1004
1119

Cloce To CPU
R1008 169R2F-GP
SC3900P50V2KX-2GP
SC3900P50V2KX-2GP
C1005
C1006
CPU_CLK(200MHz)
20 CPU_CLK
20 CPU_CLK#
CPUCLK_IN
CPUCLK_IN#

CPU_R_LDT_RST#
For HDT DBG
HDT_RST_R#
R1009
Do Not Stuff
C1007
Close CPU
X00
EC1001
CPU_R_LDT_PWRGD
CPU_R_LDT_STOP#
CPU_LDT_REQ#
CPU_SIC
CPU_SID
CPU_ALERT#

+1.1V_RUN
R1010
R1011
44D2R2F-GP
CPU_HTREF0
CPU_HTREF1
47 CPU_VDD0_RUN_FB_H
47 CPU_VDD0_RUN_FB_L
0212
TP1008
TP1009
CPU_VDD1_RUN_FB_H
CPU_VDD1_RUN_FB_L

CPU1D
4 OF 6
DANUB
F8 VDDA
F9 VDDA
A9 CLKIN_H
A8 CLKIN_L
B7 RESET#
A7 PWROK
F10 LDTSTOP#
C6 LDTREQ#
AF4 SIC
AF5 SID
AE6 ALERT#
R6 HT_REF0
P6 HT_REF1
F6 VDD0_FB_H
E6 VDD0_FB_L
Y6 VDD1_FB_H
AB6 VDD1_FB_L
G10 DBRDY
AA9 TMS
AC9 TCK
AD9 TRST#
AF9 TDI
AD7 TEST23
H10 TEST18
G9 TEST19
E9 TEST25_H
E8 TEST25_L
AB8 TEST21
AF7 TEST20
AE7 TEST24
AE8 TEST22
AC8 TEST12
AF8 TEST27
C2 TEST9
AA6 TEST6
A3 RSVD#A3
A5 RSVD#A5
B3 RSVD#B3
B5 RSVD#B5
C1 RSVD#C1
M11 VSS
W18 RSVD#W18
A6 SVC
A4 SVD
AF6 THERMTRIP#
AC7 PROCHOT#
AA8 MEMHOT#
W7 THERMDC
W8 THERMDA
W9 VDDIO_FB_H
Y9 VDDIO_FB_L
H6 VDDNB_FB_H
G6 VDDNB_FB_L
E10 DBREQ#
AE9 TDO
J7 TEST28_H
H8 TEST28_L
D7 TEST17
E7 TEST16
F7 TEST15
C7 TEST14
C3 TEST7
K8 TEST10
C4 TEST8
C9 TEST29_H
C8 TEST29_L
H18 RSVD#H18
H19 RSVD#H19
AA7 RSVD#AA7
D5 RSVD#D5
C5 RSVD#C5

X01
+1.5V_SUS
1119
RN1006
SRN1KJ-7-GP
1KR2J-1-GP
R1006
300R2J-4-GP
R1007
CPU_SVC
CPU_SVD
CPU_THERMTRIP#
CPU_PROCHOT#
CPU_MEMHOT#
TP1002
CPU_PROCHOT# 20
S1G4 not support MEMHOT
H_THERMDC 39
H_THERMDA 39
TP_CPU_VDDIO_SUS_FB_H
TP_CPU_VDDIO_SUS_FB_L
CPU_VDDNB_RUN_FB_H 47
CPU_VDDNB_RUN_FB_L 47
R1015
300R2J-4-GP
+1.5V_SUS
CPU_DBREQ#
CPU_TDO
TP_CPU_TEST17
TP_CPU_TEST16
TP_CPU_TEST15
TP_CPU_TEST14
+1.1V_RUN
R1021
Do Not Stuff
CPU_TEST10

+1.5V_RUN
R1012 Do Not Stuff CPU_LDT_REQ#
R1013 Do Not Stuff CPU_DBRDY
R1014 Do Not Stuff TP_CPU_TEST14
R1016 Do Not Stuff TP_CPU_TEST15
RN1002 SRN1KJ-7-GP CPU_TEST18 CPU_TEST19
RN1004 SRN1KJ-7-GP CPU_TEST24 CPU_TEST22
RN1003
CPU_TEST23
CPU_TEST12
CPU_TEST20
CPU_TEST21
X01
SRN1KJ-7-GP

+1.5V_SUS
to power IC FB
R1018 Do Not Stuff
R1019 510R2F-L-GP
R1020 510R2F-L-GP
R1022 Do Not Stuff
CPU_TEST23
CPU_TEST18
CPU_TEST19
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST21
CPU_TEST20
CPU_TEST24
CPU_TEST22
CPU_TEST12
CPU_TEST27
R1023 CPU_TEST9
Do Not Stuff

LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

+1.5V_SUS
R1026
1KR2J-1-GP
CPU_TEST27
R1029
Do Not Stuff
TP1001 TP_CPU_VDDIO_SUS_FB_H
TP1003 TP_CPU_VDDIO_SUS_FB_L
TP1006 TP_CPU_TEST17
TP1007 TP_CPU_TEST16

+1.5V_SUS
1119
RN1005
SRN1KJ-7-GP
R1032
2K2R2J-2-GP
R1033
1KR2J-1-GP
21 CPU_SIC
21 CPU_SID
21,39 TALERT#
Q1001
PMBS3904-1-GP

+KBC_PWR
+1.5V_RUN
R1027
Do Not Stuff
R1028
2K2R2J-2-GP
21,37,39,42 H_THERMTRIP#
Q1002
PMBS3904-1-GP

X01
For old HDT tool (3.3V level)
+3.3V_RUN
+1.5V_RUN
R1040
10KR2J-3-GP
R1039
2K2R2J-2-GP
37 CPU_PROCHOT#_EC
Q1005
PMBS3904-1-GP

+3.3V_RUN
+1.8V_RUN
R1037
Do Not Stuff
R1036
Do Not Stuff
HDT_RST#
HDT_RST_R#
Q1004
Do Not Stuff

+3.3V_RUN
+1.8V_RUN
R1034
10KR2J-3-GP
R1035
2K2R2J-2-GP
47 CPU_PWRGD_SVID_REG
CPU_R_LDT_PWRGD
Q1003
PMBS3904-1-GP
X01
R1041
Do Not Stuff

HDT Connectors

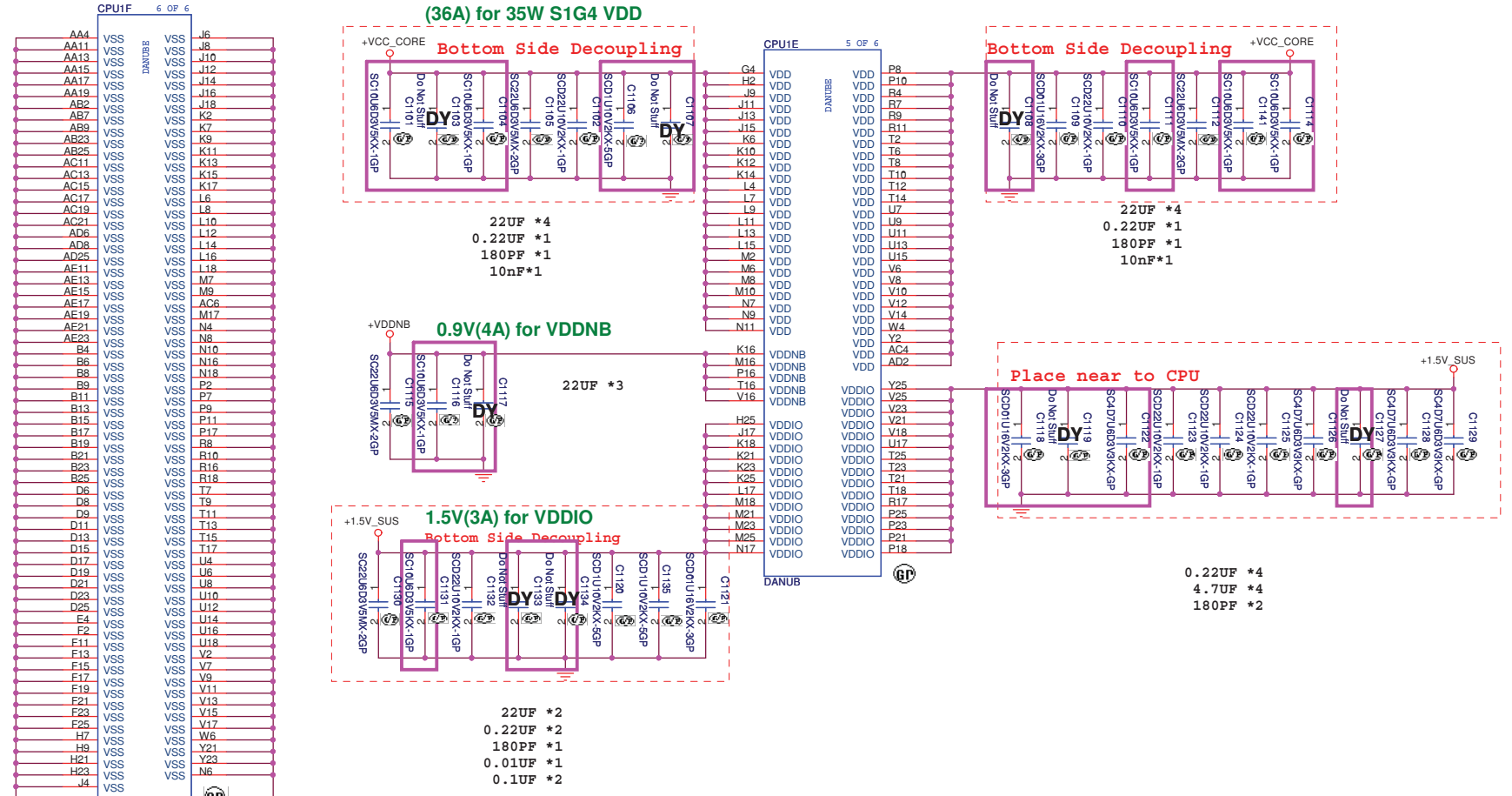
HDT1
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
+1.5V_SUS
1.5V
CPU_R_LDT_RST#
R1038
Do Not Stuff
HDT_RST#
3.3V

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)
Size: Custom
Document Number: Chelsea DJ2 AMD UMA
Rev: X01
Date: Tuesday, April 13, 2010
Sheet 10 of 90

SSID = CPU



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

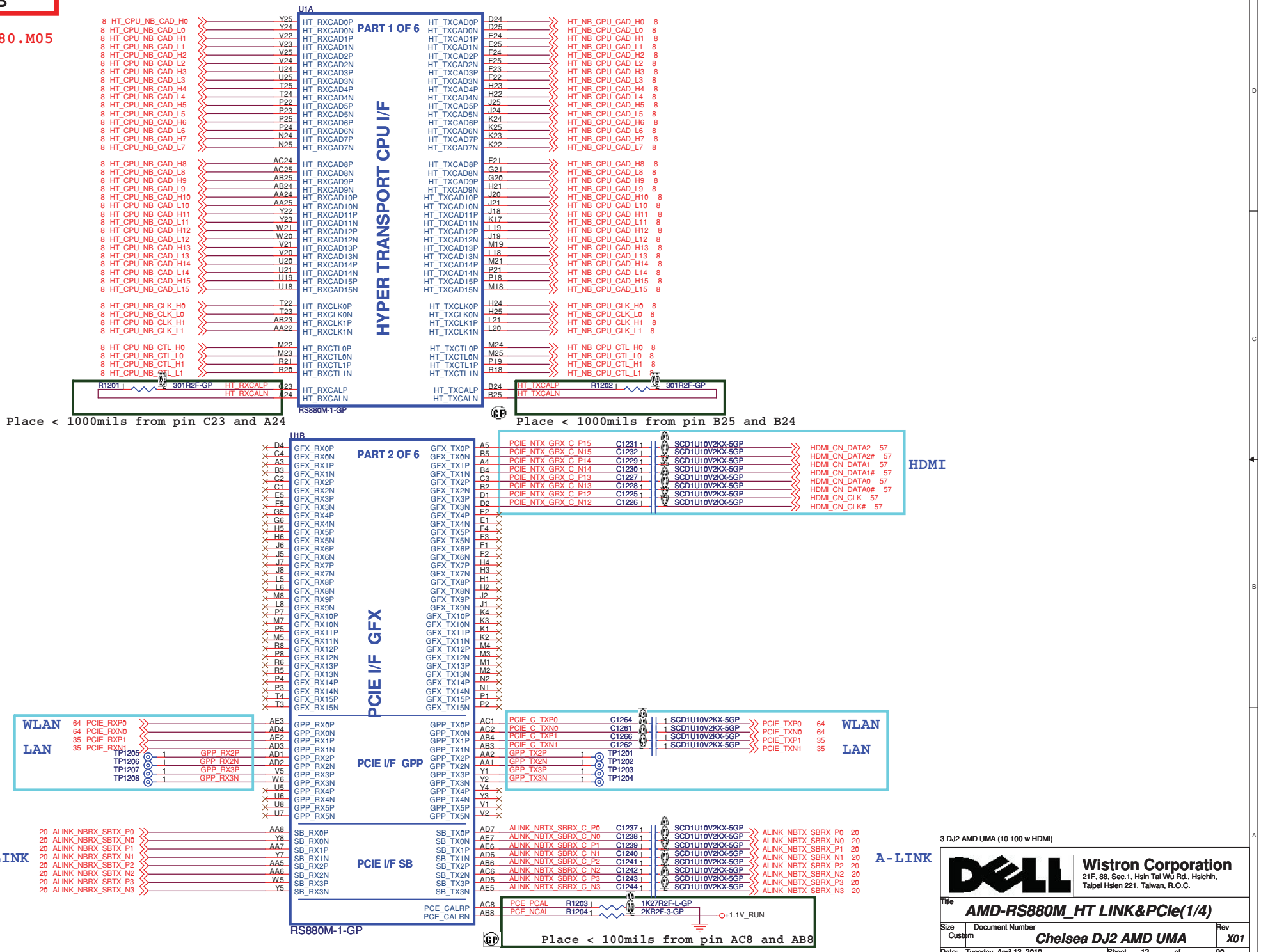
Title: CPU_Power_(4/4)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 11 of 90

SSID = N.B

RS880M : 71.RS880.M05



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_HT LINK&PCIe(1/4)

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 12 of 90

SSID = N.B

RS880M : 71.RS880.M05

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use VGA_VSYNC)

Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use VGA_HSYNC)

*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)

Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT

+1.1V_RUN — L1308 BLM15AG221SS1D-GP 220 ohm 300mA — 65mA — PLLVDD — C1312 SC2D2U6D3V3KX-GP

+1.8V_RUN — R1323 Do Not Stuff — PLLVDD18 — C1311 SC1U10V3KX-3GP

+3.3V_RUN — R1342 Do Not Stuff — +3.3V_RUN_AVDD — 110mA — C1307 SC1U10V3KX-3GP

+1.8V_RUN — 20mA — C1306 SCD1U10V2KX-5GP

+1.8V_RUN — 4mA — C1308 SCD1U10V2KX-5GP

+3.3V_RUN — R1302 3KR2J-2-GP — R1303 3KR2J-2-GP — VGA_VSYNC — VGA_HSYNC — R1304 Do Not Stuff — R1305 Do Not Stuff

Layout Note
Trace at least 15 mil

+1.8V_RUN — R1324 Do Not Stuff — 20mA — C1302 SCD1U10V2KX-5GP — C1303 — R1325 Do Not Stuff — 120mA — C1304 SCD1U10V2KX-5GP — C1305 — C1301 Do Not Stuff

TV_OUT

X00

55 M_RED — R1326 150R2F-1-GP
55 M_GREEN — R1327 150R2F-1-GP
55 M_BLUE — R1328 150R2F-1-GP

55 VGA_HSYNC — VGA_HSYNC
55 VGA_VSYNC — VGA_VSYNC
55 DDC_CLK_CON — DDC_CLK_CON
55 DDC_DATA_CON — DDC_DATA_CON

UMA: DAC_CLK and DATA with
5V-tolerant.not need level shift

R1306 715R2F-GP — DAC_RSET

Trace at least 10 mil

+1.8V_VDDA18HTPLL — +1.8V_VDDA18PCIEPLL

20 PLTRST#_NB_GPU — 41 NB_PWRGD_IN — NB_LDT_STOP# — NB_ALLOW_LDTSTOP

20 CLK_NBHT_CLK — 20 CLK_NBHT_CLK# — HT_REFCLKP — HT_REFCLKN

X01

20 NB_REFCLK_P — 20 NB_REFCLK_N — REFCLK_P/OSCIN — REFCLK_N

+3.3V_RUN — RN1302 SRN4K7J-8-GP — NB_GFX_CLK — NB_GFX_CLK# — GFX_REFCLKP — GFX_REFCLKN

TP1307 — TP1308 — NB_GPP_CLK — NB_GPP_CLK# — GPP_REFCLKP — GPP_REFCLKN

20 NB_GPPSB_CLK — 20 NB_GPPSB_CLK# — GPPSB_REFCLKP — GPPSB_REFCLKN

54 LDDC_CLK — 54 LDDC_DATA — 57 DDC_DATA_HDMI — 57 DDC_CLK_HDMI — I2C_CLK — I2C_DATA — DDC_DATA0/AUX0N — DDC_CLK0/AUX0P — DDC_CLK1/AUX1P — DDC_DATA1/AUX1N

TP1303 — TP1304 — TP_NB_DDC_CLK1 — TP_NB_DDC_DATA1

TP1305 — TP_STRP_DATA — TP_NB_RESERVED — STRP_DATA — RESERVED

R1318 2KR2J-1-GP — R1319 — RS780_AUX_CAL — 150R2F-1-GP — AUX_CAL

U1C — PART 3 OF 6

RS880M-1-GP

CRT/TVOUT: AVDD1 AVDD2 AVDDI AVSSDI AVDDQ AVSSQ C_Pr Y COMP_Pb RED REDb GREEN GREENb BLUE BLUEb DAC_HSYNC DAC_VSYNC DAC_SCL DAC_SDA DAC_RSET

PLL PWR: PLLVDD PLLVDD18 PLLVSS VDDA18HTPLL VDDA18PCIEPLL1 VDDA18PCIEPLL2 — 20mA — 120mA

LVTM: TXOUT_L0P TXOUT_L0N TXOUT_L1P TXOUT_L1N TXOUT_L2P TXOUT_L2N TXOUT_L3P TXOUT_L3N TXOUT_U0P TXOUT_U0N TXOUT_U1P TXOUT_U1N TXOUT_U2P TXOUT_U2N TXOUT_U3P TXOUT_U3N TXCLK_LP TXCLK_LN TXCLK_UP TXCLK_UN

CLOCKs PM: SYSRESET# POWERGOOD LDTSTOP# ALLOW_LDTSTOP

MIS.: TMDS_HPD HPD SUS_STAT# THERMALDIODE_P THERMALDIODE_N TESTMODE

VGA_TXAOUT0+ 54 — VGA_TXAOUT0- 54 — VGA_TXAOUT1+ 54 — VGA_TXAOUT1- 54 — VGA_TXAOUT2+ 54 — VGA_TXAOUT2- 54

VGA_TXACLK+ 54 — VGA_TXACLK- 54

VDDLTP18 — VSSLTP18 — VDDLT18_1 VDDLT18_2 VDDLT33_1 VDDLT33_2 — VSSLT1 VSSLT2 VSSLT3 VSSLT4 VSSLT5 VSSLT6 VSSLT7

+1.8V_RUN — 220 ohm 300mA — L1305 BLM15AG221SS1D-GP — R1329 0R3J-0-U-GP — 15mA — 300mA — C1310 SCD1U10V2KX-5GP — C1313 SC1U10V3KX-3GP — C1309

LVDS_DIGON — LVDS_BLON — LVDS_ENA_BL — LCDVDD_EN 54 — LBKLT_CTL 54 — PANEL_BKEN 37

RN1301 SRN4K7J-8-GP — X00

TMDS_HPD — TP1311 — HDMI_HPD_DET 57

SUS_STAT# — R1317 Do Not Stuff — SUS_STAT# 21

TESTMODE_NB — R1320 1K8R2F-GP

+1.5V_RUN — R1309 300R2J-4-GP — R1322 DY Do Not Stuff — +1.8V_RUN — R1311 2K2R2J-2-GP

20 CPU_LDT_STOP# — U1301 SN74LVC2G07DCKR-GP — NB_LDT_STOP# — C1314 SCD1U10V2KX-5GP

+1.8V_RUN — R1315 1KR2J-1-GP

20 ALLOW_LDTSTOP — R1316 Do Not Stuff — NB_ALLOW_LDTSTOP

ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted

X01

NB_GFX_CLK — NB_GFX_CLK# — RN1303 SRN4K7J-8-GP

+3.3V_RUN — R1314 4K7R2J-2-GP — NB_SUS_STAT# — R1321 DY Do Not Stuff

3 DJ2 AMD UMA (10 100 w HDMI)

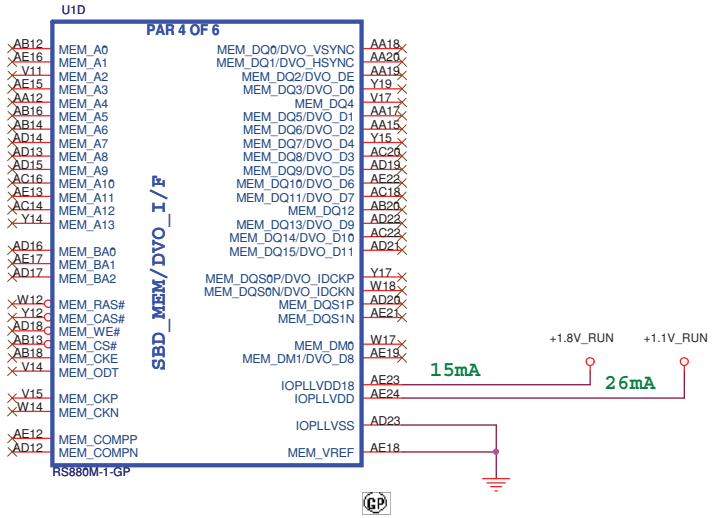
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_LVDS&CRT_(2/4)

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 13 of 90

SSID = N.B



3 DJ2 AMD UMA (10 100 w HDMI)

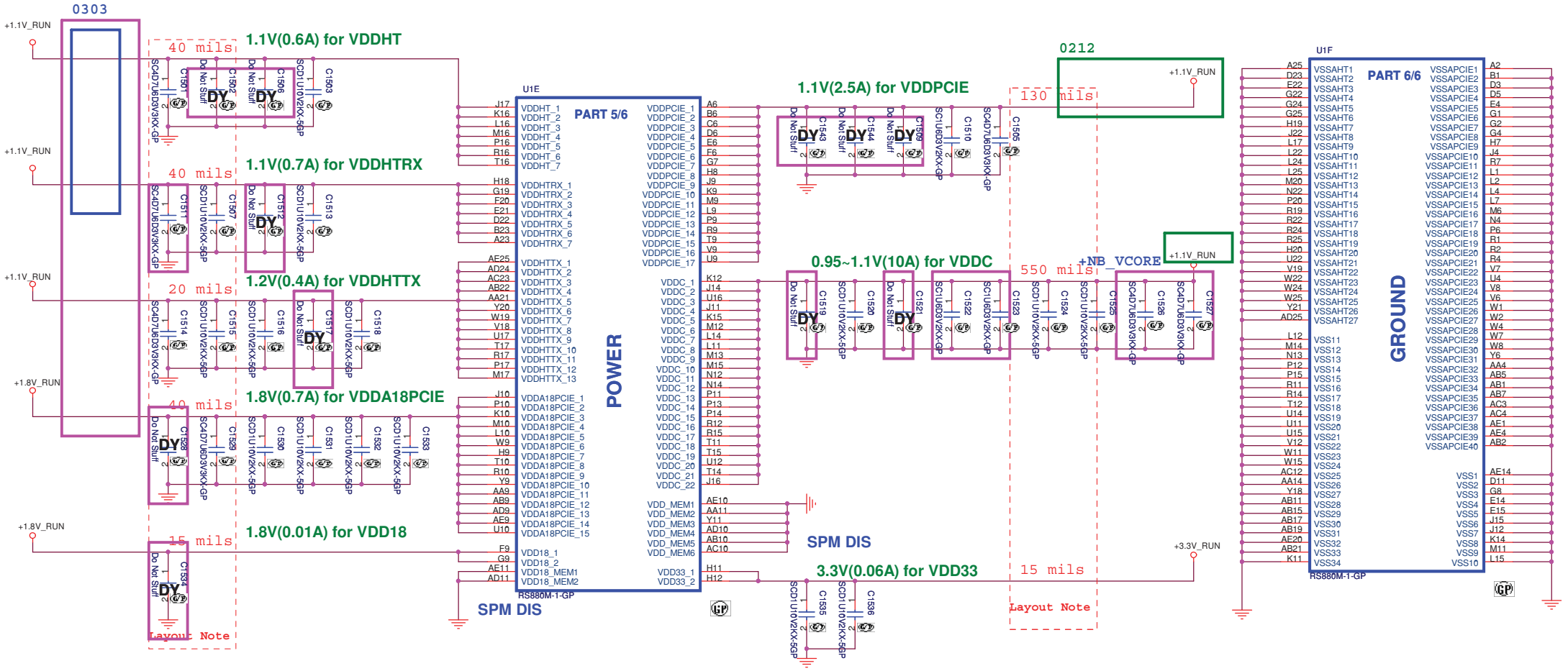
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_SidePort_(3/4)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 14 of 90

SSID = N.B



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_PWR&GD_(4/4)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 15 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*X01*

Date: Tuesday, April 13, 2010 Sheet 16 of 90

(Blanking)

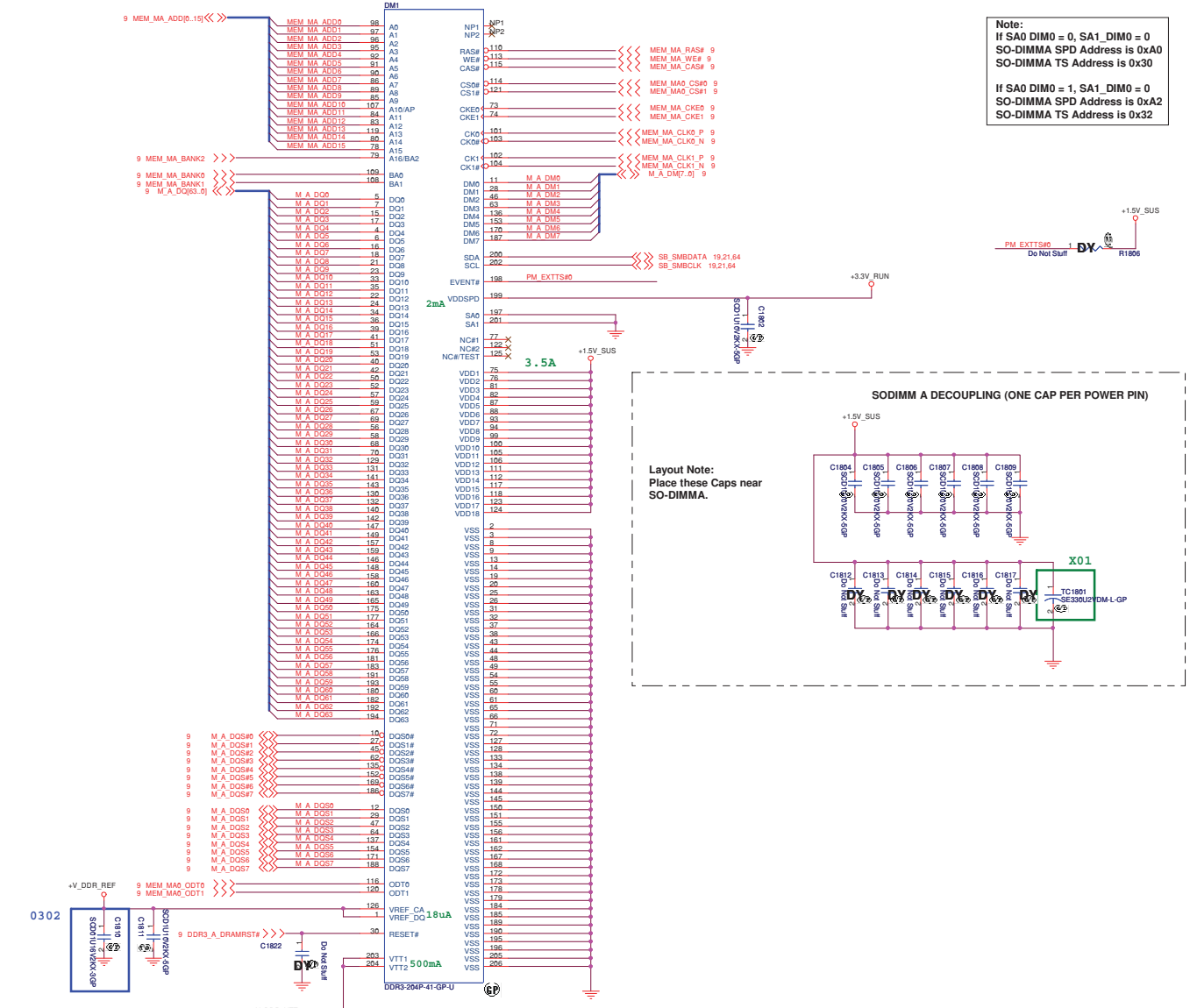
3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 17 of 90



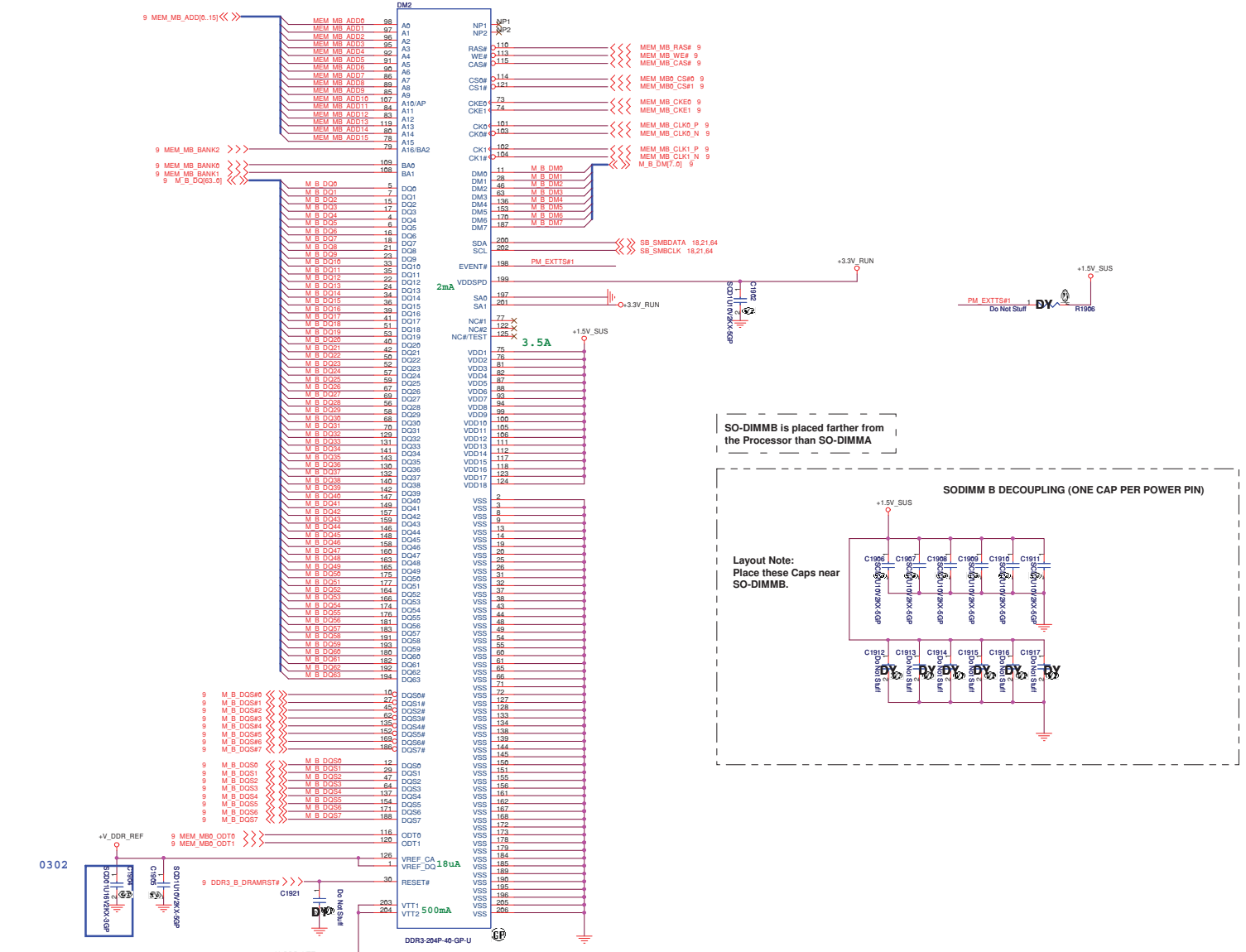
3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 18 of 90



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR3-SODIMM2
Size	Document Number: Chelsea DJ2 AMD UMA
Rev	X01
Date: Tuesday, April 13, 2010	Sheet 19 of 90

3 DJ2 AMD UMA (10 100 w HDMI)

SSID = S.B

SB700 A12 : 71.SB8[illegible].M02

placed CAP
closed SB820M

Place R <100mils form pins AD29,AD28

NOTE: SB8XX ONLY SUPPORTS 2 GPP
PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

1nd 82.30020.851
2nd 82.30020.791

1'nd 73.01G08.DHG
2'nd 73.01G08.L04

1'nd 73.01G08.DHG
2'nd 73.01G08.L04

STRAP PIN

LPC Bus Routing first connects to MINICARD then connects to KBC

3 DJ2 AMD UMA (10 100 w HDMI)

82.30001.661

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_PCIE&PCI_(1/5)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 20 of 90

SSID = S.B

USB	
Pair	Device
0	USB2
1	USB3
2	USB0 (I/O Board)
3	USB1 (I/O Board, 17")
4	WLAN
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	RESERVED
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	RESERVED

HDMI pull down
non-HDMI pull-up(internal)

SBD DDR RESET

not use

Close SB

GbE Controller Not Enabled

EC Not Implemented

JTAG_TDI
JTAG_RST#

EC Not Implemented

Not use

Strap Pin / define to use LPC or SPI ROM

3 DJ2 AMD UMA (10 100 w HDMI)

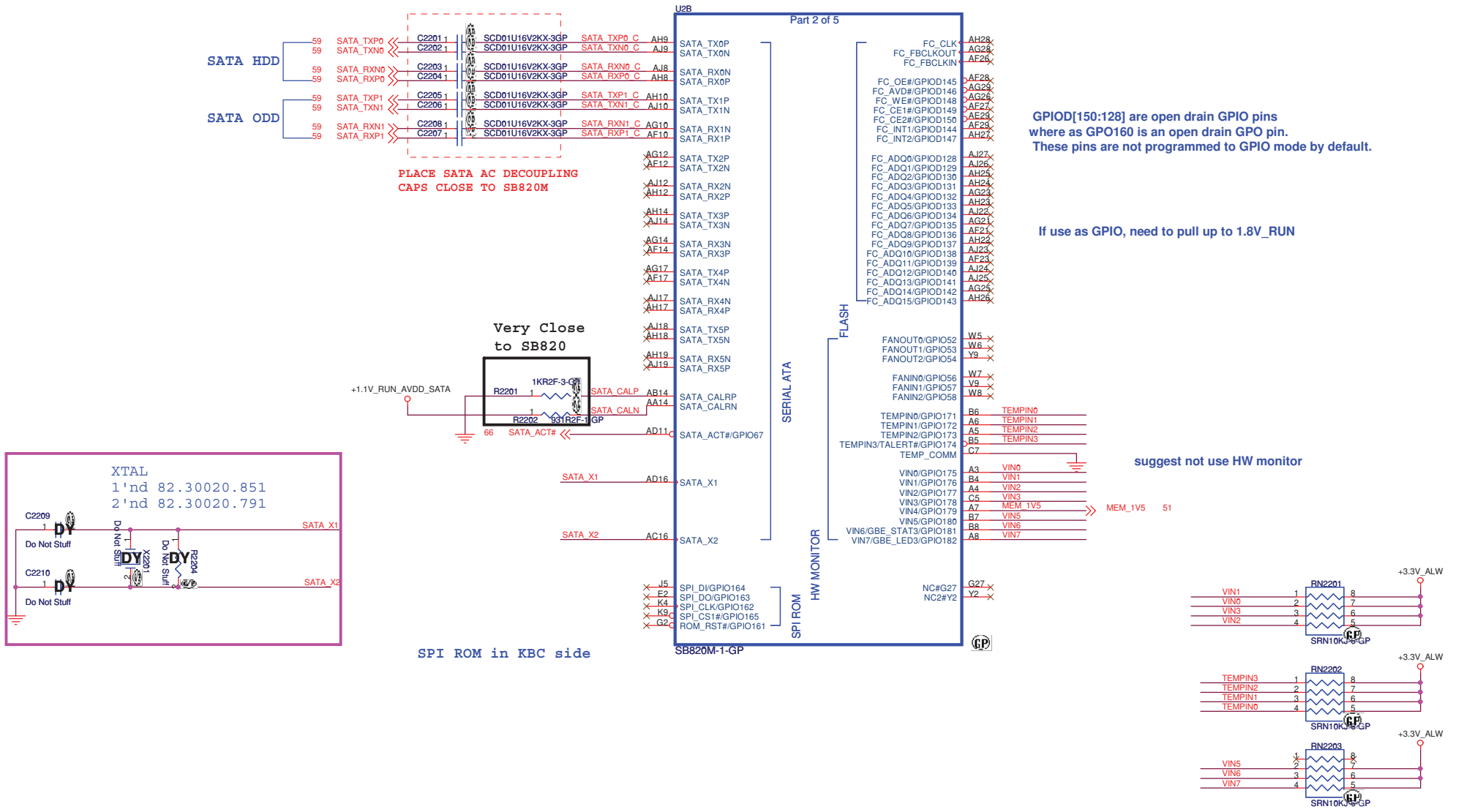
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_USB&GPIO_(2/5)

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Wednesday, April 14, 2010 | Sheet 21 of 90

SSID = S.B

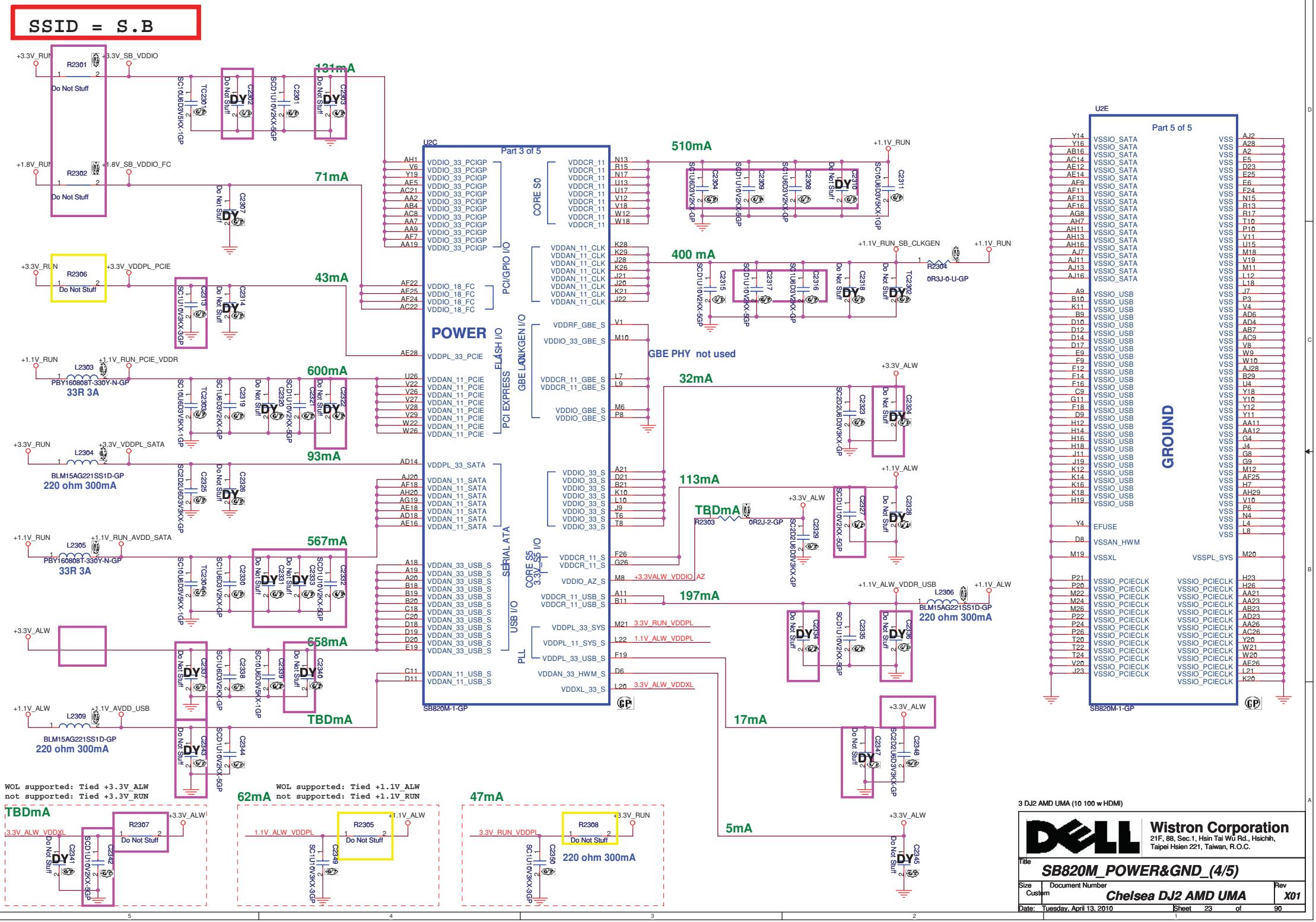


3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SB820M_SATA-IDE_(3/5)	
Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 22 of 90	

SSID = S.B



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

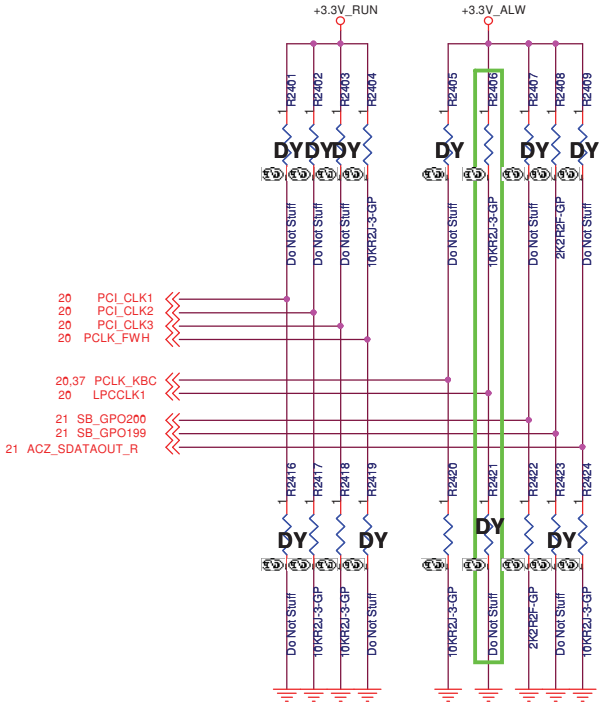
Title: SB820M_POWER&GND_(4/5)

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

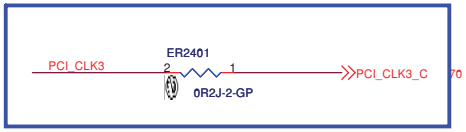
Date: Tuesday, April 13, 2010 | Sheet 23 of 90

SSID = S.B

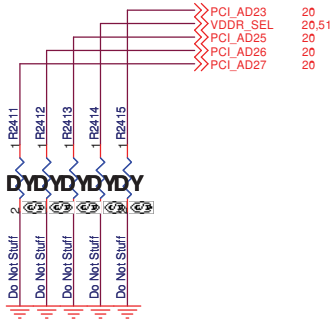
REQUIRED STRAPS



0309



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 25 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 26 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 27 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 28 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

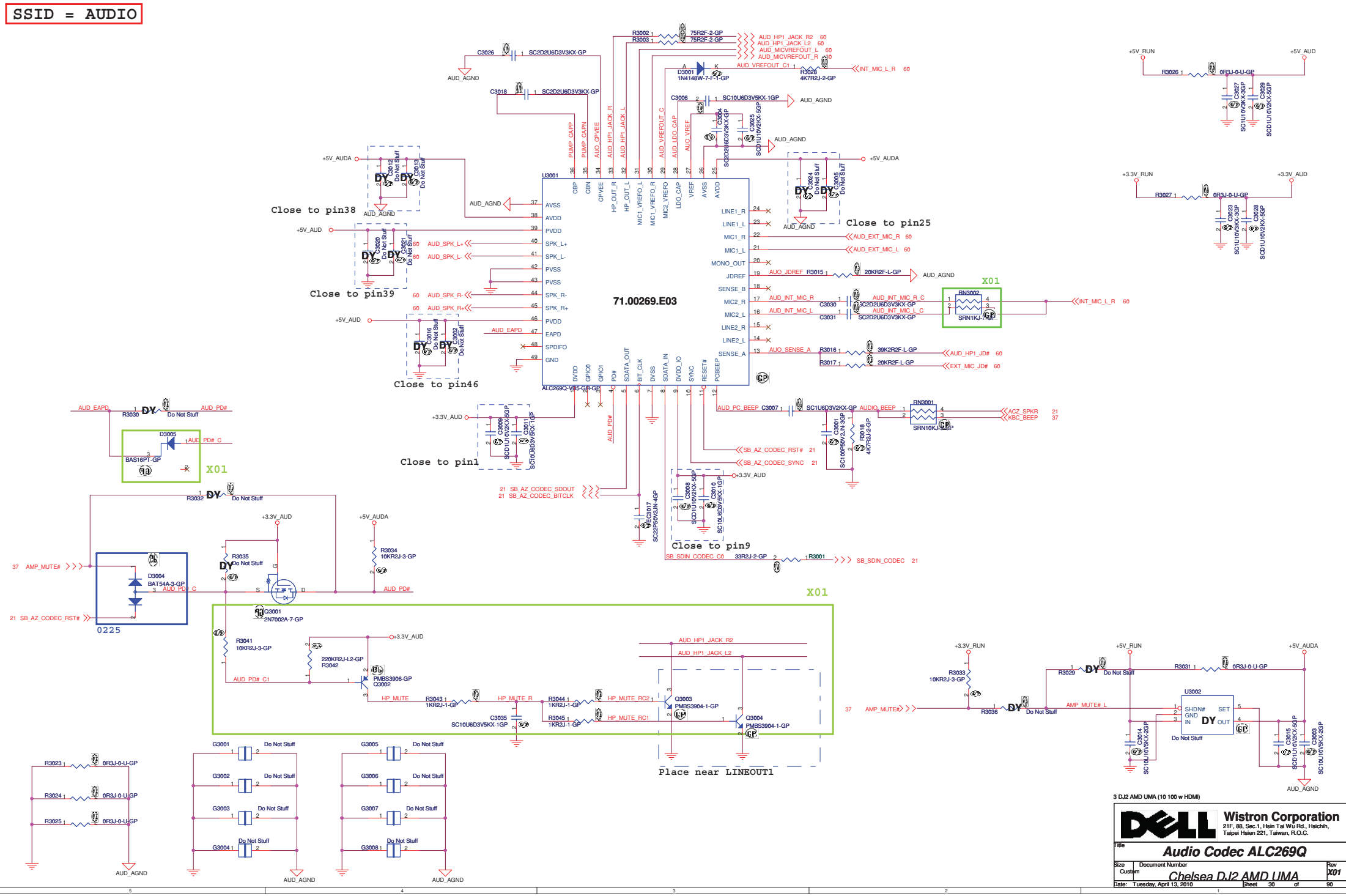
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 29 of 90

SSID = AUDIO


U3001
71.00269.E03
ALC269Q-VB5-GR-GP
Close to pin38
Close to pin39
Close to pin46
Close to pin1
Close to pin9
Close to pin25
Place near LINEOUT1
X01
0225
AUDIO_BEEP
AUD_AGND
+5V_AUDA
+5V_AUD
+3.3V_AUD
+5V_RUN
+3.3V_RUN
AUD_EAPD
AUD_PD#
AUD_PD# C
AUD_PD# C1
AMP_MUTE#
SB_AZ_CODEC_RST#
SB_AZ_CODEC_SYNC
SB_AZ_CODEC_SDOUT
SB_AZ_CODEC_BITCLK
SB_SDIN_CODEC
HP_MUTE
HP_MUTE_R
HP_MUTE_RC1
HP_MUTE_RC2
AUD_HP1_JACK_R2
AUD_HP1_JACK_L2
AUD_EXT_MIC_R
AUD_EXT_MIC_L
INT_MIC_L_R
AUD_HP1_JD#
EXT_MIC_JD#
ACZ_SPKR
KBC_BEEP
AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_R-
AUD_SPK_R+
AUD_VREFOUT_C1
AUD_JDREF
AUD_SENSE_A
AUD_PC_BEEP
AUD_INT_MIC_R
AUD_INT_MIC_L
AUD_INT_MIC_R_C
AUD_INT_MIC_L_C
R3002
R3003
R3026
R3027
R3015
R3016
R3017
R3030
R3032
R3034
R3035
R3041
R3042
R3043
R3044
R3045
R3029
R3031
R3033
R3036
R3001
RN3002
RN3001
D3001
D3004
D3005
Q3001
Q3002
Q3003
Q3004
U3002
G3001
G3002
G3003
G3004
G3005
G3006
G3007
G3008
3 DJ2 AMD UMA (10 100 w HDMI)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec ALC269Q
Size
Custom
Document Number
Chelsea DJ2 AMD UMA
Rev
X01
Date: Tuesday, April 13, 2010
Sheet 30 of 90

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3 DJ2 AMD UMA (10 100 w HDMI)

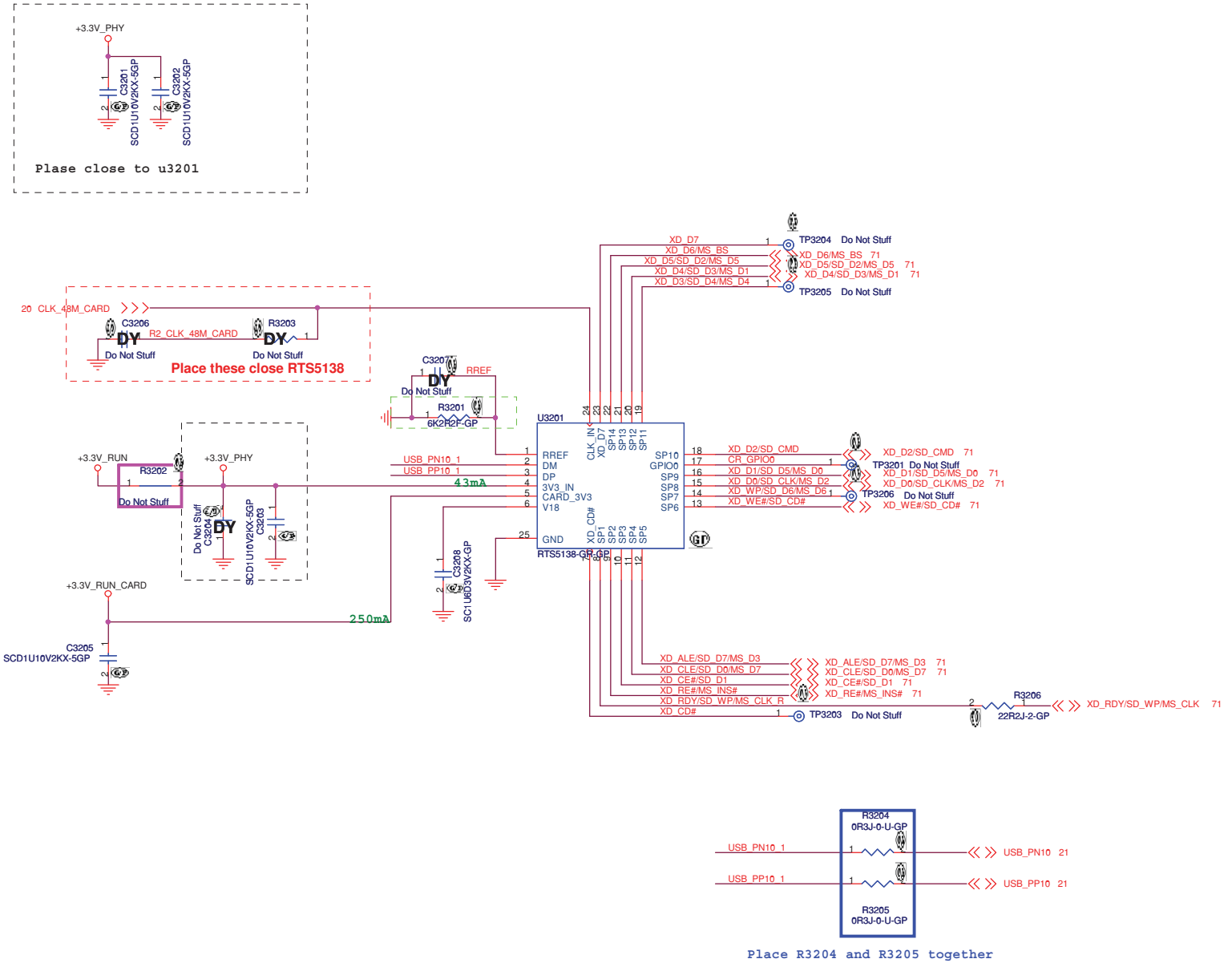
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 31 of 90

SSID = SDIO



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 33 of 90

(Blanking)

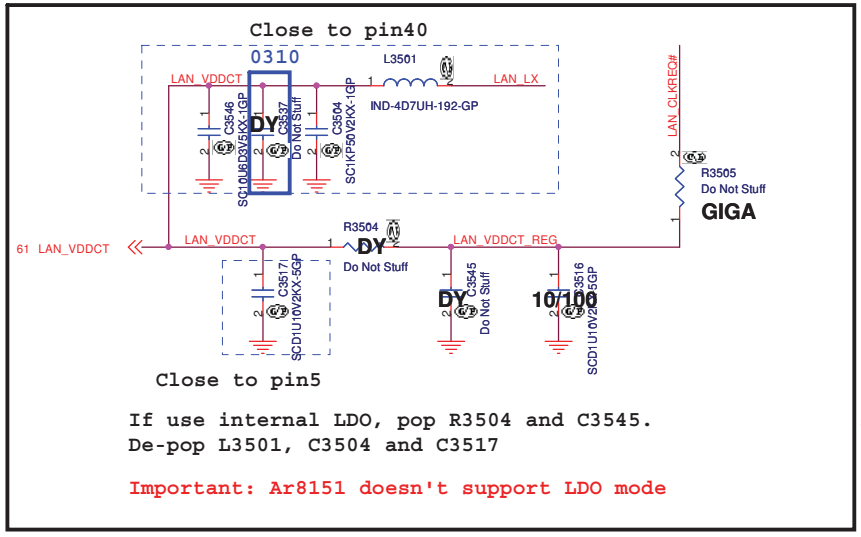
3 DJ2 AMD UMA (10 100 w HDMI)

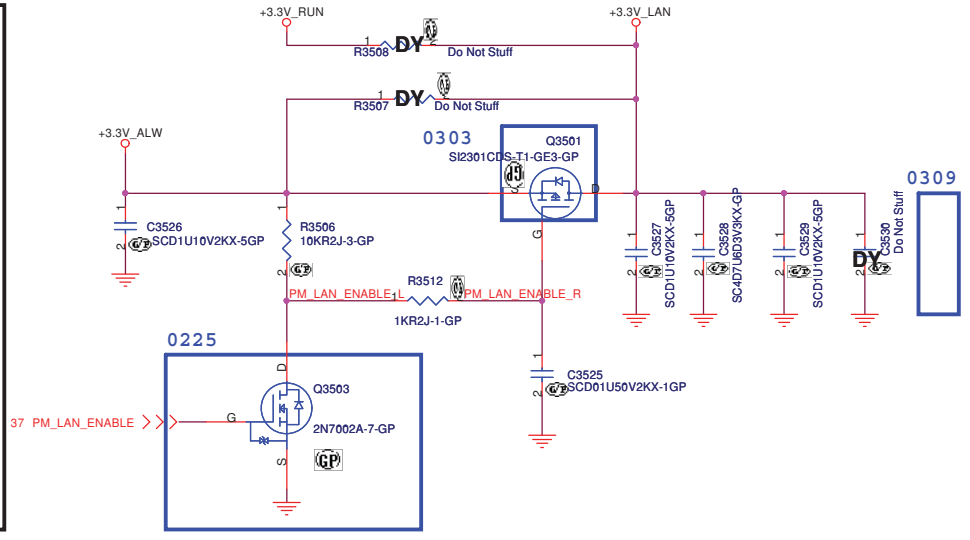
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

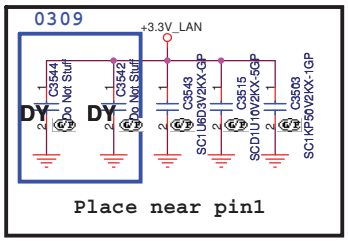
Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

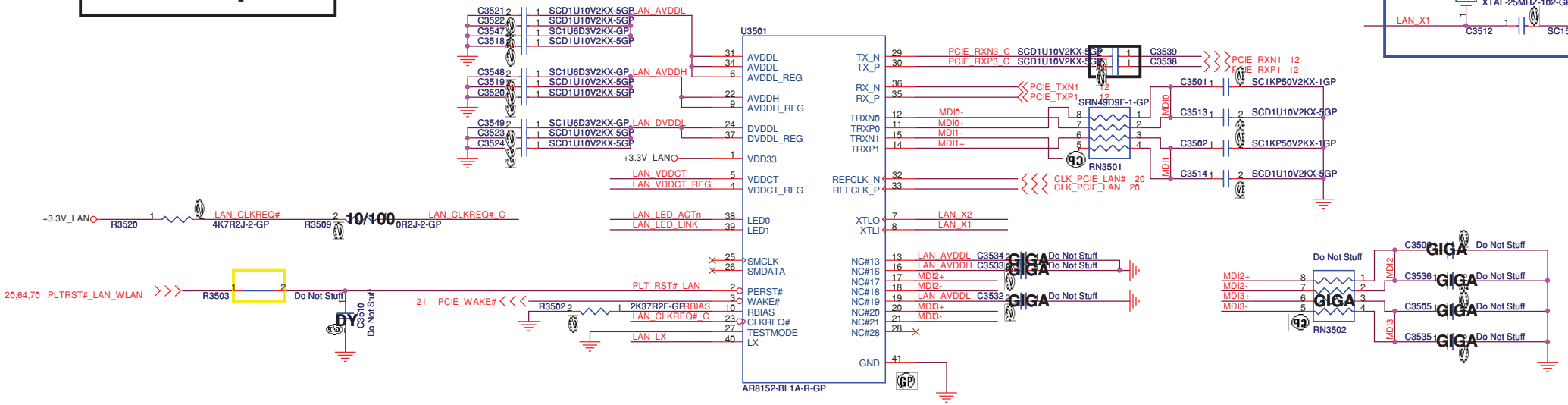
Date: Tuesday, April 13, 2010 | Sheet 34 of 90

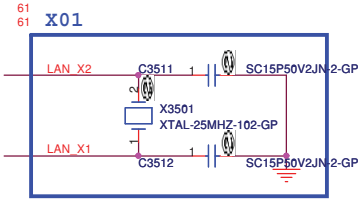




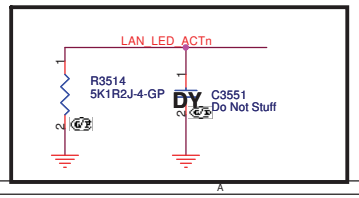


Pin6 is the AVDDL LDO output, 1uF+0.1uF(C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF(C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF(C3549 and C3523) close to Pin37;
C3524 close to Pin24.

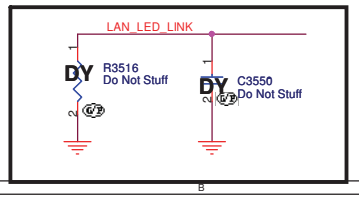




If overclocking, de-pop R3514 and C3551



If use LDO mode, pop R3516 and C3550



GIGA LAN use 71.08151.003

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AR8152/AR8151

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 35 of 90

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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SSID = KBC

CAP close to VCC-GND pin pair

MB VERSION ID			
	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

KBC CLK
EMI

Place close to KBC

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size	Document Number	Rev
A2	Chelsea DJ2 AMD UMA	X01

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(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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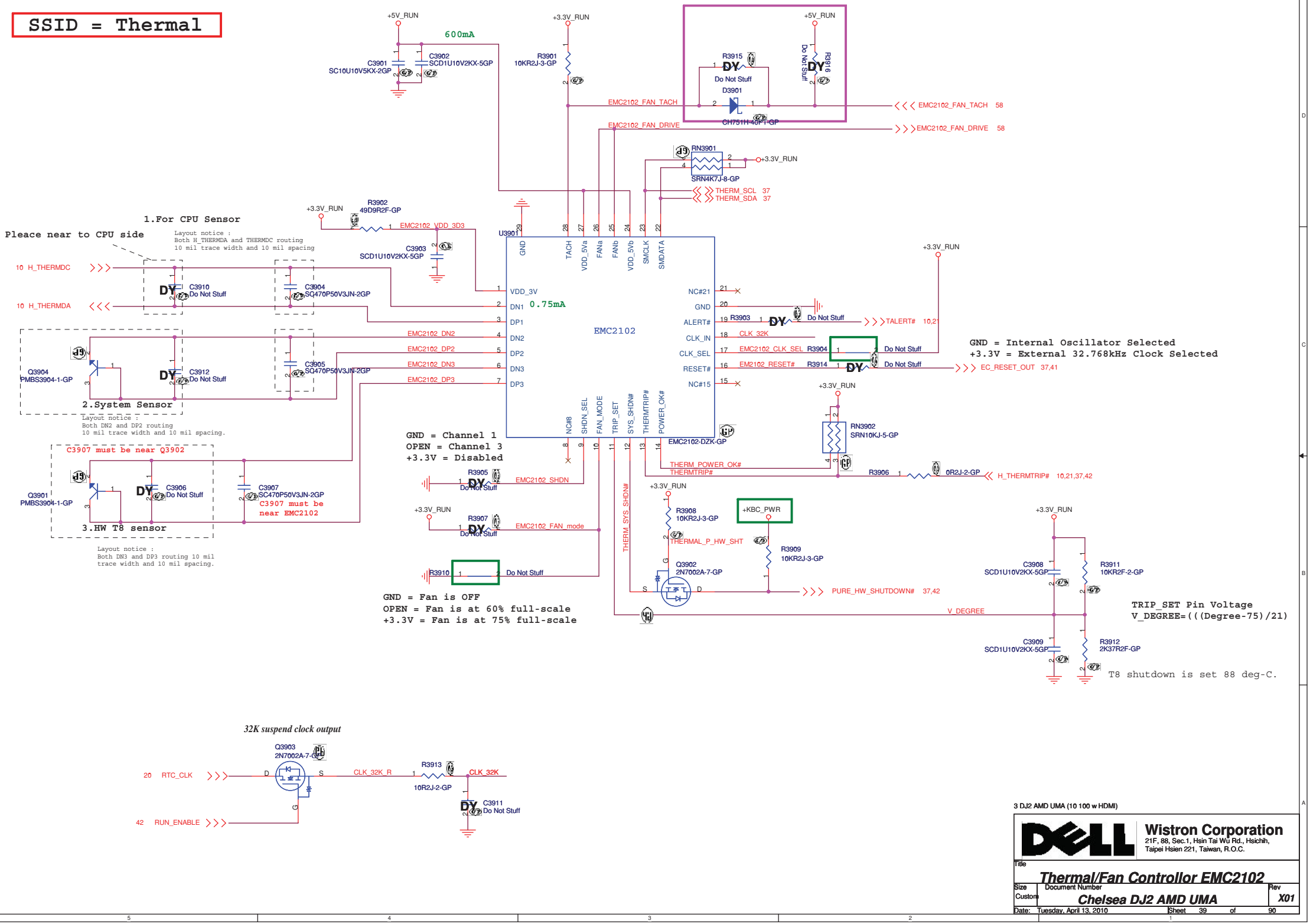
SSID = Thermal



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	X01

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(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

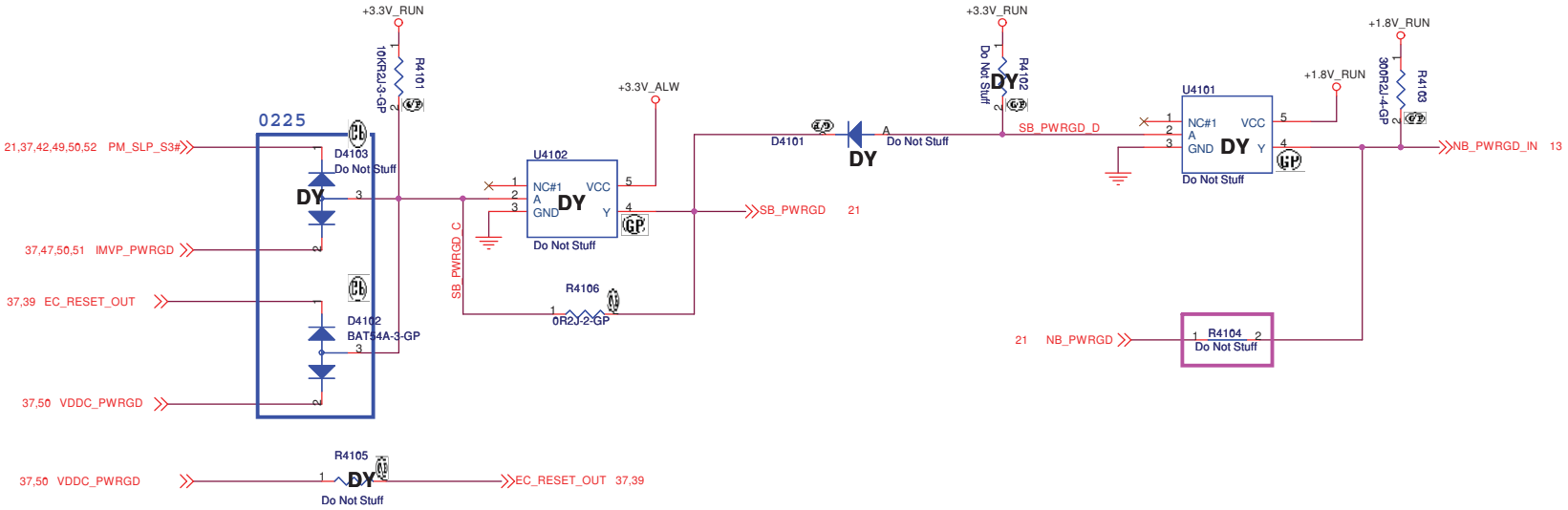
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 40 of 90

SSID = Reset.Suspend

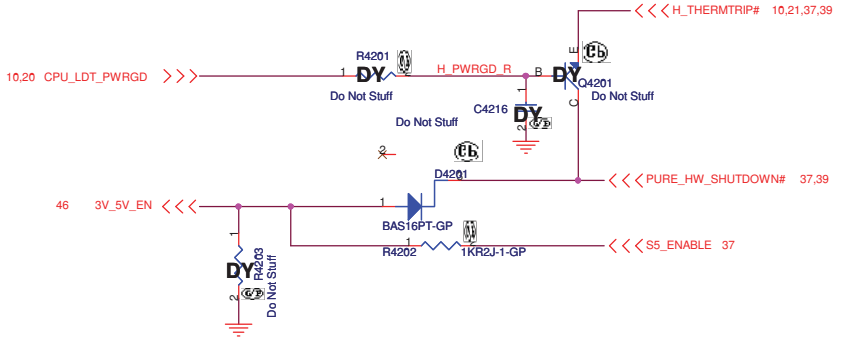


3 DJ2 AMD UMA (10 100 w HDMI)

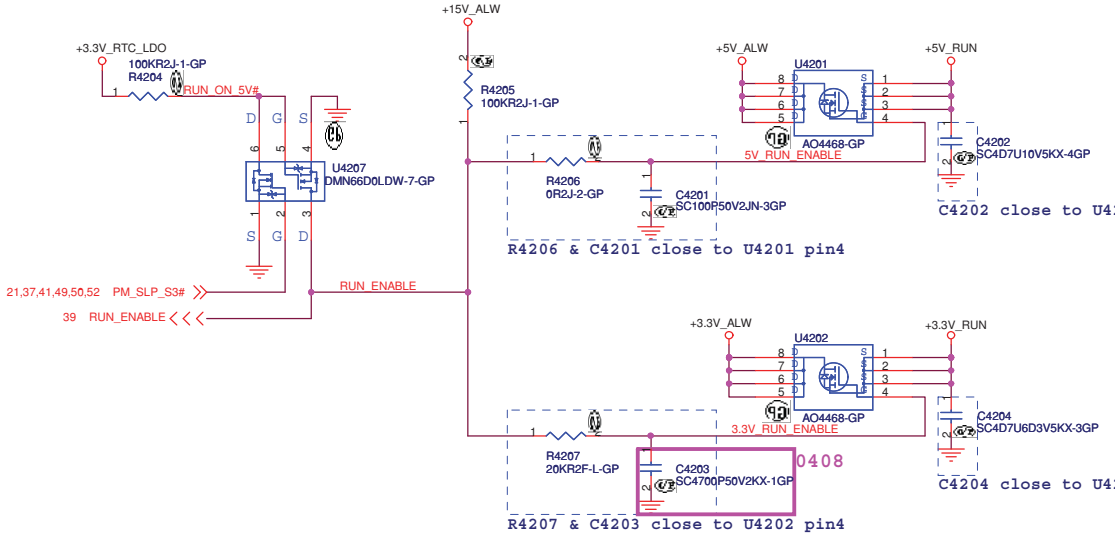
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 41 of 90	

SSID = Reset.Suspend



Run Power



Peak current: 6257.3mA (HD:1100 ODD:2500)
Design current: 4380.11 mA
11.6A
Rds=14m ohm

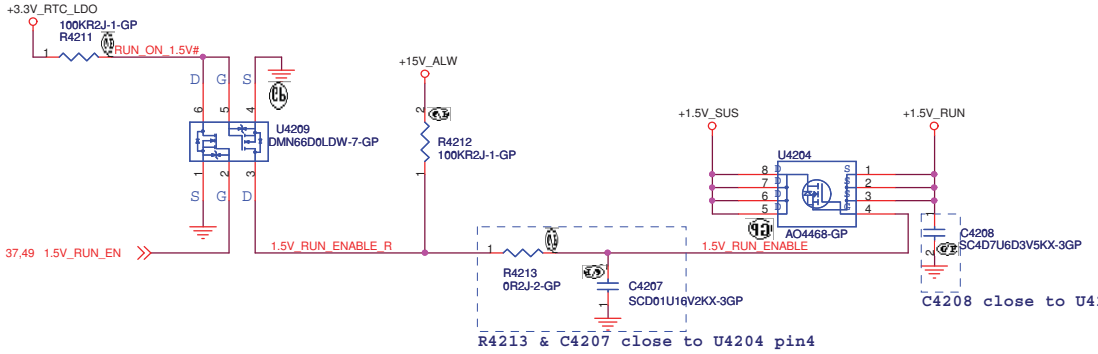
C4202 close to U4201 pin1~3

R4206 & C4201 close to U4201 pin4

Peak current: 5966mA
Design current: 4177 mA
11.6A
Rds=14m ohm

C4204 close to U4202 pin1~3

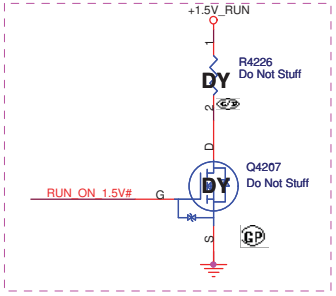
R4207 & C4203 close to U4202 pin4



Peak current: 1230mA
Design current: 861 mA
11.6A
Rds=14m ohm

C4208 close to U4204 pin1~3

R4213 & C4207 close to U4204 pin4



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

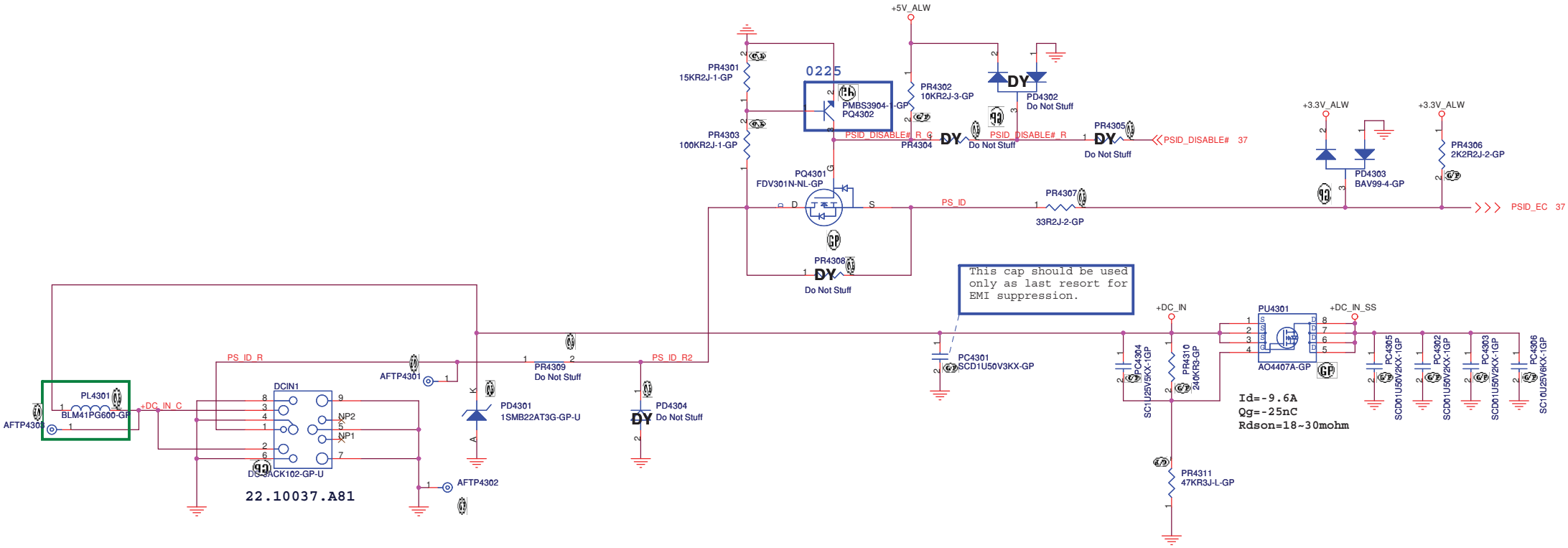
Title: Power Plane Enable

Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 42 of 90

SSID = PWR.Support

DCIN CONN



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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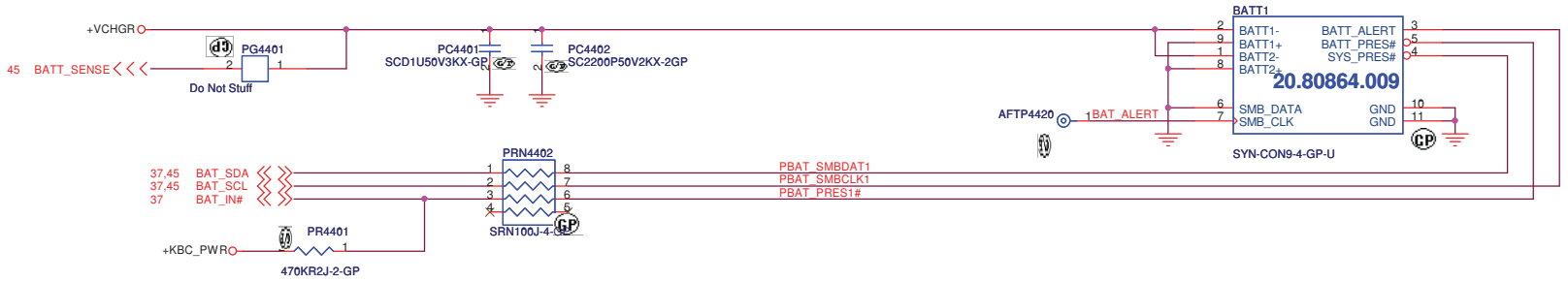
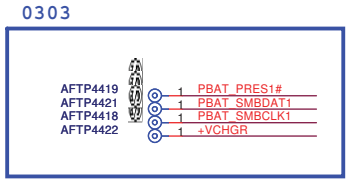
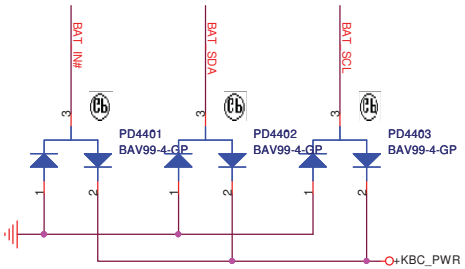
Batt Connecter







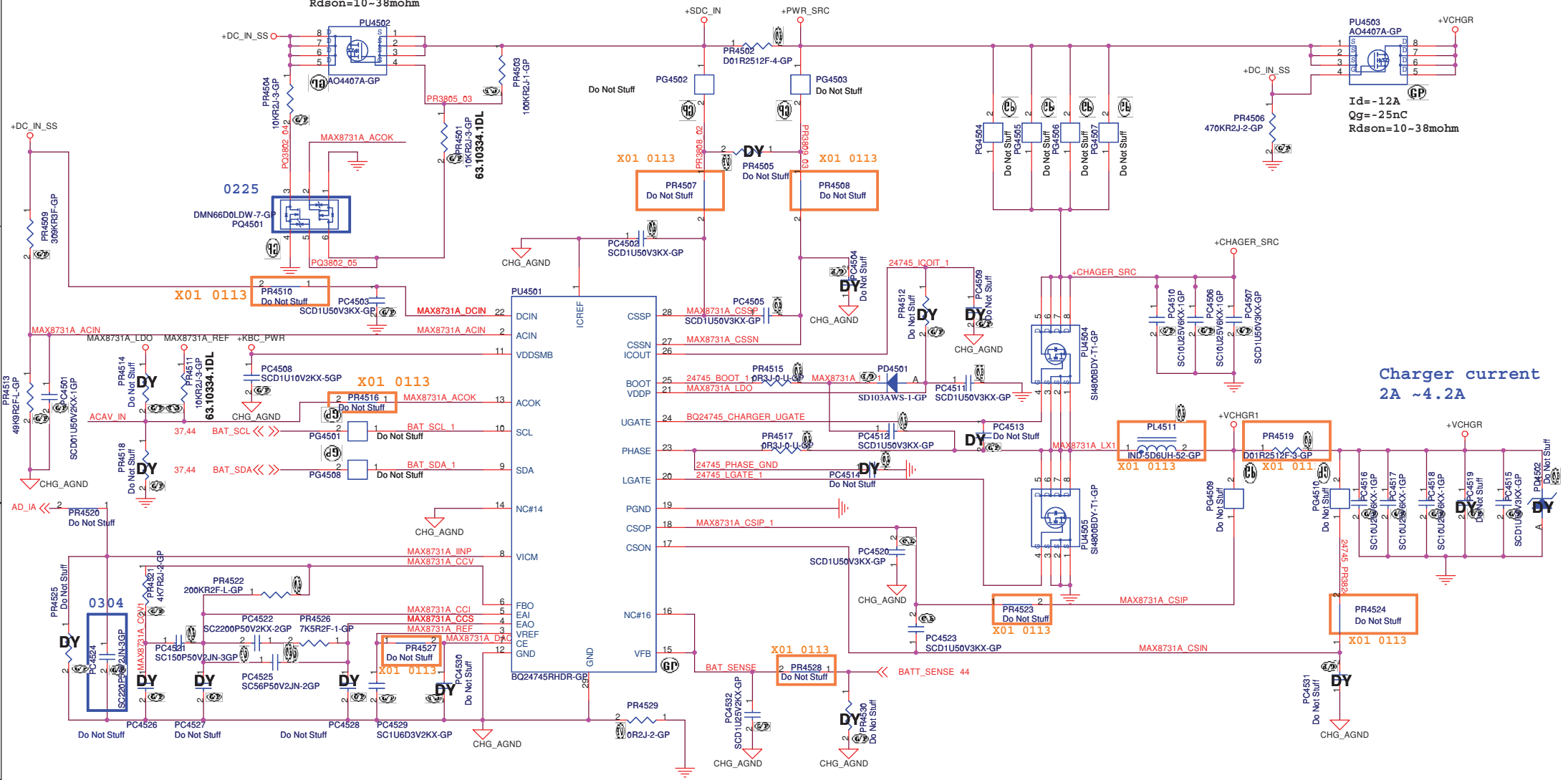
3 DJ2 AMD UMA (10 100 w HDMI)

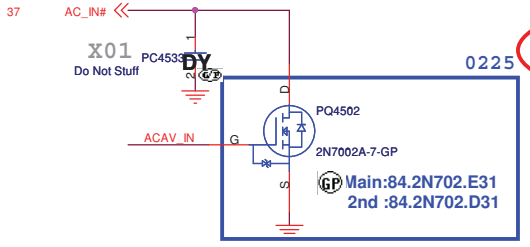
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 44 of 90	

SSID = Charger

Id=-12A
Qg=-25nC
Rdson=10~38mohm



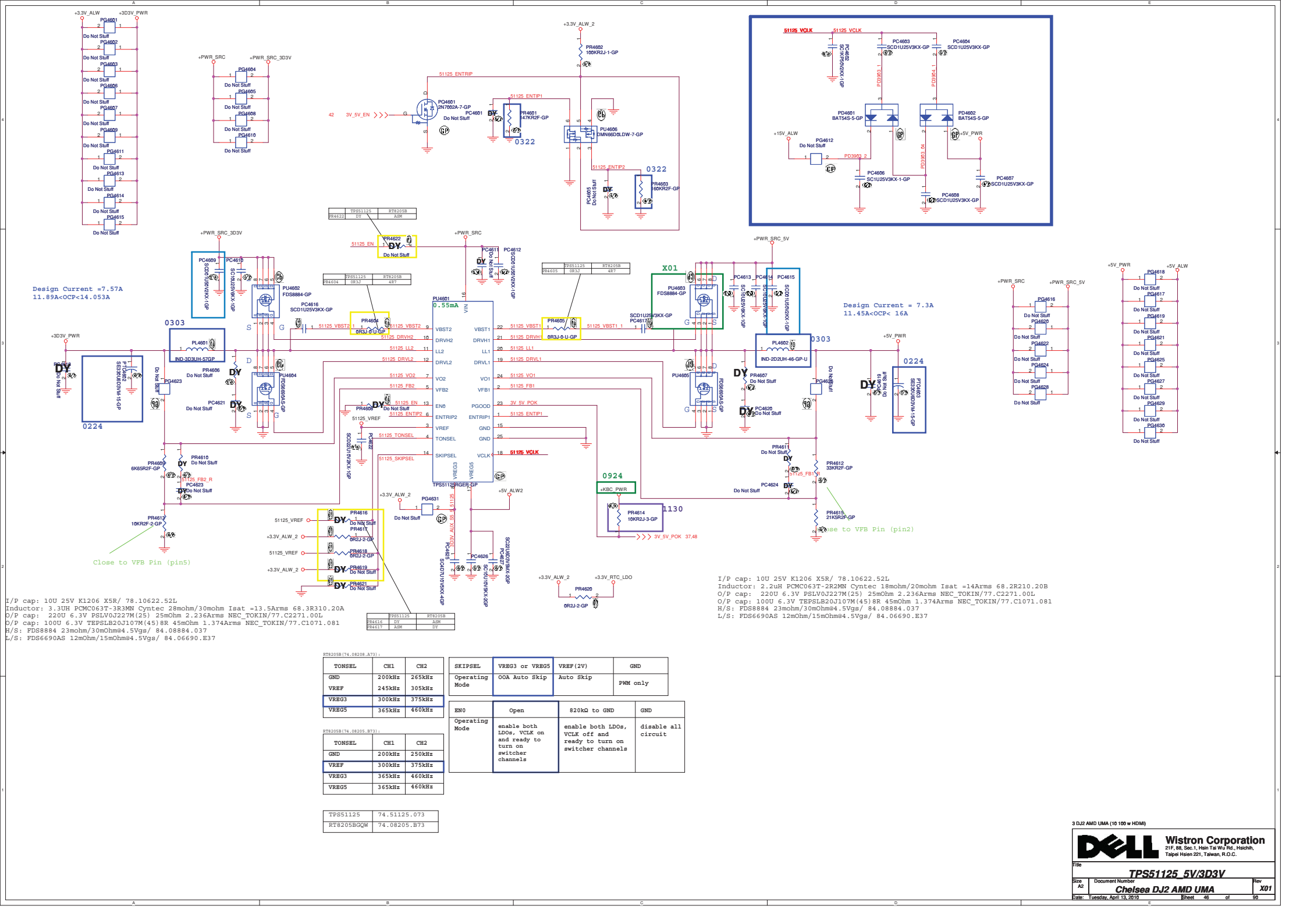


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 5.8UH SIL104R-5R8A-R DCR:24mohm Isat =7Arms Delta / 68.5R850.101
O/P cap: 10U 25V K1206 X5R/ 78.10622.52L
H/S: SI4800BDY/ 23mOhm/30mohm@4.5Vgs/ 84.04800.D37
L/S: SI4800BDY/ 23mOhm/30mohm@4.5Vgs/ 84.04800.D37

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER BQ24745	
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 45 of 90	



RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08205.B73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8205BGQW	74.08205.B73

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

Size: A2 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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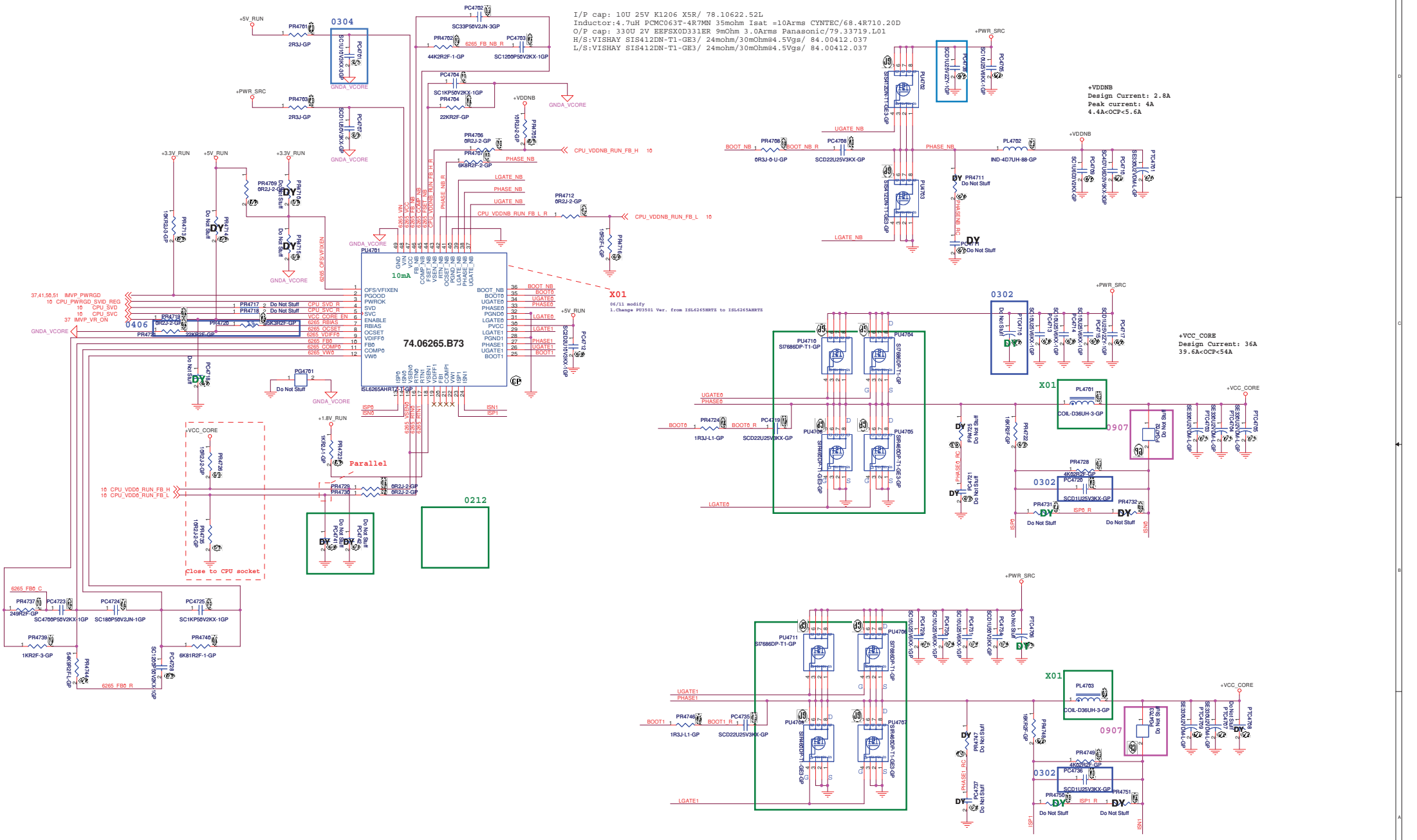
SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

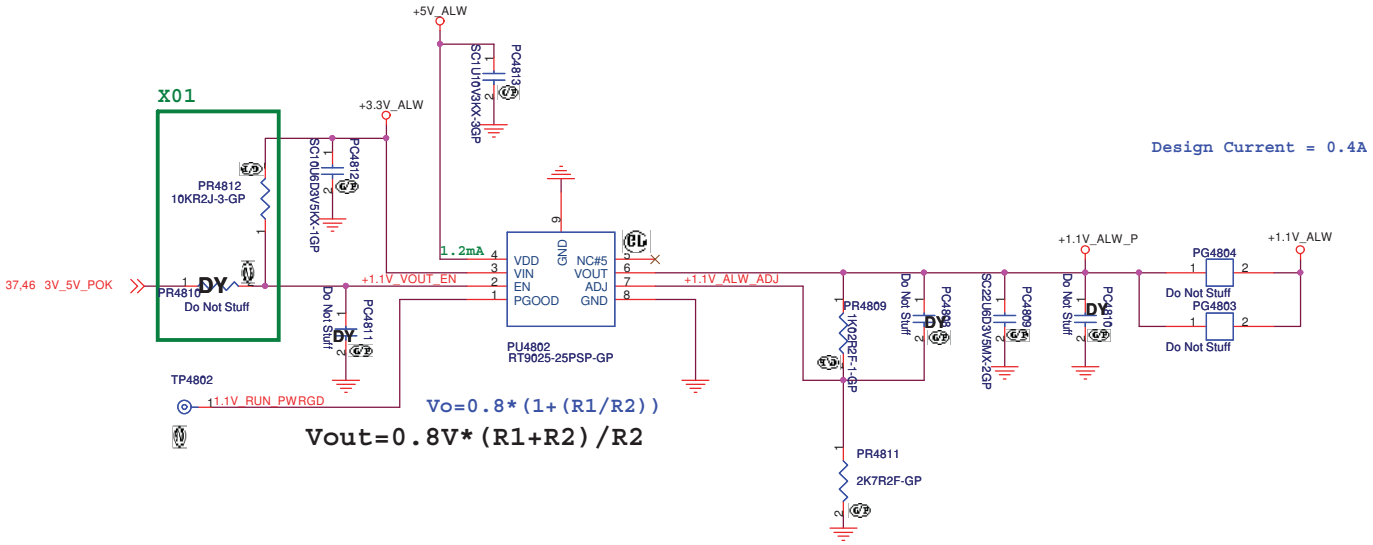
Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 47 of 90

SSID = PWR.Plane.Regulator_+1.1V_RUN

RT9025 for +1.1V_ALW



3 DJ2 AMD UMA (10 100 w HDMI)

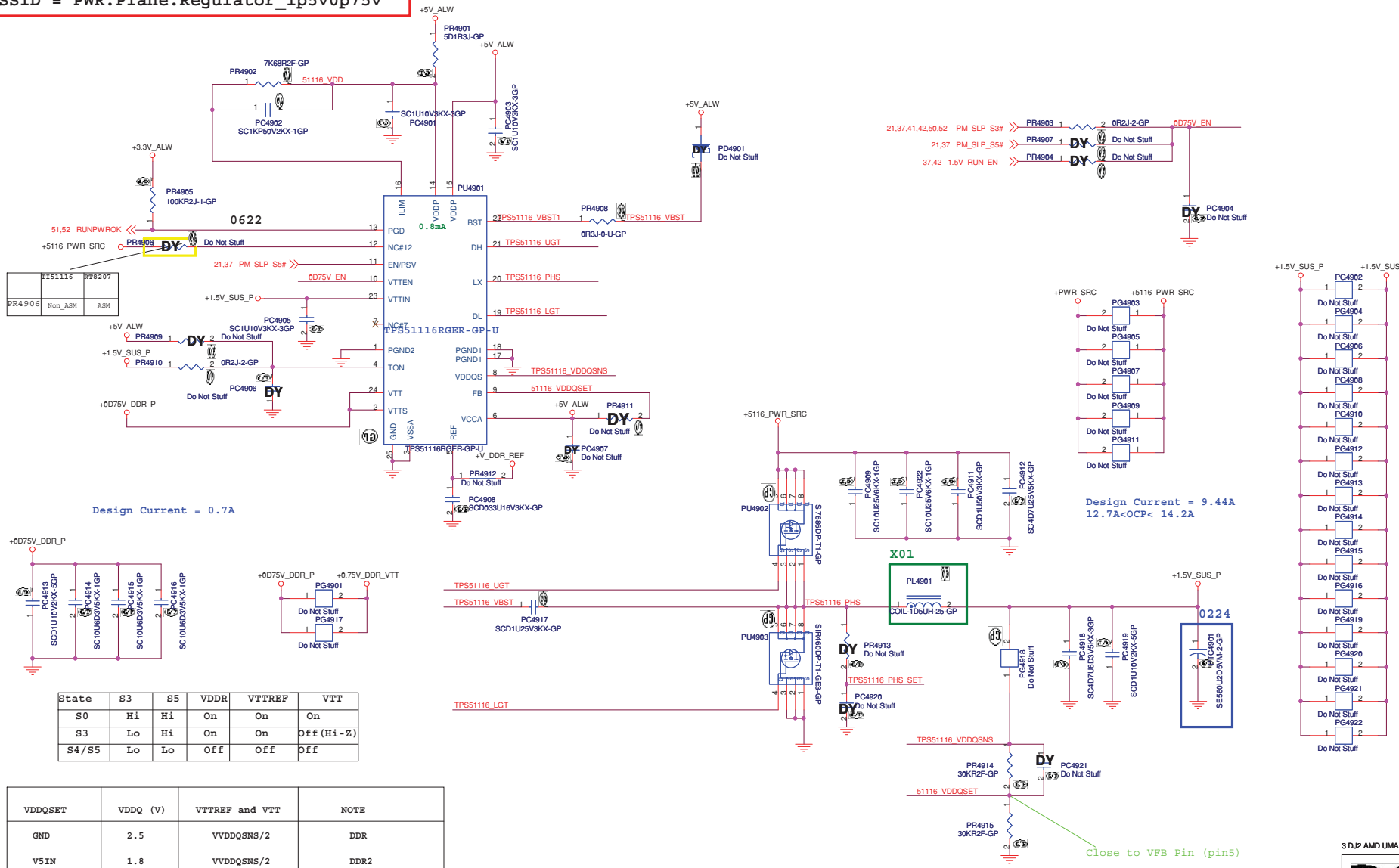
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_+1.1VALW

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 48 of 90

SSID = PWR.Plane.Regulator_1p5v0p75v



	TI51116	RT8207
PR4906	Non_ASM	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

3 DJ2 AMD UMA (10 100 w HDMI)

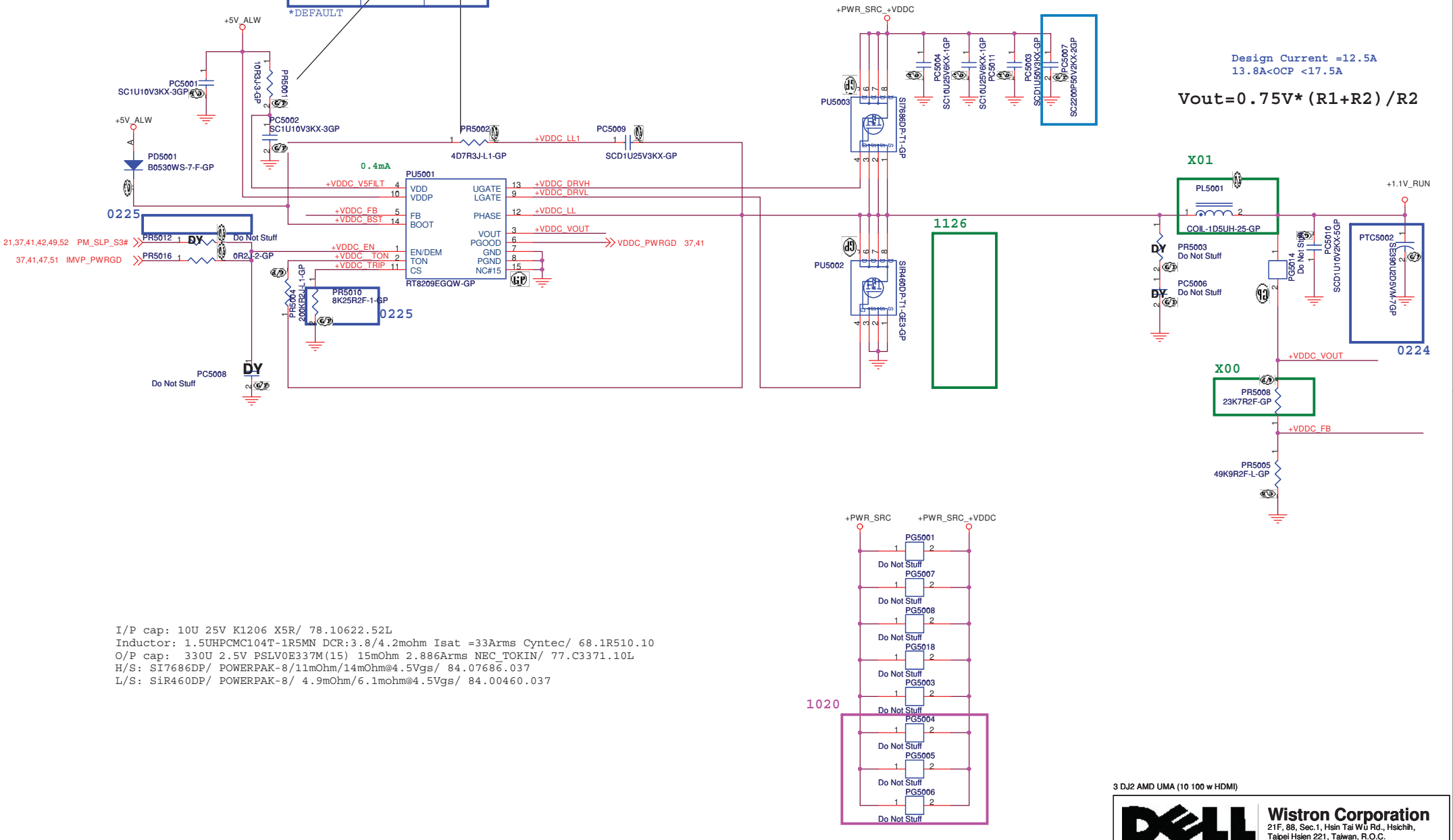
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116RGER_+1.5V_SUS
Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: X01
Date: Tuesday, April 13, 2010 | Sheet 49 of 90

SSID = PWR.Plane.Regulator_VDDC

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT



Design Current =12.5A
13.8A<OCP <17.5A

Vout=0.75V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

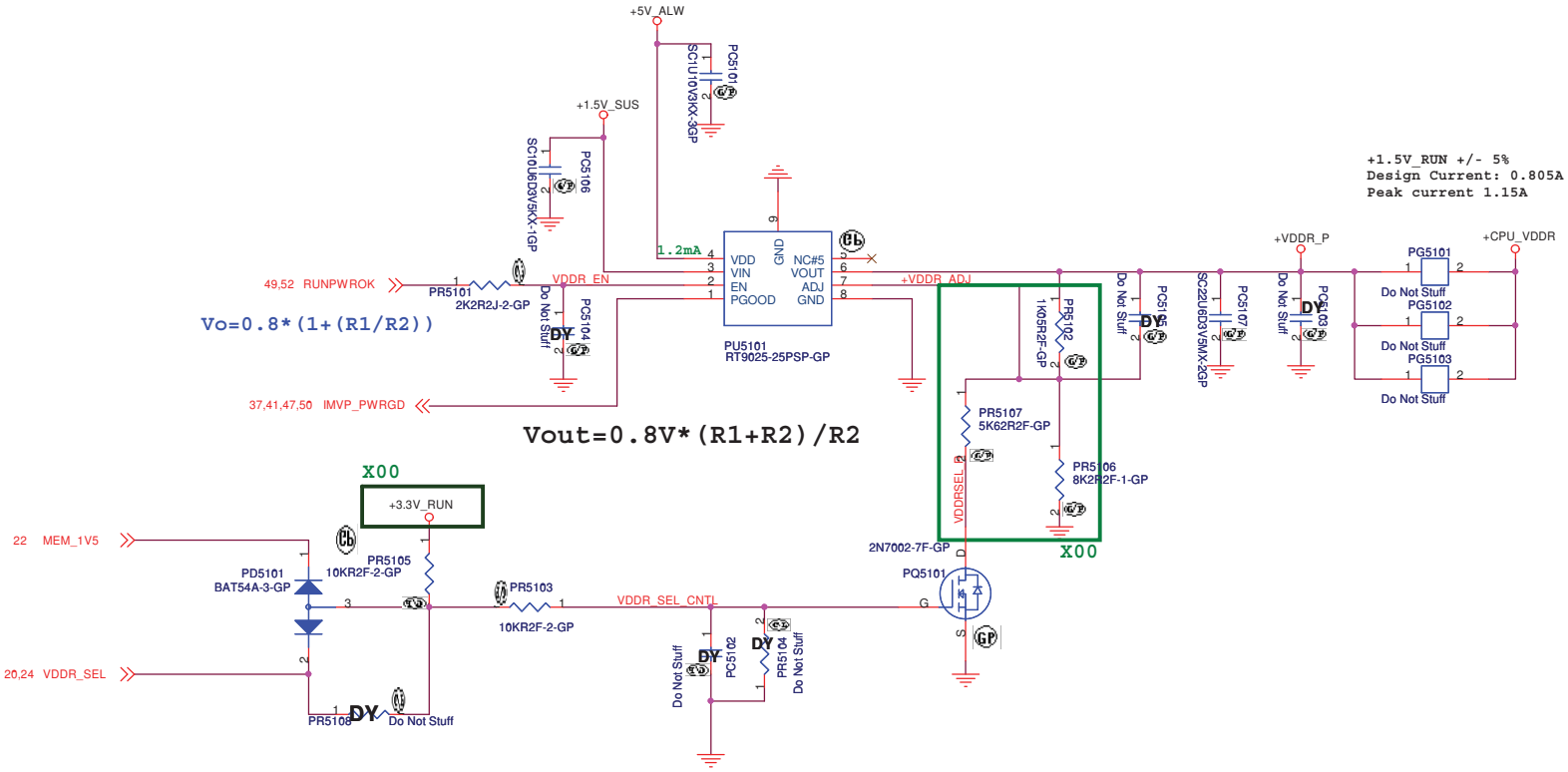
Title: RT8209 +1.1V_RUN

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 50 of 90

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

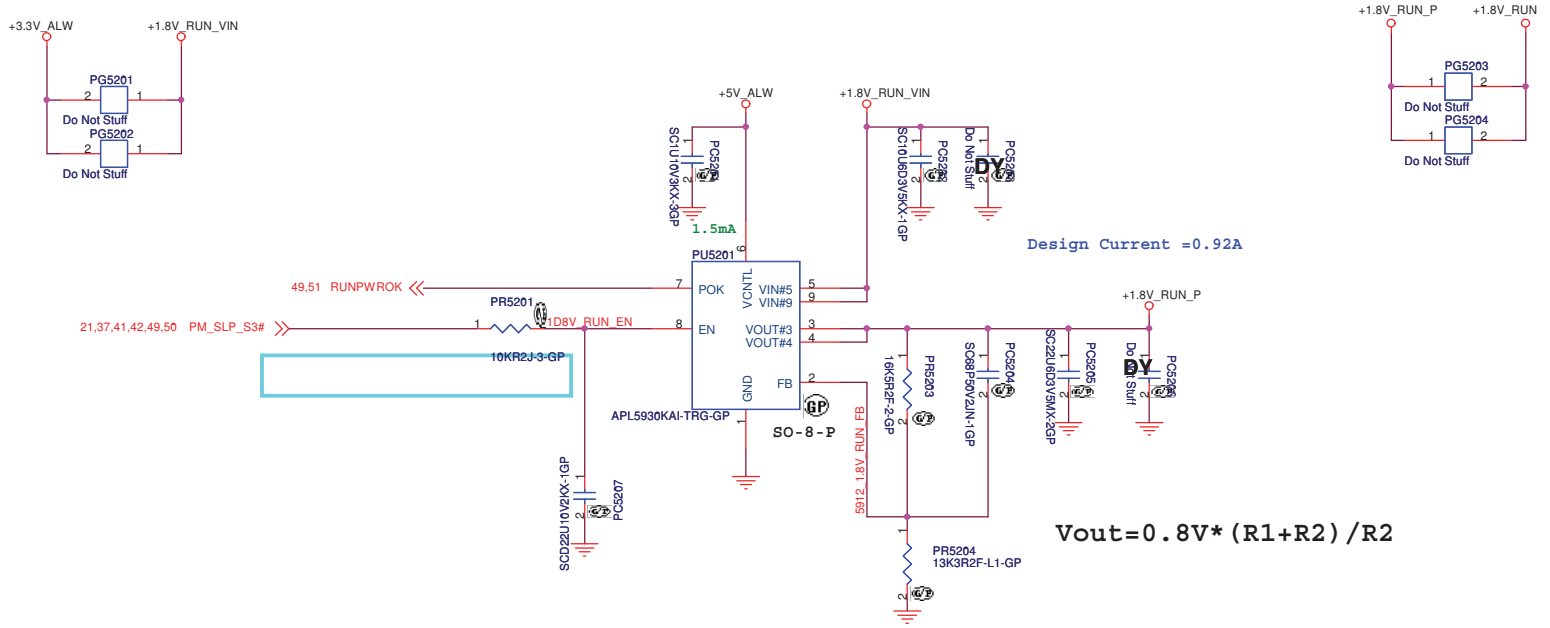
Title: RT9025 +VDDR

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 51 of 90

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



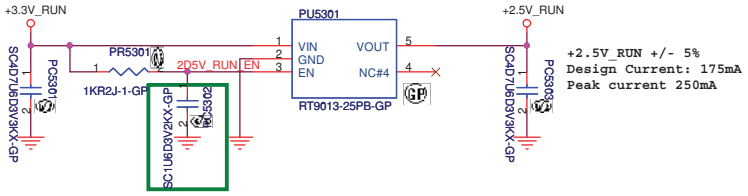
3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
APL5930 +1.8V_RUN		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 52 of 90	

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



X00

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +CPU_VDDR&+2.5V_RUN

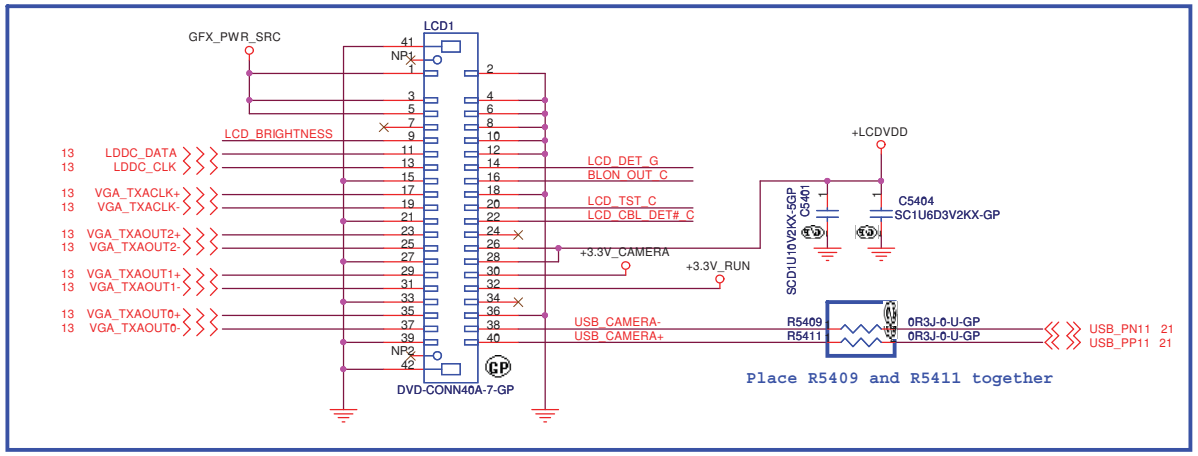
Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	X01

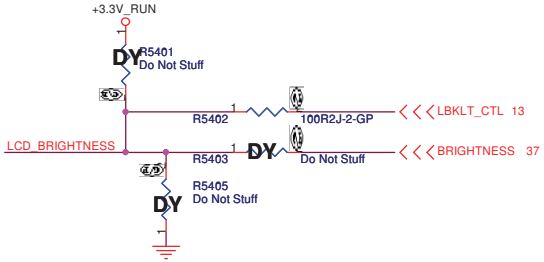
Date: Tuesday, April 13, 2010 Sheet 53 of 90

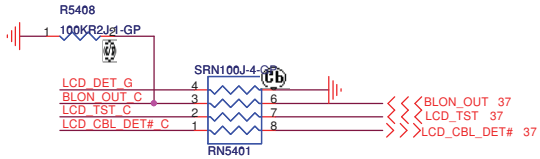
SSID = VIDEO

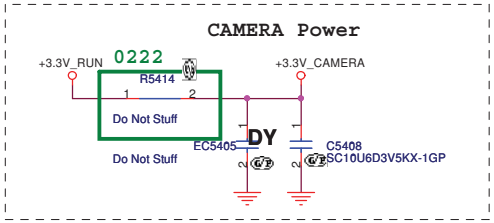
LVDS CONNECTOR

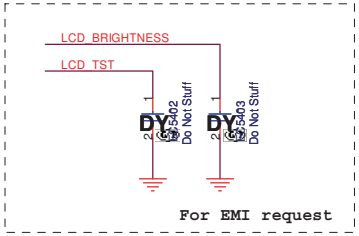
0225











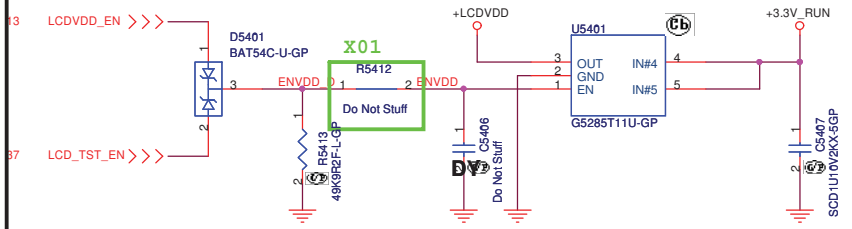
SSID = Inverter

INVERTER POWER

0224

SSID = VIDEO

LCD POWER



3 DJ2 AMD UMA (10 100 w HDMI)

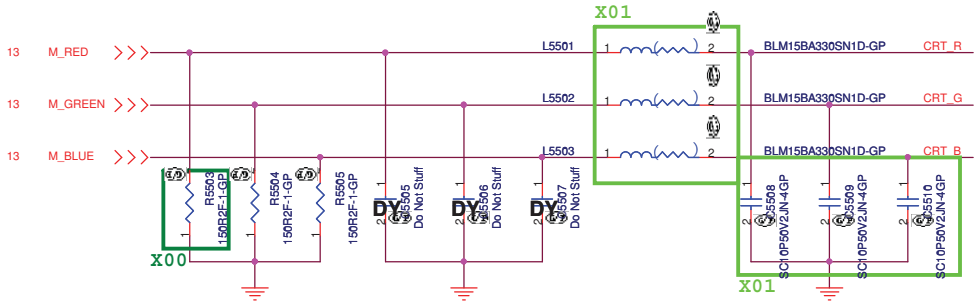
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

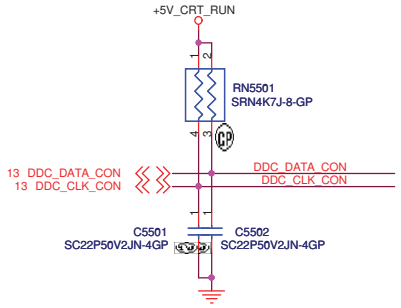
Title		
LCD/Inverter Connector		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 54 of 90	

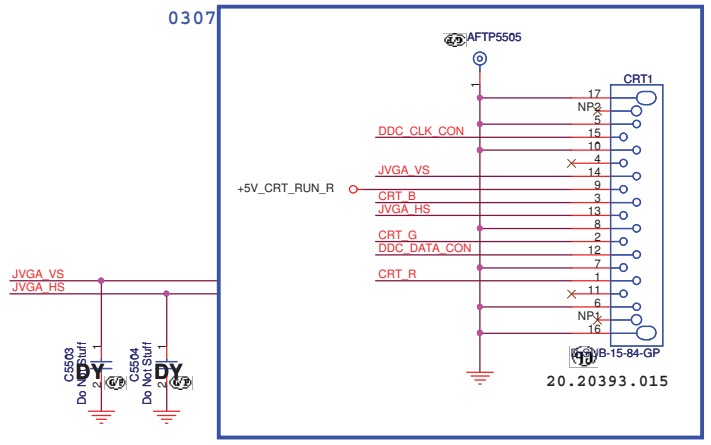
SSID = VIDEO

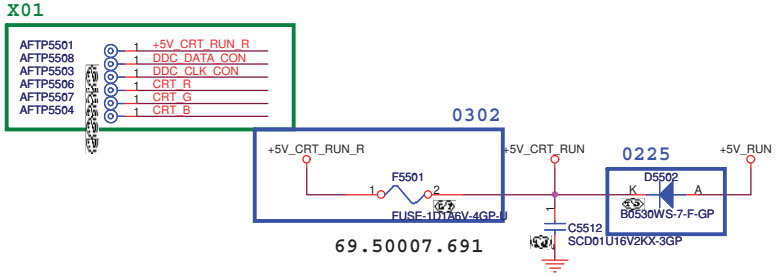
Layout Note:

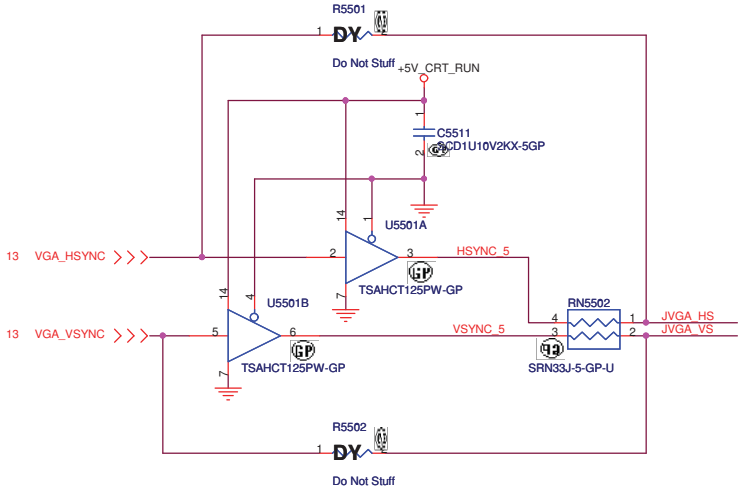
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

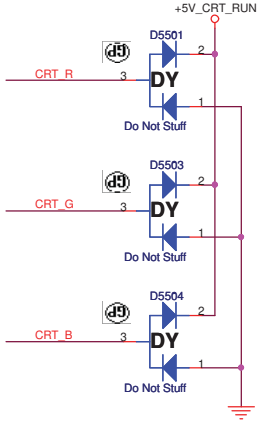


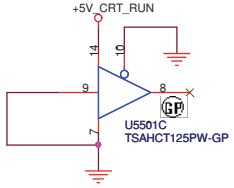


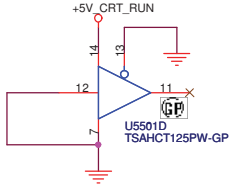












3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 55 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*X01*

Date: Tuesday, April 13, 2010 Sheet 56 of 90

SSID = VIDEO

HDMI CONNECTOR

0307

HDMI_CN_DATA2 — R5725 0R3J-0-U-GP — HDMI_CN_DATA2_R

HDMI_CN_DATA2# — R5726 0R3J-0-U-GP — HDMI_CN_DATA2#_R

put R5725 and R5726 together

0307

HDMI_CN_DATA1 — R5727 0R3J-0-U-GP — HDMI_CN_DATA1_R

HDMI_CN_DATA1# — R5728 0R3J-0-U-GP — HDMI_CN_DATA1#_R

put R5727 and R5728 together

0307

HDMI_CN_DATA0 — R5729 0R3J-0-U-GP — HDMI_CN_DATA0_R

HDMI_CN_DATA0# — R5730 0R3J-0-U-GP — HDMI_CN_DATA0#_R

put R5729 and R5730 together

0307

HDMI_CN_CLK — R5731 0R3J-0-U-GP — HDMI_CN_CLK_R

HDMI_CN_CLK# — R5732 0R3J-0-U-GP — HDMI_CN_CLK#_R

put R5731 and R5732 together

HDMI CONN

HDMI1

HDMI_CN_DATA2_R
HDMI_CN_DATA2#_R
HDMI_CN_DATA1_R
HDMI_CN_DATA1#_R
HDMI_CN_DATA0_R
HDMI_CN_DATA0#_R
HDMI_CN_CLK_R
HDMI_CN_CLK#_R
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

SKT-HDMI19P-63-GP-U

22.10296.171

0302

+5V_CRT_RUN_R

SCDT10V2KX-5GP

0302

+5V_CRT_RUN

RN5701 SRN4K7J-8-GP

5V Tolerance

13 DDC_CLK_HDMI
13 DDC_DATA_HDMI

DDC_CLK_HDMI
DDC_DATA_HDMI

12 HDMI_CN_CLK#
12 HDMI_CN_CLK
12 HDMI_CN_DATA0#
12 HDMI_CN_DATA0
12 HDMI_CN_DATA1#
12 HDMI_CN_DATA1
12 HDMI_CN_DATA2#
12 HDMI_CN_DATA2

HDMI_CN_CLK#
HDMI_CN_CLK
HDMI_CN_DATA0#
HDMI_CN_DATA0
HDMI_CN_DATA1#
HDMI_CN_DATA1
HDMI_CN_DATA2#
HDMI_CN_DATA2

0307

R5715 R5716 R5717 R5718 R5719 R5720 R5721 R5722 — 75R2F-GP

+3.3V_RUN

Q5702 PMBS3904-1-GP

HPD_HDMI_1

R5710 150KR2J-L1-GP

HPD_HDMI_CON

13 HDMI_HPD_DET

R5713 0KR2J-3-GP

R5712 DY Do Not Stuff

+5V_RUN

HDMI_PLL_GND

R5724 0R2J-2-GP

HDMI_PLL_GATE

Q5703 2N7002A-7-GP

R5714 100KR2J-1-GP

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

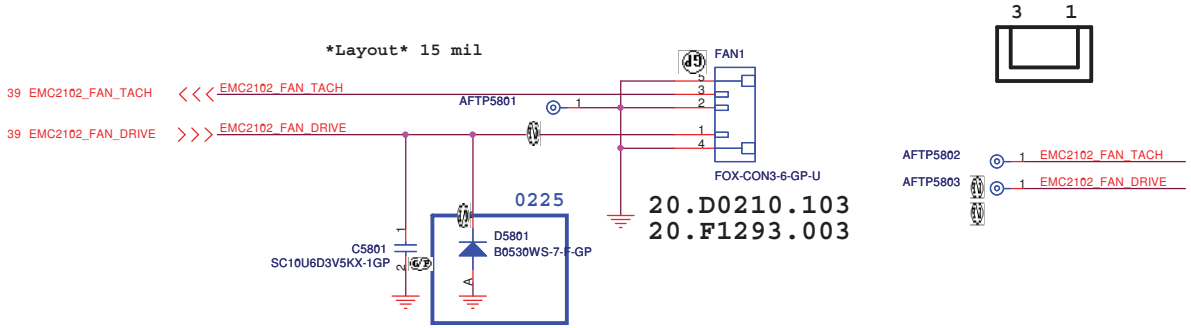
Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 57 of 90

SSID = Thermal

Fan Connector



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

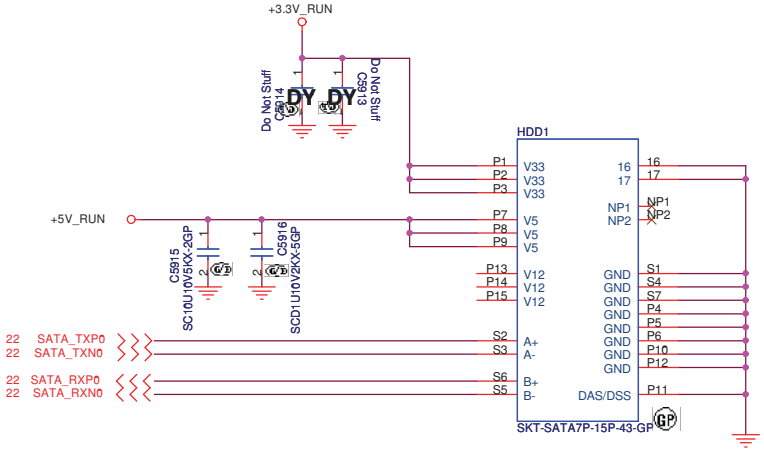
Title: ITP/Fan Connector

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Tuesday, April 13, 2010 | Sheet 58 of 90

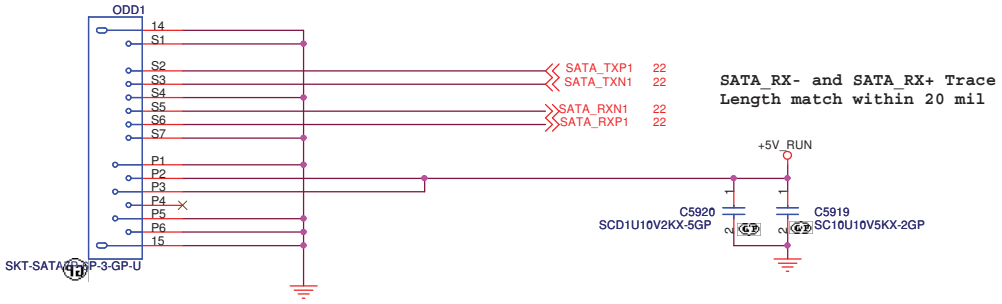
SSID = SATA

SATA HDD Connector



22.10300.A81

ODD Connector



22.10300.801

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

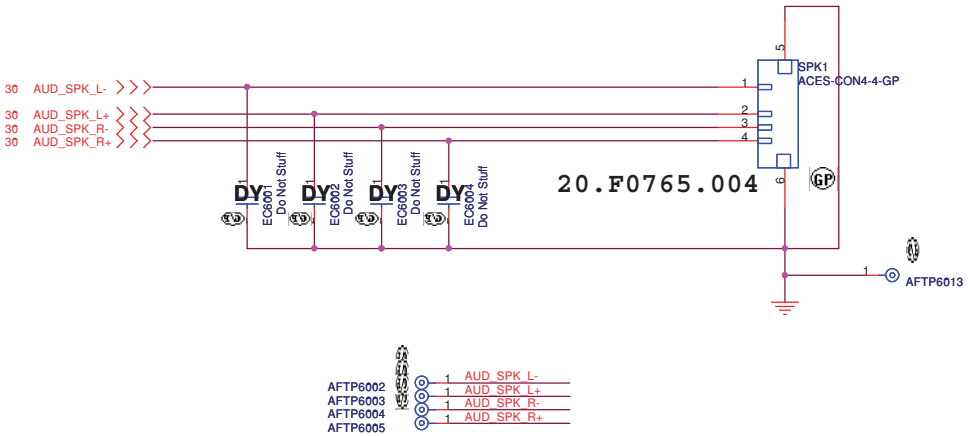
Title: HDD/ODD

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

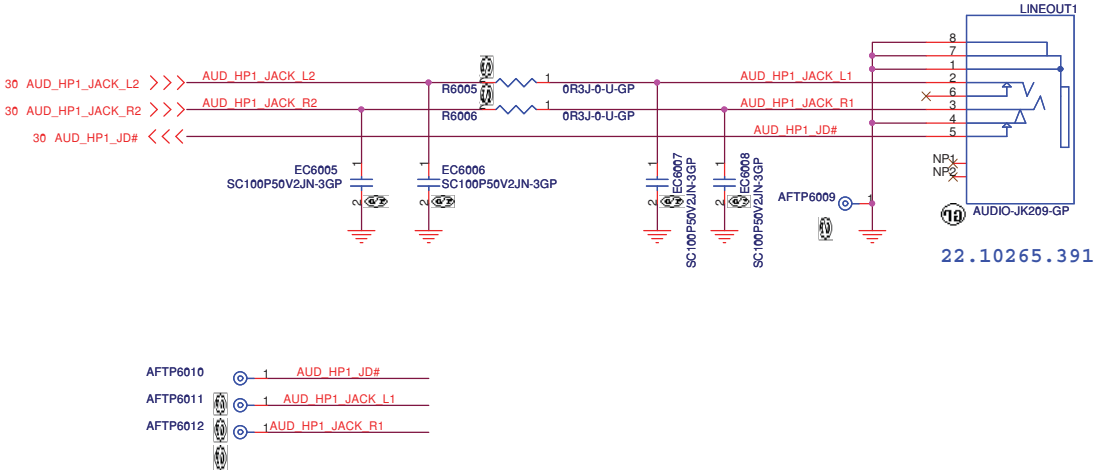
Date: Tuesday, April 13, 2010 Sheet 59 of 90

SSID = AUDIO

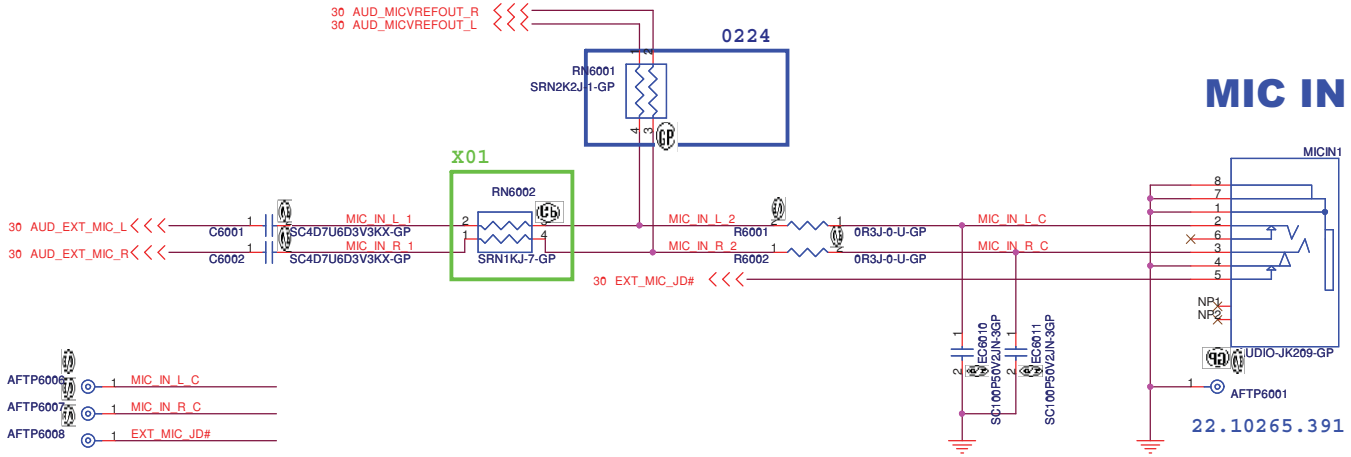
Speaker Connector



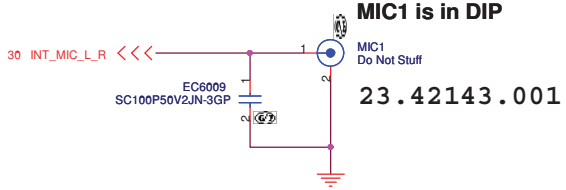
LINE1 OUT



MIC IN



Internal Microphone



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

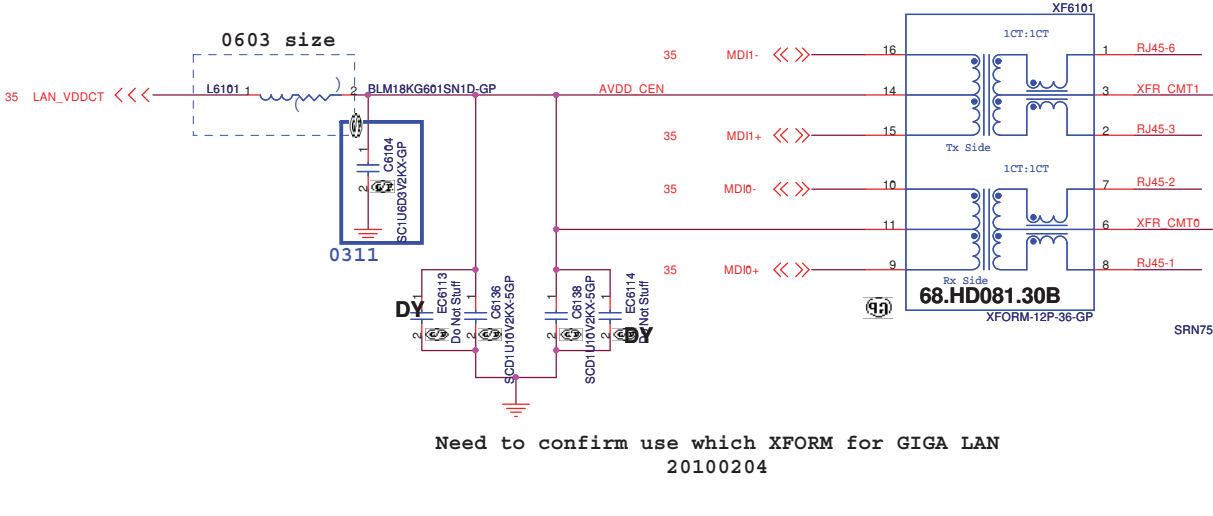
Title: Audio Jack		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 60 of 90	

```
2009-10-1 Change MDI1+(XF601.16) to MDI1+(XF601.15)
          Change MDI1-(XF601.15) to MDI1-(XF601.16)
          Change MDI0+(XF601.10) to MDI0+(XF601.9)
          Change MDI0-(XF601.9) to MDI0-(XF601.10)
          Change RJ45-3(XF601.1) to RJ45-3(XF601.2)
          Change RJ45-6(XF601.2) to RJ45-6(XF601.1)
          Change RJ45-1(XF601.7) to RJ45-1(XF601.8)
          Change RJ45-2(XF601.8) to RJ45-2(XF601.7)
```

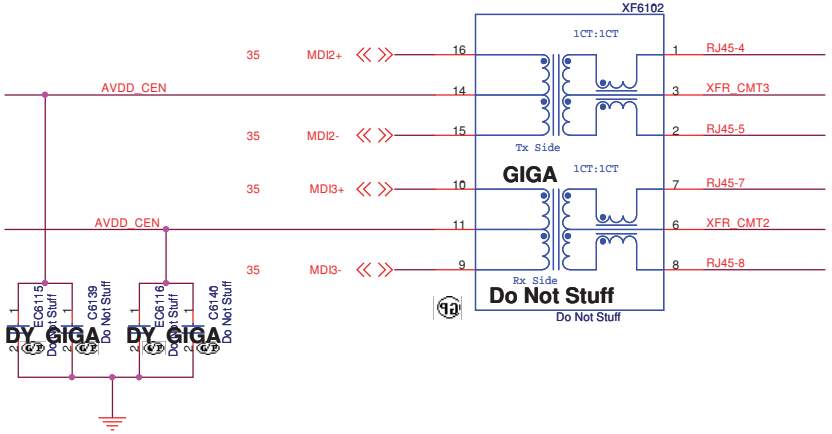
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

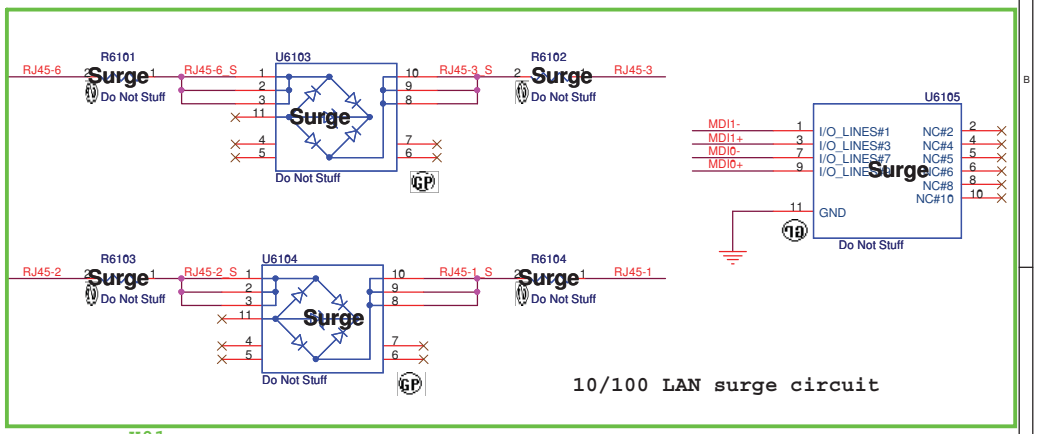
RJ45 Connector

10/100M Lan Transformer



Need to confirm use which XFORM for GIGA LAN
20100204





X01

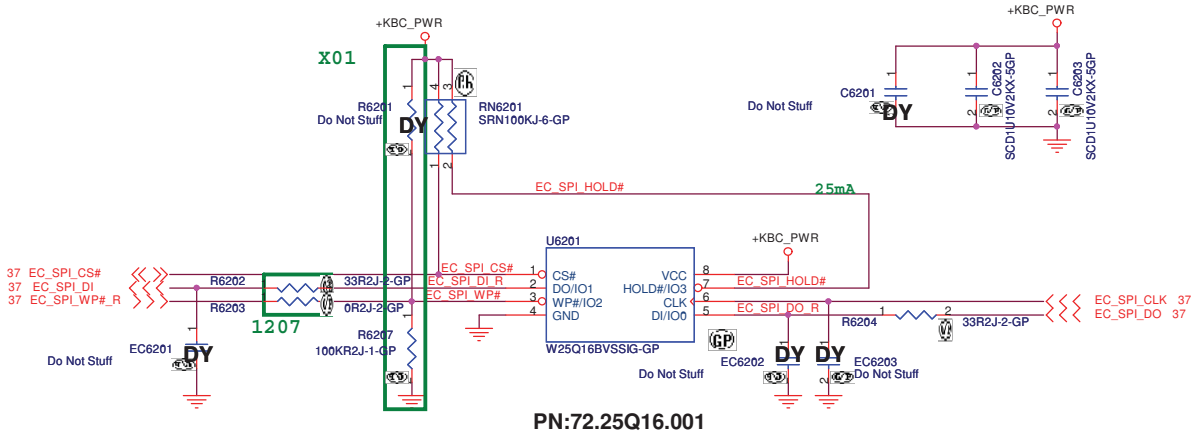
3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFORM/RJ45		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 61 of 90	

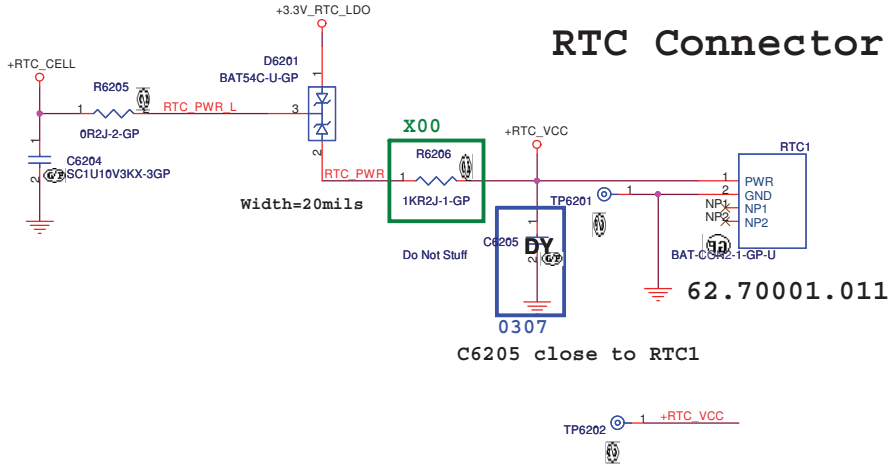
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



PN:72.25Q16.001

SSID = RBATT



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

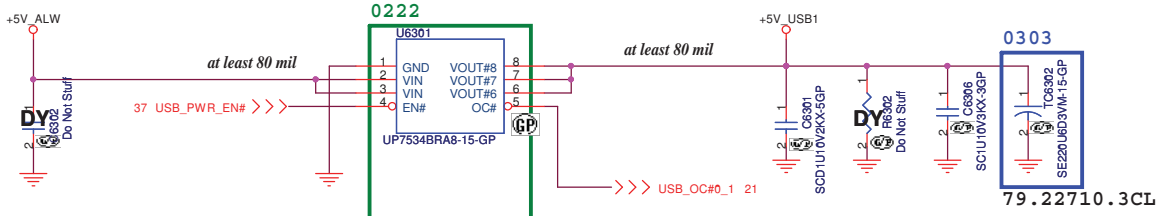
Title: Flash/RTC

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 62 of 90

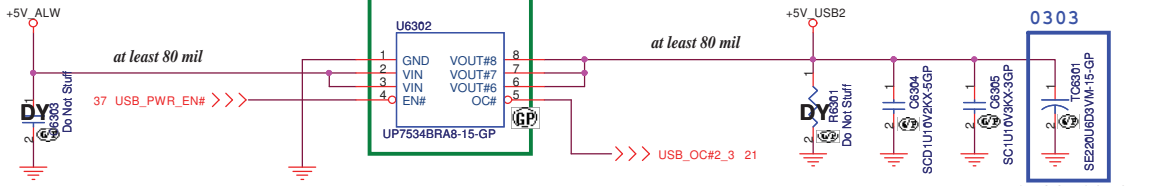
SSID = USB

USB Power

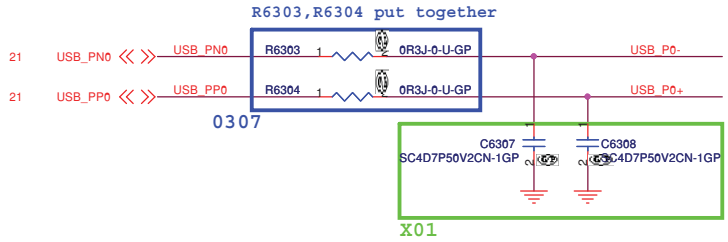


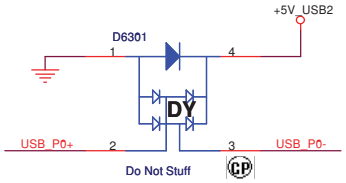
79.22710.3CL

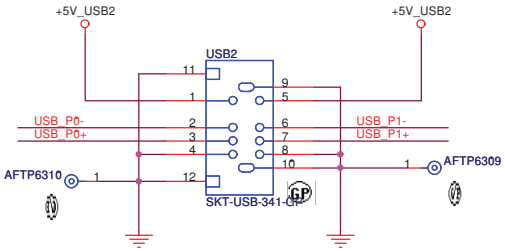
Right USB Power



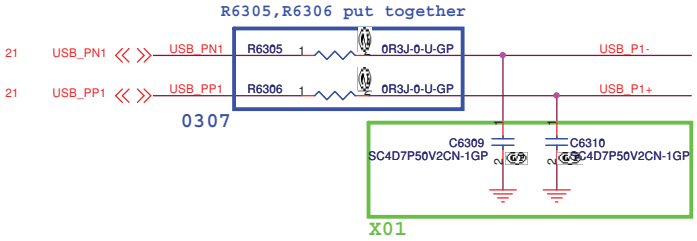
79.22710.3CL

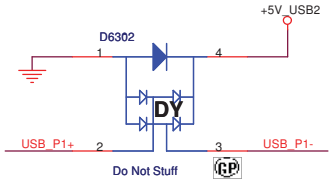


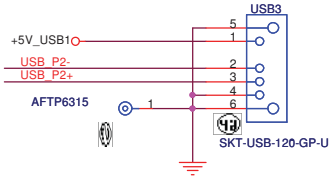




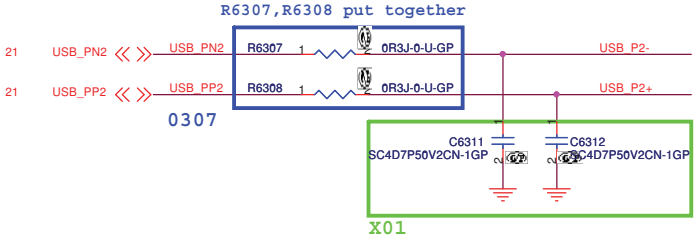
22.10254.501

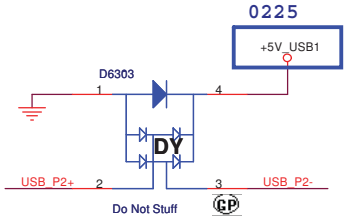


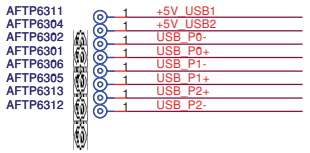




22.10218.K71







3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

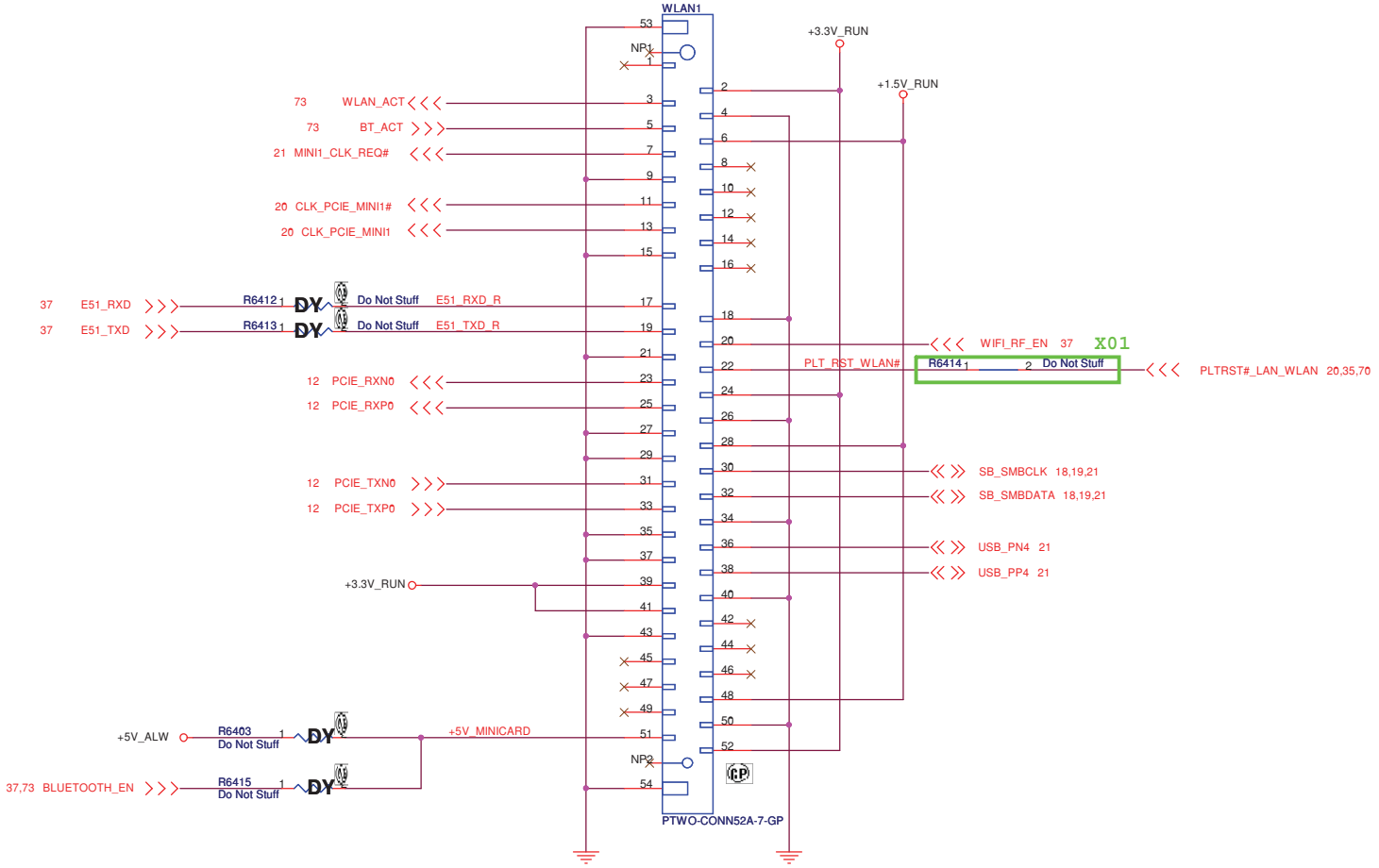
Title: USB

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

Date: Wednesday, April 14, 2010 | Sheet 63 of 90

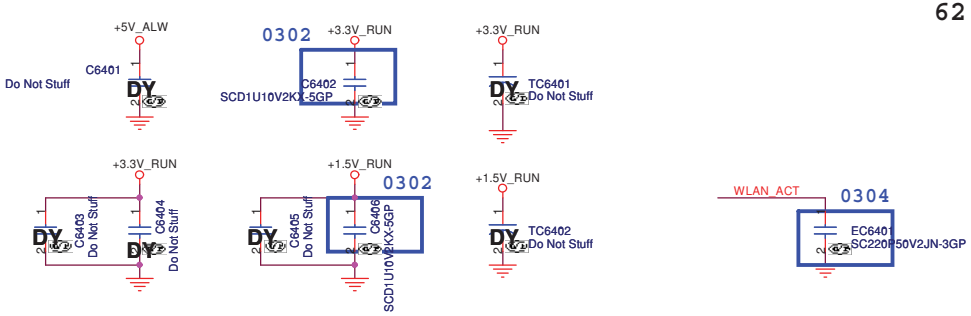
SSID = Wireless

Mini Card Connector(802.11a/b/g)



20.F1516.052

62.10043.771



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MINICARD		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

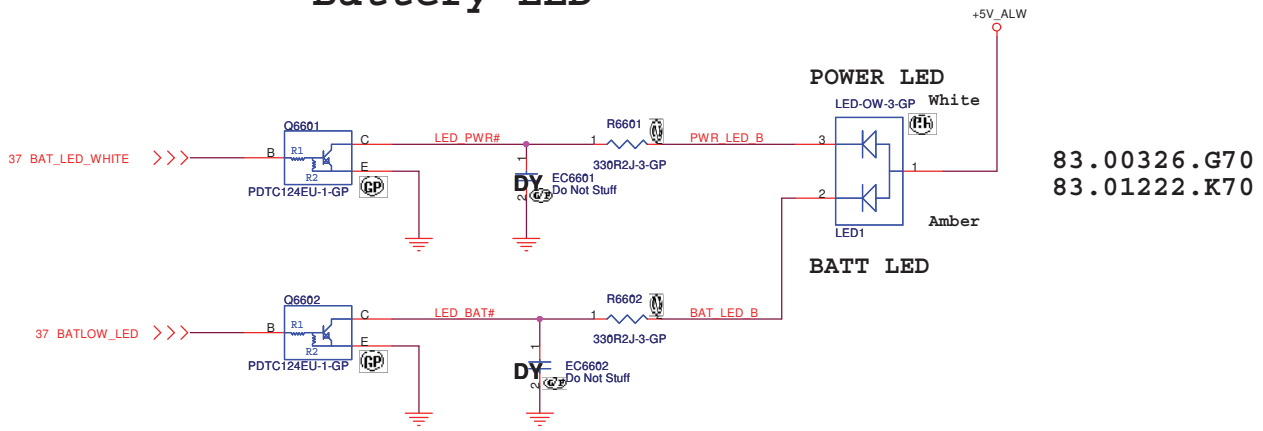
Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 65 of 90

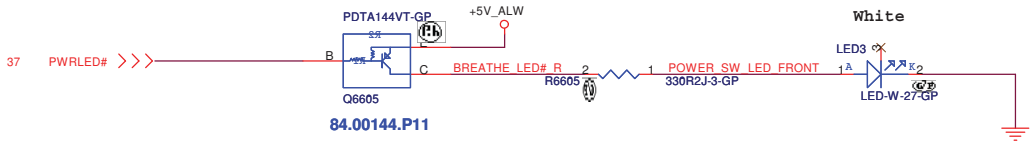
SSID = User.Interface

Battery LED



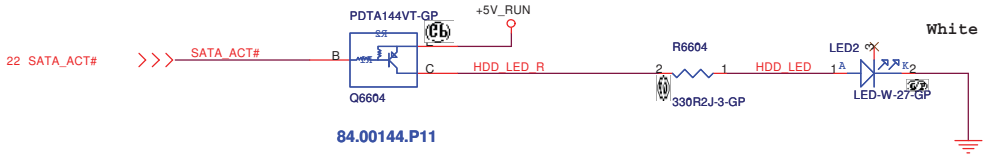
83.00326.G70
83.01222.K70

BREATHE PWR LED (Front)



84.00144.P11

HDD LED



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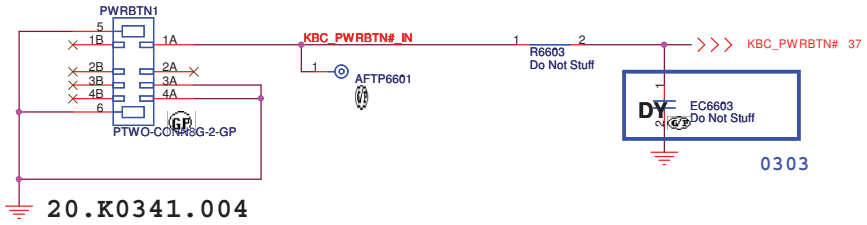

20.K0341.004

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED/PWRBTN	
Size A3	Document Number: Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 66 of 90	

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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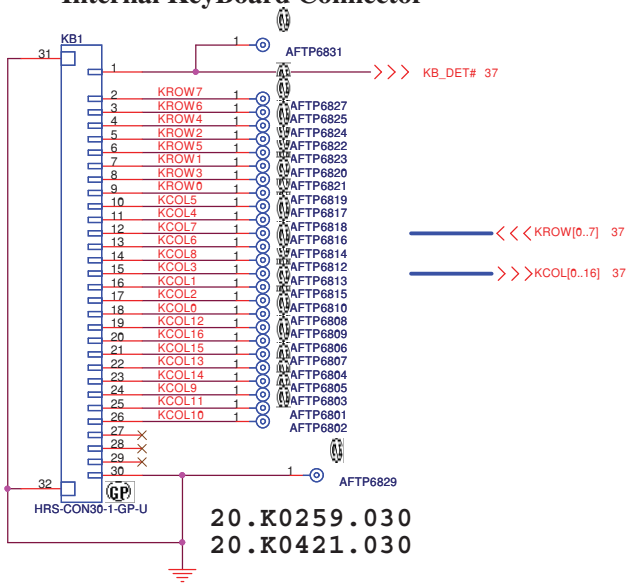
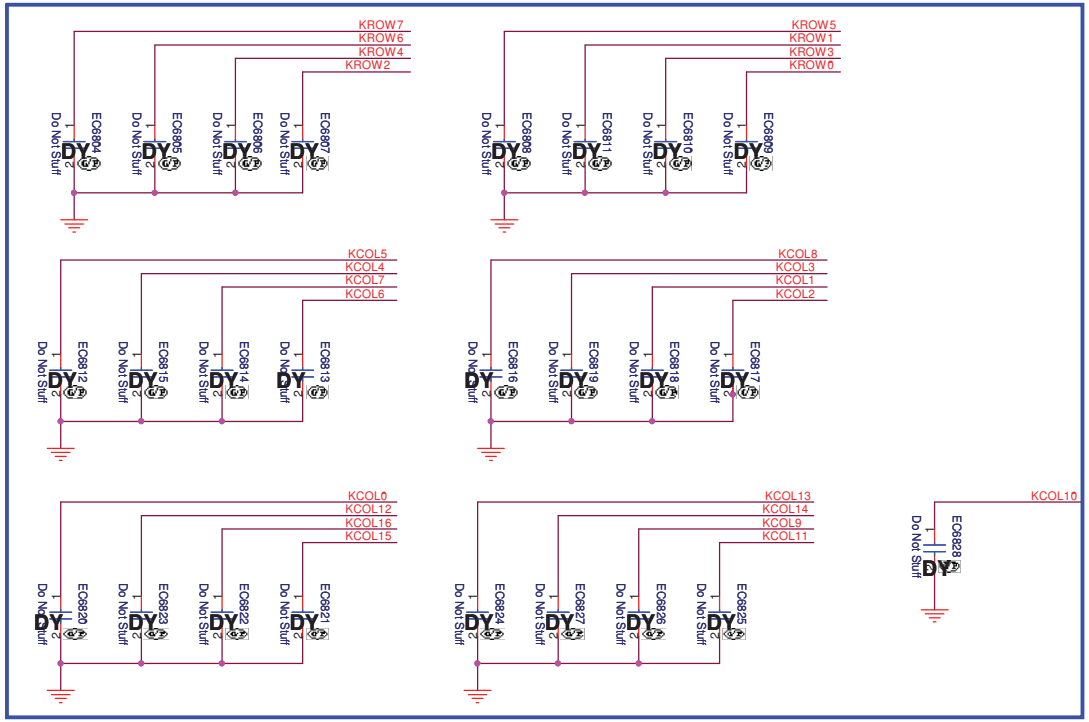
SSID = KBC

Internal KeyBoard Connector



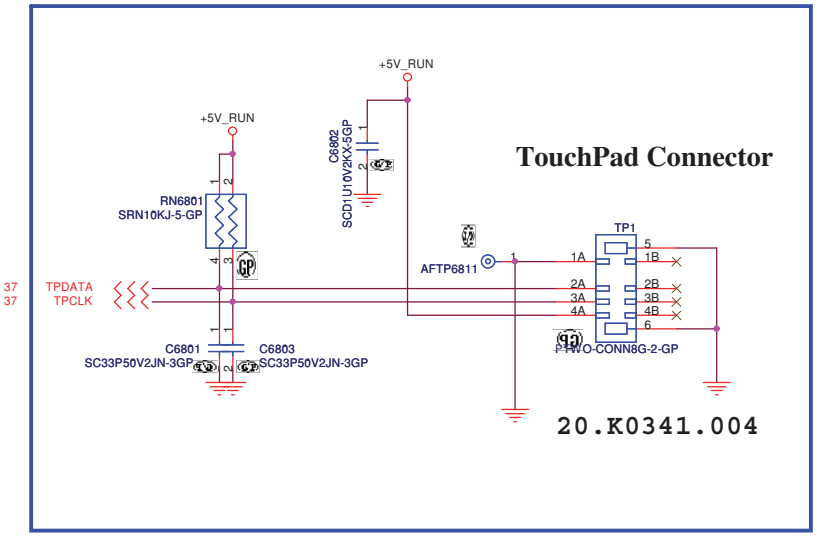
20.K0259.030
20.K0421.030

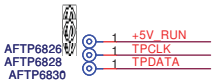
0304



SSID = Touch.Pad

0302



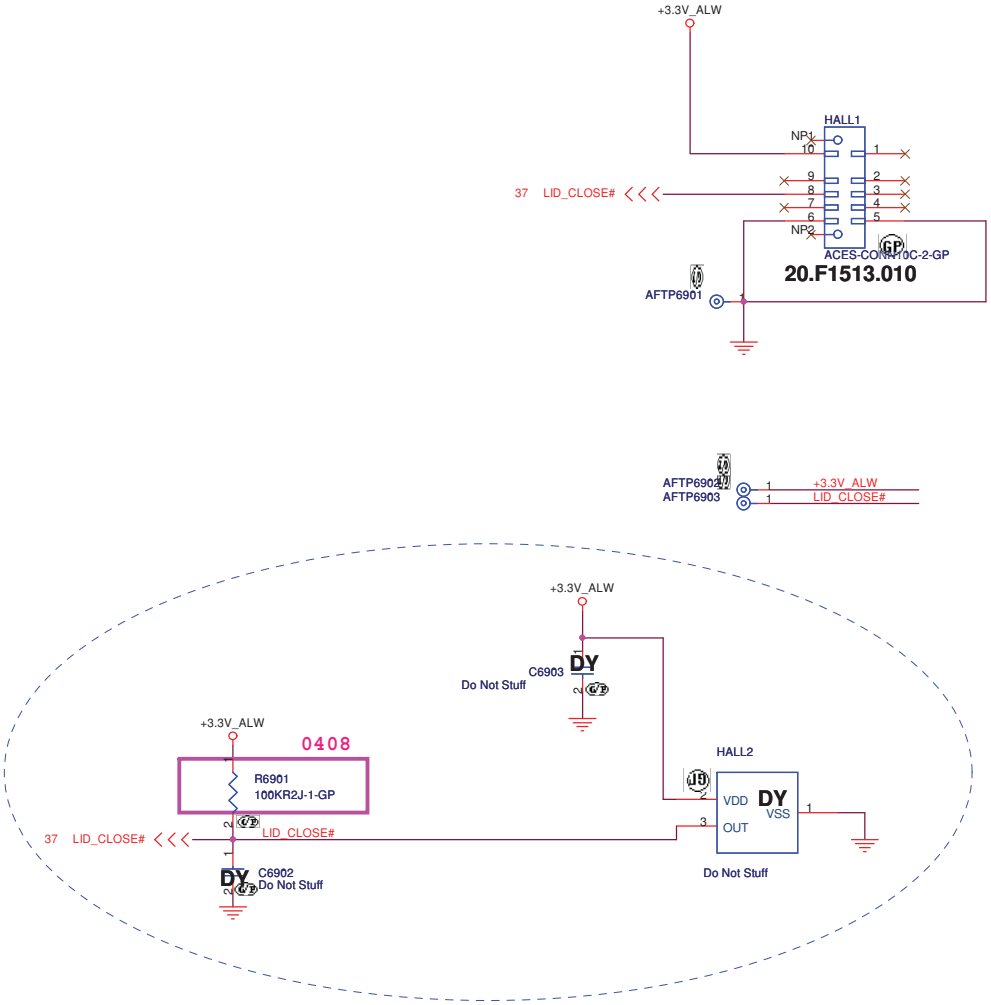


3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 68 of 90	

SSID = User. Interface



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

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A3	Chelsea DJ2 AMD UMA	X01

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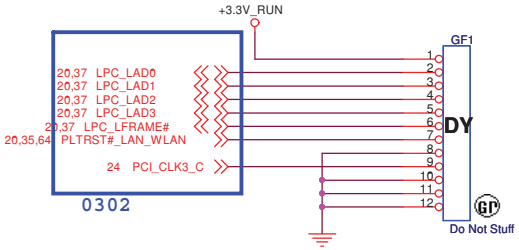

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*X01*

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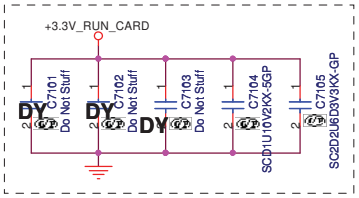
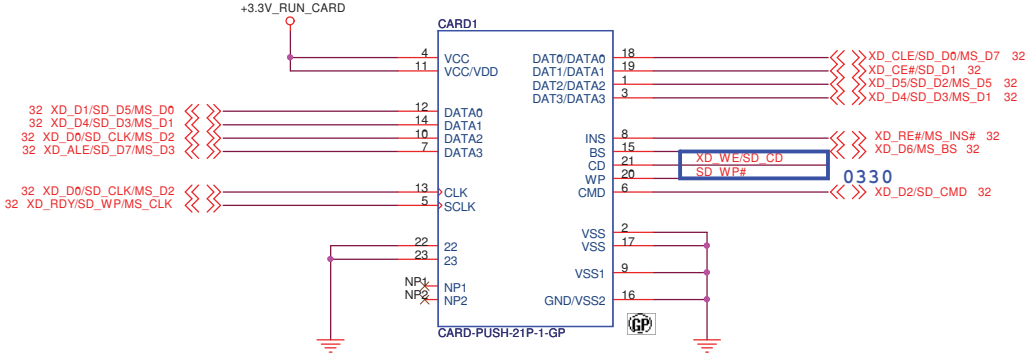
SSID = SDIO

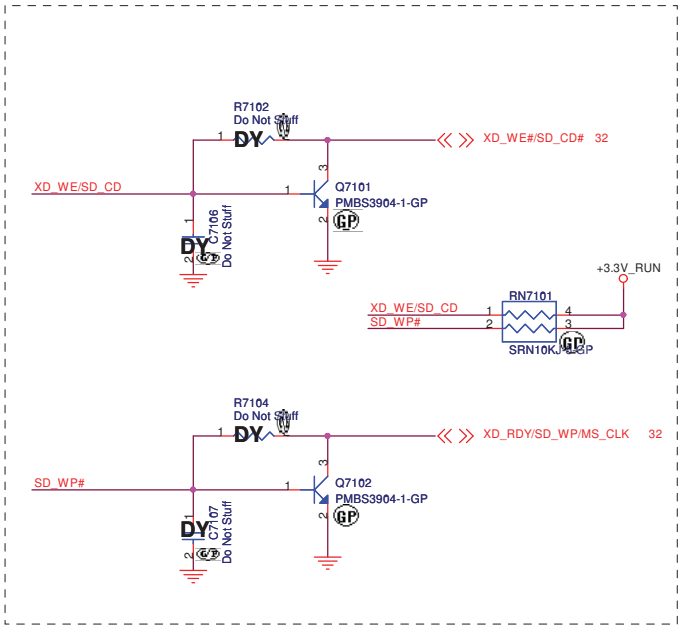
SD/XD/MS Card Reader





20.I0110.011

For reverse card connector 0330



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader Connector

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A3	Chelsea DJ2 AMD UMA	X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

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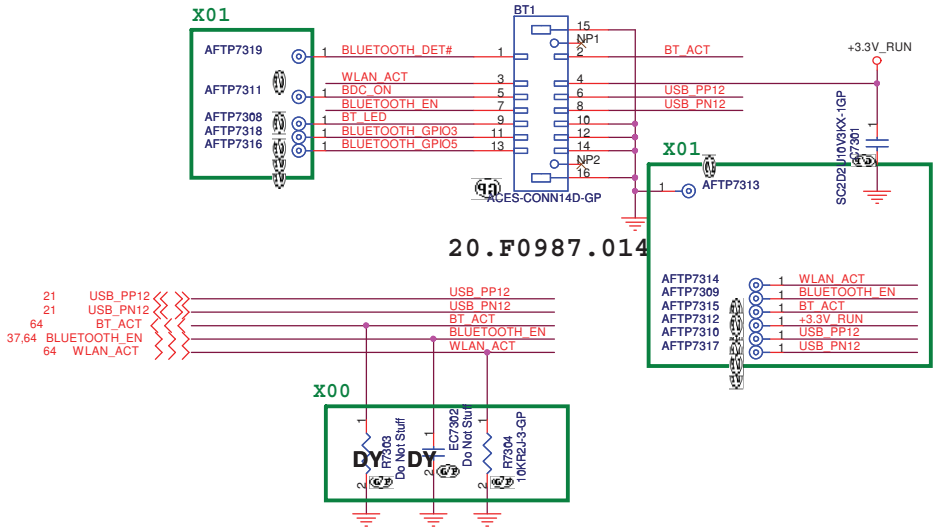
SSID = User.Interface

Bluetooth Module conn.



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*X01*

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 77 of 90

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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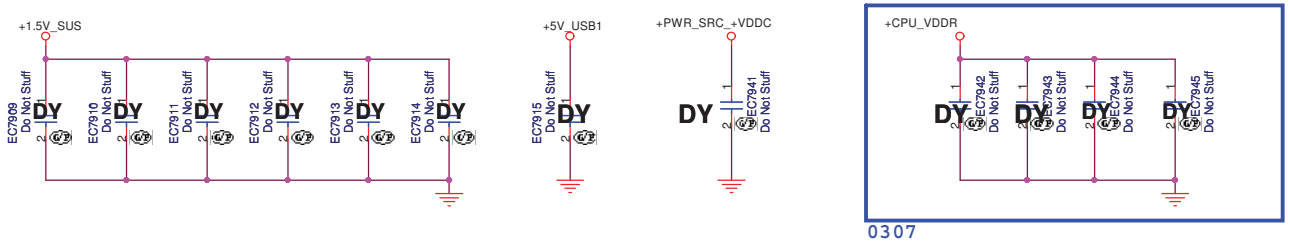
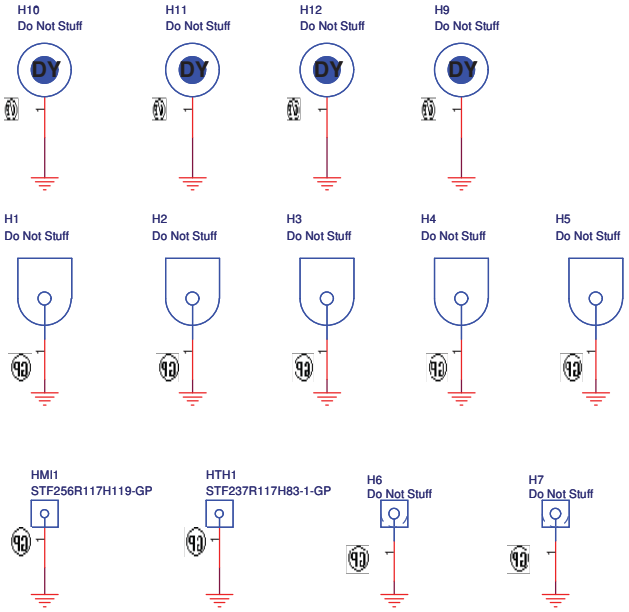
SSID = Mechanical

EMI Request





3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA PCIE(1/4)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA LVDS/TV/CRT(2/4)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA POWER/GND(3/4)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA MEMORY/STRAPS(4/4)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM (1/2)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM (2/2)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117_+VCC_GFXCORE

Size	Document Number	Rev
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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930_+1.1V_RUN

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: X01

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

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Change notes - Page 1

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	37	pop R3729 , depop R3733	MB version	EE
		2	37	DY R3712	compare DJ1 and DJ2 (for battery)	EE
		3	71	add R7101~R7104; C7106~C7107; Q7101~Q7102	For reversal cardreader connector	EE
		4	69	pop R6901	For lid_close# PU when Hall sensor BD not connect	EE
		5	70	depop GF1	non-pop debug port	EE
		6	42	C4203 from 100pF to 4.7nF	For sequence	EE
		7	61	reserve U6103, U5104, U6105	For LAN Surge	EE
		8	47	PR4720 change to 95.3Kohm(64.95325.6DL). PR4721 change to 22Kohm(64.22025.6DL).	For CPU_CORE OCP	EE
		9	20	RN2006 from 0R to 10R	For CLK_LAN slew rate fail	EE
		10	55	C5508~C5510 from 8.2pF to 10pF L5501~L5503 change to 33 ohm bead	For EMI request	EMI
		11	79	add SPR3 and SPR4	For EMI request	EMI
		12	63 21	add C6307~C6312 ; C2106~C2107 4.7pF	Fine tune USB signal	EE

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: Custom | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 89 of 90

Change notes - Page 2

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: Custom | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *X01*

Date: Tuesday, April 13, 2010 | Sheet 90 of 90