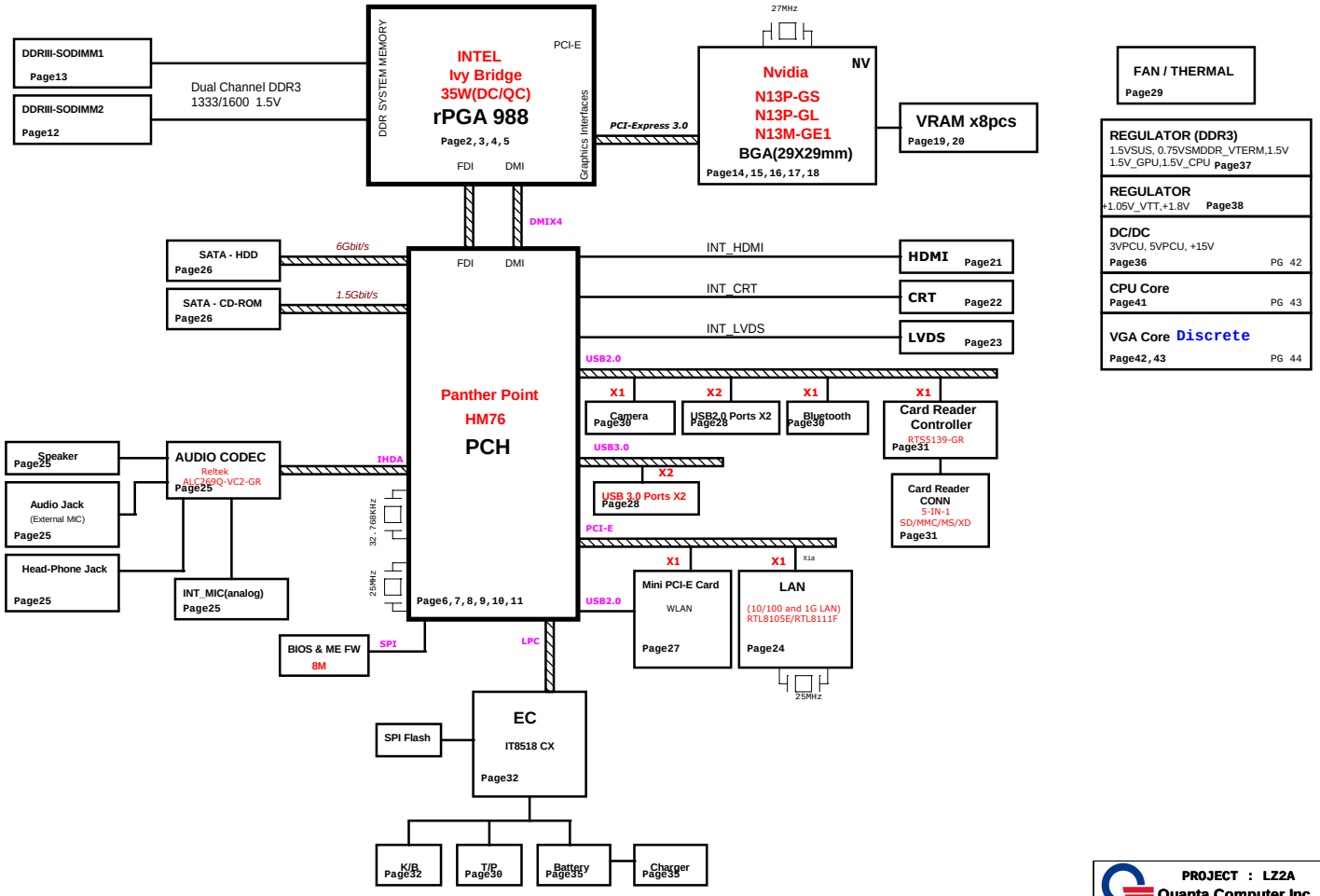
LZ3/LZ3A (Z580) Intel Chief River Platform (Optimus) Block Diagram



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Quanta Computer Inc.

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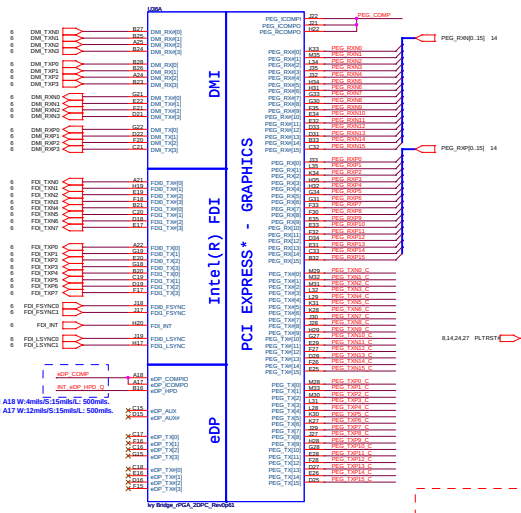
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

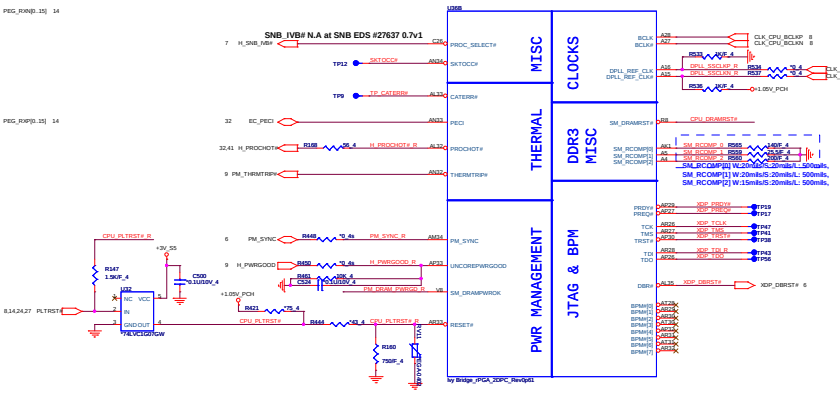
4,6,7,8,10,33,34,38,43 +1.05V_PCH
4,10,12,13,33,34,37,43 +1.05V_SUS
6,7,8,9,10,27,33,34 +3V_S5
4,33 +1.5V_CPU

Ivy Bridge Processor (DMI,PEG,FDI)



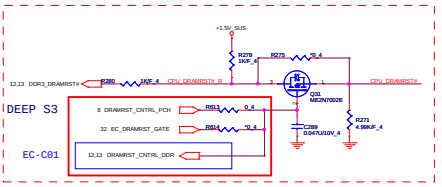
eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

Ivy Bridge Processor (CLK,MISC,JTAG)



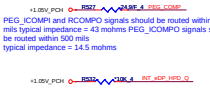
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils.
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils.
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils.

FOR DEEP S3



PEG x16 (UMA Non-stuff)

DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

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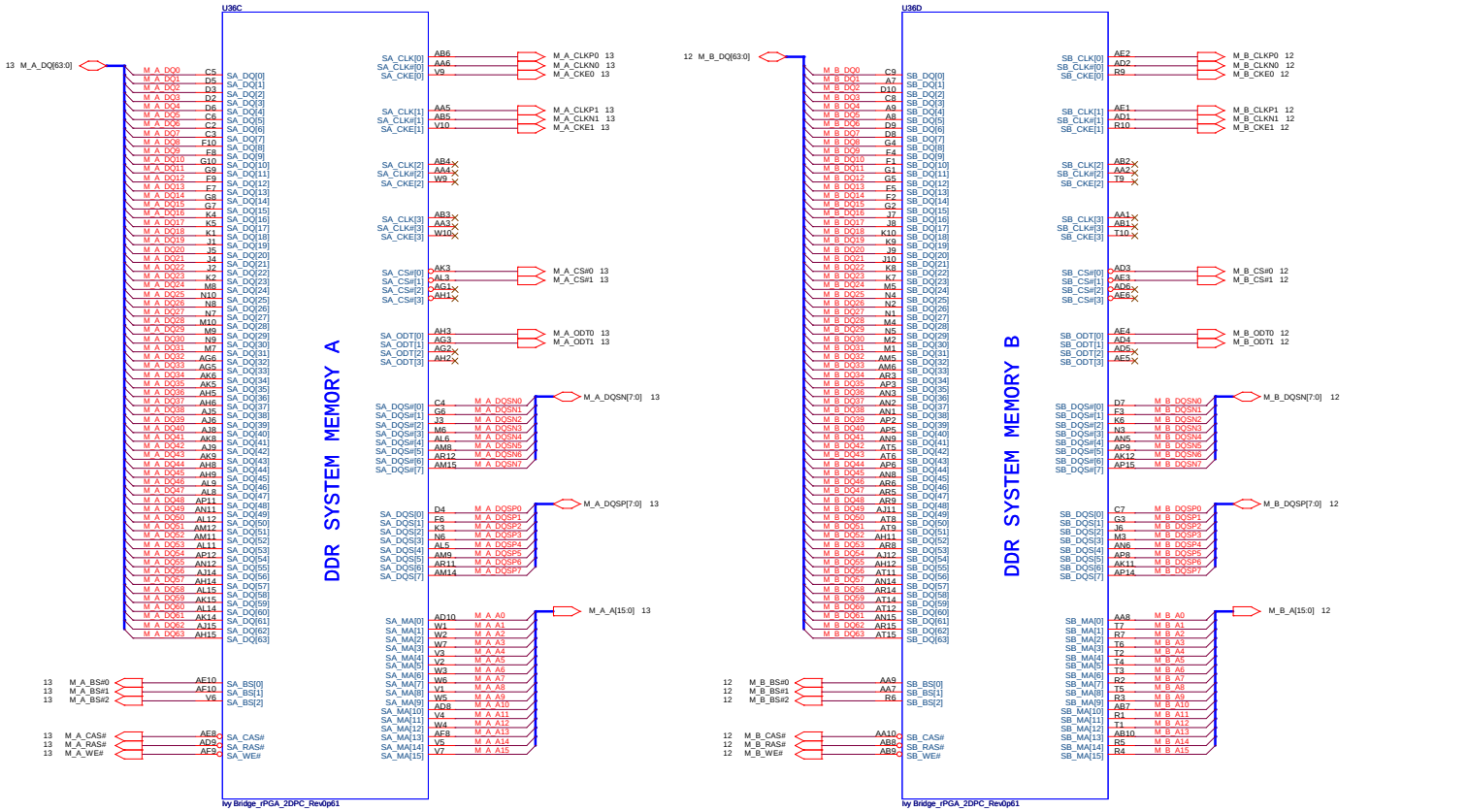
Ivy Bridge Processor (DDR3)



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Ivy Bridge Processor

Ivy Bridge Processor (GRAPHIC POWER)

04

CPU Core Power

SNB: 55A
IVY: 55A

SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

22uF_8 x8 Socket TOP cavity

22uF_8 x10 Socket TOP edge

10uF_8 x10 Socket BOT cavity

POWER

PEG AND DDR

SVID

SENSE LINES

CORE SUPPLY

CPU VTT

SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity

22uF (Reserved)

CPU VGT

SNB 45W:33A
22uF x 12
22uF x 4 (Reserved)

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

CPU MCH

SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

SNB: 5A
IVY: 5A

330uF x1, 10uF_8 x6 Socket BOT edge.

22uF (Reserved)

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

CPU VCCPL

SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU SA

SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

SNB: 6A
IVY: 6A

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

4.5A

Placement close to CPU.

0.5A

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Close to VR

Place PU resistor close to CPU

SVID DATA

Close to VR

Place PU resistor close to CPU

SVID ALERT

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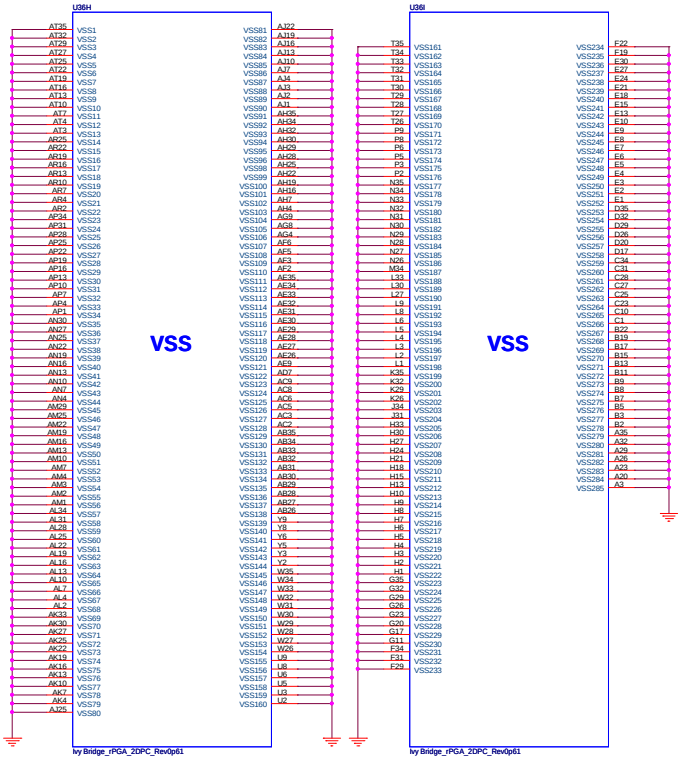
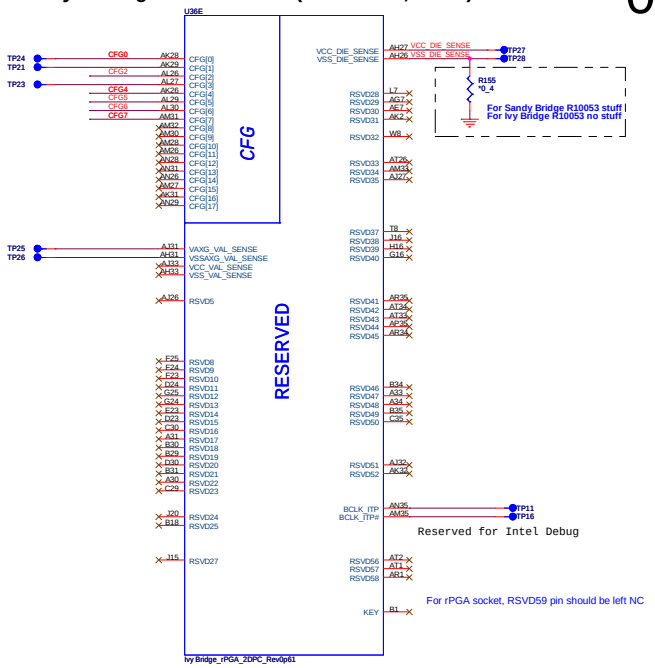
Ivy Bridge Processor (GND)



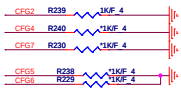
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

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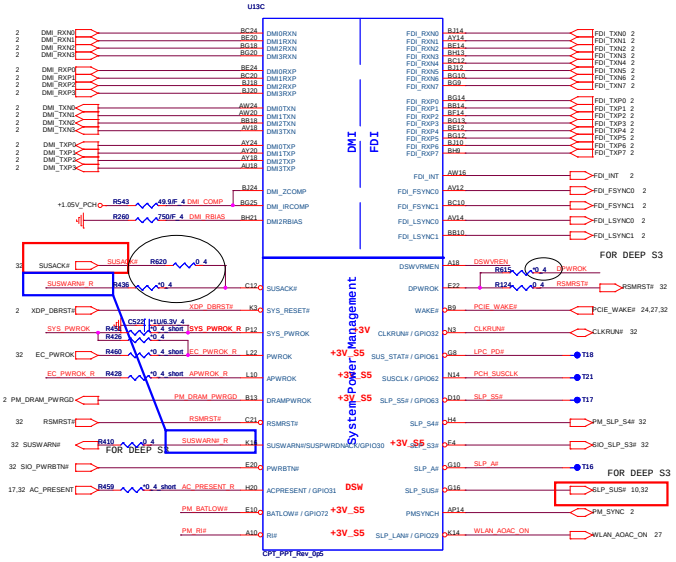
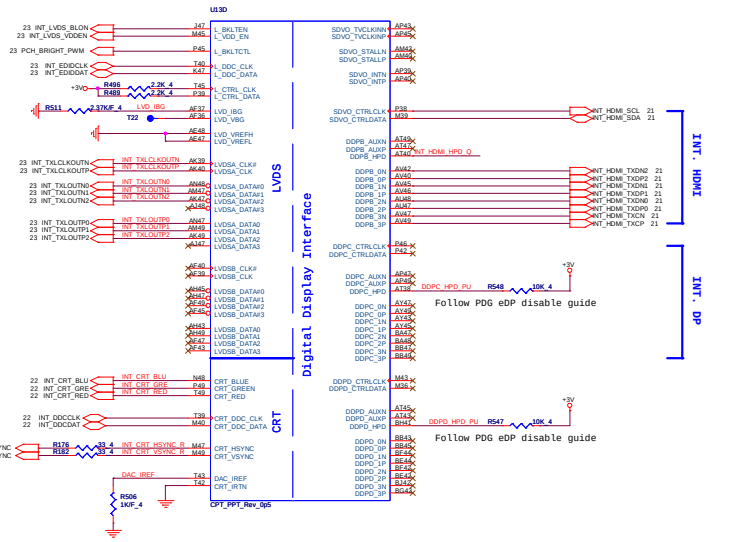
2,4,7,8,10,33,34,38,43 +1.05V_PCH
7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
2,7,8,9,10,27,31,34 +3V_S5
7,10,32 +3V_RTC

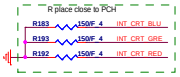
Cougar Point/Panther Point (DMI,FDI,PM)

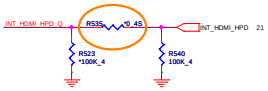


Cougar Point/Panther Point (LVDS,DDI)

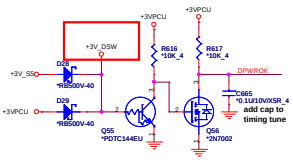


R place close to PCH

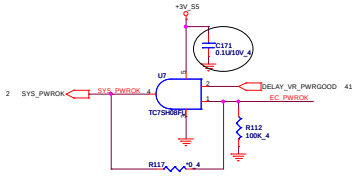


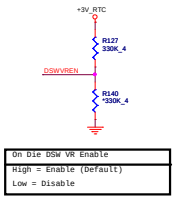


DPWROK FOR DSW (DEEP S3)

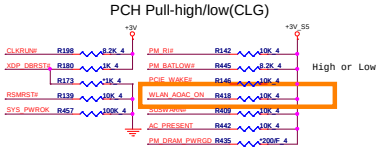


System PWR_OK(CLG)





PCH Pull-high/low(CLG)



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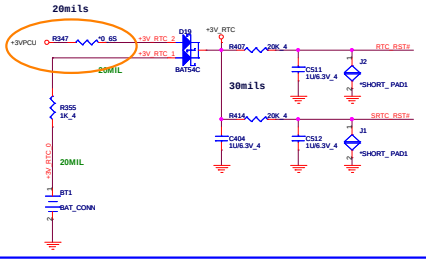
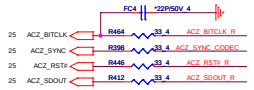
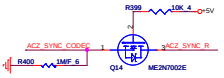
RTC Circuitry(RTC)



HDA Bus(CLG)

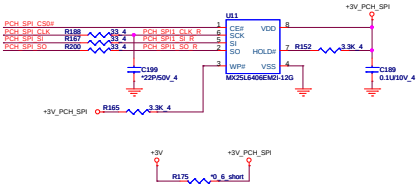




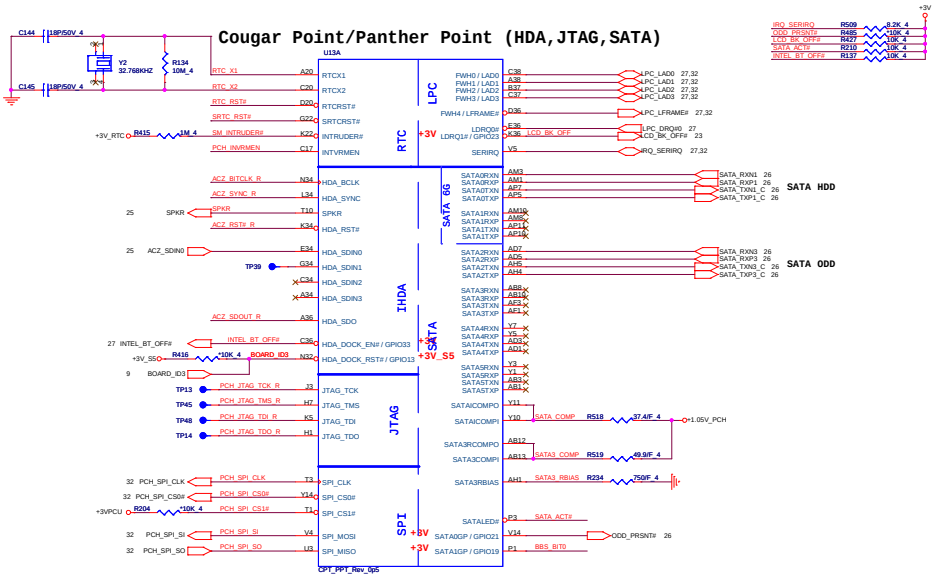
PCH Dual SPI (CLG)

32Mbit (8M Byte), SPI

AKE3EFP0N04: W25Q64CVSSIG
AKE3ENF0Q00: EN25Q64-104HIP
AKE3NFP0Z00: MX25L6406EM2I-12G
Socket: D6008000031



PCH2(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R514 *1K_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R472 *1K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R114 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R471 *1K_4 BBS_BIT1 8 R203 *1K_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R411 *1K_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R254 2.2K_4 +1.8V R255 1K_4 DF_TVS 9 H_SNB_VB# 2
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R490 *1K_4 PLL_ODVR_EN 9
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R413 1K_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R181 *1K_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

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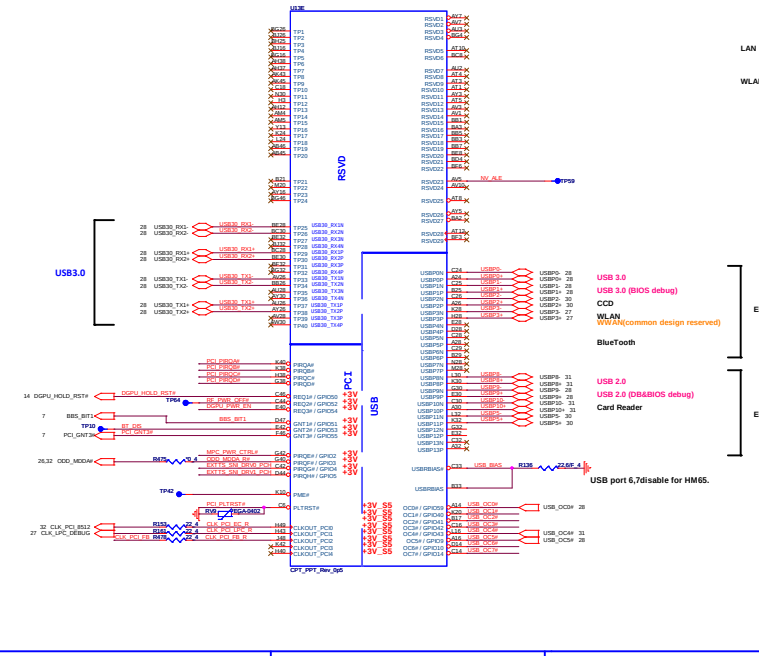
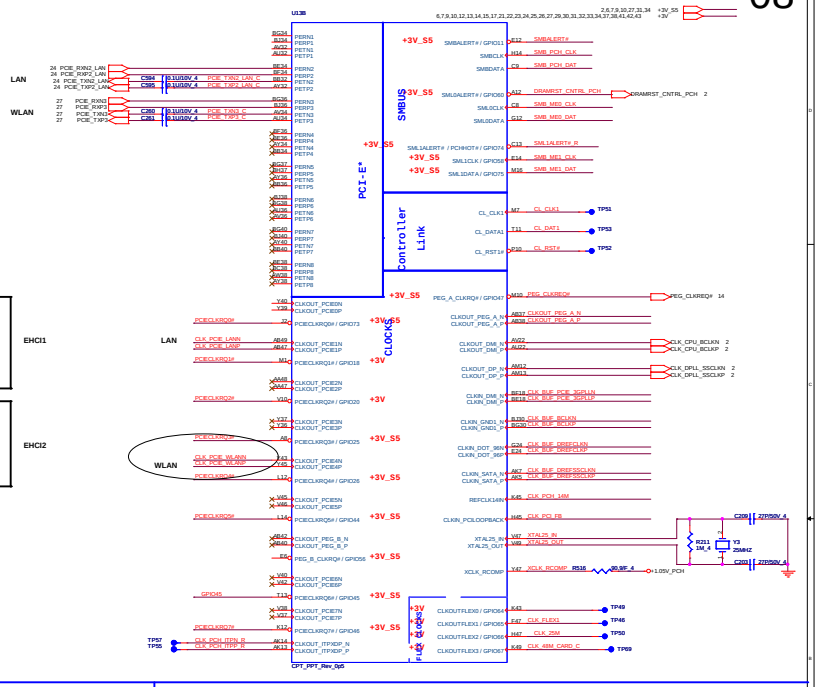
Cougar Point-M/Panther Point (PCI,USB,NVRAM)

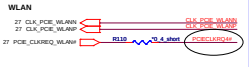


Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

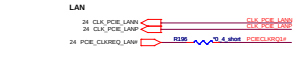


DGPU Power ON

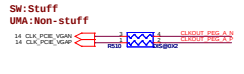
WLAN



LAN



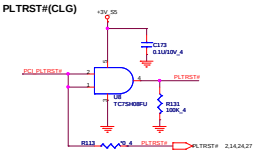
SW:Stuff UMA:Non-stuff



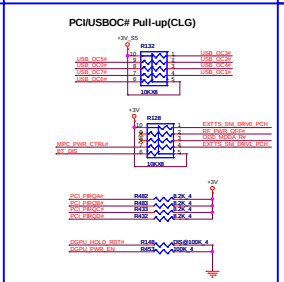
MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

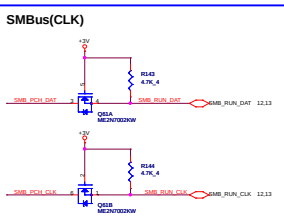
PLTRST#(CLG)



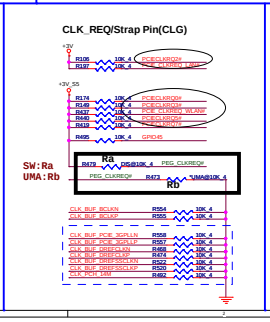
PCI/USBOC# Pull-up(CLG)



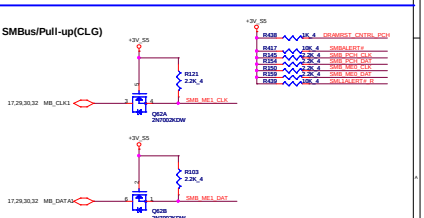
SMBus(CLK)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

09

2,6,7,8,10,27,31,34 +3V_S5
6,7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V

U13F

GPIO / CPU/MISC / NCTF

S_GPIO R507 100_4	T7	BMBUSY# / GPIO0	+3V
32 EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V
BOARD_ID1	H36	TACH2 / GPIO6	+3V
32 EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V
TP8 ICC_EN#	C10	GPIO8	+3V_S5
27 LAN_DISABLE#	C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5
HOST_ALERT#1_R	G2	GPIO15	+3V_S5
BOARD_ID2	U2	SATA4GP / GPIO16	+3V
14,43 GFXPG R100 *0_4 short GFXPG_R	D40	TACH0 / GPIO17	+3V
BIOS_REC	T5	SCLOCK / GPIO22	+3V
SYSTEM_ID1	E8	GPIO24 / MEM_LED	+3V_S5
GPIO27	E16	GPIO27	DSW
7 PLL_ODVR_EN R494 *0_4 short PLL_ODVR_EN_R	P8	GPIO28	+3V_S5
SYSTEM_ID0	K1	STP_PCI# / GPIO34	+3V
30 BT_ON#	K4	GPIO35	+3V
30 CCD_ON#	V8	SATA2GP / GPIO36	+3V
FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V
MFG_MODE	N2	SLOAD / GPIO38	+3V
DGPU_PRSNT#	M3	SDATAOUT0 / GPIO39	+3V
TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V
29,32 TEMP_ALERT#	V3	SATA5GP / GPIO49	+3V
SV_DET	D6	GPIO57	+3V_S5

TACH4 / GPIO68	+3V	C40	FB_CLAMP_PCH
TACH5 / GPIO69	+3V	B41 R122 1.5K/F_4	
TACH6 / GPIO70	+3V	C41	GPU_EVENT_PCH#
TACH7 / GPIO71	+3V	A40	PCB_LAYER_ID
+3V_S5		A20GATE	P4
		PECI	AU16
		RCIN#	P5
		PROCPWRGD	AY11
		THRMTRIP#	AY10
		INIT3_3V#	T14
		DF_TVS	AY1
		TS_VSS1	AH8
		TS_VSS2	AK11
		TS_VSS3	AH10
		TS_VSS4	AK10
		NC_1	P37

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CPT_PPT_Rev_0p5

R25 10K/F_4
R118 *GS@0_4 FB_CLAMP 15
R122 1.5K/F_4
R462 *GS@0_4 GPU_EVENT# 17
R634 10K/F_4@GS@NC +3V

NVidia N13P-GS

EC_A20GATE 32
TP58
EC_RCIN# EC_RCIN# 32
H_PWRGOOD 2
PCH_THRMTRIP# R539 390_4 PM_THRMTRIP# 2
DF_TVS 7

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R162 10K_4

+3V
EC_EXT_SMI# R130 10K_4
EC_EXT_SCI# R431 10K_4
EC_A20GATE R488 10K_4
EC_RCIN# R500 10K_4
TEMP_ALERT# R223 10K_4
BT_ON# R481 10K_4
GPIO27 R441 10K_4

Board ID

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT	0	1	1
SOVP	1	0	0

LZ1,LZ2,LZ3

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0.1]:
-->LZ1 [0.0]
-->LZ2 [0.1]
-->LZ3 [1.0]

+3V
R209 *10K_4 BOARD_ID2 R213 10K_4
R429 10K_4 BOARD_ID1 R430 *10K_4
R129 *10K_4 PCB_LAYER_ID R138 10K_4
R187 *10K_4 SYSTEM_ID0 R179 10K_4
+3V_S5
R476 10K_4 SYSTEM_ID1 R467 *10K_4
R503 10K_4 BOARD_ID3 R443 *10K_4
BOARD_ID3 7

Arvin Wang update table on 9/19 14:12

LZ2	BOARD_ID0 GPIO 71	SYSTEM_ID0 GPIO 34	SYSTEM_ID1 GPIO 24
6 Layer	0	0	1
8 Layer	1	0	1

SV_SET_UP
High = Strong (Default)

+3V
TEST_SET_UP R194 10K_4 R185 *0_4

+3V_S5
R456 *10K_4 SV_DET R458 100K_4

+3V_S5
HOST_ALERT#1_R R466 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

+3V
R195 *10K_4 DGPU_PRSNT# R186 DIS@100K_4

SGPIO

+3V
S_GPIO R508 10K_4 R505 *0_4

+3V
R491 100K_4 FDI_OVRVLTG R486 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
CCD_ON# R515 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R499 10K_4 R501 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

+3V
MFG_MODE R199 10K_4 R202 *0_4

PROJECT : LZ2A
Quanta Computer Inc.

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	Panther Point 4/6	1A

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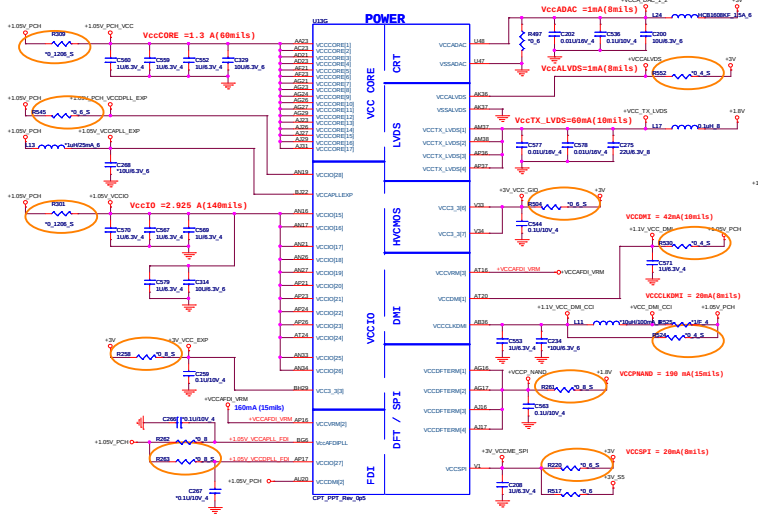
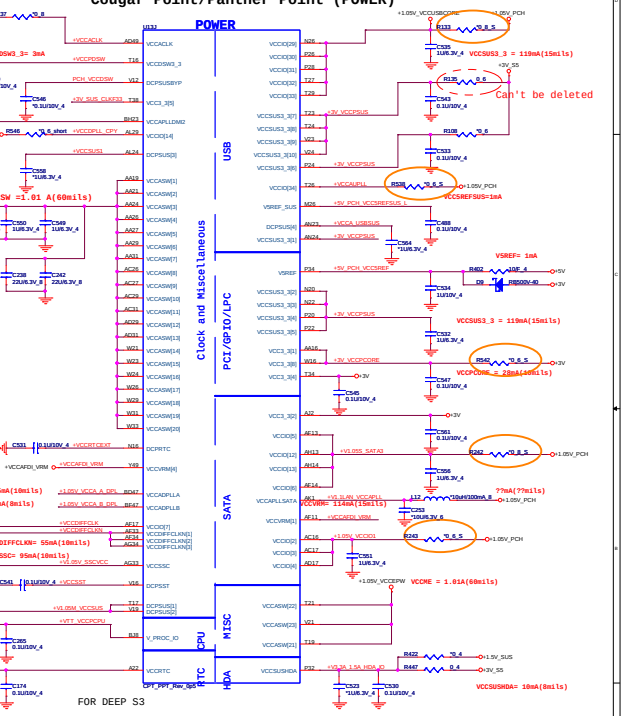
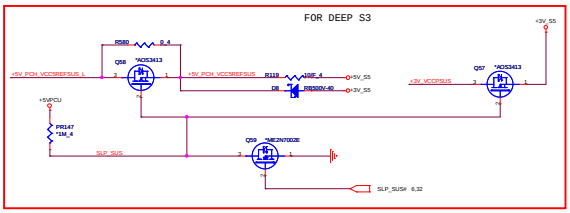
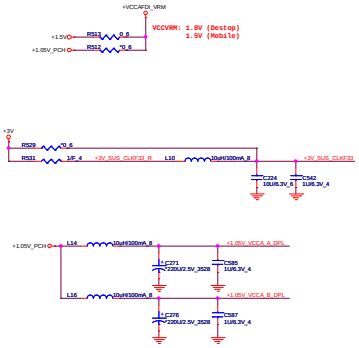
Cougar Point/Panther Point (POWER)









PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: Panther Point 5/6 Rev: 1A
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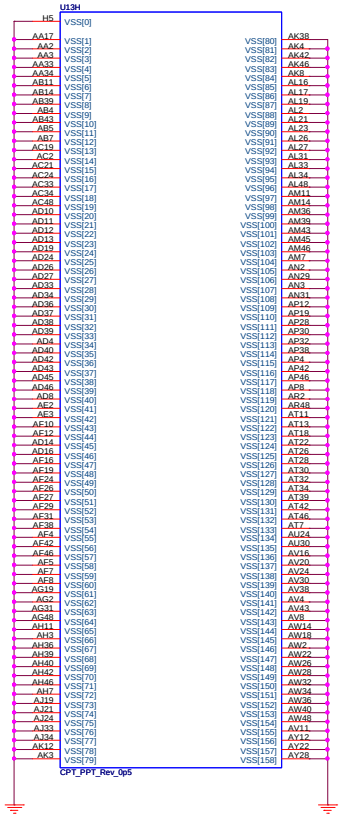
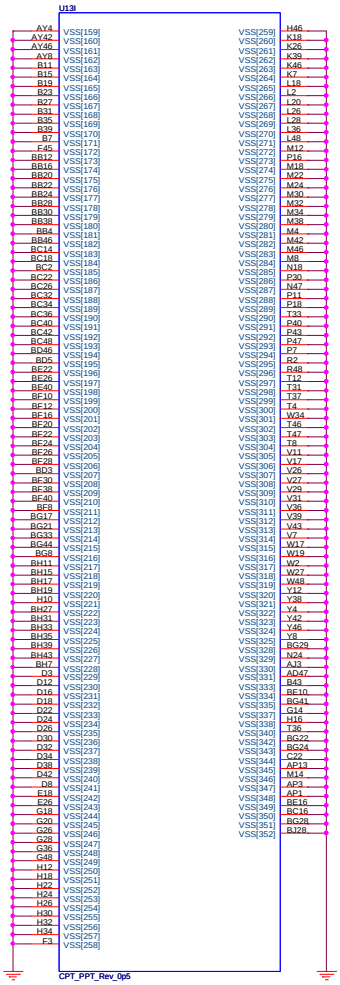
Cougar Point/Panther Point (GND)





	PROJECT : LZ2A Quanta Computer Inc.	
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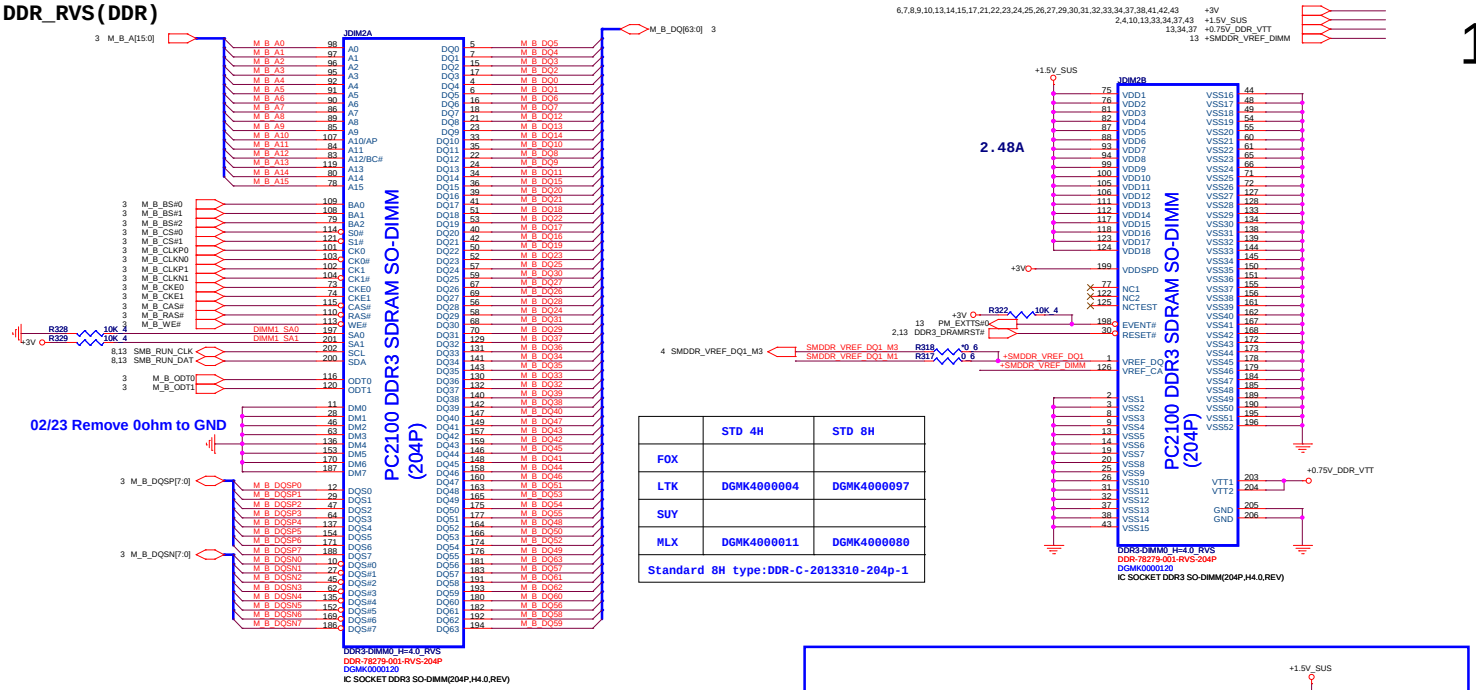
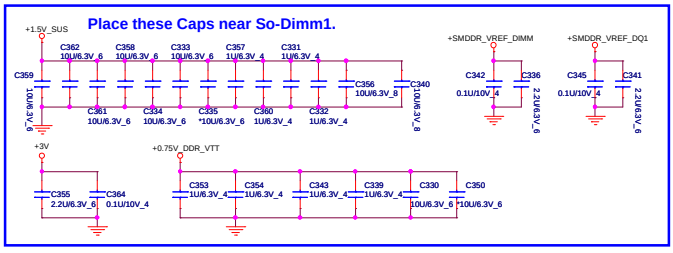
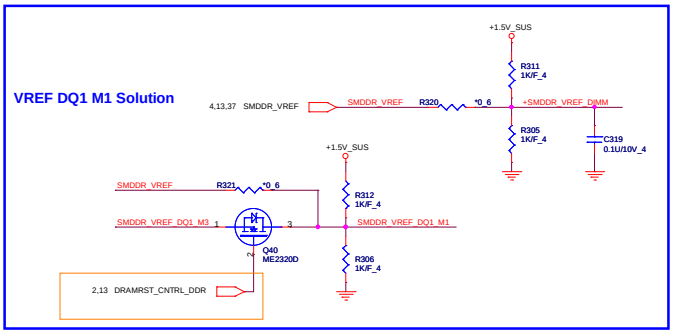
DDR_RVS(DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1





Size	Document Number: DDRIII SO-DIMM-0 — Rev: 1A
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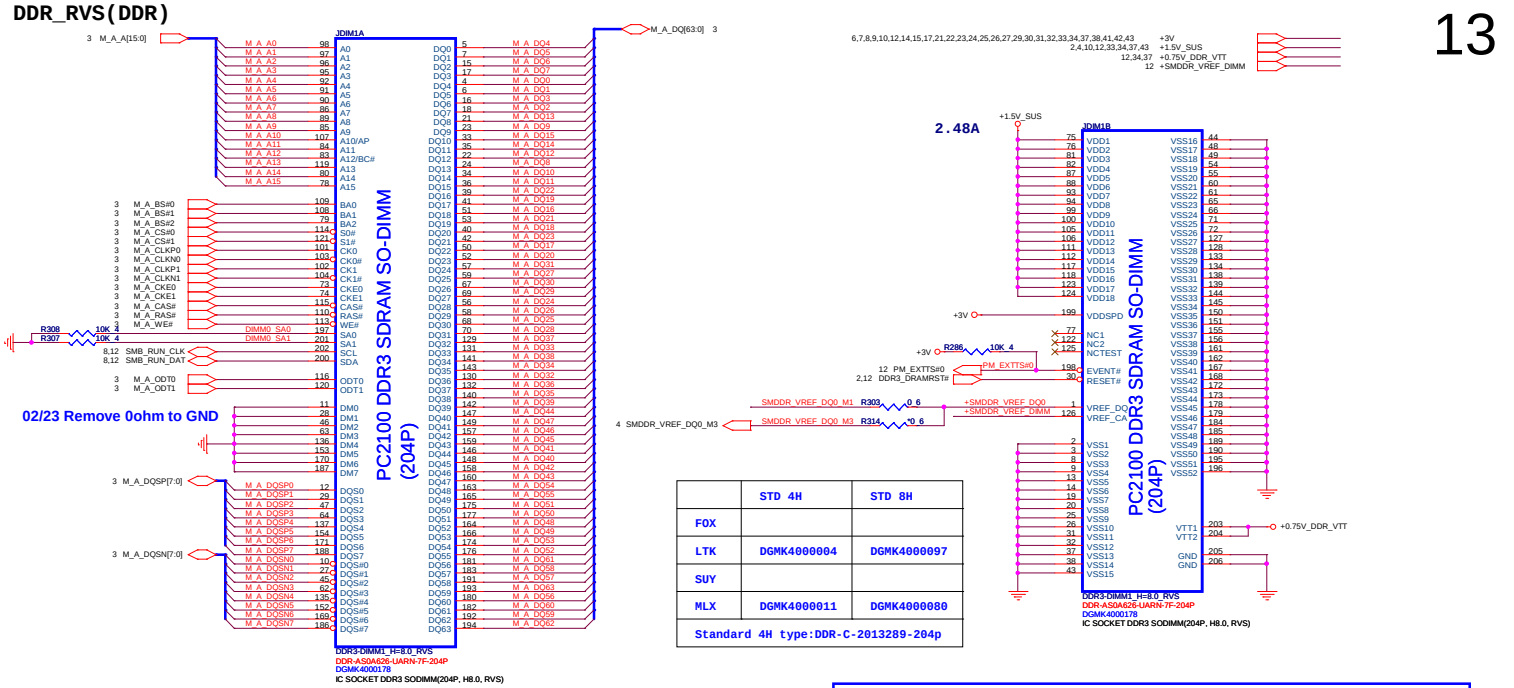
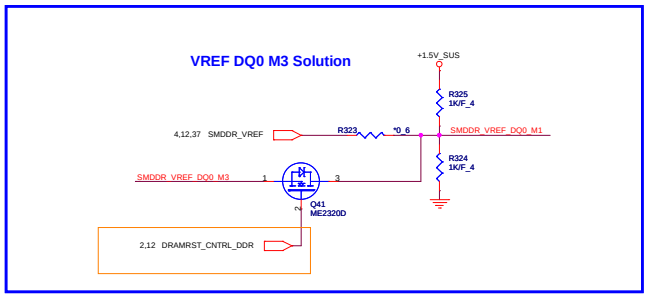
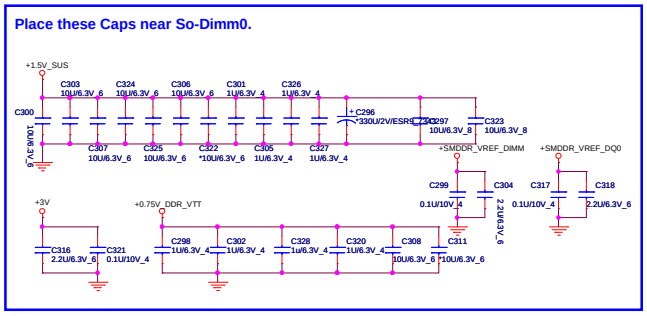
PROJECT : LZ2A
Quanta Computer Inc.

DDR_RVS(DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		





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Quanta Computer Inc.		
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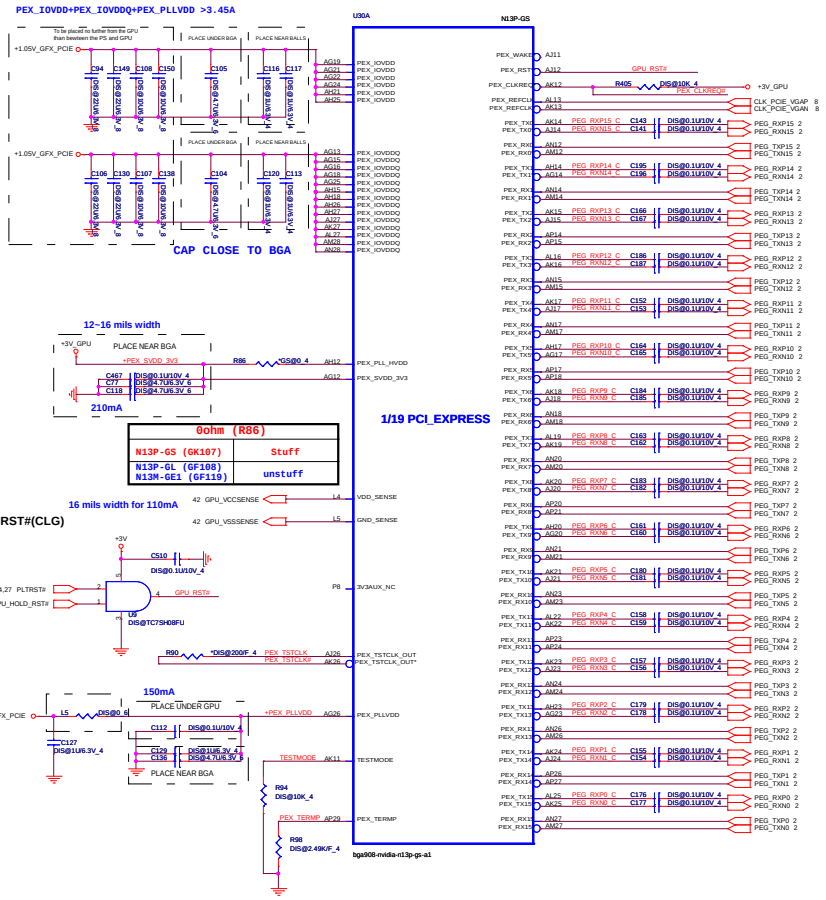
15,16,33,43 +1.05V_GFX_PCIE
17,18,43 +3V_GPU
15,19,20,33,43 +1.5V_GPU
6,7,8,9,10,12,13,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
18,33,42 GFX_CORE



0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

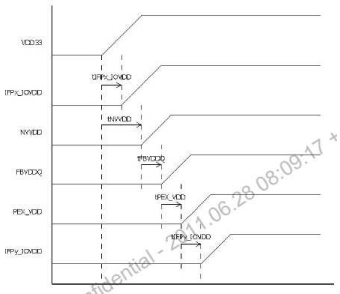


Figure 17. Recommended Power On Sequencing Order

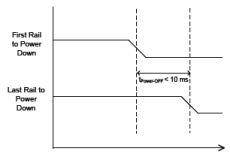
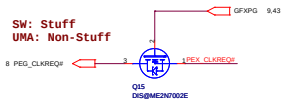


Figure 18. Recommended Power Off Sequencing Order

For power-down sequency

PEG CLK detect



	PROJECT : LZ2A Quanta Computer Inc.	
Size	Document Number Nvidia-N13P GB4-128(PCIe)	Rev 1A
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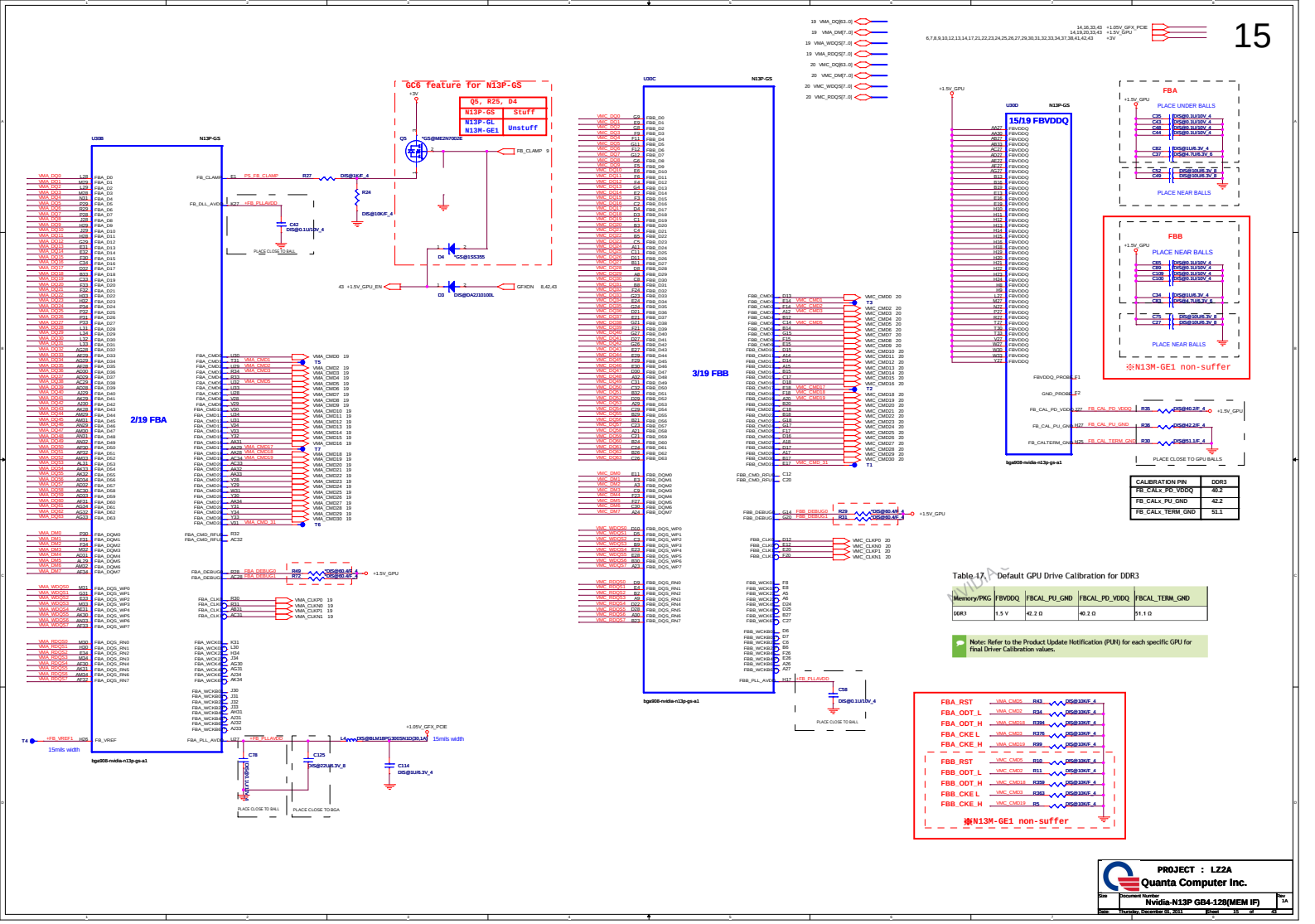
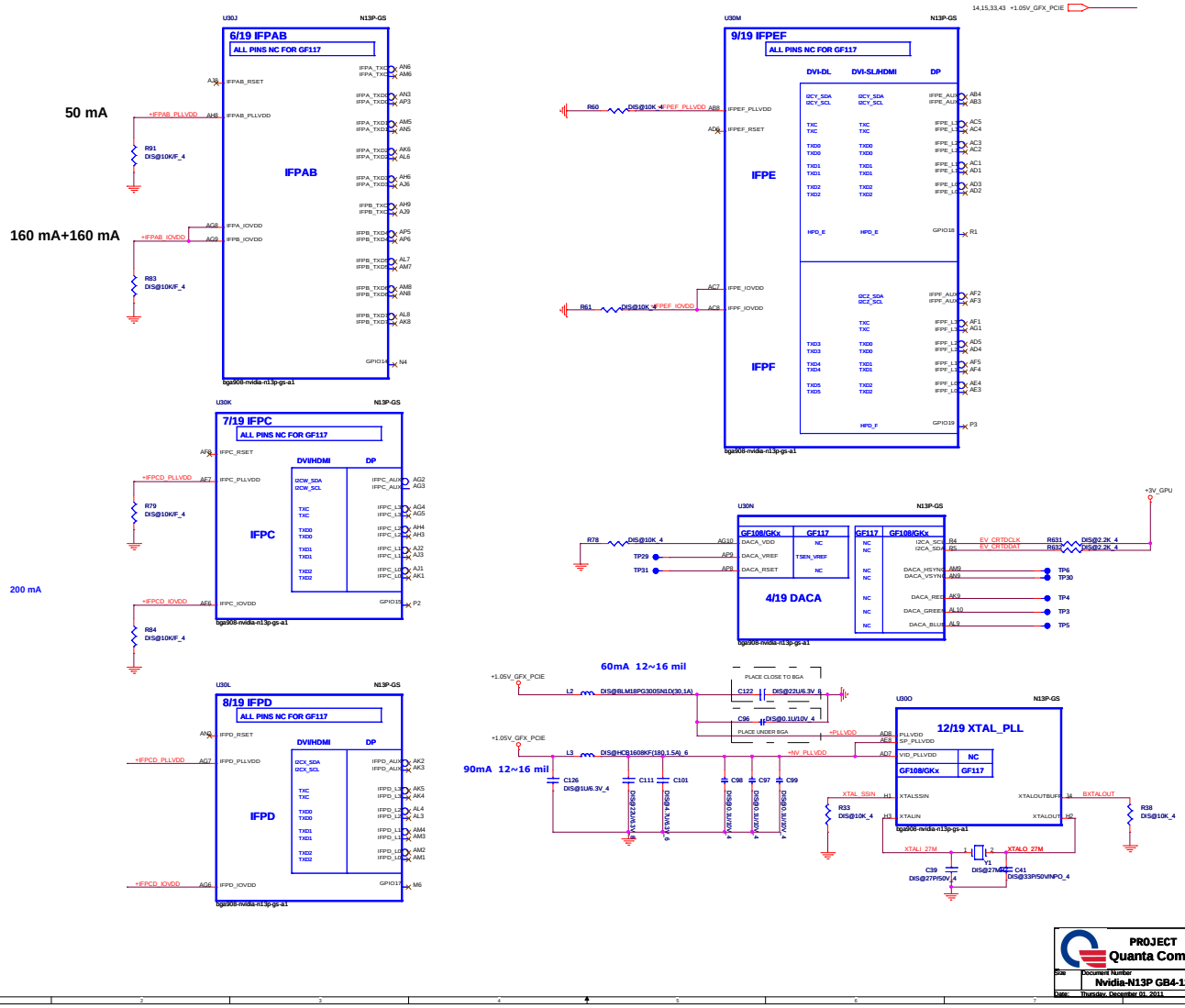

GC6 feature for N13P-GS
Q5, R25, D4
N13P-GS Stuff
N13P-GL Unstuff
N13M-GE1
Q5 *QS@MEZN7002E
D4 *QS@1SS355
D3 DIS@DA221010L
FB_CLAMP
FB_CLAMP_9
43 +1.5V_GPU_EN
GFXDN 8,42,43
U30B
N13P-GS
2/19 FBA
U30C
3/19 FBB
U30D
15/19 FBVDDQ
FBA
PLACE UNDER BALLS
PLACE NEAR BALLS
FBB
※N13M-GE1 non-suffer
CALIBRATION PIN
DDR3
FB_CALx_PD_VDDQ
40.2
FB_CALx_PU_GND
42.2
FB_CALx_TERM_GND
51.1
Table 17. Default GPU Drive Calibration for DDR3
Memory/PKG
FBVDDQ
FBCAL_PU_GND
FBCAL_PD_VDDQ
FBCAL_TERM_GND
DDR3
1.5 V
42.2 Ω
40.2 Ω
51.1 Ω
Note: Refer to the Product Update Notification (PUN) for each specific GPU for final Driver Calibration values.
FBA_RST
FBA_ODT_L
FBA_ODT_H
FBA_CKE_L
FBA_CKE_H
FBB_RST
FBB_ODT_L
FBB_ODT_H
FBB_CKE_L
FBB_CKE_H
※N13M-GE1 non-suffer
PROJECT : LZ2A
Quanta Computer Inc.
Nvidia-N13P GB4-128(MEM IF)
Thursday, December 08, 2011


50 mA
160 mA+160 mA
200 mA
90mA 12~16 mil
60mA 12~16 mil
6/19 IFPAB
ALL PINS NC FOR GF117
IFPAB
9/19 IFPEF
IFPE
IFPF
7/19 IFPC
IFPC
8/19 IFPD
IFPD
4/19 DACA
12/19 XTAL_PLL
U30J
U30K
U30L
U30M
U30N
U30O
N13P-GS
bga908-nvidia-n13p-gs-a1
+1.05V_GFX_PCIE
+3V_GPU
+PLLVDD
+NV_PLLVDD
XTAL_27M
XTALO_27M
PROJECT : LZ2A
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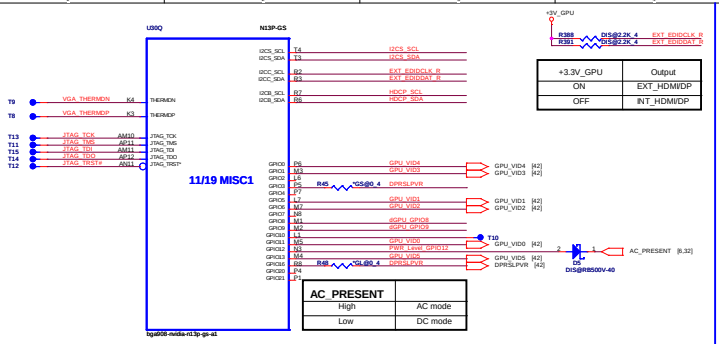
Nvidia-N13P GB4-128(Display)
Thursday, December 01, 2011



+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

AC_PRESENT	
High	AC mode
Low	DC mode

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DIP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24992FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402))
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

VRAM Configuration Table

※ROM_SI Strap Bit for RAM Mapping

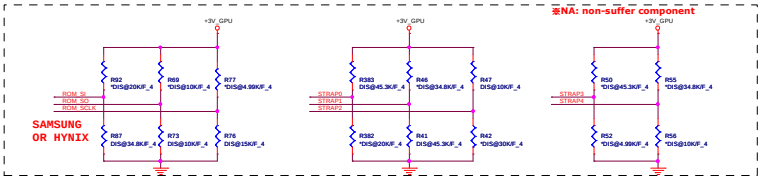
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU Model Strap Table

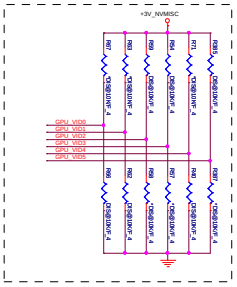
GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

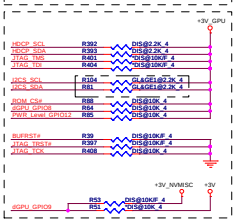
※NA: non-suffer component



NVVDD Table

	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)

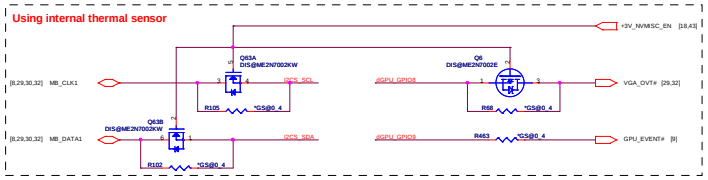




GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

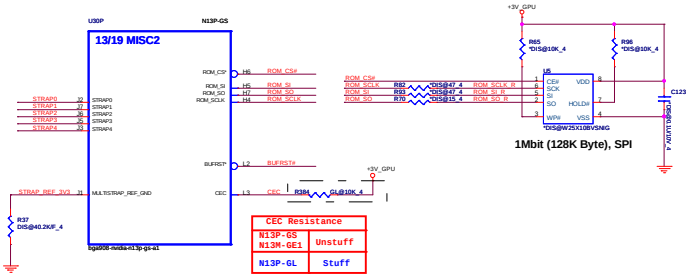
Using internal thermal sensor



	Q6,Q63, R81,R104	R68,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

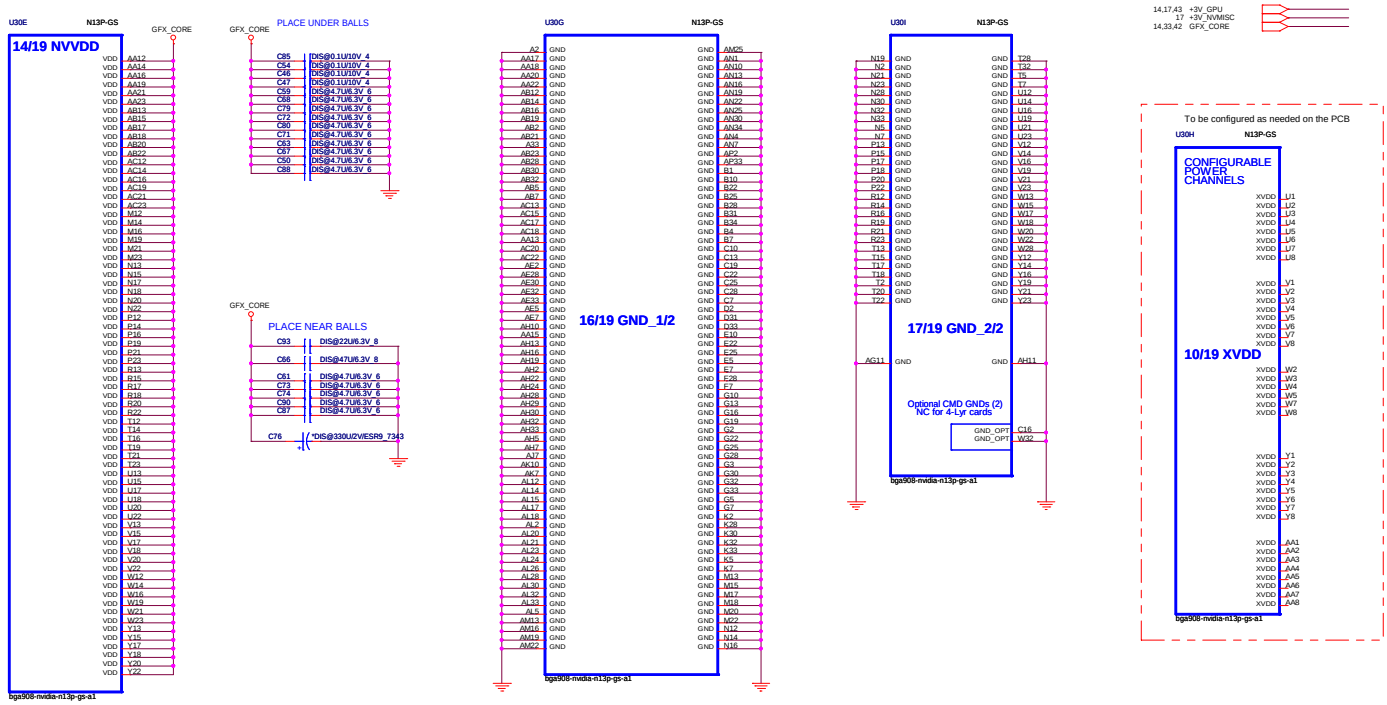


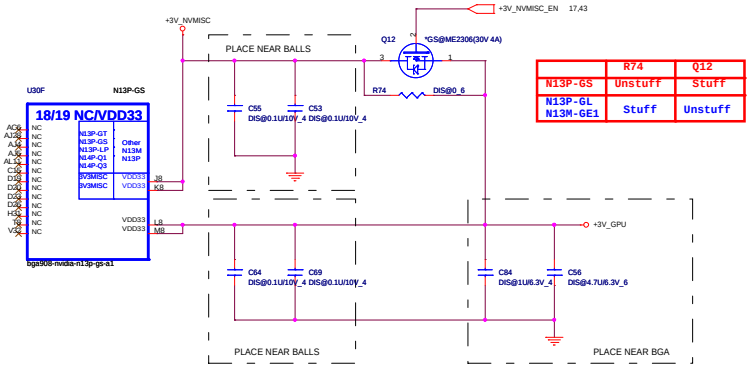
CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PES/-GL/-NS1 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/-GS/-LP and N14P-Q1/-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-NS1.

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: Nvidia-N13P GB4-128(GPIO/STRAP) Rev: 1A
Date: Thursday, December 01, 2011 Sheet: 17 of 45





	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

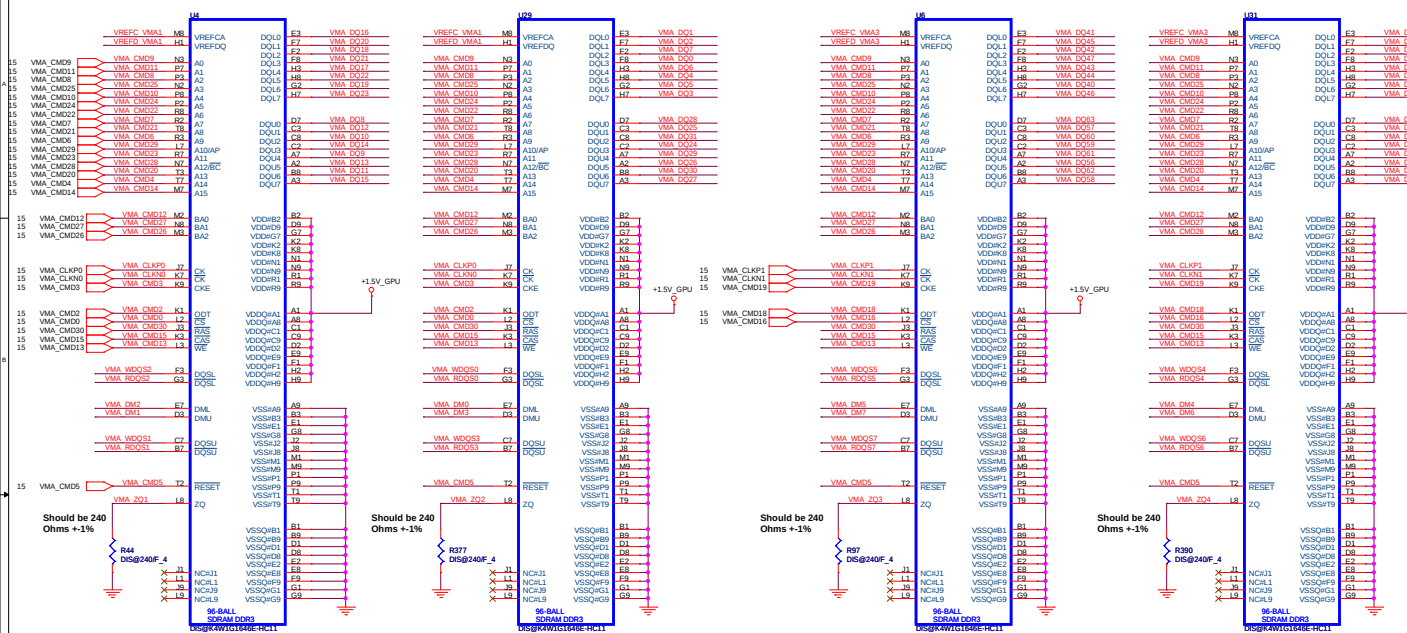
PROJECT : LZ2A
Quanta Computer Inc.

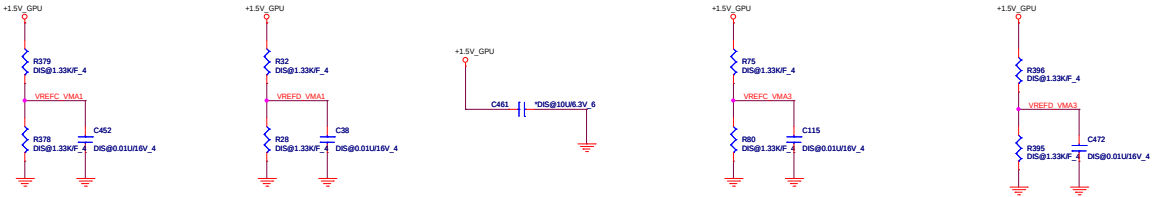
Size	Document Number	Rev
	Nvidia-N13P GB4-128(POWER)	1A
Date: Thursday, December 01, 2011	Sheet 18 of 43	

CHANNEL A: 512MB/1024MB DDR3

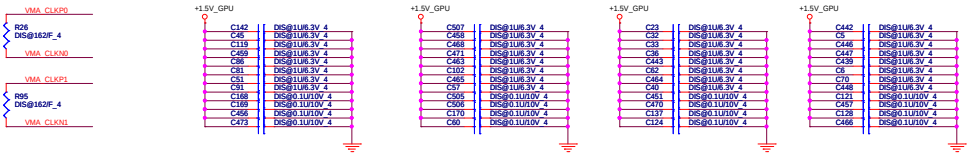
15 VMA_DQ[63..0]
15 VMA_DM[7..0]
15 VMA_WDQS[7..0]
15 VMA_RDQS[7..0]

14,15,20,33,43 +1.5V_GPU





Placement has to be close to VRAM

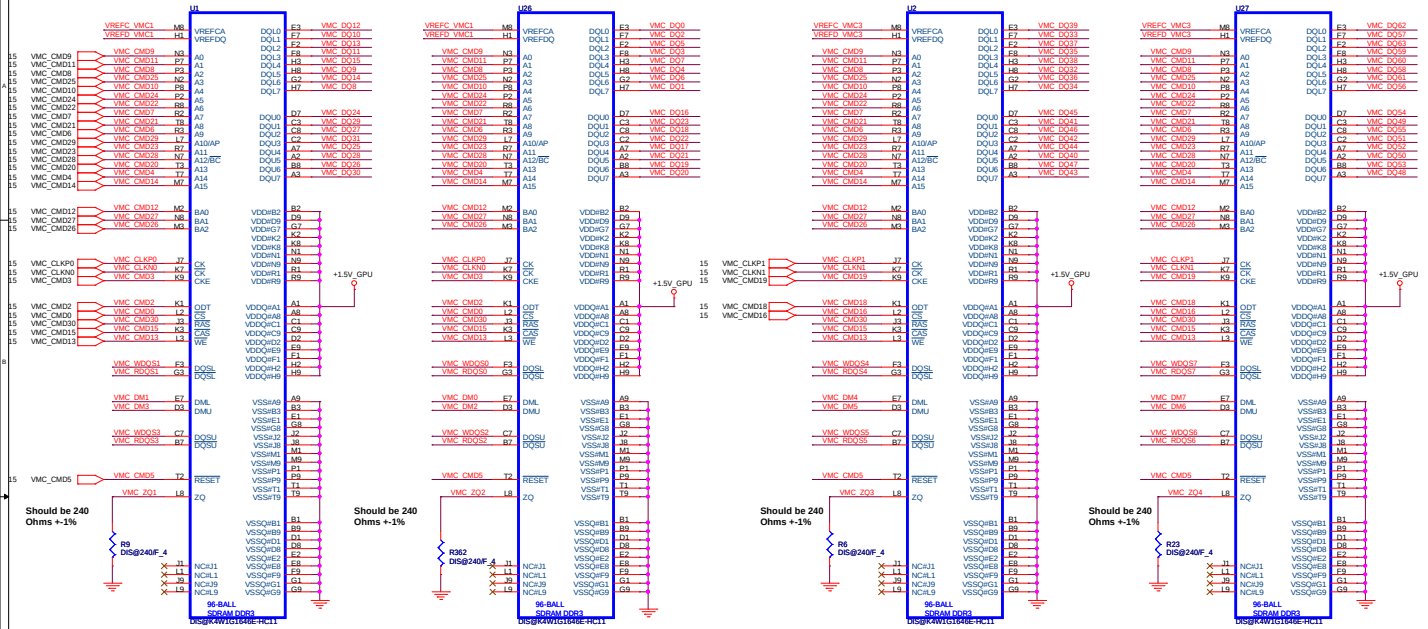


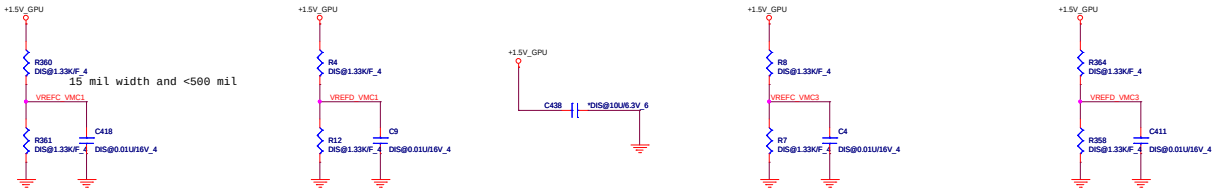
PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number		Rev
	Nvidia-N13P GB4-128(VRAM-1)		1A
Date: Thursday, December 01, 2011	Sheet 19 of 43		

CHANNEL B: 512MB/1024MB DDR3

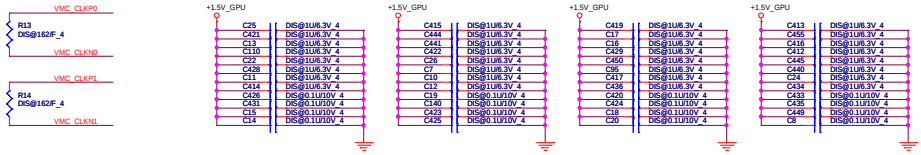
15 VMC_DQ[63..0]
15 VMC_DM[7..0]
15 VMC_WDQS[7..0]
15 VMC_RDQS[7..0]

14,15,19,33,43 +1.5V_GPU





Placement has to be close to VRAM



PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number		Rev
	Nvidia-N13P GB4-128(VRAM-2)		1A
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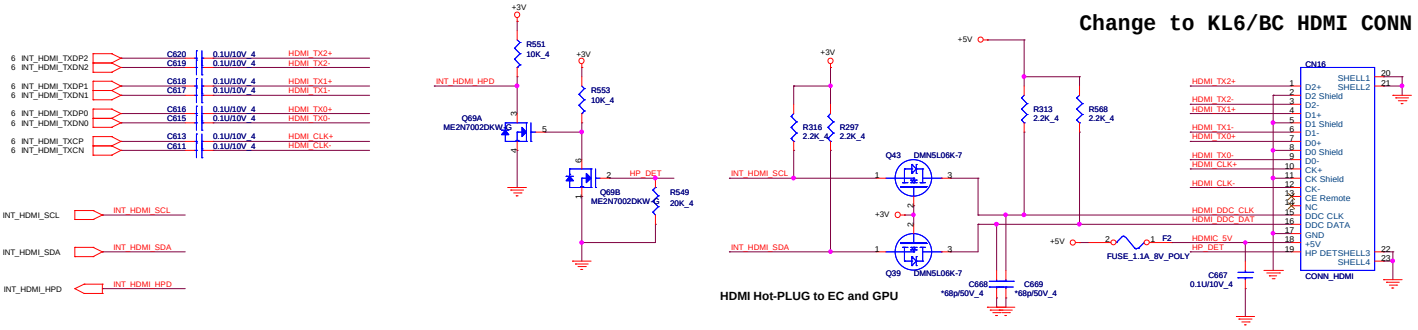
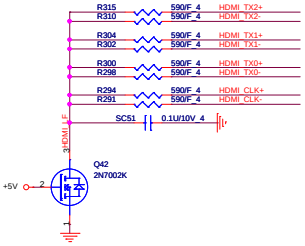
6,7,8,9,10,12,13,14,15,17,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
7,10,22,25,26,29,30,33,34 +5V

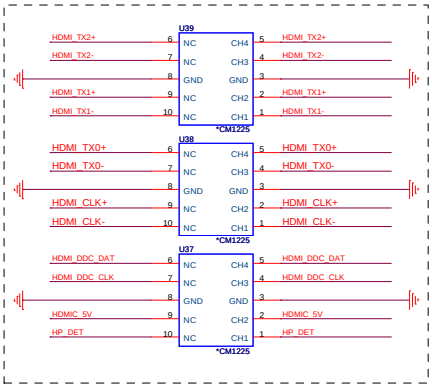
Change to KL6/BC HDMI CONN



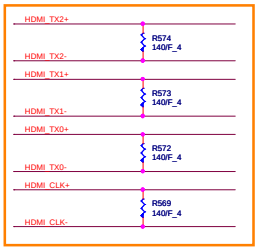
HDMI Hot-PLUG to EC and GPU



For ESD



EMI reserve for HDMI



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A
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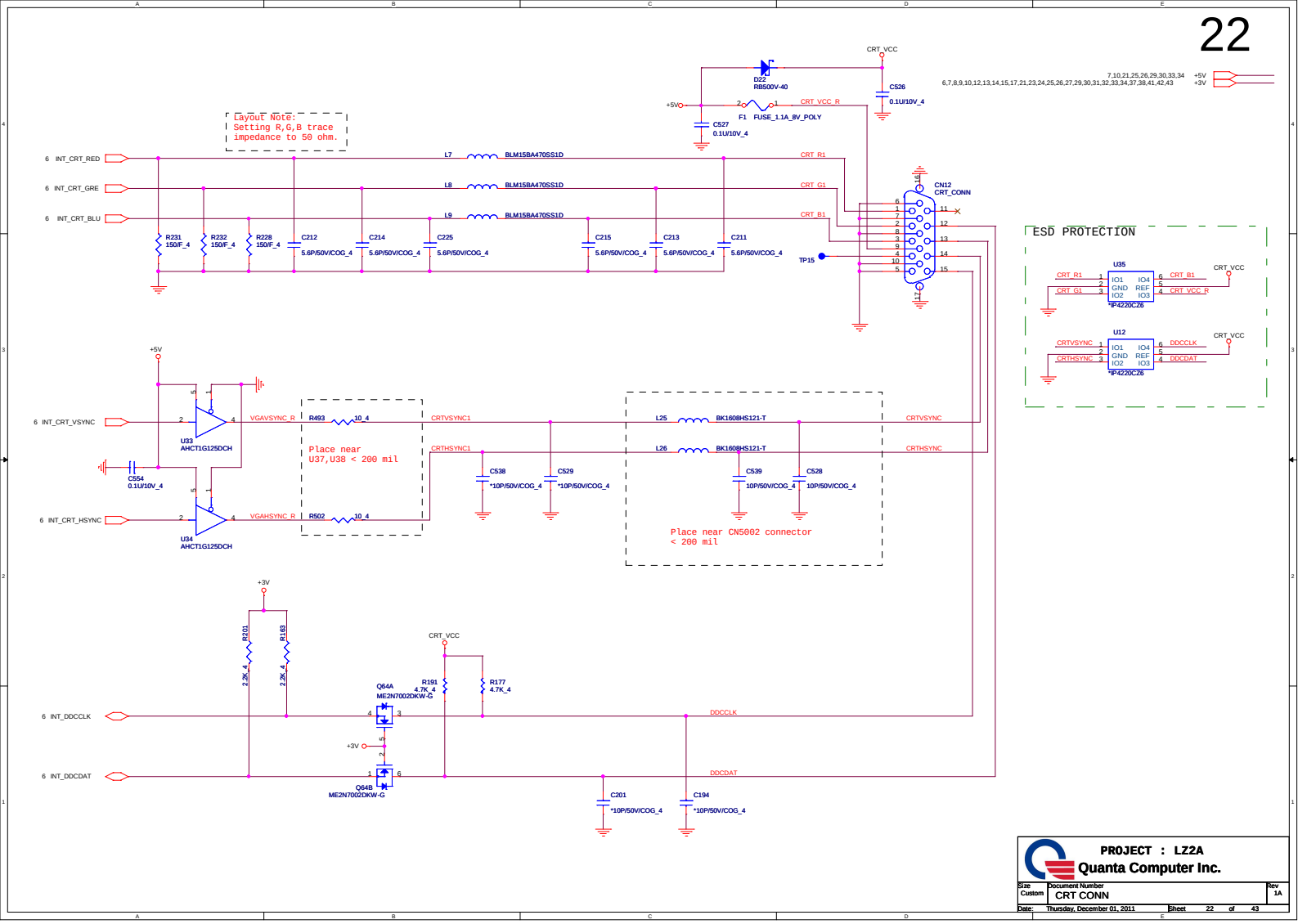

PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: CRT CONN		Rev: 1A
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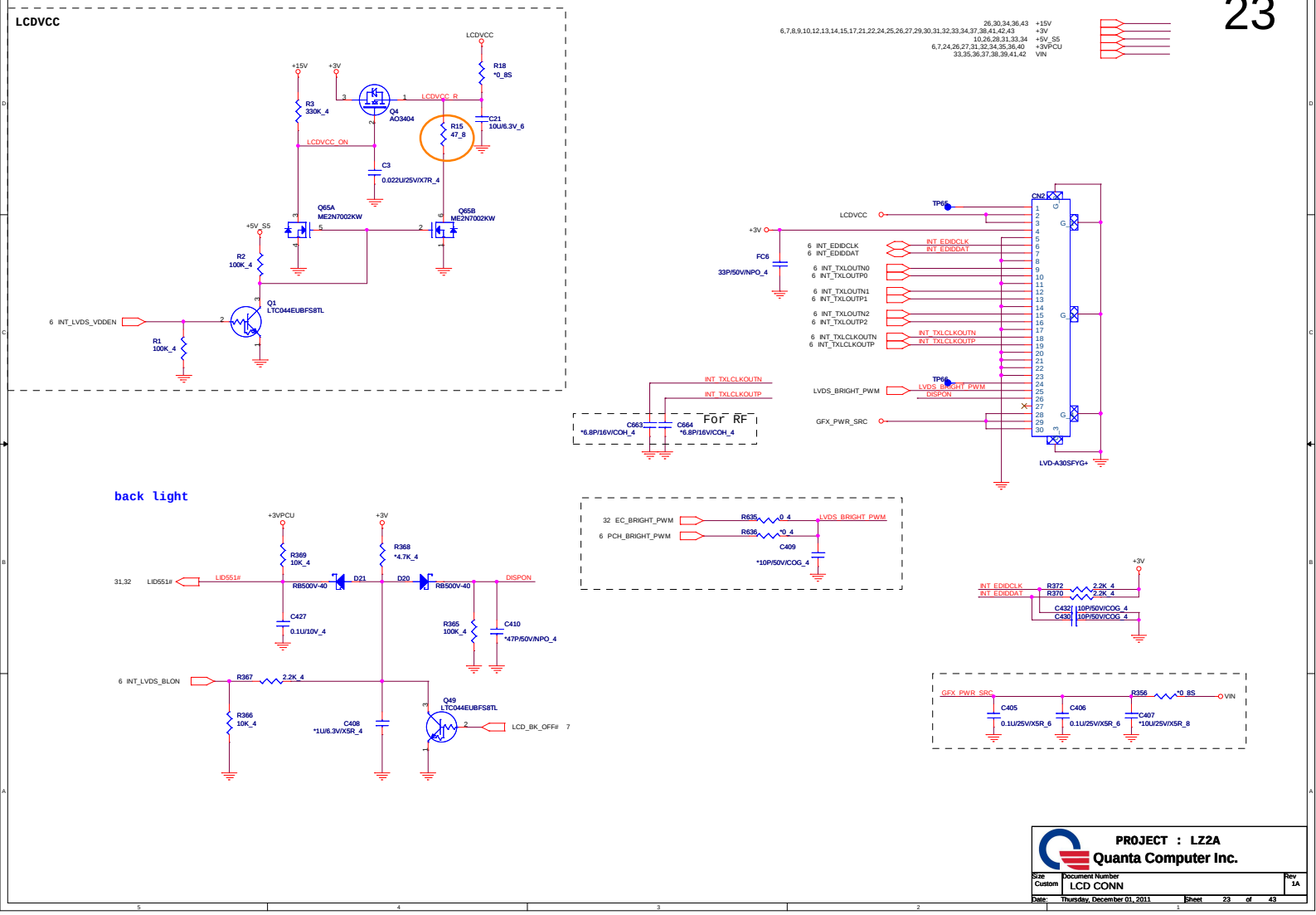

PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: LCD CONN		Rev: 1A
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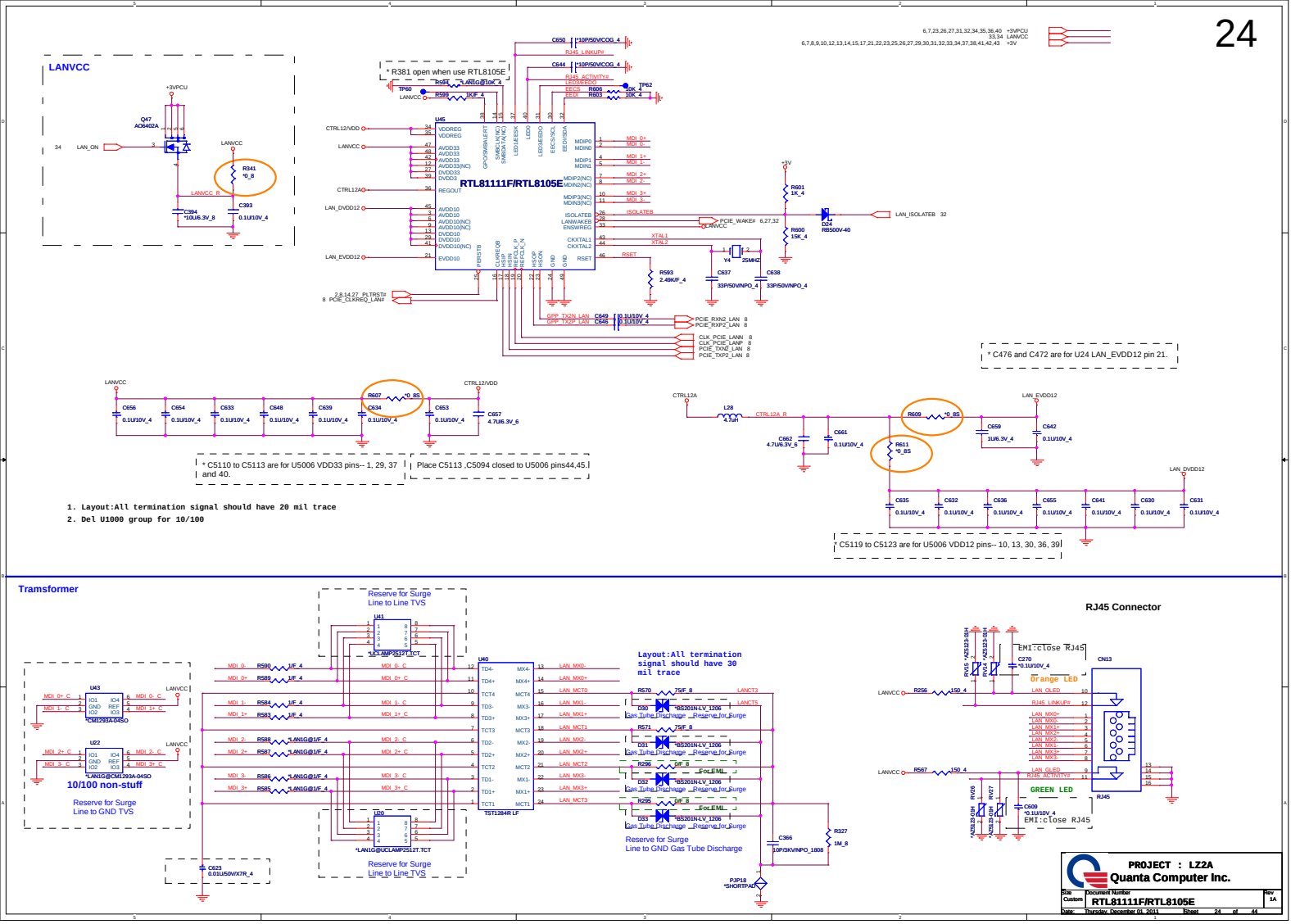

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL81111F/RTL8105E	1A

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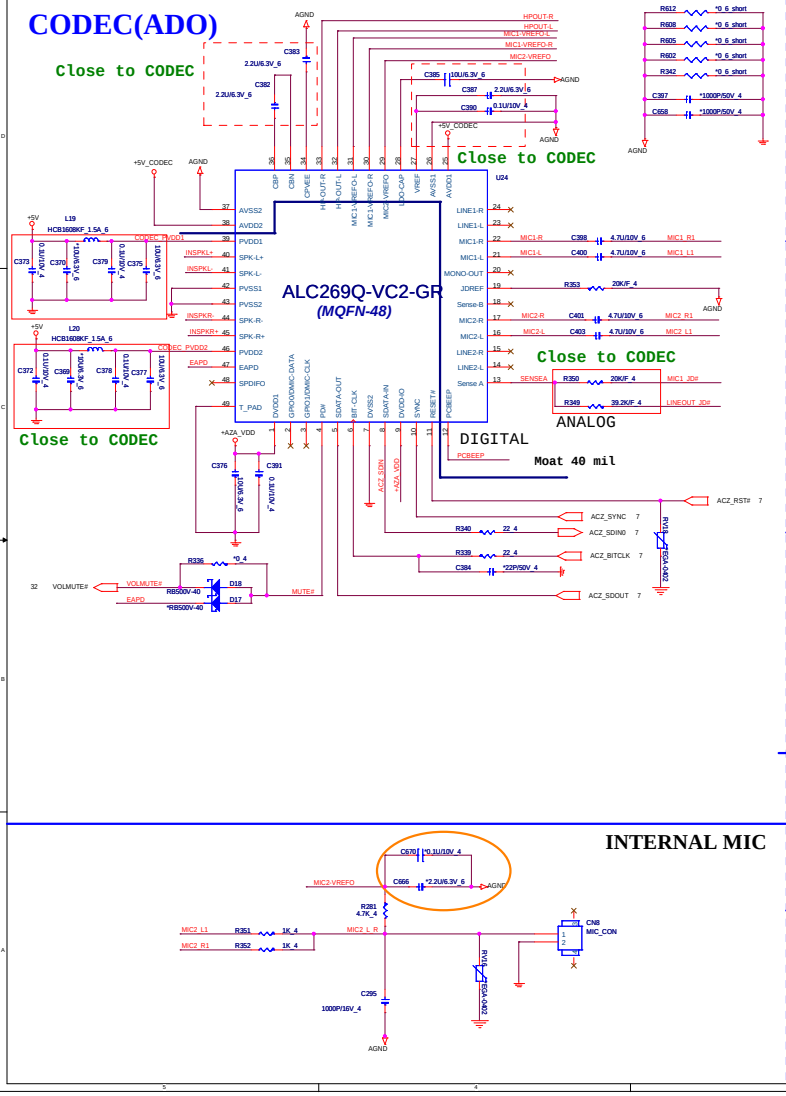
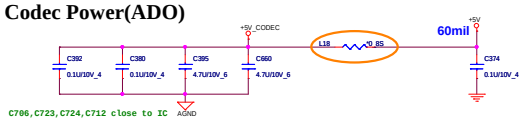
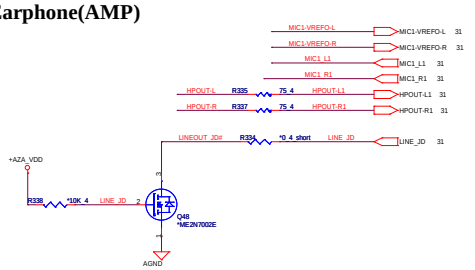
CODEC(ADO)



Codec Power(ADO)

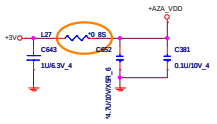


Earphone(AMP)

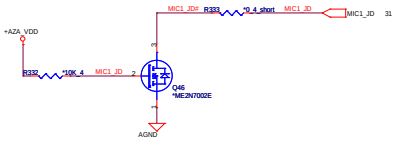


HDA Power(ADO)

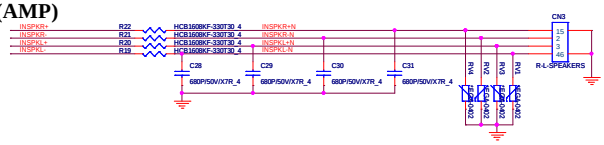
*Intel HDA Either +1.5V_S5 or +3V_S5



System MIC(AMP)

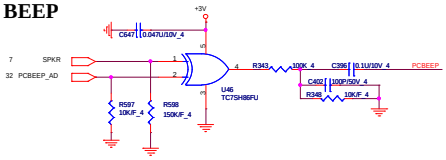


Speaker(AMP)



INTERNAL MIC

PC BEEP



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A
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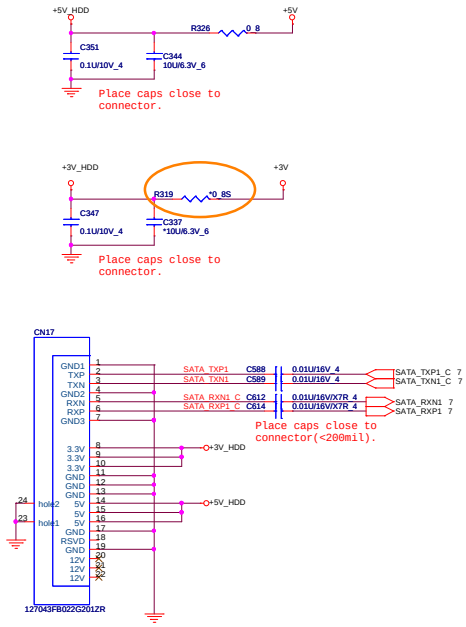
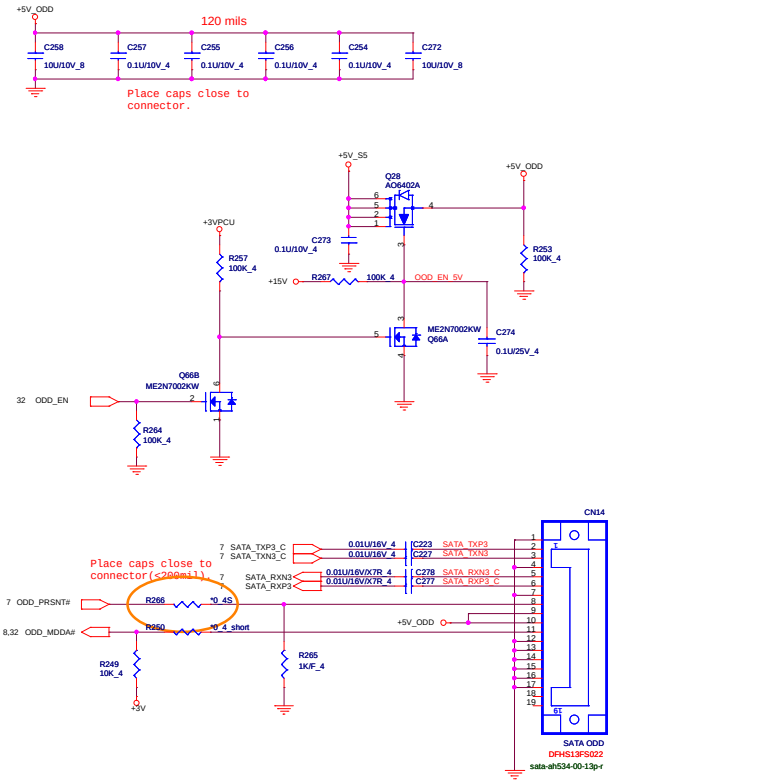
SATA HDD Connector.



SATA ODD Connector.

7,10,21,22,25,29,30,33,34 +5V
6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43 +3V
10,34,35,36,37,38,39,40,41,42,43 +5VPCU
6,7,23,24,27,31,32,34,35,36,40 +3VPCU



PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: SATA HDD/CD-ROM		Rev: 1A
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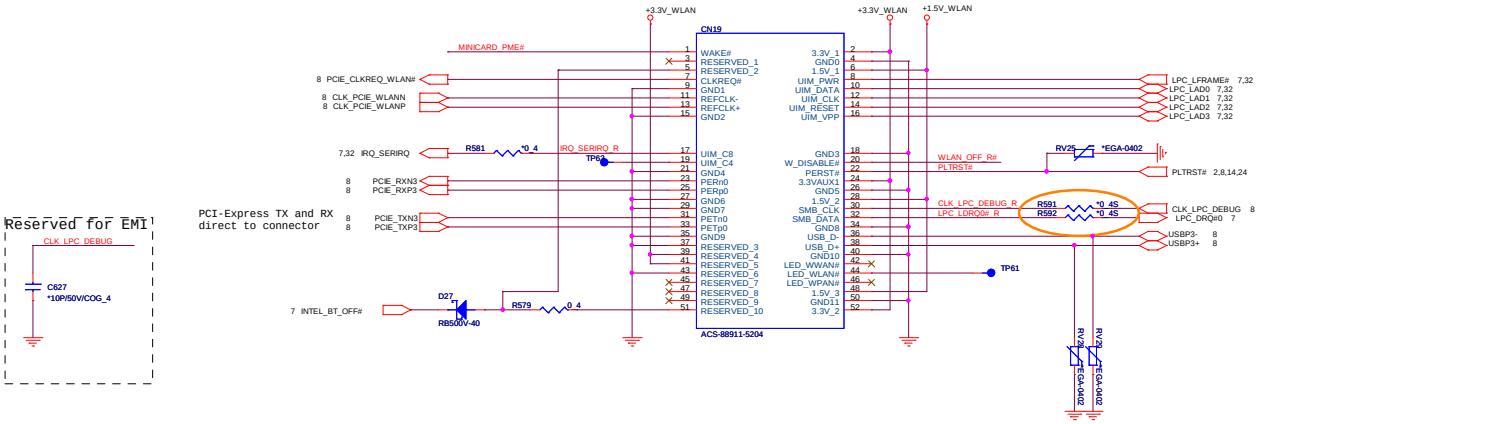
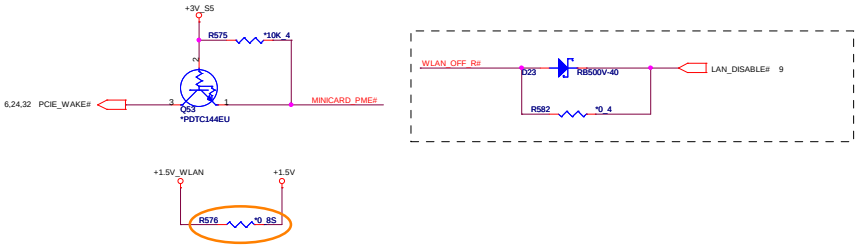
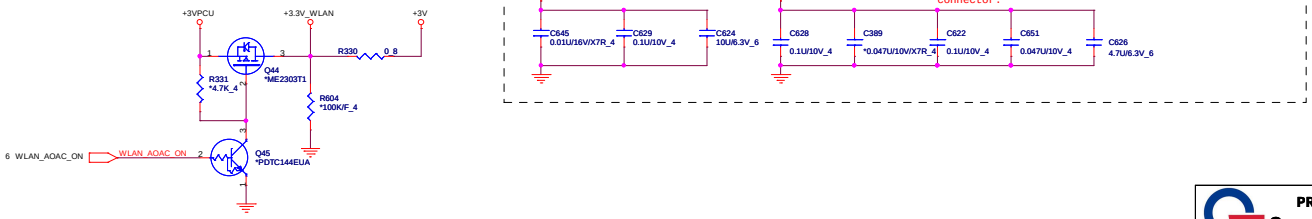
MiniCard WLAN connector

2,6,7,8,9,10,31,34 +3V_S5
4,10 +1.5V
6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,29,30,31,32,33,34,37,38,41,42,43 +3V







PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB2.0*2/WLAN/BT	Rev: 1A
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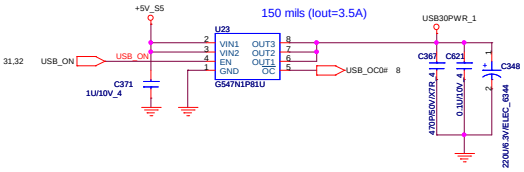
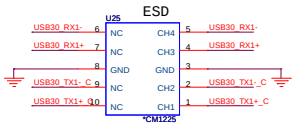
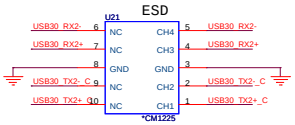
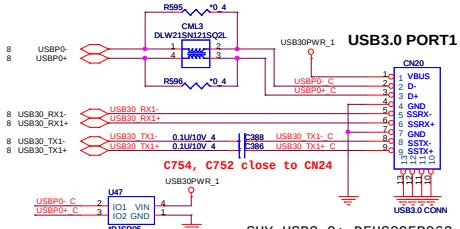
10,23,26,31,33,34 +5V_S5

USB3.0*2



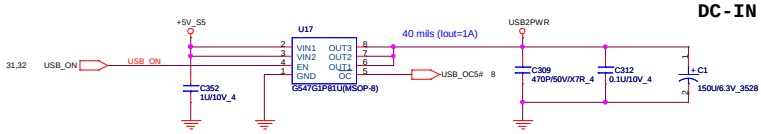




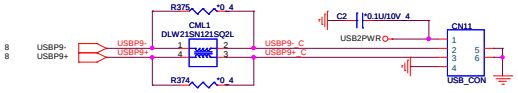


USB2.0*1

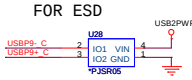
DC-IN Board



DC-IN/USB CONN



FOR ESD



PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 *1	Rev: 1A
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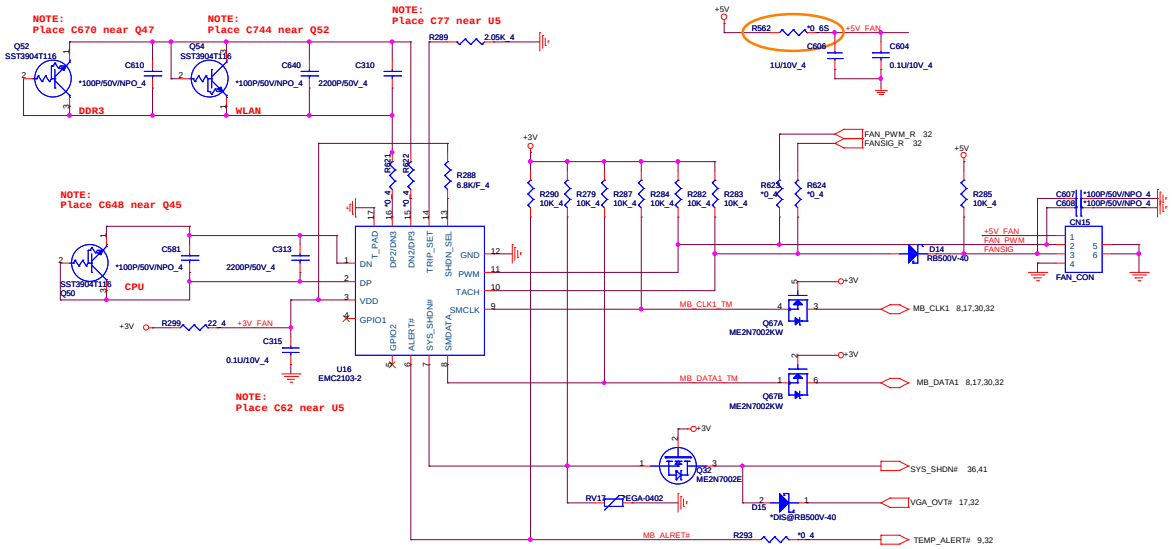
FAN CONTROL



PROJECT : LZ2A Quanta Computer Inc.		
Size: Custom	Document Number: FAN /THERMAL	Rev: 1A
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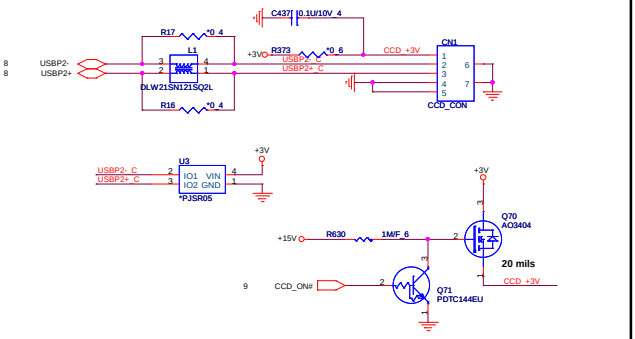
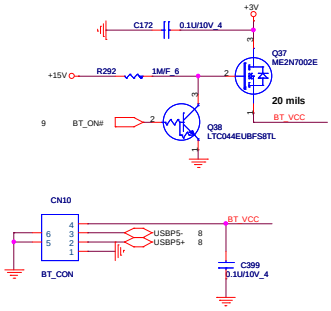
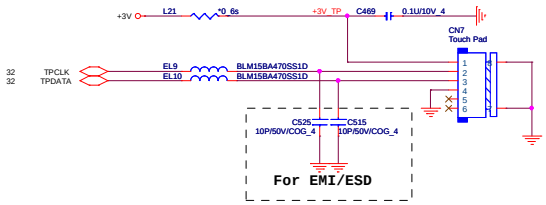
CCD BOARD



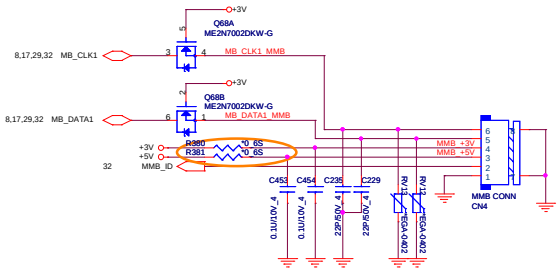
BLUETOOTH



Touch pad



MMB



6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,31,32,33,34,37,38,41,42,43 +3V
7,10,21,22,25,26,29,33,34 +5V
23,26,34,36,43 +15V

PROJECT : LZ2A Quanta Computer Inc.		
Size: Custom	Document Number: CCD/TP/MMB	Rev: 1A
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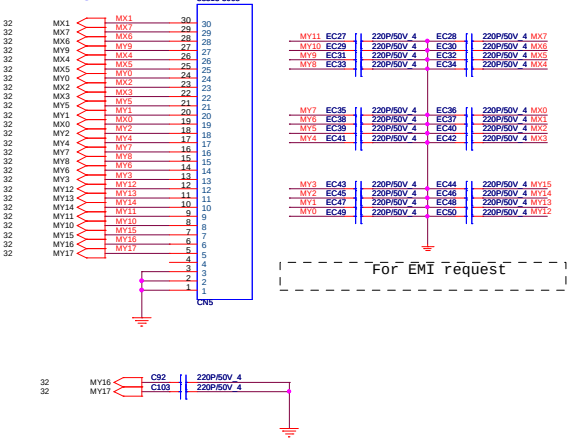
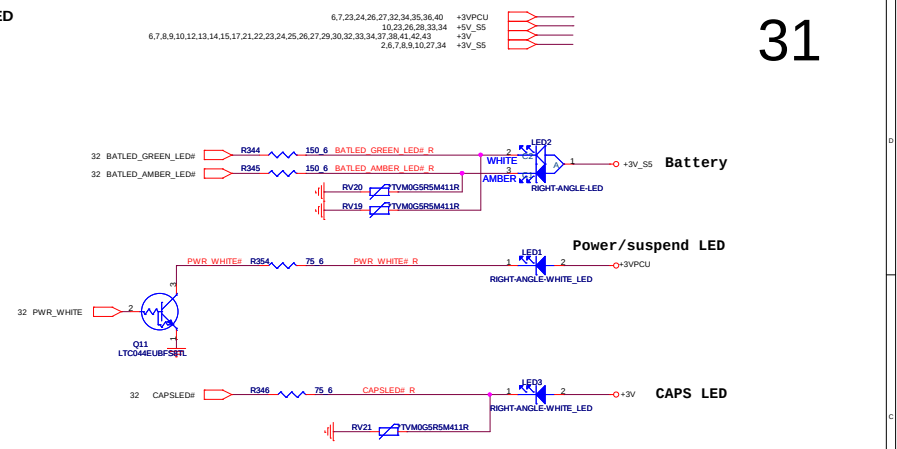
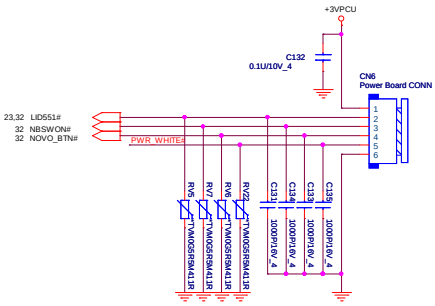
KEYBOARD



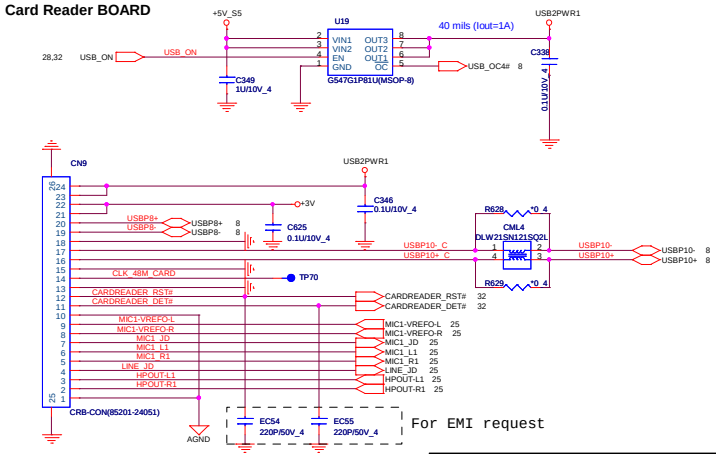
LED



POWER BOARD



Card Reader BOARD



PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: KB/PB/LED/CRB		Rev: 1A
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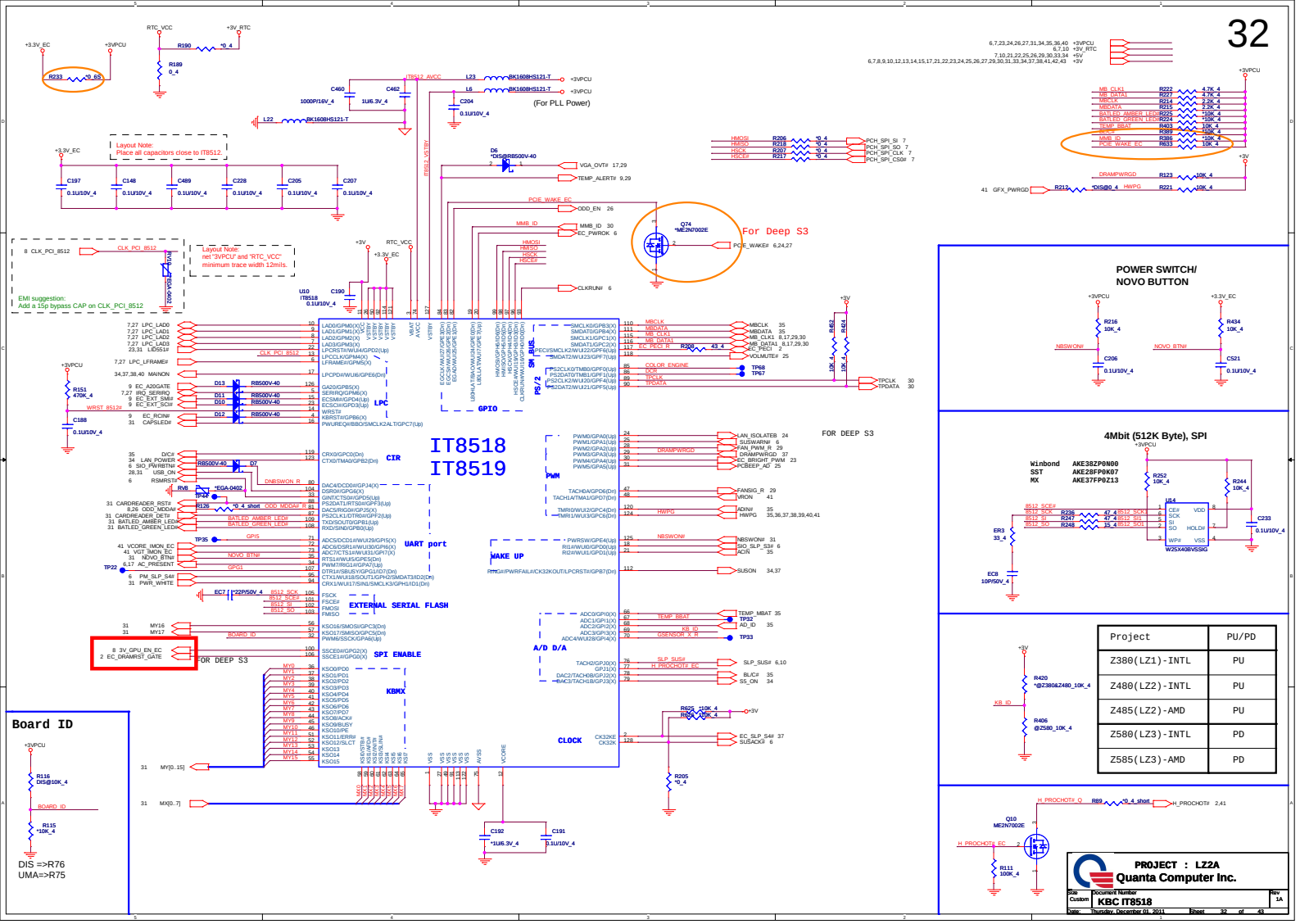

Project	PU/PD
Z380(LZ1)-INTL	PU
Z480(LZ2)-INTL	PU
Z485(LZ2)-AMD	PU
Z580(LZ3)-INTL	PD
Z585(LZ3)-AMD	PD

Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2
SMT NUT H=4/7mm

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE15 *HG-TIC248BC256D106P2
HOLE4 *H-C86D86N
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N

CPU BKT

HOLE7 *C142D102N
HOLE3 *H-TC217BC256D118P2
HOLE5 *H-O316X276ID91P2
HOLE2 *H-O316X276ID91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

33

For ESD

+0.85V SC23 SC24 *0.1U/10V_4
+1.8V
+1.05V_GFX_PCIE SC31 SC32 *0.1U/10V_4
+1.05V_PCH
+0.85V SC11 SC13 SC12 *0.1U/10V_4
+1.5V_CPU SC27 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+1.5V_SUS SC29 SC28 *0.1U/10V_4
+1.5V_CPU
+1.5V_SUS SC40 SC39 0.1U/25V_4
VIN
+3V SC33 SC30 0.1U/10V_4
+5V
+VCC_CORE SC9 SC46 0.1U/25V_4
VIN
+VCC_GFX SC15 SC18 *0.1U/10V_4
+5V SC38 SC25 SC37 0.1U/10V_4
+1.05V_GFX_PCIE SC4 *0.1U/10V_4
GFX_CORE
+VCC_GFX SC17 SC16 SC14 *0.1U/10V_4
+1.05V_PCH SC20 SC19 SC21 *0.1U/10V_4
+1.05V_PCH SC49 SC22 SC50 SC47 SC48 *0.1U/10V_4
+1.05V_GFX_PCIE SC6 SC5 *0.1U/10V_4
+VCC_CORE SC8 SC10 *0.1U/10V_4
+1.5V_GPU SC2 SC43 SC3 *0.1U/10V_4
+1.5V_GPU SC7 SC45 *0.1U/10V_4
+1.5V_GPU SC44 SC1 *0.1U/10V_4
+1.5V_SUS SC35 SC34 SC36 *0.1U/10V_4

For EMI

VIN EC6 EC20 EC12 EC25 EC1 EC18 EC2 EC21 EC5 EC3 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS EC24 3.9p/16V/NP0_4
+1.5V_SUS EC1 3.9p/16V/NP0_4
+1.5V_WLAN EC5 47P/50V/NPO_4
+3.3V_WLAN EC3 47P/50V/NPO_4
+5V EC51 EC52 0.1U/10V_4 *0.1U/10V_4

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A

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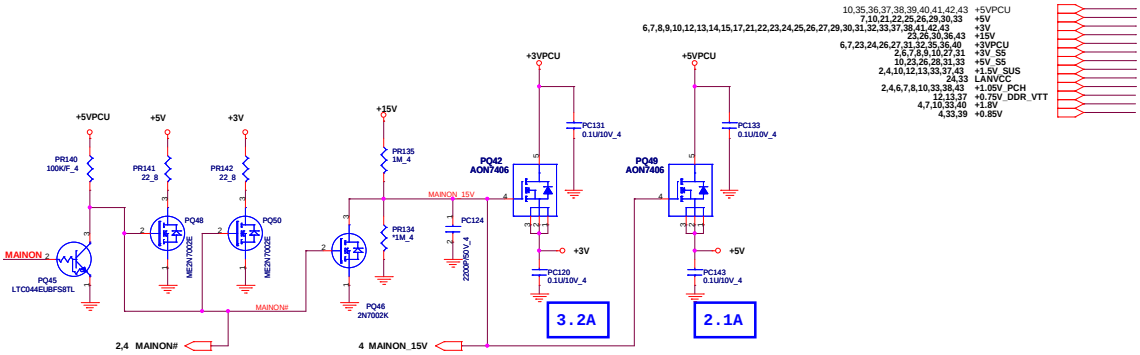
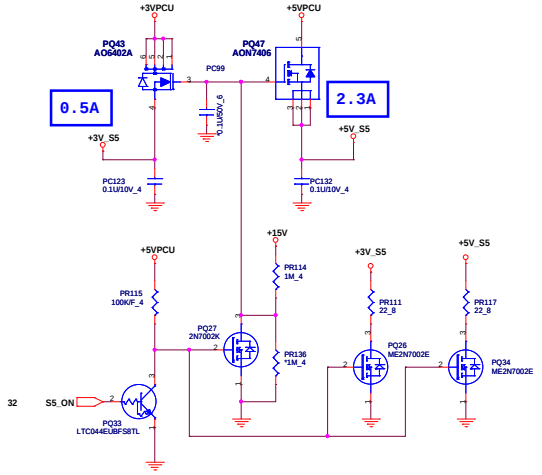
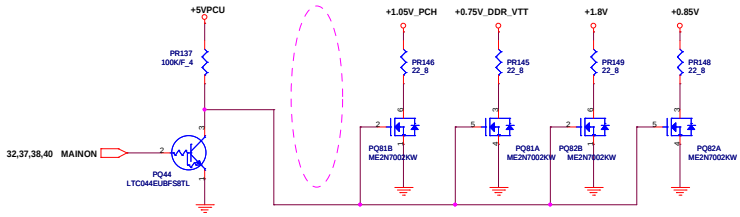
DISCHARGE

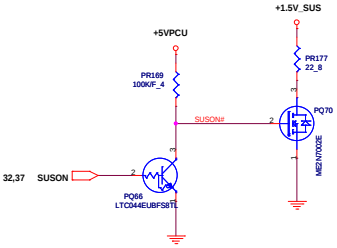
+3V, +5V



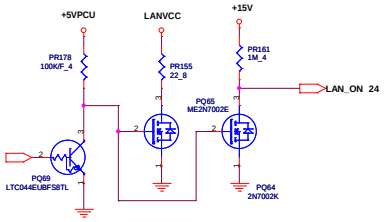
3V_S5, 5V_S5







LANVCC



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	

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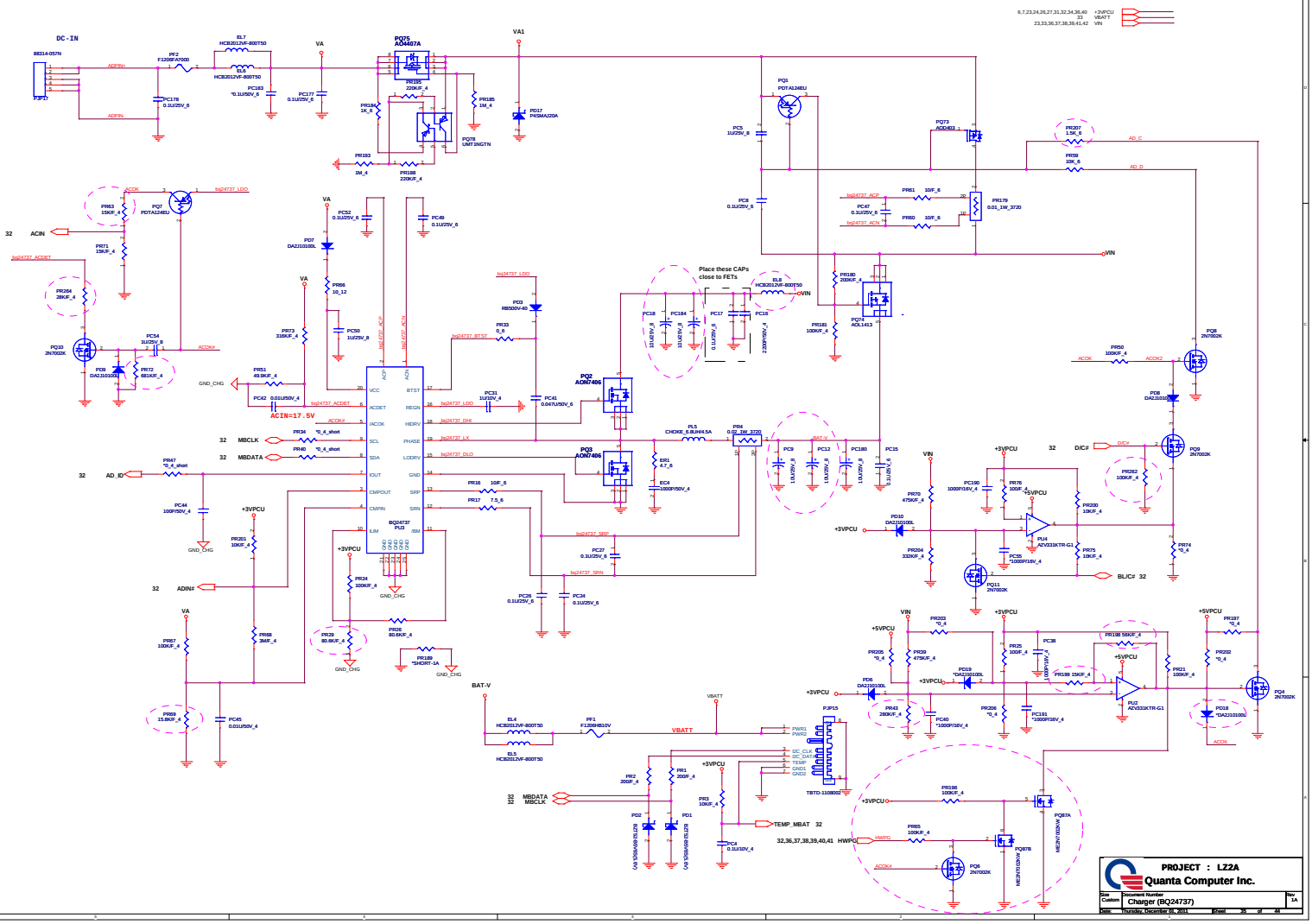
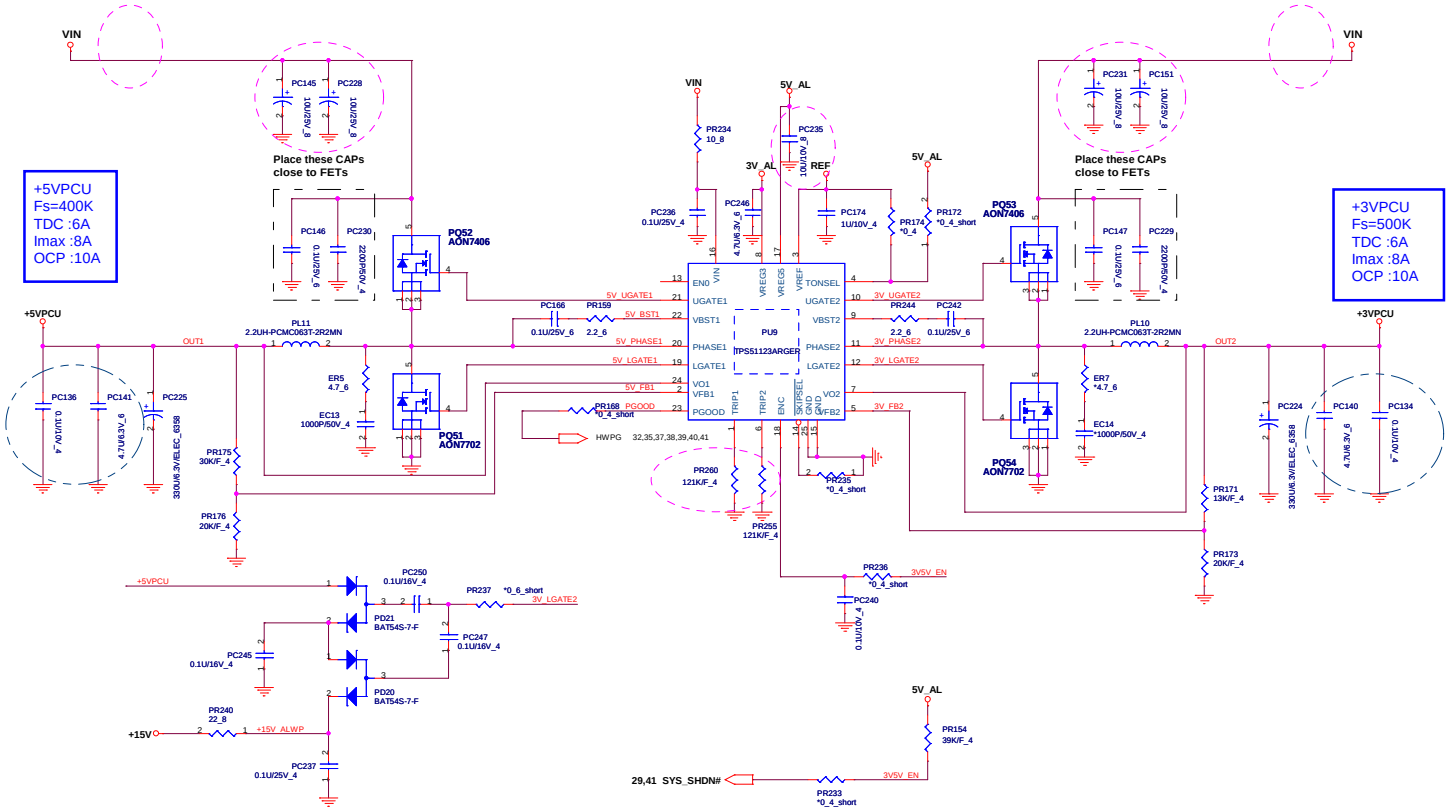

DC-IN
ACIN=17.5V
Place these CAPs close to FETs
PROJECT : LZ2A
Quanta Computer Inc.
Charger (BQ24737)
Thursday, December 08, 2011

23,33,35,37,38,39,41,42 VIN
5V_AL
3V_AL
REF
10,34,35,37,38,39,40,41,42,43 +5VPCU
23,26,30,34,43 +15V
6,7,23,24,26,27,31,32,34,35,40 +3VPCU



PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number	Rev
	3V/5V (TPS51123ARGER)	
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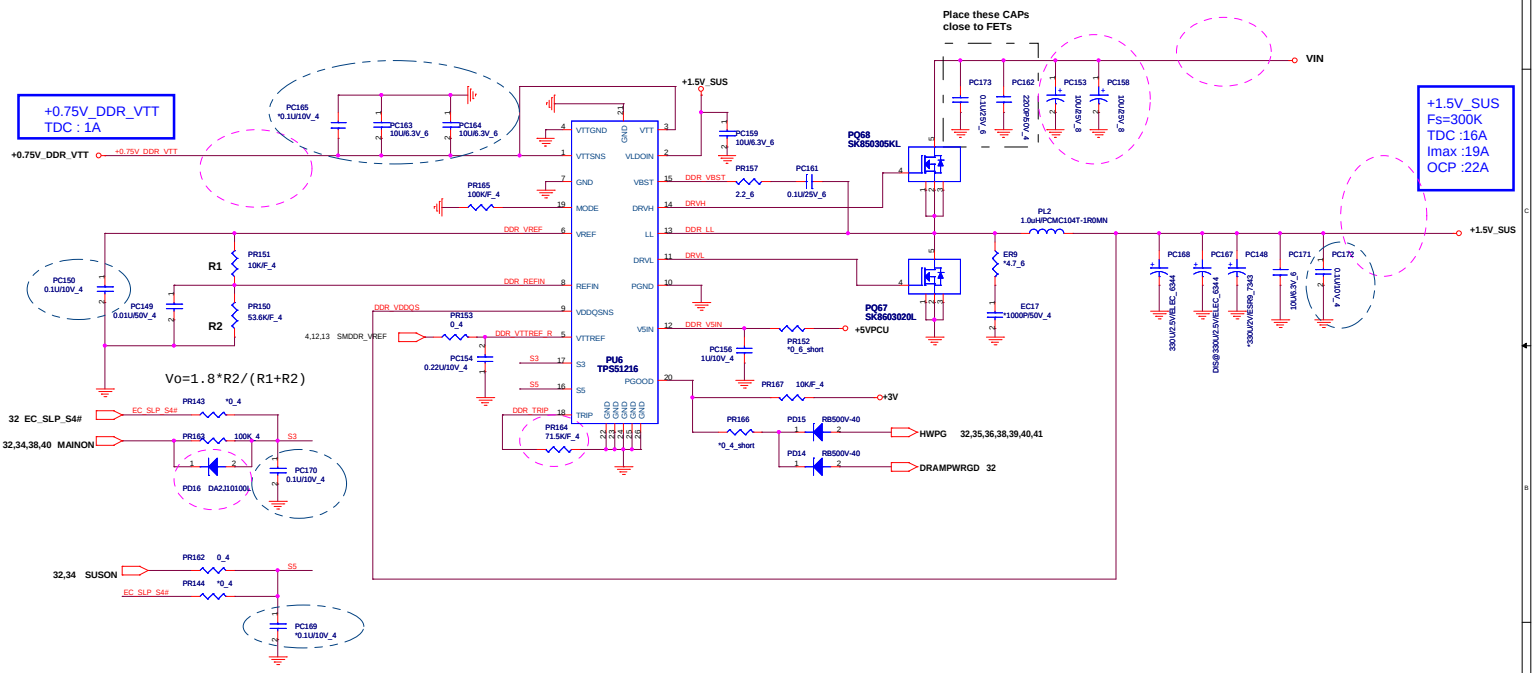
12,13,34 +0.75V_DDR_VTT
23,33,35,36,38,39,41,42 VIN
2,4,10,12,13,33,34,43 +1.5V_SUS



PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number		Rev
	DDR3/0.75V (TPS51216)		
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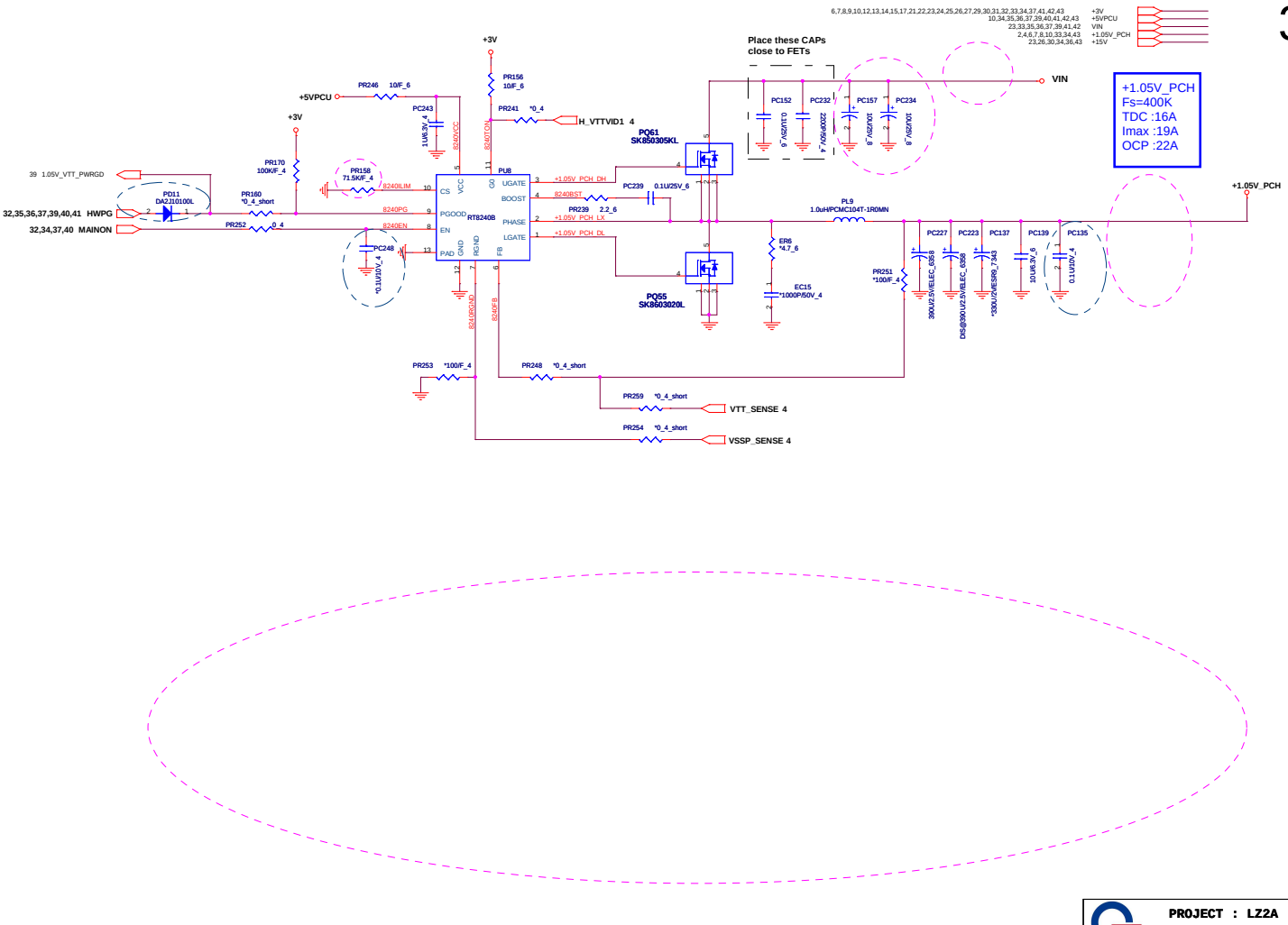

PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: +1.05V_PCH	Rev
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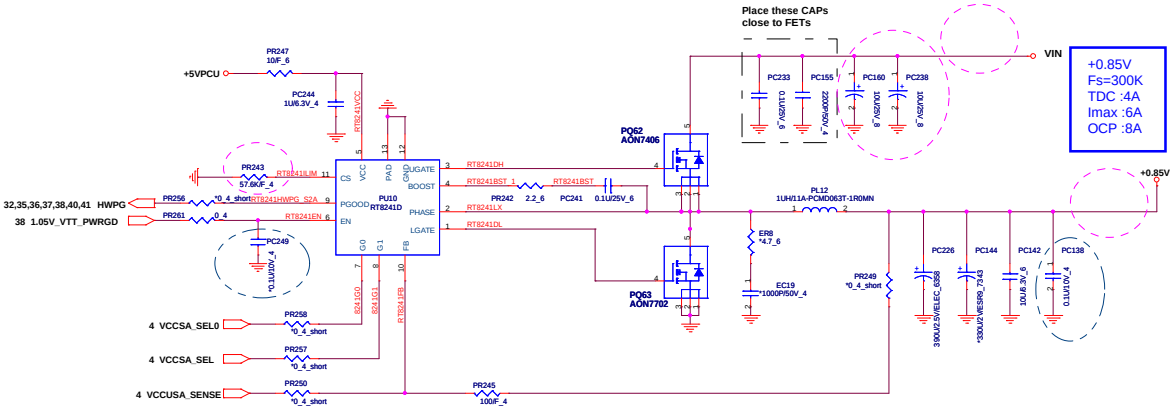
10,34,35,36,37,38,40,41,42,43 +5VPCU
23,33,35,36,37,38,41,42 VIN
4,33,34 +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	VCCSA (RT8241A)	
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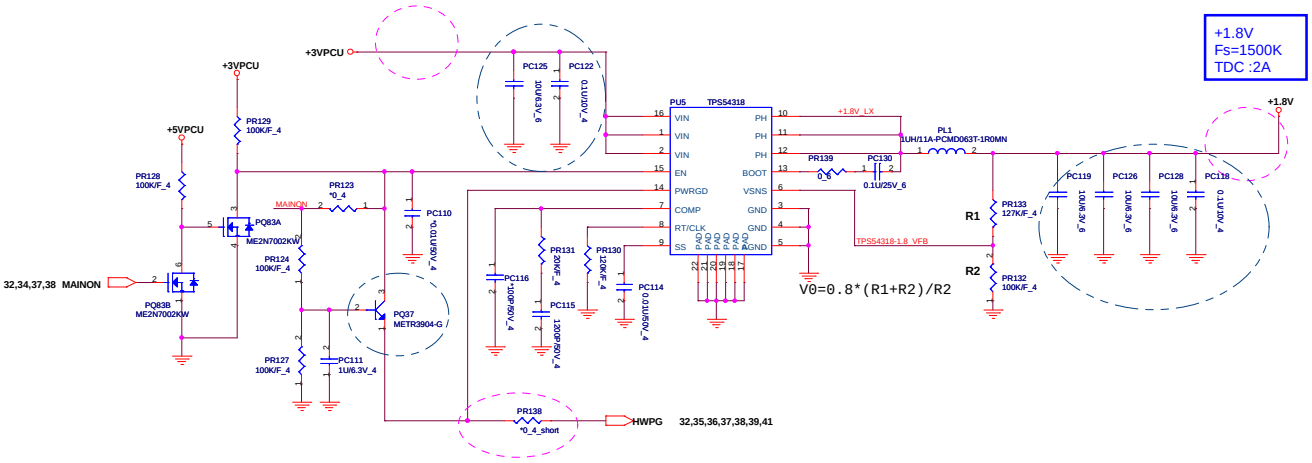
10,34,35,36,37,38,39,41,42,43 +5VPCU
6,7,23,24,26,27,31,32,34,35,36 +3VPCU
4,7,10,33,34 +1.8V



PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: 1.8V (TPS54318)	Rev
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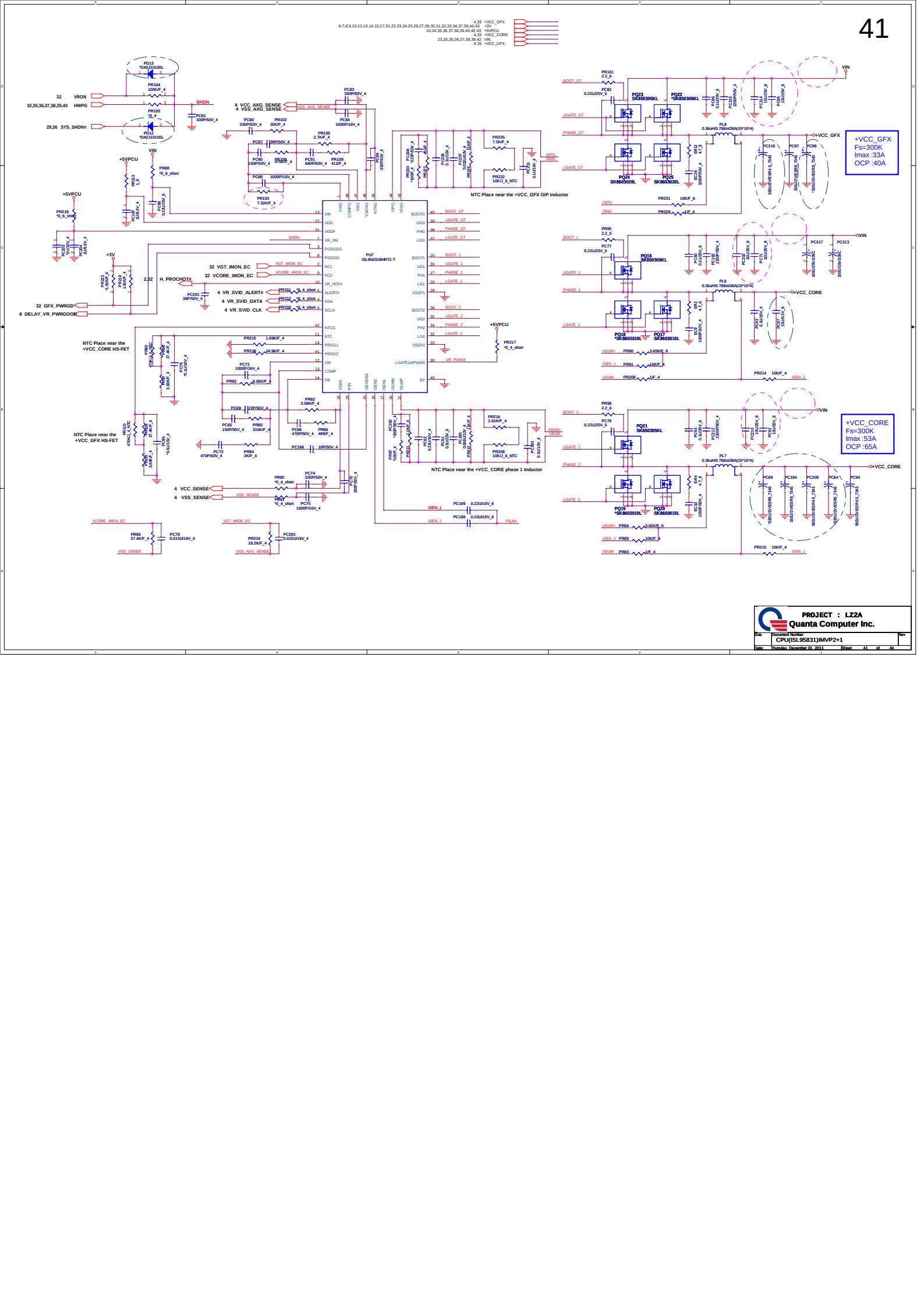
4,33 +VCC_GFX
6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,42,43 +3V
10,34,35,36,37,38,39,40,42,43 +5VPCU
4,33 +VCC_CORE
23,33,35,36,37,38,39,42 VIN
4,33 +VCC_GFX
PD13 *DA2J10100L
PR104 100K/F_4
32 VRON
32,35,36,37,38,39,40 HWPG
PR100 *0_4
29,36 SYS_SHDN#
PD12 *DA2J10100L
SHDN
PC81 100P/50V_4
VIN
+5VPCU
PR88 *0_6_short
PR213 1_6
PC218 4.7U/25V_8
PC88 0.22U/25V_6
PR218 *0_6_short
PC232 0.1U/10V_4
PC233 0.1U/10V_4
PC234 10U/6.3V_6
+3V
PR223 2.49K/F_4
PR219 1.82K/F_4
2,32 H_PROCHOT#
32 GFX_PWRGD
6 DELAY_VR_PWRGOOD
PC201 39P/50V_4
32 VGT_IMON_EC
32 VCORE_IMON_EC
4 VR_SVID_ALERT#
4 VR_SVID_DATA
4 VR_SVID_CLK
PR224 *0_4_short
PR222 *0_4_short
PR220 *0_4_short
4 VCC_AXG_SENSE
4 VSS_AXG_SENSE
VSS_AXG_SENSE
PC83 330P/50V_4
PC84 1000P/16V_4
PC80 330P/50V_4
PR102 20K/F_4
PR105 2.7K/F_4
PC87 *39P/50V_4
PC90 150P/50V_4
PR108 475K/F_4
PC91 680P/50V_4
PR109 412K/F_4
PC86 1000P/16V_4
PR103 7.32K/F_4
PC85 330P/50V_4
PC208 *220P/50V_4
PR230 *100F_4
PR233 *0_4_short
PC209 0.22U/25V_6
PC220 0.1U/10V_4
PR203 10K/F_4
PR225 7.5K/F_4
PR232 10KJ_6_NTC
PC219 0.1U/10V_4
ISPG
ISNG
NTC Place near the +VCC_GFX O/P Inductor
PU7 ISL95831BHRTZ-T
VIN
VDD
VDDP
VR_ON
PGOODG
PGOOD
NC1
NC2
VR_HOT#
ALERT#
SDA
SCLK
NTCG
NTC
PROG1
PROG2
VW
COMP
FB
VSEN
RTN
VCC
COMPG
IRG
VSENG
RTNG
ISPG
ISNG
BOOTG
UGG
PHG
LGG
BOOT1
UG1
PH1
LG1
VSSP1
BOOT2
UG2
PH2
LG2
VSSP2
LGATE1b/PWM3
EP
BOOT_GT
UGATE_GT
PHASE_GT
LGATE_GT
BOOT_1
UGATE_1
PHASE_1
LGATE_1
BOOT_2
UGATE_2
PHASE_2
LGATE_2
VR_PWM3
+5VPCU
PR217 *0_4_short
NTC Place near the +VCC_CORE HS-FET
PR89 470K/J_4
PC76 27.4K/F_4
PC70 3.83K/F_4
PR215 1.69K/F_4
PR223 24.9K/F_4
PC72 1000P/16V_4
PR93 8.06K/F_4
PR92 3.09K/F_4
PC69 *22P/50V_4
PC65 150P/50V_4
PR85 316K/F_4
PC66 470P/50V_4
PR86 499/F_4
PC196 10P/50V_4
PC73 470P/50V_4
PR94 2K/F_4
NTC Place near the +VCC_GFX HS-FET
PR105 470K/J_4
PC75 27.4K/F_4
PC68 *0.1U/10V_4
PR87 3.83K/F_4
PR82 *0_4_short
PC74 330P/50V_4
PR91 *0_4_short
PC75 1000P/16V_4
PC67 330P/50V_4
4 VCC_SENSE
4 VSS_SENSE
VSS_SENSE
VCORE_IMON_EC
PR99 27.4K/F_4
PC78 0.01U/16V_4
VSS_SENSE
VGT_IMON_EC
PR224 18.2K/F_4
PC205 0.022U/16V_4
VSS_AXG_SENSE
PC210 *330P/50V_4
PC211 0.22U/25V_6
PR216 2.61K/F_4
PR207 *10K/F_4
PC206 0.22U/25V_6
PC195 0.01U/16V_4
PR210 *10K/F_4
PR208 10KJ_6_NTC
PC203 0.1U/10V_4
VSUM+
VSUM-
NTC Place near the +VCC_CORE phase 1 Inductor
ISEN_1
ISEN_2
PC199 0.22U/10V_6
PC198 0.22U/10V_6
PR101 2.2_6
PC82 0.22U/25V_6
PQ23 SK850305KL
PQ22 *SK850305KL
PC205 0.01U/25V_6
PC204 4.7U/25V_8
PC213 220P/50V_4
PC214 4.7U/25V_8
PC207 10U/25V_8
PL8 0.36uH/0.798m/28A(10*10*4)
+VCC_GFX
PC216
PC97
PC98
PQ24 SK8603020L
PQ25 SK8603020L
ER12 4.7_6
EC25 100P/50V_4
PR231 10K/F_6
PR229 1/F_4
+VCC_GFX Fs=300K Imax :33A OCP :40A
PR95 2.2_6
PC77 0.22U/25V_6
PQ16 SK850305KL
PC120 4.7U/25V_8
PC118 220P/50V_4
PC230 10U/25V_8
PC71 4.7U/25V_8
PC217
PC213
PL6 0.36uH/0.798m/28A(10*10*4)
+VCC_CORE
ER2 4.7_6
EC9 100P/50V_4
PC63 0.3U/25V_4
PC57 100K/6.3V_6
PQ18 *SK8603010L
PQ17 SK8603010L
VSUM+ PR90 3.65K/F_6
ISEN_1 PR91 10K/F_4
VSUM- PR209 1/F_4
PR214 10K/F_4
ISEN_2
PR98 2.2_6
PC79 0.22U/25V_6
PQ21 SK850305KL
PC123 4.7U/25V_8
PC212 220P/50V_4
PC210 10U/25V_8
PC62 10U/25V_8
PL7 0.36uH/0.798m/28A(10*10*4)
+VCC_CORE
ER4 4.7_6
EC10 100P/50V_4
PC89
PC194
PC209
PC64
PC94
PQ19 *SK8603010L
PQ20 SK8603010L
VSUM+ PR84 3.65K/F_6
ISEN_2 PR89 10K/F_6
VSUM- PR83 1/F_4
PR210 10K/F_4
ISEN_1
+VCC_CORE Fs=300K Imax :53A OCP :65A
PROJECT : LZ2A
Quanta Computer Inc.
Size
Document Number
CPU(ISL95831)IMVP2+1
Rev
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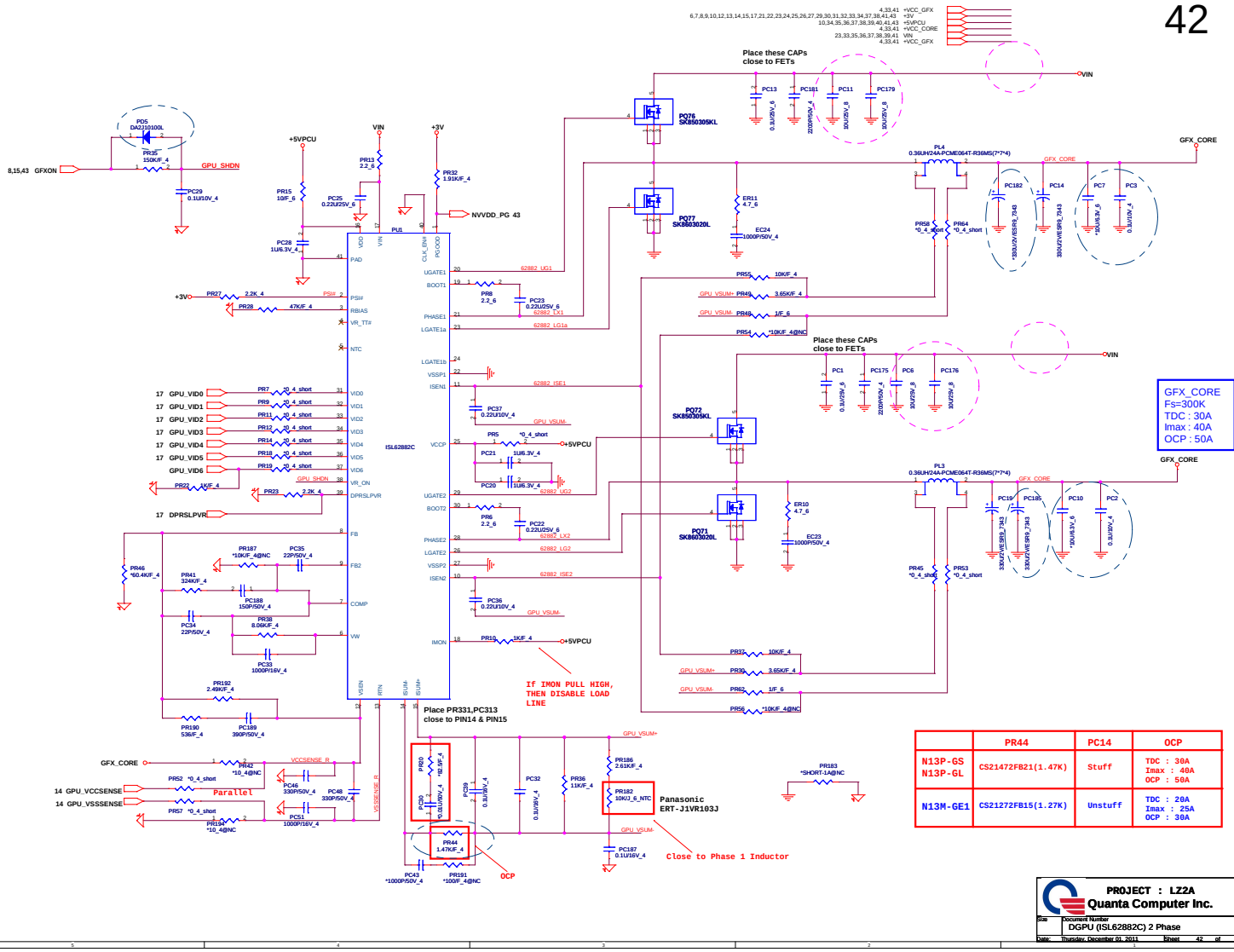
Place these CAPs close to FETS
VIN
GFX_CORE
GFX_CORE Fs=300K TDC : 30A Imax : 40A OCP : 50A
ISL62882C
IF IMON PULL HIGH, THEN DISABLE LOAD LINE
Place PR331,PC313 close to PIN14 & PIN15
Parallel
Panasonic ERT-J1VR103J
Close to Phase 1 Inductor
OCP
PR44 | PC14 | OCP
N13P-GS N13P-GL | CS21472FB21(1.47K) | Stuff | TDC : 30A Imax : 40A OCP : 50A
N13M-GE1 | CS21272FB15(1.27K) | Unstuff | TDC : 20A Imax : 25A OCP : 30A
PROJECT : LZ2A
Quanta Computer Inc.
DGPU (ISL62882C) 2 Phase
Thursday, December 01, 2011
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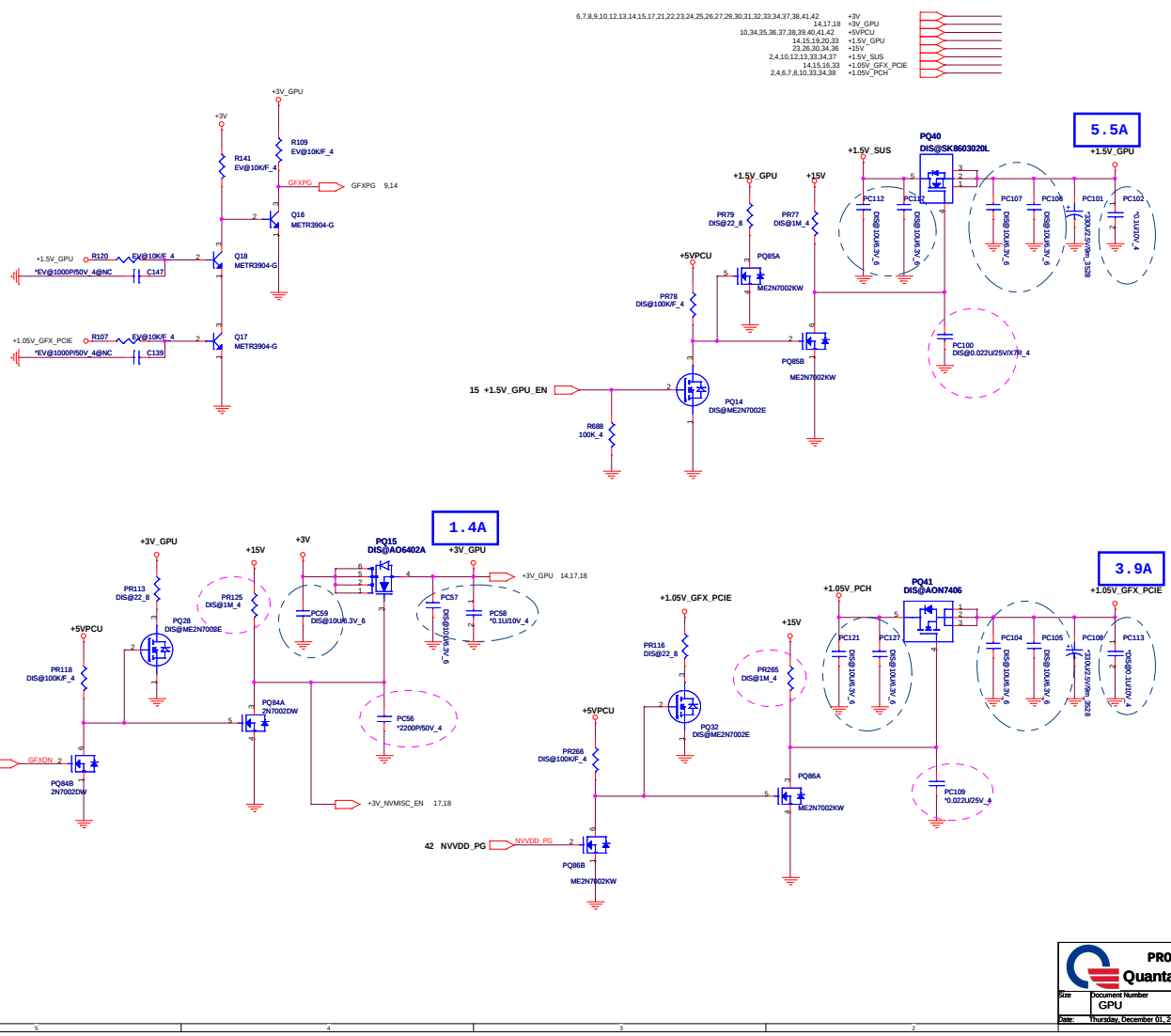

PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: GPU	Rev
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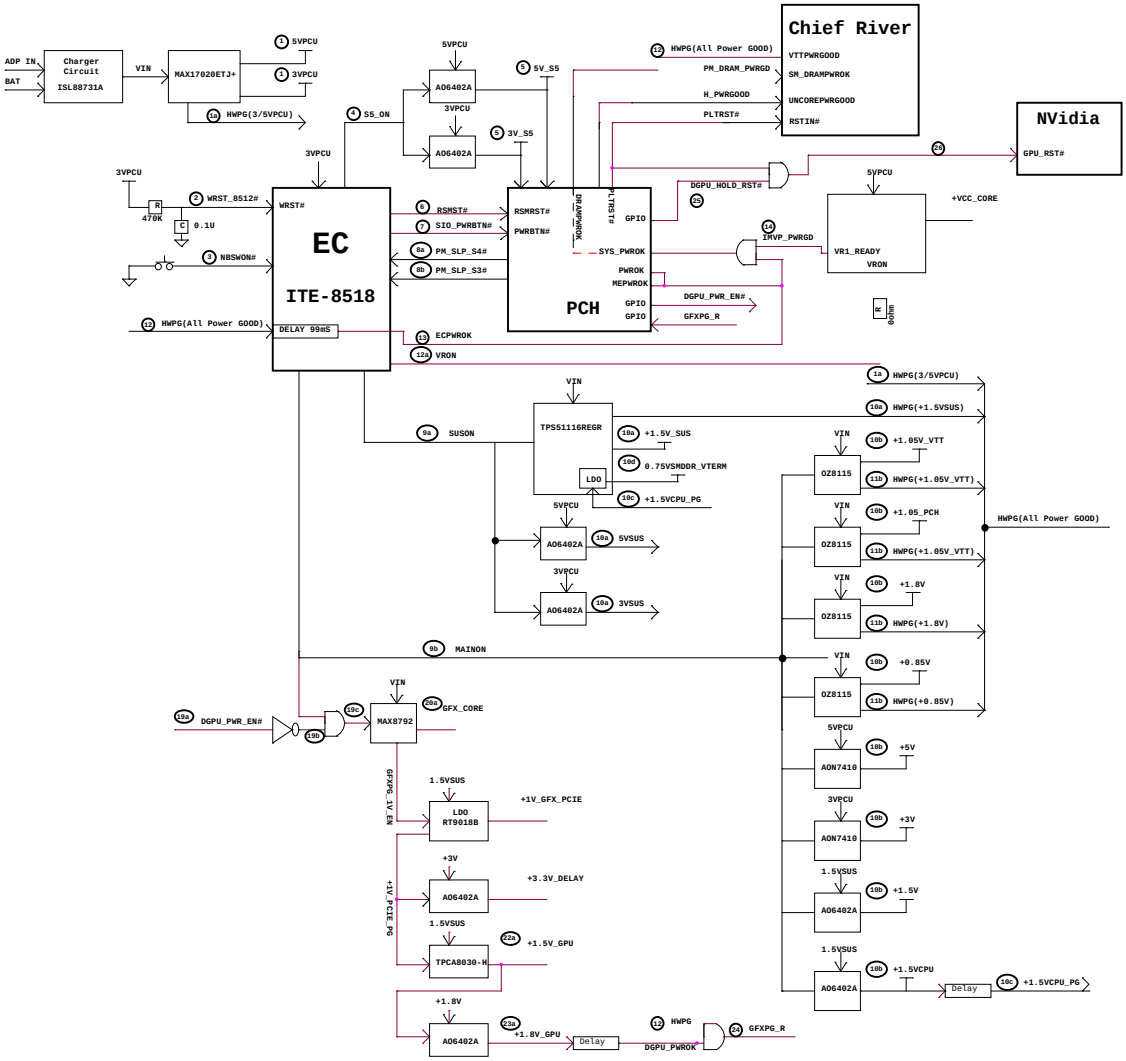
Chief River
VTTPWRGOOD
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
PM_DRAM_PWRGD
H_PWRGOOD
PLTRST#
HWPG(All Power GOOD)
NVidia
GPU_RST#
Charger Circuit
ISL88731A
ADP_IN
BAT
VIN
MAX17020ETJ+
5VPCU
3VPCU
HWPG(3/5VPCU)
S5_ON
AO6402A
5V_S5
3V_S5
EC
ITE-8518
WRST#
WRST_8512#
NBSWON#
RSMRST#
SIO_PWRBTN#
PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
DELAY 99mS
ECPWROK
VRON
PCH
SUSWARN#
GPIO
SYS_PWROK
PWROK
MEPWROK
DGPU_PWR_EN#
GFXPG_R
DGPU_HOLD_RST#
INVP_PWRGD
VR1_READY
+VCC_CORE
TPS51116REGR
LDO
SUSON
+1.5V_SUS
0.75VSMDDR_VTERM
+1.5VCPU_PG
5VSUS
3VSUS
MAINON
OZ8115
+1.05V_VTT
+1.05_PCH
+1.8V
+0.85V
HWPG(+1.05V_VTT)
HWPG(+1.8V)
HWPG(+0.85V)
HWPG(All Power GOOD)
AON7410
+5V
+3V
MAX8792
DGPU_PWR_EN#
GFX_CORE
+1V_GFX_PCIE
+3.3V_DELAY
+1.5V_GPU
+1.8V_GPU
TPCA8030-H
LDO RT9018B
Delay
DGPU_PWROK
GFXPG_R
+1.5VCPU
PROJECT LZ1
Quanta Computer Inc.
Power Sequence Diagram