

Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Cover Page

Size

Document Number

A3

LZ57

Date

Tuesday, March 29, 2011

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Rev

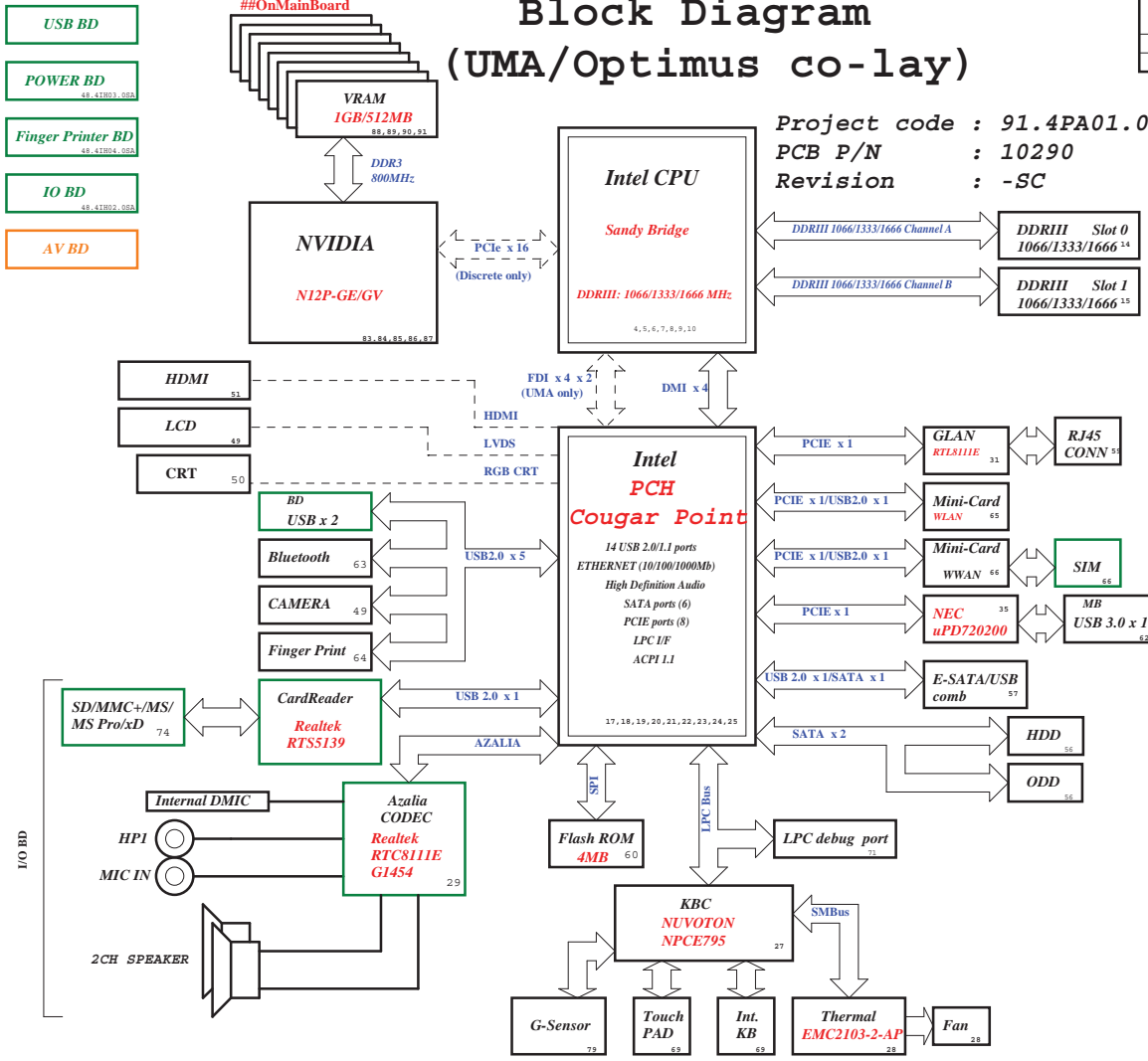
-1

Block Diagram (UMA/Optimus co-lay)

SYSTEM DC/DC RT8208B 48		CPU DC/DC NCP6131 42-44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	0DSV_S0	DCBATOUT	VCC_CORE
SYSTEM DC/DC UP6111CQHC 45		SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1DSV_VST	5V_AUX_S5	3D3V_AUX_S5
		5V_S5	3D3V_S5
SYSTEM DC/DC UP6111C 46		SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1DSV_S3	DCBATOUT	VCC_GFXCORE
	DDR_VREF_S3		
VGA RT8208B 92		TI CHARGER BQ24745 40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	+DC_IN_S5	DCBATOUT
		+PRATT	
LDO RT9025 47		SYSTEM DC/DC G9091-180T11U 24, 93	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1DSV_S0	3D3V_S5	1DSV_S5
		3D3V_S0	1DSV_VGA_S0
LDO RT9026 46		PCB LAYER	
INPUTS	OUTPUTS	L1:Top L5:VCC	
5V_S5	0D75V_S0	L2:GND L6:Signal	
		L3:Signal L7:GND	
		L4:Signal L8:Signal	

Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC

- USB BD
- POWER BD
48, 41803, 05A
- Finger Printer BD
48, 41804, 05A
- IO BD
48, 41802, 05A
- AV BD



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Title: Block Diagram
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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ
INIT3_3V#	Weak internal pull-up resistor. Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury:left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury:left floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for PD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connected to the EMBEDDED Display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETS de assertich 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
SV_S0	5V		
SDV_S0	3.3V		
IDV_S0	1.8V		
SDV_S0	1.5V		
IDV_S0	1.05V		
GDV_S0	0.95 - 0.95V		
GDV_S0	0.75V		
VCC_CORE	0.95V to 1.1V	S0	CPU Core Rail
VCC_SPCORSE	0.4 to 1.25V		Graphics Core Rail
IDV_VGA_S0	1.8V		
SDV_VGA_S0	1.5V		
IV_VGA_S0	1V		
SV_USBV_S3	5V		
IDV_USBV_S3	1.5V	S3	
DCV_USBV_S3	0.75V		
BT	4V-14.1V		AC Brick Mode only
PCBATOUT	5V-14.1V		
SV_S5	5V	All S states	
SV_AUX_S5	5V		
SDV_S5	3.3V		
SDV_AUX_S5	3.3V		
SDV_LAN_S5	3.3V	WOL_EN	Legacy WOL
SDV_AUX_SBC	3.3V	DSW_Sx	ON for supporting Deep Sleep states
SDV_AUX_S5	3.3V	G3_Sx	Powered by Li Coin Cell in G3 and +V3ALM in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	Address	HURON RIVER CBS	Bus
Device			Hex	Bus
EC SMBus 1				
Battery CHARGER			BAT_SCL/BAT_SDA	BAT_SCL/BAT_SDA
			BAT_SCL/BAT_SDA	BAT_SCL/BAT_SDA
EC SMBus 2				
PCH			SM1_CLK/SM1_DATA	SM1_CLK/SM1_DATA
ADP			SM1_CLK/SM1_DATA	SM1_CLK/SM1_DATA
PCH SMBus				
S0-DIMMA (SPD)			PCH_SMBDATA/PCH_SMBCLK	PCH_SMBDATA/PCH_SMBCLK
S0-DIMMB (SPD)			PCH_SMBDATA/PCH_SMBCLK	PCH_SMBDATA/PCH_SMBCLK
Digital POC			PCH_SMBDATA/PCH_SMBCLK	PCH_SMBDATA/PCH_SMBCLK
Q-Sensor			PCH_SMBDATA/PCH_SMBCLK	PCH_SMBDATA/PCH_SMBCLK
MI2C			PCH_SMBDATA/PCH_SMBCLK	PCH_SMBDATA/PCH_SMBCLK

PCIe Routing

LANE1	Mini Card2 (WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1 (WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

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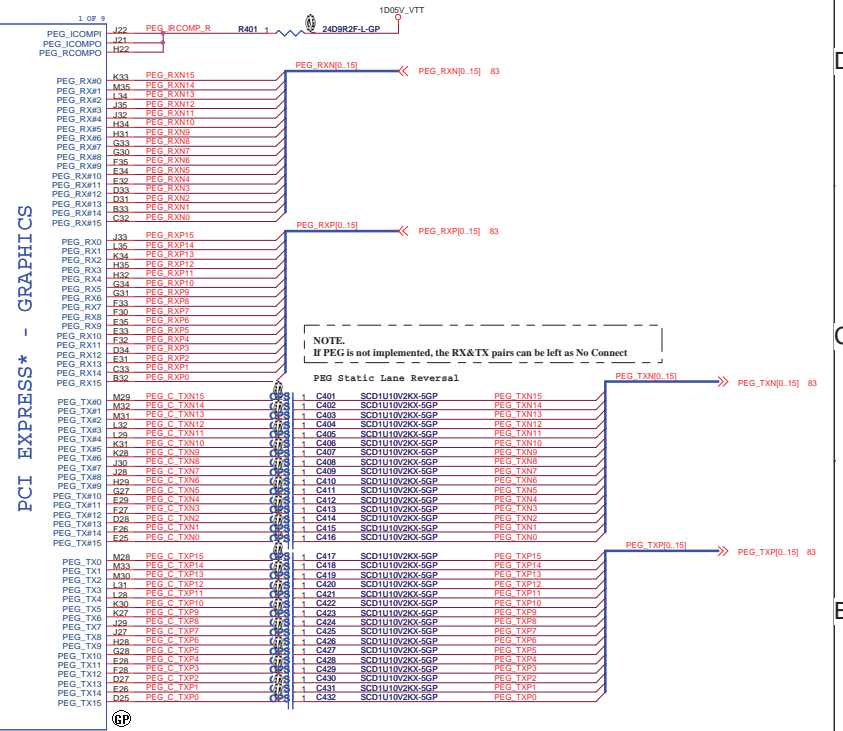
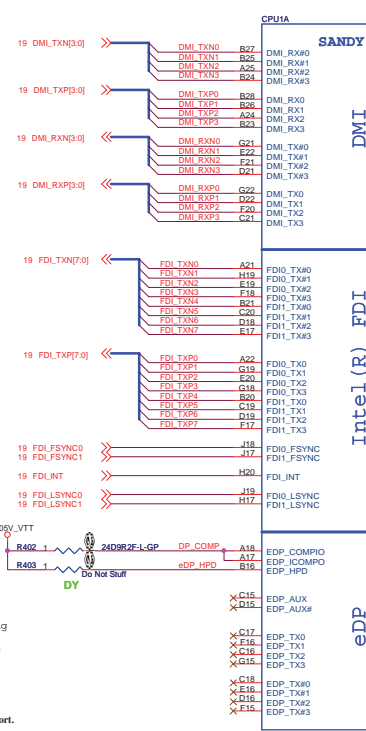
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_ROMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



62.10055.321

delete R404&RN 401 @20100630

BOB

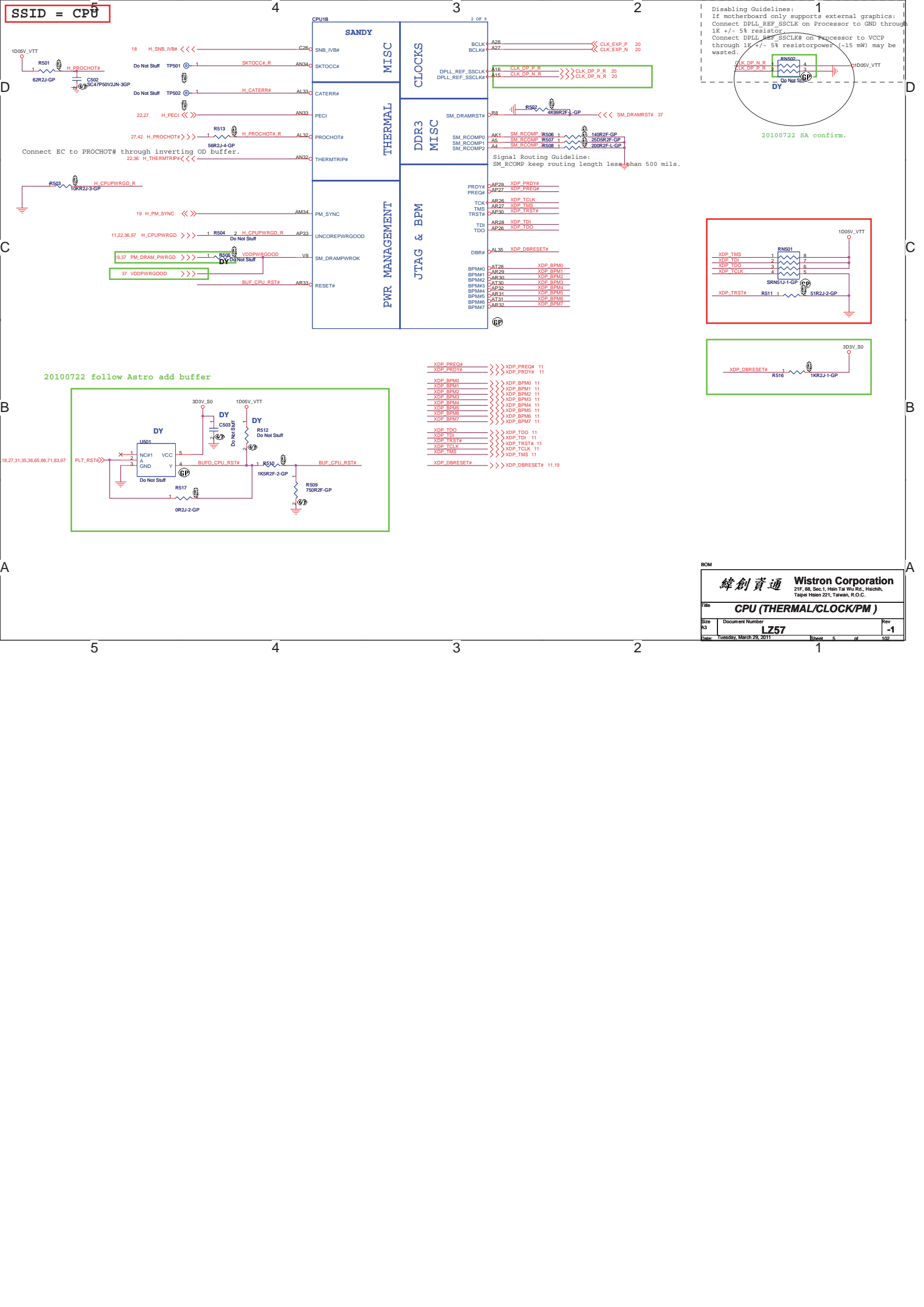
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Size A3 Document Number: **LZ57** Rev: **-1**

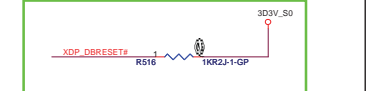
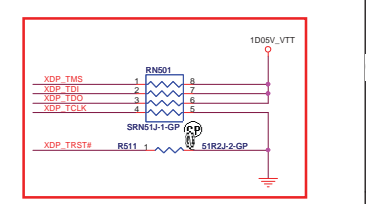
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SSID = CPU



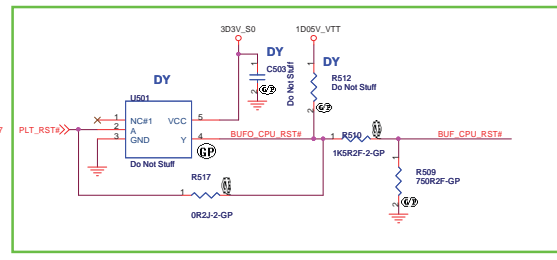
Disabling Guidelines:
 If motherboard only supports external graphics:
 Connect DPLL_REF_SCLK on Processor to GND through 1K +/- 5% resistor.
 Connect DPLL_REF_SCLK# on Processor to VCCP through 1K +/- 5% resistor (15 mW) may be wasted.

20100722 SA confirm.



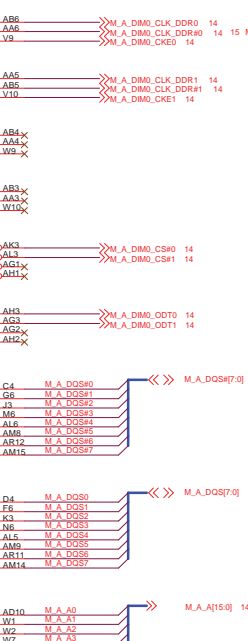
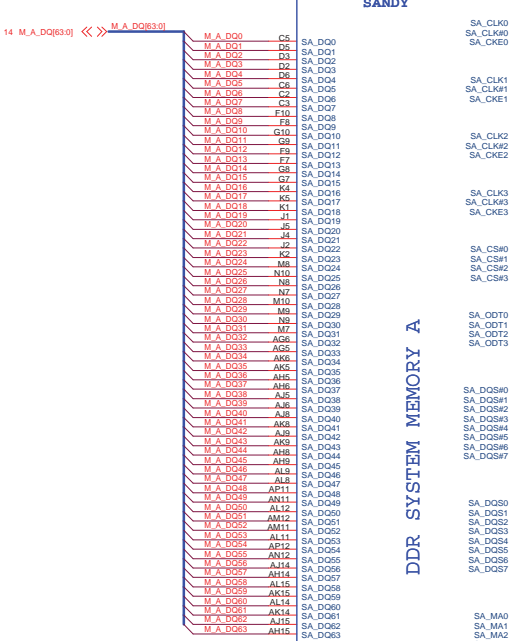
- XDP_PREQ# >>> XDP_PREQ# 11
- XDP_PRDY# >>> XDP_PRDY# 11
- XDP_BPM0 >>> XDP_BPM0 11
- XDP_BPM1 >>> XDP_BPM1 11
- XDP_BPM2 >>> XDP_BPM2 11
- XDP_BPM3 >>> XDP_BPM3 11
- XDP_BPM4 >>> XDP_BPM4 11
- XDP_BPM5 >>> XDP_BPM5 11
- XDP_BPM6 >>> XDP_BPM6 11
- XDP_BPM7 >>> XDP_BPM7 11
- XDP_TDO >>> XDP_TDO 11
- XDP_TDI >>> XDP_TDI 11
- XDP_TRST# >>> XDP_TRST# 11
- XDP_TCLK >>> XDP_TCLK 11
- XDP_TMS >>> XDP_TMS 11
- XDP_DBRESET# >>> XDP_DBRESET# 11,19

20100722 follow Astro add buffer



BOM

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Title: CPU (THERMAL/CLOCK/PM)			
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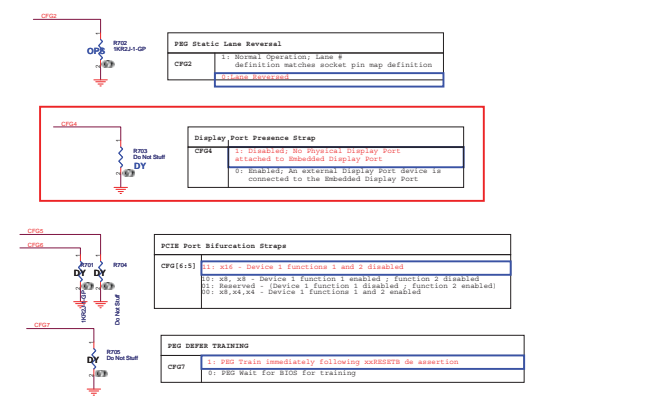
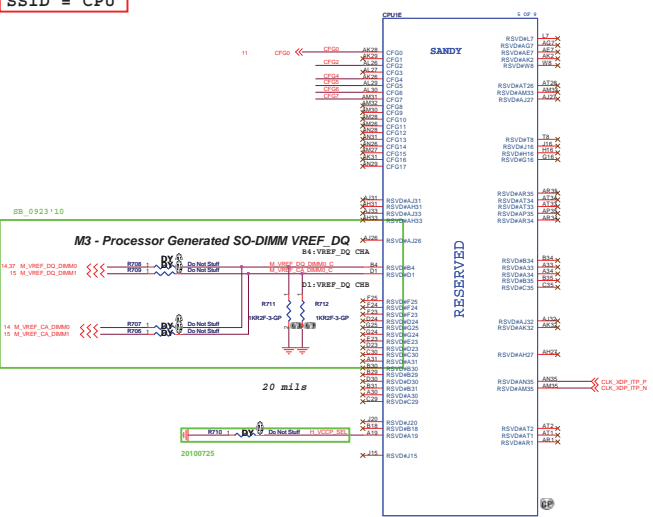
DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

BCM

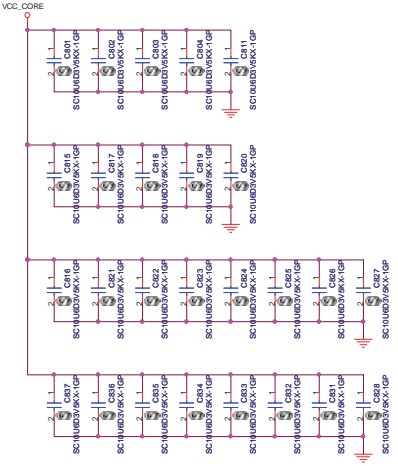
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File: CPU (DDR)
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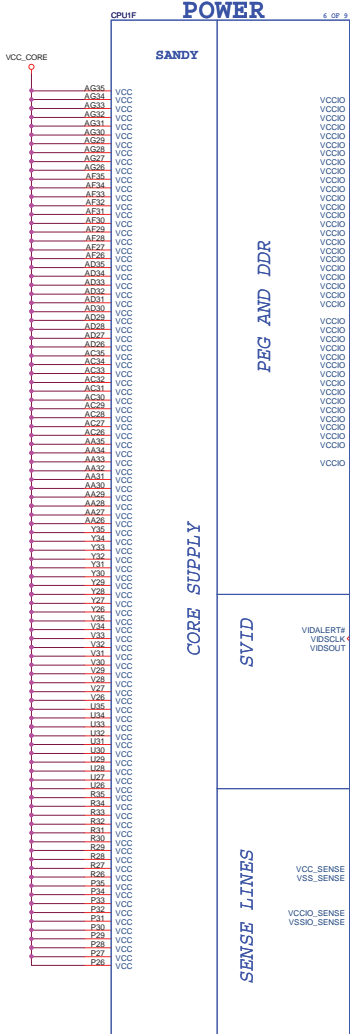


SSID = CPU

PROCESSOR CORE POWER
53A



VCC Output Decoupling Recommendation:
 4 x 470 uF at Bottom Socket Edge
 8 x 22 uF at Top Socket Cavity
 8 x 22 uF at Top Socket Edge
 8 x 22 uF at Bottom Socket Cavity



POWER

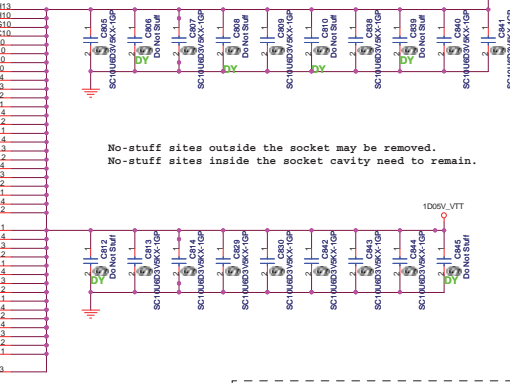
PEG AND DDR

CORE SUPPLY

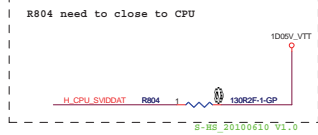
SVID

SENSE LINES

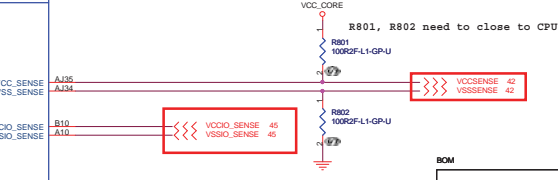
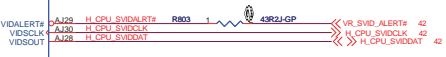
VCCIO Output Decoupling Recommendation:
 2 x 330 uF (3 x 330 uF for 2012 capable designs)
 5 x 22 uF & 8 x 0805 no-stuff at Bottom
 7 x 22 uF & 4 x 0805 no-stuff at Top



No-stuff sites inside the socket may be removed.
 No-stuff sites inside the socket cavity need to remain.



R804 need to close to CPU



BCM
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Title: **CPU (VCC CORE)**

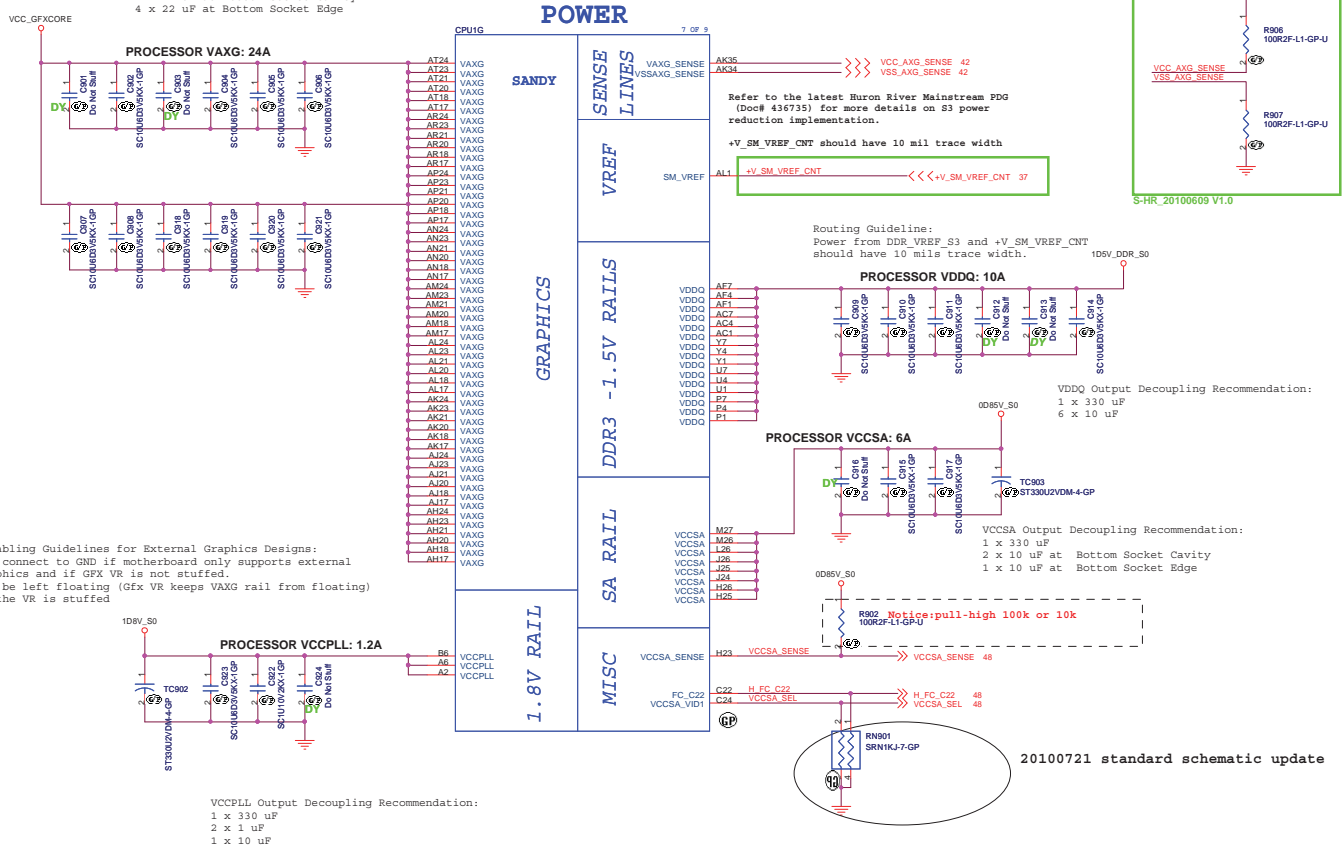
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SSID = CPU

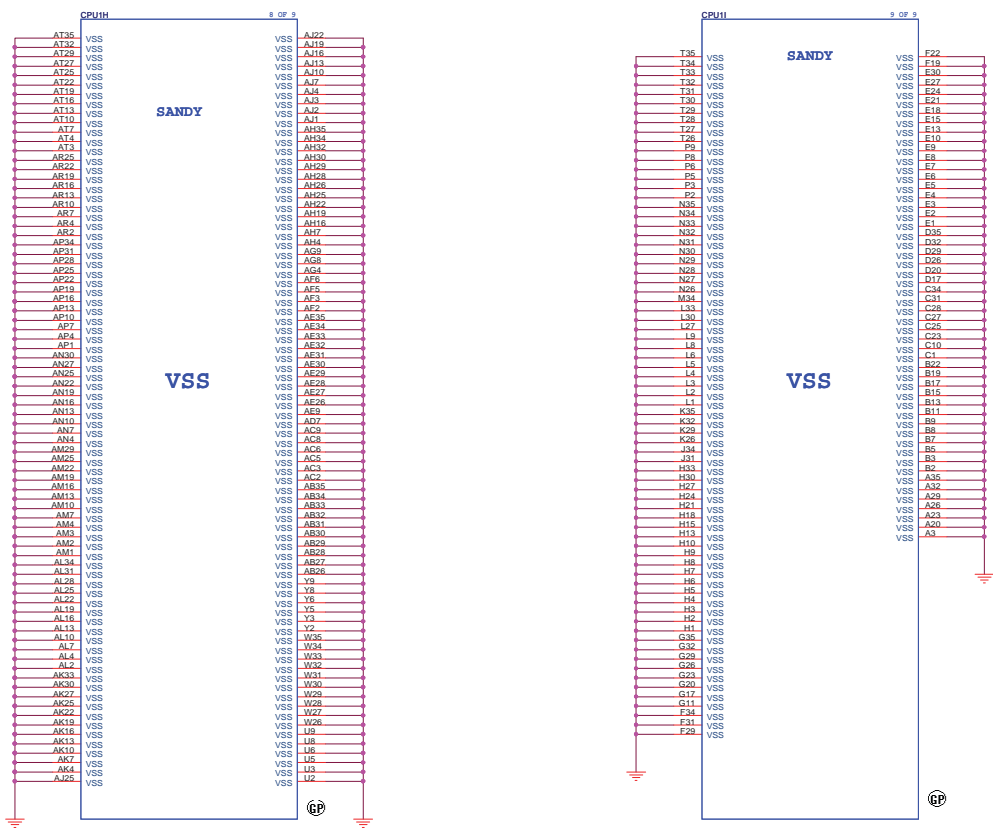
VAXG Output Decoupling Recommendation:
 2 x 470 uF at Bottom Socket Edge
 2 x 22 uF at Top Socket Cavity
 4 x 22 uF at Top Socket Edge
 2 x 22 uF at Bottom Socket Cavity
 4 x 22 uF at Bottom Socket Edge



Disabling Guidelines for External Graphics Designs:
 Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
 Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

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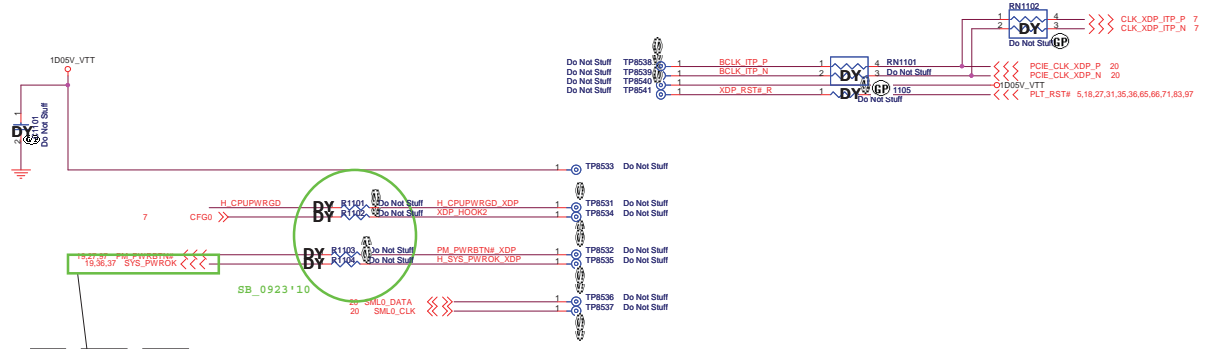
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File	CPU (VCC GFXCORE)
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5	XDP_PREQ#	>>>	XDP_PREQ#	1	TP8515	Do Not Stuff
5	XDP_PRDY#	>>>	XDP_PRDY#	1	TP8516	Do Not Stuff
5	XDP_BPM0	>>>	XDP_BPM0	1	TP8517	Do Not Stuff
5	XDP_BPM1	>>>	XDP_BPM1	1	TP8518	Do Not Stuff
5	XDP_BPM2	>>>	XDP_BPM2	1	TP8519	Do Not Stuff
5	XDP_BPM3	>>>	XDP_BPM3	1	TP8520	Do Not Stuff
5	XDP_BPM4	>>>	XDP_BPM4	1	TP8521	Do Not Stuff
5	XDP_BPM5	>>>	XDP_BPM5	1	TP8522	Do Not Stuff
5	XDP_BPM6	>>>	XDP_BPM6	1	TP8523	Do Not Stuff
5	XDP_BPM7	>>>	XDP_BPM7	1	TP8524	Do Not Stuff
5	XDP_TDO	>>>	XDP_TDO	1	TP8525	Do Not Stuff
5	XDP_TDI	>>>	XDP_TDI	1	TP8526	Do Not Stuff
5	XDP_TRST#	>>>	XDP_TRST#	1	TP8527	Do Not Stuff
5	XDP_TCLK	>>>	XDP_TCLK	1	TP8528	Do Not Stuff
5	XDP_TMS	>>>	XDP_TMS	1	TP8529	Do Not Stuff
5,19	XDP_DBRESET#	>>>	XDP_DBRESET#	1	TP8530	Do Not Stuff
5,22,36,37	H_CPUUPWRGD	>>>	H_CPUUPWRGD	1		



CAD Note: The resistor for H00K2 should be placed such that the stub is very small on CFG0 net.

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XDP	
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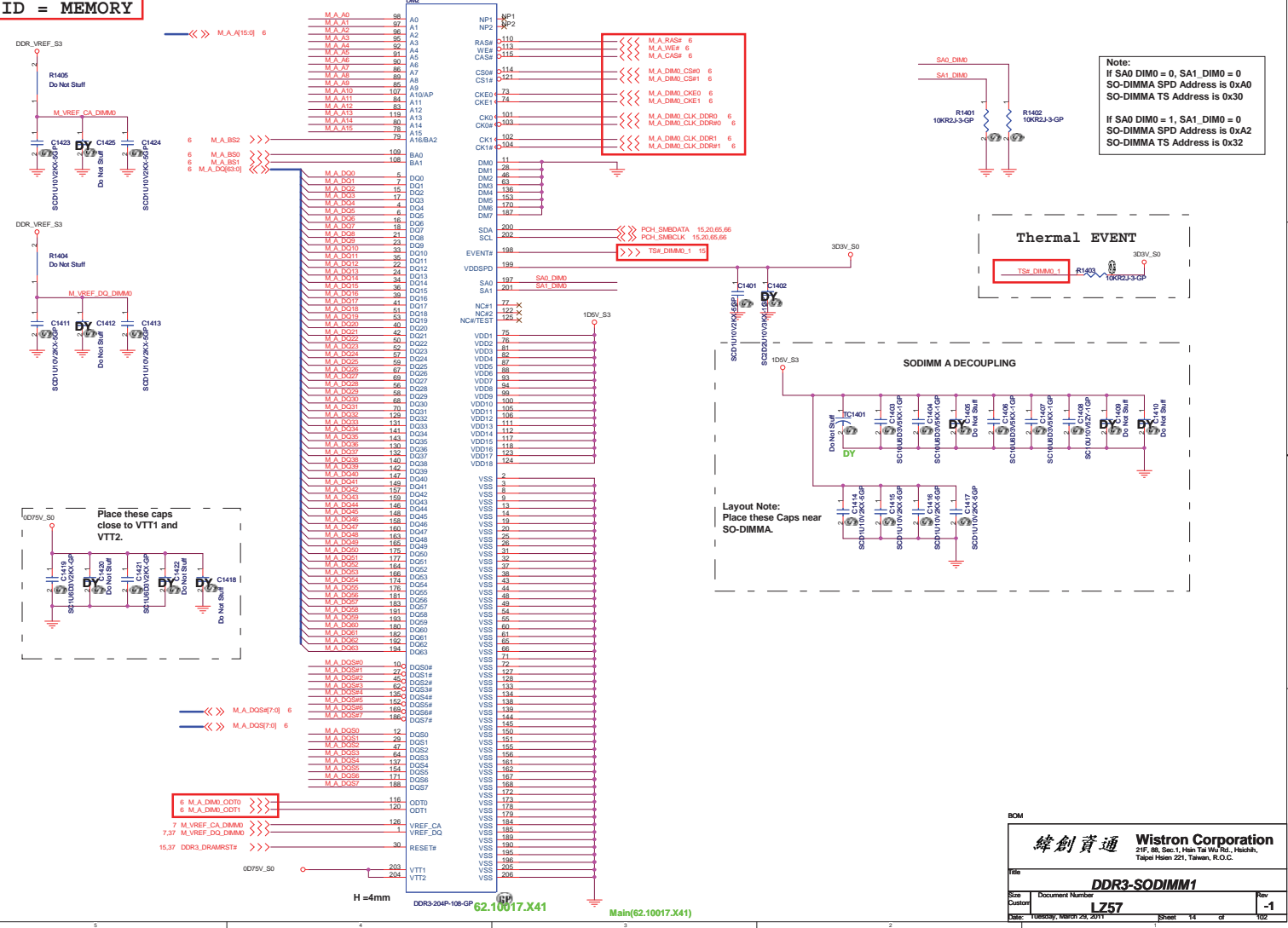
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SSID = MEMORY



SCM

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File: **DDR3-SODIMM1**

Size: **L757**

Docu: **L757**

Date: **1/28/2011**

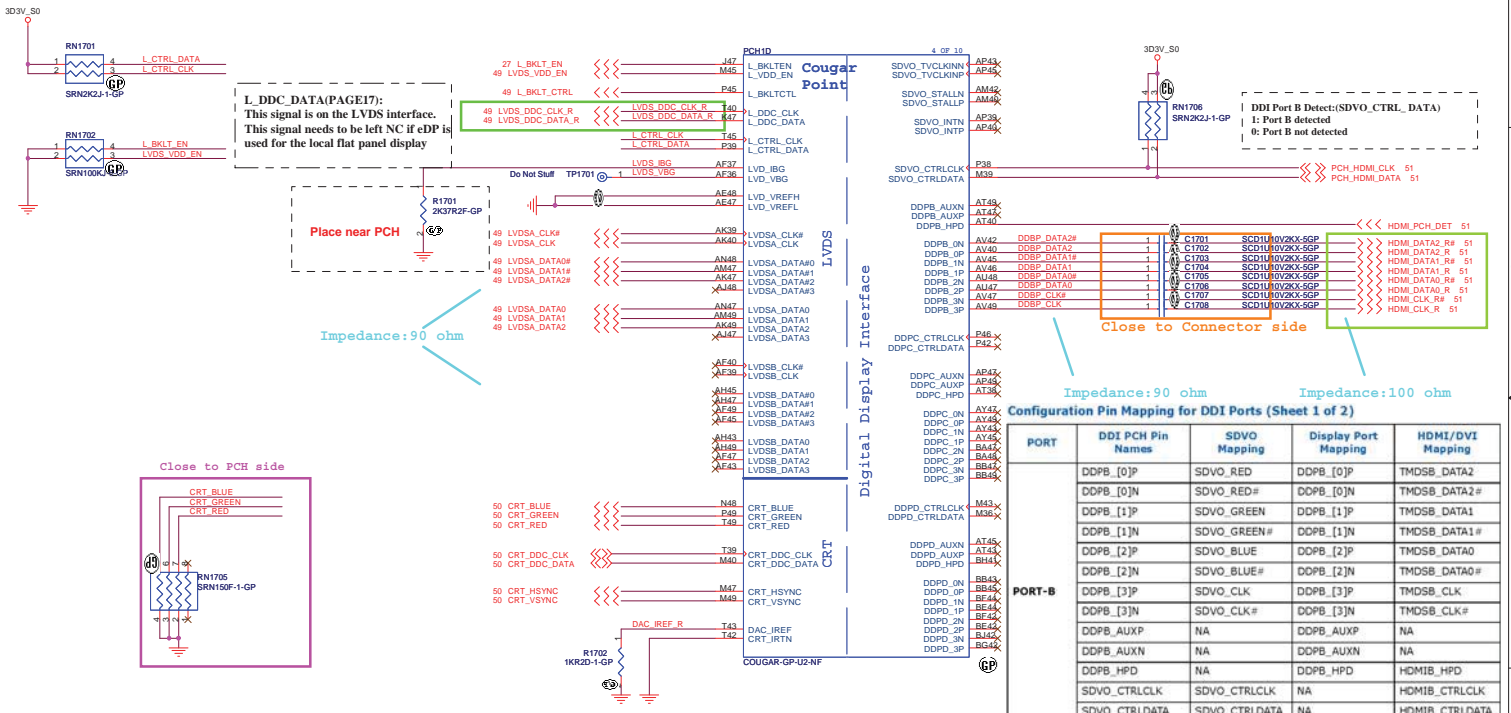
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DDR3-SODIMM2			
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Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_0[P]	SDVO_RED	DDPB_0[P]	TMDSB_DATA2
	DDPB_0[N]	SDVO_RED#	DDPB_0[N]	TMDSB_DATA2#
	DDPB_1[P]	SDVO_GREEN	DDPB_1[P]	TMDSB_DATA1
	DDPB_1[N]	SDVO_GREEN#	DDPB_1[N]	TMDSB_DATA1#
	DDPB_2[P]	SDVO_BLUE	DDPB_2[P]	TMDSB_DATA0
	DDPB_2[N]	SDVO_BLUE#	DDPB_2[N]	TMDSB_DATA0#
	DDPB_3[P]	SDVO_CLK	DDPB_3[P]	TMDSB_CLK
	DDPB_3[N]	SDVO_CLK#	DDPB_3[N]	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA	

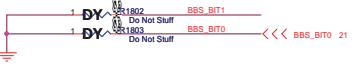
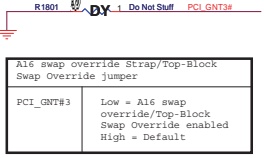
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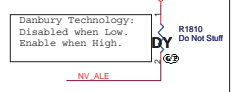
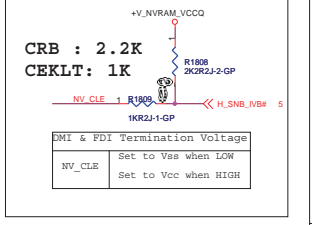
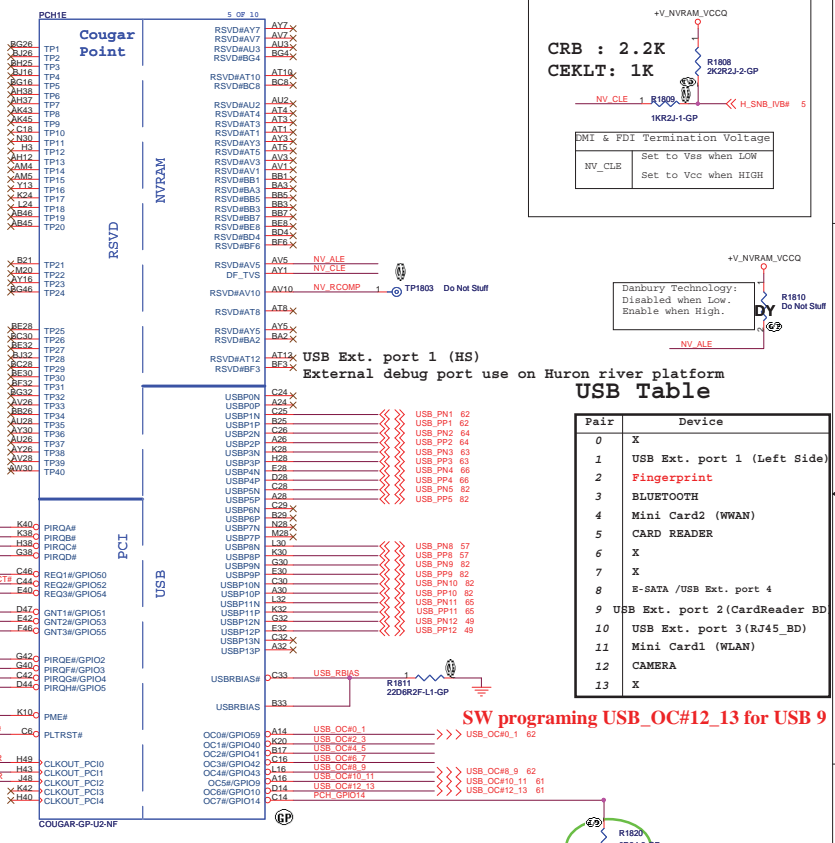
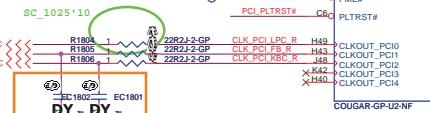
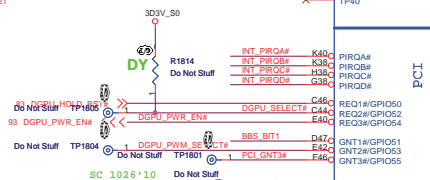
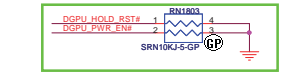
File: **PCH (LVDS/CRT/DDI)**

Size: A3 Document Number: **LZ57** Rev: **-1**

Date: (Monday, March 29, 2011) Sheet: 17 of 102



ENT1#/GPIO1	SATA1GF/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SFI (Default)



USB Ext. port 1 (HS)
External debug port use on Huron river platform
USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2 (CardReader BD)
10	USB Ext. port 3 (R045_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SW programming USB_OC#12_13 for USB 9



OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

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PCH (PCI/USB/NVRAM)
LZ57

File: LZ57, Size: A3, Document Number: LZ57, Date: 08/29/2011, Sheet: 18 of 102, Rev: -1

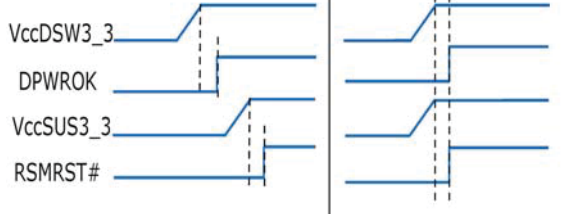
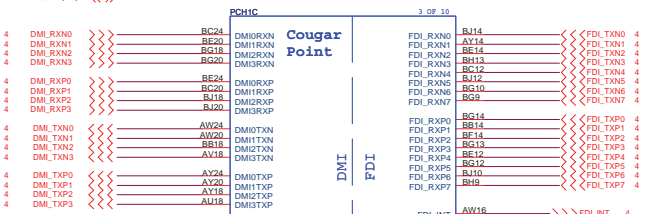
SSID = PCH



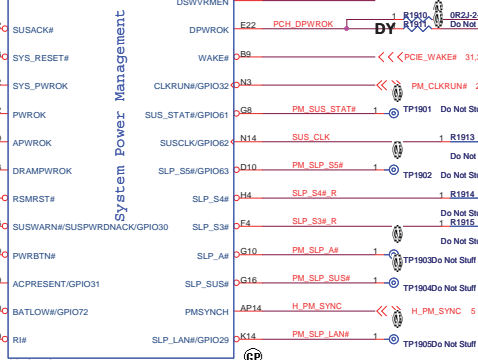
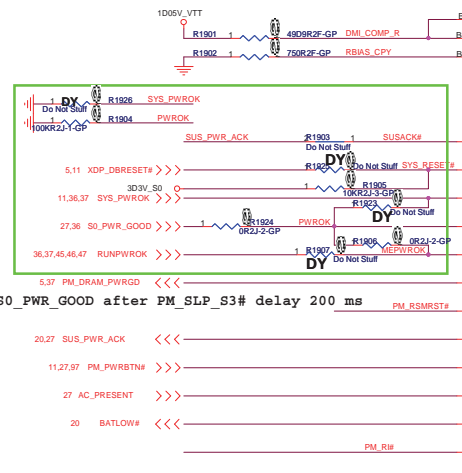
Deep S4/S5 Supported

Deep S4/S5 Not Supported

Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

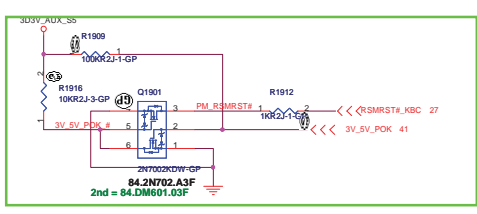
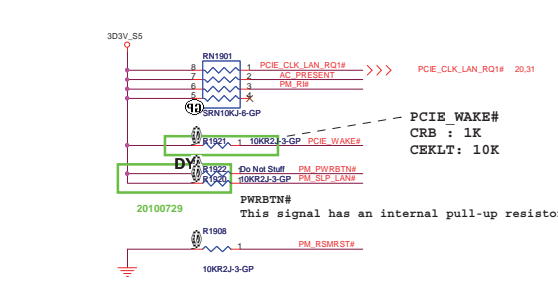


For platforms not supporting Deep S4/S5
 1. VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
 2. DPWROK and RSMRST# will rise at the same time (connected on board)
 3. SLP_SUS# and SUSACK# are left as 'no connect'
 4. SUSWARN# used as SUSPWRDNACK/GPIO30



DSVDVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled



BOM

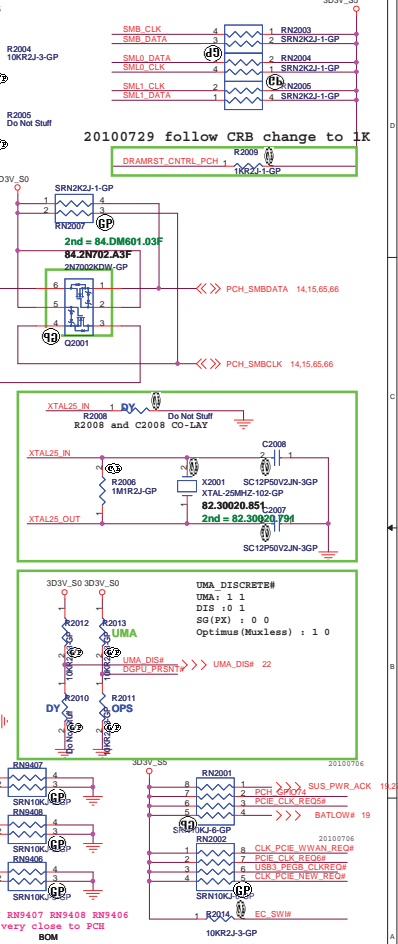
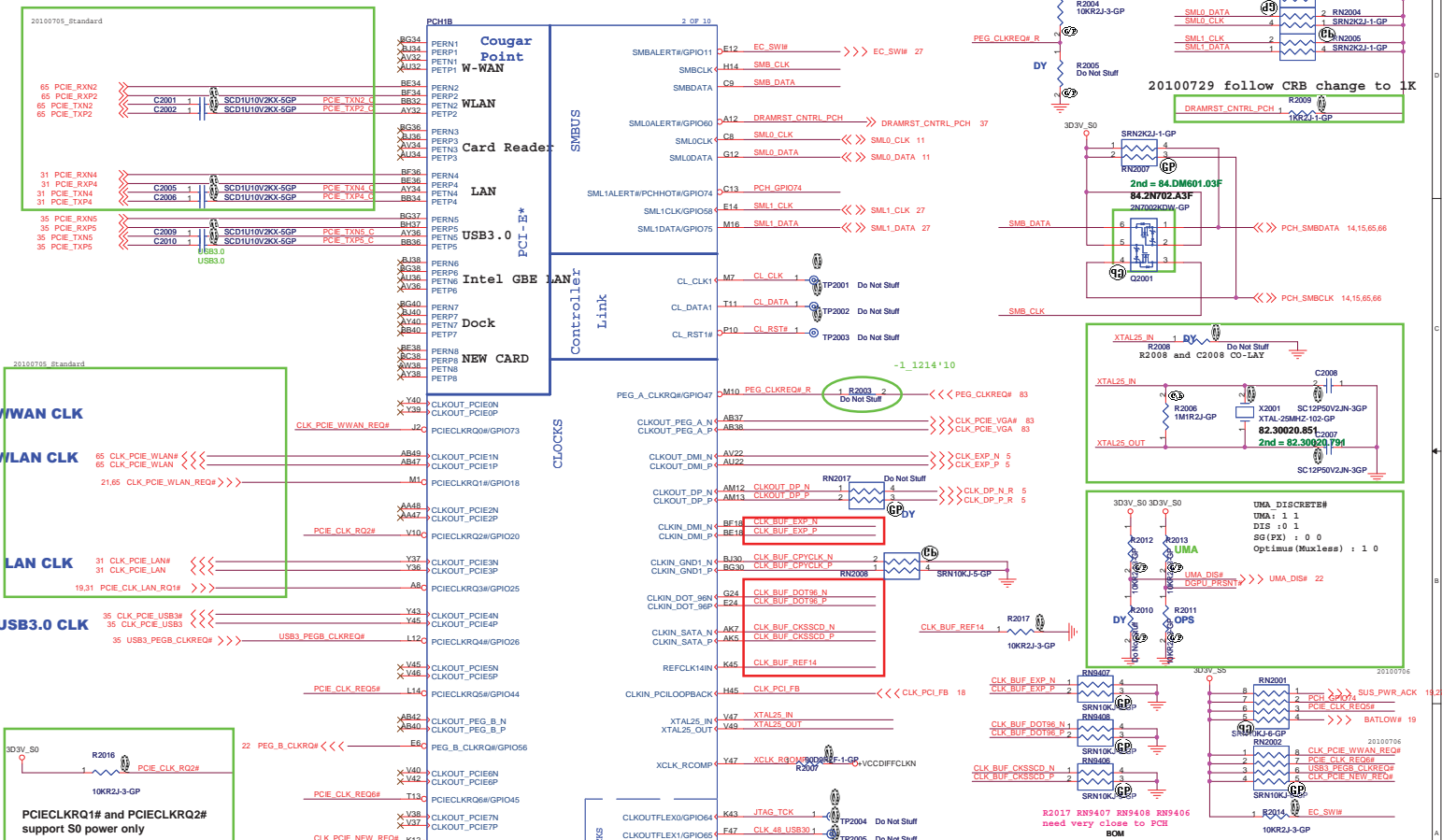
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File: **PCH (DM /FDI/PM)**

Size: K3 Document Number: **LZ57** Rev: **-1**

Date: (Issued) March 29, 2011 Sheet 19 of 102

SSID = PCH

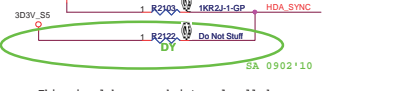
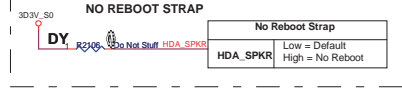
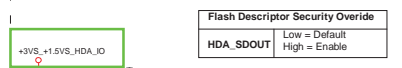
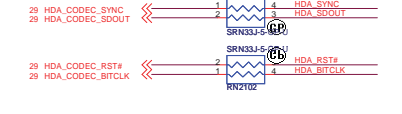
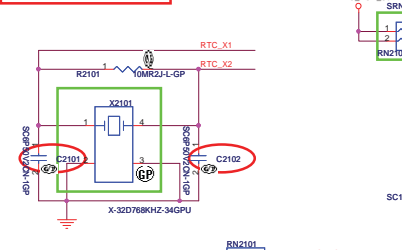


20100706
 - Prioritize 27/14/2.7-3/25-MHz FLEX on FLEX1 and FLEX3
 - Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
 if more than 2 PCI clocks + PCI loopback are routed.

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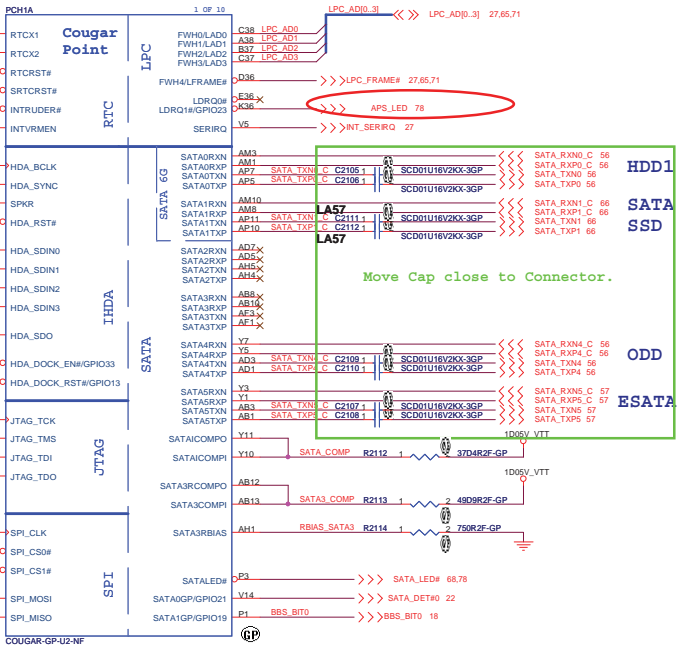
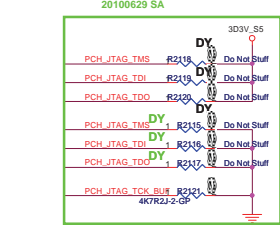
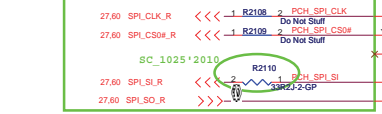
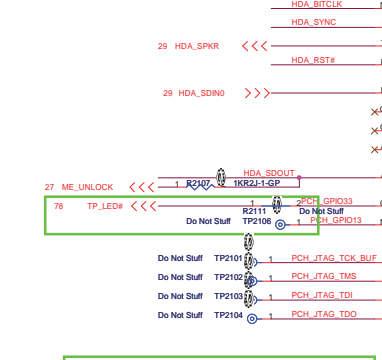
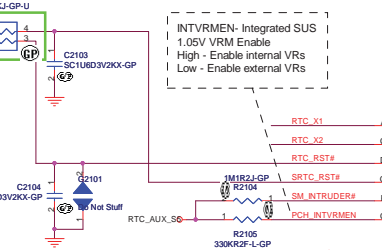
File: **PCH (PCI-E/SMBUS/CLOCK/CL)**
 Size: A3 Document Number: **LZ57**
 Date: (Sunday, March 29, 2011) Sheet: 20 of 102 Rev: **-1**

SSID = PCH



This signal has a weak internal pull down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform. co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



BOM

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File: PCH (SPI/RTC/LPC/SATA/IHDA)
Date: Tuesday, March 29, 2011
Sheet 21 of 102

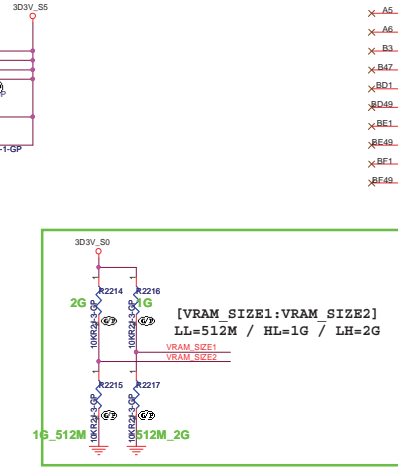
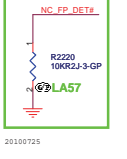
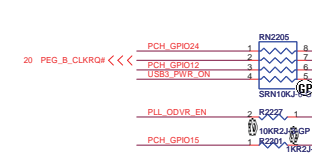
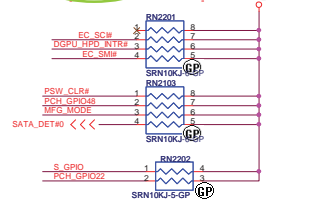
Rev -1

SSID = PCH

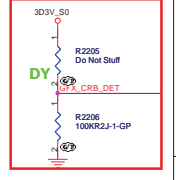
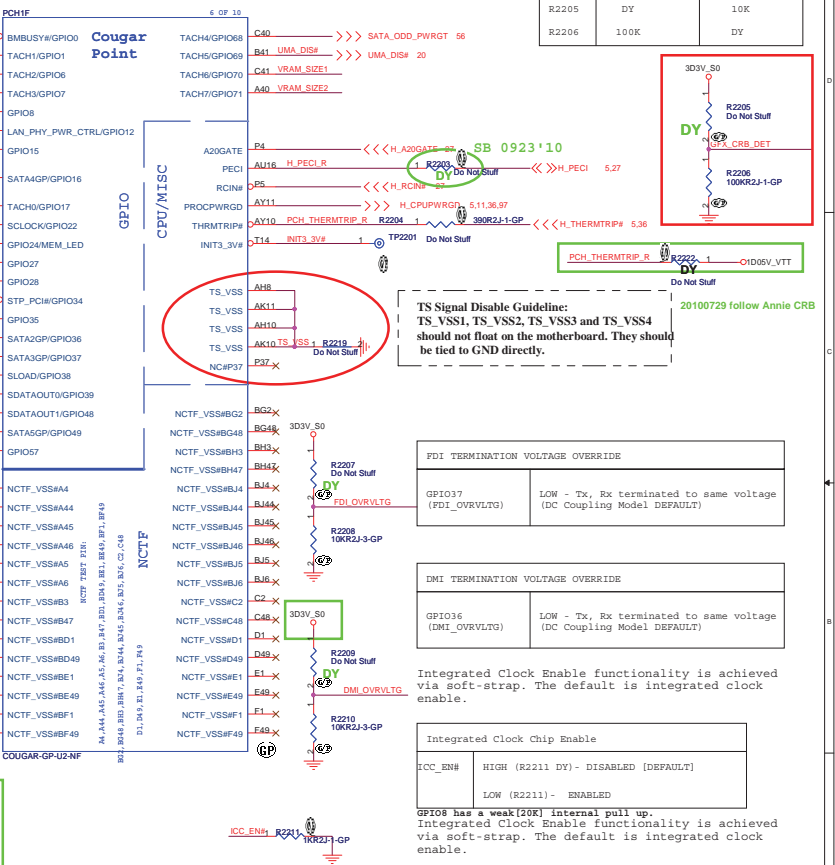
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



GPI027 has a weak [20K] internal pull up. To enable on-die PLL Voltage regulator, should not place external pull down.



Note:
For PCH debug with XDP, need to NO STUFF R2218



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPI037 (FDI_OVRVLGT)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPI036 (DMI_OVRVLGT)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

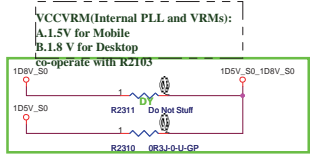
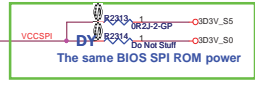
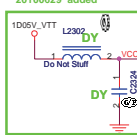
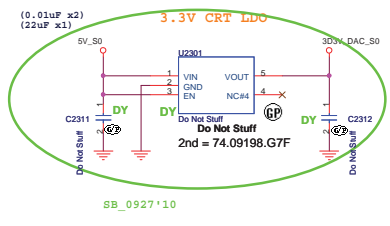
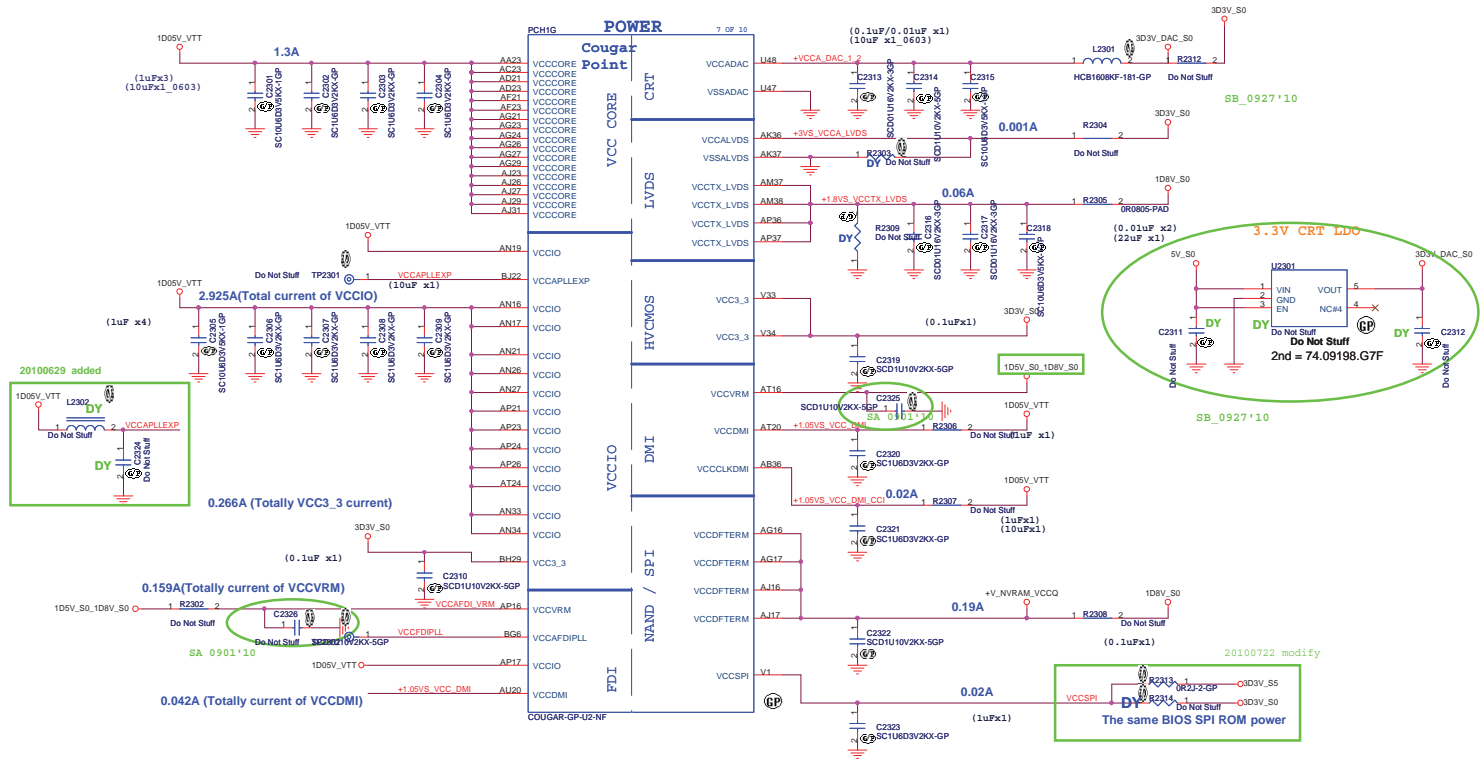
Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPI08 has a weak [20K] internal pull up. Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE

Note: This signal has a weak internal pull-up 20K.
 ENABLED -- HIGH (R2211 UNSTUFFED) DEFAULT
 DISABLED -- LOW (R2211 STUFFED)

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PCH (GPIO/CPU)	
File	LZ57
Size A3	Document Number
Date: (Monday, March 29, 2011)	Sheet 22 of 102
	Rev -1

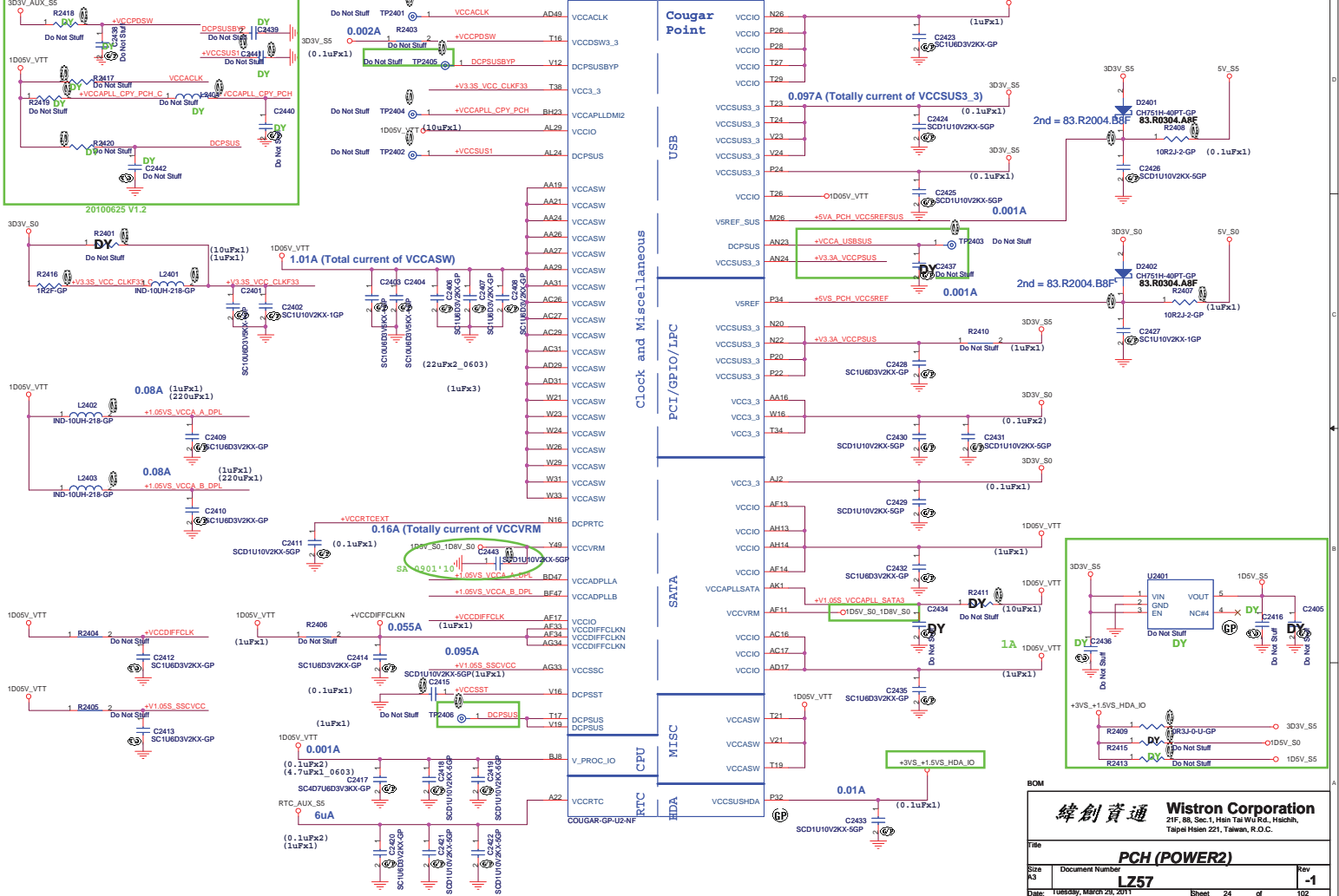


BOM

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File	PCH (POWER1)	
Size	Document Number	Rev
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SSID = PCH



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File		PCH (POWER2)	
Size	Document Number		Rev
A3	LZ57		-1
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PCHH 8 OF 10

Cougar Point

HS	VSS	AK38
AA17	VSS	AK4
AA2	VSS	AK42
AA3	VSS	AK46
AA33	VSS	AK9
AA34	VSS	AL16
AB11	VSS	AL17
AB14	VSS	AL19
AB39	VSS	AL2
AB4	VSS	AL21
AB43	VSS	AL23
AB5	VSS	AL26
AB7	VSS	AL27
AC	VSS	AL41
AC1	VSS	AL43
AC19	VSS	AL46
AC24	VSS	AM11
AC3	VSS	AM14
AC34	VSS	AM36
AC8	VSS	AM43
AD10	VSS	AM45
AD11	VSS	AM46
AD12	VSS	AM7
AD13	VSS	AM2
AD19	VSS	AM29
AD24	VSS	AM3
AD36	VSS	AM31
AD7	VSS	AP12
AD9	VSS	AP19
AD98	VSS	AP26
AD99	VSS	AP30
AD4	VSS	AP32
AD40	VSS	AP38
AD42	VSS	AP4
AD43	VSS	AP42
AD45	VSS	AP46
AD6	VSS	AR9
AD8	VSS	AR2
AE2	VSS	AR48
AE3	VSS	AT11
AE10	VSS	AT13
AE12	VSS	AT16
AD14	VSS	AT22
AD16	VSS	AT26
AE16	VSS	AT28
AE18	VSS	AT30
AE19	VSS	AT32
AF24	VSS	AT34
AF26	VSS	AT39
AF27	VSS	AT42
AF29	VSS	AT46
AF31	VSS	AT7
AF38	VSS	AV24
AF4	VSS	AV30
AF42	VSS	AV38
AF46	VSS	AV4
AF5	VSS	AV43
AF7	VSS	AV8
AF8	VSS	AW14
AG19	VSS	AW18
AG2	VSS	AW2
AG11	VSS	AW22
AG48	VSS	AW26
AH11	VSS	AW28
AH3	VSS	AW32
AH36	VSS	AW34
AH9	VSS	AW36
AH40	VSS	AW40
AH42	VSS	AW48
AH46	VSS	AW11
AH7	VSS	AW12
AH9	VSS	AW22
AI21	VSS	AW28
AI24	VSS	AW40
AI33	VSS	AW48
AK2	VSS	AY28
AK3	VSS	

COUGAR-GP-U2-NF

PCHH 9 OF 10

Cougar Point

AY4	VSS	H46
AY42	VSS	K18
AY46	VSS	K36
AY8	VSS	K39
B11	VSS	K46
B16	VSS	L18
B19	VSS	L18
B21	VSS	L20
B27	VSS	L26
B31	VSS	L28
B36	VSS	L36
B39	VSS	L46
B7	VSS	M12
F46	VSS	M18
BB16	VSS	M22
BB20	VSS	M30
BB22	VSS	M34
BB24	VSS	M38
BB28	VSS	M4
BB30	VSS	M42
BB38	VSS	M48
BB4	VSS	M8
BB46	VSS	N18
BB48	VSS	N24
BB49	VSS	N47
BC2	VSS	P18
BC26	VSS	P30
BC32	VSS	P40
BC34	VSS	P43
BC40	VSS	P47
BC42	VSS	R46
BC48	VSS	T12
BD46	VSS	T31
BE2	VSS	T37
BE22	VSS	T4
BE46	VSS	W34
BE49	VSS	T46
BF22	VSS	T47
BF24	VSS	T8
BF28	VSS	V11
BF28	VSS	V17
BF3	VSS	V36
BF30	VSS	V27
BF36	VSS	V29
BF40	VSS	V31
BF8	VSS	V36
BG17	VSS	Y28
BG21	VSS	V43
BG33	VSS	W7
BG44	VSS	W17
CG8	VSS	W19
BH11	VSS	W2
BH15	VSS	W27
BH17	VSS	W46
BH18	VSS	Y12
H10	VSS	Y38
BH27	VSS	Y4
BH31	VSS	Y42
BH33	VSS	Y46
BH35	VSS	Y8
BH39	VSS	BG28
BH43	VSS	N4
BH7	VSS	A13
D1	VSS	AD47
D12	VSS	B43
D16	VSS	BC10
D18	VSS	BC41
D22	VSS	G14
D24	VSS	H16
D28	VSS	T36
D31	VSS	BG22
D32	VSS	BG24
D34	VSS	C2
D36	VSS	AF13
D42	VSS	M14
D8	VSS	AP3
E18	VSS	AP1
F28	VSS	BE16
G18	VSS	BO16
G20	VSS	BG28
G28	VSS	R128
G48	VSS	
G48	VSS	
H12	VSS	
H18	VSS	
H22	VSS	
H24	VSS	
H26	VSS	
H30	VSS	
H32	VSS	
H34	VSS	
F1	VSS	

COUGAR-GP-U2-NF

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File

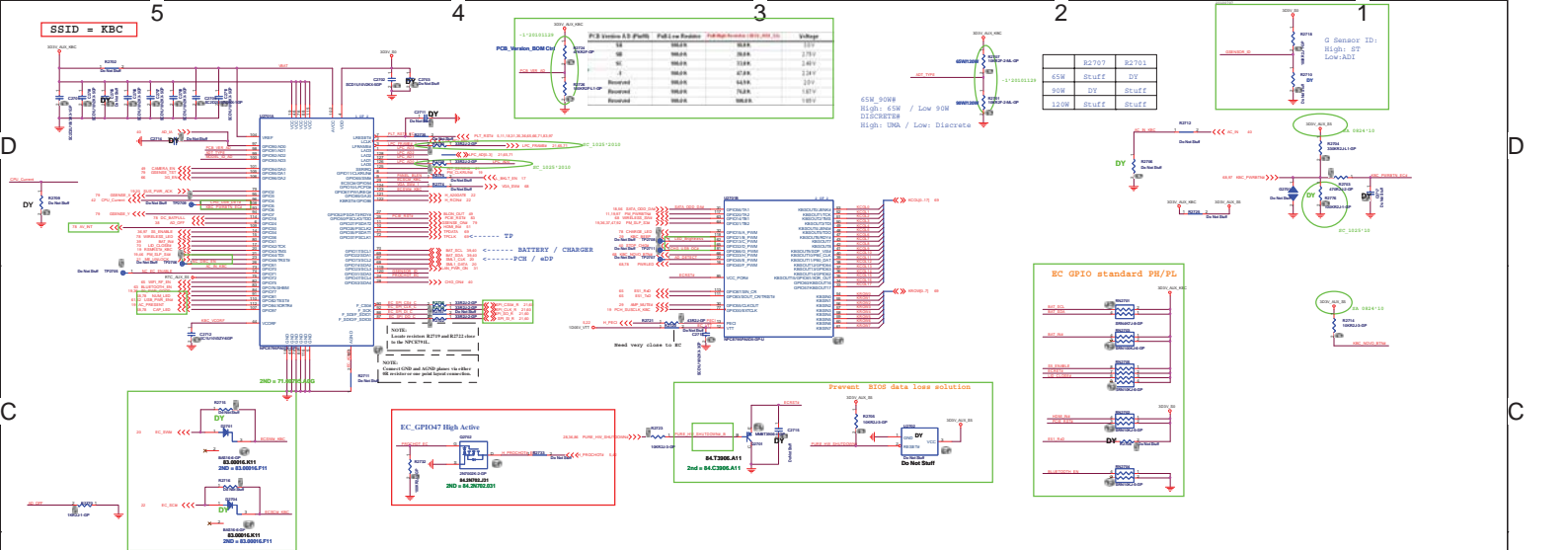
Size K3 Document Number **PCH (VSS)** Rev -1

Date: Tuesday, March 29, 2011 Sheet 25 of 102

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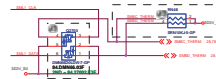
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Reserved		
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 26	of 102

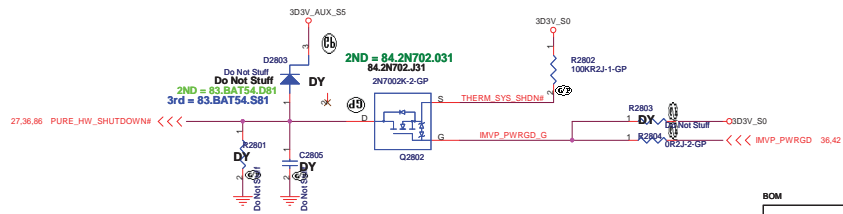
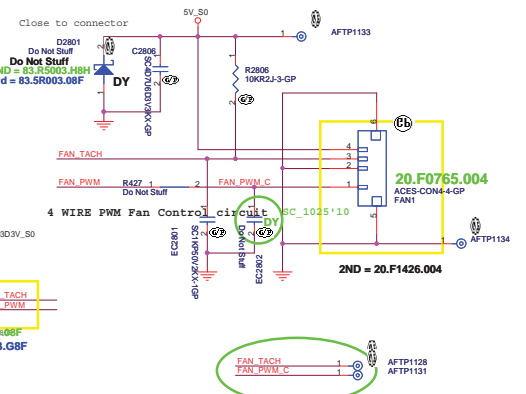
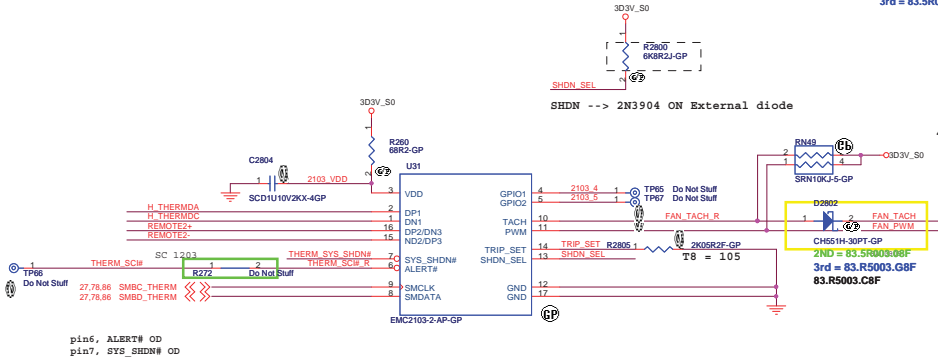
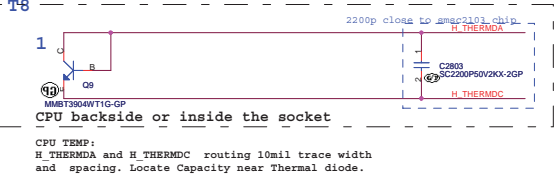
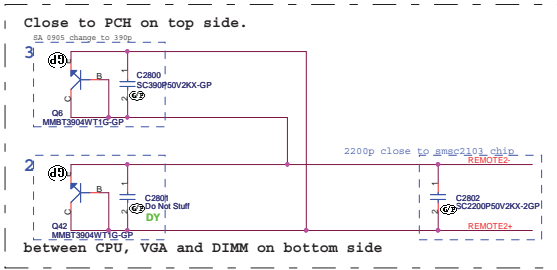


LILI Multi GPIO setting

SSSID = KBC



Model ID	BOM Ch	QFN	6A14335-00L
MODEL_ID_A01(1in10)	Pull-Low Register	Pull-High Register	Voltage
V/8 D7 00A	100.0 K	64.0 K	2.85V V
V/8 D7 OPT1M0	100.0 K	74.8 K	1.80V V
8 D7 00A	100.0 K	100.0 K	1.65V V
8 D7 OPT1M0	100.0 K	149.0 K(14.3433K L10)	1.12 V



BOM

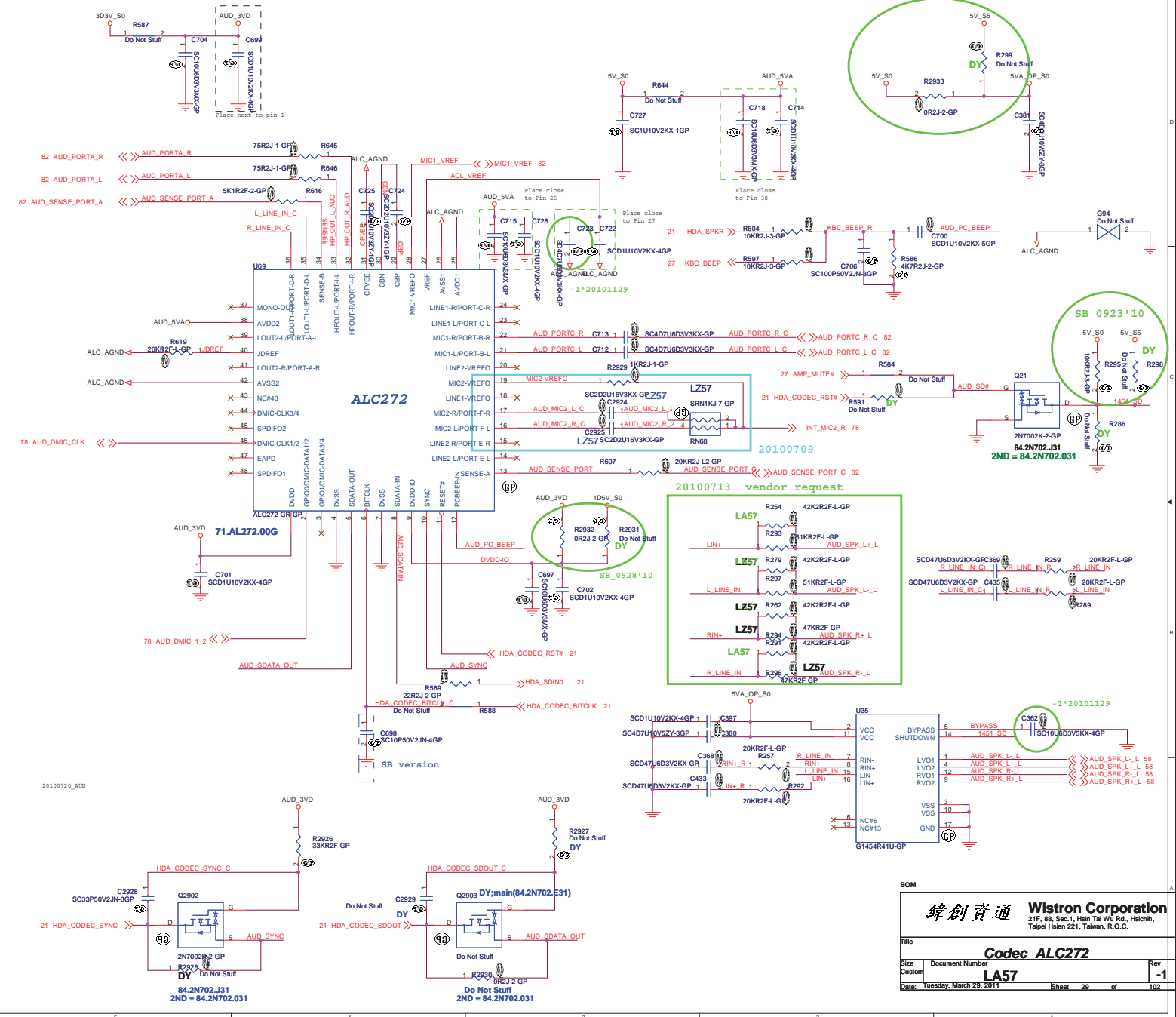
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File Thermal P2800/Fan Controller P2793

Size A3 Document Number LZ57

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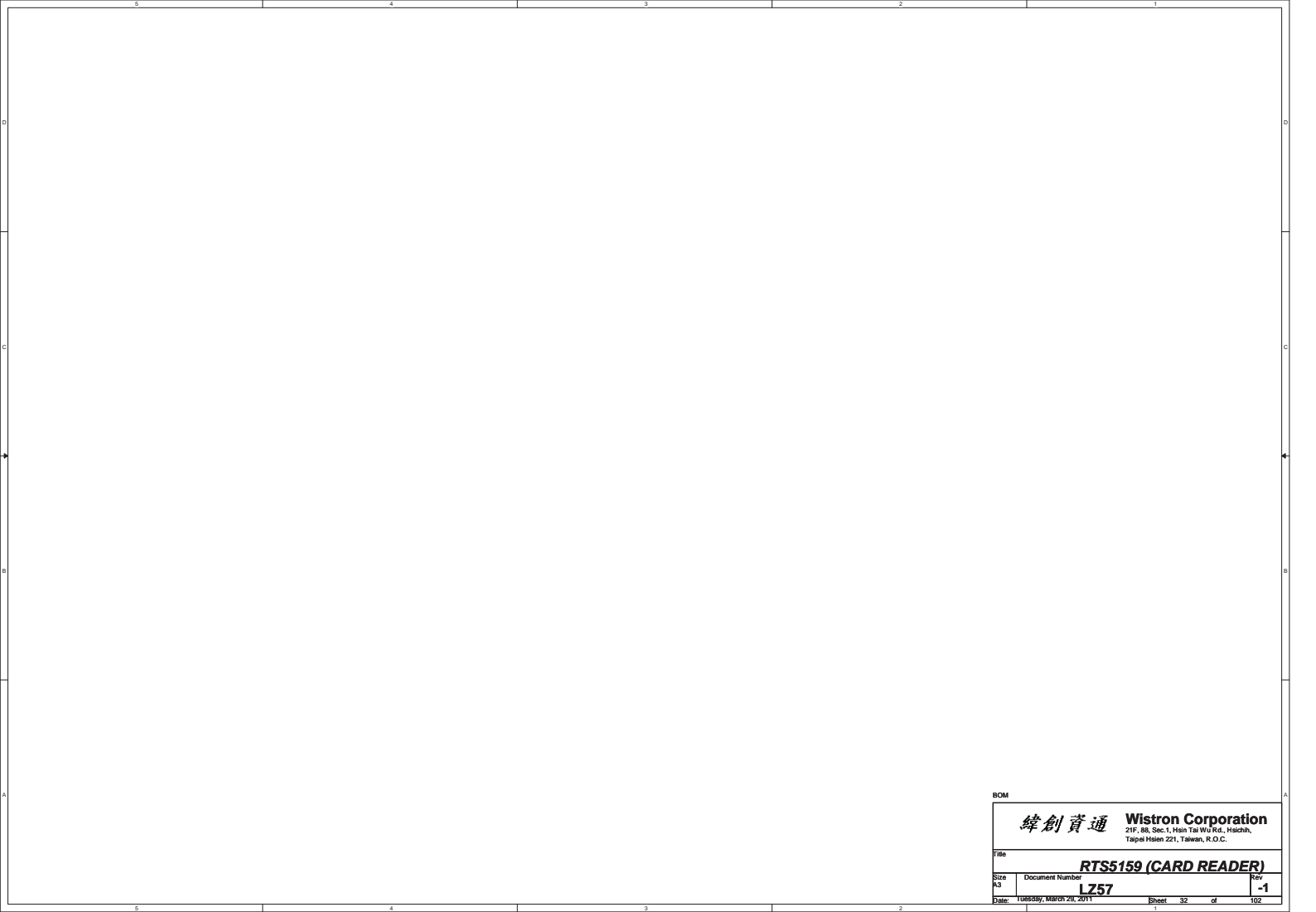


BOM	
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshu, Taipei Hsin 221, Taiwan, R.O.C.	
Title	Codec ALC272
Size	Document Number
Customer	LA57
Date:	Yurisdig, March 29, 2011
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reserved	
Size A4	Document Number LZ57
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緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
Title		RTS5159 (CARD READER)	
Size	Document Number	Rev	
A3	LZ57	-1	
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(Blanking)

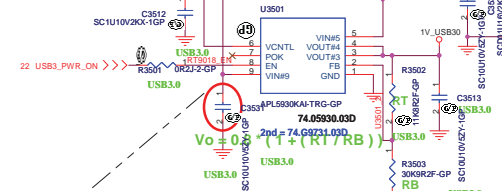
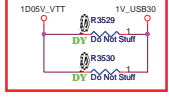
BOM

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A4	LZ57	-1	
Date:	Tuesday, March 29, 2011	Sheet	33 of 102

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BOM

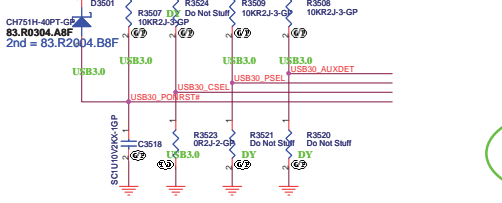
緯創資通 Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		
Reserved		
Size A4	Document Number LZ57	Rev -1
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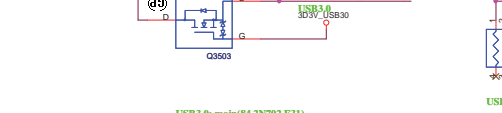
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 115V_S3 power rail.
 2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
 3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.



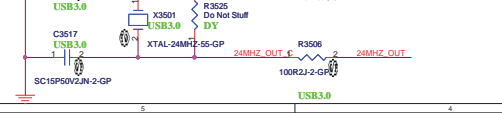
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 115V_S3 power rail.
 2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
 3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.



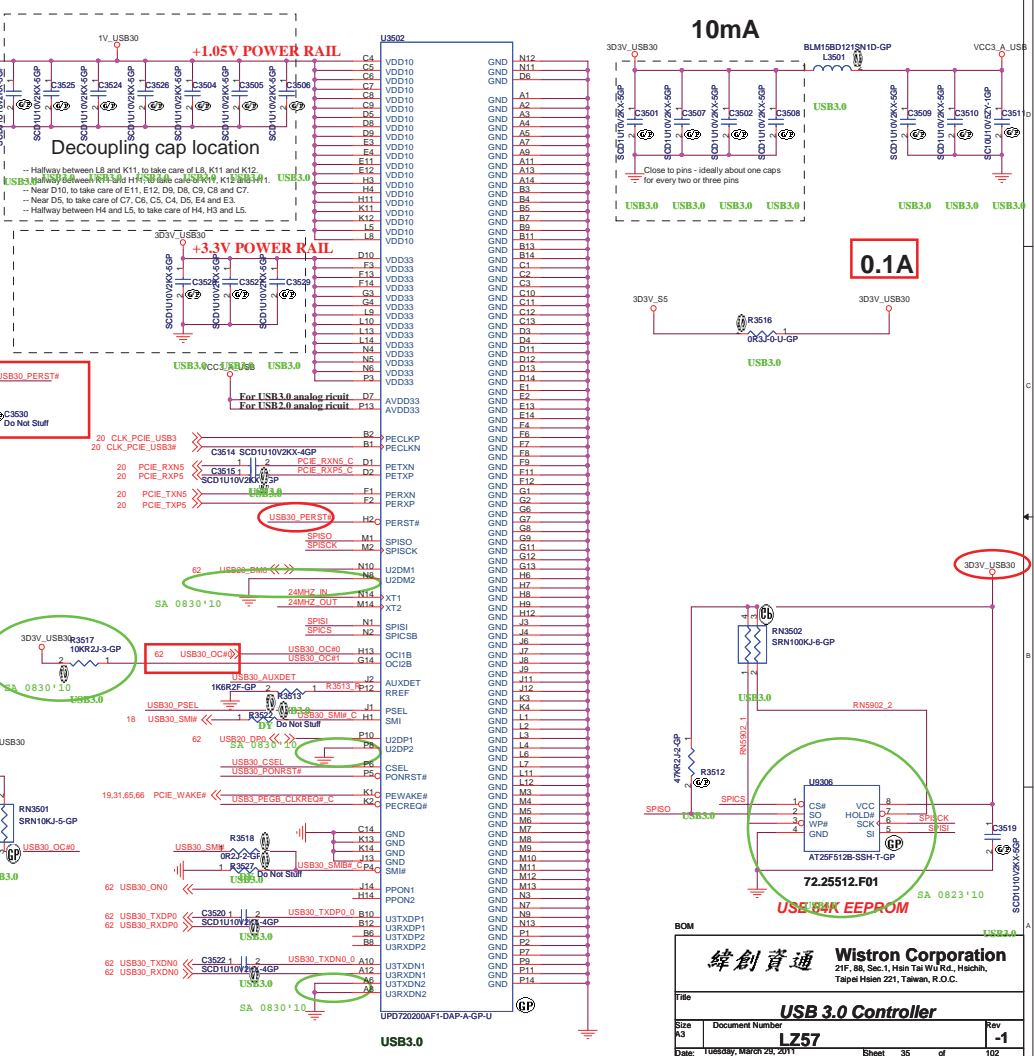
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 115V_S3 power rail.
 2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
 3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.



1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 115V_S3 power rail.
 2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
 3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.



1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 115V_S3 power rail.
 2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
 3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.

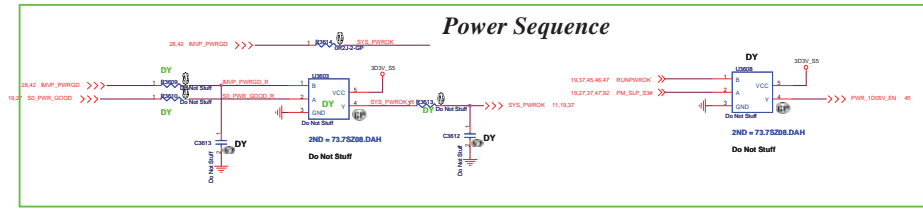


File	Document Number	Rev
USB 3.0 Controller	LZ57	-1

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

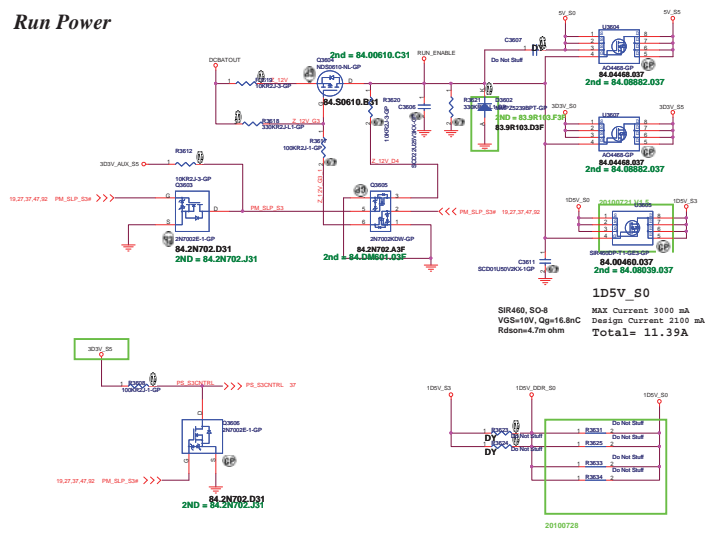
Date: 08/29/2011 Sheet 35 of 102

Power Sequence

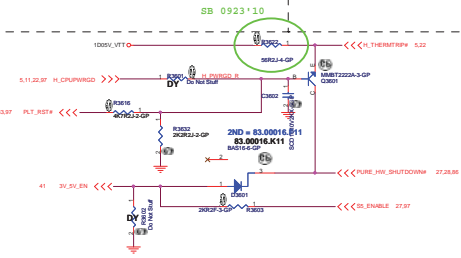


SSID = Reset.Suspend

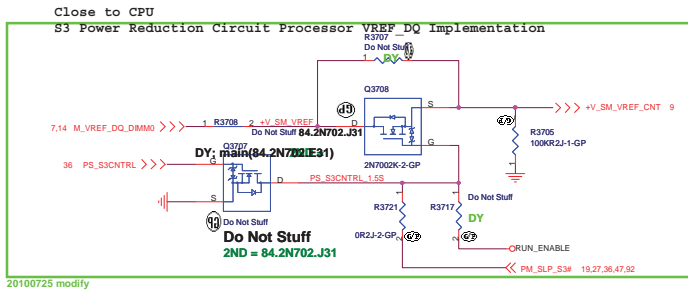
Run Power



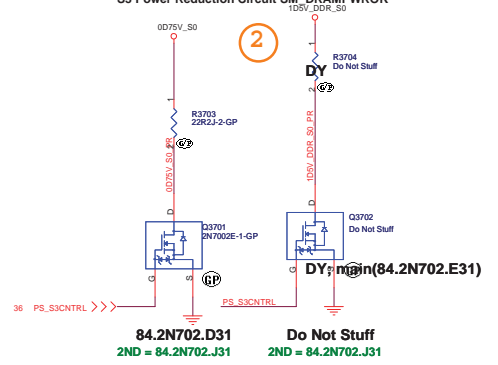
100V_S0
 SIR460, S0-8 MAX Current 3000 mA
 VGS=10V, Qg=16.8nC Design Current 2100 mA
 Rds(on)=4.7m ohm Total= 11.39A



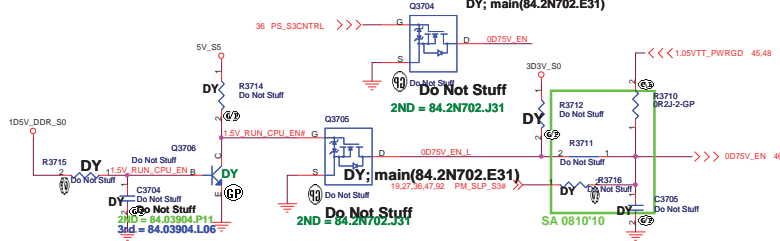
Wistron Corporation
 緯創資通
 31F, 31, Sec. 1, Ind. Tra. Park, Hsinchu, Taiwan, R.O.C.
Power Plane Enable
 Doc No: **LZ57**
 Rev: 36 of 102



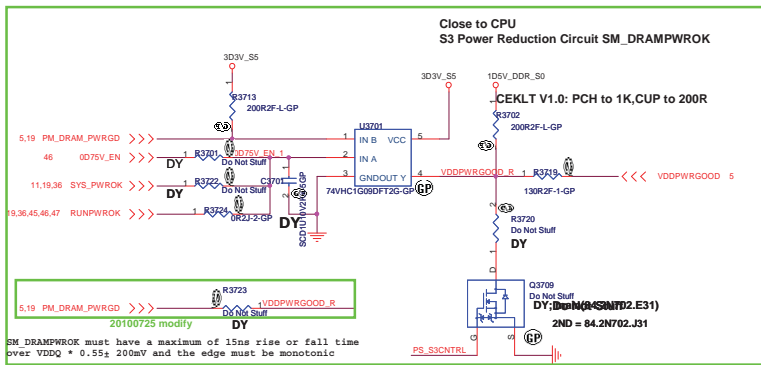
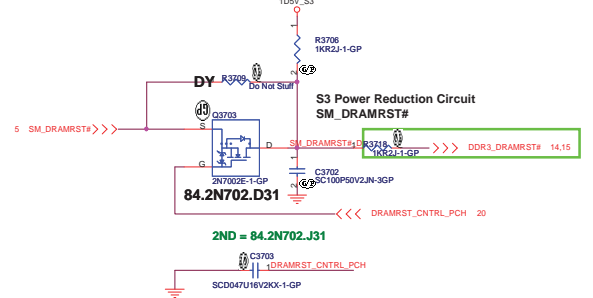
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



5 S3 Power Reduction X01 20091111



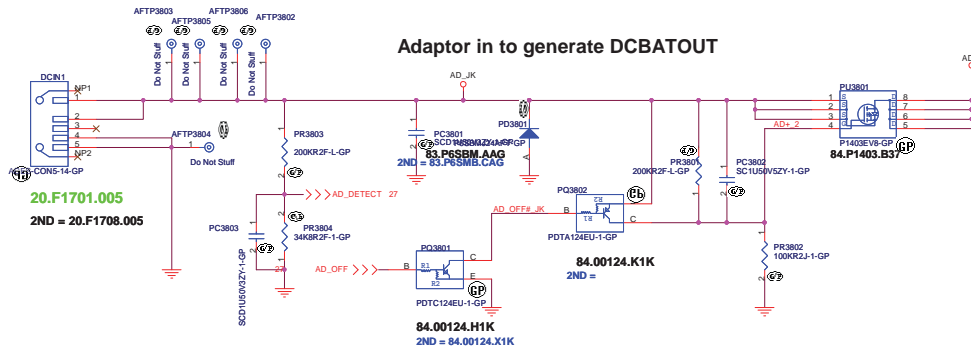
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



BOM

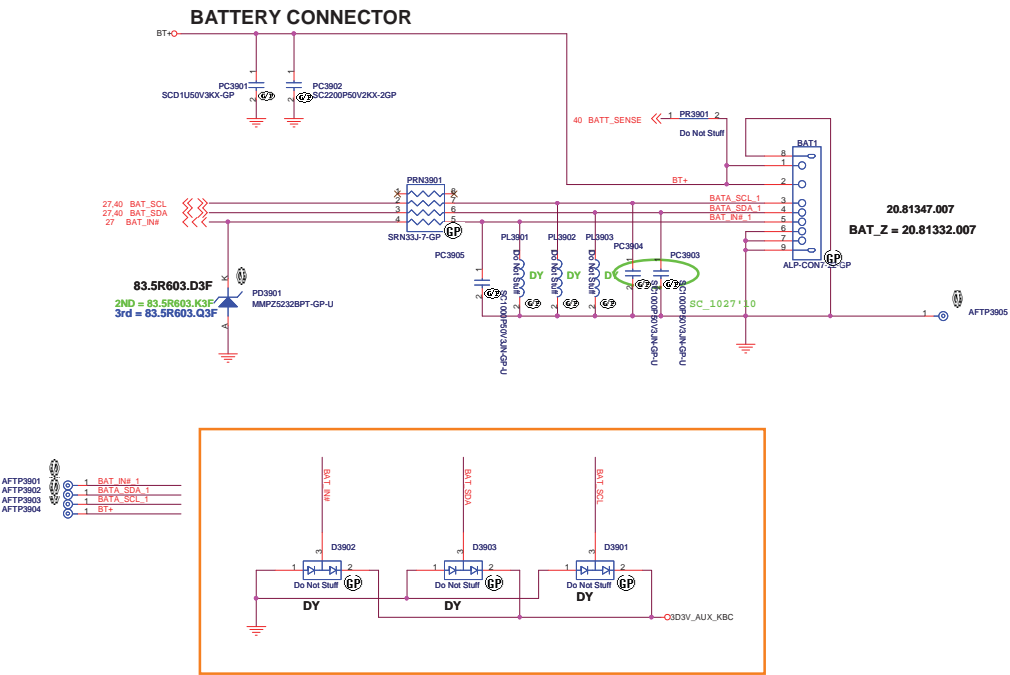
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File	ADAPTER		Rev
Size	Document Number	LZ57	-1
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BCM

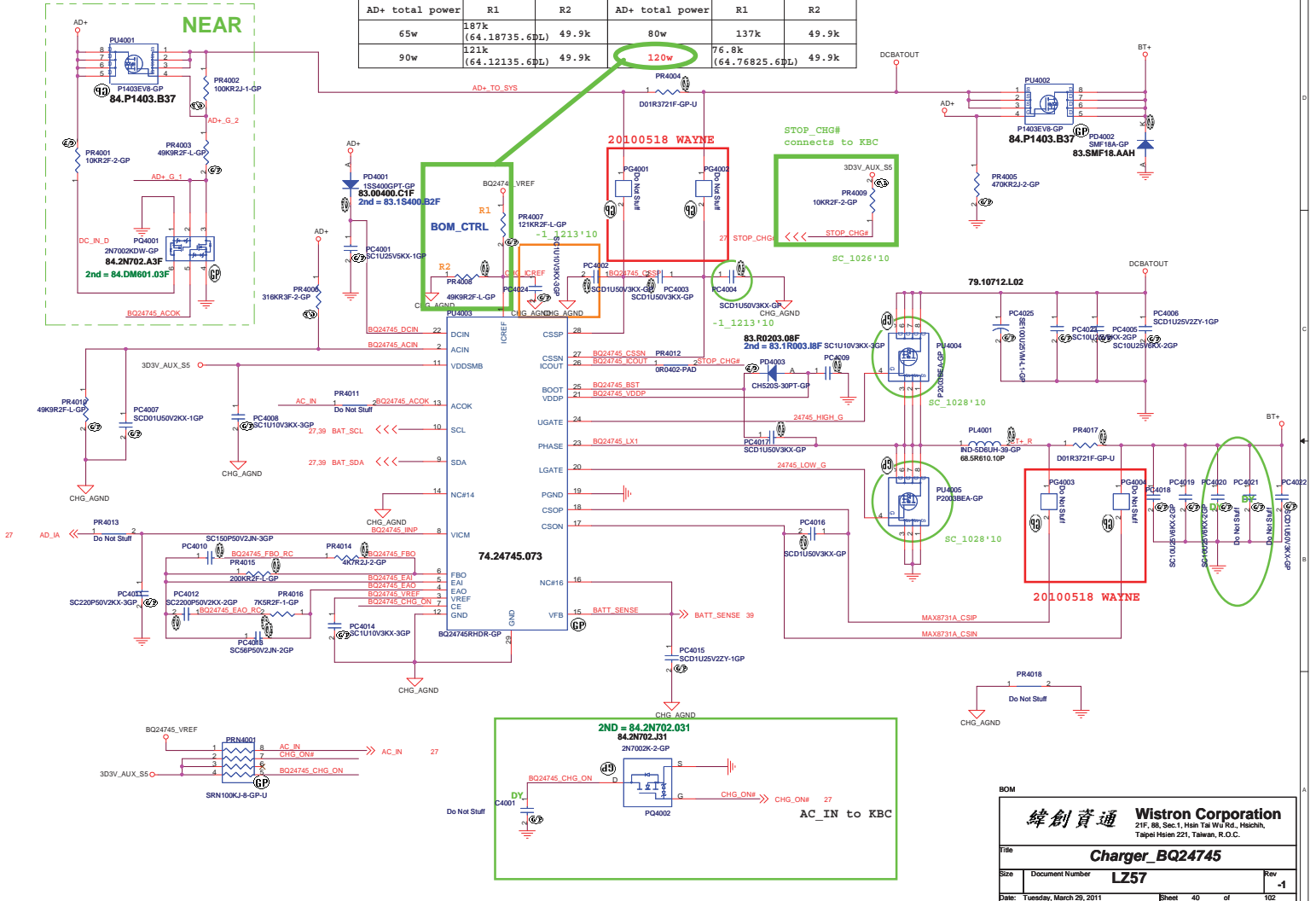
緯創資通 Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title DCIN_JACK	
Size	Document Number LZ57
Date: Tuesday, March 29, 2011	Rev -1
<small>Sheet 38 of 102</small>	



BOM

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k	120w	76.8k (64.76825.6DL)	49.9k



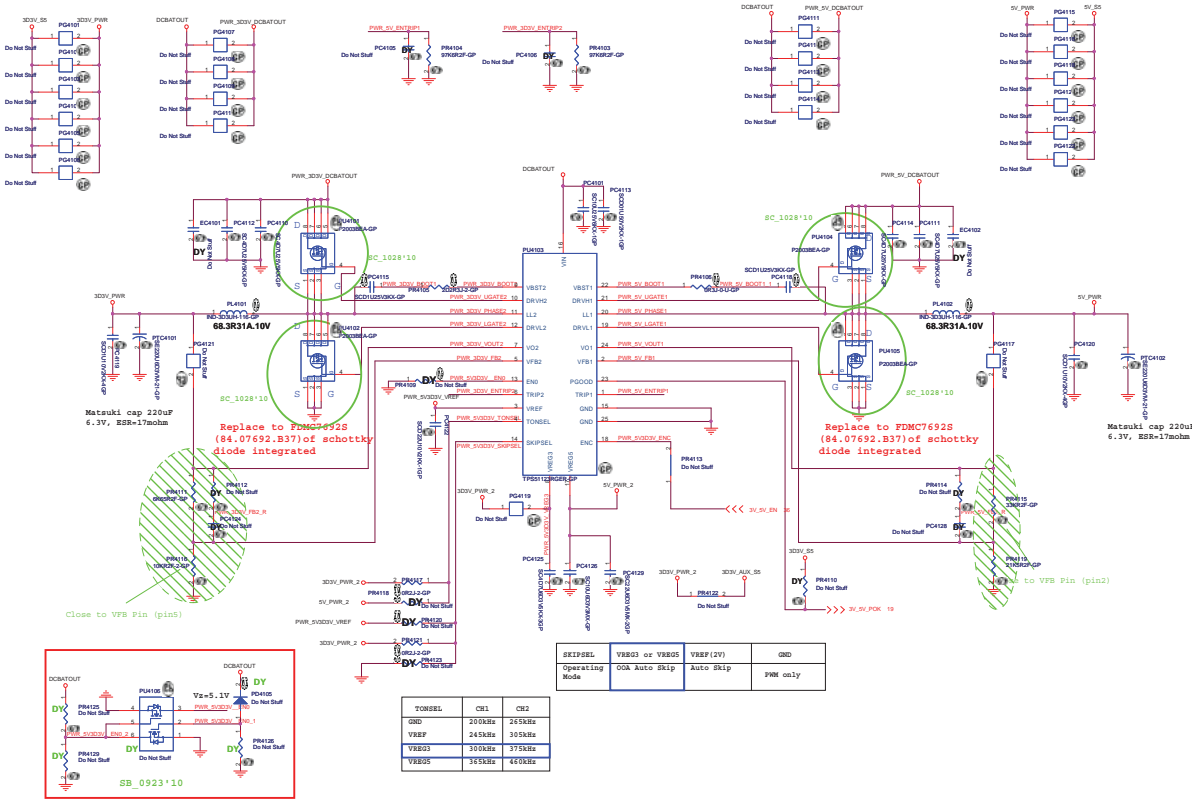
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsin 221, Taiwan, R.O.C.

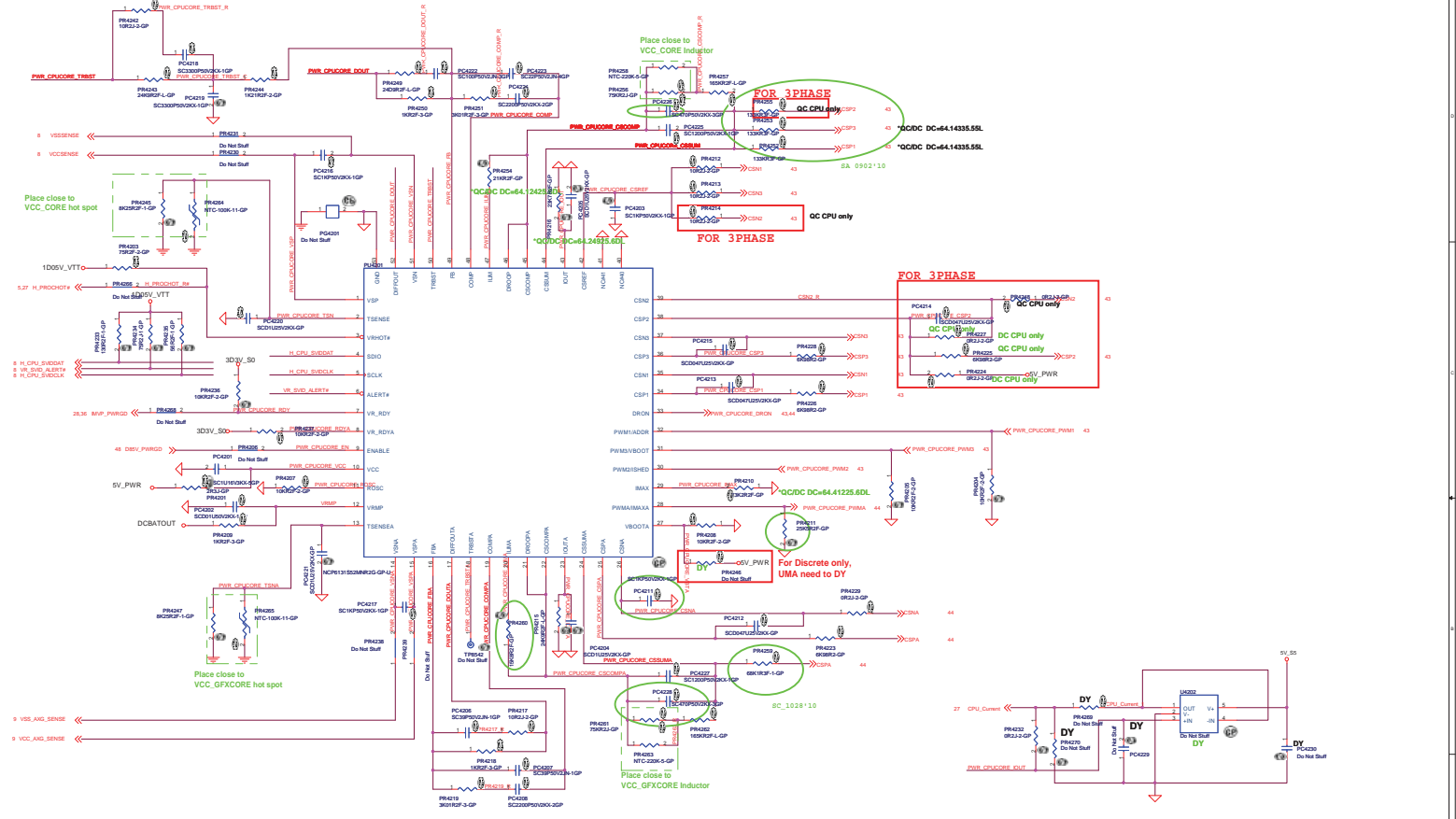
Charger_BQ24745

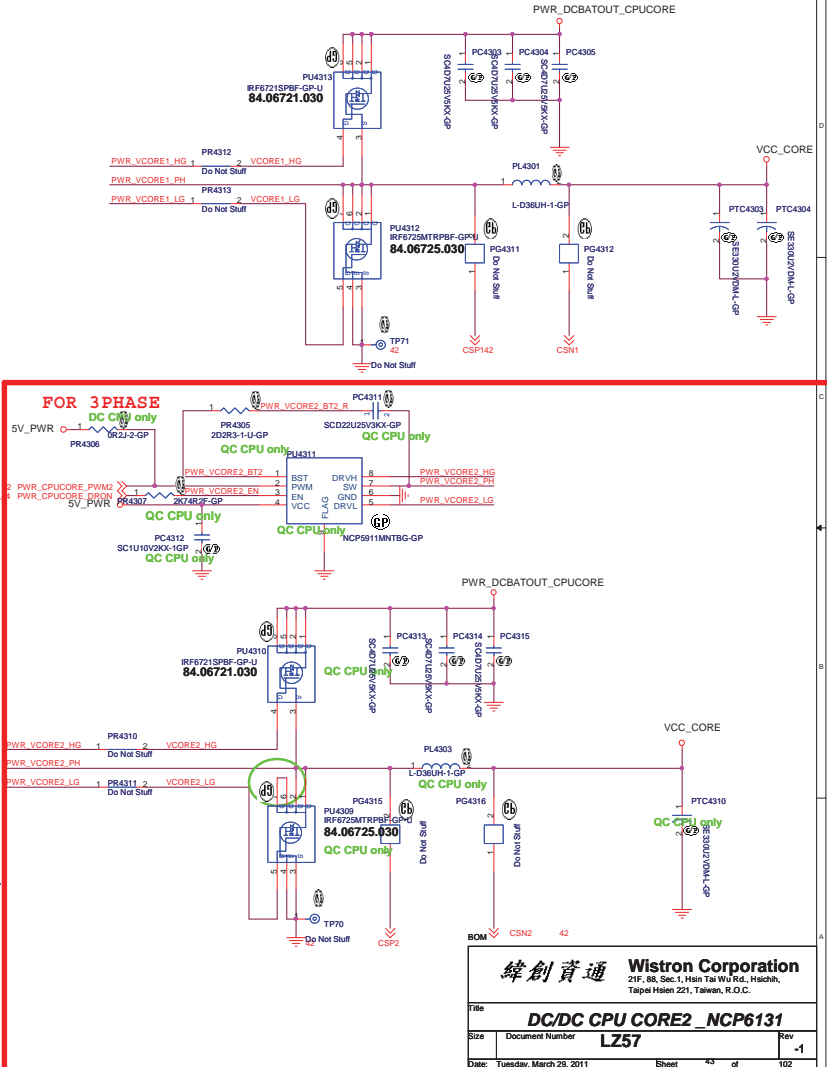
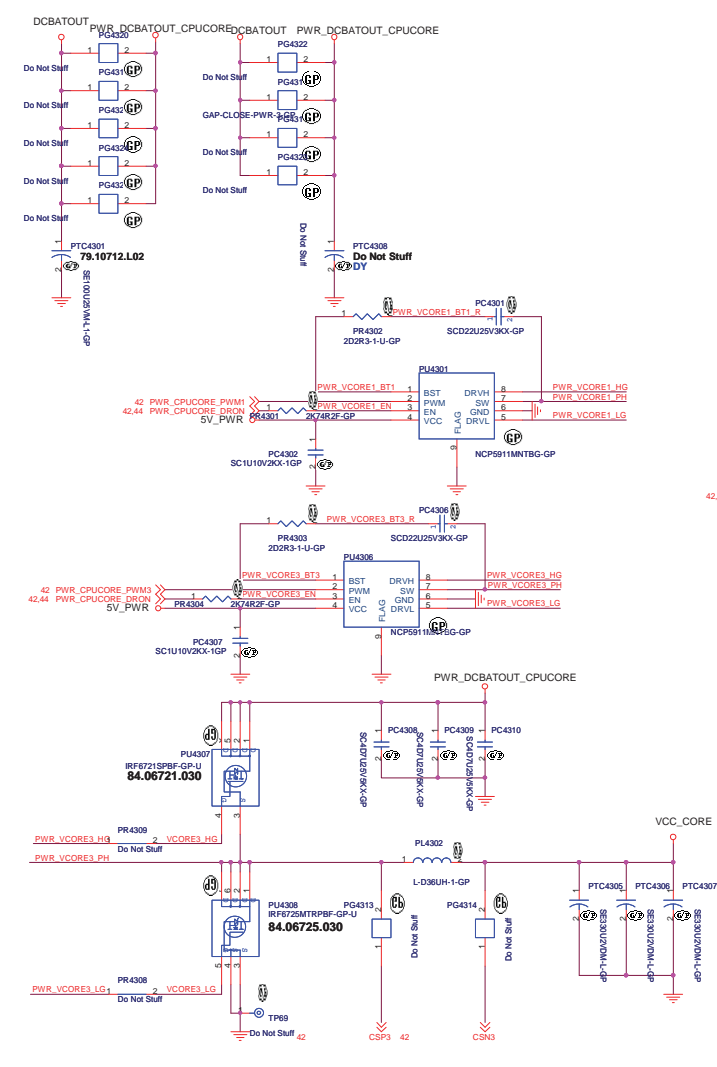
File: **LZ57**

Date: Tuesday, March 29, 2011 Sheet 40 of 102

SSID = PWR.Plane.Regulator_5v3p3v

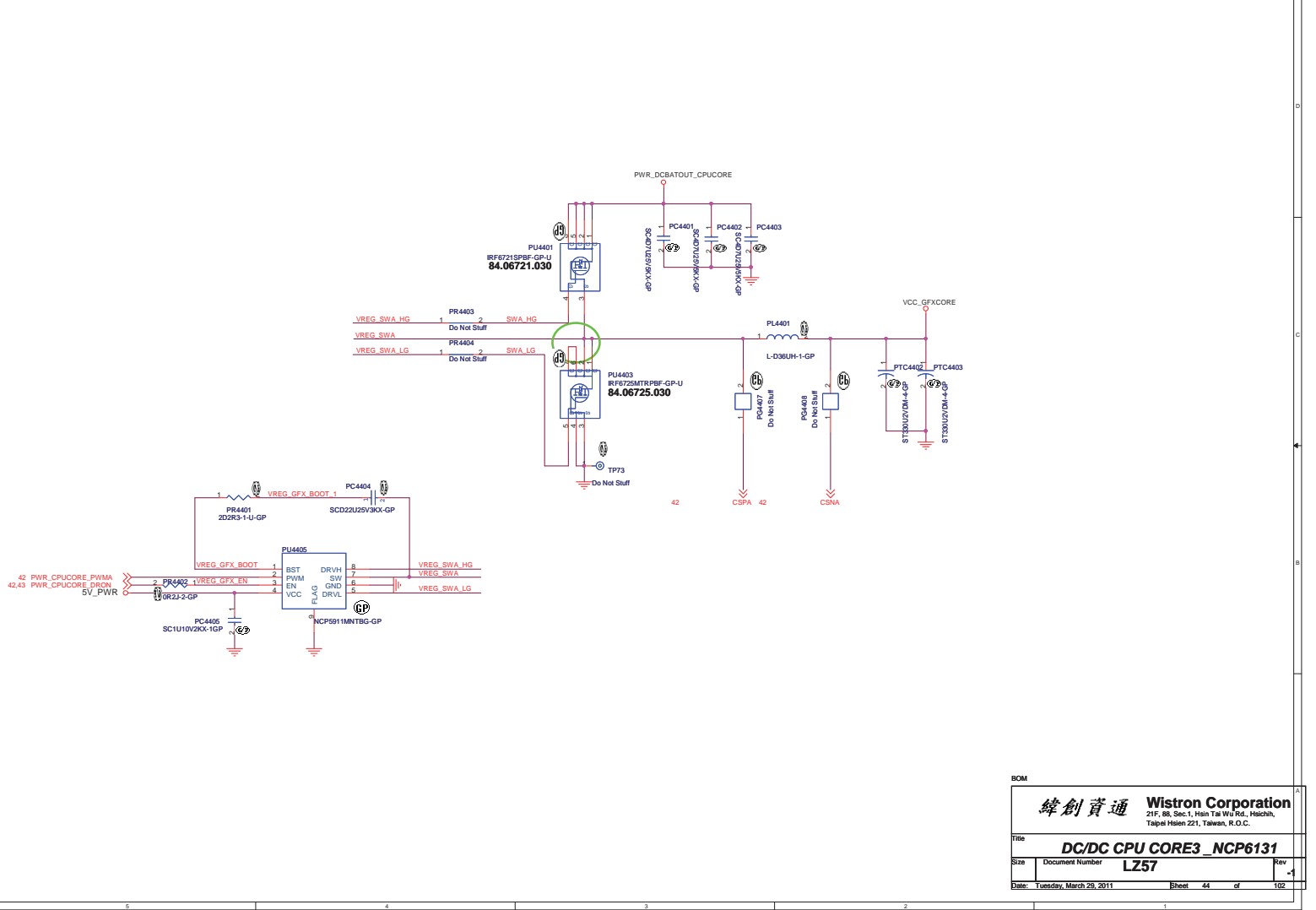






緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

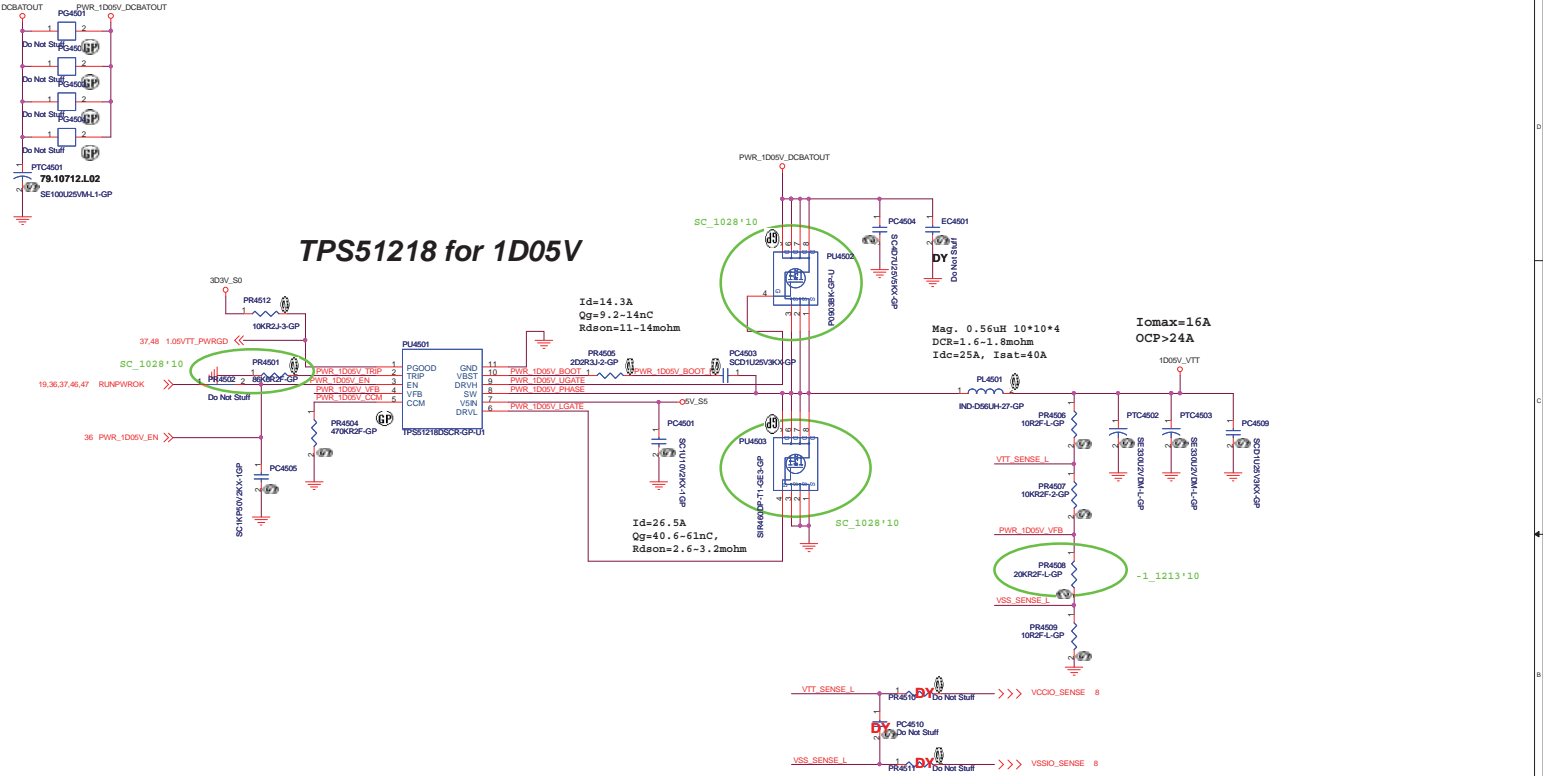
File	DC/DC CPU CORE2_NCP6131	
Size	Document Number	LZ57
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BCM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DC/DC CPU CORE3_NCP6131	
Size Document Number	Rev LZ57 1
Date Tuesday, March 29, 2011	Sheet 44 of 102

TPS51218 for 1D05V



$$V_{out} = 0.704V * (R1 + R2) / R2$$

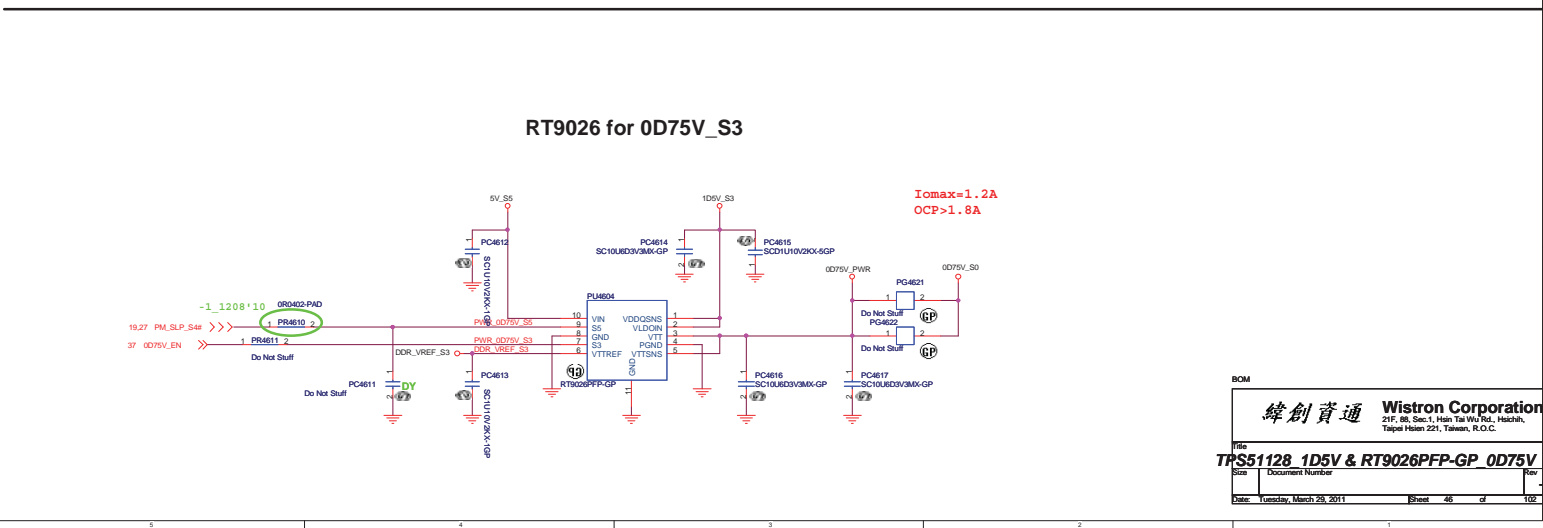
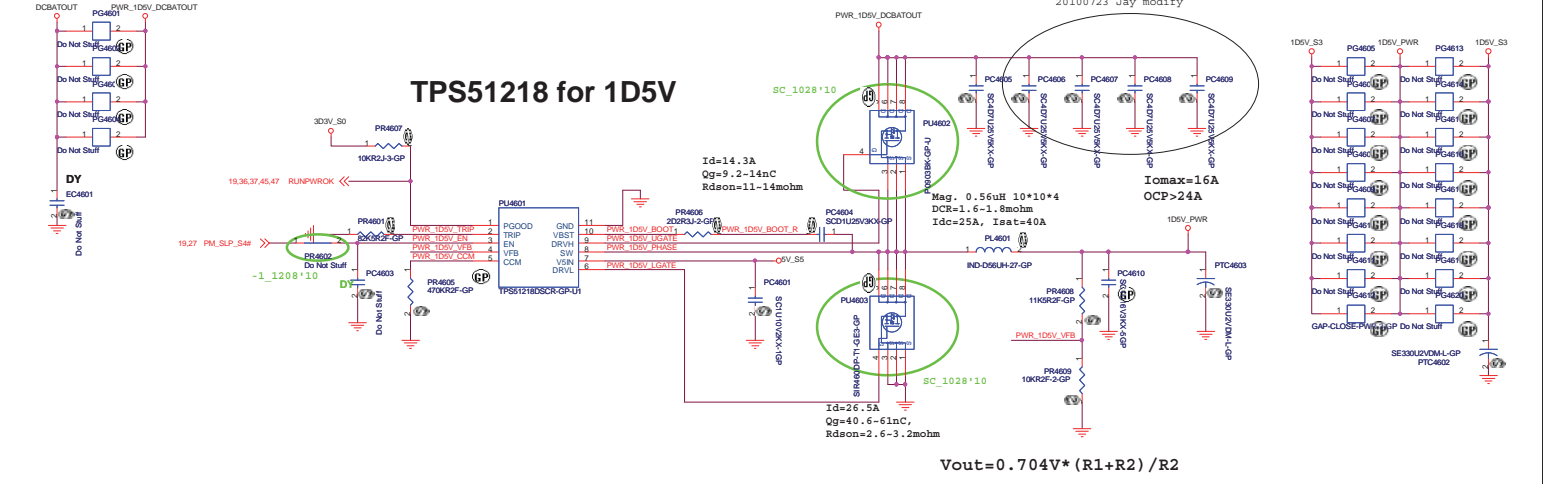
BCM

緯創資通 Wistron Corporation
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsein 221, Taiwan, R.O.C.

File: **TPS51218_1D05V**

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BCM

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

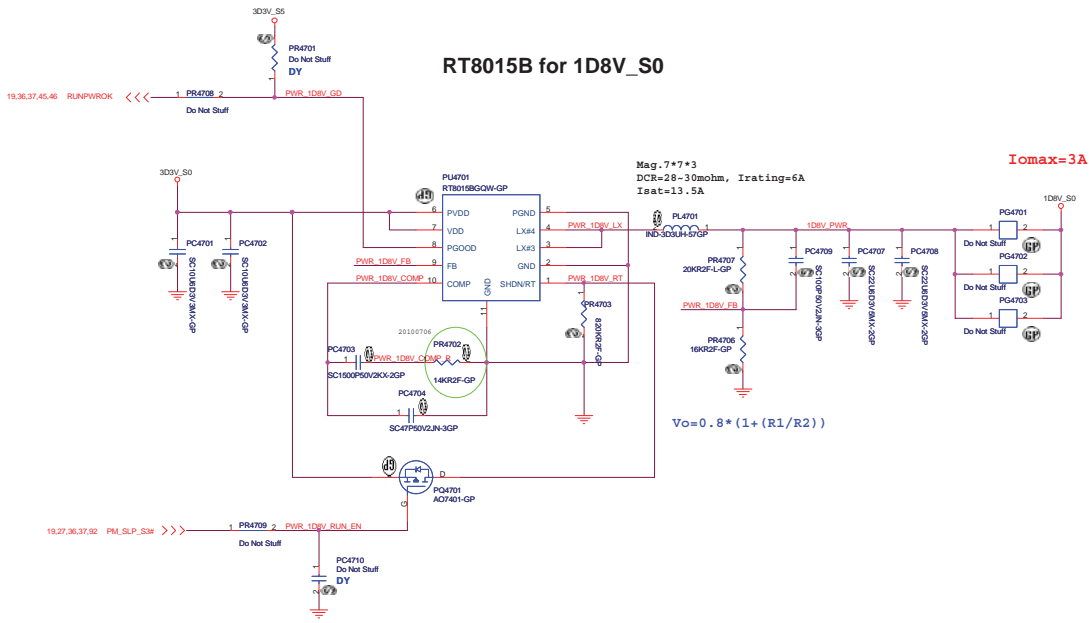
Title: **TPS51218 1D5V & RT9026PFP-GP 0D75V**

Rev: 1

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RT9025 for 1D8V_S0

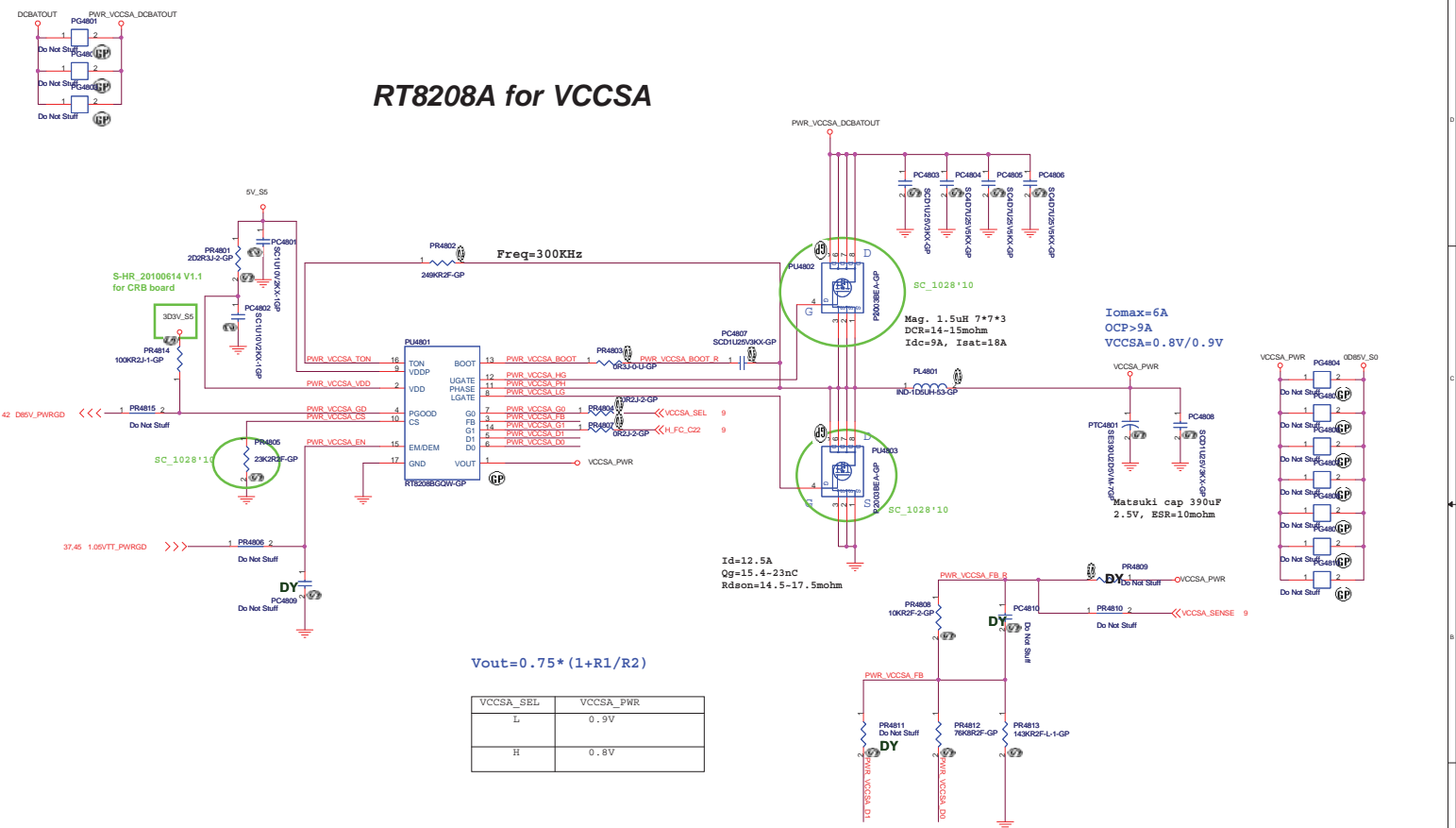
RT8015B for 1D8V_S0



BCM

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Rev: 1D8V_RT9025</p>	
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RT8208A for VCCSA



BCM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.

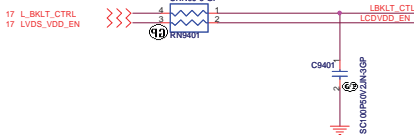
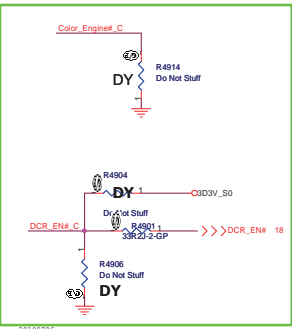
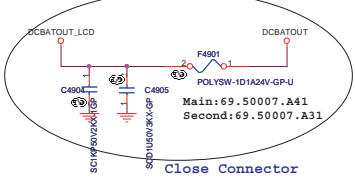
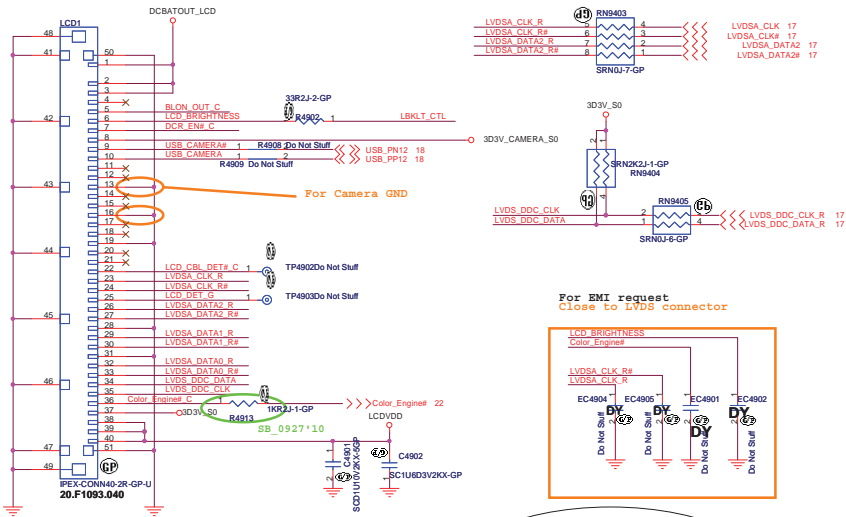
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Size: Document Number **LZ57** Rev: **-1**

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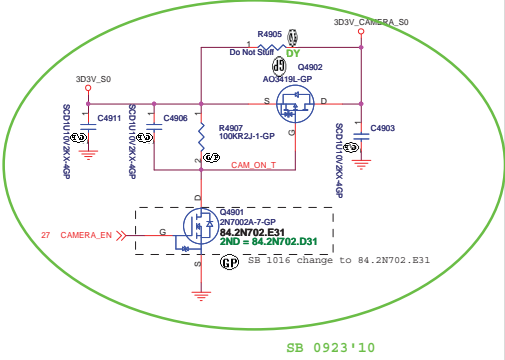
SSID = VIDEO

LVDS CONNECTOR

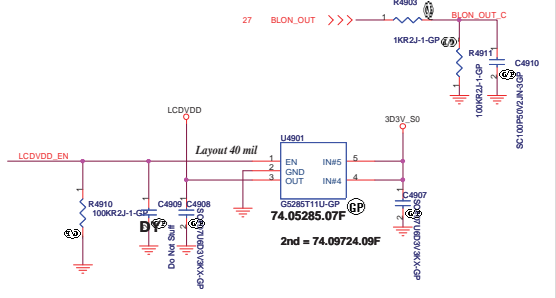


Panel BL brightness/Power En/BL En

CAMERA POWER

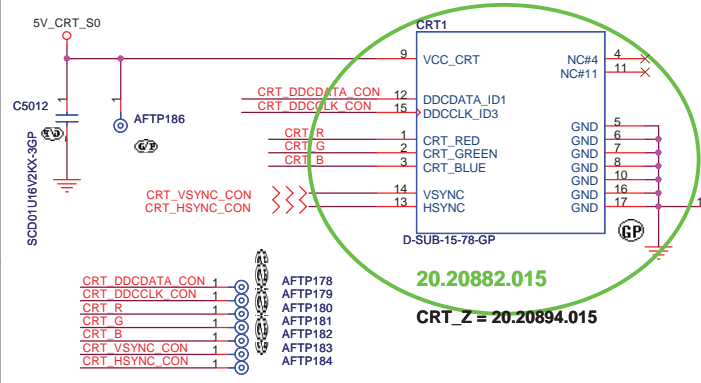


SSID = VIDEO



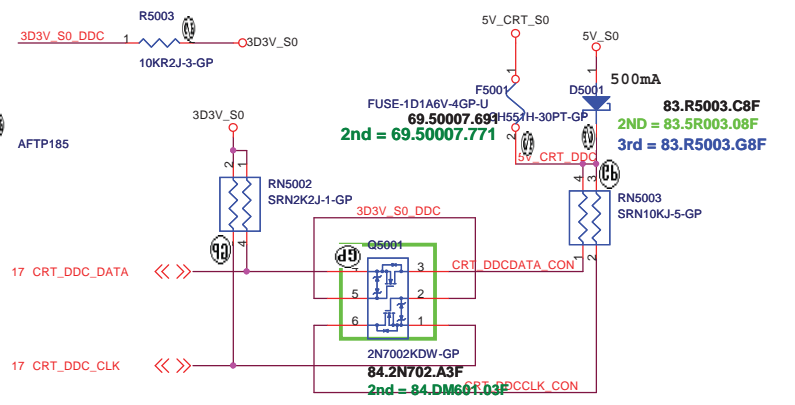
BOM

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien Z21, Taiwan, R.O.C.</p>		
<p>Title LCD Connector</p>		
<p>Size A3</p>	<p>Document Number LZ57</p>	<p>Rev -1</p>
<p>Date: 1/26/2011, March 29, 2011</p>	<p>Sheet 49</p>	<p>of 102</p>

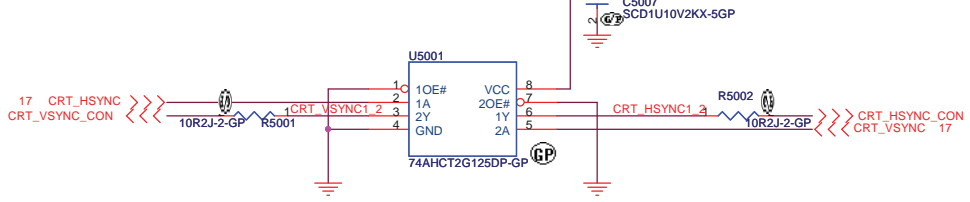


CRT DDCDATA & DDCCLK level shift

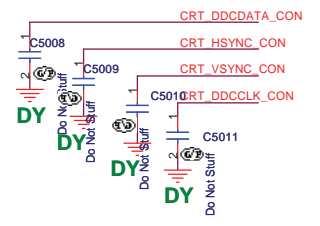
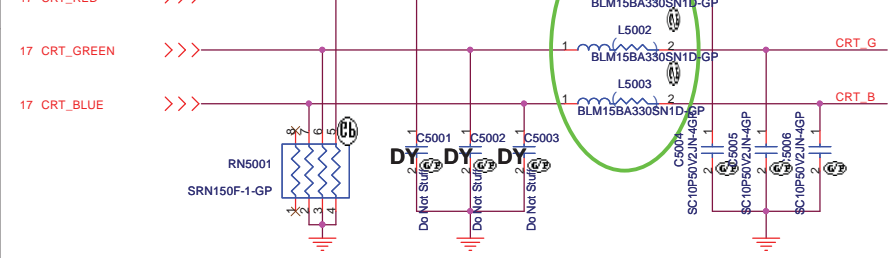
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift



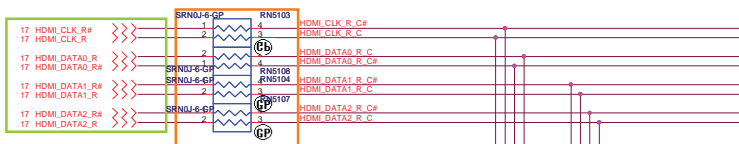
CRT RGB



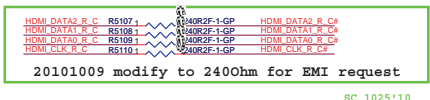
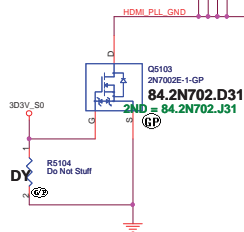
BOM

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CRT Connector		
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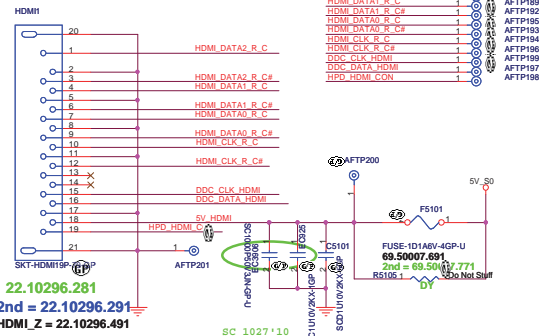
HDMI Passive Level Shifter



Close to HDMI Connector

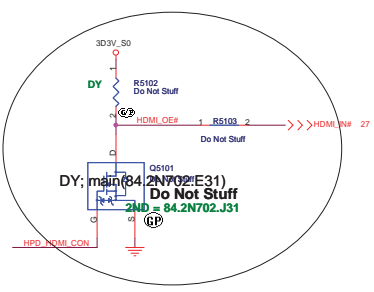


HDMI CONN

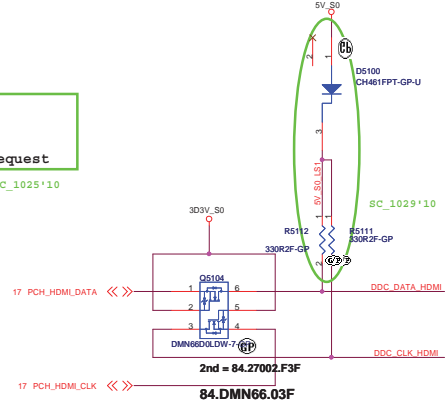
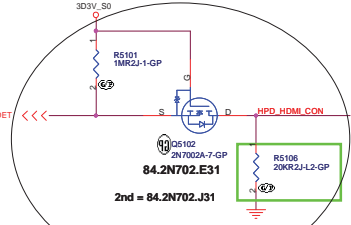


HDMI DDC Passive Level Shifter

20100727 modify, KBC isn't use.



20100727 follow intel design guide



BOM

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	HDMI Level Shifter/Connector
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BOM

緯創資通 Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title S-VIDEO	
Size A4	Document Number LZ57
Date: Tuesday, March 29, 2011	Rev -1
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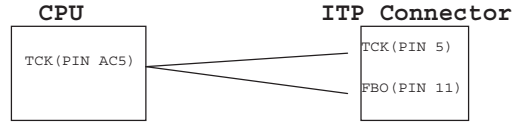
BOM

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

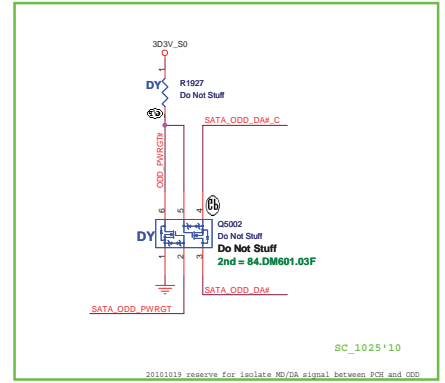
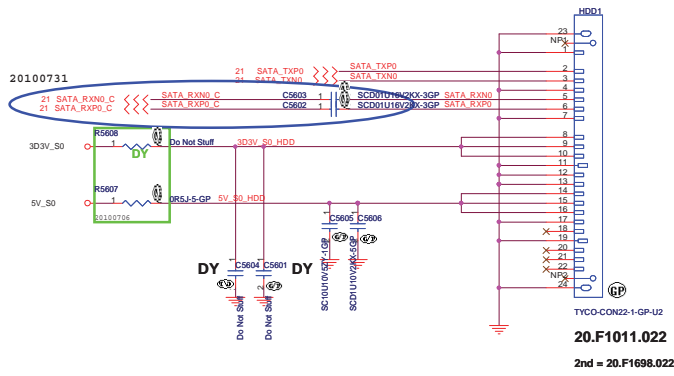


BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ITP		
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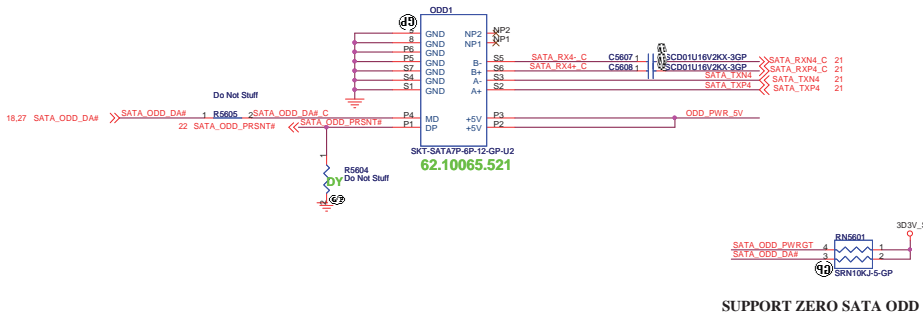
SSID = SATA

SATA HDD Connector

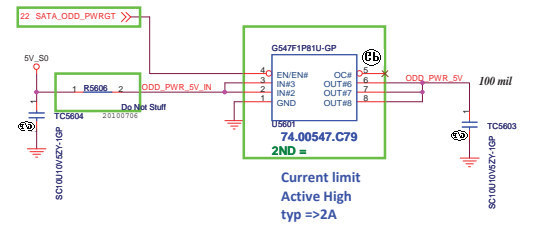


ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil
Mars:
Exchange ODD and ESATA differential pair each other.



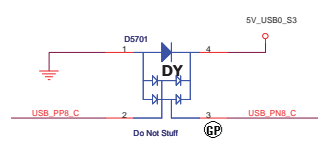
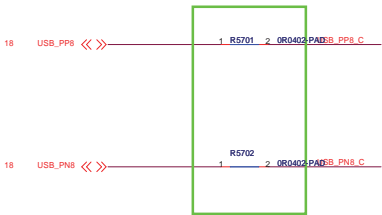
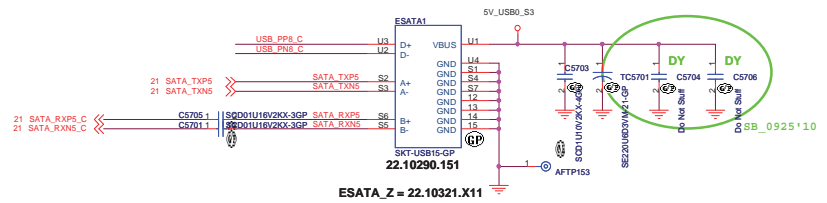
SATA Zero Power ODD



BOB

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Mian Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD	
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- USB_PN8_C 1 AFTP147
- USB_PP8_C 1 AFTP146
- SATA_TXNS 1 AFTP146
- SATA_TXPS 1 AFTP152
- SATA_RXNS 1 AFTP151
- SATA_RXPS 1 AFTP150
- 5V_USB0_S3 1 AFTP150

BOM

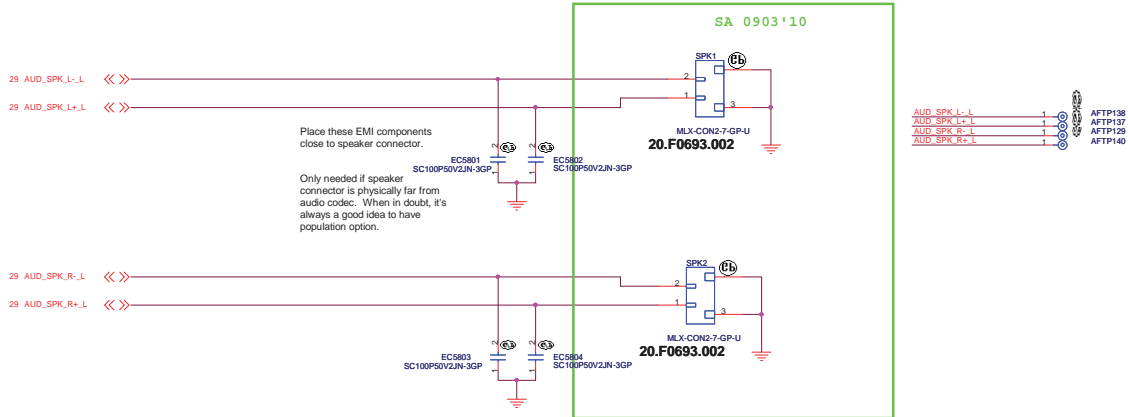
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **E-SATA/LUSB**

Size: A3 Document Number: **LZ57** Rev: **-1**

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INTERNAL STEREO SPEAKERS



BOB

緯創資通		Wistron Corporation	
<small>217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.</small>			
MIC/SPEAKER/AUDIO JACK			
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Reserved

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

Document Number

LZ57

Date

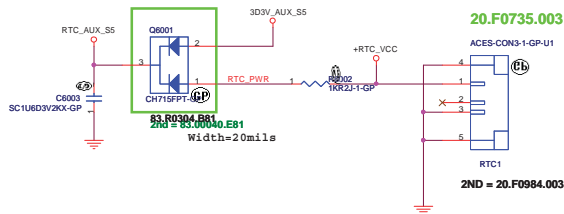
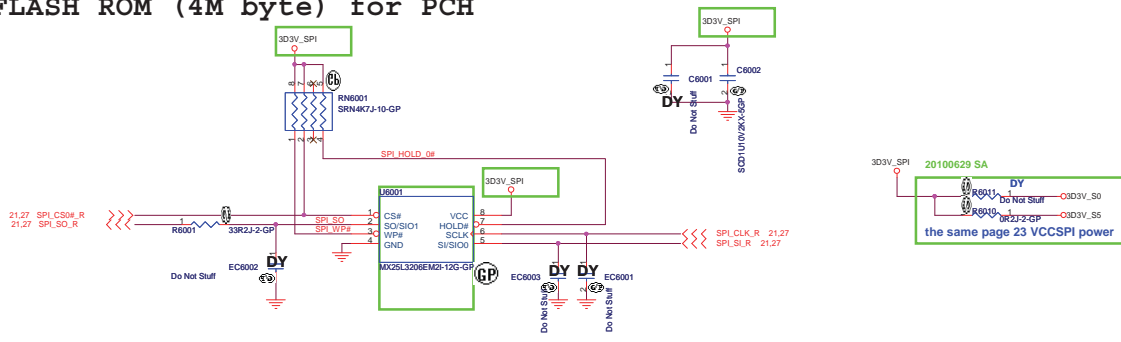
Tuesday, March 25, 2014

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Rev

-1

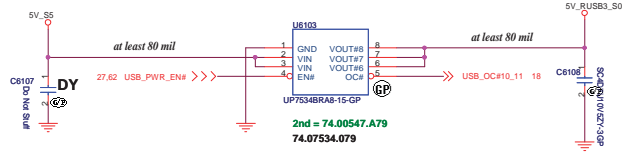
SPI FLASH ROM (4M byte) for PCH



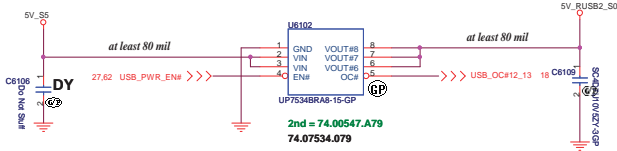
BOM

緯創資通 Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Flash/RTC	
Size: A3	Document Number: LZ57
Date: 1/8/2009, March 29, 2011	Rev: -1
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RJ45_USB Board USB Power



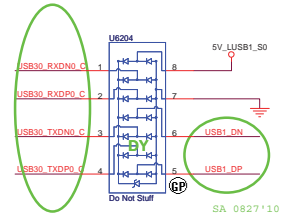
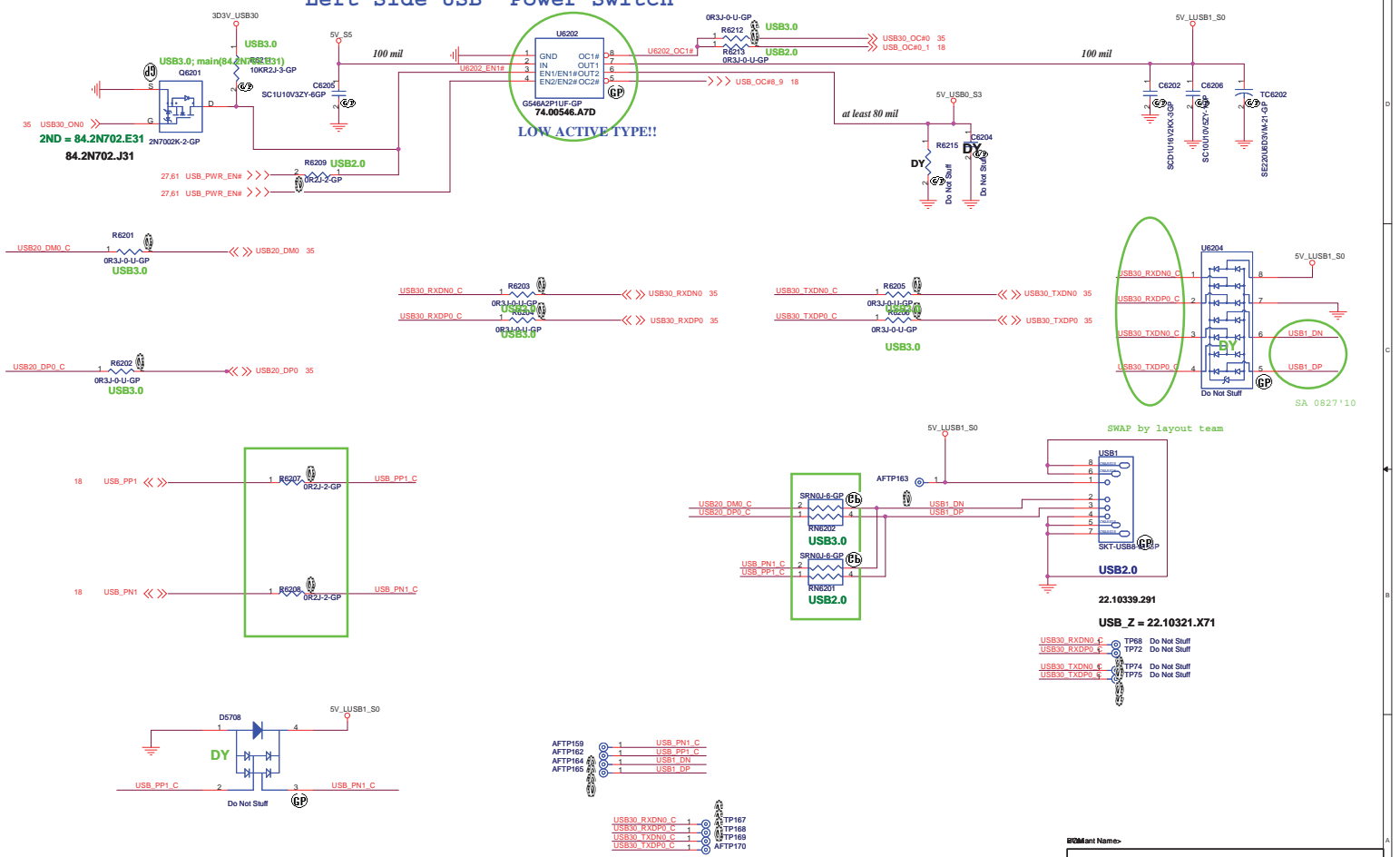
I/O Board USB Power



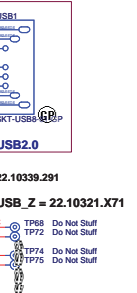
BOM

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
USB Power SW	
Size A3	Document Number LZ57
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Left Side USB Power Switch



SWAP by layout team



- USB_Z = 22.10331.X71
- USB30_RXD#0_C TP68 Do Not Stuff
 - USB30_RXDP#0_C TP72 Do Not Stuff
 - USB30_TXD#0_C TP74 Do Not Stuff
 - USB30_TXDP#0_C TP75 Do Not Stuff

- AFTP158 1 USB_PN1_C
- AFTP162 1 USB_PP1_C
- AFTP164 1 USB1_DN
- AFTP165 1 USB1_DP

- USB30_RXD#0_C 1 AFTP167
- USB30_RXDP#0_C 1 AFTP168
- USB30_TXD#0_C 1 AFTP169
- USB30_TXDP#0_C 1 AFTP170

Wistron Corporation
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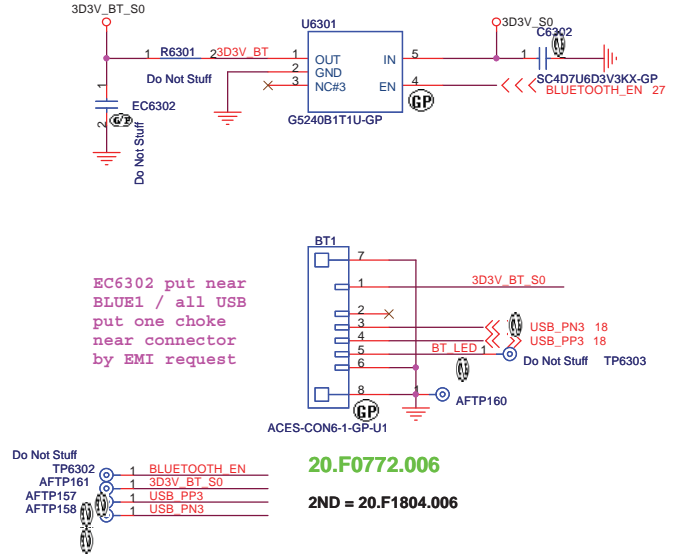
File: **USB 2.0/3.0 Port**

Size: K3 Document Number: **LZ57** Rev: **-1**

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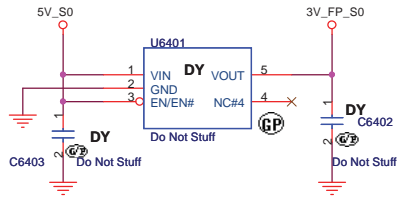
SSID = User.Interface
Bluetooth Module conn.

Bluetooth Module



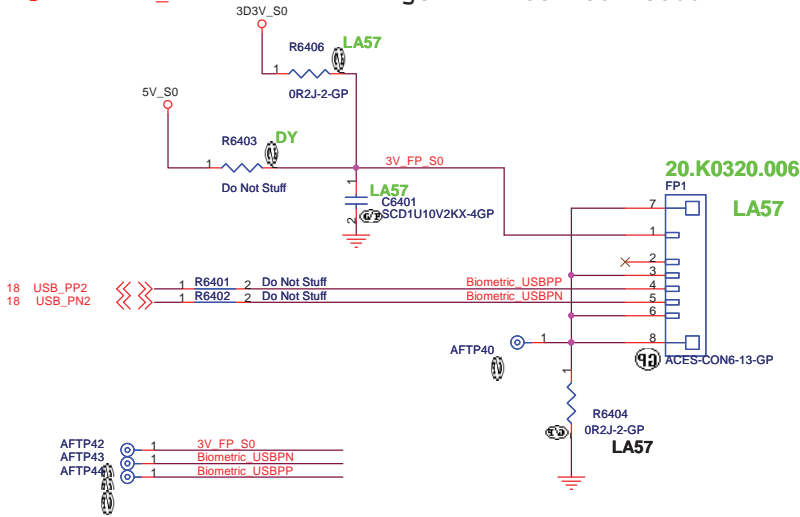
BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Bluetooth			
Size	Document Number	Rev	
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LA47 change to 3D3V_S0

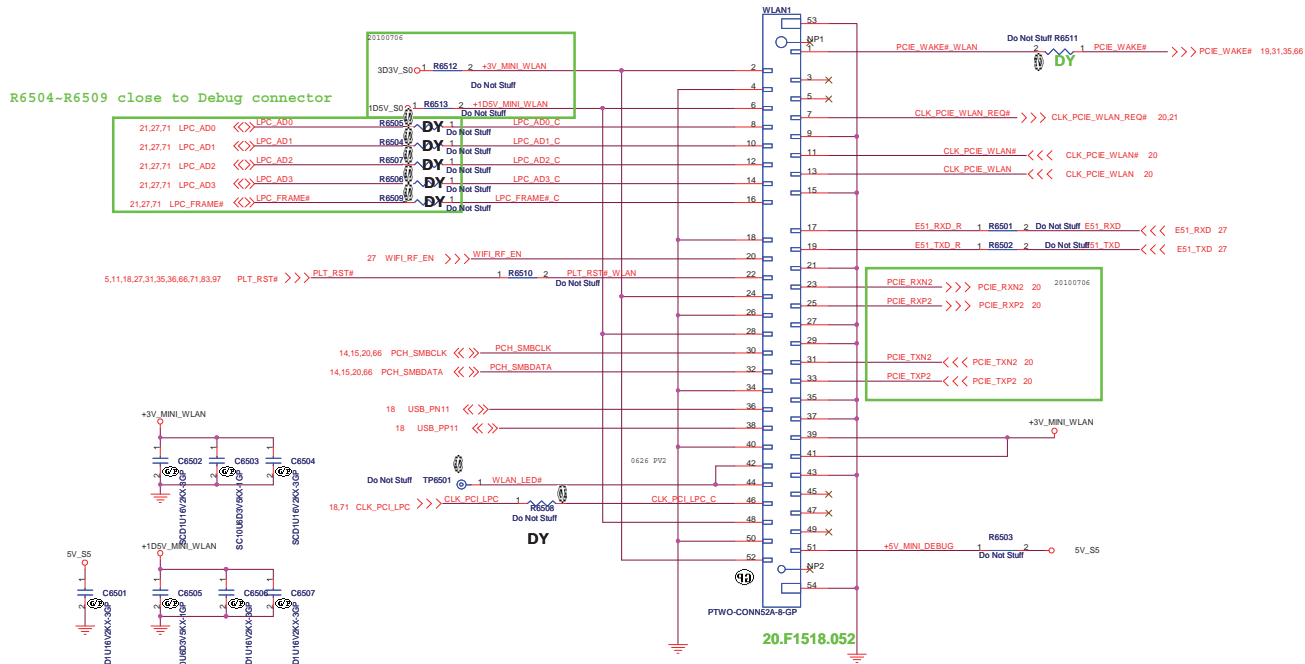
Finger Printer Connector



BOM

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
RESERVED		
Size A4	Document Number LZ57	Rev -1
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Mini Card Connector(802.11a/b/g/n)



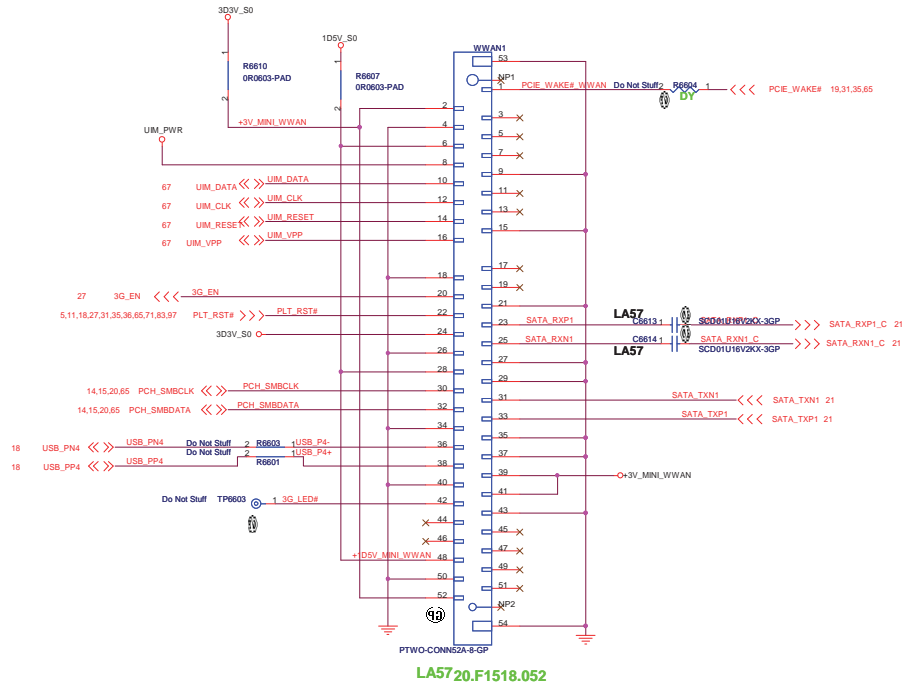
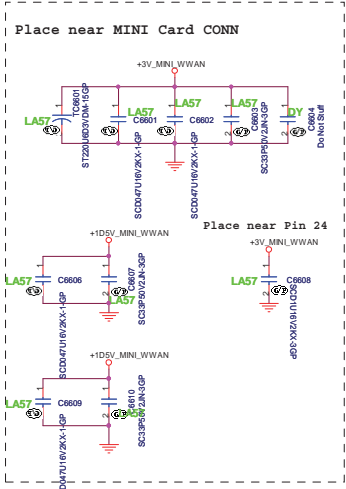
R6504-R6509 close to Debug connector

20.F1518.052

BOM

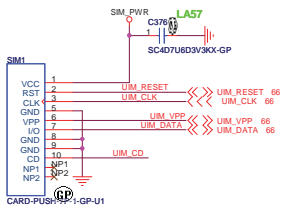
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	MINICARD(WLAN)/TTP CONN
Size	Document Number
LZ57	
Date	Thursday, March 29, 2012
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Mini Card Connector(WWAN)

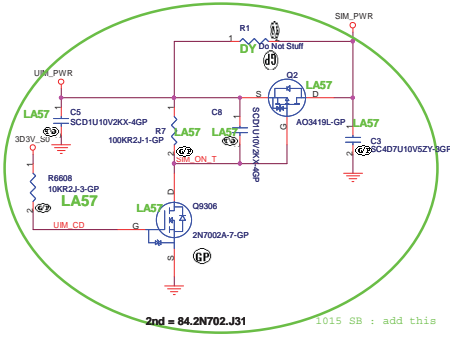


BOM

緯創資通 Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.</small>	
File	WWAN Connector
Size A3	LZ57
Date: 1080509_Maron 29, 2011	Sheet 68 of 102
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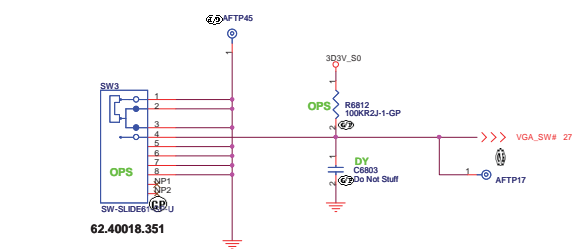


LA57
20.10073.001



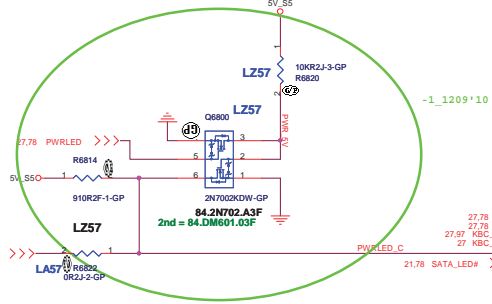
2nd = 84.2N702.J31
1015 SB : add this
84.2N702.E31

BOM	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	
SIM CARD	
Size A3	Document Number
LZ57	
Date: Tuesday, March 29, 2011	Rev -1
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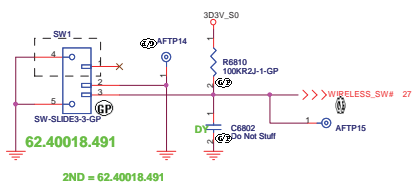


62.40018.351

Power button LED (White)

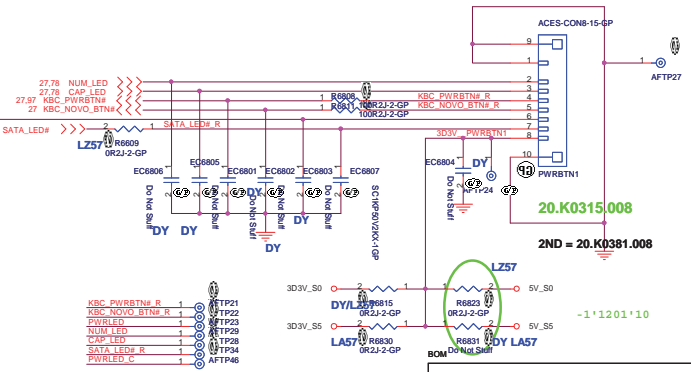


-1_1209'10



62.40018.491

2ND = 62.40018.491



- KBC_PWRBTN#_R 1 AFTP21
- KBC_NOVO_BTN#_R 1 AFTP22
- PWRLED 1 AFTP23
- NUM_LED 1 AFTP29
- CAP_LED 1 AFTP30
- SATA_LED#_R 1 AFTP34
- PWRLED_C 1 AFTP46

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsein 221, Taiwan, R.O.C.

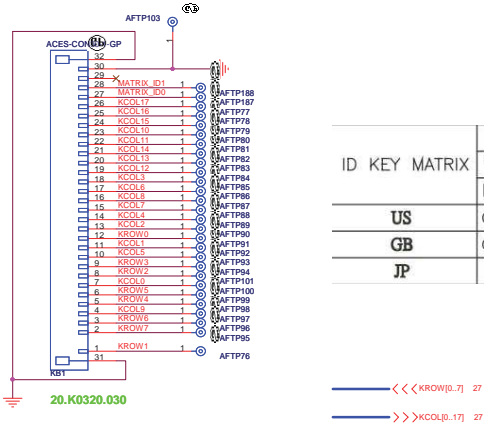
File: **LED Bard/Power Button**

Size: A3 Document Number: **LZ57** Rev: **-1**

Date: (Issued), March 29, 2011 Sheet: 68 of 102

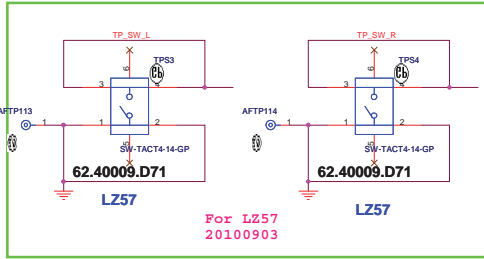
SSID = KBC

Internal Keyboard Connector

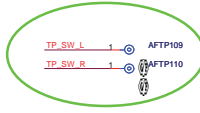


ID KEY MATRIX	SENSE			
	27	28	29	30
US	ID0	ID1	ID2	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

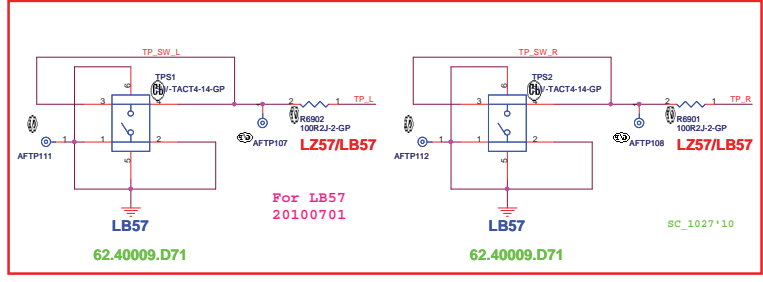
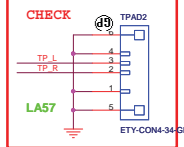
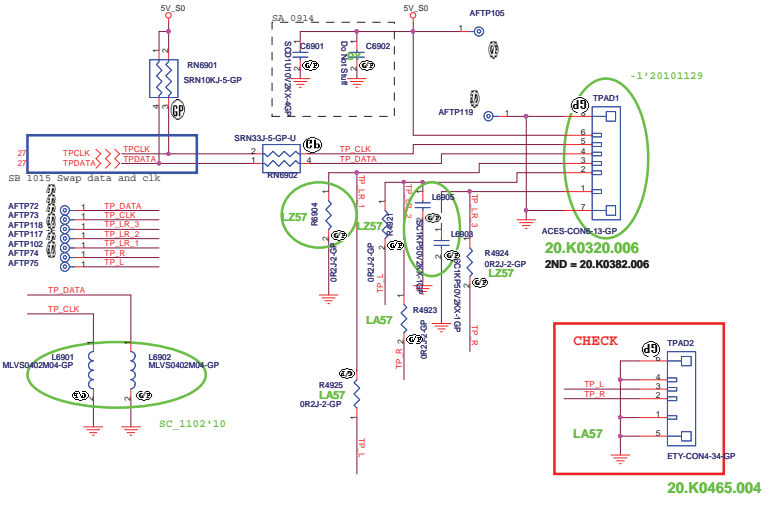
<< KROW[0..7] 27
>> KCOL[0..17] 27



For LZ57
20100903



SSID = Touch.Pad



For LB57
20100701

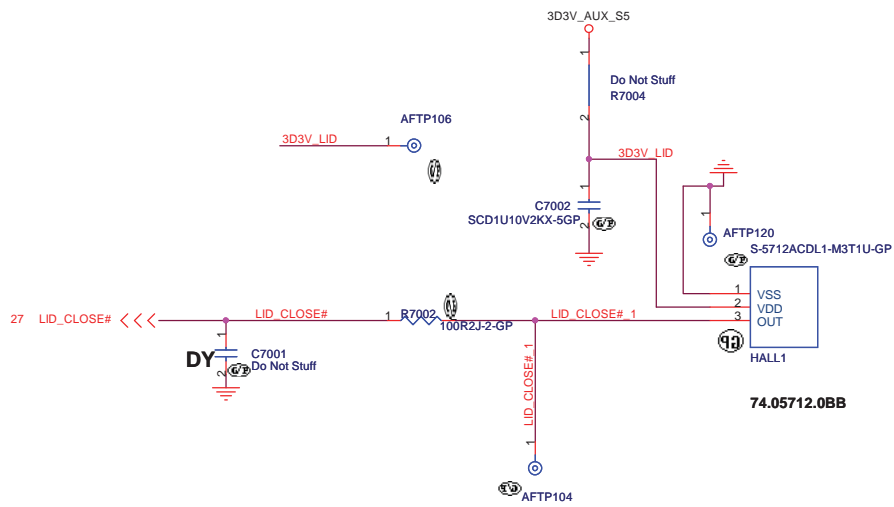
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

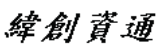
Size: A3 Document Number: **LZ57** Rev: **-1**

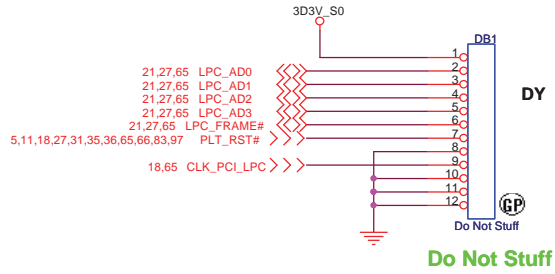
Date: Tuesday, March 28, 2011 Sheet: 69 of 102



74.05712.0BB

BOM

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Hall Sensor		
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BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <i>Dubug connector</i>		
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BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

Document Number

Rev

A4

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-1

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102

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Title Reserved		
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CARD Reader CONN	
Size A4	Document Number LZ57
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D

D

C

C

B

B

A

A

BOM

緯創資通 Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title New Card	
Size A4	Document Number LZ57
Date: Tuesday, March 29, 2011	
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BOM

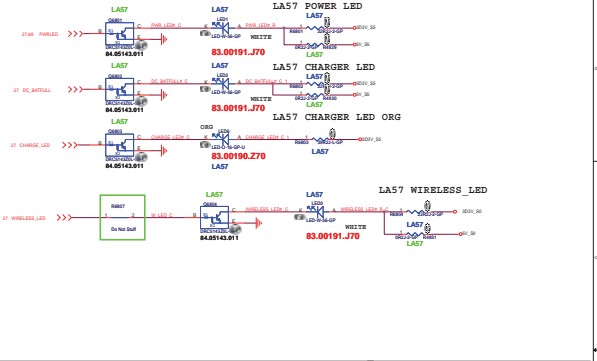
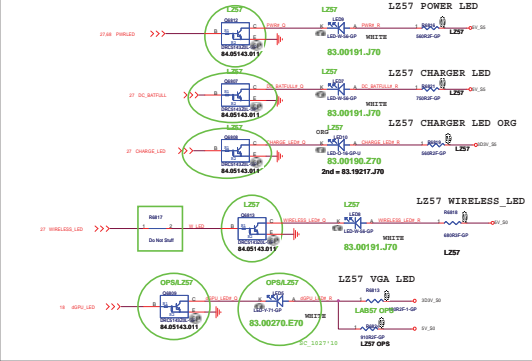
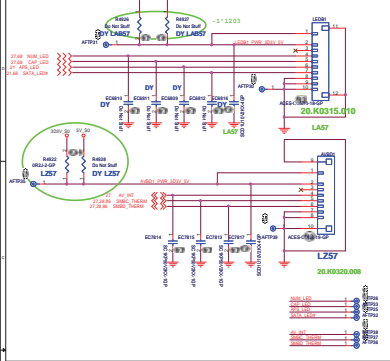
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Title Reserved		
Size A4	Document Number LZ57	Rev -1
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BOM

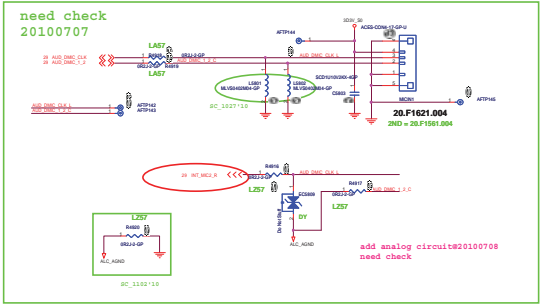
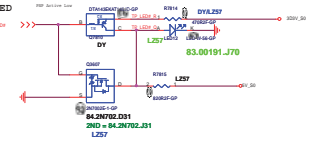
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
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LED Board CONN.

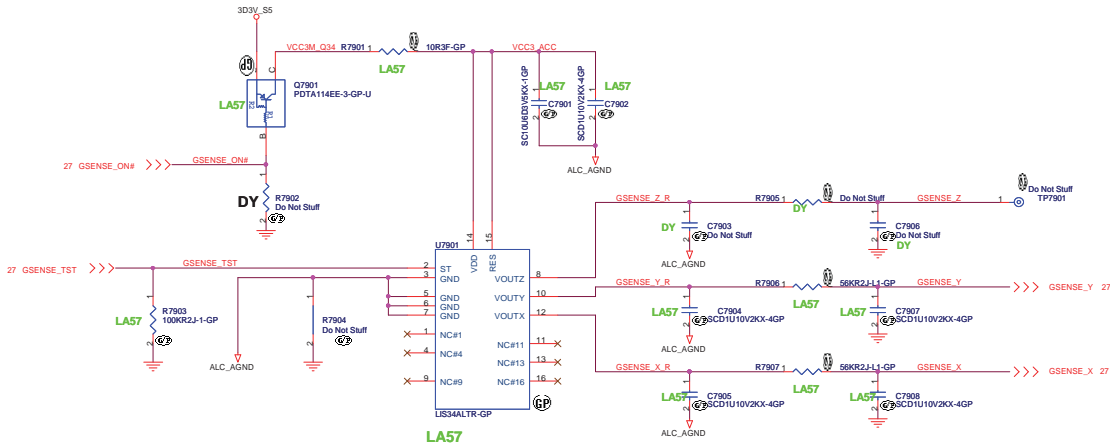


LZ57 => Analog Mic => Add analog circuit.
 LA57 => Digital Mic

LZ57 Touch Pad LED



G-Sensor

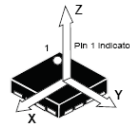


STMicro LIS34AL: 74.00034.0BZ
 ADXL335 : 74.00335.0BZ

	ADXL322	
	LIS244AL	No Accel
	LIS34AL	
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.



BOM

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
File			
		G-Sensor	
Size Custom		Document Number	Rev
		LZ57	-1
Date: 1080509_Miron 29, 2011	Sheet 79	of	102

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BOM

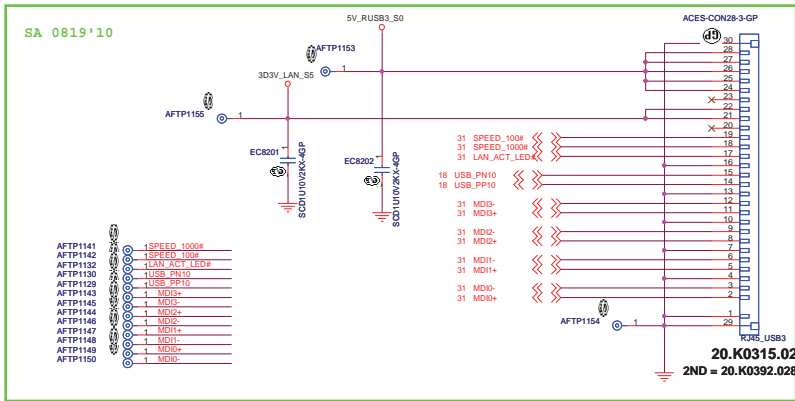
緯創資通 Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		
Reserved		
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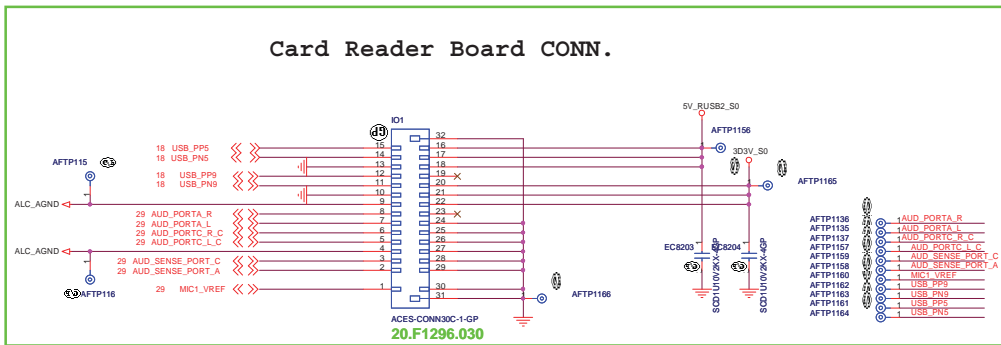
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
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RJ45_USB CONN.

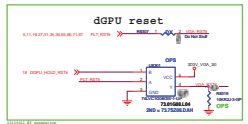
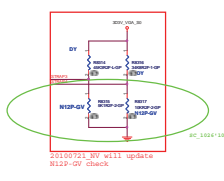
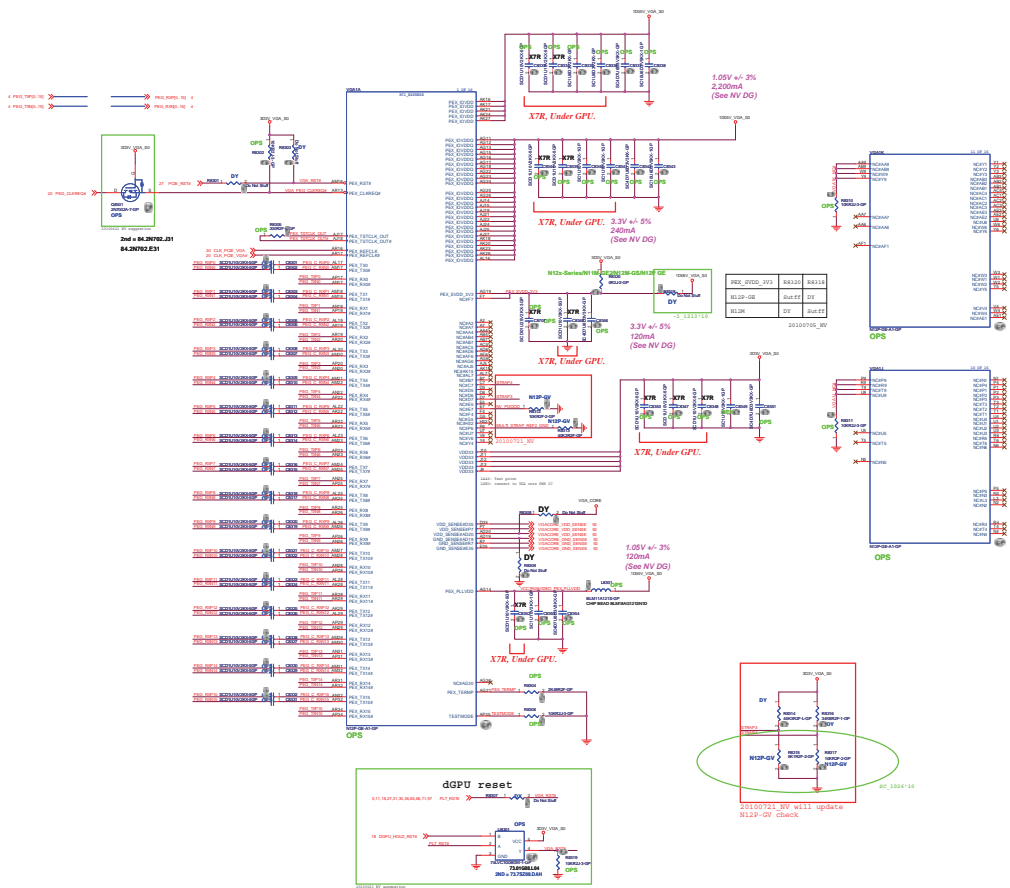


Card Reader Board CONN.

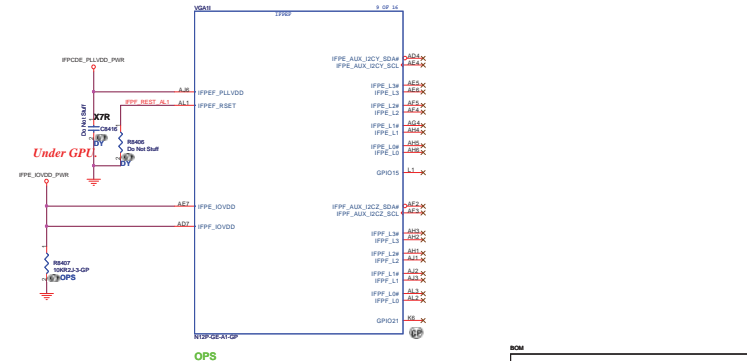
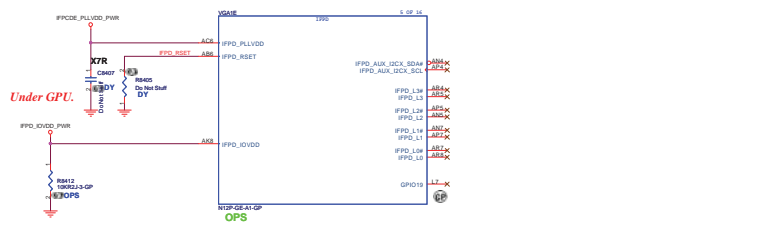
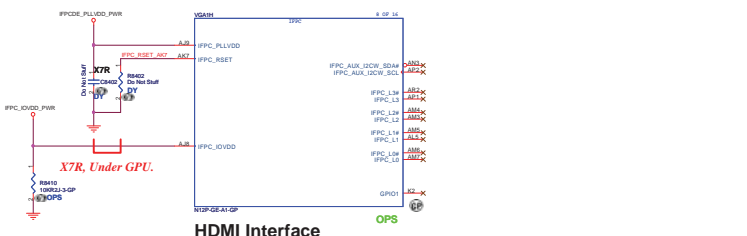
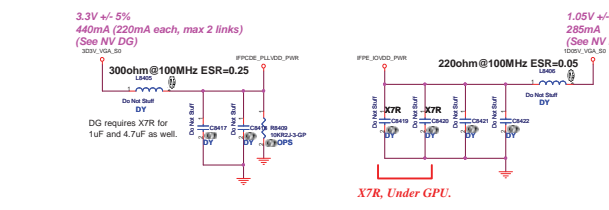
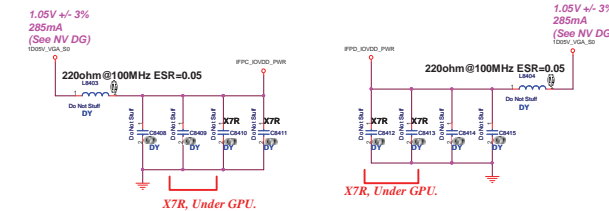
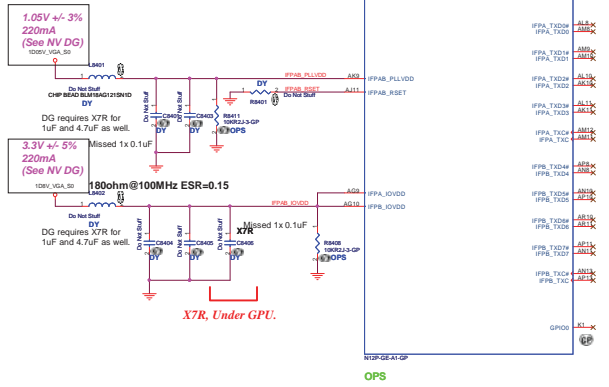


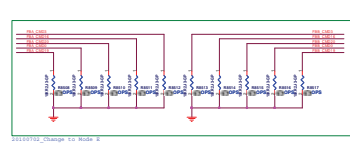
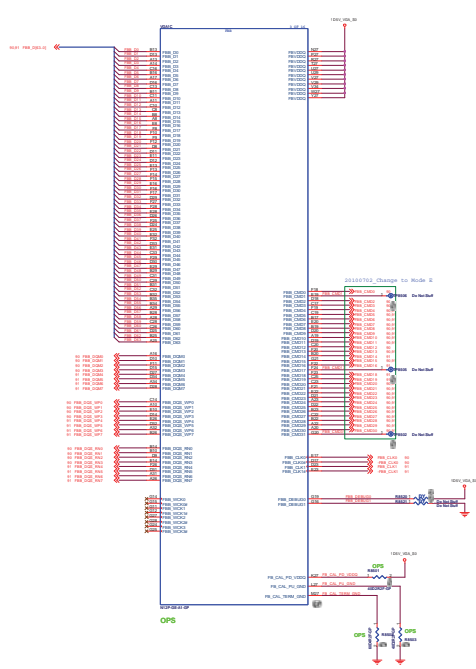
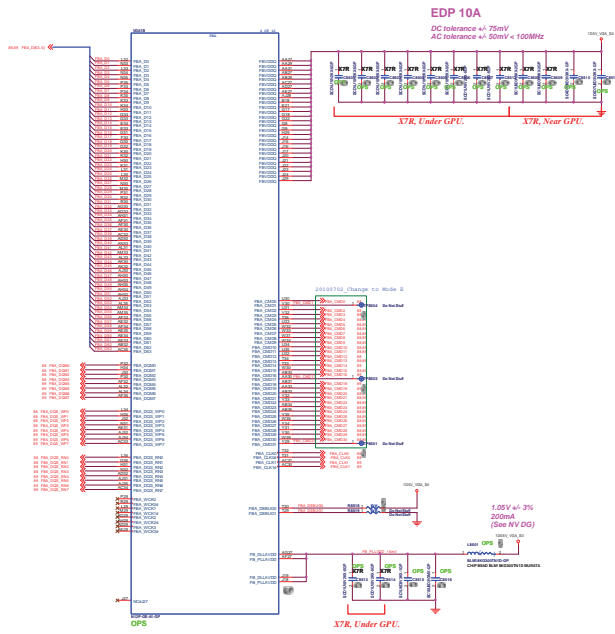
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緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
File	IO Board Connector
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LVDS Interface





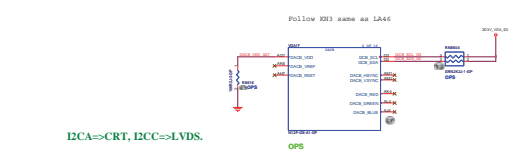
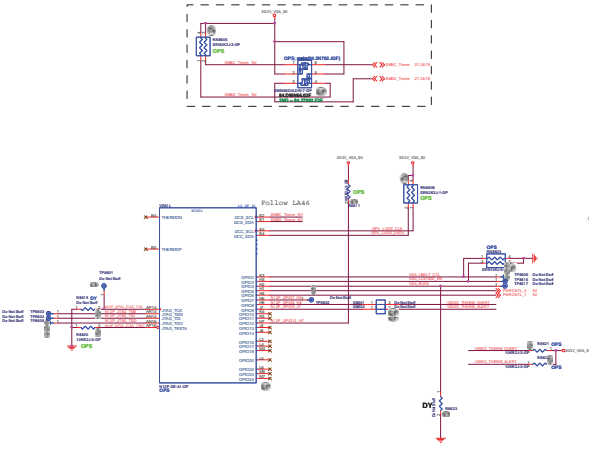
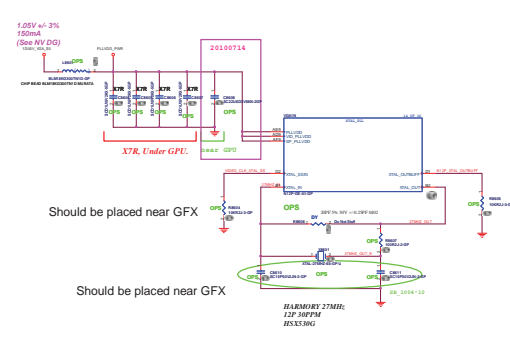
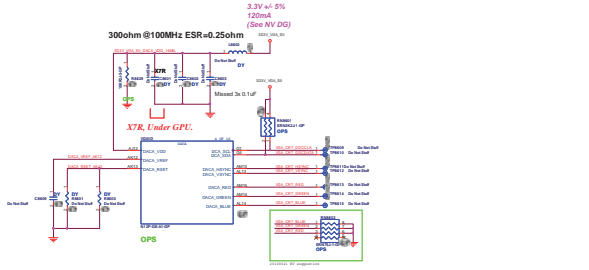
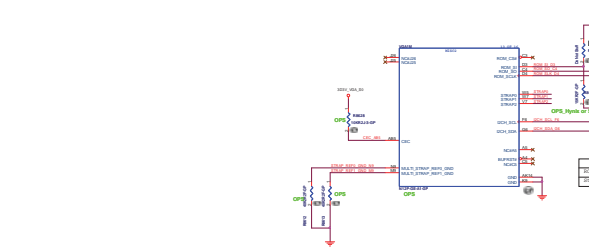
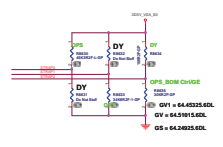


TABLE VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
	72.52G63.00U 72.52G63.10U	72.42164.C0U 72.42164.D0U	72.51G63.C0U	72.41164.H0U
ROM_SI	34.8Kohm	45.3Kohm	15Kohm	20Kohm
PD	64.34825.6DL	64.45325.6DL	64.15025.6DL	64.20025.6DL

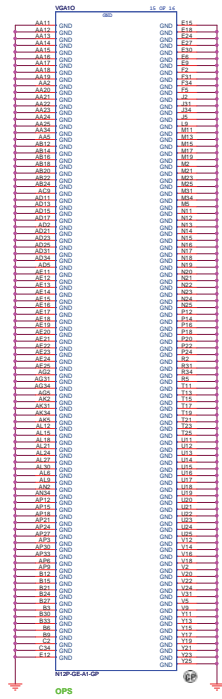
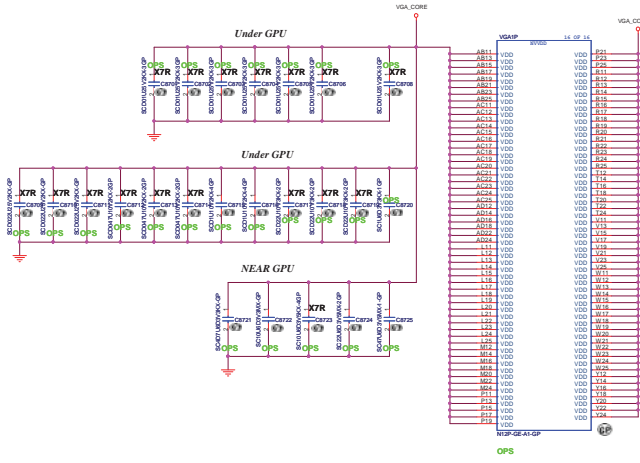


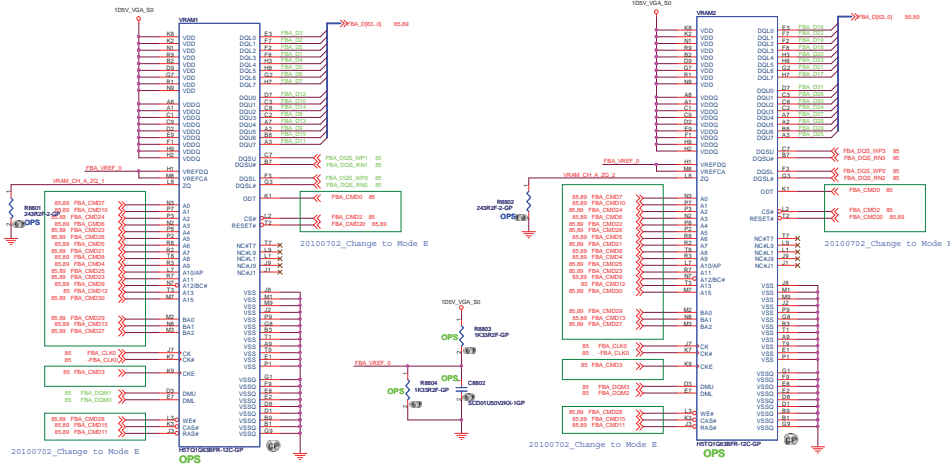
LOGIC

	N12P-GE DEV ID: 0xDEF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

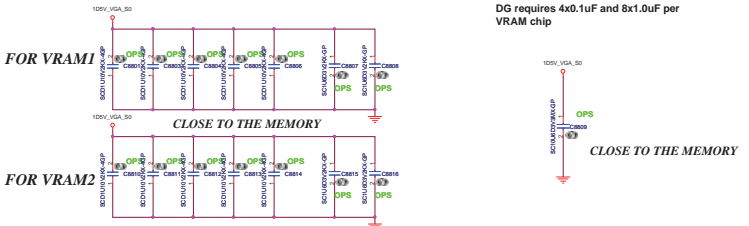
LOGIC

**EDP 50A
(TDP 37W)**



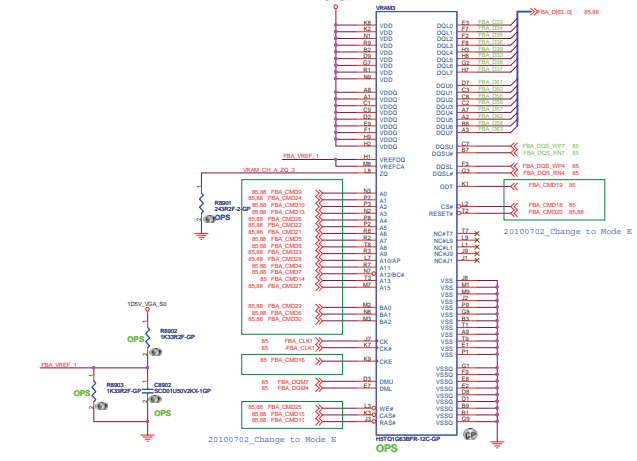


FB CMD mapping Mode D-N12x

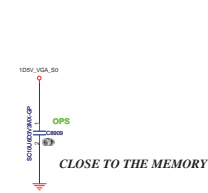
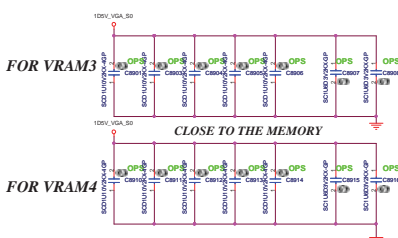
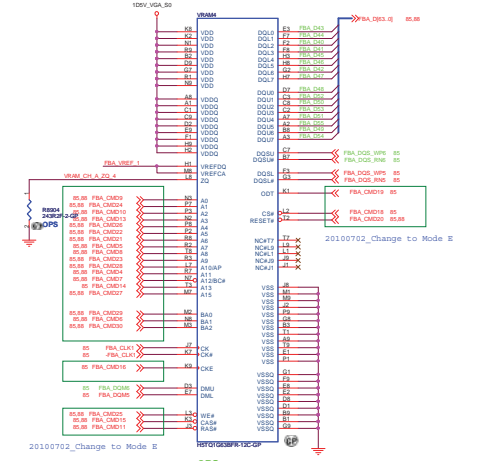


VIDEO FRAME BUFFER PORT A

Wistron Corporation <small>2/F, No. 56, T. Hsin, Ta Hsueh Rd., Taipei, Taiwan, R.O.C.</small>	
VRAM CHANNEL-A	
Doc. No.	Document Number
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Doc. Date	Version: March 28, 2011
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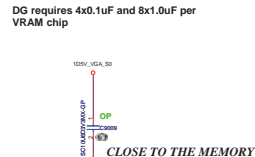
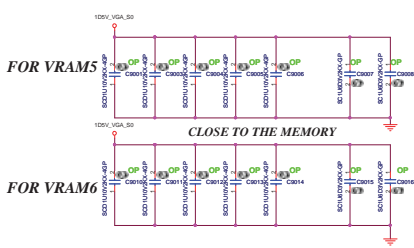
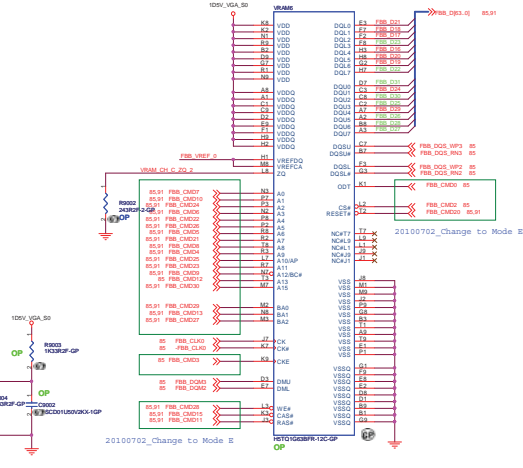
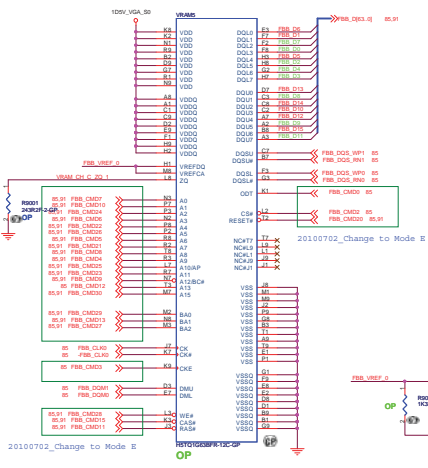


FB CMD mapping Mode D-N12x



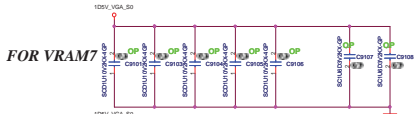
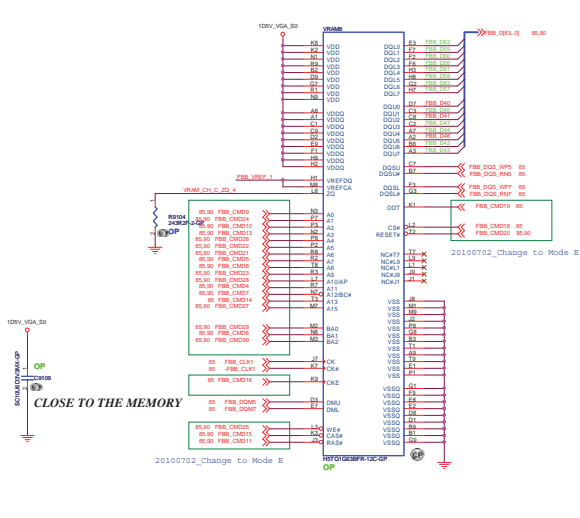
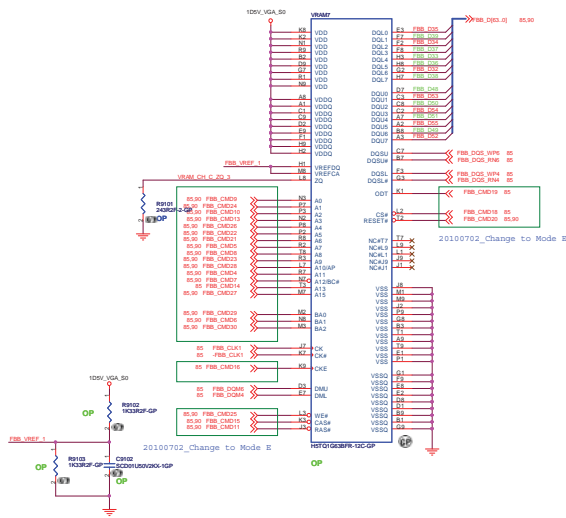
VIDEO FRAME BUFFER PORT A

VRAM CHANNEL-A	
Doc. No.	LZ57
Rev.	1
Date	2011.03.29



VIDEO FRAME BUFFER PORT C

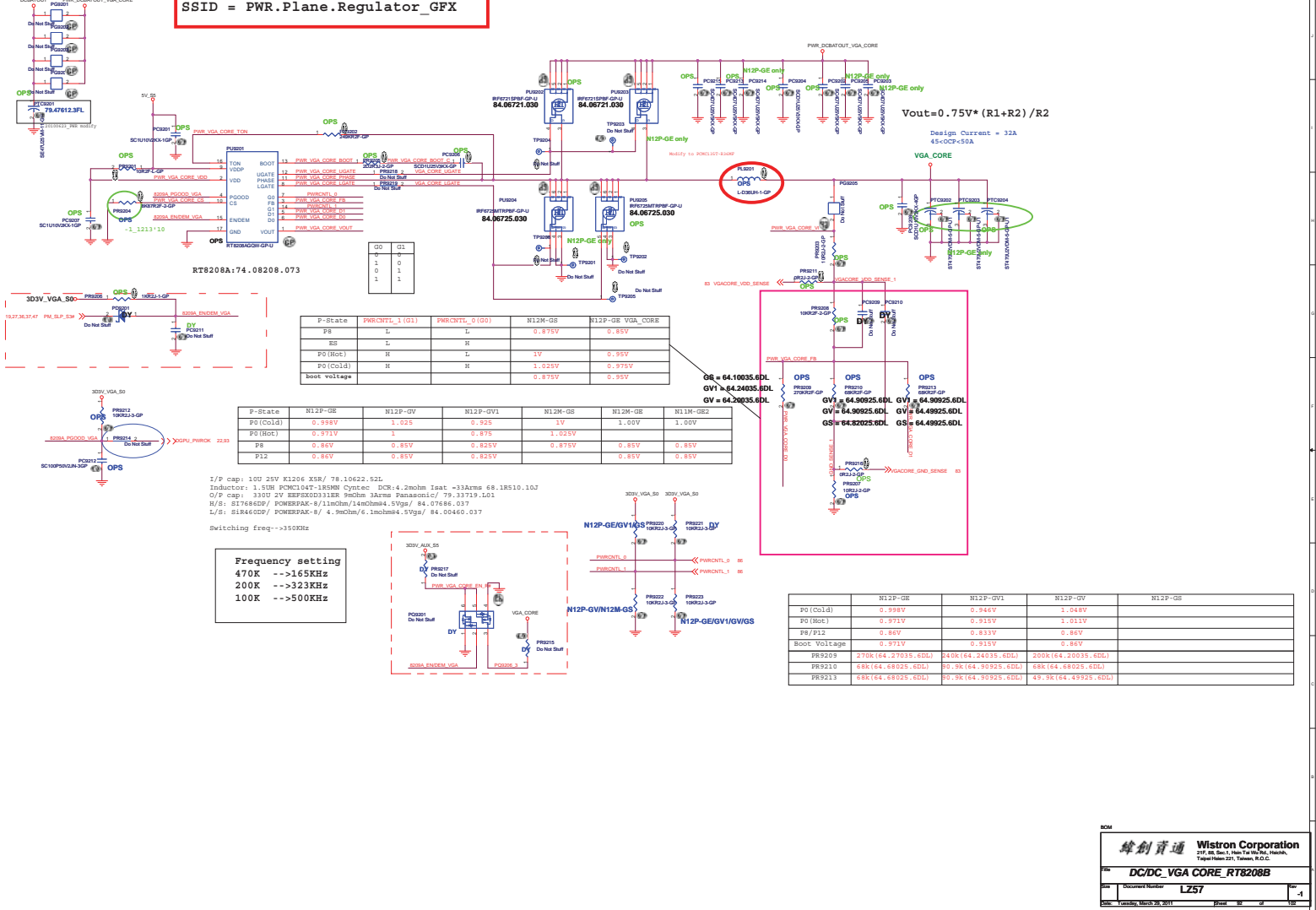
Wistron Corporation	
2/F, 88, Sec. 1, Hsin-Tai Rd., Hsinchu, Taiwan, R.O.C.	
VRAM CHANNEL-C	
Doc. Number	LZ57
Date	Version
1/1	1/1



VIDEO FRAME BUFFER PORT C

Wistron Corporation	
2/F, 88, Sec. 1, Hsin-Tai Wu Rd., Hsinchu, Taipei, Taiwan, R.O.C.	
VRAM CHANNEL-C	
Part Number	LZ57
Date	Issued
1/2011	01
1	-1

SSID = PWR.Plane.Regulator_GFX



$V_{out} = 0.75V * (R1+R2) / R2$
 Design Current = 32A
 45°C@25°C@5A

RT8208A:74.08208.073

P-State	PWRCTRL_1 (G1)	PWRCTRL_0 (G0)	N12M-GE	N12P-GE VGA_CORE
PS	L	L	1.875V	0.85V
SS	L	H	1V	0.95V
P0 (Hot)	H	L	1V	0.95V
P0 (Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV1	N12P-GV2	N12M-GE	N12M-GV1	N12M-GV2
P0 (Cold)	0.988V	1.025	0.925	1V	1.00V	1.00V
P0 (Hot)	0.971V	1	0.875	1.025V	0.80V	0.85V
PS	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
Flt	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V

I/P cap: 10U 25V K1206 XSR/ 78.10622.52L
 Inductor: 1.50u PCMC1047-183M Cyntrac DCR:4.2mohm Isat =33Arms 68.18510.10J
 O/P caps: 330U 2V XEPRX03318E 9600m 33mV Panasonic/ 79.33719.L0J
 H/S: S17686D/P POWERPAK-8/11mohm/1.4mohm4.5Vgs/ 84.07686.037
 L/S: S18460D/P POWERPAK-8/ 4.9mohm/6.1mohm4.5Vgs/ 84.00460.037
 Switching freq-->350KHz

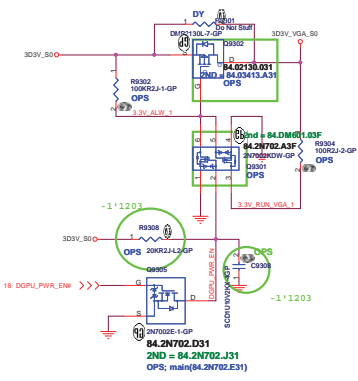
Frequency setting
 470K -->165KHz
 200K -->323KHz
 100K -->500KHz

GR = 64.10035.6DL
 GV1 = 64.54035.6DL
 GV2 = 64.20335.6DL

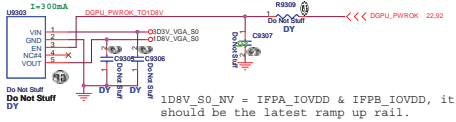
GV1 = 64.90925.6DL GV2 = 64.90925.6DL
 GV3 = 64.90925.6DL GV4 = 64.90925.6DL
 GS1 = 64.82025.6DL GS2 = 64.49925.6DL

	N12P-GE	N12P-GV1	N12P-GV2	N12P-GS
P0 (Cold)	0.988V	0.946V	1.048V	
P0 (Hot)	0.971V	0.915V	1.011V	
PS/Flt	0.86V	0.834V	0.85V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270K(64.27035.6DL)	240K(64.24035.6DL)	200K(64.20035.6DL)	
PR9210	88K(64.88025.6DL)	9K(64.90925.6DL)	88K(64.88025.6DL)	
PR9213	88K(64.88025.6DL)	9K(64.90925.6DL)	49.9K(64.49925.6DL)	

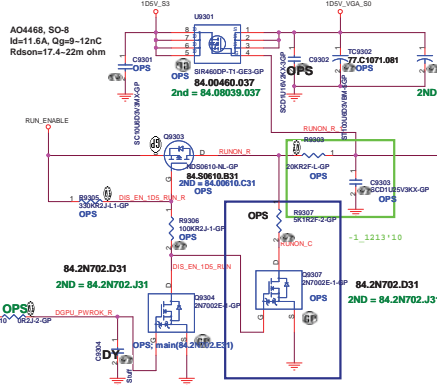
+3VS to 3.3V_DELAY Transfer



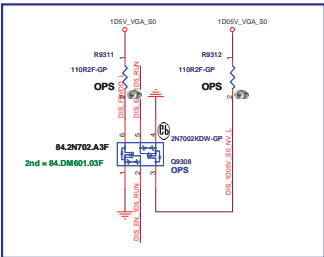
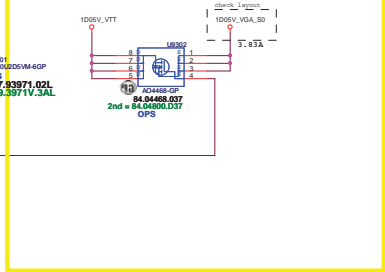
+3VS to 1.8V Transfer



1D5V_VGA_S0



1.05V to 1.05V_VGA_S0 Transfer



BOM		Wistron Corporation	
		21F, 8th. Sec.1, Neihu TAI HUI Rd., Neihu, Taipei Hsien 221, Taiwan, R.O.C.	
DISC		DISCRETE VGA POWER	
Doc	Document Number	LZ57	Rev
			-1
Date	Issued	March 25, 2011	Sheet 05 of 05

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BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		CRT Switch	
Size A3	Document Number	Rev	
	LZ57	-1	
Date: Tuesday, March 29, 2011		Sheet 95	of 102

D

D

C

C

B

B

A

A

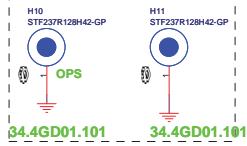
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TOUCH PANEL	
Size A4	Document Number LZ57
Date: Tuesday, March 29, 2011	Rev -1
2	Sheet 96 of 102

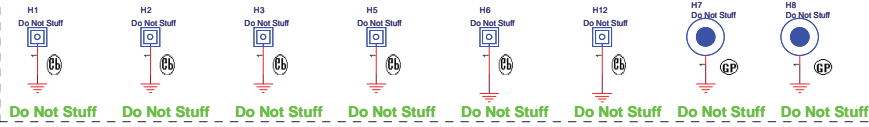
CPU Plate



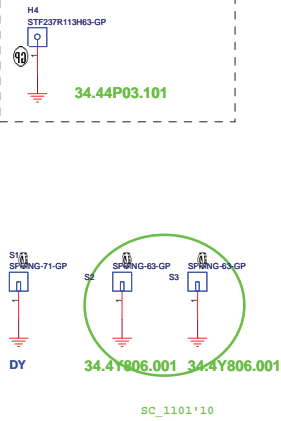
VGA Std-Off



Structure boss



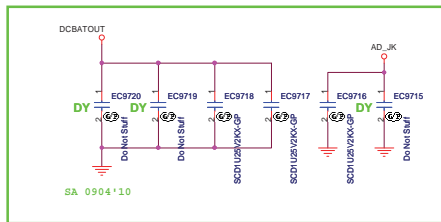
MiniPCI Std-Off



POWER TESTING POINT--TOP



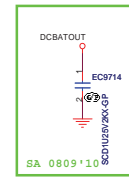
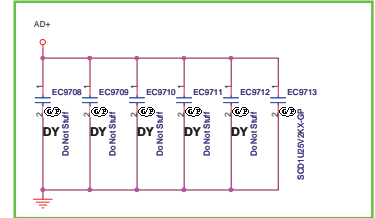
POWER TESTING POINT--Bottom



Check test point



Test Point放在Dimm Door打開可量測處



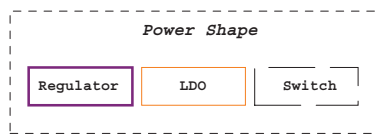
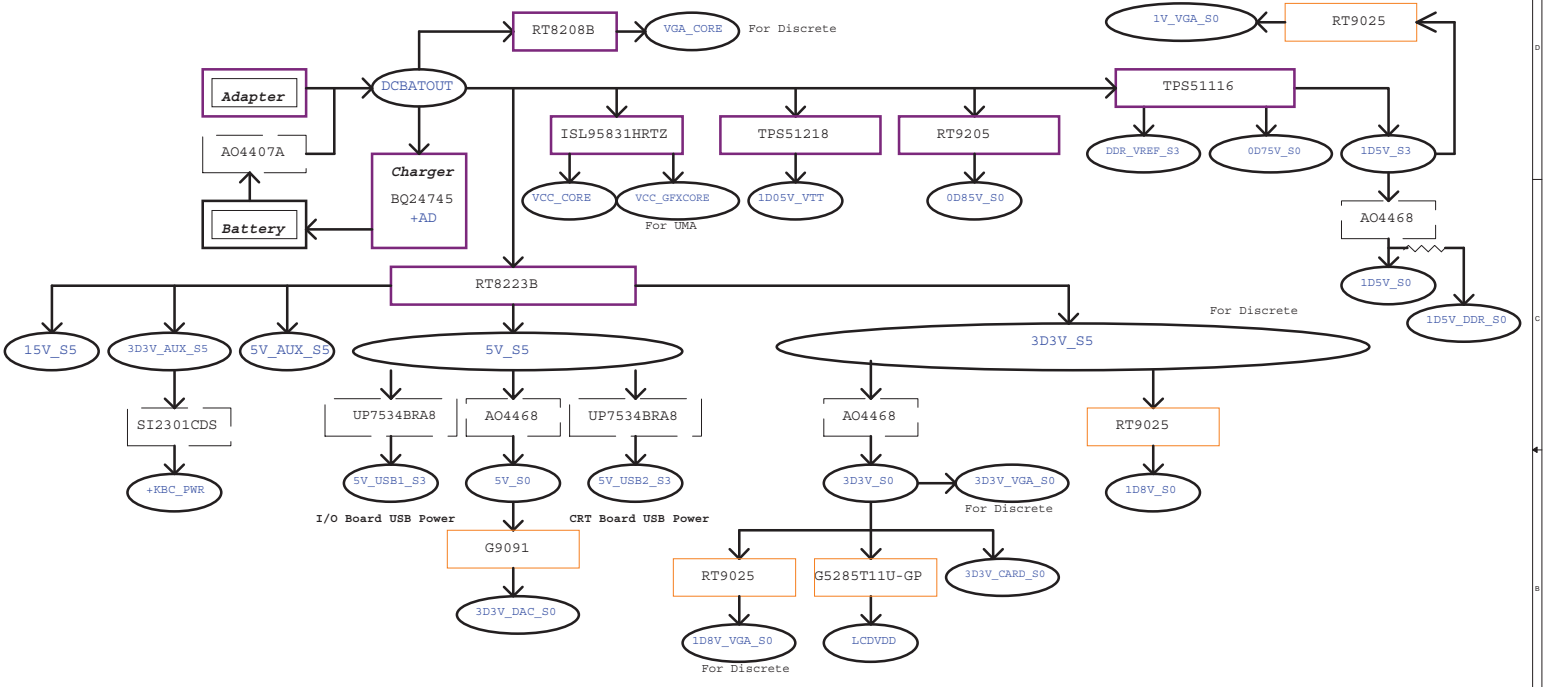
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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
Title	UNUSED PARTS/EMI Capacitors
Size	Document Number
	L757
Date:	Tuesday, March 25, 2011
Sheet	97 of 102
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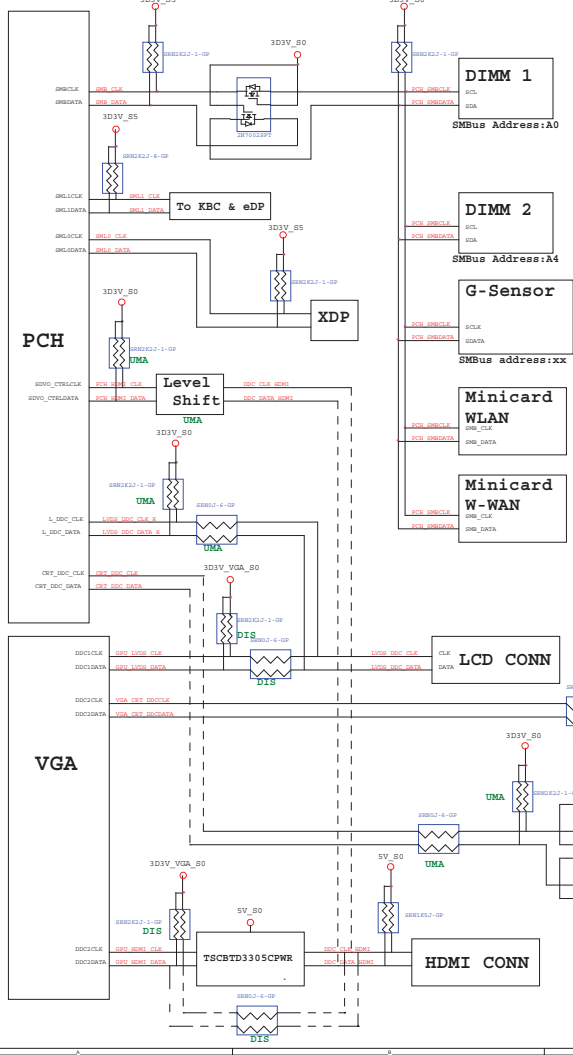
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緯創資通 Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		
Change History		
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 98 of 102	

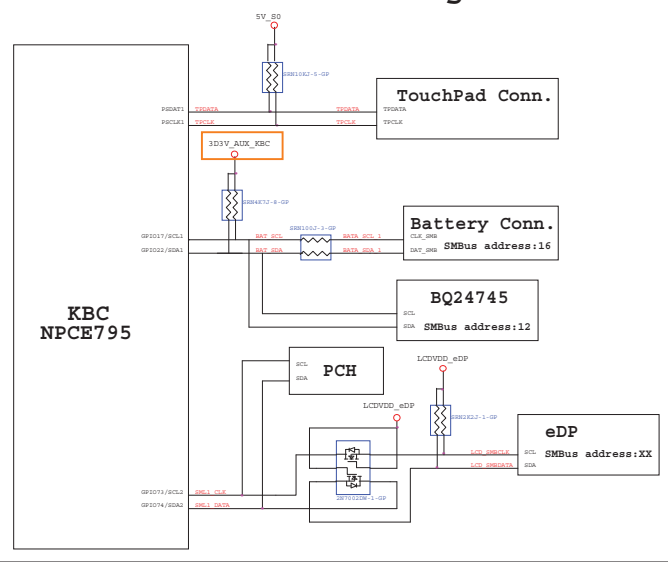


BOM			
緯創資通		Wistron Corporation	
217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.			
Power Block Diagram			
Title	Document Number	Rev	
K3	LZ57	-1	
Date: Tuesday, March 29, 2011	Sheet 100 of	102	

PCH SMBus Block Diagram

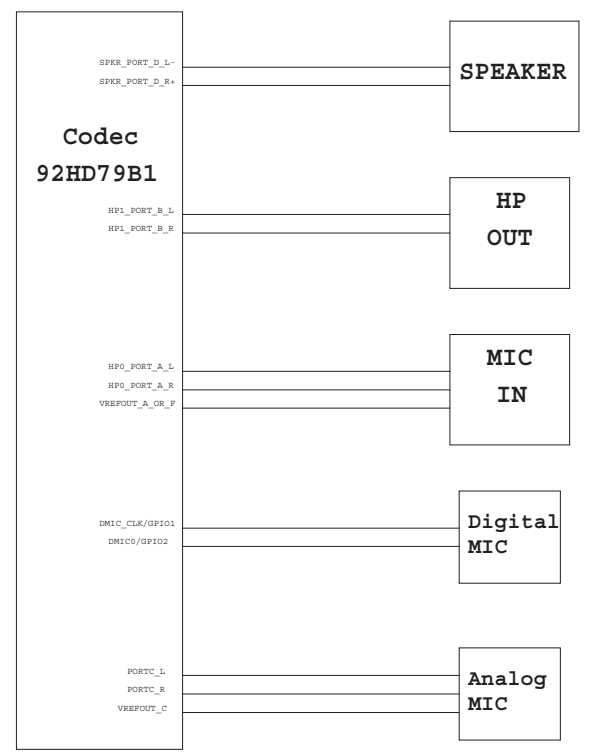
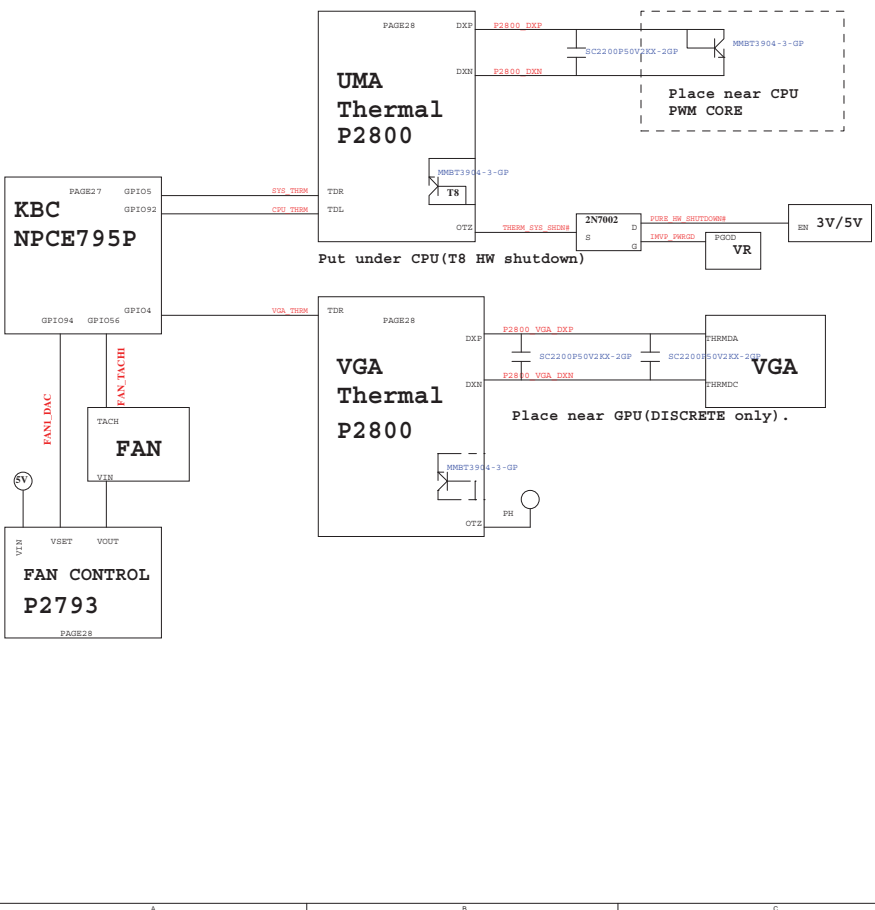


KBC SMBus Block Diagram



Thermal Block Diagram

Audio Block Diagram



BOM

緯創資通		Wistron Corporation	
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Title: Thermal/Audio Block Diagram			
Rev	Document Number	Rev	
Customer	LZ57		-1
Date: 1/10/2011		Sheet	102 of 102

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