LA46 UMA Block Diagram

LA46-UMA-1_0104

Project Code: 91.4GV01.001
PCB(Raw Card): 09922-1

USB BD
I/O BD
CRT BD
Power BD
Finger Printer BD
AV BD
BT BD

Thermal Sensor EMC2103 11

Clock GEN CK505 3

UNBUFFERED DDR3 SODIMM Socket1 12
204-PIN DDR3 SODIMM
UNBUFFERED DDR3 SODIMM Socket2 13

Channel A DDR3 800/1066
Channel B DDR3 800/1066

Intel CPU Auburndale (Dual Core)
DDR3 800/1066MHz
4,5,6,7,8,9,10

FDI
DMI x4

Intel PCH HM55
USB 2.0 (12 ports)
Serial ATA (4 ports)
PCI Express (8 ports)
AC97 2.3/Azalia Interface
ACPI 2.0
LPC I/F
PCI Rev 2.3
INT. RTC
14,15,16,17,18,19,20,21,22

Mic in
Headphone out
HD AUDIO CODEC ALC269Q-VB-GR 27
HDA Link

SATA HDD
SATA CONN 28
SATA Port 0

SATA ODD
SATA CONN 28
SATA Port 4

5-in-1 Slot
MediaCard Reader Realtek/5159 31
USB 2.0 CH4

Bluetooth 32
CH9
Camera 24
CH15
Finger Printer 35
CH10
USB BD
USB 2.0 32
CH1
USB 2.0 32
CH2
USB 2.0 32
CH8
EHCI#1
USB 2.0

LVDS
14'' WUXGA (WSXGA) LCD 24

RGB
CRT CONN 25

PCI Express 1
GLAN AR8131 29
Transformer
RJ45

USB 2.0 CH3
PCI Express 2
Mini PCI-E WLAN Card 31

USB 2.0 CH5
PCI Express 3
Mini PCI-E WWAN Card 31
SIM Slot

USB 2.0 CH12
PCI Express 4
Express Card 31
I/O BD

SPI
SPI FLASH 4MB 35

LPC Bus / 33MHz
KBC Nuvoton NPCE781E 33
LPC Debug 33

Multi-touch Touchpad
Int. KB 33
G-Sensor 35
SPI Flash 128Kb 35

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

CPU DC/DC ISL62882 38,39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025 43	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026 43	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

CHARGER BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	BT+

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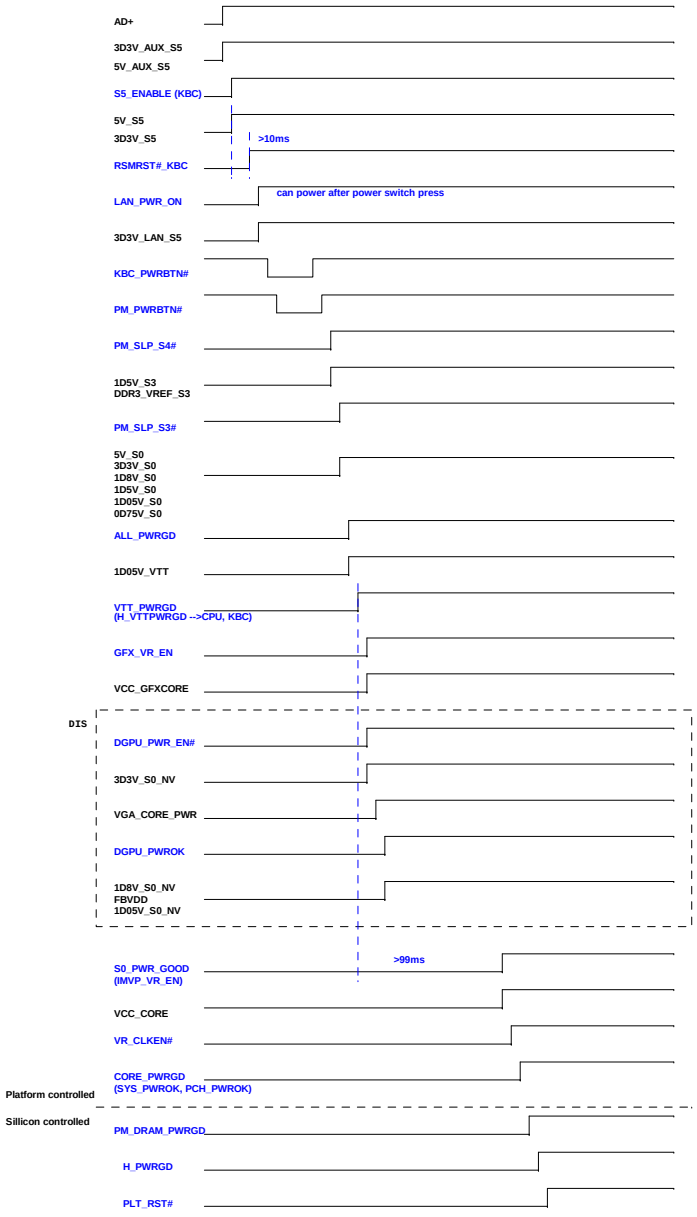
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCH Strapping

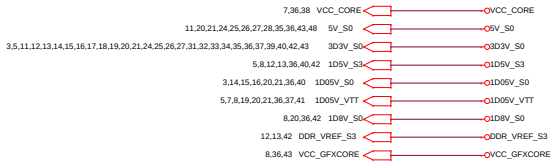
Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Sequence AC



PLANAR_ID[1..0]

KBC GPIn	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0		
	0	0	LA46_UMA- SA	SA
	0	1	LA46_UMA- SB	SB
	1	0	LA46_UMA- SC	SC
	1	1	LA46_UMA- 1	-1



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Title: Reference

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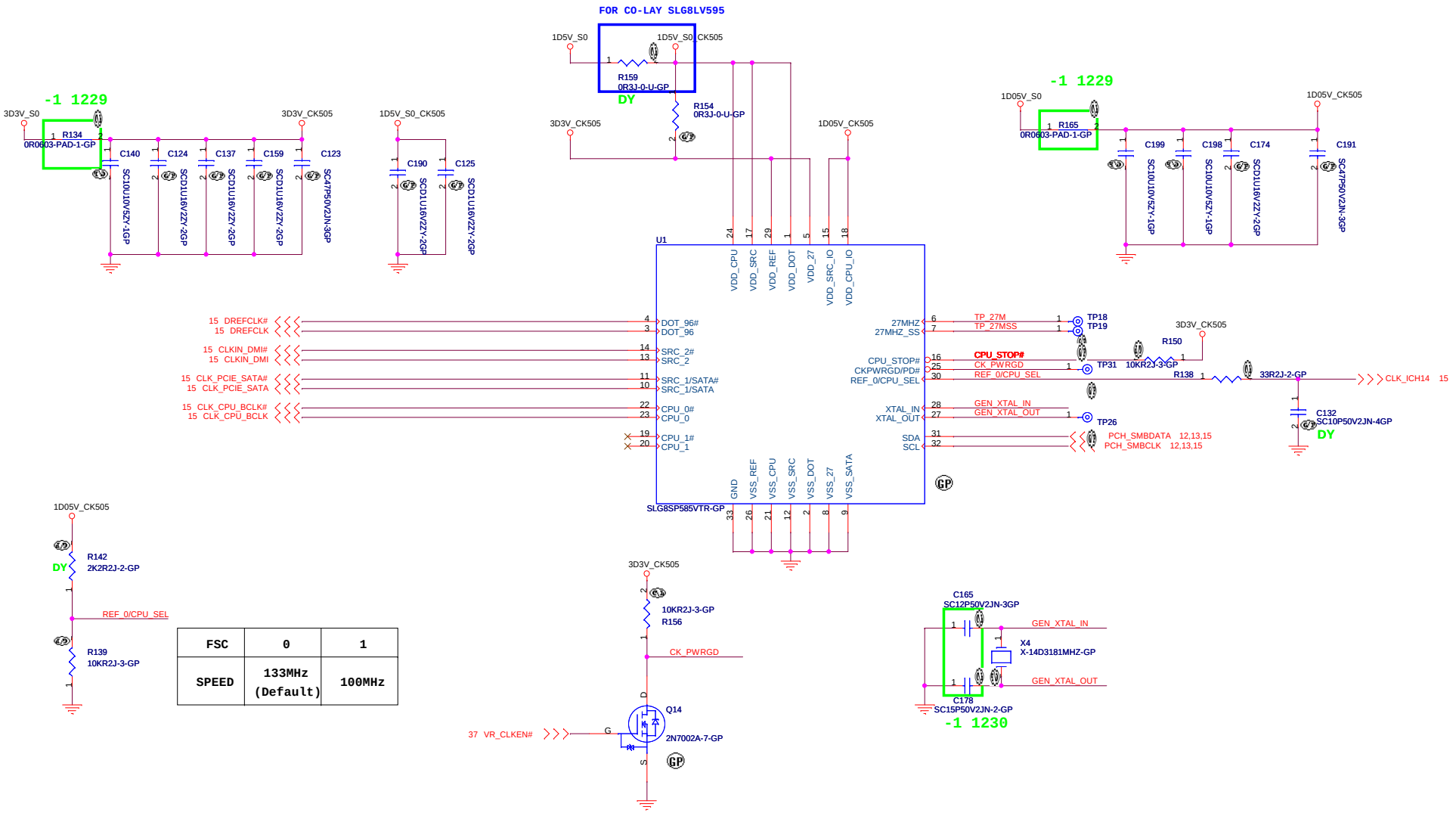

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: CLKGEN.

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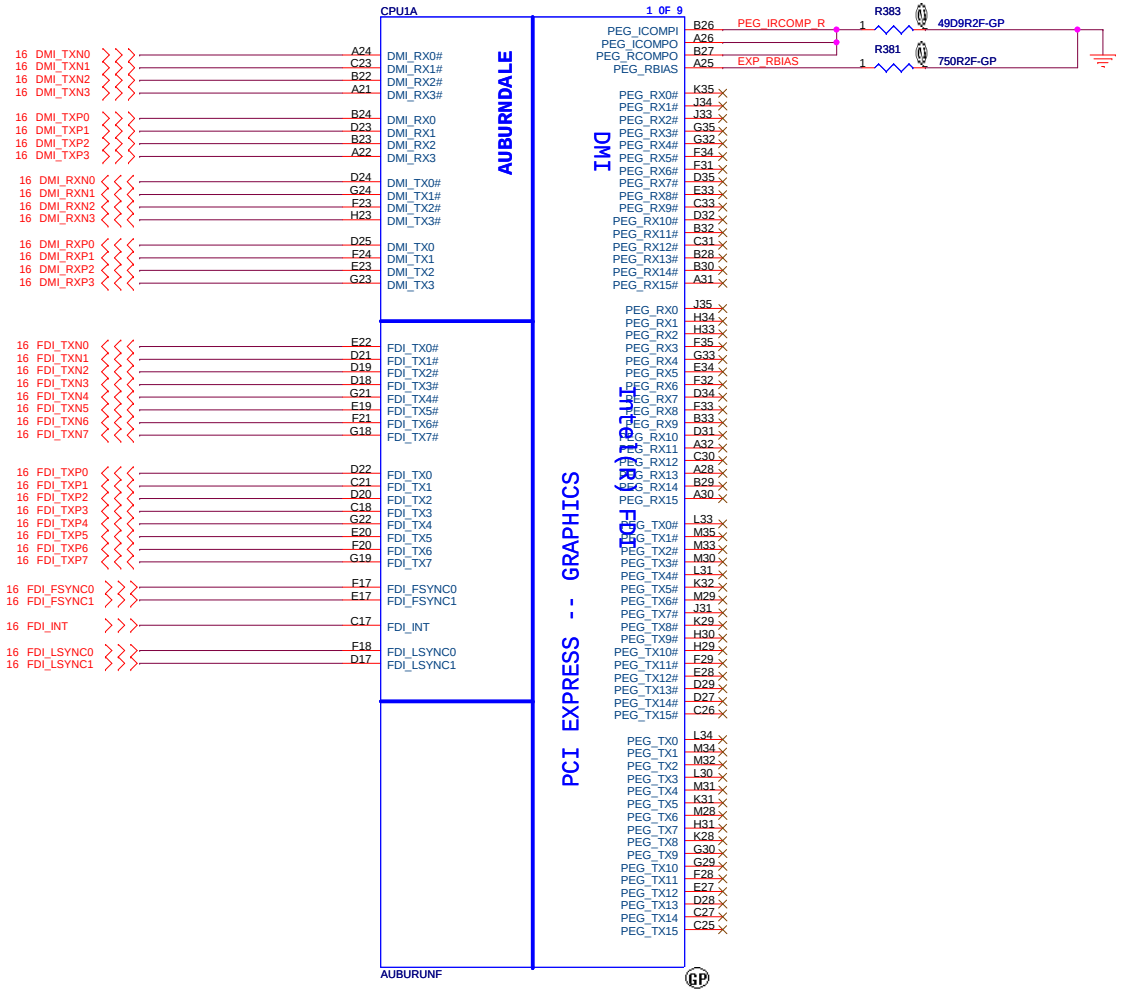

Wistron Corporation			
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
Title	CPU(1/7)-PEG / DMI /FDI		
Size A3	Document Number LA46-UMA		Rev 1
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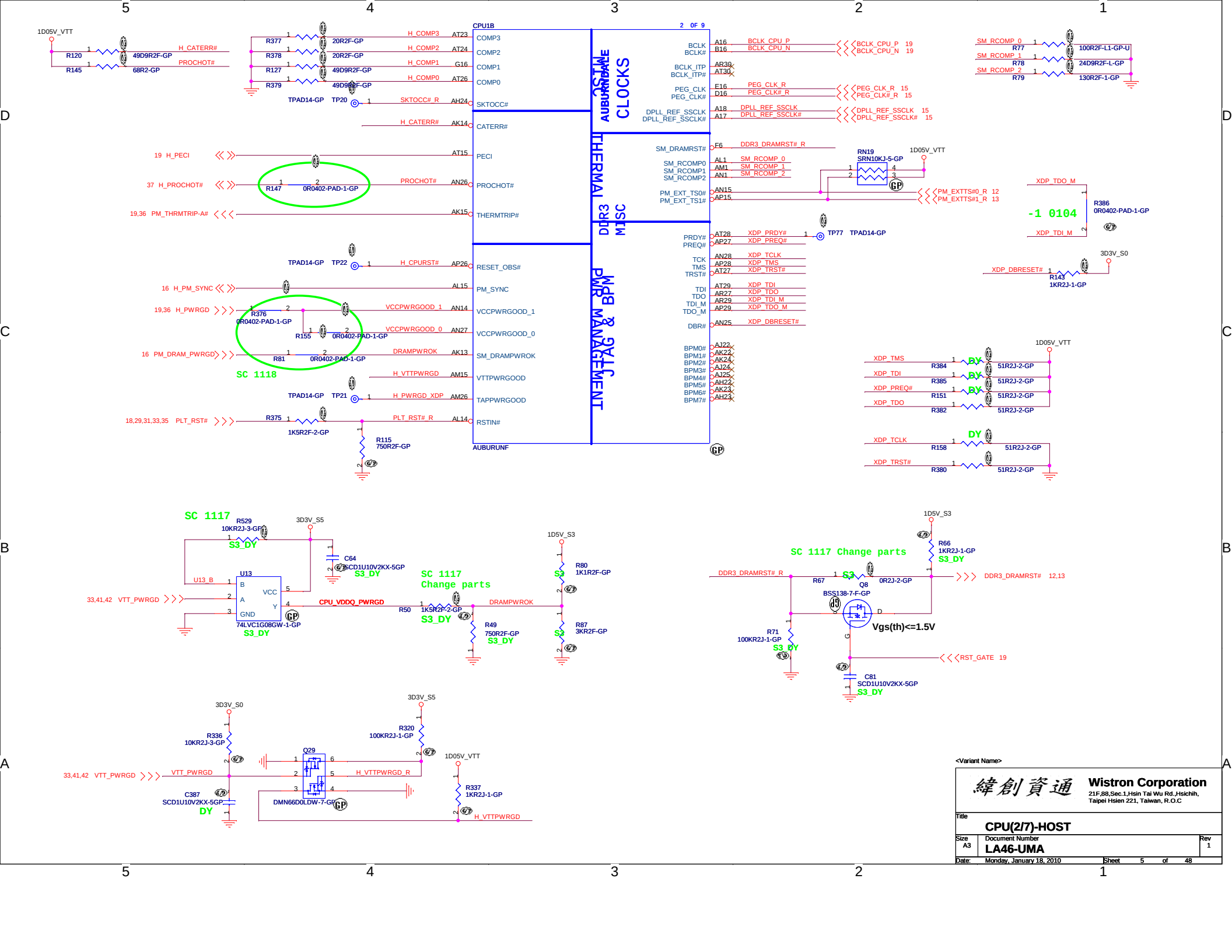
CPU1B
2 OF 9
AUBURUNF
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
SC 1118
SC 1117
SC 1117 Change parts
Vgs(th)<=1.5V
DY
S3_DY
-1 0104
<Variant Name>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C
Title
CPU(2/7)-HOST
Size
A3
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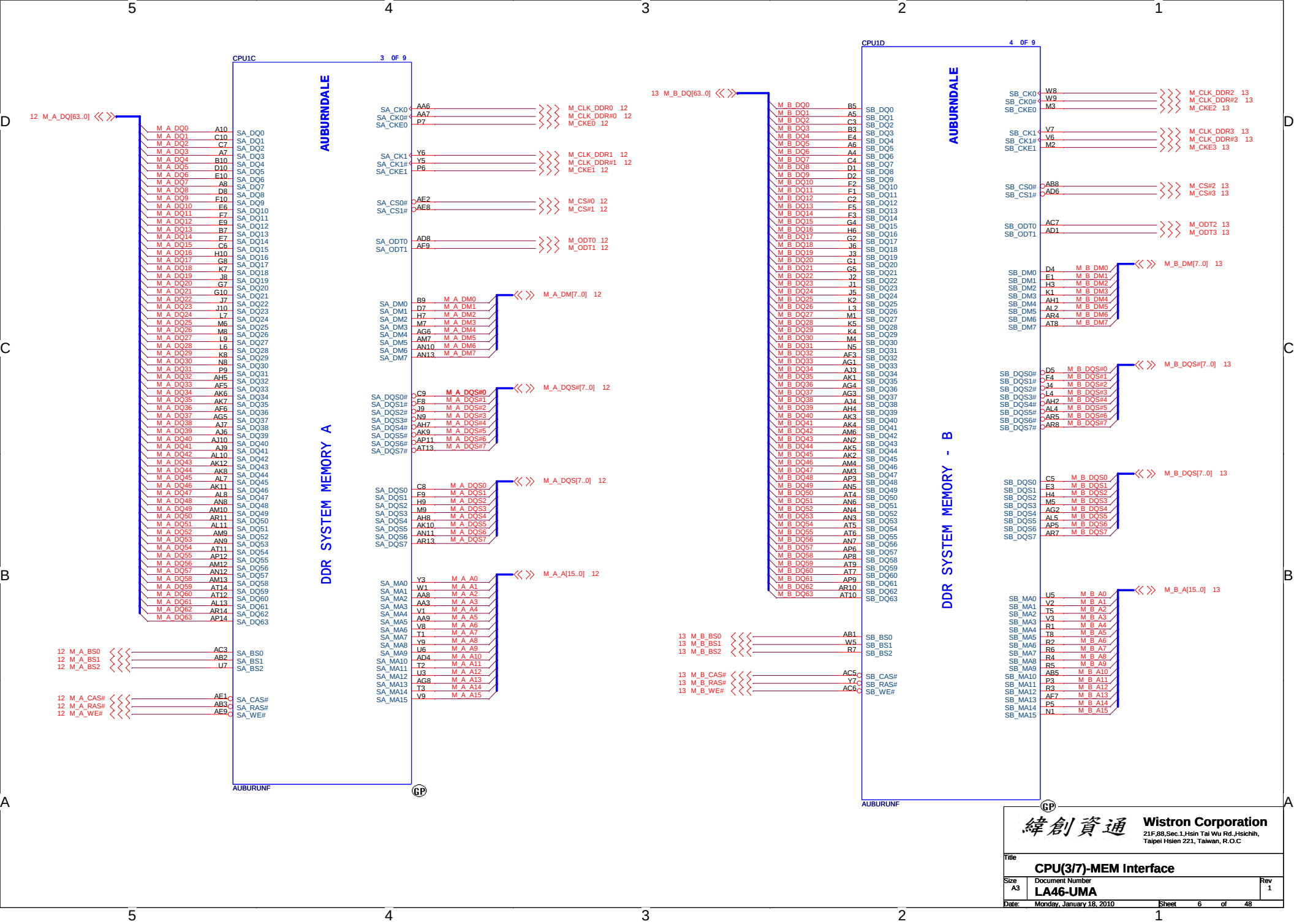

緯創資通

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Title: **CPU(3/7)-MEM Interface**

Size	Document Number	Rev
A3	**LA46-UMA**	1

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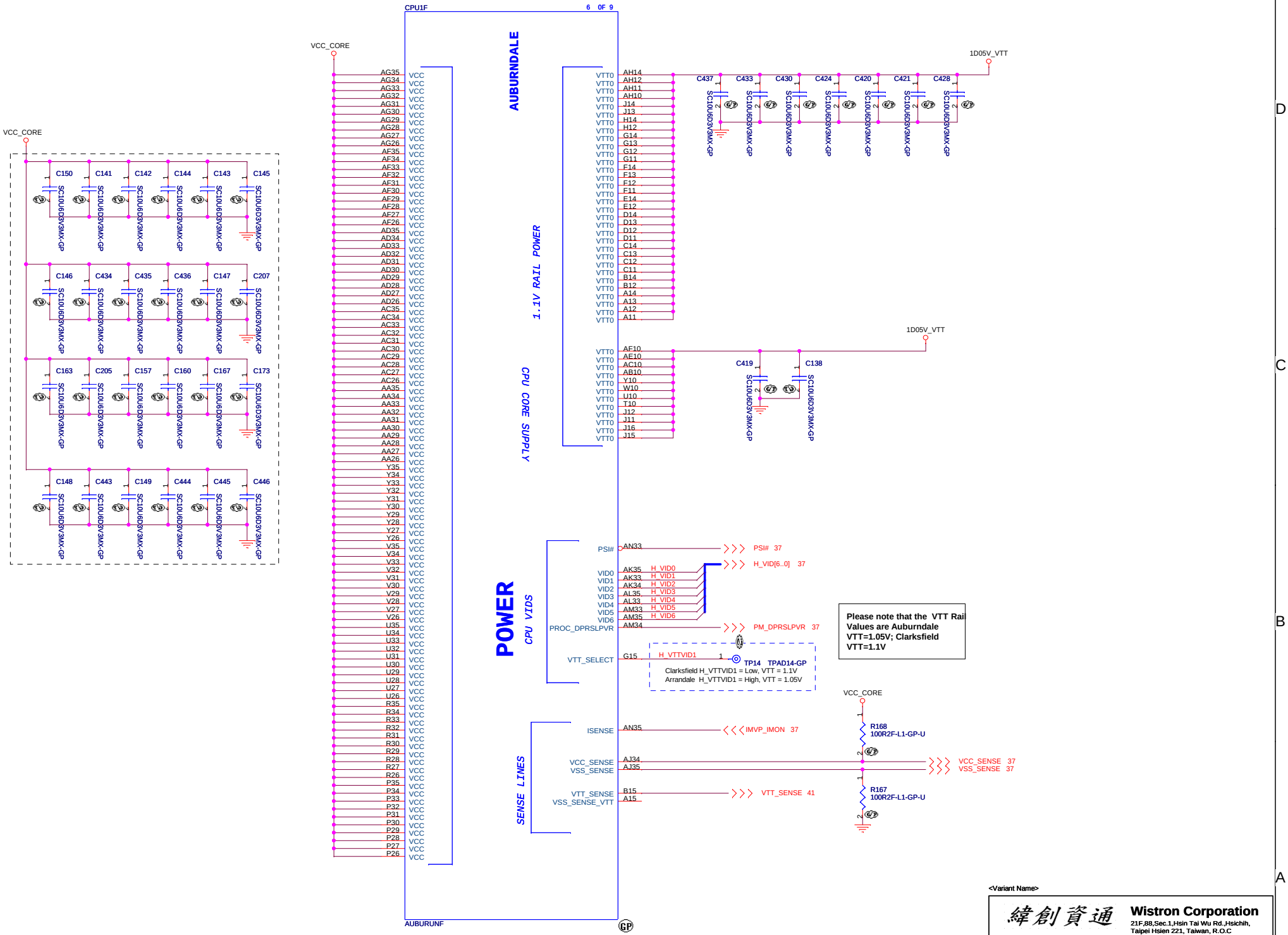

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<Variant Name>

Title: CPU(4/7)-POWER

Size: | Document Number: LA46-UMA | Rev: 1

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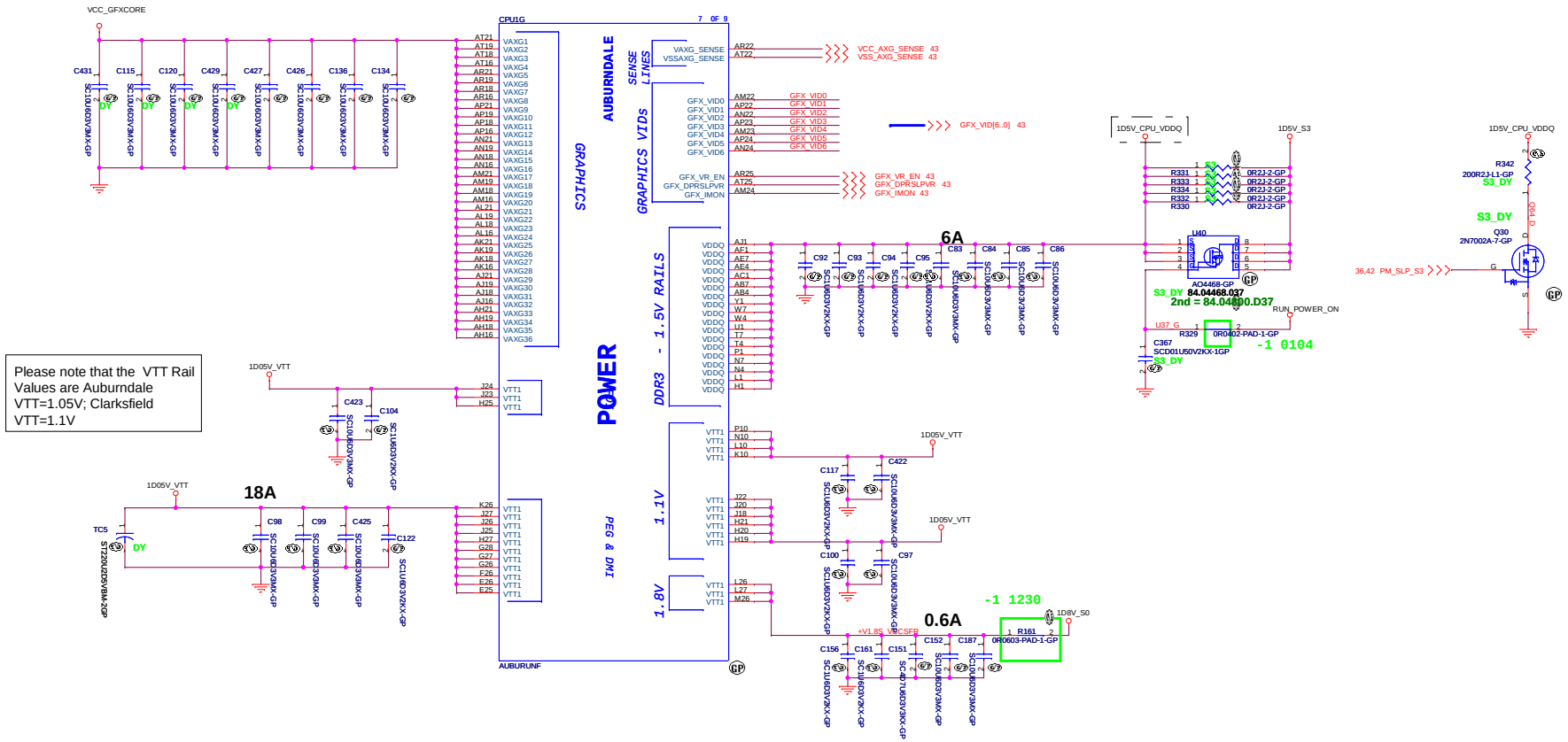

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Title	CPU(5/7)-Graphic PWR
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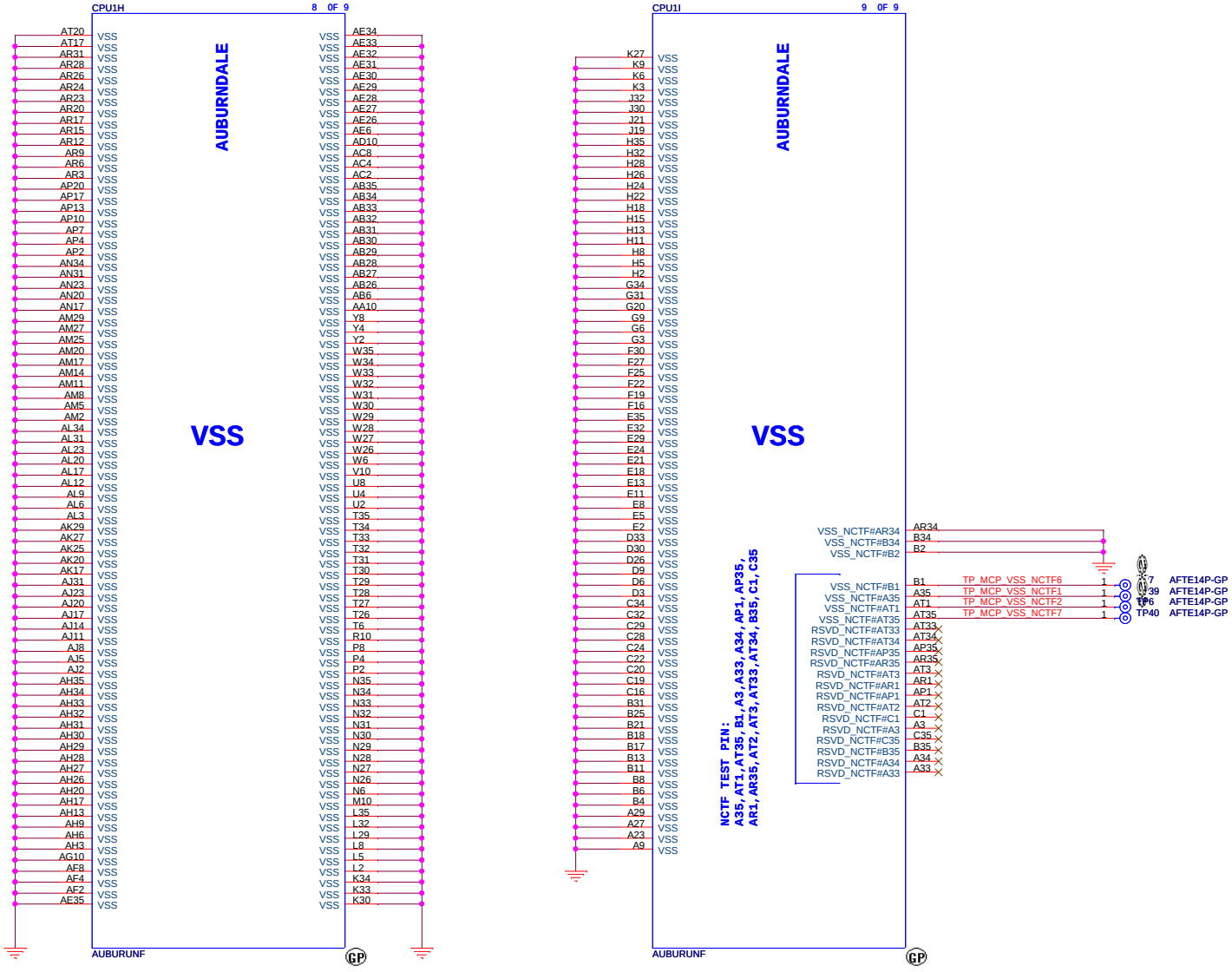

緯創資通	Wistron Corporation	21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: **CPU(6/7)-VSS**

Size	Document Number	Rev
A3	LA46-UMA	1

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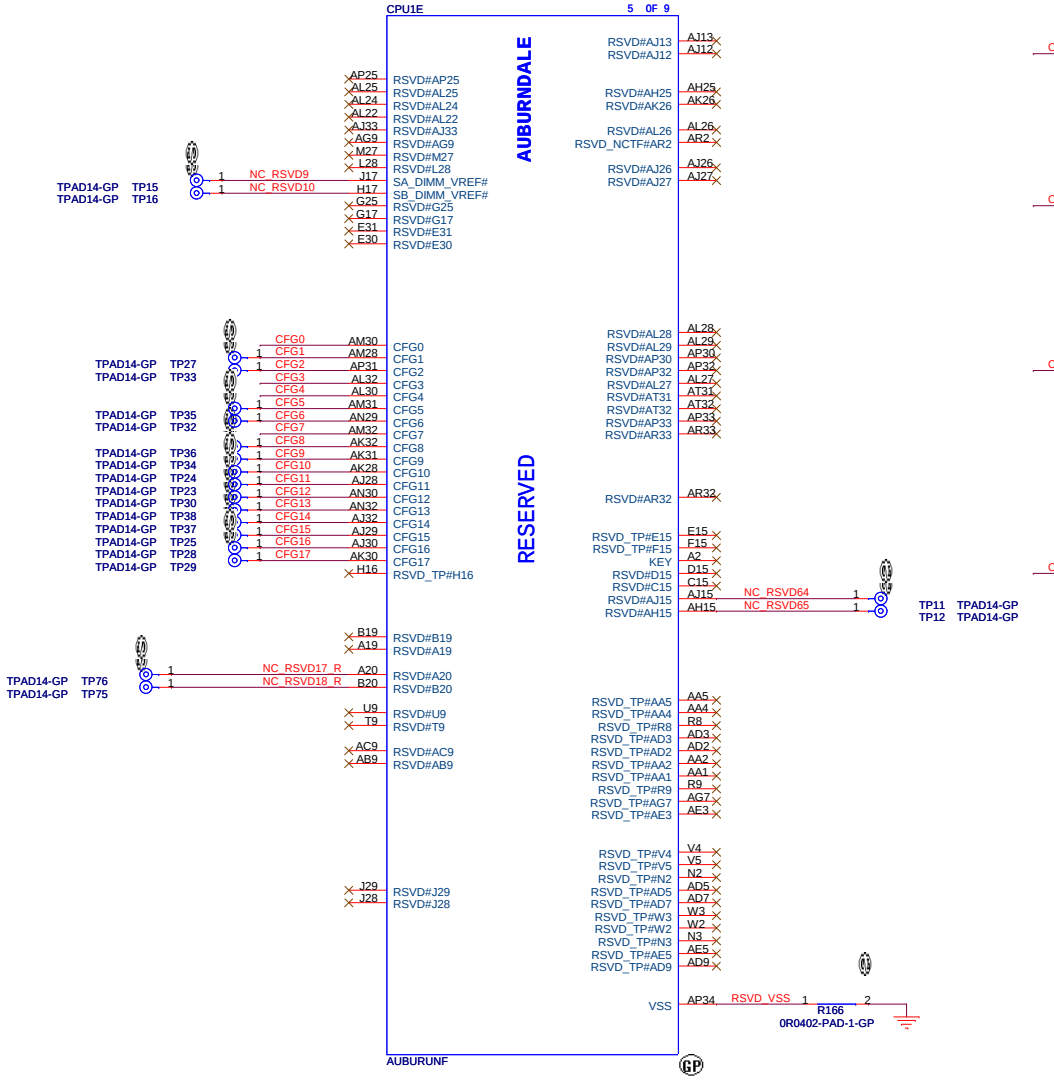

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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Title: CPU(7/7)-RESERVED

Size	Document Number	Rev
A3	LA46-UMA	1

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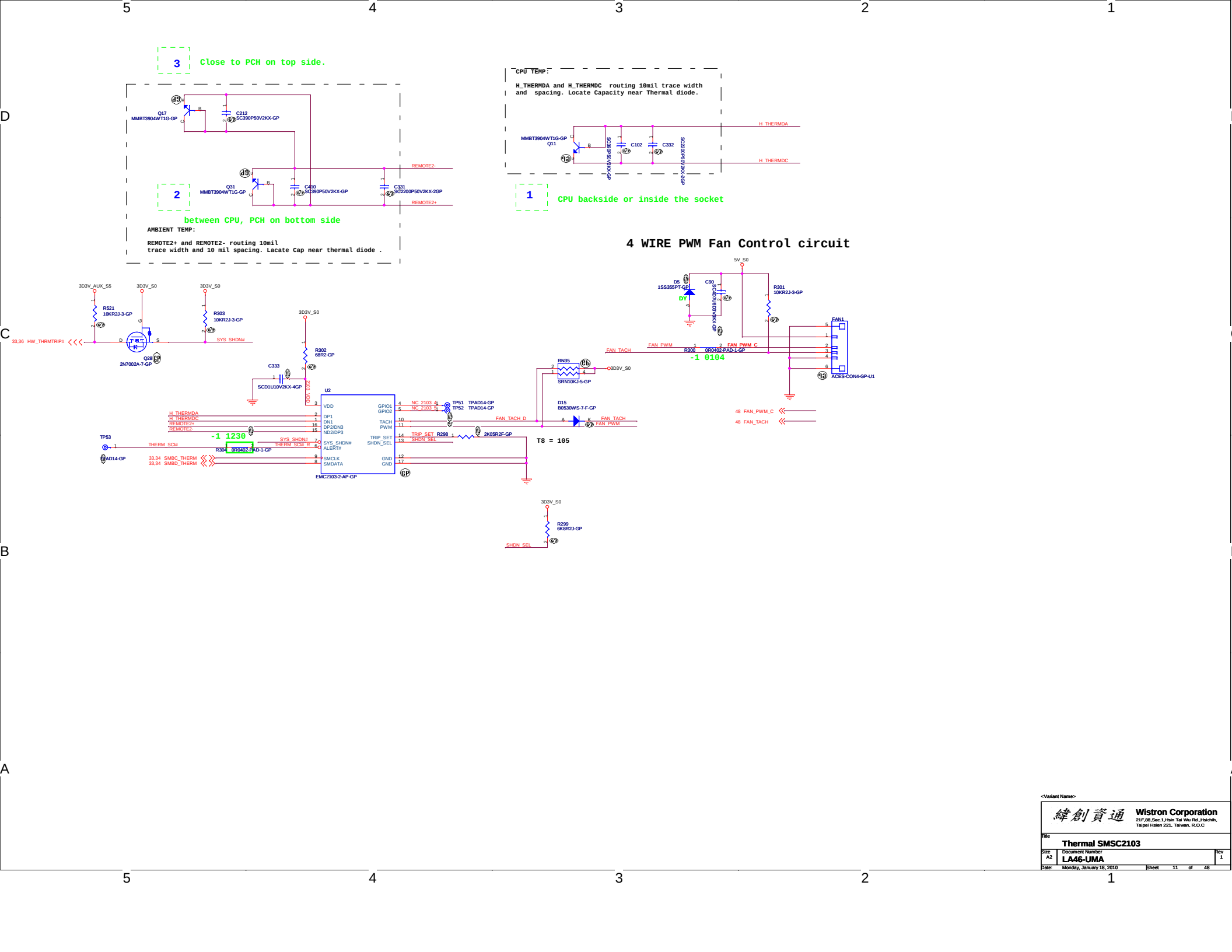

<Variant Name>

緯創資通 Wistron Corporation
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Title: Thermal SMSC2103

Size	Document Number	Rev
A2	LA46-UMA	1

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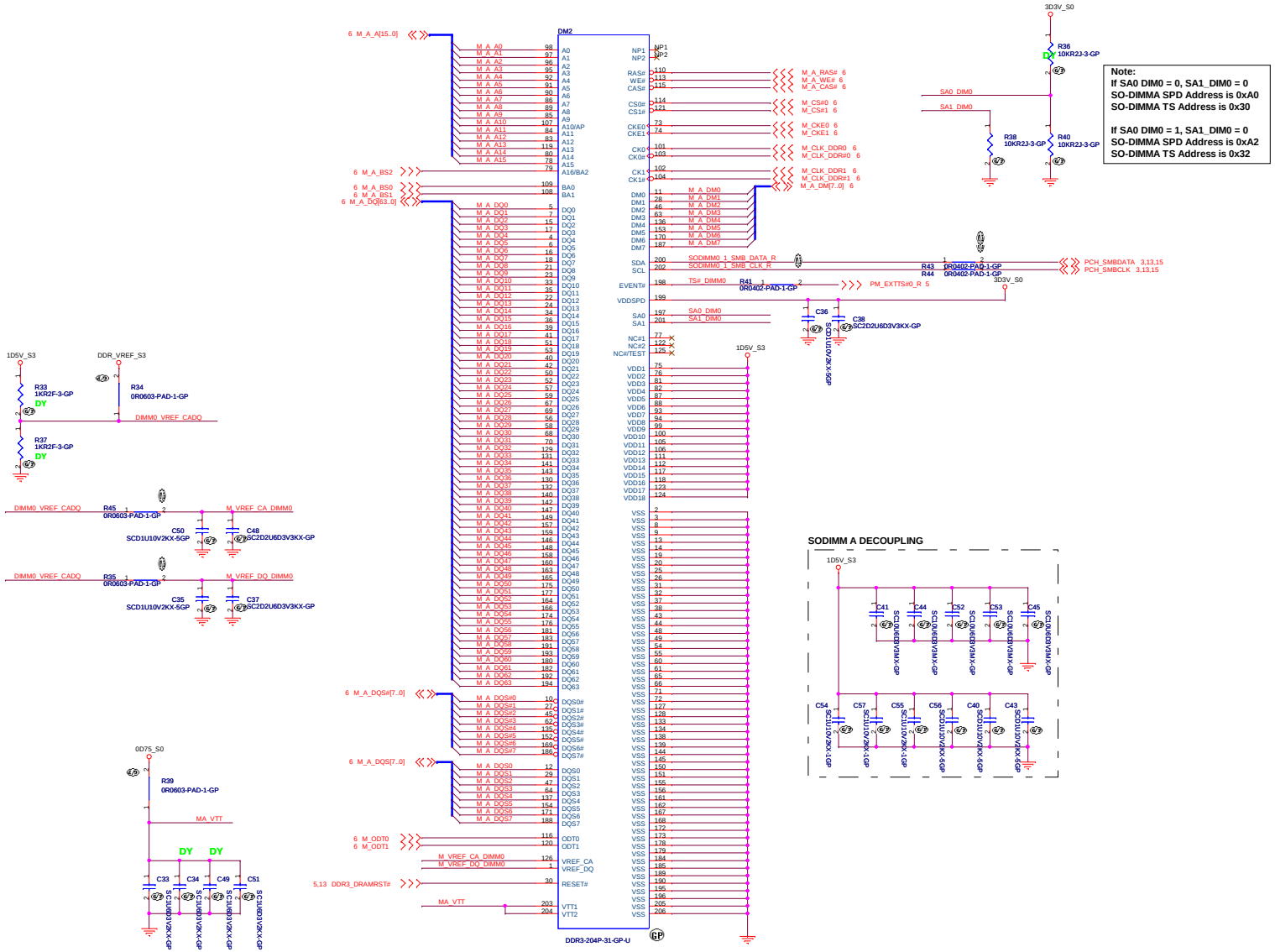

<Variant Name>

Wistron Corporation
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Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	LA46-UMA	1

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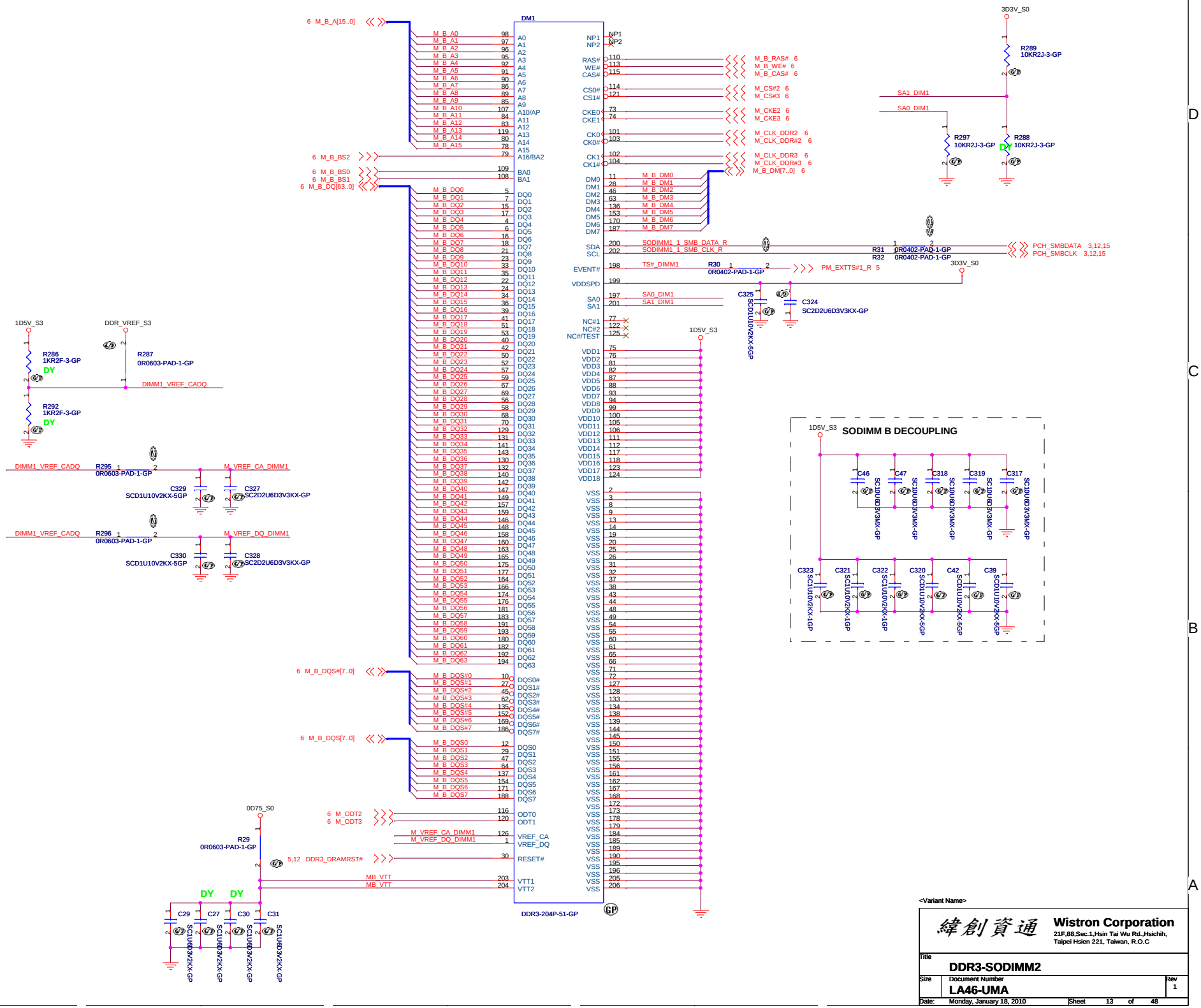

<Variant Name>

緯創資通	**Wistron Corporation** 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title	**DDR3-SODIMM2**
Size	Document Number **LA46-UMA** Rev 1
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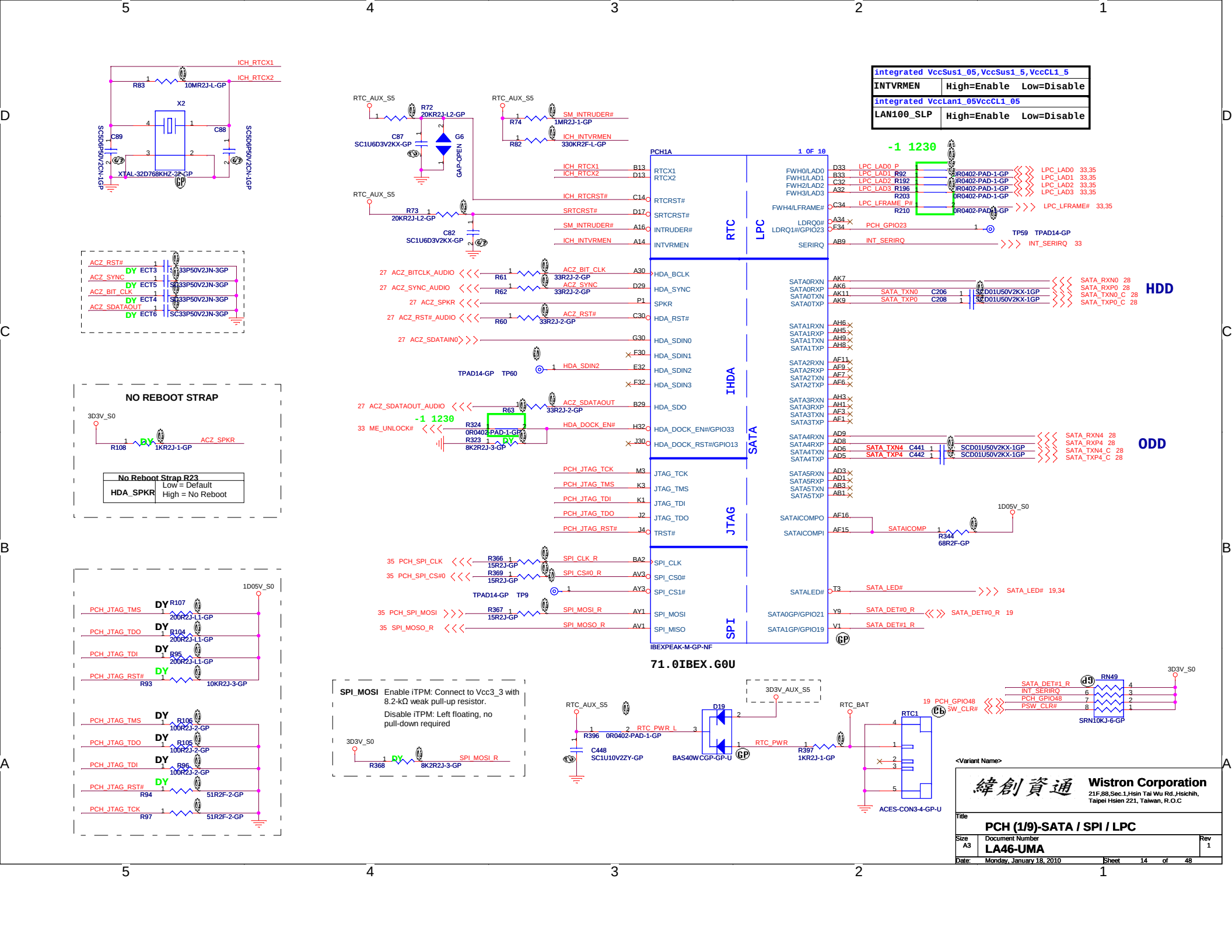
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
-1 1230
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
HDD
ODD
IBEXPEAK-M-GP-NF
71.0IBEX.G0U
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
<Variant Name>
Wistron Corporation
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PCH (1/9)-SATA / SPI / LPC
Size A3
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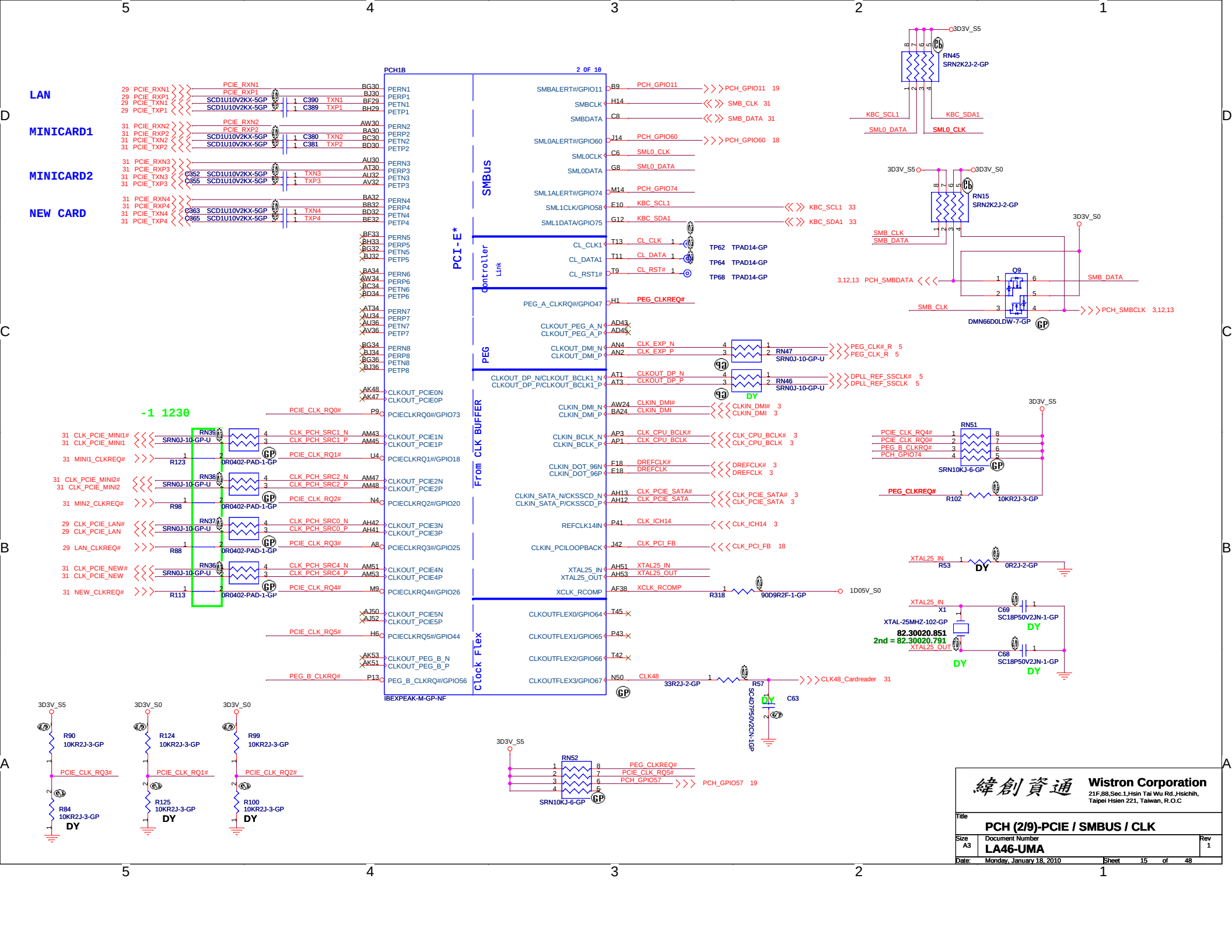
LAN
MINICARD1
MINICARD2
NEW CARD
PCH1B
2 OF 10
PCI-E*
SMBUS
Controller
Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
-1 1230
DY
Wistron Corporation
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緯創資通
Title
PCH (2/9)-PCIE / SMBUS / CLK
Size
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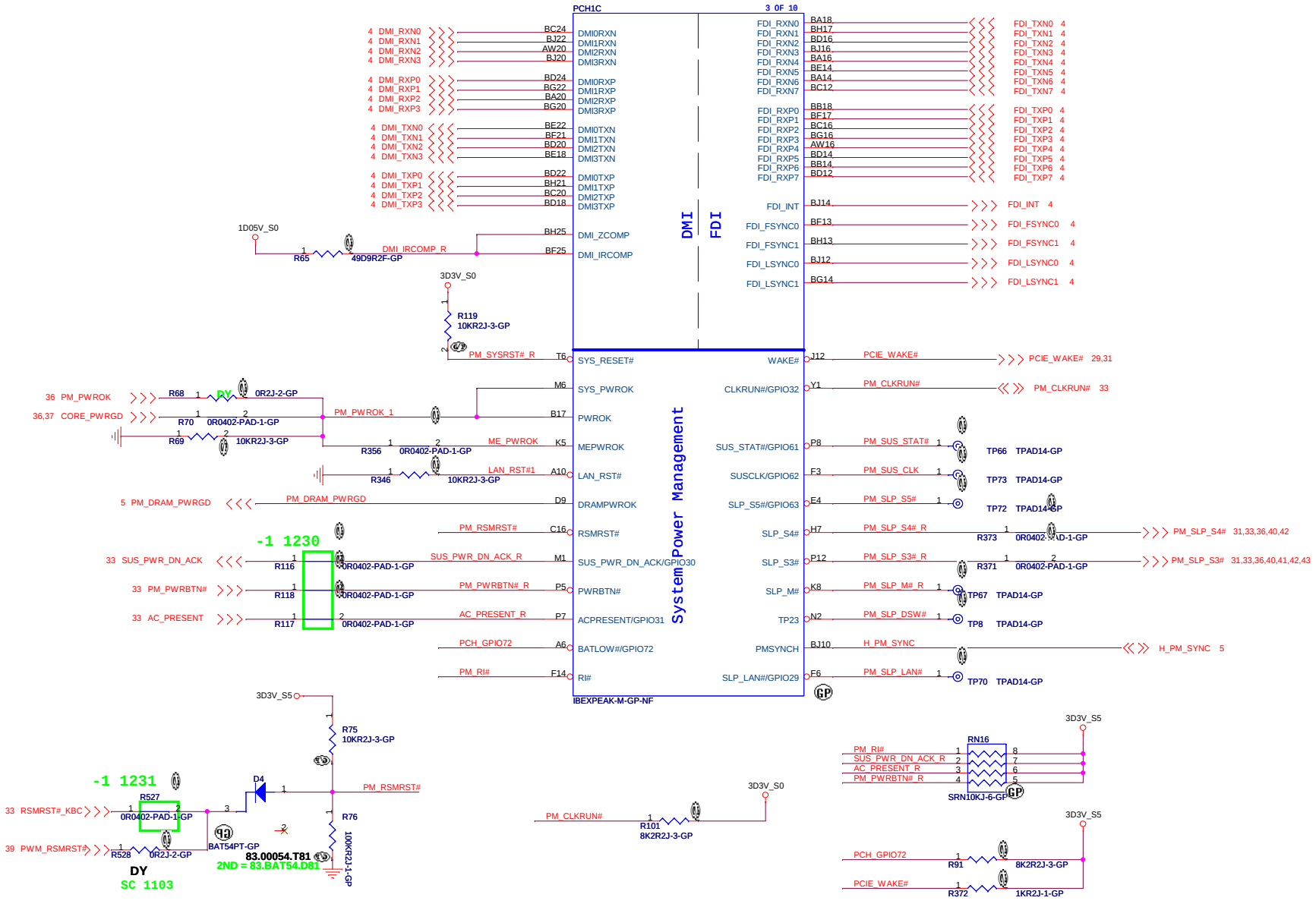

<variant_name>

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Title	PCH (3/9)-DMI / FDI / PM
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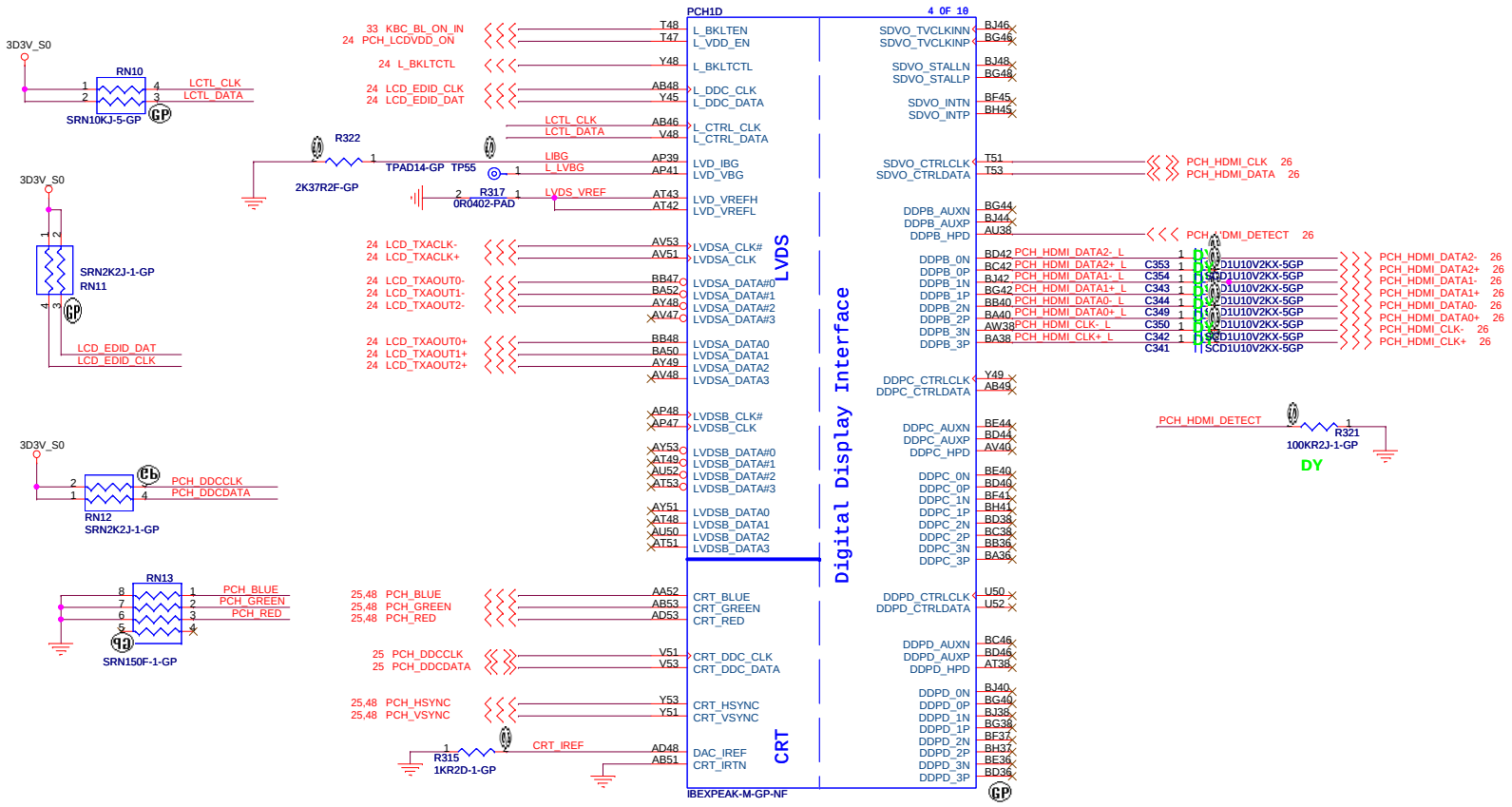

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Title	PCH (4/9)-LVDS / CRT		
Size A3	Document Number LA46-UMA		Rev 1
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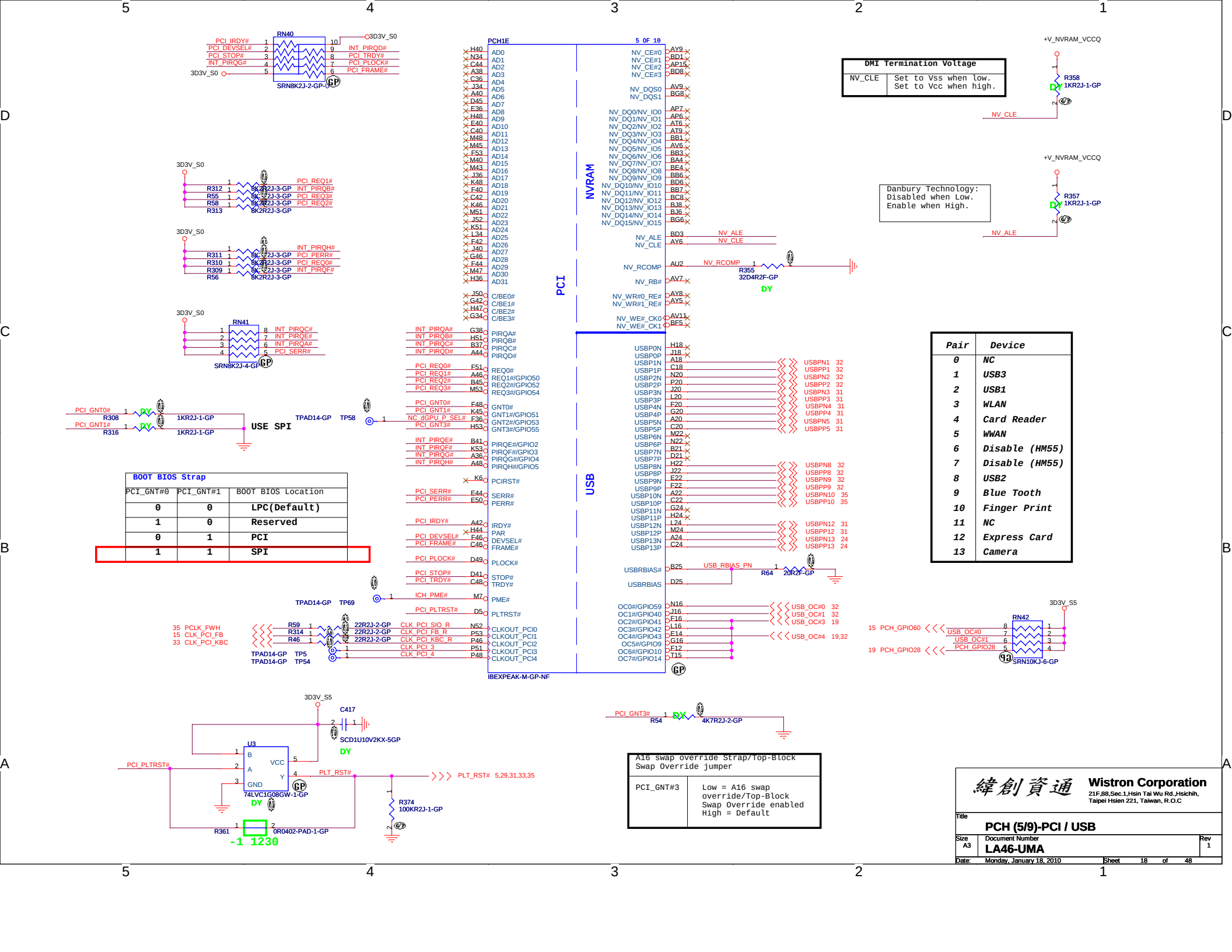
RN40
PCI_IRDY#
PCI_DEVSEL#
PCI_STOP#
INT_PIRQG#
3D3V_S0
INT_PIRQD#
PCI_TRDY#
PCI_PLOCK#
PCI_FRAME#
SRN8K2J-2-GP-U
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
RN41
INT_PIRQC#
INT_PIRQE#
INT_PIRQA#
PCI_SERR#
SRN8K2J-4-GP
R312
R55
R58
R313
PCI_REQ1#
INT_PIRQB#
PCI_REQ3#
PCI_REQ2#
8K2R2J-3-GP
R311
R310
R309
R56
INT_PIRQH#
PCI_PERR#
PCI_REQ0#
INT_PIRQF#
R308
R316
PCI_GNT0#
PCI_GNT1#
1KR2J-1-GP
DY
USE SPI
TPAD14-GP
TP58
NC_dGPU_P_SEL#
PCI_GNT3#
BOOT BIOS Strap
PCI_GNT#0
PCI_GNT#1
BOOT BIOS Location
0 0 LPC(Default)
1 0 Reserved
0 1 PCI
1 1 SPI
TP69
ICH_PME#
PCI_PLTRST#
35 PCLK_FWH
15 CLK_PCI_FB
33 CLK_PCI_KBC
R59
R314
R46
22R2J-2-GP
CLK_PCI_SIO_R
CLK_PCI_FB_R
CLK_PCI_KBC_R
CLK_PCI_3
CLK_PCI_4
TP5
TP54
3D3V_S5
C417
SCD1U10V2KX-5GP
U3
74LVC1G08GW-1-GP
PLT_RST#
PLT_RST# 5,29,31,33,35
R361
0R0402-PAD-1-GP
-1 1230
R374
100KR2J-1-GP
DMI Termination Voltage
NV_CLE
Set to Vss when low.
Set to Vcc when high.
+V_NVRAM_VCCQ
R358
1KR2J-1-GP
R357
Danbury Technology:
Disabled when Low.
Enable when High.
NV_ALE
R355
32D4R2F-GP
R64
20R2F-GP
USB_RBIAS_PN
R54
4K7R2J-2-GP
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3
Low = A16 swap override/Top-Block Swap Override enabled
High = Default
RN42
15 PCH_GPIO60
19 PCH_GPIO28
USB_OC#0
USB_OC#1
PCH_GPIO28
SRN10KJ-6-GP
USB_OC#0 32
USB_OC#1 32
USB_OC#3 19
USB_OC#4 19,32
Pair Device
0 NC
1 USB3
2 USB1
3 WLAN
4 Card Reader
5 WWAN
6 Disable (HM55)
7 Disable (HM55)
8 USB2
9 Blue Tooth
10 Finger Print
11 NC
12 Express Card
13 Camera
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
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Title
PCH (5/9)-PCI / USB
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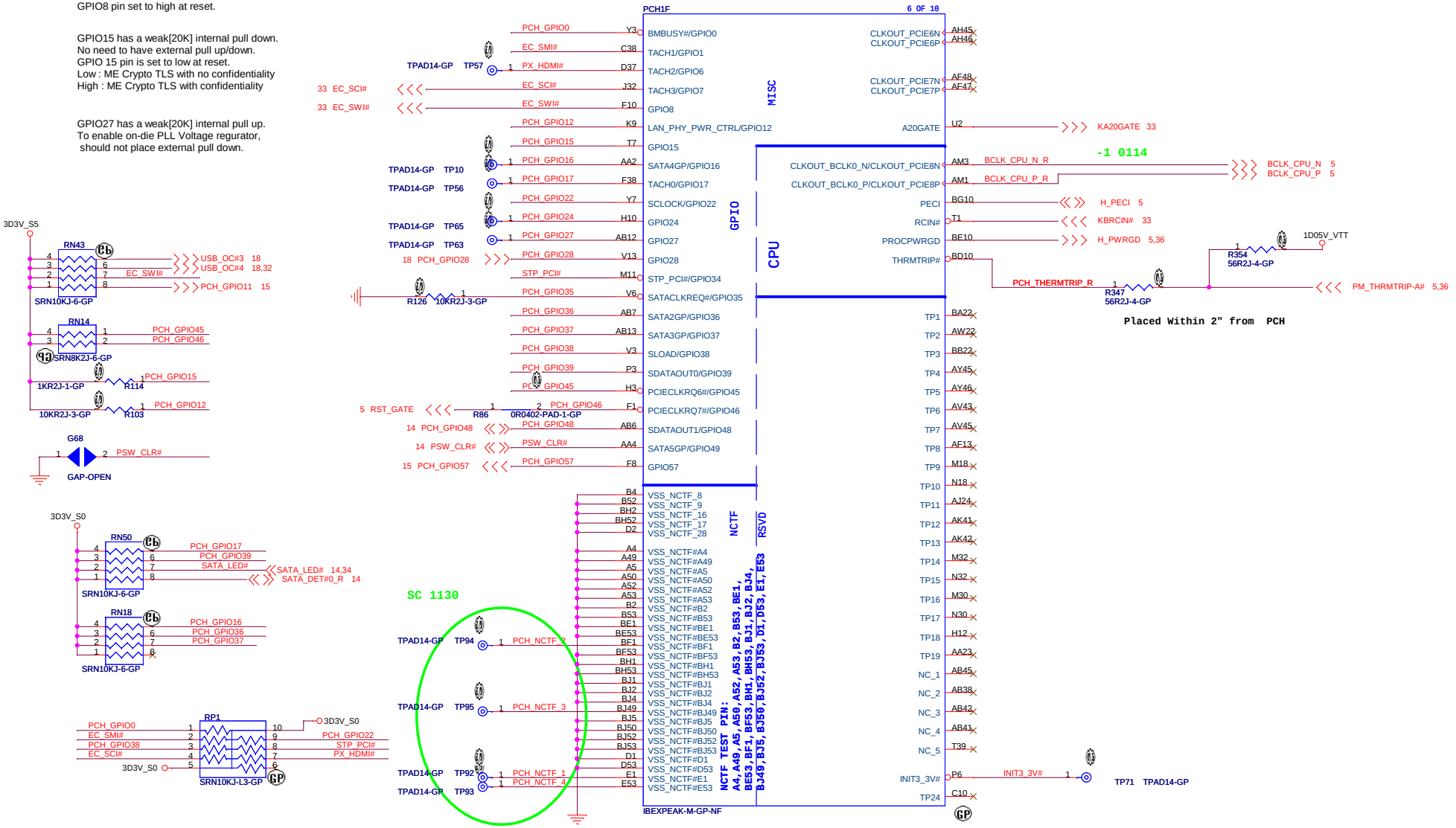
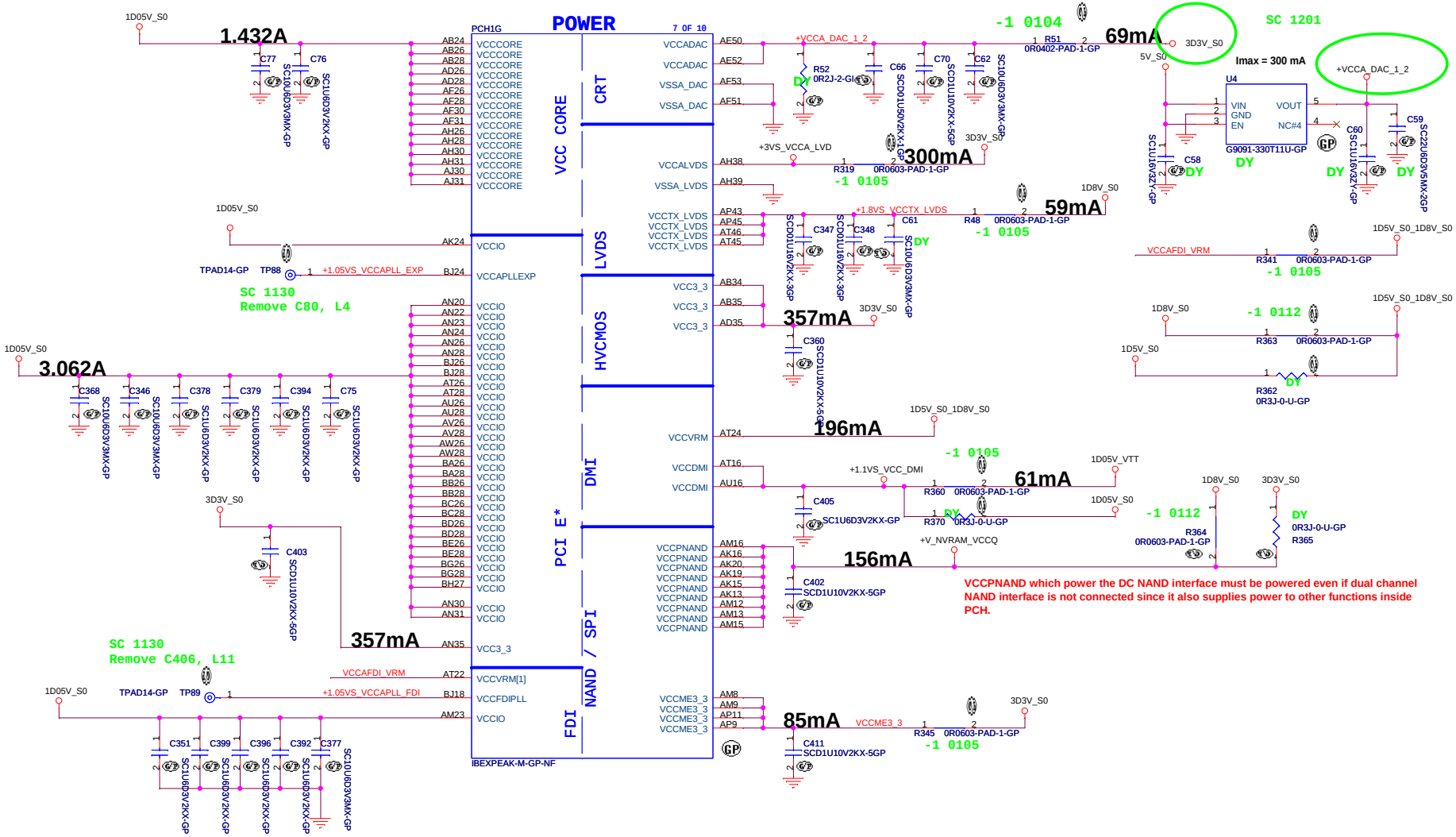
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

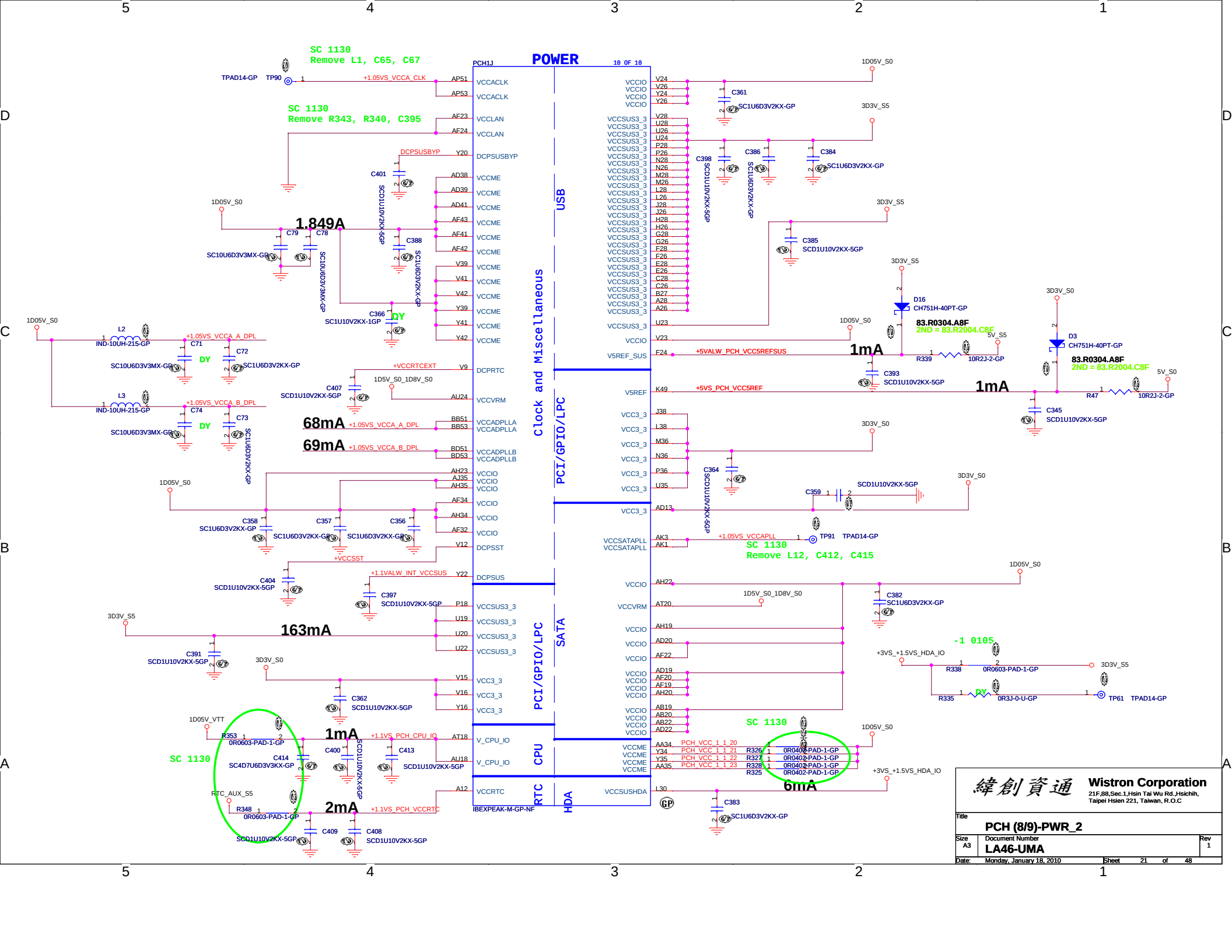
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



緯創資通	Wistron Corporation		
	21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C		
Title	PCH (6/9)-GPIO/VSS_NCTF/RSVD		
Size A3	Document Number LA46-UMA	Rev 1	
Date: Monday, January 18, 2010	Sheet 19 of 48		



Wistron Corporation	緯創資通
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title: PCH (7/9)-PWR_1	
Size: A3	Document Number: LA46-UMA
Rev: 1	
Date: Monday, January 18, 2010	Sheet 20 of 48


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
SC 1130
Remove L1, C65, C67
SC 1130
Remove R343, R340, C395
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
SC 1130
Remove L12, C412, C415
SC 1130
SC 1130
-1 0105
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
PCH (8/9)-PWR_2
Size A3
Document Number
LA46-UMA
Rev 1
Date: Monday, January 18, 2010
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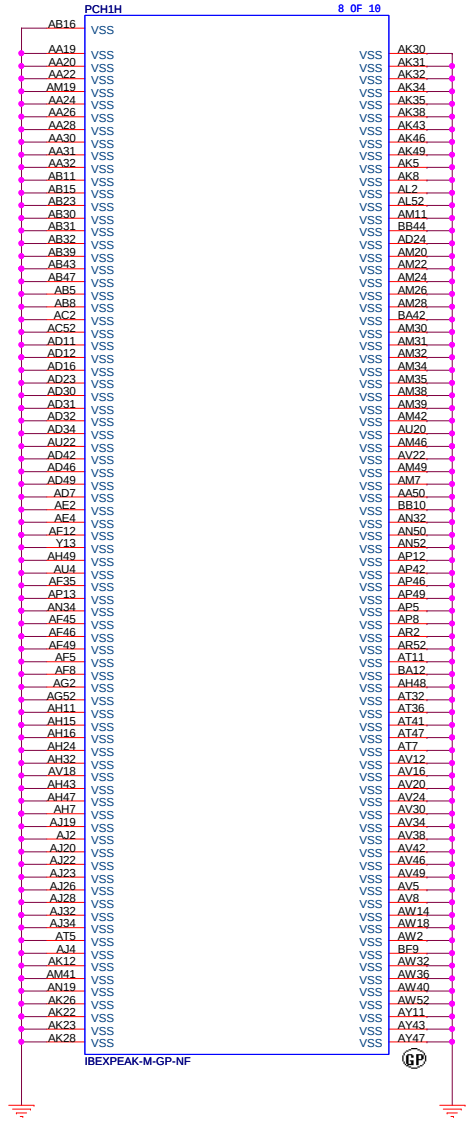

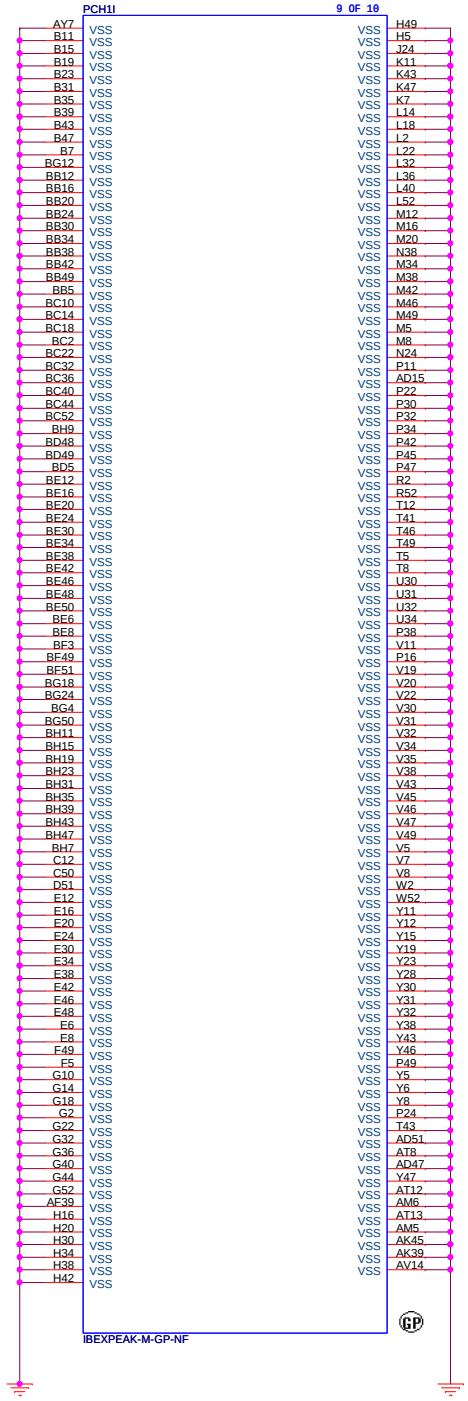

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title
PCH (9/9)-VSS

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5 4 3 2 1

D

C

B

A

緯創資通 **Wistron Corporation**
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: N/A		
Size: A2	Document Number: LA46-UMA	Rev: 1
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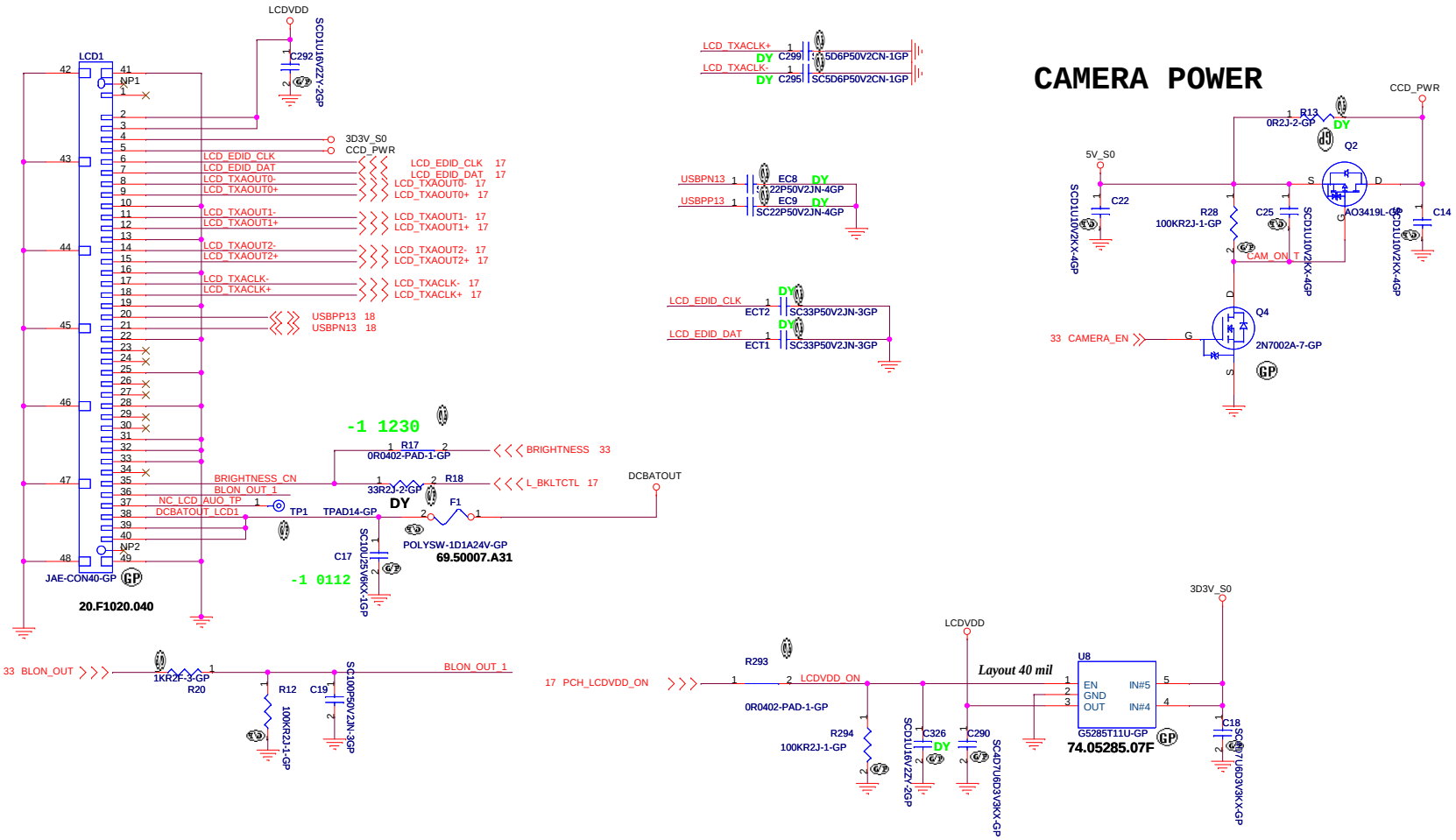
5 4 3 2 1

LCD/INVERTER/CCD CONN



Wistron Corporation	緯創資通
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	

Title: LCD & CCD

Size	Document Number	Rev
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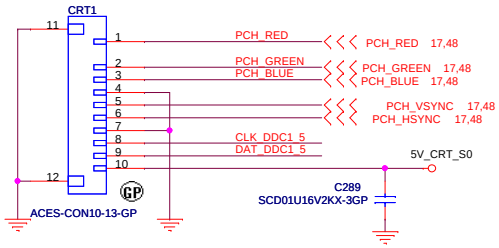
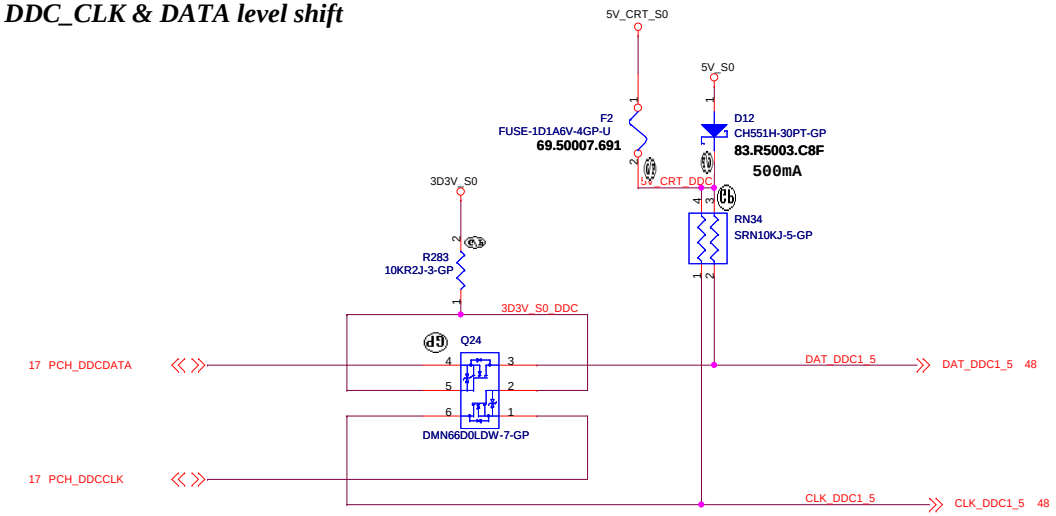


DDC_CLK & DATA level shift



緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title: CRT		
Size: A3	Document Number: LA46-UMA	Rev: 1
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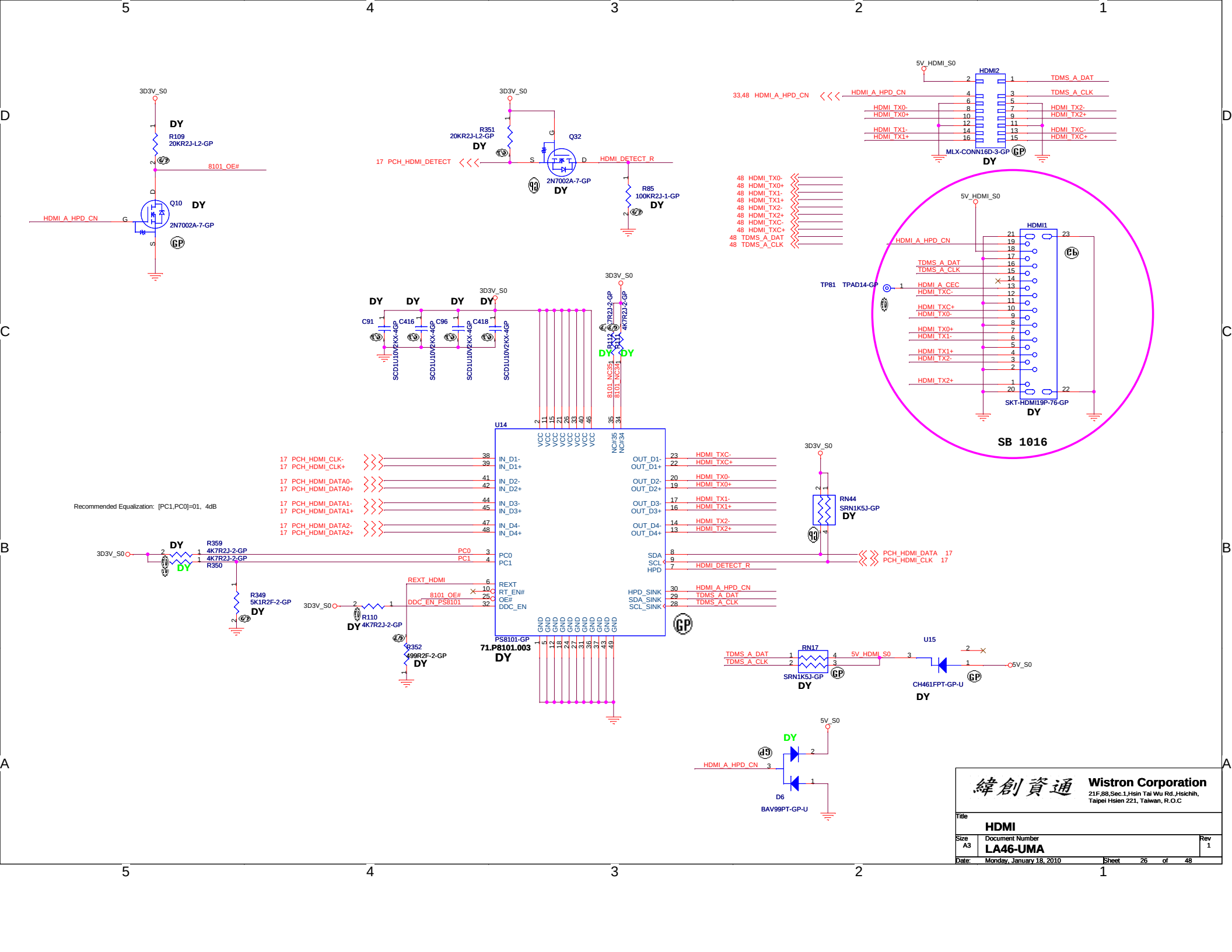
3D3V_S0
R109
20KR2J-L2-GP
DY
8101_OE#
Q10
2N7002A-7-GP
HDMI_A_HPD_CN
R351
20KR2J-L2-GP
Q32
2N7002A-7-GP
17 PCH_HDMI_DETECT
HDMI_DETECT_R
R85
100KR2J-1-GP
5V_HDMI_S0
HDMI2
MLX-CONN16D-3-GP
33,48 HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
HDMI_TXC-
HDMI_TXC+
48 HDMI_TX0-
48 HDMI_TX0+
48 HDMI_TX1-
48 HDMI_TX1+
48 HDMI_TX2-
48 HDMI_TX2+
48 HDMI_TXC-
48 HDMI_TXC+
48 TDMS_A_DAT
48 TDMS_A_CLK
HDMI1
SKT-HDMI19P-76-GP
TP81 TPAD14-GP
HDMI_A_CEC
SB 1016
C91
C416
C96
C418
SCD1U10V2KX-4GP
R412
R411
4K7R2J-2-GP
8101_NC35
8101_NC34
U14
PS8101-GP
71.P8101.003
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
17 PCH_HDMI_CLK-
17 PCH_HDMI_CLK+
17 PCH_HDMI_DATA0-
17 PCH_HDMI_DATA0+
17 PCH_HDMI_DATA1-
17 PCH_HDMI_DATA1+
17 PCH_HDMI_DATA2-
17 PCH_HDMI_DATA2+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
HDMI_TXC-
HDMI_TXC+
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
Recommended Equalization: [PC1,PC0]=01, 4dB
R359
4K7R2J-2-GP
R350
R349
5K1R2F-2-GP
PC0
PC1
REXT_HDMI
REXT
RT_EN#
OE#
DDC_EN
8101_OE#
DDC_EN_PS8101
R110
4K7R2J-2-GP
R352
99R2F-2-GP
SDA
SCL
HPD
HDMI_DETECT_R
HPD_SINK
SDA_SINK
SCL_SINK
HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
RN44
SRN1K5J-GP
PCH_HDMI_DATA 17
PCH_HDMI_CLK 17
RN17
U15
CH461FPT-GP-U
5V_S0
D6
BAV99PT-GP-U
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
HDMI
Size
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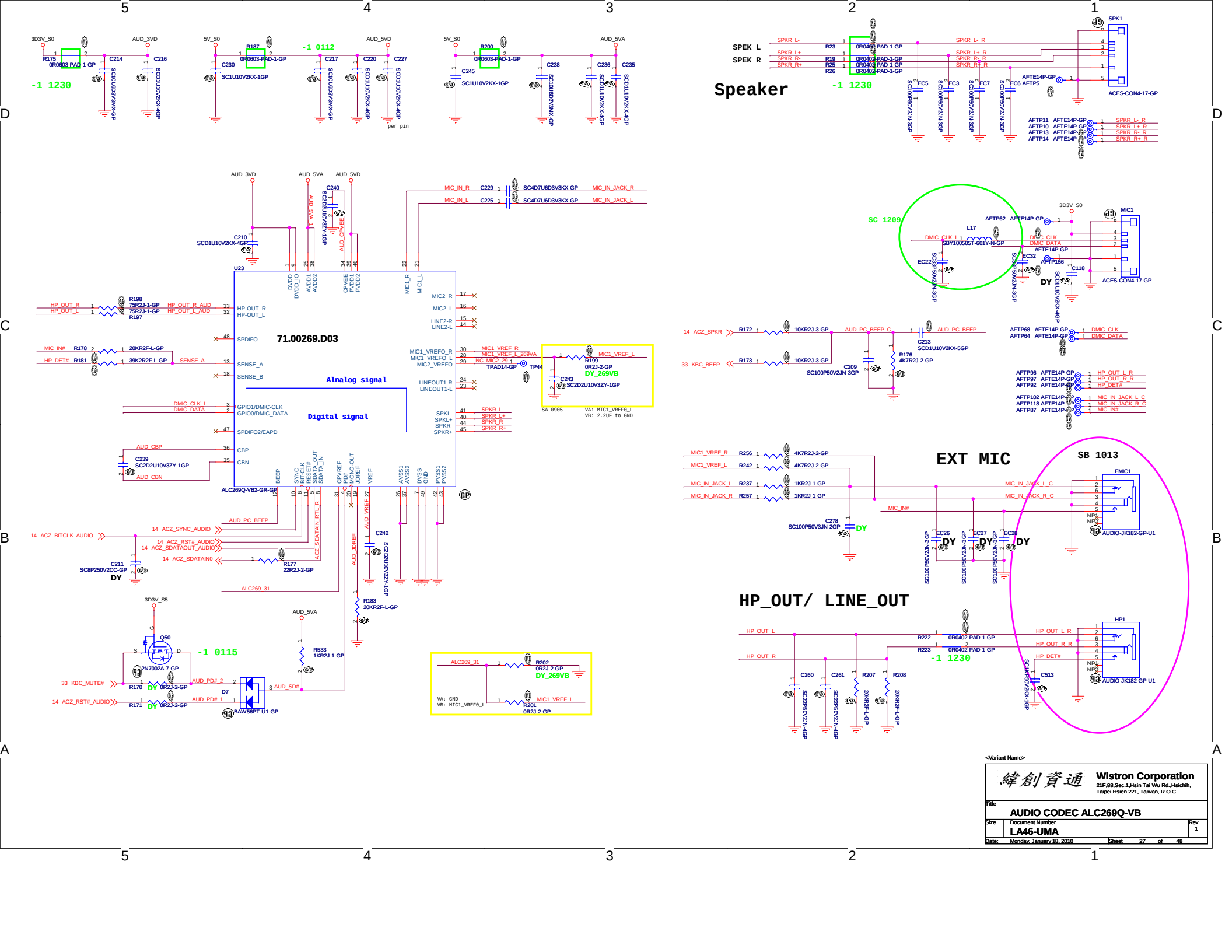
Speaker
EXT MIC
HP_OUT/ LINE_OUT
71.00269.D03
Alnalog signal
Digital signal
ALC269Q-VB2-GR-GP
SPK1
ACES-CON4-17-GP
MIC1
AUDIO-JK182-GP-U1
EMIC1
HP1
SB 1013
SC 1209
-1 1230
-1 0112
-1 0115
DY
DY_269VB
per pin
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
AUDIO CODEC ALC269Q-VB
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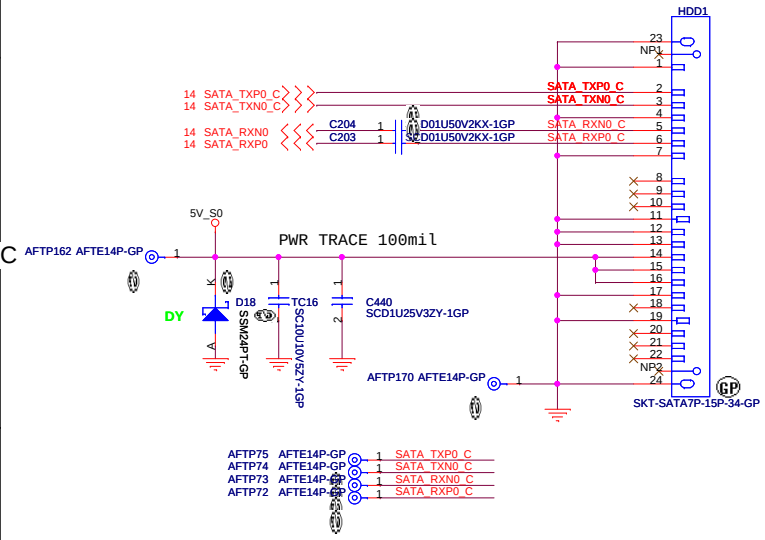
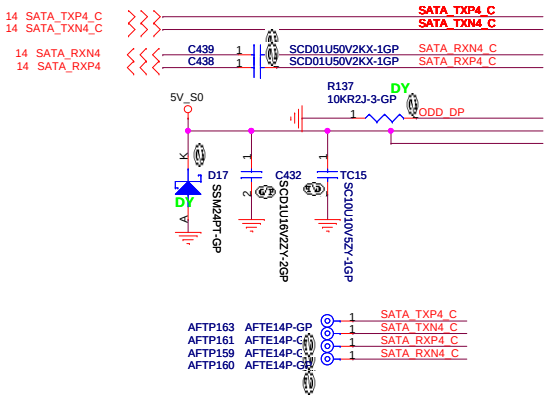
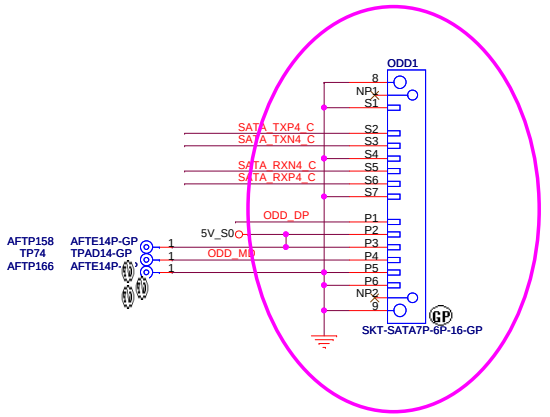
SATA Connector



ODD Connector



SB 1016



緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title: HDD & ODD		
Size: A3	Document Number: LA46-UMA	Rev: 1
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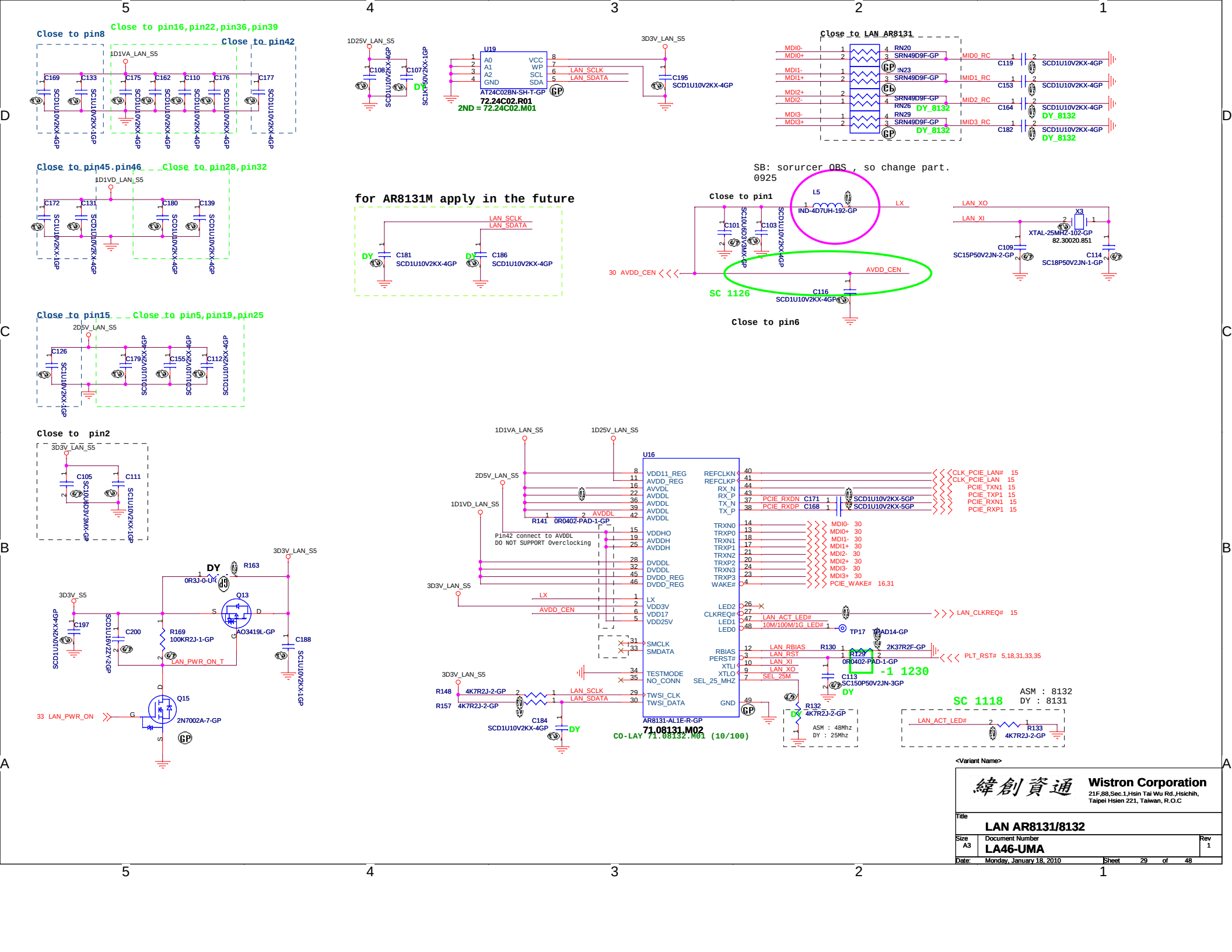
Close to pin8
Close to pin16,pin22,pin36,pin39
Close to pin42
1D1VA_LAN_S5
C169 C133 C175 C162 C110 C176 C177
SCD1U10V2KX-4GP
SC1U10V2KX-1GP
1D25V_LAN_S5
C108 C107
SCD1U10V2KX-4GP
SC1KP50V2KX-1GP
DY
U19
A0 A1 A2 GND VCC WP SCL SDA
LAN_SCLK
LAN_SDATA
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
3D3V_LAN_S5
C195
SCD1U10V2KX-4GP
Close to LAN_AR8131
MDI0- MDI0+ MDI1- MDI1+ MDI2+ MDI2- MDI3- MDI3+
RN20 SRN49D9F-GP
RN23 SRN49D9F-GP
RN26 SRN49D9F-GP
RN29 SRN49D9F-GP
DY_8132
MDI0_RC MDI1_RC MDI2_RC MDI3_RC
C119 C153 C164 C182
SCD1U10V2KX-4GP
Close to pin45,pin46
Close to pin28,pin32
1D1VD_LAN_S5
C172 C131 C180 C139
SC1U10V2KX-1GP
SCD1U10V2KX-4GP
for AR8131M apply in the future
LAN_SCLK
LAN_SDATA
DY
C181 C186
SCD1U10V2KX-4GP
SB: sorurcer OBS , so change part.
0925
Close to pin1
L5
IND-4D7UH-192-GP
LX
C101 C103
SC10U6D3V3MX-GP
SCD1U10V2KX-4GP
30 AVDD_CEN
AVDD_CEN
SC 1126
C116
SCD1U10V2KX-4GP
Close to pin6
LAN_XO
LAN_XI
X3
XTAL-25MHZ-102-GP
82.30020.851
C109
SC15P50V2JN-2-GP
C114
SC18P50V2JN-1-GP
Close to pin15
Close to pin5,pin19,pin25
2D5V_LAN_S5
C126 C179 C155 C112
SC1U10V2KX-1GP
SCD1U10V2KX-4GP
Close to pin2
3D3V_LAN_S5
C105 C111
SC10U6D3V3MX-GP
SC1U10V2KX-1GP
DY
R163
0R3J-0-U-GP
Q13
AO3419L-GP
C197 C200
R169
100KR2J-1-GP
LAN_PWR_ON_T
C188
SCD1U16V2ZY-2GP
Q15
2N7002A-7-GP
33 LAN_PWR_ON
1D1VA_LAN_S5
1D25V_LAN_S5
2D5V_LAN_S5
1D1VD_LAN_S5
3D3V_LAN_S5
U16
VDD11_REG AVDD_REG AVDDL AVDDL AVDDL AVDDL AVDDL AVDDL
VDDHO AVDDH AVDDH
DVDDL DVDDL DVDD_REG DVDD_REG
LX VDD3V VDD17 VDD25V
SMCLK SMDATA
TESTMODE NO_CONN
TWSI_CLK TWSI_DATA
GND
REFCLKN REFCLKP RX_N RX_P TX_N TX_P
TRXN0 TRXP0 TRXN1 TRXP1 TRXN2 TRXP2 TRXN3 TRXP3 WAKE#
LED2 CLKREQ# LED1 LED0
RBIAS PERST# XTLI XTLO SEL_25_MHZ
R141 0R0402-PAD-1-GP
Pin42 connect to AVDDL
DO NOT SUPPORT Overclocking
PCIE_RXDN C171
PCIE_RXDP C168
SCD1U10V2KX-5GP
CLK_PCIE_LAN# 15
CLK_PCIE_LAN 15
PCIE_TXN1 15
PCIE_TXP1 15
PCIE_RXN1 15
PCIE_RXP1 15
MDI0- 30
MDI0+ 30
MDI1- 30
MDI1+ 30
MDI2- 30
MDI2+ 30
MDI3- 30
MDI3+ 30
PCIE_WAKE# 16,31
LAN_CLKREQ# 15
LAN_ACT_LED#
10M/100M/1G_LED#
TP17 TPAD14-GP
LAN_RBIAS R130 2K37R2F-GP
LAN_RST R129 0R0402-PAD-1-GP
PLT_RST# 5,18,31,33,35
LAN_XI
LAN_XO
SEL_25M
C113 SC150P50V2JN-3GP
-1 1230
DY
R132 4K7R2J-2-GP
ASM : 48Mhz
DY : 25Mhz
SC 1118
ASM : 8132
DY : 8131
LAN_ACT_LED#
R133 4K7R2J-2-GP
R148 4K7R2J-2-GP
R157 4K7R2J-2-GP
LAN_SCLK
LAN_SDATA
C184 SCD1U10V2KX-4GP
DY
AR8131-AL1E-R-GP
71.08131.M02
CO-LAY 71.08132.M01 (10/100)
<Variant Name>
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
LAN AR8131/8132
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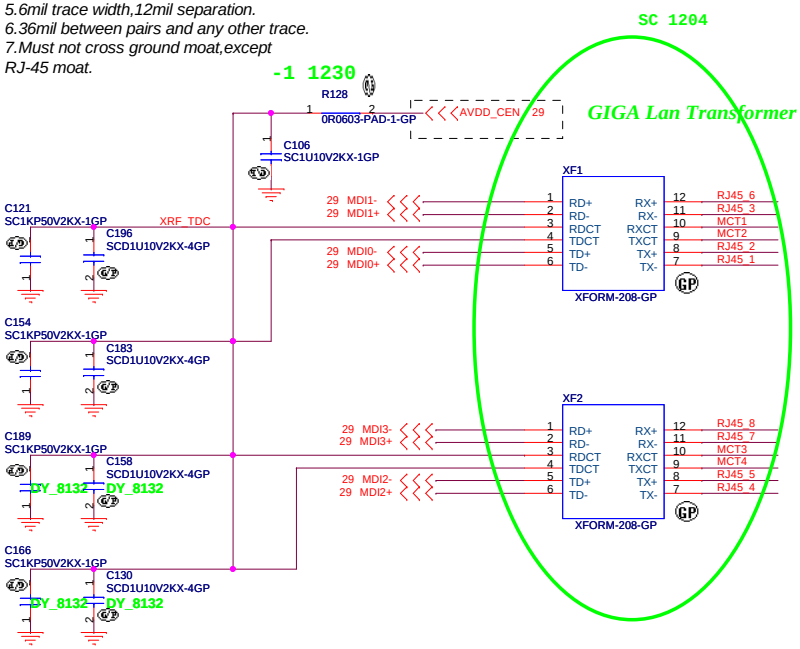
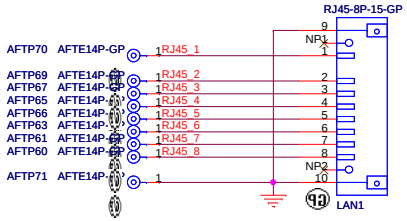
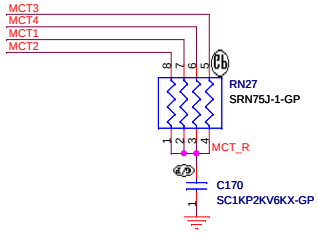
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector







<Variant Name>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: LAN CONN

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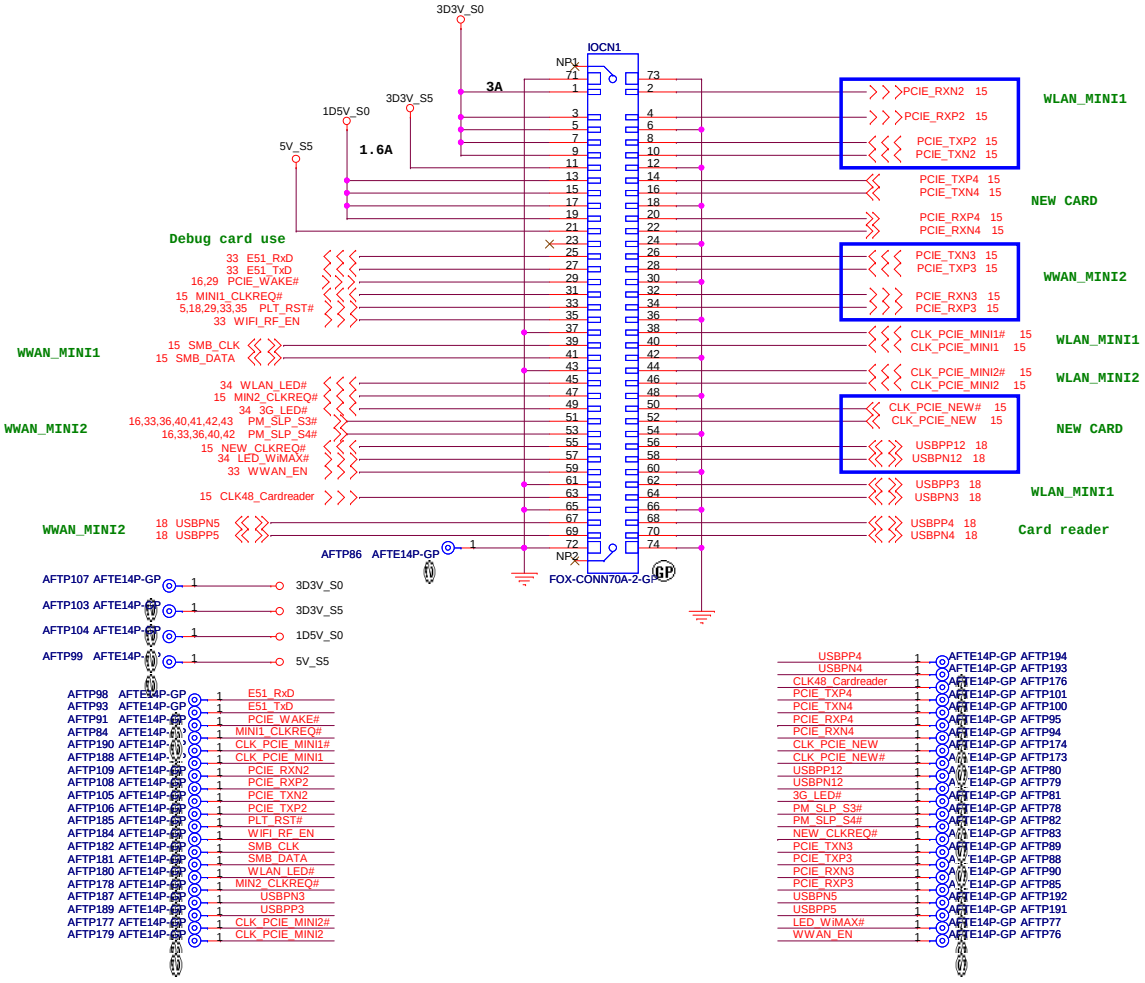
MOVE MINI CARD TO I/O BOARD



<Variant Name>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: IO CONN

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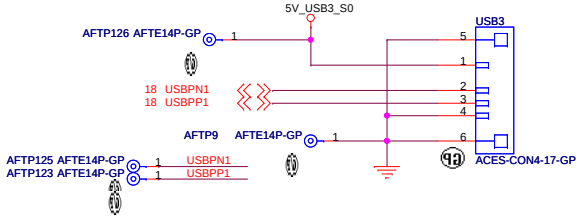
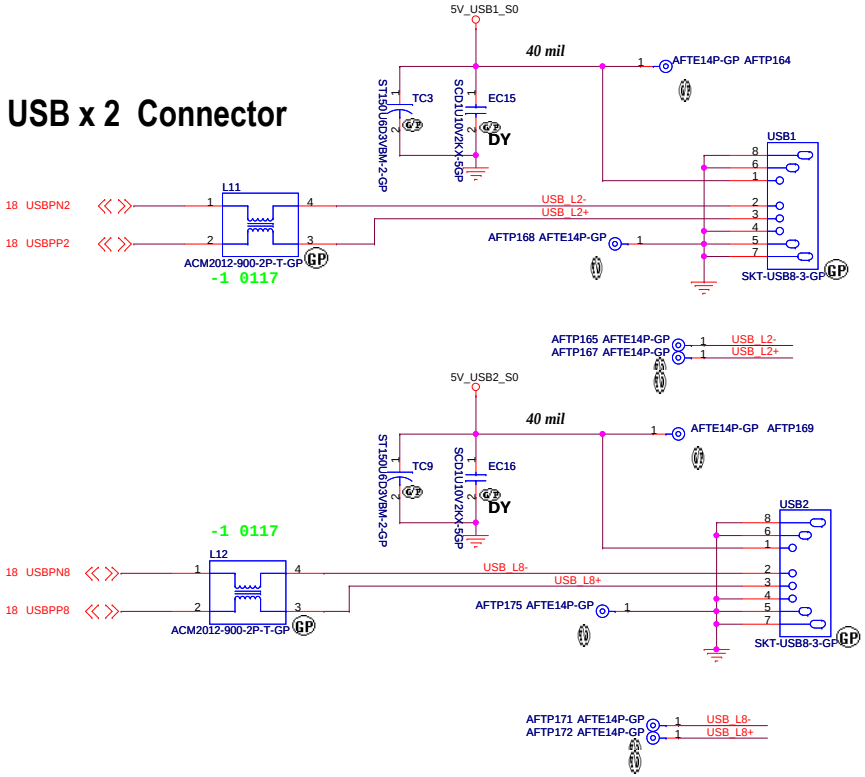
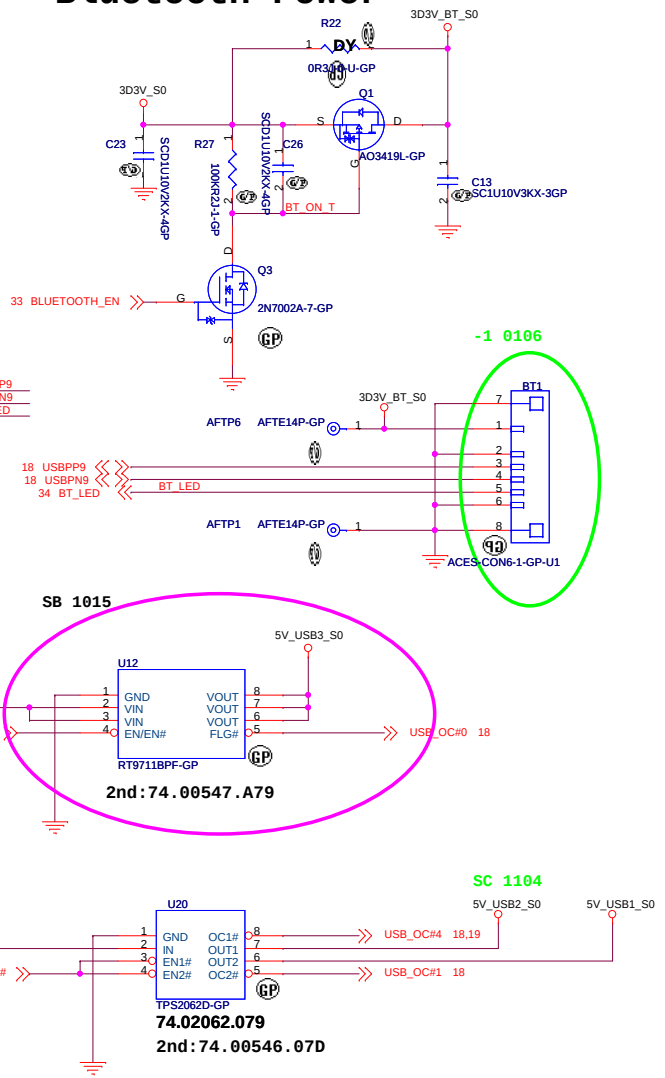
Should be in DC-IN board



USB x 2 Connector



Bluetooth Power



緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	USB & BT	
Size A3	Document Number LA46-UMA	Rev 1
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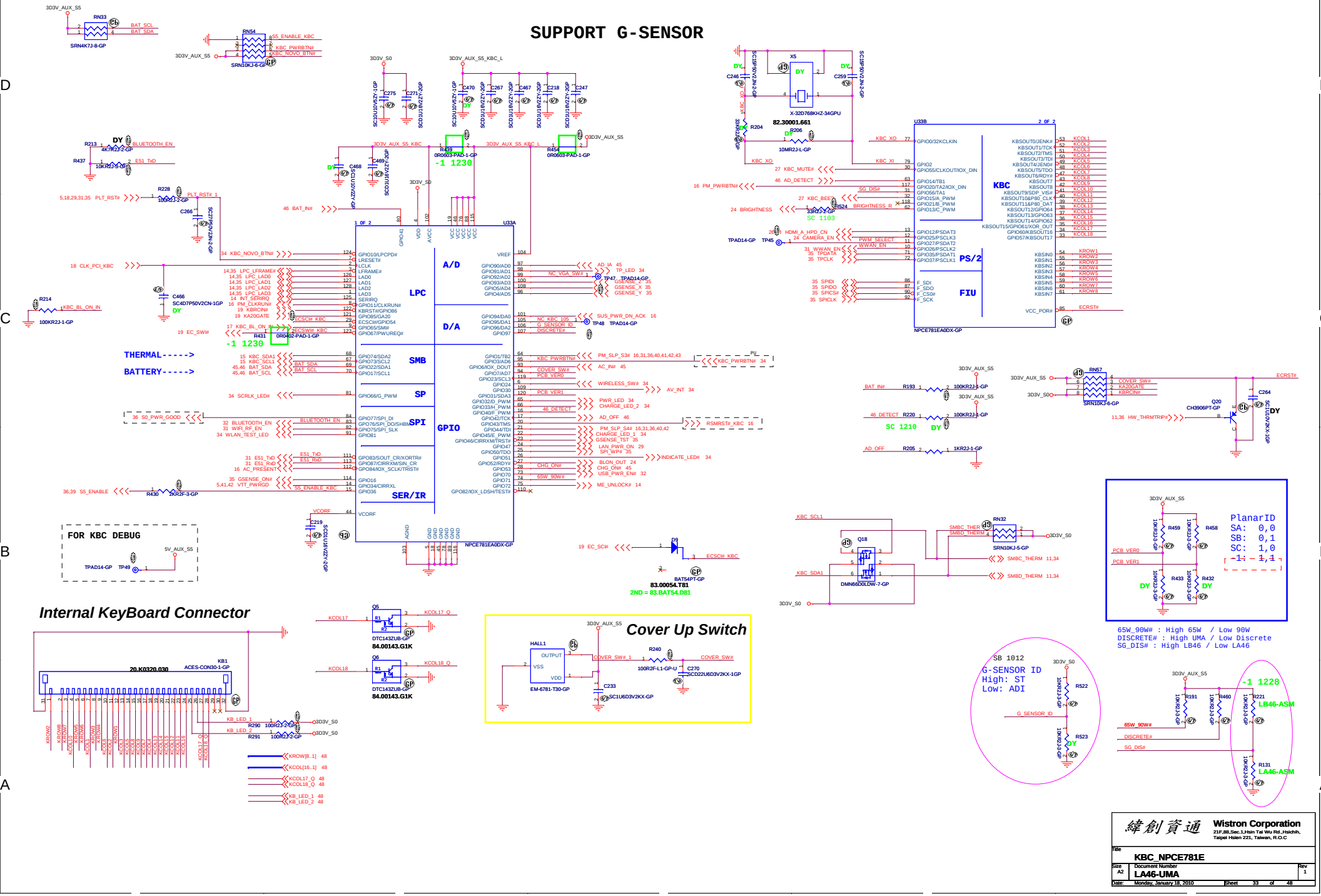
SUPPORT G-SENSOR



Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	KBC_NPCE781E	
Size A2	Document Number LA46-UMA	Rev 1
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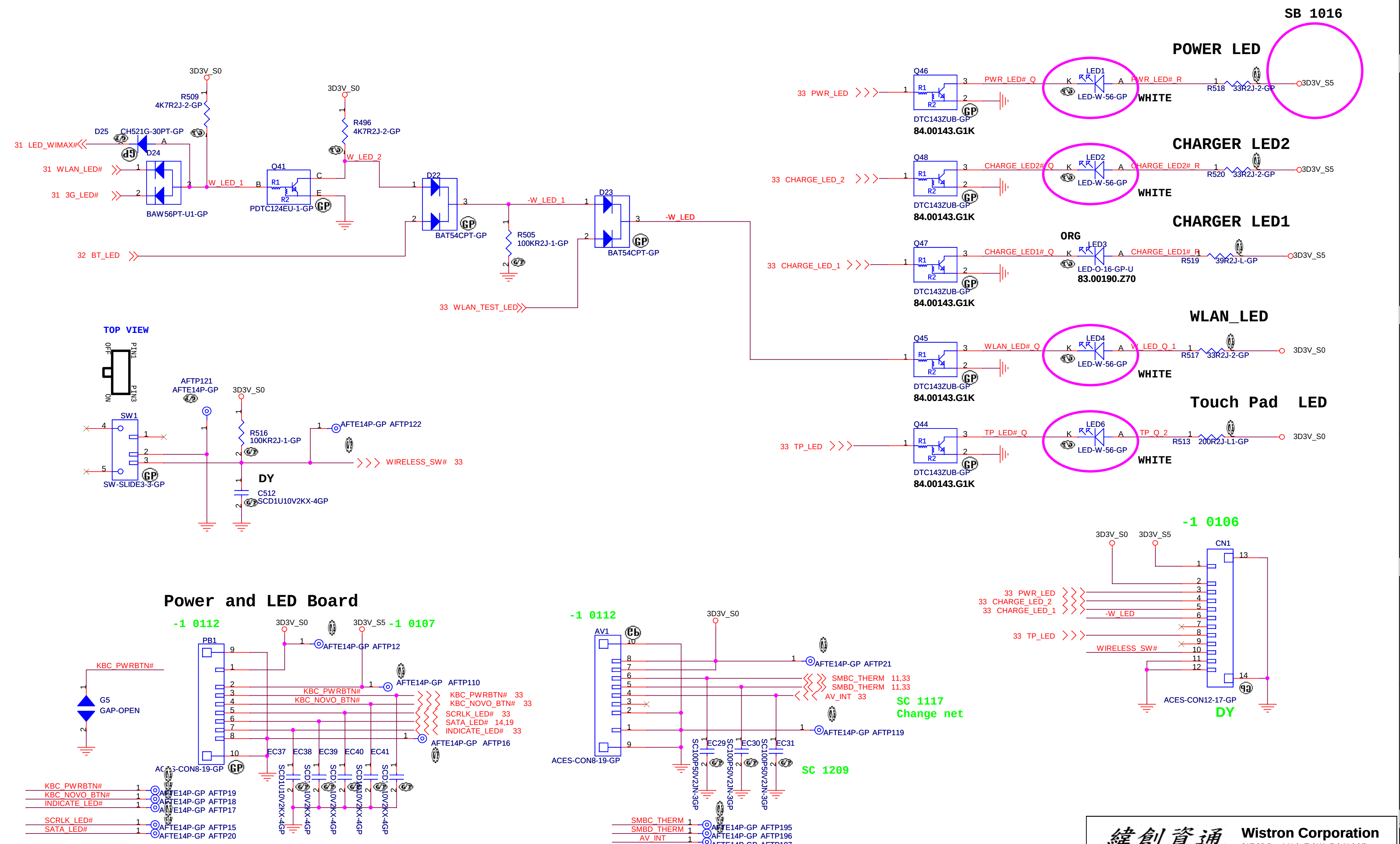

Wistron Corporation
緯創資通
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: LED_POWERBD CONN

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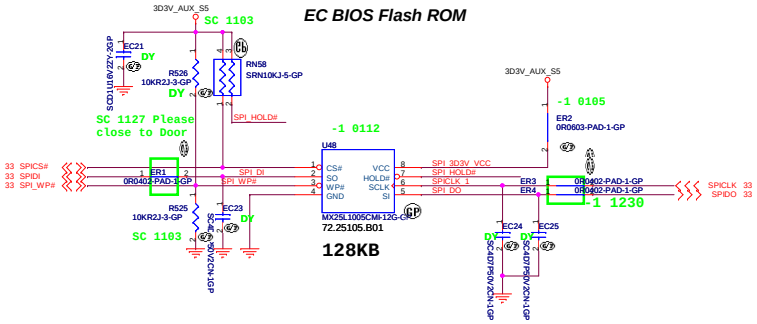
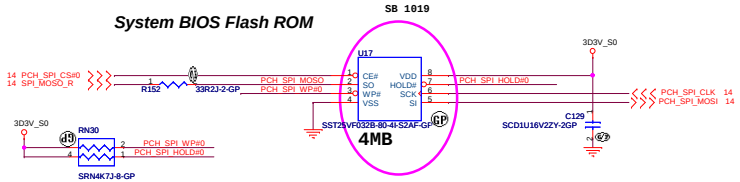
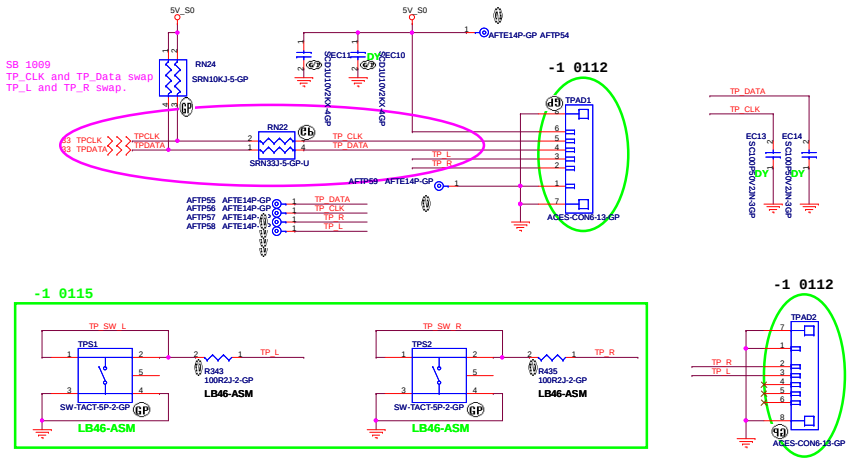
EC BIOS Flash ROM



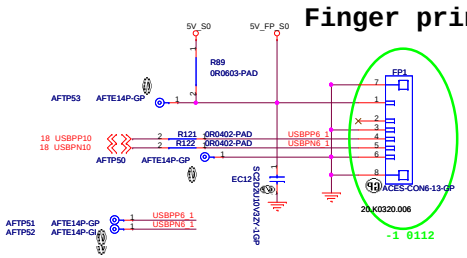
System BIOS Flash ROM



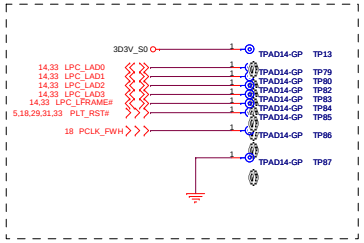
TOUCH PAD



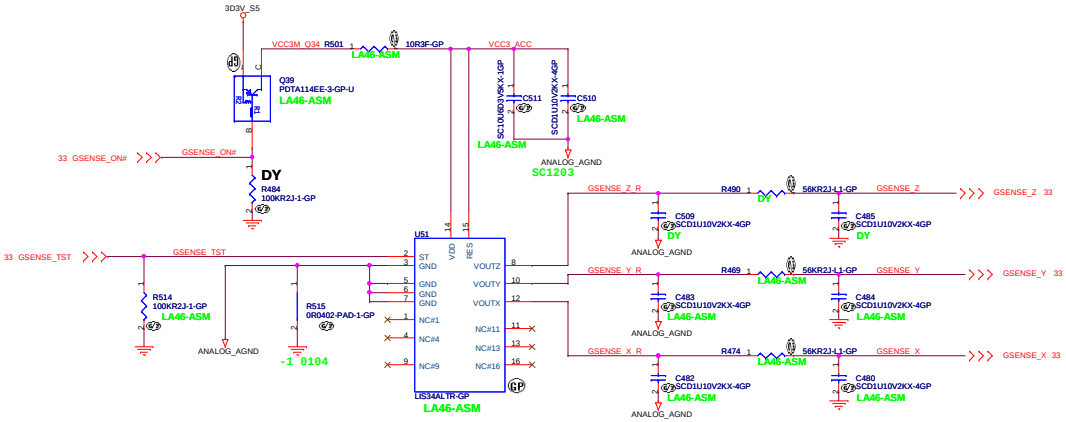
Finger printer



GOLDEN FINGER FOR DEBUG BOARD



G-Sensor



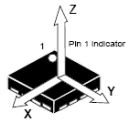
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: BIOS & TP & G-Sensor & FP
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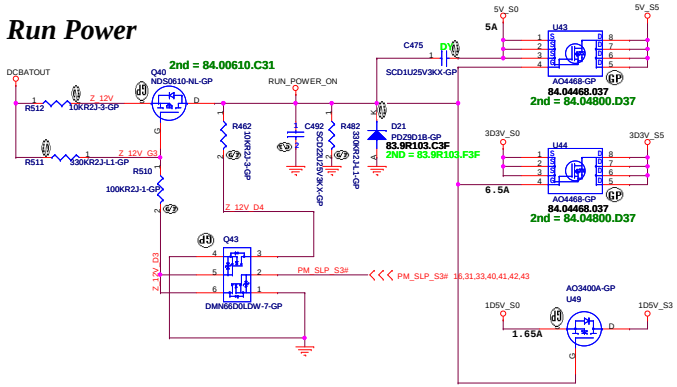
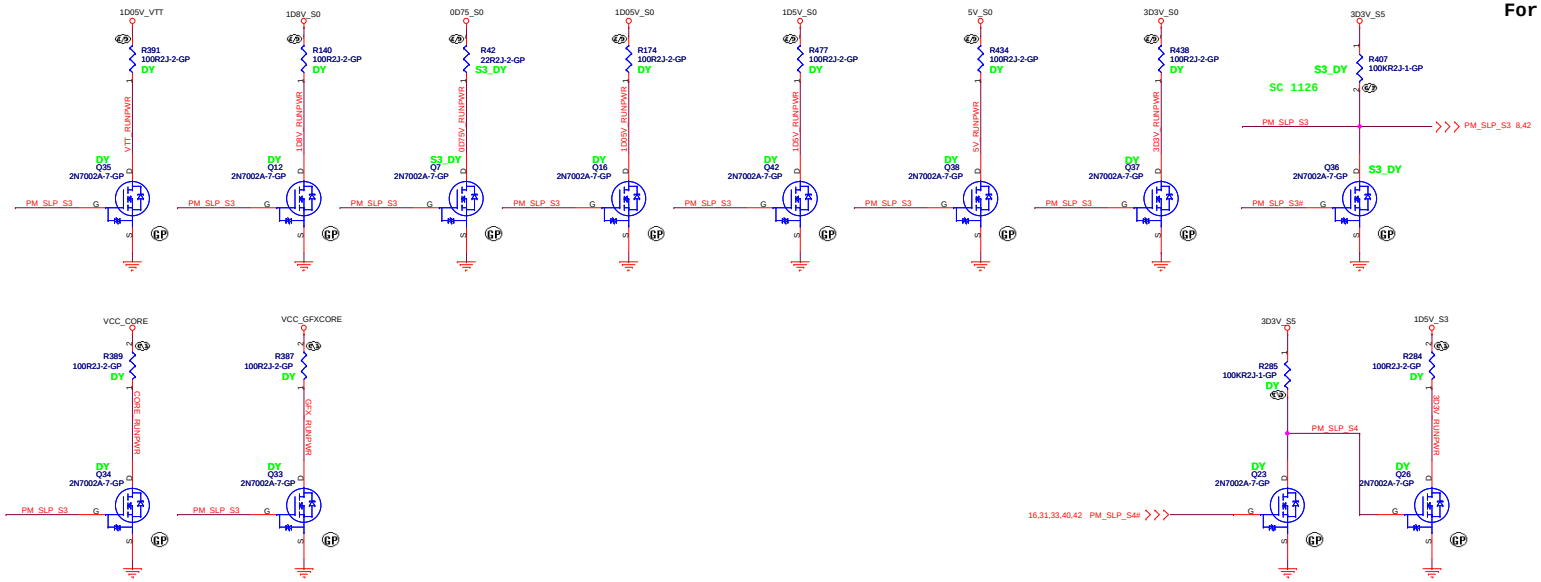
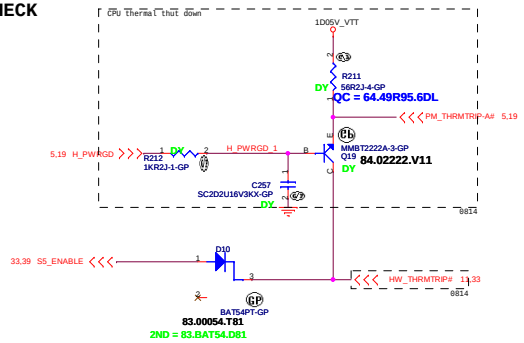
Run Power

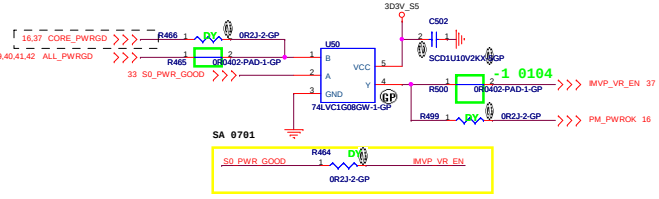


For Discharge



CHECK





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緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title: Run PWR		
Size: A2	Document Number: LA46-UMA	Rev: 1
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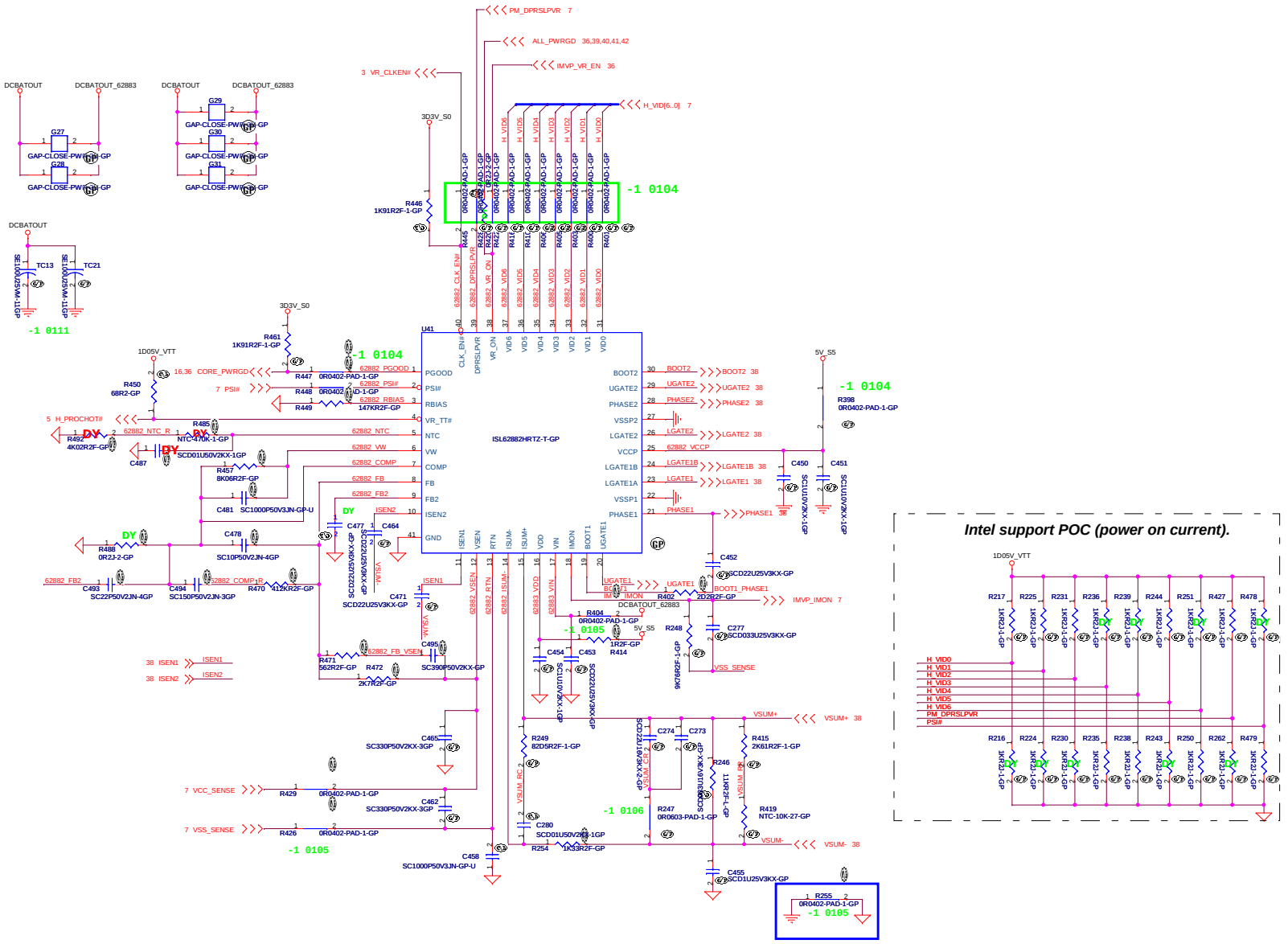

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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: ISL62882_CPU_CORE (1 of 2)

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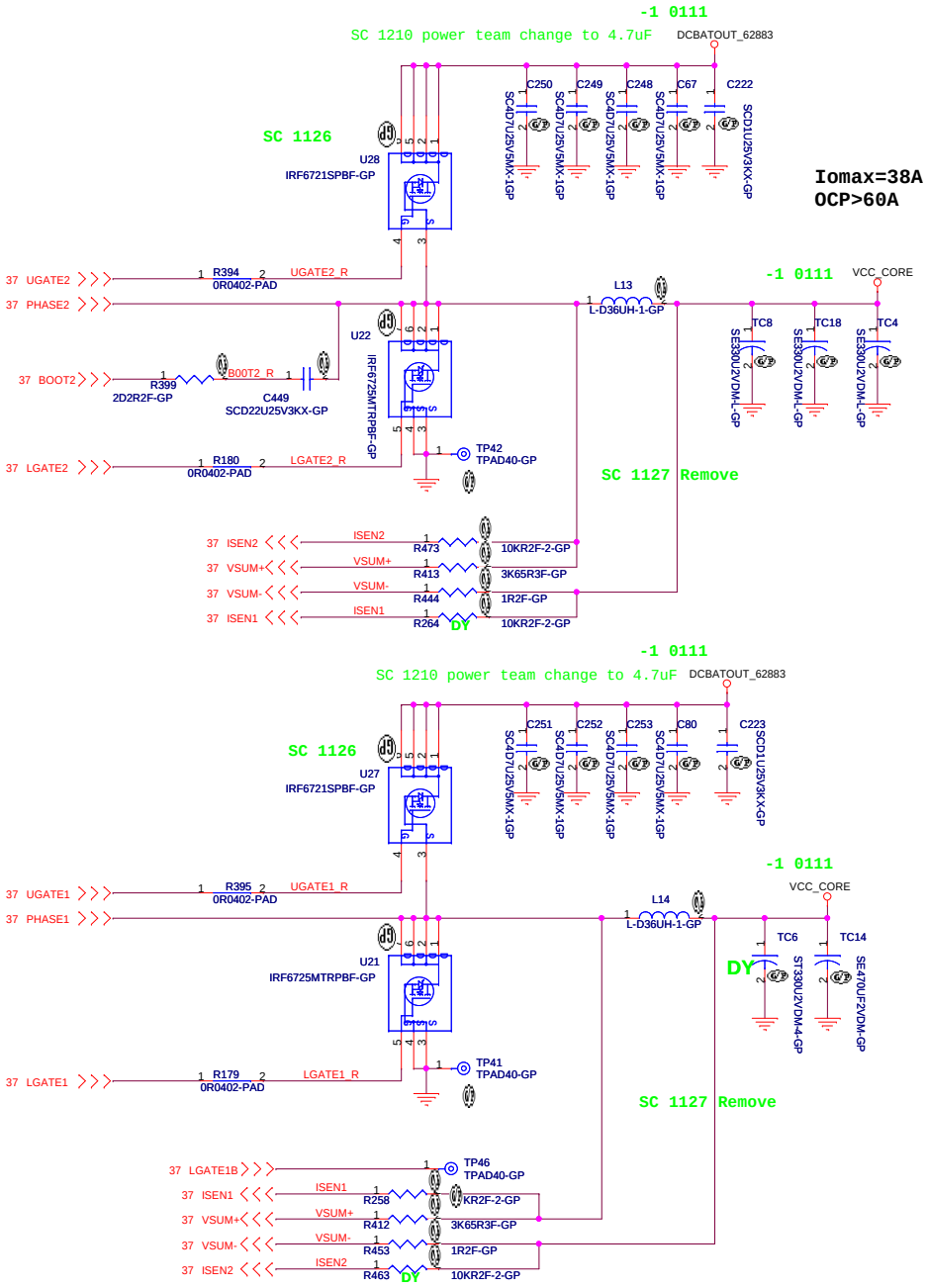

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緯創資通	**Wistron Corporation** 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
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Size: A3	Document Number: **LA46-UMA**
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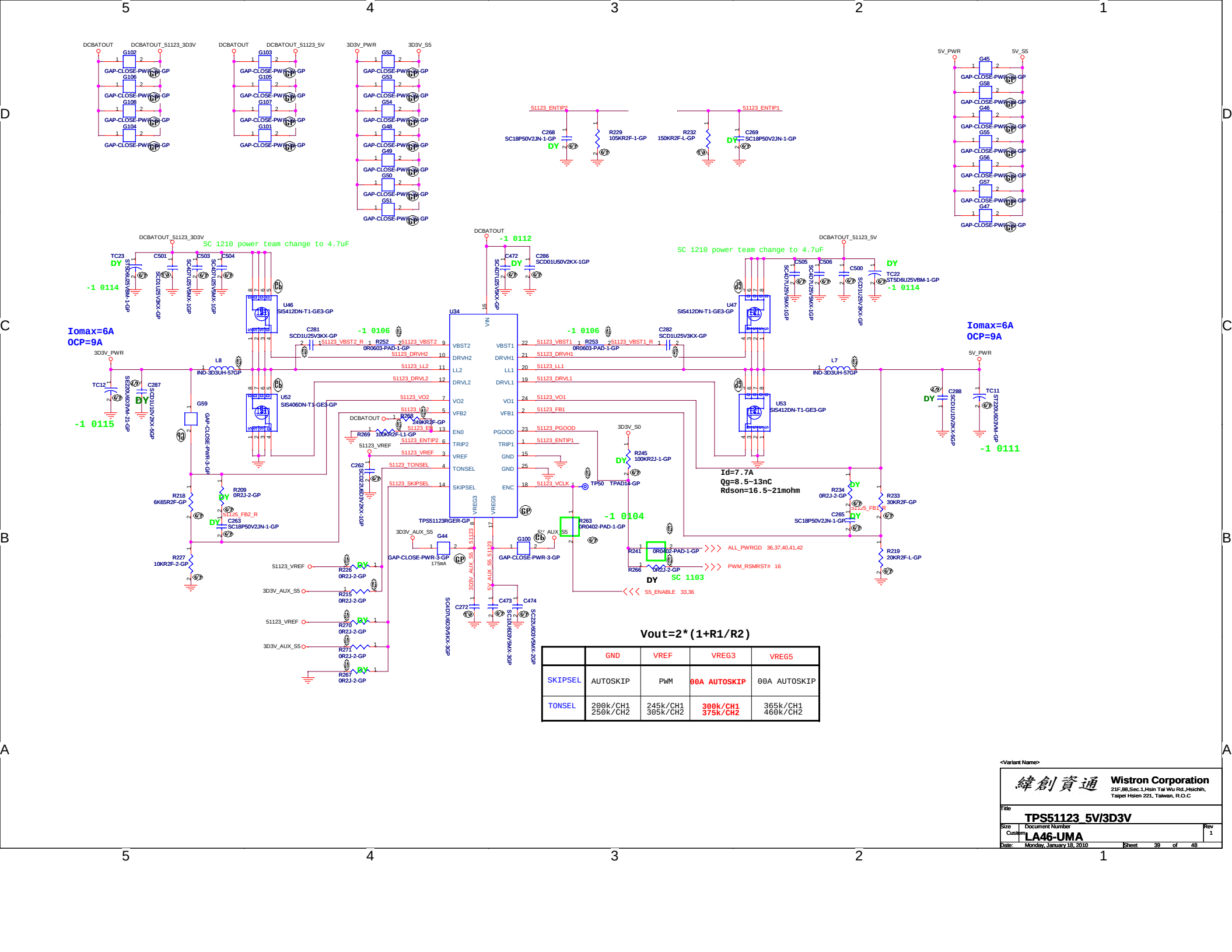
Date: Monday, January 18, 2010	Sheet 38 of 48



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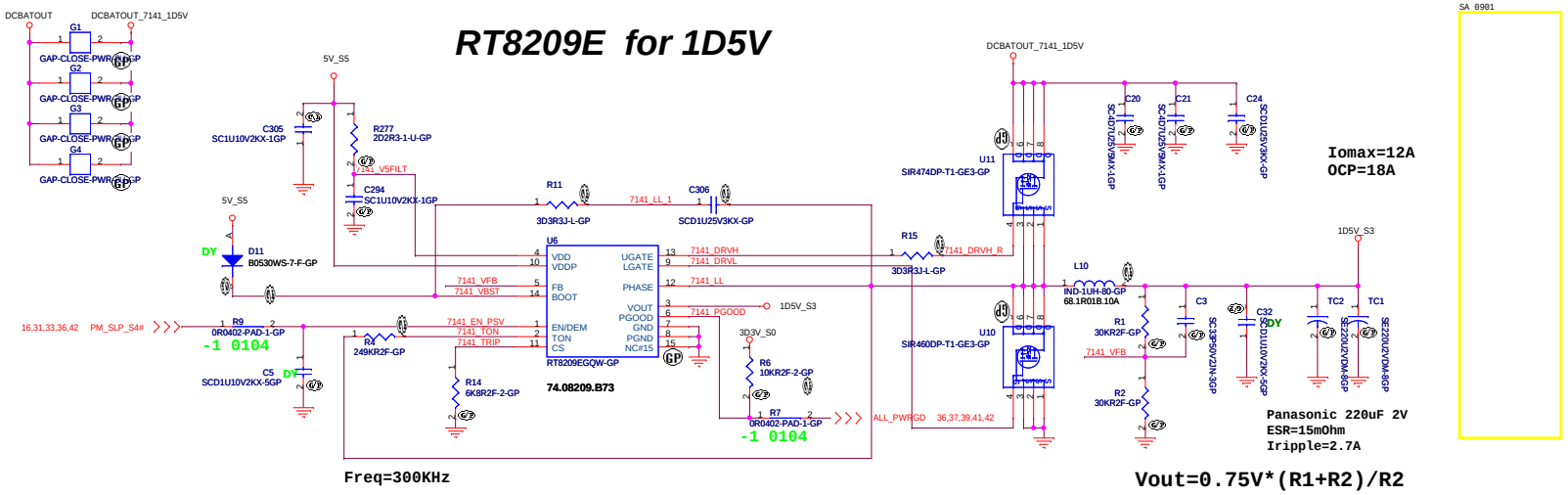
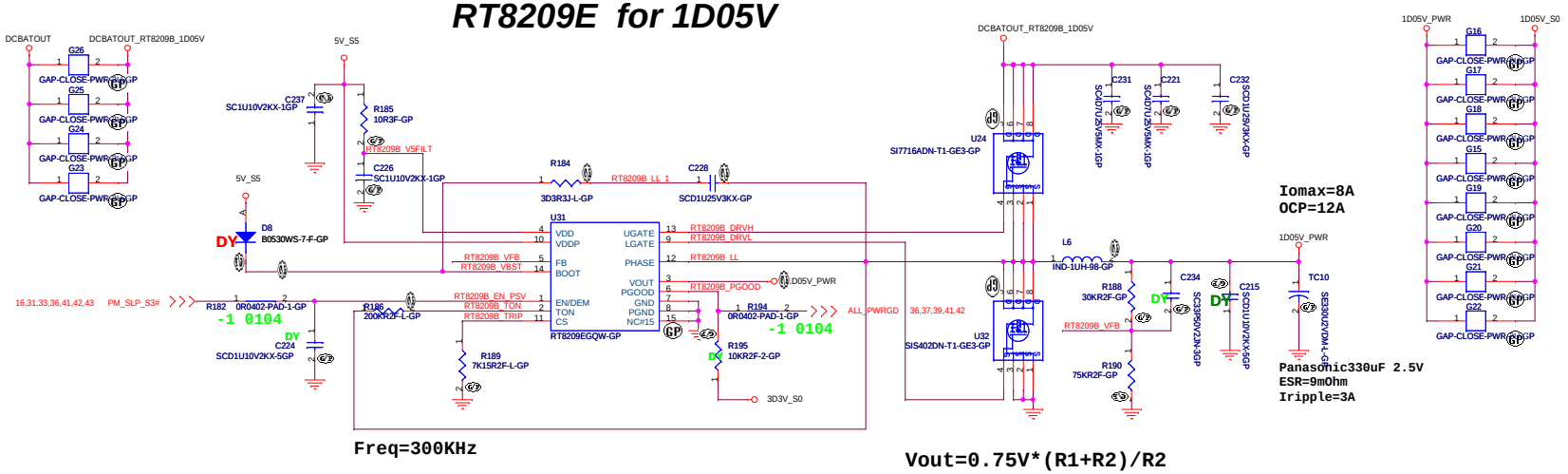
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

RT8209E for 1D5V



RT8209E for 1D05V



緯創資通 Wistron Corporation
21F.88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

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Title: RT8209E_1D5V / RT8209E_1D05V

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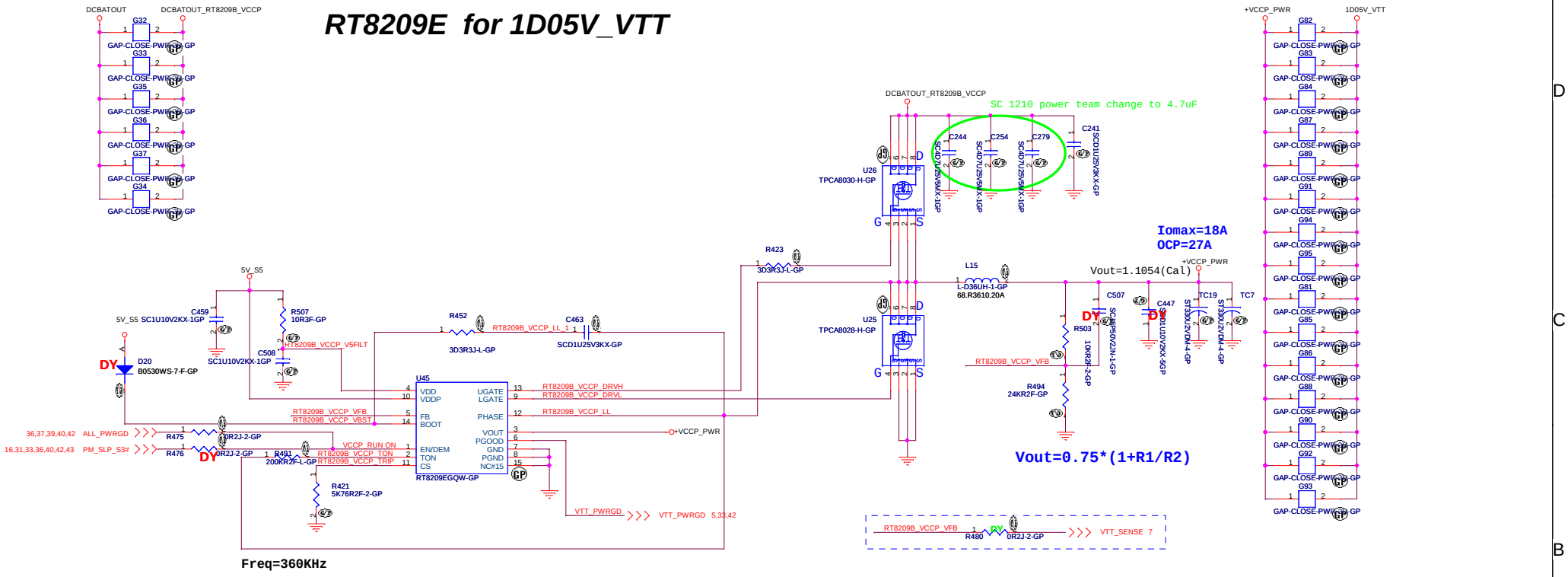
RT8209E for 1D05V_VTT



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緯創資通 Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C		
Title: RT8209E_1D05V_VTT		
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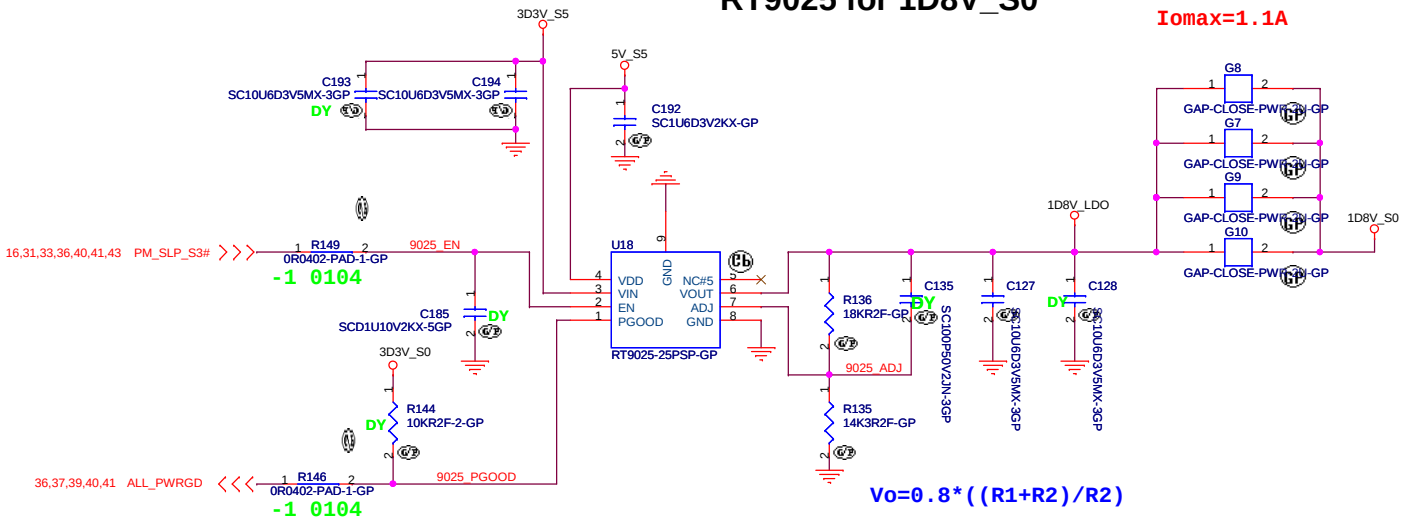
RT9025 for 1D8V_S0



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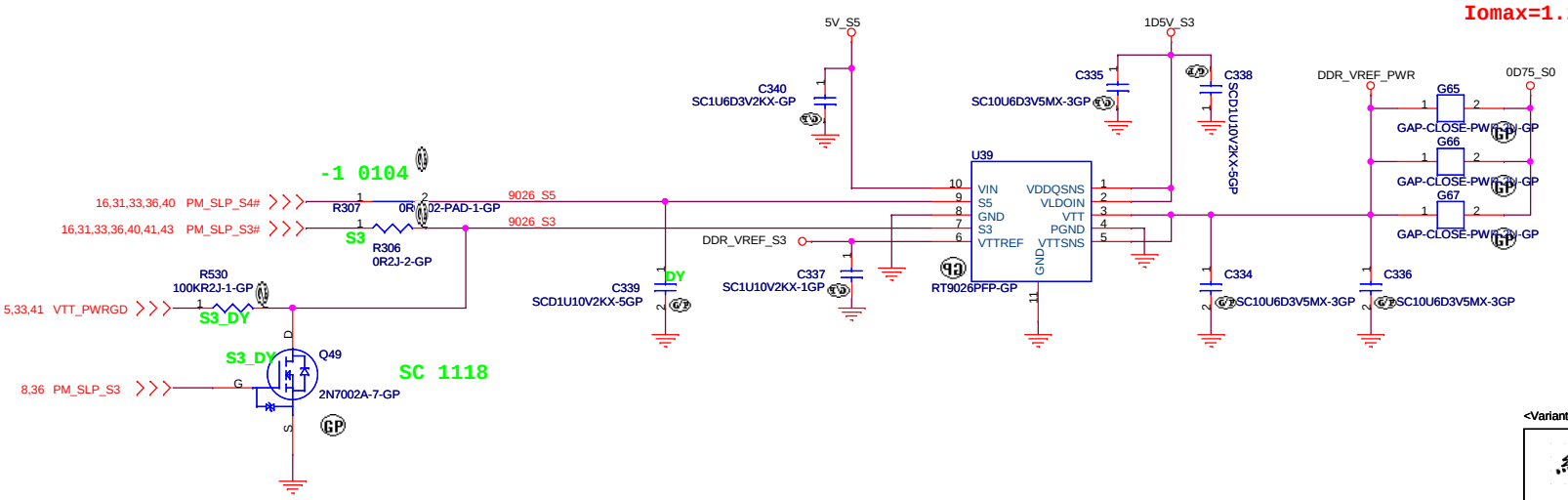

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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: RT9025_1D8V/ RT9026_0D75

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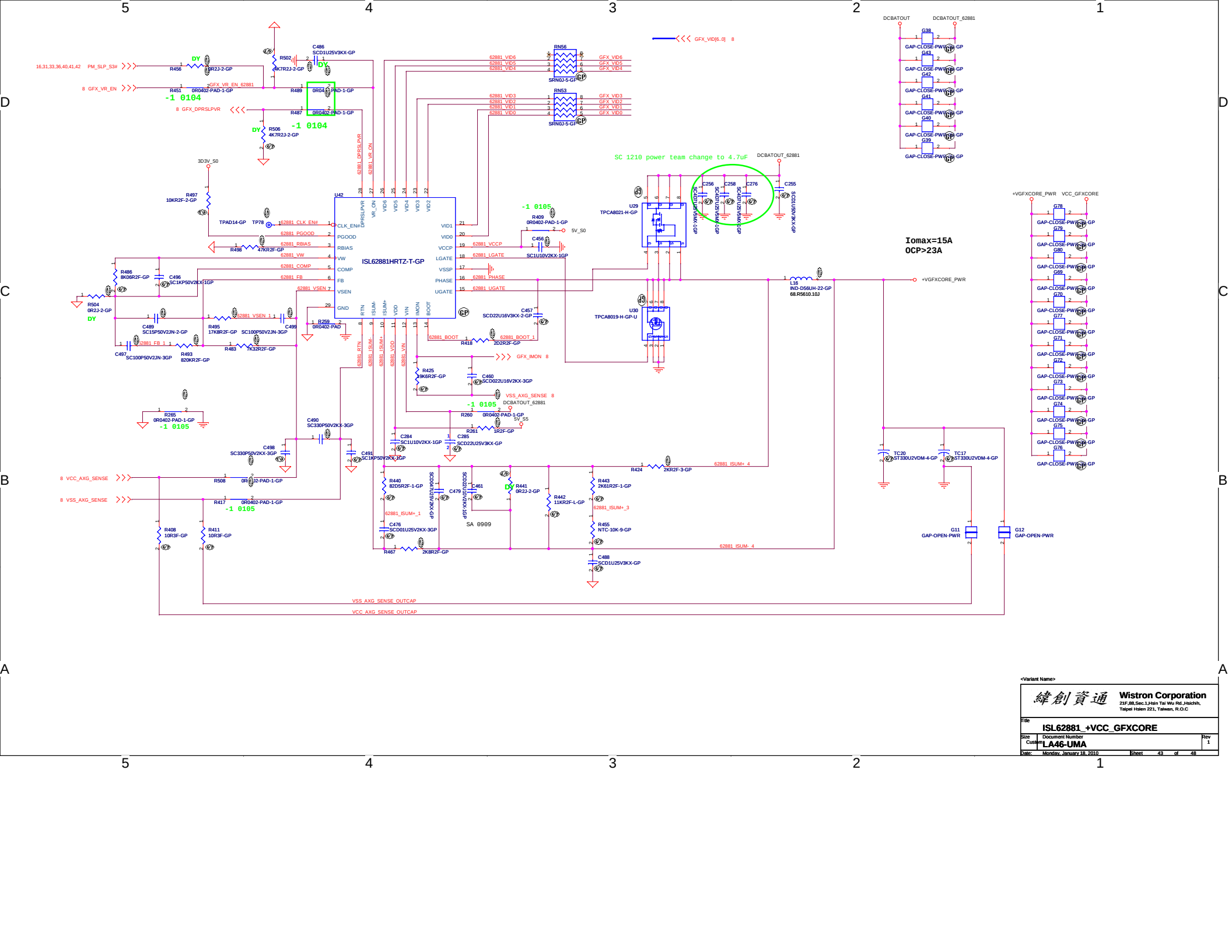
ISL62881HRTZ-T-GP
U42
SC 1210 power team change to 4.7uF
Iomax=15A
OCP>23A
-1 0104
-1 0105
DY
SA 0909
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
+VGFXCORE_PWR
VCC_GFXCORE
DCBATOUT
DCBATOUT_62881
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
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緯創資通 **Wistron Corporation**
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

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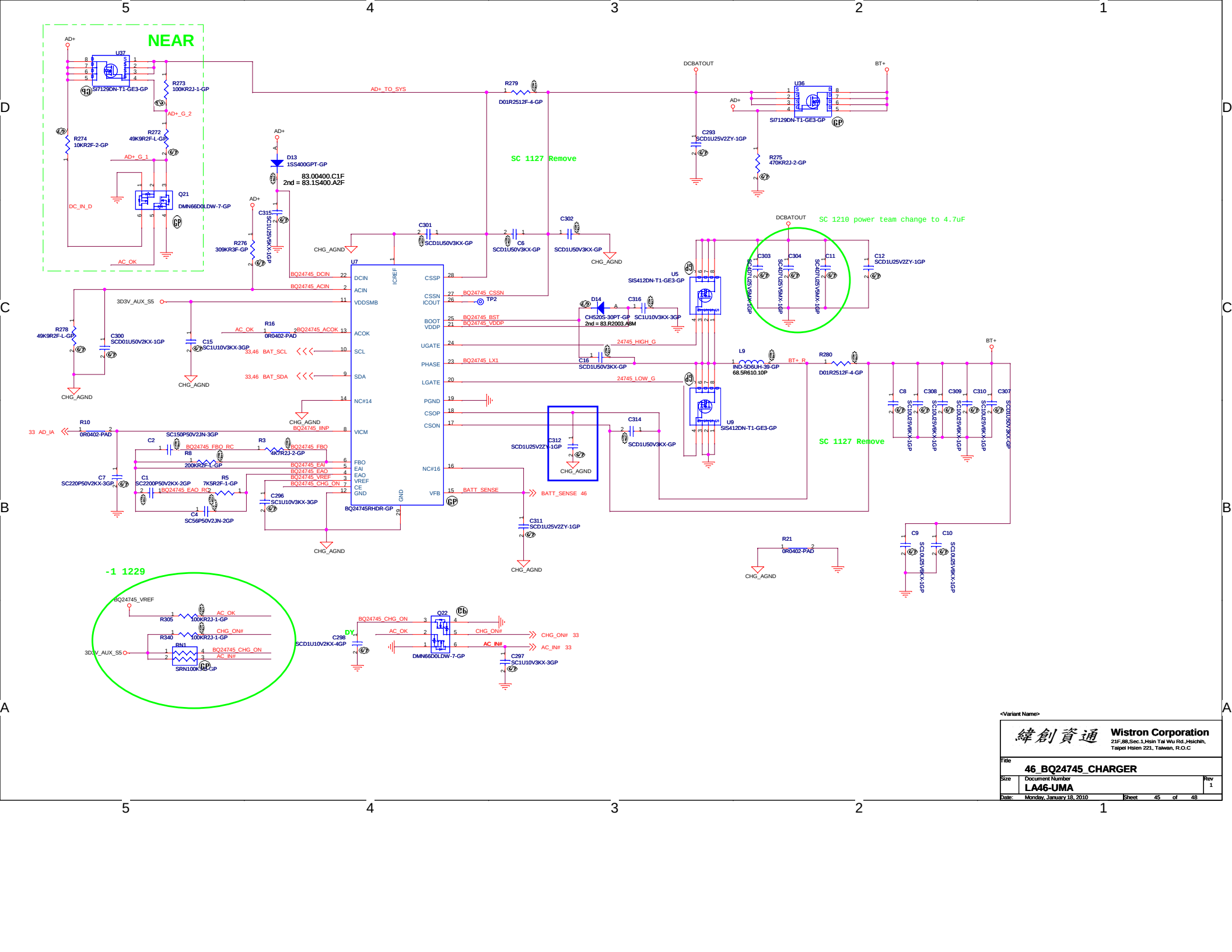
5 4 3 2 1

DS2-Intel



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Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

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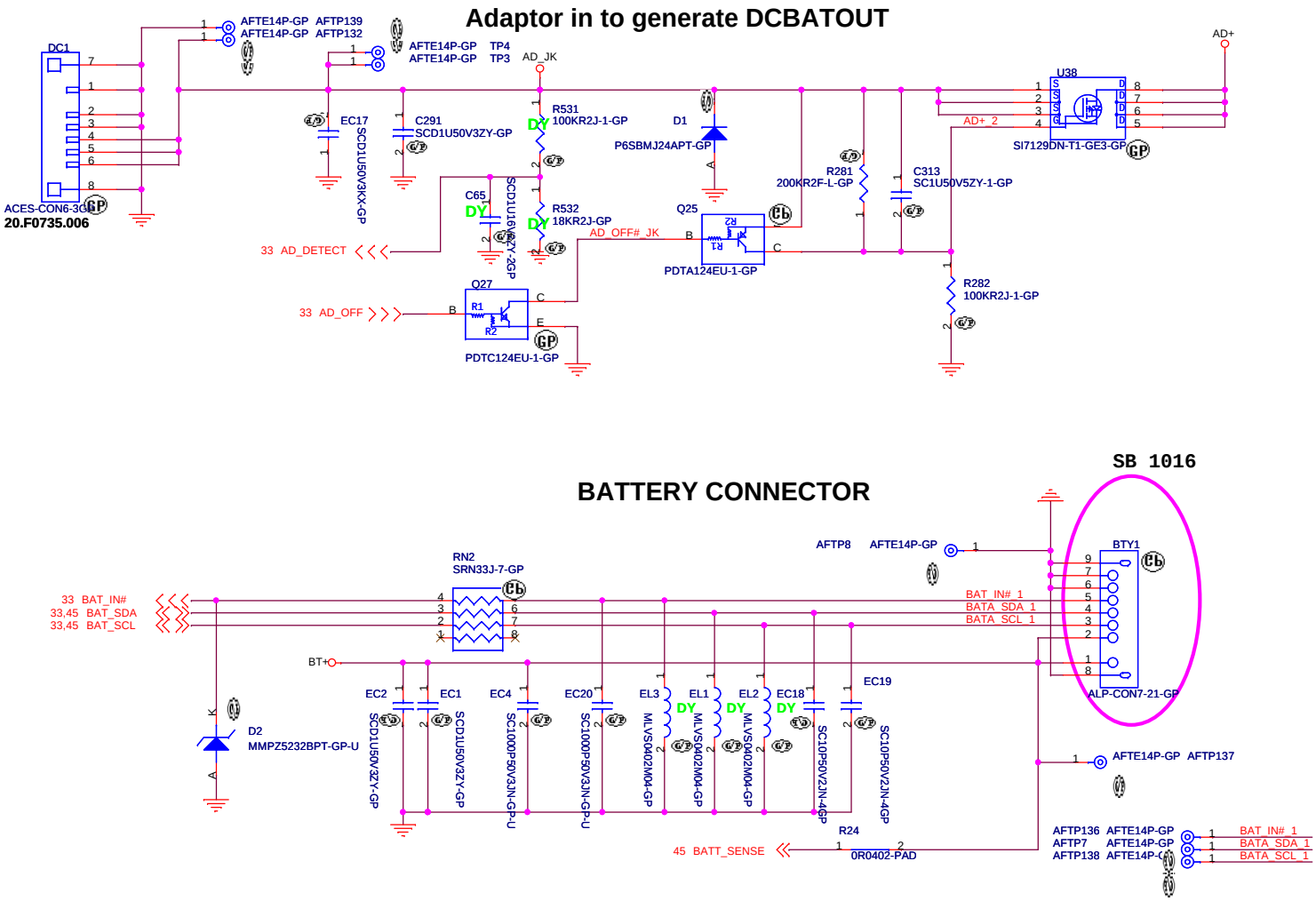

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Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

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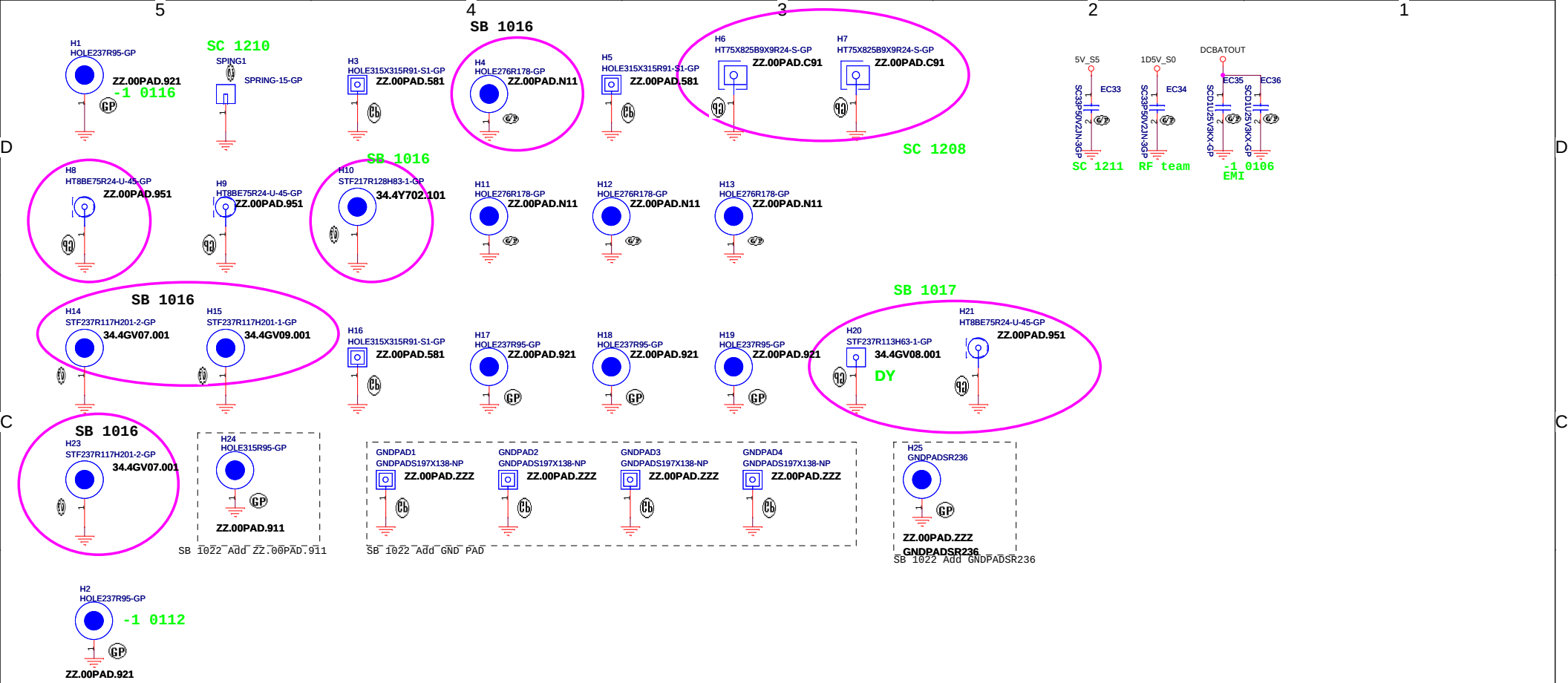

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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 48_EMI/Spring/Boss

Size	Document Number	Rev
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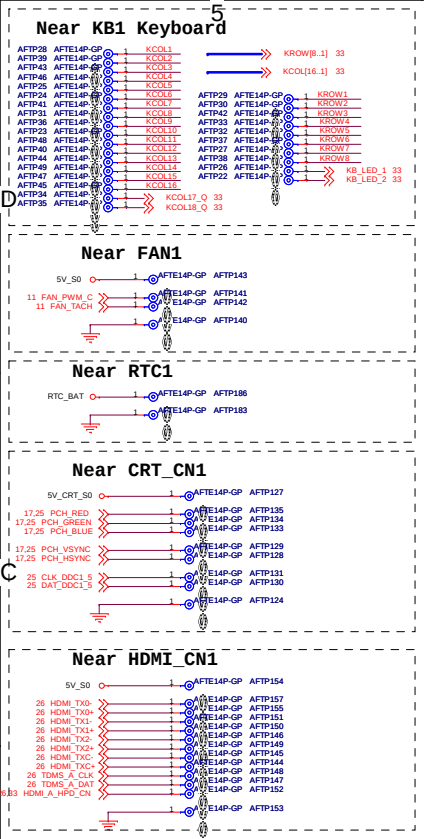

緯創資通 **Wistron Corporation**
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	AFTE_TP	
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