

# Soyuz 3.0 SYSTEM DIAGRAM

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

**Cable Docking**

- TV\_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 32

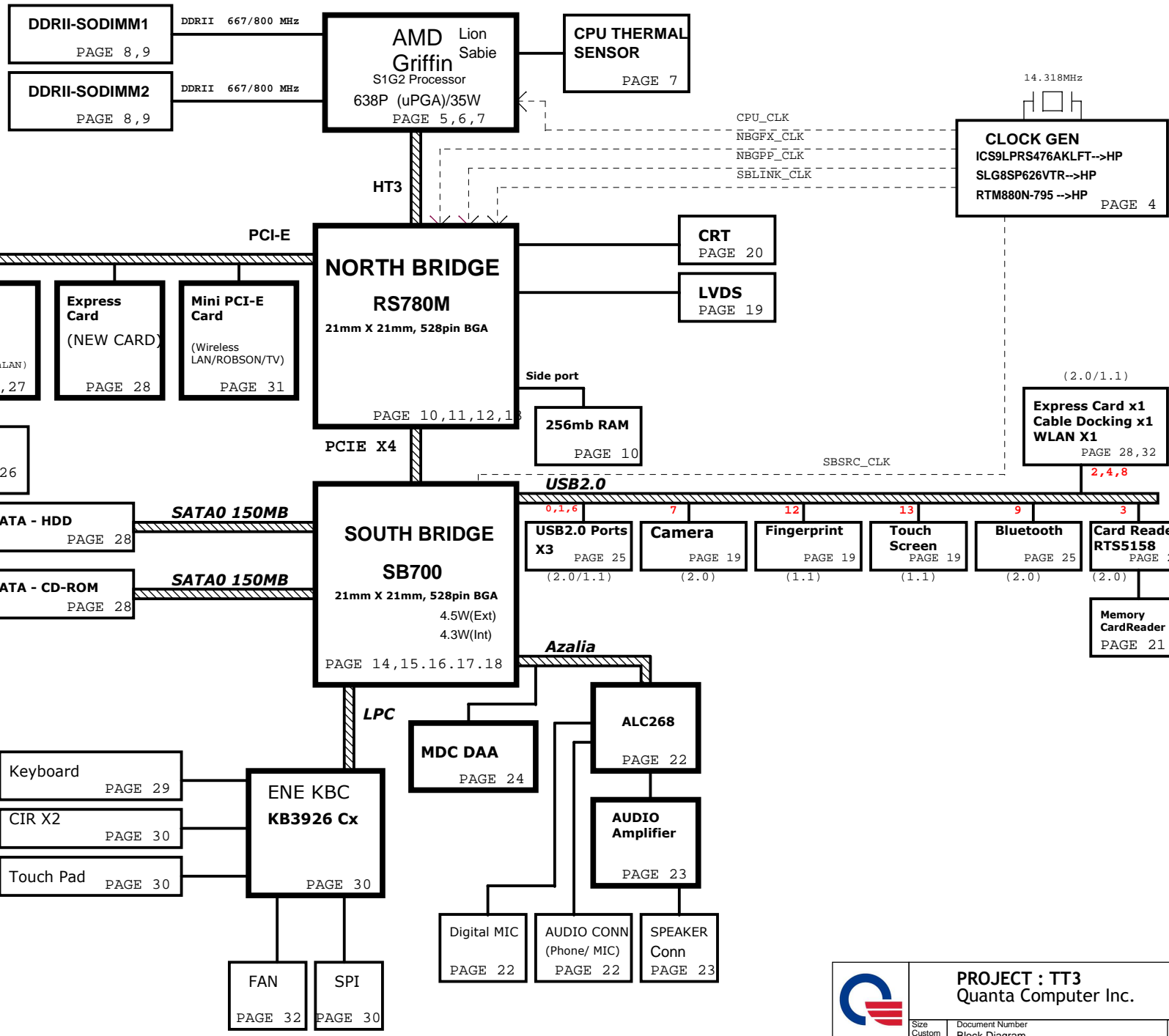
SYSTEM CHARGER(ISL6251A) PAGE 39

SYSTEM POWER MAX1631A PAGE 33

DDR II SMDR\_VTERM 1.8V/1.8VSUS PAGE 36

VCCP +1.1V AND +1.2V(RT8204) PAGE 34

CPU CORE ISL6265A PAGE 35



**PROJECT : TT3**  
Quanta Computer Inc.

|  |                               |        |
|--|-------------------------------|--------|
| Size Custom                                    | Document Number Block Diagram | Rev 1A |
| Date: Wednesday, August 27, 2008 Sheet 1 of 41 |                               |        |


NB5/RD2/HW1

# INDEX


| Pg#   | Description                   | NOTE |
|-------|-------------------------------|------|
| 1     | Schematic Block Diagram       |      |
| 2     | System Information            |      |
| 3     | Power sequence chart          |      |
| 4     | CLOCL GENERATOR               |      |
| 5-7   | AMD CPU S1G2 Griffin          |      |
| 8-9   | DDR II SO-DIMM                |      |
| 10-13 | RS780M                        |      |
| 14-18 | SB700                         |      |
| 19    | LCD CONNECTOR / LCD PWR / LID |      |
| 20    | 20--CRT,TV_OUT                |      |
| 21    | RTS5158E & CR SOCKET          |      |
| 22    | Azalia ALC268                 |      |
| 23    | JACK/AMP_TPA0312              |      |
| 24    | Si3080 and MDC1.5 Connector   |      |
| 25    | Blue Tooth / USBX3 / TPM      |      |
| 26    | RTL8111C/RJ45                 |      |
| 27    | LAN Power                     |      |
| 28    | NEW CARD/SATA ODD/SATA HDD    |      |
| 29    | LED/KEYBOARD/SW               |      |
| 30    | KB3926/ROM/TP                 |      |
| 31    | Mini CARD/Hole                |      |
| 32    | CABLE DOCKING/FAN             |      |
| 33    | 3V/5V(MAX1631A)               |      |
| 34    | +1.2V/+1.1V (RT8204)          |      |
| 35    | +CPU_CORE ISL6265             |      |
| 36    | +1.8VSUS/+1.8V/+2.5V          |      |
| 37    | +1.1V/+1.2V_S5/+1.5V          |      |
| 38    | DISCHARGE                     |      |
| 39    | Charger (ISL6251)             |      |

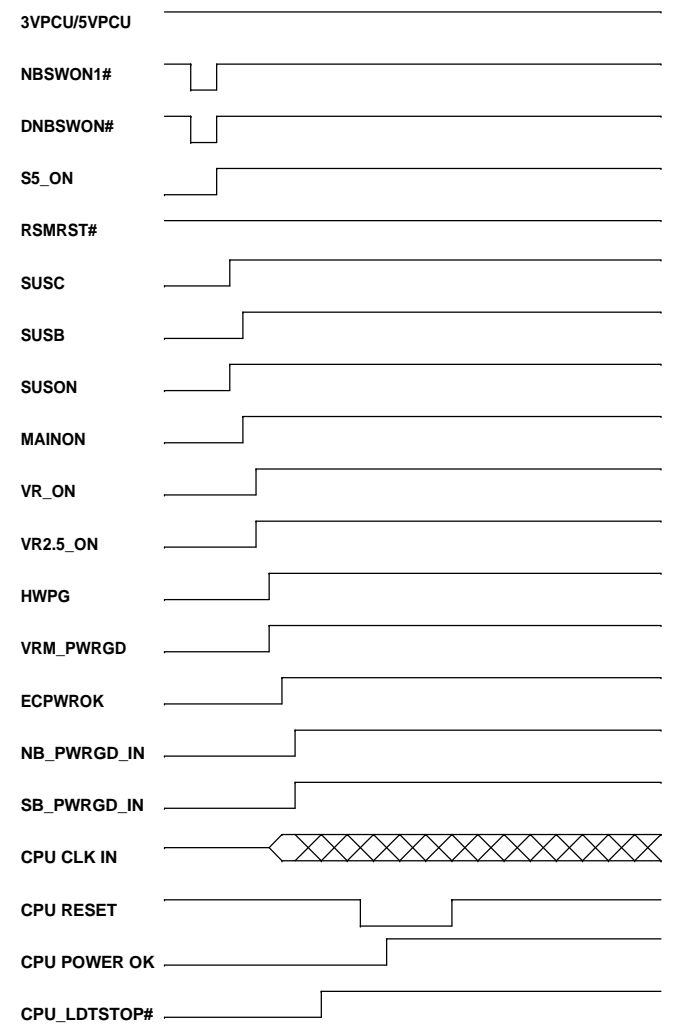
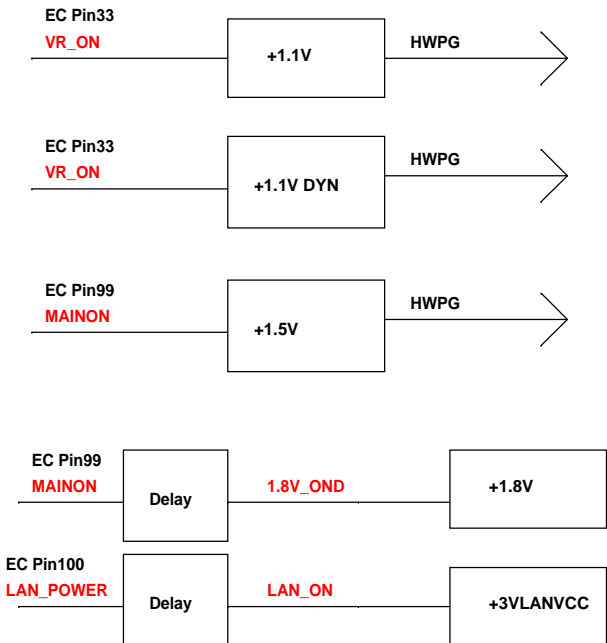
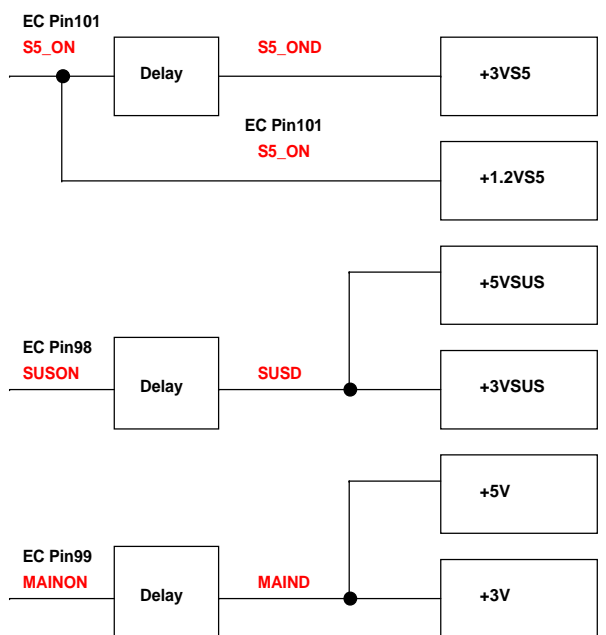
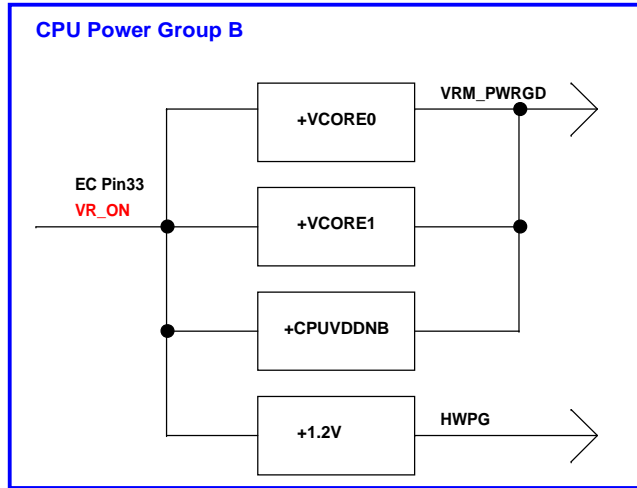
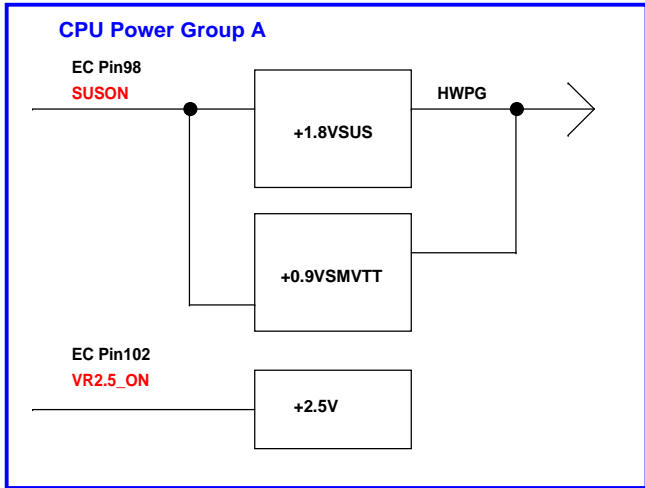
\* --> Un-stuff (ex. \*1K/04)  
 04-- 0402 footprint  
 06-- 0603 footprint  
 08-- 0805 footprint  
 12-- 1206 footprint  
 F-- 1% tolerance

# Power & Ground

| Label  | ACTIVE         | Description                         | Control Signal |
|--|----------------|-------------------------------------|----------------|
| +VIN   | S0, S3, S4, S5 | AC ADAPTER (18.5V)                  |                |
| +BATT  | S0, S3, S4, S5 | MAIN BATTERY + (6.2V-8.4V)          |                |
| +AVBAT   | S0, S3, S4, S5 | RTC & KBC POWER (3.3V)              |                |
| +12VALW  | S0, S3, S4, S5 | +12V                                |                |
| +VCORE   | S0             | CPU CORE POWER (0.375-1.5V)         | VRON           |
| +CPUVDDNB  | S0             | CPU CORE POWER (1.375-1.5V)         | VRON           |
| +1.1V_NB   | S0             | +1.1 to +1.0 DYN                    | VRON           |
| +1.1V  | S0             | +1.1V                               | VRON           |
| +1.2VS5  | S0, S3, S4, S5 |                                     | S5_ON          |
| +1.2V  | S0             | +1.2V                               | VRON           |
| +3V  | S0             |                                     | MAINON         |
| +3VSUS   | S0, S3         |                                     | SUSON          |
| +3VS5  | S0, S3, S4, S5 |                                     | S5_ON          |
| +3VPCU   | S0, S3, S4, S5 | ALWAYS POWER (3V)                   |                |
| +5V  | S0             |                                     | MAIND          |
| +5VSUS   | S0, S3         |                                     | SUSON          |
| +5VPCU   | S0, S3, S4, S5 | ALWAYS POWER (5V)                   |                |
| +1.5V  | S0             |                                     | MAIND          |
| +1.8VSUS   | S0, S3         | DDR CORE POWER                      | SUSON          |
| +1.8V  | S0             |                                     | MAINON         |
| +2.5V  | S0             | CPU VDDA                            | VR2.5_ON       |
| +0.9VSMVTT   | S0             | DDR COMMAND & CONTROL PULL UP POWER | MAINON         |
| +0.9VSMVREF_DIMM   | S0, S3         | DDR REF POWER                       | SUSON          |
| +AVDD  | S0             | AUDIO ANALOG POWER (5V)             | MAINON         |
| +3VLAVCC   | S0, S3, S4, S5 | LAN Power                           | LAN_ON         |
|  |                |                                     |                |
|  GND  | ALL PAGES      | DIGITAL GROUND                      |                |
|  AGND |                | AUDIO GND                           |                |

|                    |                                  |
|--------------------|----------------------------------|
| SMBUS              | SMBUS function define            |
| SMBCLK0<br>SMBDAT0 | DDR / DDR THER / CLOCK GEN (+3V) |
| SMBCLK1<br>SMBDAT1 | Mini Card (+3VS5)                |
| SMBCLK2<br>SMBDAT2 | New CARD (+3VS5)                 |

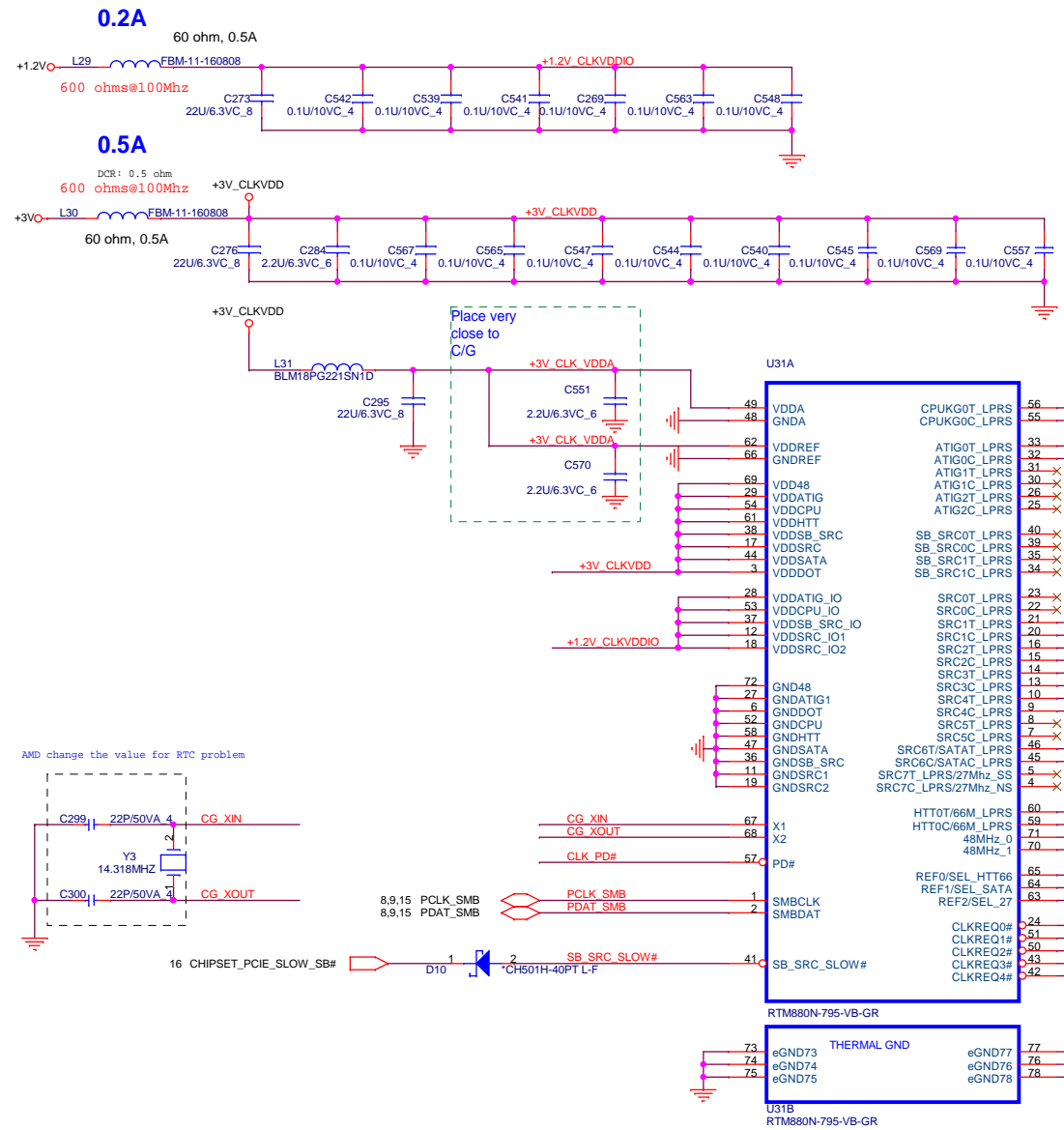
|  |  |   |
|--|--|---|
| <br>NB5/RD2/HW1 | <b>PROJECT : TT3</b><br>Quanta Computer Inc.         |   |
|  | Size Custom<br>Document Number<br>System Information | Date: Wednesday, August 27, 2008<br>Sheet 2 of 41 |



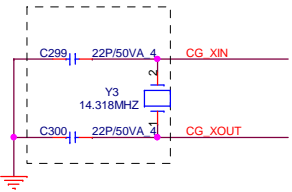
## NB CLOCK INPUT TABLE

| NB CLOCKS    | RX780         | RS780                  |
|--------------|---------------|------------------------|
| HT_REFCLKP   | 100M DIFF     | 100M DIFF              |
| HT_REFCLKN   | 100M DIFF     | 100M DIFF              |
| REFCLK_P     | 14M SE (1.8V) | 14M SE (1.1V)          |
| REFCLK_N     | NC            | vref                   |
| GFX_REFCLK   | 100M DIFF     | 100M DIFF(IN/OUT)*     |
| GPP_REFCLK   | 100M DIFF     | NC or 100M DIFF OUTPUT |
| GPPSB_REFCLK | 100M DIFF     | 100M DIFF              |

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



AMD change the value for RTC problem



16 CHIPSET\_PCIE\_SLOW\_SB#

8,9,15 PCLK\_SMB  
8,9,15 PDAT\_SMB

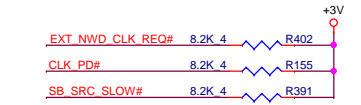
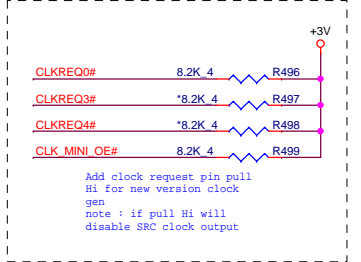
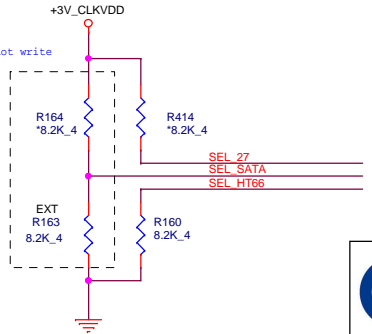
SB\_SRC\_SLOW#

when driven low SB\_SRC clocks slow only supported with to reduced setpoint custom CG IC

\* RS780 can be used as clock buffer to output two PCIe reference clocks  
By default, chip will be configured as input mode, BIOS can program it to output mode.

\* default

|           |    |  |
|-----------|----|--|
| SEL_HTT66 | 1  | 66 MHz 3.3V single ended HTT clock           |
|           | 0* | 100 MHz differential HTT clock               |
| SEL_SATA  | 1* | 100 MHz non-spreading differential SRC clock |
|           | 0  | 100 MHz spreading differential SRC clock     |
| SEL_27    | 1* | 27MHz non-spreading singled clock            |
|           | 0  | 100 MHz spreading differential SRC clock     |



Add clock request pin pull Hi for new version clock gen  
note : if pull Hi will disable SRC clock output

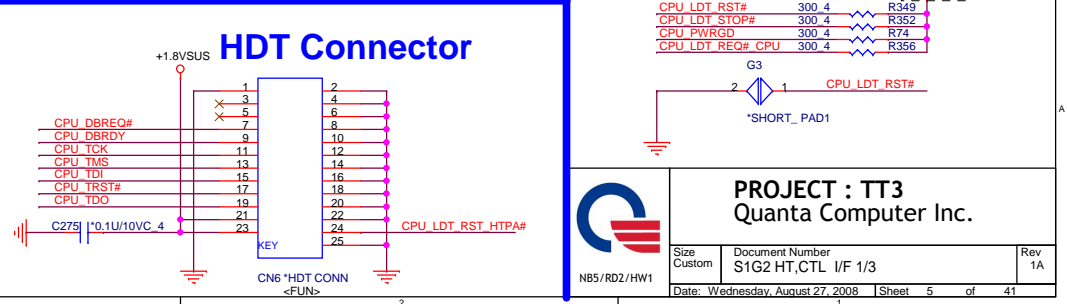
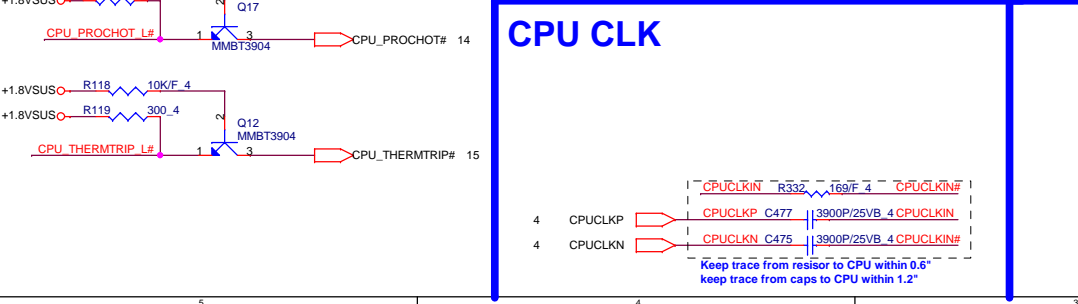
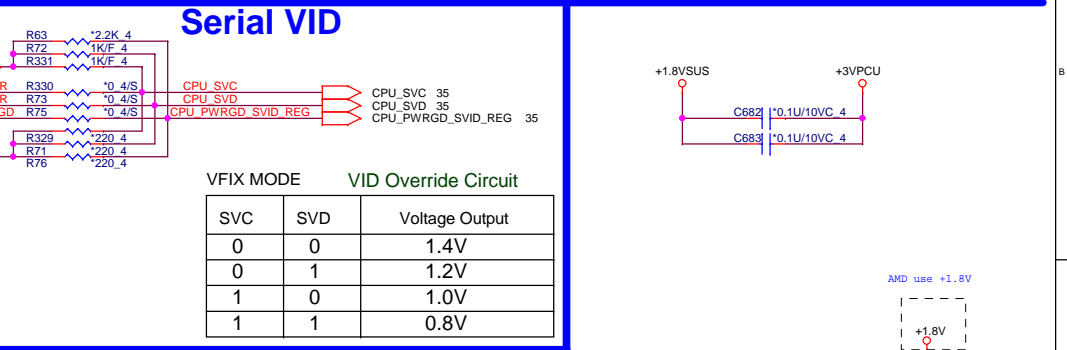
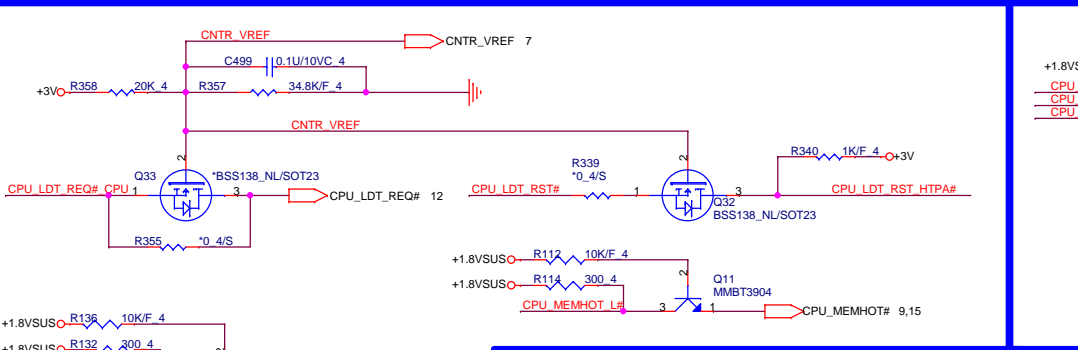
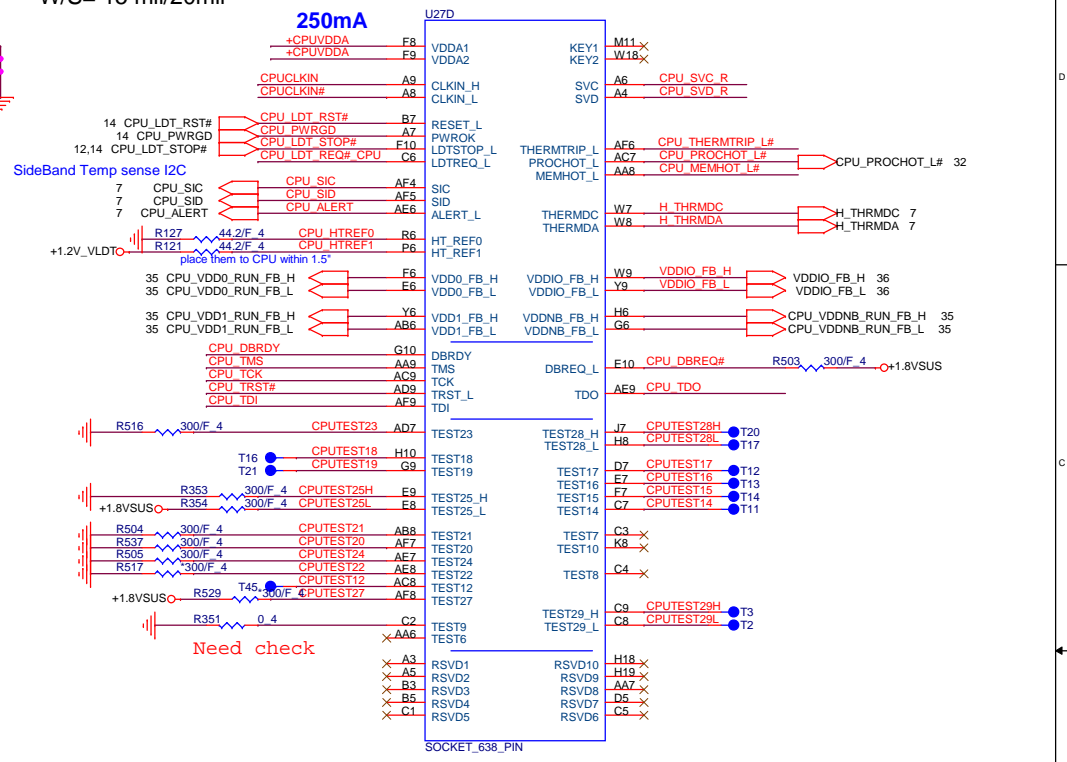
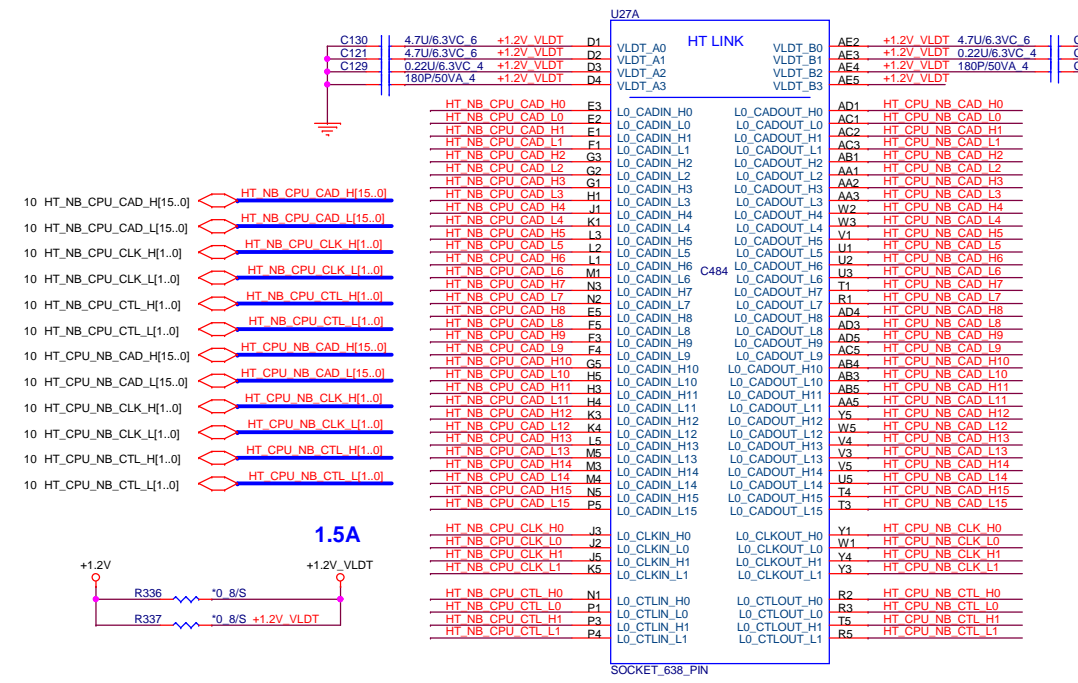
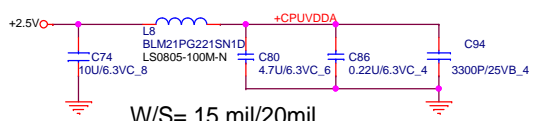


PROJECT : TT3  
Quanta Computer Inc.

|                                  |                                    |        |
|----------------------------------|------------------------------------|--------|
| Size Custom                      | Document Number<br>Clock generator | Rev 1A |
| Date: Wednesday, August 27, 2008 | Sheet 4 of 41                      |        |

+1.2V 5,13,14,16,17,34,37  
+3V 5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

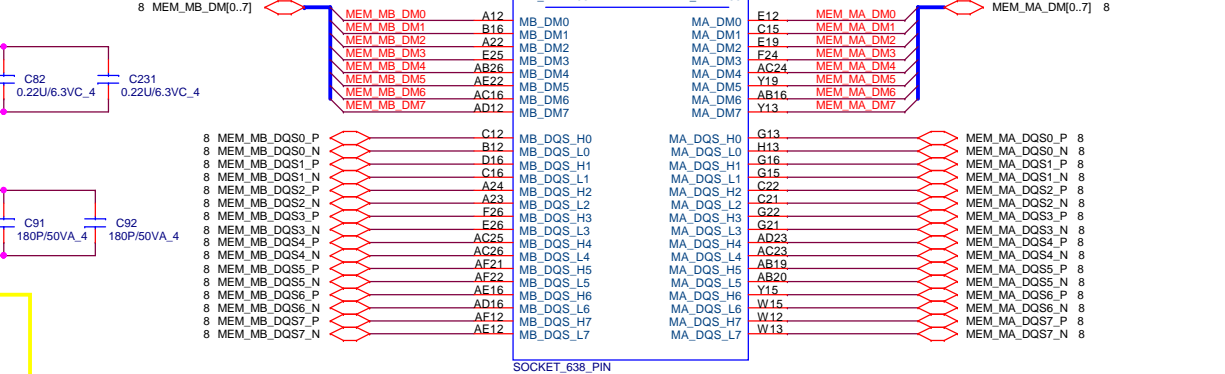
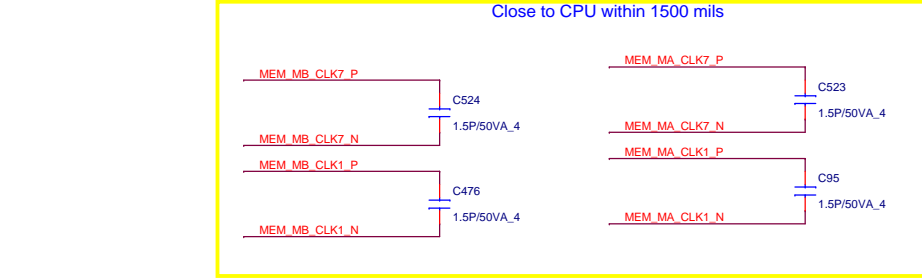
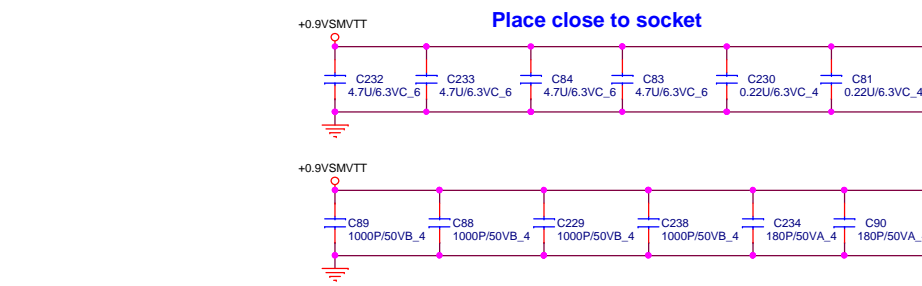
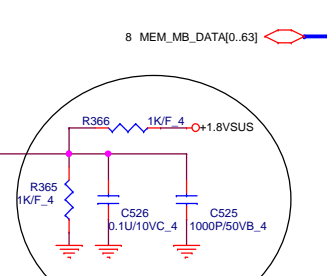
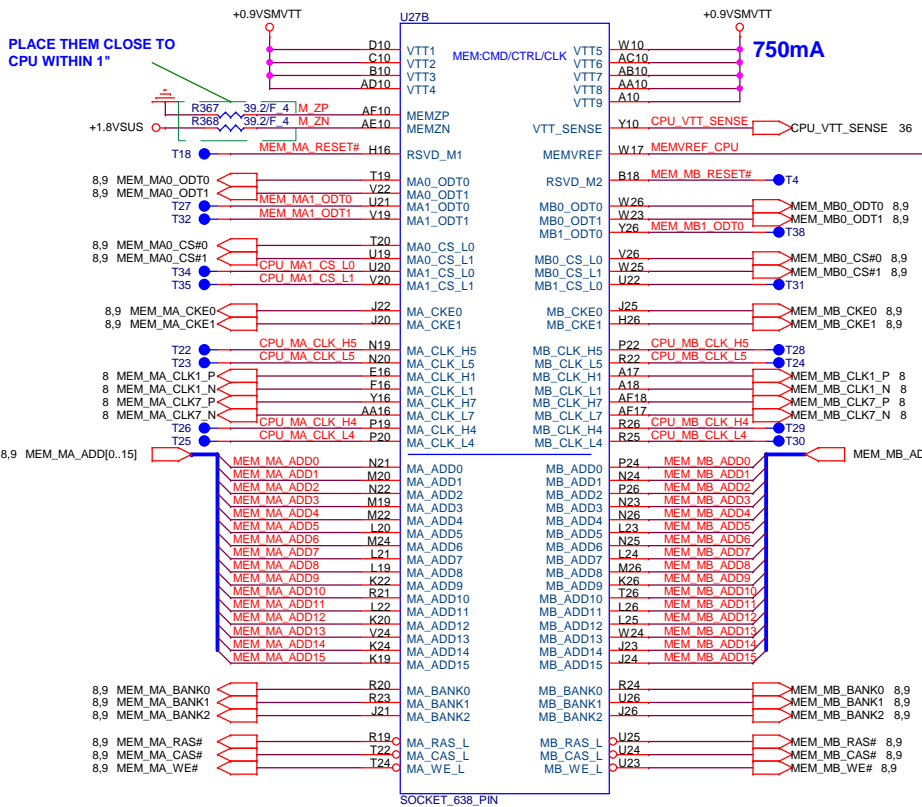
+1.2V 4,13,14,16,17,34,37  
 +1.8V 10,12,13,14,15,18,31,36,38  
 +1.8VSUS 6,7,8,9,31,35,36,37  
 +2.5V 37  
 +3V 4,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38



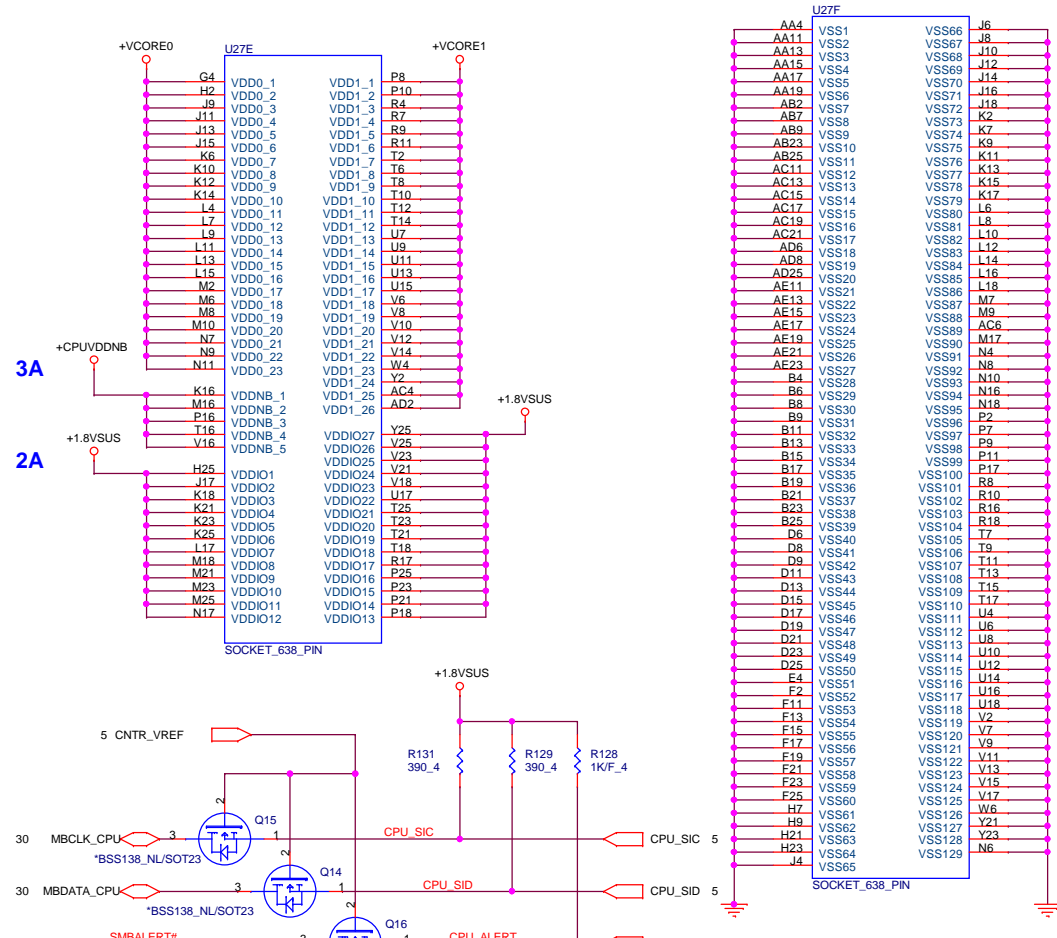
**PROJECT : TT3**  
 Quanta Computer Inc.  
 Size Custom Document Number S1G2 HT,CTL I/F 1/3 Rev 1A  
 Date: Wednesday, August 27, 2008 Sheet 5 of 41  
 NBS/RD2/HW1

# Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"





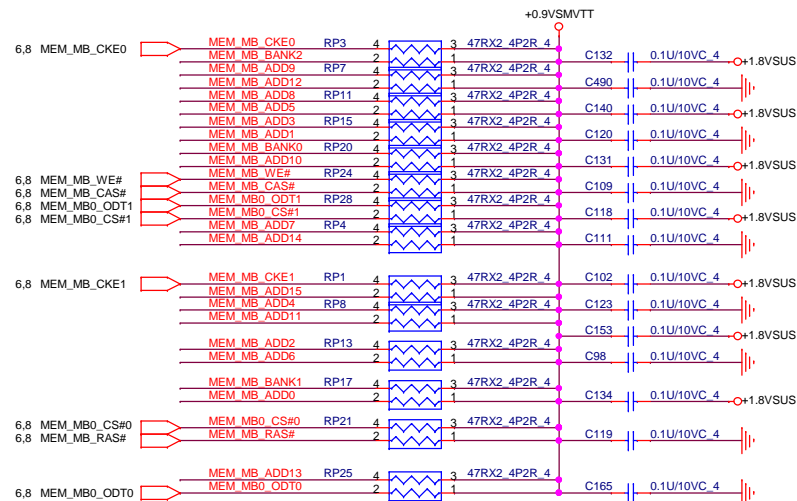
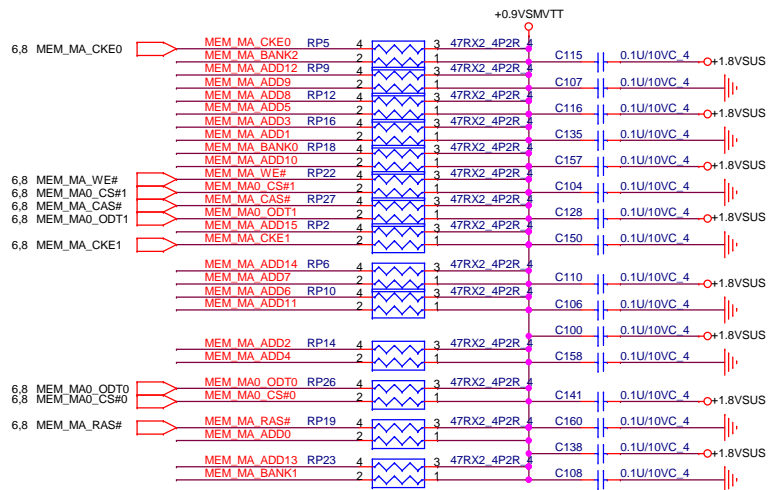




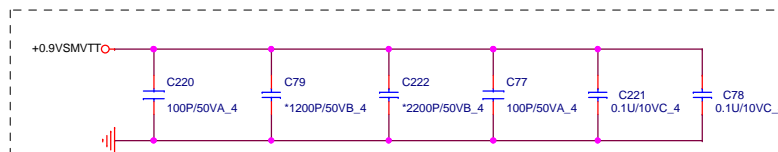


6,8 MEM\_MA\_ADD[0..15] MEM\_MA\_ADD[0..15]  
6,8 MEM\_MA\_BANK[0..2] MEM\_MA\_BANK[0..2]

6,8 MEM\_MB\_ADD[0..15] MEM\_MB\_ADD[0..15]  
6,8 MEM\_MB\_BANK[0..2] MEM\_MB\_BANK[0..2]



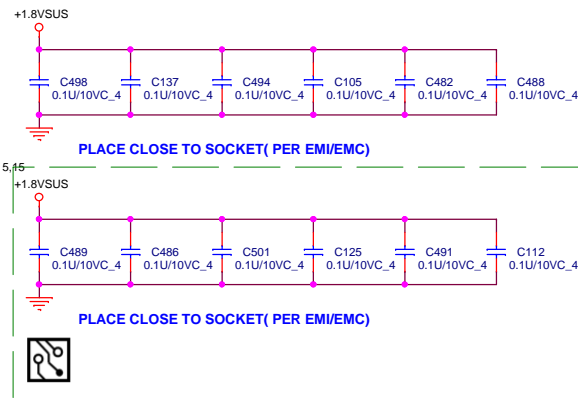
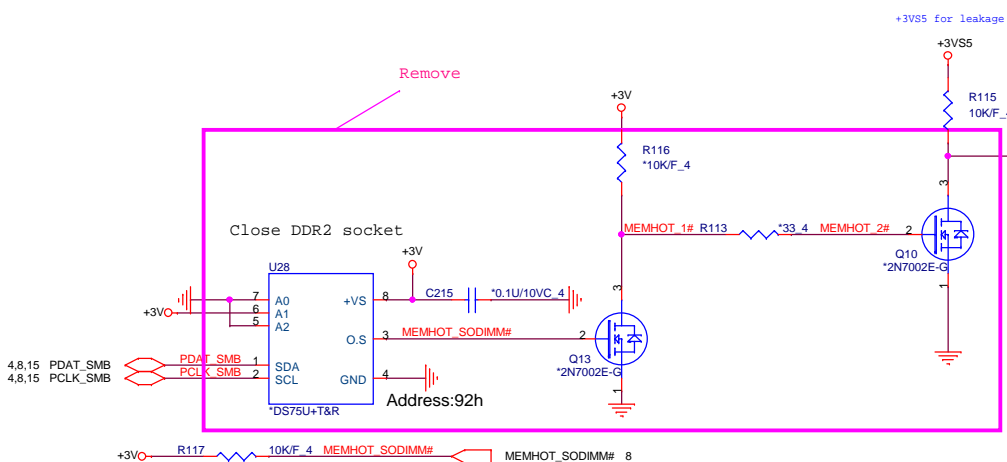
Emi request



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



+0.9VSMVTT 6,31,36  
+1.8VSUS 5,6,7,8,31,35,36,37  
+3V 4,5,7,8,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,36,38



PROJECT : TT3  
Quanta Computer Inc.

|                                  |  |               |
|----------------------------------|--|---------------|
| Size Custom                      | Document Number<br>DDR2 SODIMMS TERMINATIONS | Rev 1A        |
| Date: Wednesday, August 27, 2008 |  | Sheet 9 of 41 |

PART 1 OF 6

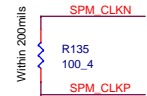
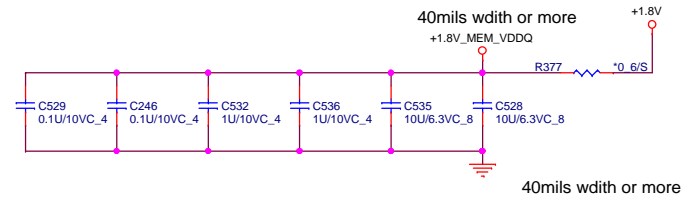
HYPER TRANSPORT CPU I/F

|                   |      |             |     |                   |
|-------------------|------|-------------|-----|-------------------|
| HT_CPU_NB_CAD_H0  | Y25  | HT_RXCAD0P  | D24 | HT_NB_CPU_CAD_H0  |
| HT_CPU_NB_CAD_L0  | Y24  | HT_RXCAD0N  | D25 | HT_NB_CPU_CAD_L0  |
| HT_CPU_NB_CAD_H1  | Y22  | HT_RXCAD1P  | E24 | HT_NB_CPU_CAD_H1  |
| HT_CPU_NB_CAD_L1  | Y23  | HT_RXCAD1N  | E25 | HT_NB_CPU_CAD_L1  |
| HT_CPU_NB_CAD_H2  | Y25  | HT_RXCAD2P  | F24 | HT_NB_CPU_CAD_H2  |
| HT_CPU_NB_CAD_L2  | Y24  | HT_RXCAD2N  | F25 | HT_NB_CPU_CAD_L2  |
| HT_CPU_NB_CAD_H3  | U24  | HT_RXCAD3P  | F23 | HT_NB_CPU_CAD_H3  |
| HT_CPU_NB_CAD_L3  | U25  | HT_RXCAD3N  | F22 | HT_NB_CPU_CAD_L3  |
| HT_CPU_NB_CAD_H4  | T25  | HT_RXCAD4P  | H23 | HT_NB_CPU_CAD_H4  |
| HT_CPU_NB_CAD_L4  | T24  | HT_RXCAD4N  | H22 | HT_NB_CPU_CAD_L4  |
| HT_CPU_NB_CAD_H5  | P22  | HT_RXCAD5P  | J24 | HT_NB_CPU_CAD_H5  |
| HT_CPU_NB_CAD_L5  | P23  | HT_RXCAD5N  | J24 | HT_NB_CPU_CAD_L5  |
| HT_CPU_NB_CAD_H6  | P25  | HT_RXCAD6P  | K24 | HT_NB_CPU_CAD_H6  |
| HT_CPU_NB_CAD_L6  | P24  | HT_RXCAD6N  | K25 | HT_NB_CPU_CAD_L6  |
| HT_CPU_NB_CAD_H7  | N24  | HT_RXCAD7P  | K23 | HT_NB_CPU_CAD_H7  |
| HT_CPU_NB_CAD_L7  | N25  | HT_RXCAD7N  | K22 | HT_NB_CPU_CAD_L7  |
| HT_CPU_NB_CAD_H8  | AC24 | HT_RXCAD8P  | F21 | HT_NB_CPU_CAD_H8  |
| HT_CPU_NB_CAD_L8  | AC25 | HT_RXCAD8N  | G21 | HT_NB_CPU_CAD_L8  |
| HT_CPU_NB_CAD_H9  | AB25 | HT_RXCAD9P  | G20 | HT_NB_CPU_CAD_H9  |
| HT_CPU_NB_CAD_L9  | AB24 | HT_RXCAD9N  | H21 | HT_NB_CPU_CAD_L9  |
| HT_CPU_NB_CAD_H10 | AA24 | HT_RXCAD9N  | J20 | HT_NB_CPU_CAD_H10 |
| HT_CPU_NB_CAD_L10 | AA25 | HT_RXCAD10P | J21 | HT_NB_CPU_CAD_L10 |
| HT_CPU_NB_CAD_H11 | Y22  | HT_RXCAD10N | J18 | HT_NB_CPU_CAD_H11 |
| HT_CPU_NB_CAD_L11 | Y23  | HT_RXCAD11P | K17 | HT_NB_CPU_CAD_L11 |
| HT_CPU_NB_CAD_H12 | W21  | HT_RXCAD12P | L18 | HT_NB_CPU_CAD_H12 |
| HT_CPU_NB_CAD_L12 | W20  | HT_RXCAD12N | L19 | HT_NB_CPU_CAD_L12 |
| HT_CPU_NB_CAD_H13 | V21  | HT_RXCAD12N | M19 | HT_NB_CPU_CAD_H13 |
| HT_CPU_NB_CAD_L13 | V20  | HT_RXCAD13P | L18 | HT_NB_CPU_CAD_L13 |
| HT_CPU_NB_CAD_H14 | U20  | HT_RXCAD13N | M21 | HT_NB_CPU_CAD_H14 |
| HT_CPU_NB_CAD_L14 | U21  | HT_RXCAD14P | P21 | HT_NB_CPU_CAD_L14 |
| HT_CPU_NB_CAD_H15 | U19  | HT_RXCAD15P | P18 | HT_NB_CPU_CAD_H15 |
| HT_CPU_NB_CAD_L15 | U18  | HT_RXCAD15N | M19 | HT_NB_CPU_CAD_L15 |
| HT_CPU_NB_CLK_H0  | T22  | HT_RXCLK0P  | H24 | HT_NB_CPU_CLK_H0  |
| HT_CPU_NB_CLK_L0  | T23  | HT_RXCLK0N  | H25 | HT_NB_CPU_CLK_L0  |
| HT_CPU_NB_CLK_H1  | AB23 | HT_RXCLK1P  | L21 | HT_NB_CPU_CLK_H1  |
| HT_CPU_NB_CLK_L1  | AA22 | HT_RXCLK1N  | L20 | HT_NB_CPU_CLK_L1  |
| HT_CPU_NB_CTL_H0  | M22  | HT_RXCTL0P  | M24 | HT_NB_CPU_CTL_H0  |
| HT_CPU_NB_CTL_L0  | M23  | HT_RXCTL0N  | M25 | HT_NB_CPU_CTL_L0  |
| HT_CPU_NB_CTL_H1  | R21  | HT_RXCTL1P  | P19 | HT_NB_CPU_CTL_H1  |
| HT_CPU_NB_CTL_L1  | R20  | HT_RXCTL1N  | R18 | HT_NB_CPU_CTL_L1  |
| HT_RXCALP         | C23  | HT_TXCALP   | B24 | HT_TXCALP         |
| HT_RXCALN         | A24  | HT_TXCALN   | B25 | HT_TXCALN         |

follow AMD check list to change part number 300 ohm to 301 ohm

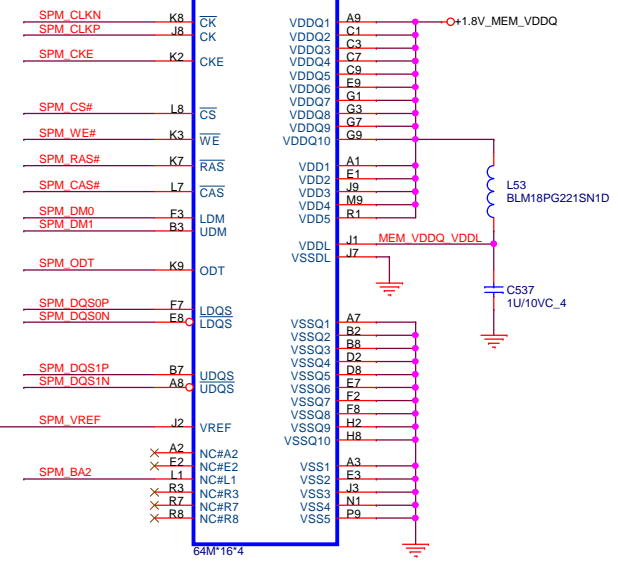
follow AMD check list to change part number 300 ohm to 301 ohm

|                        |                        |
|------------------------|------------------------|
| HT_CPU_NB_CAD_H[15..0] | HT_CPU_NB_CAD_H[15..0] |
| HT_CPU_NB_CAD_L[15..0] | HT_CPU_NB_CAD_L[15..0] |
| HT_CPU_NB_CLK_H[1..0]  | HT_CPU_NB_CLK_H[1..0]  |
| HT_CPU_NB_CLK_L[1..0]  | HT_CPU_NB_CLK_L[1..0]  |
| HT_CPU_NB_CTL_H[1..0]  | HT_CPU_NB_CTL_H[1..0]  |
| HT_CPU_NB_CTL_L[1..0]  | HT_CPU_NB_CTL_L[1..0]  |
| HT_NB_CPU_CAD_H[15..0] | HT_NB_CPU_CAD_H[15..0] |
| HT_NB_CPU_CAD_L[15..0] | HT_NB_CPU_CAD_L[15..0] |
| HT_NB_CPU_CLK_H[1..0]  | HT_NB_CPU_CLK_H[1..0]  |
| HT_NB_CPU_CLK_L[1..0]  | HT_NB_CPU_CLK_L[1..0]  |
| HT_NB_CPU_CTL_H[1..0]  | HT_NB_CPU_CTL_H[1..0]  |
| HT_NB_CPU_CTL_L[1..0]  | HT_NB_CPU_CTL_L[1..0]  |

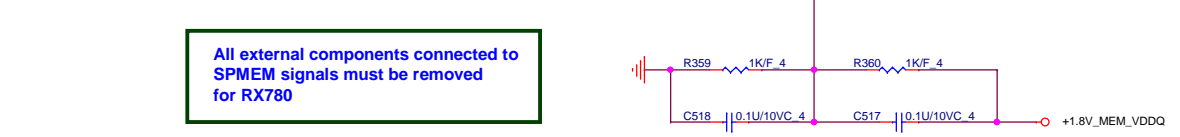


Close to U23

|         |    |        |      |    |          |
|---------|----|--------|------|----|----------|
| SPM BA0 | L2 | BA0    | DQ15 | B9 | SPM DQ15 |
| SPM BA1 | L3 | BA1    | DQ14 | B1 | SPM DQ14 |
| SPM A12 | R2 | A12    | DQ13 | D9 | SPM DQ9  |
| SPM A11 | P7 | A11    | DQ12 | D1 | SPM DQ12 |
| SPM A10 | M2 | A10/AP | DQ11 | D3 | SPM DQ8  |
| SPM A9  | P8 | A9     | DQ10 | D7 | SPM DQ10 |
| SPM A8  | A8 | A8     | DQ9  | C2 | SPM DQ13 |
| SPM A7  | P2 | A7     | DQ8  | C8 | SPM DQ11 |
| SPM A6  | N7 | A6     | DQ7  | F9 | SPM DQ5  |
| SPM A5  | N3 | A5     | DQ6  | F1 | SPM DQ3  |
| SPM A4  | N8 | A4     | DQ5  | H9 | SPM DQ4  |
| SPM A3  | M2 | A3     | DQ4  | H1 | SPM DQ1  |
| SPM A2  | M2 | A2     | DQ3  | H3 | SPM DQ0  |
| SPM A1  | M3 | A1     | DQ2  | G2 | SPM DQ2  |
| SPM A0  | M8 | A0     | DQ1  | G8 | SPM DQ6  |
| SPM A0  | M8 | A0     | DQ0  |    |          |

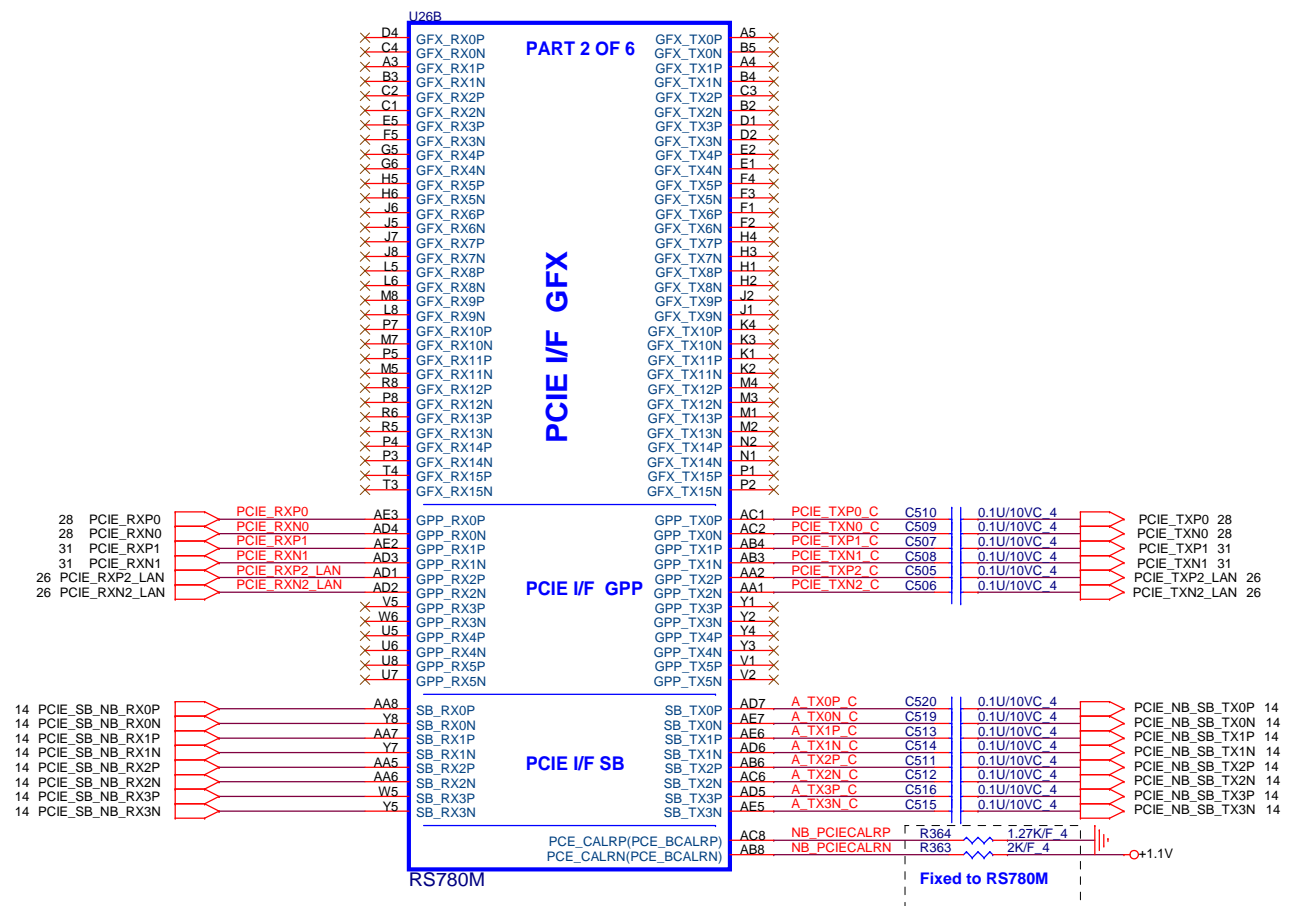


|          |       |              |                          |      |           |
|----------|-------|--------------|--------------------------|------|-----------|
| SPM A0   | AB12  | MEM_A0(NC)   | MEM_DQ0(DVO_VSYNC(NC))   | AA18 | SPM DQ0   |
| SPM A1   | AE16  | MEM_A1(NC)   | MEM_DQ1(DVO_HSYNC(NC))   | AA20 | SPM DQ1   |
| SPM A2   | V11   | MEM_A2(NC)   | MEM_DQ2(DVO_DE(NC))      | AA19 | SPM DQ2   |
| SPM A3   | AE15  | MEM_A3(NC)   | MEM_DQ3(DVO_D0(NC))      | Y19  | SPM DQ3   |
| SPM A4   | AA12  | MEM_A4(NC)   | MEM_DQ4(NC)              | Y17  | SPM DQ4   |
| SPM A5   | AB16  | MEM_A5(NC)   | MEM_DQ5(DVO_D1(NC))      | AA17 | SPM DQ5   |
| SPM A6   | AB14  | MEM_A6(NC)   | MEM_DQ6(DVO_D2(NC))      | AA15 | SPM DQ6   |
| SPM A7   | AD14  | MEM_A7(NC)   | MEM_DQ7(DVO_D4(NC))      | Y15  | SPM DQ7   |
| SPM A8   | AD13  | MEM_A8(NC)   | MEM_DQ8(DVO_D3(NC))      | AC20 | SPM DQ8   |
| SPM A9   | AD15  | MEM_A9(NC)   | MEM_DQ9(DVO_D5(NC))      | AD19 | SPM DQ9   |
| SPM A10  | AC16  | MEM_A10(NC)  | MEM_DQ10(DVO_D6(NC))     | AC18 | SPM DQ11  |
| SPM A11  | AE13  | MEM_A11(NC)  | MEM_DQ11(DVO_D7(NC))     | AB20 | SPM DQ12  |
| SPM A12  | AC14  | MEM_A12(NC)  | MEM_DQ12(NC)             | AD22 | SPM DQ13  |
| SPM A13  | Y14   | MEM_A13(NC)  | MEM_DQ13(DVO_D9(NC))     | AC22 | SPM DQ14  |
| SPM BA0  | AD16  | MEM_BA0(NC)  | MEM_DQ14(DVO_D10(NC))    | AD21 | SPM DQ15  |
| SPM BA1  | AE17  | MEM_BA1(NC)  | MEM_DQ15(DVO_D11(NC))    |      |           |
| SPM BA2  | AD17  | MEM_BA2(NC)  |                          |      |           |
| SPM CAS# | W12C  | MEM_CASb(NC) | MEM_DQS0P(DVO_IDCKP(NC)) | Y17  | SPM DQS0P |
| SPM CAS# | Y12C  | MEM_CASb(NC) | MEM_DQS0N(DVO_IDCKN(NC)) | W18  | SPM DQS0N |
| SPM WE#  | AD18C | MEM_WEb(NC)  | MEM_DQS1P(NC)            | AD20 | SPM DQS1P |
| SPM CS#  | AB13C | MEM_CSb(NC)  | MEM_DQS1N(NC)            | AE21 | SPM DQS1N |
| SPM CKE  | AB18  | MEM_CKE(NC)  | MEM_DM0(NC)              | W17  | SPM DM0   |
| SPM ODT  | V14   | MEM_ODT(NC)  | MEM_DM1(DVO_D8(NC))      | AE19 | SPM DM1   |
| SPM CLKP | W15   | MEM_CKPN(NC) |                          |      |           |
| SPM CLKN | W14   | MEM_CKPN(NC) |                          |      |           |



All external components connected to SPME signals must be removed for RX780

|            |                           |
|------------|---------------------------|
| +0.9VSMVTT | 6,9,31,36                 |
| +1.1V      | 11,12,13,37               |
| +1.8V      | 5,12,13,14,15,18,31,36,38 |

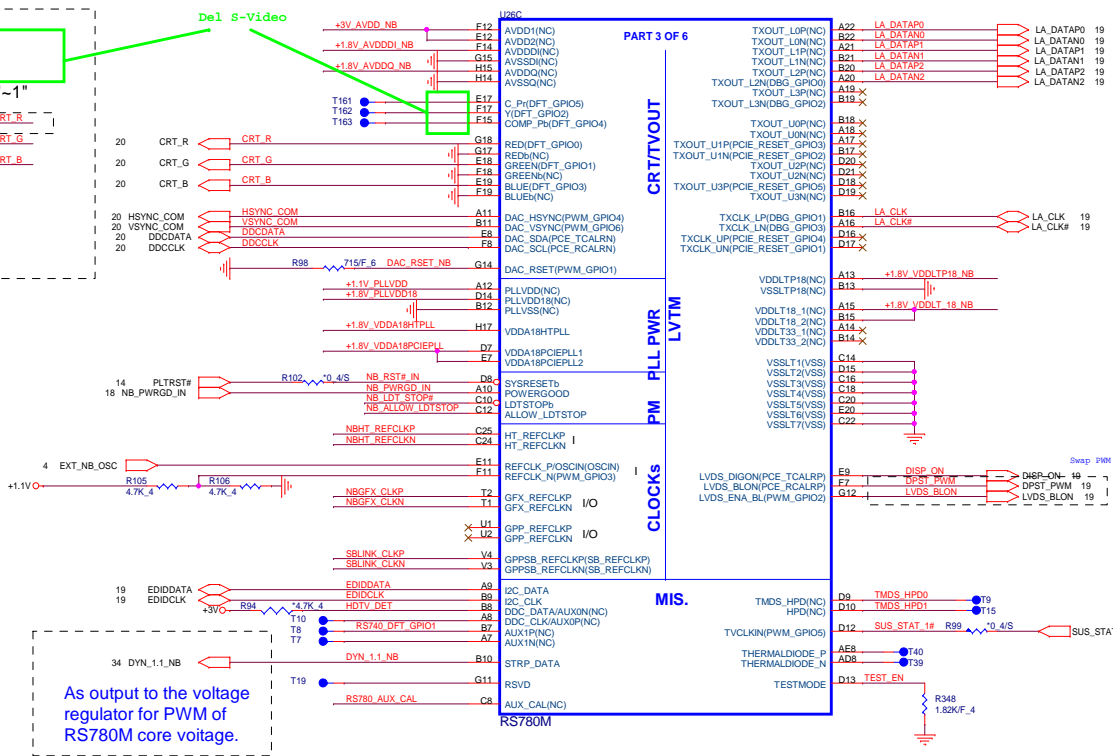
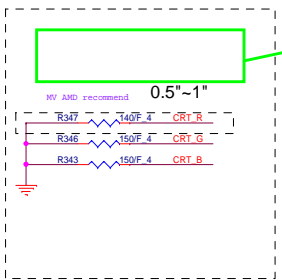
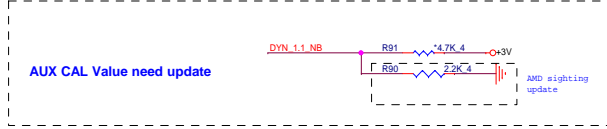
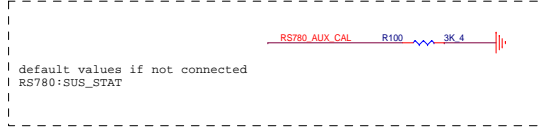
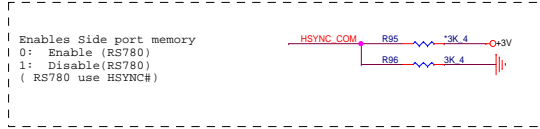
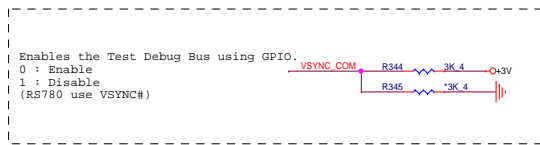


➔ +1.1V 10,12,13,37

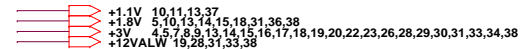
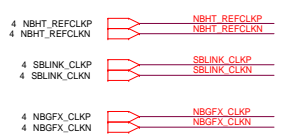
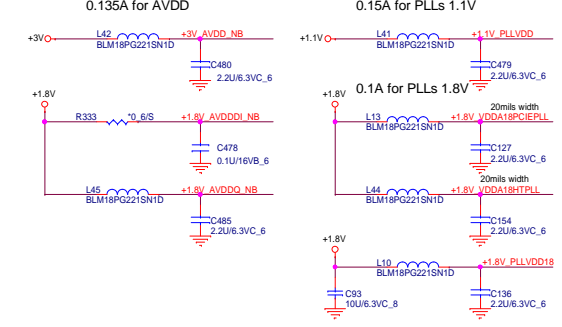
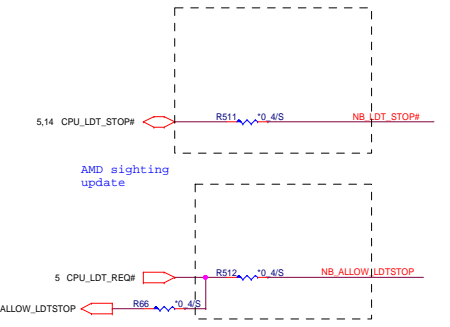


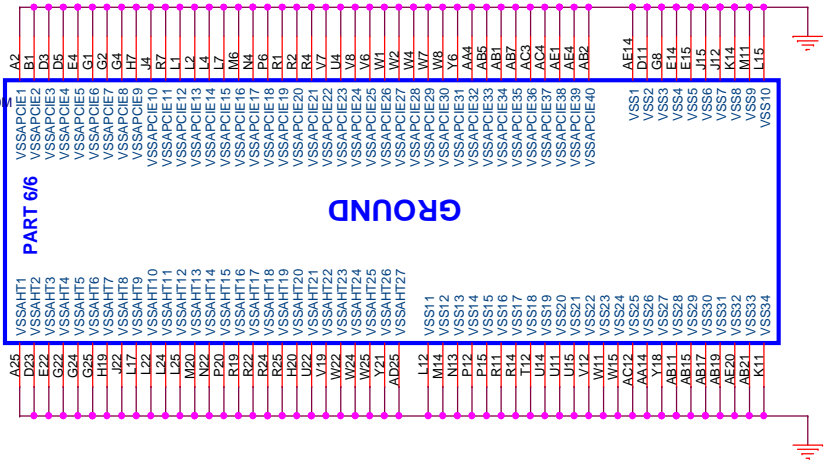
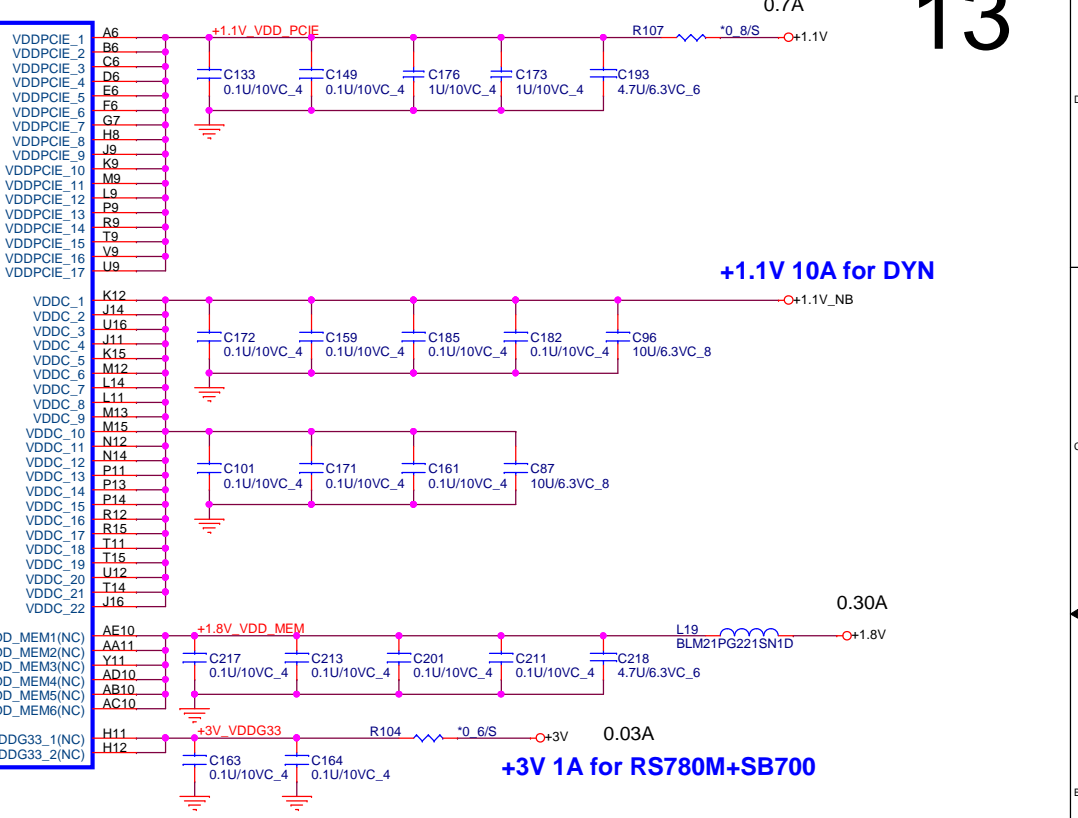
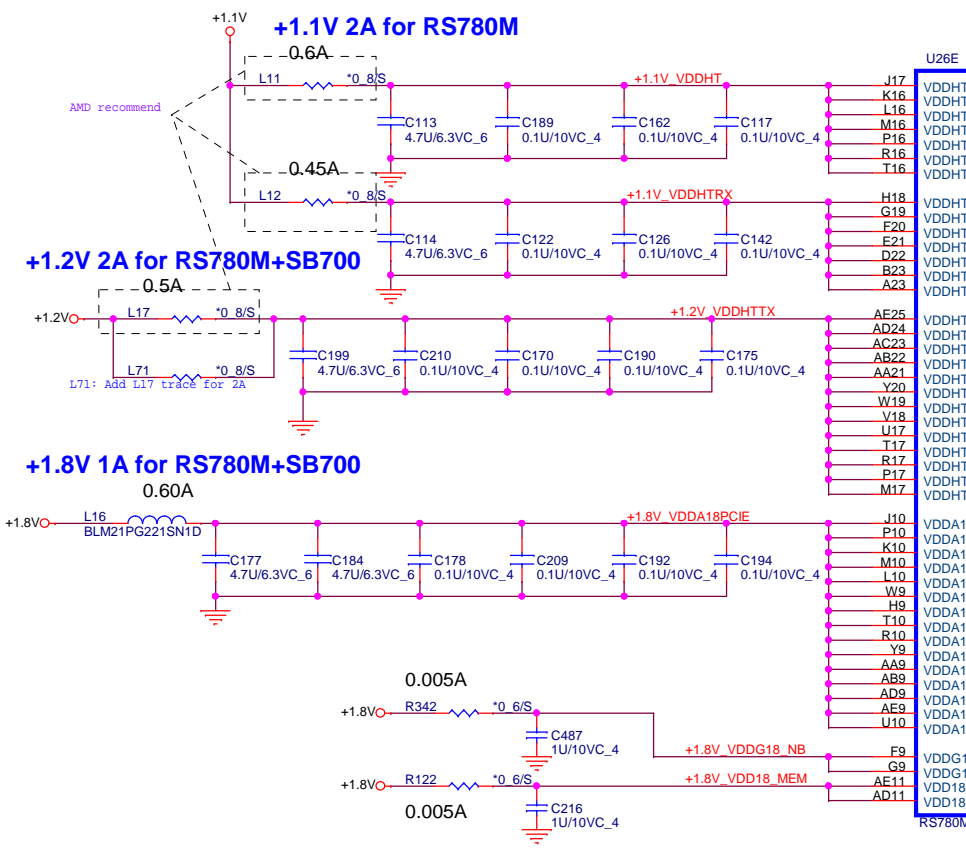
**PROJECT : TT3**  
Quanta Computer Inc.

|   |  |           |
|---|--|-----------|
| Size<br>B                                       | Document Number<br>RS780M-PCIE I/F 2/4 | Rev<br>1A |
| Date: Wednesday, August 27, 2008 Sheet 11 of 41 |  |           |



As output to the voltage regulator for PWM of RS780M core voltage.





- +1.1V NB 34
- +1.1V 10, 11, 12, 37
- +1.2V 4, 5, 14, 16, 17, 34, 37
- +1.8V 5, 10, 12, 14, 15, 18, 31, 36, 38
- +3V 4, 5, 7, 8, 9, 12, 14, 15, 16, 17, 18, 19, 20, 22, 23, 26, 28, 29, 30, 31, 33, 34, 38



**PROJECT : TT3**  
**Quanta Computer Inc.**

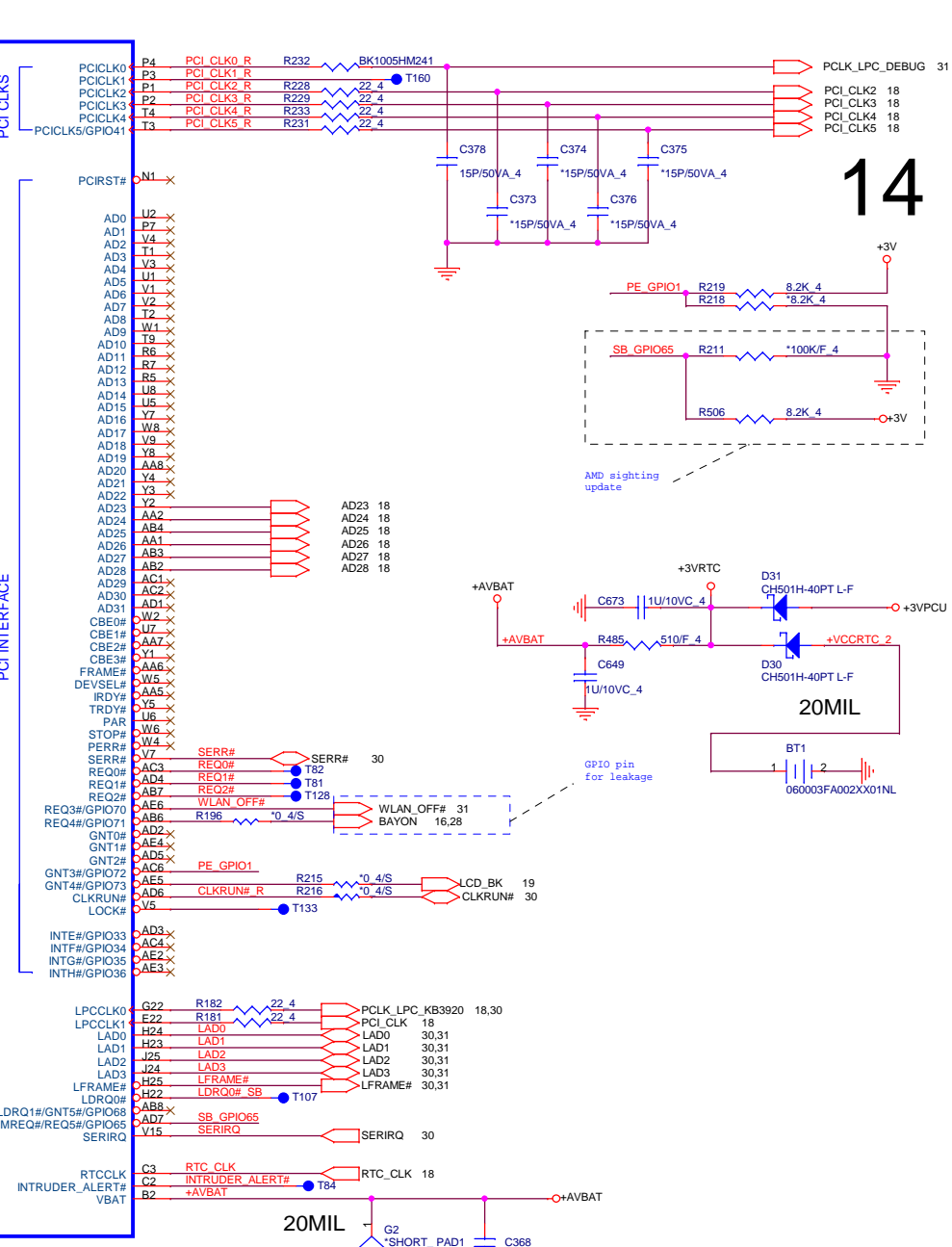
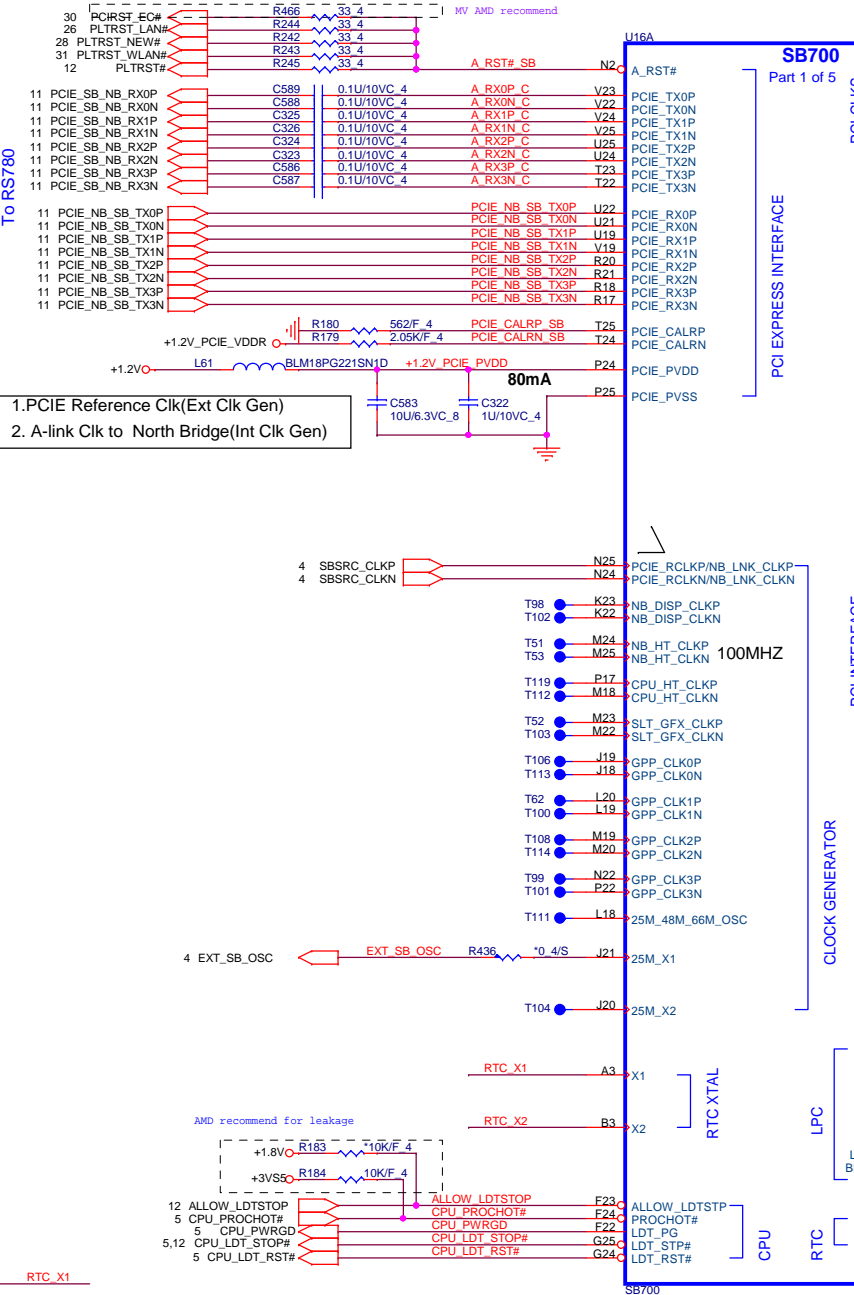
|   |                                     |           |
|---|-------------------------------------|-----------|
| Size<br>B   | Document Number<br>RS780M-POWER 4/4 | Rev<br>1A |
| Date: Wednesday, August 27, 2008 1 Sheet 13 of 41 |                                     |           |

PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U600

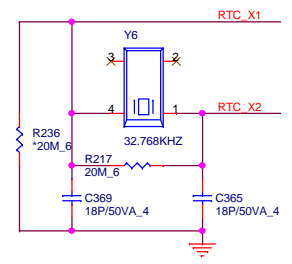


To RS780

1. PCIe Reference Clk (Ext Clk Gen)
2. A-link Clk to North Bridge (Int Clk Gen)



14



- +1.2V 4,5,13,16,17,34,37
- +1.8V 5,10,12,13,15,18,31,36,38
- +3V 4,5,7,8,9,12,13,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38
- +3VPCU 5,19,25,29,30,32,33,35,37,39



PROJECT : TT3  
Quanta Computer Inc.

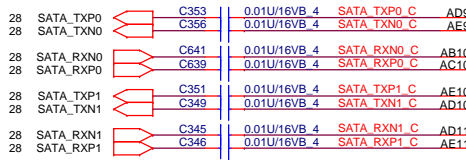
|                                  |  |                |
|----------------------------------|--|----------------|
| Size Custom                      | Document Number SB700-PCIE/PCI/CPU/LPC 1/4 | Rev 1A         |
| Date: Wednesday, August 27, 2008 |  | Sheet 14 of 41 |



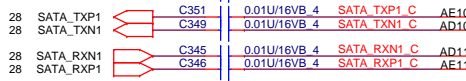


**PLACE SATA AC COUPLING CAPS CLOSE TO SB600**

### SATA1



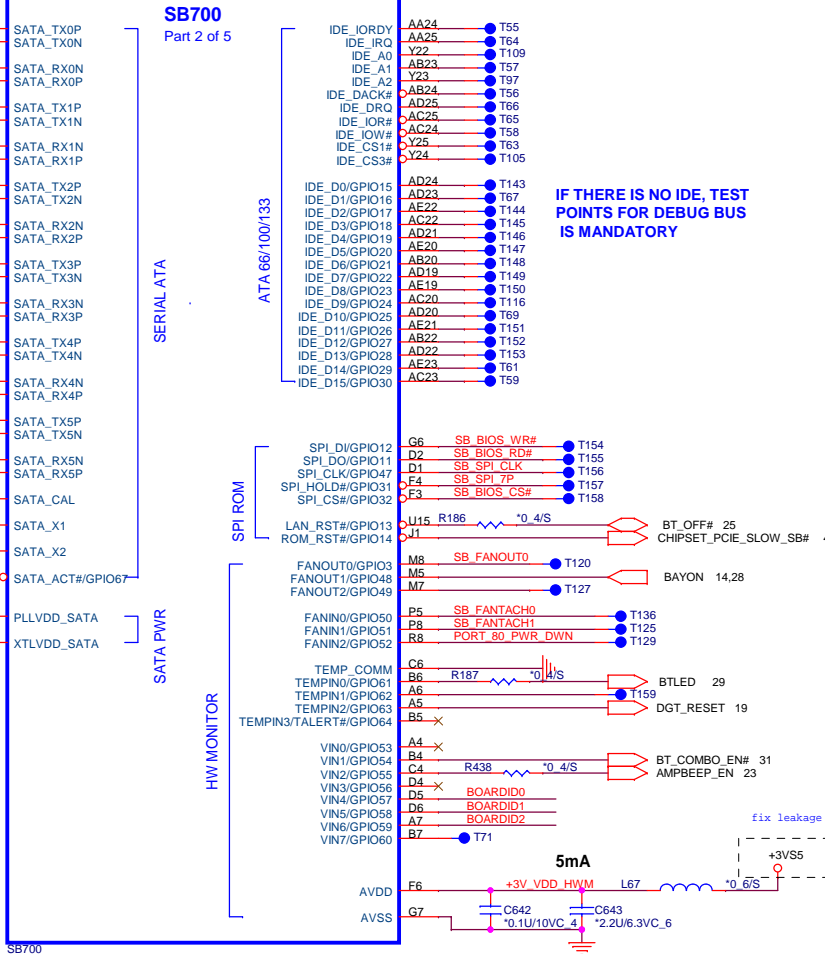
### SATA ODD



U16B

### SB700

Part 2 of 5

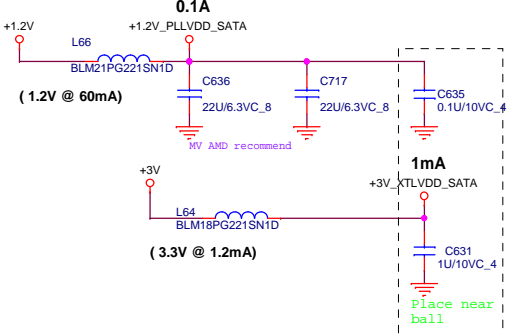
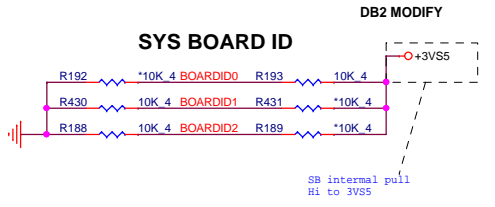
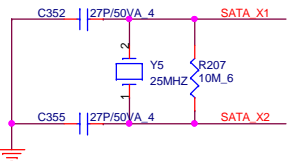
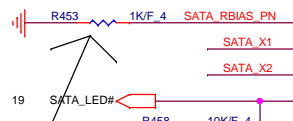


**IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY**

| VRAM / Clock Gen | Samsung Realtek | Qimonda ICS | Hynix Siligo |
|------------------|-----------------|-------------|--------------|
| Board ID         | (0.0.0)         | (1.0.0)     | (0.1.0)      |
| BOARDID0         | R192 Stuff      | R193 Stuff  | R192 Stuff   |
| BOARDID1         | R430 Stuff      | R430 Stuff  | R431 Stuff   |
| BOARDID2         | R188 Stuff      | R188 Stuff  | R188 Stuff   |

**PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U600**

**NOTE:**  
 R635 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

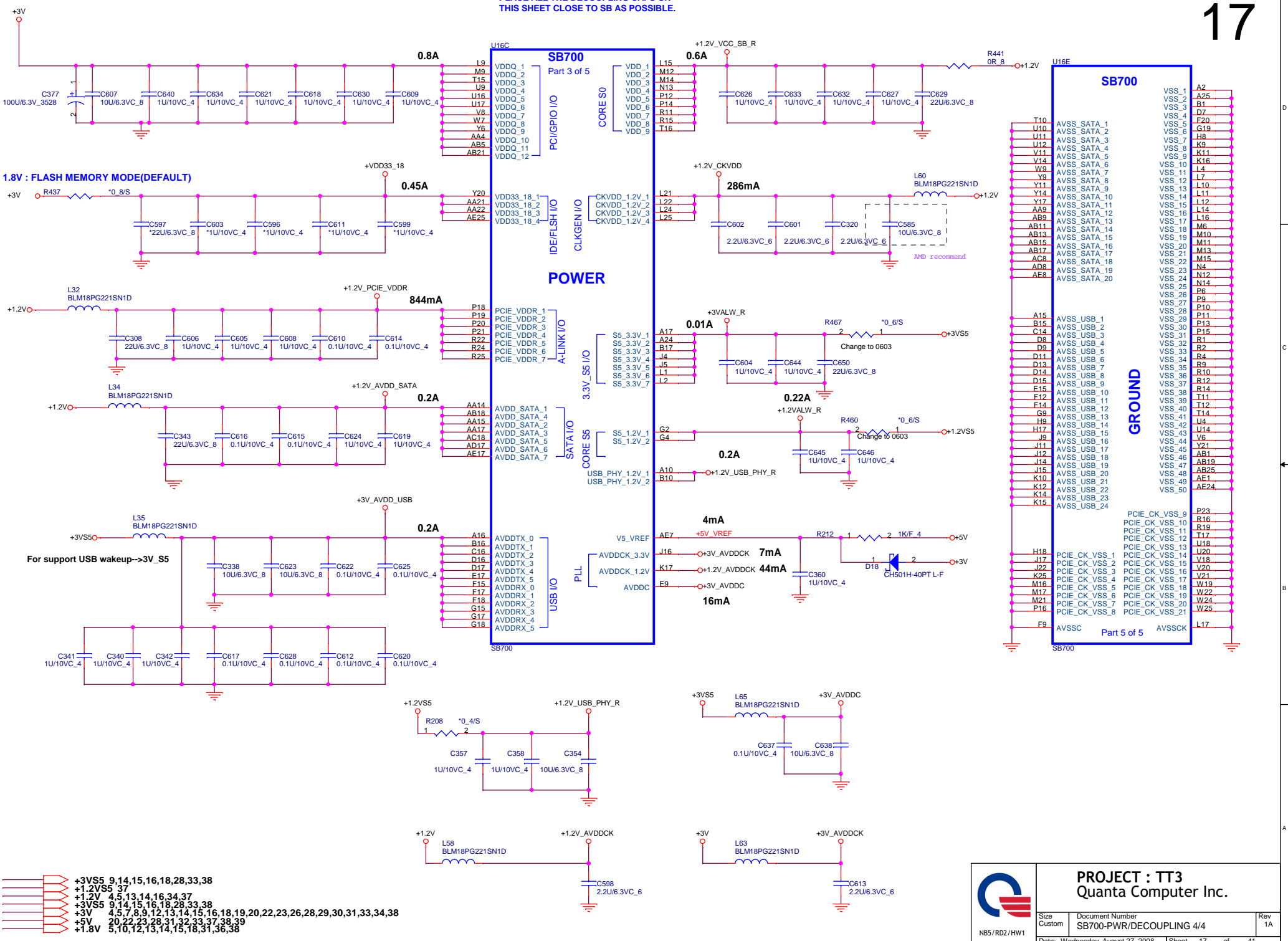


+1.2V 4,5,13,14,17,34,37  
 +3V 4,5,7,8,9,12,13,14,15,17,18,19,20,22,23,26,28,29,30,31,33,34,38

**PROJECT : TT3**  
 Quanta Computer Inc.

|   |  |        |
|---|--|--------|
| Size Custom                                     | Document Number SB700-SATA/IDE/HWM/SPI 3/4 | Rev 1A |
| Date: Wednesday, August 27, 2008 Sheet 16 of 41 |  |        |

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



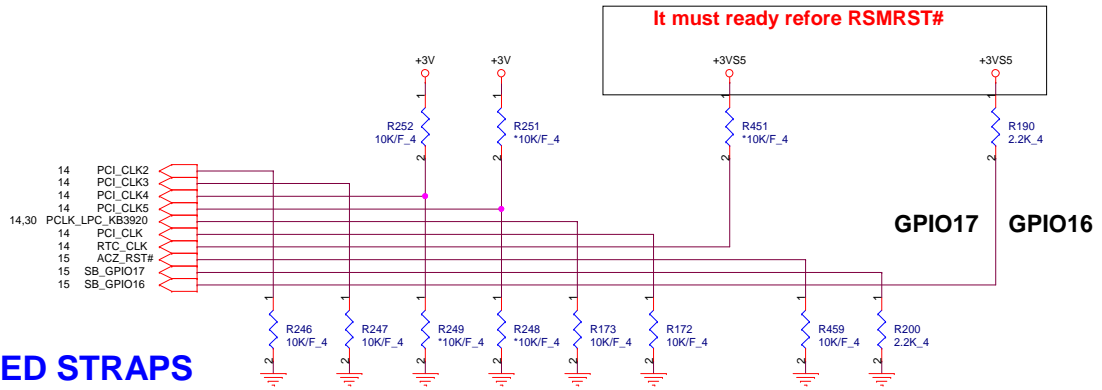
- +3VS5 9,14,15,16,18,28,33,38
- +1.2V\_S5 37
- +1.2V 4,5,13,14,16,34,37
- +3VS5 9,14,15,16,18,28,33,38
- +3V 4,5,7,8,9,12,13,14,15,16,18,19,20,22,23,26,28,29,30,31,33,34,38
- +5V 20,22,23,28,31,32,33,37,38,39
- +1.8V 5,10,12,13,14,15,18,31,36,38



**PROJECT : TT3**  
**Quanta Computer Inc.**

|                                  |  |                |
|----------------------------------|--|----------------|
| Size Custom                      | Document Number SB700-PWR/DECOUPLING 4/4 | Rev 1A         |
| Date: Wednesday, August 27, 2008 |  | Sheet 17 of 41 |

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



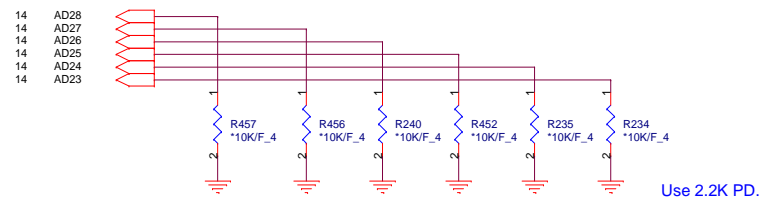
**OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.**

**REQUIRED STRAPS**

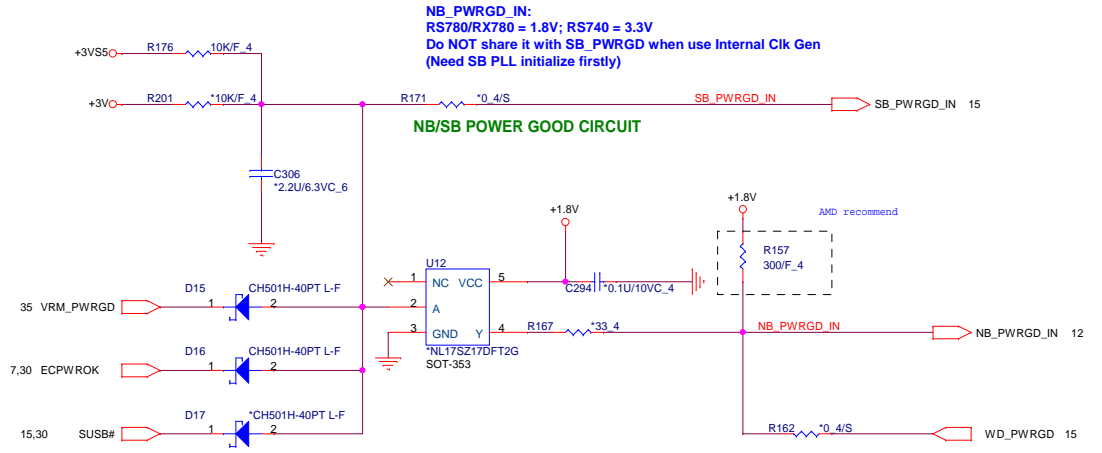
|                  | PCI_CLK2                           | PCI_CLK3                       | PCI_CLK4 | PCI_CLK5 | PCLK_LPC_KB3920        | PCI_CLK                    | RTC_CLK                                     | AZ_RST#                         | GP17   | GP16    |
|------------------|------------------------------------|--------------------------------|----------|----------|------------------------|----------------------------|---|---------------------------------|--|---------|
| <b>PULL HIGH</b> | BOOTFAIL TIMER ENABLED             | USE DEBUG STRAPS               | RESERVED | RESERVED | EC ENABLED             | CLKGEN ENABLED             | INTERNAL RTC<br>DEFAULT                     | ENABLE PCI MEM BOOT             | ROM TYPE:<br>H, H = Reserved<br>H, L = SPI ROM |         |
| <b>PULL LOW</b>  | BOOTFAIL TIMER DISABLED<br>DEFAULT | IGNORE DEBUG STRAPS<br>DEFAULT |          |          | EC DISABLED<br>DEFAULT | CLKGEN DISABLED<br>DEFAULT | EXT. RTC (PD on X1, apply 32KHz to RTC_CLK) | DISABLE PCI MEM BOOT<br>DEFAULT | L, H = LPC ROM<br>L, L = FWH ROM               | DEFAULT |

**DEBUG STRAPS**

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



|                  | PCI_AD28                  | PCI_AD27               | PCI_AD26                 | PCI_AD25               | PCI_AD24                           | PCI_AD23 |
|------------------|---------------------------|------------------------|--------------------------|------------------------|------------------------------------|----------|
| <b>PULL HIGH</b> | USE LONG RESET<br>DEFAULT | USE PCI PLL<br>DEFAULT | USE ACPI BCLK<br>DEFAULT | USE IDE PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT | RESERVED |
| <b>PULL LOW</b>  | USE SHORT RESET           | BYPASS PCI PLL         | BYPASS ACPI BCLK         | BYPASS IDE PLL         | USE EEPROM PCIE STRAPS             |          |



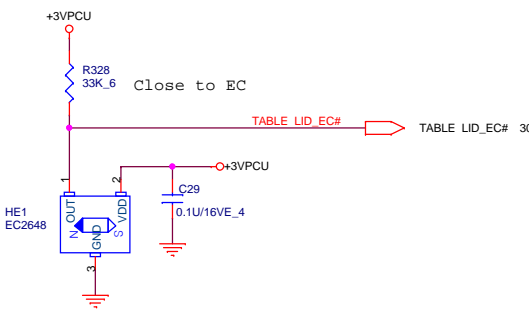
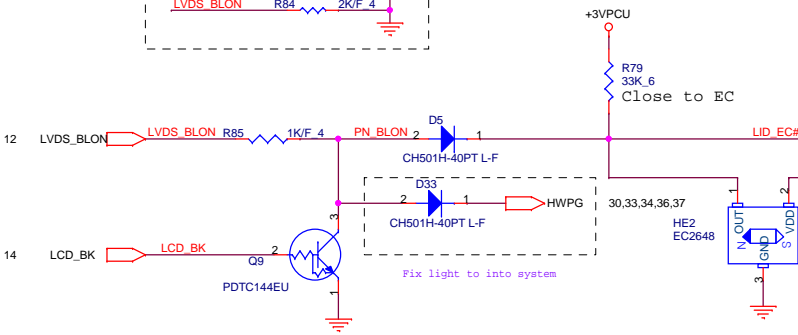
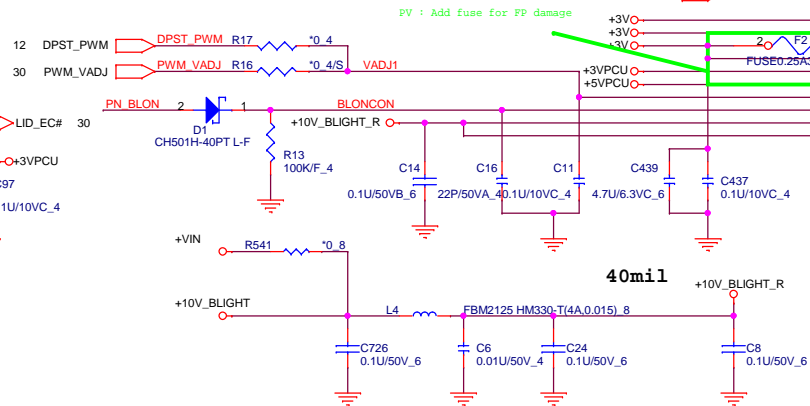
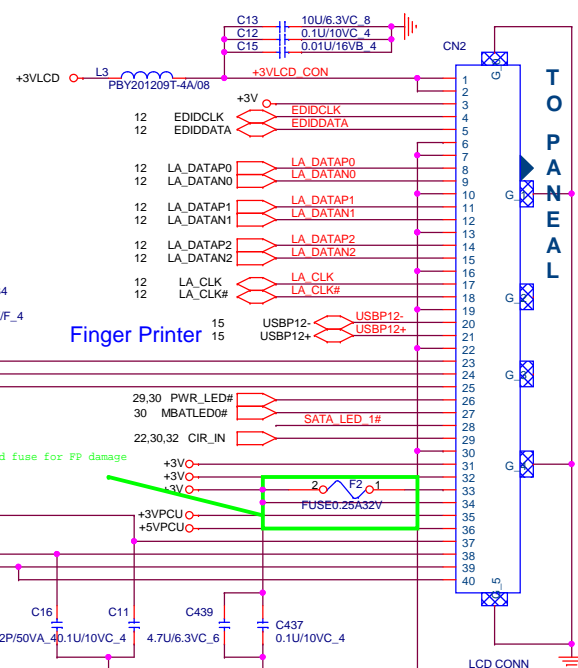
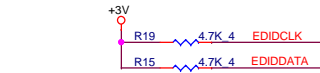
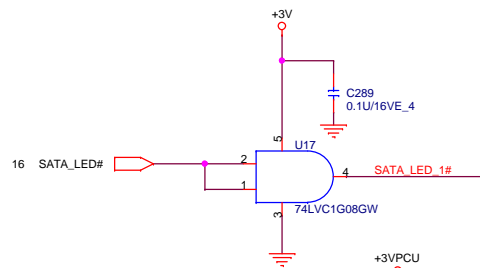
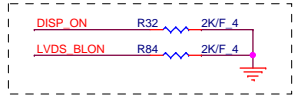
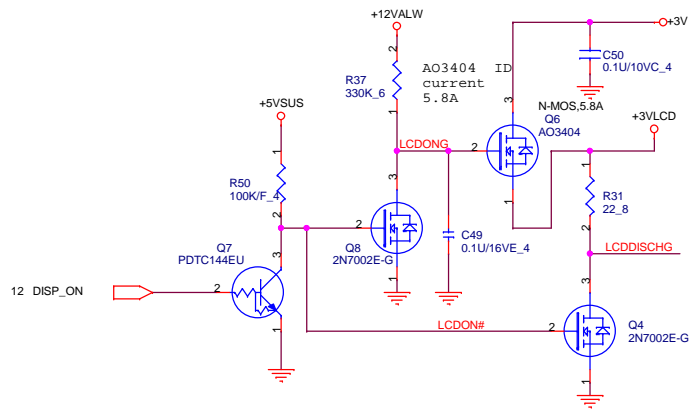
NB\_PWRGD\_IN:  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

AL17SZ17000 IC(SP) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(SP) SN74AUC1G17DBVR(SOT23-5) SOT23-5

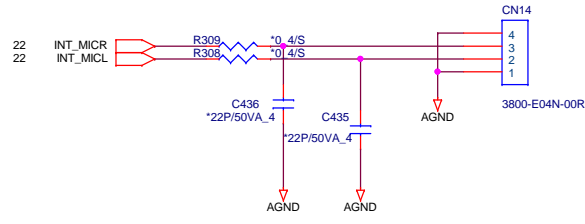
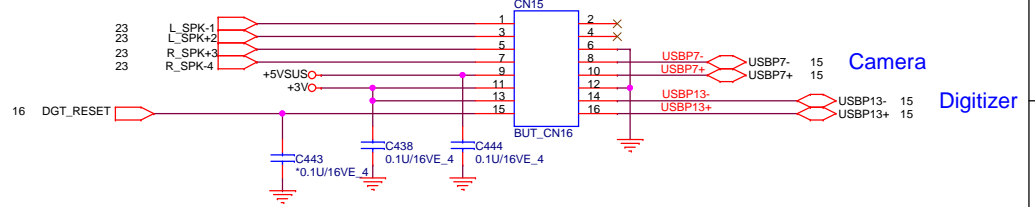
+1.8V 5,10,12,13,14,15,31,36,38  
+3V 4,5,7,8,9,12,13,14,15,16,17,19,20,22,23,26,28,29,30,31,33,34,38  
+3VS5 9,14,15,16,17,28,33,38

**PROJECT : TT3**  
**Quanta Computer Inc.**

Size Custom Document Number SB700-STRAPS,PWRGD Rev 1A  
Date: Wednesday, August 27, 2008 Sheet 18 of 41



Speaker / DMIC  
 +5VSUS --> Camera  
 +3V --> Digitizer  
 Digitizer control signal

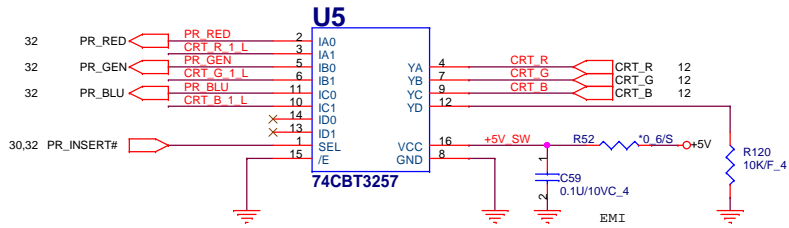


- +3VPCU 5,14,25,29,30,32,33,35,37,39
- +3V 4,5,7,8,9,12,13,14,15,16,17,18,20,22,23,26,28,29,30,31,33,34,38
- +3VSUS 15,21,24,25,29,31,33,34,35,36,38
- +5V 17,20,22,23,28,31,32,33,37,38,39
- +12VALW 28,31,33,38

**PROJECT : TT3**  
 Quanta Computer Inc.

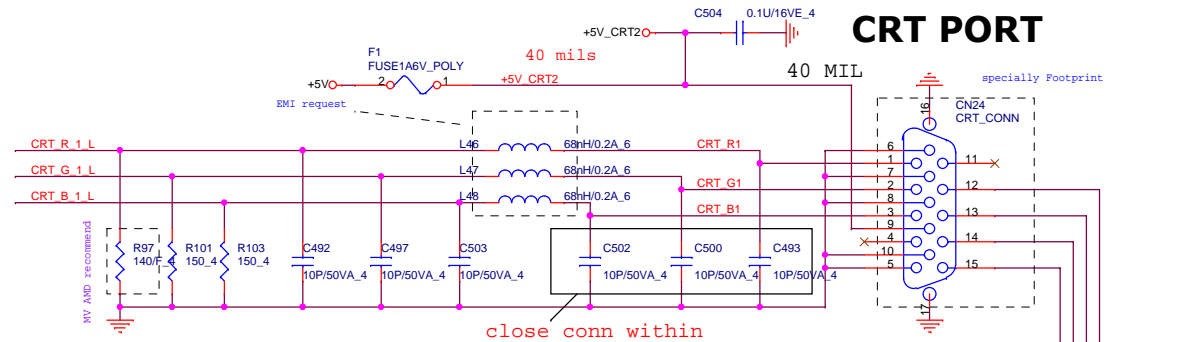
|                                  |                                       |        |
|----------------------------------|---------------------------------------|--------|
| Size Custom                      | Document Number<br>LCD CONN,HDMI CONN | Rev 1A |
| Date: Wednesday, August 27, 2008 |                                       |        |
| Sheet 19 of 41                   |                                       |        |

CRT SWITCH

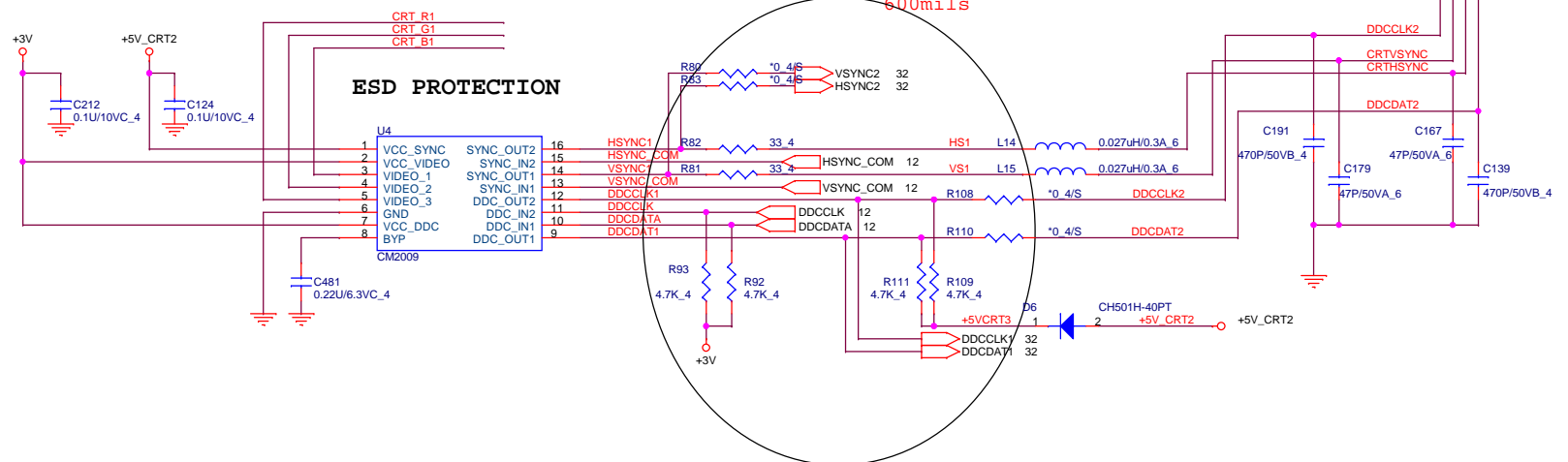


| inputs |     | function   |
|--------|-----|------------|
| /E     | SET |            |
| L      | L   | Y - port 0 |
| L      | H   | Y - port 1 |
| H      | X   | Disconnect |

CRT PORT



ESD PROTECTION



Del S-Video



+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,22,23,26,28,29,30,31,33,34,38  
+5V 17,22,23,28,31,32,33,37,38,39

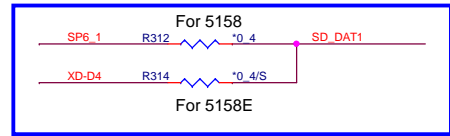
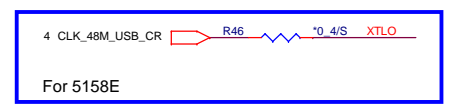
**PROJECT : TT3**  
Quanta Computer Inc.

|   |                            |        |
|---|----------------------------|--------|
| Size Custom                                     | Document Number CRT_TV_OUT | Rev 1A |
| Date: Wednesday, August 27, 2008 Sheet 20 of 41 |                            |        |

NB5/RD2/HW1

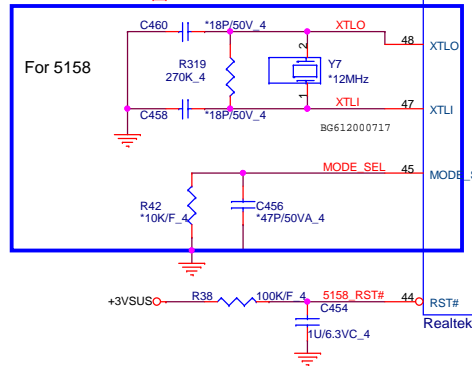


Fix card reader led problem

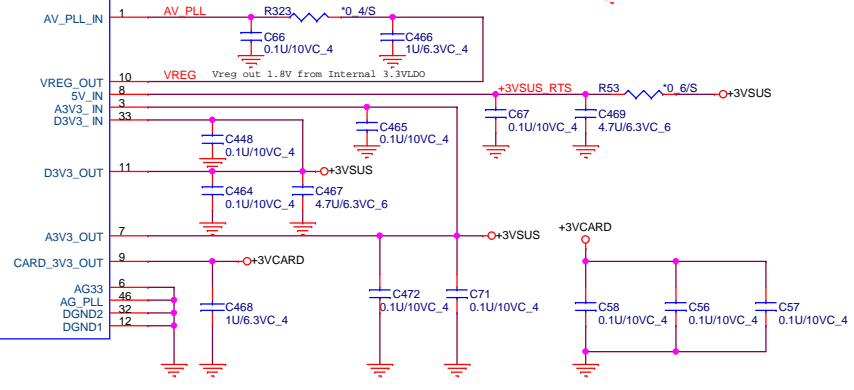
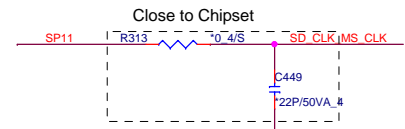


Note:

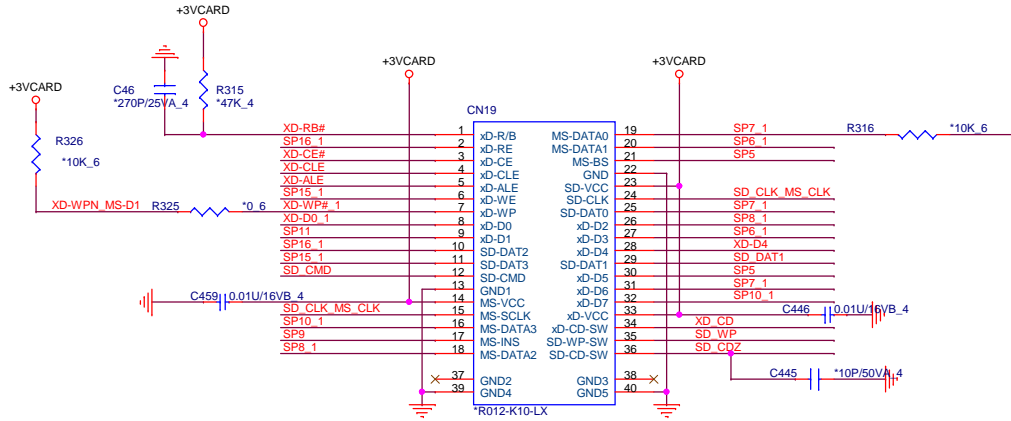
| SP0  | SD/MMC  | MS      | XD     |
|------|---------|---------|--------|
| SP1  |         |         | XD_CD# |
| SP2  | SD_WP   |         |        |
| SP3  | SD_CD#  |         |        |
| SP4  |         | XD_D4   |        |
| SP5  |         | MS_BS   | XD_D5  |
| SP6  |         | MS_D1   | XD_D3  |
| SP7  | SD_DAT0 | MS_D0   | XD_D6  |
| SP8  | SD_DAT7 | MS_D2   | XD_D2  |
| SP9  |         | MS_INS# |        |
| SP10 | SD_DAT6 | MS_D3   | XD_D7  |
| SP11 | SD_CLK  | MS_SCLK | XD_D1  |
| SP12 | SD_DAT5 |         | XD_D9  |
| SP13 | SD_DAT4 |         | XD_WP# |
| SP14 |         |         | XD_R/# |
| SP15 | SD_DAT3 |         | XD_WE# |
| SP16 | SD_DAT2 |         | XD_RE# |
| SP17 |         |         | XD_ALE |
| SP18 |         |         | XD_CE# |
| SP19 |         |         | XD_CLE |



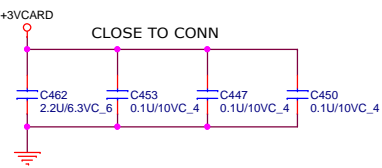
|     |                           |        |
|-----|---------------------------|--------|
| .43 | XD_CLE                    | XD_CLE |
| .42 | XD_CE#                    | XD_CE# |
| .41 | XD_ALE                    | XD_ALE |
| .40 | SD_DAT2/XD_RE#/CF_D12     | SP16   |
| .39 | SD_DAT3/XD_WE#/CF_D5      | SP15   |
| .38 | XD_RB#                    | SP15   |
| .37 | XD_WP#                    | SP15   |
| .36 | SD_CMD                    | SD_CMD |
| .35 | XD_D0                     | XD_D0  |
| .34 | SP11                      | SP11   |
| .33 | SD_DAT4/XD_WP#/CF_D6      | SP10   |
| .32 | SD_CMD                    | SD_CMD |
| .31 | SD_CLK/XD_D1/MS_CLK/CF_D7 | SP8    |
| .30 | XD_D0                     | SP7    |
| .29 | SP9                       | SP7    |
| .28 | SP8                       | SP7    |
| .27 | SP7                       | SP7    |
| .26 | SP6                       | SP6    |
| .25 | SP5                       | SP5    |



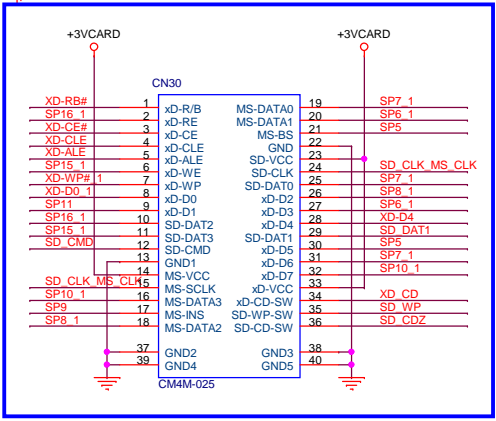
4 IN1 CARD READER  
XD, MMC / SD, MS / MSP



- SP7 R39 56.4 SP7\_1
- SP8 R44 56.4 SP8\_1
- SP10 R48 56.4 SP10\_1
- XD-D0 R55 56.4 XD-D0\_1
- XD-WP# R58 56.4 XD-WP#\_1
- SP15 R59 56.4 SP15\_1
- SP16 R61 56.4 SP16\_1
- SP6 R502 56.4 SP6\_1



Add Connector for EMI request

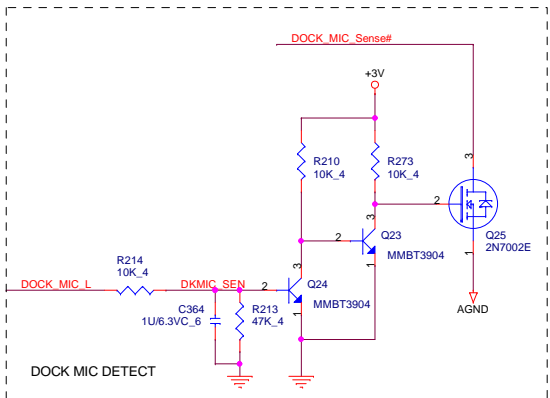
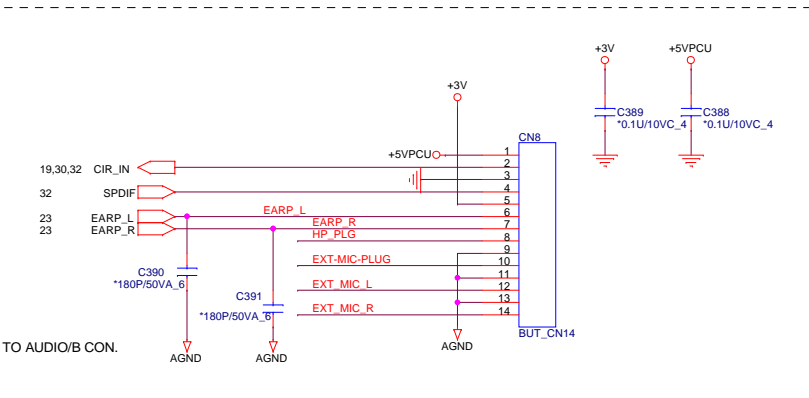
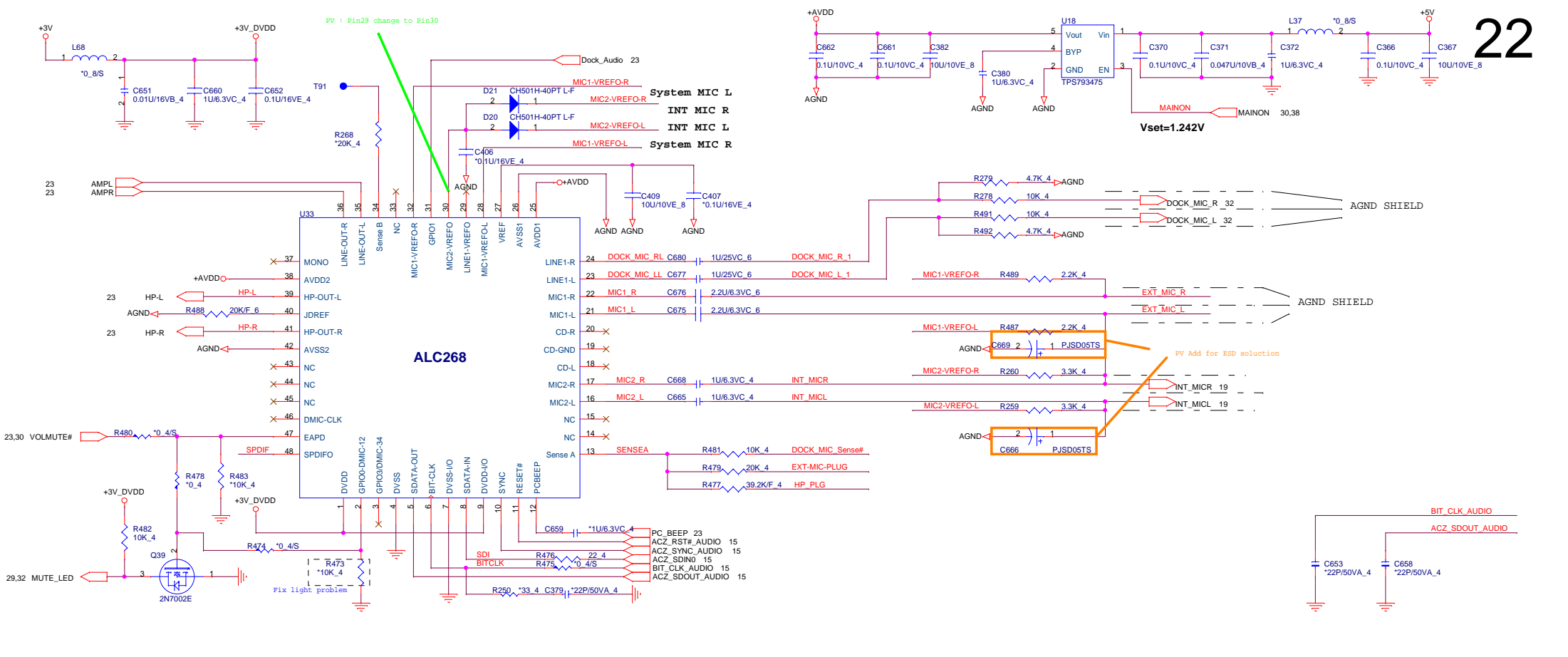


+3VSUS 15,24,25,29,31,33,34,35,36,38



PROJECT : TT3  
Quanta Computer Inc.

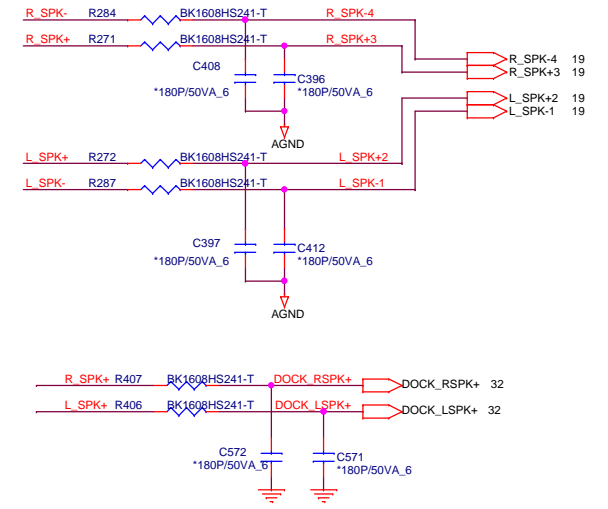
|                                  |  |                |
|----------------------------------|--|----------------|
| Size Custom                      | Document Number<br>RT5158 CARD READER CONTROLLER | Rev 1A         |
| Date: Wednesday, August 27, 2008 |  | Sheet 21 of 41 |



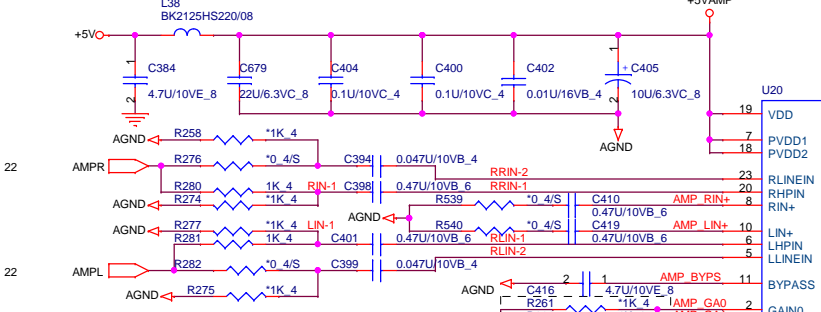
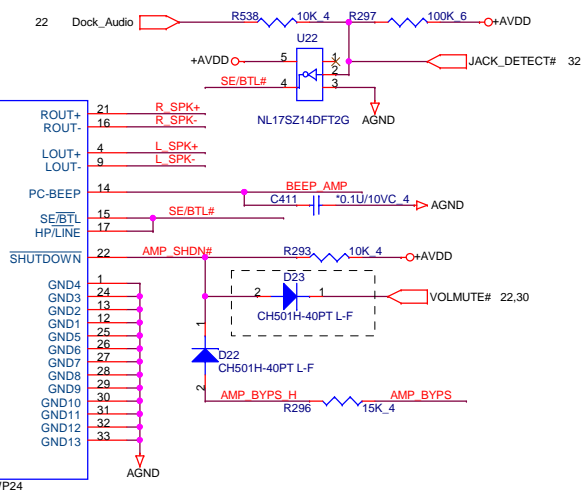
- +3V 4, 5, 7, 8, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 23, 26, 28, 29, 30, 31, 33, 34, 38
- +5V 17, 20, 23, 28, 31, 32, 33, 37, 38, 39
- +AVDD 23
- +5VPCU 19, 28, 29, 30, 33, 34, 35, 36, 37

|                |  |  |
|----------------|--|--|
|                | <b>PROJECT : TT3</b><br>Quanta Computer Inc. |  |
|                | Size<br>Custom                               | Document Number<br>Realtek Azalia ALC268 |
| NB5/RD2/HW1    | Date: Wednesday, August 27, 2008             | Rev<br>1A                                |
| Sheet 22 of 41 |  |  |

INT. SPEAKER



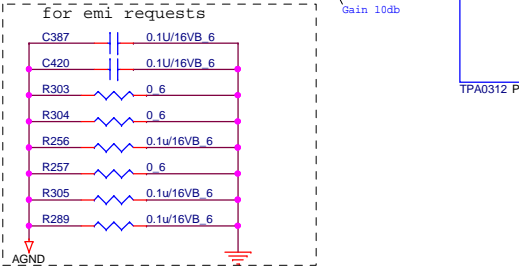
AUDIO AMPLIFIER



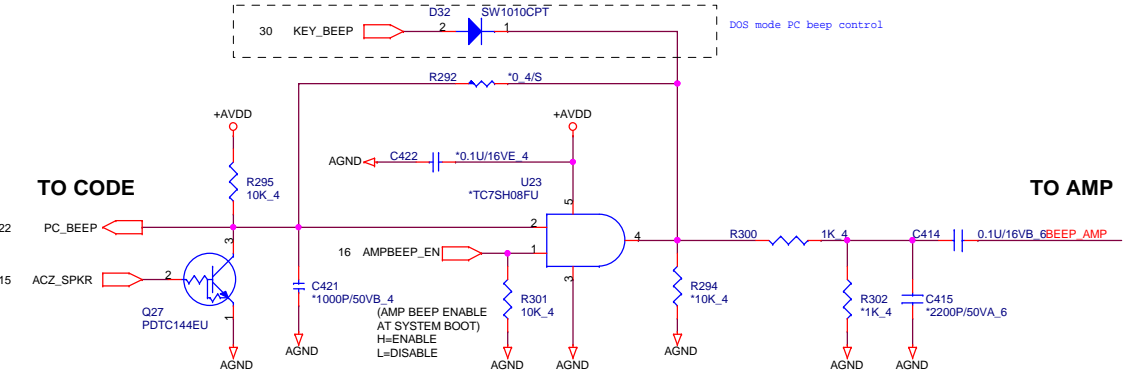
SI-2 remove r739 ,r731 from reatek request for fix BO voice when audio jack unplug

0312 Gain Table

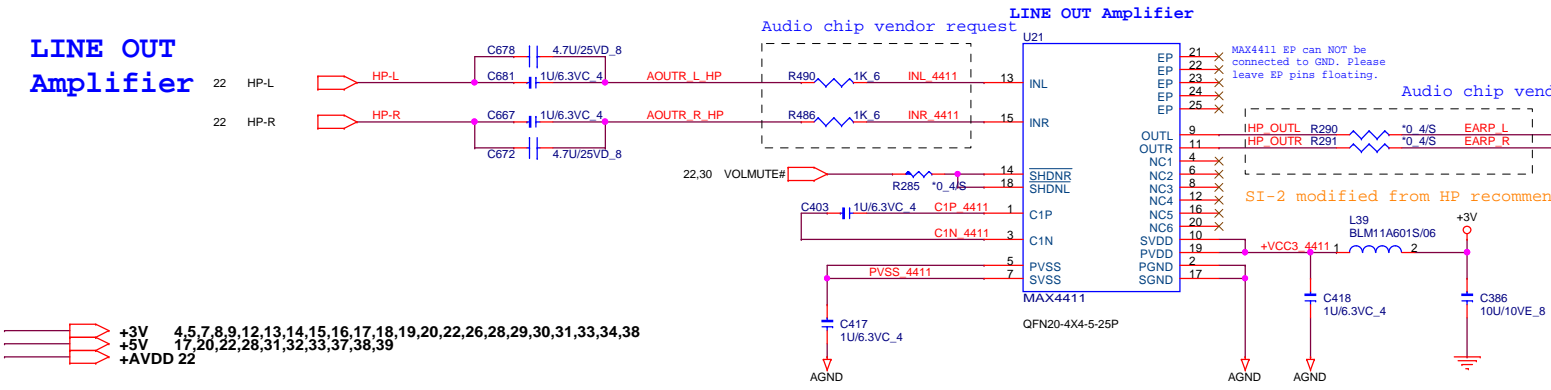
| GAIN0 | GAIN1 | SE/BTL | AV(INV) |
|-------|-------|--------|---------|
| 0     | 0     | 0      | 6dB     |
| 0     | 1     | 0      | 10dB    |
| 1     | 0     | 0      | 15.6dB  |
| 1     | 1     | 0      | 21.6dB  |
| x     | x     | 1      | 4.1dB   |



PCSPK BEEP



LINE OUT Amplifier



- +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,26,28,29,30,31,33,34,38
- +5V 17,20,22,28,31,32,33,37,38,39
- +AVDD 22

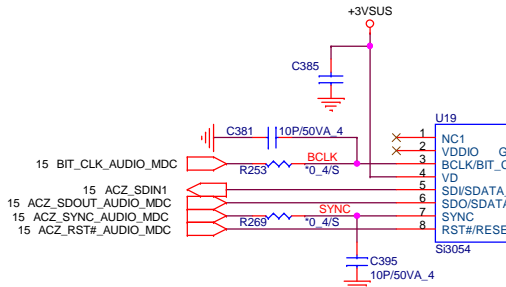
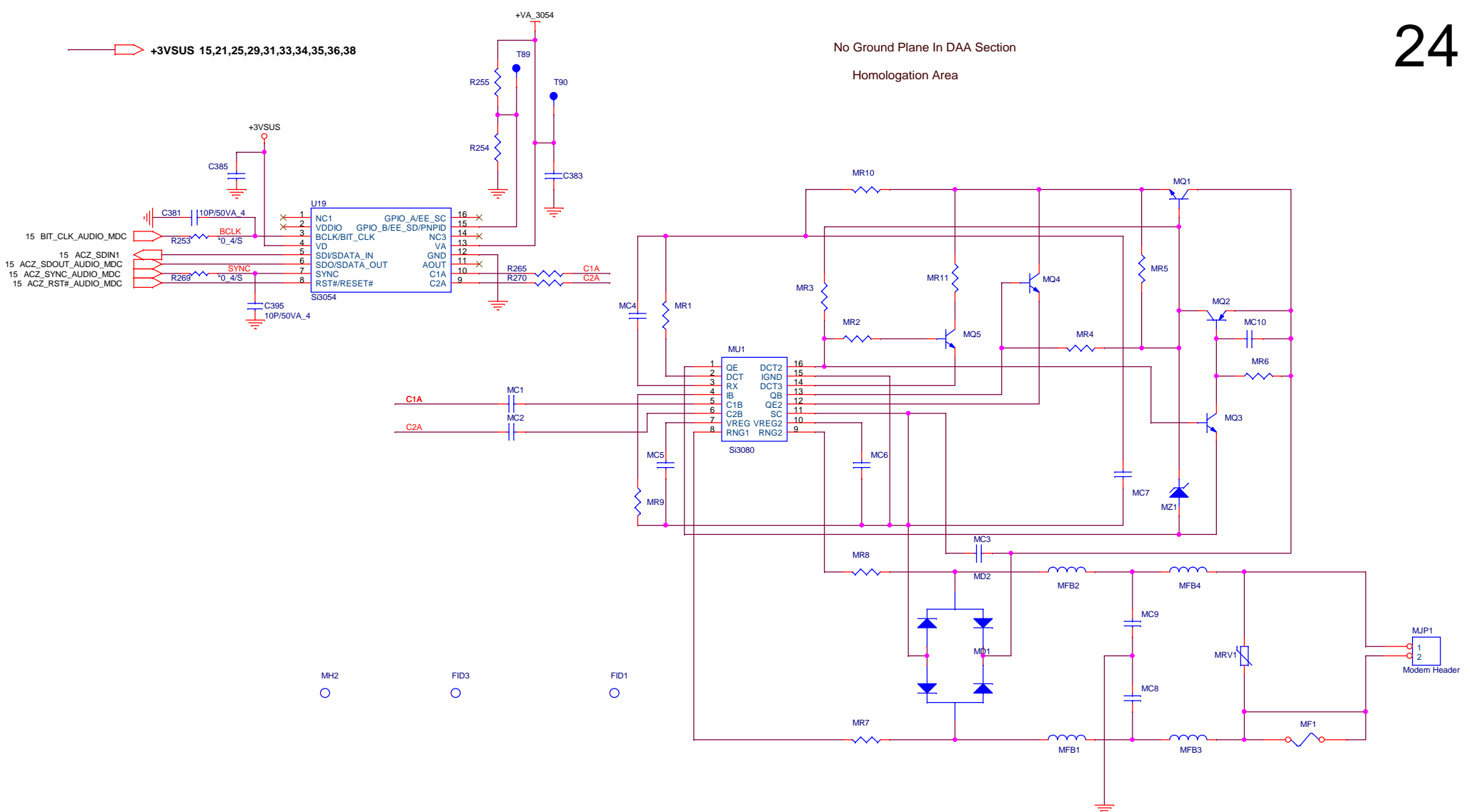


PROJECT : TT3  
Quanta Computer Inc.

|   |                                  |        |
|---|----------------------------------|--------|
| Size Custom                                     | Document Number JACK/AMP_TAP0312 | Rev 1A |
| Date: Wednesday, August 27, 2008 Sheet 23 of 41 |                                  |        |

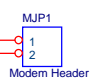
No Ground Plane In DAA Section

Homologation Area



15 BIT\_CLK\_AUDIO\_MDC  
15 ACZ\_SDIN1  
15 ACZ\_SDOUT\_AUDIO\_MDC  
15 ACZ\_SYNC\_AUDIO\_MDC  
15 ACZ\_RST#\_AUDIO\_MDC

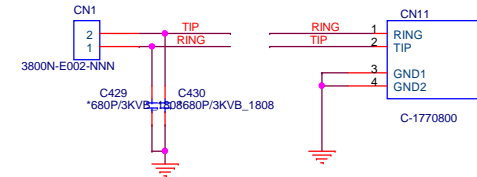
MH2 ○ FID3 ○ FID1 ○



**DESIGN SUBJECT TO CHANGE**

**SILICON LABORATORIES CONFIDENTIAL**

**RJ11**

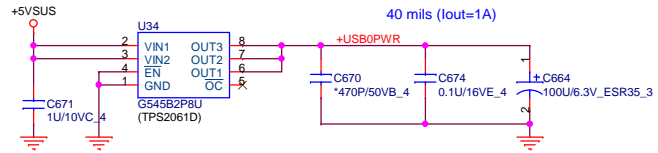


**PROJECT : TT3**  
**Quanta Computer Inc.**

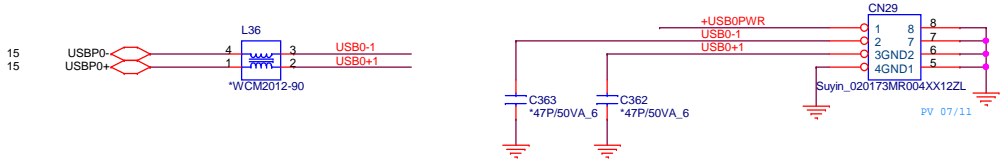
|                                  |                                       |                |
|----------------------------------|---------------------------------------|----------------|
| Size<br>Custom                   | Document Number<br><b>MODEM (DAA)</b> | Rev<br>1A      |
| Date: Wednesday, August 27, 2008 |                                       | Sheet 24 of 41 |

NB5/RD2/HW1

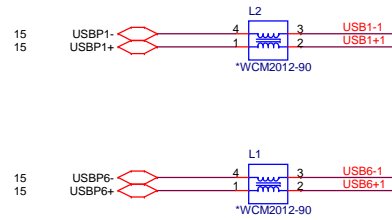
# USBX1



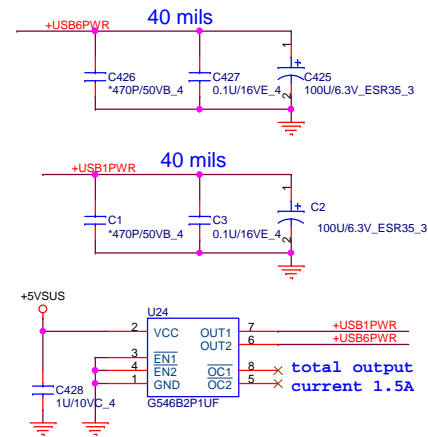
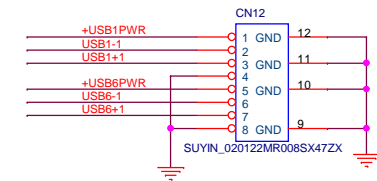
# USB 0



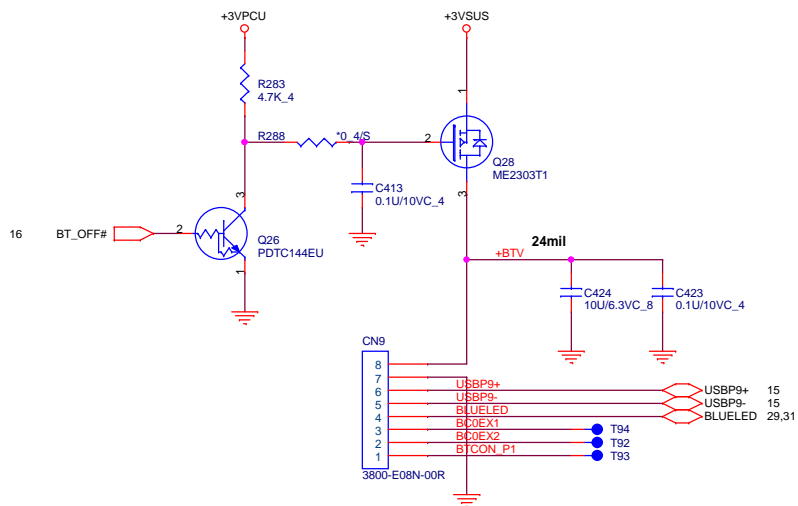
# USBX2



# USB 1 & 6



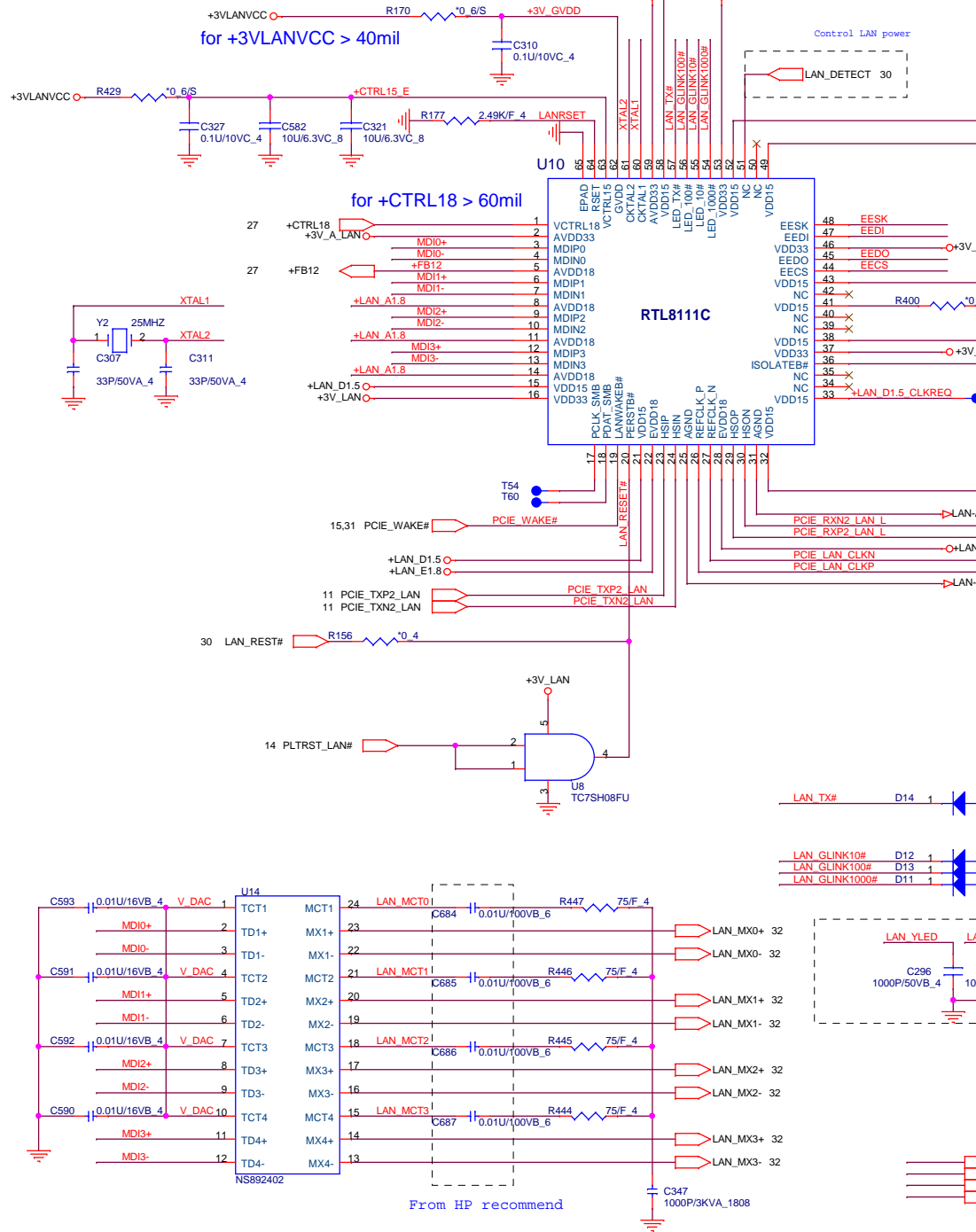
# BLUETOOTH



+3VPCU 5,14,19,29,30,32,33,35,37,39  
 +3VSUS 15,21,24,29,31,33,34,35,36,38  
 +5VSUS 19,30,32,33,38

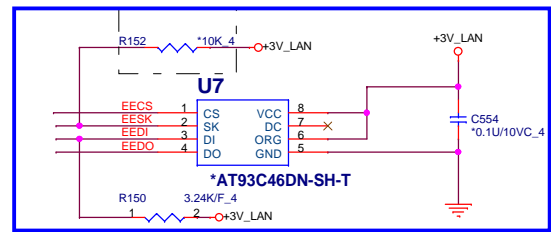
|             |                                  |  |                |
|-------------|----------------------------------|--|----------------|
|             |                                  | <b>PROJECT : TT3</b><br>Quanta Computer Inc. |                |
| Size Custom | Document Number Blue Tooth/USBX3 | Rev 1A                                       |                |
| NB5/RD2/HW1 |                                  | Date: Wednesday, August 27, 2008             | Sheet 25 of 41 |

# RTL8111C(10/100/1000)

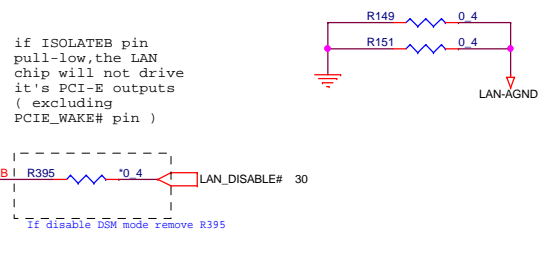


for 93C56 used. NC if 93C46 is used.

# 26

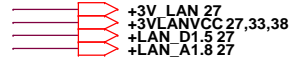
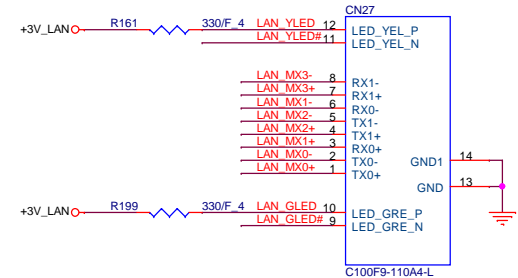
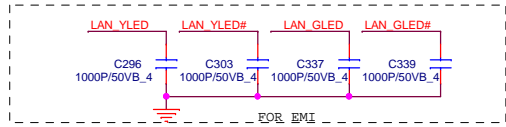
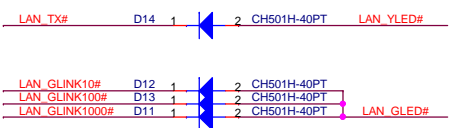


Remove LAN EEPROM



if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCI\_WAKE# pin)

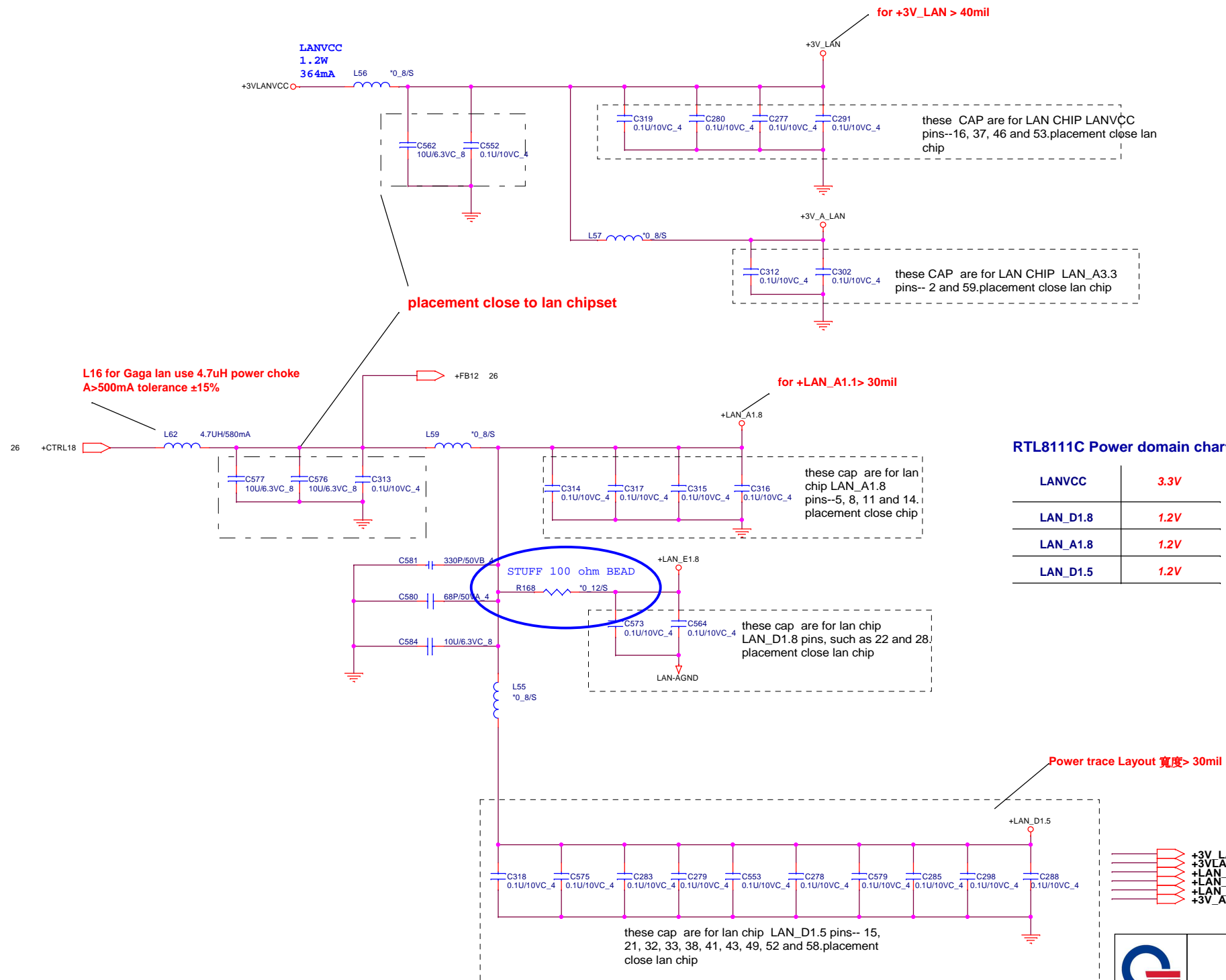
## RJ45



**PROJECT : TT3**  
**Quanta Computer Inc.**

|                                  |                                  |                |
|----------------------------------|----------------------------------|----------------|
| Size Custom                      | Document Number Pealtek RTL8111C | Rev 1A         |
| Date: Wednesday, August 27, 2008 |                                  | Sheet 26 of 41 |





RTL8111C Power domain chart

|          |      |
|----------|------|
| LANVCC   | 3.3V |
| LAN_D1.8 | 1.2V |
| LAN_A1.8 | 1.2V |
| LAN_D1.5 | 1.2V |

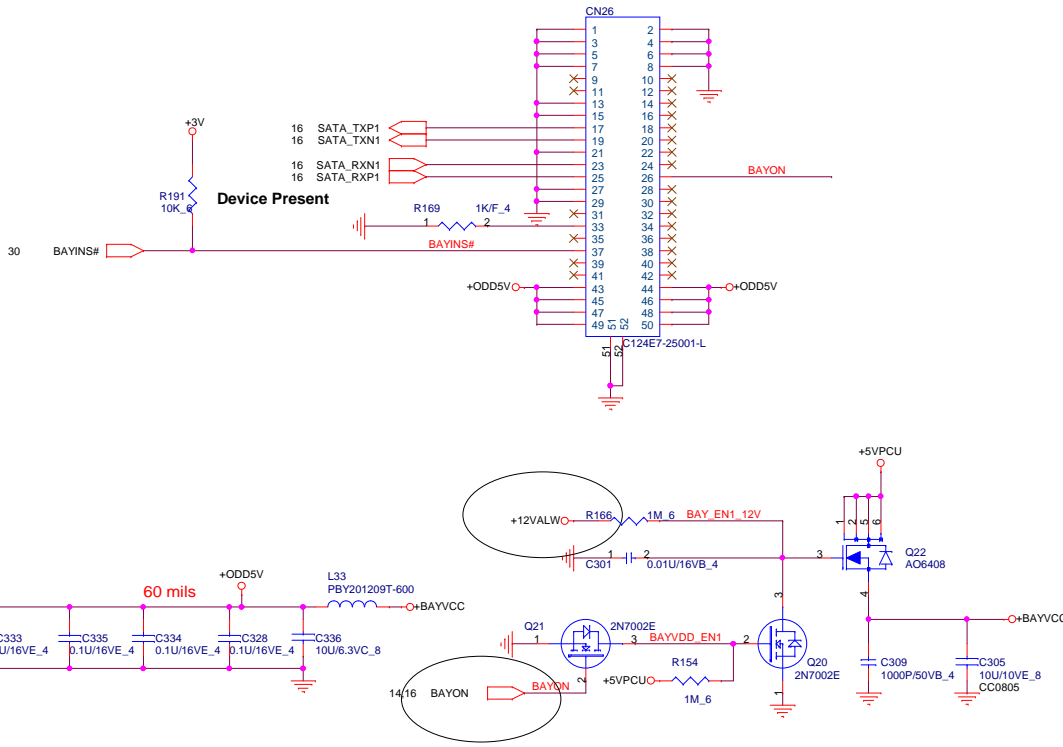
- +3V\_LAN 26
- +3VLANVCC 26,33,38
- +LAN\_D1.5 26
- +LAN\_A1.8 26
- +LAN\_E1.8 26
- +3V\_A\_LAN 26



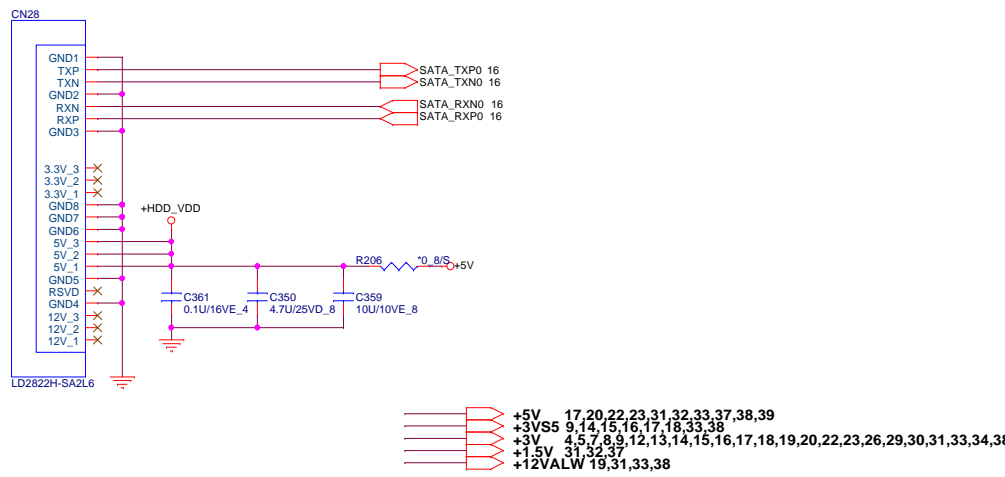
**PROJECT : TT3**  
Quanta Computer Inc.

|   |                           |        |
|---|---------------------------|--------|
| Size A3   | Document Number LAN POWER | Rev 1A |
| Date: Wednesday, August 27, 2008   Sheet 27 of 41 |                           |        |

### SATA ODD

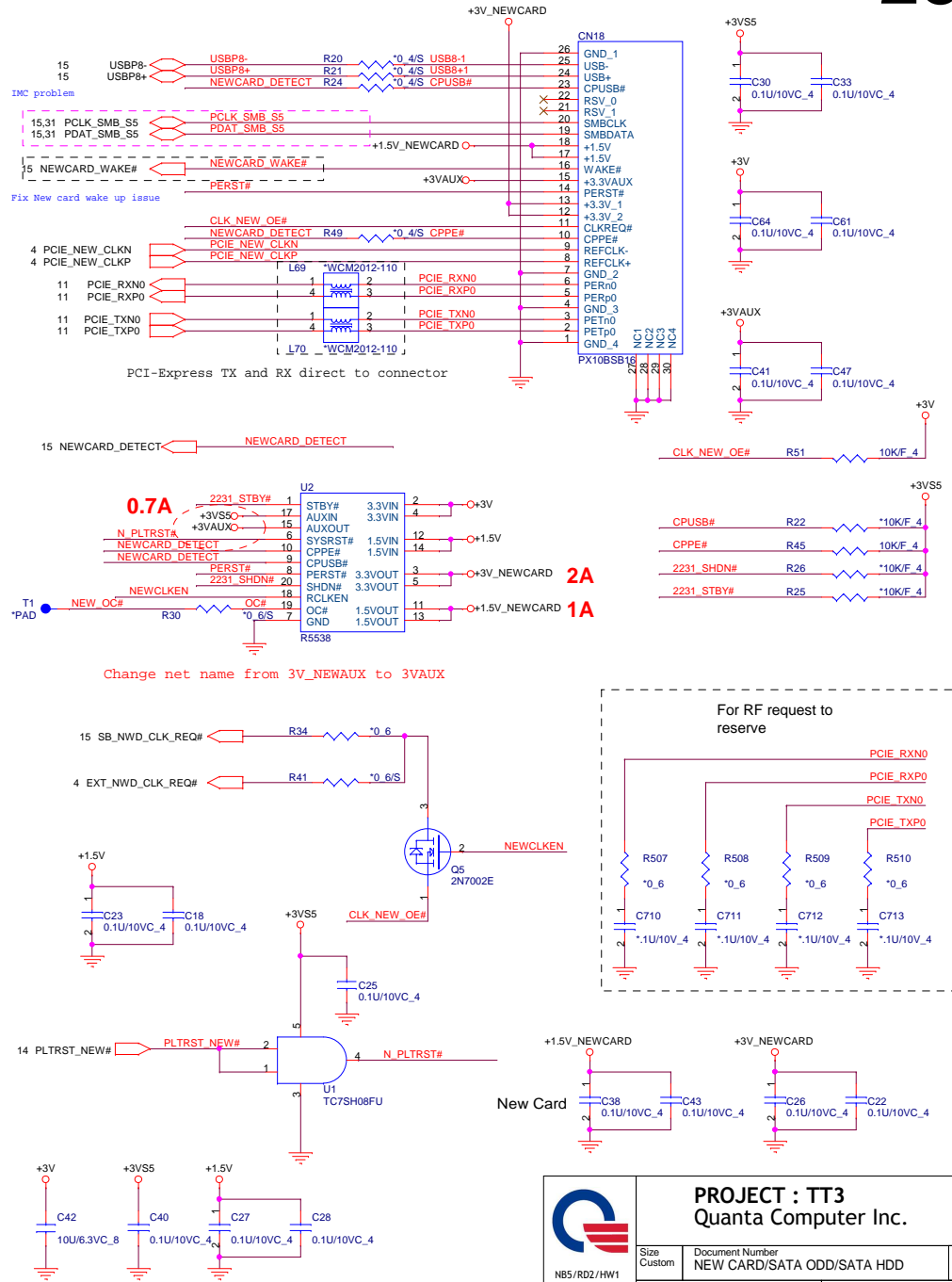


### SATA CONNECTOR



### NEWCARD

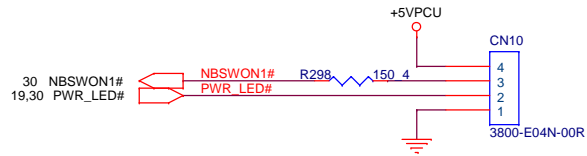
### NEWCARD (PCIEXPRESS\*1 + USB\*1)



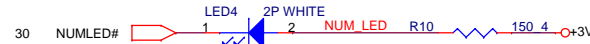
**PROJECT : TT3**  
**Quanta Computer Inc.**

|                                  |   |                |
|----------------------------------|---|----------------|
| Size Custom                      | Document Number<br>NEW_CARD/SATA ODD/SATA HDD | Rev 1A         |
| Date: Wednesday, August 27, 2008 |   | Sheet 28 of 41 |

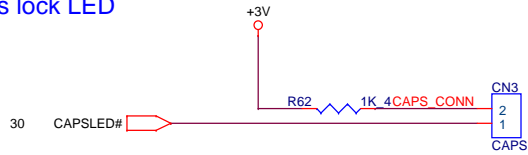
## FOR POWER ON SW BOARD



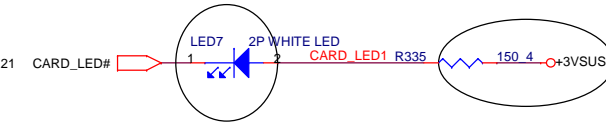
## Num lock LED



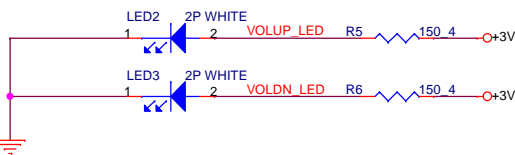
## Caps lock LED



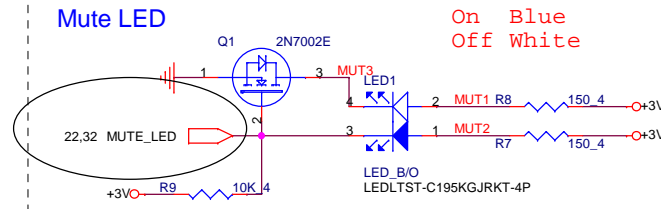
## Card Reader LED



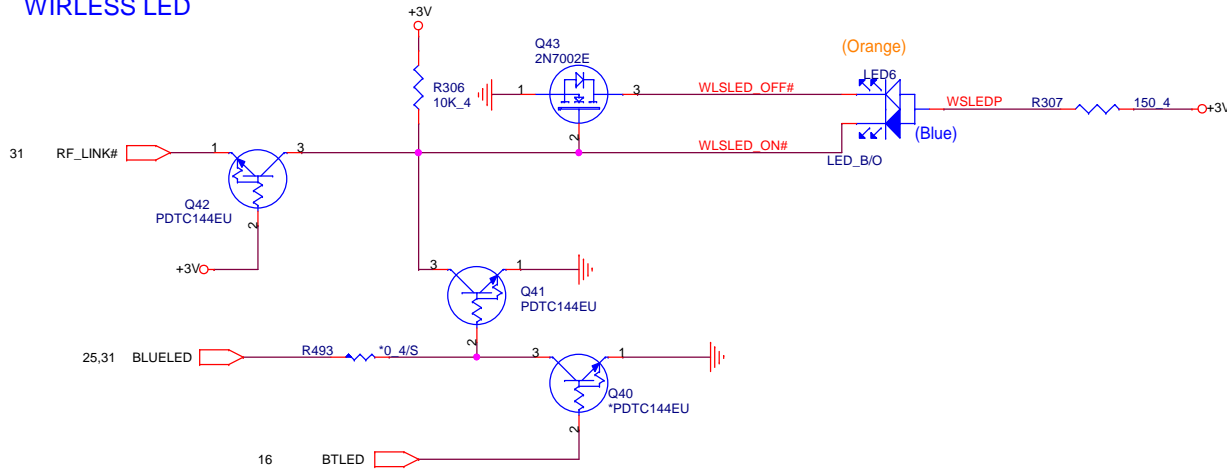
## Volume up/down LED



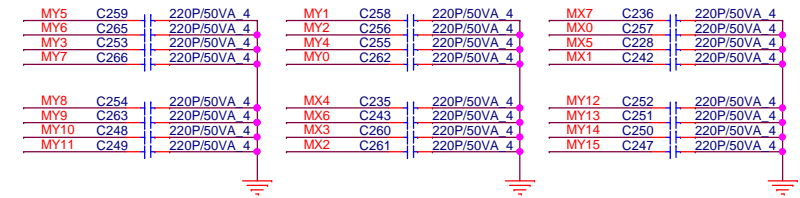
## Mute LED



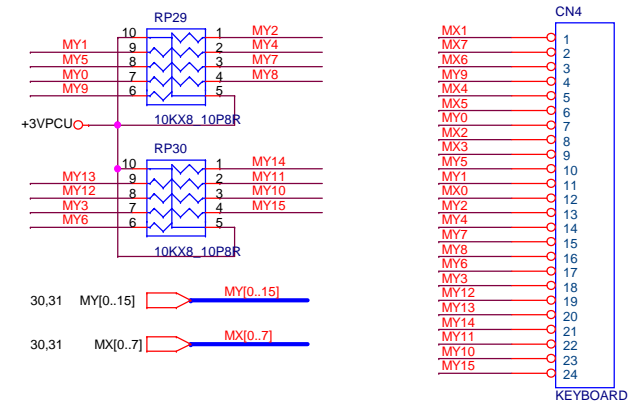
## WIRLESS LED



## Keyboard



## KEYBOARD PULL-UP

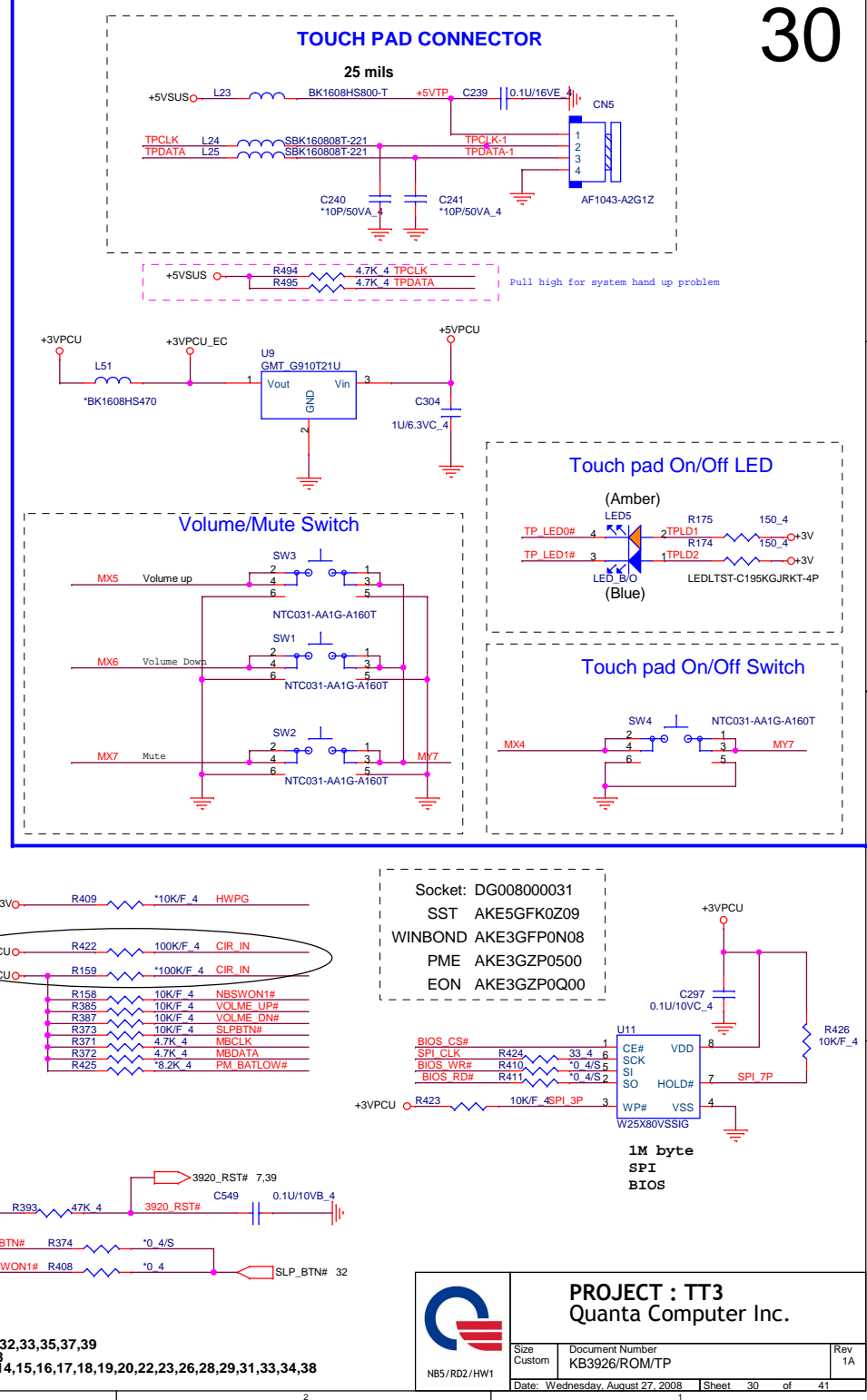
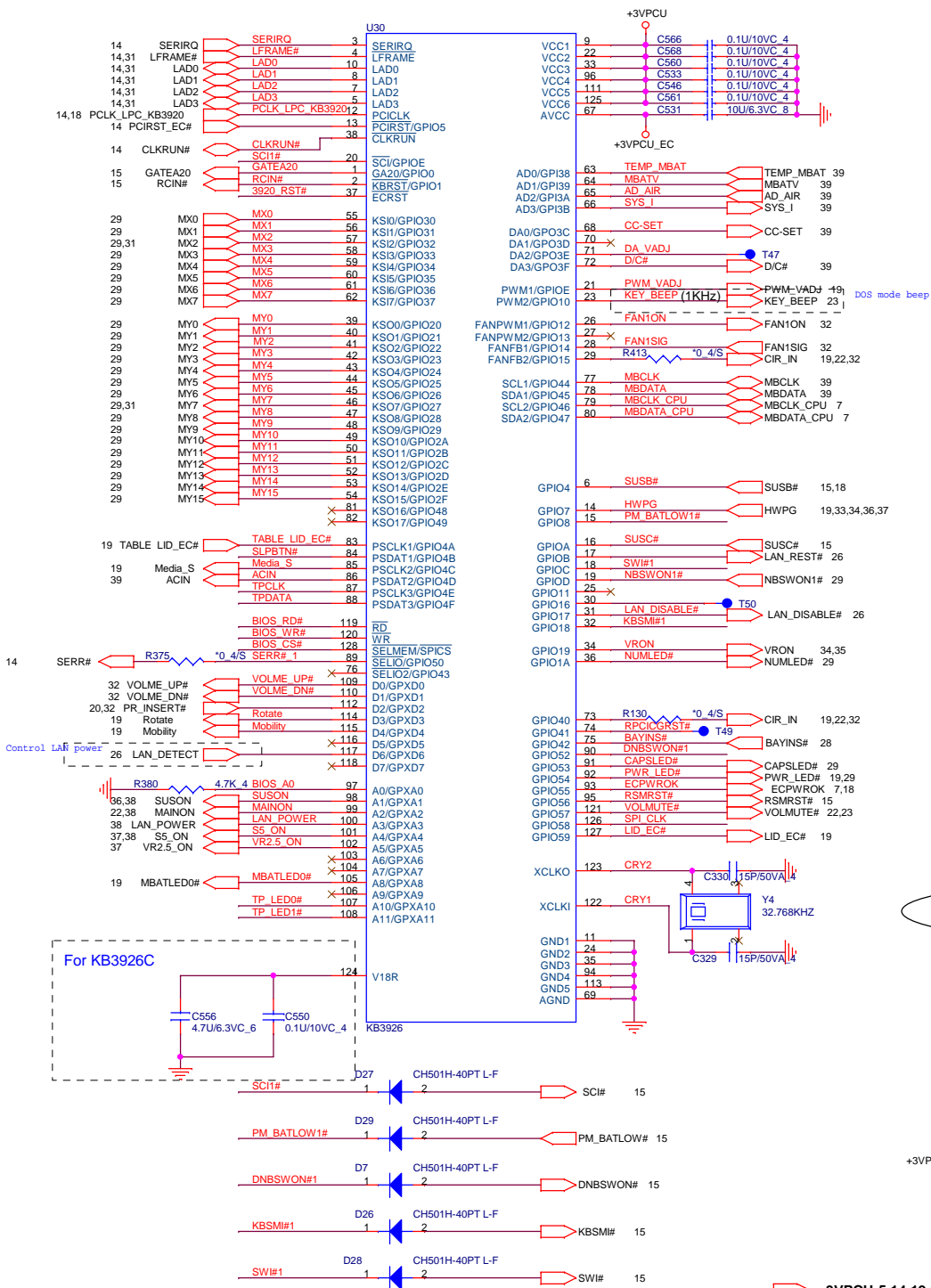


▶▶▶ +5VPCU 19,22,28,30,33,34,35,36,37  
▶▶▶ +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38  
▶▶▶ +3VSUS 15,21,24,25,31,33,34,35,36,38



**PROJECT : TT3**  
Quanta Computer Inc.

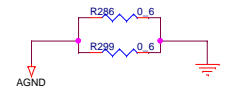
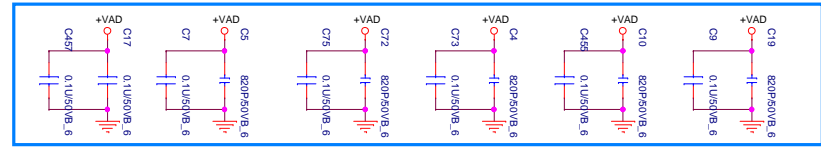
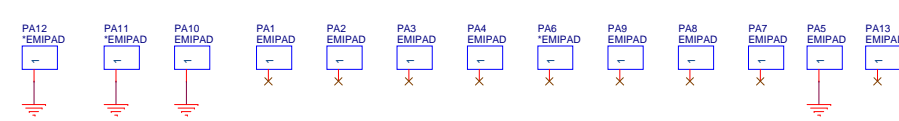
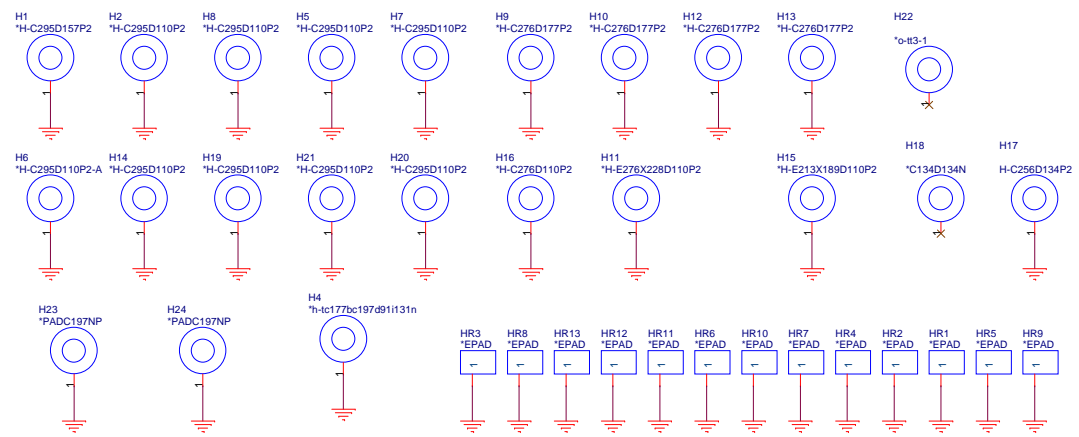
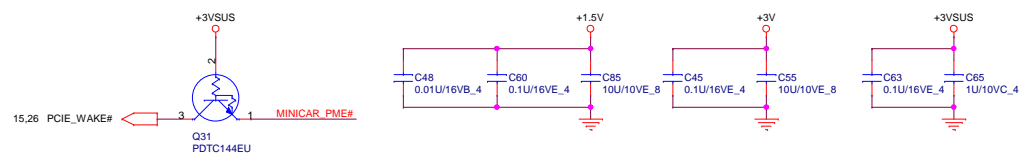
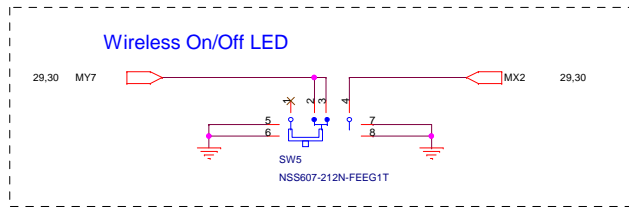
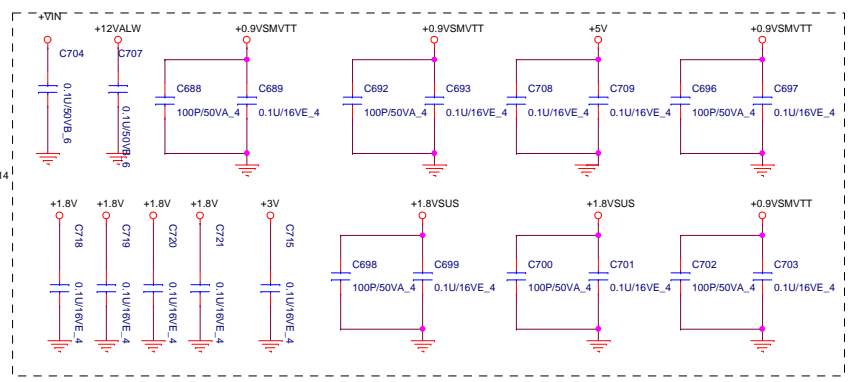
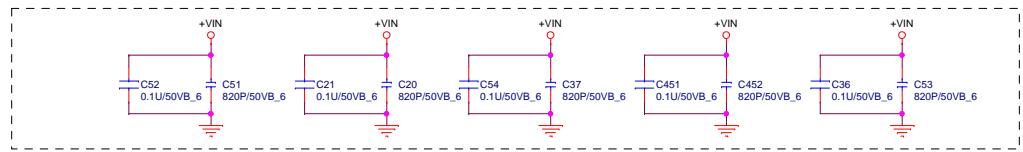
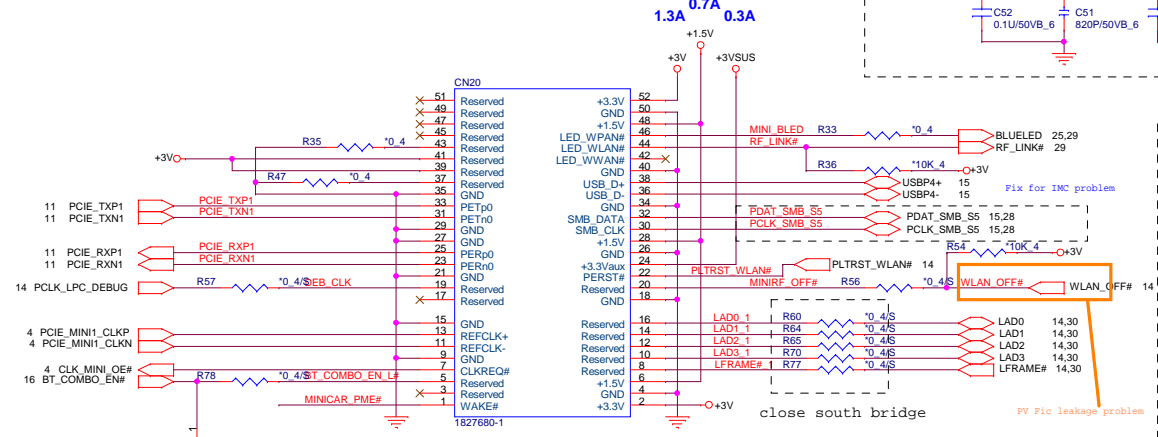
|                                  |                                    |                |
|----------------------------------|------------------------------------|----------------|
| Size B                           | Document Number<br>LED/KEYBOARD/SW | Rev 1A         |
| Date: Wednesday, August 27, 2008 |                                    | Sheet 29 of 41 |




+3VPCU 5,14,19,25,29,32,33,35,37,39  
 +5VSUS 19,25,32,33,38  
 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,31,33,34,38

+1.5V 28,32,37  
 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,33,34,38  
 +3VSUS 15,21,24,25,29,33,34,35,36,38  
 +VIN 19,32,33,34,35,36,38,39

### Mini PCI-E Card 1 WLAN

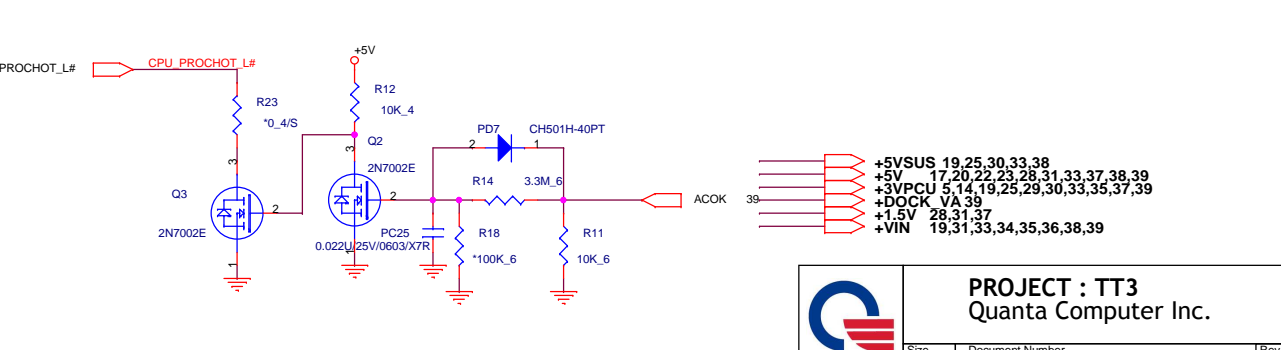
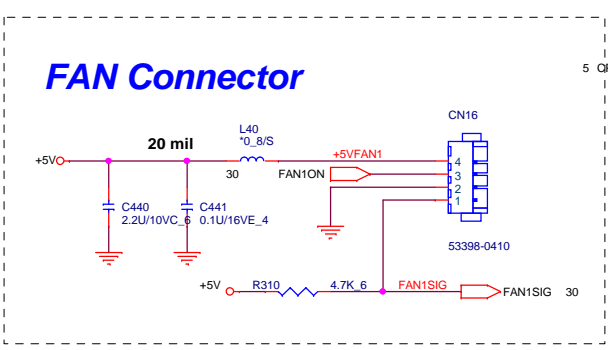
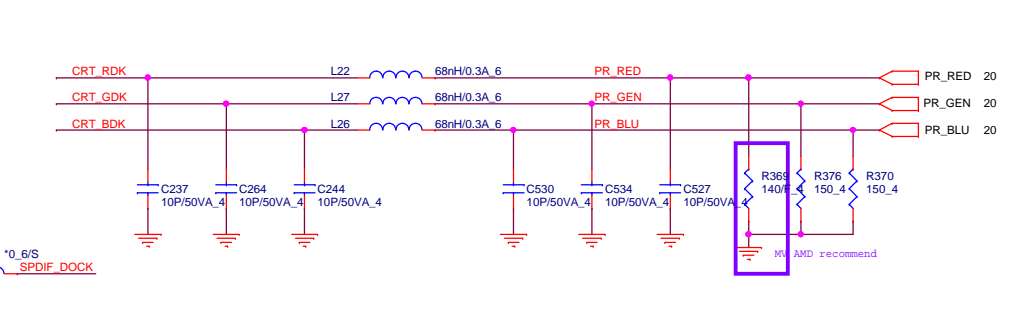
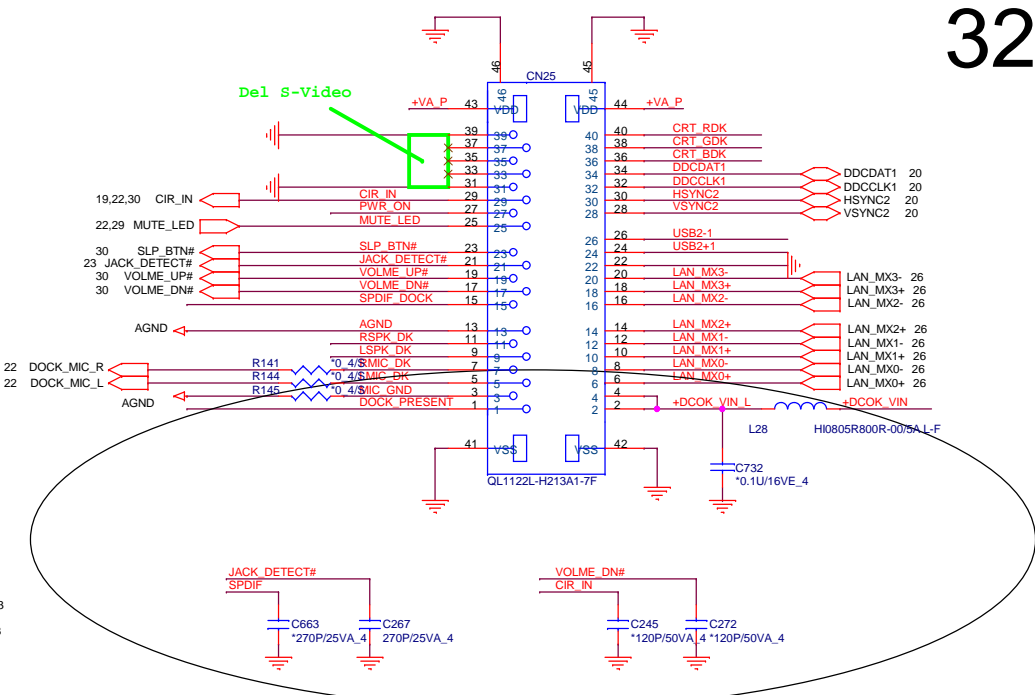
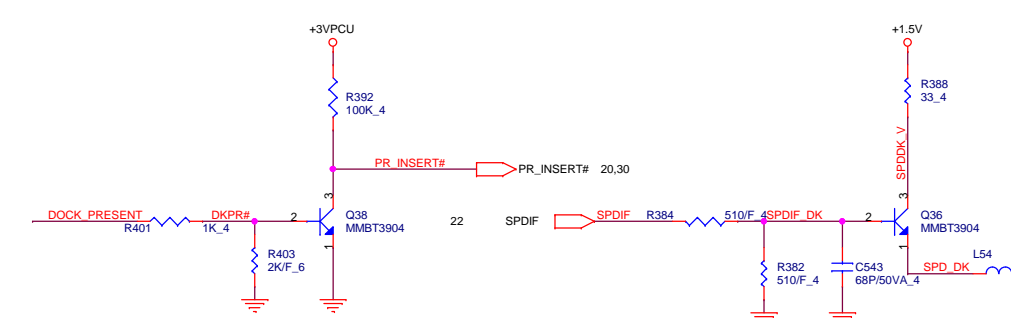
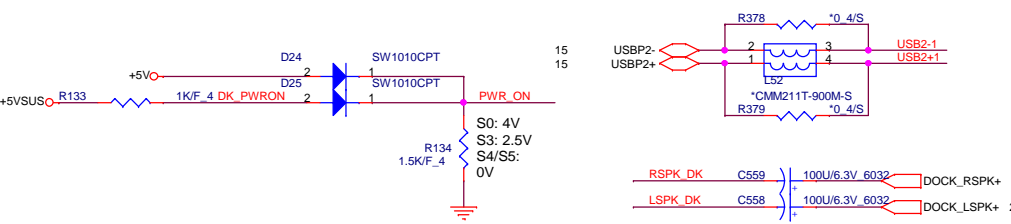
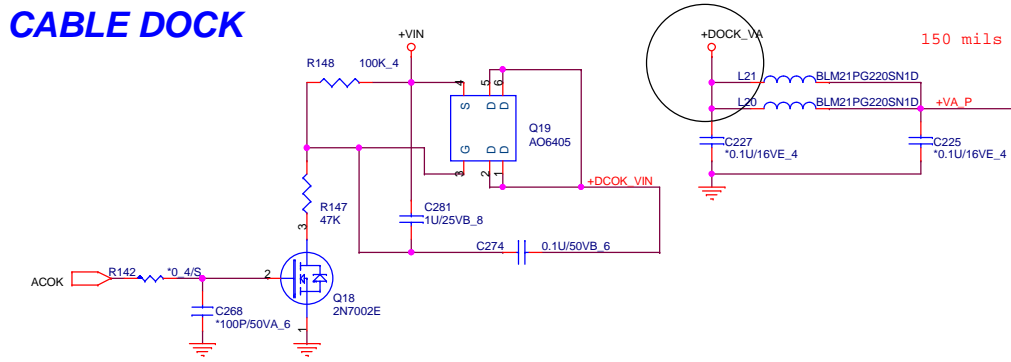




**PROJECT : TT3**  
Quanta Computer Inc.

|                                  |                                |                |
|----------------------------------|--------------------------------|----------------|
| Size Custom                      | Document Number Mini CARD/Hole | Rev 1A         |
| Date: Wednesday, August 27, 2008 |                                | Sheet 31 of 41 |

# CABLE DOCK

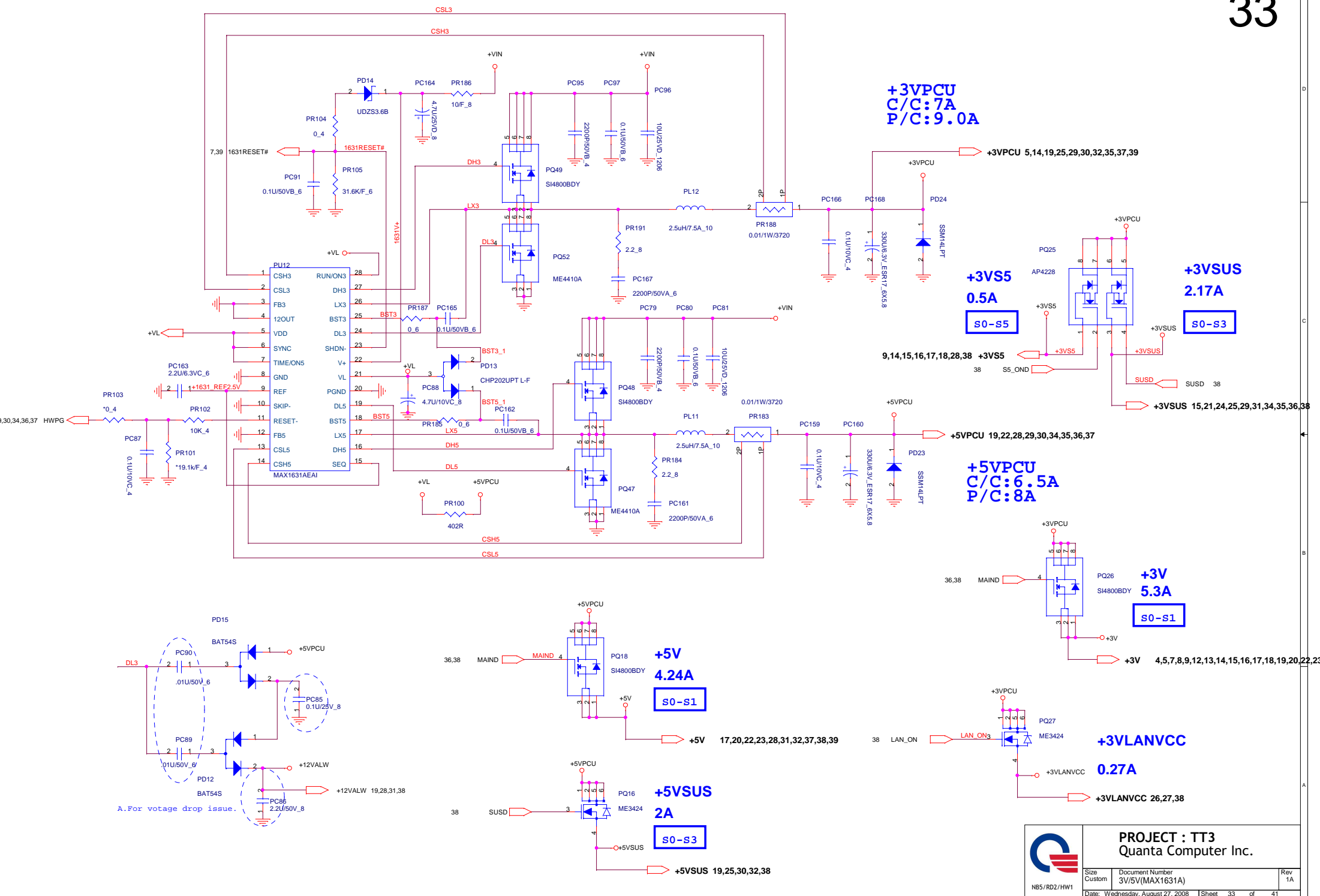


- +5VSUS 19,25,30,33,38
- +5V 17,20,22,23,28,31,33,37,38,39
- +3VPCU 5,14,19,25,29,30,33,35,37,39
- +DOCK\_VA 39
- +1.5V 28,31,37
- +VIN 19,31,33,34,35,36,38,39



**PROJECT : TT3**  
Quanta Computer Inc.

|   |                               |        |
|---|-------------------------------|--------|
| Size Custom                                     | Document Number CABLE DOCKING | Rev 1A |
| Date: Wednesday, August 27, 2008 Sheet 32 of 41 |                               |        |



**+3VPCU**  
C/C: 7A  
P/C: 9.0A

**+3VS5**  
0.5A  
S0-S5

**+3VSUS**  
2.17A  
S0-S3

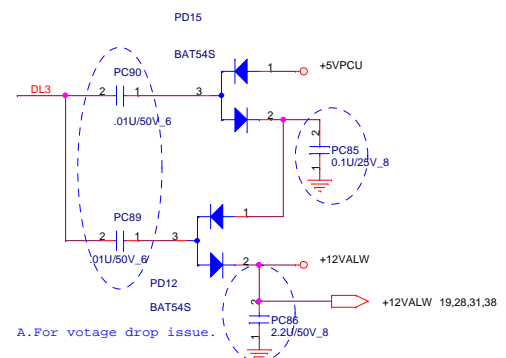
**+5VPCU**  
C/C: 6.5A  
P/C: 8A

**+5V**  
4.24A  
S0-S1


**+5VSUS**  
2A  
S0-S3

**+3V**  
5.3A  
S0-S1

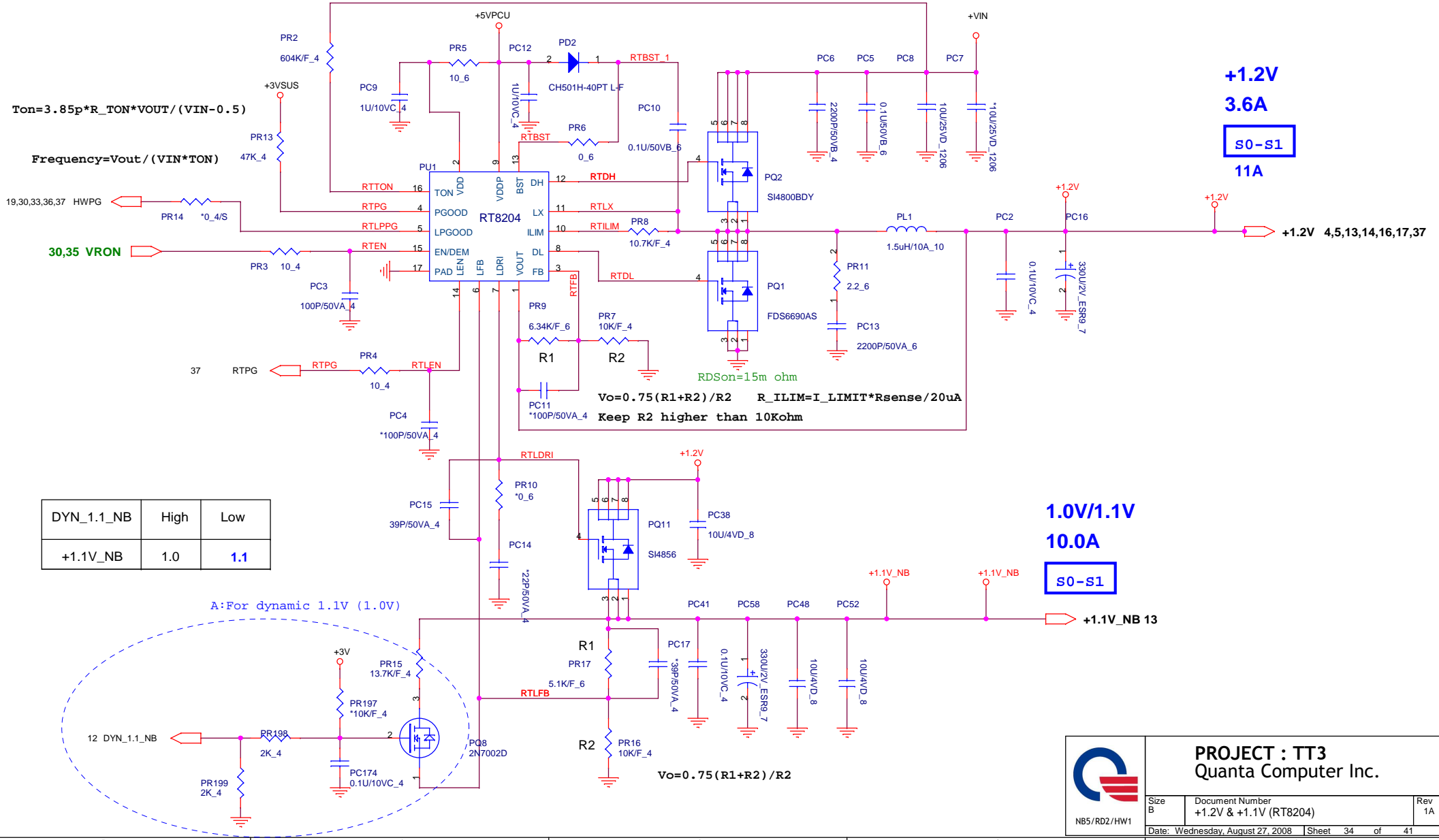
**+3VLANVCC**  
0.27A



A. Por voltage drop issue.

|   |                                    |                                  |   |        |
|---|------------------------------------|----------------------------------|---|--------|
|  |                                    |                                  | <b>PROJECT : TT3</b><br>Quantas Computer Inc. |        |
| Size Custom<br>NB5/RD2/HW1  | Document Number<br>3V/5V(MAX1631A) | Date: Wednesday, August 27, 2008 | Sheet 33 of 41                                | Rev 1A |





|            |      |     |
|------------|------|-----|
| DYN_1.1_NB | High | Low |
| +1.1V_NB   | 1.0  | 1.1 |

A: For dynamic 1.1V (1.0V)



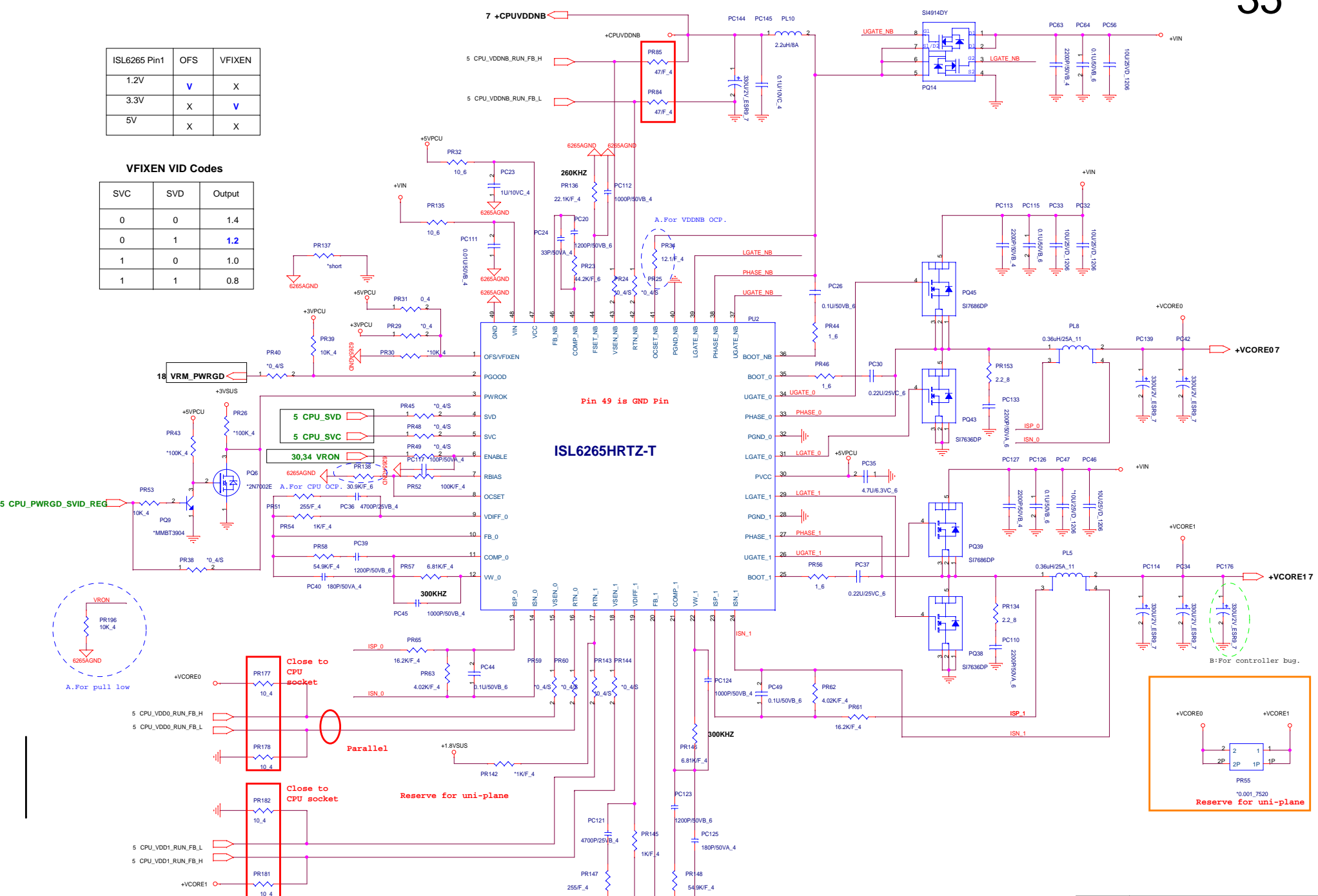
**PROJECT : TT3**  
Quanta Computer Inc.

|                                  |   |                |
|----------------------------------|---|----------------|
| Size B                           | Document Number<br>+1.2V & +1.1V (RT8204) | Rev 1A         |
| Date: Wednesday, August 27, 2008 |   | Sheet 34 of 41 |

| ISL6265 Pin1 | OFS | VFIXEN |
|--------------|-----|--------|
| 1.2V         | V   | X      |
| 3.3V         | X   | V      |
| 5V           | X   | X      |

VFIXEN VID Codes

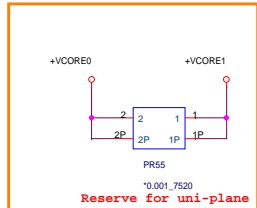
| SVC | SVD | Output |
|-----|-----|--------|
| 0   | 0   | 1.4    |
| 0   | 1   | 1.2    |
| 1   | 0   | 1.0    |
| 1   | 1   | 0.8    |

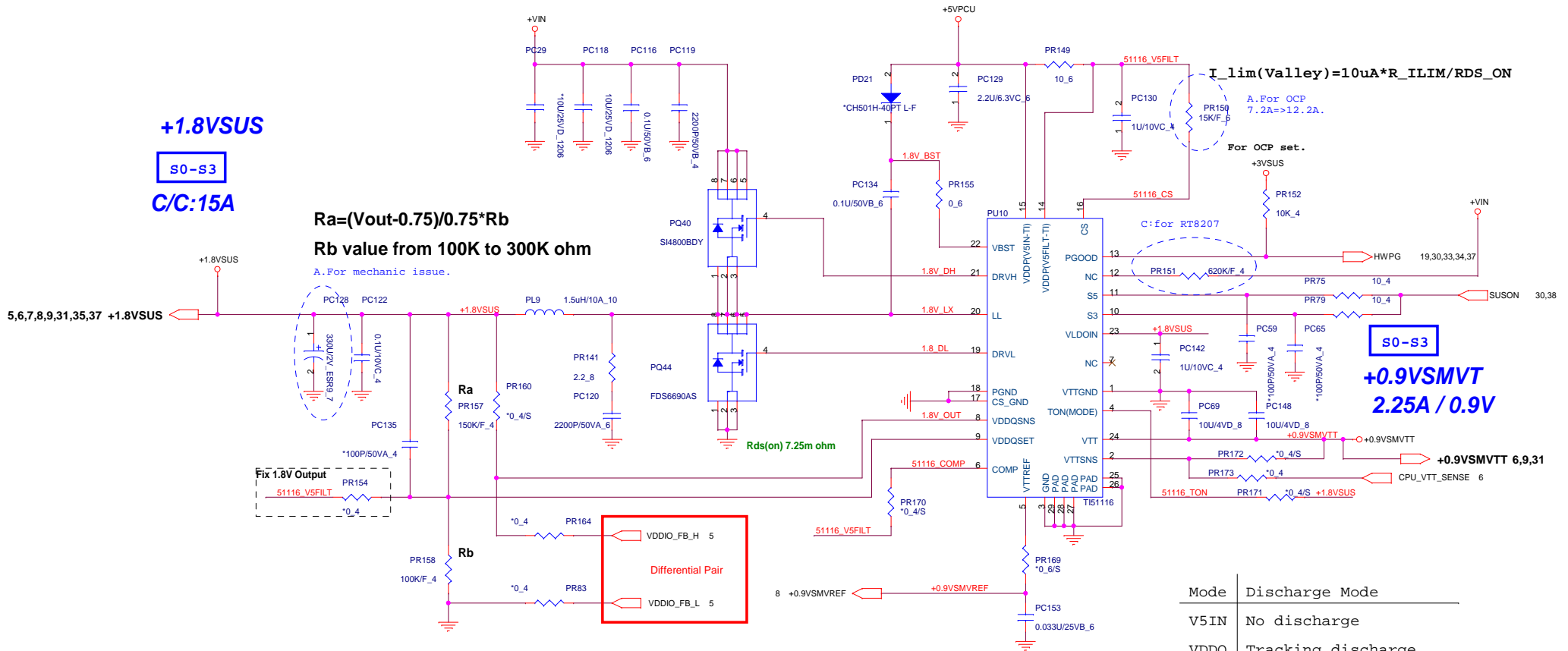


Pin 49 is GND Pin

ISL6265HRTZ-T

300KHZ





**+1.8VSUS**

**S0-S3**

**C/C:15A**

$Ra = (V_{out} - 0.75) / 0.75 * Rb$   
**Rb value from 100K to 300K ohm**

A. For mechanic issue.

5,6,7,8,9,31,35,37 +1.8VSUS

Fix 1.8V Output  
 PR154  
 51116\_V5FILT  
 \*0.4

VDDIO\_FB\_H 5  
 VDDIO\_FB\_L 5  
**Differential Pair**

Rds(on) 7.25m ohm

$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS\_ON}$

A. For OCP  
 7.2A => 12.2A.

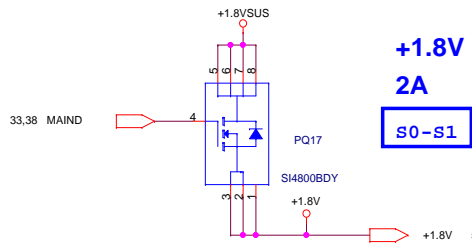
For OCP set.

C: for RT8207

**S0-S3**

**+0.9VSMVT**  
**2.25A / 0.9V**

+0.9VSMVTT 6,9,31



**+1.8V**

**2A**

**S0-S1**

|      |                        |
|------|------------------------|
| Mode | Discharge Mode         |
| V5IN | No discharge           |
| VDDQ | Tracking discharge     |
| Gnd  | Non-tracking discharge |

$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(\mu A)$

$I_{OCP} = V_{trip} / R_{ds\_on} + I_{Ripple} / 2$

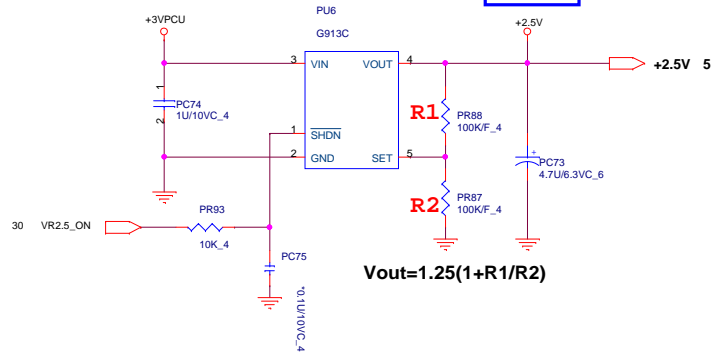
| VDDQSET | VDDQ(V)    | VTTREF and Vtt | Note               |
|---------|------------|----------------|--------------------|
| GND     | 2.5        | $V_{vddqsn}/2$ | DDR                |
| V5IN    | 1.8        | $V_{vddqsn}/2$ | DDR2               |
| FB      | adjustable | $V_{VDDQSN}/2$ | $1.5V < VDDQ < 3V$ |

**PROJECT : TT3**  
**Quanta Computer Inc.**

|                                  |   |        |
|----------------------------------|---|--------|
| Size Custom                      | Document Number 1.8VSUS/DDR_VTER/+1.8V/2.5V | Rev 1A |
| Date: Wednesday, August 27, 2008 | Sheet 36 of 41                              |        |

**+2.5V**  
**0.25A**

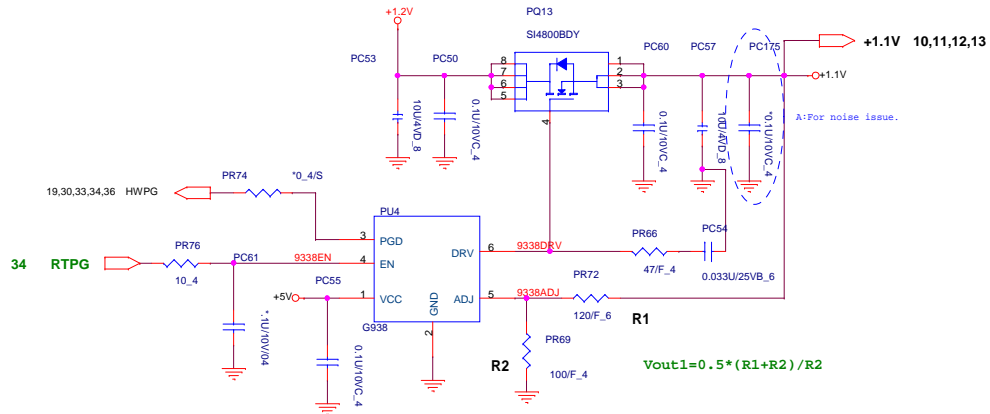
**S0-S1**



$V_{out} = 1.25(1 + R1/R2)$

**+1.1V**  
**2.A**

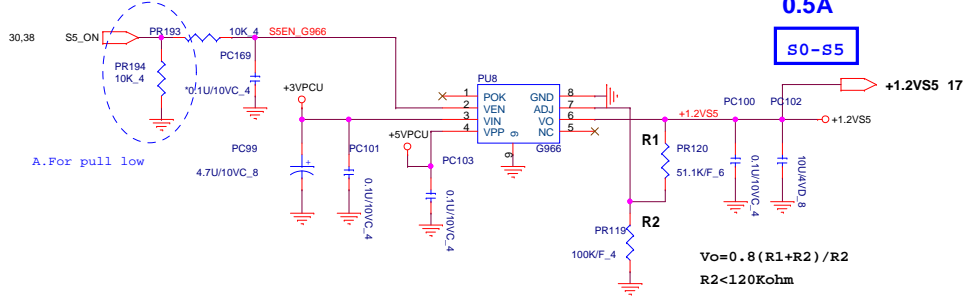
**S0-S1**



$V_{out} = 0.5 * (R1 + R2) / R2$

**+1.2VS5**  
**0.5A**

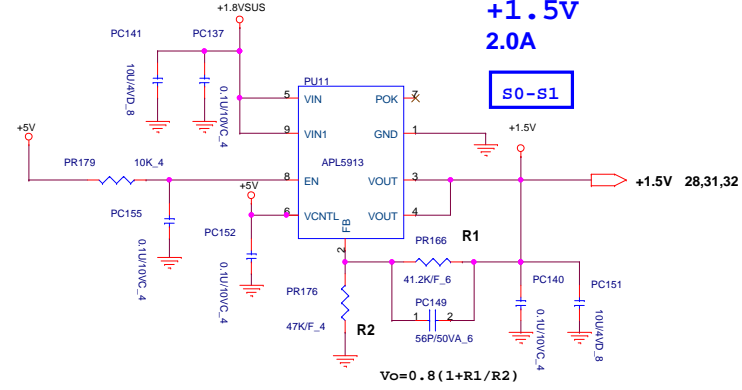
**S0-S5**



$V_o = 0.8 (R1 + R2) / R2$   
 $R2 < 120Kohm$

**+1.5V**  
**2.0A**

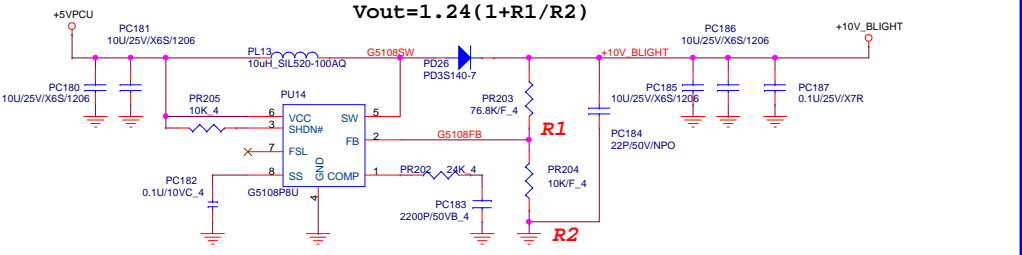
**S0-S1**



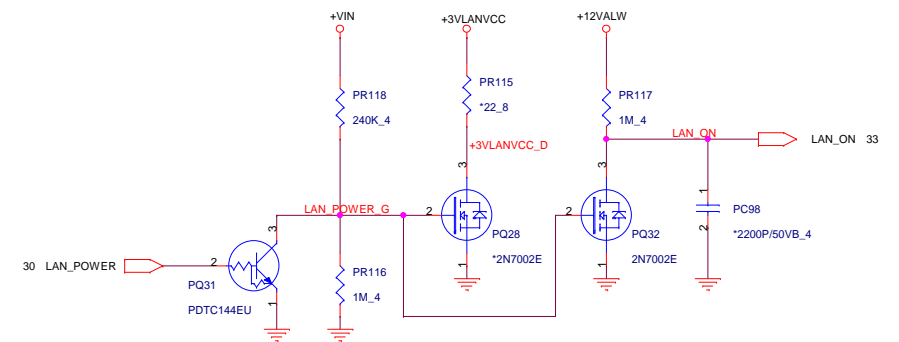
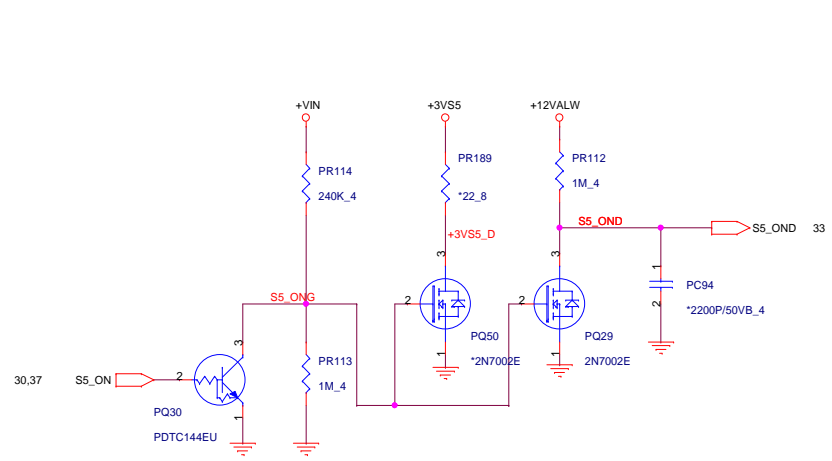
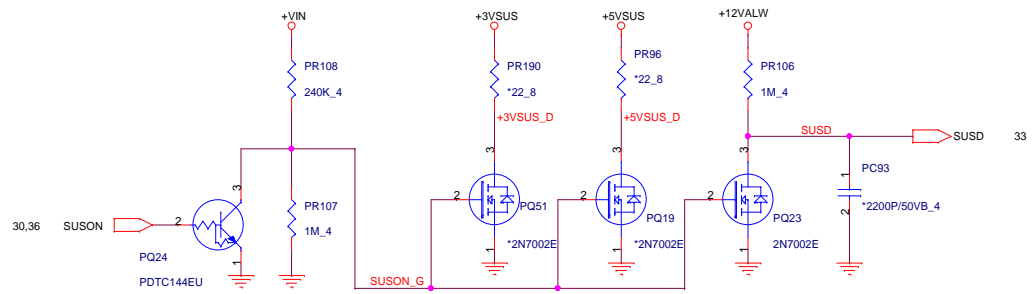
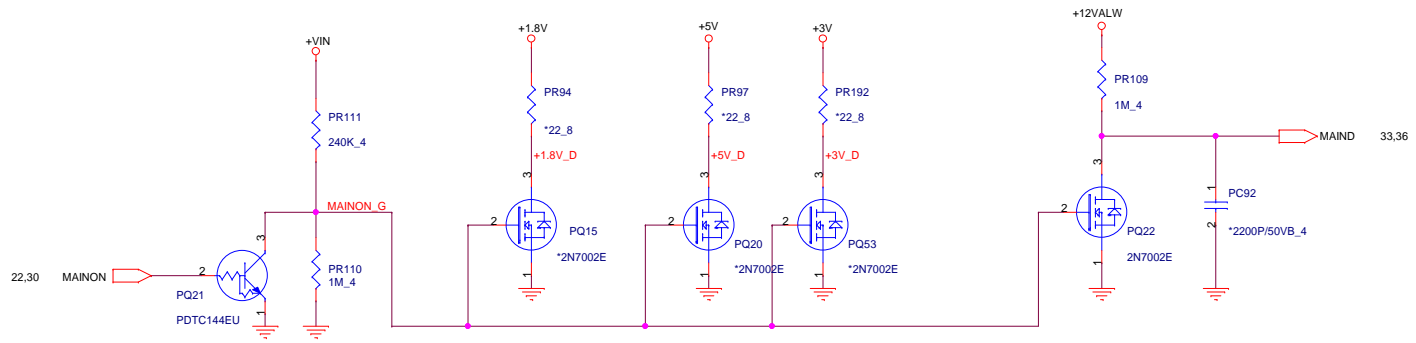
$V_o = 0.8 (1 + R1/R2)$


**Boost 10V**

$V_{out} = 1.24(1 + R1/R2)$

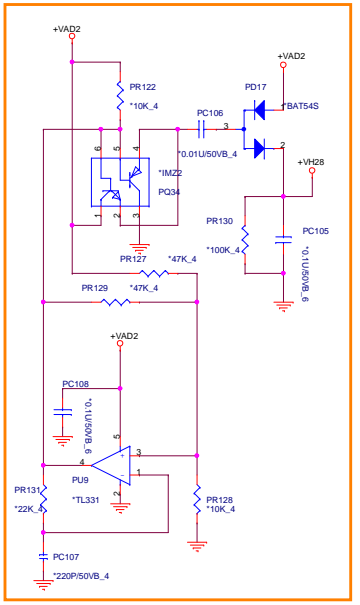
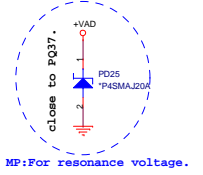
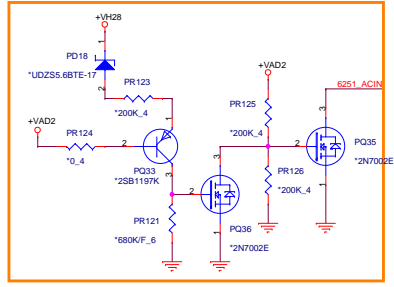
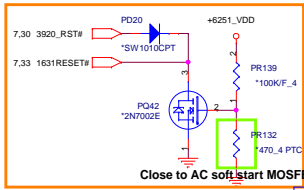
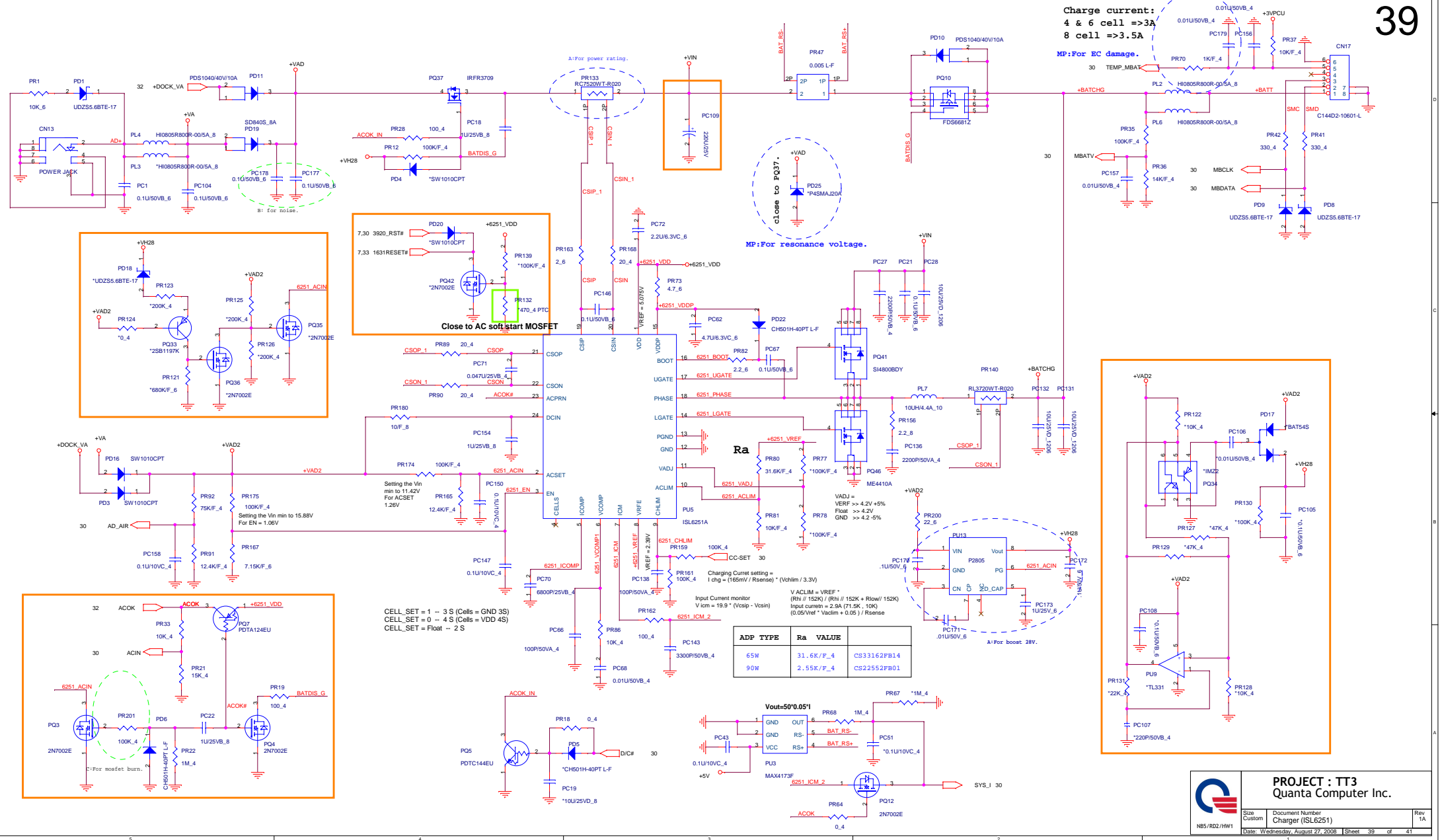


|             |  |  |  |
|-------------|--|--|--|
|             |  | <b>PROJECT : TT3</b><br>Quanta Computer Inc. |  |
|             |  | Size Custom                                  | Document Number<br>+1.2V_S5+1.5V+1.1V+2.5V |
| NBS/RD2/HW1 |  | Date: Wednesday, August 27, 2008             | Sheet 37 of 41                             |



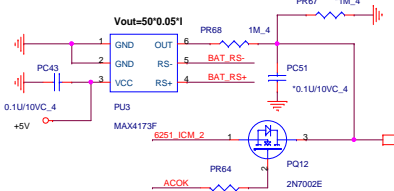
|  |   |                              |           |
|--|---|------------------------------|-----------|
| <br>NB5/RD2/HW1 | <b>PROJECT : TT3</b><br>Quanta Computer Inc.    |                              |           |
|  | Size<br>Custom                                  | Document Number<br>DISCHARGE | Rev<br>1A |
|  | Date: Wednesday, August 27, 2008 Sheet 38 of 41 |                              |           |

Charge current =  
4 & 6 cell =>3A  
8 cell =>3.5A  
MP: For EC damage.



CELL\_SET = 1 -- 3 S (Cells = GND 3S)  
CELL\_SET = 0 -- 4 S (Cells = VDD 4S)  
CELL\_SET = Float -- 2 S

| ADP TYPE | Ra VALUE              |
|----------|-----------------------|
| 65W      | 31.6K/F_4 CS33162FB14 |
| 90W      | 2.55K/F_4 CS2552FB01  |



**PROJECT : TT3**  
**Quanta Computer Inc.**

|                                  |                   |        |
|----------------------------------|-------------------|--------|
| Size Custom                      | Document Number   | Rev 1A |
| NBS/RD/HW1                       | Charger (ISL6251) |        |
| Date: Wednesday, August 27, 2008 | Sheet 39          | of 41  |