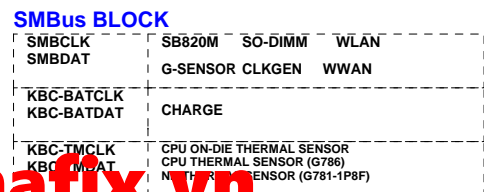


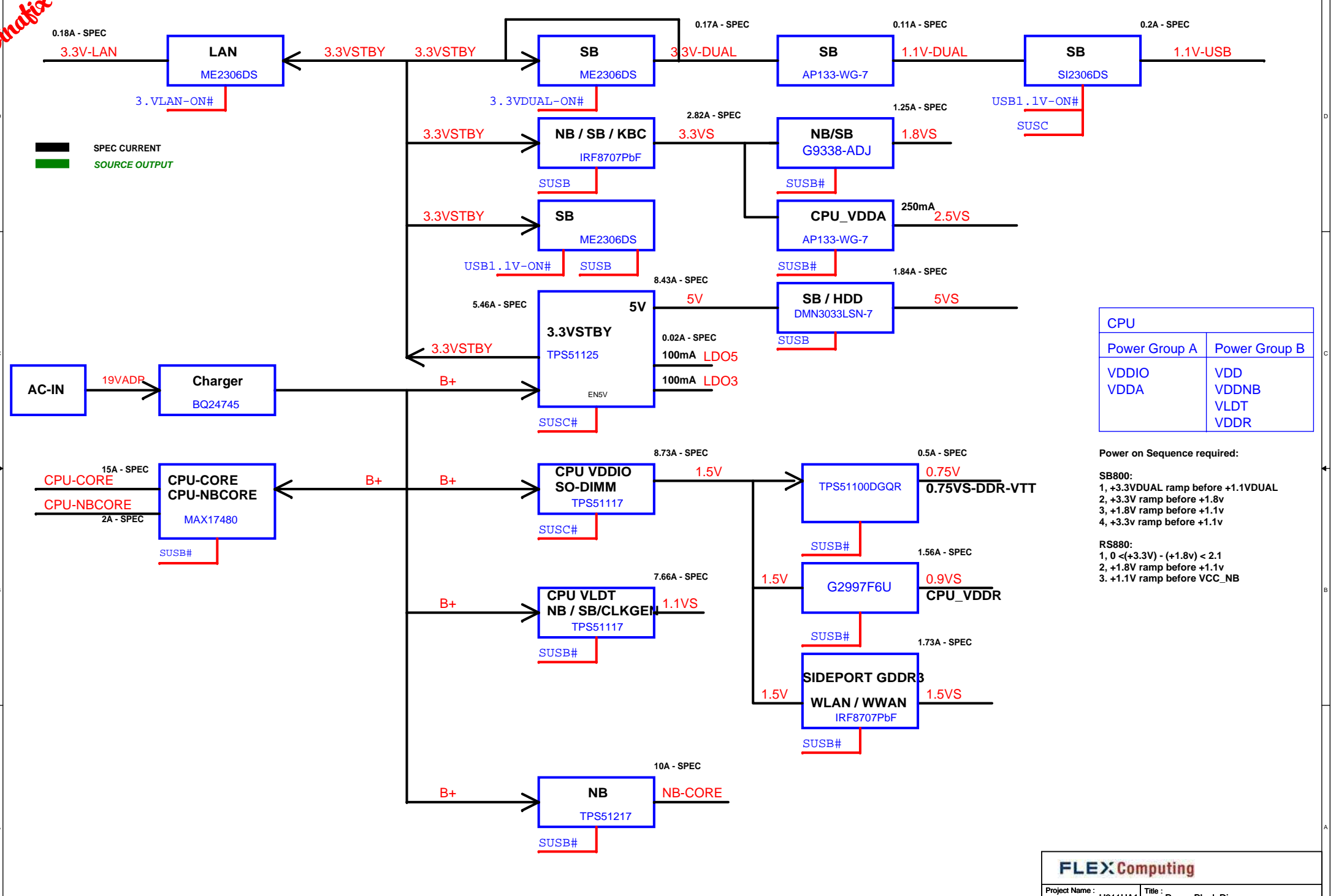
HT power supply is 1.10V
16x16 HT Link
12W: 1.0 GMz HT1
15W: 1.6 GHz HT3

LED STATUS		
(1) TP (Dual Color)	white : On amber : Off	M/B P.25
(1) RF (Dual Color)	white : enable amber : disable	USB D/B
(2) Power on	white : Power on blink white : Standby	P.22
(1) Battery Charging	amber	LED D/B
(2) Dual color HDD	white : Active amber : Park	P.22
(1) Num Lock	white	KB
(2) Mute LED	amber	
(3) Caps Lock	white	P.25



ARWEN 2.0 UA
 HPMH-40GAB5100-D*00 - PWA M/B 1.7G Athlon 1M L2 K125
 HPMH-40GAB5100-D*10 - PWA M/B 1.3G Athlon*2 2M L2 K325
 HPMH-40GAB5100-D*20 - PWA M/B 1.5G Turion*2 2ML2 K625

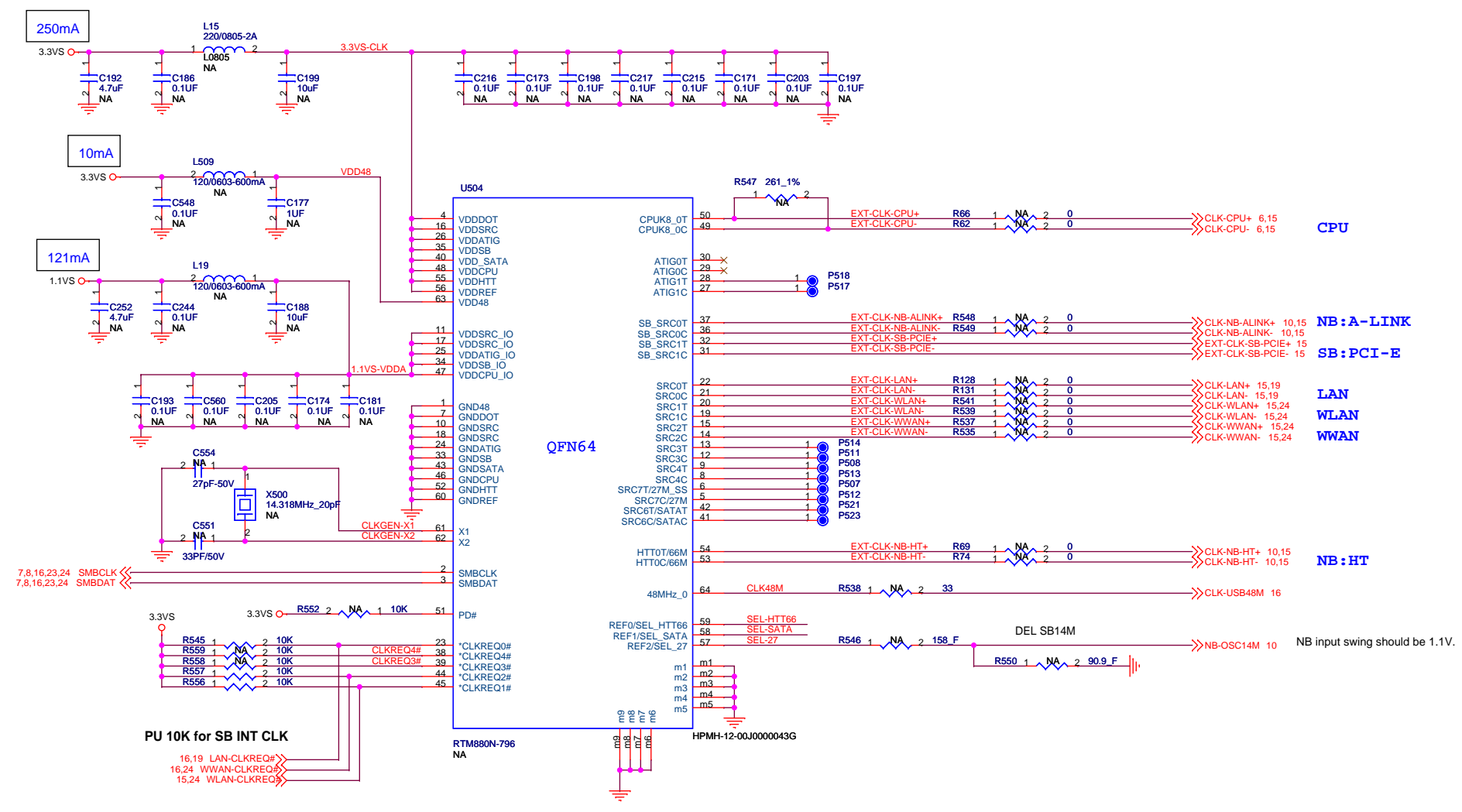
vinafix



H310-UA Power Block Diagram

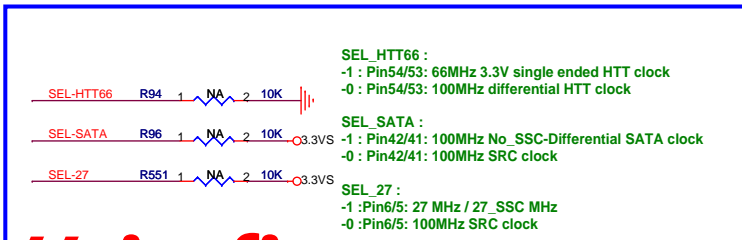
<http://vinafix.vn>

CLOCK GENERATOR



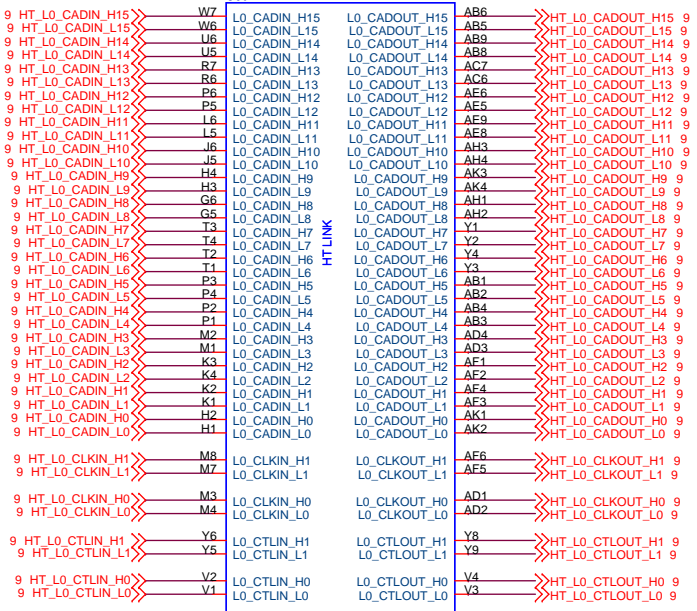
PU 10K for SB INT CLK
 16,19 LAN-CLKREQ#
 16,24 WWAN-CLKREQ#
 15,24 WLAN-CLKREQ#

CLKREQ#	DEVICE
CLKREQ0#	LAN
CLKREQ1#	WLAN
CLKREQ2#	WWAN
CLKREQ3#	NA
CLKREQ4#	NA



VLDT Trace at Itast 200 mils wide

Vicm(DC)=600 mV

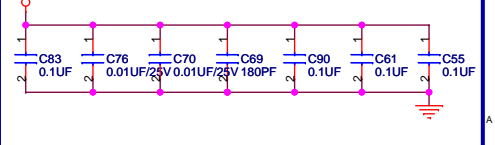
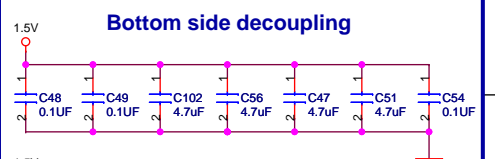
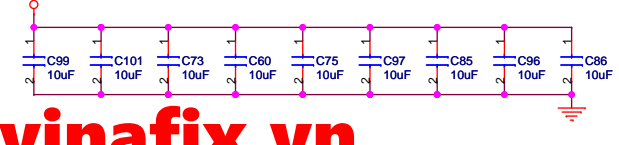
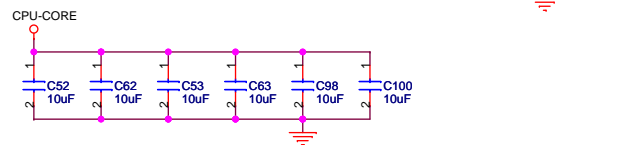
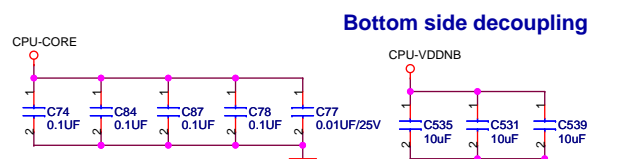
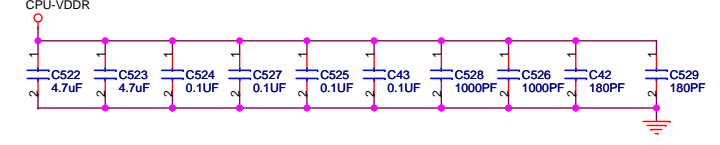
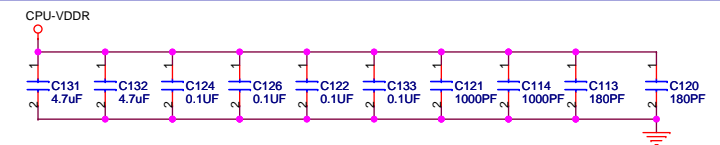
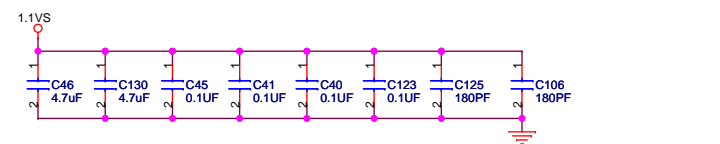


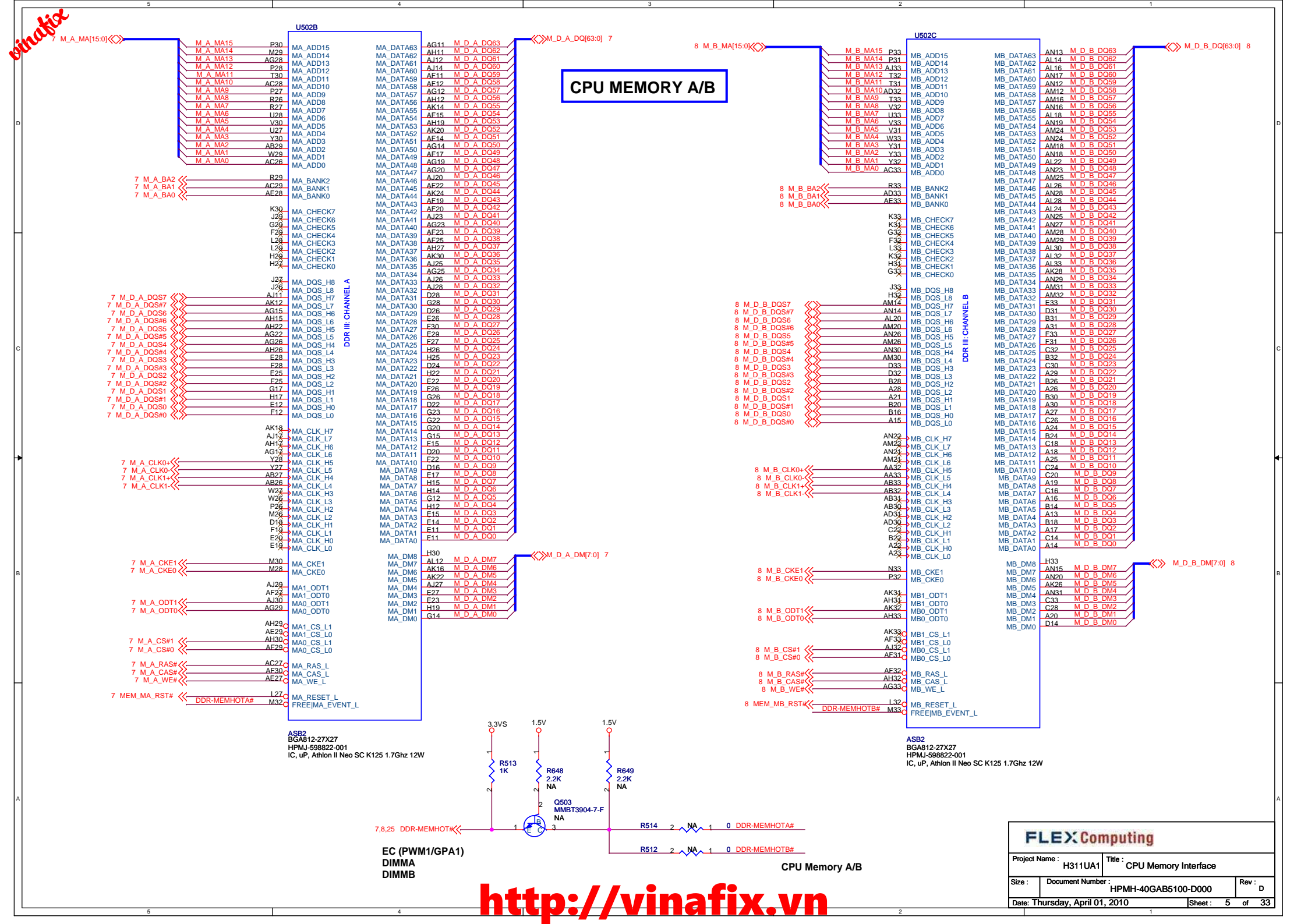
ASB2
BGAB12-27X27
HPMJ-598822-001
IC, uP, Athlon II Neo SC K125 1.7Ghz 12W

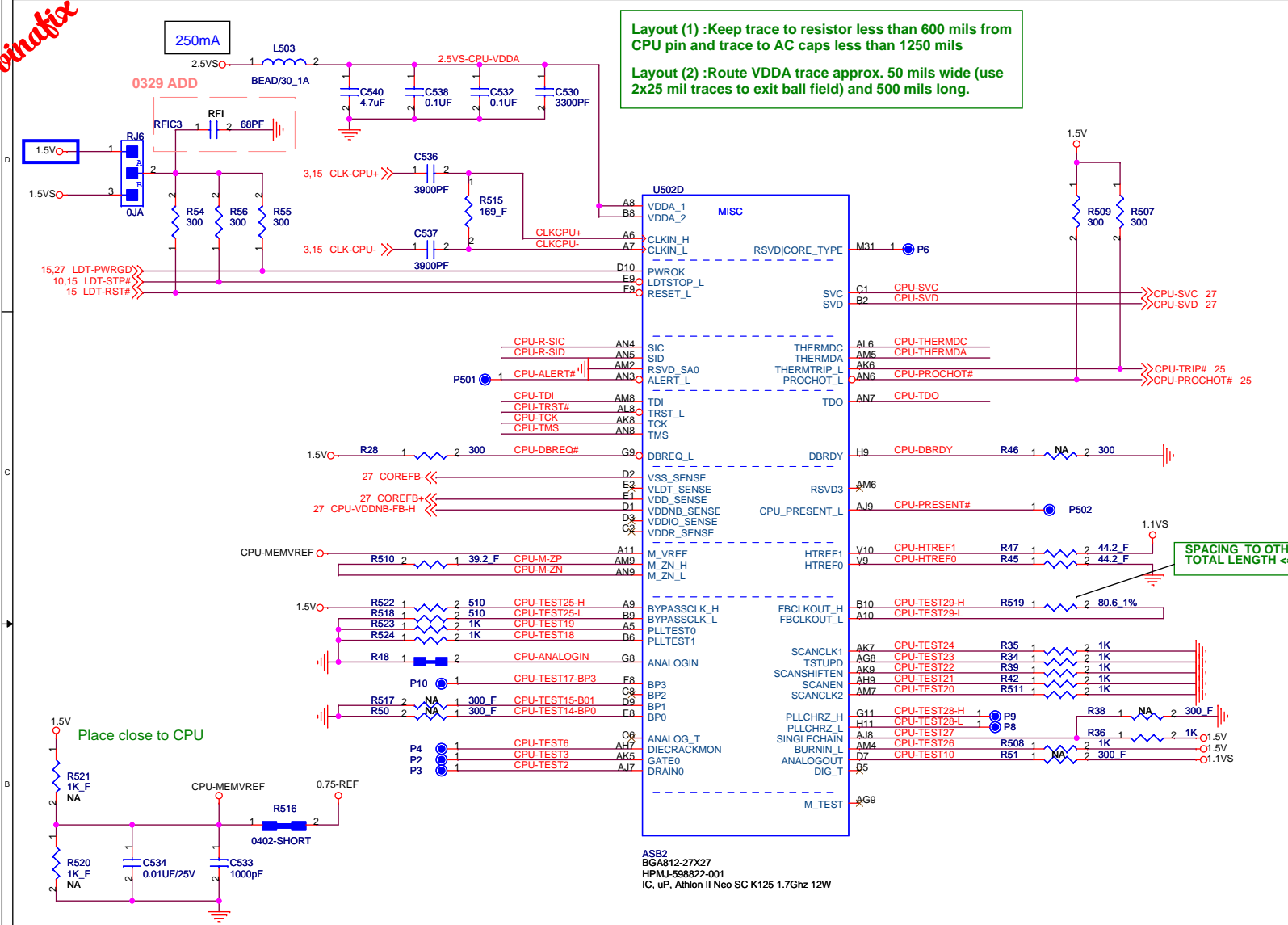
ASB2
BGAB12-27X27
HPMJ-598822-001
IC, uP, Athlon II Neo SC K125 1.7Ghz 12W

ASB2
BGAB12-27X27
HPMJ-598822-001
IC, uP, Athlon II Neo SC K125 1.7Ghz 12W

ASB2
BGAB12-27X27
HPMJ-598822-001
IC, uP, Athlon II Neo SC K125 1.7Ghz 12W





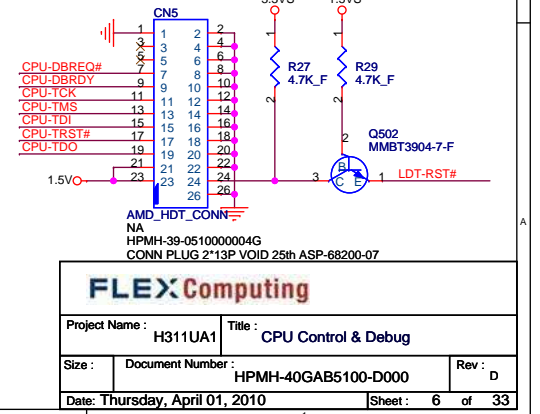
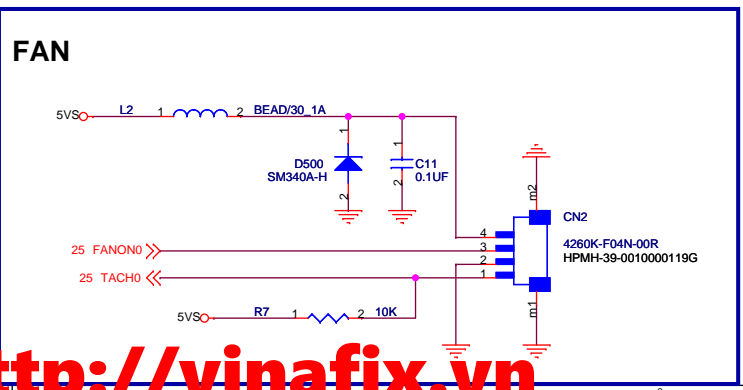
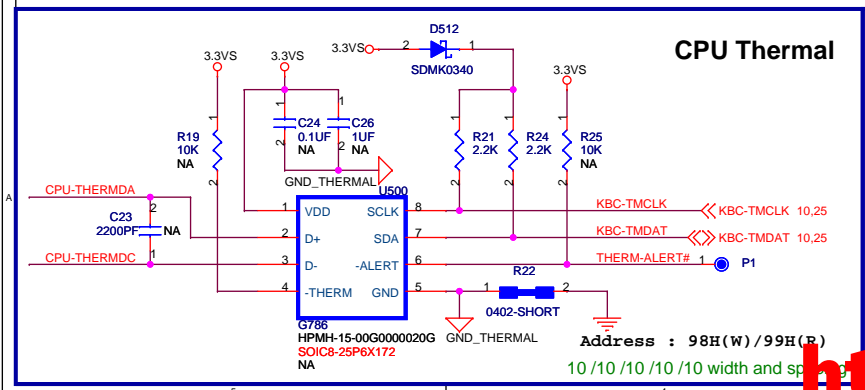


Layout (1) :Keep trace to resistor less than 600 mils from CPU pin and trace to AC caps less than 1250 mils
Layout (2) :Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

**SPACING TO OTHER >=0.3MM
TOTAL LENGTH <= 38.1MM**

9CH(W)/9DH(R)

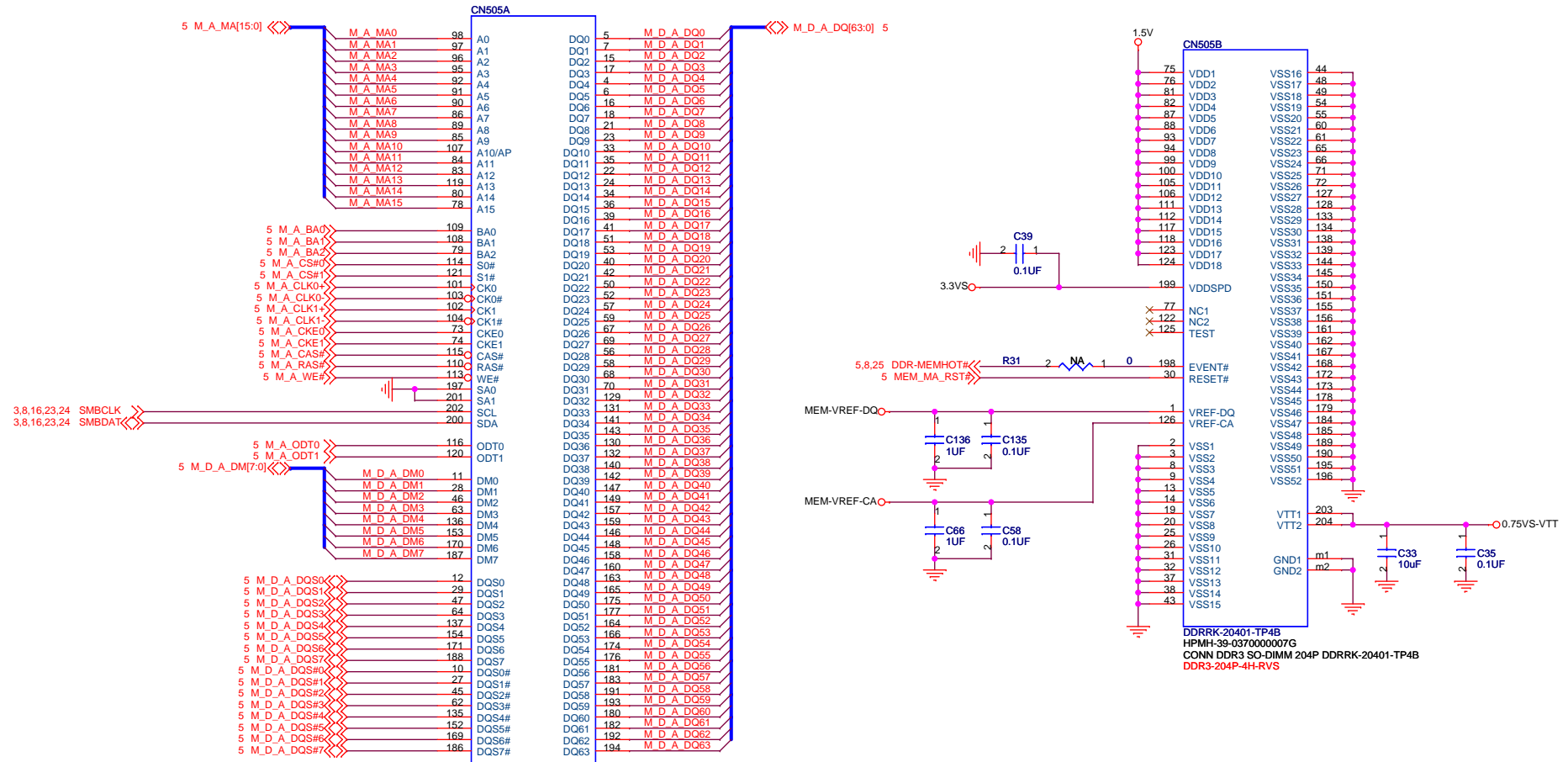
HDT Header



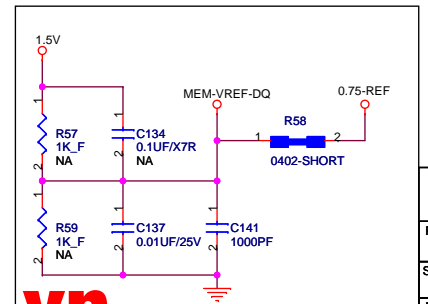
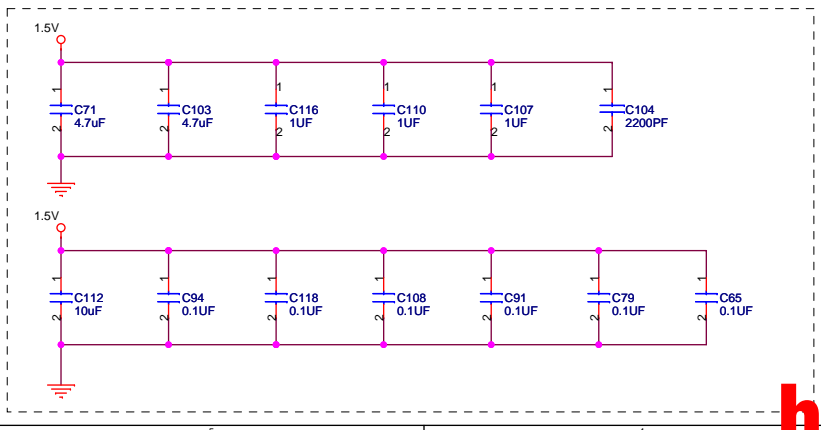
FLEX Computing	
Project Name : H311UA1	Title : CPU Control & Debug
Size :	Document Number : HPMH-40GAB5100-D000
Date : Thursday, April 01, 2010	Rev : D
Sheet : 6 of 33	

Memory Channel A

vinafix



Layout :
Place these Caps near So-DimmA



FLEX Computing

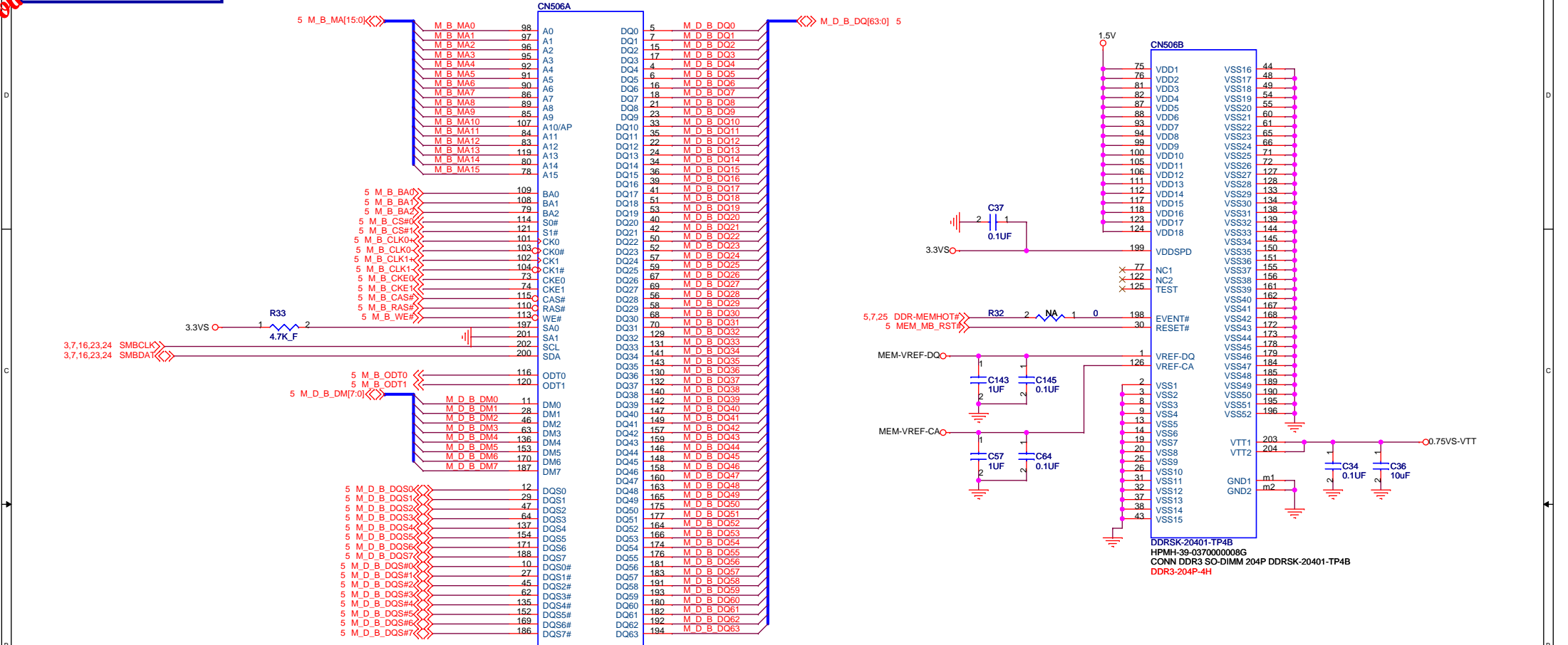
Project Name : H311UA1 Title : Memory Channel A

Size : Document Number : HPMH-40GAB5100-D000 Rev : D

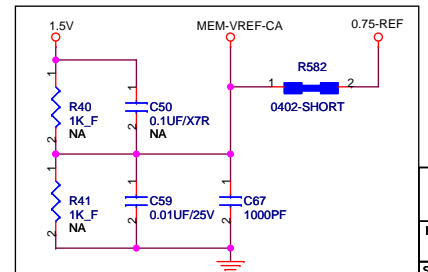
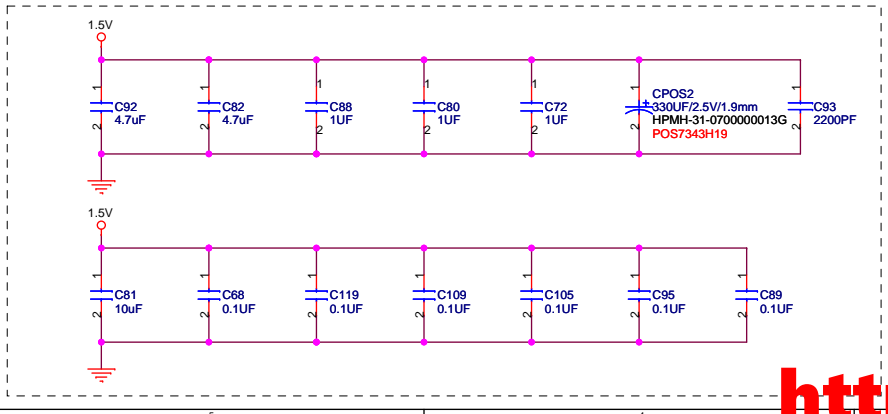
Date : Thursday, April 01, 2010 Sheet : 7 of 33

http://vinafix.vn

Memory Channel B

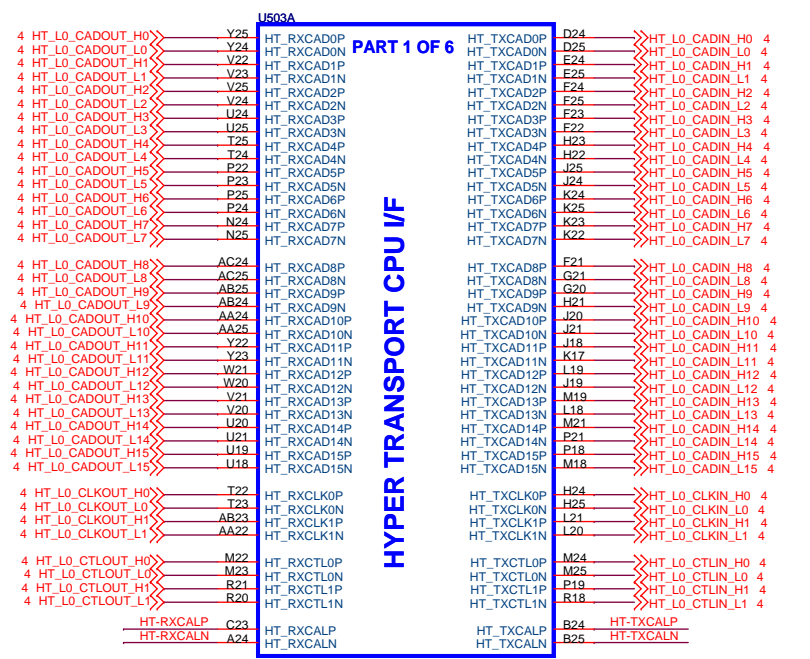


Layout :
Place these Caps near So-DimmA

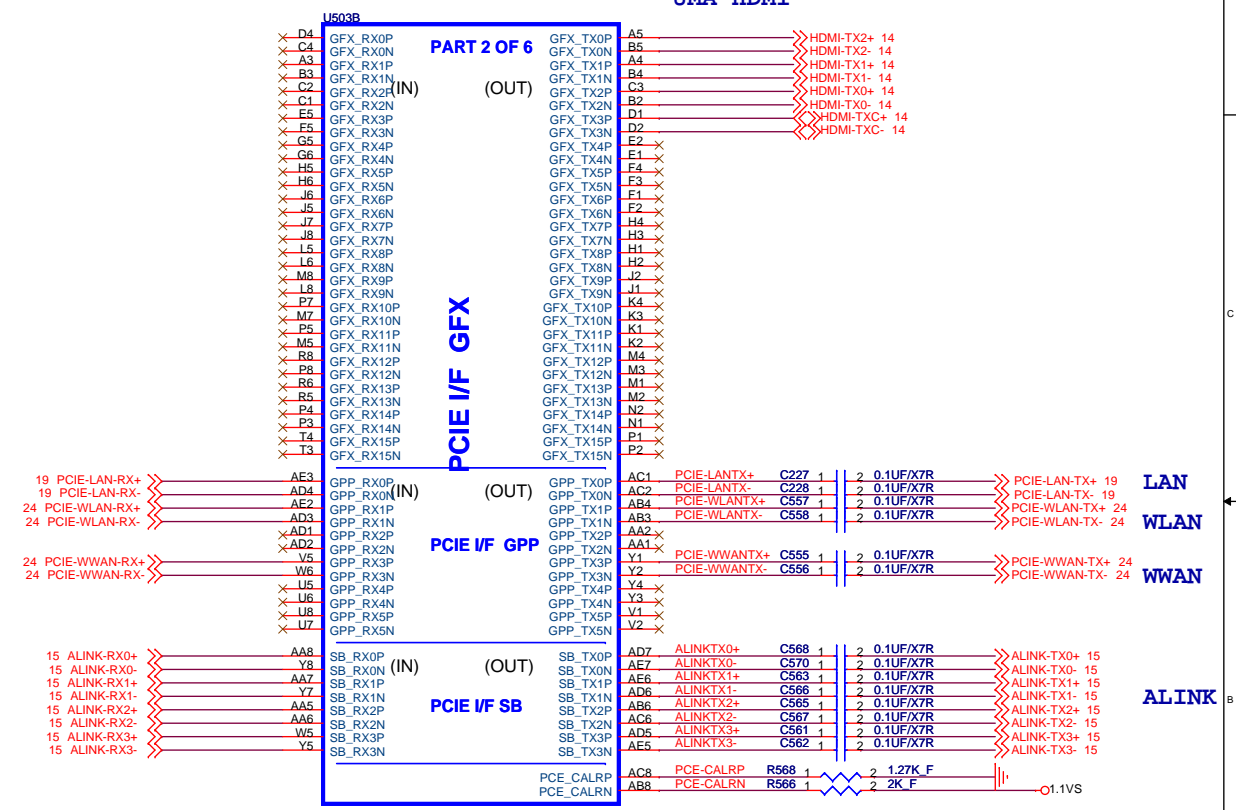
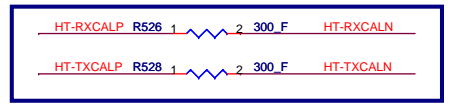


<http://vinafix.vn> place near SO-DIMM socket

vinafix.vn



RS880M HPMJ-534109-001 FCBGA528-RS780M 301 ohm to 300 ohm



RS880M HPMJ-534109-001 FCBGA528-RS780M

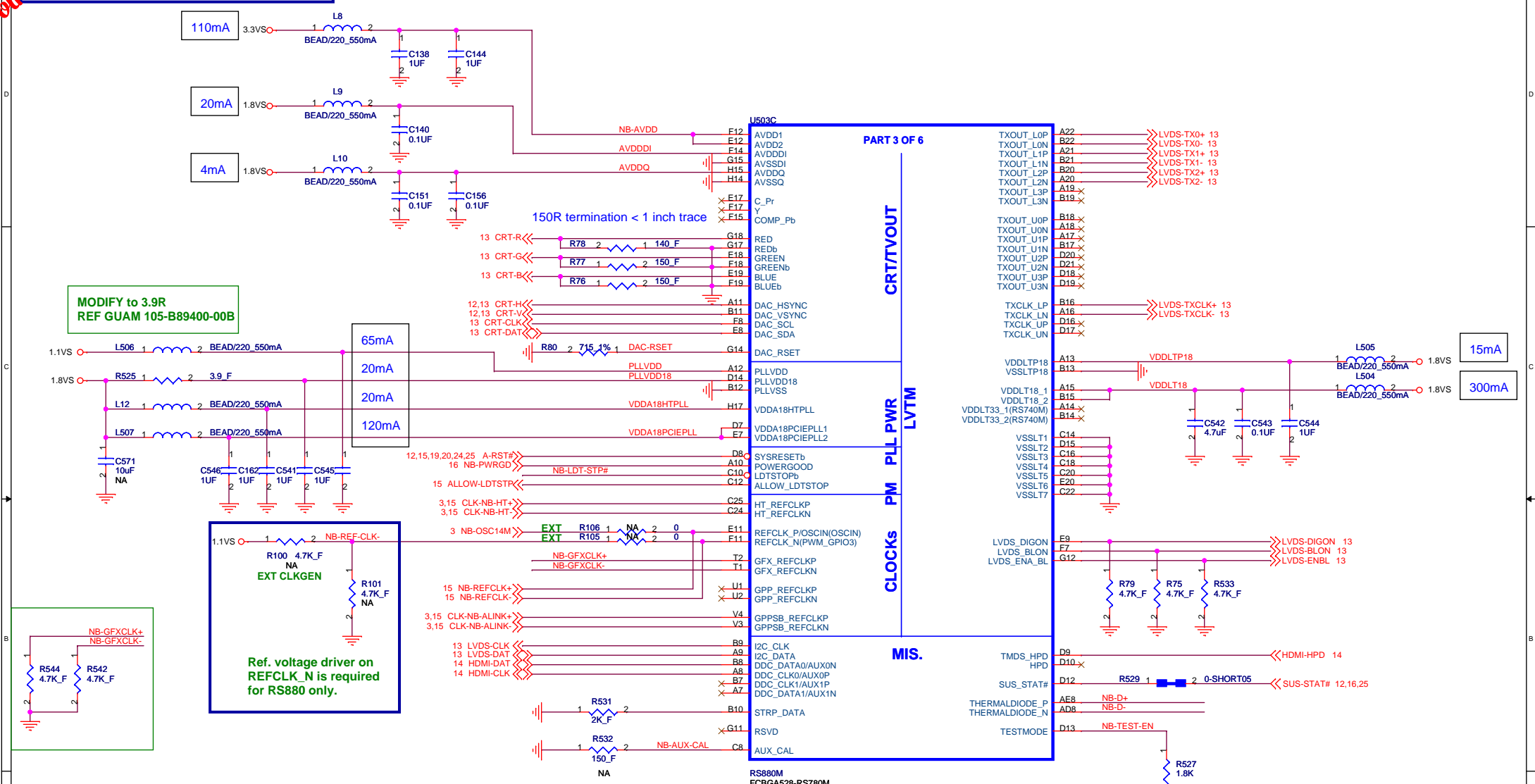
FLEX Computing

Project Name : H311UA1 Title : RS880M HT/PCIE/HDMI Interface

Size : Custom Document Number : HPMH-40GABS100-D000 Rev : D

Date : Thursday, April 01, 2010 Sheet : 9 of 33

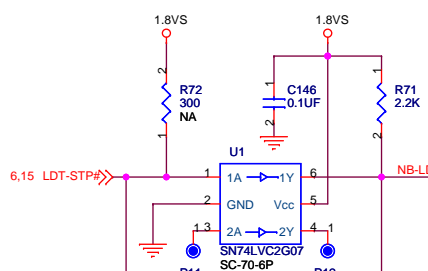
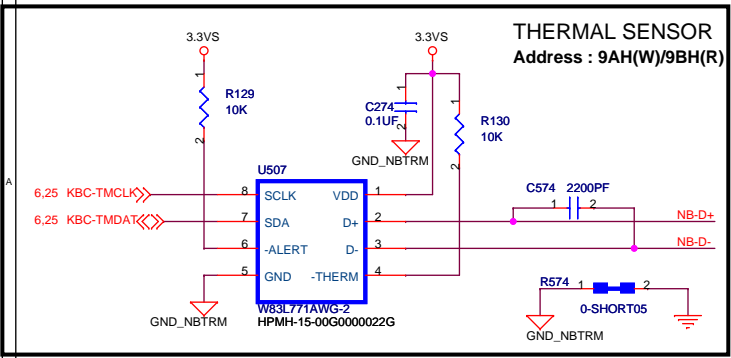
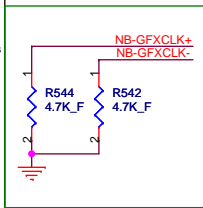
RS880M CRT/LVDS/SYSTEM I/F



MODIFY to 3.9R
REF GUAM 105-B89400-00B

EXT CLKGEN
R100 4.7K_F
R101 4.7K_F
NA
NA

Ref. voltage driver on REFCLK_N is required for RS880 only.



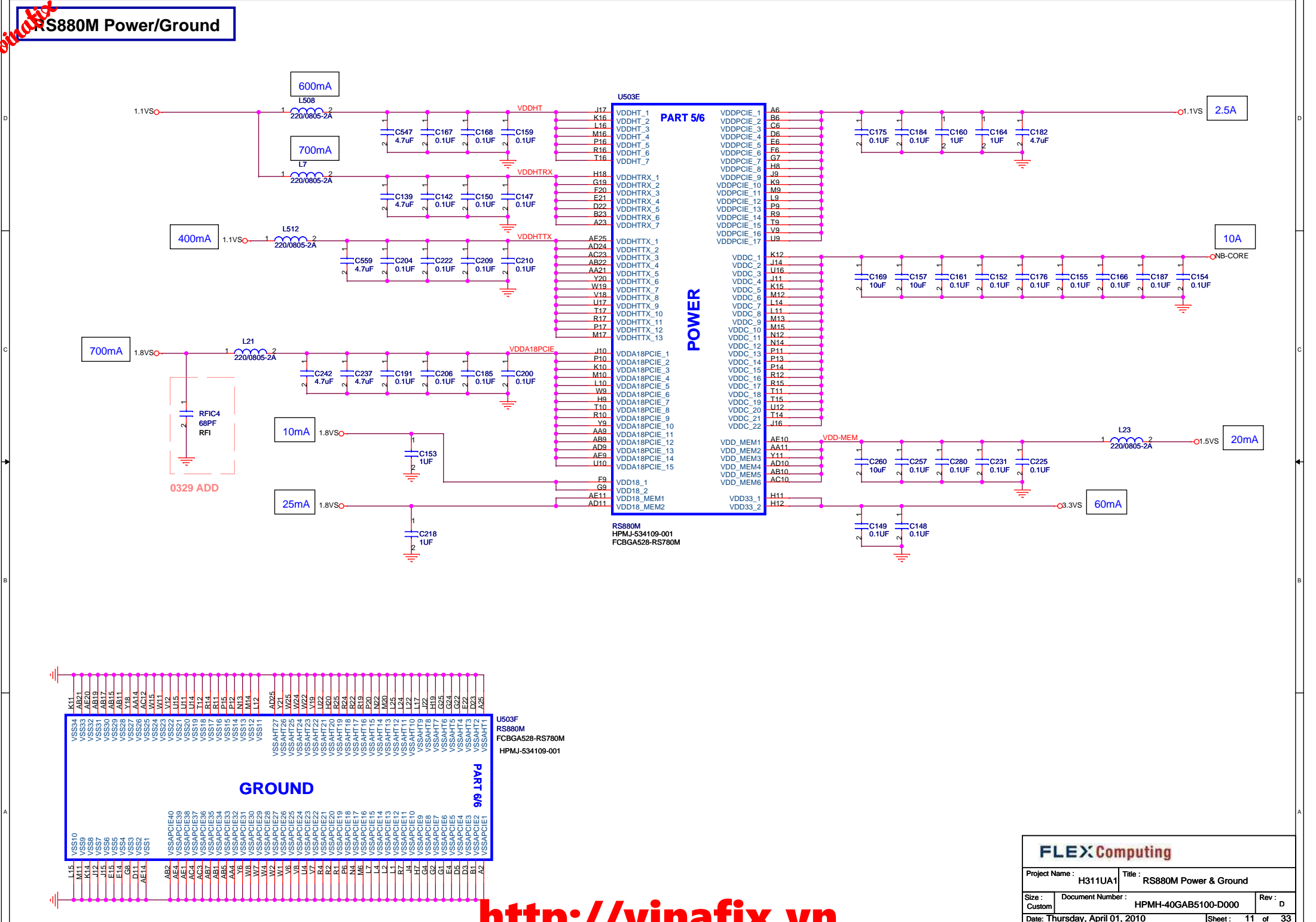
When processor observes LDTSTOP# asserti on more than 40ns after its HyperTransport neighbor(s), it may fail to disable the receivers within the allocated times. this may cause a training failure when LDTSTOP# is deasserted.

FLEX Computing

Project Name : H311UA1 Title : RS880M Video Interface

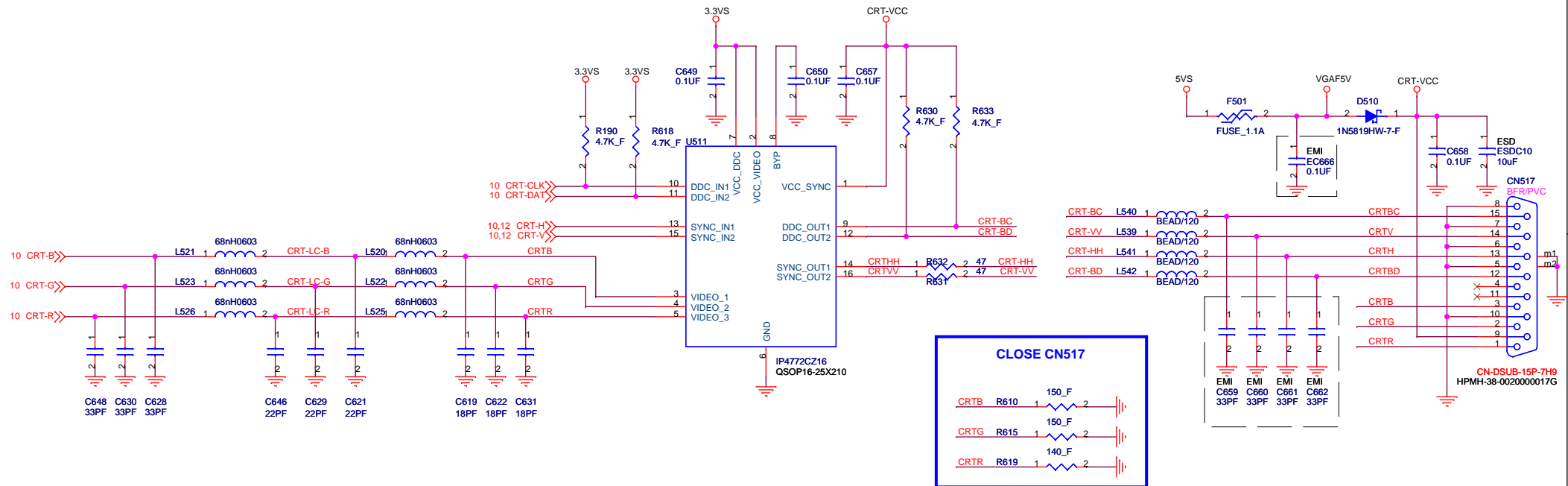
Size : Custom Document Number : HPMH-40GAB5100-D000 Rev : D

Date: Thursday, April 01, 2010 Sheet: 10 of 33



FLEX Computing

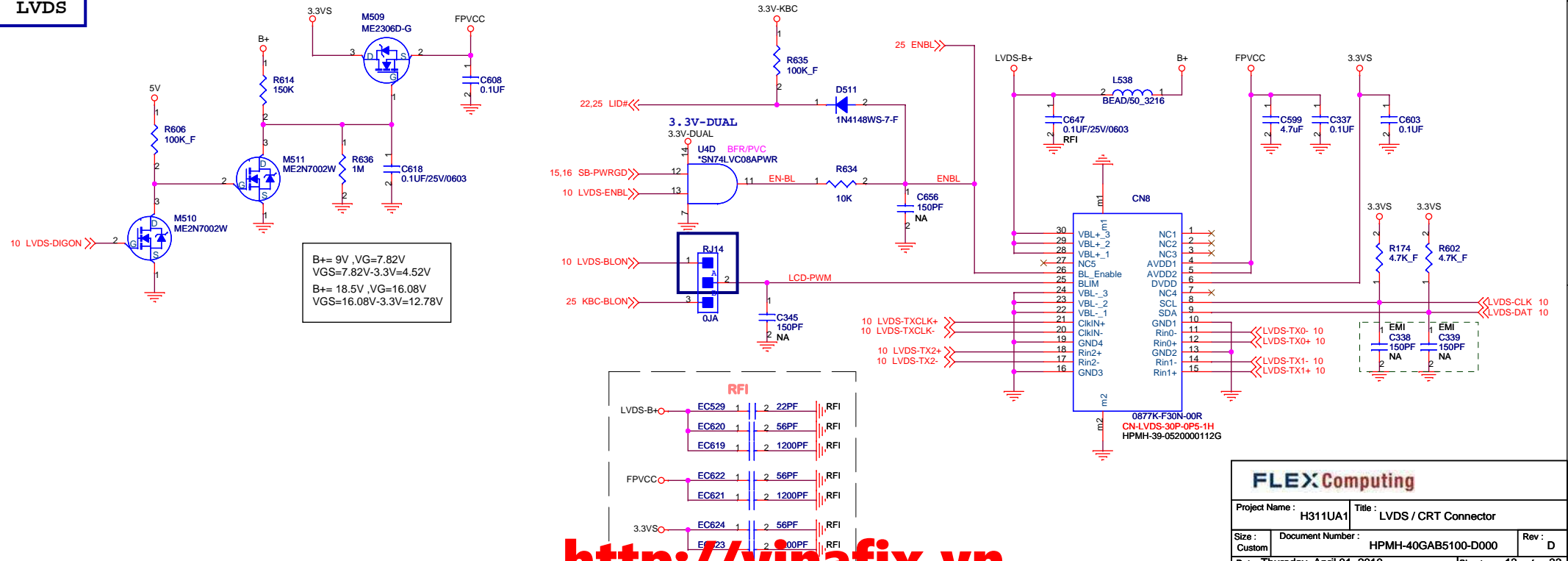
Project Name : H311UA1		Title : RS880M Power & Ground	
Size : Custom	Document Number : HPMJ-40GABS100-D000	Rev : D	
Date : Thursday, April 01, 2010	Sheet : 11		of 33



CLOSE CN517

- CRTB R610 1 150_F 2
- CRTG R615 1 150_F 2
- CRTTR R619 1 140_F 2

LVDS



B+= 9V, VG=7.82V
 VGS=7.82V-3.3V=4.52V
 B+= 18.5V, VG=16.08V
 VGS=16.08V-3.3V=12.78V

RFI

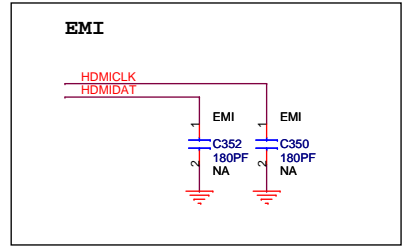
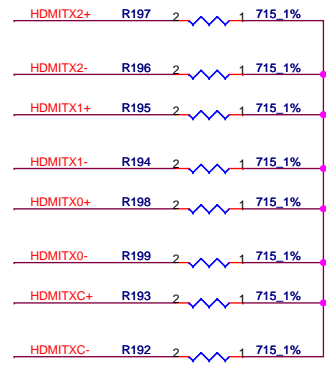
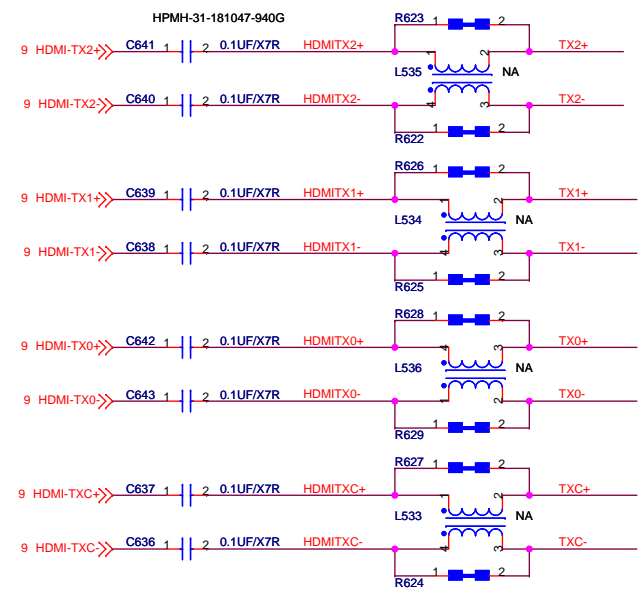
- LVDS-B+ EC529 1 2 22PF RFI
- EC620 1 2 56PF RFI
- EC619 1 2 1200PF RFI
- FPVCC EC622 1 2 56PF RFI
- EC621 1 2 1200PF RFI
- 3.3VS EC624 1 2 56PF RFI
- EC623 1 2 300PF RFI

vinafix
EMI

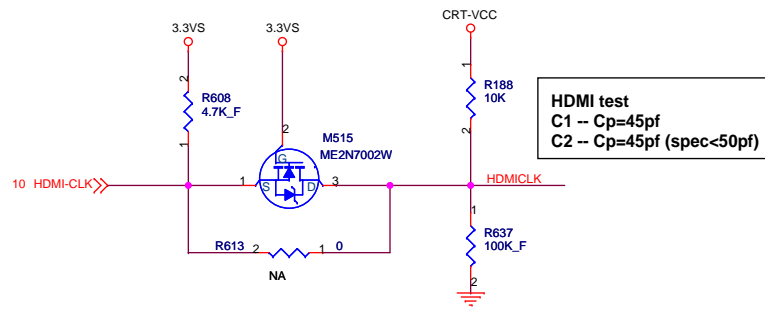
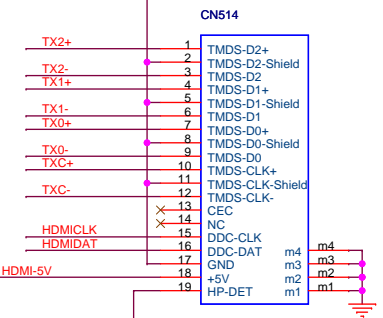
Main HPMH-32-200000056G - CHOKE 90ohm 0805 YCM0805F2SF-900T04
2nd HPMH-32-400108-000G - CHOKE COIL 90ohm WCM2012F2SF-900T04

Connected a 715-Ω 5% resistor on each signal connected with a FET to GND (one FET per pair) located on the TMDS connector side of the series capacitors.

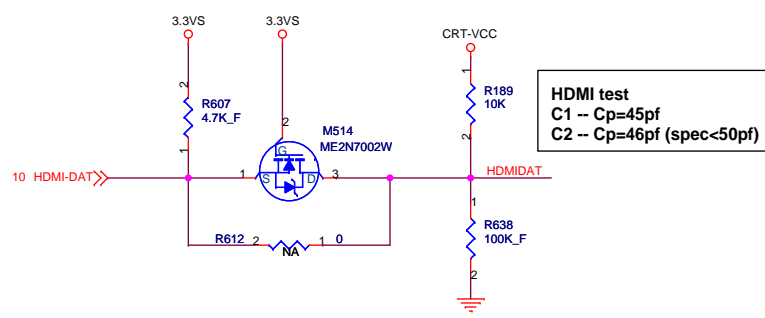
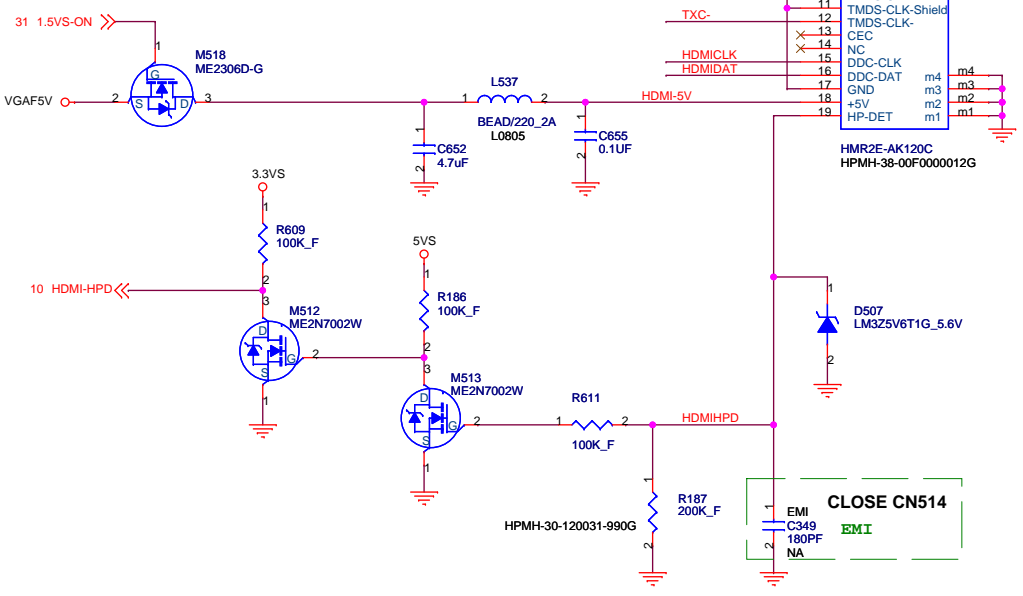
CLOSE CN514



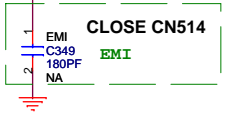
HDMI



HDMI test
C1 -- Cp=45pf
C2 -- Cp=45pf (spec<50pf)



HDMI test
C1 -- Cp=45pf
C2 -- Cp=46pf (spec<50pf)

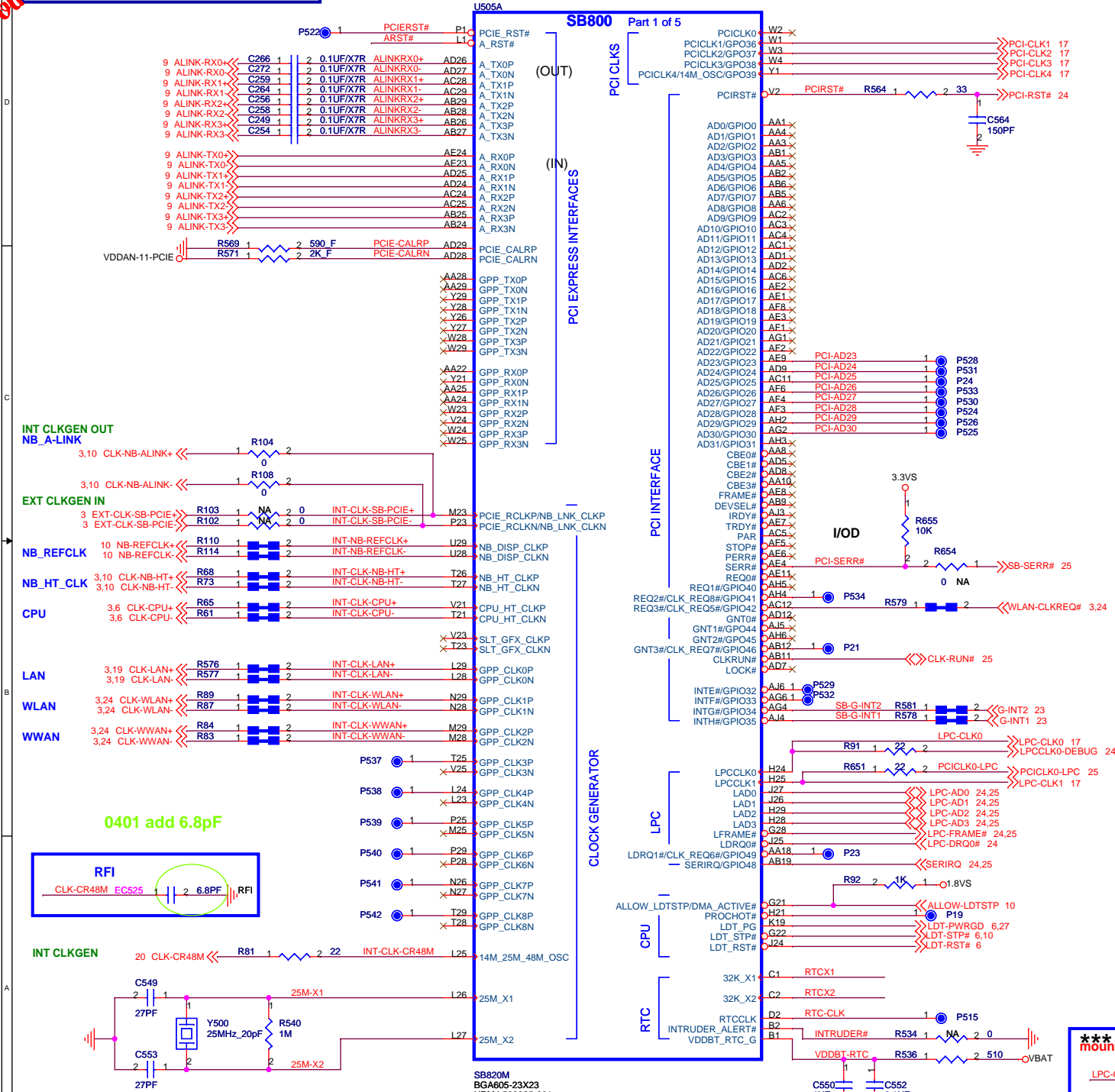


FLEX Computing

Project Name : H311UA1		Title : HDMI Connector	
Size : Custom	Document Number : HPMH-40GABS100-D000	Rev : D	
Date : Thursday, April 01, 2010	Sheet : 14 of 33		

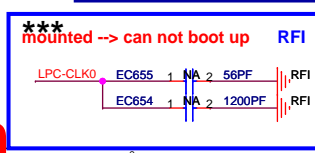
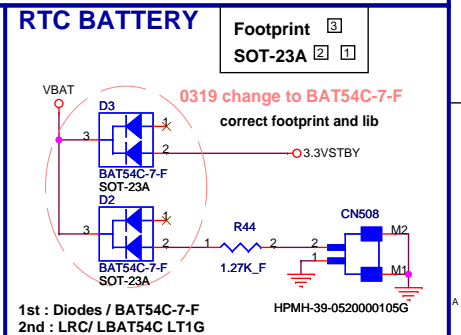
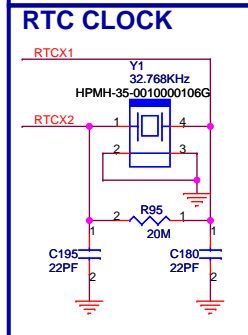
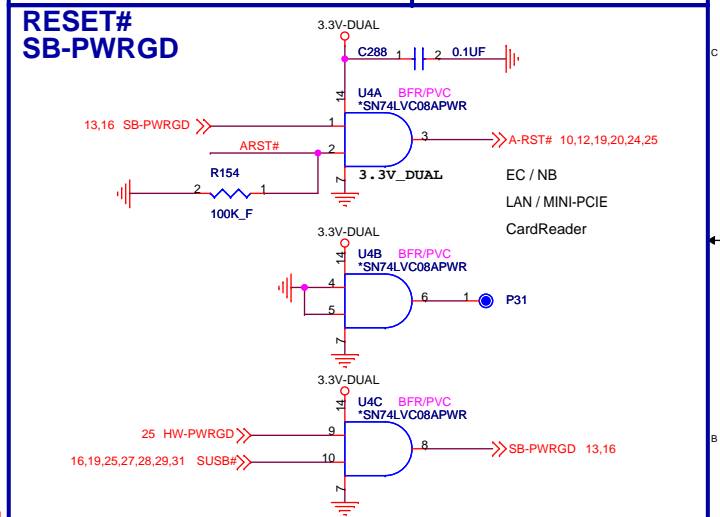
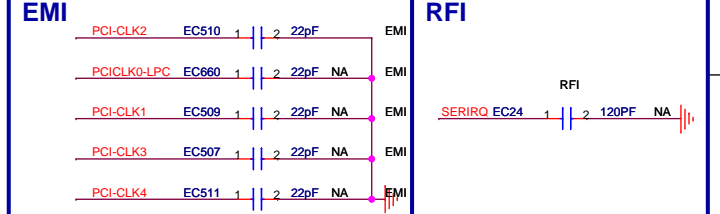
<http://vinafix.vn>

SB820M PCIE/PCI/CPU/LPC



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

SB820M DEBUG STRAPS SB820M has 15K Internal PU for PCI-AD[27:23]
Reserve TP and delete for layout spacing



FLEX Computing

Project Name : H311UA1 Title : SB820M PCIE/PCI/CPU/LPC

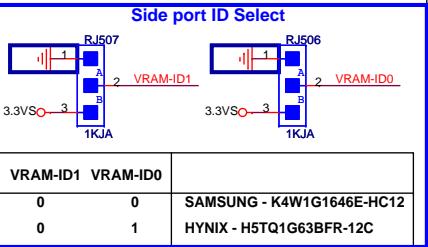
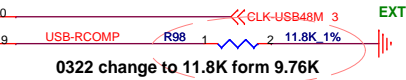
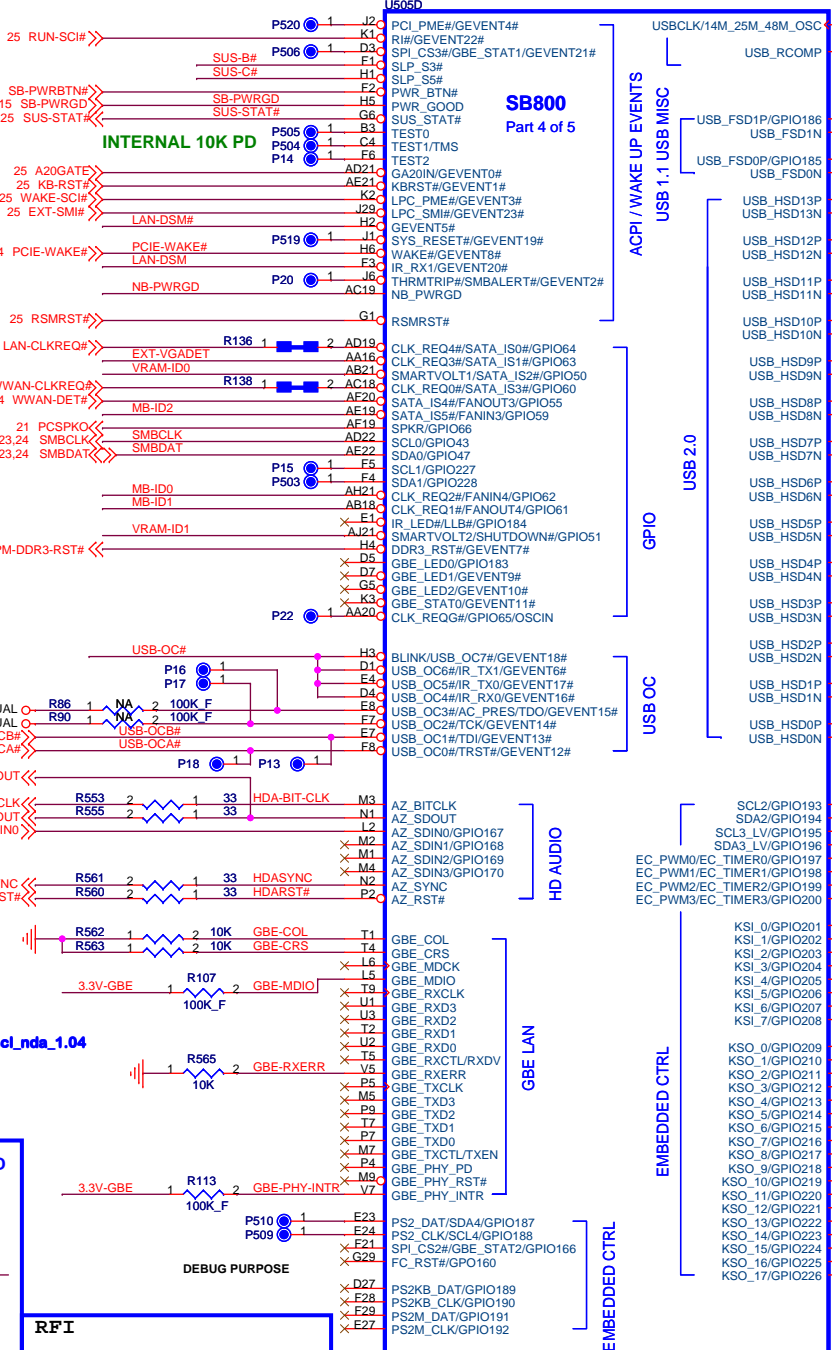
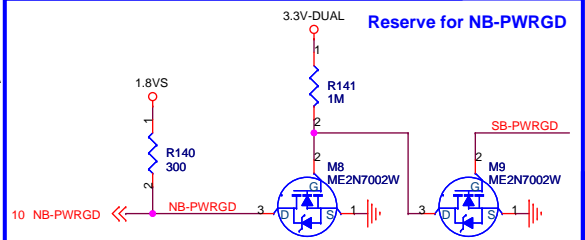
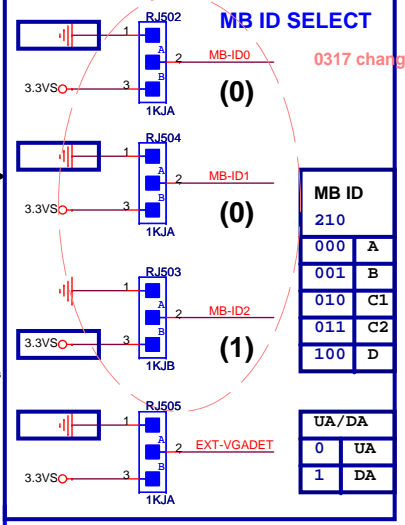
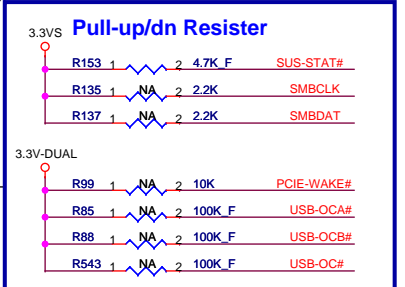
Size : Document Number : HPMH-40GAB5100-D000 Rev : D

Date : Thursday, April 01, 2010 Sheet : 15 of 33

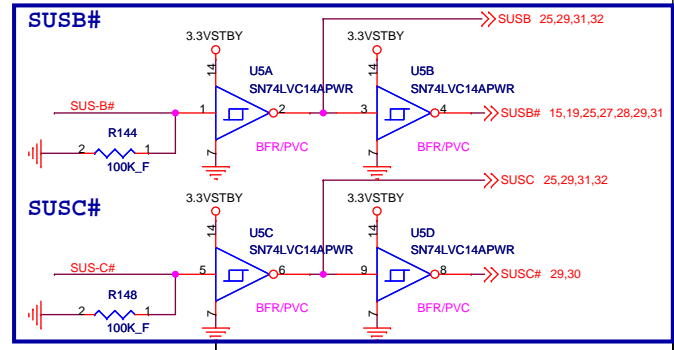
SB820M ACPI/GPIO/USB/AUDIO

LAN-DSM FUNCTION
 CABLE IN Hi
 CABLE OUT Low

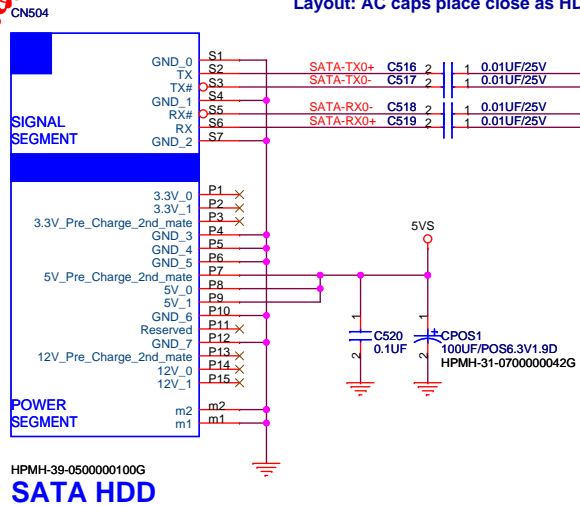
Auxiliary Clocks
 In integrated clock mode pads 14M_25M_48M and USBCLK output 14.318 MHz clocks by default (can also be configured to output 25 or 48 MHz). Output of these clocks varies cyclically, thus they are not recommended for use as PLL inputs. They are intended for use as auxiliary clocks only



- WWAN
- WLAN
- Card Reader
- Webcam
- BT
- PORT 3
- PORT 2
- PORT 1
- PORT 0



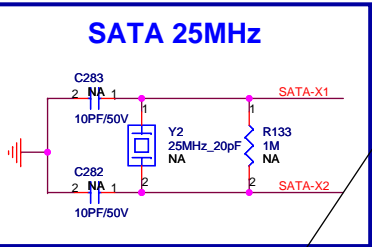
Layout: AC caps place close as HDD connector



SATA HDD

HPMH-39-050000100G

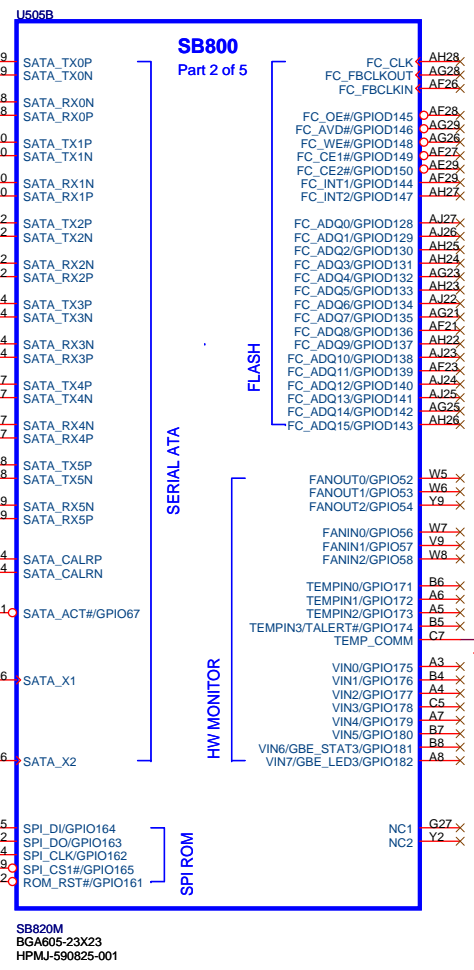
TO MEET SB800 SCL1.02 ITEM 41-20 / 41-25 DNI SATA XTAL circuit's parts.



SATA 25MHz

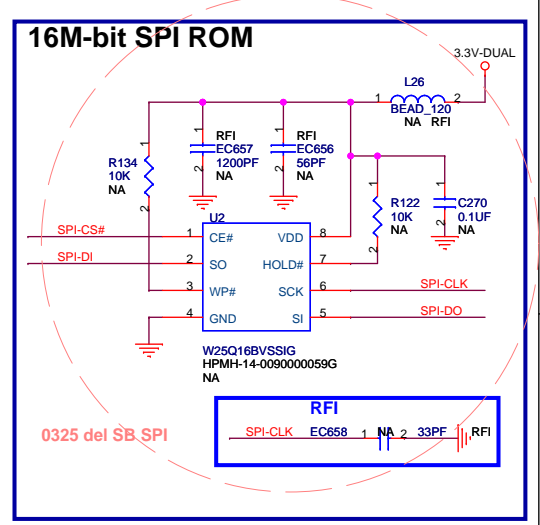
* Flash controller function is not supported on SB8xx platforms.
** A-Link Express III, PCIe Gen 2 speeds, and embedded controller functions are only supported on the SB810 and SB850.

3.3V - Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.



SB820M
BGA605-23X23
HPMJ-590825-001

SB820M SATA / IDE / SPI / STRAPS

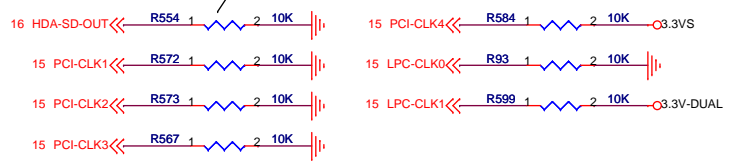


16M-bit SPI ROM

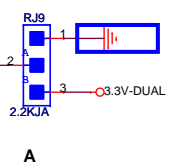
0325 del SB SPI

Temperature Monitor Not Implemented: Connected to GND.

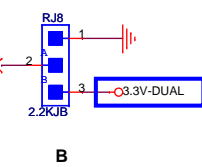
SB820 H/W STRAPS



RJ9A - L



RJ8B - H



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

FLEX Computing

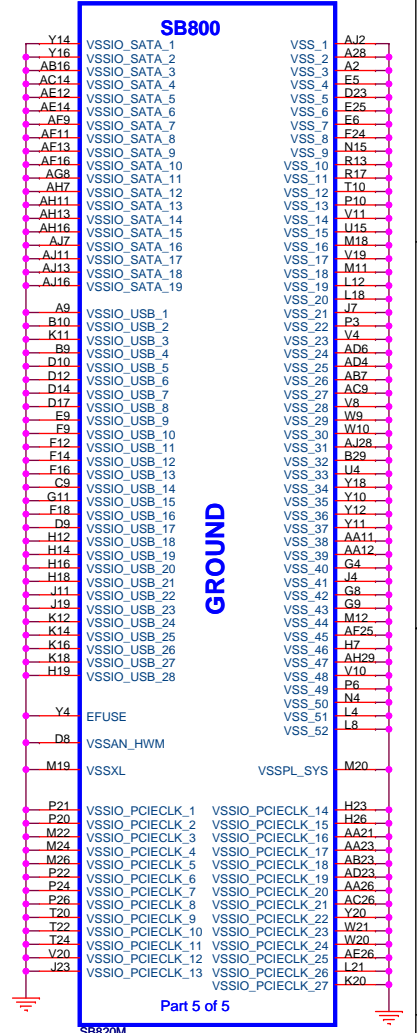
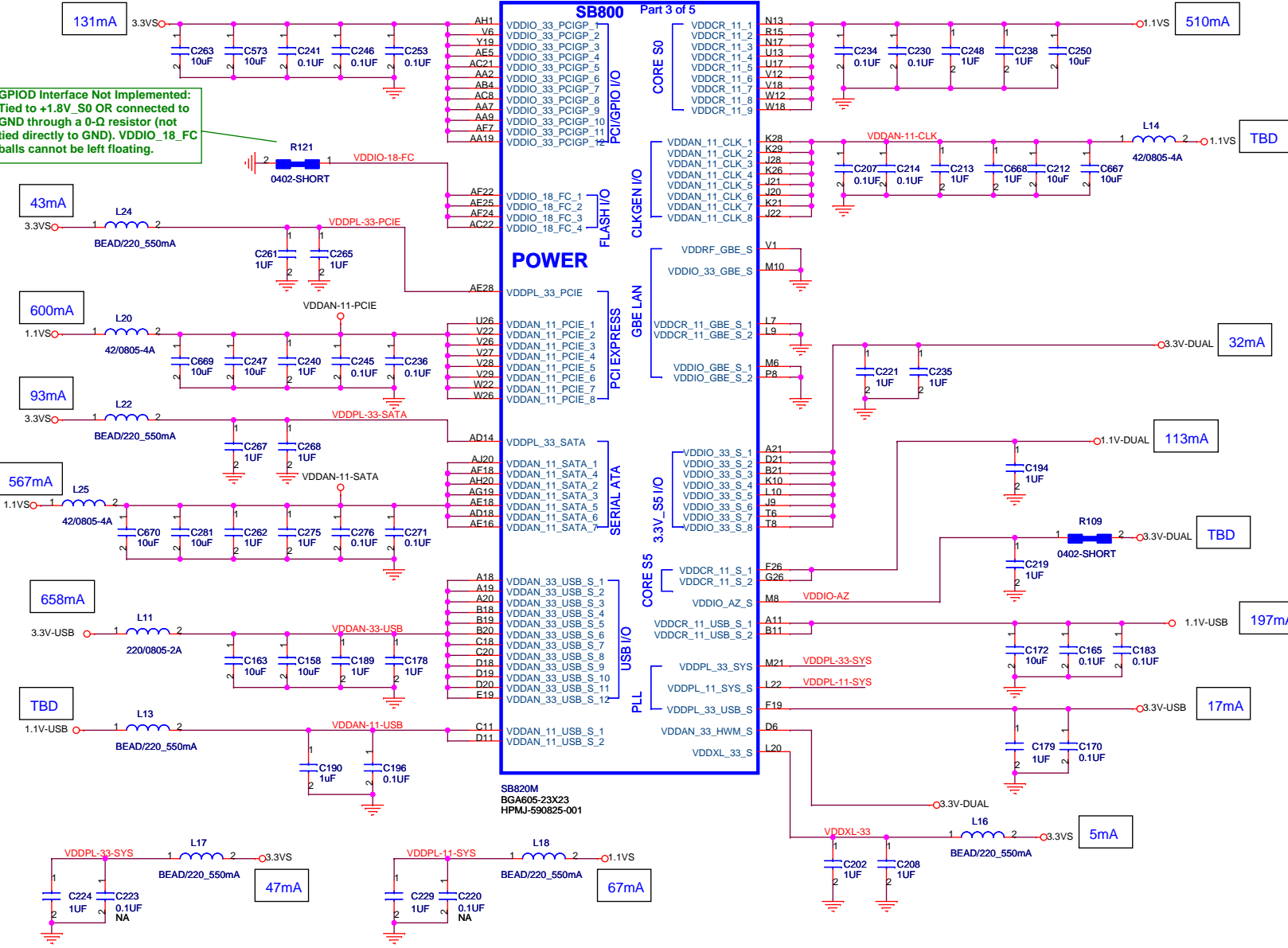
Project Name : H311UA1 Title : SB820M SATA / IDE / SPI / STRAPS

Size : Document Number : HPMH-40GABS100-D000 Rev : D

Date : Thursday, April 01, 2010 Sheet : 17 of 33

vinafix

GPIO Interface Not Implemented:
Tied to +1.8V_S0 OR connected to GND through a 0-Ω resistor (not tied directly to GND). VDDIO_18_FC balls cannot be left floating.



1.1V_USB	S3	S4	S5
AC	ON	ON	ON
DC	ON	OFF	OFF

FLEX Computing

Project Name: H311UA1 Title: SB820M PWR / GND

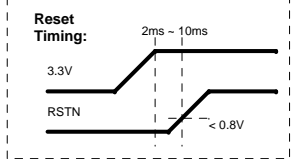
Size: Document Number: HPMH-40GAB5100-D000 Rev: D

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<http://vinafix.vn>

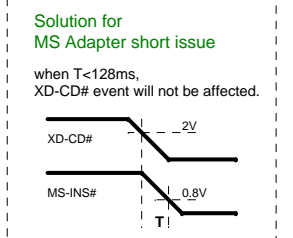
Alcor AU6433-GEF Card supported:

- SD v2.0 (SDHC)
- MMC v4.2
- MS v1.43
- MS-PRO v1.03
- MS PRO-HG v1.01
- xD v1.2



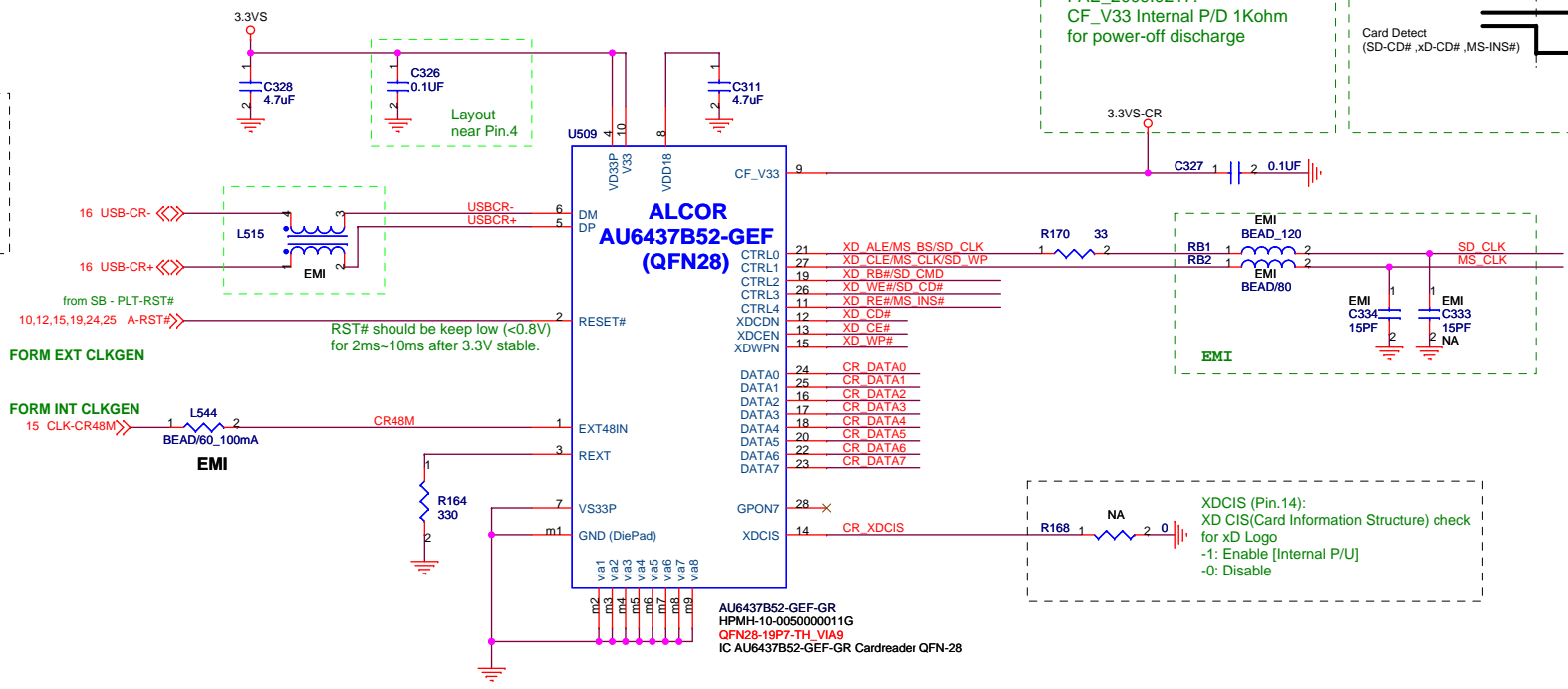
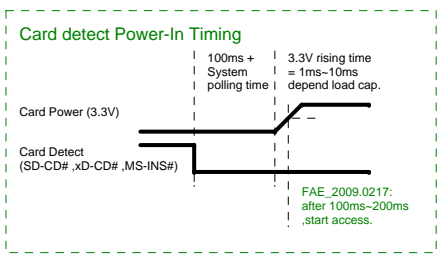
FAE_2009.0117:
Memory Stick Formatter for MS Logo
- Enable

FAE_2009.0117:
SD write protect
- Decided by SD-WP of SD Card



Card Power V33 = 3.3V ~ 2.8V
Card Power OCP = 420mA

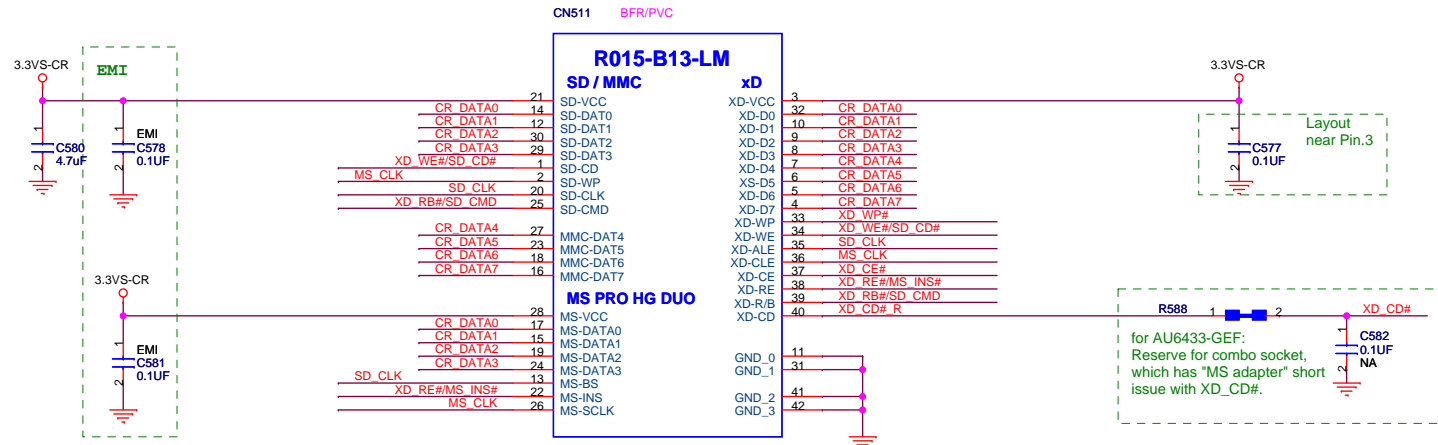
FAE_2009.0217:
CF_V33 Internal P/D 1Kohm
for power-off discharge



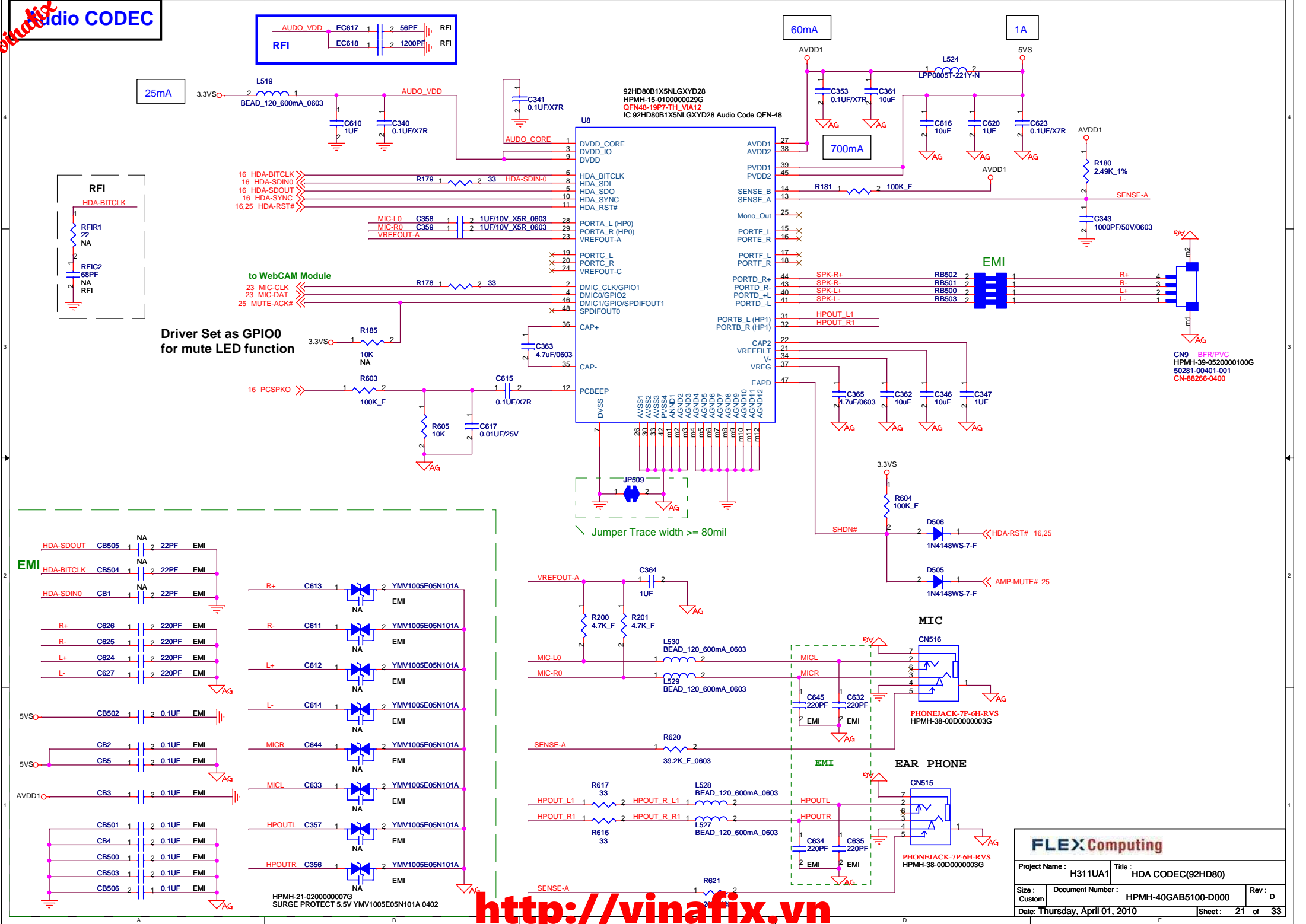
Memory Card Socket

R015-B13-LM
HPMH-38-0610000002G

- Card type Supported:
- SD
 - SD IO
 - MMC
 - MMC4.0
 - MS
 - MS Pro
 - xD

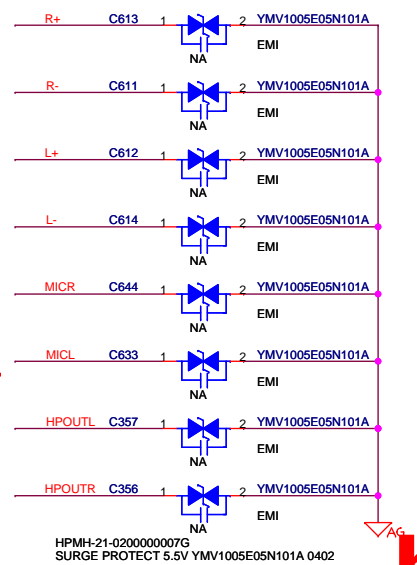
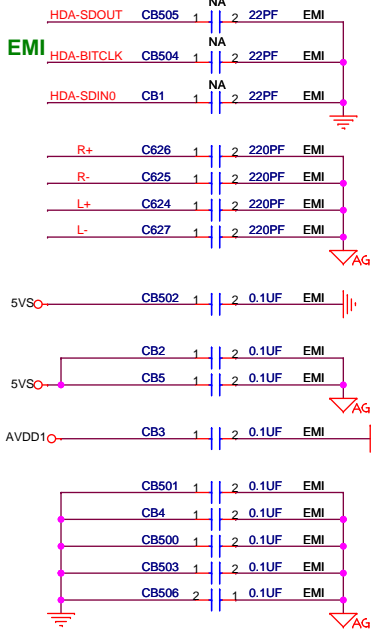


R015-B13-LM
HPMH-38-0610000005G
CN-7IN1CARD-42P-OP7-5H3
CONN 7IN1 PUSH-PUSH R015-B13-HM 40P

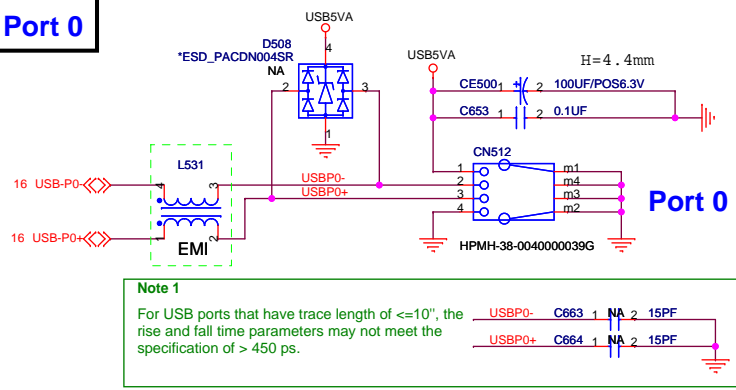


Driver Set as GPIO0 for mute LED function

Jumper Trace width >= 80mil



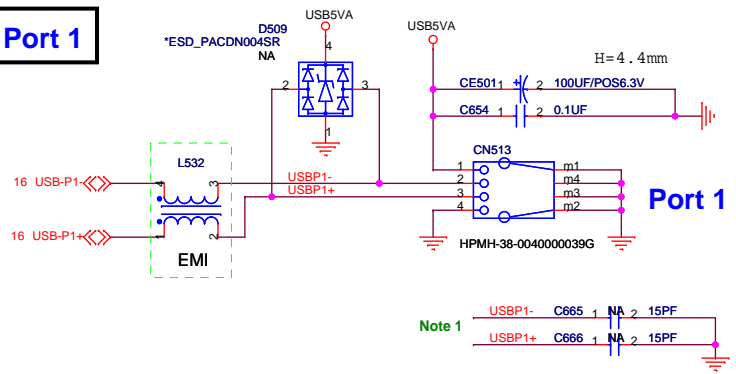
USB Port 0



Note 1
For USB ports that have trace length of <=10", the rise and fall time parameters may not meet the specification of > 450 ps.

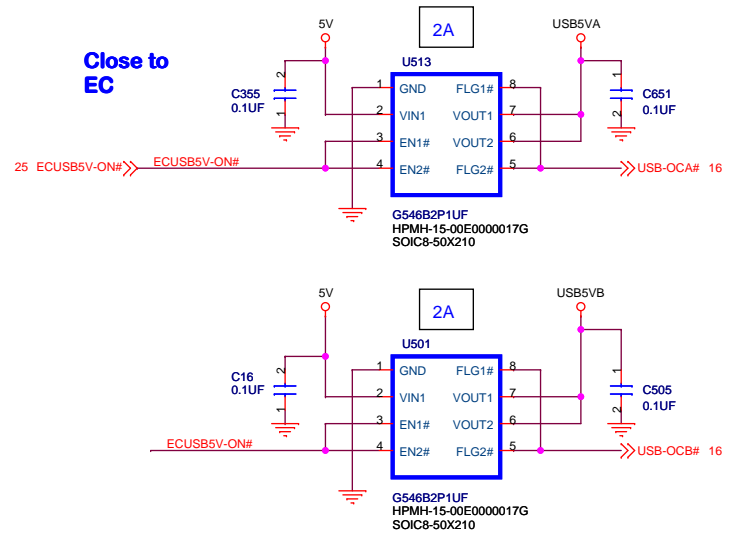
USBP0- C663 1 NA 2 15PF
USBP0+ C664 1 NA 2 15PF

USB Port 1

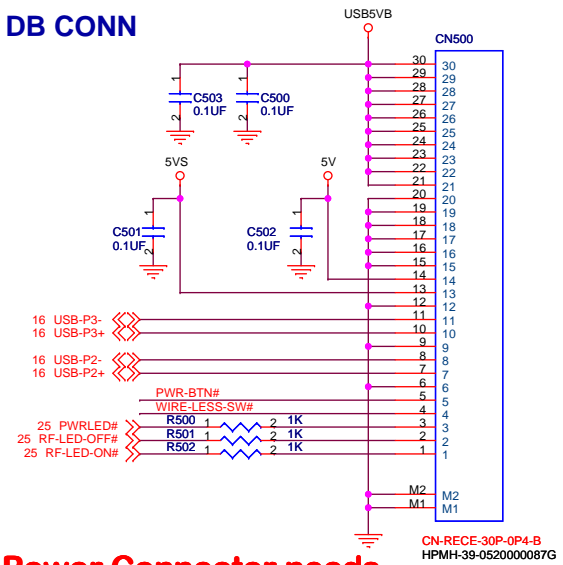


Note 1
USBP1- C665 1 NA 2 15PF
USBP1+ C666 1 NA 2 15PF

Close to EC

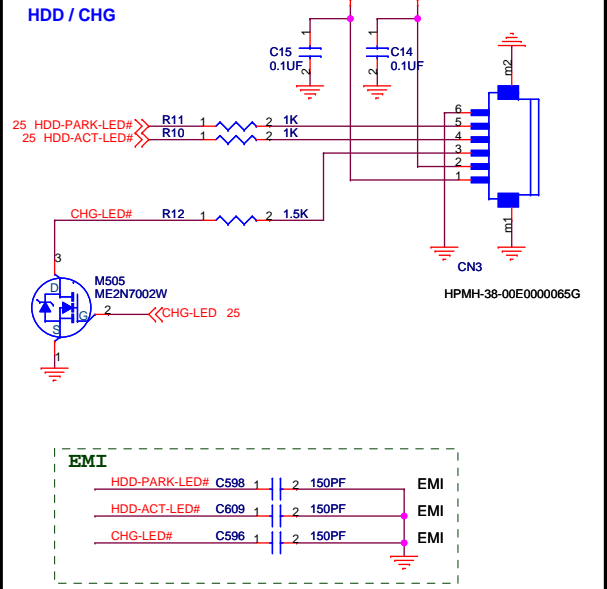


USB DB CONN



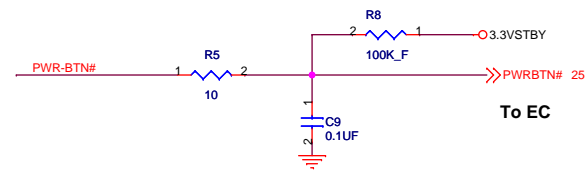
USB Power Connector needs >2A

LED DB CONN

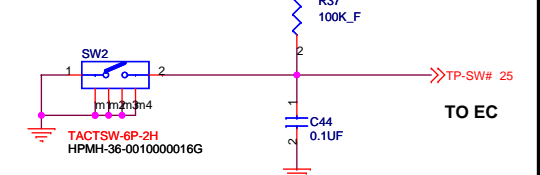


EMI
HDD-PARK-LED# C598 1 2 150PF EMI
HDD-ACT-LED# C609 1 2 150PF EMI
CHG-LED# C596 1 2 150PF EMI

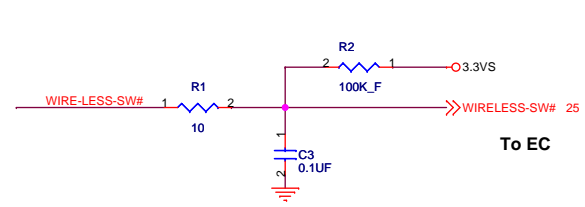
Power ON/OFF Button



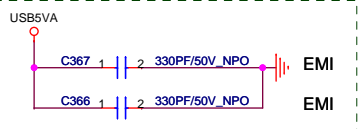
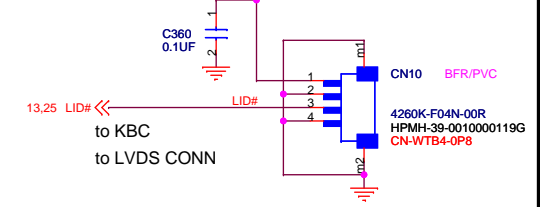
TP LOCK SWITCH



Wireless ON/OFF Button

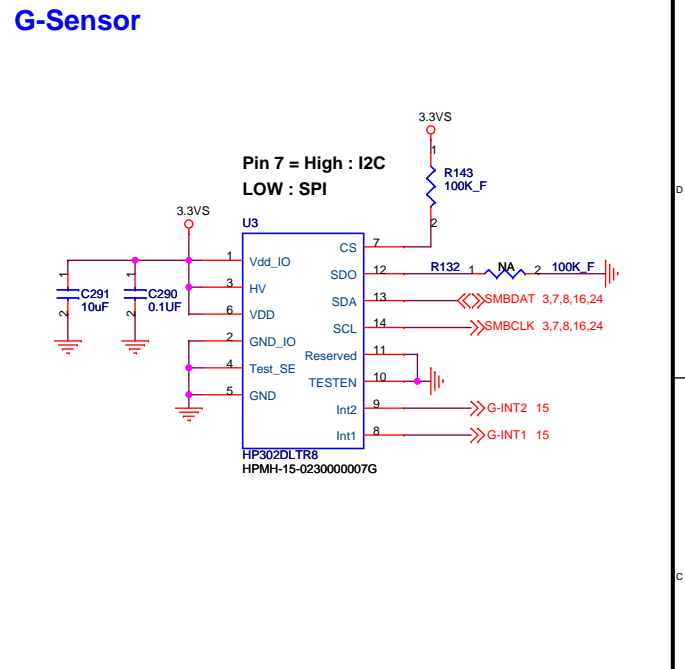
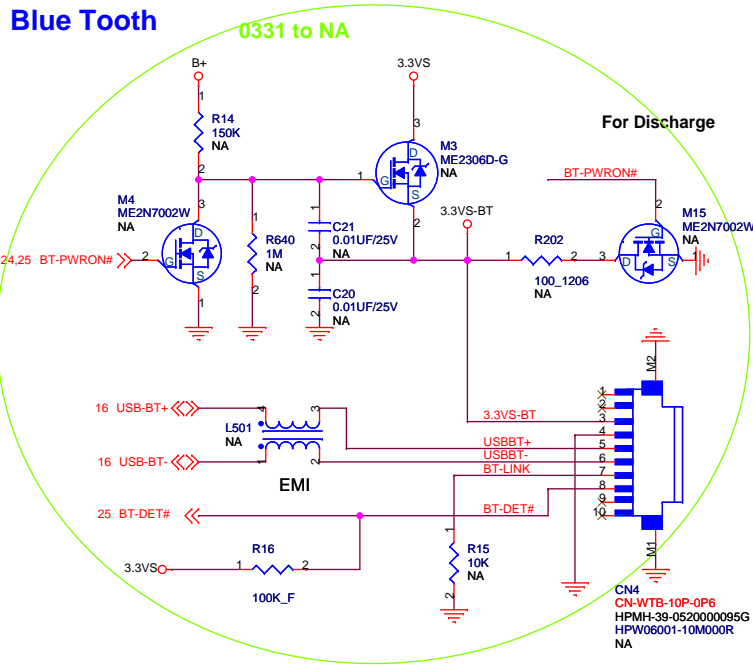
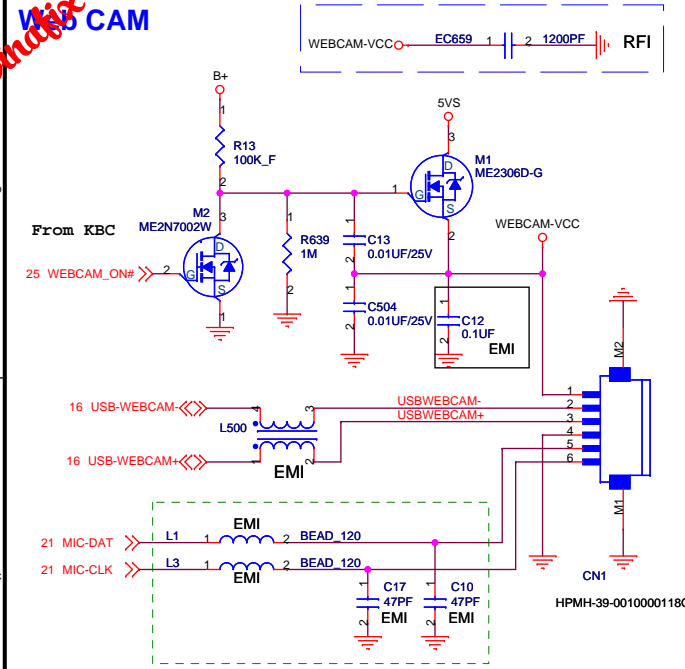


LID Switch

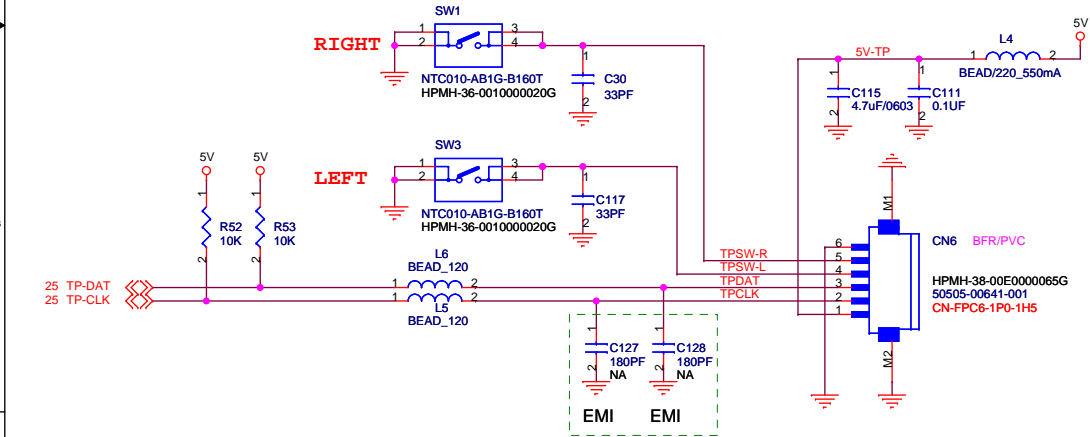


FLEX Computing		
Project Name :	H311UA1	Title : USB / USB CON
Size : Custom	Document Number : HPMH-40GABS100-D000	Rev : D
Date : Thursday, April 01, 2010	Sheet : 22 of 33	

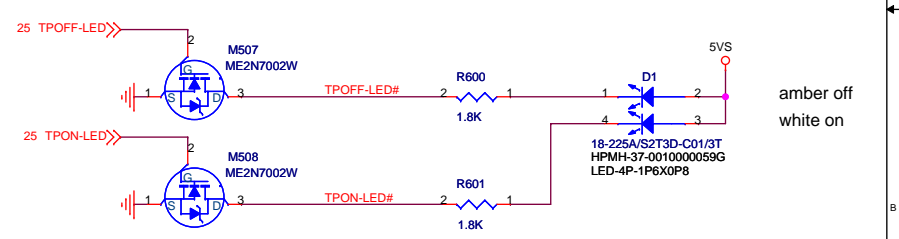
<http://vinafix.vn>



Touch Pad

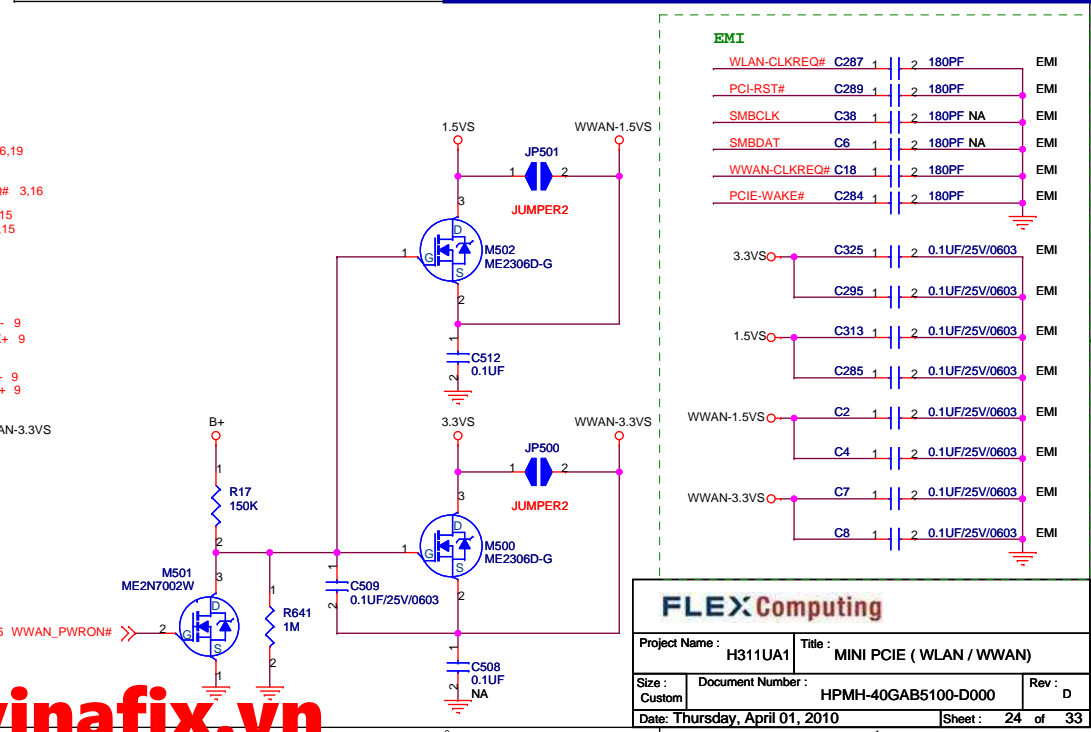
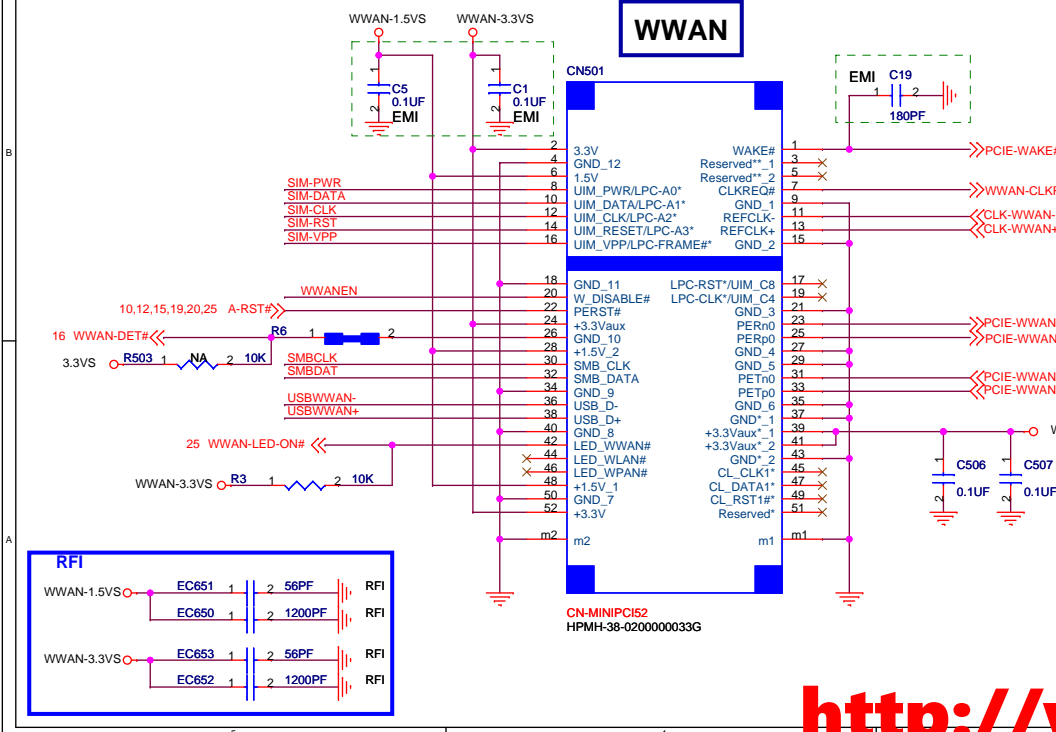
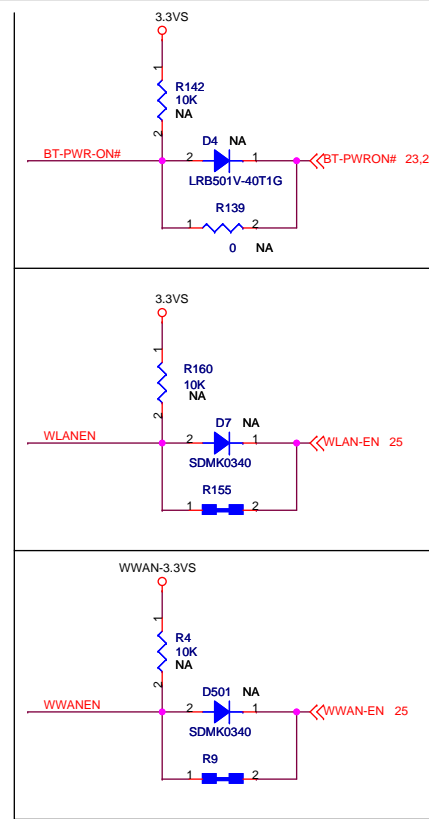
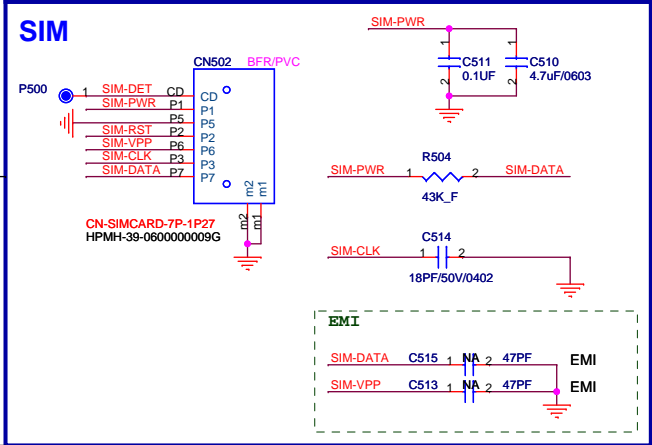
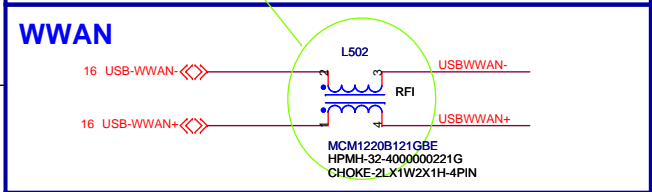
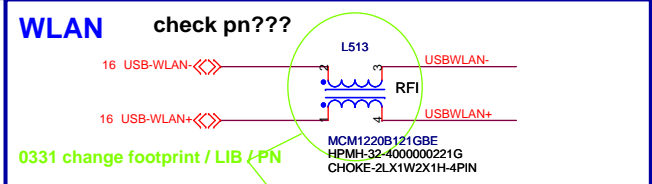
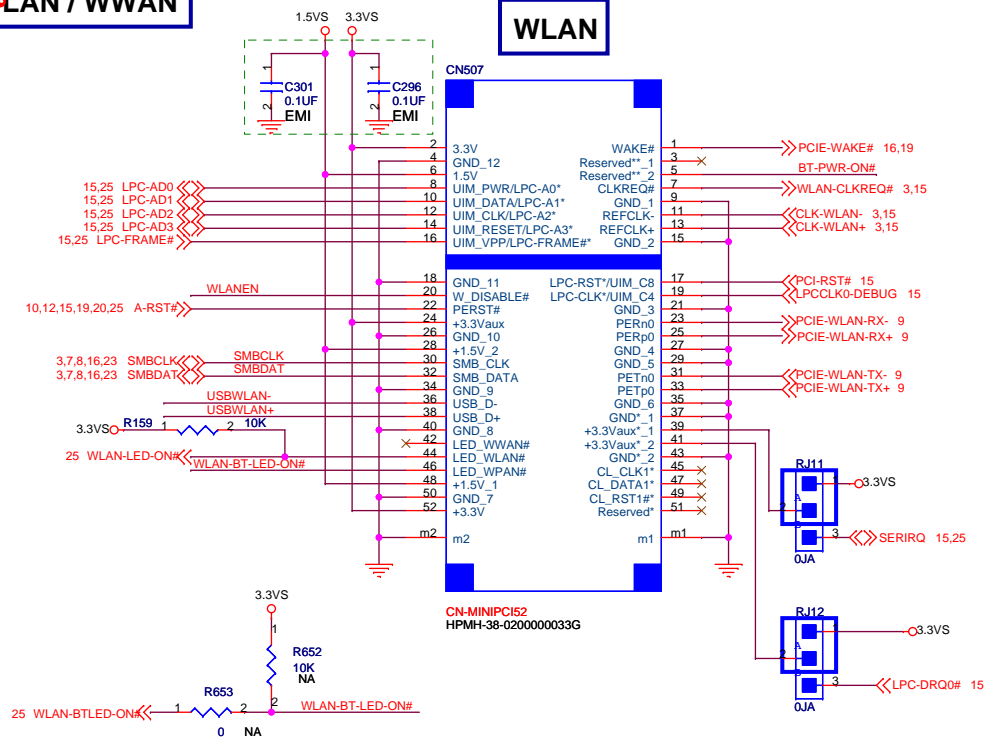


Touch Pad Active LED



Web CAM	Blue Tooth	WWAN-3.3V	WWAN-1.5V
R13=100K/ R639=1M B+= 9V ,VG=8.18V VGS=8.18V-5V=3.18V VGS(th)=1.5V (Max=3V)	R14=150K / R640=1M B+= 9V ,VG=7.82V VGS=7.82V-3.3V=4.52V VGS(th)=1.5V (Max=3V)	R17=150K / R641=1M B+= 9V ,VG=7.82V VGS=7.82V-3.3V=4.52V VGS(th)=1.5V (Max=3V)	R17=150K / R641=1M B+= 9V ,VG=7.82V VGS=7.82V-1.5V=6.32V VGS(th)=1.5V (Max=3V)
R13=100K/ R639=1M B+= 18.5V ,VG=16.81V VGS=16.81V-5V=11.81V VGS(th)=1.5V (Max=3V)	R14=150K / R640=1M B+= 18.5V ,VG=16.08V VGS=16.08V-3.3V=12.78V VGS(th)=1.5V (Max=3V)	R17=150K / R641=1M B+= 18.5V ,VG=16.08V VGS=16.08V-3.3V=12.78V VGS(th)=1.5V (Max=3V)	R17=150K / R641=1M B+= 18.5V ,VG=16.08V VGS=16.08V-1.1V=14.15V VGS(th)=1.5V (Max=3V)

WLAN / WWAN



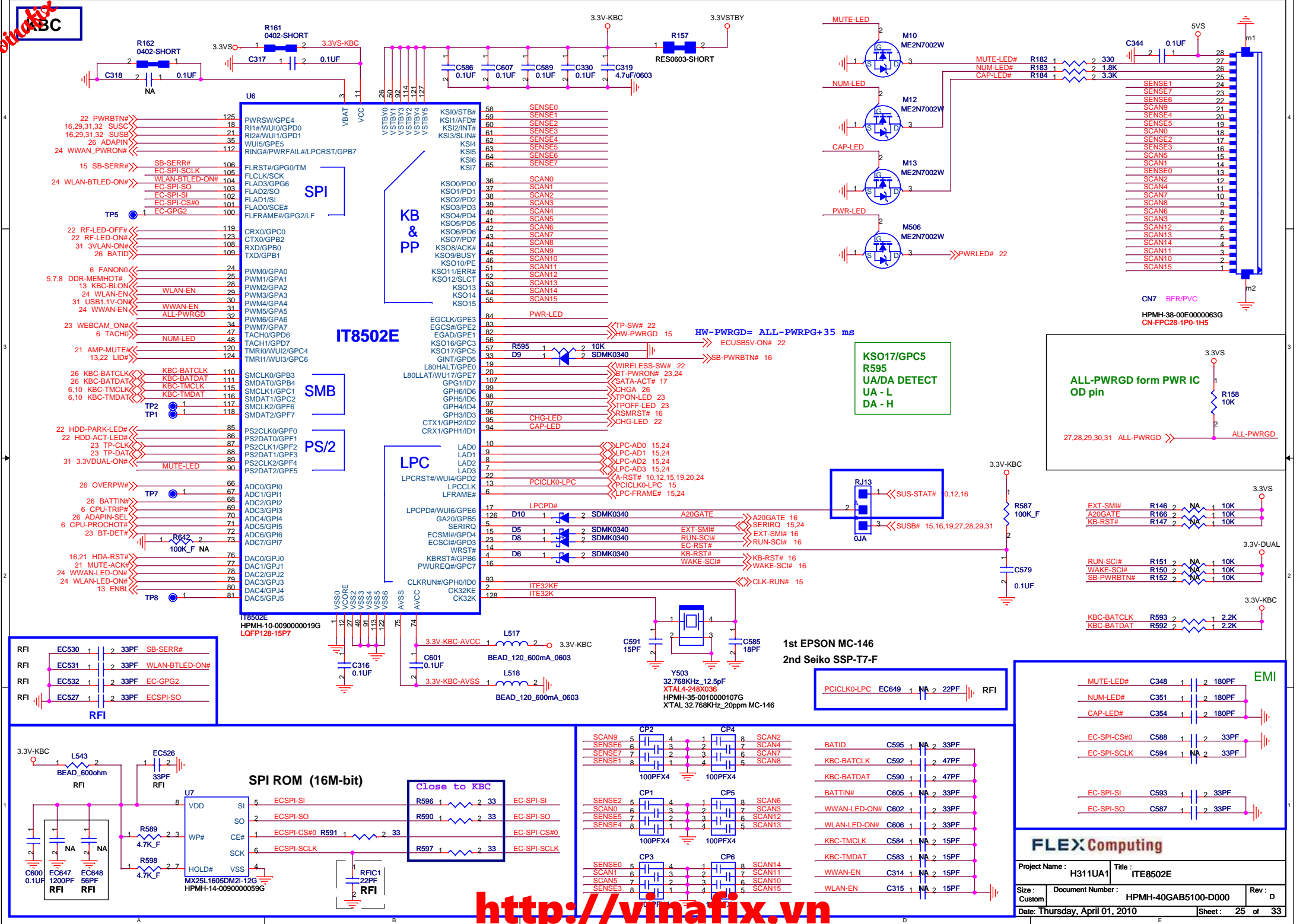
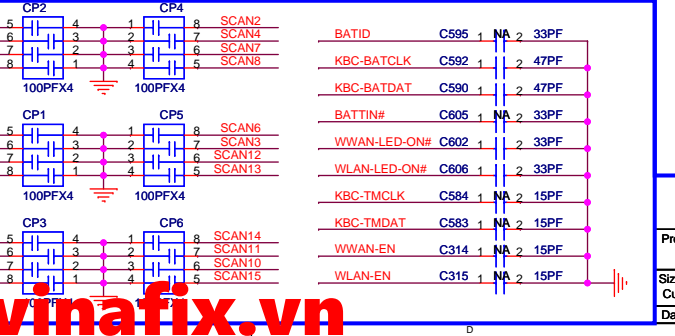
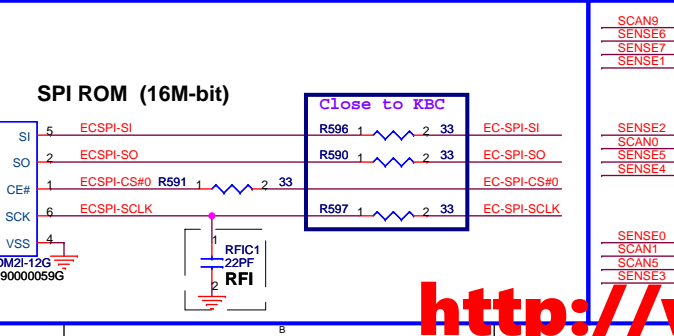
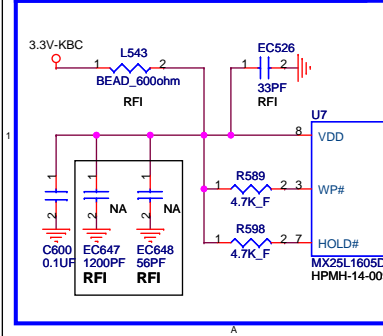
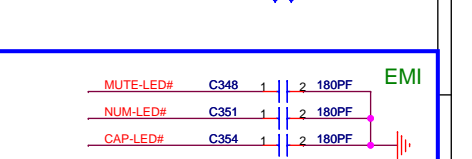
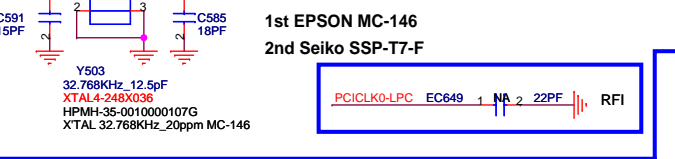
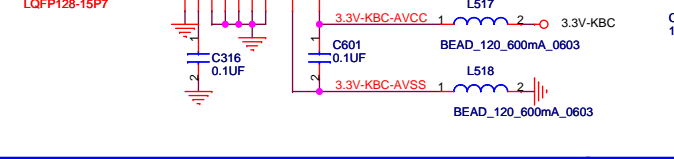
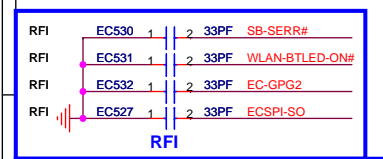


Table of pin connections for the ITE8502E microcontroller, including signals like PWRBTN#, SB-SERR#, WLAN-BTLED-ON#, and various power and ground pins.

Table of pin connections for the LPC microcontroller, including signals like KSO0/PD0, KSO1/PD1, KSO2/PD2, and various power and ground pins.

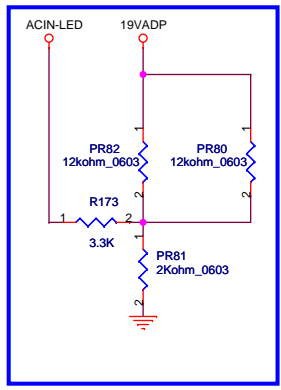
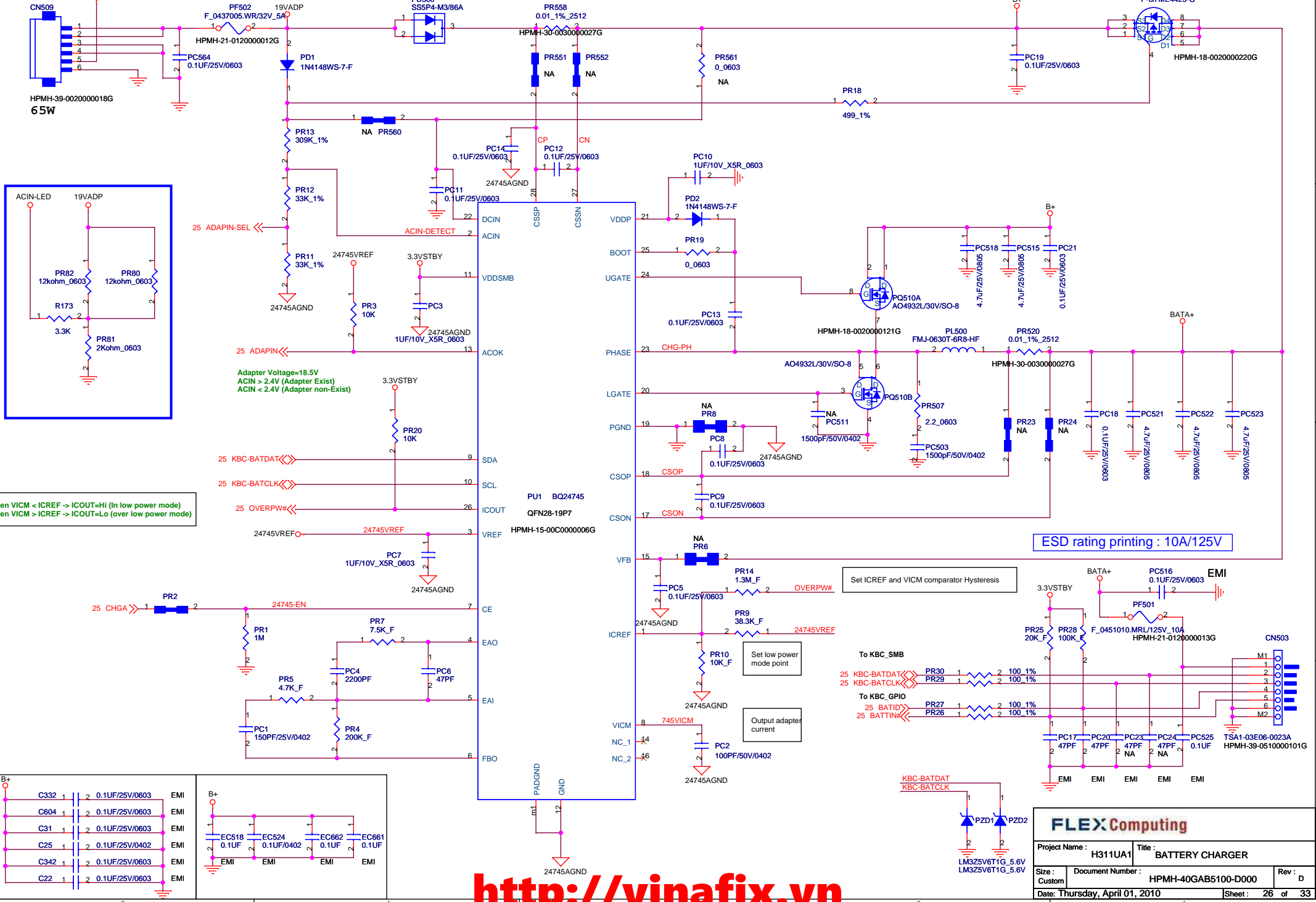
Table of pin connections for the PS/2, SMB, and PS/2 controllers, including signals like PS2CLK0/GPF0, PS2DAT0/GPF1, and SMB signals.

Table of pin connections for the LED drivers and other peripheral components, including signals like MUTE-LED, NUM-LED, CAP-LED, and PWR-LED.



FLEX Computing logo and project information: Project Name: H311UA1, Title: ITE8502E, Document Number: HPMH-40GAB5100-D000, Date: Thursday, April 01, 2010, Sheet: 25 of 33.

ESD rating printing : 5A/125V



25 ADAPIN-SEL

ACIN-DETECT

Adapter Voltage=18.5V
ACIN > 2.4V (Adapter Exist)
ACIN < 2.4V (Adapter non-Exist)

When VICM < ICREF -> ICOUT=Hi (In low power mode)
When VICM > ICREF -> ICOUT=Lo (over low power mode)

ESD rating printing : 10A/125V

Set ICREF and VICM comparator Hysteresis

Set low power mode point

Output adapter current

To KBC_SMB
25 KBC-BATDAT PR30 1 2 100 1%
25 KBC-BATCLK PR29 1 2 100 1%

To KBC_GPIO
25 BATID PR27 1 2 100 1%
25 BATTIN PR26 1 2 100 1%

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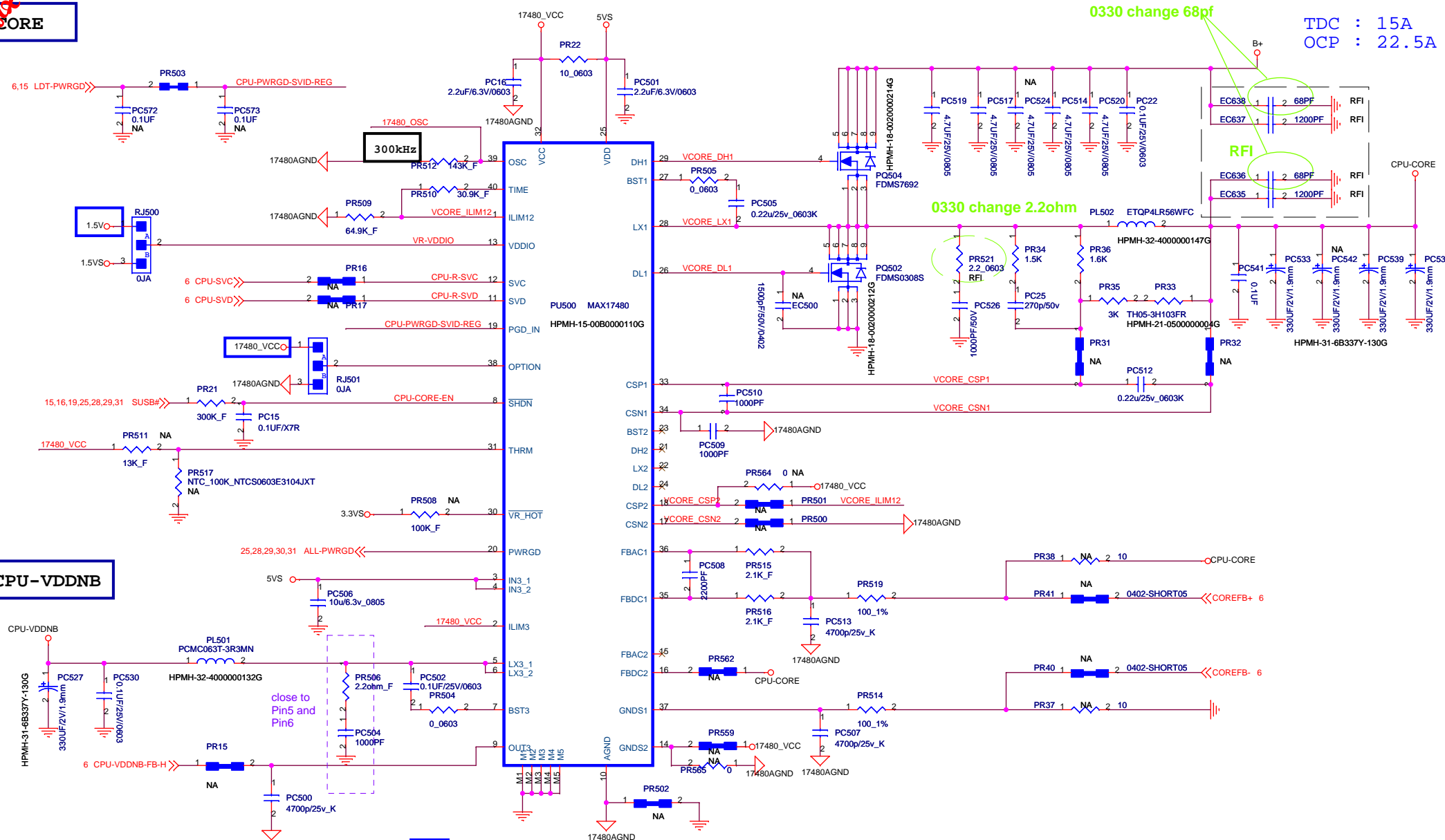
Project Name : H311UA1 Title : BATTERY CHARGER

Size : Custom Document Number : HPMH-40GABS100-D000 Rev : D

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CORE

TDC : 15A
OCP : 22.5A

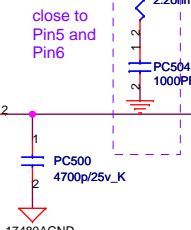


0330 change 68pf

0330 change 2.2ohm

RFI

CPU-VDDNB



SVC	SVD	BOOT VOLTAGE V _{OUT} (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

AMD Steven Review
While the system is in S3, CPU drives SVD high to VDDIO, and drives SVC low to ground. VDDIO stays powered on from S0 through S3. VDDIO_RUN does not stay powered on in S3 state and is effectively ground.

<http://vinafix.vn>

FLEX Computing

Project Name : H311UA1 Title : CPU_CORE

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EN/PSV high: >2.9V (set Auto-skip mode)
EN/PSV low: <0.7V (set PWM mode)

$$I_{ocp} = \frac{(PR18 \cdot 10)}{R_{ds(on)}} + I_{o(max)} / 3$$

$$= \frac{(12 \cdot 10)}{12} + 4.9 = 14.5A$$

$$V_o = 0.75 \cdot (1 + (PR529 / PR531))$$

$$= 0.75 \cdot (1 + 0.47) = 1.107V$$

Max=8A
OCP=12A

G0	G1	
0	0	0.95V
1	0	1.1V

EN/DEM= high @ Diode-Emulation Mode (Skip mode)
EN/DEM=floating @ Forced-CCM Mode (PWM mode)
EN/DEM high: >2.9V
EN/DEM low: <0.8V

$$V_o = 0.75 \cdot (1 + (PR8 / PR534))$$

$$= 0.75 \cdot (1 + 0.333) = 0.95V$$

Max=10A
OCP=15A

0.95VS

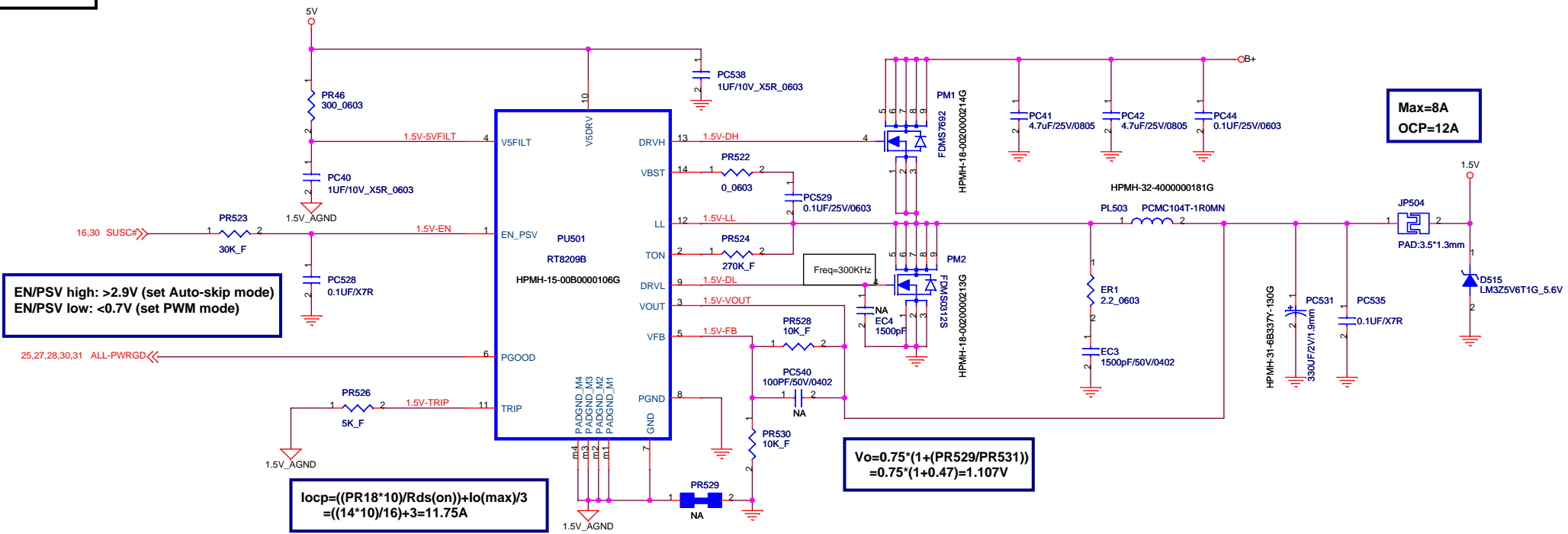
FLEX Computing

Project Name: H311UA1 Title: 1.1VS / NB-CORE

Size: Custom Document Number: HPMH-40GABS100-D000 Rev: D

Date: Thursday, April 01, 2010 Sheet: 28 of 33

1.5V_DDR



EN/PSV high: >2.9V (set Auto-skip mode)
EN/PSV low: <0.7V (set PWM mode)

$$I_{ocp} = ((PR18 * 10) / R_{ds(on)}) + I_o(max) / 3$$

$$= ((14 * 10) / 16) + 3 = 11.75A$$

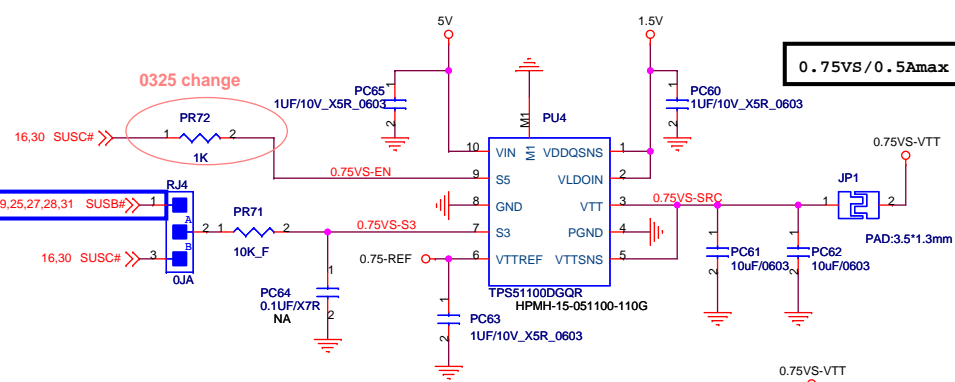
$$V_o = 0.75 * (1 + (PR529 / PR531))$$

$$= 0.75 * (1 + 0.47) = 1.107V$$

Max=8A
OCP=12A

0.75VS DDR3-VTT

Integrated Divider Tracks 1/2
VDDQSNS for VTT and VTTREF



0.75VS / 0.5Amax

0.9V=1.5A

$$V_{out} = 0.8 * (R1 + R2) / R2$$

CPU-VDDR 0.9V

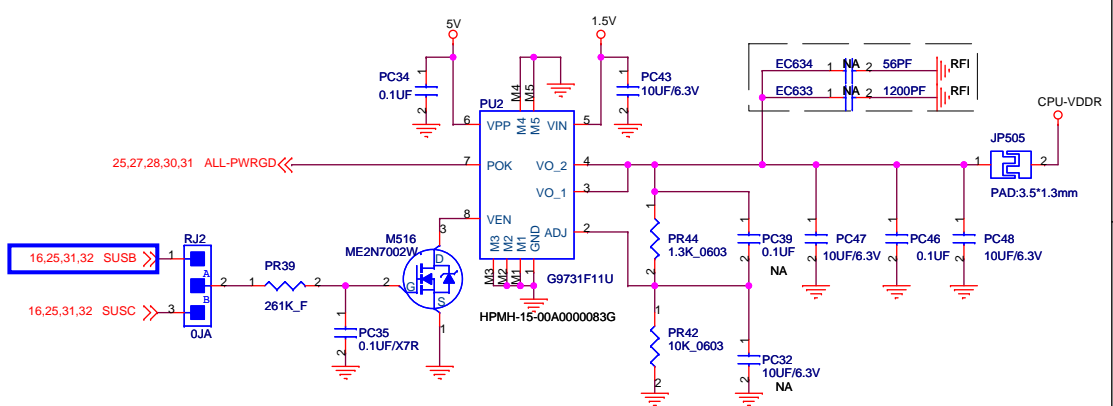


Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

FLEX Computing

Project Name: H311UA1 Title: 1.5V / 0.75VS / CPU-VDDR

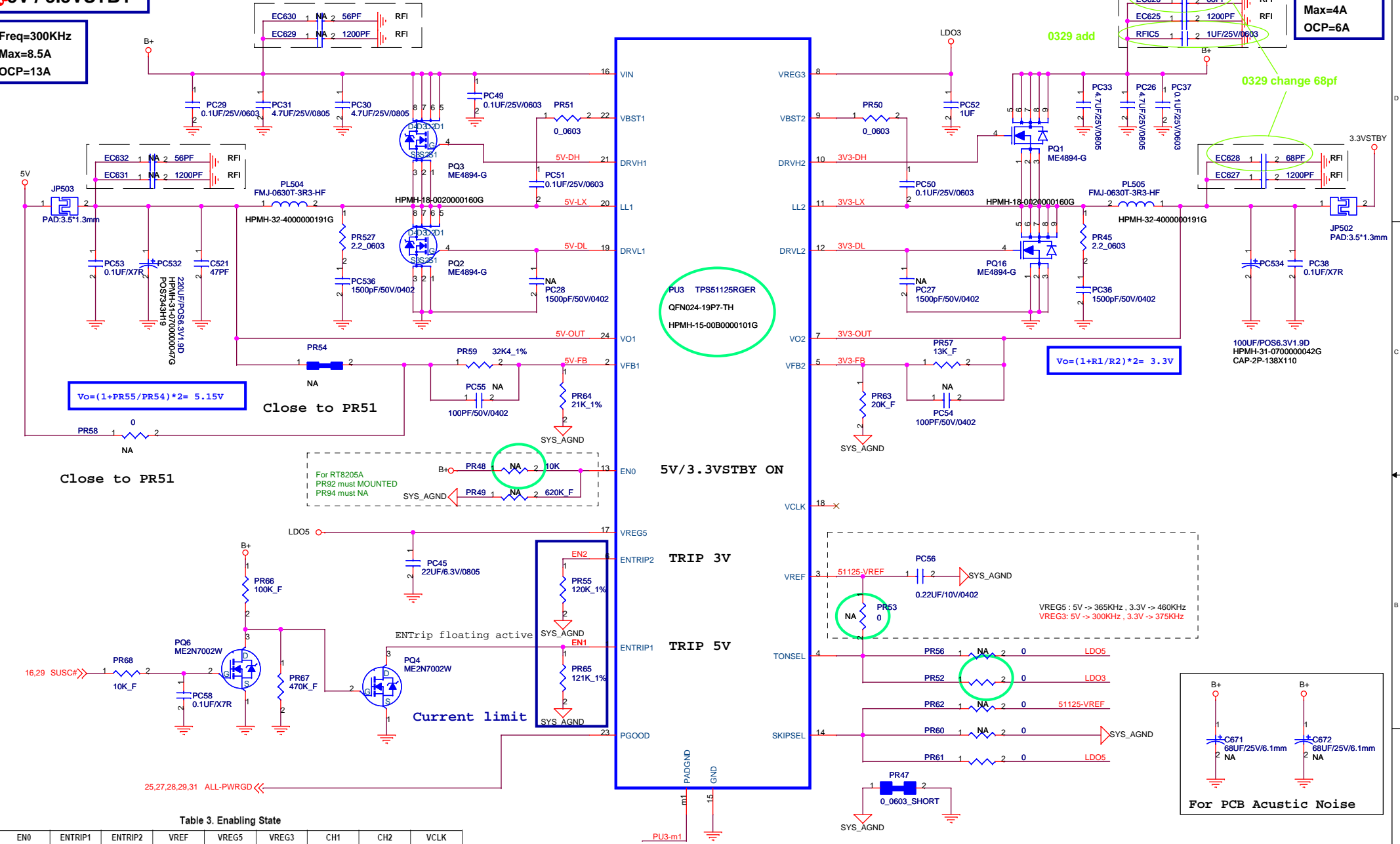
Size: Custom Document Number: HPMH-40GABS100-D000 Rev: D

Date: Thursday, April 01, 2010 Sheet: 29 of 33

5V / 3.3VSTBY

Freq=300KHz
Max=8.5A
OCP=13A

Freq=375KHz
Max=4A
OCP=6A



$V_o = (1 + PR55 / PR54) * 2 = 5.15V$

$V_o = (1 + R1 / R2) * 2 = 3.3V$

Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Off	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

PU3-m1
For layout request, no connect anything.

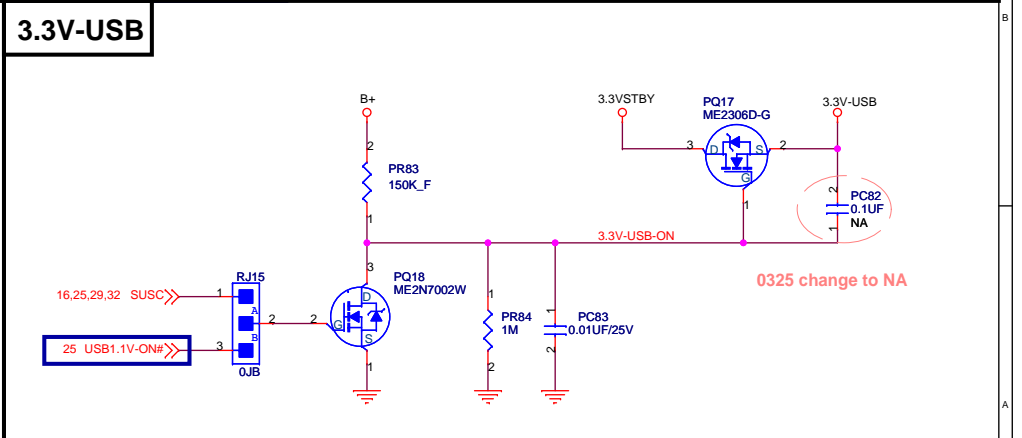
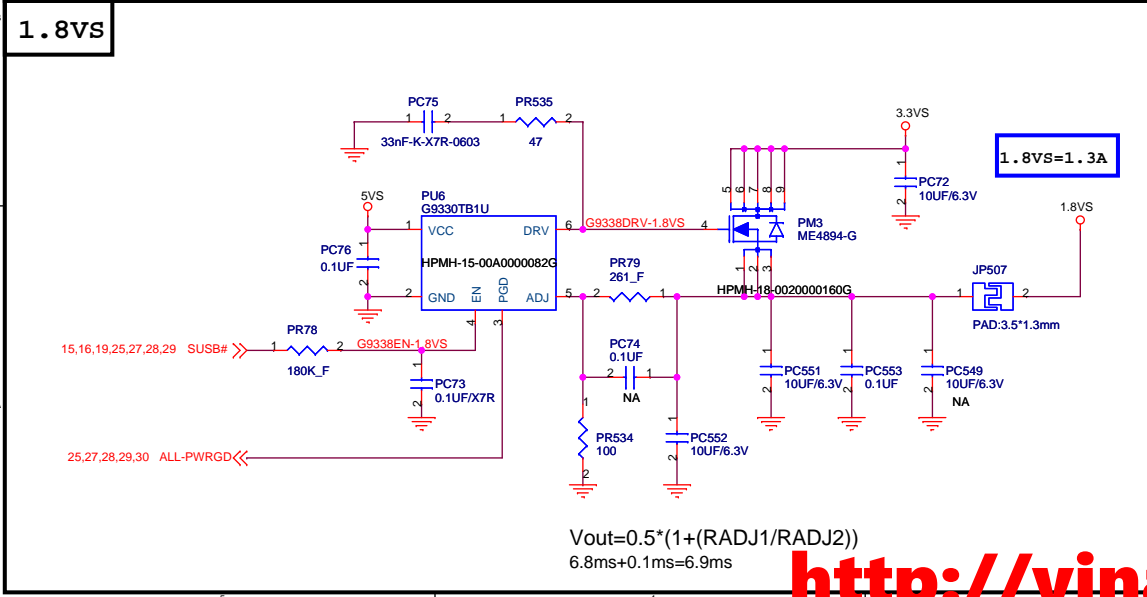
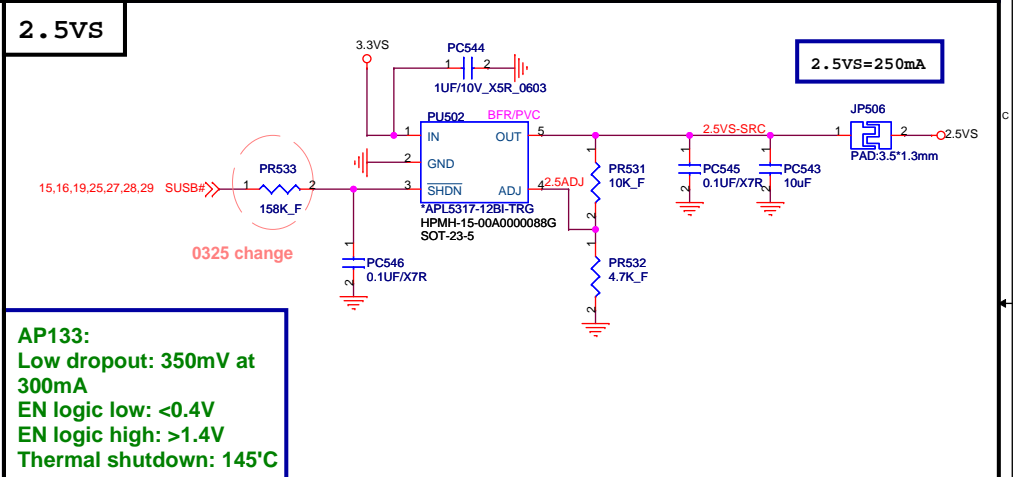
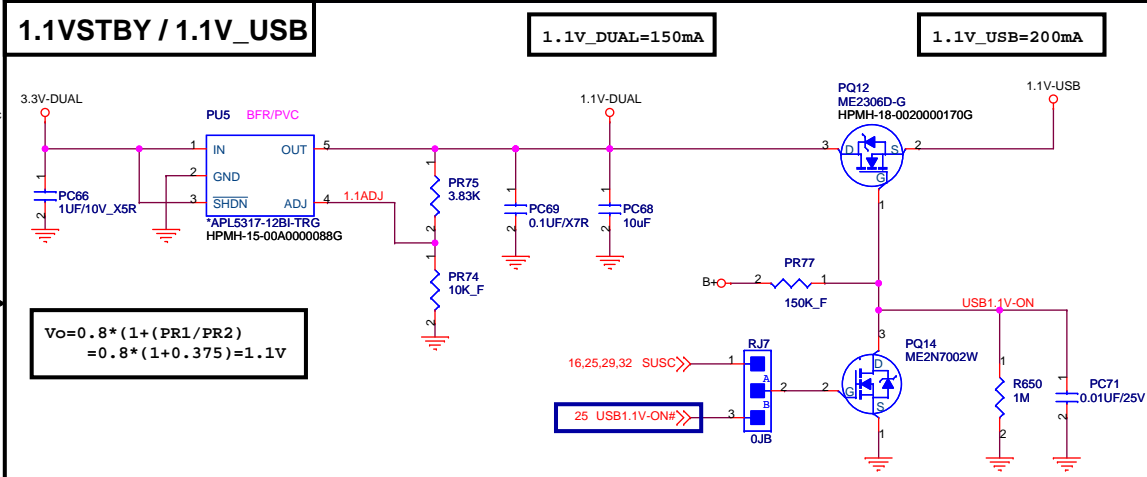
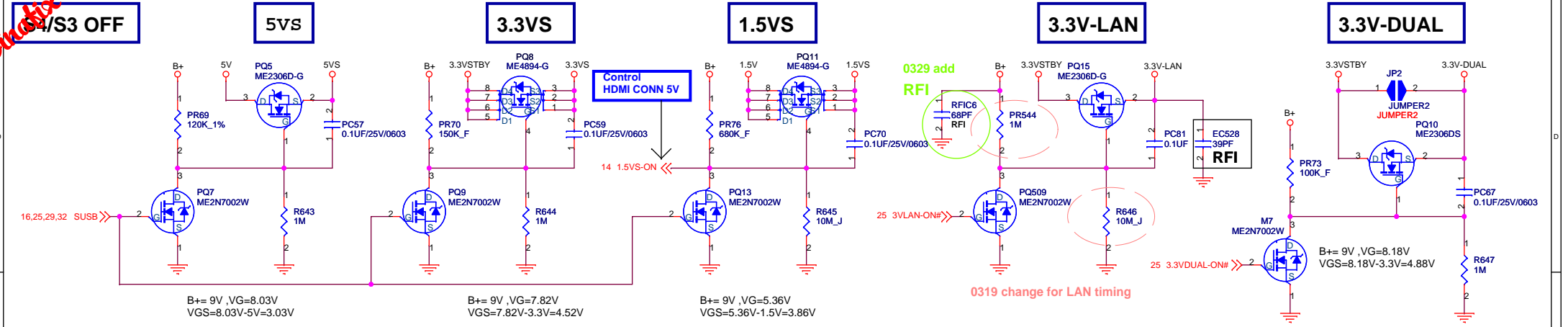
FLEX Computing

Project Name: H311UA1 Title: 5V / 3.3VSTBY

Size: Document Number: HPMH-40GAB5100-D000 Rev: D

Date: Thursday, April 01, 2010 Sheet: 30 of 33

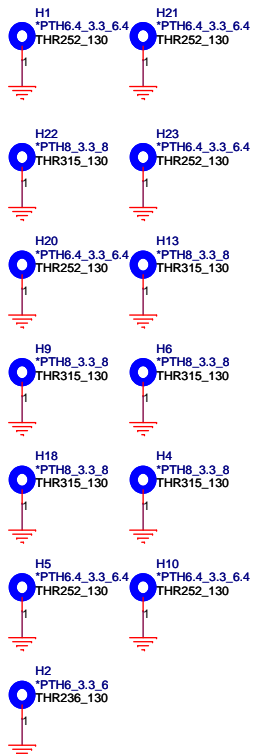
[vinafix](http://vinafix.vn)



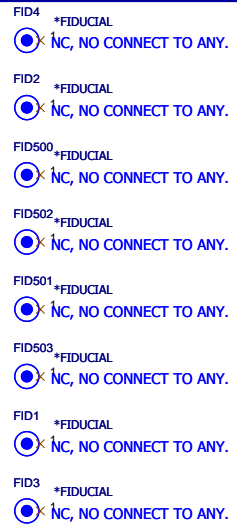
<http://vinafix.vn>

Screw Hole

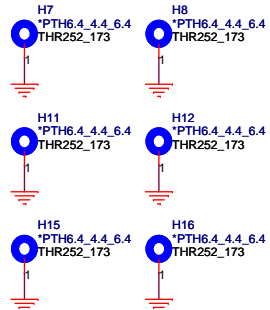
MB x 16



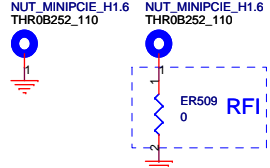
FID



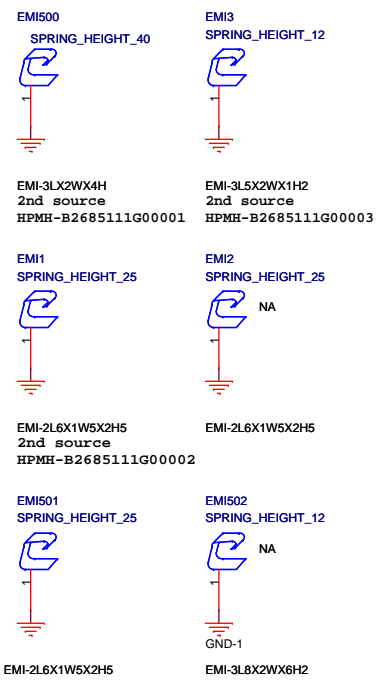
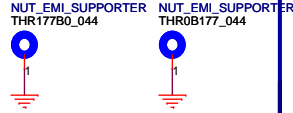
CPU/VGA x 8



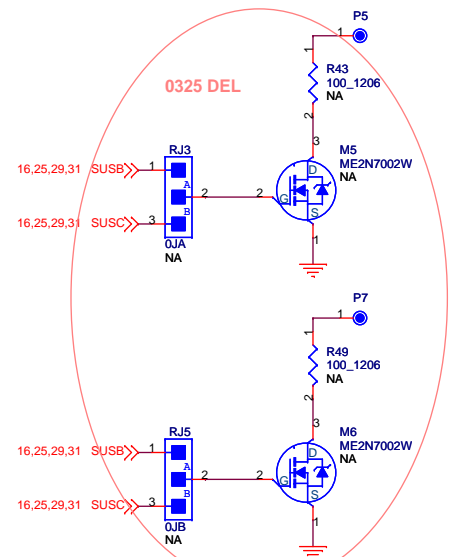
MINI CARD x 2



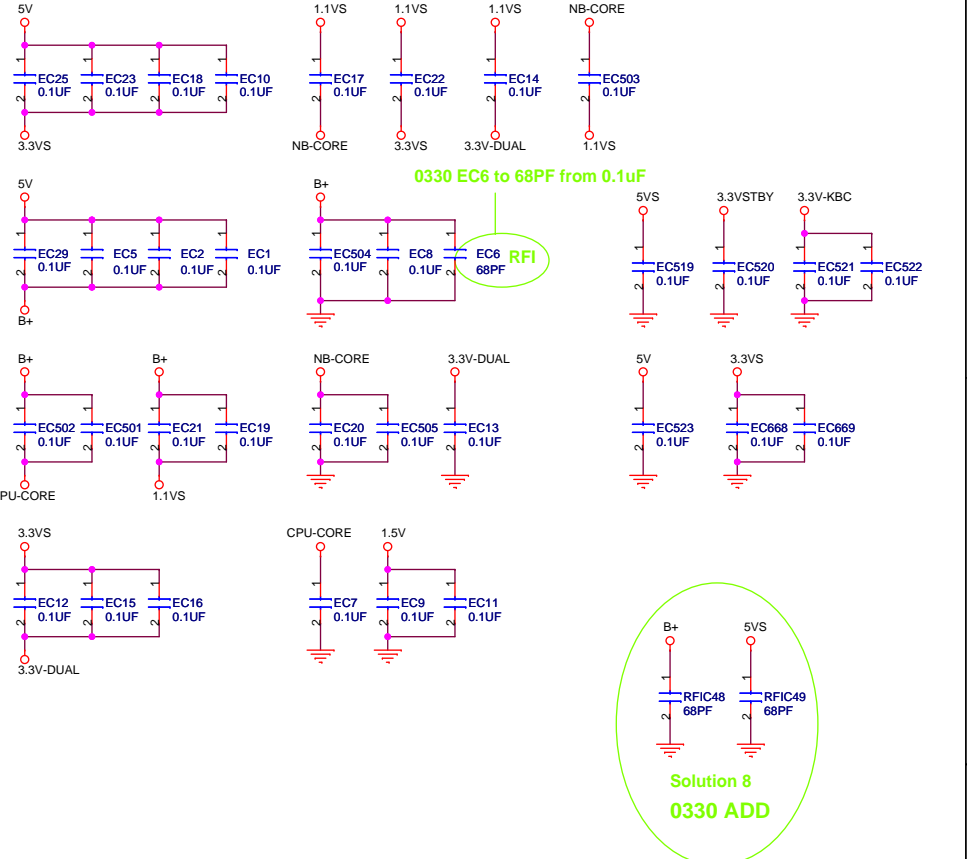
EMI x 2



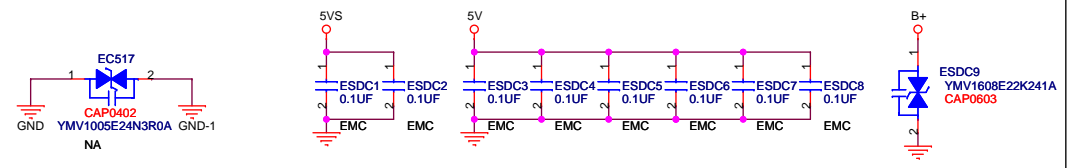
Discharge



EMI Caps



ESD



EE Caps

