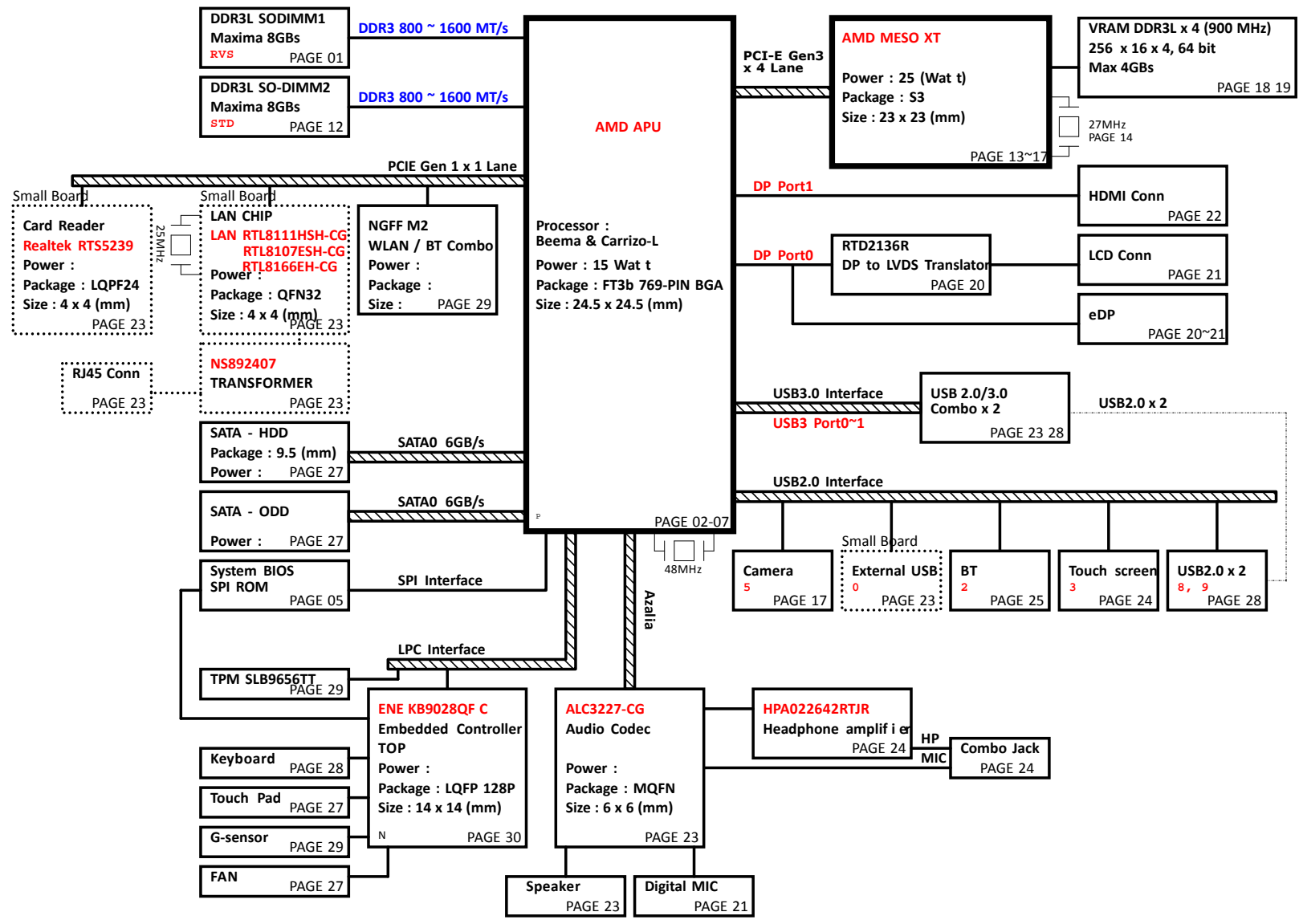


Chocolate AMD Beema DIS/UMA (14.0"/15.6"/17.3")




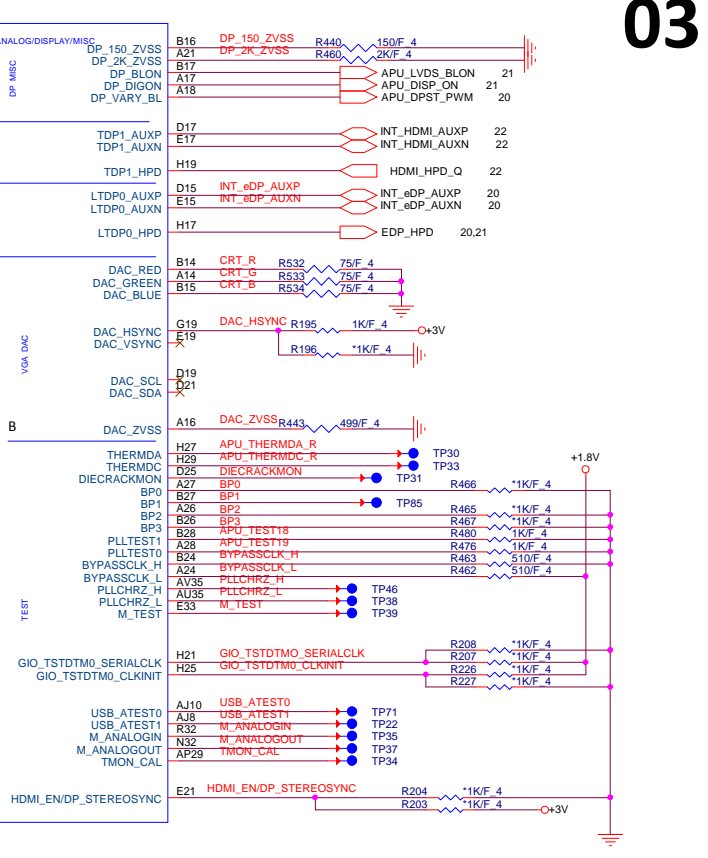
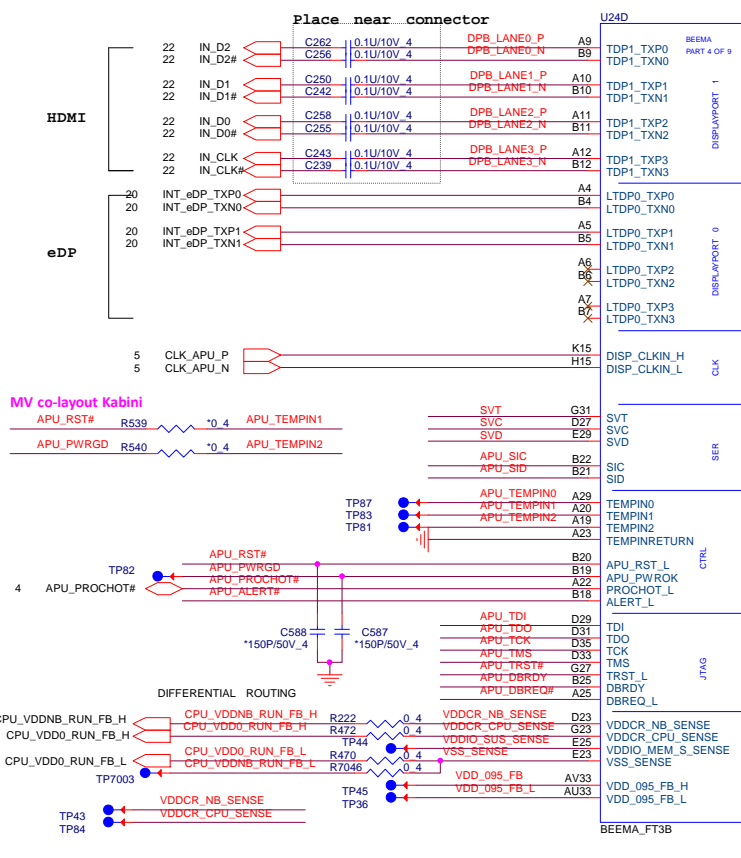
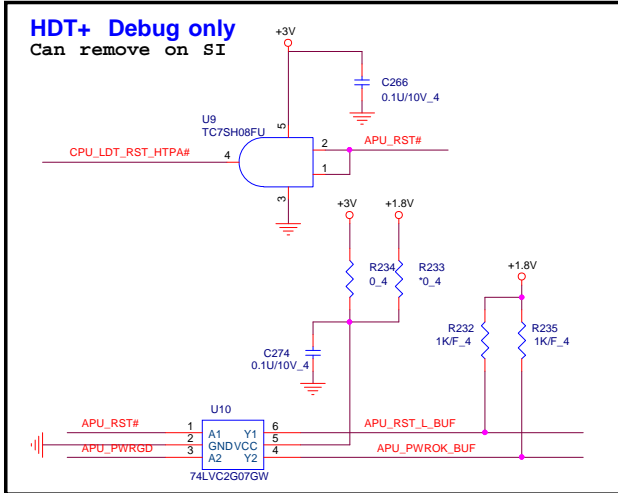
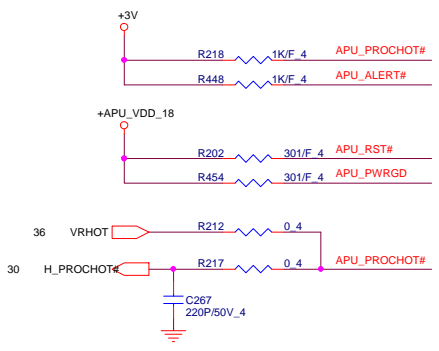
PCB 10L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1 (HIGH)
- LAYER 4 : IN2 (LOW)
- LAYER 5 : SVCC
- LAYER 6 : GND
- LAYER 7 : IN3 (HIGH)
- LAYER 1 : IN4 (HIGH)
- LAYER 1 : GND
- LAYER 1 : BOT

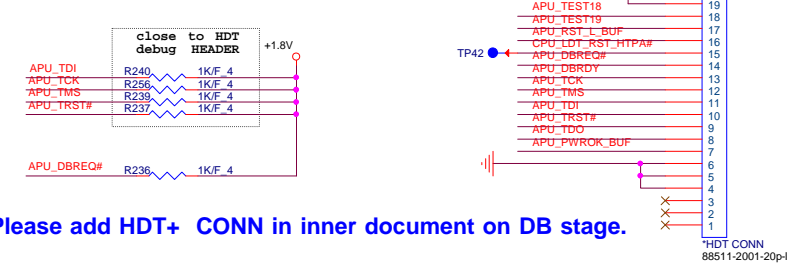
Power Source

- BQ24728H**
System Charge Power (+BATCHG)
PAGE 31
- RT7238B / RT7238C**
System Power (+3VPCU/+5VPCU/+3VS5/+5VS5)
PAGE 32
- RT8231BGQW**
System Memory Power (+1.35VSUS/+0.65V_DDR_VTT)
PAGE 33
- APW8824 / APW8824**
Processor Power (+0.95V5/+1.5V55)
PAGE 34
- AOZ1267Q1-02 / RT8068AZQW**
Processor Power (+0.95V/+1.8V55)
PAGE 35
- ISL62771**
Processor Power (+VCC_CORE/+VDDNB_CORE)
PAGE 36 37
- APL3523A * 3**
Load switch (+3V/+3VLANVCC/+5V/+3VSUS/+1.5V/+1.8V)
PAGE 38
- RT8899AGQW**
DGPU Power (+VGA_CORE/+1.35V_VGA)
PAGE 38 40
- RT8068A / APL3523A**
DGPU Power (+0.95V_VGA/+1.8V_VGA/+3V_VGA)
PAGE 41

	PROJECT : X22		
	Quanta Computer Inc.		
Size	Document Number	Rev	
NB5/RD3	Block Diagram	1A	
Date: Tuesday, November 18, 2014 Sheet 1 of 41			

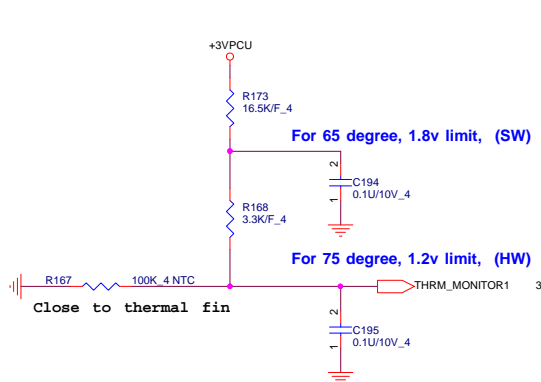


HDT+ Connector for Debug only

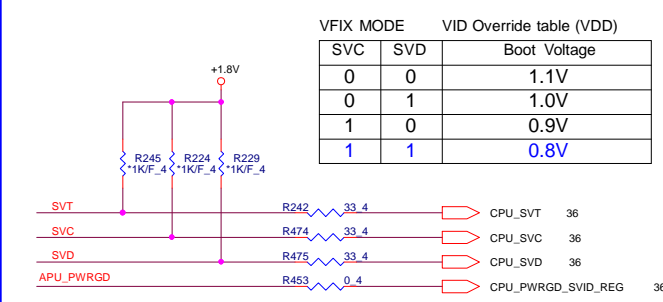


Please add HDT+ CONN in inner document on DB stage.

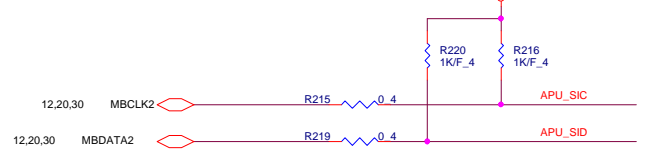
IO Thermal Protect



Serial VID

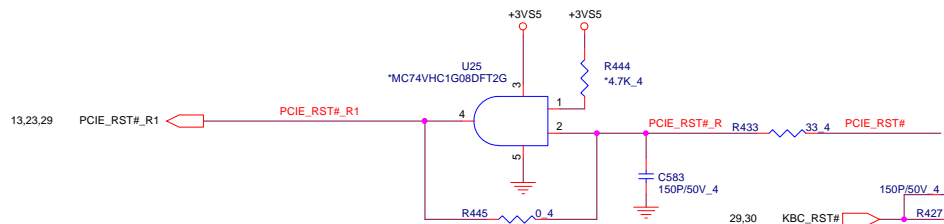


Thermal Sensor



PROJECT : Y2x
Quanta Computer Inc.

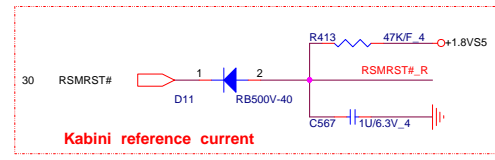
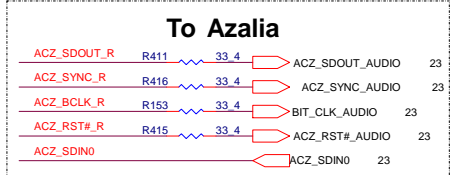
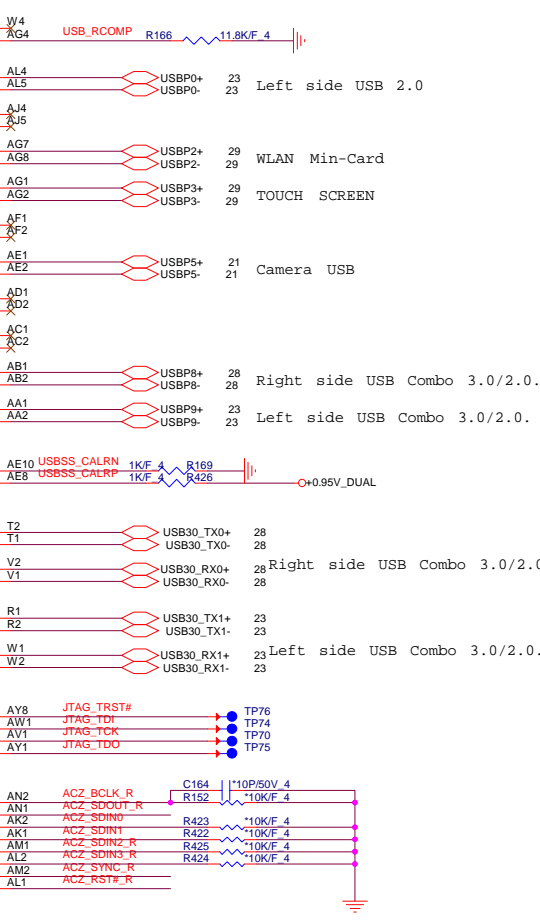
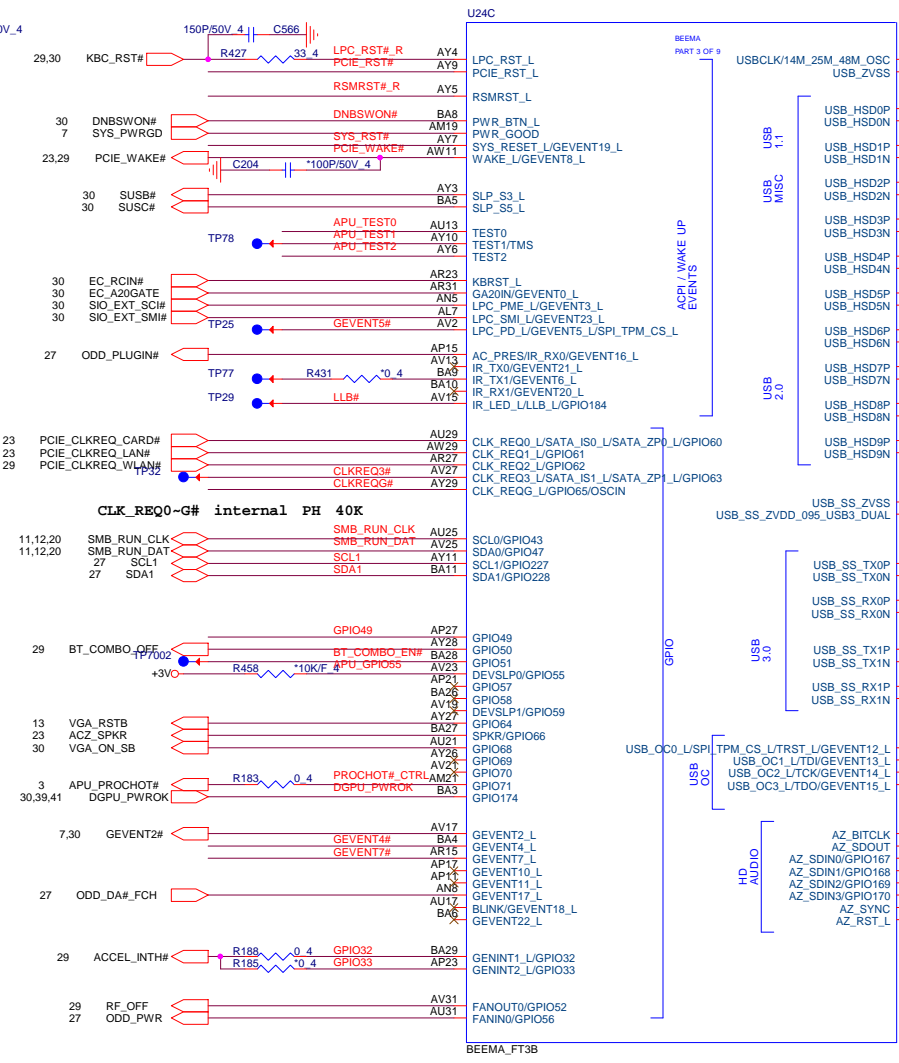
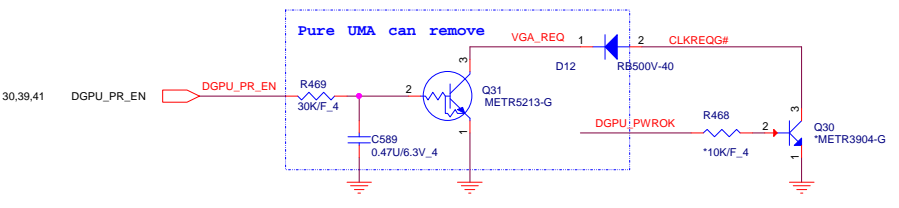
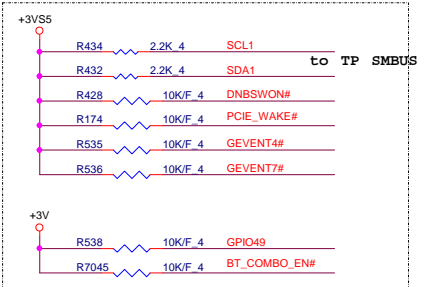
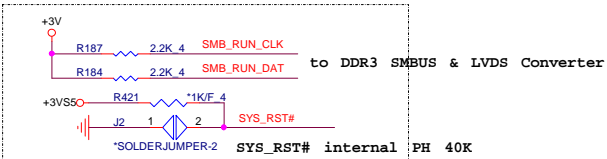
Size	Document Number	Rev
	DISMI (2/6)	1A
Date: Tuesday, November 18, 2014 Sheet 3 of 41		



NC, no install by default

R171 *1K/F 4 APU_TEST0 R172 15K/F 4
 R436 *1K/F 4 APU_TEST1 R435 15K/F 4
 R414 *1K/F 4 APU_TEST2 R420 15K/F 4

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



BOARD ID SETTING

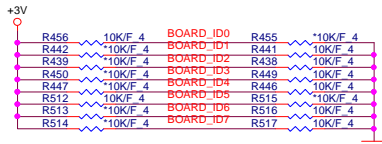
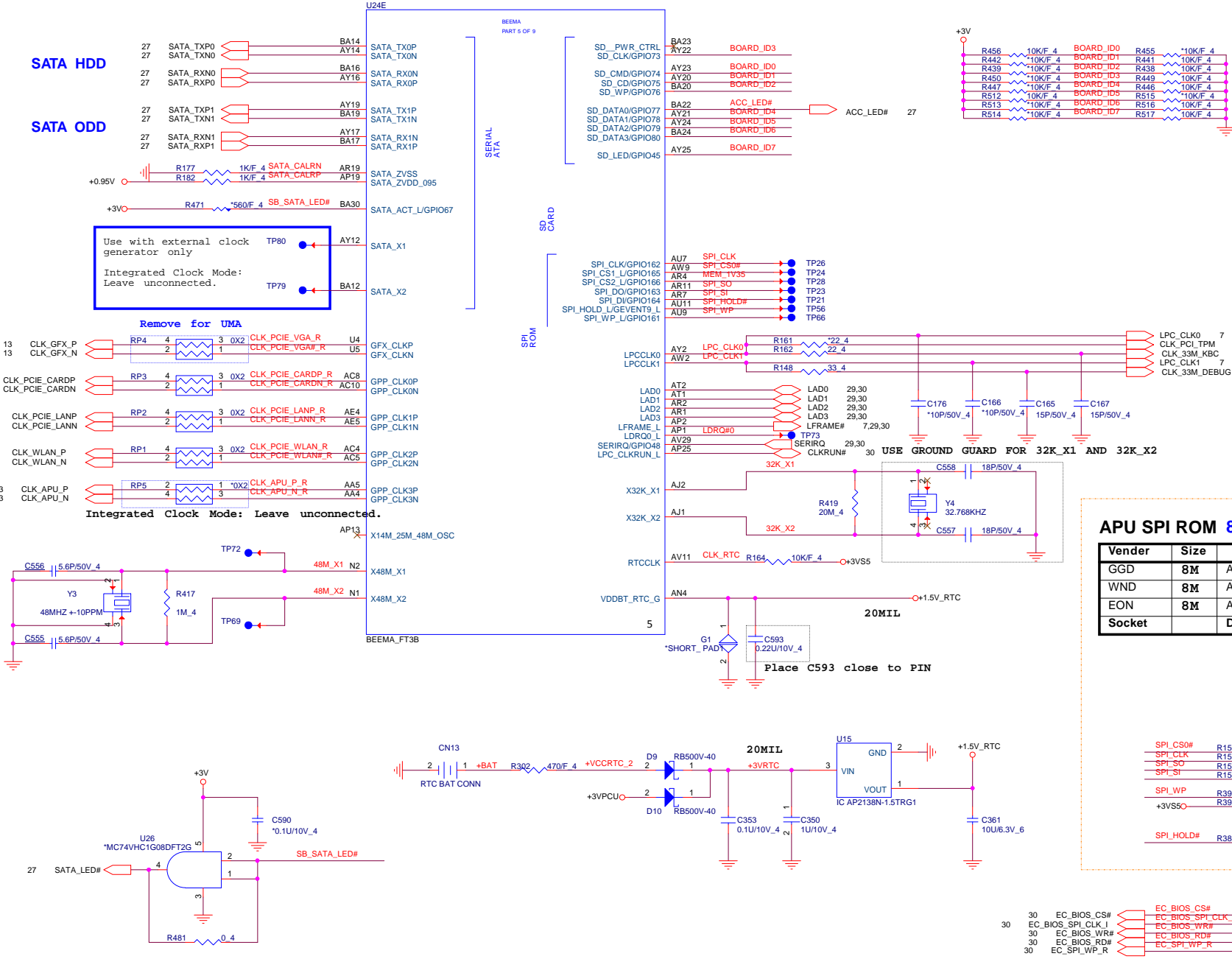
Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve

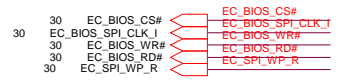
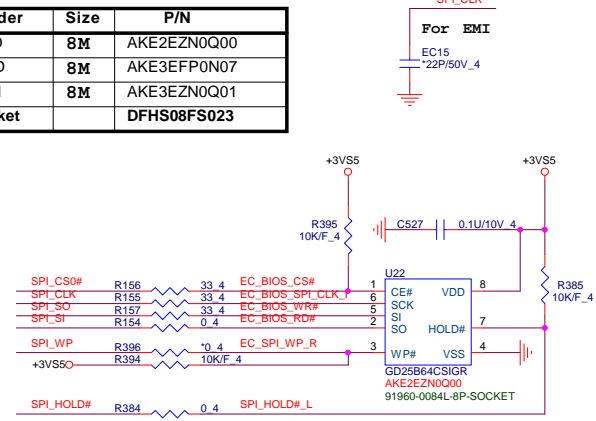
Board ID [5]	Definition
0	Beema
1	Carrizo-L

Board ID [7:6]	Definition
000	Reserve



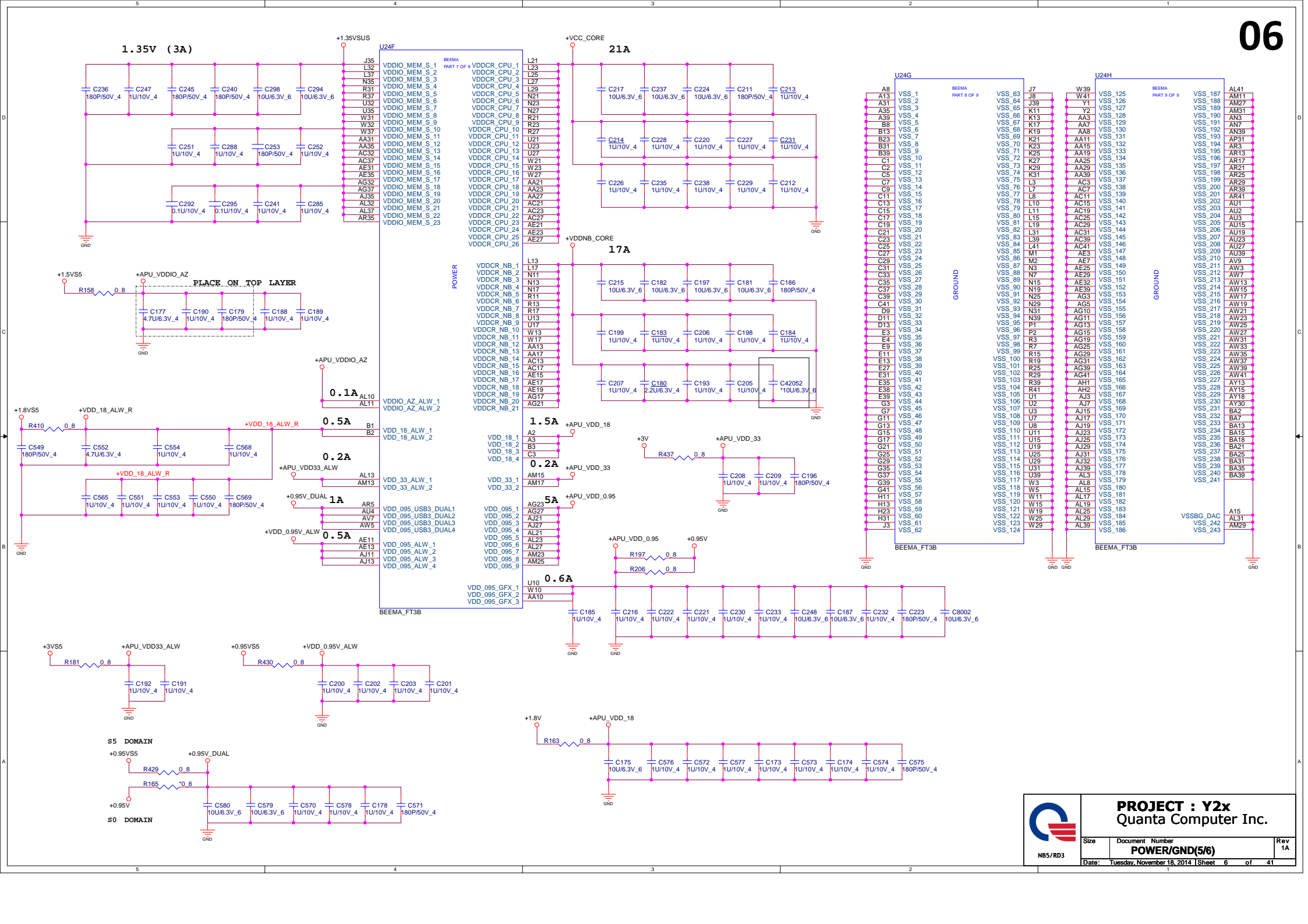
APU SPI ROM 8M SPI EC ROM

Vender	Size	P/N
GGD	8M	AKE2EZN0Q00
WND	8M	AKE3EFP0N07
EON	8M	AKE3EZN0Q01
Socket		DFHS08FS023



PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number SATA/CLK (4/6)	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 5 of 41		



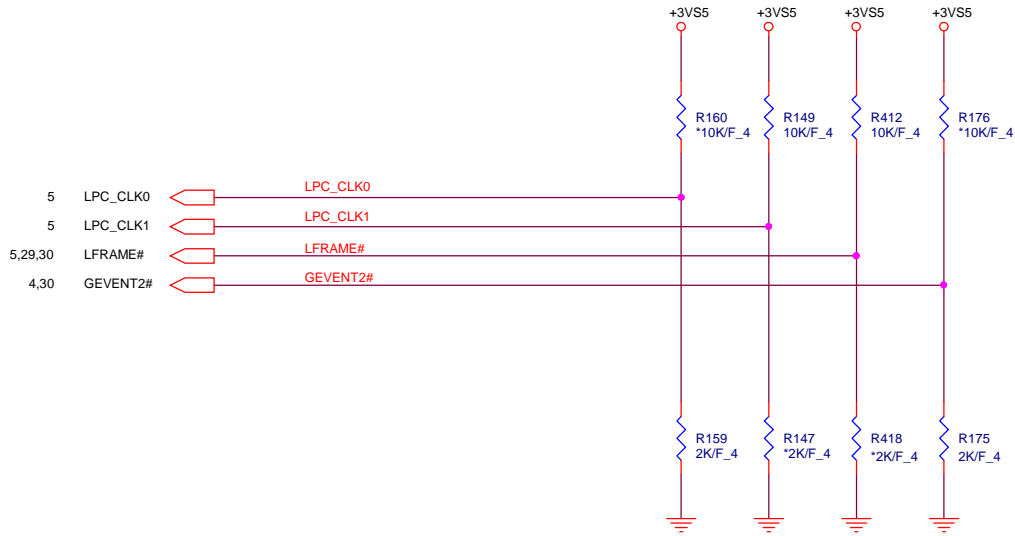
PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
NB5/RD3	POWER/GND(5/6)	1A
Date:	Tuesday, November 18, 2014	Sheet 6 of 41

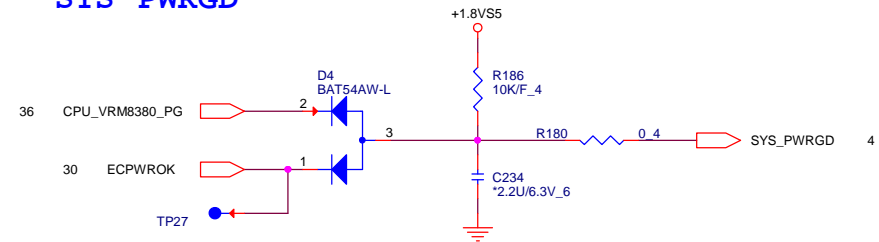


STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



SYS_PWRGD



REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

<p>NB5/RD3</p>	<p>PROJECT : Y2x Quanta Computer Inc.</p>	
	<p>Size</p>	<p>Document Number STRAP (6/6)</p>
<p>Date: Tuesday, November 18, 2014 Sheet 7 of 41</p>		



NB5

PROJECT : Y71
Quanta Computer Inc.

Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 8 of 41		



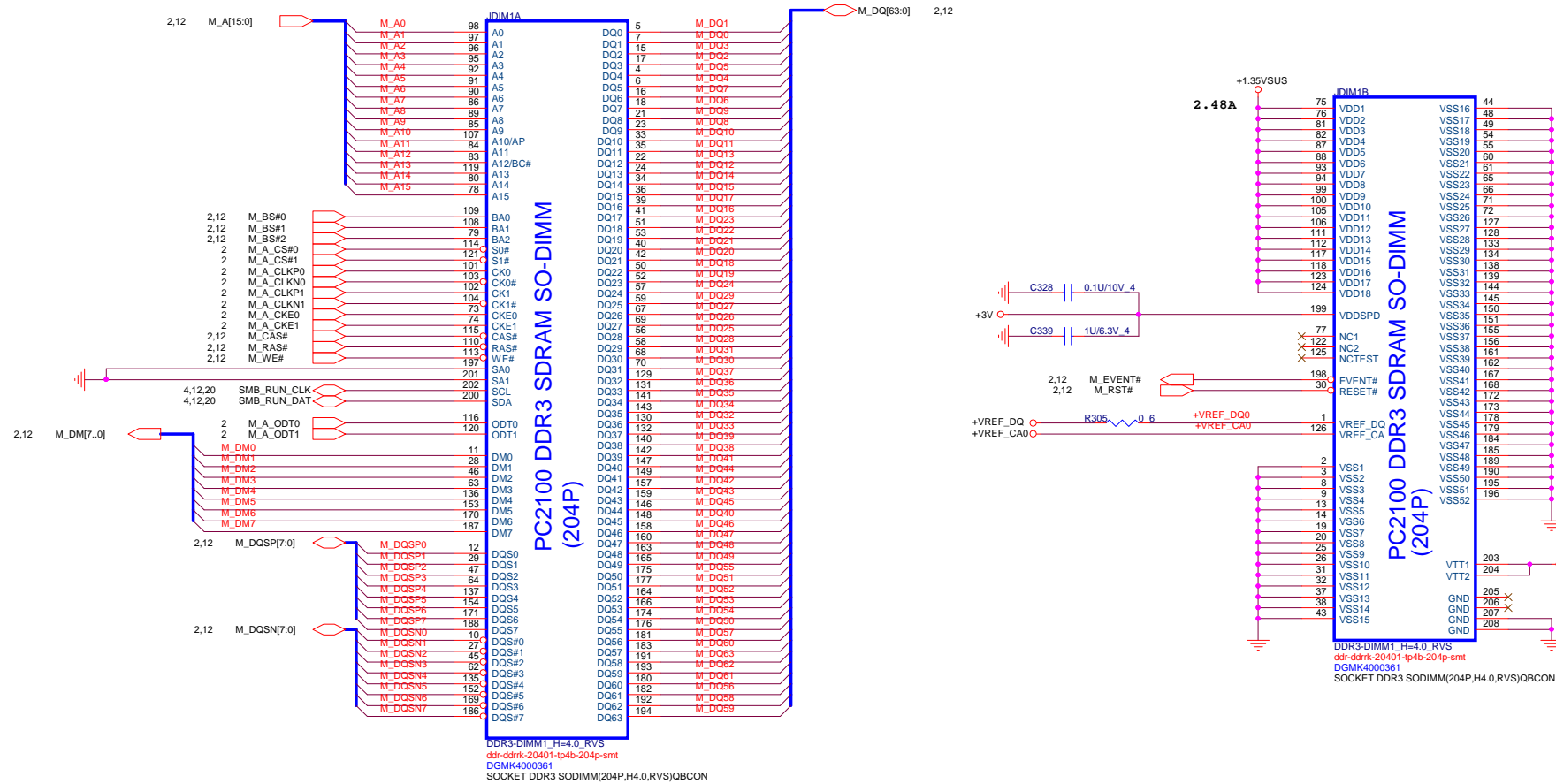
PROJECT : Y71
Quanta Computer Inc.

Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 9 of 41		

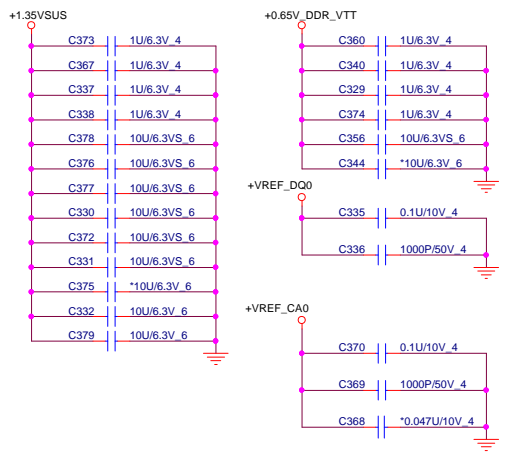


PROJECT : Y71
Quanta Computer Inc.

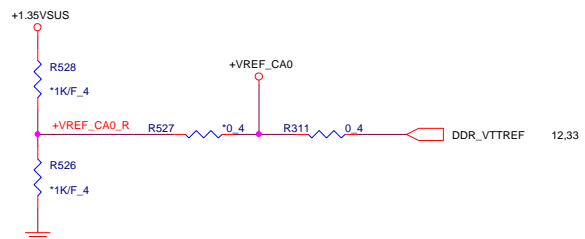
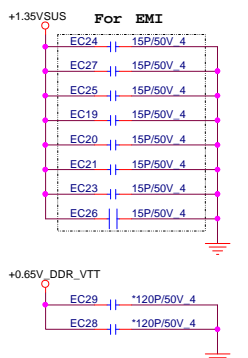
Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 10 of 41		



Place these Caps near So-Dimm0.

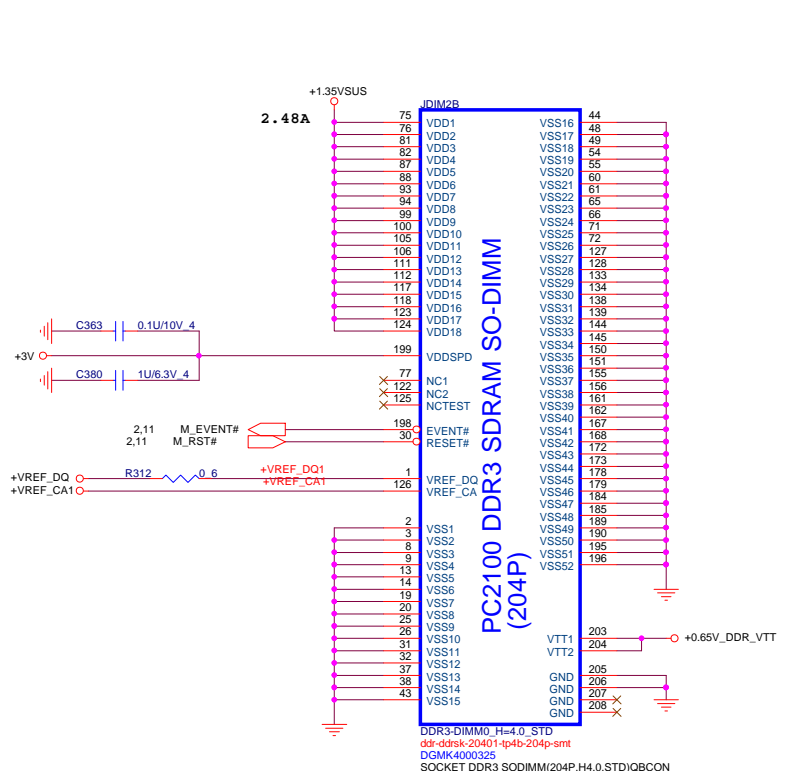
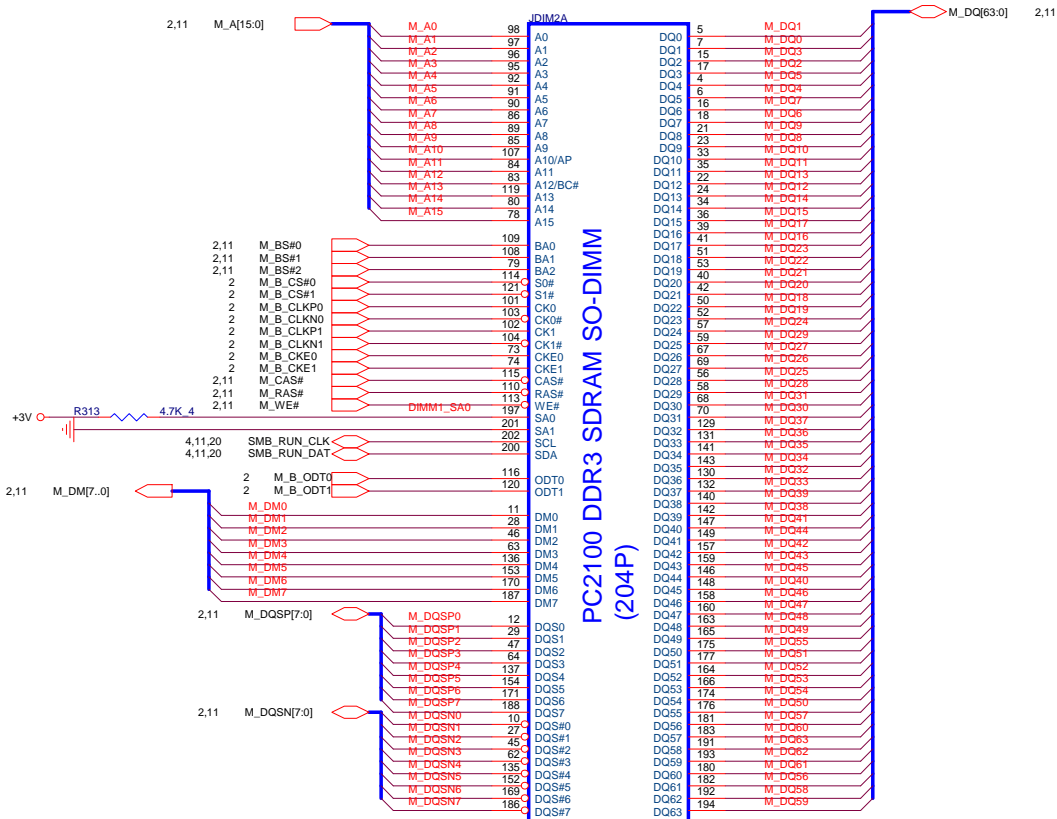


For EMI



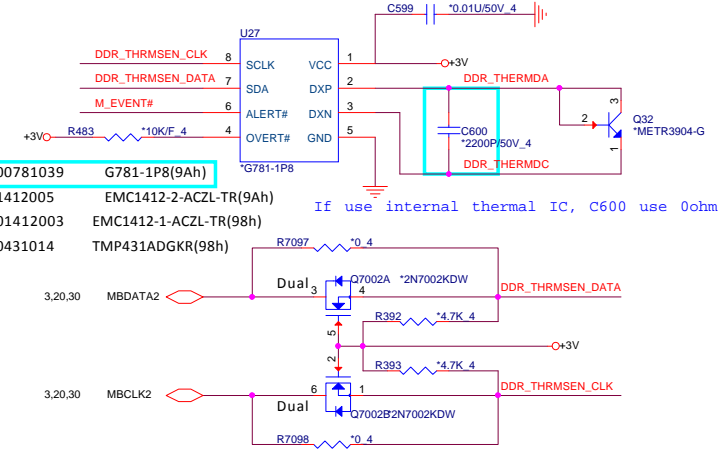
PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RV5 (4.0H)	1A
Date: Tuesday, November 18, 2014 Sheet 11 of 41		




DDR3-DIMM0_H=4.0 STD
 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000325
 SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCCN

Local Thermal Sensor For DDR3



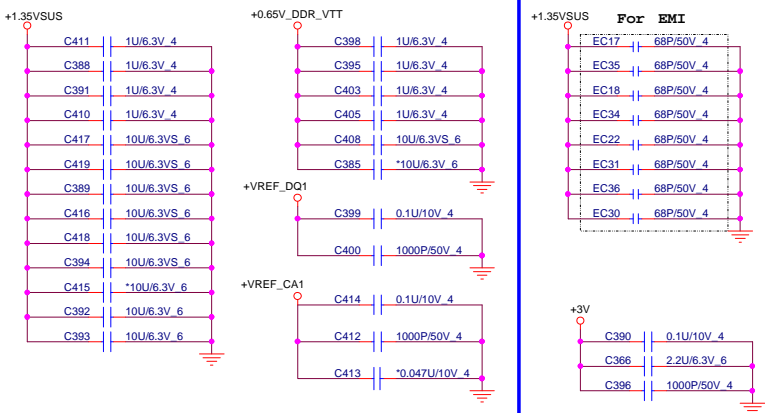
- Main:AL000781039 G781-1P8(9Ah)
- 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
- Main:AL001412003 EMC1412-1-ACZL-TR(98h)
- 2nd:AL000431014 TMP431ADGKR(98h)



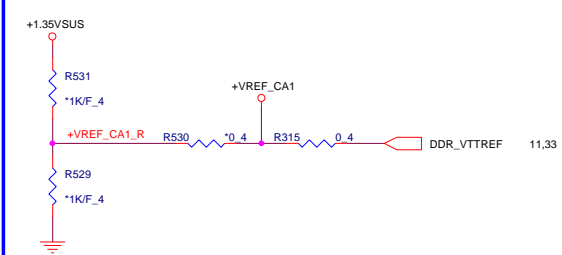
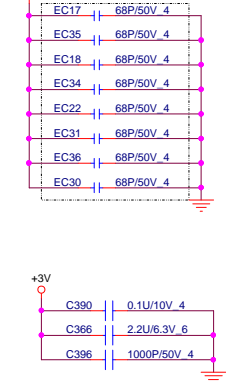
PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
NB5/RD3	DDR3 DIMM1-STD (4.0H)	1A
Date: Tuesday, November 18, 2014 Sheet 12 of 41		

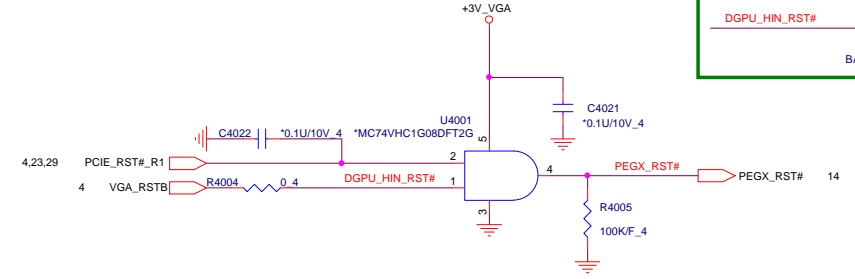
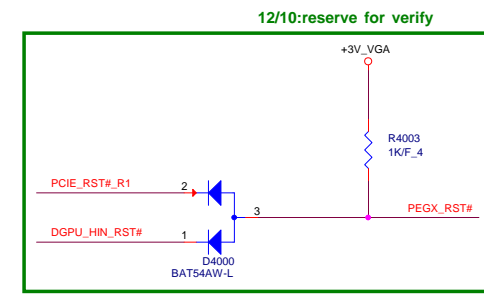
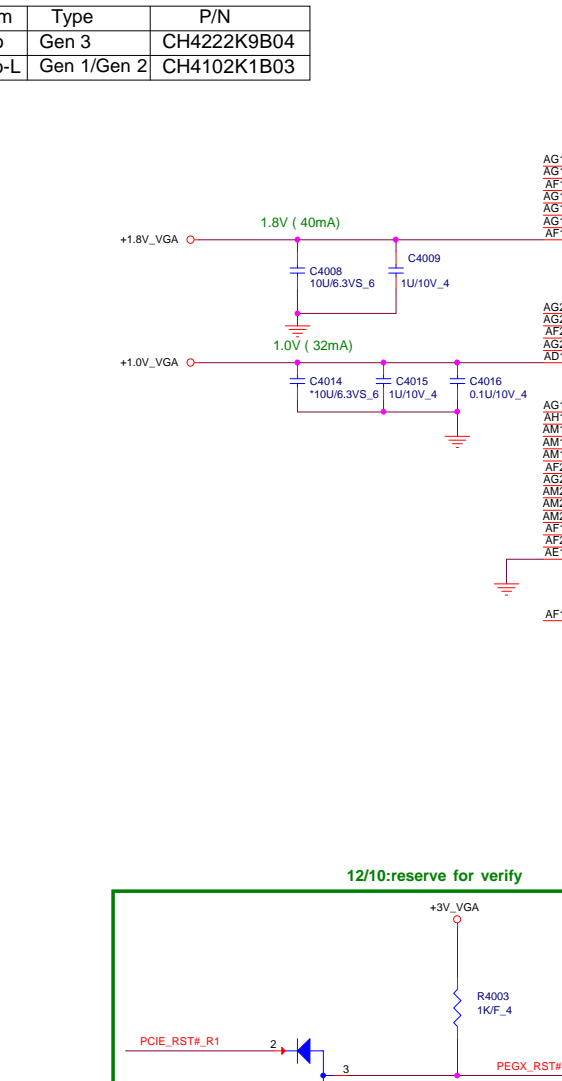
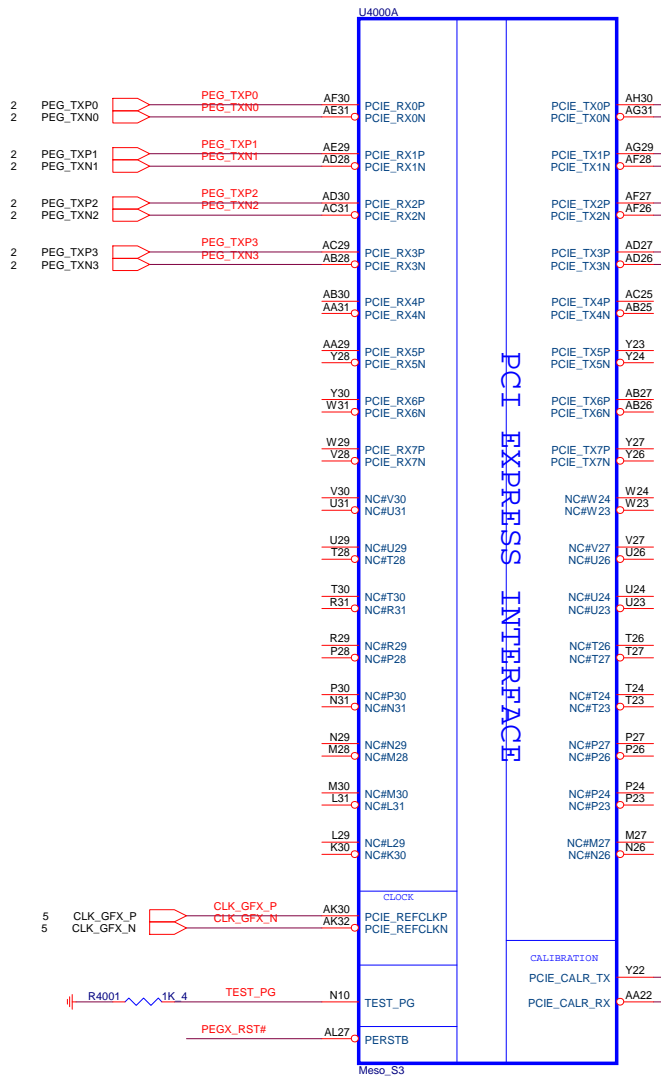
Place these Caps near So-Dimm1.



For EMI

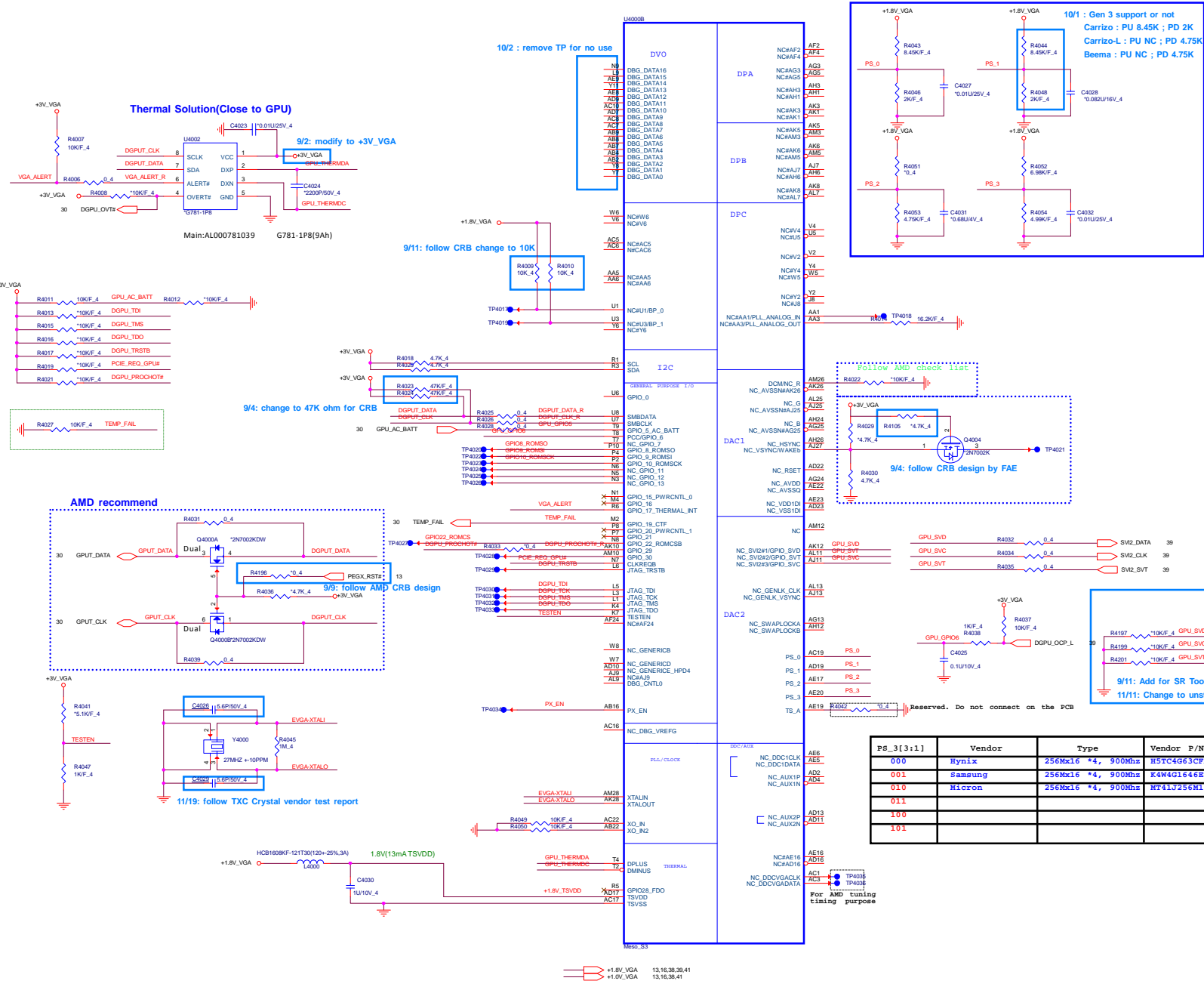


Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03



- 14,16,38,41 +3V_VGA
- 14,16,38,39,41 +1.8V_VGA
- 16,38,41 +1.0V_VGA

	PROJECT : X22		
	Quanta Computer Inc.		
Size	Document Number	Rev 1A	
NB5/RD3	MESO_S3 PCIE/DP power		
Tuesday, November 18, 2014		Sheet	13 of 43



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (pF)	0805 (3,4)	R _{pu} (Ohm)	R _{pd} (Ohm)	BIB(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5630	101
		3400	10000	110
		4750	NC	111

Resistor Divider Lookup Table

C (pF)	0805 (3,4)	R _{pu} (Ohm)	R _{pd} (Ohm)	BIB(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5630	101
		3400	10000	110
		4750	NC	111

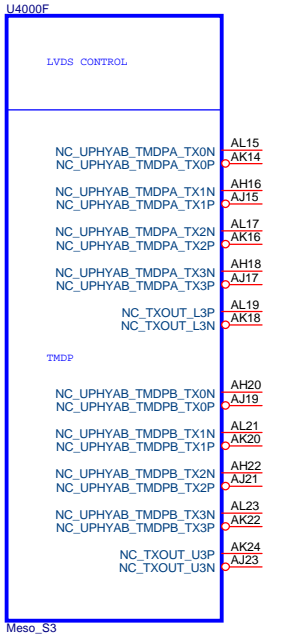
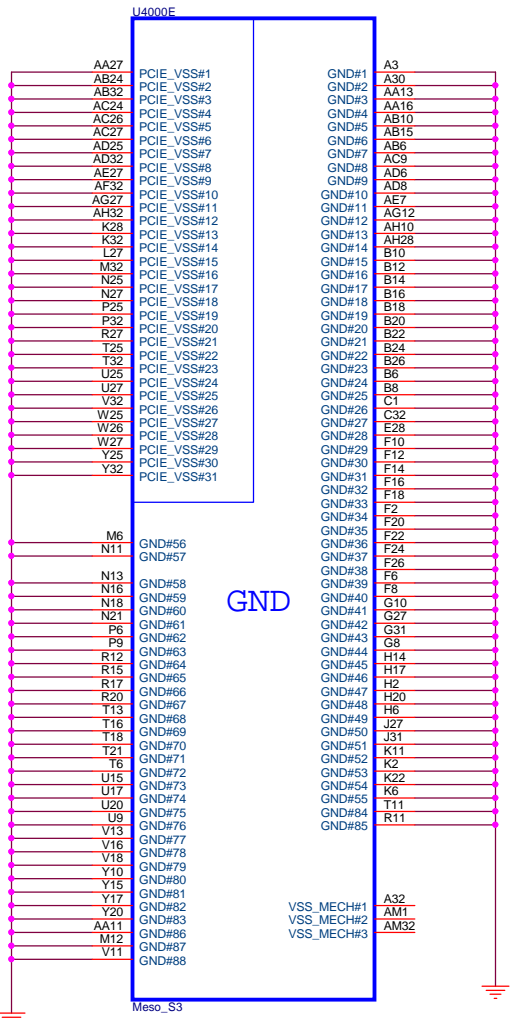
MLPS Circuit

PS_0, PS_1, PS_2, PS_3

BIT5 => BIT0

PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

MLPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG[0]	If STRAP BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_012	ROM_CONFIG[1]	If STRAP BIOS_ROM_EN = 0, ROM_CONFIG[0] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29)	Design dependent, see the description.
PS_013	ROM_CONFIG[2]		Design dependent, see the description.
PS_041	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_015	N/A	Reserved.	1
PS_111	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_112	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_113	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_114	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_115	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_211	N/A	Reserved.	0
PS_212	N/A	Reserved.	0
PS_213	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_214	N/A	Reserved.	1
PS_215	N/A	Reserved	1
PS_311	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID device.	Design dependent, see the description.
PS_312	BOARD_CONFIG[1]		Design dependent, see the description.
PS_313	BOARD_CONFIG[2]		Design dependent, see the description.
PS_314	N/A	Reserved.	1
PS_315	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

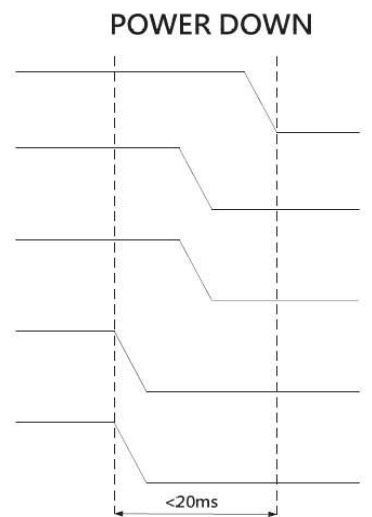
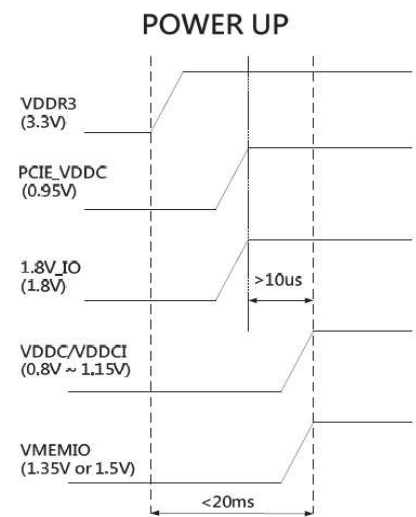
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	x
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYS	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

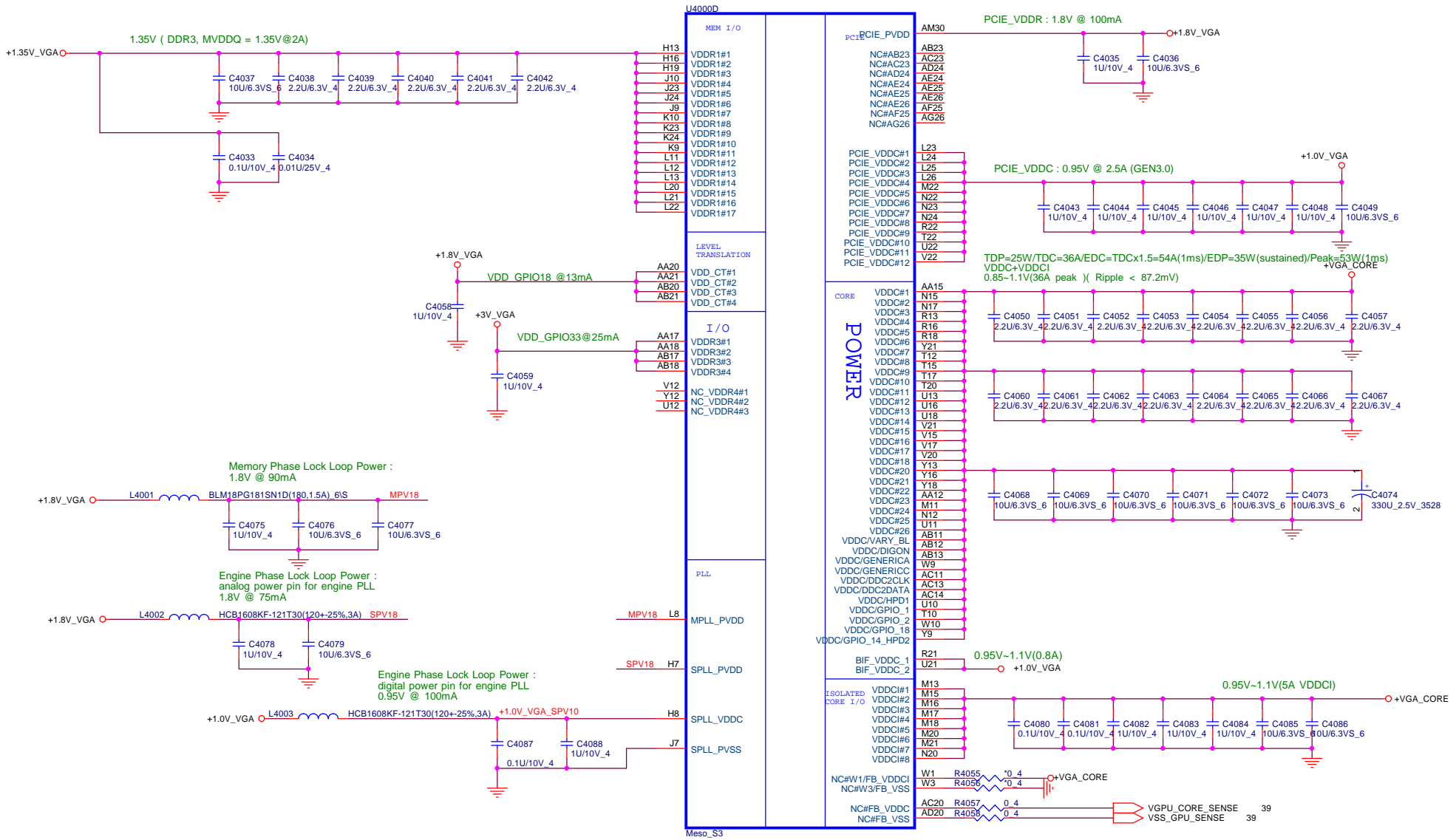
POWER UP / POWER DOWN SEQUENCE



PROJECT : X22
Quanta Computer Inc.

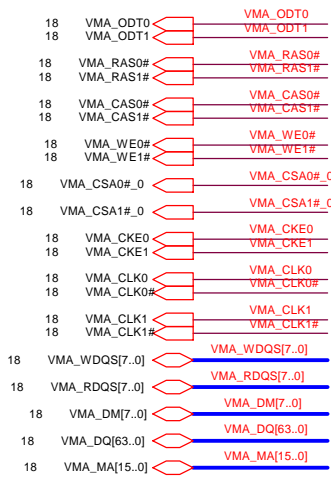
Size	Document Number	Rev
	MESO_S3_GND/LVDS/Strap	1A
Date:	Tuesday, November 18, 2014 1 Sheet	15 of 43

NB5/RD3

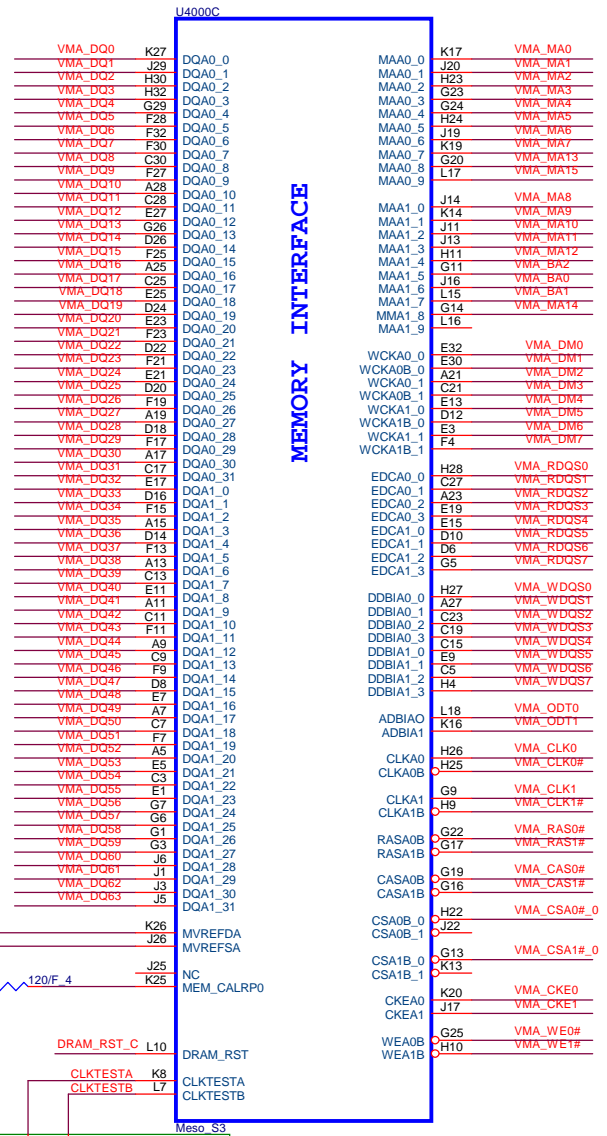


- +1.35V_VGA 17,18,38,39
- +1.8V_VGA 13,14,38,39,41
- +1.0V_VGA 13,38,41
- +VGA_CORE 38,39,40

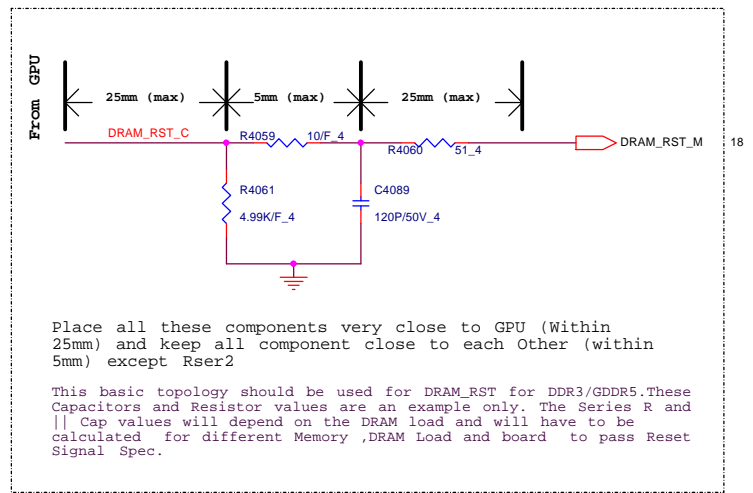
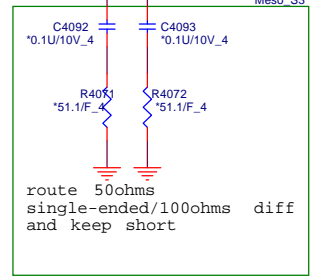
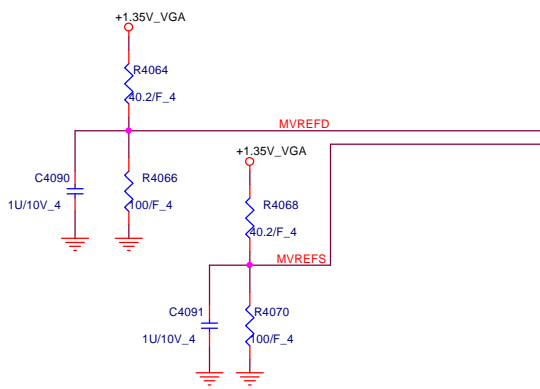
	PROJECT : X22		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	MESO_S3 Power	1A	
Date:	Tuesday, November 18, 2014	Sheet	16 of 43



support 1Gbit
VRAM (64M X 16)



MEMORY INTERFACE



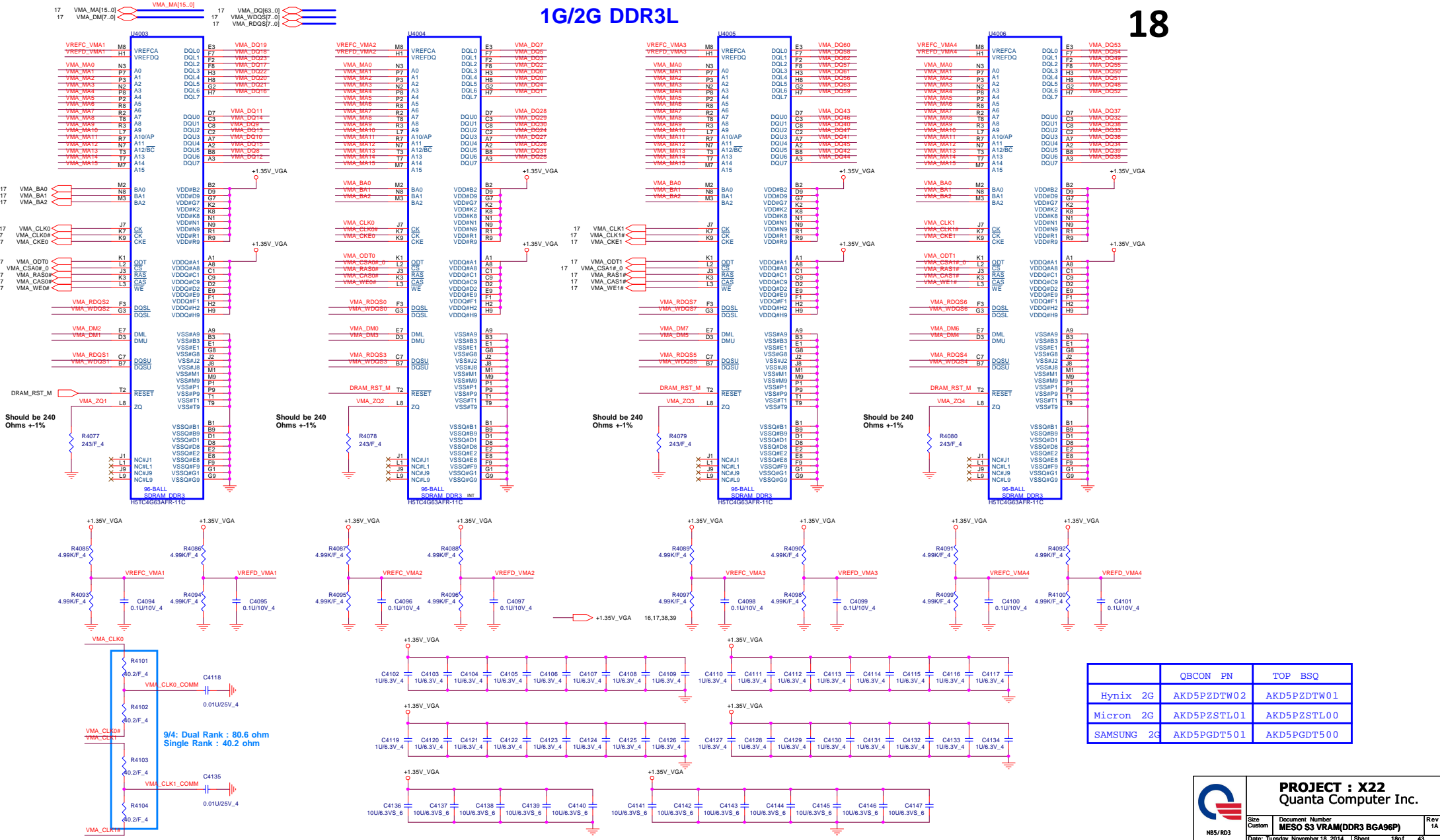
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM Load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

	PROJECT : X22		Rev 1A
	Quanta Computer Inc.		
Size	Document Number		17 of 43
	MESO_S3_MEM_Interface		
Date:	Tuesday, November 18, 2014 Sheet		

1G/2G DDR3L


18



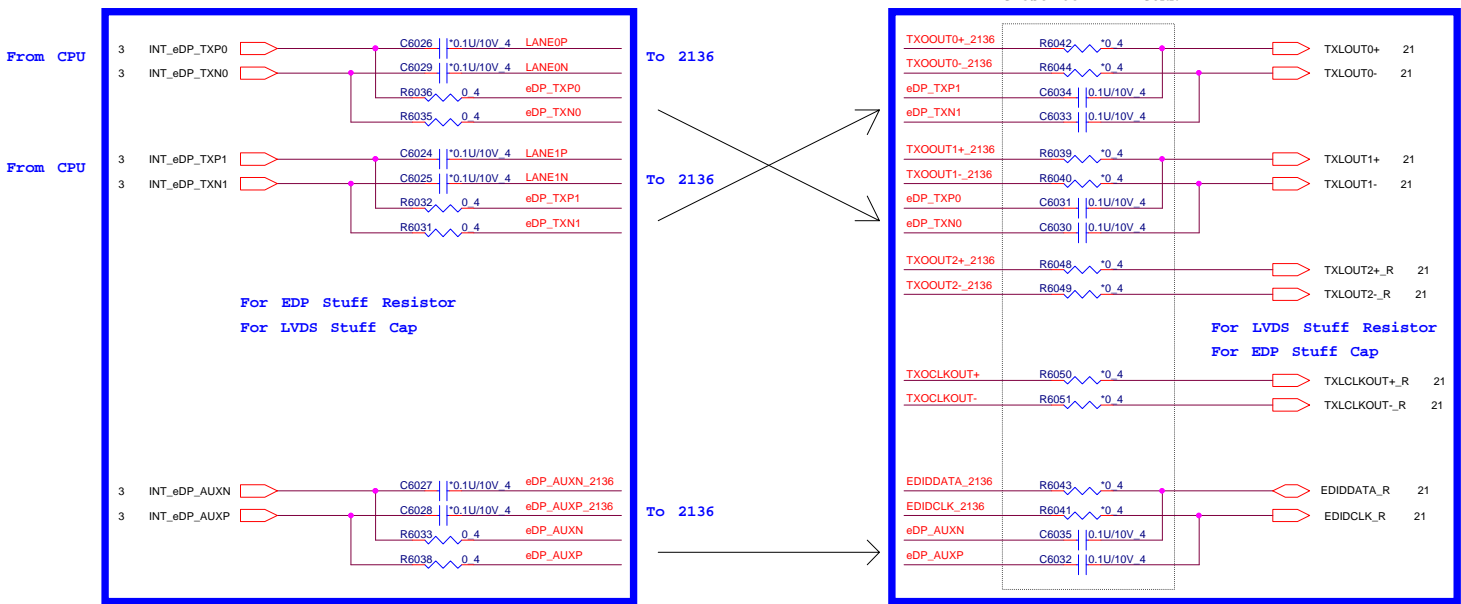
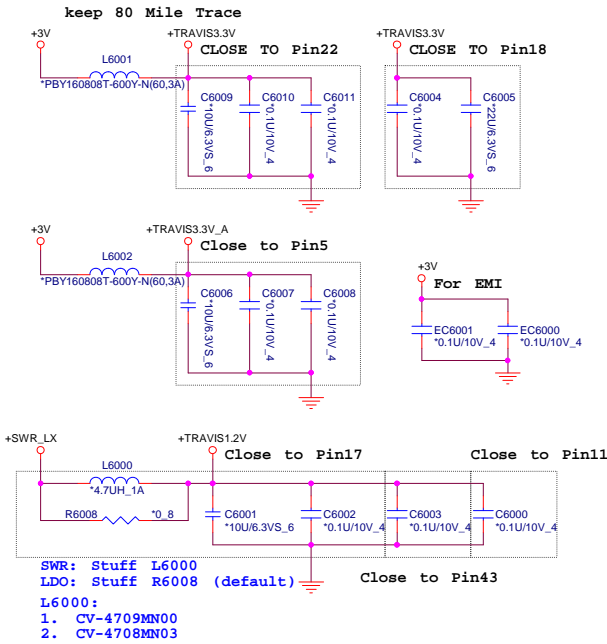
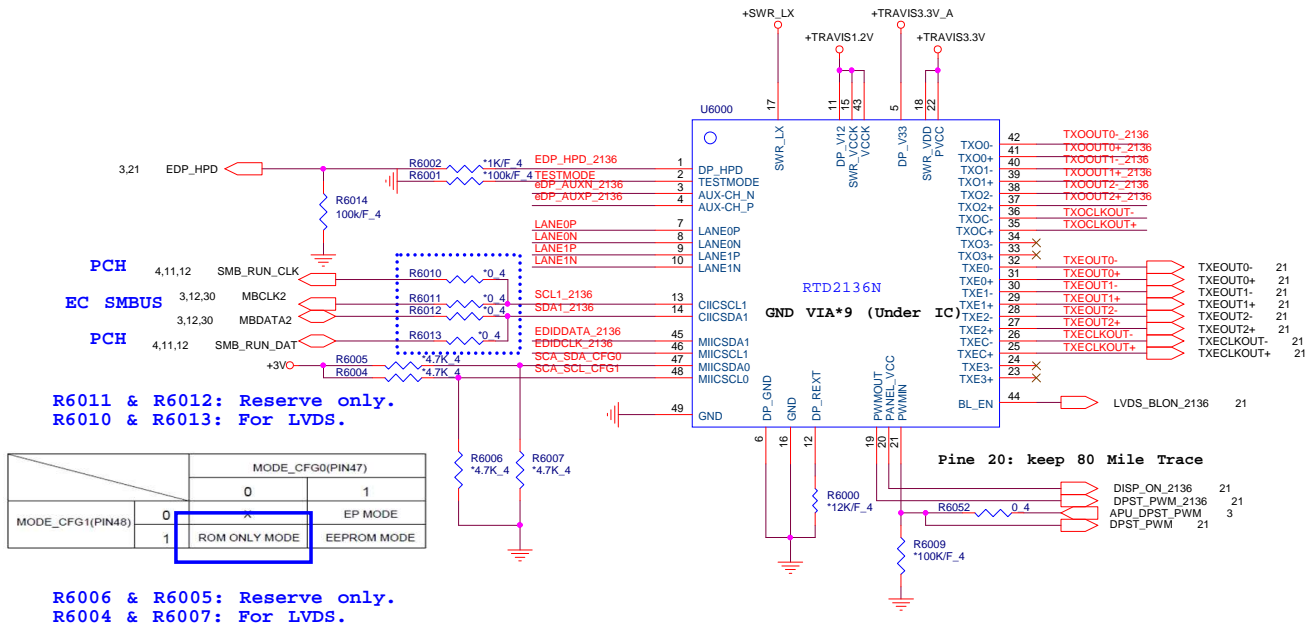
	QBCON PN	TOP BSQ
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

PROJECT : X22
Quanta Computer Inc.

Size: Custom	Document Number: MESO S3 VRAM(DDR3 BGA96P)	Rev: 1A
Date: Tuesday, November 18, 2014		Sheet: 18 of 43

 NBS/RD3	PROJECT : X22 Quanta Computer Inc.		
	Size Custom	Document Number MESO S3 VRAM(DDR3 BGA96P)	Rev 1A
	Date: Tuesday, November 18, 2014 Sheet 19 of 43		

Pine 15/17: keep 20 Mile Trace
 Pine 18: keep 80 Mile Trace

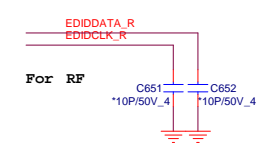
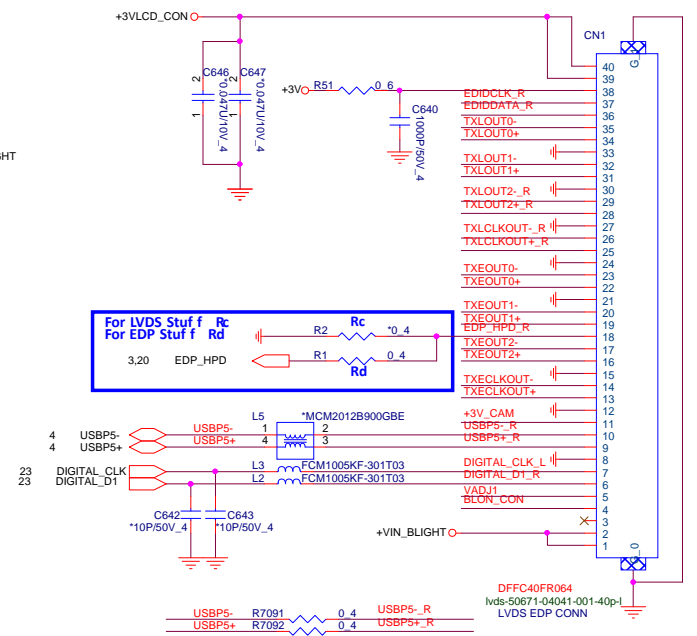
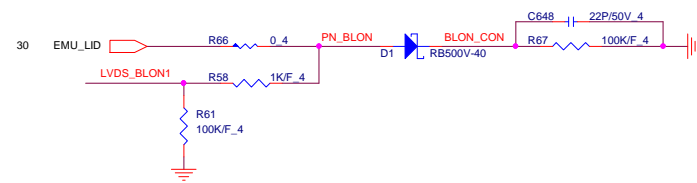
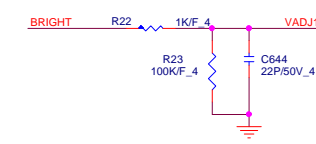
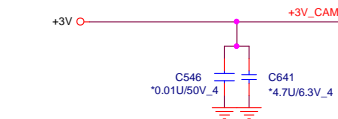
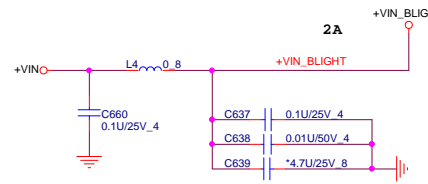
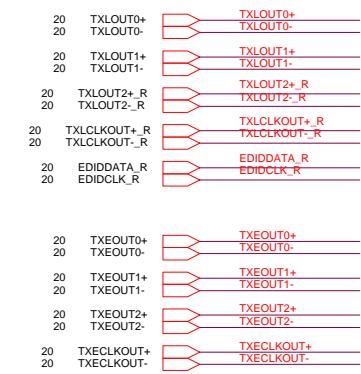
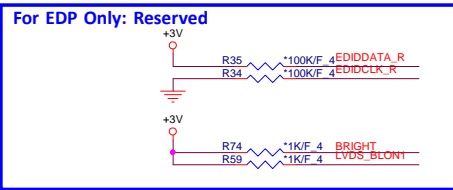
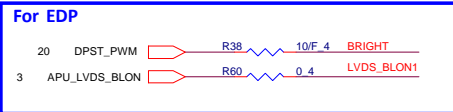
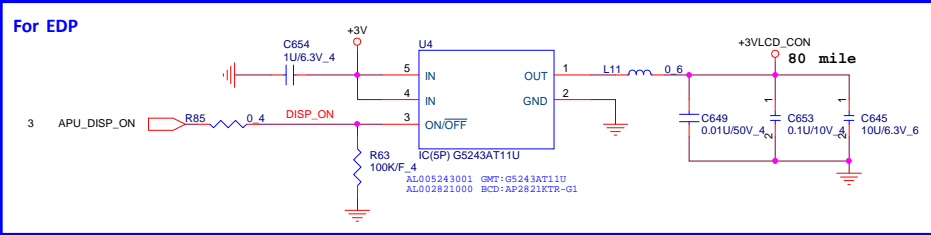
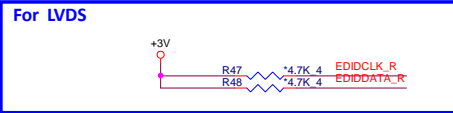
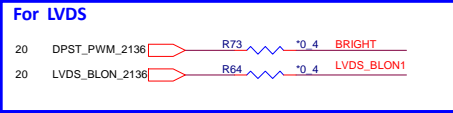
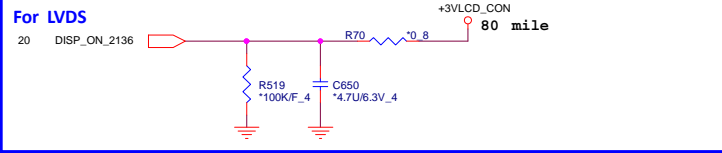


Note.
 14" & 15" only eDP panel.
 17" have both LVDS & eDP panel.

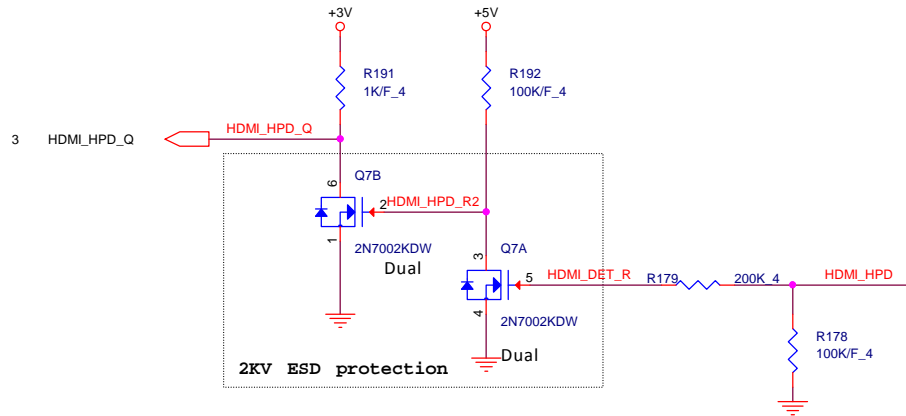
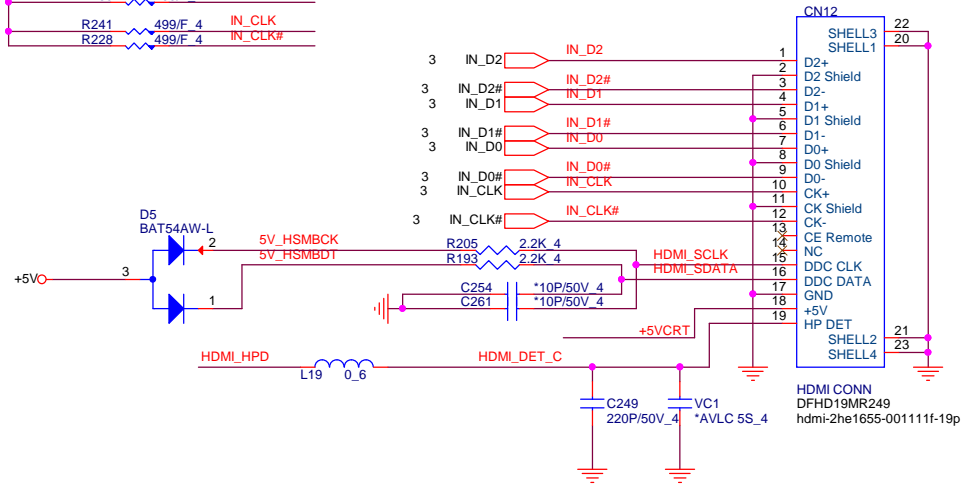
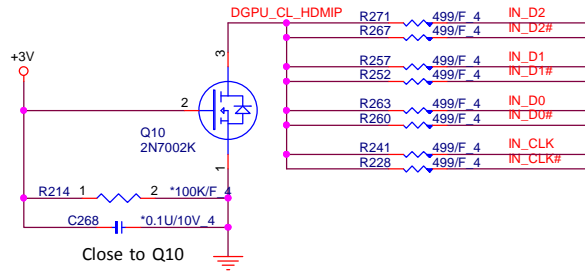
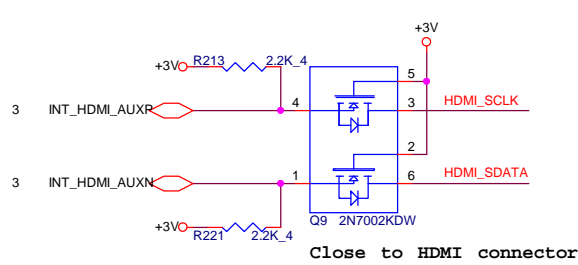
	PROJECT : Y2x Quanta Computer Inc.	
	Size Custom Document Number LVDS Converter RTD2136	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 20 of 41		

LVDS CONN.

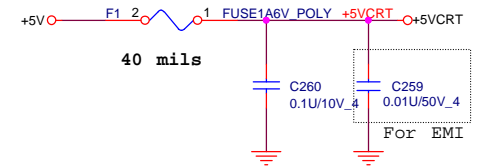
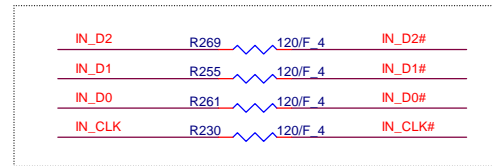
Note.
14" & 15" only eDP panel.
17" have both LVDS & eDP panel.



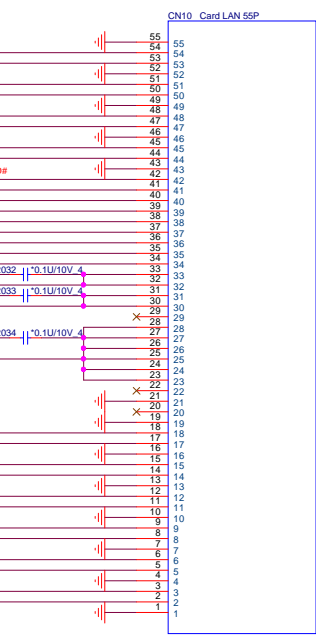
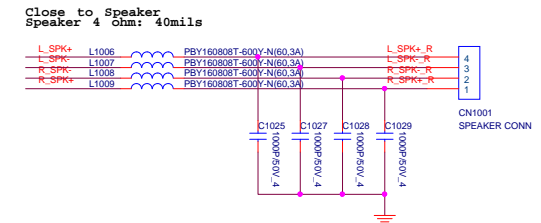
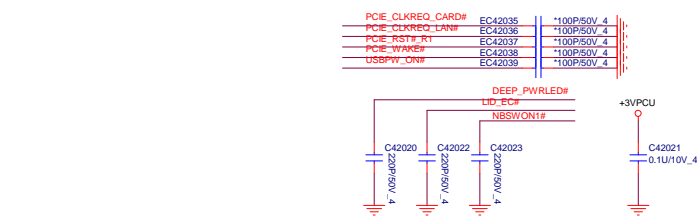
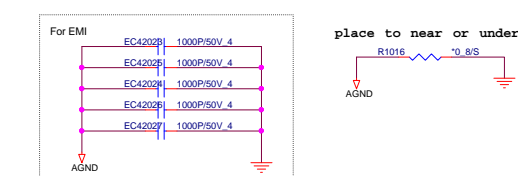
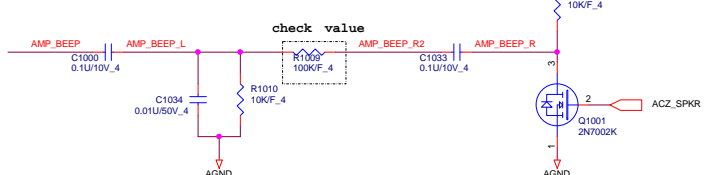
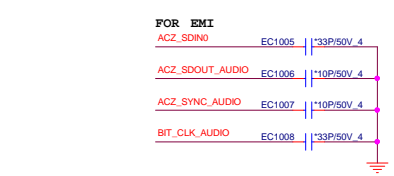
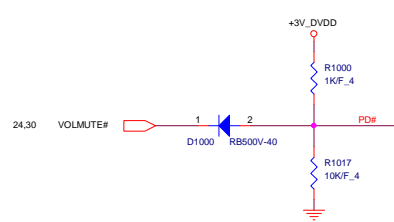
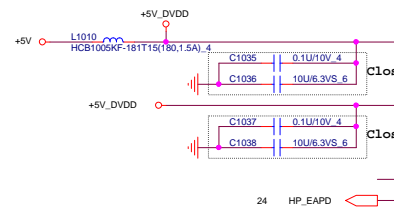
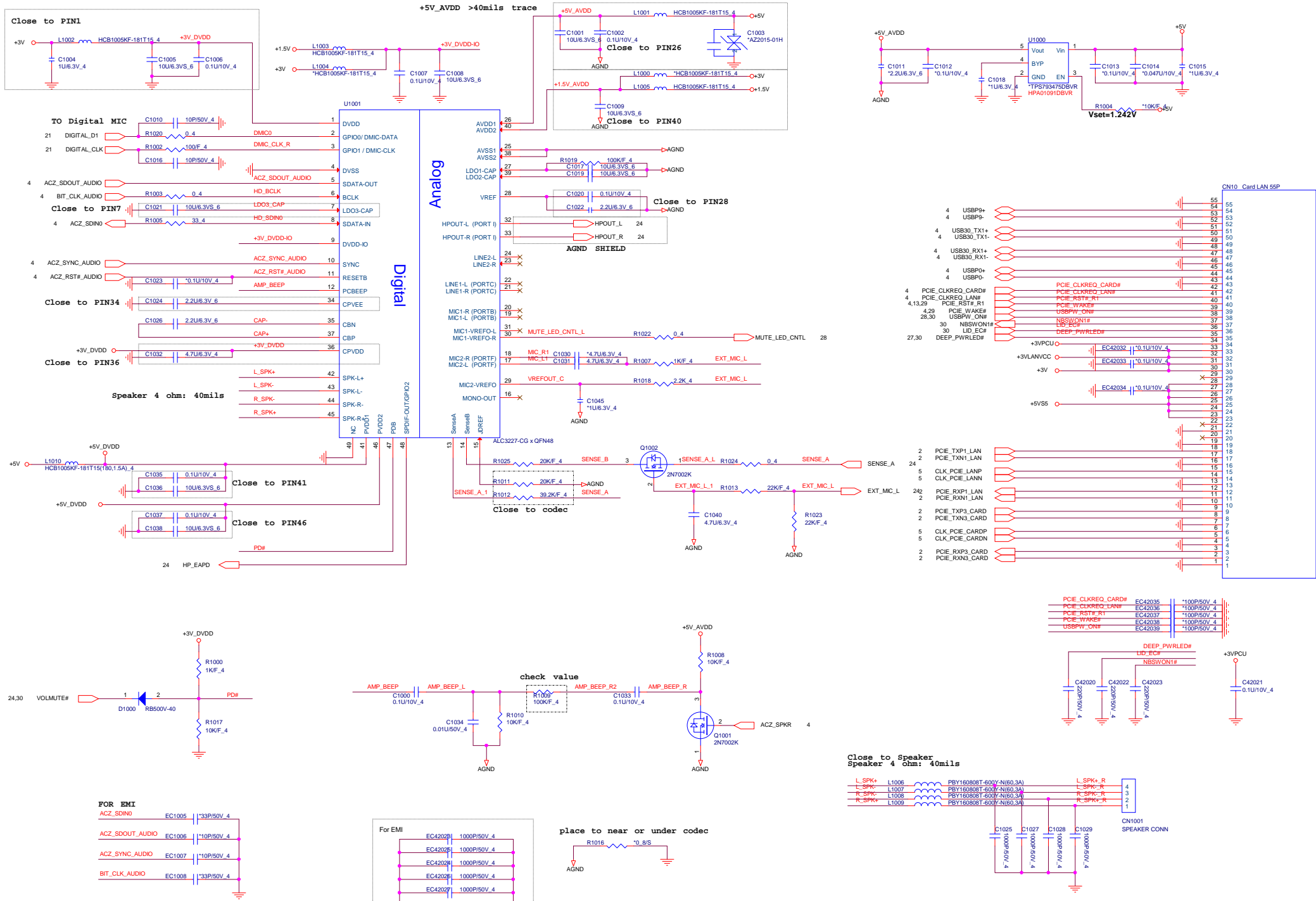
	PROJECT : Y2x		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	LCD CONN/Camera/D-MIC	
Date: Tuesday, November 18, 2014		Sheet 21	of 41

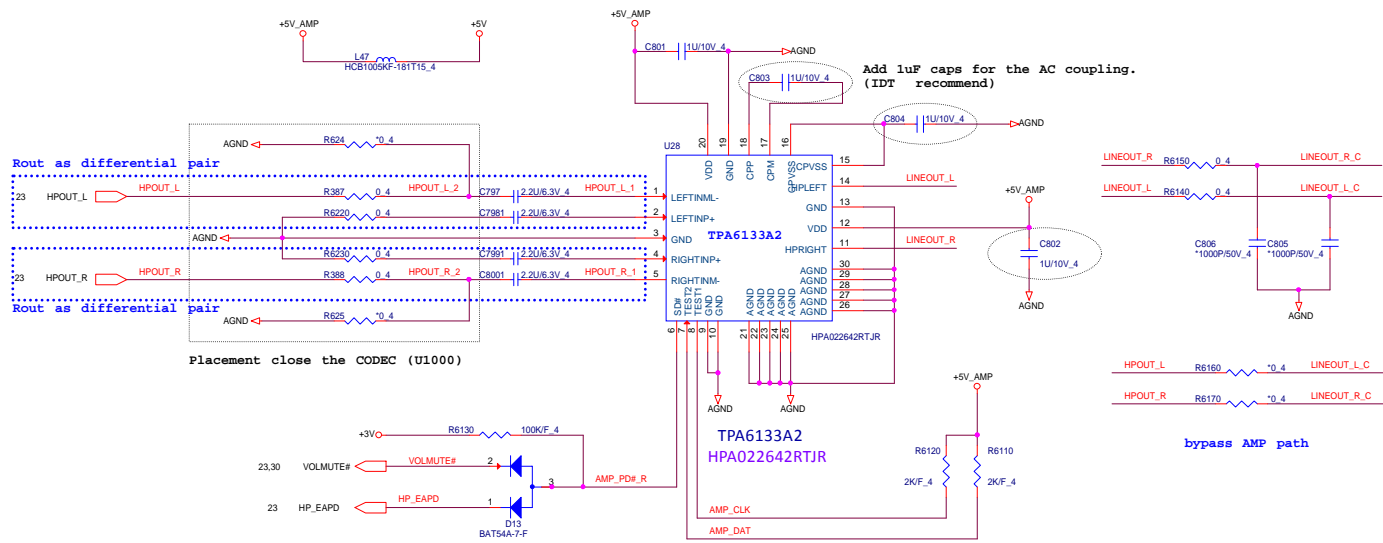


For EMI

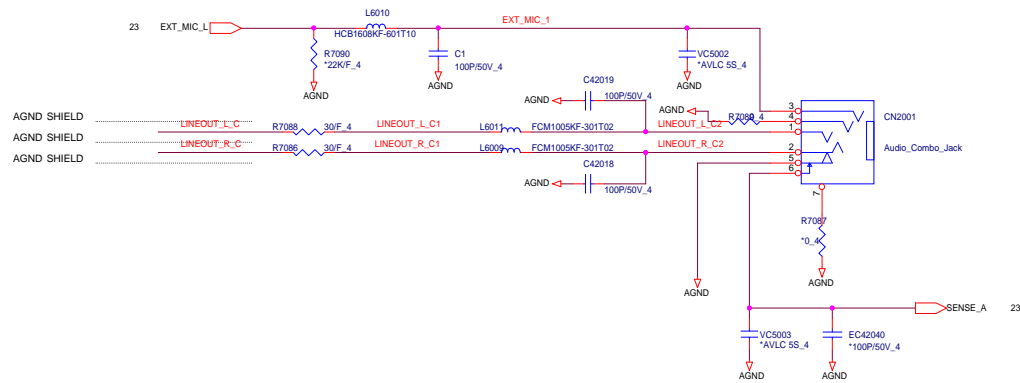


	PROJECT : Y2x Quanta Computer Inc.	
	Size B NB5/RD3	Document Number HDMI
Date: Tuesday, November 18, 2014 Sheet 22 of 41		

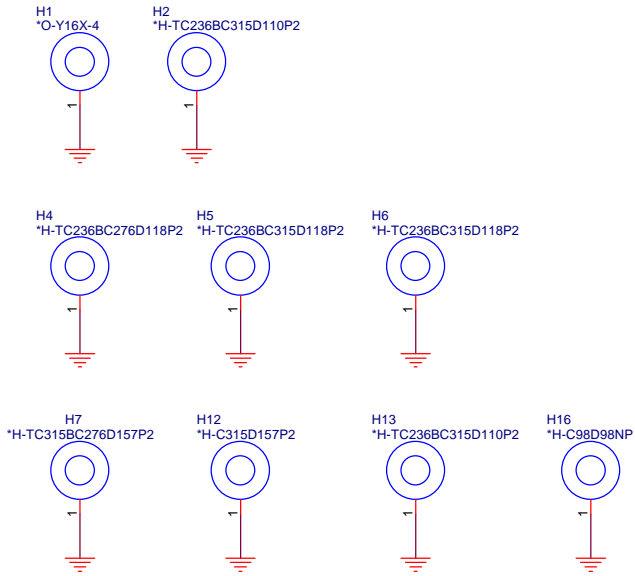




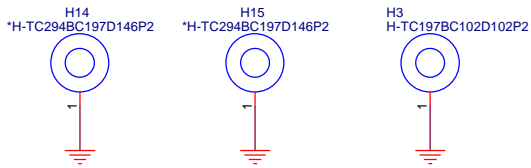
Audio Combo



Holes

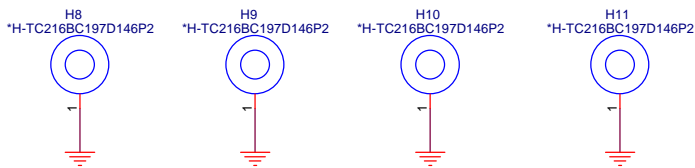


GPU HOLES

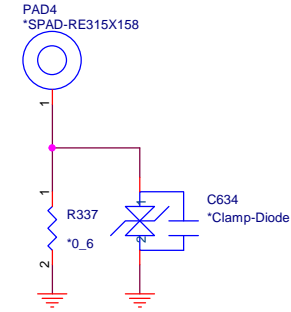


WLAN NUT

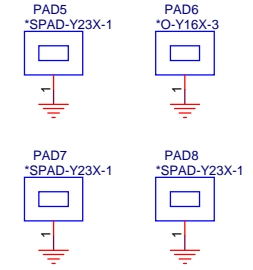
APU HOLES



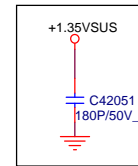
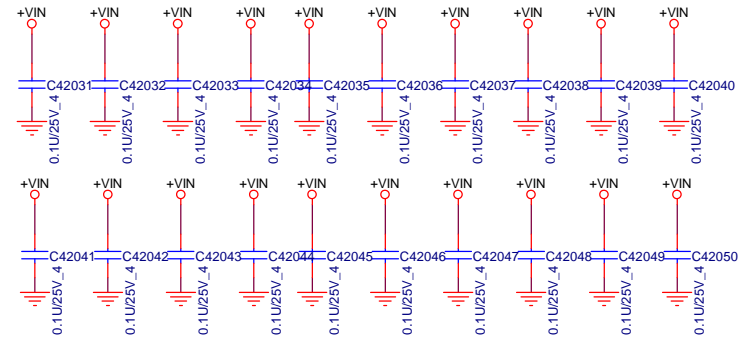
Metal ESD



EMI



Place on +VIN path



11/17 EMI request

		<p>PROJECT : Y2x Quanta Computer Inc.</p>	
<p>NB5/RD3</p>		<p>Date: Tuesday, November 18, 2014 Sheet 25 of 41</p>	

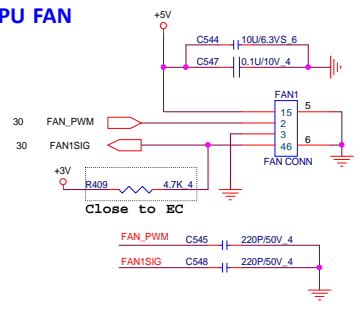


PROJECT : Y2x
Quanta Computer Inc.

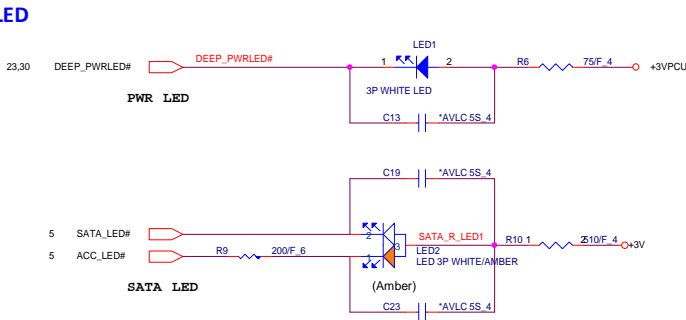
Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014		Sheet 26 of 41

Power Button on Connector (Molex or DB)

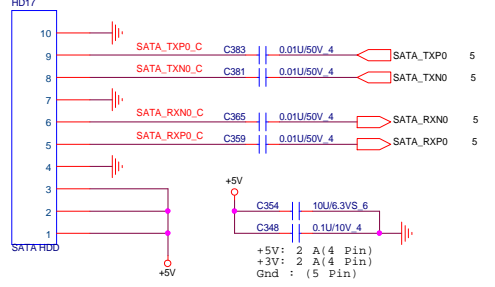
CPU FAN



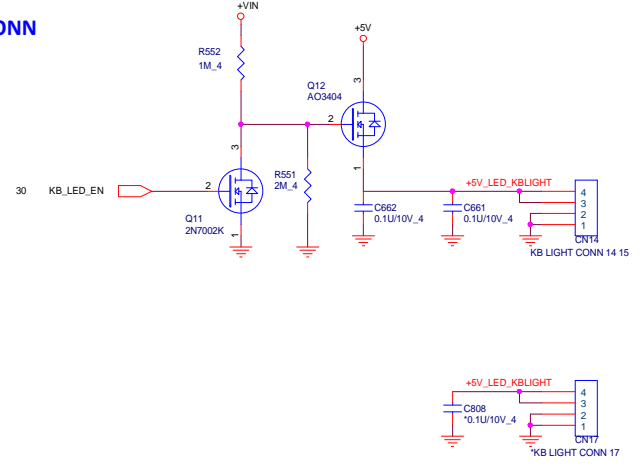
LED



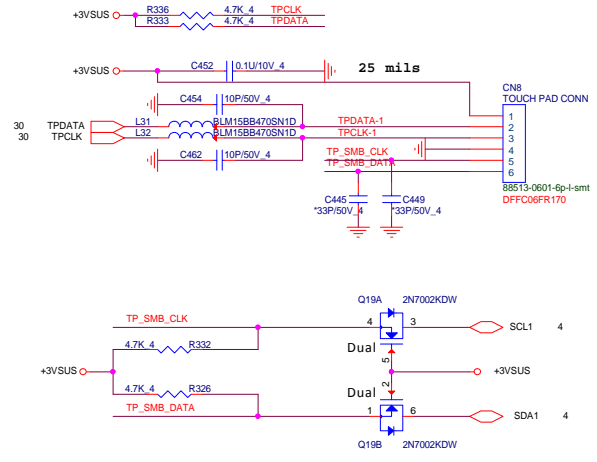
SATA HDD CONN (Cable type)



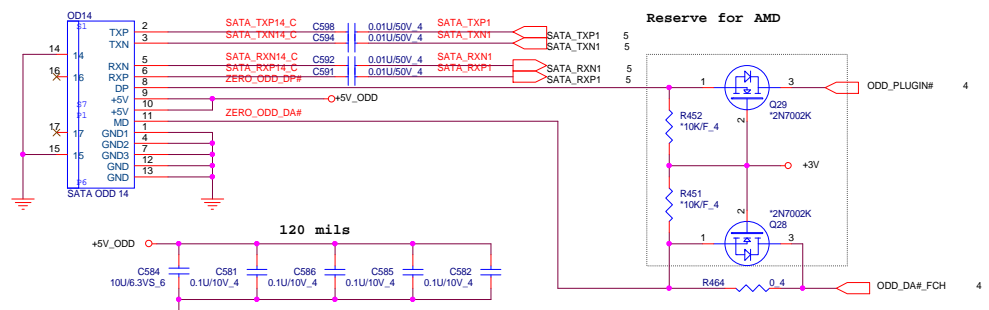
KB LIGHT CONN



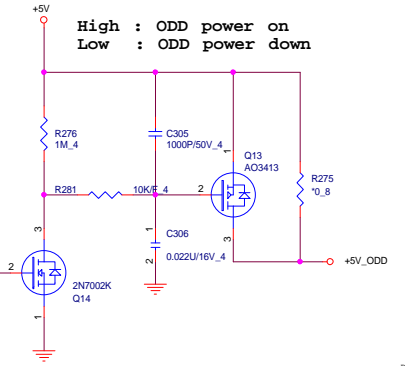
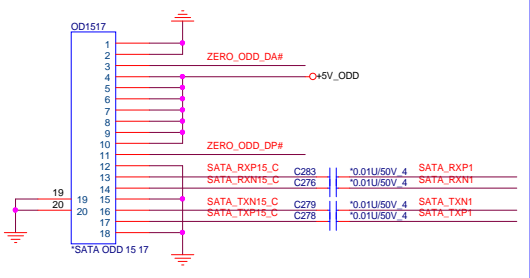
Touch Pad

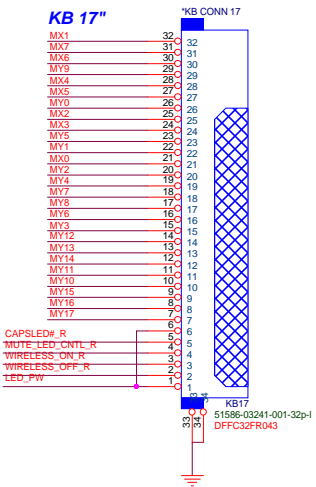
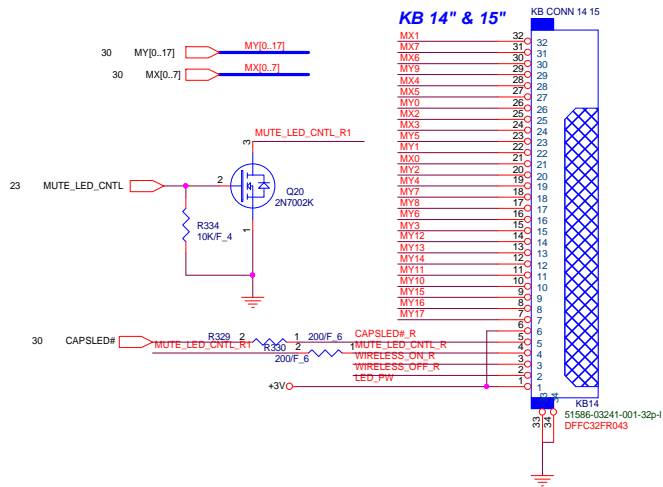


14" SATA ODD CONN

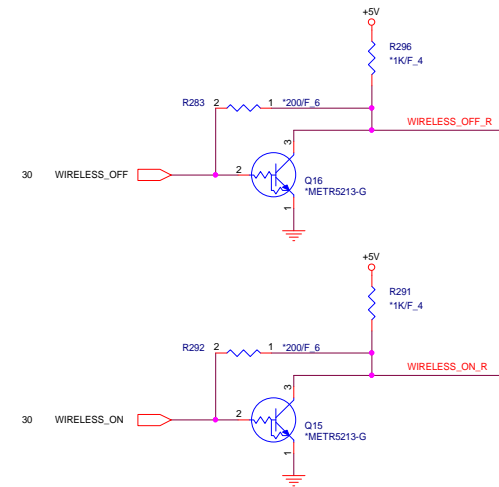
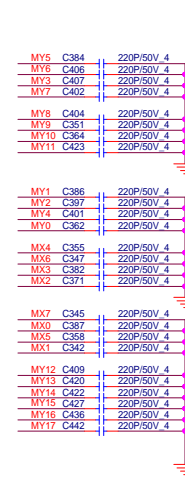
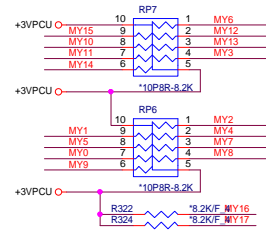


15" & 17" SATA ODD CONN

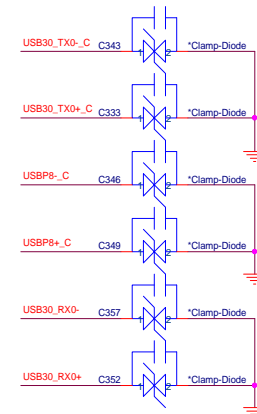
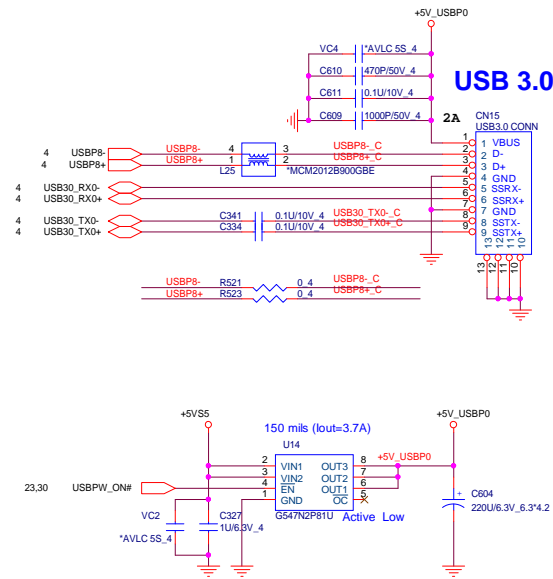




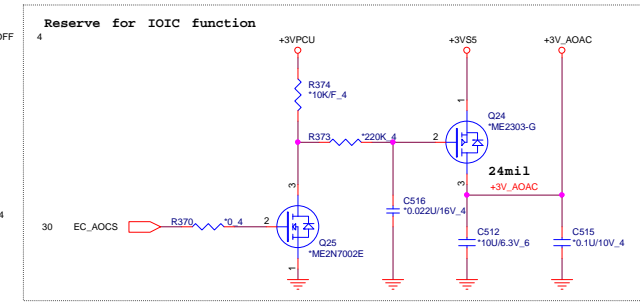
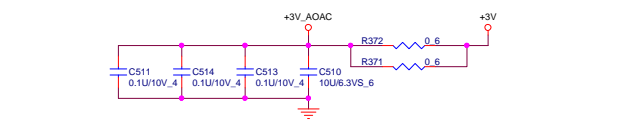
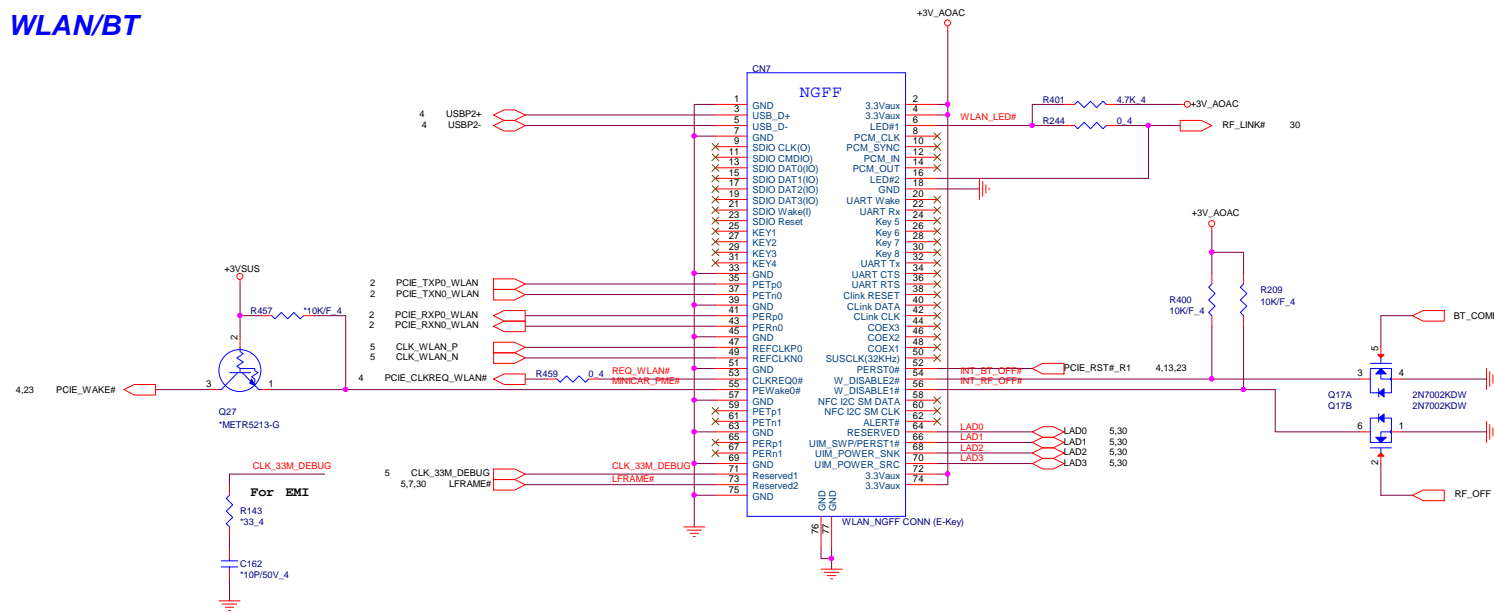
KEYBOARD PULL-UP



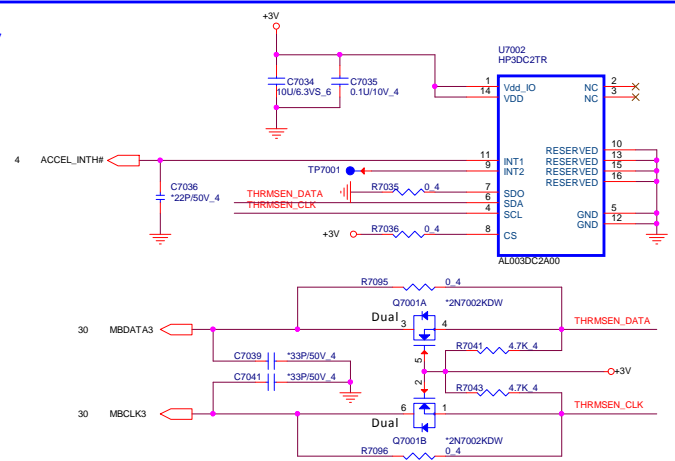
Left USB 2.0/3.0 Combo



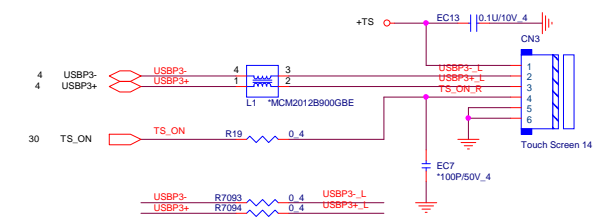
WLAN/BT



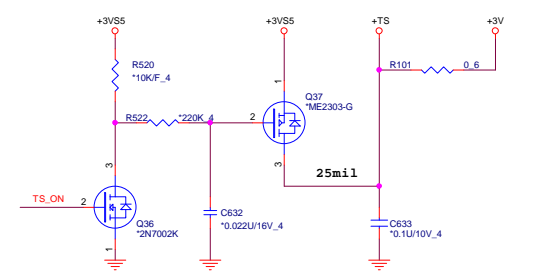
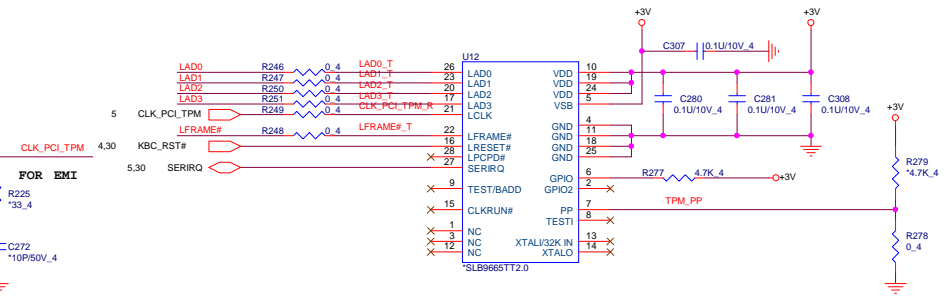
Accelerometer Sensor



Touch screen

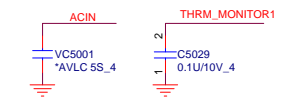


TPM (2.0)

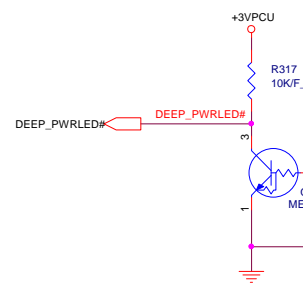
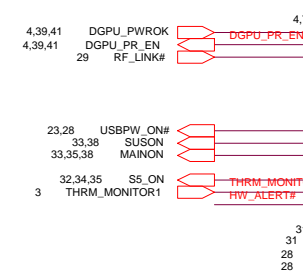


<p>NBS/RD3</p>	<p>PROJECT : Y2x Quanta Computer Inc.</p>	
	<p>Size Custom</p>	<p>Document Number WLAN/G Sensor/TPM/TS</p>
<p>Date: Tuesday, November 18, 2014</p>		<p>Sheet 29 of 41</p>

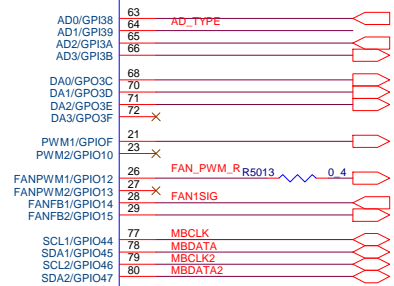
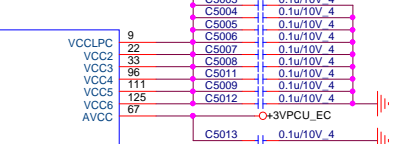
Because EC set to OD pin.
+3V
R5035 10K/F 4 EC_A2OGATE
R5036 10K/F 4 EC_RCIN#



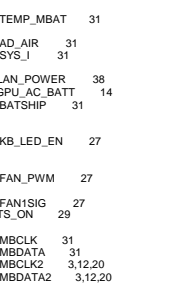
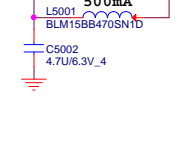
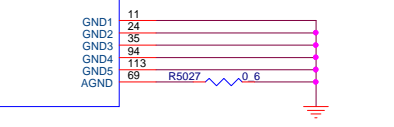
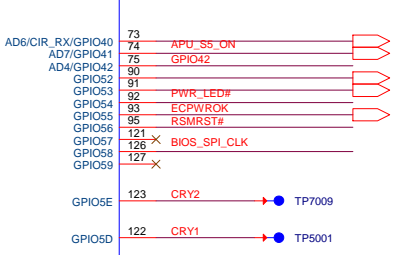
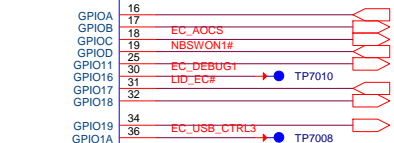
For GPU Thermal
For G-sensor
4.39.41 DGPU_PWROK
4.39.41 DGPU_PR_EN
29 RF_LINK#



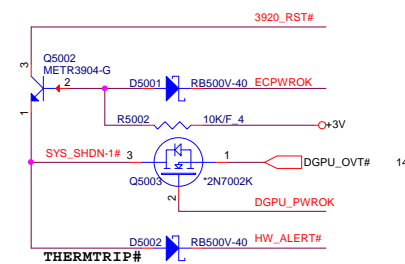
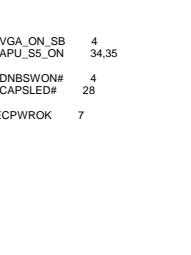
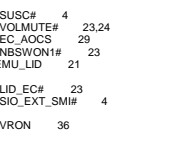
Pin header table for U5001. Columns include pin number, signal name, and component value. Signals include SERIRQ, LFRAME#, LAD0, LAD1, LAD2, LAD3, CLK_33M_KBC, KBC_RST#, CLKRUN#, SIO_EXT_SCH#, EC_A2OGATE, EC_RCIN#, EC_A2OGATE, EC_RCIN#, MX0-MX7, MY0-MY17, GPURT_CLK, GPURT_DATA, MBCLK3, MBDATA3, TPCLK, TPDATA, BIOS_RD#, BIOS_WR#, BIOS_CS#, BIOS_WP#, ACIN, R5021, R5022, TP7006, TP7007, TP7005, S5_ON, THRM_MONITOR1, HW_ALERT#, R5025, HW_ALERT#_R, 5VS5_ON, MBATTLEDON#, AC_LED_ON#, WIRELESS_ON#, WIRELESS_OFF#, +3VPCU, C5030, C5031, DEEP_PWROK, DEEP_PWROK#, PWR_LED#.



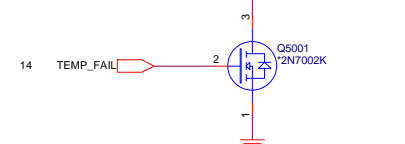
SCL1/SDA1: For Battery & Charger
SCL2/SDA2: For CPU/DDR thermal & *LVDS Converter



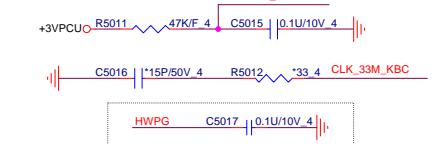
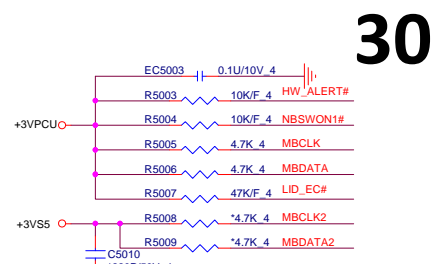
SCL1/SDA1: For Battery & Charger
SCL2/SDA2: For CPU/DDR thermal & *LVDS Converter



DGPU Thermal protect

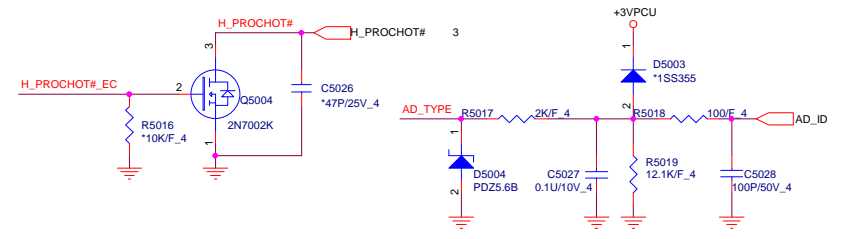


Reserve for ENE hold time issue
MBCLK2 C5019 *10P/50V 4
MBDATA2 C5020 *10P/50V 4
GPURT_CLK C5021 *10P/50V 4
GPURT_DATA C5022 *10P/50V 4
MBCLK C5023 *10P/50V 4
MBDATA C5024 *10P/50V 4

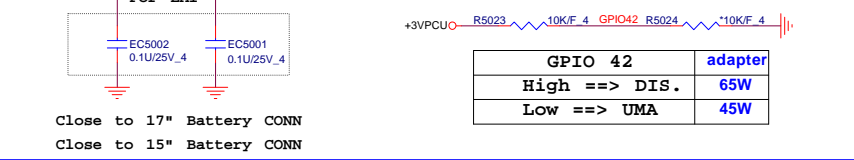


For +VIN noise
HWPG C5017 0.1u/10V 4
FAN1SIG C5018 0.1u/10V 4
DGPU_PR_EN C5001 0.1u/10V 4
SERIRQ C5025 100P/50V 4
APU_SS_ON R525 100K/F 4

Smart adapter Type check

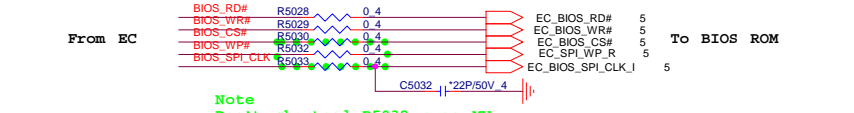


Adapter select



GPIO 42	adapter
High ==> DIS.	65W
Low ==> UMA	45W

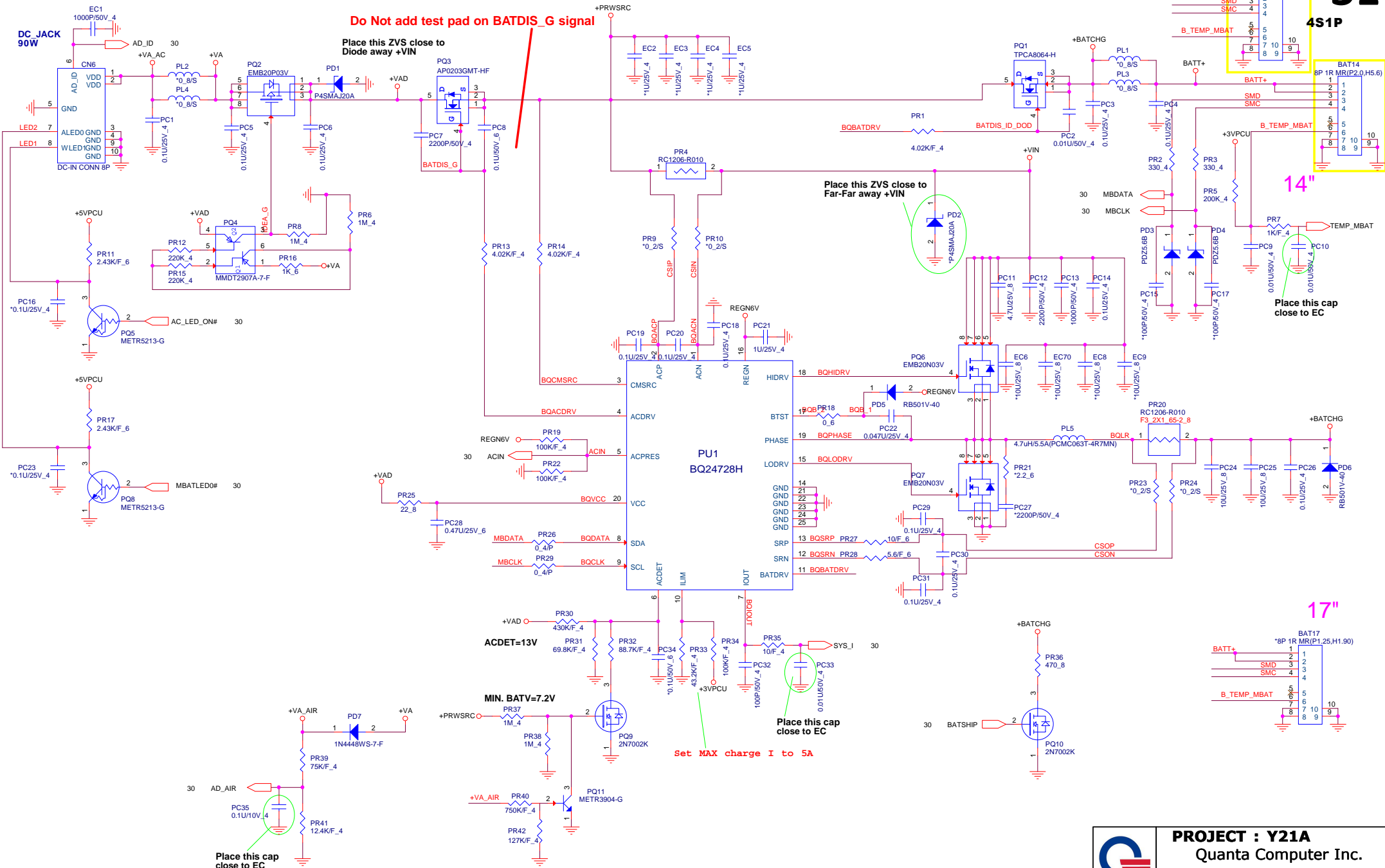
Close to 17" Battery CONN
Close to 15" Battery CONN




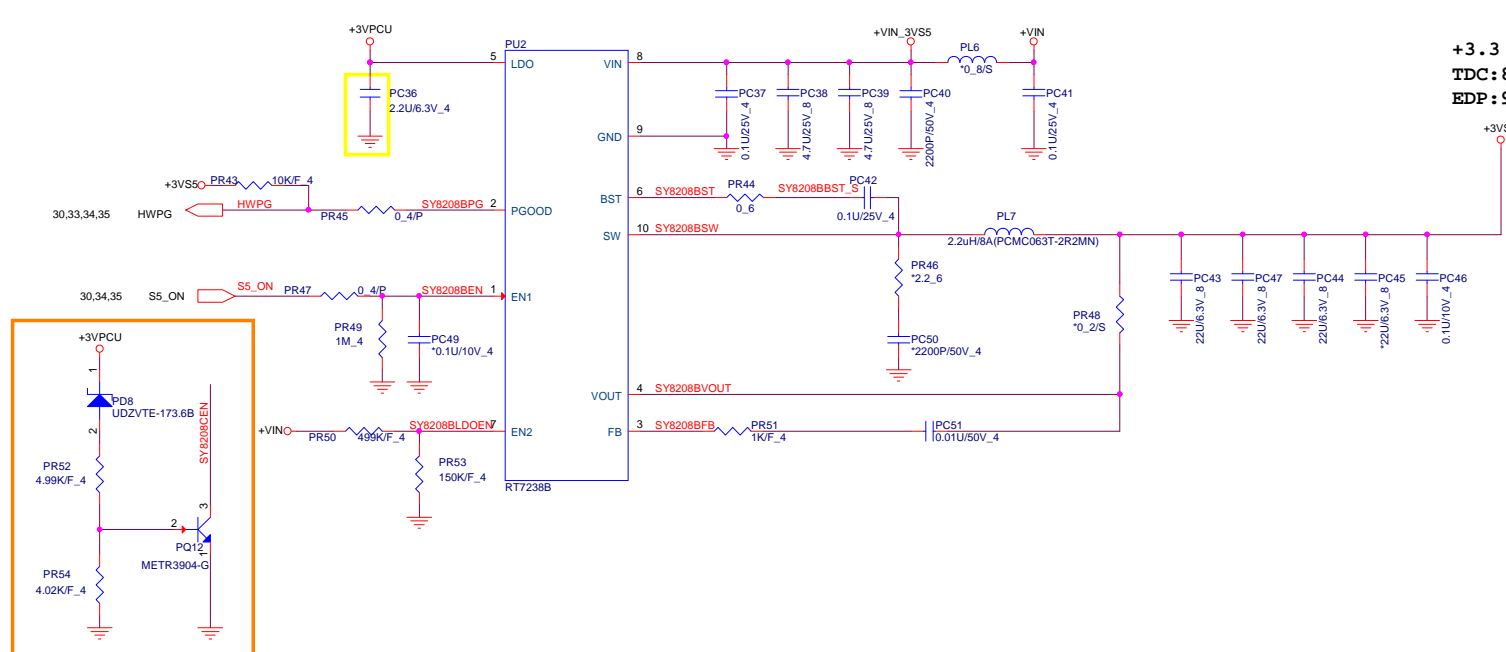
Note Don't shortpad R5032 even MV.

PROJECT : Y2x
Quanta Computer Inc.

Size Custom	Document Number EC KB9028QF	Rev 1A
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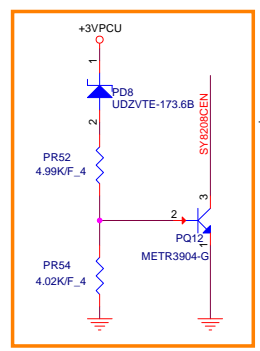


 PROJECT : Y21A Quanta Computer Inc.			Size	Document Number	Rev
			Custom	Charger (BQ24728H)	1A
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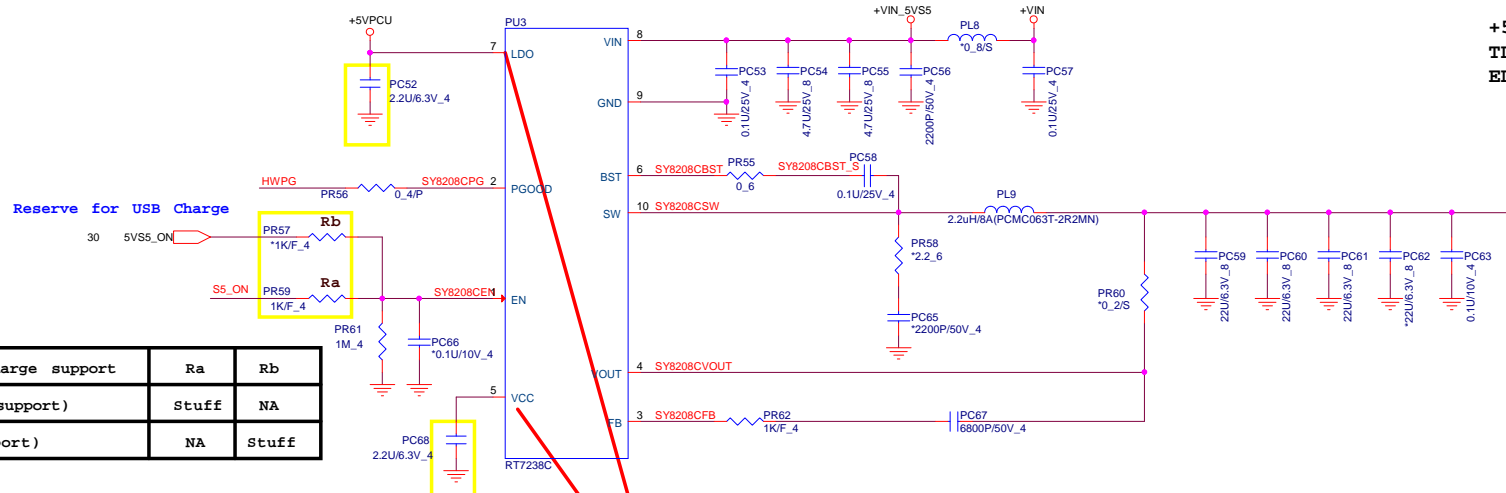


+3.3 Volt +/- 5%
TDC:8A
EDP:9A

+3VS5 4,5,6,7,29,30,34,38,39,41
 +5VS5 23,28,33,35,36,38,39,41



Reserve



+5 Volt +/- 5%
TDC:8A
EDP:9A

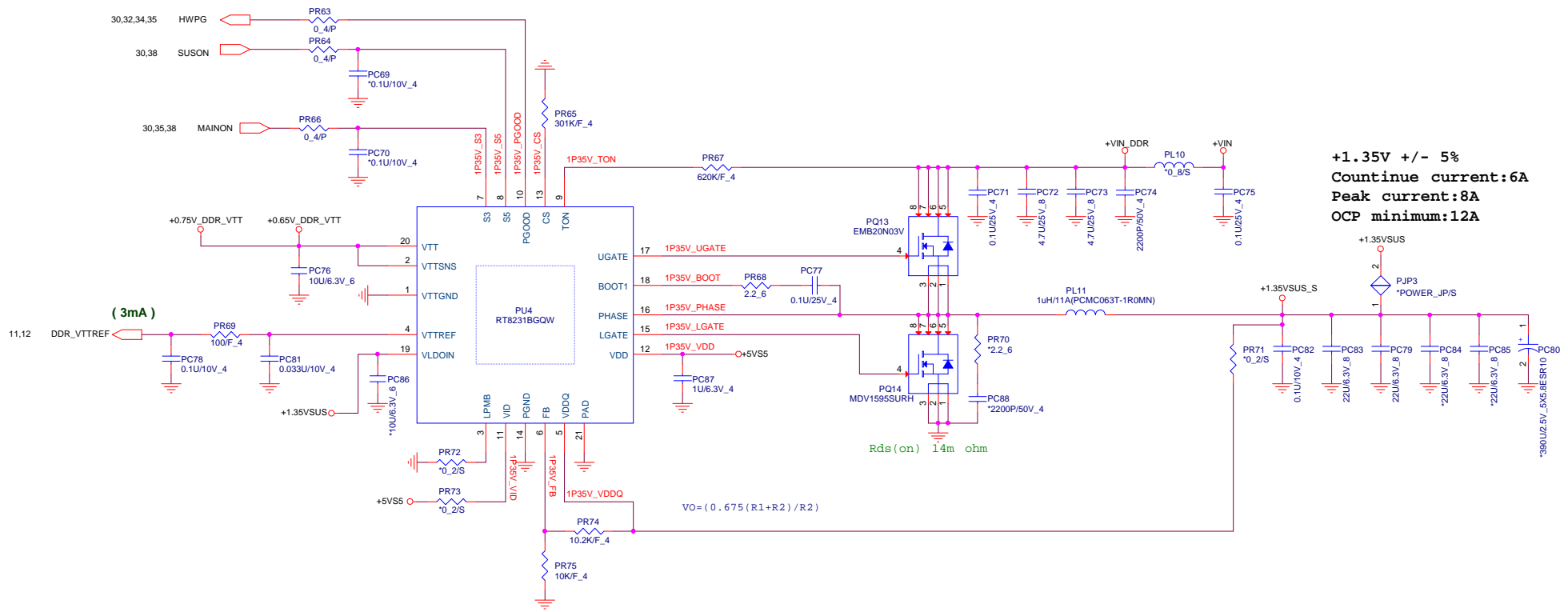
Reserve for USB Charge

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

PROJECT : Y21A
 Quanta Computer Inc.

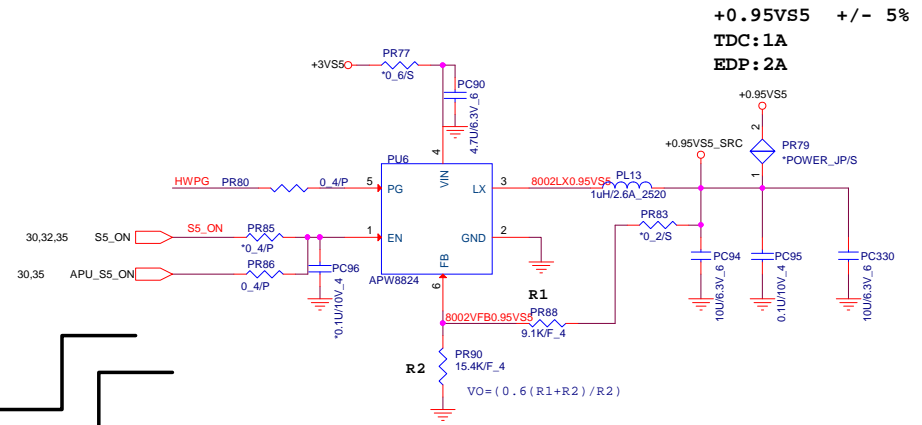
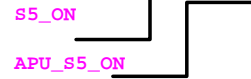
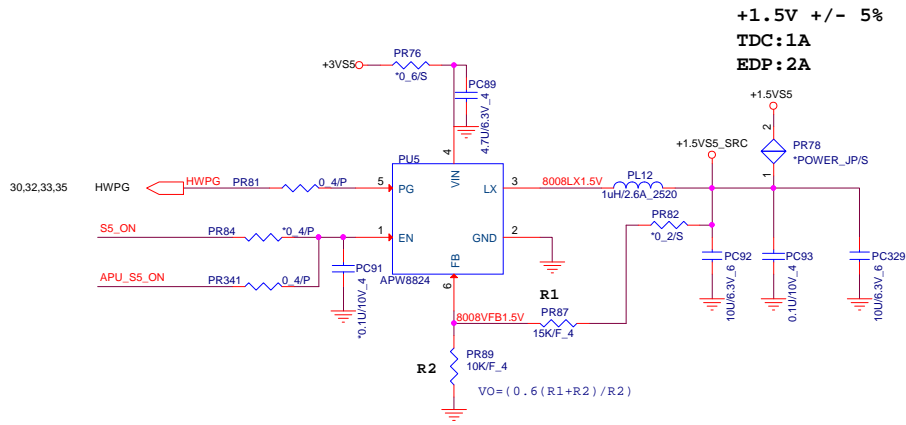
Size Custom	Document Number 3/5VPCU(SY8208B/SY8208C)	Rev 1A
Date: Tuesday, November 18, 2014	Sheet 32	of 41




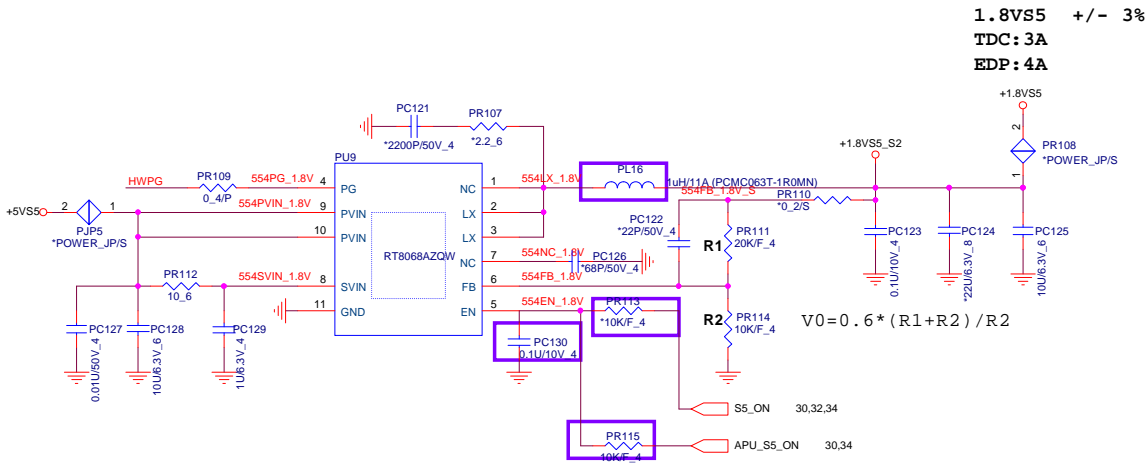
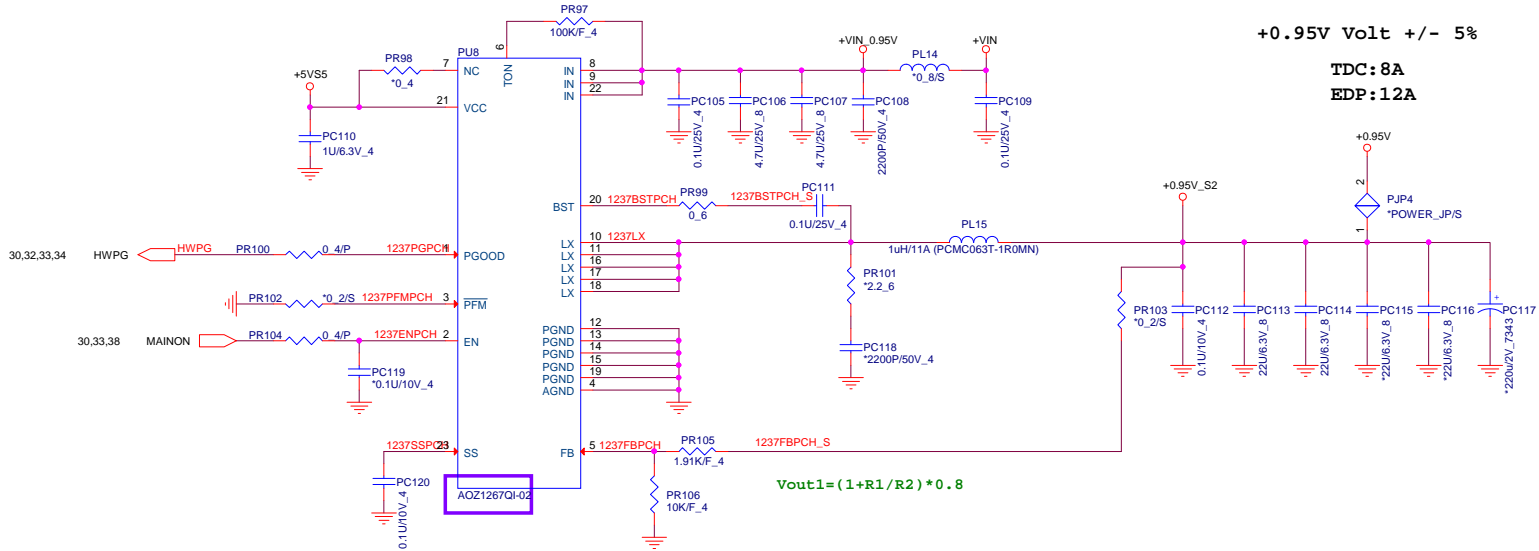
+1.35VSUS 2.6,11,12,25


PROJECT : Y12A-BTM
Quanta Computer Inc.

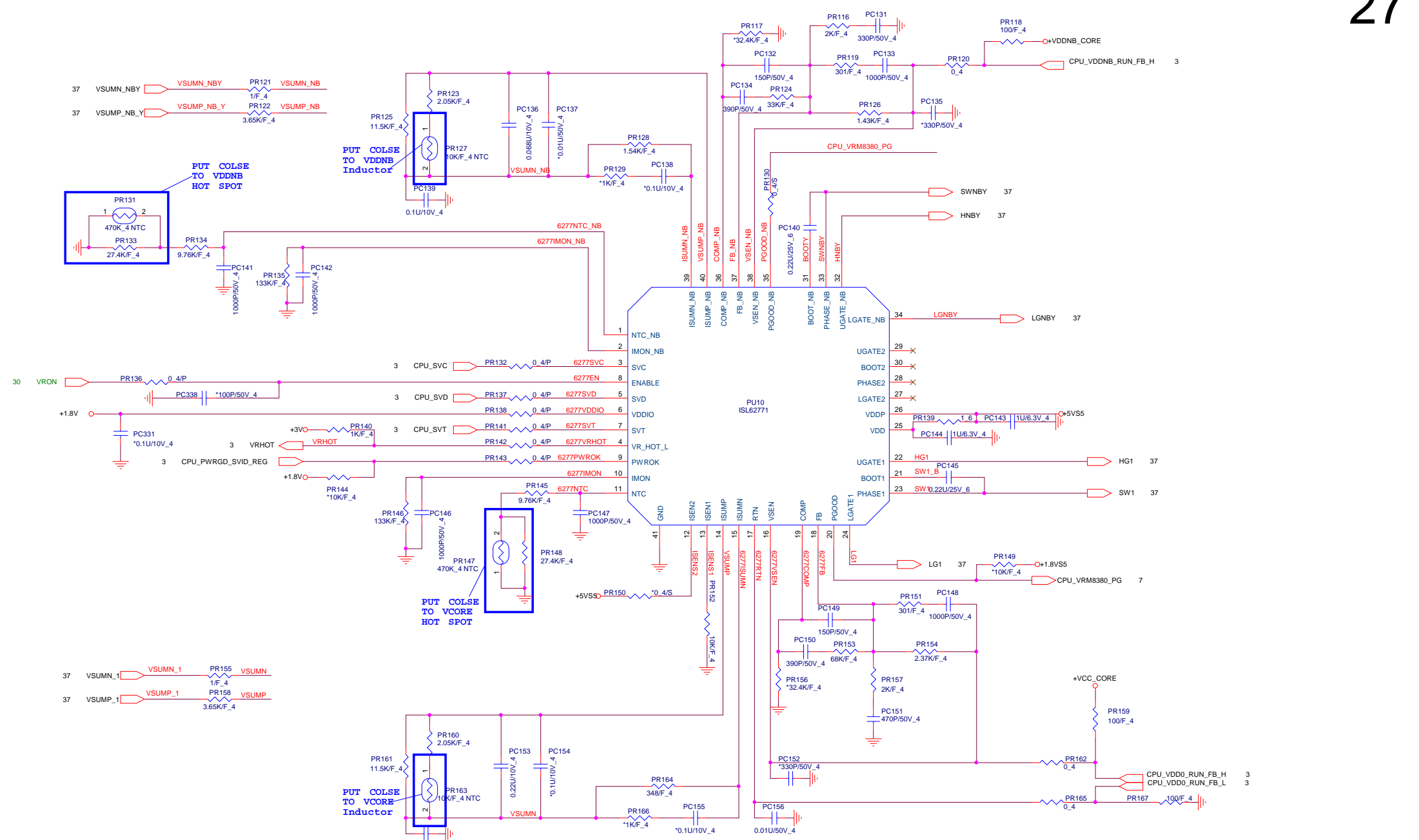
Document Number	DDR3 (RT8231B)1.8VS5	Rev	1A
Date:	Tuesday, November 18, 2014	Sheet	33 of 41




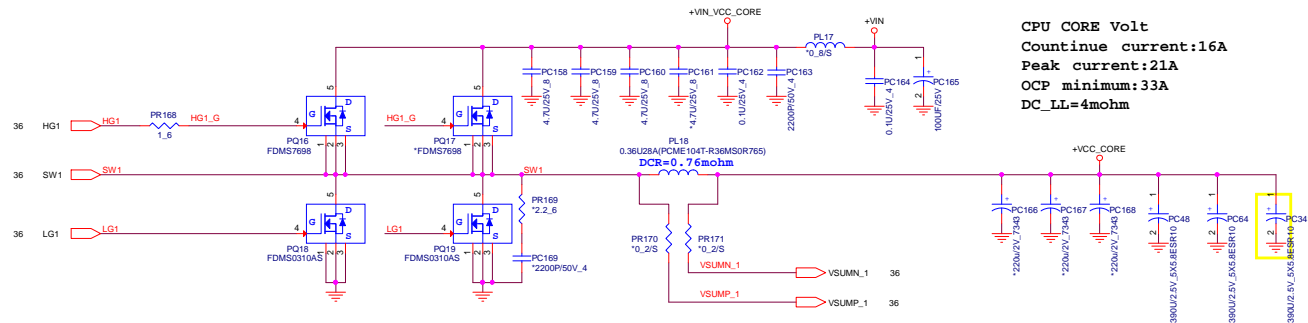
	PROJECT : Y21A		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number +1.1V55 (RT8228)/2.5V	
Date: Tuesday, November 18, 2014		Sheet 34 of 41	



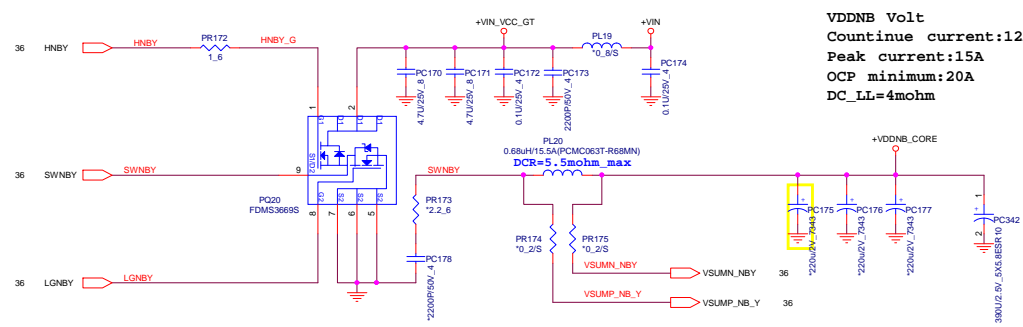
	PROJECT : Y21A		
	Quanta Computer Inc.		
	Size Custom	Document Number +1.1VS5 (RT8228)/2.5V	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 35 of 41			



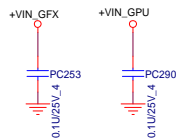
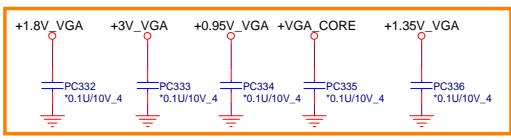
	PROJECT : Y02 Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	CPU Core1 (ISL62771)	1A
Date: Tuesday, November 18, 2014 Sheet 36 of 41			



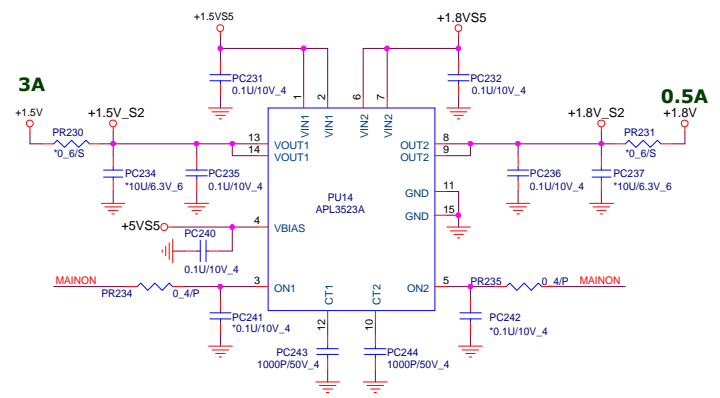
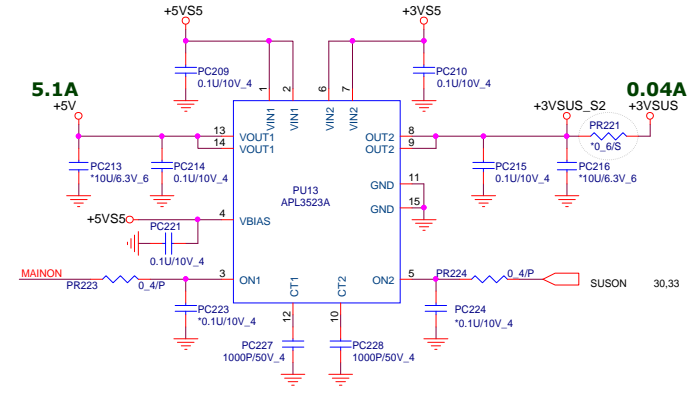
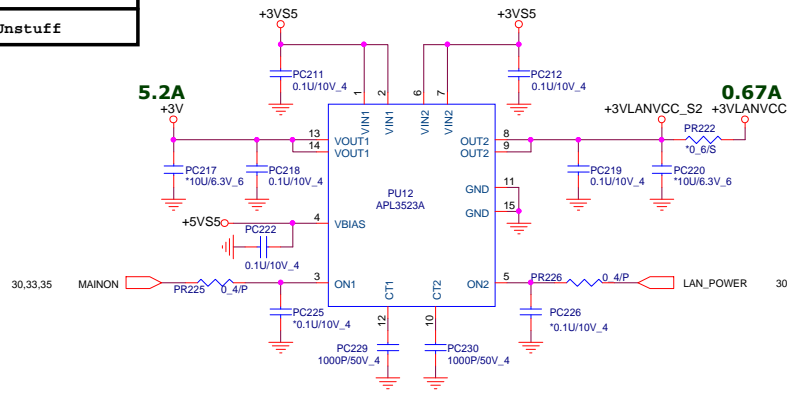
CPU CORE Volt
 Countinue current:16A
 Peak current:21A
 OCP minimum:33A
 DC_LL=4mohm



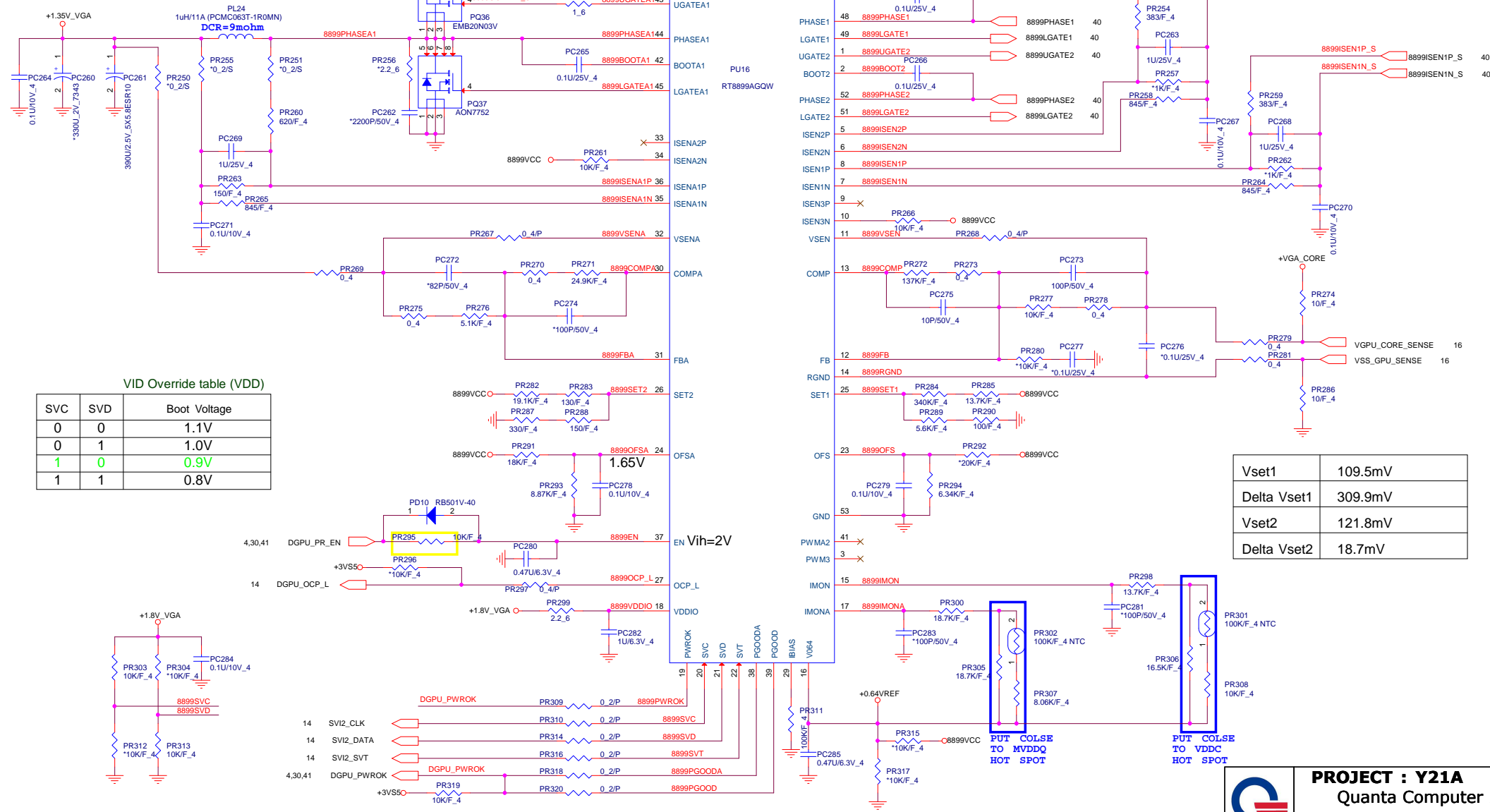
VDDNB Volt
 Countinue current:12A
 Peak current:15A
 OCP minimum:20A
 DC_LL=4mohm



UMA only	Stuff
discrete	Unstuff



+MVDDQ Volt +/- 5%
 Countinue current:6A
 OCP_TDC=12.6A
 OCP_SPIKE=18A(lms)
 Vboot=0.9V
 LL=0 V/A
 external offset=0.45V



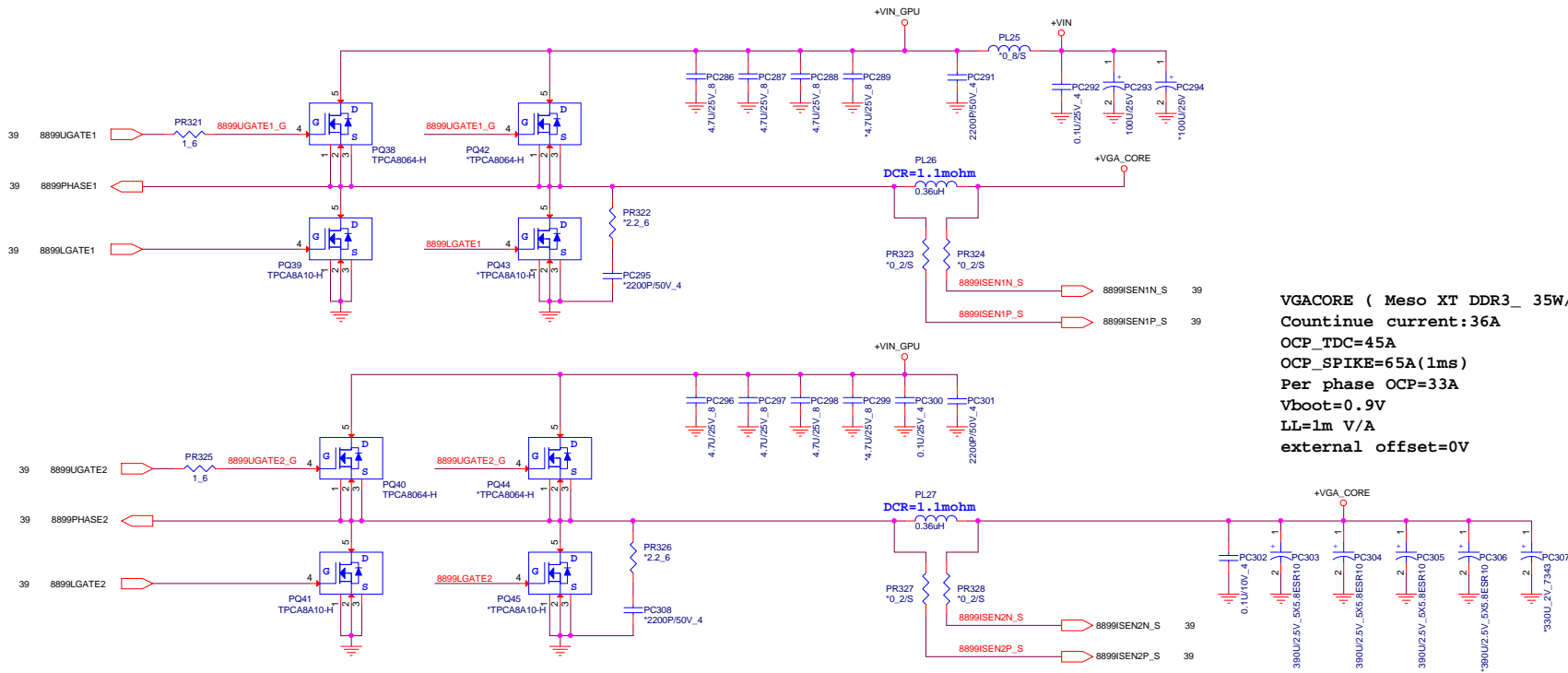
VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V


Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

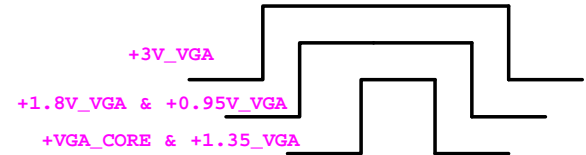
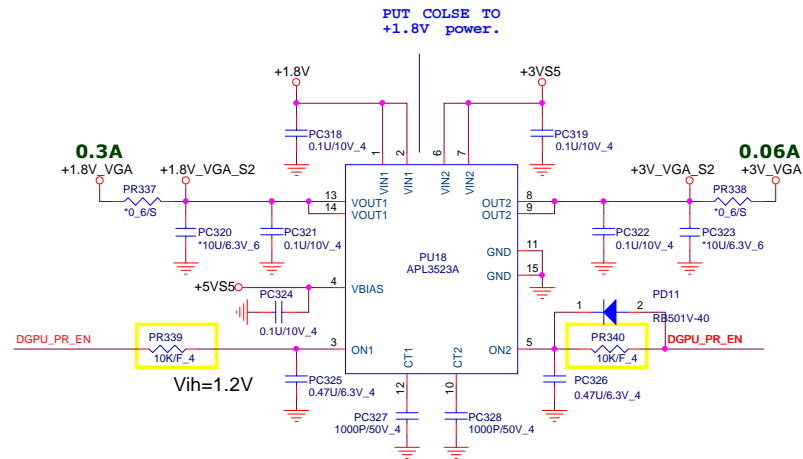
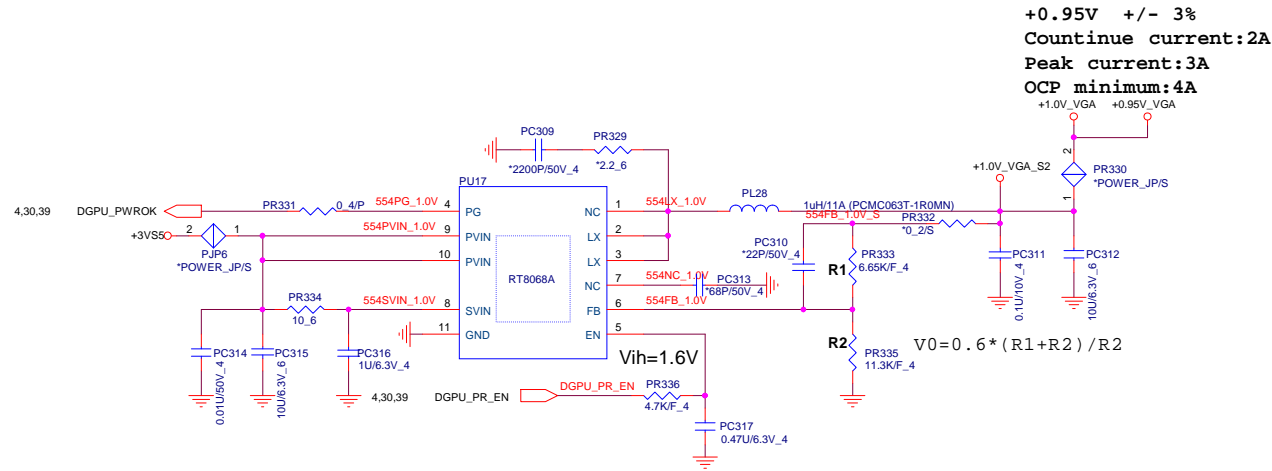
PROJECT : Y21A
Quanta Computer Inc.

Size Custom	Document Number Vcore(RT8899A)	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 39 of 41		



VGACORE (Meso XT DDR3_ 35W/53W(1ms))
Countinue current:36A
OCF_TDC=45A
OCF_SPIKE=65A(1ms)
Per phase OCF=33A
Vboot=0.9V
LL=1m V/A
external offset=0V

	PROJECT : Y21A		
	Quanta Computer Inc.		
Size Custom	Document Number CPU Core2	Rev 1A	
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- +3V_VGA 13,14,16,38
- +1.0V_VGA 13,16,38
- +1.8V_VGA 13,14,16,38,39

	PROJECT : Y21A	
	Quanta Computer Inc.	
Size Custom	Document Number +VGA POWER	Rev 1A
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